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John G. Kenney

Decision Feedback Equalization (DFE) in a data recovery channel filters the bit decision in the current symbol period in generating the sample at the comparator in the subsequent clock period. The operations of sampling, comparing, filtering the decision bits into a feedback signal, and subtraction of that feedback signal are cascaded, thereby establishing the critical timing path. Thus, this system, though simple, requires its components to have large bandwidths in order to achieve the high-speed response necessary to perform the described feedback function. For the entire system to run at speeds comparable to those of competing technologies (100MHz to 250MHz), the components must have bandwidths greater than 100MHz, and work together to provide a loop bandwidth of at least 100MHz.

A 300MHz latching comparator and a 125MHz 6-bit current-DAC were designed in a 5V, 1um CMOS n-well process for use in a DFE loop. Both blocks

are fully differential and achieve an accuracy of ½ LSB (10uA) over a differential signal range of 1.28mA. This is true for their operations at speed, in isolated simulation and as contiguous blocks. The DAC power consumption is relatively high at 23mW, due to internal switching circuits which require a static current, but the comparator's power consumption is minimal at 5mW.

A DAC and Comparator for a 100MHz Decision Feedback Equalization Loop

by

Linda M. Engelbrecht

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Linda M. Engelbrecht, Author

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DEDICATION

My gratitude to Professor John Kenney for the practical experience this project has provided me, and for his direction and patience in working with me. I am also extremely grateful to my husband, Dennis, and all my children, for their domestic assistance and loving kindness during this project. Finally, thanks to Sam Mahjouri, Rich Lewison, and Brett Forejt for all their help at work which has allowed me to finish preparing this thesis.

A DAC AND COMPARATOR FOR A 100MHZ DECISION FEEDBACK EQUALIZATION LOOP

1. MOTIVATION FOR A DECISION FEEDBACK SYSTEM

1.1 INTRODUCTION

The challenge in contemporary magnetic recording channels is the equalization of the time-domain response of the channel so that each magnetic flux transition may be accurately detected. With data storage requirements of high bit densities and fast data rates, accurate data detection becomes increasingly difficult. As the channel's bit responses are sampled closer in time there is a tendency for adjacent bits to time-shift and attenuate the peaks of each others' response. This phenomenom is called Intersymbol Interference (ISI), and there are several general system types that have been developed to solve the issue of ISI and provide improved data detection. Among these methods are Decision Feedback Equalization (DFE) and Partial Response Maximum Likelihood (PRML) detection.

1.1.1 DFE System Description

To briefly describe a DFE system, it requires first a continuous-time filter in the forward signal path which is responsible for the phase equalization of the analog input (the read channel's time-domain response). The filter is targeted to equalize a dibit. The read head's dibit response is shown in Figure 1.1 and is

the linear summation of the read head's response to two successive step changes in magnetic flux, the steps being opposite one another in polarity. The filter's response to the dibit generated from the read head is shown in Figure 1.2. The filter increases the slope of the bits' leading edges by delaying low frequency energy in the impulse response relative to the high frequency energy. Figure 1.2 shows the filter's response, 1+f(z), which shapes the analog signal such that its information is concentrated at its leading edge, leaving a gradually-diminishing tail following its peak. It is this "tail" or the filter's impulse response, f(z), which begins at sample n=1, that the decision feedback loop must cancel.

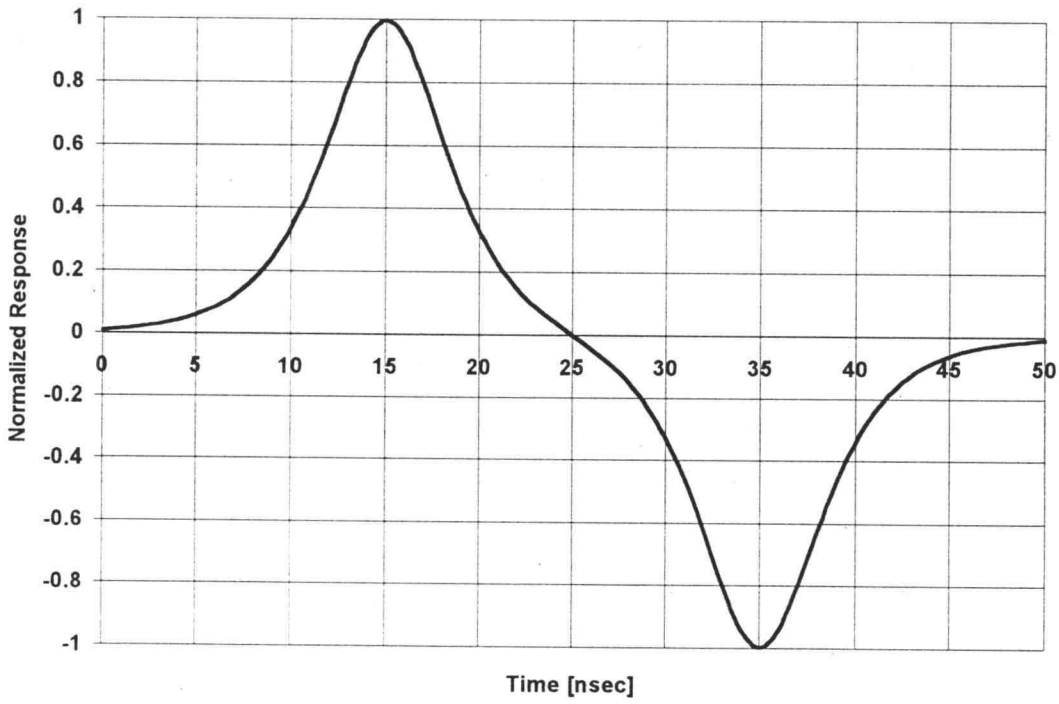


Figure 1.1: Read head's dibit response

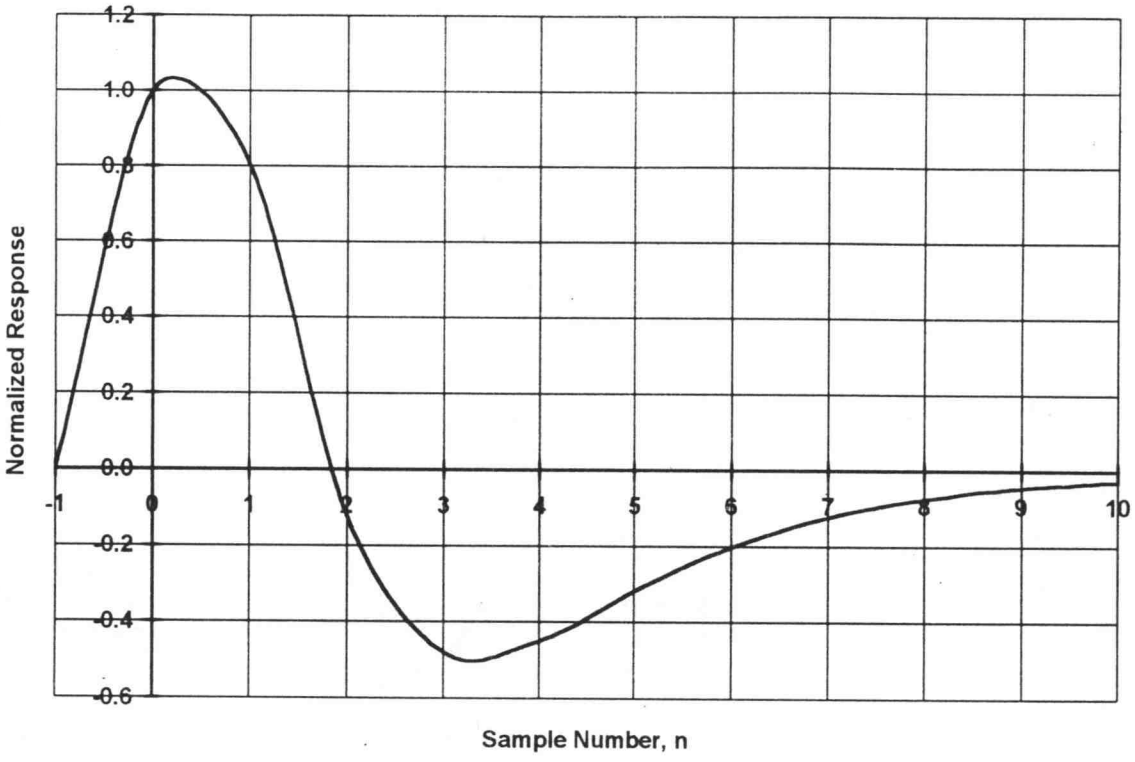


Figure 1.2: Dibit response of the forward signal path continuous-time filter in DFE

A simple decision feedback system is illustrated in Figure 1.3 to assist in explaining the feedback loop's function. All the signals shown are differential.

The system considered in this report uses current to implement its feedback signal, as this simplifies the summing of the forward and feedback signals. $\mathbf{a_k}$ is an analog bit stream, $\mathbf{i_{ff}}$ is the feed-forward current output from the filter's transconductor, $\mathbf{i_{fb}}$ is the feedback current from the 6-bit current-mode DAC, and $\mathbf{v_k}$ is the equalized signal that results from the sum of $\mathbf{i_{ff}}$ and $\mathbf{i_{fb}}$. $\mathbf{a'_k}$ is the output of the comparator and for two-level decision feedback equalization, it

is either a +1 or a -1. Finally, **sp[0:5]** is the DAC control word generated by the digital feedback filter.

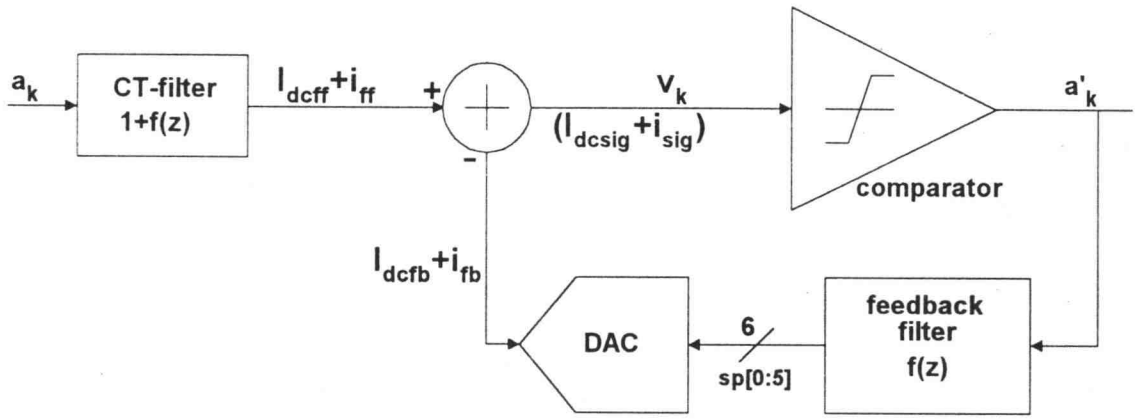


Figure 1.3: Basic decision feedback equalization loop

The sequence of differential sums, $\mathbf{v_k}$s, will always be close to either +1 or -1, thus representing the input sequence of $\mathbf{a_k}$ bits. The comparator digitizes the $\mathbf{v_k}$ sequence to generate the recovered data stream. The feedback filter uses this data stream to compute and output control words to the DAC which cancel the energy of the tail over the next 10 cycles.

This method requires that the continuous-time filter in the forward signal path and the feedback filter be designed with the same impulse response, so that f(z), (the "tails"), will be cancelled over successive clock cycles to eliminate intersymbol interference.

1.1.2 DFE Comparison to a PRML System

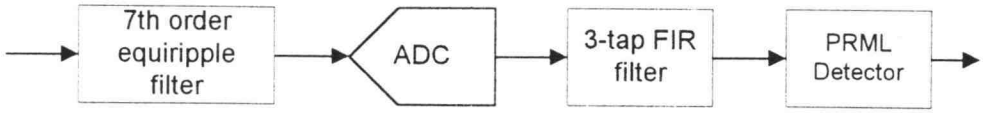


Figure 1.4: Simplified PRML system

For comparison, a simplified PRML system representative of the system in [1] is presented in Figure 1.4. In PRML, the read channel's response must also be filtered to conform to a specific spectral target that will enable the system to detect data transitions or peaks.

As shown, the system uses a programmable, seventh-order filter with two programmable zeroes in the forward signal path, an ADC (typically 5 or 6 bits), a three-tap adaptive equalizer, and a Viterbi or PRML detector, for the detection of signal peaks in $\mathbf{a_k}$.

The seventh-order continuous-time filter of Figure 1.4 is very complex compared to the continuous-time filter of the DFE system (which would generally be a second-order all-pass filter using two poles and two zeroes). In addition, to enable the datapath to run at 100mhz, the data stream to the equalizer (FIR filter) and the Viterbi must be interleaved by sampling track and hold circuits. The ADC and Viterbi-detector blocks usually consume significant amounts of power and area, and along with the adaptive equalizer are also complex in

design. All of these blocks are unneccessary in a DFE system. In general, the method of ISI cancellation in a DFE system allows it to be inherently less complex, thus consuming less power and area, as compared to a PRML channel.

Current PRML channels being developed like the one referenced in [1], operate at sample rates anywhere between 100-200MHz. The DFE system components considered in this report are targeted for system operation at 100MHz. The difficult issue in the DFE system of Figure 1.3 is the critical timing path around the loop to the summing node. As DFE does not have the ability to store past information with which to make its decision about a signal peak, it is vital that the sampling (by the comparator) and its resultant output from the DAC as i_{fb} be available at the summing node within one clock period. This means that the DAC, analog summing node, and the Comparator must be able to operate individually at speeds, that when combined in sequence, yield a settled signal at the summing node within 10ns.

1.2 DFE BLOCK DESCRIPTIONS

For this investigation, three of the five blocks shown in Figure 1.3 are designed: the analog summation, the DAC, and the comparator. The summing node is actually included as part of the DAC block. The DAC is implemented using n-FET current-sinks and the summing node for i_{ff} and i_{fb} was designed into the DAC block in order to reduce routing between the forward and feedback

paths. Within the DAC, the current sum is mirrored and output from the block via a high-impedance cascode pair. This signal undergoes a current-to-voltage conversion prior to being input to the comparator as v_k. The comparator is a regenerative-latch with an n-FET differential input pair and a p-FET regeneration source. The DAC design is discussed in detail in section 2.1, the comparator in section 2.2, and their interface in section 2.3.

1.3 SYSTEM SPECIFICATION

1.3.1 DC Bias Currents in Forward and Feedback Paths

The loop is designed for a maximum forward signal current of $1240\,\mu A$ peak differential with a common-mode or DC bias current of $870\,\mu A$. This is the differential current that would be output by the forward filter. The forward current is presented to the summing node where the feedback loop subtracts out the unwanted portion of the signal current via the DAC. The signal current that results from this subtraction is mirrored and becomes the input to the comparator which makes a decision about the polarity of the differential signal. The comparator needs only to distinguish the sign of the differential signal current, $i_{sigp} - i_{sign}$, when the difference is as small as 1/2 lsb ($10\,\mu A$). In order to ensure proper interfacing among the blocks, the signals and their common-mode or DC bias currents are as follows:

$I_{dcff} = 870\,\mu A$

$I_{dcfb} = 320\,\mu A$

$I_{dcsig} = 550\,\mu A$

and $I_{dcff} - I_{dcfb} = I_{dcsig}$. **(1.1)**

There were two design points to consider in choosing these DC bias currents. I_{dcfb} is the common mode bias of the 6-bit DAC and was set to $320\,\mu A$ when the DAC unit current was chosen to be $10\,\mu A$ as a reasonable current per unit branch to limit the power consumption of the DAC core. With a code of 0 as its control word, the current output of the DAC is differentially balanced and both positive and negative outputs of the DAC are sinking $320\,\mu A$ (refer to Table 2.1).

It was expected that the maximum differential signal current from the forward path, $i_{ff} = i_{ffp} - i_{ffn}$, would be about twice what the DAC could sink. A decision threshold value of about 2/3 of that maximum signal current (2/3 x $620\,\mu A$ single-ended [se]), was chosen to put upper and lower bounds on the comparator inputs. This lead to choosing $I_{dcsig} = 550\,\mu A$. This allows biasing of the mirror FETs around a signal swing of $\pm 400\,\mu A$ on the single-ended DAC output currents, i_{sigp} and i_{sign}. Having established I_{dcfb} and I_{dcsig}, I_{dcff} followed from the equality of equation (1.1) above.

1.3.2 Signal Currents

The maximum signal current levels in both the forward and feedback paths are given in Table 1.1. All the signals in this table have been defined above with the exception of the single-ended DAC sink currents, i_{dacp} and i_{dacn}. Thus, the resultant differential signal current at the output of the DAC is described as $i_{sig} = (i_{ffp} - i_{dacp}) - (i_{ffn} - i_{dacn})$, and does not exceed a value of $\pm 800\,\mu A$.

Table 1.1: Maximum Signal Currents

i_{ffp}, i_{ffn}	+620 μA peak single-ended (pk se) + 870 μA common-mode (cm) = 1490 μA max. -620 μA peak se + 870 μA cm = 250 μA min.
i_{ffp}-i_{ffn}	1240 μA peak differential (pk diff)
i_{dacp}	-620 μA pk se (code +31) max. (note: these figures don't include dc source current,
i_{dacn}	-640 μA pk se (code -32) max. or the 320 μA dc bias current).
i_{sigp}, i_{sign}	+400 μA pk se + 550 μA cm = 950 μA max. -400 μA pk se + 550 μA cm = 150 μA max.

1.3.3 Critical Path Timing and Error Specifications.

In order for the comparator to have time to make a decision, the DAC output, i_{sig}, must be settled to within 1/2 LSB (10 μA) in no more than 6.5ns after a control codeword change on **sp[0:5]**. Moreover, the codeword change must occur during the time that the comparator is latching a decision from the

previous signal input. This is shown in Figure 1.5 below. The comparator's low-true control signals, **nrst** and **ncmp** must be two-phase, non-overlapping signals within the comparator (external to the comparator, the control bits are **compare** and **reset,** both inverted within the comparator block). Based on this type of comparator's general performance, a decision is latched typically between 1ns and 2ns [5], [6], and the DAC is given about 1.5ns to switch code values in its core. Thus, more time is available for the DAC output to settle if the codeword is changed at 1ns to 2ns following **ncmp** going true.

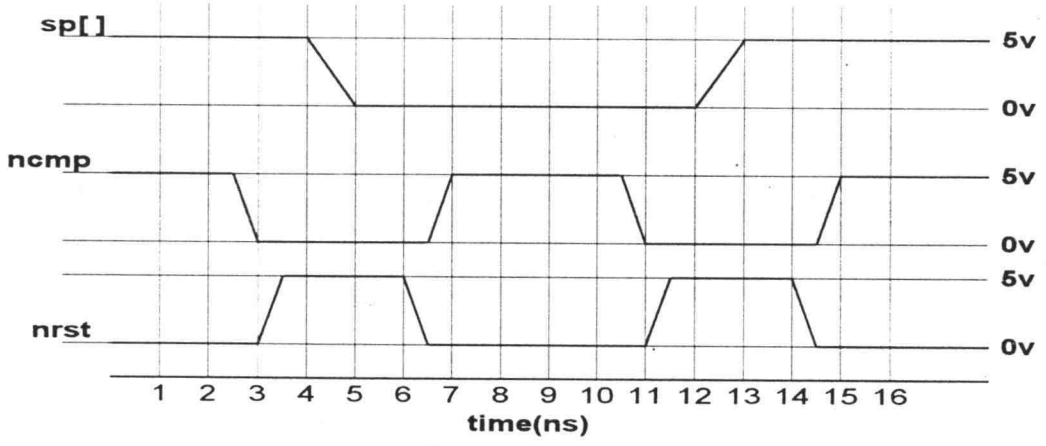


Figure 1.5: DAC-comparator signal timing diagram

The DAC is targeted to achieve a maximum differential nonlinearity error of less than 1/2 LSB over all codes and worst case process-voltage-temperature corners (PVT). Likewise, the comparator design is targeted to be able to make a

correct decision with a minimum input differential voltage corresponding to a 1/2 LSB differential output from the DAC of 10 μA.

2. BLOCK DESIGN

2.1 DIGITAL TO ANALOG CONVERTER (DAC)

The DAC is composed of two sections. The first section is the DAC core which responds directly to the digital feedback filter to provide the signal feedback in the loop. It uses the 6-bit control word from the feedback filter to activate switches which sink current from the complementary sides of the DAC at the analog summing node, through the six current sink branches. Within this core, there are two blocks named SWLEV2 and SWLEV3 which are used to control the voltage levels on the gates of the switches; their designs will also be reviewed. The second section provides bias voltages for the DAC core and the signal path FETs, and contains the analog summing node of the forward and feedback signal currents. The complementary sides of the current output from the signal path are compared against one another at the comparator to determine the sign of the signal at the summing node. It was intended that there be enough margin designed into the possible signal sums, along with sufficient accuracy of the DAC feedback signal, such that any threshold mismatch or random offsets at the differential output current mirror would not result in a sign error upon comparison. This margin is quantified in the design discussions on the core and the signal path that follow.

2.1.1 DAC Core Design

The quantization of current in the core is accomplished using six sets of arrayed n-FETs. The number of parallel FETs in each set is determined by an appropriate power of 2 (2^0 through 2^5), as shown in Figure 2.1. A unit current of $10\,\mu A$ (differentially, 1LSB=$20\,\mu A$) was desired to keep the power consumption of the DAC at approximately 5mW. Using a conduction factor of $k'_n = 90\mu A / v^2$ and assuming a $V_T \approx 0.7v$ and a $V_{gs} = V_{dsat} + V_T \approx 1.2v$, an original estimate of the sink FETs' unit size *W/L* ratio was calculated as 7/8 using the equation $\left(\frac{w}{l}\right) = \frac{2I_{dsat}}{k'\left(V_{gs} - V_T\right)^2}$. The ratio was increased to 7/6 and after a higher gate voltage was chosen and after SPICE simulations revealed a larger $V_T \approx 0.8$.

The gate length was chosen to be 3.2um based on previous designs in silicon for this particular CMOS process. Nearly halving the gate length was desirable for limiting the total area of the core, especially for the two MSB branches which have 16 and 32 arrayed sink FETs respectively. However, halving the gate length also increases the percent difference in unit current between each branch due to current density and threshold mismatches of the smaller devices. The percent current density and threshold mismatch are calculated for devices of lengths 3.2um and 1.2um for comparison in section 2.1.1.1.

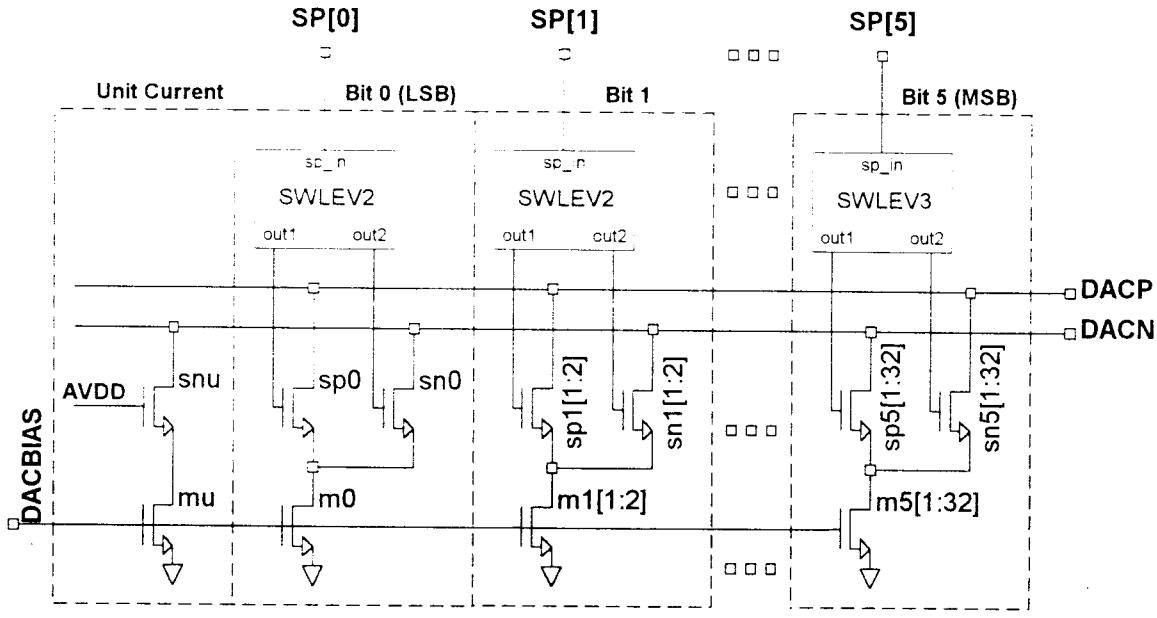


Figure 2.1: DAC Core - current sink branches 0-5

The branch switches are controlled by the 6-bit control word output of the feedback filter. The DAC control bus is labeled **SP[5:0]** in Figure 2.1. It is split out to the inputs of the six SWLEV blocks as **SP[0] - SP[5].** The SWLEV blocks will be discussed in section 2.1.1.2 provide a reduced switching voltage range. Using the SPICE dc operating point solution to attain a value for the backgate voltage on the n-FET switches, a nominal threshold voltage was determined for the switch devices. The gate voltage "on-off" range for the switches was then determined by fixing a nominal value for the drain voltage of the sink FETs, $V_{d_{sink}}$, so that an "off" switch had $V_{g_{sw}} < V_{d_{sink}}$. Likewise, an "on" switch had its nominal V_{dsat} voltage set to $V_{g_{sw}} - V_{d_{sink}} - V_{th_{sw}} \approx 0.5v$.

The code control table for the DAC is shown in Table 2.1. It shows that the decimal code of +31 (count 63) will result in 620 μA being sunk from the **dacp** node, while the code -32 (count 0) will result in 640 μA being sunk from the **dacn** node. The DAC is differentially balanced at code 0 (count 32) when both **dacp** and **dacn** have 320 μA being sunk by the DAC branches.

Table 2.1: DAC Control Codes and Resulting Differential Output

Current weight	32:1	16:1	8:1	4:1	2:1	1:1	Differential sum of currents w=10uA	uA	dec. code
sp[5-0]	[5]	[4]	[3]	[2]	[1]	[0]	$i_{dacp} - i_{dacn}$		
i_{dacn}=1w	0	1	1	1	1	1	+32w+16w+8w+4w+2w+1w-1w= 62w	620	+31
	0	1	1	1	1	0	+32w+16w+8w+4w+2w-1w-1w= 60w	600	+30
	0	1	1	1	0	1	+32w+16w+8w+4w-2w+1w-1w= 58w	580	+29
	0	0	0	0	1	0	+32w-16w-8w-4w+2w-1w-1w = 4w	40	+ 2
	0	0	0	0	0	1	+32w-16w-8w-4w-2w+1w-1w = 2w	20	+ 1
diff. Balanced	0	0	0	0	0	0	+32w-16w-8w-4w-2w-1w-1w = 0w	0	0
	1	1	1	1	1	1	-32w+16w+8w+4w+2w+1w-1w = -2w	- 20	- 1
	1	1	1	1	1	0	-32w+16w+8w+4w+2w-1w-1w = -4w	- 40	- 2
	1	1	1	1	0	1	-32w+16w+8w+4w-2w+1w-1w = -6w	- 60	- 3
	1	0	0	0	1	0	-32w-16w-8w-4w+2w-1w-1w = -60w	-600	- 30
	1	0	0	0	0	1	-32w-16w-8w-4w-2w+1w-1w = -62w	-620	- 31
i_{dacp}=0	1	0	0	0	0	0	-32w-16w-8w-4w-2w-1w-1w = -64w	-640	- 32

2.1.1.1 Current Mismatch between Core Branches

Pelgrom *et al.* [2], have shown that the measured current mismatch in two parallel-connected MOSFETs is accurately modeled by the following equation:

$$\frac{\sigma^2(I_d)}{I_d^2} = \frac{4\sigma^2(V_{TO})}{(V_{GS}-V_{TO})^2} + \frac{\sigma^2(\beta)}{\beta^2}. \qquad \textbf{(2.1)}$$

To calculate the standard deviation of the current, (2.1) was used in conjunction with the mismatch data for V_{TO} (0v substrate voltage) and the current factor, $\beta = k'\left(\frac{w}{l}\right)$, and is documented in [2]. Their standard deviations, as given in (2.2), are described using an empirical area proportionality constant *A*, for local variations and a spatial parameter, *S*, for global variations, both of which were also derived in [2]. For example, in (2.2) the term A_{VTO} represents the variance of threshold voltage with device area, while S_{VTO} represents the variance of threshold voltage with the global spacing of devices across a wafer. *D* is the horizontal spacing between devices.

$$\sigma^2(V_{TO}) = \frac{A_{VTO}^2}{WL} + S_{VTO}^2 D^2 \qquad \text{and} \qquad \frac{\sigma^2(\beta)}{\beta^2} = \frac{A_\beta^2}{WL} + S_\beta^2 D^2. \qquad \textbf{(2.2)}$$

It was found that the variations of V_{TO} and β with spacing were negligible with respect to the variations of these parameters with area, so the calculation for current mismatch was done using only the areal variation terms for each parameter.

The empirical results of [2] show a value of $30\,mv-\mu m$ for A_{VTO} for a 50nm gate-oxide process, and a value of $1.9\%\,\mu m$ for A_β for a 25nm gate-oxide process. Also from [2], Pelgrom reports that threshold mismatch is directly proportional to the gate oxide thickness, whereas β mismatch remains constant with respect to different gate oxide thicknesses. Using this finding, the $1\,\mu m$ CMOS process in which the DAC is designed has a gate-oxide thickness of 20nm, so the A_{VTO} value can be divided by 2.5 yielding $12\,mv-\mu m$. A_β doesn't scale so the quoted value of $1.9\%\,\mu m$ is used. These values of A_{VTO} and A_β were substituted into (2.2) along with the sink FET unit area of $WL=(3.7\,\mu m)(3.2\,\mu m)$ and the computed variances were entered into (2.1). This result was multiplied by the square of the DAC unit current of $10\,\mu A$, and the standard deviation of the current in any one of the parallel sink FETs was found to be $0.132\,\mu A$. This is compared to the current variation in a device with the same *W/L* ratio but with area $WL=(1.4\,\mu m)(1.2\,\mu m)$, which is computed to be $\sigma(I_d)=0.351\mu A$. Because FETs mu-m5 in Figure 2.1 are always sinking current, each sink FET contributes to error in the feedback signal regardless of the code. Using a sink FET size of *W/L*=1.4/1.2, the signal error could be as much as $22.13\,\mu A$, or 1 lsb. Based on the design size of *W/L*=3.7/3.2, mismatch could result in up to $8.34\,\mu A$. This level of mismatch is barely acceptable at less than 1/2 LSB. These results indicate that in practice, keeping the *W/L* ratio and

device size of 7/6 would have been important to obtaining acceptable matching performance in the DAC core.

2.1.1.2 SWLEV Blocks

To reduce current transients when switching between current branches on a code change, a block called SWLEV2 was designed to provide a reduced switching voltage range. The topology for this block was taken from a design by Segaram [3] and is illustrated below in Figure 2.2. The nominal voltage range that SWLEV2 was designed to provide is 1.5v< $Vout_{SWLEV2}$ <3.5v. Reducing the voltage swing to 2v at the gates of the switches cuts the magnitude of the current transient by more than one third, with respect to an otherwise 3.3v swing (**VDD-V_{dm0}**).

The capacitances that act as a load on the two summing nodes, **dacp** and **dacn**, are primarily the drain-source capacitance (C_{ds}) of the signal path source FETs *P*3 and *P*4 (144um/2um devices) shown in Figure 2.5, and the gate-source capacitance (C_{gs}) of the switch arrays for the six branches, **sp[ ]** and **sn[ ]**. The switch array load value is calculated to be 2.1fF per each 2um/1.2um switch or approximately 135fF total in the worst case of code 0, when all the switches to the **dacn** line are on. However, because one of the switching paths is conducting at all times on each current leg, and because the switches are providing a cascoding effect, there is little change in capacitive loading on **dacp** or **dacn** with changes in code.

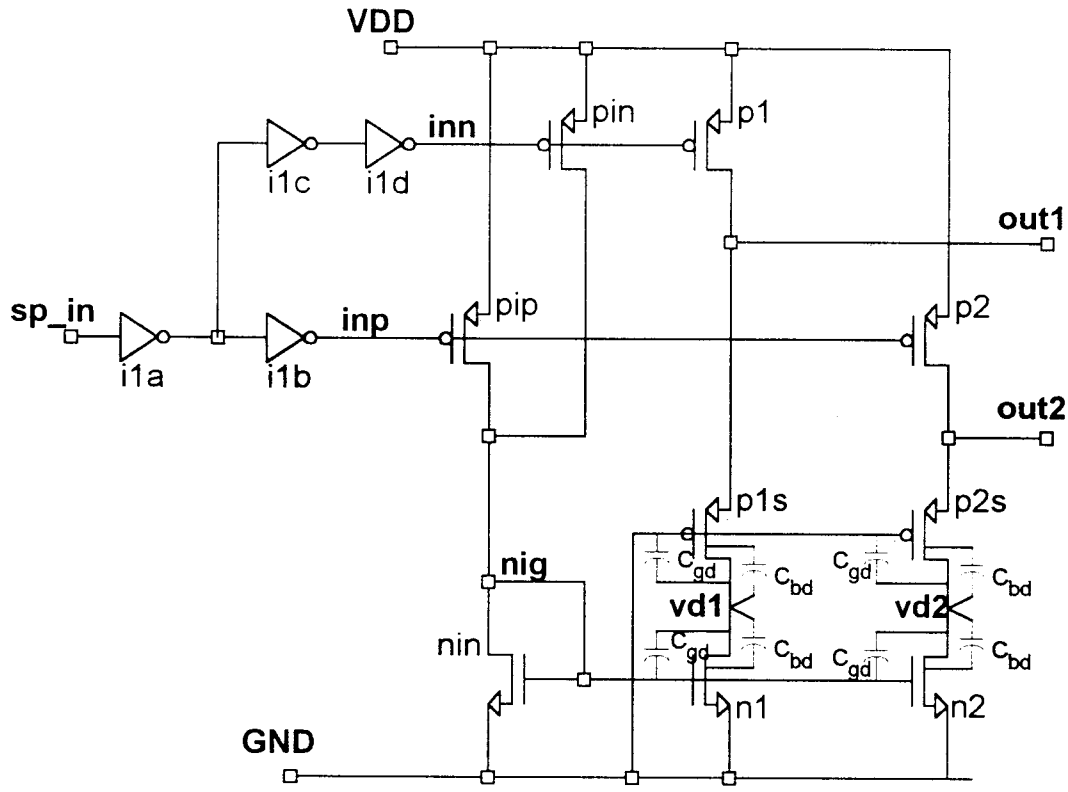


Figure 2.2: SWLEV2 Block with c_{bd}/g_{ds} parasitc dependence for output-low discharge

The inverters at the input of Figure 2.2 are present to speed up the edges of the control signal coming in on **sp_in**. The input inverters are sized to ensure that SWLEV2's outputs change such that in each branch pair, both switches are momentarily on. Code changes result in a changing edge on **sp_in**, and the goal is to keep at least one (or both) outputs, **out1** and **out2**, above the V_T of their branch's switch. This is to prevent further current transients that would result

from having both switches off during a code change due to a slow output change in the SWLEV2 block. This condition is illustrated in Figure 2.3.

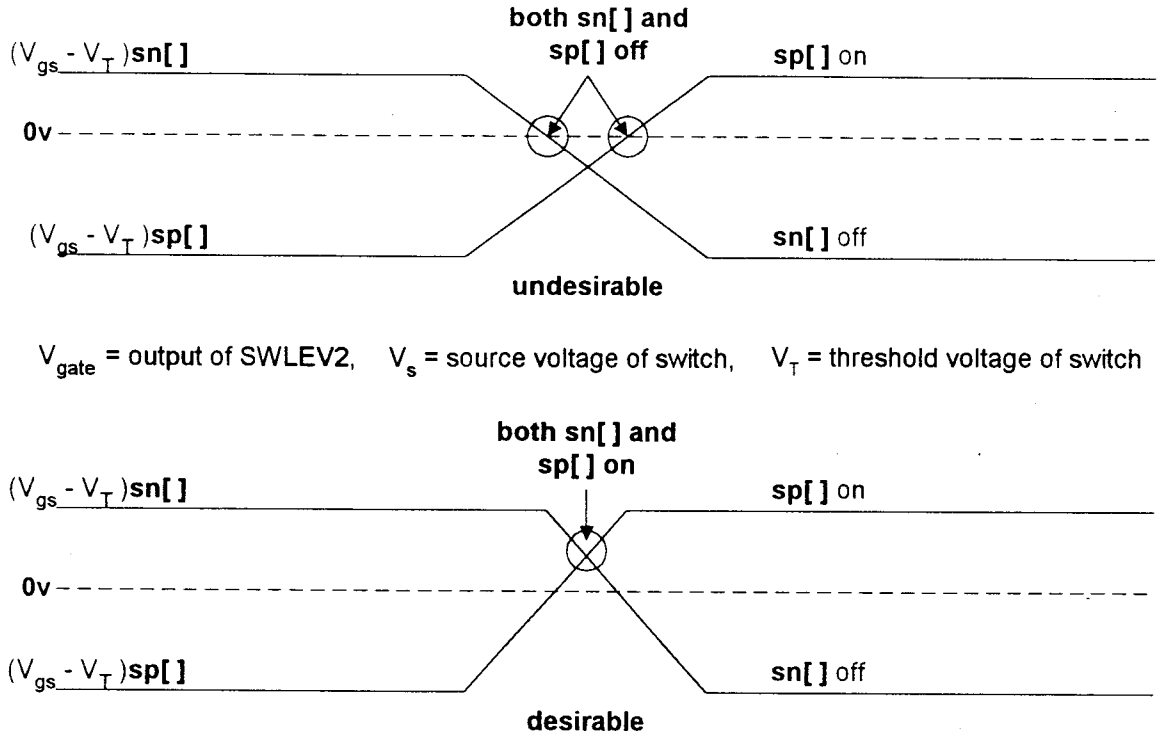


Figure 2.3: Effect of SWLEV2 block on switching characteristics

The central circuit of SWLEV2 and SWLEV3 can be seen to have an active current path through FETs *pin* or *pip*, whichever device is turned on by a 0v input at its gate. That current in combination with FET *nin* sets up a gate voltage for the pull-down FETs, *n*1 and *n*2. The devices *p*1 and *p*2 provide the pull-up strength for an out_high output. The DC analysis for one of the outputs is as follows:

$$out\_low = V_{sg}(p1s) = V_{gs}(n1) - V_{TN} + V_{dsat}(p1s)$$

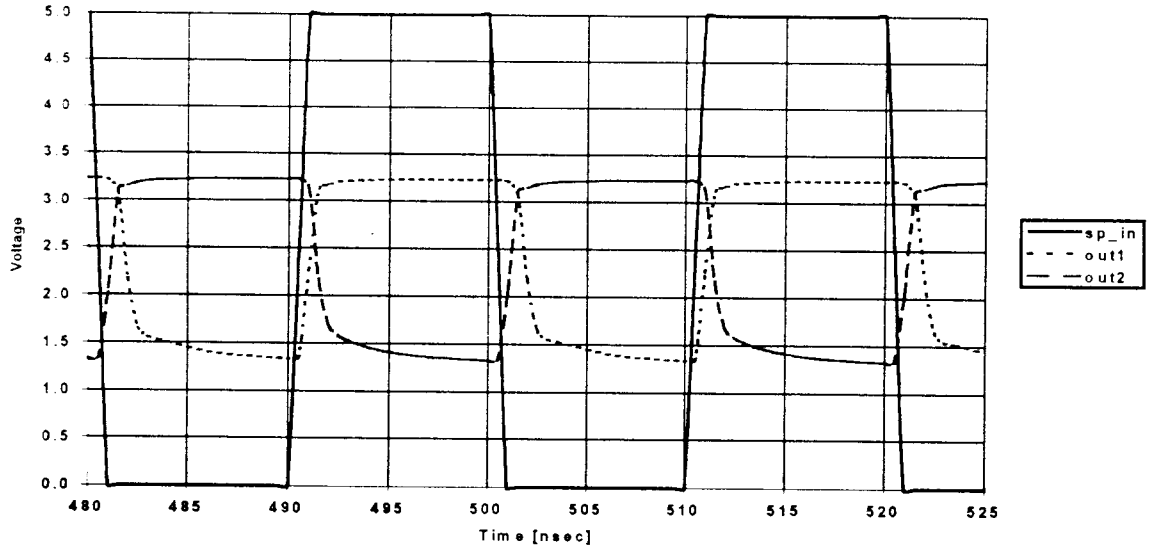
$$= nig - V_{TN} + V_{dsat}(p1s) \qquad \textbf{(2.3)}$$

$$out\_high = V_{DD} - V_{ds}(p1) \quad \text{where} \qquad \textbf{(2.4)}$$

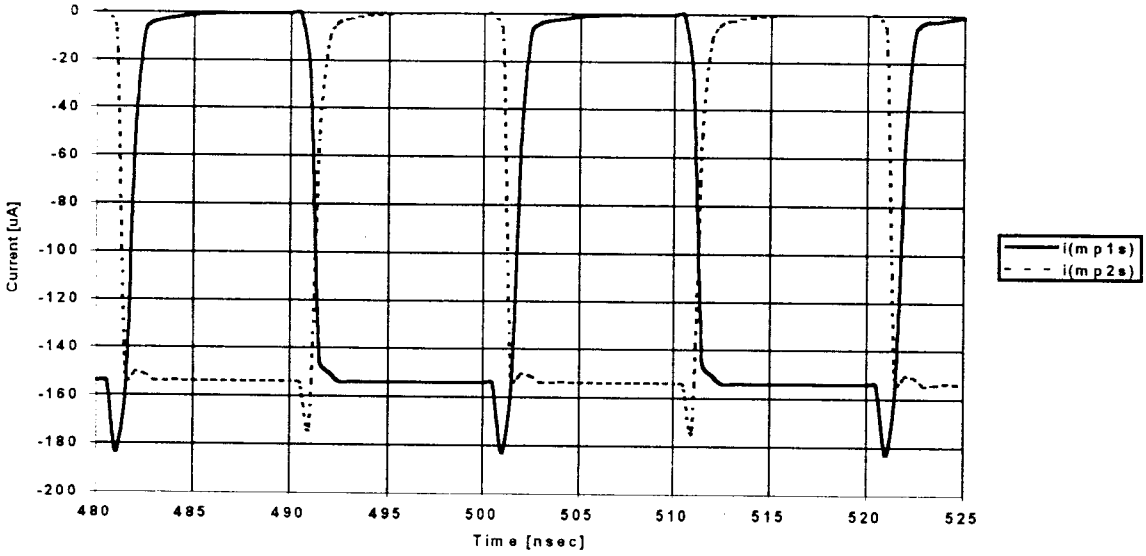
$$V_{ds}(p1) = \left(V_{DD} - V_{TP}\right) \pm \sqrt{\left(V_{DD} - V_{TP}\right)^2 - 2C_1\left(nig - V_{TN}\right)^2}, \quad \text{and} \quad C_1 = \frac{k'_n/2(w/l)_{n1}}{k'_p(w/l)_{p1}}.$$

FETs *p*1*s* and *p*2*s* are always on and saturated (although just barely when their series n-FET, *n*1 or *n*2 is fully conducting). FETs *n*1 or *n*2 will conduct in saturation when their respective output is at the out_high level of ~3.4v. The complementary n-FET will be barely conducting when its output is at the out_low level ~ 1.2v.

The width of the input devices, *pip* and *pin*, are responsible for the maximum output voltage level, as their width controls the value of **nig** via the current that they source. With regards to Figure 2.2, the parasitic drain-bulk capacitances on *n*1 and *n*2 are responsible for the out_low output's R-C time constant, which is shown in Figure 2.4. As a pull-up turns on, *p*2 for example, and **out2** goes to the out_high voltage level, the complementary output, **out1**, has its pull-up turned off and FET *n*1's V_{ds} shrinks. The drain-source impedance of *p*1*s* starts rising and increasingly less current flows in this branch. SPICE simulations show that the R_{ds} of the p-FETs averages $\approx 800K\Omega$ (this is only at the knee of the v_{ds} / i_{ds} curve), while both *p*1*s* and *n*1 are turning off, as shown in Figures 2.4a and b. The C_{db} of *n*1 is about 8.5fF. Referring to Figure 2.2 it can be seen



(a)



(b)

Figure 2.4: Complementary outputs of SWLEV2 block (a) high and low output voltage characteristic clocked by sp_in, and (b) current through series p-FET.

that both C_{db} and C_{gd} for *p*1*s* are in parallel with *n*1's parasitic, and they account for another 6.5fF. The rate of approaching the out1_low voltage level is roughly equal to

$$r_{ds} \times c_{d1} \approx 12ns.$$

In Figure 2.4a it shows an exponential decay on **out1** throughout a single clock cycle when **out2** is high, but in fact, the out_low voltage doesn't reach it's final value; *n*1 is still slowly pulling current from the parasitic C_{d1} when the DAC code changes. As Figures 2.3 and 2.4 indicate, it is desirable that *n*1 or *n*2 discharge their parasitic drain capacitance somewhat slower than the complementary output rises, as this allows the complementary switches in the core to both be momentarily on. All that matters is that the out_low value reaches a level where it shuts off its branch switch at the beginning of a new code cycle, but in fact, in the slowest corner case, the shut-off voltage is reached in 1.3ns, and in the nominal case, in 0.6ns.

2.1.2 Output and Bias Circuits

The DAC core sinks current away from the analog summing node and the resulting signal current is output from the DAC via a differential pair of high-swing cascode mirrors, as shown in Figure 2.5. Connecting the gate of *M*4(8) to the drain of *M*2(6) makes for a low-impedance input for the signal current at those drains, and the output mirror creates a high-impedance at **Vout**.

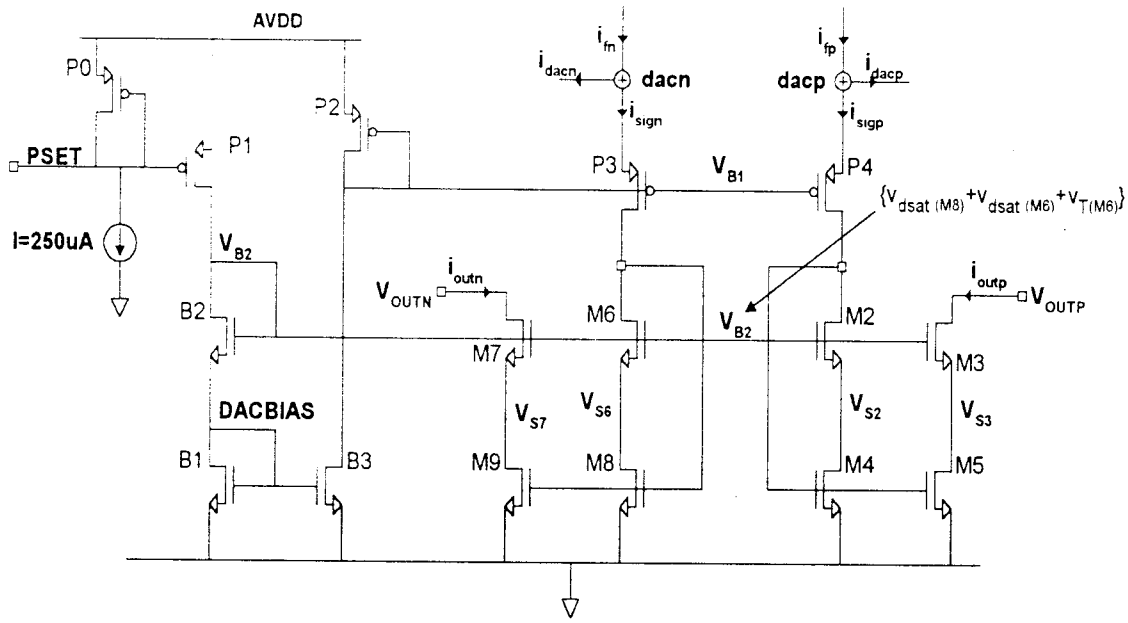


Figure 2.5: The DAC Signal Path and Bias Circuit

2.1.2.1 Bias Circuit

The sizes of the devices in Figure 2.5 are given in Table 2.2. The bias circuit generates its reference current from the input voltage labeled **pset**. The

Table 2.2: Device Sizes for the Circuit of Figure 2.5

Device Label	W/L
P0	125/3.2
P2	4/5
B2	134.4/1.8
P3, P4	144/2
M4, M5, M8, M9	105.6/3.2

Device Label	W/L
P1	5/3.2
B1	10.6/10
B3	11.3/10
M2, M3, M6, M7	240/1.2

pset voltage applied to the gate of any p-FET device of the same length of 3.2um, will generate a current in the amount of $2\,\mu A$ per 1um of width because of the ratio of the magnitude of the current source to the width of device *P*0 (250uA/125um). The current being mirrored in this reference circuit then is nominally $10\,\mu A$. The device *P*2 is not matched to any other FET, but has a long gate length in order to keep its *Vds* large and therefore keep the bias voltage $\mathbf{V_{B1}}$ at approximately 1.3v.

To keep the output stage devices in saturation over the signal current range ($150\,\mu A$ to $950\,\mu A$), the bias voltage $\mathbf{V_{B2}}$ needs to be approximately $V_{dsatM8} + V_{dsatM6} + V_{TM6}$. The threshold voltage of device M6 is the larger portion of the bias value due to the FET's backgate bias which increases the threshold voltage. It follows that $\mathbf{V_{s2(3)}}$ is able to remain at about 2/3 the total voltage drop across the cascode FETs. Also the FET *B*1 was used to create a voltage **DACBIAS** $\approx V_{dsatB1} + V_{TB1}$ to bias the sink FETs in the DAC core.

2.1.2.2 Output Circuit

Some characteristics of the output circuit were mentioned above. The input impedance was required to be very low in the signal current path. Figure 2.6(a) and (b) show the signal path cascode and its small-signal equivalent circuit.

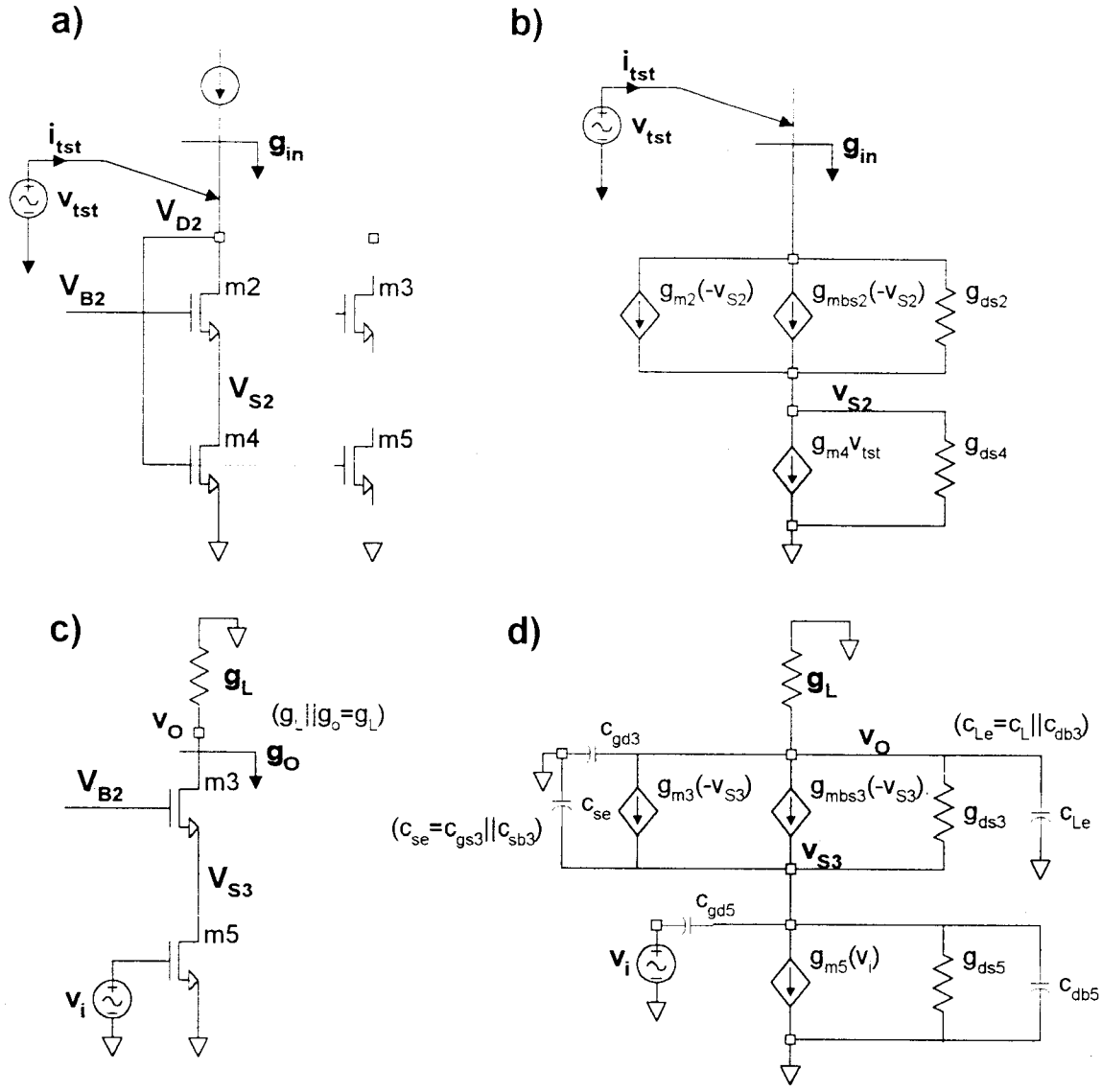


Figure 2.6: Small-Signal Models of the Signal Path: a) schematic of signal path cascode, b) small-signal equivalent circuit of (a) to calculate g_{in}, c) schematic of the output signal mirror, and d) small-signal equivalent circuit of (c) with parasitics.

Summing currents at $\mathbf{V_{s2}}$ in (b) yields

$$i_{tst} = -g_{m2}V_{s2} + g_{mbs2}V_{bs2} + g_{ds2}(V_{tst} - V_{s2}) \quad \text{and} \qquad \textbf{(2.5)}$$

$$i_{tst} = g_{ds4}V_{s2} + g_{m4}V_{tst} \Rightarrow V_{s2} = \frac{i_{tst} - g_{m4}V_{tst}}{g_{ds4}} \qquad \textbf{(2.6)}$$

Substituting the expression for $\mathbf{V_{s2}}$ in (2.6) into (2.5) and gathering terms gives

$$i_{tst}\left(\frac{g_{ds4} + g_{ds2} - g_{m2}}{g_{ds4}}\right) = V_{tst}\left(\frac{g_{ds4}g_{ds2} + g_{m4}g_{m2} + g_{m4}g_{ds2}}{g_{ds4}}\right) + g_{mbs2}V_{bs2}.$$

Neglecting the $g_{mbs2}V_{bs2}$ term and realizing that the g_m terms are an order of magnitude greater than the g_{ds} terms, an approximate expression for g_{in} results:

$$g_{in} = \frac{i_{tst}}{V_{tst}} \approx \left(\frac{g_{ds4}g_{ds2} + g_{m4}g_{m2} + g_{m4}g_{ds2}}{g_{ds4} + g_{ds2} + g_{m2}}\right) \approx g_{m4}. \qquad \textbf{(2.7)}$$

g_{m4} was calculated to be about $1730\,\mu S$ while the SPICE small-signal analysis reported g_{m4} =$1352\,\mu S$ or $740\,\Omega$.

Also of interest is the output circuit's frequency analysis as the components of the feedback loop are required to operate at 200MHz. As an independent stage, referring to Figure 2.6(c) and (d), the output cascode would have a high-impedance output node equivalent to $g_o \approx \left(\frac{g_{ds3}g_{ds5}}{g_{m3}}\right)$, which is calculated to be roughly $4.15\,M\Omega$. The cascode design provides isolation for the signal nodes, $\mathbf{V_{s3}}$ and $\mathbf{V_{s7}}$ (from Figure 2.5), keeping the signal current steady at those nodes when voltage glitches occur at V_{out}. Both figures indicate that there is however, an external load present which dominates the total output conductance, and renders the impedance low at the output nodes. This will be

shown in section 2.3 where the interface between the DAC and the comparator is discussed.

To do the frequency analysis, an ac voltage source was placed at the gate of *m*5 (in Figure 2.6(d)) to represent the small-signal voltage changes that occur as the signal current changes. Taking into account the parasitic capacitances and the external load capacitance shown in Figure 2.6(d), the current is summed at the drain of *m*3 as follows: $V_o\left(Sc_{gd3}+Sc_{Le}+g_L+g_{ds3}\right)=V_{s3}\left(g_{ds3}+g_{m3}\right)$ which yields an expression for $\mathbf{V_{s3}}$,

$$V_o\frac{\left(Sc_{gd3}+Sc_{Le}+g_L+g_{ds3}\right)}{\left(g_{ds3}+g_{m3}\right)}=V_{s3} \qquad \textbf{(2.8)}$$

Summing currents at $\mathbf{V_{s3}}$ gives

$$-Sc_{se}V_{s3}-g_{m3}V_{s3}-g_{ds3}V_{s3}+V_o g_{ds3}=Sc_{gd5}V_{s3}-Sc_{gd5}V_i+g_{m5}V_i+g_{ds5}V_{s3}+Sc_{db5}V_{s3}.$$

The expression in (2.8) is substituted for $\mathbf{V_{s3}}$. The equation is simplified using the approximations $g_{m3}>>g_{ds3},g_{ds5}$ and $g_L>>g_{ds3}$. Doing the multiplication with $\mathbf{V_{s3}}$ results in an expression for the total transfer function:

$$V_i\left(Sc_{gd5}-g_{m5}\right)=$$
$$V_o\left[\frac{S^2\left(c_{gd3}+c_{Le}\right)\left(c_{se}+c_{gd5}+c_{db5}\right)+S\left(g_{m3}\left(c_{gd3}+c_{Le}\right)+g_L\left(c_{se}+c_{gd5}+c_{db5}\right)\right)+g_{m3}\left(g_L+g_{ds3}\right)}{g_{m3}}\right]$$

The capacitance values are calculated refering to [4]. The gate-drain capacitances, c_{gd3} and c_{gd5}, are approximately $c_{gdovl}=L_D C_{ox} W_{neff}$, where L_D is the

lateral diffusion overlap in microns, W_{neff} is the effective width of the drain or source area, $W_{neff} = W_{drawn} - 2W_D$. Here, the width diffusion, W_D, is 0.34um for an n-channel device. C_{ox} is the capacitance per unit area of the gate oxide, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = 1.73 fF/\mu m^2$ in the process being used. Using these expressions and the device widths, c_{gd3} and c_{gd5} are calculated to be on the order of 35fF (SPICE reports 43.2f and 18.4f, respectively). The evaluation of c_{se}, c_{Le}, and c_{db5} are also made using the expressions in [4] with the following constants for an n-channel device: $C_{jo} = 0.32 fF/\mu m^2$, $C_{jsw} = 0.27 fF/\mu m$, and $PB = 0.8v$. The three capacitances, c_{se}, c_{Le}, and c_{db5}, were calculated to be between 150fF and 240fF, with an estimate of 200fF for c_L. Thus, a further simplification is made using $c_{Le} >> c_{gd3}$ and $c_{se}, c_{db5} >> c_{gd5}$ to give

$$\frac{V_o}{V_i} = \frac{g_{m3}\left(Sc_{gd5} - g_{m5}\right)}{g_L g_{m3} + S\left(g_{m3}c_{Le} + g_L\left(c_{se} + c_{db5}\right)\right) + S^2 c_{Le}\left(c_{se} + c_{db5}\right)}.$$

The final result after multiplication and combining terms is:

$$\frac{V_o}{V_i} = -\frac{g_{m5}}{g_L} \times \frac{\left(1 - S\frac{c_{gd5}}{g_{m5}}\right)}{\left(1 + S\frac{\left(g_{m3}c_{Le} + g_L\left(c_{se} + c_{db5}\right)\right)}{g_L g_{m3}} + S^2\frac{c_{Le}\left(c_{se} + c_{db5}\right)}{g_L g_{m3}}\right)}. \quad \textbf{(2.9)}$$

The value of the right-half plane zero is computed at 97Grad/sec or ~16GHz, (SPICE puts it at 30GHz) while the two left-half plane poles were found

solving the quadratic in S, and were calculated to be at 175MHz and 2.2GHz. SPICE finds the first or dominant pole right at 125MHz.

The gain of the output stage is not of concern except for stability, as R_L= 1/ G_L causes a current to voltage conversion of the output signal current. However, the choice of R_L in conjunction with the DC bias current of the output mirrors and signal current swing, does determine the voltage range of the converted signal, and this range should be as large as possible. The choice of R_L is discussed further in Section 2.3.

2.1.3 DAC Simulation Results

2.1.3.1 Output Linearity

The DAC was simulated over fifteen PVT corner cases listed below with the following denotations: F, S, N⇒ fast, slow, and nominal process; H, L, N ⇒ 5.25v, 4.75v, and 5.0v AVDD voltage; 85, 0, 50 ⇒ operational temperature in degrees C.

FL85	FL0	FN50	FH85	FH0
NL85	NL0	NN50	NH85	NH0
SL85	SL0	SN50	SH85	SH0

The worst-case nonlinearity occurs for the Fast, Low voltage, 85 deg. C case and is shown in Figure 2.7. The figure illustrates the absolute current deviation from the ideal unit-current for that case multiplied by the code's number of units.

This calculation is plotted when going from code -32 to +31, and from code +31 to -32. The figure shows that the nonlinearity is symmetric about the code axis, the greatest nonlinearity being about -8 μA.

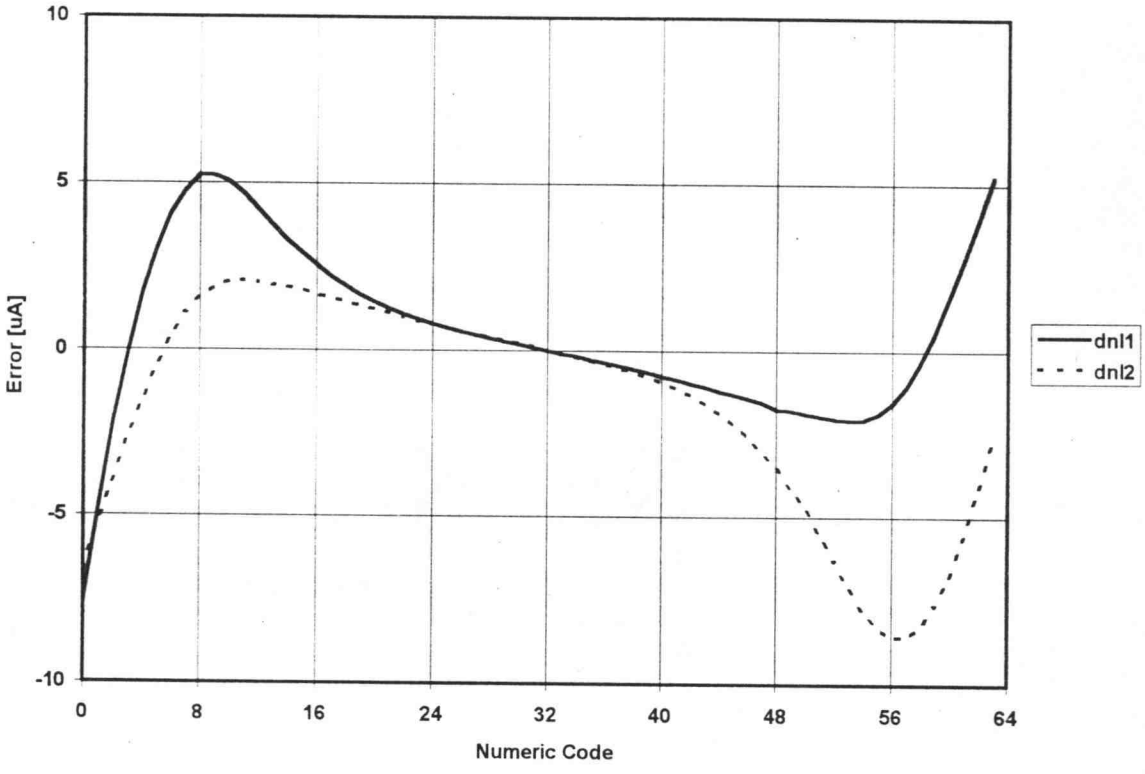


Figure 2.7: Plot of DAC nonlinearity for code stepping -32 to +31 (dnl1) and +31 to -32 (dnl2)

2.1.3.2 Output Transition Speed for Maximum Code and Signal Changes

The DAC's settling time must be less than about 6ns of a 100MHz period, and must meet this requirement for a worse case code change of 1/4 the code scale, or a numeric change of 16, ±8 about a code of 0. To view an unrealistic

case but one that would indicate the limits of the DAC's speed, a simulation using a maximum signal swing and full-scale code change was done. The maximum possible current change in the DAC would occur for the ideal forward signal currents and the feedback currents shown in Figure 2.8. In figure (a) the

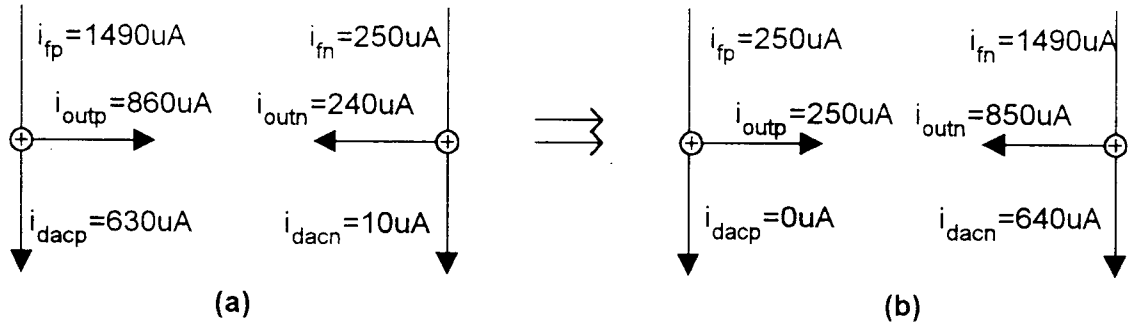


Figure 2.8: Maximum current swing in the DAC signal path. (a) maximum positive differential (code =+31), and (b) maximum negative differential (code =-32)

forward current starts at a maximum differential of 1240 μA (1490 μA-250 μA), and the DAC must sink a maximum differential of 620 μA. The resulting differential output current swing should be i_{outp}-i_{outn}=620 μA. In figure (b) the opposite differential is shown.

Simulating the above maximum changes it was found that in the two worst PVT cases (FL85 and SN85) the differential output settled within 8ns. A second simulation was performed using a code transition of 0 to -1, so that all the control word bits would have to change simultaneously from 0 to 1. The feed-forward

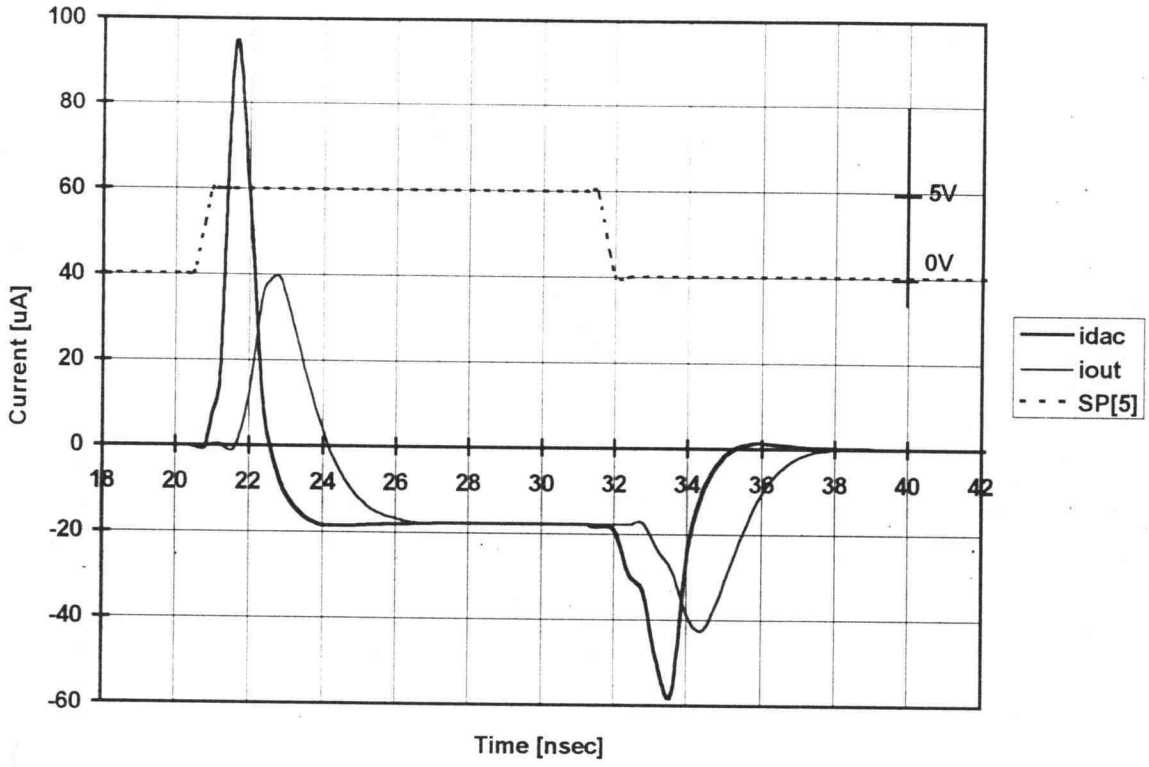


Figure 2.9: Differential transient response of the DAC core (idac) with change of control codeword SP[0:5]. Also shown is the differential DAC output (iout) due to the same step change.

current was fixed at the forward signal path's common-mode current of 870 μA, and the transient response to this code step is shown in Figure 2.9.

In this example, the code is going from 0 (000000) to -1 (111111) and then back to 0. This is a worst-case PVT corner using SLOW process models at 85 degrees C and a 4.75v supply, and consequently, the unit current is only 8.87 μA. Thus, the expected final value should be only 17.74 μA. From the time the code begins to change at 20.5ns, indicated by the code bit SP[5], to the time

i_{dac} settles to within 3.3% (0.59 μA) of the final value there is a period of 4.5ns. The settling characteristic of i_{out} is shown to lag that of i_{dac} by 1.5ns to 2ns, since it is generated after the signal summation of i_{dac} and i_{ff}, and then mirrored to the output of the DAC. The simulation shows that its settling time from the time of the code change to 3.3% of final value is 5.8ns. The 1/2 LSB error level was 1/2 the signal output in this case, and the 3.3% error was chosen arbitrarily to illustrate the DAC's ability to settle close to an ideal value in a reasonable time. If settling to 1/4 LSB is examined (settling within 4.4 μA), both i_{dac} and i_{out} reach this level of accuracy in less than 5ns.

2.1.3.3 Power Consumption

Based on the DC bias currents, the signal path was expected to dissipate 550 μA, the core sink branches 640 μA, and the bias circuit was designed to use 35 μA, which would result in a total of 1.23mA or 6.1mw. SPICE simulations indicate that the AVDD-supplied portion of the DAC does indeed use very close to this original power estimate as the results range over PVT between 5.7mw to 6.2mw.

Unfortunately, this is not the total of the DAC's power consumption, and a valuable lesson has been learned regarding the pitfalls of switch-control circuits. As it turns out, the switching circuits (SWLEV2 and SWLEV3), which were considered for their ability to speed the core's settling time, have a large power drain built into their topology. One of the outputs must be high for any input

level which results in near-constant current consumption, along with the input branch which is also a static power drain as it is always on. The SWLEV2 block, which is designed to drive a 50fF load, uses 150 μA in its output branch; its input and bias FETs use 400 μA, for a total of 550 μA. The SWLEV3 block is designed to drive a 100fF load for the two most significant bits, and this block uses a total of 1.4mA. The DAC uses four SWLEV2 blocks and two SWLEV3 blocks. This brings the total of the VDD-supplied blocks to 5mA or 25mw of power. Obviously, this is not an acceptable result, and the SWLEV circuits should not be used in a low-power design.

2.2 REGENERATIVE LATCHING COMPARATOR DESIGN

It is important for several aspects of the comparator to discuss its design in conjunction with the DAC-to-comparator interface circuit, shown in Figure 2.11. However, the basic design of the comparator will be reviewed here with regards to Figure 2.10.

The goal of this comparator design was primarily to achieve high speed and accuracy to a differential 1/2 LSB current output from the DAC of 10 μA. The comparator has no offset cancellation and as noted in [5], a regenerative latch design suffers from mismatch effects of the process and will usually attain

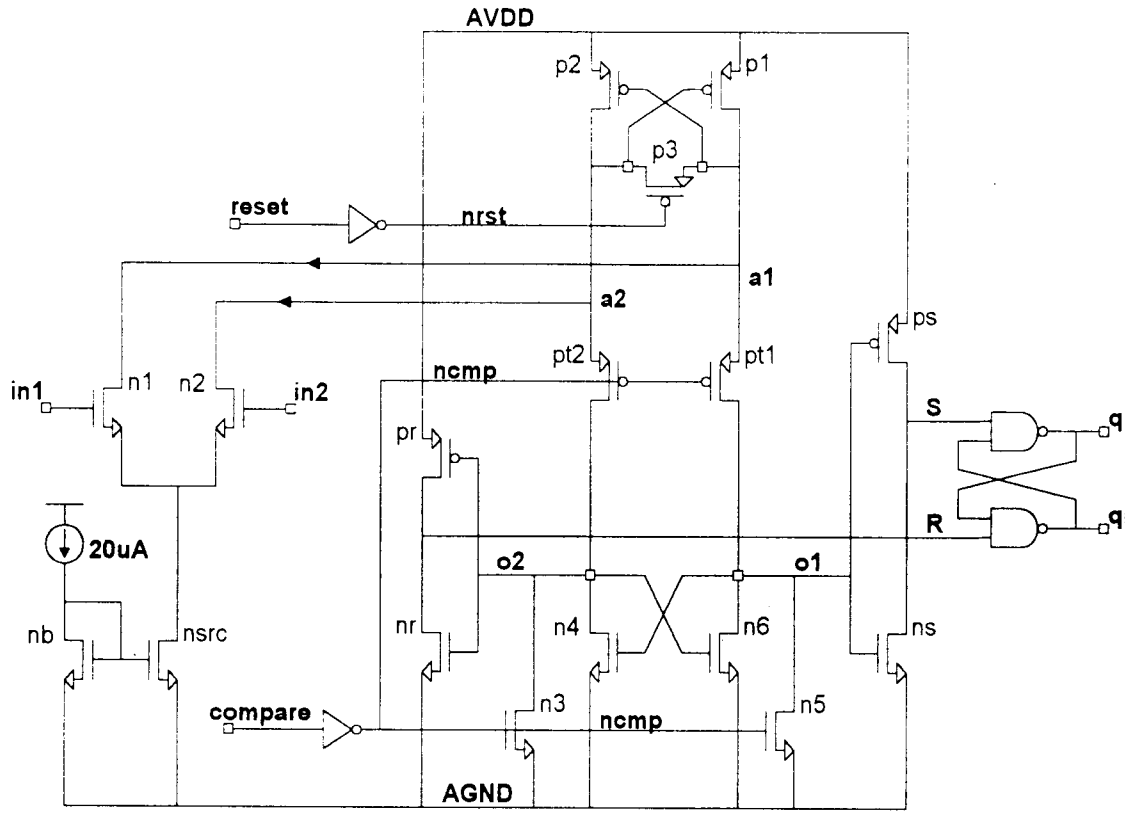


Figure 2.10: Regenerative-latching Signal Comparator

input offsets in the several tens of millivolts. Multistage offset cancellation using both input offset and output offset cancellation are discussed in [5], and can be used to reduce the input-referred offset.

2.2.1 Topology and Description

The basic architecture of the comparator of Figure 2.10 was taken from [6] as in that design, the intent was to minimize the regeneration time constant, τ_{reg}.

Regarding the figure, two-phase, non-overlapping clocks are used to generate a reset period and a regeneration period. During the reset period the compare signal is low so FETs *pt*1 and *pt*2 are off, isolating the input stage of the core from the output stage. Also the precharge FETs, *n*3 and *n*5 are on, pulling the output nodes, **o1** and **o2**, to AGND. FET *p*3 is on pulling the two input nodes, **a1** and **a2** to the same voltage level. During regeneration mode, **nrst** goes high (**reset** goes low) and **ncmp** goes low (**compare** goes high) allowing current to be sourced from *p*1 and *p*2 through *pt*1 and *pt*2, which also allows the input voltages to be pulled apart via the positive feedback loop provided by both the n- and p- flip-flops.

The major causes of offset in this circuit are due to mismatches in the input pair, *n*1 and *n*2, between *p*1 and *p*2, *pt*1 and *pt*2, and secondarily, between the precharge and n-channel flip-flop transistors. Charge injection from *pt*1 and *pt*2 will introduce another differential error. The sum of the offsets due to the above charge injection and the p-FET pair mismatch is reduced by the gain of the input stage, $\frac{g_{mp1}}{g_{mn1}}$.

Once regeneration is begun, $\tau_{reg} = \frac{C_{in}}{g_m}$, where C_{in} is the total of all the input and parasitic capacitances at node **a1** or **a2**, and g_m is the transconductance of either of the input FETs, *p*1 or *p*2. With some approximation, C_{in} is comprised of the gate-to-source and gate-to-drain capacitances of *n*1,*p*1, *pt*1, and *p*3. It is clear from the above equation that a

smaller C_{in} and a maximized g_m produces a smaller value for τ_{reg}, and thus a faster comparator. The tradeoffs made are in minimizing the sizes of the FETs to reduce the parasitics, at the expense of larger offsets and less current.

2.2.2 Comparator Design

To facilitate a high-speed design, minimum length transistors are used and an attempt is made to minimize the regeneration time constant. The relative sizes of FETs *p*3 to *p*1 and *p*2 are crucial for fast regeneration. When regeneration is begun, there is a short time during which $\tau_{reg} = \frac{C_{in}}{\left(g_{mp1} - 2g_{dsp3}\right)}$ as device *p*3 is not yet all the way off. In fact, its fast turn-off will cause some charge injection at the input nodes, resulting in a differential offset from their reset value. The above equation shows that τ_{reg} doesn't become positive until $g_{dsp3} < \frac{g_{mp1}}{2}$. At some point, $I_{p1} = I_{p3}$, and the rate of change of V_{a1}-V_{a2} reaches a minimum. It is derived in [6] that

$$W_{p3} > \frac{W_{p1}}{4} \qquad \textbf{(2.10)}$$

to ensure that *p*3 supplies enough current to continue to charge node **a1** beyond a voltage where *p*1 is in saturation.

The FET sizes were completely designed around the goal of making $\tau_{reg} \approx 250ps$. Widths of 10um were chosen for the input differential pair, *n*1 and *n*2. V_{TO} mismatch from section 2.1.1.1, equation 2.2, results in a random

offset of approximately 4mv using the 10um width. Even though factors of temperature, power supply variation, and substrate noise will contribute additional offset, the 10um width serves as a good starting point. A calculation of C'_{gs} and C'_{gd} for this width resulted in $C'_{gs} + C'_{gd} \approx 18fF$ for these devices after increasing the result again by half. It was then assumed that the value of $C'_{gs} + C'_{gd}$ would be roughly the same for FETs *p*1, *pt*1 and *p*3. This yielded an estimate for C'_{in} on the order of 80fF, and this would require $g_{mp1} \geq 320\mu s$ to achieve the stated regeneration time constant. The approximation $g_{mp1} \approx k'\left(\frac{W}{L}\right)(v_{gsp1} - V_T)$ was used to compute widths for *p*1 and *p*2, having fixed their lengths at $1\,\mu m$. In the process being used, $k'_p \approx 34\,\mu A/V^2$, and the value of $(v_{gsp1} - V_T)$ was set at 0.3v. This gave $W_{p1,2} \approx 32\mu m$. The ratio of the conduction factors k'_n/k'_p in the process is about 2.6, so the widths of *n*4 and *n*5 were originally sized by dividing $W_{p1,2}$ by this ratio. The FET sizes of *p*3, *pt*1, and *pt*2, are proportional to the width of *p*1 because the capacitance related to the width of *p*1 includes the parasitics capacitances from these transistors. Because *p*3 is shared between nodes **a1** and **a2**, its size is dictated by equation (2.10), but FETs *pt*1 and *pt*2 must perform with the same characteristics as *p*3 in a single-ended manner.

The widths of *pt*1 and *pt*2 (thus, *p*3) can be specifically calculated by looking at the relationship of *pt*1 to *p*1. The authors of [6] noted that the current

generated in *p*1 when the portion of C_{in} which was due to the surrounding parasitics, C_p, was equivalent to the total gate capacitance of *p*1 (C_{gp1}), that current I_{dsp1}, would yield the optimum value for τ_{reg}. Using the relation $I_{dsp1} = \frac{C_{gp1}\Delta V}{\Delta t}$, with $\Delta V = 2.5v$ (this was an estimate for the change in voltage at **a1** or **a2** during regeneration) and $\Delta t = \tau_{reg} = 250ps$, I_{dsp1} is calculated to be $400\mu A$. If the saturation equation is used with this value for I_{dspt1}, and a $V_{gspt1} = 2.5v$, then the widths of *pt*1 and *pt*2 are found to be 9.2 μm.

FETs *n*1 and *n*2 were sized using the approximation $g_{mn1} \approx \sqrt{2k'I(W/L)}$, such that the input offset of the p-FET flip-flop pair was effectively reduced by a factor of at least $\frac{g_{mp1}}{g_{mn1}} \approx 2.5$. Both g_{mn1} and g_{mp1} are calculated in the following section.

2.2.2.1 Regeneration Time Constant

The gate-drain and gate-source capacitances were calculated for *pt*1, *p*1, and *p*3, using [4], as well as the g_m of devices *p*1 and *p*2. Using $C_{gs} = C_{gsovl} + \frac{2}{3}C_{ox}WL$, $C_{gd} = C_{gdovl} + \frac{1}{2}C_{ox}WL$ for *p*3 (non-sat at the start of regeneration), and $C_{gd} = C_{gdovl}$, the capacitances from the devices above are as follows:

*p*1,2 C_{gs} = 43.57fF, C_{gd} = 2.05fF

$pt1,2$ C_{gs} = 11.53fF, C_{gd} = 1.70fF Total C_{in} = 88.94fF

$p3$ C_{gs} = 10.35fF, C_{gd} = 1.70fF

$n1,2$ C_{gs} = 15.94fF, C_{gd} = 2.10fF

These capacitances are within ±15% of the values that SPICE reports. g_m for $p1,2$ is approximated as $g_{mp1} \approx \sqrt{2k'I(W/L)}$ using an I_d of 312 μA for a small input signal level at the slowest PVT corner, which yields 875 μS. For this case, SPICE reports a g_m of only 480 μS, so this is what is used. Additionally, C_{in} = 100fF is used to add 10% of margin to the calculation. Finally, $\tau_{reg} = \frac{C_{in}}{g_m} = \frac{100fF}{480\mu S} = 208ps$.

2.2.2.2 Simulation Results

A simulation plot of the comparator response is shown in section 2.3 where the DAC-Comparator interface is discussed. The comparator makes correct decisions in the same PVT corners listed for the DAC, when a 34mv differential signal is applied to the inputs. In the nominal case, the time elapsed from **ncmp** beginning to go true, to the time **q** and **qn** have reached 10% of their final value, is 1.8ns. The same measure for the SLOW, 4.75v supply, 85 deg. C case is 2.3ns.

The power consumption of the comparator is as follows:

Nominal case I_{AVDD} = 83.3 μA I_{VDD} = 954 μA (S-R latch)

$Power_{AVDD}$ = 0.396mw $Power_{VDD}$ = 4.77mw

Total power 5.17mw

2.3 DAC-COMPARATOR INTERFACE

The DAC-Comparator interface is shown in Figure 2.11. It is important to note that the nodes **sigp** and **sign** are subject to kickback from switching off *p*3 inside the comparator (Figure 2.10) when going into the regeneration phase. Transient immunity on the output nodes of the DAC then is very important for guarding the integrity of the output signal current during the comparator's reset-to-compare phase transition. This transient immunity is provided by the cascode output stage of the DAC (see Figure 2.5).

In order operate the feedback loop at high speed, the DAC output which is the input to the comparator at the interface nodes **sigp** and **sign**, requires a low impedence so that the time constant of the interface $\tau_{IF} = R_P \times C_{in}$, is small.

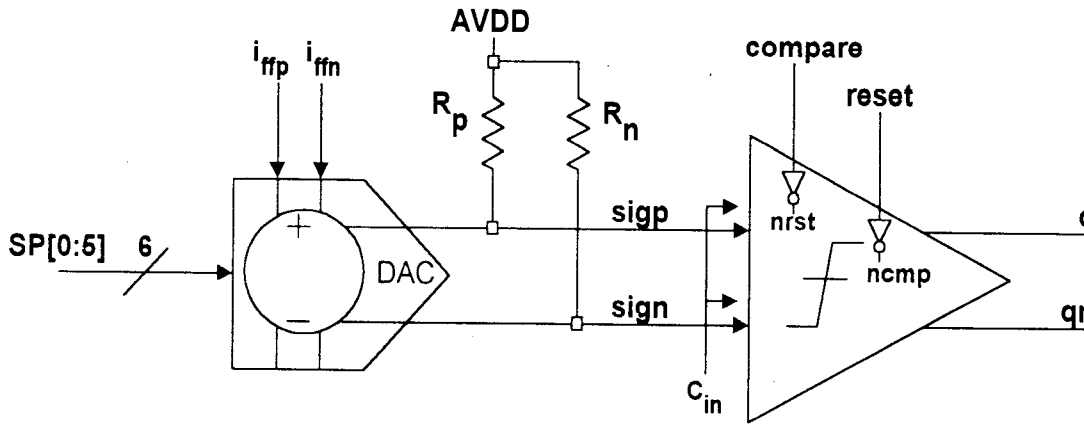


Figure 2.11: DAC-to-Comparator Interface

Basically, the interface should be a low impedence voltage source inputing to a high-impedence circuit (the comparator has a high-impedance, differential pair input), so that the signal is not attenuated or distorted. As mentioned above, within the comparator, the kickback voltage which occurs when the reset switch ($p3$) turns off, will be coupled back to **sigp** and **sign** through the gate-source parasitic capacitors of FETs $n1$ and $n2$ ($C_{gs} \approx 17fF$; see Figure 2.10). Having a low resistance at the interface nodes then will help to suppress the amplification of this transient. For the circuit shown in Figure 2.11, $R_P = 3420\Omega$ and C_{in} of the comparator is 17fF, which ensures the low impedance of the DAC output, and yields a small $\tau_{IF} = 58ps$.

2.3.1 Current-to-Voltage Converter

A resistor size must be chosen for the I-V converter. The maximum single-ended current signal swing from the DAC is from $950\mu A$ to $150\mu A$ with a common-mode current of $550\mu A$. Taking into account the need to leave enough headroom for the comparator's input devices by keeping the input a threshold above the input source node (**ins** in Figure 2.10), a value for R_p and and R_n were found as follows:

Minimum *Vin*(1.5v) - Maximum *Vin* (4.75v-low VDD) = 3.25v max se. signal swing, V_{max}. And,

$$R_p = \frac{V_{\max}}{I_{\max-se}} = \frac{3.25v}{950\mu A} = 3.42k\Omega$$

so the highest input voltage due to lowest signal current will be $V_{DD} - \left(I_{\min-se} \times R_p\right) = 4.49v = V_{in-\max}$, and the lowest input voltage due to the highest signal current will be $V_{DD} - \left(I_{\max-se} \times R_p\right) = 1.50v = V_{in-\min}$, which is for a low supply voltage. Thus, the signal voltage swing is as large as can be allowed, which gives more signal-to-noise immunity. This simple current-to-voltage conversion on a $10\mu A$ differential signal ideally results in 34mv difference at the comparator input, which is close to half the signal level needed to be outside the offset level.

2.3.2 Results

A simulation where a forward path signal is combined with the DAC code transitioning from -8 to +8 to result in a $10\mu A$ differential output, was done for different nominal and slow PVT corners. The results for a SLOW, 5.0v, 85 degree C case are shown in Figure 2.12.

Although it is not shown, the code change occurs from -8 to +8 at 14ns, and then back to +8 at 22ns. The simulations indicated that the resultant signal on **sigp** and **sign** was correct in output magnitude for each particular case according to the DAC's performance for that case. That is, each PVT case results in a different unit current and thus, a different output current from the ideal nominal case. However, the linearity is still preserved over each case. In

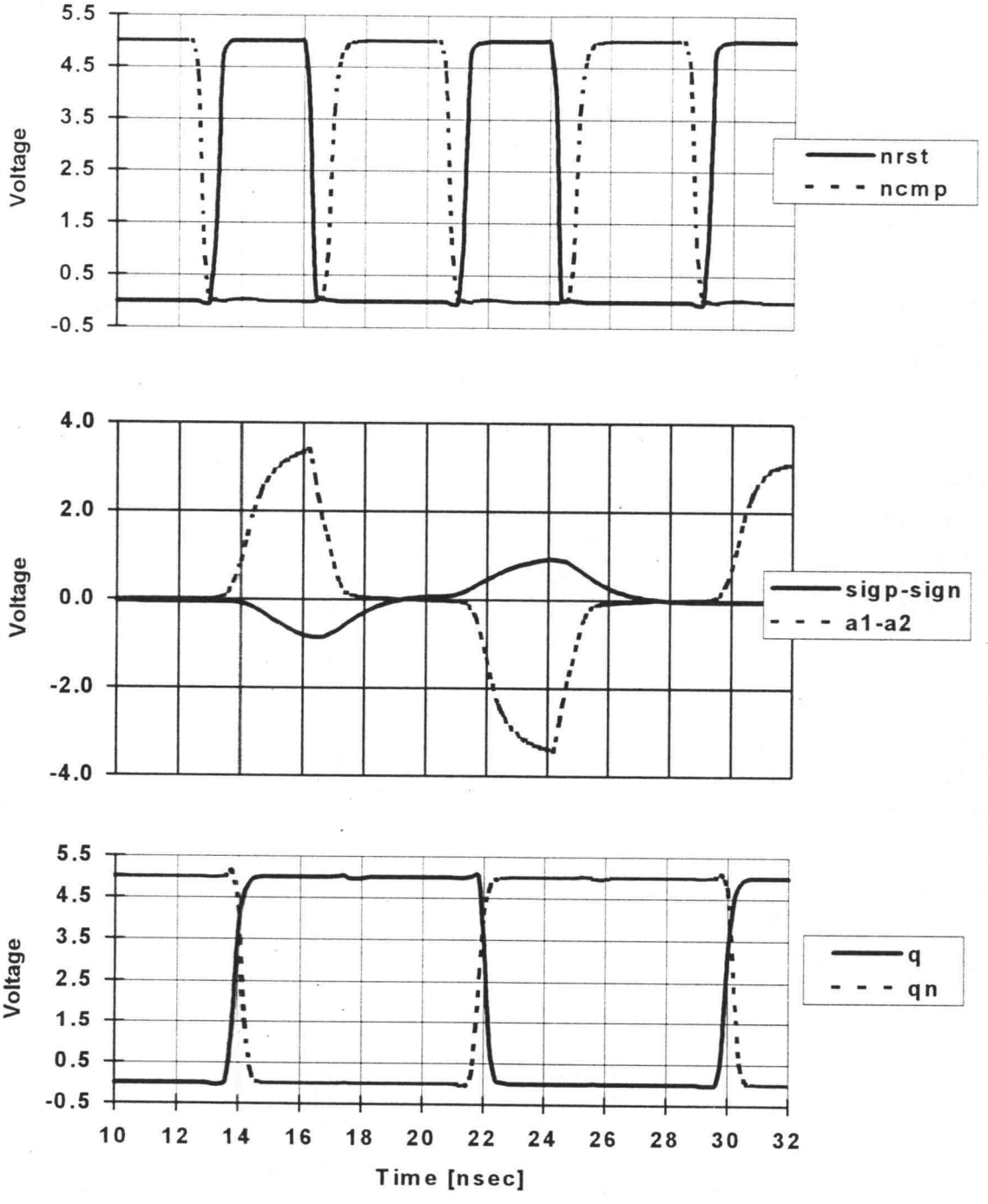


Figure 2.12: Simulation of DAC-Comparator interaction; sigp-sign is the differential interface voltage signal between the DAC and the comparator, with q and qn the comparator output, both shown in Figure 2.11; nrst, ncmp, and a1-a2 are signals internal to the comparator in Figure 2.10, with a1-a2 being the differential result during regeneration.

the slowest PVT corner, the output current of the DAC leads the settled voltage value on **sigp** and **sign** by .55ns.

The simulations also indicated that over the 15 PVT cases listed for the DAC, the DAC-comparator interface block was able to achieve a correct decision at the comparator's output latch for a 1/2 LSB differential signal on the interface node. The internal comparator nodes **a1** and **a2** shown in Figure 2.10, are the regeneration nodes of the comparator. These nodes show best the analog response of the comparator to a differential input, prior to amplification and the output latch. Nodes **a1** and **a2** are shown in Figure 2.12 with their response to the equivalent 1/2 LSB voltage input which is shown differentially as **sigp-sign**.

All simulations were run at 100MHz meaning that code changes in the DAC occurred within 10ns of one another. In Figure 2.12, the comparator control signals **ncmp** and **nrst** are shown rather than the system-level signals, **compare** and **reset**, as the internal signals are non-overlapping and it is easier to view their low-true periods. Inside the comparator, **ncmp** and **nrst** are cycled at maximum periods of 3.5ns and 2.5ns respectively, as is shown in the top graph of **ncmp** and **nrst** (in Figure 2.12).

The overall power consumption of the interface block is as follows:

Nominal case	I_{AVDD} = 1.38mA	I_{VDD} = 4.61mA
	$Power_{AVDD}$ = 6.90mw	$Power_{VDD}$ = 23.1mw
Total power	30.0mw	

3. CONCLUSIONS

The DAC, analog summation, and comparator components of the DFE feedback loop were successfully designed and schematically simulated to achieve >100Mhz performance in most cases, to the accurracy of 1/2 LSB of the designed full-scale range of the DAC (1.28mA differential).

The DAC and analog summation design were the most thoroughly investigated of the three blocks. Many issues were revealed in the DAC such as the core device lengths were found to be marginal to meet the accuracy specification of 1/2 LSB in terms of current matching. Also, the voltage switching circuit which provided the core switches with a reduced gate voltage range was found to consume large amounts of power due to static current. The nonlinearity of the DAC is within the goal of < 1/2 LSB, but in some of the more severe PVT cases, there is not much margin. The signal summation point operates well in simulation, with very little disturbance due to code changes, as the core switches' gate capacitance was kept to a minimum and the summation point was, by design, a low impedence node.

The goal of achieving a small regeneration time constant was reached and the comparator makes correct decisions in many severe PVT cases, at speeds greater than 200MHz.

The designed components were interfaced and clocked at 100Mhz to partially simulate a DFE loop and to determine the timing relationships between the control signals of the blocks. These simulations produced a timing diagram

for the DAC control codeword, and the reset and compare control signals of the comparator, that allowed the partial loop to interact correctly.

The power goal was not met. It was anticipated that the two blocks plus the interface current from the resistors would consume no more than 2mA total, for a power total of 10mw. The SWLEV circuits consume large amounts of static power and a different approach must be taken to reduce the gate voltage levels for the switches inside the DAC. The power consumption of the comparator was minimal at just over 5mW. The partial loop interface used nominally 30mW, with 75% of the power being used by the DAC's voltage switching blocks.

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