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Nilakantan Seshan for the degree of Master of Science in

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Kartikeya Mayaram

The design of two 2.4GHz CMOS LC balanced oscillators in the $0.25\mu m$ National BiCMOS process for Bluetooth specifications is presented. These oscillators achieve low phase noise with low power consumption. At a frequency offset of 500KHz from the 2.11GHz carrier, the measured phase noise is -101.9dBc/Hz for the NMOS oscillator with a power dissipation of 12.5mW. The complementary oscillator has a phase noise of -103.6dBc/Hz at 500KHz offset from the 2.19GHz carrier and a power disipation of 6.25mW from a 2.5V power supply. A wide tuning range of 16% is obtained by means of a PMOS varactor in conjunction with an array of switched capacitors.

Design of Low Power 2.4GHz CMOS LC Balanced Oscillators with Low Phase Noise and Large Tuning Range

by

Nilakantan Seshan

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DESIGN OF LOW POWER 2.4GHz CMOS LC BALANCED OSCILLATORS WITH LOW PHASE NOISE AND LARGE TUNING RANGE

1. INTRODUCTION

The past decade has seen tremendous growth in wireless communication. The reduction in the channel spacing and demand for low power, low cost solutions has made wireless system design even more challenging [1], [28]. VCOs are critical blocks of frequency synthesizers and phase-locked loops (PLLs) which are key components in wireless systems. Fig. 1.1 shows the block diagram of a phase-locked loop. It consists of a phase comparator or a phase detector followed by a loop filter and a VCO in a feedback loop. The phase detector compares the phases of the input and the output and generates an error signal. The loop filter is a lowpass filter which filters out the high frequency components and presents a dc level to the oscillator. The output of the filter is the control voltage to the VCO which varies the oscillation frequency until the loop is locked and the phases are aligned. The frequency divider may or may not be required depending on the application. In case the input frequency should be multiplied by a factor M, a frequency divider ($\div M$) can be used in the feedback loop as shown in Fig. 1.1.

Two important considerations in VCO designs are phase noise and tuning range. The phase noise of the system outside the loop bandwidth of the PLL is

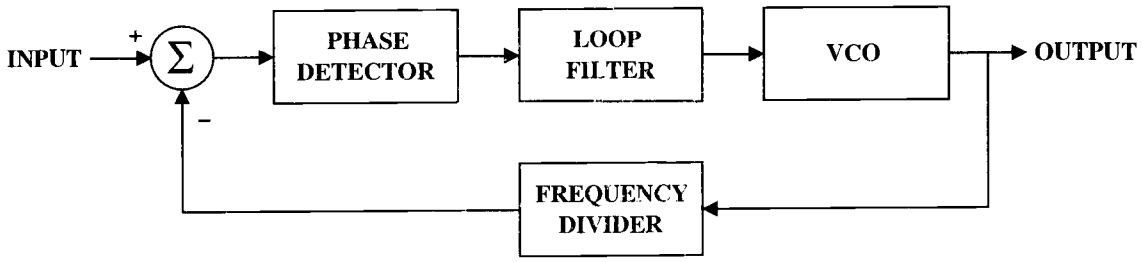


Figure 1.1. The block diagram of a phase-locked loop.

determined by the VCO phase noise. Hence, it is imperative to minimize the phase noise of the VCO. In order for the PLL to lock-on to the reference frequency, a high tuning range is desired. At the same time, it is necessary to maintain a small VCO gain to prevent amplification of any noise on the control node and deterioration of phase noise [6].

A significant amount of work has been done in the past in the area of VCO design [2] - [6], [20] - [33]. However, the competitive nature of the wireless market is forcing designers to explore new techniques to reduce phase noise and improve tuning range. The lack of accurate RF models for MOSFETs, inductors and varactors adds to the difficulties of RF design. Another obstacle to faster and better designs is the lack of simulators capable of predicting phase noise. Presently SpectreRF, Agilent EEsof ADS and EldoRF are the only commercially available tools to simulate phase noise. In [3], Hajimiri and Lee have presented a linear time-variant model to predict phase noise. Although the model provides insight into the conversion of device noise into phase noise, its automated implementation requires significant effort. All the above mentioned factors have added to the complexity of RF design and the design

of VCOs with low phase noise and high tuning range still poses a challenge for circuit designers.

In this thesis, two low power CMOS VCO designs targeted for Bluetooth specifications are presented. The Bluetooth standard is gaining acceptance around the world for personal area networks. Both these oscillators provide low phase noise with low power consumption and offer a wide tuning range. These two oscillators have been fabricated in the $0.25\mu m$ National BiCMOS process.

The emphasis of this research has been to reduce the power consumption of the oscillators while maintaining good phase noise performance. Various techniques for reducing phase noise have been studied and implemented. The design has been done completely in CMOS and the use of a PMOS transistor as a varactor has been studied. The thesis is organized as follows. A brief introduction to oscillators and phase noise is provided in Section 2. Sections 3 and 4 describe the tank components, namely, on-chip spiral inductors and varactors, respectively. Section 5 presents a detailed analysis of phase noise in oscillators validated by simulations. The design of the oscillators and the buffer is explained in Section 6, followed by the measurement results in Section 7. Conclusions and future work are presented in Section 8.

2. OSCILLATORS AND PHASE NOISE

2.1. Introduction to Oscillators

Oscillators are closed loop systems which employ a positive feedback loop. Oscillators can be classified as resonatorless oscillators or ones that have a resonator. Examples of resonatorless oscillators are ring oscillators and relaxation oscillators, whereas LC oscillators fall in the latter category. Resonatorless oscillators are not popular in RF design due to their low quality factor and the presence of many noisy active and passive devices in the signal path. Therefore LC oscillators are more suitable for low noise applications [36]. At present LC oscillators are being designed for several GHz and higher. In order to understand the principle of operation of the oscillator, consider the feedback system shown in Fig. 2.1.

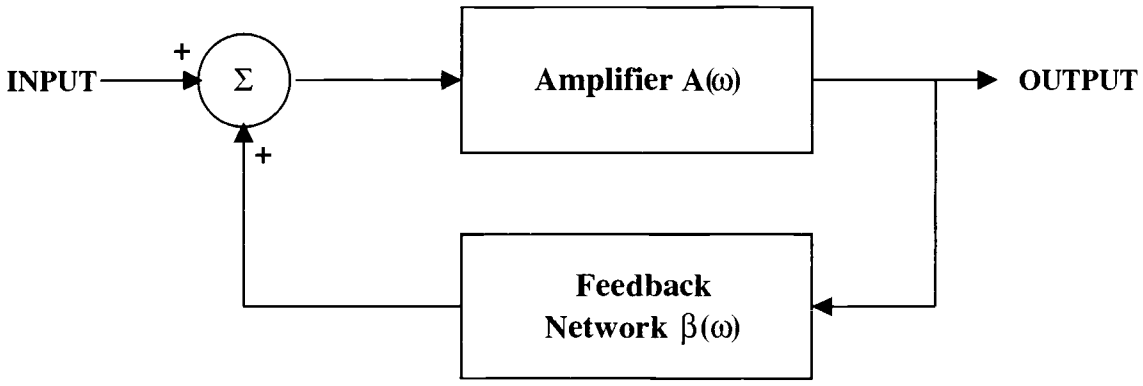


Figure 2.1. The block diagram of an oscillator. The positive-feedback loop consists of an amplifier and a frequency-selective network.

The closed loop gain of the system is given by

$$A_f(s) = \frac{A(s)}{1 - A(s)\beta(s)} \tag{2.1}$$

where $A(s)$ represents the gain of the amplifier and $\beta(s)$ is the gain of the feedback network. The loop gain of the circuit is given by

$$L(s) = A(s)\beta(s). \tag{2.2}$$

If at a specific frequency ω_0 the loop gain $L(s)$ is equal to unity, then the closed loop gain from Eq. (2.1) will be infinite. This implies that at that specific frequency ω_0, the output will be finite even if the input is zero. Thus the condition for oscillation at a frequency of ω_0, called the *Barkhausen criterion*, is given by

$$L(j\omega_0) = A(j\omega_0)\beta(j\omega_0) = 1. \tag{2.3}$$

This provides the condition for oscillations at ω_0: the magnitude of the loop gain should be unity and the phase of the loop gain must be zero [34].

To apply the Barkhausen criterion to a circuit, consider the oscillator circuit shown in Fig. 2.2. The gain from the gate of M_{N1} to its drain is $-g_{m1}R_P$, where g_m is the transconductance of the transistor and R_P is the tank resistance at resonance. Similarly, the gain from the gate of M_{N2} to its drain is $-g_{m2}R_P$. The loop gain is then $g_{m1}R_P g_{m2}R_P$, with a phase of 360^0. Thus the condition required to start the oscillations is given by

$$g_{m1}R_P g_{m2}R_P \geq 1. \tag{2.4}$$

If the above condition is satisfied, the circuit will amplify any small noise present in the circuit and steady oscillations would be obtained.

An alternative perspective of looking at oscillators is by considering the negative resistance. The lossy tank can be modeled as an inductor L, capacitor C and

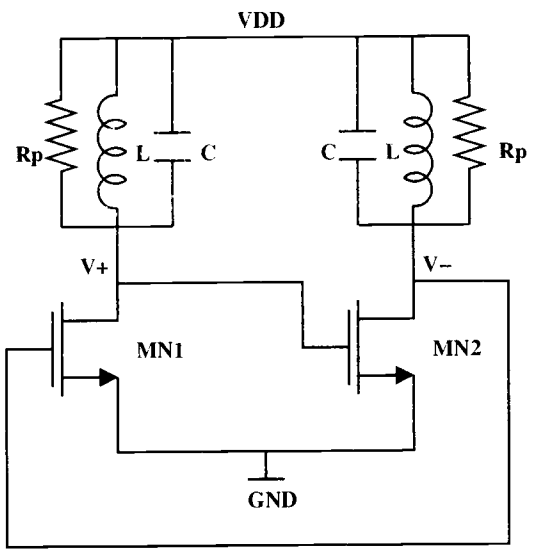


Figure 2.2. Circuit to illustrate how the Barkhausen criterion is applied to oscillators.

resistor R_P in parallel. If a current impulse is injected into the tank, the voltage waveform is a decaying sinusoid due to the resistive losses as shown in Fig. 2.3. But if a negative resistance is added to the circuit to cancel the losses due to the resistance R_P, the decaying behavior disappears and the resulting waveform is shown in Fig. 2.3. Thus, nullifying the resistance in the tank guarantees steady oscillations.

For the circuit shown in Fig. 2.4, the resistance looking into the tank from the differential output terminals is $2R_P$. The resistance looking into the cross-coupled devices is $-2/g_m$, assuming a perfectly symmetrical circuit. Since both the resistances are in parallel, the effective resistance of the circuit is

$$R_T = \frac{-2/g_m 2R_P}{2R_P - 2/g_m}. \tag{2.5}$$

If the resistance R_T is negative, there won't be any losses in the circuit and oscillations will be sustained. Therefore, for stable oscillations, we require

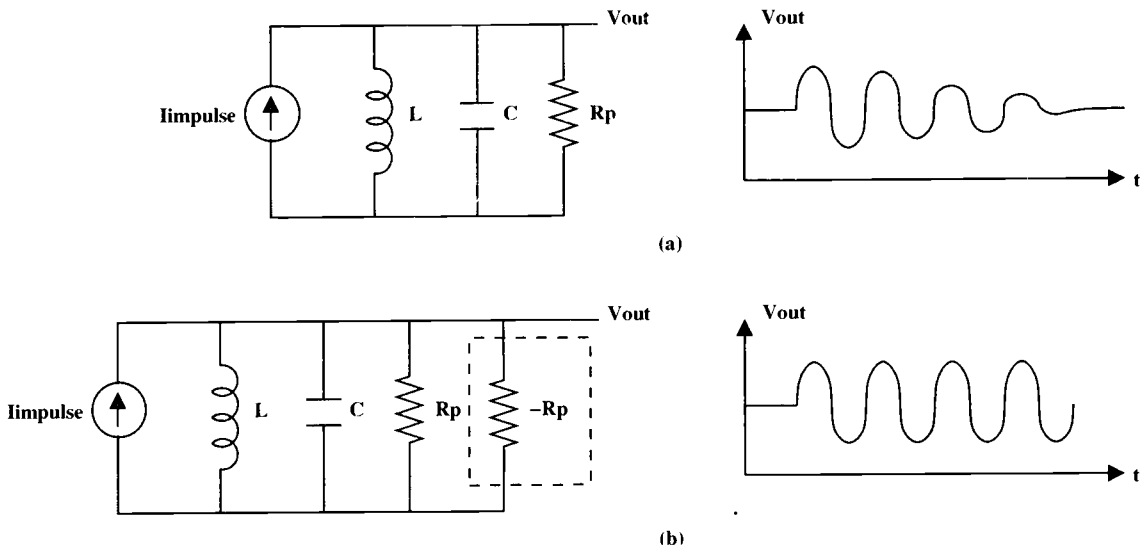


Figure 2.3. (a) Tank circuit shows decaying response due to circuit losses. (b) With the addition of a negative resistance, oscillations can be stabilized.

$$2R_P - 2/g_m \geq 0 \Rightarrow g_m R_P \geq 1. \tag{2.6}$$

As seen from (2.4) and (2.6), the start-up loop gain conditions are different. Therefore it is necessary to understand the context in which each can be used. If the circuit has the sources of the cross-coupled devices grounded, as in Fig. 2.2, (2.4) should be used. On the other hand, if the circuit has the sources of the cross-coupled devices connected to some current source, as shown in Fig. 2.4, (2.6) should be used.

2.2. Oscillator Topologies

There are various types of oscillators employing an LC tank including Colpitts oscillators, Hartleys oscillators, transformer coupled oscillators or LC balanced oscillators. All these oscillators use a LC tank which determines the frequency of

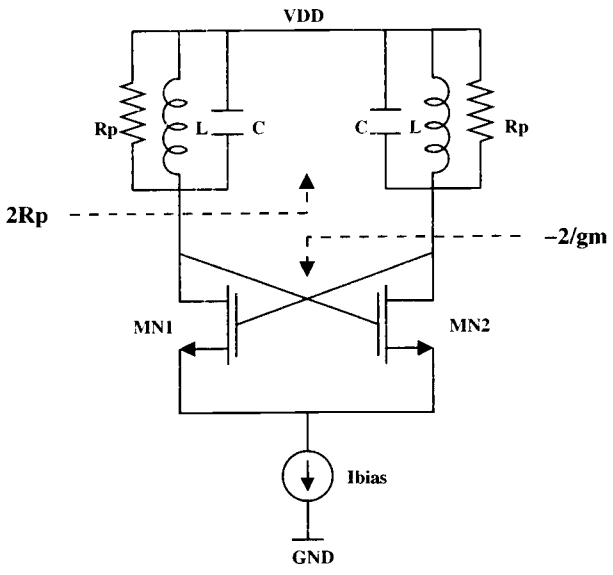


Figure 2.4. Circuit demonstrating the condition for start-up using the negative resistance concept.

oscillation. The tank in these oscillators provides considerable attenuation to signals at frequencies other than the oscillation frequency. Amongst all the oscillators mentioned, the LC balanced oscillators are widely employed. Consequently the focus of this research is on LC balanced oscillators. Since differential structures provide better immunity from external sources of noise, the LC balanced oscillators were designed for differential operation.

LC balanced oscillators comprise of either cross-coupled NMOS or PMOS transistors or both. The schematic of the oscillators with just NMOS or PMOS transistors is shown in Figs. 2.5-2.6. The cross-coupled transistors provide the necessary start-up loop gain for oscillations to build up. Since the g_m of the PMOS transistors is smaller than that of the NMOS transistors for identical currents, the

size of the PMOS devices for the same start-up loop gain would be much larger than the NMOS devices. This would cause the tank capacitance to vary with temperature because of the large temperature dependent capacitances of the PMOS transistors. Thus the NMOS cross-coupled LC balanced oscillator is a better choice than the PMOS cross-coupled one.

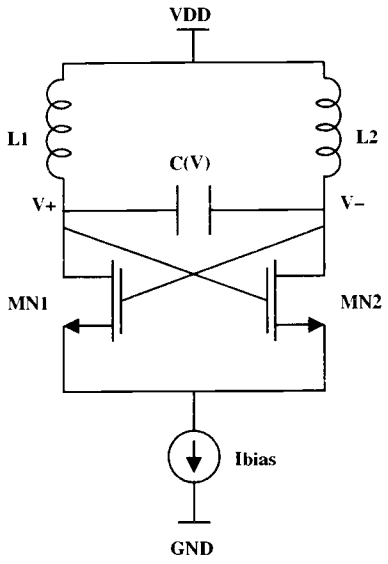


Figure 2.5. NMOS oscillator.

A combination of the PMOS and NMOS cross-coupled pairs gives the complementary oscillator topology. The two cross-coupled stages in the complementary oscillator provide the necessary start-up loop gain for smaller values of current as compared to the ones with just the NMOS or PMOS cross-coupled pair. Fig. 2.7 shows the complementary oscillator circuit.

The biasing current source is called the tail current source. This tail current source could be implemented as either PMOS or NMOS current mirrors, although

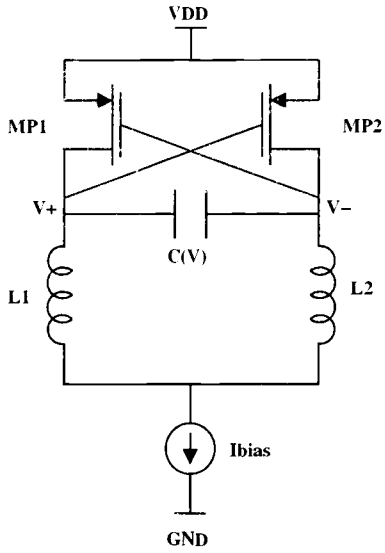


Figure 2.6. PMOS oscillator.

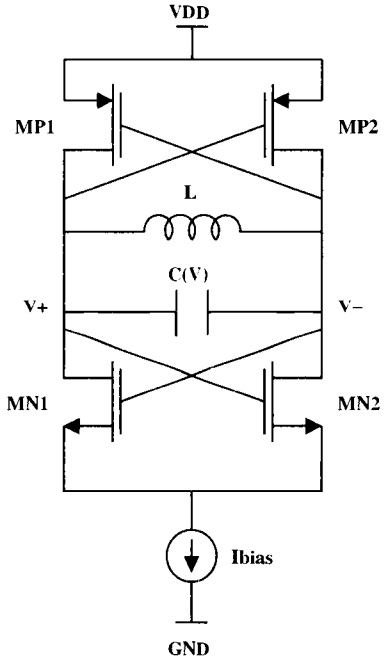


Figure 2.7. Complementary oscillator.

NMOS is implied in Figs. 2.5-2.7. Since PMOS transistors have lower flicker noise as compared to NMOS transistors [5], the PMOS tail current source is preferred.

For completeness, the oscillator circuit without the tail current source is shown in Fig. 2.8. The oscillators described earlier were all current biased oscillators. For this oscillator, the supply voltage needs to be adjusted for the desired oscillator current, accordingly it is a voltage biased oscillator. The disadvantages of this oscillator are that it consumes more current as compared to the current biased oscillators and any supply voltage variation may cause the oscillation frequency to deviate from the desired value.

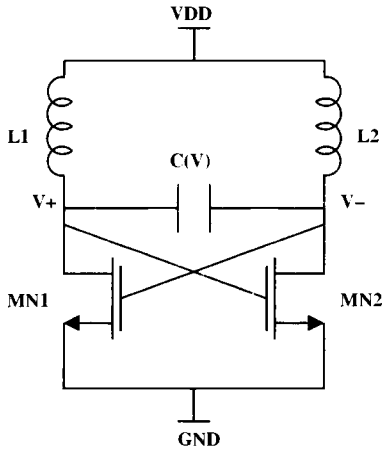


Figure 2.8. Voltage biased oscillator.

The other oscillator circuits such as Colpitts, Hartleys etc., have a different tank configuration and these are not included here since the focus is on LC balanced oscillators.

The start-up loop gain ensures that any noise in the circuit gets amplified and the output voltage begins to increase due to the positive feedback. As the

signal continues to increase, the nonlinearity of the cross-coupled pair prevents the amplitude from rising indefinitely. Due to its bandpass characteristics, the LC tank filters out signals at frequencies other than the frequency at which the tank resonates. Therefore only the oscillation frequency is present at the oscillator output. The oscillation frequency for all the oscillators discussed is given by

$$f_{OSC} = \frac{1}{2\pi\sqrt{LC}} \tag{2.7}$$

where L is the tank inductance and C is the tank capacitance which includes the parasitic capacitance of the cross-coupled pair.

The next two sections present some of the performance metrics of an oscillator.

2.3. Phase Noise

Phase noise is an important performance specification for VCOs [2], [3], [35]. Phase noise can be defined as the short term random frequency fluctuations. To understand what this means, consider the frequency spectrum of an ideal oscillator shown in Fig. 2.9. For an ideal oscillator oscillating at frequency ω_0, the spectrum is an impulse at ω_0. An actual oscillator has a skirt around ω_0 as illustrated in Fig. 2.10. Since this skirt around the carrier is a result of the various noise sources in the oscillator, it is called the phase noise sideband. The oscillator spectrum also has harmonics at $2\omega_0$, $3\omega_0$,..., etc. as shown in Fig. 2.10.

The significance of phase noise can be understood by considering an example of a receiver [37]. The mixer downconverts the RF signal into the signal at IF by means of a local oscillator (LO). If the desired RF signal is weak, but has a large adjacent channel signal, then in the absence of LO phase noise, both the signals are downconverted to IF without any interference. But if the LO has phase

Figure 2.9. Power spectrum of an ideal oscillator.

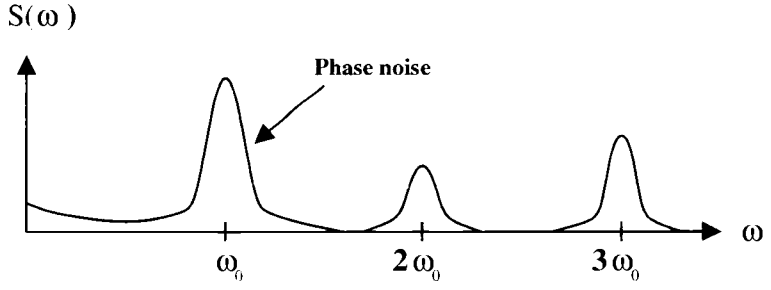


Figure 2.10. Power spectrum of an actual oscillator.

noise, the downconverted adjacent channel signal may interfere with the desired downconverted signal as seen in Fig. 2.11. This adjacent channel interference is highly undesirable and it may completely mask out the desired signal if the interferer is large. Hence phase noise specifications are very stringent [25], [28].

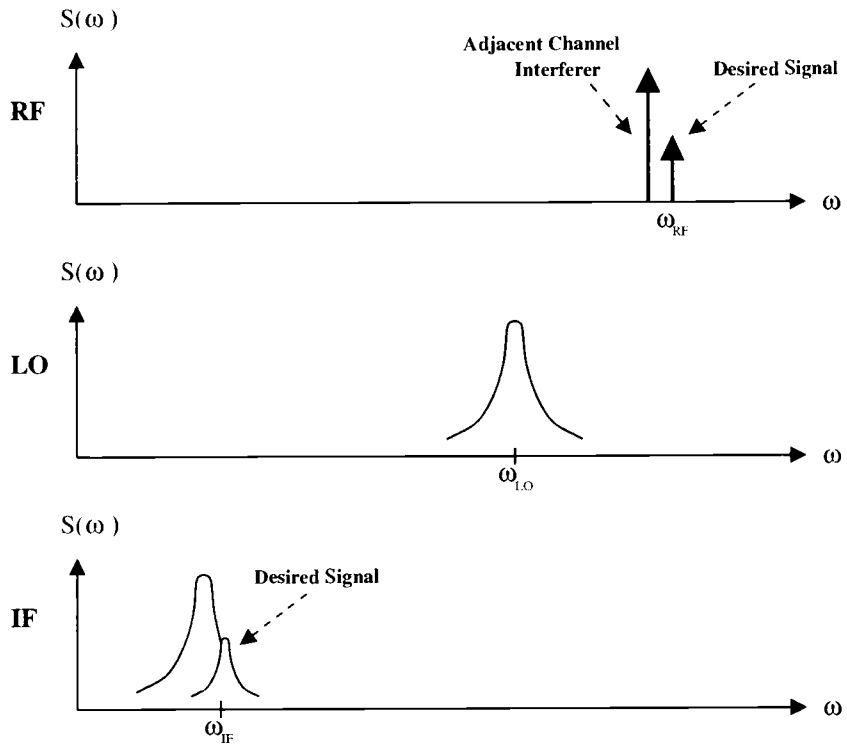


Figure 2.11. Effect of a strong adjacent channel interferer in the presence of LO phase noise.

Phase noise is characterized in terms of single sideband noise spectral density. Single sideband phase noise is given by

$$L\{\Delta\omega\} = 10log_{10}(\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}) \tag{2.8}$$

where $P_{carrier}$ is the power at the oscillator fundamental frequency and $P_{sideband}(\omega_0 + \Delta\omega, 1Hz)$ represents the single sideband noise power measured in a one Hertz band-

width at a frequency offset of $\Delta\omega$ from the carrier. This is illustrated in Fig. 2.12 along with the magnified portion of the phase noise curve. It can be observed that the plot of $L(\Delta\omega)$ has three distinct regions: $1/f^3$ (-30 dB/decade) region due to the flicker noise, $1/f^2$ (-20 dB/decade) region due to thermal noise and the flat region due to the noise floor. The mechanisms responsible for these features are explained in detail in [3], [4], [35].

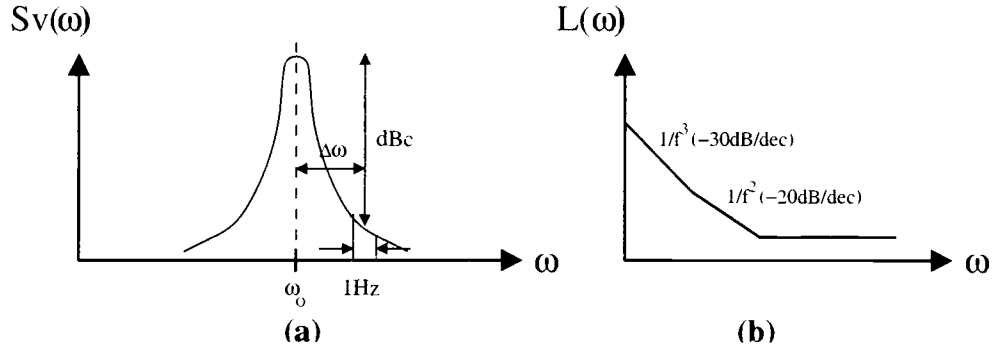


Figure 2.12. Phase noise of an oscillator (a) Characterization of phase noise. (b) Various regions in a typical phase noise curve.

Another way of quantifying the same phenomenon in the time domain rather than the frequency domain is timing jitter or clock jitter. Jitter represents the random fluctuations in the transition points of a periodic waveform. This definition is mostly used when ring oscillators are considered. Since the focus of this work is on wireless applications, phase noise is a more suitable performance metric.

2.4. Tunability of Oscillators

All oscillators which are used in phase-locked loops (PLLs) are designed to be tunable. The reason for this is that the free-running oscillation frequency of the

tank would be different from the reference frequency. Thus in order to synchronize the oscillator frequency with the reference frequency, the oscillator frequency needs to be adjustable. Most applications specify the tuning range in absolute units such as 200MHz or in terms of percentage of the center frequency such as 10% tuning.

Since the frequency of oscillation is determined by the inductor and the capacitance in the tank, changing any one of these varies the oscillation frequency. The variation in frequency is obtained by varying the control voltage which changes the tank inductance or capacitance, consequently the name voltage controlled oscillators. The rate of change of oscillation frequency with respect to the control voltage is defined as the VCO gain(K_{VCO}) and is given by the following expression

$$K_{VCO} = \frac{df_{OSC}}{dV_C} \tag{2.9}$$

where f_{OSC} is the oscillation frequency and V_C is the control voltage. A larger K_{VCO} implies a larger variation in the frequency for a given voltage change, i.e., a large tuning range. However, a larger gain will amplify any noise present on the control node, resulting in the degradation of the phase noise performance of the oscillator. One way of overcoming this problem is explained in Section 4.4.

2.4.1. *Inductively Tuned VCOs*

As the name suggests, inductively tuned VCOs are tuned by varying the tank inductance by means of a control voltage. This can be done either by selecting a different inductor for the tank from a bank of inductors for different control voltages [6], [7] or by switching ON/OFF an inductor in the circuit for a certain time interval depending on the control voltage [8].

Fig. 2.13 shows the schematic of an inductively tuned oscillator employing the latter method. The circuit has two inductors in parallel. One of the inductors

is switched ON or OFF depending on the control voltage applied to the gate of the switching transistors M_{S1} and M_{S2}. When the control voltage is 0 volts, the switching transistors are OFF, and the frequency of oscillation is determined by the inductor L_1 and is the minimum value. On the other hand, when V_{DD} is applied to the gate, both the inductors are in parallel and the frequency of oscillation is the largest. Between these two extremes, the effective inductance is L_1 in parallel with a fraction of L_2, where the fraction is proportional to the time duration the transistors are ON in one cycle.

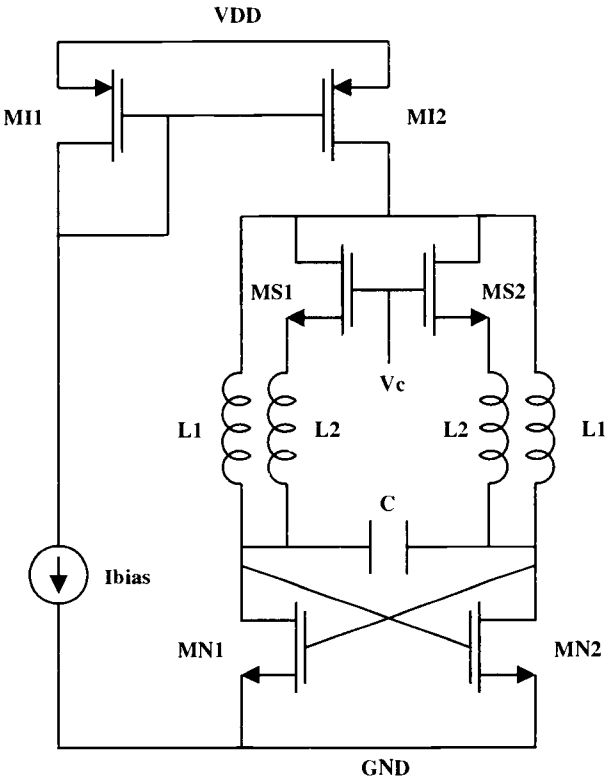


Figure 2.13. Schematic of the inductively tuned oscillator.

The tuning characteristics for the inductively tuned VCO are shown in Fig. 2.14. The current consumption of the VCO was 4.4mA from a 2.5V power supply. The highest frequency of oscillation is 2.584GHz whereas the lowest frequency of oscillation is 2.143GHz giving a tuning range of 441MHz which corresponds to 18.375% tuning. This oscillator has a K_{VCO} of around 180MHz/V. This value of K_{VCO} is very large making this oscillator very susceptible to noise on the control node.

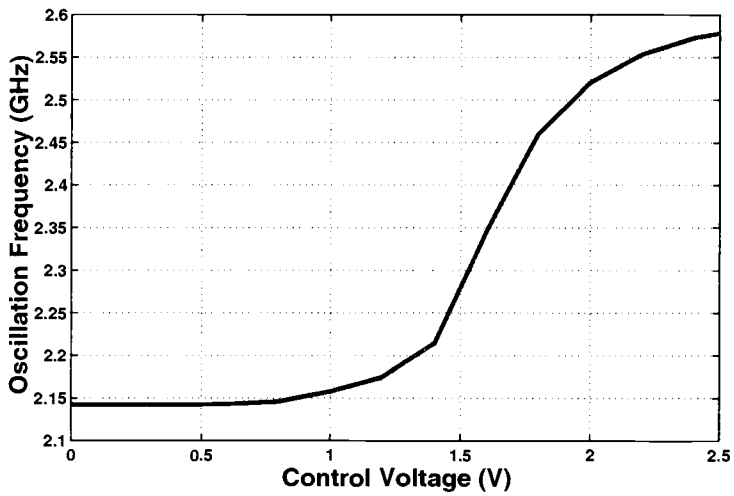


Figure 2.14. Tuning characteristics of the inductively tuned oscillator.

2.4.2. *Capacitively Tuned VCOs*

Another means of tuning the oscillator is by using voltage dependent capacitances in the LC tank. Junction diodes and MOS varactors are most commonly used for tuned VCOs. These devices show a variation of capacitance with voltage.

The advantage of capacitively tuned VCOs over inductively tuned ones is that they occupy less die area and have better phase noise performance [8]. The oscillators may employ just a single varactor when the VCO gain is small or a varactor in combination with switchable capacitors when the gain is large. A detailed description of the different types of varactors is given in Section 4.

3. INDUCTORS

3.1. Introduction

Inductors form an integral part of the resonating tank used in LC oscillators. Both off-chip and on-chip inductors are used in oscillators. Because of the present trend of designing a system-on-a-chip, on-chip inductors are preferred. This also reduces the losses due to interconnects and sensitivity to noise when off-chip inductors are used. Although inductors consume a large amount of die-area, their size decreases with higher oscillation frequencies. Thus on-chip inductors are popular in RF LNAs and oscillators.

On-chip spiral inductors are widely used when inductance values smaller than 10nH are desired [35]. These inductors are capable of providing quality factors up to 15. The capacitance to the substrate determines the self-resonating frequency of the inductor. The self-resonance frequency limits the use of the inductor beyond a certain frequency. For higher quality factors and larger self-resonance frequencies, bond-wire inductors are commonly used.

Since inductors determine the oscillation frequency and also influence the phase noise, an accurate prediction of both requires good inductor models. Modeling of passive devices still poses a difficult problem to circuit designers. Accurate modeling of inductors requires an in-depth understanding of electromagnetism and inductor parasitics which become very important at RF [9], [10]. The accuracy with which the frequency of oscillation or the phase-noise of the oscillator can be predicted depends directly on the accuracy of the inductor model. ASITIC (Analysis and simulation of Inductors and Transformers for ICs) [39] and Agilent EEsof ADS-MOMENTUM are two software tools available for characterizing inductors.

ASITIC is an interactive tool capable of simulating spiral on-chip inductors in the IC environment. Depending on the dimensions of the inductor provided by the user, ASITIC generates a pi model for the inductor which can be included in simulations.

3.2. Simple Inductors

The layout and the physical model of a spiral inductor obtained from ASITIC are shown in Figs. 3.1 and 3.2, respectively. The dashed lines represent the components which are not modeled by ASITIC. In Fig. 3.2, L_S represents the series inductance and R_S represents the series resistance of the spiral and the underpass. The series resistance symbolizes the energy loss due to the skin effect at RF in the spiral, as well as due to the induced eddy currents in any conducting media close to the inductor such as the substrate [10]. The oxide capacitance between the spiral and the silicon substrate is modeled by C_{P1} and C_{P2}. The silicon substrate can be modeled by a resistances R_{SUB} or by a parallel combination of a resistance R_{SUB} and a capacitance C_{SUB}. The capacitance C_W between the input and output ports is due to the coupling between the underpass and the spiral.

The quality of an inductor is determined by its quality factor Q which is defined as

$$Q = \omega \frac{Energy\ stored}{Average\ power\ dissipated}. \tag{3.1}$$

For an inductor, the magnetic energy is of interest. The parasitic capacitances are responsible for the electric energy which is counter productive. Thus the energy stored represents the difference in the magnetic and the electric energy. The average power dissipated is the resistive loss in the inductor. For this reason, the

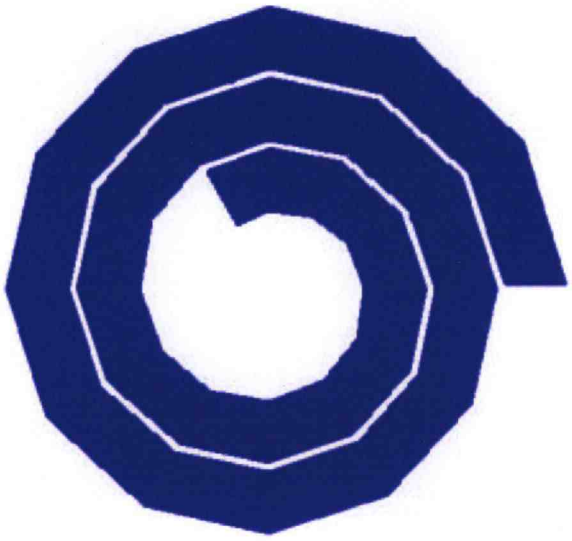


Figure 3.1. Layout of an on-chip spiral inductor.

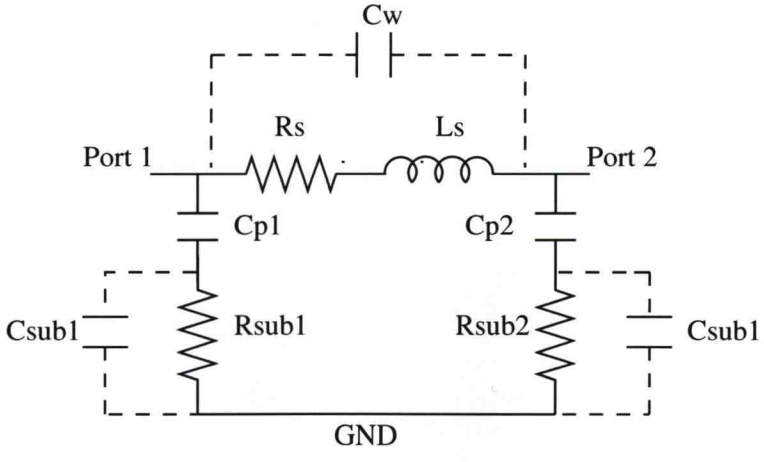


Figure 3.2. Inductor model provided by ASITIC. The components shown by dashed lines are included in more accurate inductor models.

key to obtaining high Q inductors is to lower the series resistance of the inductor and reduce the parasitics to the substrate.

Another important factor determining the inductor performance is the self-resonance frequency. It is the frequency at which the peak magnetic and electric energies are equal. Consequently the quality factor of the inductor reduces to zero at the self-resonance frequency. Beyond the self-resonance frequency, no net magnetic energy is available from the inductor. Therefore the self-resonance frequency places a limit on the maximum useful frequency. Since this frequency is determined by the series inductance and the parasitic capacitances, it can be increased by reducing the parasitic capacitances.

In most technologies, the top most metal layer has the lowest sheet resistance. Therefore inductors are mostly laid out on the top most metal layer. This reduces the series resistance of the inductor. As an example, in the $0.35\mu m$ TSMC 4 metal layer process, the top most metal layer has a sheet resistance of $51\text{m}\Omega/\square$ whereas the lower 3 layers have a sheet resistance of 80-$83\text{m}\Omega/\square$. Also the distance of the top metal layer from the substrate is larger giving smaller parasitic capacitances. Both of these are favorable from the view point of quality factor and the self-resonance frequency.

3.3. Stacked Inductors

It has been shown in [12] that stacking improves the quality factor of the inductors. Stacking metal layers means shorting adjacent metal layers with vias so that the effective thickness of the inductor increases as demonstrated in Fig. 3.3. This causes the series resistance of the inductor to reduce. Although this means the spacing between the inductor and the substrate decreases, causing an increase in the

parasitic capacitances, this is overshadowed by the decrease in the series resistance of the inductor, thereby increasing the quality factor. But stacking more and more layers eventually causes this benefit to diminish. Accordingly the number of layers to be stacked should be cautiously chosen.

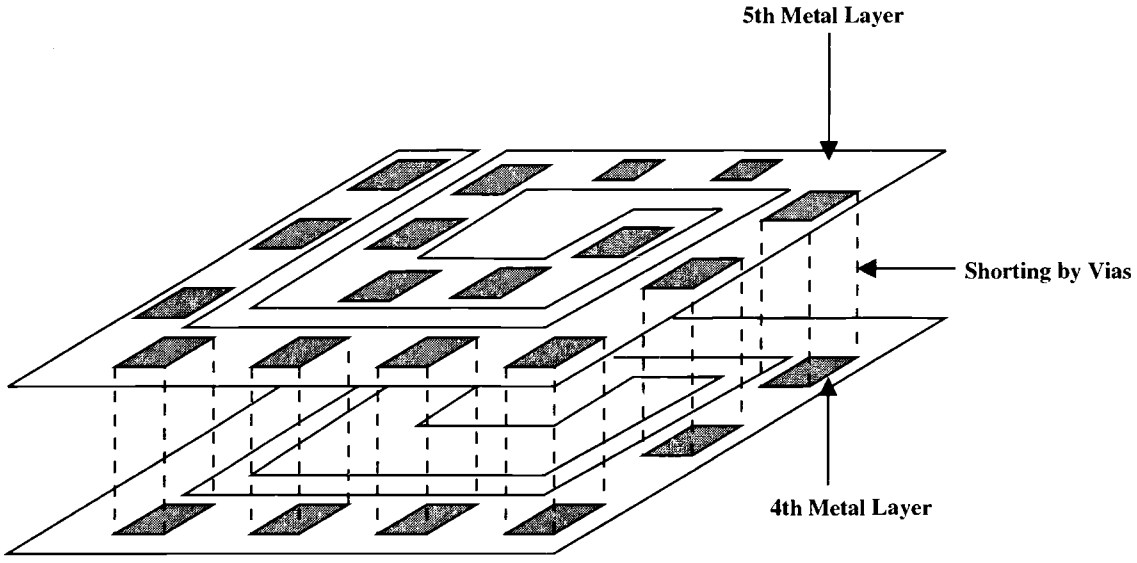


Figure 3.3. Stacking metal layers to improve the inductor quality factor. The 5th and 4th metal layers have been stacked.

3.4. Symmetric Spiral Inductors

Since most oscillators designed are differential, differential operation of inductors is gaining importance. As shown in [11] and Section 3.5, differential operation of inductors shows better quality factor than single-ended operation. The layout of a symmetric center-tapped inductor, which can be used in such cases, is shown in Fig. 3.4. The difference between the simple inductor and the symmetric spiral is the absence of the underpass at one end of the symmetric spiral. When the symmetric

spiral is connected to the two differential terminals of the circuit, the differential outputs see the same inductance. Also the presence of the center-tap makes it possible to connect the center terminal to the power supply. Symmetric spiral inductors can be stacked.

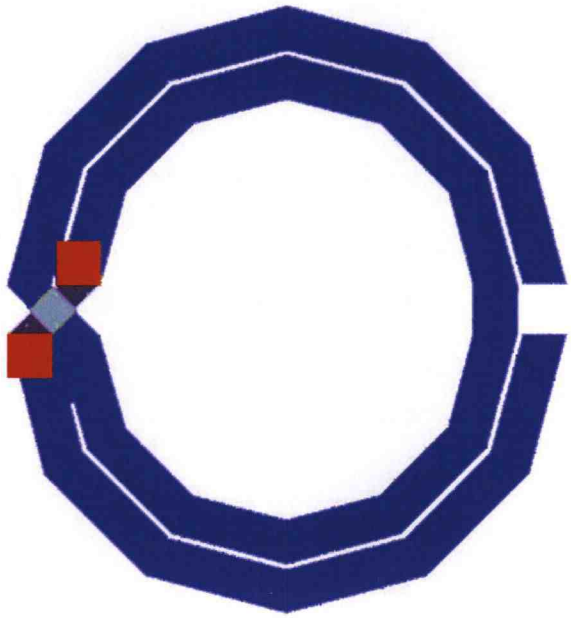


Figure 3.4. Layout of a symmetric spiral inductor.

3.5. Comparison of Inductors

This section compares three different inductors, all of which have been modeled using ASITIC, for the $0.35\mu m$ TSMC 4 metal layer process. These include a 1nH simple inductor, a 2nH simple inductor and a 2nH symmetrical spiral inductor. Only the top most metal layer was used for these inductors. The values of the inductance and the quality factors is tabulated in Table 3.1. Q_S represents the

single-ended quality factor of the inductors, whereas Q_D is the differential quality factor of the inductors, both of which are given by ASITIC.

Inductor	*Inductance*	*Series Resistance*	Q_S	Q_D
1nH Simple	1nH	2.23Ω	6.327	6.557
2nH Simple	1.98nH	3.34Ω	6.538	7.654
2nH Symmetrical	2nH	3.41Ω	6.38	7.457

Table 3.1. Comparison of inductors.

It can be observed from Table 3.1 that the differential quality factors are larger than the single-ended quality factors. This can be explained by considering Figs. 3.5-3.6 [13]. Fig. 3.5 shows the equivalent circuit of the inductor under single-ended operation, whereas Fig. 3.6 shows the same under differential operation. For single-ended operation, port 2 is grounded and the signal is applied to port 1, whereas for differential operation, the signal is applied across the two ports.

As seen from Fig. 3.5, the input impedance looking through port 1 is the parallel combination of the two components: one due to the inductance(L) in series with the resistance(R_S) and the second due to the parasitic capacitance(C_P) and resistance(R_P). Thus, the input impedance for the single-ended case is given by

$$Z_S = (R_S + jX_L)||(R_P - jX_C) \tag{3.2}$$

where $X_L = 2\pi fL$ and $X_C = 1/2\pi fC_P$ Therefore, on simplification,

$$Re(Z_S) = \frac{R_S^2 R_P + R_S R_P^2 + R_P X_L^2 + R_S X_C^2}{(R_S + R_P)^2 + (X_L + X_C)^2} \tag{3.3}$$

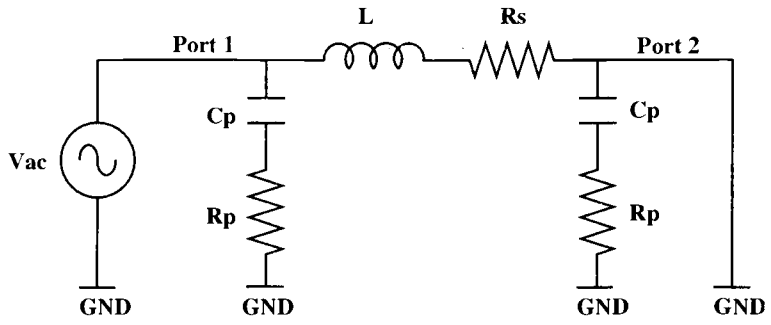


Figure 3.5. Circuit to obtain the inductor quality factor under single-ended excitation.

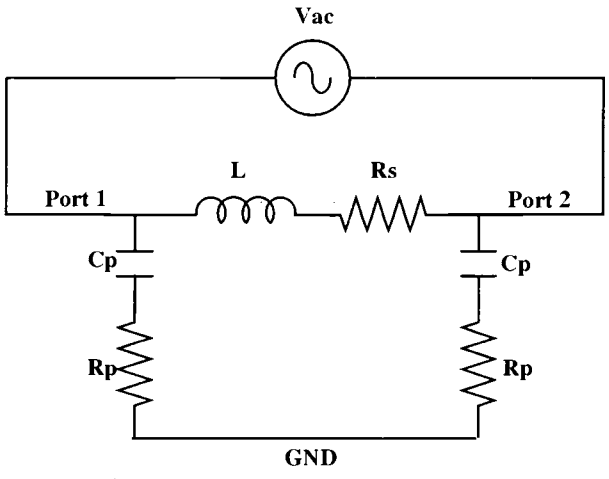


Figure 3.6. Circuit to obtain the inductor quality factor under differential excitation.

where $Re(Z_S)$ represents the real part of the input impedance.

For the differential excitation, as seen from Fig. 3.6, the input impedance is again a combination of two terms: the first component is the same as for the single-ended case, i.e. the series L-R_S combination, whereas the second is the series combination of the two parasitic C_P-R_P circuits. The input impedance for the differential case is given by

$$Z_D = (R_S + jX_L)||(2R_P - j2X_C) \tag{3.4}$$

which yields

$$Re(Z_D) = \frac{2R_S^2R_P + 4R_SR_P^2 + 2R_PX_L^2 + 4R_SX_C^2}{(R_S + 2R_P)^2 + (X_L + 2X_C)^2}. \tag{3.5}$$

Assuming $R_S \ll R_P$ and $X_L \ll X_C$, which are generally true, gives

$$Re(Z_S) = R_S + \frac{R_S^2R_P + R_PX_L^2}{R_P^2 + X_C^2} \tag{3.6}$$

and

$$Re(Z_D) = R_S + \frac{R_S^2R_P + R_PX_L^2}{2R_P^2 + 2X_C^2}. \tag{3.7}$$

The quality factor of the inductor can be written as

$$Q = \frac{2\pi fL}{Real(Z_{INPUT})}. \tag{3.8}$$

Comparing (3.6) and (3.7), we observe that the real part of the input impedance is the same for single-ended and differential excitation at low frequencies. This is because the parasitics do not affect the inductors due to the high capacitive impedance. Accordingly both cases will have similar quality factors at low frequencies. However, as the frequency increases, the impedance of the parasitics increases more for the differential case, causing the real part of the input impedance to drop, as evident from (3.7). This results in an improvement of the quality factor.

3.6. Inductor Layout

The inductors used in the VCOs designed were stacked inductors. The National process had five metal layers. The inductors were formed by stacking the metal layers 2, 3, 4 and 5. Metal layer 1 was used for the underpass. The vias were placed at minimum allowable separation to allow maximum shorting between the stacked layers.

The value of the inductors used were 1nH and 2nH. The quality factor and the self-resonance frequency of the two inductors were obtained using the inductor model provided by National. The quality factor can be obtained in simulations by applying an ac signal of magnitude one to the relevant inductor port and using the following expression:

$$Q = \frac{\frac{1}{I_{IMAG}}}{\frac{1}{I_{REAL}}} \tag{3.9}$$

where I_{REAL} and I_{IMAG} are the real and imaginary parts of the ac current through the voltage source. The quality factor of the two inductors is shown in Figs. 3.7-3.8.

It can be observed from the plots that the quality factor for the 1nH inductor is 6.77 at 2.4GHz and the self-resonance frequency is 36GHz. The 2nH inductor has a quality factor of 6.61 at 2.4GHz with a self-resonance frequency of 28GHz. The above mentioned quality factors are single-ended quality factors, which means they are obtained with one port of the inductor grounded and the signal applied to the other port.

Fig. 3.9 shows the quality factor plot of the 2nH inductor when it is differentially operated. The signal is applied between the two ports. It can be observed that the quality factor at 2.4GHz is 7.69 and the self resonance frequency is 34GHz. Thus differential operation of inductors does enhance the quality factor of the inductor.

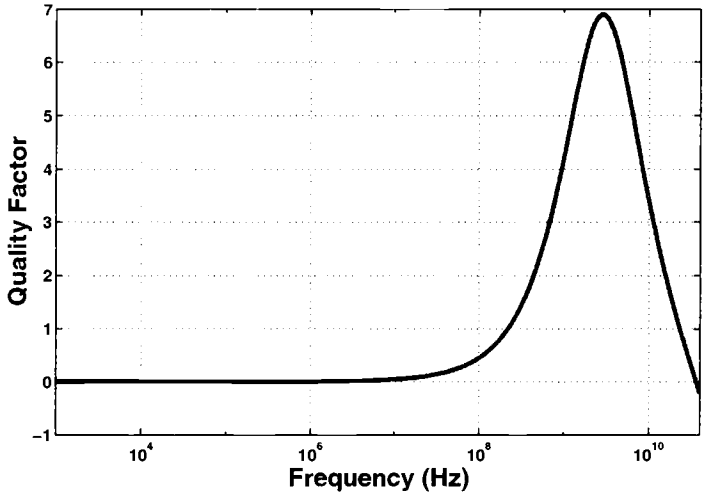


Figure 3.7. Quality factor versus frequency plot for the 1nH inductor.

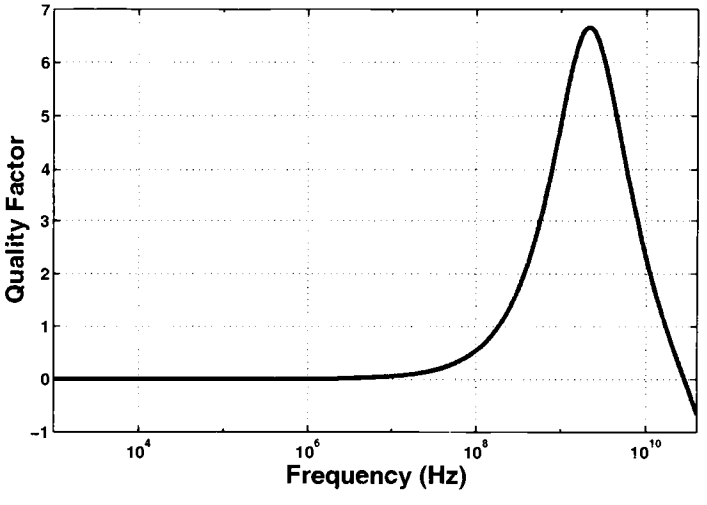


Figure 3.8. Quality factor versus frequency plot for the 2nH inductor.

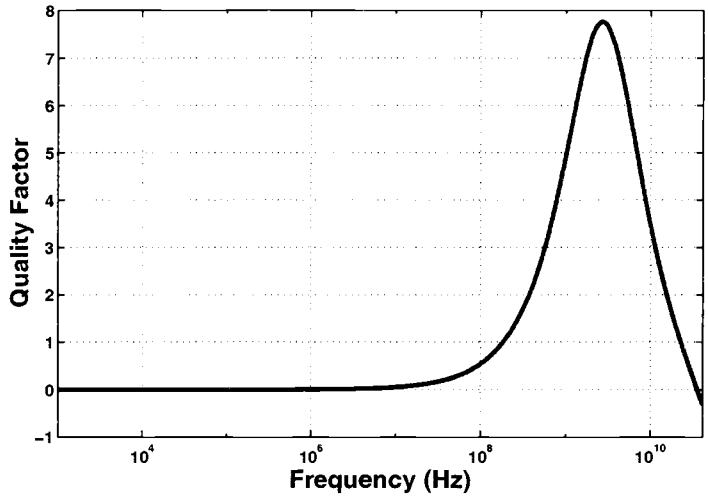


Figure 3.9. Differential quality factor plot for the 2nH inductor.

The layout of the two inductors is shown in Figs. 3.10-3.11. The 1nH inductor occupies an area of $175\mu m \times 200\mu m$ whereas the 2nH inductor spans an area of $182\mu m \times 200\mu m$.

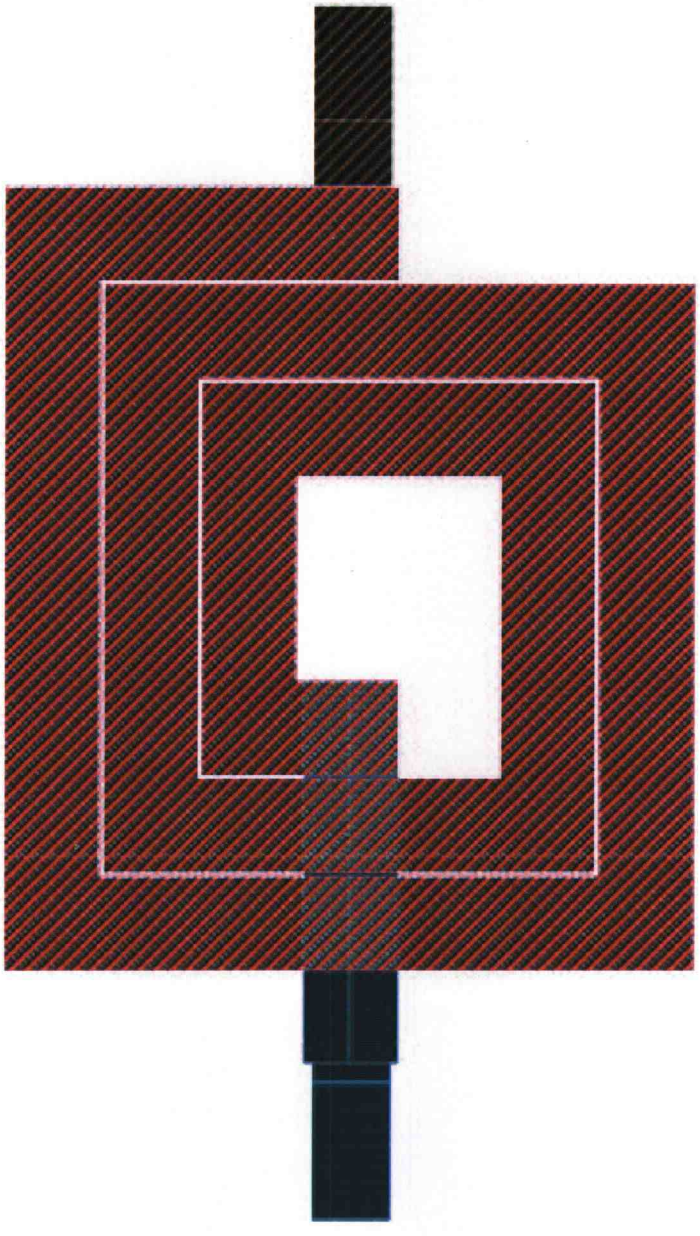


Figure 3.10. Layout of the 1nH inductor.

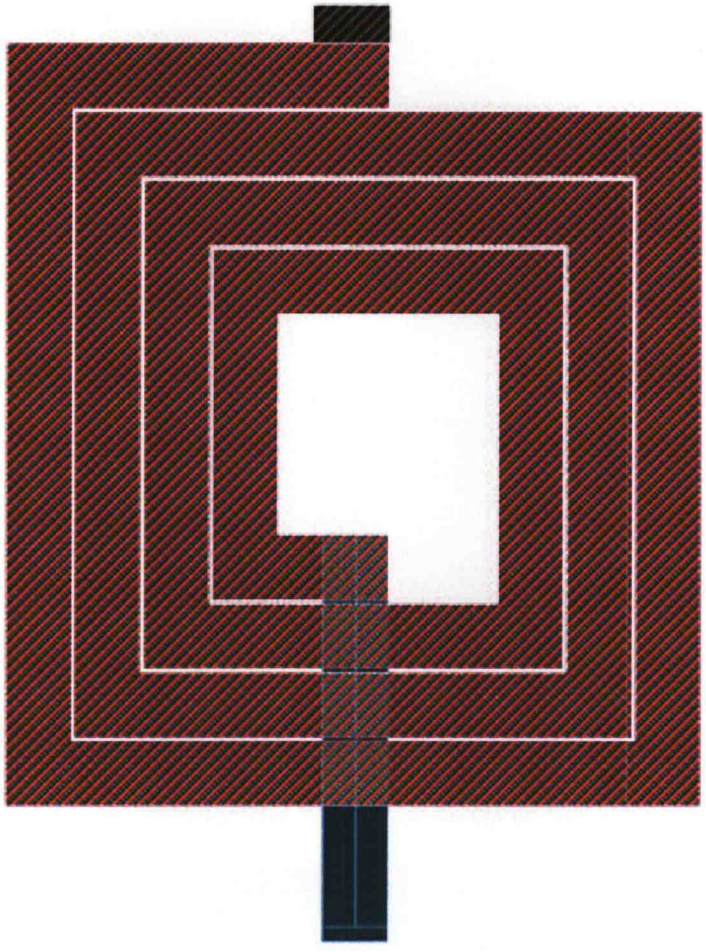


Figure 3.11. Layout of the 2nH inductor.

4. VARACTORS

4.1. Introduction

Although inductors can be used for tuning an oscillator, voltage dependent capacitors (varactors) are more commonly used for varying the frequency of oscillation. Varactors can be of various types: p-n junctions, MOS transistors and MOS transistors in conjunction with binary weighted switched capacitors. All of these are capable of providing a voltage dependent capacitance variation. Ideally it is expected that the tuning characteristic is linear, since a non-linear characteristic will have a steeper slope for the same voltage variation. This means that the K_{VCO} would be larger, causing the control node to be sensitive to noise.

The varactor should have a large quality factor, ideally infinite. This is possible only when the series resistance is zero. Another desired feature of the varactor is the ratio of the maximum capacitance to the smallest capacitance be large for a larger tuning range. Practically most of the varactors are non-linear and have a limited C_{MAX}/C_{MIN} ratio. Also the parasitic resistances cause a degradation in the quality factor.

The most popular type of varactor used in CMOS technologies is the MOS varactor.

4.2. MOS Varactors

MOS varactors can be of three types, namely inversion mode varactors, accumulation mode varactors and gated varactors [14], [15], [16]. Fig. 4.1 shows the

cross-section of the three different varactors. The description of each varactor is discussed below.

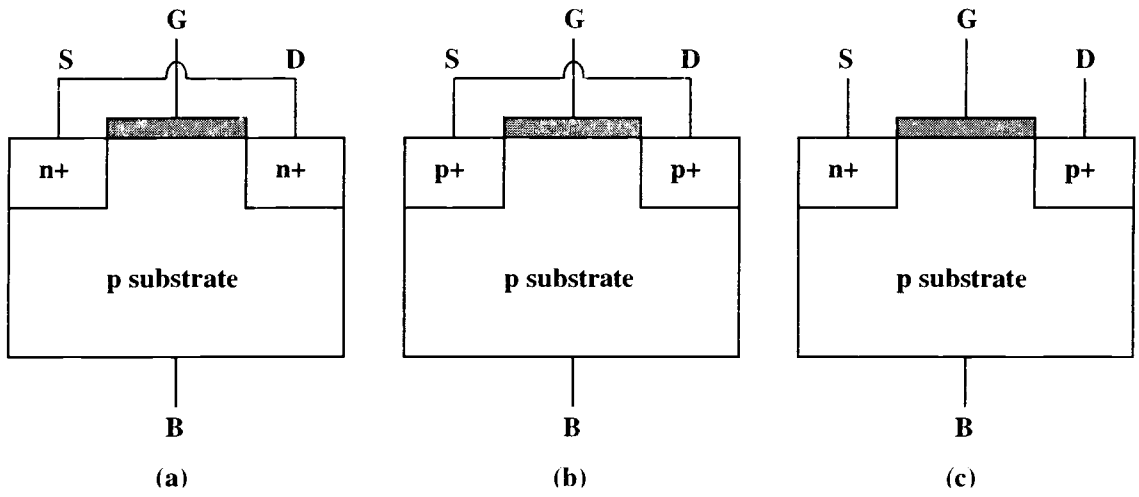


Figure 4.1. Cross-section of the different varactors: (a) Inversion mode varactor. (b) Accumulation mode varactor. (c) Gated varactor.

4.2.1. *Inversion Mode Varactor*

The C-V characteristics of the MOS capacitor shown in Fig. 4.1(a), with the drain, source and bulk terminals tied, is shown in Fig. 4.2. The capacitance per unit width of the transistor is plotted against the gate-source voltage. The simulations for C-V characteristics of the varactors were performed using MEDICI [40], which is a two-dimensional device simulator.

Three distinct regions can be observed from the C-V characteristics. In the accumulation region, which occurs when $V_{GS} \ll V_{TH}$, the interface between the gate oxide and silicon is negative allowing the holes to move freely. As V_{GB} increases, the holes are repelled and a depletion layer is formed below the oxide, and the transistor

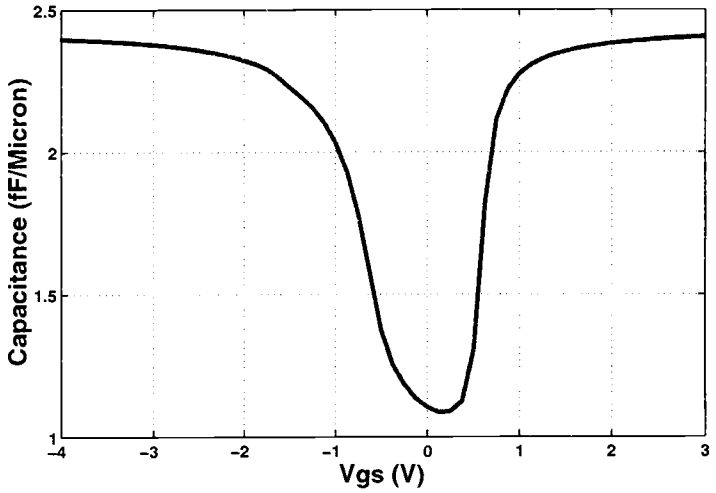


Figure 4.2. C-V characteristics of the MOS capacitor.

operates in the depletion region. As the voltage increases further, negative charges get attracted to the positively charged gate oxide giving rise to the inversion mode of operation. Depending on the density of negative charge carriers in the interface, this region of operation is subdivided into weak, moderate and strong inversion regions. In the accumulation and the strong inversion regions, the MOS capacitance reaches a value of C_{OX}, the gate oxide capacitance.

For an inversion mode varactor, the device should not enter the accumulation region [14], [15]. This is accomplished by connecting the bulk to the appropriate bias so that the pn junctions of the transistors are always reverse biased. Fig. 4.3 shows the tuning characteristics of the varactor shown in Fig. 4.1(a), with the bulk tied to the most negative supply.

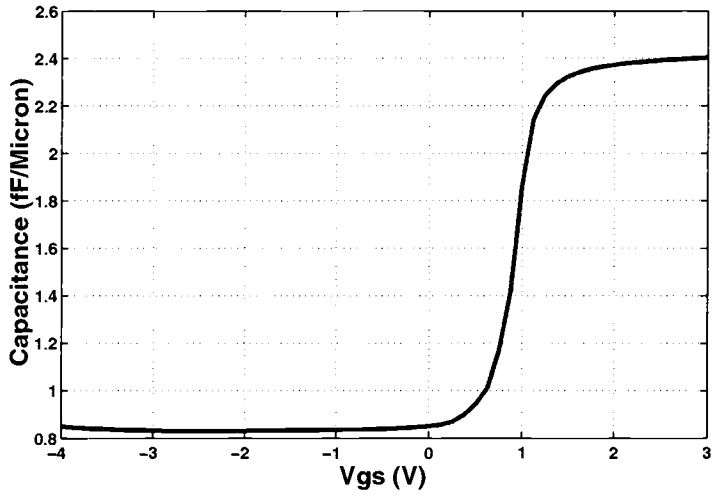


Figure 4.3. C-V characteristics of the inversion mode varactor.

It can be observed that for positive voltages, the n+ drain-source regions provide the electrons for the formation of the inversion layer, and the device operates in the inversion region. The device doesn't enter the accumulation region since the bulk is never positive as compared to the gate. A capacitance variation (C_{MAX}/C_{MIN}) of 2.82 is observed.

4.2.2. *Accumulation Mode Varactor*

Another alternative for obtaining the capacitance tuning is by operating the transistor in accumulation and depletion regions only [14], [15], [27]. Since the inversion regime is undesired, the doping profile of the drain-source regions is changed. For the accumulation mode varactor in Fig. 4.1(b), the drain-source diffusions are p+ type. The capacitance variation of this varactor is depicted in Fig. 4.4.

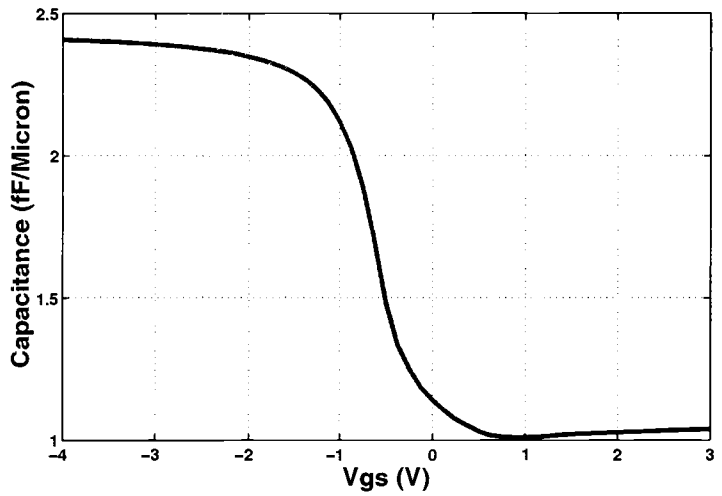


Figure 4.4. C-V characteristics of the accumulation mode varactor.

It is seen from these characteristics, that the device operates in the accumulation region for negative voltages and flattens out at positive voltages. The capacitance variation (C_{MAX}/C_{MIN}) obtained with this varactor is 2.32.

4.2.3. *Gated Varactor*

Another varactor which is capable of providing a wide tuning range is the gated varactor [16], [17]. The inversion mode and accumulation mode varactors are two terminal varactors, in the sense that the voltage of one terminal (gate) is varied with respect to the other (source). The gated varactor is a three terminal varactor as shown in Fig. 4.1(c). For the gated varactor, the device capacitance is defined as the capacitance seen from the drain, unlike the inversion mode and accumulation mode varactors, where the device capacitance was the capacitance looking through

the gate. A family of C-V curves can be obtained by sweeping the gate voltage with the drain voltage fixed and then repeating this for different drain voltages. The capacitance variation for the gated varactor is depicted in Fig. 4.5.

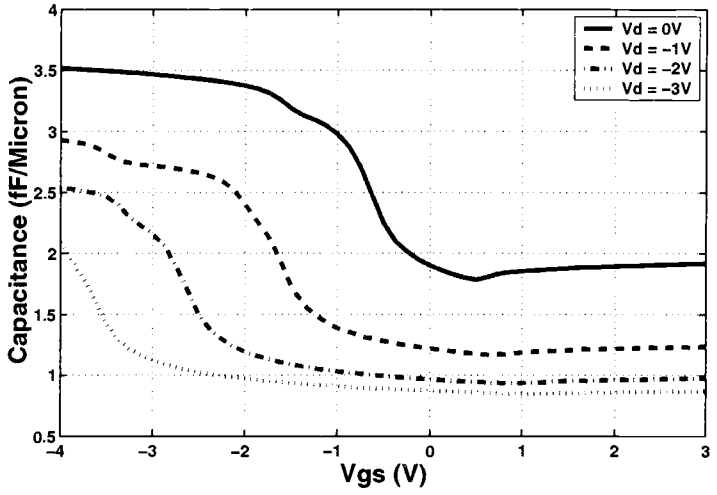


Figure 4.5. C-V characteristics of the gated varactor.

With the drain voltage fixed, a variation in the gate voltage causes the capacitance under the gate to vary in a manner similar to the accumulation mode varactor. Reducing the gate voltage causes the gate-bulk capacitance to increase from C_{OX} in series with $C_{DEPLETION}$ to C_{OX}. The capacitance looking through the drain is the parallel combination of the gate-bulk capacitance and the source-bulk depletion capacitance. Therefore the largest capacitance for this varactor is larger than that for the inversion and accumulation mode varactors, i.e. C_{OX}. As the drain voltage is decreased, the source-bulk voltage increases causing the depletion layer to increase. This reduces the source-bulk depletion capacitance thereby decreasing

the capacitance seen through the drain. Thus, by changing the drain and the gate voltage simultaneously, it is possible to move from one curve to the other. The capacitance variation (C_{MAX}/C_{MIN}) for this varactor is around 4, which is much greater than that obtained with the inversion or accumulation mode varactors.

4.3. MOS Transistors as Varactors

In the absence of models for the varactors explained in the previous section, the designer has to rely on the MOS transistor for use as a varactor. The tuning characteristics of NMOS and PMOS transistors are explained in this section. All the simulations were performed using HSPICE with a transistor size of $300\mu m/0.24\mu m$.

The gate of the transistors was connected to the oscillator and the control voltage was applied to either the bulk terminal or the drain-source terminal. For each of the transistors (NMOS and PMOS), two set of simulations were performed to obtain the capacitor tuning characteristics. The gate of the transistor was biased at the same potential as in the oscillator circuit. An ac signal was superimposed on the gate to observe the frequency dependent capacitances. The value of *Cgtot* gives the total capacitance seen from the gate node. One of the circuit schematics used for simulation is given in Fig. 4.6

The C-V plot obtained for the NMOS transistor, with the bulk terminal swept from -2.5V to 2.5V and the drain-source terminals connected to 2.5V to prevent the p-n junction diode from turning ON, is shown in Fig. 4.7.

Increasing the bulk potential causes the transistor to move from the accumulation region to the depletion region. The gate-bulk capacitance changes from C_{OX} in the accumulation region to C_{OX} in series with $C_{DEPLETION}$ in the depletion region. Similar characteristics were obtained for the PMOS transistor with the bulk

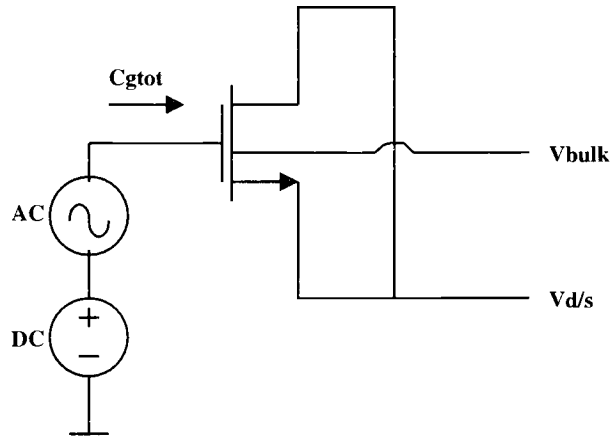


Figure 4.6. Circuit used to determine the C-V characteristics of the varactor based on a MOS transistor.

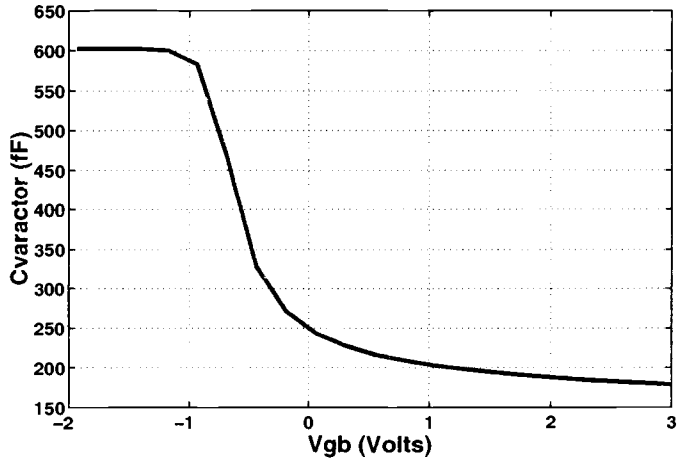


Figure 4.7. C-V characteristics of an NMOS transistor when the bulk voltage is varied.

node swept and the drain-source terminals connected to -2.5V. The result for the PMOS transistor is illustrated in Fig. 4.8.

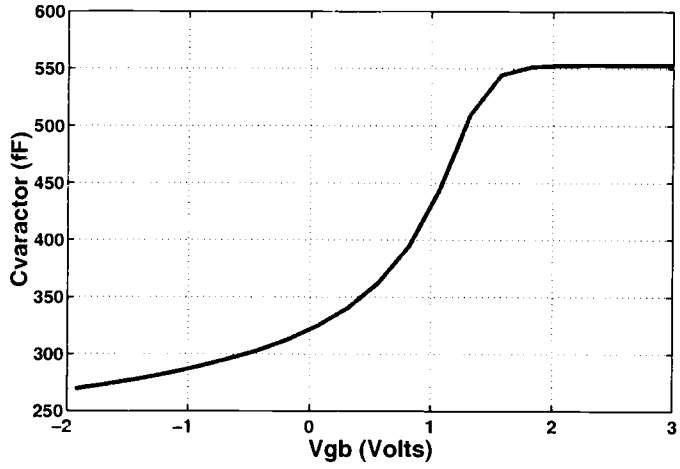


Figure 4.8. C-V characteristics of a PMOS transistor when the bulk voltage is varied.

The results obtained for the NMOS and PMOS transistors with the drain-source terminals swept and the bulk terminal biased appropriately to reverse bias the junctions are shown in Figs. 4.9-4.10.

Applying the control voltage to the drain-source terminal causes the junction depletion capacitance to change. The device is in the depletion region when $|V_{GS}|<|V_{TH}|$ and in the inversion region when $|V_{GS}|>|V_{TH}|$. Accordingly the capacitance seen from the gate changes sharply as the device moves from one region of operation to the other.

It can be observed from Figs. 4.7-4.10 that the C-V characteristics obtained are smoother when the bulk is varied. Therefore the bulk node was chosen as the

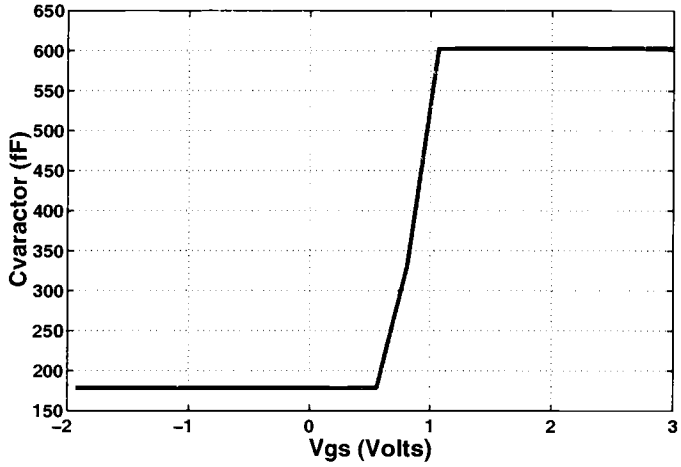


Figure 4.9. C-V characteristics of an NMOS transistor with varying Vd/s.

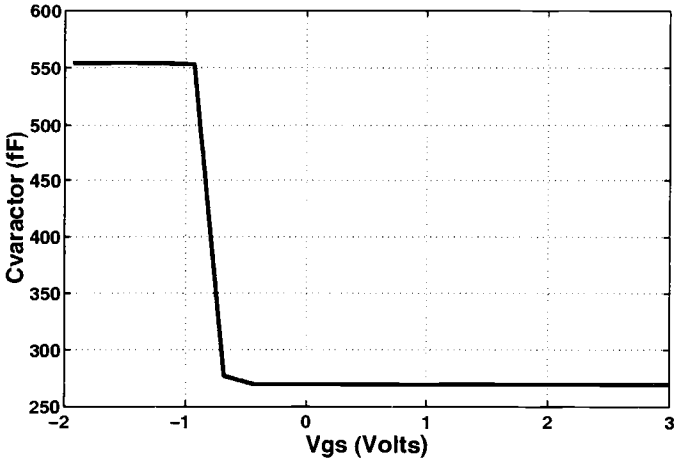


Figure 4.10. C-V characteristics of a PMOS transistor with varying Vd/s.

control terminal in the oscillators designed. Since the bulk terminal needs to be varied, only a PMOS transistor can be used for the varactor, as its bulk terminal is available in an N-well process. Although the capacitance variation in Fig. 4.10 is small, a high tuning range was achieved by using this varactor in conjunction with an array of binary weighted capacitors as described in the next section.

4.4. Varactor Implementation Using Switched Capacitor Array

Increasing the tuning range of the varactors increases the K_{VCO}. This increase in the VCO gain implies a larger gain for any noise coupling to the control node. This in turn, will degrade the phase noise performance of the VCO. Consequently a circuit which has a large tuning range but a small K_{VCO} is desirable. One such circuit is shown in Fig. 4.11 [6]. The varactor is designed to provide a small tuning range with a small K_{VCO}, preferably in the range of 20-30MHz/V. The fixed capacitors are switched ON or OFF by means of a switch realized by the NMOS transistor. Thus the varactor is responsible for the fine tuning and the switched capacitor provides the necessary coarse tuning. The typical tuning curves for this circuit are shown in Fig. 4.12. Tuning elements corresponds to the switch state (ON/OFF). Any variations during fabrication could cause the frequency tuning to be discontinuous. Therefore a certain amount of overlap between the curves is necessary.

The capacitances in the switched capacitor implementation are chosen as C, 2C and 4C. When the switches are turned ON in a binary sequence from 000 to 111, the capacitances C, 2C, 3C, 4C... get added to the tank capacitance. The switch sizes are chosen as W/L, 2W/L and 4W/L. This ensures that the capacitance of the

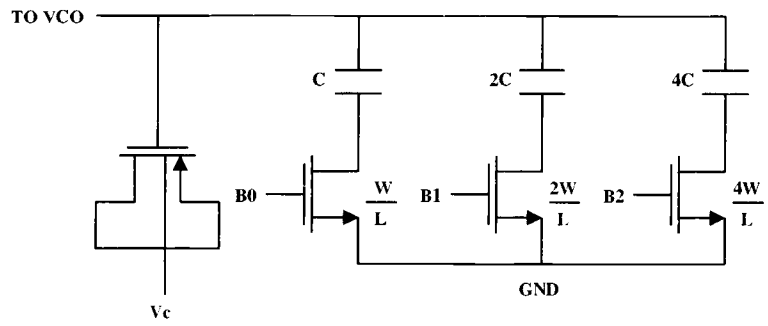


Figure 4.11. Binary weighted switched capacitor circuit to provide higher tuning range without increasing the VCO gain.

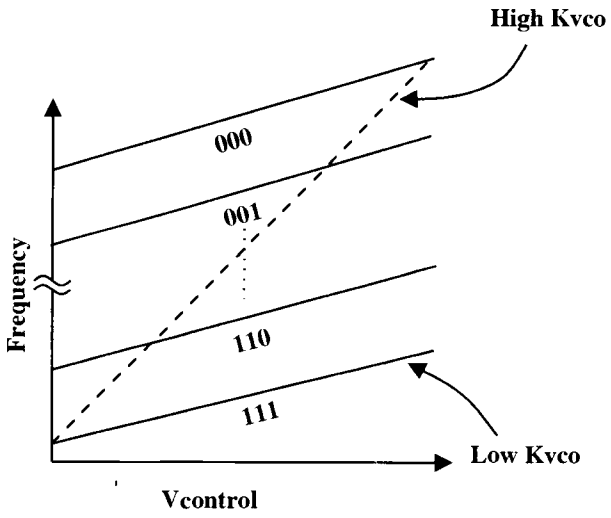


Figure 4.12. Tuning characteristics explaining the principle of switched tuning.

switch scales linearly with the binary capacitances, thereby providing more uniform tuning curves.

The use of this circuit in an actual implementation would require a digital control block which would track the frequency provided by the oscillator and accordingly control the varactor control voltage in case of small variations or change the bits to move on the other tuning curves for larger frequency variations. The greater the number of switched capacitors, the smaller the tuning range of the varactor to span the same frequency tuning range. Increasing the number of switched capacitors would require a smaller capacitance making it difficult to realize well matched capacitances. Accordingly a trade-off is necessary to decide the number of steps to be used.

The quality factor of the switched capacitor array affects the tank quality factor. Hence it is necessary to know the quality factor of the varactors when the switch is ON or OFF. Fig. 4.13 shows the quality factor of only the switched capacitor array when all the switches are OFF, whereas Fig. 4.14 depicts the quality factor when all the switches are ON.

It can be observed from Fig. 4.13, that the quality factor is very large when the switches are OFF, and the capacitor bank doesn't deteriorate the tank quality factor. When the switches are ON, the quality factor drops down by several orders of magnitude and affects the tank quality factor. The parasitics and gate resistance would further degrade the quality factor. Consequently the start-up condition for the oscillators should be determined with all the switches ON. This will ensure oscillations under all varactor switch settings.

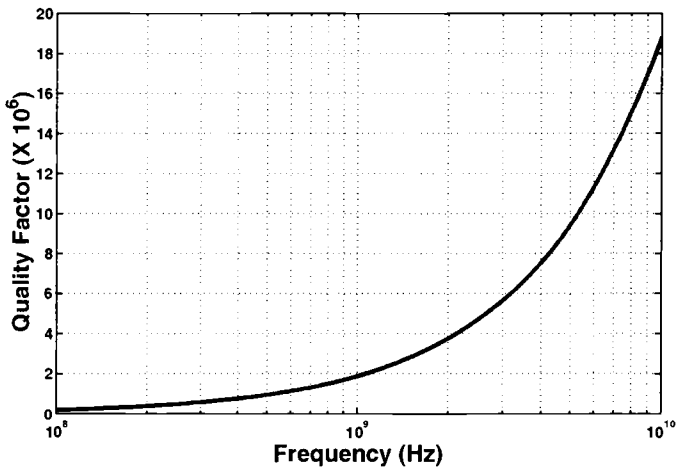


Figure 4.13. Quality factor of the switched capacitor circuit when all switches are OFF.

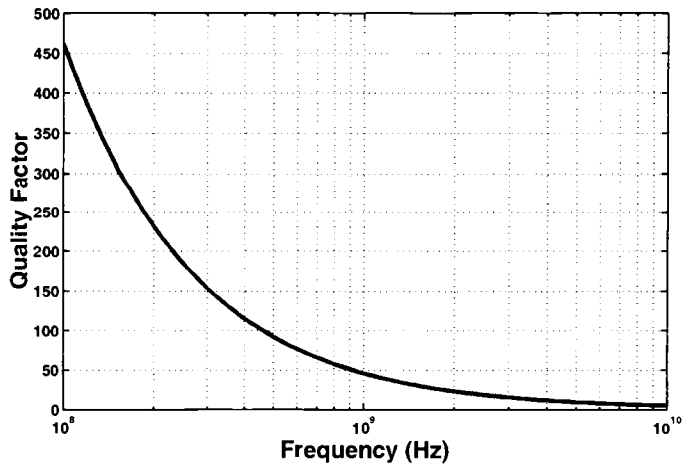


Figure 4.14. Quality factor of the switched capacitor circuit when all switches are ON.

4.5. Varactor Layout

The layout of the varactor is crucial since the tuning curves depend directly on the binary weighted capacitances and the matching between them. The poly-substrate oxide capacitance was used for generating the capacitors. The layout of the array of capacitors used for switched tuning is illustrated in Fig. 4.15. The smallest capacitance C was chosen to be the unit capacitance and was repeated depending on the capacitance value desired. Thus for 2C, two unit capacitors were connected in parallel. The binary weighted capacitors were arranged such that the linear gradients along the x-direction and y-direction were minimized. The letter D indicates the dummy capacitors used around the array for matching purposes. Although the dummy capacitors used in this case were the same as the unit capacitance, smaller dummy capacitors could be used to save area.

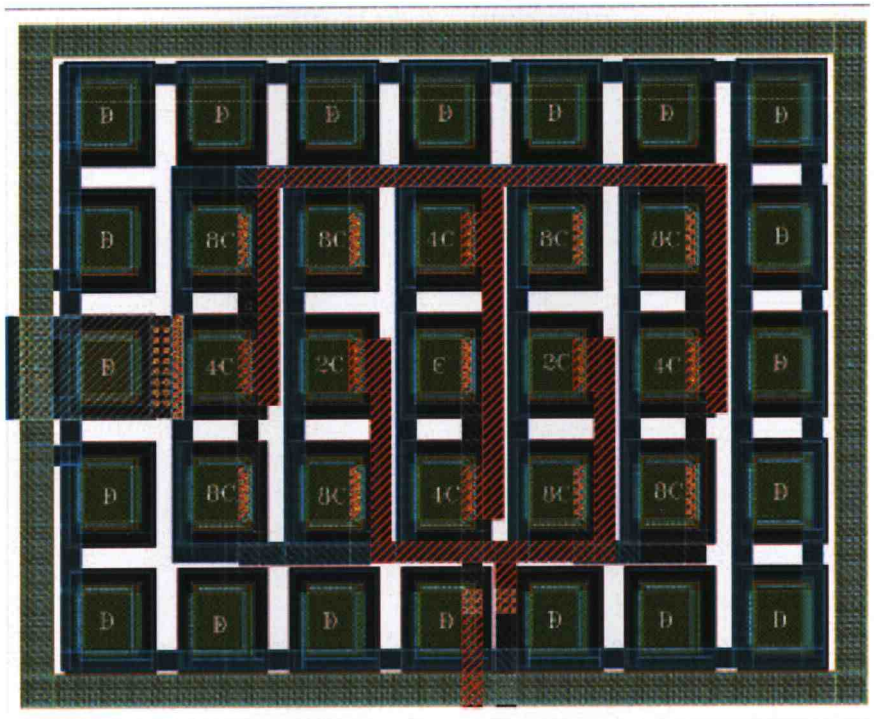


Figure 4.15. Layout of the capacitor bank used in the varactor circuitry.

5. PHASE NOISE IN OSCILLATORS

5.1. Contributors of Phase Noise

Device noise and interference noise are responsible for phase noise. Since the oscillators in consideration are purely CMOS, only the intrinsic noise sources present in CMOS oscillators are covered. Device noise comprises of thermal noise and flicker (1/f) noise, which are the most significant contributors. Thermal noise is noise due to the random thermal movement of the carriers within the body of a resistor. It has a power spectral density which is uniform in the frequency domain, hence, it is referred to as white noise. Flicker noise is due to the entrapment of the carriers in the energy states which are present at the interface between the gate oxide and the silicon substrate. The carriers are trapped and released randomly and this gives rise to flicker noise. Flicker noise has a 1/f dependence. Interference noise is due to noise in the supply lines or noise coupling through the substrate. The effect of supply and substrate noise is explained in Section 5.3.

If we consider the oscillators described in Section 2, the noise contributors are:

1) Thermal and flicker noise of the cross-coupled pairs.

2) Thermal and flicker noise of the tail current transistors.

3) Thermal noise of the tank inductor series resistance.

4) Thermal and flicker noise of the varactor.

5) Noise due to buffers.

The flicker noise in the circuit contributes to the -30dB/decade region in the phase noise curve and the thermal noise is responsible for the -20dB/decade region of the phase noise curve. Simulations were performed on several circuits and

general observations were made. At lower offset frequencies, the flicker noise of the cross-coupled pair and the flicker noise of the tail current transistors dominates. Depending on the topology and the design, one may be more dominant than the other. At higher offset frequencies, the resistance of the inductor is the most important contributor of phase noise. The thermal noise of the cross-coupled pair and the tail transistors can also be significant. Another factor in simulation, which influences how well the simulated phase noise curve would match the measured data, is the noise model used for the transistors. Depending on whether the NOIMOD parameter in the MOSFET model is set to 2 or 4, the curves may be different. Different models predict different noise contribution to phase noise. Thus, the results may not match simulation if the noise models are inaccurate. The noise model used for the design of the oscillators described in Section 6 was NOIMOD = 2 and the parameters for the model were provided by National. In addition to these, the buffer which is added for measurement purposes adds noise. Prediction of varactor noise depends on the accuracy of the varactor model.

5.2. Factors Influencing Phase Noise

There are several factors which affect the phase noise in oscillators. Some of them may be more dominant than others depending on the oscillator topology. Since phase noise depends on the amount of noise generated by the devices and the transfer function from device noise to phase noise, changing any parameter in the circuit might change both, i.e., the generated noise and the transfer function. Therefore, to analyze how a particular parameter affects phase noise is a complex problem. However, the effect of some parameters on phase noise is easy to understand. This

section explains the effect of such parameters on phase noise. The simulations were performed using SpectreRF.

5.2.1. *Oscillator Topology*

The choice of a proper oscillator topology is beneficial from the phase noise point of view. For identical bias currents, the complementary structure has a voltage swing almost double that in the case of a NMOS structure [20], [21]. The explanation for this is as follows. Fig. 5.1 shows the simplified diagram of the two oscillators. Assume that the inductance and series resistance for the NMOS oscillator is L/2 and R/2, where L and R represent the inductance and series resistance of the complementary oscillator.

Both oscillators consume the same current, I, and the transistors are assumed to switch ON and OFF completely. For the NMOS oscillator, the current, I, flows through one inductor in one half of the cycle and through the other inductor in the other half as illustrated in Fig. 5.1. The current and voltage waveforms at the two output nodes are shown in the Fig. 5.2 for the NMOS oscillator. Figs. 5.2(a) and (b) show the current waveform through the two transistors as they switch ON and OFF. Figs. 5.2(c) and (d) depict the voltage drop across the two inductors. The pre-filtered waveform across the differential output is shown in Fig. 5.2(e). The tank filters the components other than the fundamental and the differential output voltage swing is given by

$$V_{OUTPUT} = \frac{4}{\pi} I R_P/2 = \frac{2}{\pi} I R_P \tag{5.1}$$

where $R_P/2 = (1 + Q^2)R/2$ is the equivalent parallel resistance of the tank and Q is the quality factor of the inductor. This filtered waveform is what appears at the oscillator output and is shown in Fig. 5.2(f).

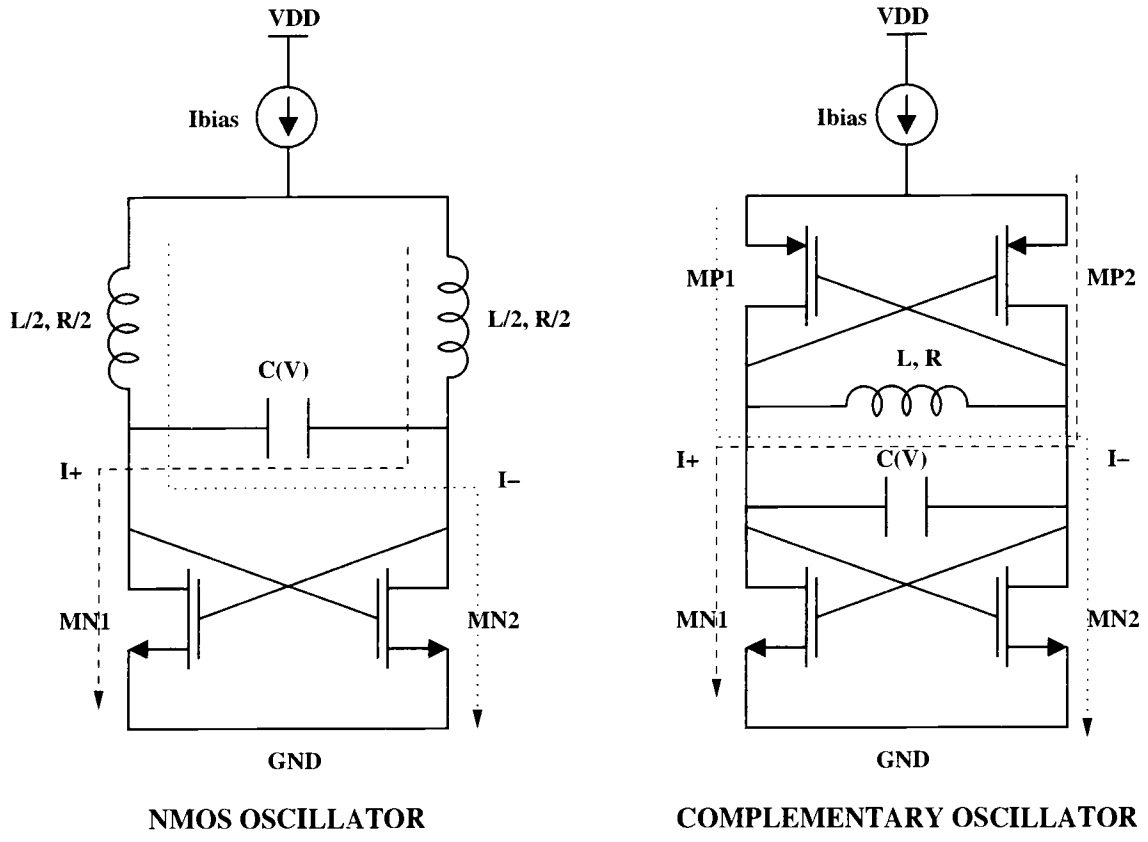


Figure 5.1. Comparison of the complementary and the NMOS oscillator for identical currents.

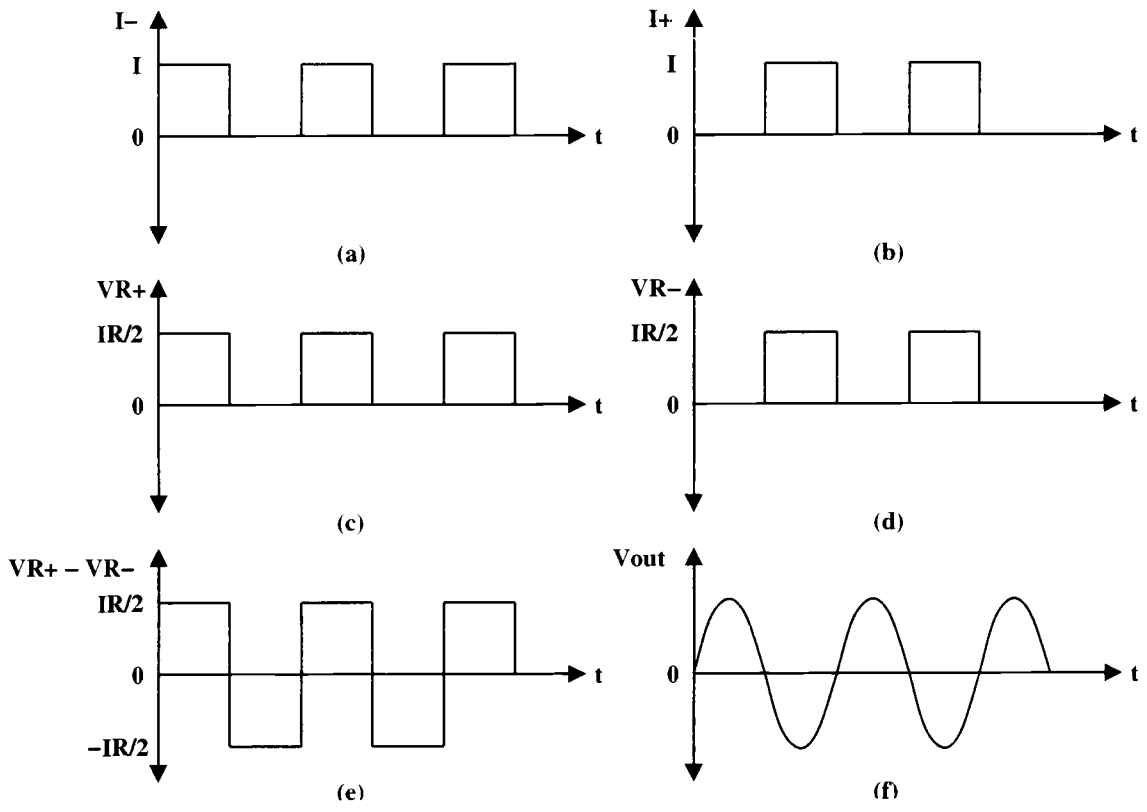


Figure 5.2. Current and voltage waveforms for the NMOS oscillator. (a) Current through MN2. (b) Current through MN1. (c) Voltage drop across the inductor connected to the drain of MN1. (d) Voltage drop across the inductor connected to the drain of MN2. (e) Pre-filtered voltage across the differential output. (f) Differential output voltage after the harmonics have been filtered by the tank.

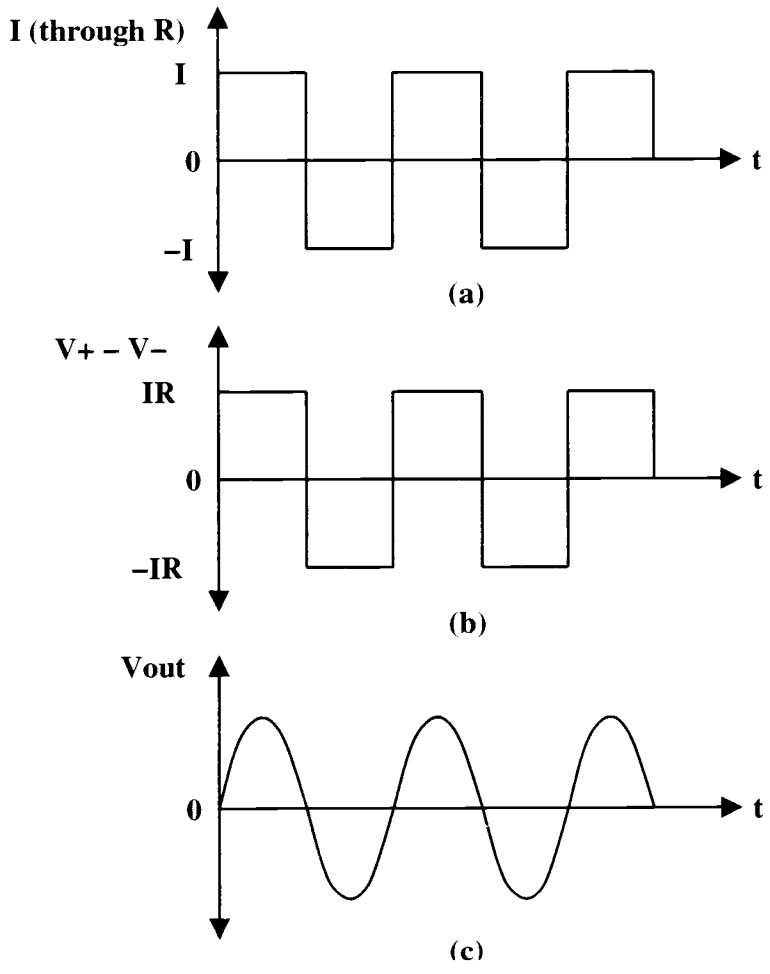


Figure 5.3. Current and voltage waveforms for the complementary oscillator. (a) Current through the inductor. (b) Pre-filtered voltage across the inductor. (c) Differential output voltage after the harmonics have been filtered by the tank.

In contrast to the NMOS oscillator, in the complementary oscillator the current, I, flows through the tank in the opposite direction in the two half cycles as depicted in Fig. 5.3. The waveform of the current through the inductor is shown in Fig. 5.3(a) along with the pre-filtered differential output in Fig. 5.3(b). The differential voltage swing, as shown in Fig. 5.3(c) for the complementary oscillator, is

$$V_{OUTPUT} = \frac{4}{\pi} I R_P. \tag{5.2}$$

From (5.1) and (5.2) it can be observed that the complementary oscillator has twice the voltage swing as compared to the NMOS oscillator. In the above derivation, ideal switching and the same quality factor for the inductors were assumed, which might not be the case. For this reason the voltage swing ratio might be smaller than two. Also this derivation is only valid as long as both the oscillators are operating in the current limited regime. In the voltage limited regime, the voltage swing saturates and consequently an improvement in swing cannot be obtained [20].

Increasing the voltage swing increases the carrier power, thereby implying an improvement in the phase noise from (2.8). Note that the complementary structure has more devices than the NMOS structure whereby more device noise can be expected to contribute to the phase noise. However, the increase in noise is small compared to the increased voltage swing. As a result, the complementary structure has a better phase noise performance. This can be clearly seen from Fig. 5.4 where the simulated phase noise of the two oscillators with identical bias currents is plotted. The voltage swing for the NMOS oscillator was 0.3V and 0.7V for the complementary one. At a frequency offset of 3MHz, the phase noise improvement with the complementary structure is about 7dBc/Hz.

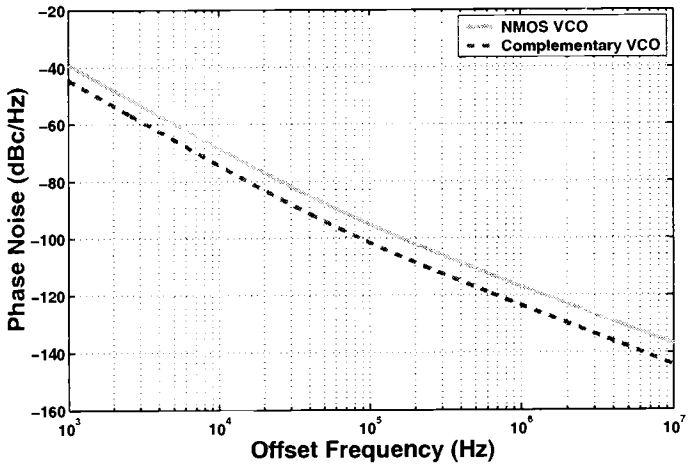


Figure 5.4. Comparison of the phase noise performance of the NMOS and the complementary topologies.

5.2.2. *Inductor Series Resistance*

As explained in Section 3.2, inductors are generally lossy due to the series resistance of the metal. In most cases, this resistance is the primary contributor of thermal noise. In order to understand the effect of the series resistance, the resistance was swept and phase noise simulations were performed. The results obtained are shown in Figs. 5.5-5.6.

As evident from Fig. 5.5, the voltage swing decreases with an increase in the series resistance. The voltage swing for the oscillator is given by

$$V_{OUTPUT} \propto IQ^2 R_S \tag{5.3}$$

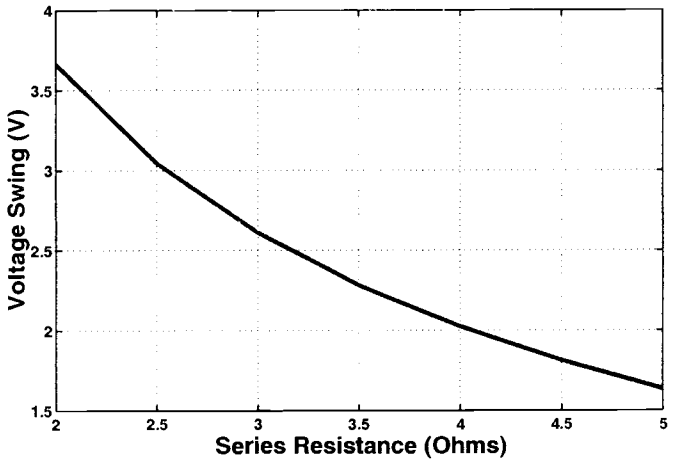


Figure 5.5. Effect of inductor series resistance on the voltage swing.

and Q is given by $\omega L/R_S$, neglecting the resistance of the varactors. Therefore, the voltage swing is inversely proportional to the series resistance and an increase in the series resistance results in a drop in the voltage swing.

A smaller series resistance implies less tank losses and, accordingly, a larger quality factor. This means that the oscillator can filter out noise more efficiently. Due to the higher selectivity of the tank, the phase noise is lowered. In conclusion, a smaller series resistance will give better phase noise performance which is also substantiated by simulation results shown in Fig. 5.6. Varying the series resistance does not affect the phase noise in the flicker region as evident from Fig. 5.6(a), but affects the phase noise in the thermal region significantly as seen from Figs. 5.6(b) and (c).

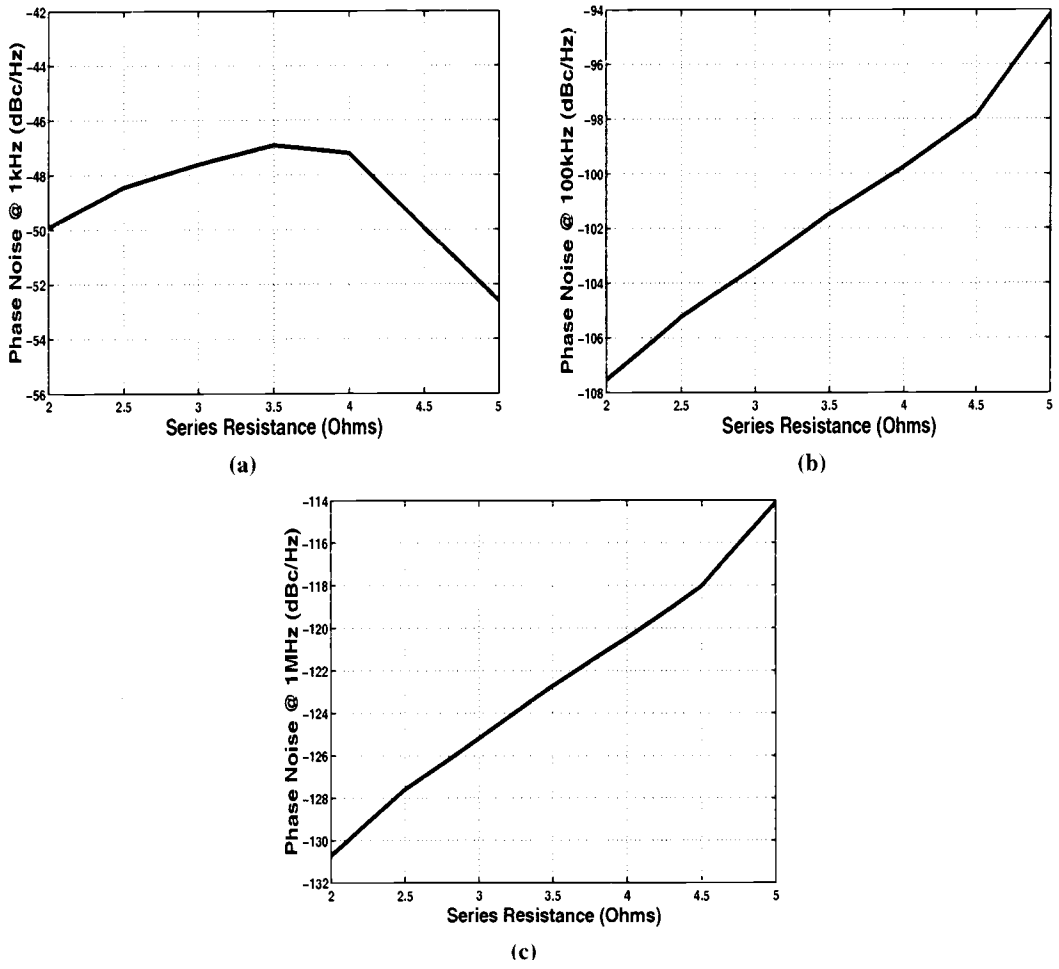


Figure 5.6. Effect of inductor series resistance on phase noise at the following frequencies: (a) 1kHz offset from the carrier. (b) 100kHz offset from the carrier. (c) 1MHz offset from the carrier.

5.2.3. *Oscillator Bias Current*

Since phase noise is always measured with respect to the carrier, one way of reducing phase noise would be by increasing the carrier power, i.e. increasing the signal swing. From (5.3), the voltage swing is proportional to the oscillator current and increasing the bias current should improve the phase noise performance. Simulations were performed to observe the effect of changing the oscillator bias current on the voltage swing and phase noise. The plot of voltage swing versus the oscillator current is shown in Fig. 5.7.

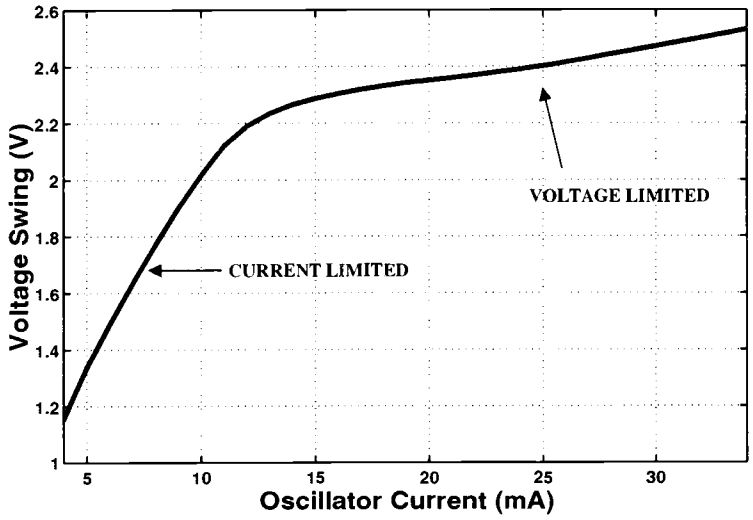


Figure 5.7. Voltage swing versus oscillator bias current.

It can be observed from Fig. 5.7 that the voltage does increase with the oscillator current. Initially the variation is linear and after a certain value, the voltage swing is limited by the supply. The region where the change is observed is called the current limited region and the limited swing region is called the voltage

limited region [20]. The variation in the phase noise at various frequencies for different oscillator bias currents is depicted in Fig. 5.8.

It can be observed from Fig. 5.8 that an increase in the voltage swing doesn't necessarily imply better phase noise performance. In the current limited region, the implication holds true and better phase noise performance is obtained. However, in the voltage limited region, some devices may leave their desired region of operation resulting in poor phase noise performance. One example is the tail current source which may go into the non-saturation region at large output voltage swings. To have the best possible performance, it is preferable to operate the oscillator in the current limited region, or at the edge of the current and voltage limited regions [22].

5.2.4. *Tail Current Source Dimensions*

The tail current source is a significant contributor to phase noise as shown in [23]. In order to understand how the sizing of the current mirror affects the phase noise at the output of the oscillator, SpectreRF simulations were performed by sweeping the device sizes. The results of the simulation are shown in Figs. 5.9-5.10. It can be observed from Fig. 5.9 that changing the width of the current mirror doesn't significantly affect the phase noise. On the other hand, changing the length of the current mirrors significantly affects the phase noise, as seen from Fig. 5.10. This is because flicker noise is more dependent on the length of the devices rather than the width, as evident from the flicker noise models [41]. It is desirable to keep the channel length of the current mirrors large. Increasing the channel length causes the flicker noise to decrease, thereby reducing the upconversion of flicker noise to phase noise. Also with a larger channel length, the output resistance (r_O) of the tail current source is higher, which prevents the degradation of the tank quality factor

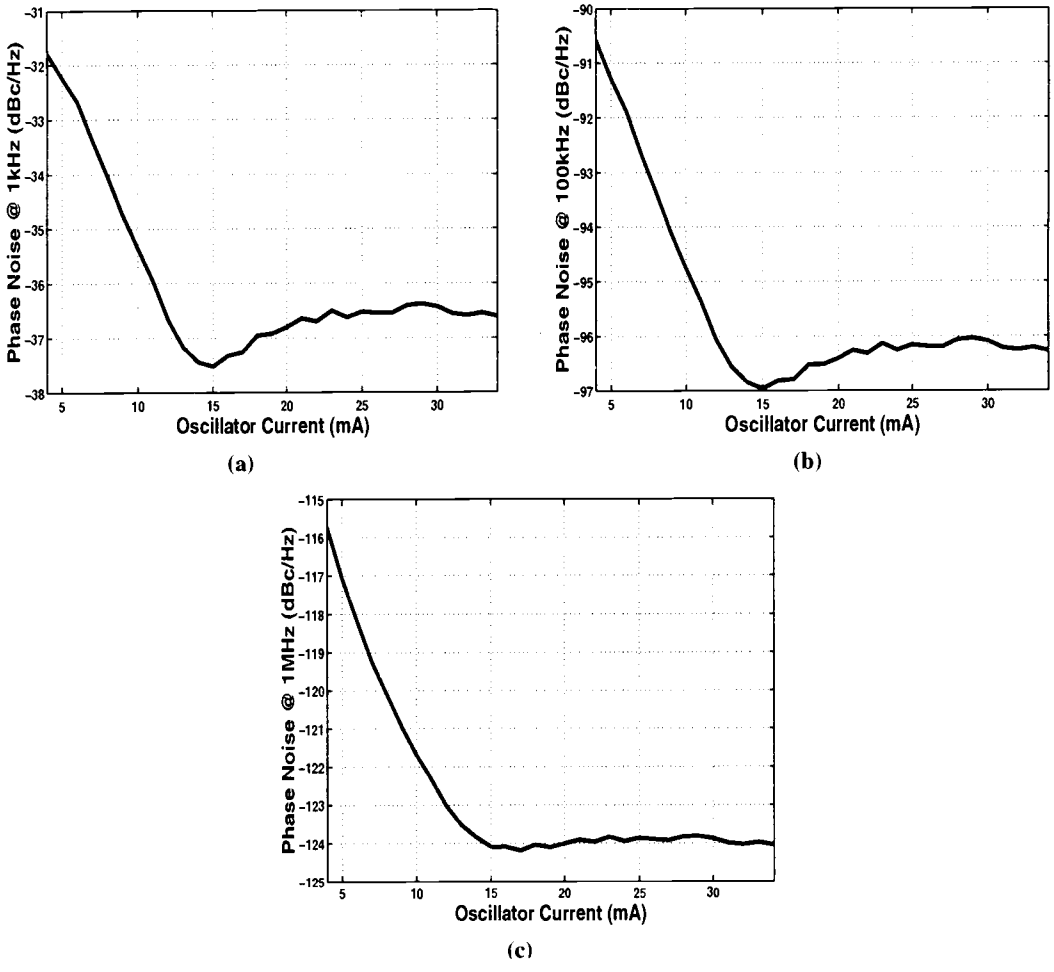


Figure 5.8. Effect of varying the oscillator current on phase noise at the following frequencies: (a) 1kHz offset from the carrier. (b) 100kHz offset from the carrier. (c) 1MHz offset from the carrier.

[24]. At 1kHz offset, the improvement in phase noise is around 7dBc/Hz with a channel length of 2.4μm as compared to the one with the minimum channel length of 0.24μm, whereas at 100kHz and 1MHz offsets, the improvements are 5dBc/Hz and 2dBc/Hz, respectively. This reduction in flicker noise affects the -30dB/decade part of the phase noise curve significantly.

5.2.5. *Differential Operation of Inductors*

As demonstrated in Section 3.4, differential operation of inductors results in a better quality factor as compared to single ended operation. This fact could be used in oscillators to improve the phase noise performance. Simulations were performed using the inductors shown in Table 3.1 in the NMOS and complementary oscillators. For the NMOS oscillator two set of simulations were done. In the first, two separate 1nH simple spiral inductors were used and the other set used a 2nH symmetric spiral. The center tap of the symmetric spiral was connected to the supply node. A 2nH simple spiral could not be used for this oscillator due to an unavailability of the center tap for biasing. The simulation results are shown in Fig. 5.11.

As seen from Fig. 5.11, the improvement in phase noise with the symmetric spiral at 3MHz offset was about 2dBc/Hz.

For the complementary oscillator, all three inductors were tried. Two 1nH simple inductors were connected in series between the output nodes in one case. The second case used a 2nH simple spiral between the output nodes and in the last experiment, the 2nH symmetric spiral was connected across the output nodes with the center tap unconnected. The phase noise plots for these three cases is shown in Fig. 5.12.

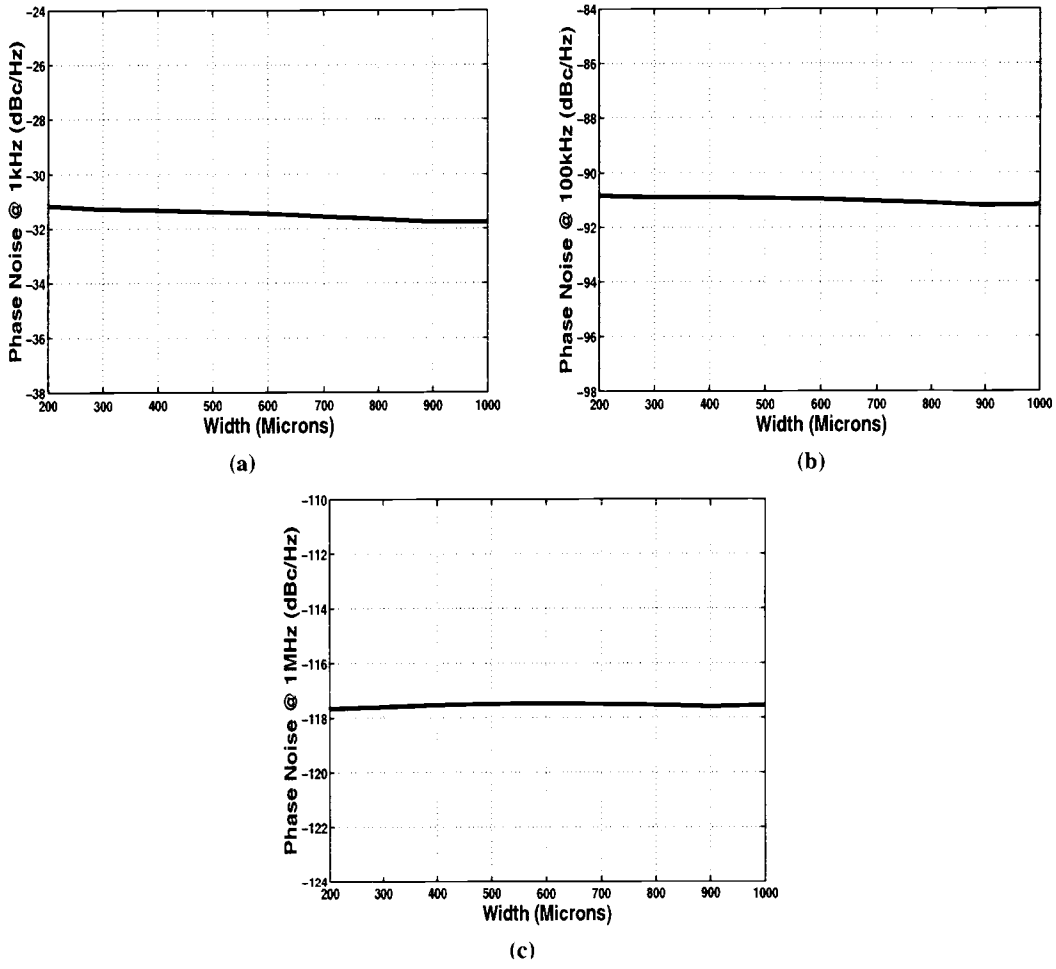


Figure 5.9. Effect of varying the width of the tail current source on phase noise at the following frequencies: (a) 1kHz offset from the carrier. (b) 100kHz offset from the carrier. (c) 1MHz offset from the carrier.

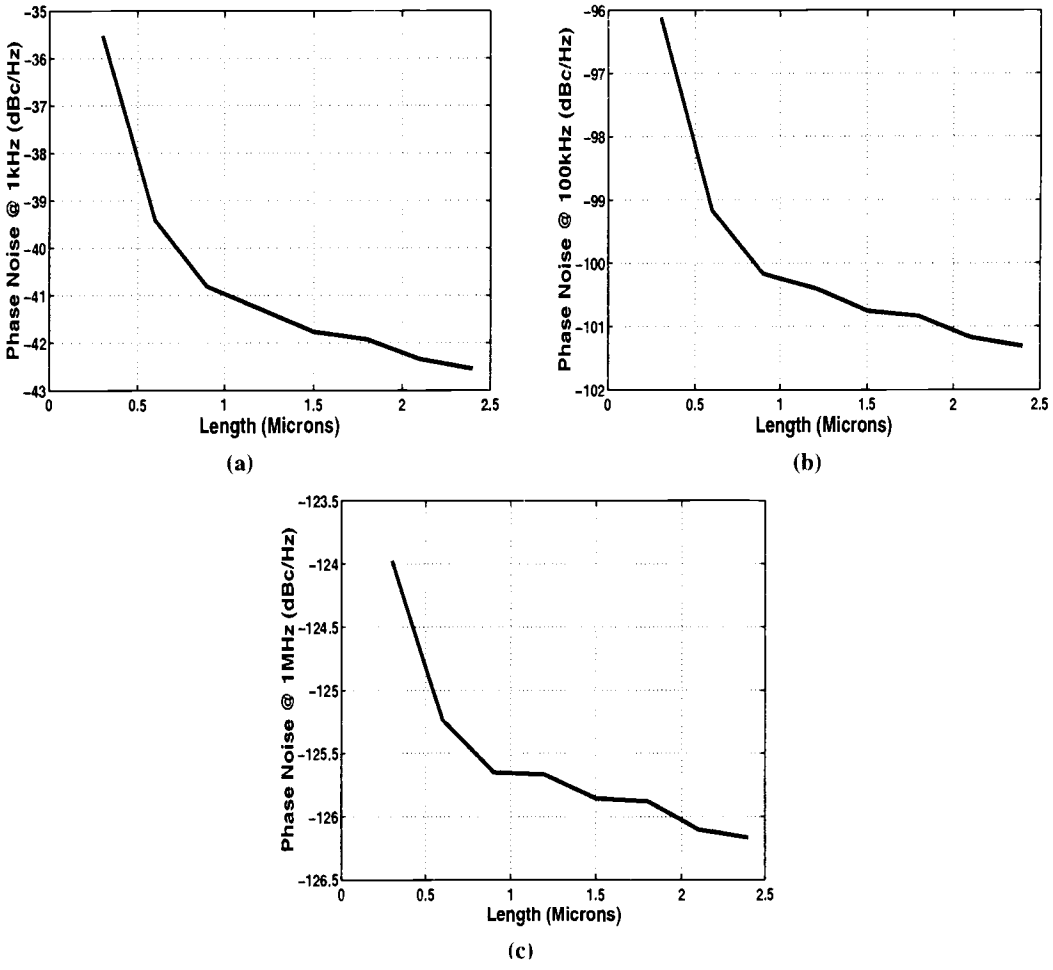


Figure 5.10. Effect of varying the length of the tail current source on phase noise at the following frequencies: (a) 1kHz offset from the carrier. (b) 100kHz offset from the carrier. (c) 1MHz offset from the carrier.

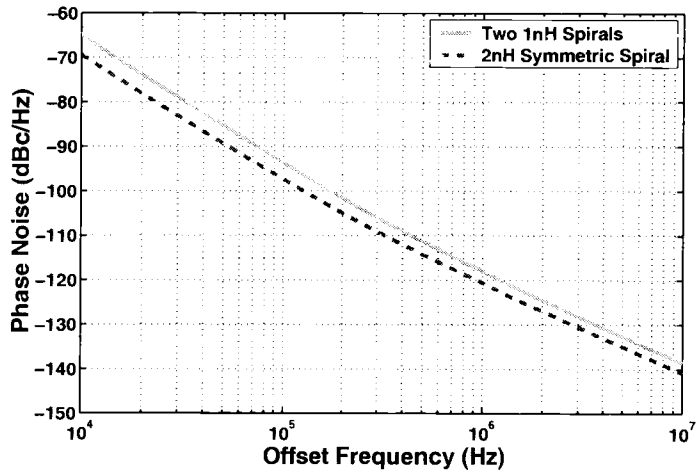


Figure 5.11. Comparison of phase noise performance of NMOS oscillator with different inductors.

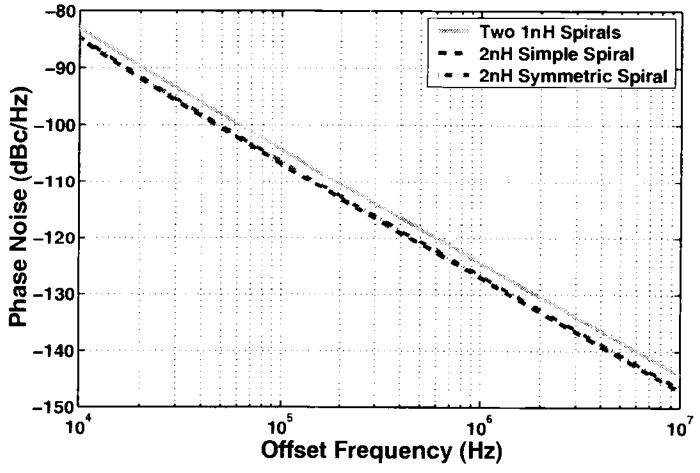


Figure 5.12. Comparison of phase noise performance of complementary oscillator with different inductors.

Similar to the NMOS oscillator, the complementary oscillator shows 2.5dBc/Hz improvement at 3MHz offset when the inductors are used differentially. Both the 2nH inductors show almost identical phase noise performance. In practice one could expect the 2nH simple inductor to show a slightly inferior performance since the tank would be unbalanced due to the underpass being connected to one output node. The tank sees the same inductance from either sides when the symmetric spiral is used. Hence, it is desirable to use the symmetric spiral.

5.3. Supply and Substrate Noise

One other major concern while designing VCOs is the environment in which the VCO is used. Usually VCOs are designed for single chip applications. Since the chip has many different blocks operating at the same time, there could be cross talk between the various blocks. If a noisy metal line is next to a clean one, the capacitance between the two lines will cause noise coupling. If any circuit on the chip results in current surges from the supply, then due to the inductance associated in the supply lines, large voltage transients could be produced. Also any noise in the equipment connected to the power supply might cause additional supply noise. All these can be lumped as supply noise.

Another form of interference noise is substrate noise. Since the digital blocks are switching at high frequencies, the parasitic capacitances of the transistors cause noise to be injected into the substrate. This noise generated by the digital circuits could find its way to the analog block through the substrate and affect the performance of the analog block. The amount of noise coupling through the substrate is dependent on the distance of the analog block from the digital block and the type of substrate. If the doping of the substrate is low, then the substrate has a higher

resistance and substrate coupling will be lower. Also if the analog block is farther away from the digital block, the coupling between them would be less. Nevertheless, some amount of substrate noise is coupled into the analog blocks. Therefore the circuits designed should be insensitive to supply and substrate noise.

This section explains how supply or substrate noise manifest as phase noise at the output of the oscillator [12], [25]. As shown in Fig. 5.13, white noise, 1/f noise and deterministic noise were added to the supply and substrate nodes. All the simulations were performed using SpectreRF. Since the periodic steady state analysis (PSS) does not permit the use of a sinusoidal voltage source in the circuit, the injection of noise was performed using noise power spectral densities.

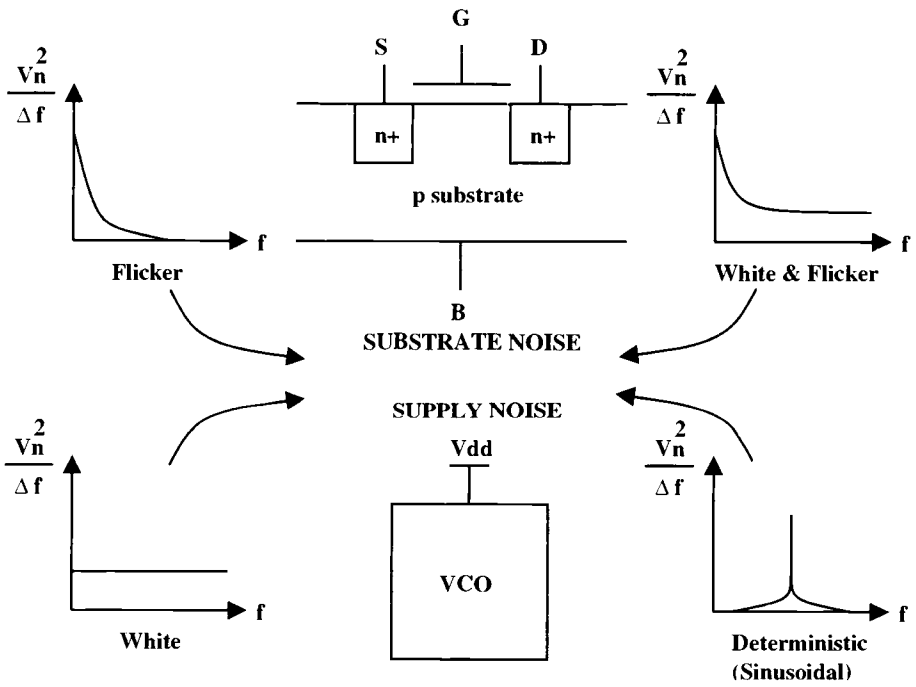


Figure 5.13. Injection of noise of various power spectral densities to Vdd or bulk to study the effect of supply noise and substrate noise on phase noise.

Fig. 5.14 shows the results obtained when only white noise is present on the supply lines and the substrate. The phase noise at the ouput of the oscillator is plotted before any noise was added and when white noise was added to the supply and substrate node. As expected, white noise shifts just the -20dB/decade part of the curve upwards without affecting the -30dB/decade part. The shift is more in the case of supply noise than substrate noise. This means that the sensitivity of phase noise to supply noise is more than that to substrate noise.

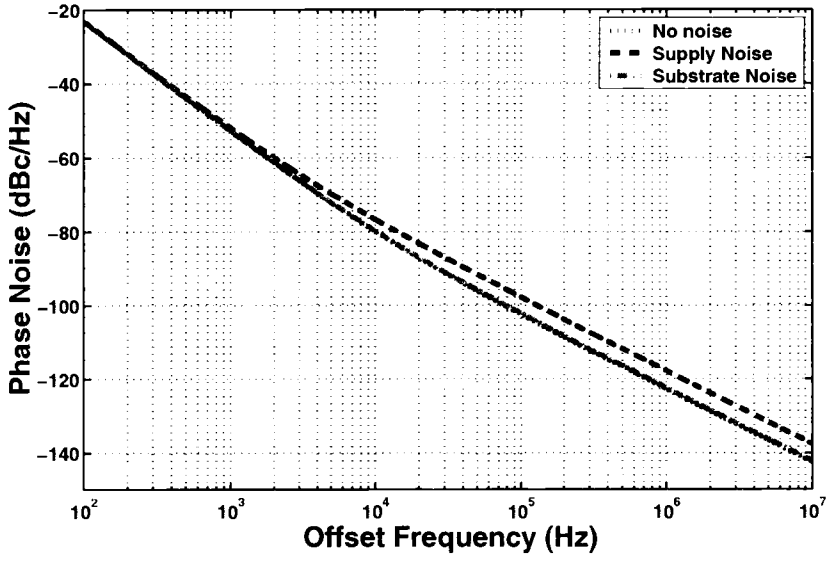


Figure 5.14. Phase noise in the presence of white noise in the supply and substrate.

The effect of 1/f noise present on supply and substrate is illustrated in Fig. 5.15. In this case, the flicker noise shifts the -30dB/decade part of the phase noise curve, leaving the -20dB/decade region unaffected. Similar to the white noise, flicker noise on the supply affects phase noise more than that in the substrate.

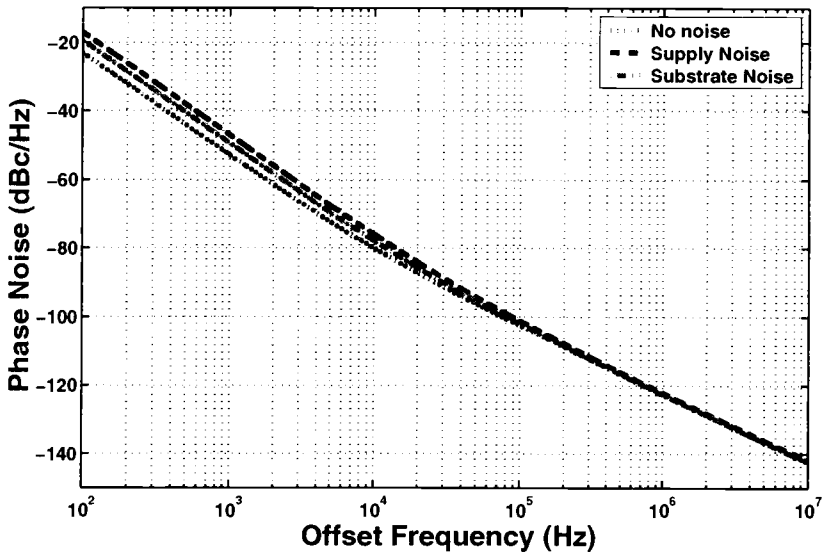


Figure 5.15. Effect of flicker noise in the supply and substrate on phase noise.

To study the effect of deterministic noise, a sinusoidal signal at a frequency of 100kHz was applied at the supply and substrate. The simulation results are plotted in Fig. 5.16. It can be observed that the deterministic signal at 100kHz shows up as a spike at 100kHz offset from the carrier without any change in the -20dB/decade or -30dB/decade region. This is expected as the oscillator is a nonlinear block. Therefore mixing of two frequencies will give the sum and difference of the frequencies. In this case the carrier frequency at f_{OSC} and the signal at 100kHz mix to produce the signal at f_{OSC}+100kHz. In this case too the supply noise is more dominant than substrate noise.

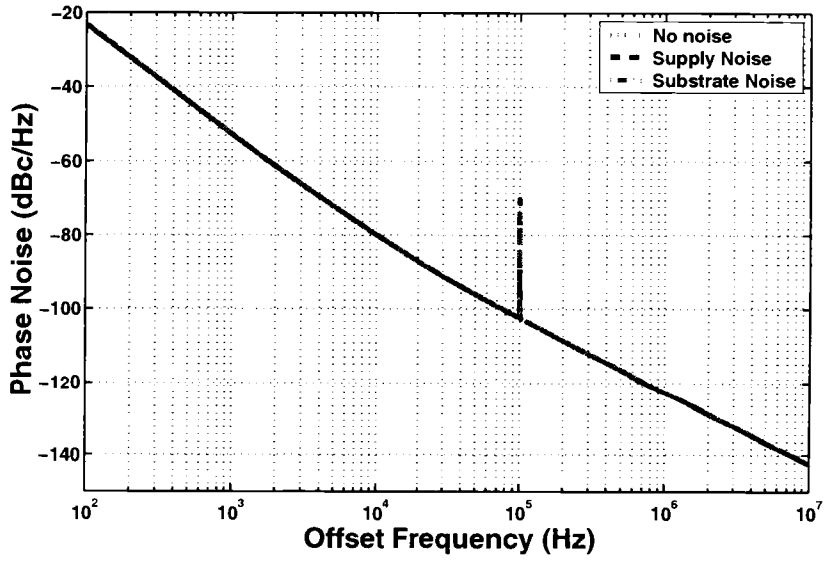


Figure 5.16. Phase noise in the presence of deterministic noise in the supply and substrate.

The conclusion from this exercise is that supply and substrate noise both affect phase noise and may need to be reduced. Supply noise is shown to be more influential on phase noise than substrate noise. One technique of reducing supply noise coupling is by using a voltage regulator.

In order to understand the effectiveness of a supply voltage regulator in reducing supply noise coupling to phase noise, a regulator was added to the circuit. Fig. 5.17 shows the simplified schematic of the regulator. The high resistance between the source and drain of the transistor provides the regulation. Addition of white and flicker noise on the supply lines increases the phase noise in both the regions (-20dB/decade and -30dB/decade) as seen from Fig. 5.18. The same plot shows the phase noise in the presence of the regulator. The presence of the regulator in the circuit curbs supply noise coupling. With the regulator in the circuit, the phase noise performance is similar to the one without any noise added. Thus it can be concluded that the regulator helps in rejecting supply noise. The measurements from a previous chip are consistent with the simulation results [25].

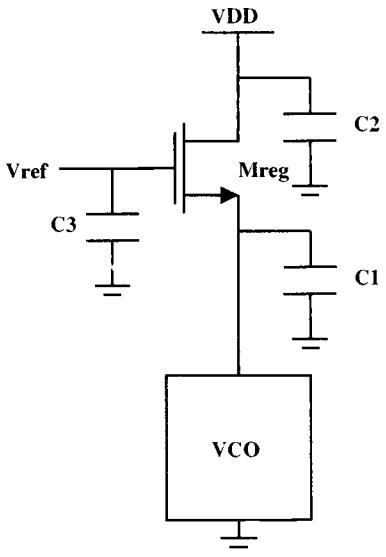


Figure 5.17. Schematic of supply voltage regulator.

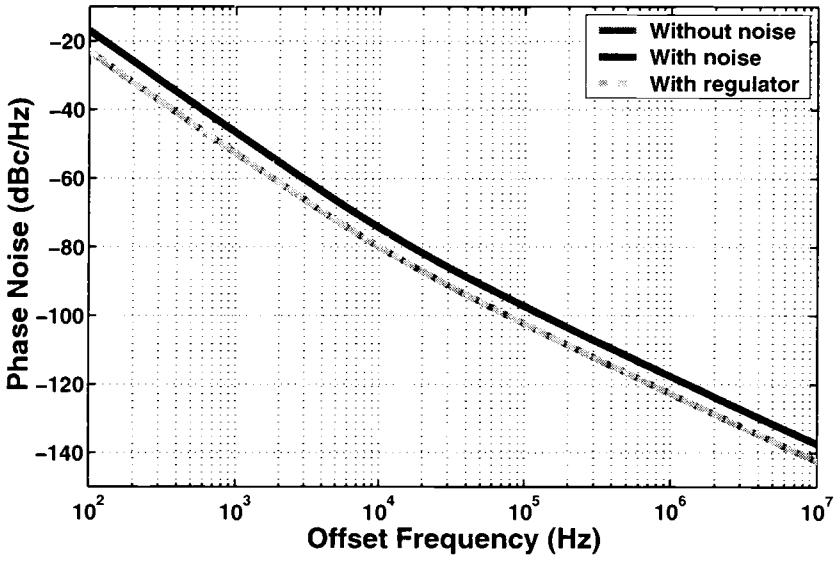


Figure 5.18. Comparison of phase noise in the absence and presence of a supply voltage regulator.

6. OSCILLATOR DESIGN

6.1. Specifications

The design of the oscillators was targeted for the Bluetooth specifications. The NMOS topology and the complementary oscillator were designed in the 0.25μm National BiCMOS process. Although the process was a BiCMOS process, the design was implemented in CMOS only. The center frequency of these oscillators was 2.4GHz. The critical specification for this standard is the phase noise in the third neighboring channel, i.e. -119 dBc/Hz at 3MHz offset. The other phase noise specifications are -100dBc/Hz at 500kHz offset and -110dBc/Hz at 2MHz offset from the carrier frequency. The desired tuning range is around 97MHz. It is also necessary to have a sufficient margin on these specifications to ensure that silicon meets the specifications. Low current consumption was one of the goals of this design. The voltage swing at the output of the oscillators was required to be at least 1 volt peak-to-peak. Although the Bluetooth tuning range specification is 4% of the carrier, a tuning range of about 20% was targeted. This was done in order to meet industry demands of around 10% variation on each side of the carrier. This larger tuning range specification ensures that the oscillator will be tunable to 2.4GHz inspite of any variations during the fabrication process.

6.2. Design of the Oscillator Core

The NMOS oscillator and the complementary oscillator were presented in Section 2.2. The oscillator core for both topologies along with the tail current sources are shown in Fig 6.1. Both the circuits have advantages and disadvantages.

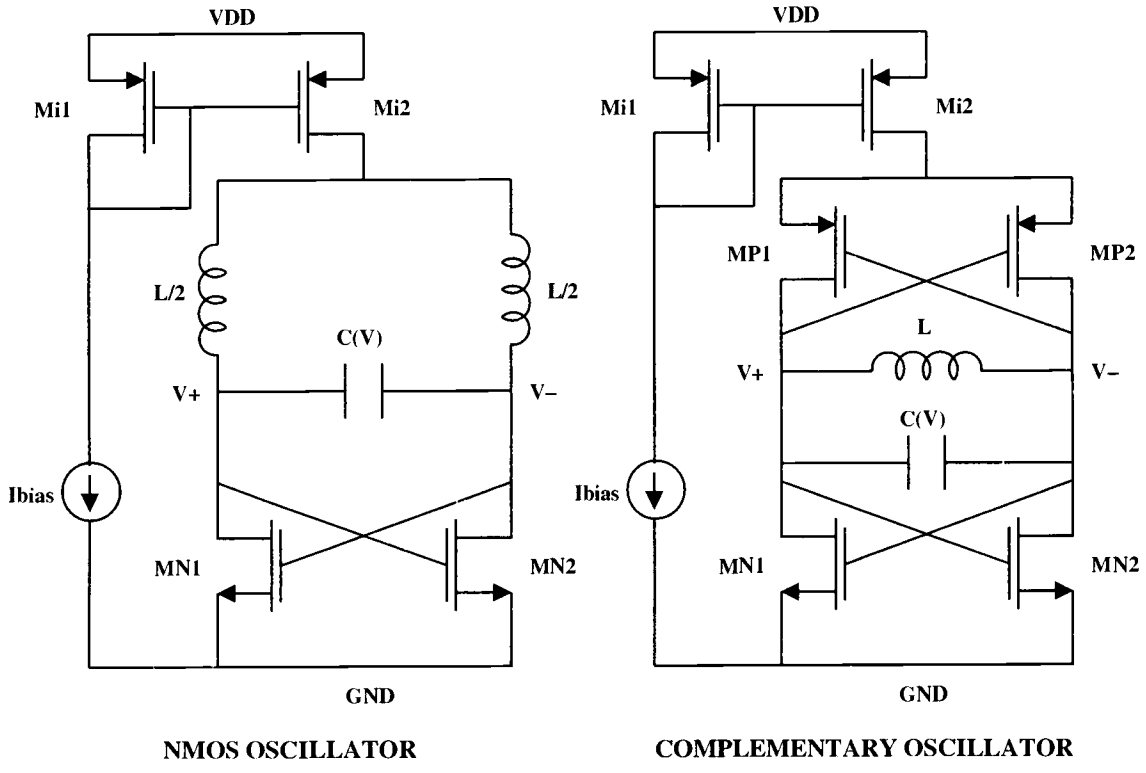


Figure 6.1. Oscillator core for complementary and the NMOS topologies with tail current sources.

According to [3] and [4], the circuit should be as symmetrical as possible and they suggest that the PMOS devices should be approximately 3 times wider than the NMOS devices in the complementary oscillator. This ensures the g_m of the NMOS and PMOS transistors to be similar since the mobility of the PMOS transistors (μ_P) is about three times smaller than the mobility of the NMOS transistors (μ_N). For the NMOS topology, only the cross-coupled NMOS transistors add parasitic capacitance to the tank, whereas for the complementary topology, both the NMOS and PMOS transistors increase the tank capacitance. Thus, the ratio of the fixed capacitance to the parasitic capacitance reduces in the complementary oscillator. This is a disadvantage as the parasitic capacitances change in the various region of operation of the device as well as with temperature and consequently change the oscillation frequency. A large oscillation frequency requires the passive device values to be small, and if the inductor values are fixed, the capacitances might be so small that the complementary structure would not be suitable. However for a center frequency of 2.4GHz, the values of capacitances required were realizable.

The complementary structure has the advantage of lower bias current required for startup. Another advantage of the complementary structure is the increased voltage swing as explained in Section 5.2.1. In order to compare the simulation results with measurements, both these oscillators were designed.

The current consumption of the NMOS oscillator core was selected to be 4mA, whereas for the complementary structure it was chosen to be 2mA. This choice was determined by the voltage swing required at the output of the oscillator and noting that the complementary oscillator has almost twice the swing for the same bias current. The cross-coupled transistors were chosen to have minimum channel length to reduce parasitic capacitances. For the complementary structure, the PMOS transistor widths were chosen to be three times the NMOS transistor

widths. Since the quality factor of the LC tank was not accurately known, the sizes of the cross-coupled pair were swept. Initially, the loop gain was not sufficient to start the oscillations. The value of g_m required to just start oscillations was noted and the sizes were adjusted to maintain twice the g_m required to just start oscillations. This ensured that the loop gain was about two. Also the current through the oscillator was kept adjustable so that the loop gain could be increased further, if required, during measurements.

Inductors from the National library were used. The NMOS oscillator had two 1nH inductors, whereas the complementary oscillator had a 2nH inductor. The simulations were performed using the pi-model for the inductors provided by National. A fixed capacitor was initially used for maintaining the frequency of oscillation and then varactors were introduced in the circuit.

The tail current source could be realized by either NMOS current mirrors or PMOS current mirrors. Since NMOS transistors have more flicker noise as compared to similar sized PMOS transistors, the PMOS current mirror was used for biasing. The current mirroring ratio was tweaked and the effect on phase noise was observed. For a ratio of 1:10, the power consumption was minimum, but as observed from Fig 6.2, the phase noise performance was inferior as compared to the 1:1 ratio case. With 1:1 mirroring ratio, the power consumption was almost double. The phase noise comparison indicates that the phase noise deterioration is predominant at lower offset frequencies due to the greater flicker noise of the current mirror MI1, and the effect on phase noise at the required frequency offsets i.e. 500kHz and above is less. Accordingly the decision was made in favor of lower power consumption.

The NMOS oscillator core along with the biasing consumed 4.5mA whereas the complementary one consumed 2.2mA from a 2.5V power supply. In Section 5.2.4, it was pointed out that the current mirrors should be designed with larger

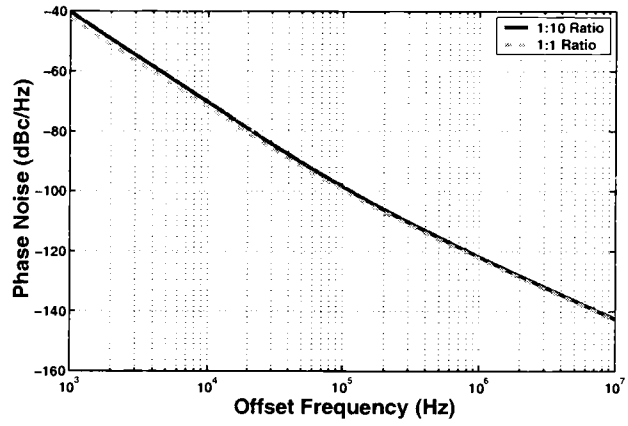


Figure 6.2. Comparison of phase noise for different current mirroring ratios.

lengths and their widths did not affect the phase noise significantly. This was taken into account while sizing the current mirrors.

Table 6.1 shows the designed values of the oscillator core. The value of the fixed capacitor mentioned in the table is the final value obtained after the buffers were added.

As explained in Section 4.4, PMOS transistors were used as varactors along with a switched capacitor array. A tuning range of about 400MHz was targeted. The schematic of the varactor circuit is shown in Fig. 6.3. Four capacitors were switched using NMOS transistors, implying 16 tuning steps from 0000 to 1111. Fig. 6.4 illustrates the ideal desired tuning curves. The K_{VCO} was required to be around 20MHz/V and to ensure continuous frequency tuning over process, voltage and temperature variations, the fine tuning range in simulation was assumed to be 2-3

Parameter	*NMOS Osc. Value*	*Comp. Osc. Value*
NMOS width W_N	400μm	120μm
NMOS length L_N	0.24μm	0.24μm
PMOS width W_P	-	360μm
PMOS length L_P	-	0.24μm
Current mirror width W_{i1}	80μm	80μm
Current mirror length L_{i1}	1.44μm	1.44μm
Current mirror width W_{i2}	800μm	800μm
Current mirror length L_{i2}	1.44μm	1.44μm
Fixed capacitor	1.4pF	1pF

Table 6.1. Designed values of the oscillator core.

times the coarse tuning step. The LSB of the coarse tuning is the step size when the bit B_0 changes from OFF to ON, with all other switches OFF. So the total frequency range in terms of LSBs is equal to 18LSBs, which implies 18LSBs = 400MHz. Hence 1LSB = 22.22MHz and 3LSBs = 66.66MHz. Thus the PMOS varactor should be capable of providing fine tuning of around 66MHz and the switched capacitor bank should have a LSB of 22MHz.

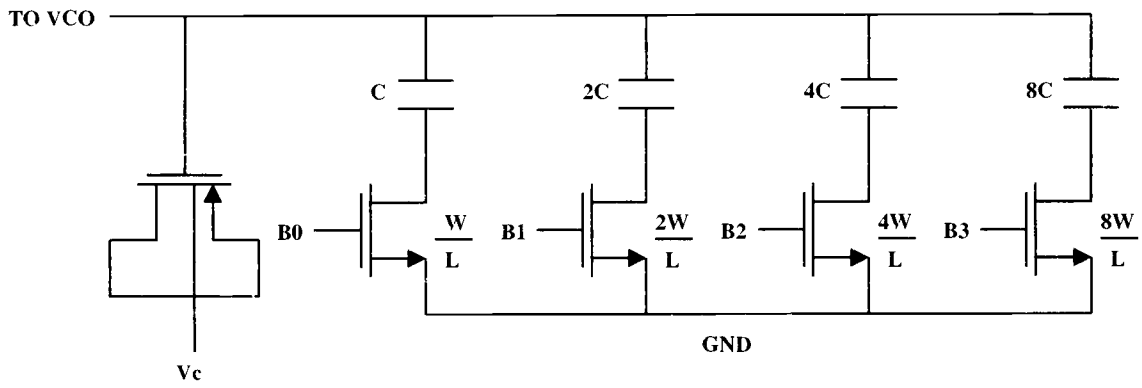


Figure 6.3. Capacitive tuning block consisting of PMOS varactor and four binary weighted capacitors.

The first step was to obtain the PMOS varactor capable of providing the fine tuning range. A PMOS accumulation varactor was simulated to obtain the desired tuning characteristics. The width of the varactor was designed to obtain a 66MHz tuning. The tuning curve obtained using a varactor with a width of $300\mu m$ and a length of $0.24\mu m$ is plotted in Fig. 6.5. It can be observed that the tuning range of the varactor is (2.339GHz - 2.2724GHz) = 66.86MHz over a control voltage of 4V, which gives a K_{VCO} around 16.7MHz/V. This value is in the desired range of 10-30MHz/V.

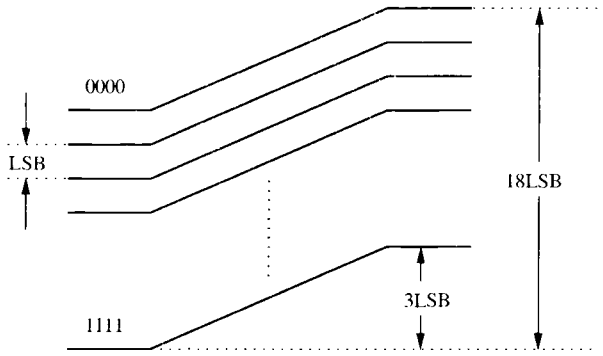


Figure 6.4. Tuning characteristics desired from the varactor of Fig. 6.3.

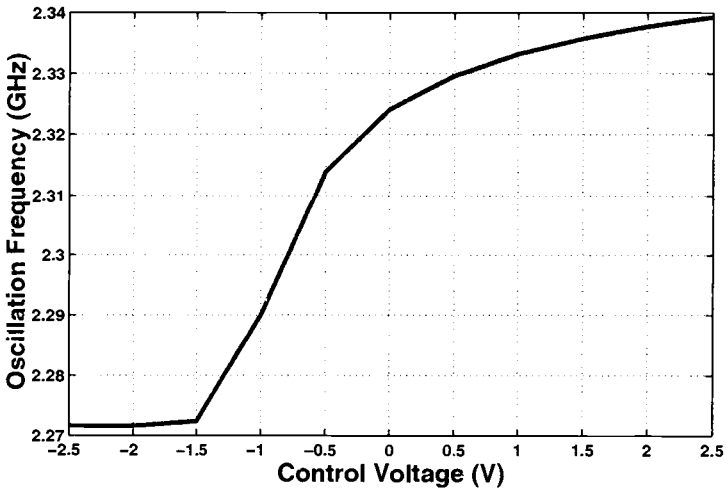


Figure 6.5. Tuning range of the PMOS varactor.

The next step was to determine the value of the binary weighted switched capacitor, C. The constraint on selecting the value of C was the LSB required. In order to observe the changes in the LSB when the switch state changes from OFF to ON, just the switch controlled by bit B_0 was used, as illustrated in Fig. 6.6. The switch size was fixed at $100\mu m/0.24\mu m$ initially. The difference in the oscillation frequency when B_0 is changed from 0V to 2.5V, with the varactor control voltage fixed, gives the LSB.

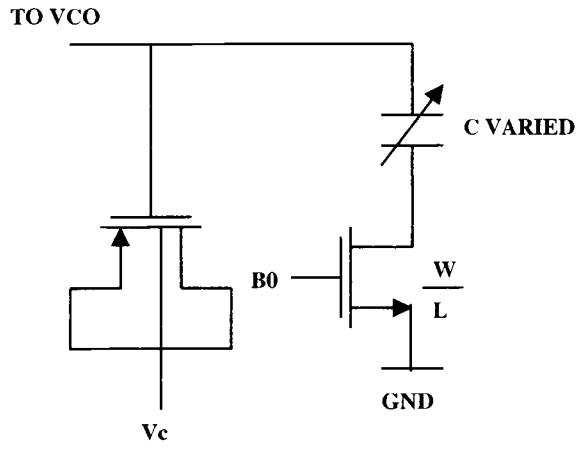


Figure 6.6. Varactor circuit to determine the value of C.

Simulations were performed in SpectreRF by sweeping the value of the capacitor C, for different control voltages. The difference between the oscillation frequencies when the switch was changed from the OFF to the ON state is plotted versus the capacitor value C in Fig. 6.7. As observed from the figure, as the value of C increases, the frequency of oscillation reduces and hence the difference between the oscillation frequencies in the OFF and the ON state increases. In order to obtain a LSB of around 25MHz, the value of C should be between 125fF and 150fF.

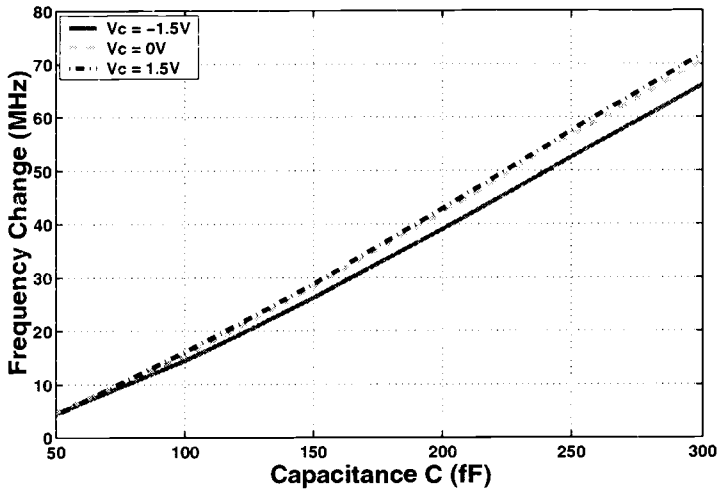


Figure 6.7. Oscillation frequency change plotted as a function of the capacitor value.

Once the value of C was determined, the switch sizes were designed. The sizing of the switches is also critical. When the switches are ON, the ON resistance causes the quality factor to degrade. The thermal noise of the switches degrades the phase noise. The ON resistance of the switches, which operate in the linear region, is given by

$$R_{ON} = \frac{1}{K'W_S/L_S(V_{GS} - V_{TH})}. \tag{6.1}$$

One way of reducing the ON resistance is by increasing the width of the switches, since the lengths are designed to be the minimum channel length. If the width is increased, the parasitic capacitance of the switch also increases. This capacitance is not desirable when the switch is turned OFF. The reason for this is as follows. When the switch is OFF, we expect no capacitance to be added to the varactor. The binary weighted capacitance C and the parasitic capacitance are

in series and their effect is still present in the varactor. Since the binary weighted capacitance C is itself small, the parasitic capacitance could dominate and therefore the varactor might see a capacitance C which is the same as what it sees when the switch is OFF. This causes the tuning characteristics of the oscillator to deteriorate. Thus a trade-off is necessary to decide the switch sizes.

The trade-off was done based on the data shown in Table 6.2. This data was obtained by using 4 switches whose width was swept and the ON resistance and phase noise were noted when the switch was ON, and the capacitance contributed by the switches was noted when the switches were OFF.

Width of LSB switch	R_{ON}	Phase Noise @ 1MHz	C_{switch}
25μm	40.86Ω	-115.034dBc/Hz	35.829fF
30μm	34.32Ω	-115.886dBc/Hz	42.928fF
40μm	26.09Ω	-116.944dBc/Hz	57.135fF
50μm	21.09Ω	-117.611dBc/Hz	71.33fF
100μm	10.92Ω	-119dBc/Hz	142.35fF
200μm	5.67Ω	-119.723dBc/Hz	284.33fF

Table 6.2. Variation of ON resistance and OFF capacitance with switch size.

Choosing the switch width of 50μm or smaller implied the switch capacitance would be around one-third of the binary weighted capacitance. But the phase noise performance would be degraded by 1.5dBc/Hz or more, for switches below 50μm

width. Going from 50μm to 100μm, the capacitance increased to almost the binary weighted capacitance value, which was undesirable. Consequently the switch size was chosen to be 50μm. With this value for the switch width, the binary weighted capacitor was modified to 150fF for the desired tuning characteristics.

The final designed values of the frequency tuning circuit are as shown in Table 6.3.

Parameter	*Value*
PMOS varactor width	300μm
PMOS varactor length	0.24μm
LSB switch width	50μm
LSB switch length	0.24μm
Capacitor C	150fF

Table 6.3. Designed values of the tuning circuit.

The tuning characteristics for both the oscillators were obtained by using a PERL script which swept the control voltage of the varactor and also the bits of the binary switched capacitor array. The tuning characteristics for the NMOS oscillator are shown in Fig. 6.8, whereas the one for the complementary oscillator are shown in Fig. 6.9.

From these plots it can be observed that the curves are not exactly offset from each other by the same amount. This would have been true in an ideal case when the binary weighted array did not contribute any capacitance when it was

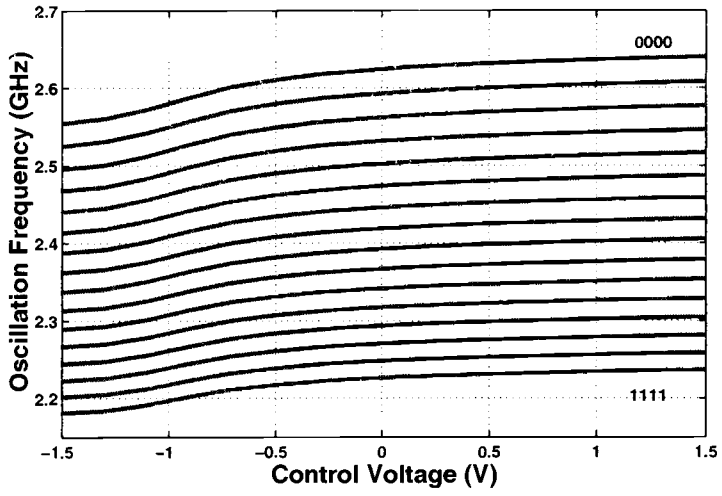


Figure 6.8. Tuning range of the NMOS oscillator.

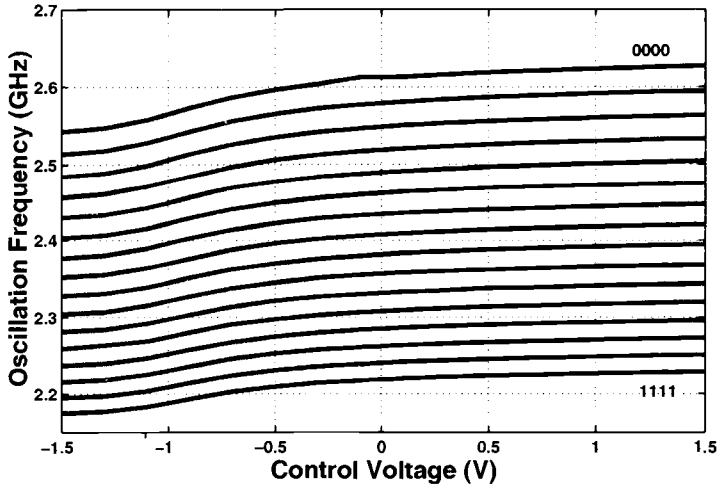


Figure 6.9. Tuning range of the complementary oscillator.

OFF. However, capacitance is present in the ON and OFF states of the switches. As a result, the curves are shifted by unequal amounts depending on how many switches are ON and how many are OFF. One more thing to observe is that the curves have smaller C_{MAX}/C_{MIN} ratio as more switches are turned ON and lower C_{MAX}/C_{MIN} as switches are being turned OFF. When the capacitances are added in the ON state, the varactor capacitor ratio is deteriorated as shown by the following equation

$$\frac{C_{MAX}}{C_{MIN}} < \frac{C_{MAX}+C}{C_{MIN}+C}. \tag{6.2}$$

Accordingly, the tuning curve is affected and the curves deviate from the desired characteristics.

The tuning range obtained for the NMOS oscillator was 452MHz compared to 446MHz for the complementary oscillator.

6.3. Buffer Design

In order to prevent the loading of the oscillator core, source followers were used to buffer the oscillator output. The schematic of the buffer is shown in Fig. 6.10. Two buffers were used, one for each of the differential outputs. Since the output of the buffers are probed, the simulations were performed with a series RC network representing the pad resistance and capacitance. The resistance was 20Ω and the pad capacitance was 400fF. A 50Ω resistance was added in parallel with this to model the terminating impedance looking into the RF probes. A separate supply was used for the buffers.

The buffers were capacitively coupled to the core. This enabled the buffers to be biased independent of the oscillator common mode voltage. A simple biasing circuitry comprising of diode connected transistors along with a resistance of

$5k\Omega$ was used to bias the source followers (Appendix C). The sizing of these diode connected transistors was obtained such that the gate-source voltage provided the voltage necessary for buffer biasing.

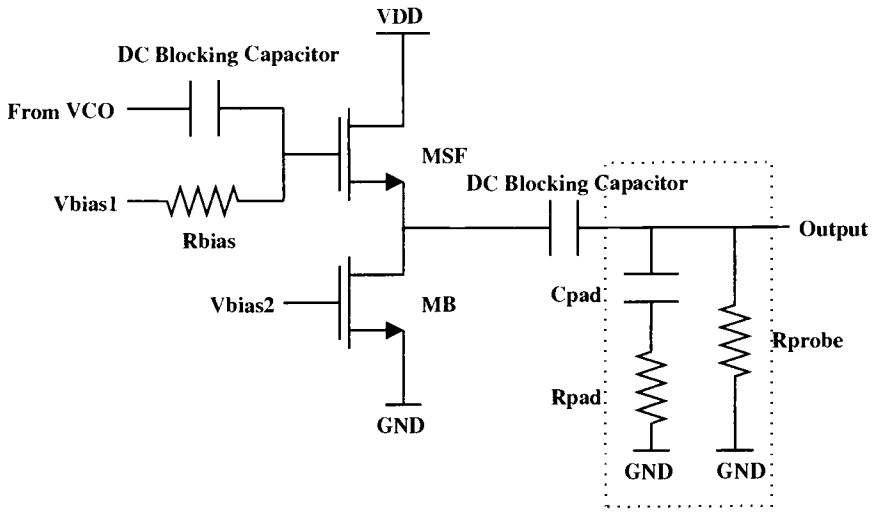


Figure 6.10. Simplified schematic of the buffer.

To decide the amount of current to be pumped into the buffer to get a reasonable performance, transient simulations were performed on just the buffer by varying the bias current. The source follower was biased with the appropriate voltage, as it would be in the presence of the oscillator. The results of the simulation are shown in Fig. 6.11.

It can be observed that the waveform is distorted as the current reduces. For 5mA current, the waveform is highly distorted and the performance is best for 20mA. Hence, a 15mA current was used for the buffer and the current was made adjustable in case it would be necessary to increase the current during measurements. A biasing

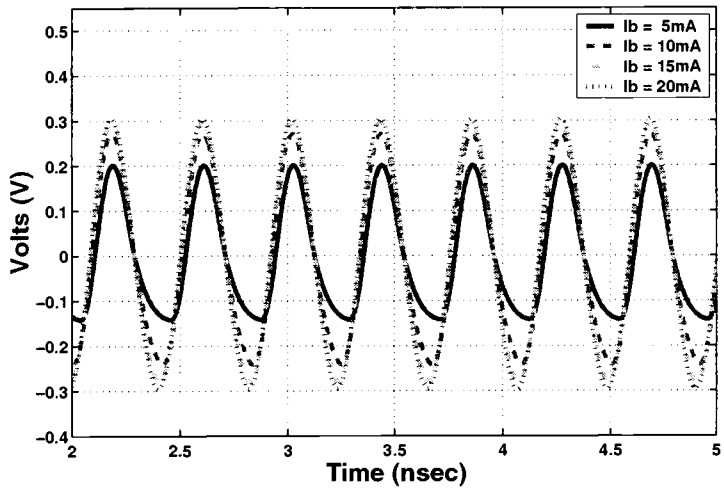


Figure 6.11. Output waveform of the buffer for different buffer currents.

current of 1mA was used and a 1:15 mirroring ratio provided the necessary current through the source followers.

The sizing of the source follower transistors was decided by noting that these transistors contributed considerable noise and deteriorated the phase noise performance. This can be observed from Fig. 6.12 where the phase noise is plotted for various source follower transistor widths.

As observed from Fig. 6.12, it is desirable to keep the source follower widths small for better phase noise performance. However, smaller widths would increase the dc level shift provided by the source follower. Since the signals at the output of the buffer are large, if the dc shift is also large, the biasing transistors may enter the non-saturation region. As a trade off, the width of the source followers was chosen as 500μm.

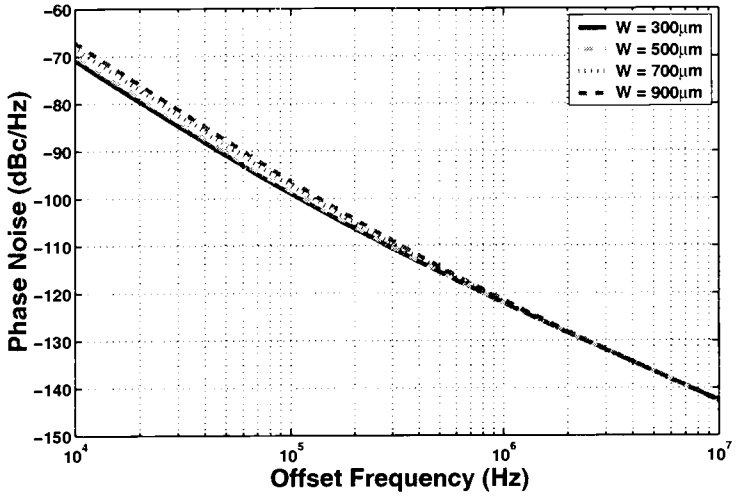


Figure 6.12. Phase noise plot for different values of the source follower transistor width.

One more parameter to be decided was the value of the DC blocking capacitors. The plots of the ac response of the buffer are illustrated in Fig. 6.13. As the capacitor is swept from 5pF to 20pF, the gain from the output of the oscillator core to the output of the buffer increases. This is expected since the increase in capacitance implies its impedance to the ac signal reduces, thereby the ac drop across the capacitor decreases, which improves the gain. For area considerations, a 6.5pF capacitance was used.

Table 6.4 shows the designed values of the buffer components. Except for the current mirrors, the channel lengths for all transistors was chosen as the minimum channel length.

Fig. 6.14 shows the ac response of the designed buffer. At lower frequencies, the blocking capacitors are responsible for the low gain and at higher frequencies, the roll-off is due to the source follower frequency response.

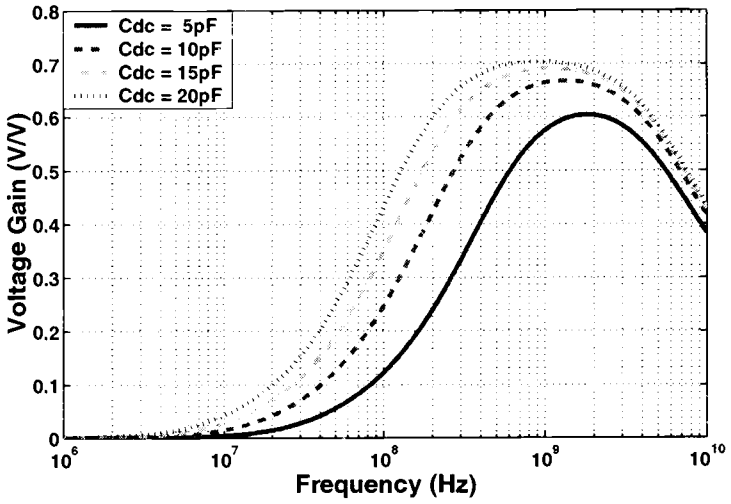


Figure 6.13. AC response of the buffer for various values of the DC blocking capacitor.

Parameter	*Value*
Source follower width	500μm
Source follower length	0.24μm
Bias transistor width	1500μm
Bias transistor length	1.44μm
Diode connected transistors width	50μm
Diode connected transistors length	0.24μm
DC blocking capacitor C_{DC}	6.5pF
R_{bias}	4.23kΩ

Table 6.4. Designed values of the buffer circuit.

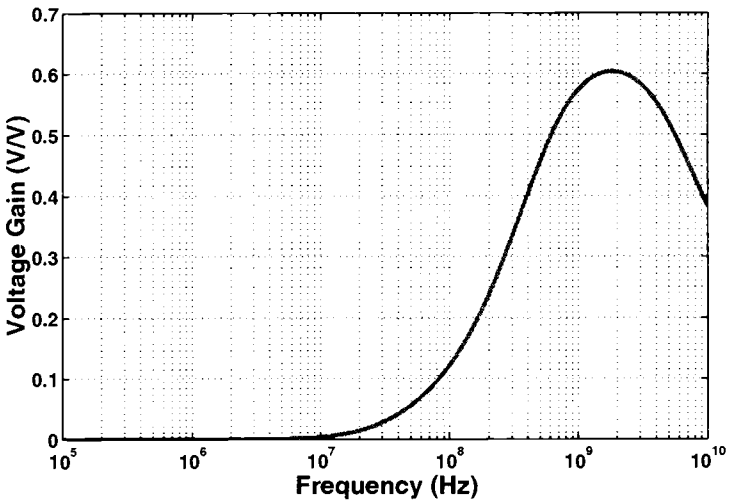


Figure 6.14. Frequency response of the buffer, including the effect of the dc blocking capacitors.

The complete schematics of both oscillators are given in Appendices A and B.

6.4. Layout Considerations

The performance of analog integrated circuits is heavily dependent on layout [36], [38]. Matching of devices plays an important role in the circuit performance, especially for differential circuits. Any mismatch between the components results in increased offset voltage, higher current mismatch and even-order distortion, which deteriorate the circuit performance. The layout should be such that the parasitics are minimal. Parasitic capacitances will cause the frequency of oscillation to vary.

The issue with any differential circuit is the symmetry between the two halves of the circuit. Any asymmetry in the two sides of the oscillator will cause an unbal-

ance in the tank causing the center frequency to change. Accordingly both halves of the oscillator were laid out identically.

The resistors and capacitors were surrounded by dummies to improve the matching between them. The switched capacitor bank was laid out such that the linear gradients along the wafer caused minimum mismatch. All transistors were interdigitated to minimize the gradient errors.

An important consideration during the layout of the oscillators is the metal width. The resonating tank causes the current in the tank to be Q times larger than the oscillator bias current. Consequently the metal lines connecting the tank components were sufficiently wide to withstand the large currents [35].

Since the resistance of the metal lines degrades the quality factor of the tank, utmost care was taken to see that the metal lines are not unnecessarily long. The resistance was further reduced by using the topmost metal layer due to its low resistivity and by stacking the top two metal layers. Contacting the gates of the cross-coupled pair on both ends reduced the gate resistance by four times, thereby improving the tank quality factor.

Figs. 6.15-6.16 show the layout of the NMOS oscillator and the complementary oscillator, respectively. Both layouts are identical except for the cross-coupled pair and inductor layout. The symmetry in the two halves is evident. In the NMOS oscillator, the two inductors were kept as far apart as possible to reduce any unwanted coupling between them. Each oscillator occupies an area of $840.6\mu m \times 1475.6\mu m$.

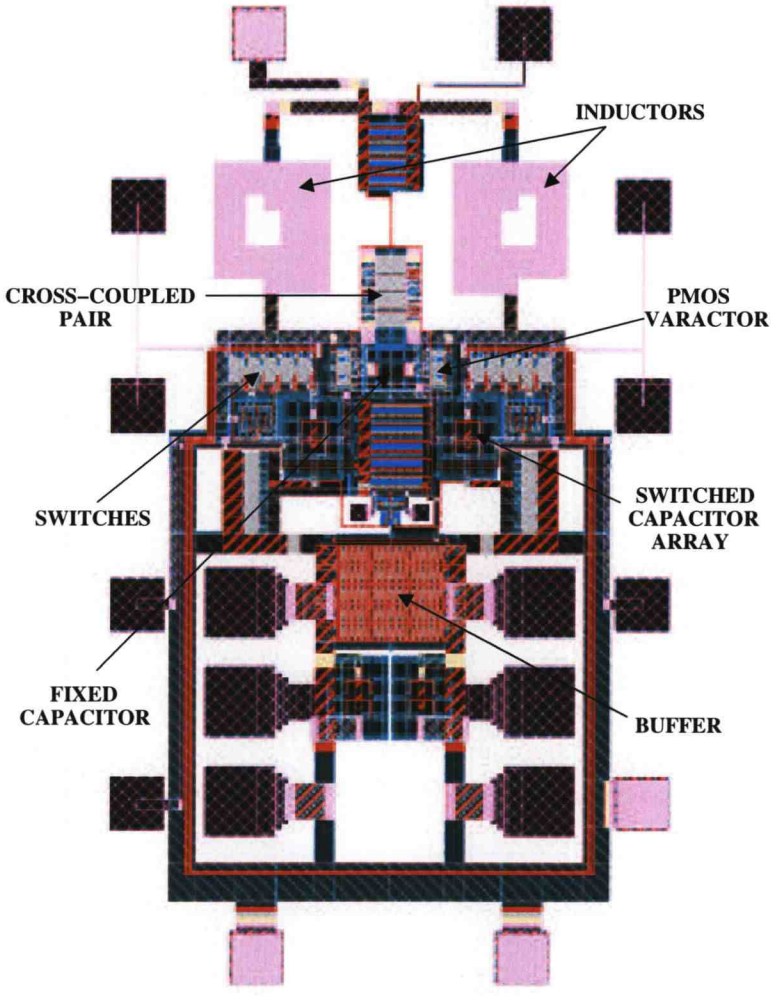


Figure 6.15. Layout of the NMOS oscillator.

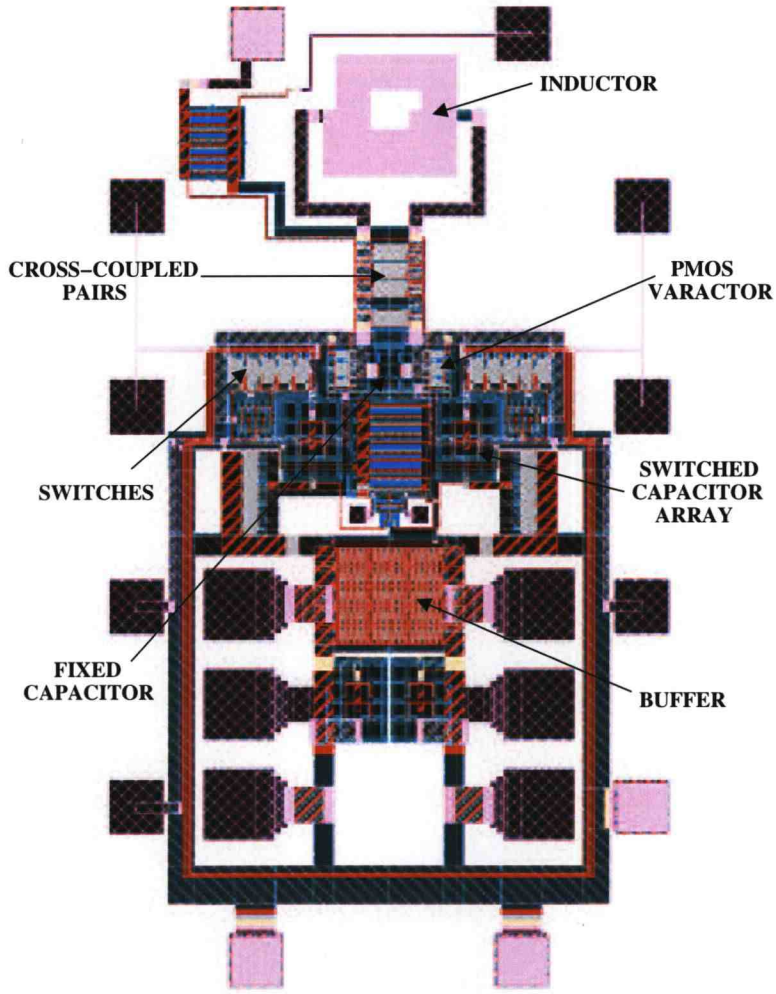


Figure 6.16. Layout of the complementary oscillator.

6.5. Simulated Performance

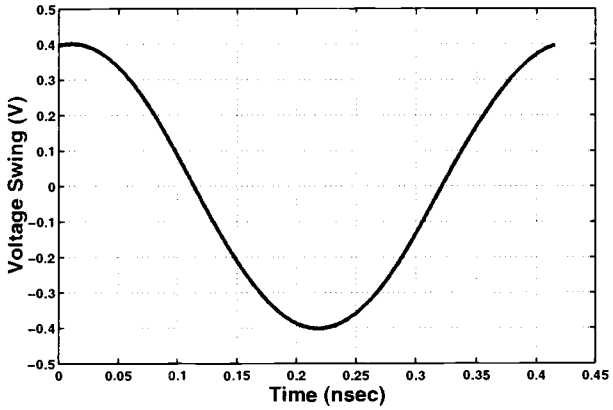
The output voltage waveforms over one period, obtained from SpectreRF PSS analysis, for both the oscillators is shown in Fig. 6.17.

The harmonic content of the two signals shown in Fig. 6.17 is shown in Fig. 6.18. For the NMOS oscillator, the third harmonic is 41.20dB below the fundamental whereas for the complementary oscillator the third harmonic is 44.96dB below the fundamental. Normally, a third harmonic suppression of around 45dB is considered reasonable. In this case, the complementary oscillator has good third harmonic suppression.

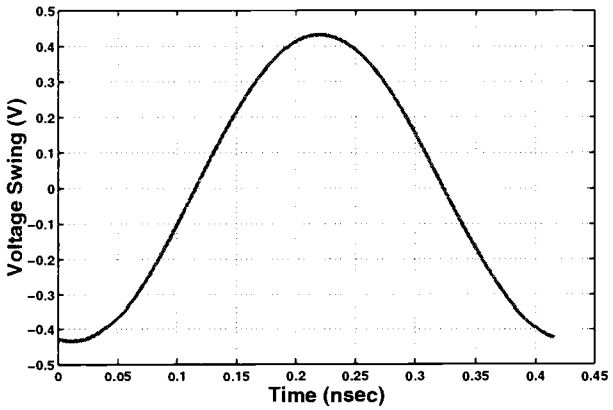
The simulated performance of the two oscillators along with the specifications is shown in Table 6.5.

It can be observed from Table. 6.5, that at 3MHz offset from the carrier, the phase noise has a margin of 13dBc/Hz over the specification. Also the tuning range is well above the required value. Another point to note which has already been discussed earlier, is that for half the current consumption, the complementary oscillator has the same swing as the NMOS oscillator and hence has similar phase noise performance. Thus, the complementary oscillator outperforms the NMOS oscillator. The phase noise plots for both the oscillators is shown in Fig. 6.19.

The noise contributors for the two oscillators at various frequencies are illustrated in Figs. 6.20-6.21. At 1kHz offset from the carrier, the flicker noise due of the tail current source (MI1) is the most significant contributor of phase noise, whereas at 3MHz offset, the thermal noise due to the inductors is the most dominant.

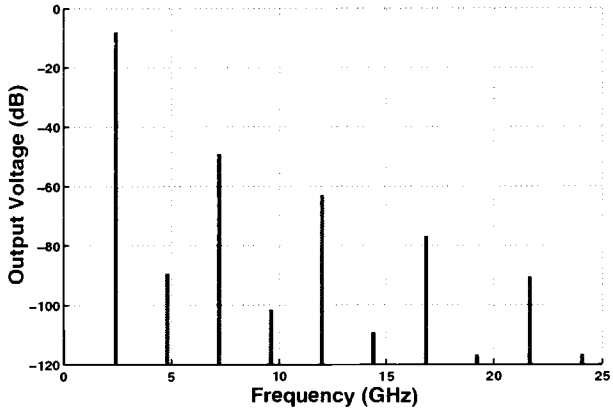


(a)

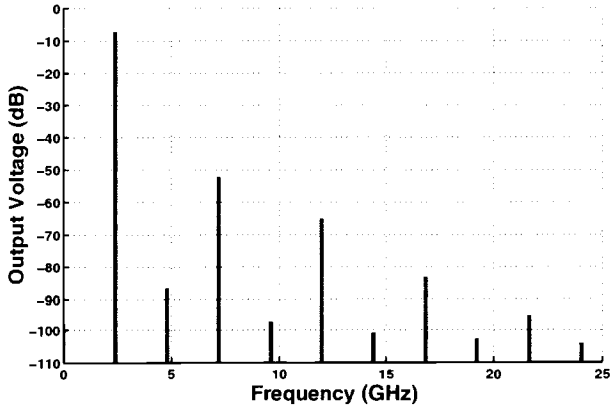


(b)

Figure 6.17. Simulated output voltage waveforms. (a) NMOS oscillator. (b) Complementary oscillator.



(a)

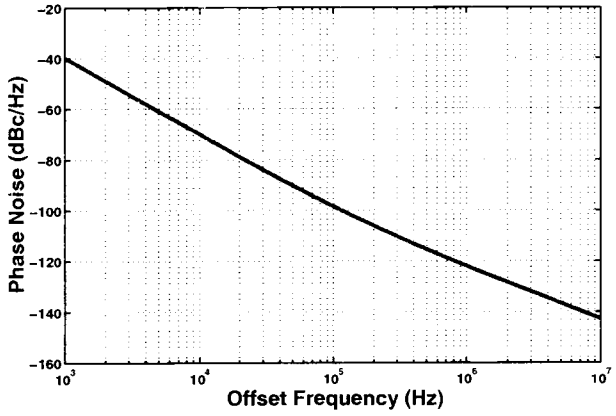


(b)

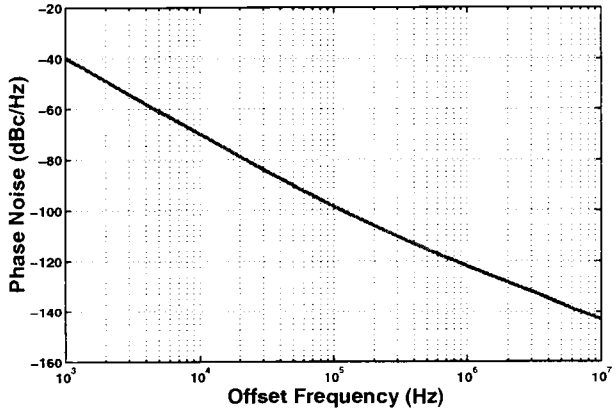
Figure 6.18. Fundamental and the harmonics in the output waveforms. (a) NMOS oscillator. (b) Complementary oscillator.

Parameters	Bluetooth Specs	Simulations NMOS VCO	Simulations COMP VCO
Frequency	2.4GHz	2.4GHz	2.4GHz
Output Voltage Swing	-	0.8Vpp	0.862Vpp
Phase Noise @ 500kHz	-100dBc/Hz	-116dBc/Hz	-115dBc/Hz
Phase Noise @ 2MHz	-110dBc/Hz	-128dBc/Hz	-128dBc/Hz
Phase Noise @ 3MHz	-119dBc/Hz	-132dBc/Hz	-132dBc/Hz
Supply Voltage	-	2.5V	2.5V
Current Consumption	-	4.46mA	2.22mA
Power Dissipated	-	11.14mW	5.55mW
Tuning Range	97MHz	452MHz	446MHz

Table 6.5. Comparison of specifications with simulated results.



(a)



(b)

Figure 6.19. Simulated phase noise plots. (a) NMOS oscillator. (b) Complementary oscillator.

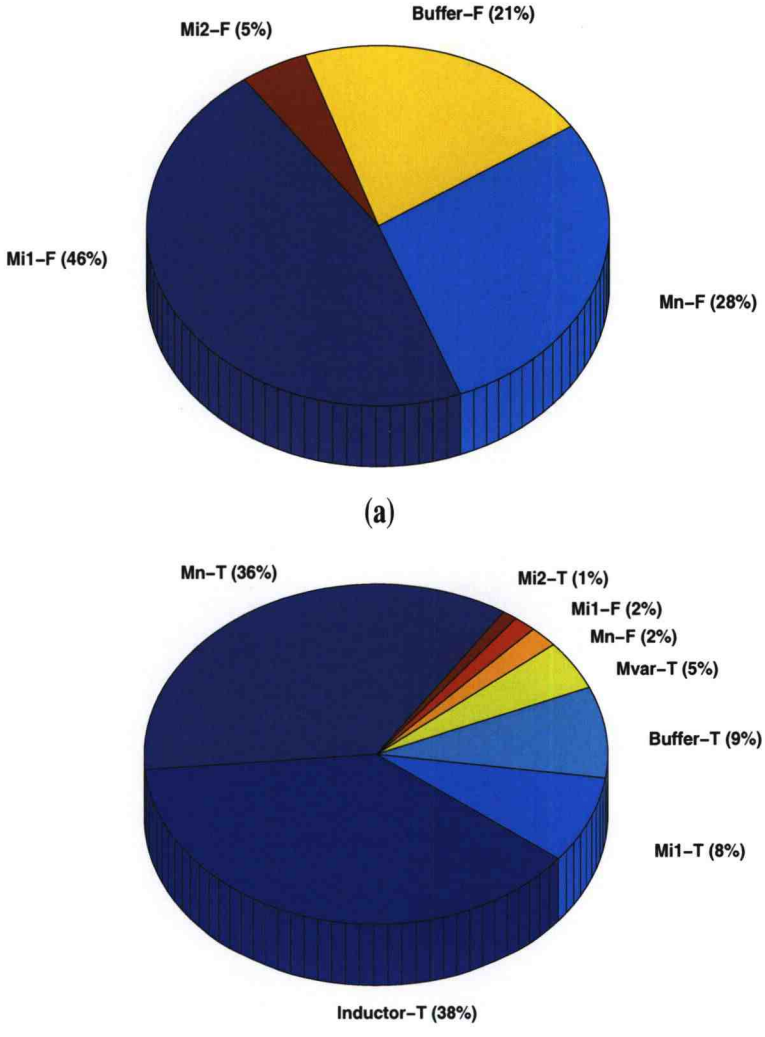
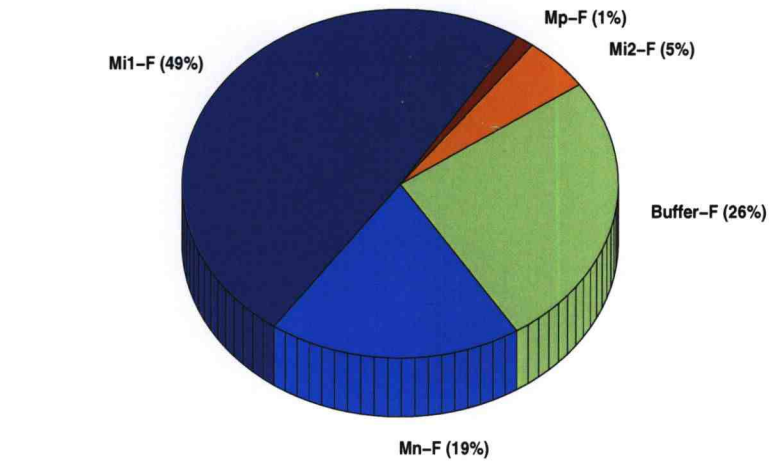
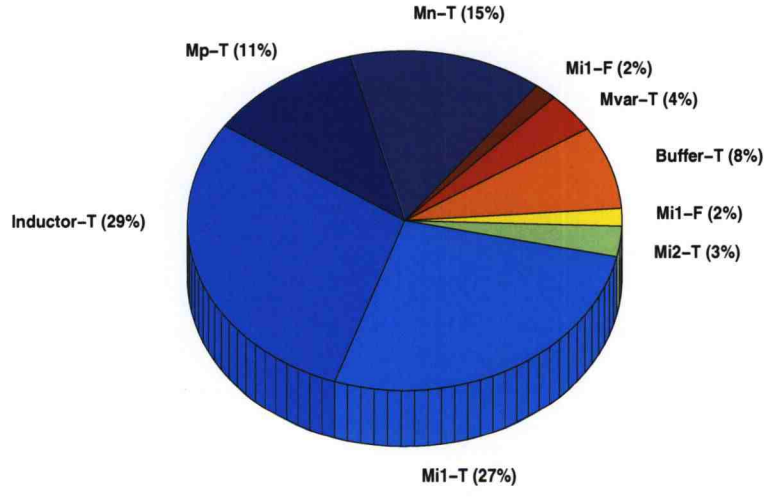


Figure 6.20. Phase noise contributors in the NMOS oscillator at the following frequencies: (a) 1kHz offset from the carrier. (b) 3MHz offset from the carrier.



(a)



(b)

Figure 6.21. Phase noise contributors in the complementary oscillator at the following frequencies: (a) 1kHz offset from the carrier. (b) 3MHz offset from the carrier.

7. MEASUREMENTS

7.1. Measurement Set-up

The two oscillators were fabricated in the 0.25μm National BiCMOS process. The die photographs of the two oscillators are shown in Figs. 7.1-7.2.

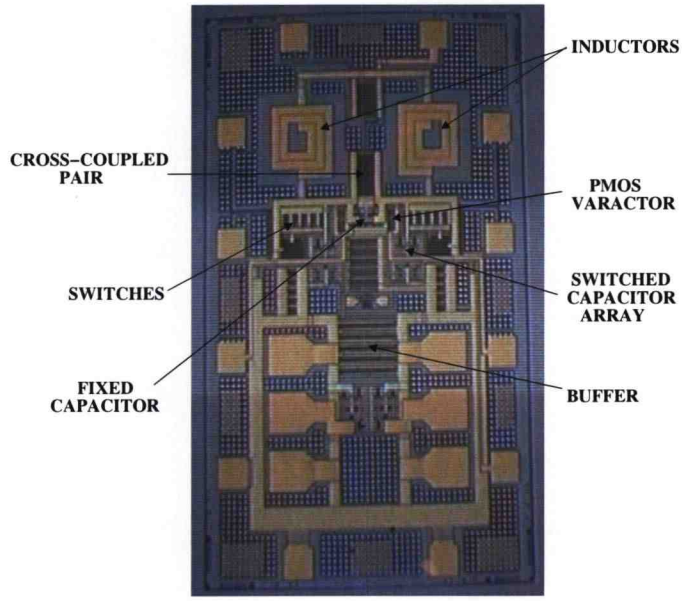


Figure 7.1. Die photo of the NMOS oscillator.

A probe card was used to bias the oscillators. The measurement set-up consisted of a CASCADE probe station with a probe card holder and a HP89441 Vector Signal Analyzer. Linear power supplies from Power Designs Inc. were used for precision dc voltages since they are cleaner than switching power supplies. An HP34401A multimeter was used to monitor the current through the oscillators and an universal counter HP53132A was used to measure the oscillation frequency. The

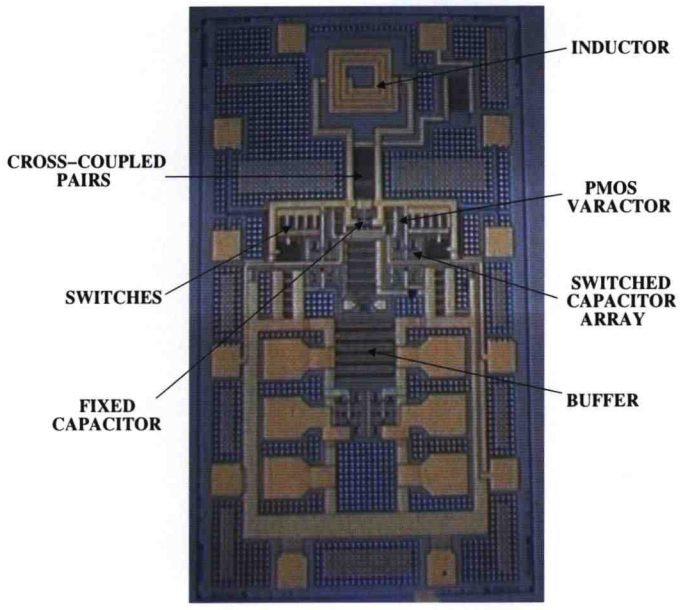


Figure 7.2. Die photo of the complementary oscillator.

RF signal at the output of the oscillator was probed using 3GHz active probes. Active probes utilize an active component such as a FET as a buffer. The FET input results in a larger input impedance, i.e., a larger input resistance (typically > 20kΩ) and a low input capacitance (typically < 1pF). The measurements were done in a screen room to shield the measurements from external noise. The use of passive probes was not possible due to the tight spacing the DC and RF probe pads.

7.2. Measurement Results

The tuning range of both oscillators was measured for two different cases. In the first case, the control voltage was applied to the bulk terminal of the PMOS varactor and its drain-source terminals were maintained at -1.5 volts. In the second

case, the bulk node of the varactor was connected to Vdd and the voltage on its drain-source terminals was swept. The tuning characteristics of both oscillators are shown in Figs. 7.3-7.6. For the NMOS oscillator, the oscillator current was 5.6mA with buffer current of 39.3mA, while the complementary oscillator had 4.6mA oscillator current and 34.9mA buffer current.

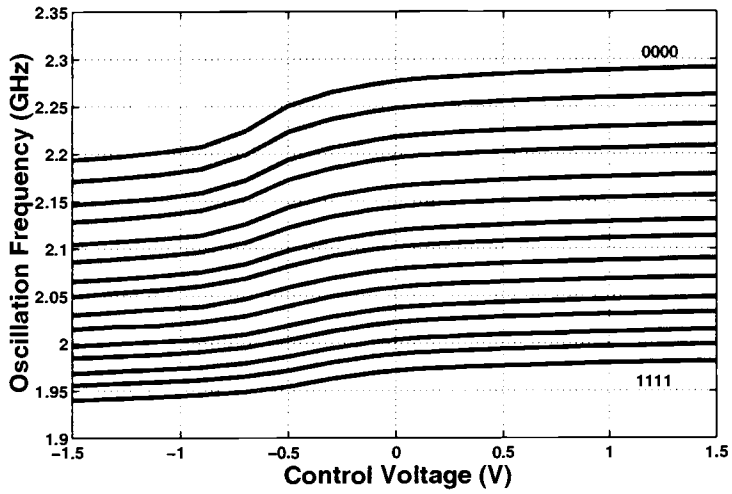


Figure 7.3. Tuning range of the NMOS oscillator with the bulk terminal swept.

Although the oscillators were designed to have a center frequency of 2.4GHz, the measured center frequencies were 2.11GHz and 2.19GHz. This shift in the center frequency corresponds to about 20% increase in the LC product. One reason for lower center frequency could be due to larger parasitic capacitances than expected. These parasitic capacitances would include interconnect capacitance, MOS parasitic capacitance and inductor capacitance to the substrate. The solution to this problem would be to layout the oscillators with capacitances that could be cut using the

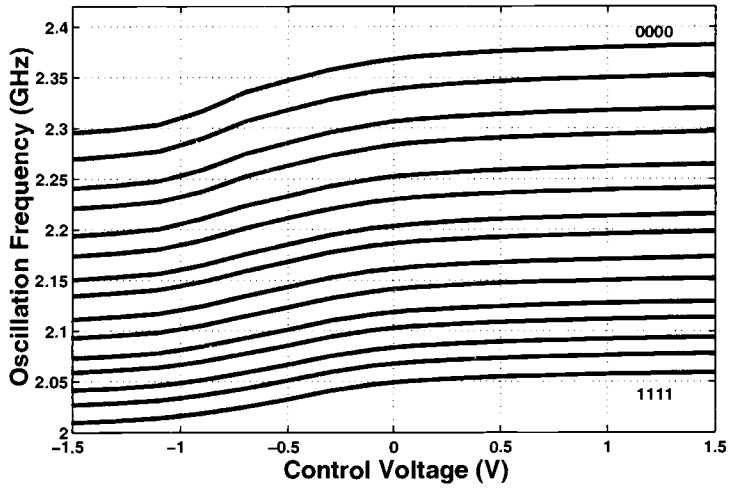


Figure 7.4. Tuning range of the complementary oscillator with the bulk terminal swept.

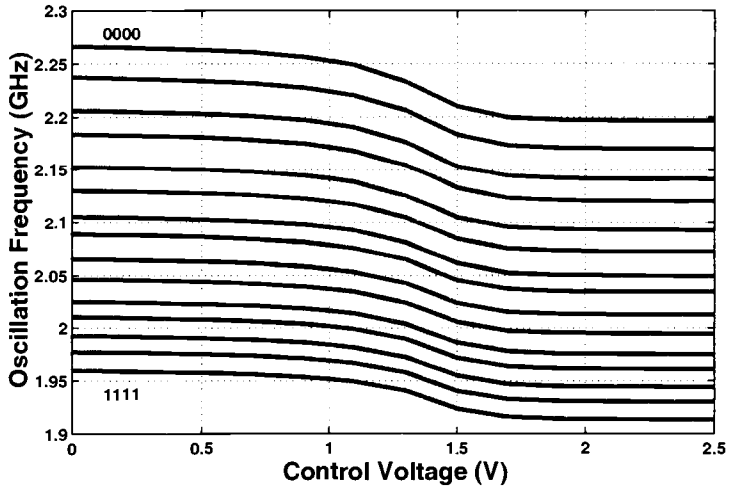


Figure 7.5. Tuning range of the NMOS oscillator with the drain-source terminals swept.

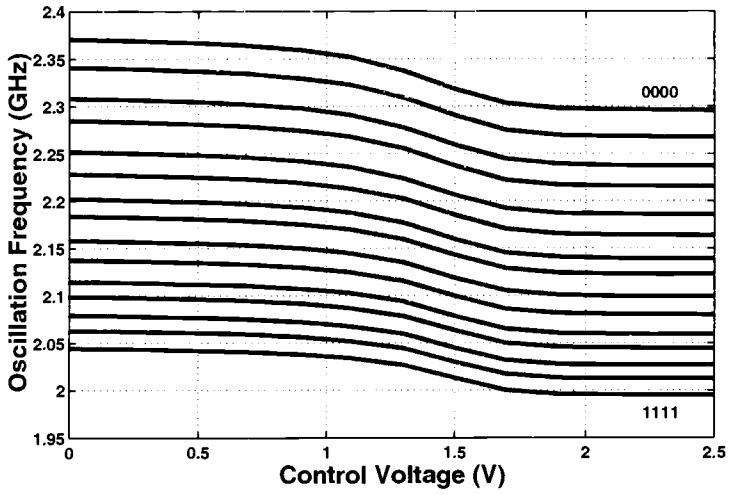


Figure 7.6. Tuning range of the complementary oscillator with the drain-source terminals swept.

laser if need be. The inductors used in the oscillators were not characterized in this fabrication run. Differences between the modeled and fabricated inductors could also cause the frequency to deviate. The parasitic extraction of the layout was performed on an earlier version of the extraction tool and it had some known problems. Extractions performed on the new environment might show different parasitics. Another important factor affecting the center frequency is the use of active probes. Since the active probes capacitively load the oscillator tank, the frequency would reduce.

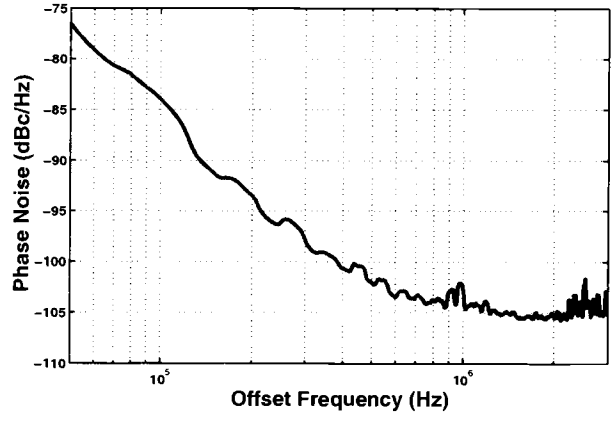
With the bulk terminal swept, the tuning range achieved with the NMOS oscillator was 363MHz and 385.75MHz for the complementary oscillator. The tuning range obtained with the drain-source terminals swept was 364.25MHz for the NMOS oscillator compared to 387MHz for the complementary oscillator. Although the

tuning range is the same independent of which terminal is varied, the difference in the two tuning curves is evident from VCO gains (K_{VCO}) of the two characteristics. For the complementary oscillator, the K_{VCO} is between 15-26MHz/V when the control voltage is applied to the bulk of the PMOS varactor whereas it is between 24-37MHz/V with the control voltage applied to the drain-source terminals. Using the bulk terminal as the control node reduces the VCO gain, thereby minimizing the amplification of noise on the control node. This result is consistent with the simulation results as explained in Section 4.3.

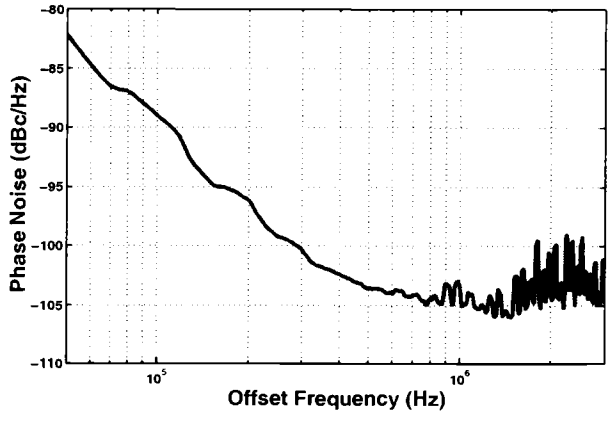
The strength of the output signal was very low, i.e., around -20dBm. Hence it was not possible to get reliable phase noise measurements beyond 1MHz. One of the reasons for the low signal power could be larger parasitic resistances of the interconnects and the inductor which could have drastically reduced the quality factor of the tank. The attenuation due to the active probes used for measurements also reduced the signal strength. Fig. 7.7 shows the phase noise curves of the NMOS and complementary oscillator. The current through the NMOS oscillators was 5mA whereas the complementary oscillator had 2.5mA current. These values of current were larger than those used in simulations because the oscillators did not oscillate at smaller currents. This could be due to the lower quality factor of the circuit than expected. Since the measurements were noisy beyond 1MHz, the curves were extrapolated with a -20dB/decade line to predict the phase noise at 2MHz and 3MHz offset from the carrier.

The measured performance of the two oscillators and the Bluetooth specifications are shown in Table 7.1.

The NMOS oscillator fails to meet the specification at 3MHz offset. Increasing the oscillator current will reduce the phase noise but increase the power consumption.



(a)



(b)

Figure 7.7. Measured phase noise plots. (a) NMOS oscillator. (b) Complementary oscillator.

Parameters	Bluetooth Specs	Measurements NMOS VCO	Measurements COMP VCO
Frequency	2.4GHz	2.11GHz	2.19GHz
Phase Noise @ 500kHz	-100dBc/Hz	-101.9dBc/Hz	-103.6dBc/Hz
Phase Noise @ 2MHz	-110dBc/Hz	-113.9dBc/Hz	-115.6dBc/Hz
Phase Noise @ 3MHz	-119dBc/Hz	-117.5dBc/Hz	-119.2dBc/Hz
Supply Voltage	-	2.5V	2.5V
Current Consumption	-	5mA	2.5mA
Power Dissipated	-	12.5mW	6.25mW
Tuning Range	97MHz	363MHz	385.75MHz

Table 7.1. Comparison of specifications with measured results.

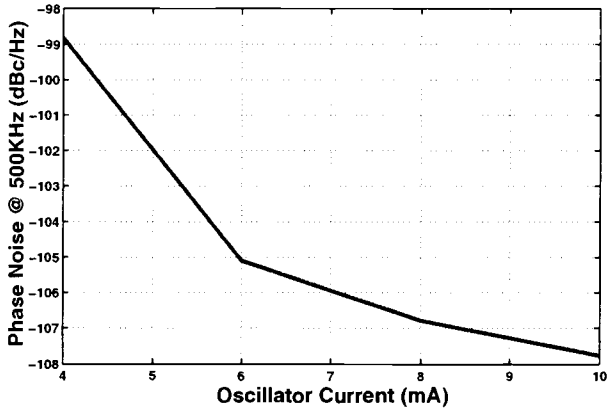
The phase noise curves for both oscillators with varying oscillator bias currents are shown in Fig. 7.8. It can be observed that in both cases the increase in the oscillator bias current is accompanied by improved phase noise performance. It can also be seen that for identical currents the complementary oscillator has better phase noise performance. This is consistent with the prediction in Section 5.2.1.

7.3. Comparison of Various Oscillators

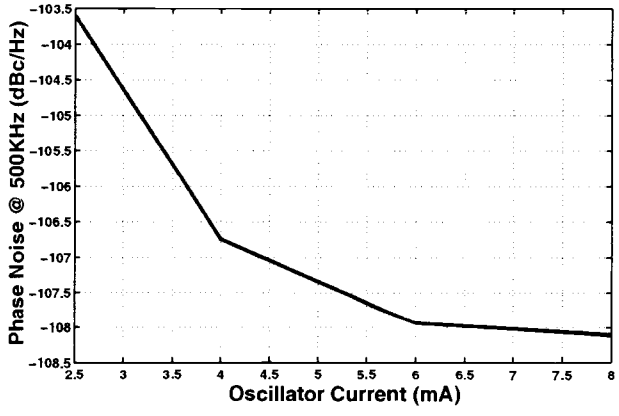
Table 7.2 compares the oscillators discussed above with the ones that have been published in literature. In order to compare oscillators with different center frequencies and power consumption, the term *Figure of Merit* (FOM) is often used [26]. The FOM is given by

$$FOM = 20log_{10}(Frequency) - Phasenoise - 10log_{10}(Power). \tag{7.1}$$

It can be observed from Table 7.2, that the oscillators published in literature have either a high tuning range or low phase noise, while the oscillators designed in this work have both low phase noise and high tuning range. These show comparable performance to those previously published in literature when both FOM and tuning range are considered.



(a)



(b)

Figure 7.8. Effect of varying the oscillator current on phase noise. (a) NMOS oscillator. (b) Complementary oscillator.

VCO	Design	f_{OSC} (GHz)	Tuning Range (MHz)	Phase Noise @ 3MHz (dBc/Hz)	Power Diss. (mW)	FOM
NMOS	CMOS	2.11	363	-117.5	12.5	323
COMP	CMOS	2.19	385.75	-119.2	6.25	328
[28]	Bipolar	2.4	500	-129	18	334
[29]	Bipolar	2.56	500	-134	14	341
[30]	Bipolar	2.4	-	-122	50	323
[31]	CMOS	2.4	128	-123	5.5	333
[32]	CMOS	2.4	260	-133	3.75	345
[33]	Bipolar	2.4	350	-129	1.8	344

Table 7.2. Performance comparison of various oscillator designs.

8. CONCLUSION

The design of CMOS LC VCOs for Bluetooth specifications has been presented. These VCOs are capable of providing a large tuning range with low phase noise and low power consumption. Two different VCO topologies have been compared and the complementary structure has better phase noise performance than the NMOS structure. The performance of the two oscillators has been validated with measurements. The oscillators compare well with the ones presented in literature. Measurements will be performed using passive probes to compare with the results obtained using active probes.

Future work should include the study of other oscillator topologies like the Colpitts oscillator and their comparison to the LC balanced oscillator for phase noise performance. Accumulation mode varactors can also be used in the oscillators to observe the tuning range. Symmetric spiral inductors should also be included in one oscillator circuit. The preliminary results of this design form the basis for oscillator designs in the 4.2-5.7GHz frequency range.

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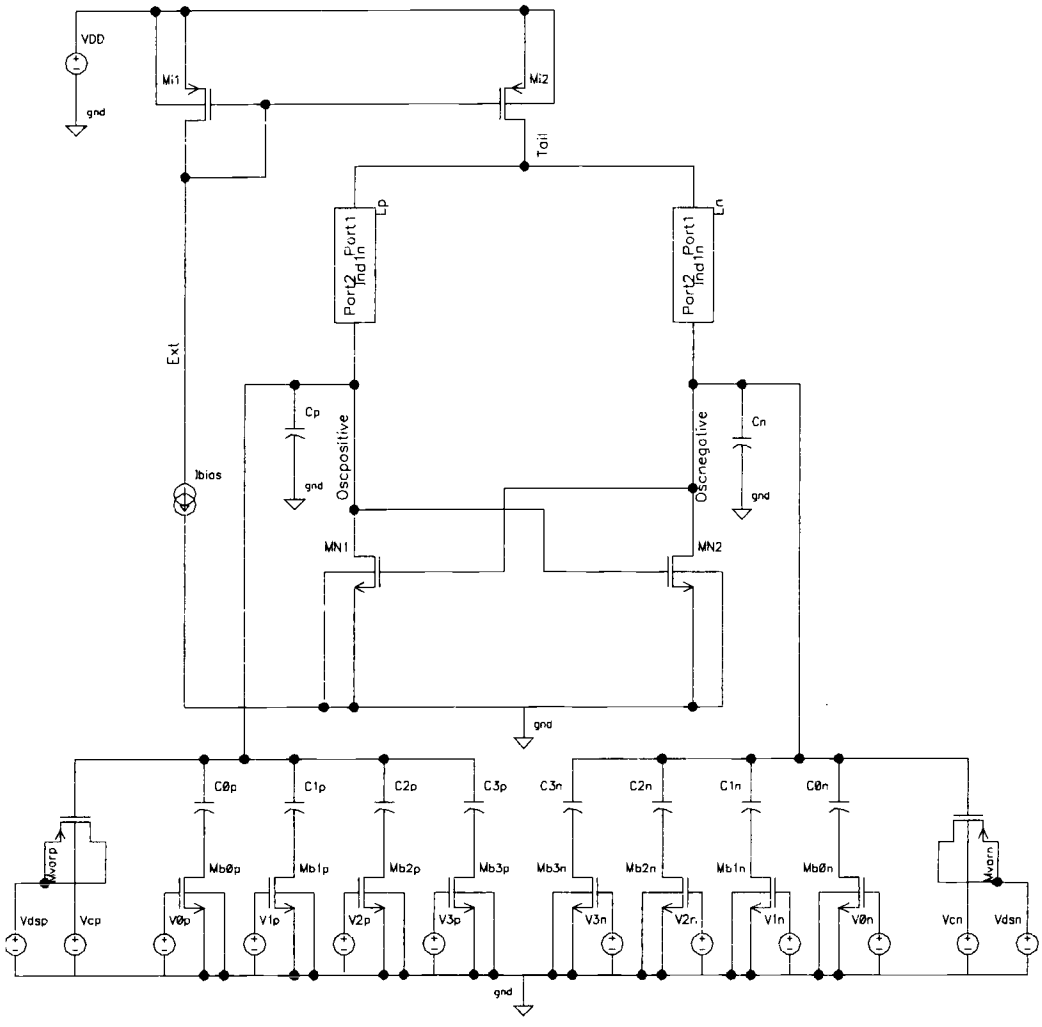
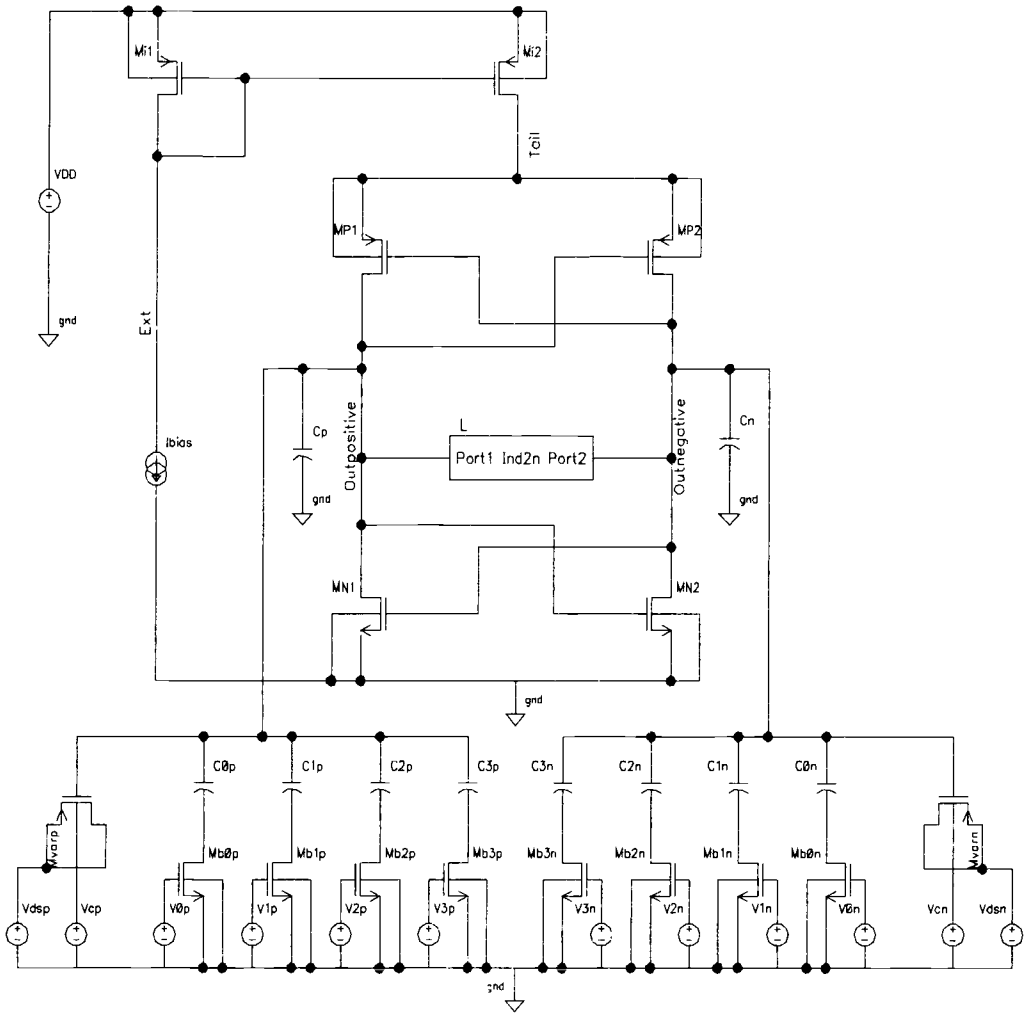
APPENDICES

APPENDIX A. NMOS oscillator core schematic from CADENCE



APPENDIX B. Complementary oscillator core schematic from CADENCE



APPENDIX C. Buffer schematic from CADENCE