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Title: Prediction of Phase Noise and Jitter in Ring Oscillators.

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This thesis presents distinctly different methods of accurately predicting phase noise and absolute jitter in ring oscillators. The phase noise prediction methods are the commercially available SpectreRF and *isf_tool*, a simulator developed in this work from the Hajimiri and Lee theory of phase noise. Absolute jitter due to deterministic supply and substrate noise is predicted by Spectre time domain simulations and equations developed that can predict the absolute jitter due to a sinusoidal noise source at any frequency. These jitter prediction methods show that ring oscillator circuits respond differently to deterministic noise that is injected symmetrically versus noise that is injected asymmetrically, and a new jitter metric, peak jitter, is developed in this work to characterize absolute jitter caused by deterministic noise sources.

These prediction methods are validated with measurements from two test chips with a combined 18 oscillators and 5 distinct architectures, and both are fabricated in the TSMC 0.35μm process. Each prediction method is shown to be consistent with over 2500 phase noise measurements taken from 10 oscillators and 5 architectures and over 1200 absolute jitter measurements due to sinusoidal supply and substrate noise taken from 11 oscillators and 3 architectures.

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Prediction of Phase Noise and Jitter in Ring Oscillators

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Nathen Barton, Author

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PREDICTION OF PHASE NOISE AND JITTER IN RING OSCILLATORS

1. INTRODUCTION

Recent years have witnessed explosive growth in the wireless communications industry, microprocessor complexity and speed and emerging technologies such as personal digital assistants. These applications incorporate systems such as radio frequency (RF) front ends, timing and synchronization circuits, and infrared input-output circuits. All of these systems need an oscillator to generate pure tones in the frequency domain and precise delays in the time domain. Oscillators can generally be placed into two categories: resonator based oscillators employing LC tanks and resonatorless oscillators that work on the principle of positive feedback. Historically, resonator-based oscillators have dominated the RF industry, primarily because they are superior to resonatorless oscillators consuming the same amount of power. There is however, significant interest in replacing them with simpler, more area-efficient resonatorless oscillators such as ring oscillators built with cheap, CMOS-only technology. In other fields already using ring oscillators, the steady demand for faster circuits, less power consumption and greater immunity to interference noise is fueling research into new topologies and better design techniques.

1.1. PLL Overview

In most systems, a single high-precision oscillator generates a reference signal and all subsystems use local Phase Locked Loops (PLLs) to generate a copy of the reference signal for use in that block. The high-precision oscillator is usually an external quartz crystal-based part that resonates at a fixed frequency and the signal is brought onto every chip in the system. The purpose of the PLL is to force the phase error of the local oscillator, which is inferior in performance to the high-precision oscillator, to be nearly zero. That is to say, the local oscillator now has performance that is comparable to the reference oscillator. Generating

local copies of the reference signal is done to reduce loading the high-precision oscillator and synthesizing an output frequency f_o from the input frequency f_i by using frequency dividers

$$f_o = \frac{M}{N} \cdot f_i \tag{1.1}$$

where M and N are frequency divider ratios as shown in the PLL block diagram in Figure 1.1. Assuming an ideal PLL and $N = M = 1$, the phase detector (PD) generates a current or a voltage that is linearly dependent on the phase error between the local oscillator and the reference source [1]. The output signal of the PD is low pass filtered by the loop filter $H(s)$ to stabilize the loop and set the loop bandwidth. Usually the loop filter is comprised of a simple RC network, although active filters are also used. The penalty for using an active filter is increased noise. The loop filter is generally second or third order: in first-order loops there will be a static phase error between the signal source and PLL output [2]. Filter orders above three are rarely used since there is marginal benefit and difficulty in guaranteeing the stability of the PLL [2].

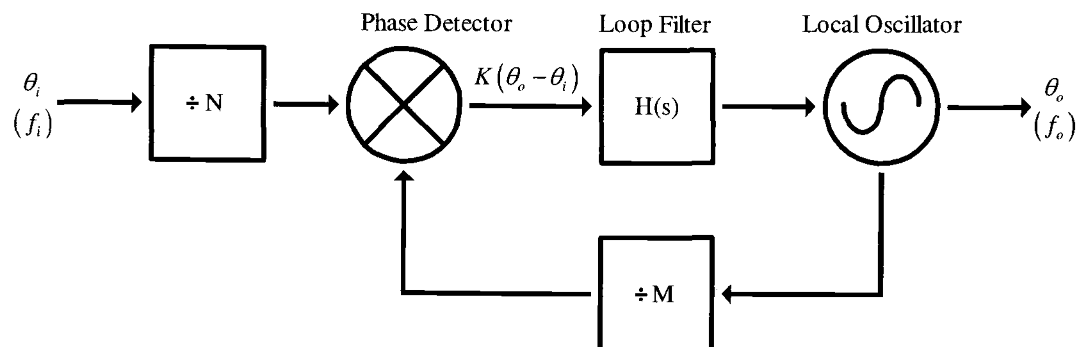


Figure 1.1 Block diagram of a PLL.

As noted previously, a PLL can be used to generate an output signal that is nearly as clean as the input signal. Figure 1.2 shows typical PSDs about the carrier of the local oscillator, reference source and PLL output. Although in an ideal oscillator the PSD would be a delta function, all physically realizable oscillators have noise sidebands about the carrier. These sidebands represent power at frequencies other than the carrier and are referred to as

phase noise. This represents uncertainty in the exact oscillation frequency. It can be seen that inside the loop bandwidth, the PLL phase noise spectrum is nearly identical to the reference source. Outside the loop bandwidth, however, the phase noise of the local oscillator dominates the spectrum [3]. The loop bandwidth determines the transition point. The naive reaction would be to simply increase the loop bandwidth. However at some point, this would cause the system to become unstable and also overlooks another tradeoff. Because the reference signal originates from off chip, high frequency noise could couple into the signal line. If the loop bandwidth is too high, the output of the PLL will contain this noise as well. The loop bandwidth sets the tradeoffs between stability, rejecting local oscillator phase noise close to the center frequency, and rejecting high frequency phase noise coupled into the reference oscillator. The loop bandwidth also sets other PLL parameters that are application specific. The conclusion to be drawn is that the phase noise spectrum of the local oscillator is crucial to the performance of the system in which the PLL is placed.

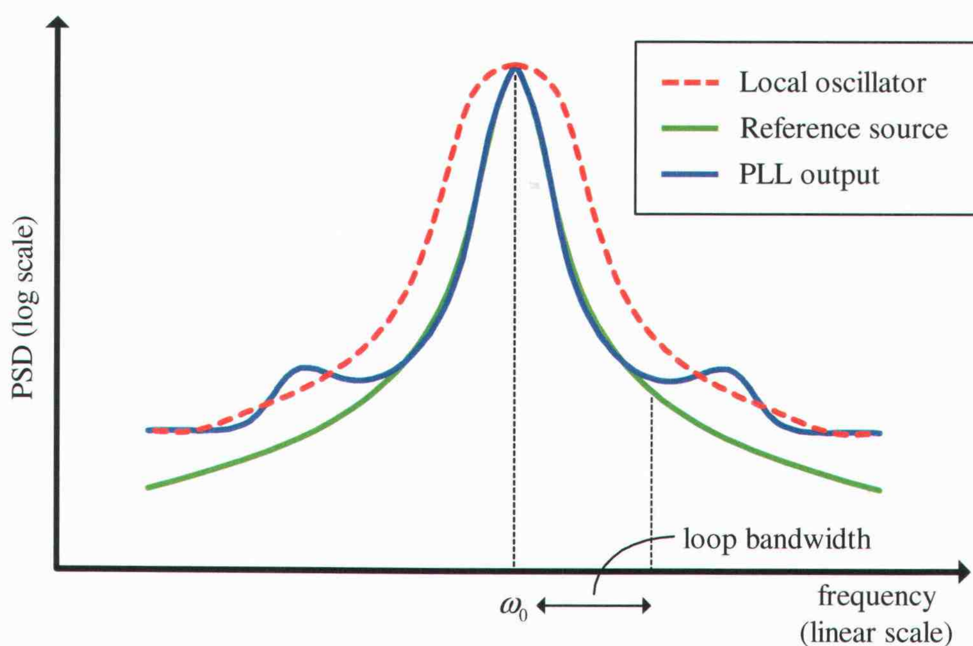


Figure 1.2 The power spectral densities (PSD) in a typical PLL system.

1.2. Phase Noise versus Jitter

Phase noise in oscillators was earlier defined as the uncertainty in the exact frequency. Jitter in oscillators is the dual case: uncertainty in the exact period. In some applications such as RF receivers, the spectral purity about the carrier is of prime importance, but in timing applications such as digital logic, timing jitter is the preferred performance metric. This is because digital designers typically work in terms of timing delays. Although timing jitter can sometimes be calculated from phase noise, this is usually not done for several reasons. First, phase noise is only measured in a narrow frequency band about the oscillator's carrier, while for an accurate timing jitter conversion the entire phase noise spectrum is needed [4]. Second, phase noise is the result of measuring noise power over a wide bandwidth in the frequency domain and, as such, is incapable of accurately measuring phase noise due to tones. Finally, with the easy availability of jitter measurement equipment, difficult and error-prone conversions are unnecessary.

1.3. Device Noise in MOSFET Transistors

Although phase noise and jitter can be caused by external sources, intrinsic device noise in MOSFETs is the inherent contributor. This phenomenon is caused by small fluctuations in voltage and current within the devices themselves [5]. MOS devices have two types of noise sources. The first is thermal noise, caused by the random thermal motion of electrons. It is proportional to the absolute temperature and is unaffected by the presence or absence of dc current. The PSD of thermal noise is flat with frequency; therefore, thermal noise is a white noise. The second type of noise is flicker noise. Although flicker noise is not well understood, there is reason to believe flicker noise in MOS transistors is due to electrons being trapped and released in the interface between the MOSFET channel and the gate oxide. The time constants involved with the trap-and-release mechanism give rise to a $1/f$ spectral shape of the PSD [5]. If the intrinsic device noise were measured with a spectrum analyzer, a plot similar to Figure 1.3 would be obtained. At low frequencies the device's flicker noise would dominate; at high frequencies the device's thermal noise would dominate. The point at which the PSDs are equal is referred to as the $1/f$ device noise corner. In MOS devices, the noise corner is usually between 2MHz and 10MHz.

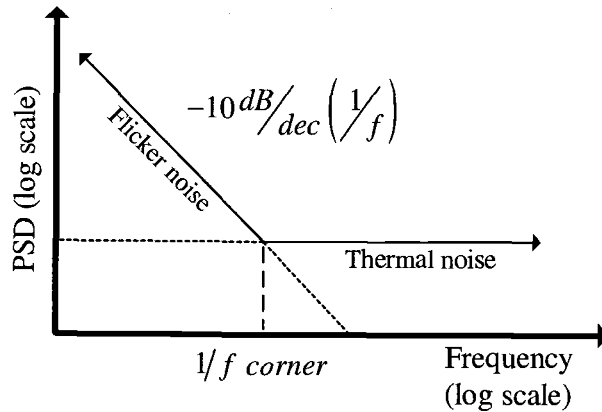


Figure 1.3 Flicker noise dominates the PSD of a MOS device at low frequencies while thermal noise dominates at high frequencies.

The accurate prediction of MOSFET noise is a field in itself and there are numerous commonly accepted equations to model it. SPICE simulators have two different models [6] to calculate MOSFET channel thermal noise. The first model, called the SPICE2 model, predicts

$$\overline{i_n^2} = \frac{8kT}{3}\left(g_m + g_{mbs} + g_{ds}\right)\Delta f \tag{1.2}$$

where k is Boltzmann's constant, T is the temperature in °K and g_m, g_{mbs} and g_{ds} are the transconductances. This model is based on channel resistance. More recently, the BSIM3v3 thermal noise model, based on the inversion channel charge Q_{inv}, has become popular

$$\overline{i_n^2} = \frac{4kT\mu_{eff}}{L_{eff}^2}\left|Q_{inv}\right|\Delta f \tag{1.3}$$

where μ_{eff} is the effective mobility and Q_{inv} is the charge in the inversion layer. Although not available in SPICE, another popular model for thermal noise [7] is

$$\overline{i_n^2} = 4kT\gamma g_{ds0}\Delta f \tag{1.4}$$

where γ is dependent on the channel length and biasing, and g_{dsO} is the drain-source conductance at zero V_{DS}. Although there are a number of thermal noise models, they are based on easily determined quantities and yield similar results for any given MOSFET. Flicker noise models, on the other hand, can show large variations in results and contain empirical fitting parameters. In Spectre there are three flicker noise models [6] to choose from. The SPICE2 model is given by

$$\overline{i_n^2} = \frac{K_f I_{ds}^{ef}}{C_{ox} L_{eff}^2 f^{af}} \Delta f \tag{1.5}$$

where I_{ds} is the drain current, L_{eff} is the effective channel length, and ef, af and K_f are constants that depend on each specific device and process, although af is usually close to unity. The value for K_f is generally measured for an array of transistor sizes in any given process. This equation is considered most accurate for a device in saturation, while a similar equation available in Spectre and considered most accurate for a device in the linear region is given by

$$\overline{i_n^2} = \frac{K_f g_m^2}{W_{eff} L_{eff} C_{ox}^2 f^{af}} \Delta f \tag{1.6}$$

where W_{eff} is the effective width. Although the variable K_f appears in both (1.5) and (1.6), they are, in fact, different constants. The K_f in (1.6) is often several orders of magnitude larger than the K_f in (1.5). The flicker noise models of (1.5) and (1.6) are not intuitive, and the BSIM3v3 model for flicker noise is very complicated:

$$\overline{i_n^2} = \frac{q^2 kT \mu_{eff} I_{ds}}{10^8 \cdot C_{ox} L_{eff}^2 f^{af}} \left(N_A \cdot \log\left(\frac{N_0 + 2\cdot 10^{14}}{N_l + 2\cdot 10^{14}} \right) + N_B \left(N_0 - N_l \right) + \frac{N_C}{2} \left(N_0^2 - N_l^2 \right) \right) \Delta f$$

$$+ \frac{V_{tm} I_{ds} \Delta L_{clm}}{10^8 \cdot W_{eff} L_{eff}^2 f^{af}} \cdot \frac{N_A + N_B N_l + N_C N_l^2}{\left(N_l + 2\cdot 10^{14} \right)^2} . \tag{1.7}$$

N_A, N_B and N_C are all empirical fitting parameters from the saturation, linear and cutoff regions of operation, respectively, and N_0 and N_l are charge densities. The BSIM3v3 model of flicker noise is a recent development and the parameters N_A, N_B and N_C are not available in most processes. At some companies it is common practice to use the SPICE default values with this model. More on this model can be learned from [6] and [8].

The exact mechanisms in which thermal and flicker noise are transformed into phase noise is given a detailed study in this work.

1.4. Challenges in Oscillator Design

Although the study of oscillators is certainly not a new subject, there are many difficult problems that remain to be solved. Several of these problems are:

- Accurately predicting phase noise. Only recently has it been possible to predict phase noise *a priori*. Three commercial simulators are now available, SpectreRF from Cadence, ADS from Agilent-EEsof, and ELDO from Mentor Graphics. Although there is general agreement regarding their potential accuracy, there has been no detailed comparison between simulation and measurements.
- Reducing sensitivity to supply and substrate noise. Oscillators are often placed in system-on-a-chip environments where deterministic supply and substrate noise can dominate intrinsic device noise. Work is needed to understand how supply and substrate noise couple into the oscillator, and how the effects of this noise on the oscillator can be minimized.
- Obtaining design insight. Although the commercial tools are capable of making predictions, they do not provide design insight into minimizing phase noise. Recently, a general theory of phase noise published by Hajimiri and Lee (H&L) predicts phase noise and gives design insight. However, the theory is difficult to implement and is not universally accepted. Again, there has been no detailed comparison between the theory and measurements.

1.5. Thesis Organization

This work focuses on the three problems listed above: accurately predicting phase noise, reducing sensitivity to supply and substrate noise, and obtaining design insight. In Chapter 2, the general theory of phase noise published by Hajimiri and Lee is studied and a mistake in their treatment of ring oscillators is identified and corrected. Then, a detailed methodology to implement the theory for phase noise simulation is described. The sources of error in this method are studied and two methods for calculating cyclostationary noise are presented. Chapter 3 shows a new jitter metric, peak jitter [9]-[10], which is needed to characterize the jitter caused by deterministic noise sources. Equations are developed that can predict the peak

jitter due to a sinusoidal noise source at any frequency. Two test chips were designed to verify the results obtained in Chapters 2 and 3; they are described in Chapter 4. Ten oscillators were used to study flicker noise models and the phase noise performance of different architectures. These oscillators have also been used to illustrate the characteristics of SpectreRF and the Hajimiri and Lee theory in predicting phase noise. Eight oscillators were designed to study the relationship between supply and substrate noise in single-ended and differential oscillators. Chapter 5 presents measurements; it includes a comparison of SpectreRF simulations and simulations based on the Hajimiri and Lee theory using over 150 phase noise measurements from nine oscillators and five architectures. The measurements shown are averages created from over 2500 individual phase noise measurements. Also Chapter 5 compares jitter measurements from 11 oscillators done with Spectre time domain simulations and the predictive jitter equations developed in Chapter 3. Chapter 6 correlates mismatches in oscillator circuits with the jitter measurements of Chapter 5 and shows how mismatches influence an oscillator's susceptibility to supply and substrate noise. This chapter also explores the oscillator components most sensitive to noise and uses simulations and measurements to compare the phase noise performance of different architectures. Chapter 7 develops methods to reduce phase noise. Conclusions are presented in Chapter 8.

2. PHASE NOISE IN RING OSCILLATORS

In an ideal oscillator, the output voltage as a function of time can be described by

$$v(t) = A\cos(\omega_0 t + \theta) \tag{2.1}$$

where ω_0 is the oscillation frequency, A is the oscillation amplitude and θ is the relative phase. As noted in Chapter 1, the PSD of this time domain waveform is given by a pair of delta functions at $\pm\omega_0$ as shown in Figure 2.1. All physically realizable oscillators, however, have sidebands about each carrier as shown by Figure 1.2. A more practical equation for oscillators is given by (2.2)

$$v(t) = A(t) \cdot f\left[\omega_0 t + \phi(t)\right] \tag{2.2}$$

where $A(t)$ and $\phi(t)$ are stochastic processes. The statistical properties in $\phi(t)$ and $A(t)$ give rise to sidebands about the carrier, as shown in Figure 2.2. Phase noise is simply the normalization of the power in a 1Hz bandwidth with respect to the carrier and is a function of the frequency offset from the carrier

$$L\{\Delta\omega\} = 10 \cdot \log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}\right]. \tag{2.3}$$

A detailed examination of phase noise in CMOS oscillators, shown in Figure 2.2, reveals three distinct regions. The region closest to the carrier shows a slope of -30 $dB/decade$ while the region farthest from the carrier has a flat noise floor. Between these regions, the PSD has a slope of -20 $dB/decade$. This observation, along with a linear, time invariant model (LTI), was first published by Leeson [11].

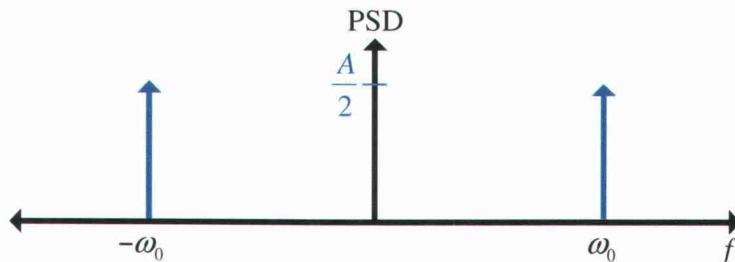


Figure 2.1 The PSD of an ideal oscillator is a pair of delta functions.

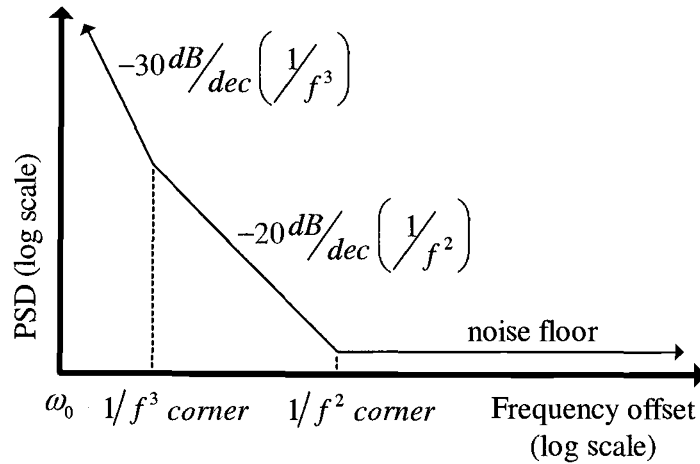


Figure 2.2 Real oscillators have sidebands about the carrier with distinct characteristics.

Leeson's model predicted the following behavior for $L\{\Delta\omega\}$:

$$L\{\Delta\omega\}=10\cdot\log\left\{\frac{2FkT}{P_{sig}}\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\left(1+\frac{\Delta\omega_{1/f}}{|\Delta\omega|}\right)\right\} \tag{2.4}$$

where P_{sig} is the power of the waveform, k is Boltzmann's constant, T is the absolute temperature and Q is the quality factor. The quantity $\Delta\omega_{1/f}$ is the frequency corner between the $1/f^3$ and $1/f^2$ regions as shown in Figure 2.2. F and $\Delta\omega_{1/f}$ are both fitting parameters used to match the model to measurements. Leeson identified the phase noise in the $1/f^3$ region as the result of device $1/f$ noise up converting to frequencies close to the carrier, and phase noise in the $1/f^2$ region a result of thermal noise. Although based on observations, Leeson's model was unable to explain the up-conversion of device $1/f$ noise and, due to the fitting parameter F, was unable to predict phase noise *a priori*. Although the work of others [12]-[13] provided an analytical basis for the up-conversion of device $1/f$ noise and provided more insight into the fitting parameter F [14], [15], LTI models have been shown to be fundamentally flawed [16].

2.1. Hajimiri and Lee Theory of Phase Noise

Hajimiri and Lee (H&L) [16] published a general theory of phase noise. They studied an oscillator's reaction to a noise source by characterizing the relationship between noise and phase noise as a linear, but time variant, system. To model the relationship, they assumed there was some transfer function between each noise source and the instantaneous amplitude and excess phase of the oscillator, $A(t)$ and $\phi(t)$, as defined by (2.2). For their analysis, noise inputs take the form of current sources in parallel with capacitors and voltage sources in series with inductive branches. The transfer functions are characterized by their impulse responses $h_{\phi}(t,\tau)$ and $h_{A}(t,\tau)$, as shown in Figure 2.3(a) and Figure 2.3(b), respectively. These impulse responses are time variant, as the following circuit example demonstrates.

The circuit in Figure 2.4(a) is an ideal parallel LC oscillator. Figure 2.4(b) and Figure 2.4(c) show the result of injecting 4pC of charge at the peak oscillator voltage and near the oscillator voltage zero crossing, respectively. In the case shown in Figure 2.4(b), injecting the charge at time instant τ_1 caused a change in the oscillation amplitude but not the phase. Figure 2.4(c) shows that injecting the charge at the time instant τ_2 caused a change in the phase but not the amplitude. This time dependence is proof that the system is indeed time variant. Note that in both cases the instantaneous voltage deviation ΔV was 0.8V. The instantaneous voltage deviation ΔV is governed by

$$\Delta V = \frac{\Delta q}{C_{tot}} \tag{2.5}$$

where Δq is the injected charge

$$\Delta q = \int_{-\infty}^{\infty} i(t)\, dt \tag{2.6}$$

and C_{tot} is the total capacitance at that node. In this case, ΔV can be calculated as $4pC/5pF = 0.8V$ matching the simulated result in Figure 2.4. In Figure 2.4(b), the amplitude after time τ_1 maintained its new value, contrary to the impulse response shown in Figure 2.3(b). This is because, in the case of the ideal LC oscillator, there are no lossy and energy restoration elements that are present in all physically realizable oscillators. In a practical oscillator there is only one amplitude possible for steady state oscillation and automatic gain limiting or circuit non-linearity will force the circuit to return to this amplitude.

There is, however, no phase restoration mechanism. If $v(t)=A(t)\cdot f\left[\omega_0 t+\phi(t)\right]$ is a solution, then $v(t)=A(t)\cdot f\left[\omega_0 t+\phi(t)+\vartheta\right]$ is also a solution, where ϑ is a constant. This is to say, the circuit has no memory of what the correct phase should be, so it has no means to restore the correct phase. These concepts are illustrated in the state-space diagrams of Figure 2.5 for a practical oscillator. Steady state oscillation lies on the orbit shown and, independent of when or how much noise is injected, the oscillator moves back to the steady state orbit [16], [18]. However the phase error $\varphi u(t-\tau)$, where $u(t)$ is the step function, persists as $t \to \infty$. The oscillator traverses one complete orbit for every oscillation cycle.

Simulations can also be used to check the assumption of linearity between injected charge and phase error. This is done by injecting different charge amounts and measuring the resulting phase deviation. Figure 2.6 shows two oscillator circuits. Figure 2.6(a) is a 5-stage ring oscillator with an oscillation frequency of 267MHz while Figure 2.6(b) is an LC balanced oscillator with a nominal oscillation frequency of 1607MHz. Current impulses have been injected at the zero crossing of the rising edge into both circuits in the nodes indicated; the resulting phase error was measured over a sweep of charge magnitudes. The results of the sweeps are shown in Figure 2.7(a) and Figure 2.7(b). It can be seen that the charge-to-phase transfer curve is linear for charge injection that is within certain bounds. A more detailed analysis of the linearity of the charge-to-phase transfer function will be presented in a later section. For our purpose here, it is enough to recognize that the charge-to-phase transfer function is nearly linear, although the oscillator circuit contains strongly non-linear elements and voltage-current behavior. It is also worth noting that the injected charge due to intrinsic device noise or interference would be significantly smaller than the charge amounts injected in Figure 2.7.

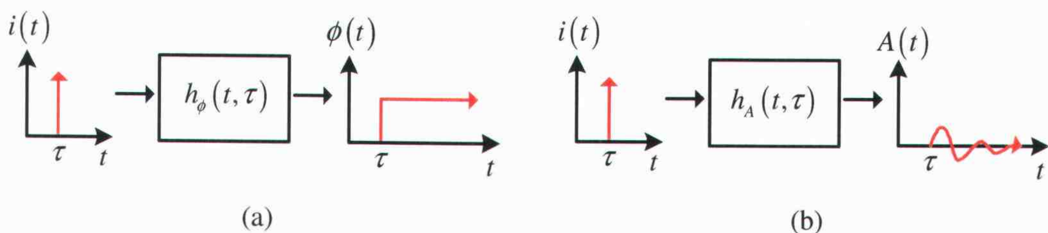


Figure 2.3 Noise current causes a step change in the phase of an oscillator (a) while the same noise current causes only a temporary disturbance in the amplitude (b).

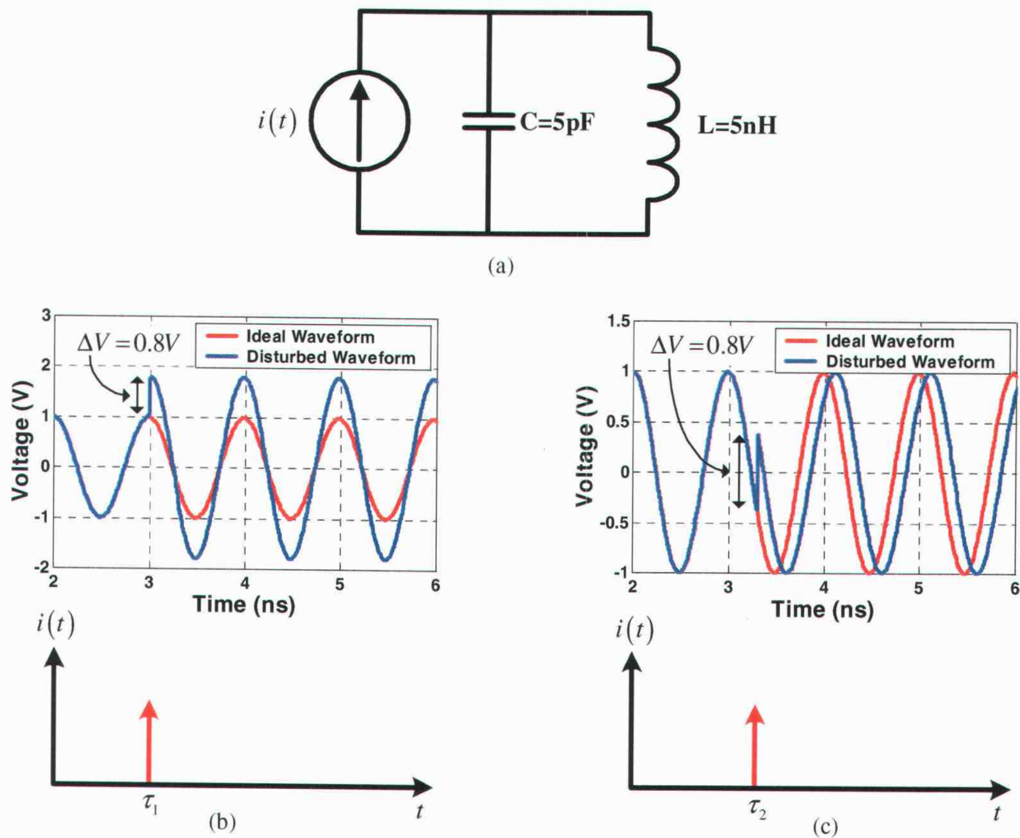


Figure 2.4 (a) An ideal LC oscillator. (b) The result of injecting a current impulse at the peak of the oscillation and (c) near a zero crossing.

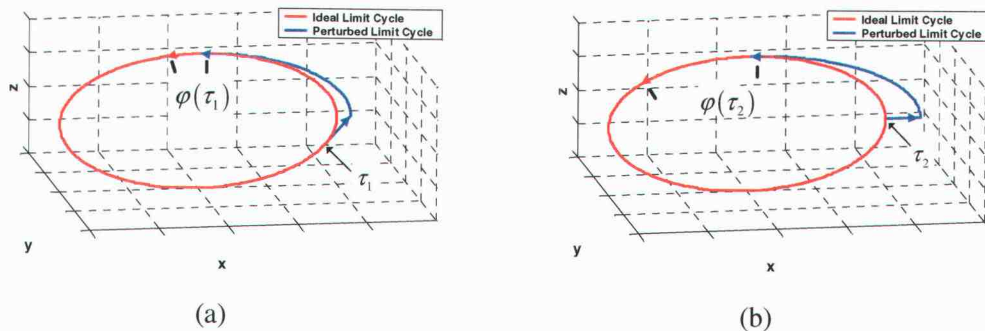


Figure 2.5 State-space diagram for noise injected at (a) τ_1 and (b) τ_2 for a practical oscillator. Noise causes a phase error φ from the ideal trajectory; the magnitude of the phase error depends on the instant in time τ when the noise was injected.

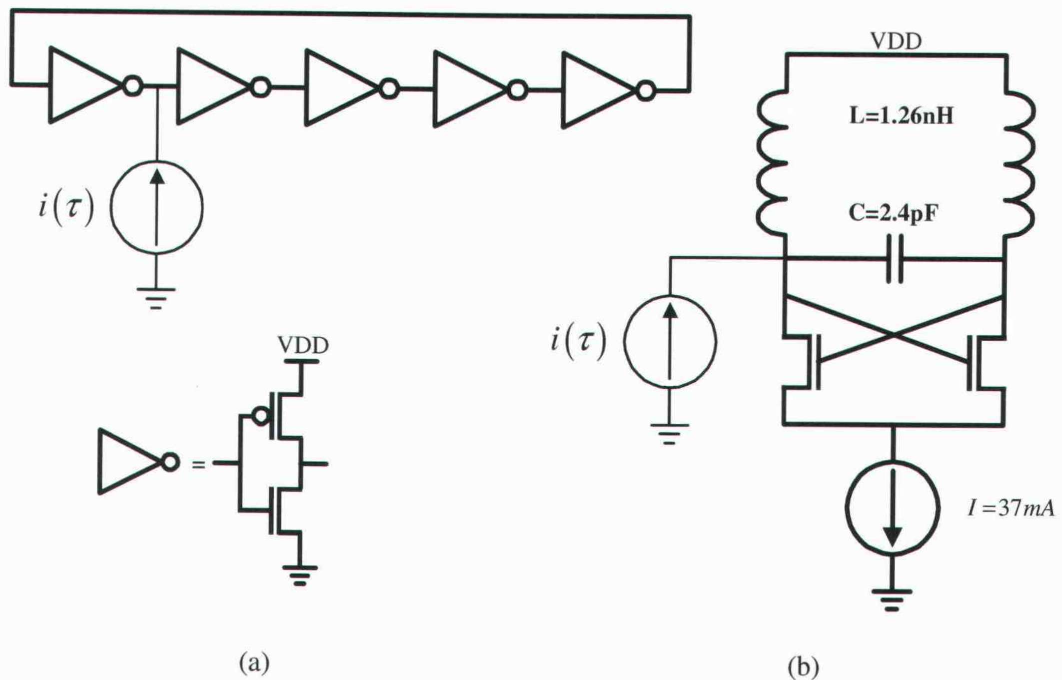


Figure 2.6 (a) 5-stage ring oscillator and (b) balanced LC oscillator.

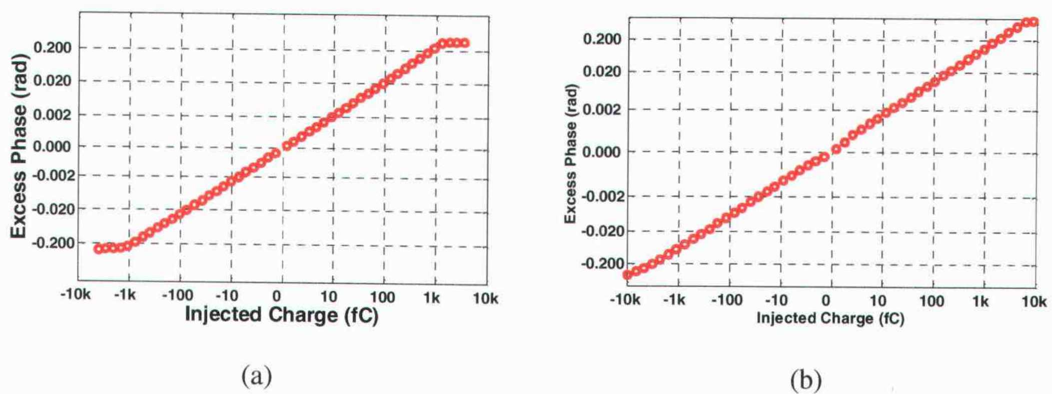


Figure 2.7 Phase shift versus injected charge for (a) the 5-stage ring oscillator and (b) the balanced LC oscillator.

With linearity demonstrated, it has also been shown that the phase error is proportional to the ratio of the injected charge to the maximum charge at that node, q_{max}, and the time at which the charge was injected, τ. With this information and the impulse response model of Figure 2.3, the impulse response for excess phase can be written as

$$h_\phi(t,\tau)=\frac{\Gamma(\omega_0\tau)}{q_{\max}}u(t-\tau) \tag{2.7}$$

where $\Gamma(\omega_0 t)$ is the *impulse sensitivity function* (ISF), a dimensionless periodic function with period 2π that describes the sensitivity of the excess phase $\phi(t)$ to a unit impulse at time $t=\tau$. Assuming the ISF is known, the excess phase due to an arbitrary noise source $i(t)$ is given by the superposition integral

$$\phi(t)=\frac{1}{q_{\max}}\int_{-\infty}^{t}\Gamma(\omega_0\tau)i(\tau)\,d\tau . \tag{2.8}$$

Since the ISF is periodic it can be decomposed into a Fourier series

$$\Gamma(\omega_0\tau)=\frac{c_0}{2}+\sum_{n=1}^{\infty}c_n\cos(n\omega_0\tau+\theta) \tag{2.9}$$

and (2.9) can be placed into (2.8)

$$\phi(t)=\frac{c_0}{2q_{\max}}\int_{-\infty}^{t}i(\tau)\,d\tau+\frac{1}{q_{\max}}\sum_{n=1}^{\infty}c_n\int_{-\infty}^{t}i(\tau)\cos(n\omega_0\tau)\,d\tau . \tag{2.10}$$

Let $i(t)=I_i\cos(\omega_i t)$ so that

$$\phi(t)=\frac{I_i c_0}{2q_{\max}}\int_{-\infty}^{t}\cos(\omega_i\tau)\,d\tau+\frac{I_i}{q_{\max}}\sum_{n=1}^{\infty}c_n\int_{-\infty}^{t}\cos(\omega_i\tau)\cos(n\omega_0\tau)\,d\tau \tag{2.11}$$

which can be integrated according to [20]

$$\int\cos(\omega_i t)\cos(n\omega_0 t)\,dt=\frac{\sin\left[(\omega_i+n\omega_0)t\right]}{\omega_i+n\omega_0}+\frac{\sin\left[(\omega_i-n\omega_0)t\right]}{\omega_i-n\omega_0} \tag{2.12}$$

resulting in

$$\phi(t)=\frac{I_i c_0\sin(\omega_i t)}{2q_{\max}\omega_i}+\frac{I_i}{2q_{\max}}\sum_{n=1}^{\infty}\frac{c_n\sin\left[(\omega_i+n\omega_0)t\right]}{\omega_i+n\omega_0}+\frac{I_i}{2q_{\max}}\sum_{n=1}^{\infty}\frac{c_n\sin\left[(\omega_i-n\omega_0)t\right]}{\omega_i-n\omega_0} . \tag{2.13}$$

It is evident from (2.13) that excess phase due to sinusoids far from dc or $n\omega_0$ will be strongly attenuated due to the growth of the denominator and that, for any particular value of ω_i, $\phi(t)$ will primarily be described by one Fourier coefficient and one complementary pair of

sinusoids. With an expression for the excess phase $\phi(t)$ developed, it is useful to remember that an oscillator converts phase to voltage via

$$v(t)=\cos\left(\omega_0 t+\phi(t)\right) \tag{2.14}$$

which can be expanded as

$$v(t)=\cos(\omega_0 t)\cos\left(\phi(t)\right)-\sin(\omega_0 t)\sin\left(\phi(t)\right). \tag{2.15}$$

For small values of $\phi(t)$, the narrow band approximations

$$\cos\left(\phi(t)\right)\approx 1 \tag{2.16}$$

$$\sin\left(\phi(t)\right)\approx \phi(t) \tag{2.17}$$

can be used to simplify (2.15) into

$$v(t)=\cos(\omega_0 t)-\phi(t)\sin(\omega_0 t). \tag{2.18}$$

Suppose $\phi(t)=\dfrac{I_0 c_0 \sin(\Delta\omega)}{2q_{\max}\Delta\omega}$ where $\Delta\omega \ll \omega_0$, then

$$v(t)=\cos(\omega_0 t)-\frac{I_0 c_0 \sin(\Delta\omega)\sin(\omega_0 t)}{2q_{\max}\Delta\omega} \tag{2.19}$$

which can be simplified to

$$v(t)=\cos(\omega_0 t)+\frac{I_0 c_0 \cos\left[(\omega_0+\Delta\omega)t\right]}{2q_{\max}\Delta\omega}-\frac{I_0 c_0 \cos\left[(\omega_0-\Delta\omega)t\right]}{2q_{\max}\Delta\omega}. \tag{2.20}$$

With this assumption, which is an extension of (2.13), it can be seen that the spectrum of $v(t)$ contains a carrier at ω_0 and two equal sidebands at $\omega_0 \pm \Delta\omega$. The power in the sidebands can be normalized relative to the carrier, resulting in a single sideband power P_{SBC}

$$P_{SBC}\approx 10\cdot\log_{10}\left(\frac{I_0 c_0}{4q_{\max}\Delta\omega}\right)^2. \tag{2.21}$$

This can be generalized to include any sinusoidal noise described by $n\omega_0 + \Delta\omega$

$$P_{SBC}\approx 10\cdot\log_{10}\left(\frac{I_n c_n}{4q_{\max}\Delta\omega}\right)^2. \tag{2.22}$$

Equation (2.22) can be solved for a noise source with a white power spectral density $\overline{i_n^2}/\Delta f$,

$$L\{\Delta\omega\} = 10 \cdot \log_{10}\left(\frac{\Gamma_{rms}^2}{q_{\max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{2 \cdot \Delta\omega^2}\right) \tag{2.23}$$

where $L\{\Delta\omega\}$ is the total single sideband phase noise in dB below the carrier per unit bandwidth at an offset frequency of $\Delta\omega$. Γ_{rms} is the *root mean square* value of the ISF. This equation represents the phase noise in the $1/f^2$ region of the phase noise spectrum. To find the phase noise in the $1/f^3$ region, it is useful to note that flicker noise can be described by

$$\overline{i_{n\,1/f}^2} = \overline{i_n^2} \cdot \frac{\omega_{1/f}}{\Delta\omega} \tag{2.24}$$

where $\omega_{1/f}$ is the frequency of the device $1/f$ noise corner. This device noise corner is the frequency point at which the flicker noise has the same power as the thermal noise. Equation (2.24) can be substituted into (2.22) to solve for the phase noise in the $1/f^3$ region of the phase noise spectrum:

$$L\{\Delta\omega\} = 10 \cdot \log_{10}\left(\frac{c_0^2}{q_{\max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{4\Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega}\right). \tag{2.25}$$

The frequency point at which the phase noise due to the white noise is equal to the phase noise due to the flicker noise is defined as the ω_{1/f^3}, or simply the $1/f^3$ phase noise corner. Equations (2.23) and (2.25) can be solved to yield an analytical expression for the frequency corner

$$\omega_{1/f^3} = \omega_{1/f} \cdot \frac{c_0^2}{2\Gamma_{rms}^2} \tag{2.26}$$

where c_0 is the dc average value of the ISF. This result indicates that phase noise in the $1/f^3$ region is governed by the symmetry properties of the ISF. It will be shown later that the exact shape of the ISF is dependent on the oscillator architecture, component values and biasing. This analysis is valid for uncorrelated noise sources, but some noise sources like supply and substrate noise have a high degree of correlation [21]. As an example, consider the case of Figure 2.8. In this case the excess phase $\phi(t)$ due to injected noise is given by a summation that represents the superposition of (2.8)

$$\phi(t)=\frac{1}{q_{max}}\int_{-\infty}^{t} i(\tau)\left[\sum_{n=0}^{N-1}\Gamma\left(\omega_0\tau+\frac{2\pi n}{N}\right)\right]d\tau \tag{2.27}$$

where N is the number of stages in the ring oscillator. Equation (2.27) can be shown to be zero at dc and multiples of $N\omega_0$. The derivation is done in Appendix B; the result is (2.28)

$$\phi(t)=\frac{N c_0}{2q_{max}}\int_{-\infty}^{t} i(\tau)\,d\tau+\frac{N}{q_{max}}\sum_{n=1}^{\infty}c_{Nn}\left(\int_{-\infty}^{t} i(\tau)\cos(nN\omega_0\tau)\,d\tau\right) \tag{2.28}$$

where c_i is the ith Fourier coefficient of the ISF. Equation (2.28) can be solved in a manner similar to (2.10)

$$\phi(t)=\frac{NI_i}{2q_{max}}\cdot\left[\frac{c_0\sin(\omega_i t)}{\omega_i}+\sum_{n=1}^{\infty}\frac{c_n\sin\left[(\omega_i+nN\omega_0)t\right]}{\omega_i+nN\omega_0}+\sum_{n=1}^{\infty}\frac{c_n\sin\left[(\omega_i-nN\omega_0)t\right]}{\omega_i-nN\omega_0}\right]. \tag{2.29}$$

The implication of (2.29) is that correlated noise injected symmetrically far from dc or integer multiples of $N\omega_0$ should make negligible contributions to the excess phase of an oscillator. Equation (2.22) can be updated to reflect any correlated noise described by $nN\omega_0 + \Delta\omega$

$$P_{SBC}\approx 10\cdot\log_{10}\left(\frac{NI_{Nn}c_{Nn}}{4q_{max}\Delta\omega}\right)^2. \tag{2.30}$$

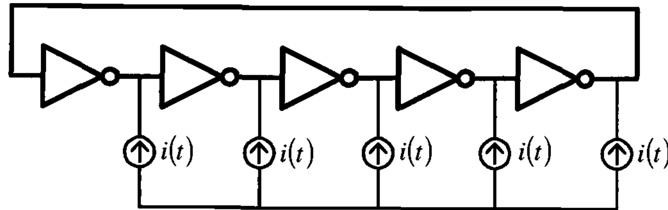


Figure 2.8 Symmetric noise injection.

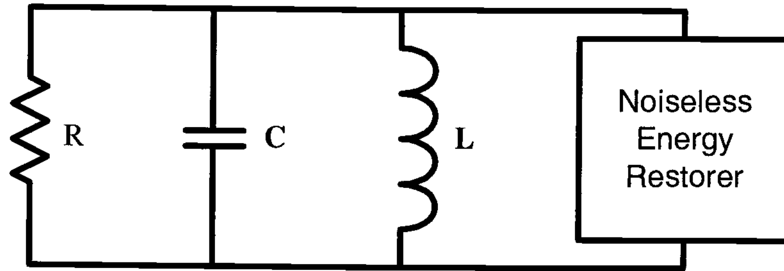


Figure 2.9 LC oscillator with tank loss R and a noiseless energy restorer.

2.2. Cyclostationary Noise

The results of (2.23) and (2.25) are valid for an oscillator such as that illustrated in Figure 2.9. In this oscillator, the only noise source in the system is that which is associated with the tank loss R and, provided that the value of R does not change over time, the thermal noise associated with R will be stationary. Many noise sources in oscillators are not stationary; instead, their noise densities will vary with time. If the statistical properties of a noise source vary periodically, the noise source is said to be *cyclostationary* [18]. As an example, consider Figure 2.10 which is identical to Figure 2.9 except that the resistor has been replaced with a diode-connected MOSFET transistor. This transistor is always in saturation, so a commonly accepted expression for its thermal noise density is [19]

$$\overline{i_n^2} = 4kT\gamma g_m. \tag{2.31}$$

An expression for g_m is

$$g_m = k'\frac{W}{L}\left(V_{gs}\left(\omega_0 t\right) - V_t\right) \tag{2.32}$$

and combining (2.31) with (2.32) yields

$$\overline{i_n^2} = \frac{4kT\gamma k'}{L}\left(V_{gs}\left(\omega_0 t\right) - V_t\right) \tag{2.33}$$

which clearly shows the cyclostationary nature of the transistor's thermal noise. A white cyclostationary noise source $i_n(t)$, however, can be decomposed as

$$i_n\left(t\right) = i_{n0} \cdot \alpha\left(\omega_0 t\right) \tag{2.34}$$

which separates cyclostationary white noise into stationary white noise source and a periodic function describing the amplitude modulation. The function $\alpha(\omega_0 t)$ is $i_n(t)$ normalized to a magnitude of 1, according to

$$\alpha(\omega_0 t)=\frac{i_n(t)}{\max\left[i_n(t)\right]} \tag{2.35}$$

where max(.) is the maximum value function. This defines $i_{n0}=\max[i_n(t)]$. As an example, the α calculated from (2.33) is

$$\alpha=\frac{\sqrt{\frac{4kT\gamma k'}{L}\left(V_{gs}(\omega_0 t)-V_t\right)}}{\max\left[\sqrt{\frac{4kT\gamma k'}{L}\left(V_{gs}(\omega_0 t)-V_t\right)}\right]} \tag{2.36}$$

and i_{n0} is

$$\max\left[\sqrt{\frac{4kT\gamma k'}{L}\left(V_{gs}(\omega_0 t)-V_t\right)}\right]. \tag{2.37}$$

In this way cyclostationary noise can be treated as stationary noise applied to a system with an effective ISF given by

$$\Gamma_{eff}(x)=\Gamma(x)\cdot\alpha(x). \tag{2.38}$$

The impulse sensitivity function has information about the oscillator's sensitivity to noise as a function of time, but it has no information as to when in time noise is actually present. The function $\alpha(\omega_0 t)$ has this information and $\Gamma_{eff}(x)$ contains both the oscillator's sensitivity to noise and when in the oscillation cycle noise is present. The effective ISF can be directly substituted into (2.23) and (2.25). Nearly all practical oscillators have cyclostationary noise sources. Previously it has been stated that the $1/f^3$ phase noise corner is dependent on the dc value of the ISF; in cyclostationary noise processes, the $1/f^3$ phase noise corner is dependent on the average value of the effective ISF.

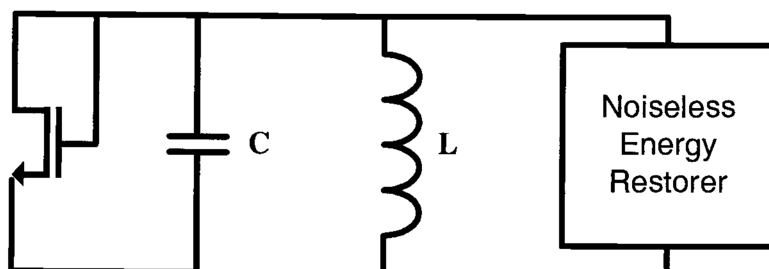


Figure 2.10 LC oscillator with a diode-connected transistor and a noiseless energy restorer.

2.3. Implementation of ISF Calculation Software

In the previous section, the importance of the effective impulse sensitivity function has been outlined. This section will detail a robust methodology to find the phase noise of an oscillator by implementing the Hajimiri and Lee theory of phase noise which uses transient simulations and a controlling program. This involves two steps:

- Finding the impulse sensitivity function.
- Finding the cyclostationary noise.

To be useful, the program should exhibit several properties:

- Require a minimum of human intervention or interaction.
- Adapt to different circuit topologies, biasing schemes and number of stages.
- Simulate circuits as quickly as possible, using minimum length transient simulations.

To implement the Hajimiri and Lee theory of phase noise as a circuit simulator, the programs *isf_tool*, *gds_tool* and *noise_tool* have been written. *Isf_tool* can calculate the phase noise due to an arbitrary number of noise sources associated with MOS transistors and resistors of nearly any oscillator circuit. At startup, the program reads in a number of user-defined parameters from the configuration file *isf.cfg*. The noise sources that are to be evaluated for their contribution to phase noise are specified here and, for each of these noise sources, the program iterates as shown in Figure 2.11 (the block diagram of the program). The responsibilities of *isf_tool* are to calculate the noise multipliers and the transfer function between each noise source and excess phase. Because ring oscillators are a cascade of identical stages, it is sufficient to calculate the noise in one stage and scale the result by the

number of stages. The alternative would be to calculate noise sources in each stage which would be inefficient. As an example of the noise multiplier calculation, consider the 5-stage ring oscillator in Figure 2.22. *Isf_tool* will recognize the presence of one PMOSFET noise source $\overline{i_0^2}$ and one NMOSFET noise source $\overline{i_1^2}$ in five identical stages and will calculate a noise multiplier of 5 for each. The noise multiplier of each transistor in the biasing circuit shown in Figure 4.23(c) would be 1. The other function of *isf_tool*, calculating the ISF, is explained below. *Isf_tool* relies on the two programs *gds_tool* and *noise_tool* to calculate the cyclostationary thermal noise and the flicker noise corner of each MOSFET device. Sections 2.4 and 2.5 explain how these analyses are performed.

The ISF contains the sensitivity of the oscillator to noise as a function of time. Although several methods can be used to find the ISF, the most accurate is a direct measurement of the impulse response and calculating $\Gamma(t)$ from it [16], [22]. In this method, N impulses are injected during transient simulations over one complete oscillation cycle, and the resulting time shifts, Δt, from the undisturbed oscillation trajectory are measured. The phase shift, $\varphi(t)$, can be calculated as

$$\varphi(t)=\frac{2\pi\,\Delta t}{T} \tag{2.39}$$

where T is the period of the oscillation.

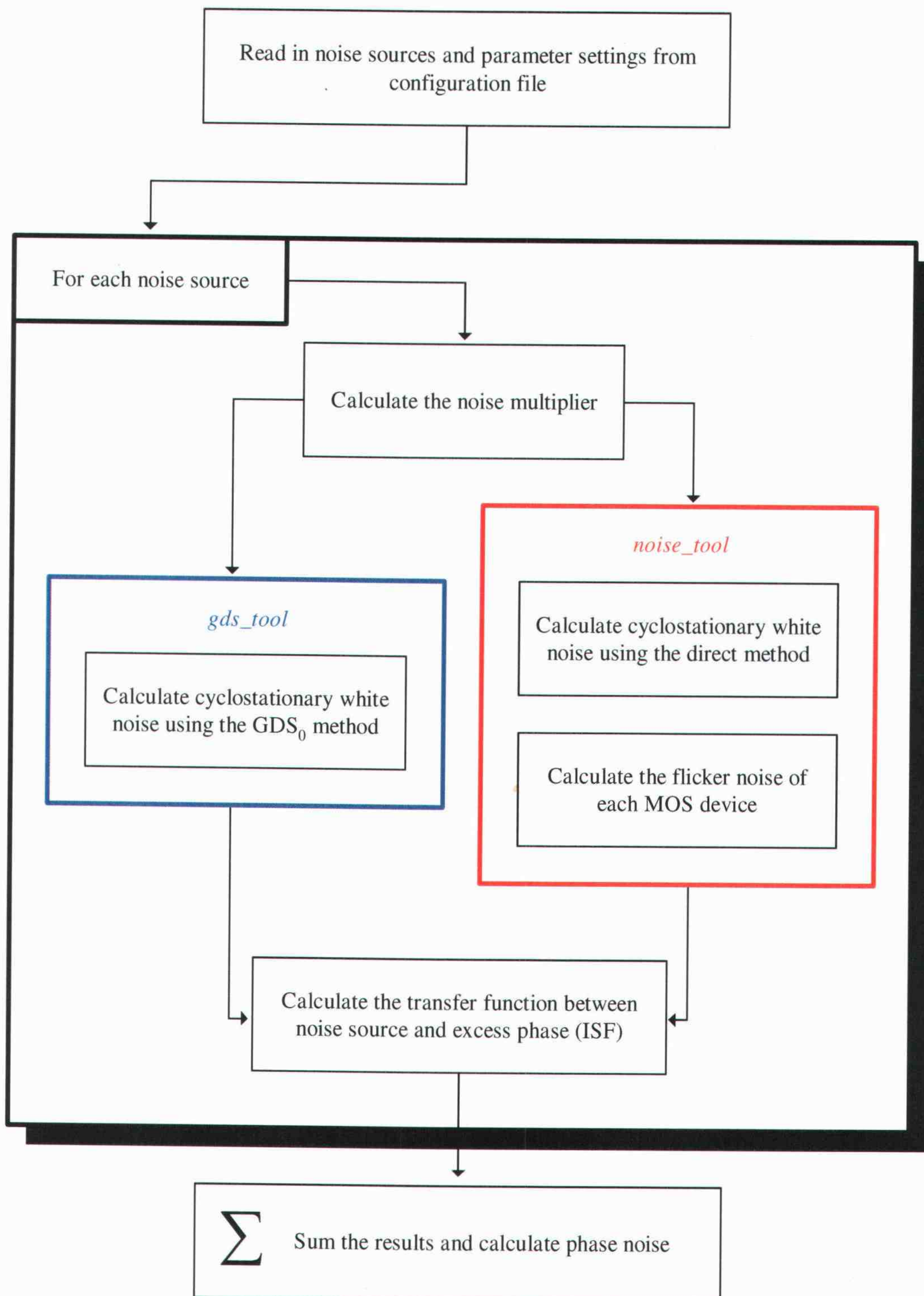


Figure 2.11 Block diagram of the H&L-based phase noise simulator. The direct and indirect methods of calculating cyclostationary noise are discussed in Section 2.4.

2.3.1. *Types of impulses*

The impulse injected may be a current pulse or a voltage pulse, depending on the impedance of the node the impulse is injected into and the circuit components. Current pulses are suitable for injecting into high impedance nodes and must be injected in parallel with a capacitor. The relationship between current and voltage in capacitors is given by (2.40)

$$i_c = C\frac{dV}{dt} \tag{2.40}$$

which, solved for ΔV in (2.41), shows the linear relationship between the injected charge and the voltage deviation caused by the injected charge. If the injected charge is small enough, the resulting phase shift will be small, validating the use of the small angle approximations in (2.16) and (2.17).

$$\Delta V = \frac{q_{inj}}{C_{tot}} \tag{2.41}$$

Injection of current pulses is only suitable for high impedance nodes. Consider the situation of finding the ISF at the supply node of Figure 2.12(a). In this circuit, the supply is biased with a voltage source. The small-signal model of a voltage source is a short circuit so, in the small signal sense, it would be attempting to find the ISF of Figure 2.12(b). The voltage source will maintain a constant value at the supply and the current impulses *i(t)* will be shunted through the voltage source to ground. In this application, injecting a voltage impulse in series with an inductor would allow the ISF to be simulated. The relationship between voltage and current in inductors is given by

$$v_L = L\frac{dI}{dt}. \tag{2.42}$$

Equation (2.42) can be solved for ΔI

$$\Delta I = \frac{\Phi_{inj}}{L_{tot}} \tag{2.43}$$

where Φ_{inj} is the magnetic flux injected into the inductor. Voltage pulse injection is not suitable for high impedance nodes such as those internal to the oscillator. Using the circuit in Figure 2.13 as an example, if a voltage source *v(t)* were used to find the ISF at this internal node, that node would be forced to ground and the circuit's operation would be disrupted. In most phase noise prediction applications, current impulse injection is the only option. In this

work, only current impulse injection is shown, but it should be realized that it is trivial to perform voltage impulse injection. One must, however, be careful to use the correct noise density in (2.23) and (2.25). Current impulse injection implies that the ISF found contains the sensitivity of the oscillator to current noise as a function of time, so noise current density must be used. In the dual case of voltage impulse injection, the voltage noise density must be used. The equation for phase noise due to white voltage noise is given by

$$L\{\Delta\omega\}=10\cdot\log_{10}\left(\frac{\Gamma_{rms}^2}{\Phi_{\max}^2}\cdot\frac{\overline{v_n^2}/\Delta f}{2\cdot\Delta\omega^2}\right). \tag{2.44}$$

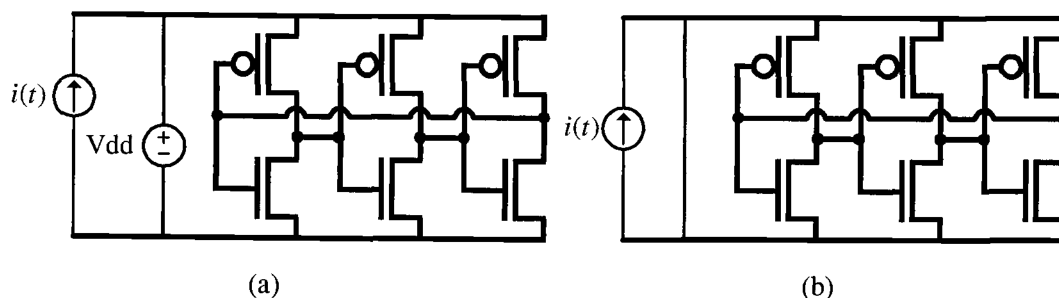


Figure 2.12 Using current pulses at the supply node as in (a) would cause the supply to act as a short circuit for the current as in (b).

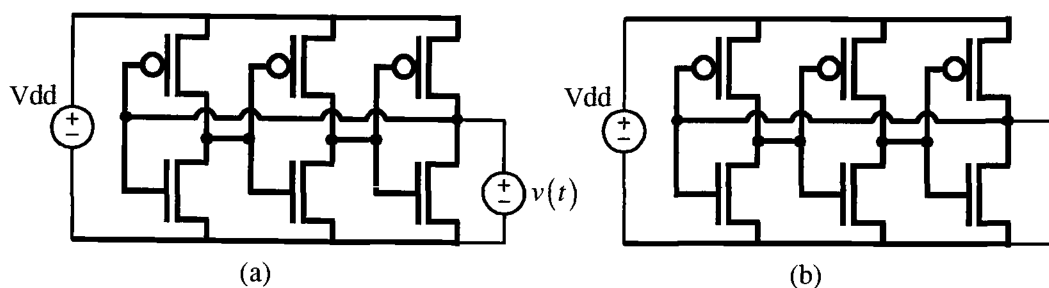


Figure 2.13 Using voltage pulses at a node internal to the oscillator as in (a) would force that node to ground as in (b).

Once the pulses are injected and the phase shift $\varphi(t)$ is measured, the phase shifts $\varphi(t)$ are normalized by the amount of injected charge and the maximum charge to give the ISF, which is then used in (2.23) and (2.25)

$$\Gamma(t)=\frac{q_{\max}}{q_{inj}}\varphi(t)=\frac{q_{\max}}{q_{inj}}\cdot\frac{2\pi\,\Delta t}{T}. \tag{2.45}$$

As shown in Appendix A, at first glance it appears that q_{max} is a required quantity, but it is actually not needed. This is favorable because it is difficult to determine q_{max} while q_{inj} is a known quantity. A more practical form of the ISF is

$$\tilde{\Gamma}(t)=\varphi(t)=\frac{2\pi\,\Delta t}{T}. \tag{2.46}$$

Equations (2.23) and (2.25) change to

$$L\{\Delta\omega\}=10\cdot\log_{10}\left(\frac{\tilde{\Gamma}_{rms}^2}{q_{inj}^2}\cdot\frac{\overline{i_n^2}/\Delta f}{2\cdot\Delta\omega^2}\right) \tag{2.47}$$

$$L\{\Delta\omega\}=10\cdot\log_{10}\left(\frac{\tilde{c}_0^2}{q_{inj}^2}\cdot\frac{\overline{i_n^2}/\Delta f}{4\Delta\omega^2}\cdot\frac{\omega_{1/f}}{\Delta\omega}\right) \tag{2.48}$$

respectively, where $\tilde{c}_0$ is a Fourier coefficient from $\tilde{\Gamma}(x)$.

2.3.2. *Injecting the impulses*

In theory, impulses are infinitely narrow in time and infinite in amplitude. In SPICE, however, impulses must be approximated by trapezoidal pulses, and a balance must be made between the time constant of the pulse and the time constants of the circuit. Figure 2.14 shows the pulse shape chosen for *isf_tool.* This is the nth current pulse from a family of N current pulses. The three variables that describe the pulse are the height of the pulse, A_i, the width of the pulse, τ_{pw}, and the area under the curve, q_{inj}. Only two of the variables are independent, specifying two determines the third. In the configuration file *isf.cfg*, these numbers may be entered as pulse amplitude in *mA*, pulse width as a percent of the oscillation frequency λ_{pw}, and injected charge in femto-coulombs q_{inj}. Because of the units chosen, there is a factor of 10^7 in the equation that relates them, as shown in Figure 2.14.

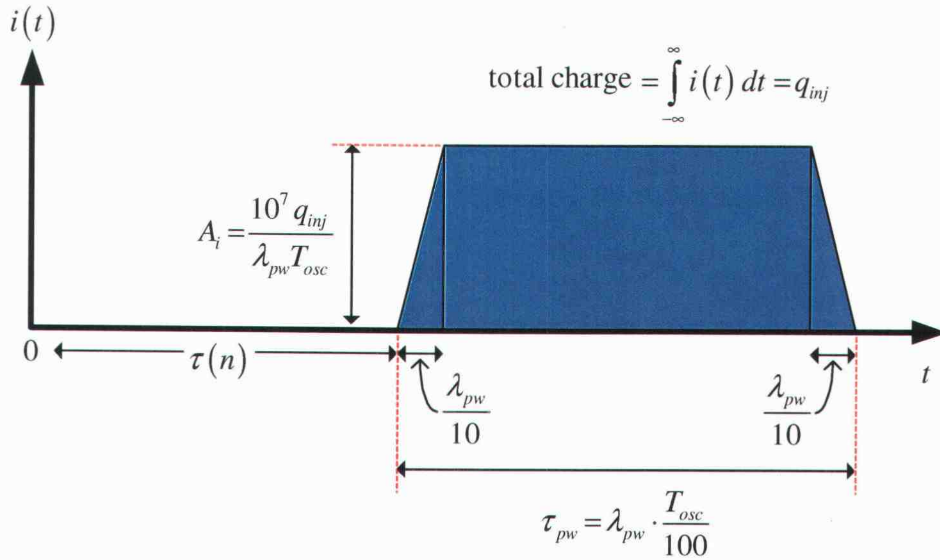


Figure 2.14 Diagram of the family of impulses *isf_tool* injects into a circuit and the equations that relate the physical parameters.

The quantity $\tau(n)$ shown in Figure 2.14 has two components

$$\tau(n) = \tau_{settle} + \sum_{n=0}^{N-1} \frac{nT_{osc}}{N} \tag{2.49}$$

where N is the number of times the ISF is sampled. The first component, τ_{settle}, should be chosen to ensure the oscillator just reaches a steady state trajectory. Choosing a τ_{settle} greater than this only increases the simulation time. The proper value should be based on the stability of the oscillation period and the waveform envelope. Figure 2.15(a) shows the startup transient and waveform envelope of the oscillator in Figure 2.6(b), while the curve in Figure 2.15(b) shows the error from the settled envelope of the waveform. The use of interpolation will be explained shortly. Figure 2.16(a) shows the period of the oscillator, and Figure 2.16(b) shows the error from the settled period of the oscillator. Figure 2.16(b) shows the danger of using only the settling of the period to determine if the oscillator is in steady state oscillation. Here the period settles to about 0.63ns with cycle stability better than 0.01% for several cycles. This, however, is not the steady state period. LC oscillators typically settle to a stable oscillation period more quickly than they settle to a stable waveform envelope, while ring oscillators typically settle to a stable envelope before settling to a stable period. This is

because the LC oscillator has a high tank Q that quickly filters out energy at frequencies other than ω_0. But because of the high tank Q, the oscillation amplitude cannot build up quickly. The argument for ring oscillators is the opposite; a ring oscillator has an extremely low "tank Q" and can quickly increase amplitude but takes time to settle to the correct period.

The program *isf_tool* initially performs three transient simulations to accurately determine the frequency of oscillation and τ_{settle}.

Although in Figure 2.15(a) there are a large number of time steps per period, the exact amplitude of each peak of the oscillator is not well defined, as shown by the squares in Figure 2.17(a). To more accurately determine the magnitude of each peak, quadratic interpolation should be performed on the three points that define the peak

$$V_{approximate}(t) = a_2 t^2 + a_1 t + a_0 . \tag{2.50}$$

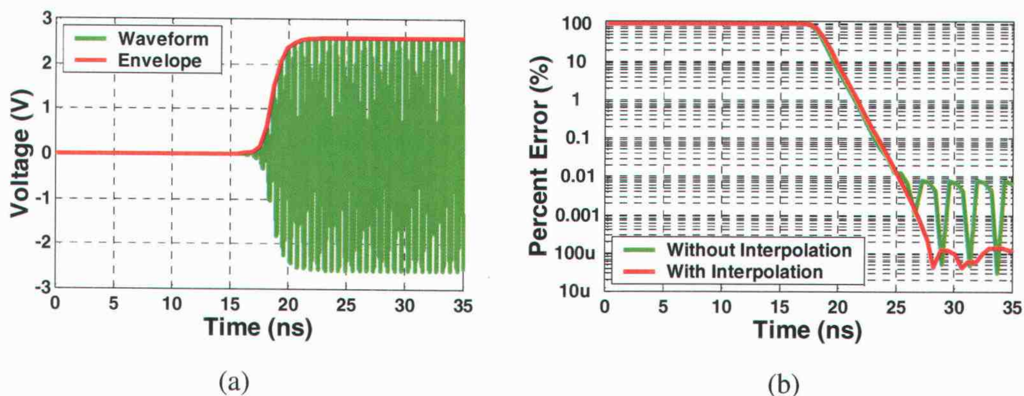
Although the interpolated values are shown as circles, the value of the peak should be found by taking the derivative of the quadratic and solving for the time at which the peak occurs

$$t_{\max} = -\frac{a_2}{2a_1} \tag{2.51}$$

and finally, the approximate peak voltage is $V_{approximate}(t_{\max})$. Figure 2.15(b) shows the difference between using interpolation and not using interpolation. With interpolation, the error in estimating the envelope of the waveform can be reduced by about two orders of magnitude. Interpolation to find the zero crossings of the waveform must also be carried out, as shown in Figure 2.17(b). Here squares show the data from the simulation and a circle shows the zero crossing calculated from linear interpolation. The time shifts due to injected charge are usually smaller than the distance between time points, so without interpolation no useful data can be obtained.

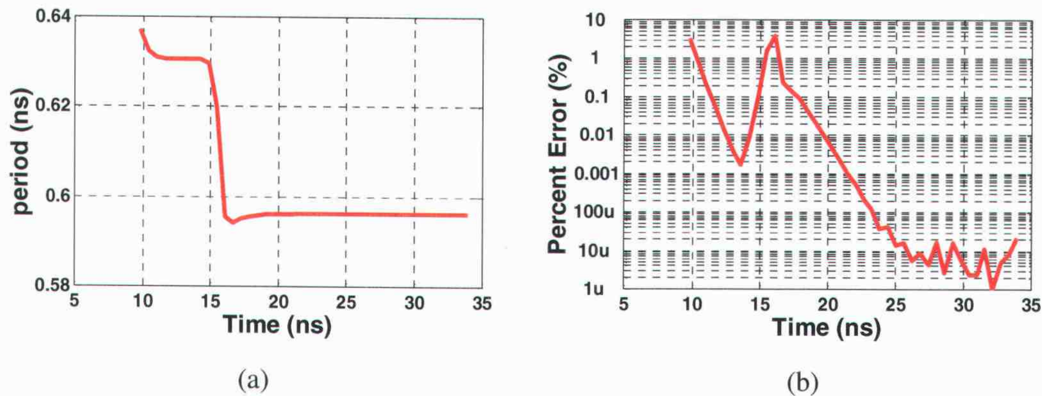
The second component of $\tau(n)$ shown in Figure 2.14 is $\sum_{n=0}^{N-1} \frac{nT_{osc}}{N}$. This causes the current impulses to progressively sample the ISF N times. Figure 2.18(a) illustrates an ISF that has been sampled 10 times, while Figure 2.18(b) shows an ISF that has been sampled 40 times. The formula for the time delay in (2.49) should be followed exactly. The ISFs in Figure 2.18(a) and (b) are complete in 2π. When the exact magnitudes of the ISF Fourier coefficients are being calculated, the last point in the ISF should be removed. The Fourier series transform

assumes the data is strictly periodic. Including the extra point would be the same as calculating the Fourier coefficients of the waveform in Figure 2.19.



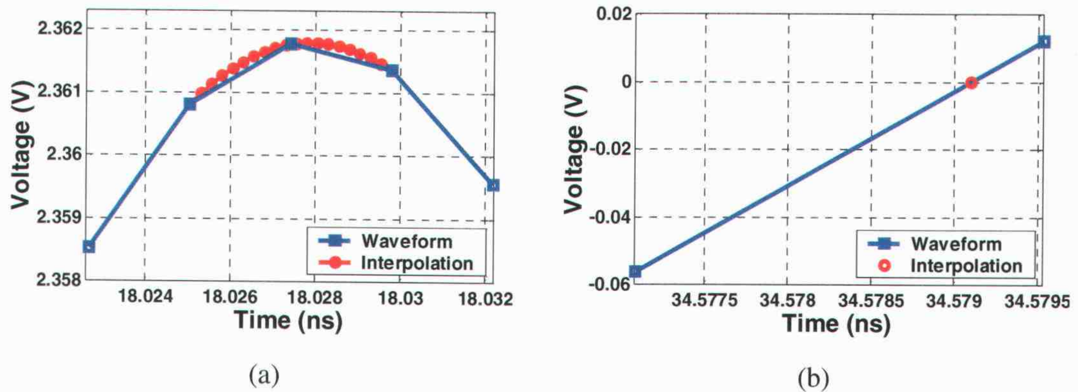
(a) (b)

Figure 2.15 (a) The startup transient of the oscillator in Figure 2.6(b). (b) The error of the oscillator's envelope compared to the steady state amplitude.



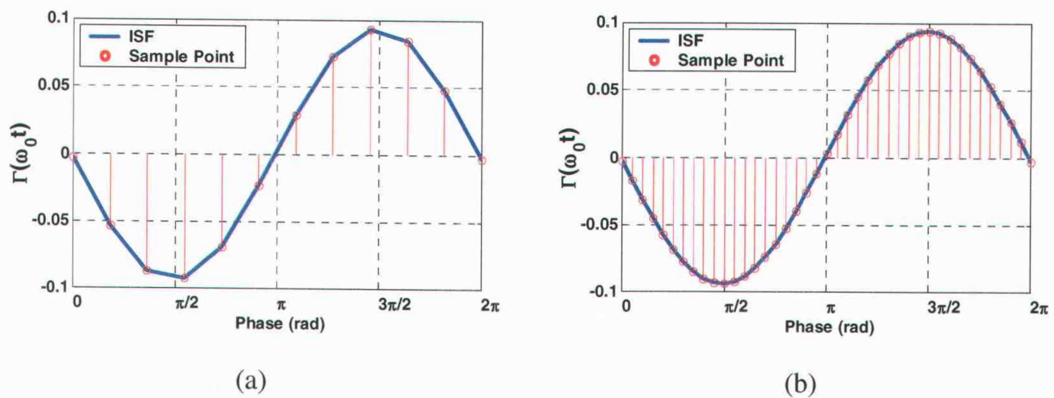
(a) (b)

Figure 2.16 (a) Period of the oscillator in Figure 2.6(b) from startup. (b) The error from each period to the previous period.



(a) (b)

Figure 2.17 (a) Quadratic interpolation is performed on each amplitude peak. (b) Linear interpolation is performed to find the approximate zero crossing of every rising edge. Squares show each data point.



(a) (b)

Figure 2.18 (a) The 10-point sampled ISF of the circuit in Figure 2.4(a) and (b) the 40-point ISF of the circuit in Figure 2.4(a).

2.3.3. *Number of pulses to inject*

The ISF is a continuous waveform that can only be sampled N times with this method. As such, it is important that the ISF be sampled at a rate high enough to capture its frequency content. In Figure 2.18(a), the ISF is well characterized by 10 samples, but 10 samples are not enough to characterize the ISF illustrated in Figure 2.20. A secondary reason to sample the ISF at a high rate is to ensure that it is smooth and contains no discontinuities. Jaggedness and discontinuities are clear indications that an error occurred in the calculation of the ISF.

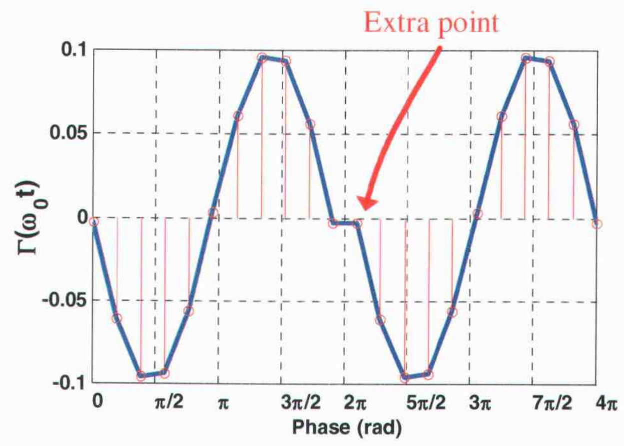


Figure 2.19 Calculating the Fourier coefficients of the ISF in Figure 2.18(a) without removing the last point is the same as calculating the Fourier coefficients of this waveform.

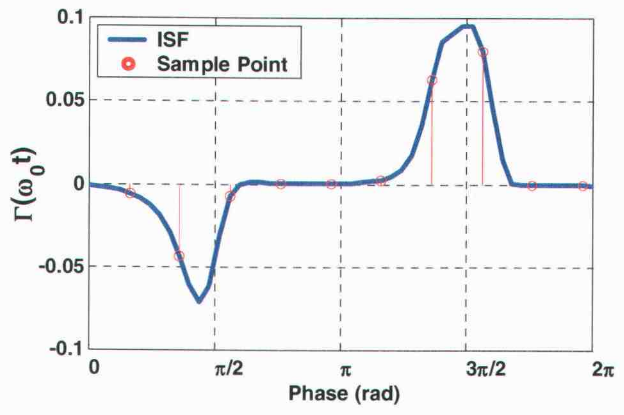


Figure 2.20 An under-sampled ISF of a 9-stage current-starved ring oscillator.

2.3.4. *Charge injection and pulse width linearity*

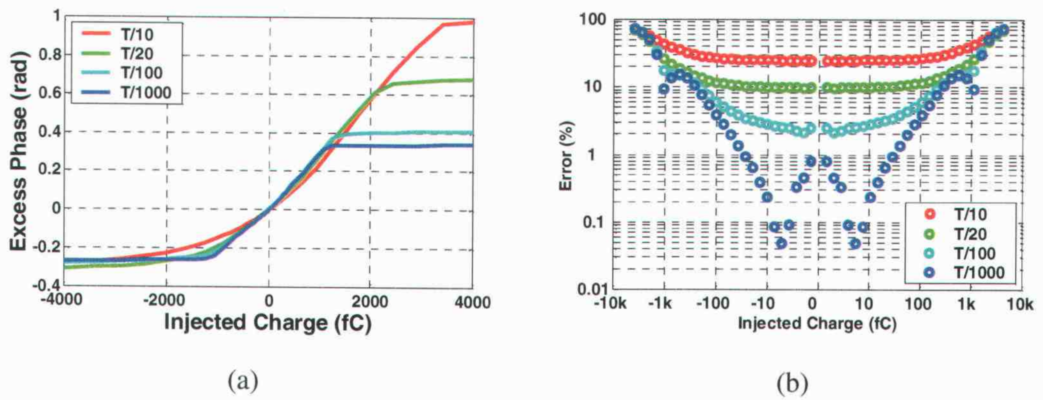
Hajimiri and Lee's theory of phase noise depends on the linearity between injected charge and excess phase. This linearity stems from the concept of small-signal analysis and from the narrow band approximations (2.16) and (2.17) involved in the derivations. From this it is clear that the amount of charge injected should be small relative to the charge present at the oscillator's node, $C_{node}V_{node}$. If the injected charge is too small, however, numerical noise in the simulator could swamp out the induced phase shifts. The other free variable is the pulse width in which the charge is injected. Simulation results for the circuit in Figure 2.6(a) exploring linearity are shown in Figure 2.21. Figure 2.21(a) shows the excess phase versus the magnitude of the injected charge for several pulse widths that are fractions of the oscillator's period T. Ideally these curves would be linear, pass through the origin and would be described by $\varphi = K \cdot q_{inj}$ where K is a constant. Figure 2.21(b) calculates the error between the simulated phase shifts and the "ideal" curve $K \cdot q_{inj}$. The slope K was determined by identifying the point at which the injected charge was small yet the ISF remained smooth. It can be seen that using a pulse width of $T/1000$ gives the best accuracy, and the minimum error occurs with a charge injection of ±5.2fC. There was 645fC of charge present at the injected oscillator node, giving an optimum ratio of

$$\frac{C_{node}\,V_{node}}{injected\ charge} = \frac{124}{1}. \tag{2.52}$$

Even though 124:1 is optimum, ratios as low as 6:1 still give acceptable results. Figure 2.21(b) clearly shows that only pulse widths between T/100 and T/1000 or smaller should be used.

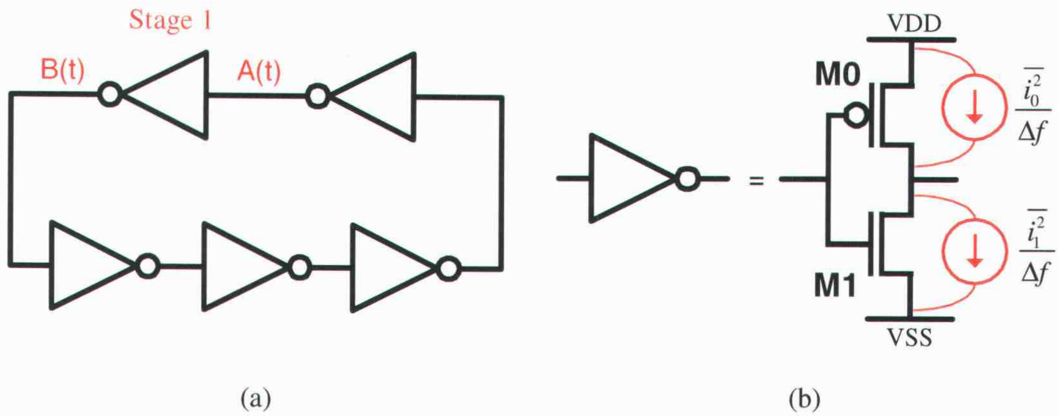
2.4. Methods to calculate cyclostationary noise

As mentioned previously, although MOSFET device noise is inherently white or $1/f$ in nature, its spectral density is bias dependant. In oscillators, the bias point is a periodic function giving rise to cyclostationary noise sources. This section outlines two different methods to calculate cyclostationary noise by way of an example. The 5-stage ring oscillator in Figure 2.22 is analyzed to determine the cyclostationary noise sources $\overline{i_0^2}/\Delta f$ and $\overline{i_1^2}/\Delta f$ in Stage 1.



(a) (b)

Figure 2.21 (a) Excess phase versus injected charge and (b) the error from the "ideal".



(a) (b)

Figure 2.22 The circuit example schematic of (a) a 5-stage ring oscillator and (b) each delay cell with white noise sources.

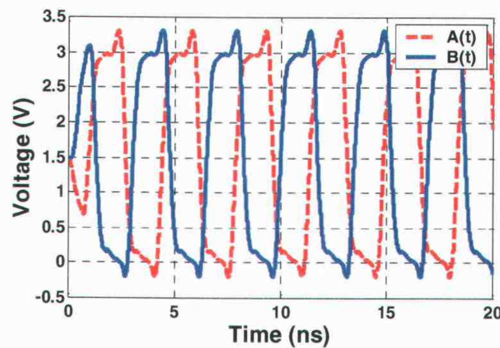


Figure 2.23 Node voltages A(t) and B(t) as a function of time.

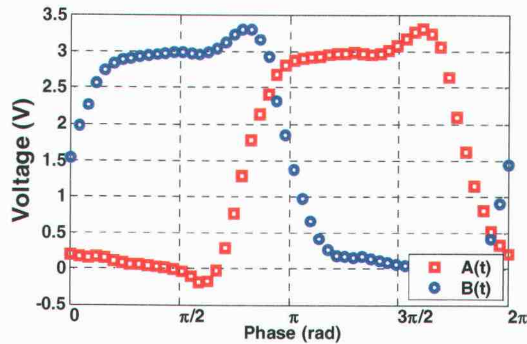


Figure 2.24 Node voltages A(t) and B(t) are discretized into N points.

Because all stages are identical, it is sufficient to find the noise sources in one stage. To calculate the noise, the circuit is simulated in the time domain to the point where it reaches a steady state, as shown in Figure 2.23. Once the steady state has been reached, one cycle of voltages $A(t)$ and $B(t)$ is extracted and this period is split into N discrete time points, as shown in Figure 2.24. The time points are equally spaced in time.

2.4.1. Direct method

At this point two methods are used to extract the cyclostationary noise data. The first is to directly simulate the noise at each of the N points. A single delay cell is split into individual transistors, as shown in Figure 2.25(a). In this method the node voltages A(nT/N) and B(nT/N), as n is varied from $0 \rightarrow N$, are used to force the circuit to each of the N discrete operating points. Noise analysis is done at all N points, and the thermal noise for both transistors is extracted to make an N-point curve of the cyclostationary noise, as shown in Figure 2.26.

2.4.2. Indirect method

In the indirect method, a single delay cell is also split into individual transistors. The gates of the transistors are biased with A(*nT/N*), as *n* is varied from $0 \rightarrow N$, but the drains are shorted to the sources, as shown in Figure 2.25(b). The dc operating point is found and gds_0 is extracted for all *N* points. Then the equation for thermal noise

$$\frac{\overline{i^2}}{\Delta f} = \frac{8kTgds_0}{3} \tag{2.53}$$

is used to find the thermal noise density. The noise density found using this method is shown in Figure 2.27.

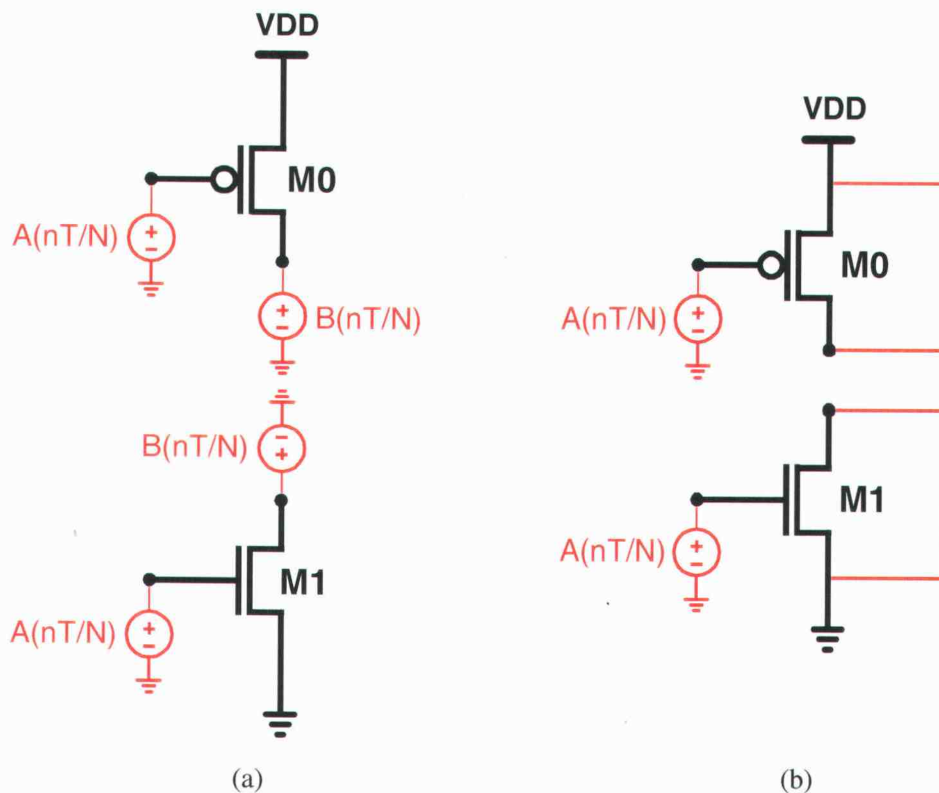


Figure 2.25 (a) In the direct method, voltage sources force the transistors to each discrete operating point and noise analysis is then performed. (b) In the indirect method, the gates are forced to each discrete operating point. The drain is shorted to the source, and gds_0 is found.

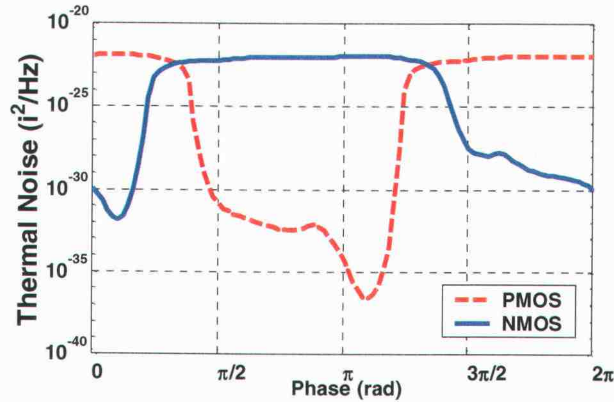


Figure 2.26 Cyclostationary noise calculated using the direct method.

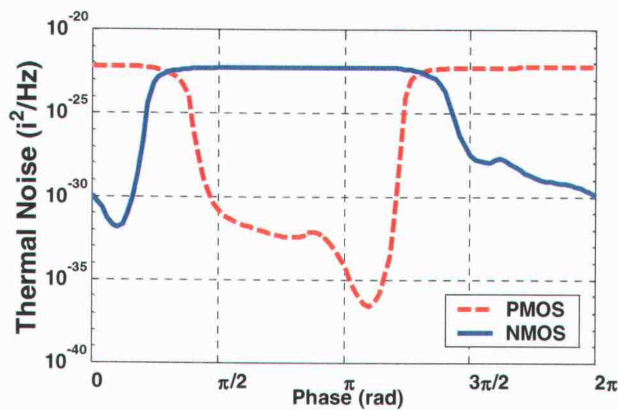
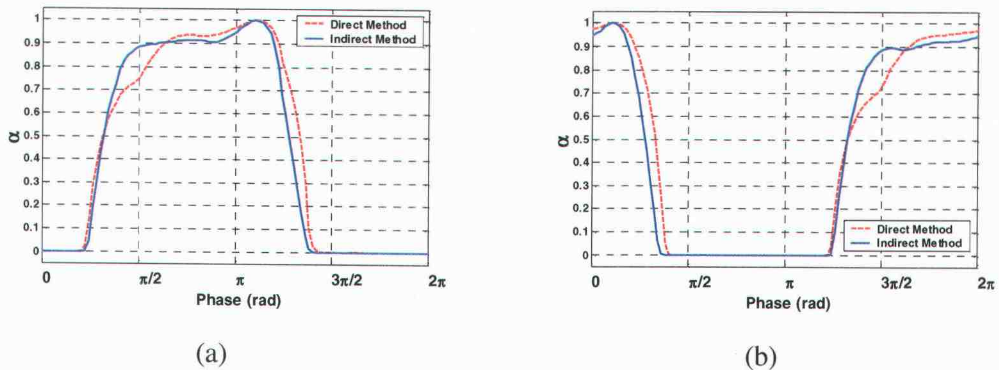


Figure 2.27 Cyclostationary noise calculated using the indirect method.

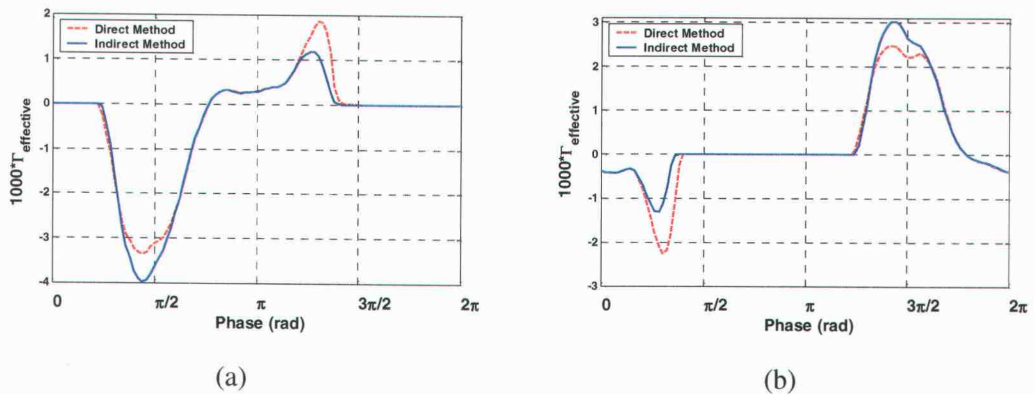
Using the definition of $\alpha(x)$ in (2.34), the α curves for the two different methods are shown in Figure 2.28. Both methods show that for the 5-stage ring oscillator the NMOS and PMOS transistors are either generating a large amount of thermal noise or are completely turned off. Although it appears from Figure 2.28 that the methods generate nearly identical results, the differences are significant when the effective ISFs are calculated in Figure 2.29. The ISFs calculated using the direct method are more symmetric than the indirect method counterparts. This result holds true for nearly all oscillator architectures and bias points, and

indicates the indirect method will predict more flicker noise up-conversion than the direct method. The difference is enough that phase noise simulations using both methods are presented in Chapter 5.



(a) (b)

Figure 2.28 The cyclostationary noise for (a) the NMOS transistor and (b) the PMOS transistor for both methods.



(a) (b)

Figure 2.29 The effective ISFs for (a) the NMOS transistor and (b) the PMOS transistor for both methods.

2.5. Calculating the Device Flicker Noise Corner

As explained previously, the phase noise close to the oscillation frequency is dominated by device flicker noise. Equation (2.26) shows the relationship between the flicker noise

corner of a device, $\omega_{1/f}$, and the flicker noise corner of the oscillator, ω_{1/f^3}. It is apparent that to accurately predict the phase noise spectrum close to the oscillation frequency, the flicker noise corner of all devices must be known. To calculate the flicker noise corners, the direct method of finding cyclostationary thermal noise was modified to also provide the instantaneous flicker noise corner over one cycle of oscillation. The device flicker noise corner $\omega_{1/f}$ is chosen as the peak magnitude of the curve because the peak magnitude of the ISF occurs at the same point. Again using the simple 5-stage single-ended ring oscillator in Figure 2.22 as an example, Figure 2.30 shows the instantaneous flicker noise corner of both devices for one oscillation cycle and several supply voltages. The flicker noise model and values of K_f are those used in Chapter 5 to obtain agreement between simulations and measurements. It can be seen from the plots that K_f increases as the supply voltage increases, a trend that follows from (1.2) and (1.6)

$$\omega_{1/f} \propto \frac{Flicker\ Noise}{Thermal\ Noise} \approx K \frac{g_m^2}{g_m} \approx K g_m \tag{2.54}$$

where K is a constant. Although in Figure 2.30(a) the device noise corner $\omega_{1/f}$ for the NMOS transistor is shown to be as high as 12MHz in a 0.35μm process, simulations in Figure 2.31 show that the same circuit in a 0.25μm process has equally high device flicker noise corners. This process was chosen for comparison because the BSIM3 flicker noise models were available based on measured devices.

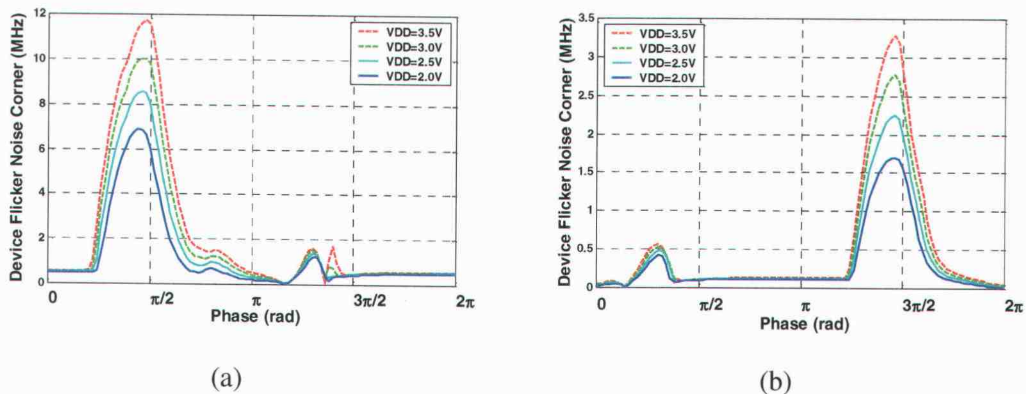
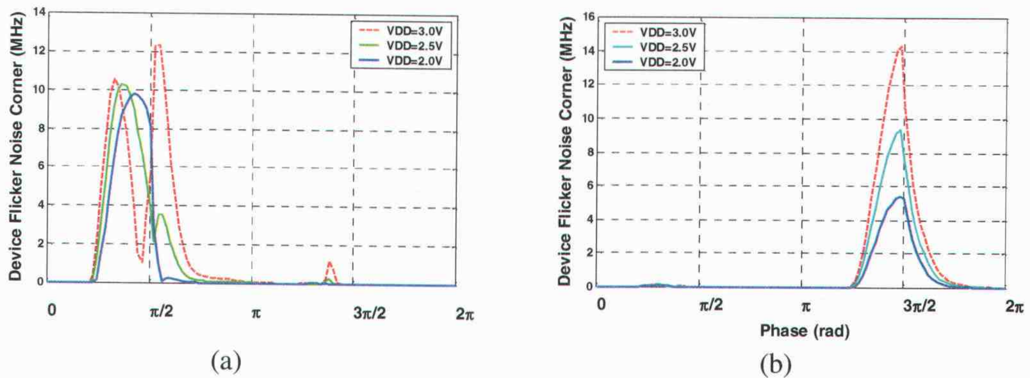


Figure 2.30 Instantaneous device flicker noise corner for (a) the NMOS transistor and (b) the PMOS transistor in Figure 2.22 using SPICE2 flicker and thermal noise models.



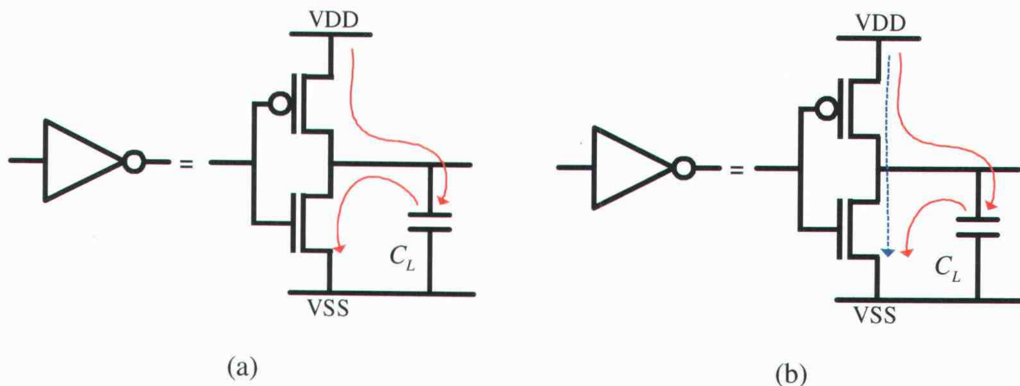
(a) (b)

Figure 2.31 Instantaneous device flicker noise corner for (a) the NMOS transistor and (b) the PMOS transistor in Figure 2.22 using the BSIM3 flicker and thermal noise models.

2.6. Short Circuit Current

Clearly shown in Leeson's phase noise model (2.4) and also true in the Hajimiri and Lee phase noise model, phase noise is inversely proportional to the power of the waveform. This power, however, is generally not the same as the power consumption of the oscillator because some power is lost due to the short circuit current [17]. Figure 2.32 illustrates the lost current. The power efficiency of an oscillator, E, can be defined as

$$E = \frac{P_{waveform}}{P_{dissipation}}. \tag{2.55}$$



(a) (b)

Figure 2.32 In an ideal ring oscillator (a) all current is used to charge the load capacitor, while in real oscillators (b) some current (dashed) is discharged directly to ground.

As an example, consider the delay cell of Figure 2.32 in a 3-stage ring oscillator. The oscillation frequency can be calculated as

$$\omega_o = \frac{\sqrt{3}}{2} \cdot \frac{g_m}{C_L} \tag{2.56}$$

where C_L is the load capacitance. The power dissipated by the capacitor is also the power of the waveform

$$P_{waveform} = \frac{C_L V_{sig}^2 \omega_o}{2\pi} \tag{2.57}$$

where V_{sig} is the voltage swing of the oscillator. Equation (2.56) can be substituted into (2.57)

$$P_{waveform} = \frac{\sqrt{3}\, \overline{g_m}\, V_{sig}^2}{4\pi} \tag{2.58}$$

to develop an equation for the power of the waveform. An equation for the average transconductance $\overline{g_m}$ is

$$\overline{g_m^2} = \frac{k' W \overline{I_D}}{L} \tag{2.59}$$

where $\overline{I_D}$ is the average supply current. This leads to

$$V_{dd} \cdot \overline{I_D} = P_{dissipation} = \frac{\overline{g_m^2}\, V_{dd}\, L}{k' W} \tag{2.60}$$

where V_{dd} is the supply voltage. The ratio of (2.58) to (2.60) is the definition of E

$$E = \frac{\sqrt{3}\, \overline{g_m}\, V_{sig}^2}{4\pi\, \overline{I_D}\, V_{dd}} = \frac{\sqrt{3}\, \overline{g_m}\, V_{sig}^2}{4\pi\, P_{dissipation}} \tag{2.61}$$

which shows that power efficiency and thus phase noise is dependent on the square of the voltage swing. Phase noise measurements and simulations of five architectures and ten oscillators in Chapter 5 show the two architectures with rail-to-rail voltage swing to be superior to the three architectures with less than rail-to-rail voltage swing by at least 10dB.

2.7. Phase Noise Figure of Merit

It is easily seen from (2.4) that the phase noise of an oscillator is dependent on the square of the oscillation frequency and linearly on its power dissipation. Comparing the phase noise

performance of oscillators with different oscillation frequencies and power dissipations is an apples to oranges comparison unless the phase noise is normalized with respect to oscillation frequency and power dissipation. Power normalization can be done according to

$$L\{\Delta\omega\} = L\{\Delta\omega\} - 10 \cdot \log_{10}\left(\frac{P}{P_{Ref}}\right) \tag{2.62}$$

where P is the power dissipation of the oscillator and P_{Ref} is the power dissipation of a reference oscillator. This can be seen in simulation as shown by Figure 2.33. In Figure 2.33(a), a simple, 3-stage single-ended oscillator with a power dissipation of 10mW is compared to a nearly identical oscillator where each transistor width has been scaled by five times to increase the power consumption to 50mW. Because all the transistor widths were scaled by the same factor, only the power dissipation changes and the frequency of oscillation remained constant. Figure 2.33(a) shows that the oscillator with more power dissipation has superior phase noise performance. Once the phase noise of the 50mW oscillator has been normalized with respect to 10mW in Figure 2.33(b), the oscillators have identical performance as expected.

Frequency normalization can be done according to

$$L\{\Delta\omega\} = L\{\Delta\omega\} - 10 \cdot \log_{10}\left(\frac{f}{f_{Ref}}\right) \tag{2.63}$$

where f is the frequency of oscillation and f_{Ref} is the frequency of a reference oscillator. Again, simulations show the validity of this normalization. Figure 2.34 shows simulations using SpectreRF and H&L done on three, 3-stage simple single-ended ring oscillators. The oscillator circuits are identical except for fixed capacitors that have been added to each stage to adjust the frequencies of oscillation to 200MHz, 100MHz and 50MHz. Each circuit has identical power dissipation. Figure 2.34(b) shows the result of normalizing phase noise to the 200MHz oscillator.

In general, oscillators are compared to a 1Hz, 1 watt reference oscillator at some specific offset frequency in what is known as a figure of merit (FOM)

$$FOM(\Delta\omega) = 20 \cdot \log_{10}(f_o) - L\{\Delta\omega\} - 10 \cdot \log_{10}(P) \; . \tag{2.64}$$

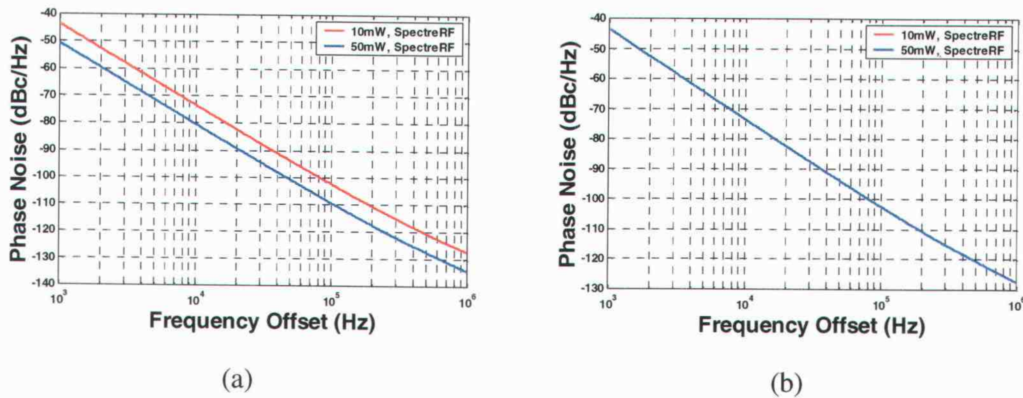


Figure 2.33 Phase noise (a) before power normalization and (b) after power normalization.

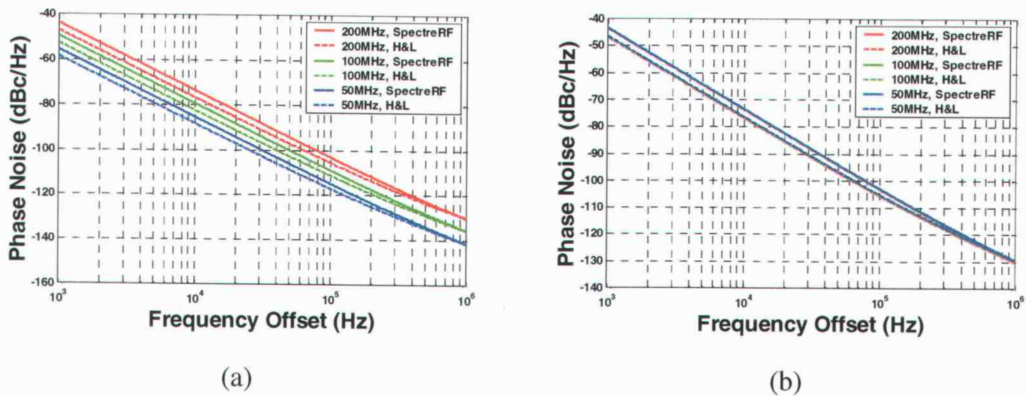


Figure 2.34 Phase noise (a) before frequency normalization and (b) after frequency normalization.

2.8. An improvement in Hajimri and Lee's Work

In the original paper outlining their general theory of phase noise, a single α curve is shown as the cyclostationary noise modulation function. This curve, shown in Figure 15 of [16], is for a simple 5-stage single-ended ring oscillator and is given as evidence that cyclostationary noise is not important in the treatment of phase noise in ring oscillators. It is clear, however, from previous sections that cyclostationary noise cannot be ignored in ring oscillators. Another implication of [16] is that symmetric oscillator rise and fall times always imply minimal flicker noise up-conversion because symmetric rise and fall times imply a symmetric ISF. To test this theory, the simple, 5-stage single-ended ring oscillator in Figure

2.35 was simulated. As shown in Figure 2.35(b), the delay cell's PMOS transistor is fixed in size, while the width of the NMOS device is adjusted. Simulations using the Hajimiri and Lee theory of phase noise and SpectreRF have been performed over a sweep of transistor sizes. These were used to calculate the oscillator flicker noise corner and figure of merit. If symmetric rise and fall times imply minimum flicker noise up-conversion, it is expected that the oscillator flicker noise corner would be a minimum at a NMOS transistor width of approximately 20μm, since the mobility of NMOS transistors is approximately four times that of PMOS transistors. It can be seen in Figure 2.36(a) that only SpectreRF with the BSIM3v3 flicker noise model predicts a local minimum with width, and at a width that gives a non-symmetric ISF. Figure 2.36(b) shows the FOM at a 1MHz offset with only white noise considered. This plot also shows an absence of a "magic" ratio that significantly minimizes phase noise.

The Hajimiri and Lee model neglected the importance of cyclostationary noise in ring oscillators. If cyclostationary noise is considered, then it is the symmetry of the effective ISF that is important and the relationship between rise and fall times, the ISF and flicker noise up-conversion becomes a complex issue.

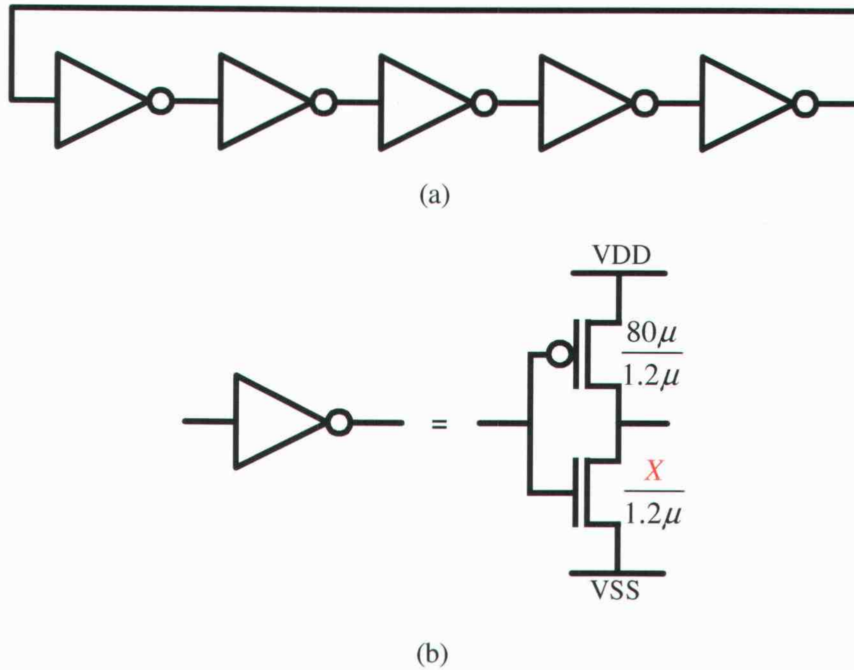
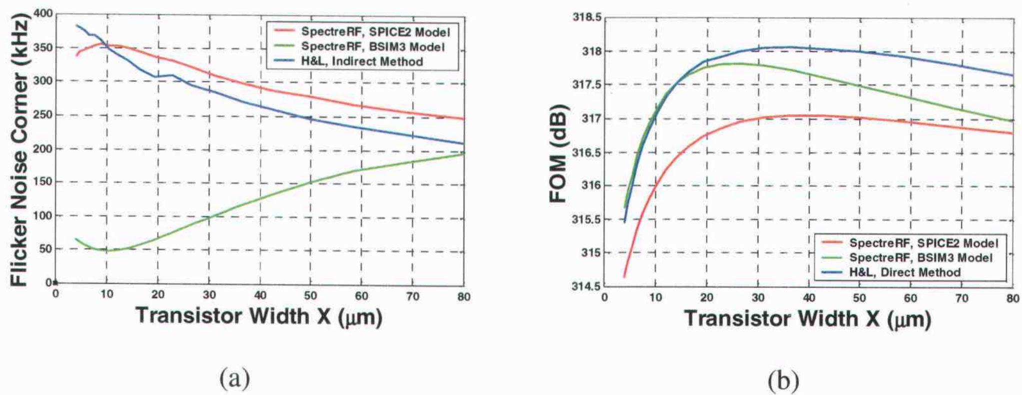


Figure 2.35 (a) A 5-stage ring oscillator and (b) delay cell with adjustable NMOS width.



(a) (b)

Figure 2.36 The oscillator flicker noise corner versus transistor width for several flicker noise models is given in (a) while (b) calculates the 1MHz figure of merit.

3. JITTER IN RING OSCILLATORS

Phase noise in oscillators is defined as the uncertainty of the exact frequency. Jitter in oscillators is the dual case where the uncertainty is in the exact period. Phase noise is important in communications systems where spectral purity about the carrier must meet specifications. Data sampling, clock recovery and digital logic applications, however, are primarily concerned with timing margins. Events on a chip are expected to occur at specific instances in time. In the case of data sampling, uncertainty in these events degrades the maximum achievable linearity. Jitter in clock recovery applications increases the bit error rate (BER) and, in digital logic applications, a reduction in jitter allows the logic to operate at higher frequencies. Ring oscillators are crucial blocks in these and other applications. The performance of a ring oscillator, however, is significantly limited by noise. This in turn limits the performance of the system in which it is placed. On-chip oscillators suffer not only from intrinsic device noise but also from noise coupled onto the supply lines and into the silicon substrate from the switching nature of the digital blocks.

In general noise sources can be categorized into two broad groups:

- Random signals which are stochastic in nature such as thermal, shot and flicker noise.
- Deterministic signals such as supply and substrate noise, electromagnetic or direct coupling of power lines (60Hz) and broadcast (TV, radio, etc.) signals.

The relationship between random noise sources and oscillator jitter has been studied extensively [17], [23], [24] and will not be covered in this work. Little previous work, however, exists regarding jitter and deterministic noise sources. In [24], oscillator jitter due to deterministic noise sources is studied with the limitation that the noise frequency is significantly less than the oscillation frequency.

3.1. Jitter Definitions

In an ideal oscillator, the zero crossings of the rising edge happen precisely at nT, where n is the nth period and T, the period, is a constant. However, in the presence of noise, deterministic or otherwise, T becomes a function of n, denoted by T_n. This results in a time

deviation of $\Delta T_n = T_n - \bar{T}$ from the mean period $\bar{T}$ at every cycle. This deviation (or jitter) ΔT_n can be expressed as absolute or long-term jitter [4] in that it shows the cumulative effect of noise on the period of the oscillator

$$\sigma_{aj} = \sum_{n=1}^{N} \Delta T_n . \tag{3.1}$$

Another jitter metric is cycle jitter

$$\sigma_{cj} = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} \Delta T_n^2} \tag{3.2}$$

which also considers the short-term dynamics of jitter. The jitter metric cycle-to-cycle jitter depends completely on the short-term dynamics

$$\sigma_{c-cj} = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} \left(T_{n+1} - T_n\right)^2} . \tag{3.3}$$

3.2. Peak Jitter

It has been widely shown that in the presence of device noise only, the absolute jitter of a free-running oscillator generally monotonically increases with the square root of the measurement interval ΔT [17], [23]

$$\sigma_{aj} \approx \kappa\sqrt{\Delta T} \tag{3.4}$$

as shown in Figure 3.1(a). It will be shown later that the absolute jitter of a free-running oscillator in the presence of purely sinusoidal noise injection at one frequency is periodic in time, as shown in Figure 3.1 (b). The complete response to device and deterministic noise is the summation of the individual responses, shown in Figure 3.1 (c). When considering only the jitter due to device noise, represented by (3.4), κ is an important figure of merit. A new figure of merit is defined in this work for jitter due to deterministic noise, and it is the peak magnitude of the absolute jitter, as shown in Figure 3.2. Mathematically, peak jitter is

$$peak\ jitter = \max\left(\sigma_{aj}\right) - \min\left(\sigma_{aj}\right) . \tag{3.5}$$

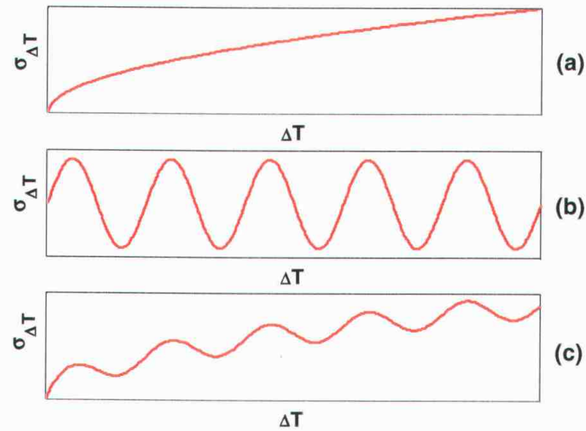


Figure 3.1 Absolute jitter due to (a) device noise, (b) sinusoidal noise, and (c) both device and sinusoidal noise.

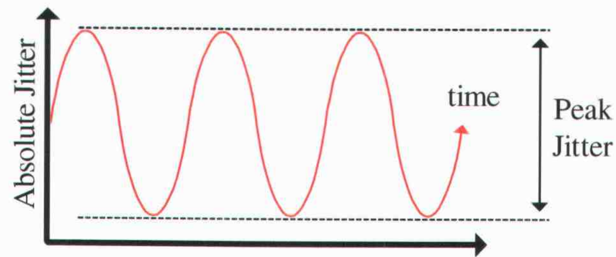


Figure 3.2 The definition of peak jitter.

3.3. Time Domain Analysis

In [17], it is noted that absolute phase jitter is given by

$$\sigma_{\Delta\phi} = E\left\{\Delta\phi^2\right\} = E\left\{\left\lfloor \phi(t+\Delta T) - \phi(t) \right\rfloor^2\right\} \tag{3.6}$$

where $E\{.\}$ is the expected value, ΔT is the observation time and from (2.8)

$$\Delta\phi = \int_0^{\Delta T} \frac{\Gamma(\omega_0 \tau)}{q_{\max}} i(\tau)\, d\tau\, . \tag{3.7}$$

From probability theory [25], the expected value of a function of a random variable is given by

$$E\left[g(x)\right]=\int_{-\infty}^{\infty} g(x)\,f_x(x)\,dx. \tag{3.8}$$

Using the result of (3.6) and (3.7) in (3.8) gives

$$\sigma_{\Delta\phi}^2=\frac{1}{q_{\max}^2}\int_0^{\Delta T}\int_0^{\Delta T}\Gamma(\omega_0\tau_1)\Gamma(\omega_0\tau_2)\cdot E\left[i(\tau_1)i(\tau_2)\right]d\tau_1 d\tau_2. \tag{3.9}$$

Suppose the noise current *i(t)* is defined as a pure sinusoid at frequency ω_i and peak magnitude I_i, $i(t)=I_i\cos(\omega_i t+\theta)$, then its autocorrelation is defined as

$$R_{ii}(t_1,t_2)=E\left[i(t_1)i(t_2)\right] \tag{3.10}$$

which can be solved resulting in

$$E\left[i(t_1)i(t_2)\right]=\frac{I_i^2}{2}\cos\left[(\tau_1-\tau_2)\omega_i\right]. \tag{3.11}$$

Equation (3.11) can be substituted into (3.9)

$$\sigma_{\Delta\phi}^2=\frac{I_i^2}{2q_{\max}}\int_0^{\Delta T}\int_0^{\Delta T}\Gamma(\omega_0\tau_1)\Gamma(\omega_0\tau_2)\cos\left[(\tau_1-\tau_2)\omega_i\right]d\tau_1 d\tau_2 \tag{3.12}$$

and the use of the trigonometric identity $\cos(\alpha-\beta)=\cos(\alpha)\cos(\beta)+\sin(\alpha)\sin(\beta)$ gives

$$\sigma_{\Delta\phi}^2=\frac{I_i^2}{2q_{\max}^2}\cdot\left[\int_0^{\Delta T}\int_0^{\Delta T}\Gamma(\omega_0\tau_1)\Gamma(\omega_0\tau_2)\cos(\omega_i\tau_1)\cos(\omega_i\tau_2)\,d\tau_1 d\tau_2+\right.$$
$$\left.+\int_0^{\Delta T}\int_0^{\Delta T}\Gamma(\omega_0\tau_1)\Gamma(\omega_0\tau_2)\sin(\omega_i\tau_1)\sin(\omega_i\tau_2)\,d\tau_1 d\tau_2\right]. \tag{3.13}$$

The integrals can be separated

$$\sigma_{\Delta\phi}^2=\frac{I_i^2}{2q_{\max}^2}\cdot\left[\int_0^{\Delta T}\Gamma(\omega_0\tau_1)\cos(\omega_i\tau_1)\,d\tau_1\int_0^{\Delta T}\Gamma(\omega_0\tau_2)\cos(\omega_i\tau_2)\,d\tau_1\right.$$
$$\left.+\int_0^{\Delta T}\Gamma(\omega_0\tau_1)\sin(\omega_i\tau_1)\,d\tau_1\int_0^{\Delta T}\Gamma(\omega_0\tau_2)\sin(\omega_i\tau_2)\,d\tau_1\right] \tag{3.14}$$

and simplified to

$$\sigma_{\Delta\phi}^2 = \frac{I_i^2}{2q_{\max}^2} \cdot \left[\left(\int_0^{\Delta T} \Gamma(\omega_0\tau)\cos(\omega_i\tau) \right)^2 + \left(\int_0^{\Delta T} \Gamma(\omega_0\tau)\sin(\omega_i\tau) \right)^2 \right]. \tag{3.15}$$

Again using the Fourier expansion from (2.9), (3.15) can be integrated, and with the relationship between absolute phase jitter and absolute jitter defined by (3.16) [17],

$$\sigma_{aj} = \frac{\sigma_{\Delta\phi}}{\omega_0} \tag{3.16}$$

the equation for absolute jitter is

$$\begin{aligned}\sigma_{\Delta T}^2 = \frac{I_i^2}{8\omega_0^2 q_{\max}^2} \bullet \Bigg\{ & \left(\frac{c_0 \sin(\omega_i \Delta T)}{\omega_i} + \sum_{n=1}^{\infty} \frac{c_n \sin\left[(n\omega_0 + \omega_i)\Delta T\right]}{n\omega_0 + \omega_i} \right. \\ & \left. + \sum_{n=1}^{\infty} \frac{c_n \sin\left[(n\omega_0 - \omega_i)\Delta T\right]}{n\omega_0 - \omega_i} \right)^2 + \left[\frac{c_0}{\omega_i} - \frac{c_0 \cos(\omega_i \Delta T)}{\omega_i} \right. \\ & + \sum_{n=1}^{\infty} c_n \left(\frac{\cos\left[(n\omega_0 - \omega_i)\Delta T\right]}{n\omega_0 - \omega_i} - \frac{1}{n\omega_0 - \omega_i} \right) \\ & \left. + \sum_{n=1}^{\infty} c_n \left(\frac{1}{n\omega_0 + \omega_i} - \frac{\cos\left[(n\omega_0 + \omega_i)\Delta T\right]}{n\omega_0 + \omega_i} \right) \right]^2 \Bigg\}. \end{aligned} \tag{3.17}$$

In the case of noise that is injected symmetrically, the starting point of (3.7) should be changed to the equation for excess phase (2.27). The analysis is similar to that which leads to (3.17). The equation for absolute jitter when noise is injected symmetrically into all stages is given by (3.18).

In both equations N is the number of stages in the ring oscillator and ω_i is the noise frequency. The c_n's are the Fourier coefficients of the ISF [20]. I_i is the peak value of the noise current and ΔT is the measurement interval. These equations allow calculation of the absolute jitter as a function of ΔT due to injected sinusoidal noise by using the Fourier coefficients of the ISF. The significant differences between (3.17) and (3.18) are that in (3.17) all Fourier coefficients are important, while in (3.18) only the Fourier coefficients that are at integer multiples of N are significant to jitter. Also, in (3.17) there is a peaking of the jitter at integer multiples of ω_0, while in (3.18) there is peaking at only integer multiples of $N\omega_0$. Both (3.17) and (3.18) are periodic in ΔT.

$$
\begin{aligned}
\sigma_{\Delta T}^{2} = \frac{N\ I_i^2}{8\omega_0^2 q_{\max}^2} \bullet \Bigg\{ & \left(\frac{c_0 \sin(\omega_i \Delta T)}{\omega_i} + \sum_{n=1}^{\infty} \frac{c_{nN} \sin\left[(nN\omega_0 + \omega_i)\Delta T\right]}{nN\omega_0 + \omega_i} \right. \\
& \left. + \sum_{n=1}^{\infty} \frac{c_{nN} \sin\left[(nN\omega_0 - \omega_i)\Delta T\right]}{nN\omega_0 - \omega_i} \right)^2 + \left[\frac{c_0}{\omega_i} - \frac{c_0 \cos(\omega_i \Delta T)}{\omega_i} \right. \\
& + \sum_{n=1}^{\infty} c_{nN} \left(\frac{\cos\left[(nN\omega_0 - \omega_i)\Delta T\right]}{nN\omega_0 - \omega_i} - \frac{1}{nN\omega_0 - \omega_i} \right) \\
& + \sum_{n=1}^{\infty} c_{nN} \left(\frac{\cos\left[(nN\omega_0 - \omega_i)\Delta T\right]}{nN\omega_0 - \omega_i} - \frac{1}{nN\omega_0 - \omega_i} \right) \\
& \left. + \sum_{n=1}^{\infty} c_{nN} \left(\frac{1}{nN\omega_0 + \omega_i} - \frac{\cos\left[(nN\omega_0 + \omega_i)\Delta T\right]}{nN\omega_0 + \omega_i} \right) \right]^2 \Bigg\}. \qquad (3.18)
\end{aligned}
$$

3.4. Peak Jitter Figure of Merit

From (3.17) and (3.18) it is evident that absolute jitter is proportional to the amount of injected noise and inversely proportional to the oscillation frequency. The 5-stage simple ring oscillator in Figure 3.3 has been simulated with Spectre in the time domain to verify these results. To model substrate noise, a current source in parallel with a resistor is connected to the bulks of all NMOS transistors as shown in Figure 3.3(b). If it became necessary to set the frequency of oscillation, the value of the capacitor C was adjusted. The first experiment was to inject sinusoidal currents over a wide range of frequencies and calculate the resulting jitter. Figure 3.4(a) shows the results for noise current magnitudes of 500μA and 750μA. In Figure 3.4(b), each jitter curve has been normalized to the 500μA noise current injection waveform, and it can be seen that the 750μA noise current injection waveform is roughly 1.5 times greater, as predicted by (3.17) and (3.18). In the second experiment, the capacitor C was adjusted to give oscillation frequencies of 200MHz, 100MHz and 50MHz and a constant amplitude noise current was swept over frequency. The peak jitter responses are shown in Figure 3.5(a), and the responses normalized to the 200MHz waveform are shown in Figure 3.5(b). Although somewhat noisy due to simulator artifacts, jitter is shown to be inversely

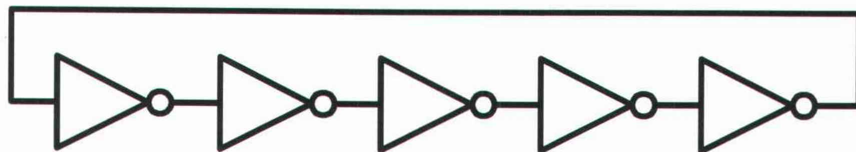
proportional to the frequency of oscillation. To make fair comparisons between different oscillators, these dependencies can be normalized by use of (3.19) and (3.20).

$$\sigma_{\Delta T}(\omega_i) = \frac{\sigma_{\Delta T}(\omega_i)}{I} \tag{3.19}$$

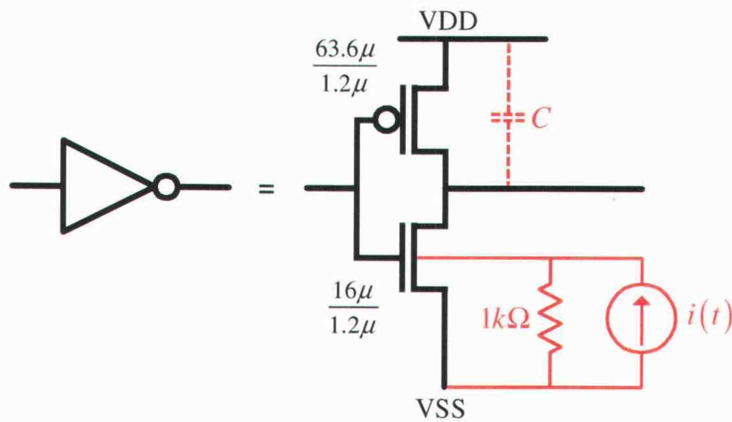
$$\sigma_{\Delta T}(\omega_i) = \omega_0\, \sigma_{\Delta T}(\omega_i) \tag{3.20}$$

The results of (3.19) and (3.20) can be combined for an oscillator figure of merit

$$FOM(\omega_i) = \frac{\omega_0\, \sigma_{\Delta T}(\omega_i)}{I}\,. \tag{3.21}$$

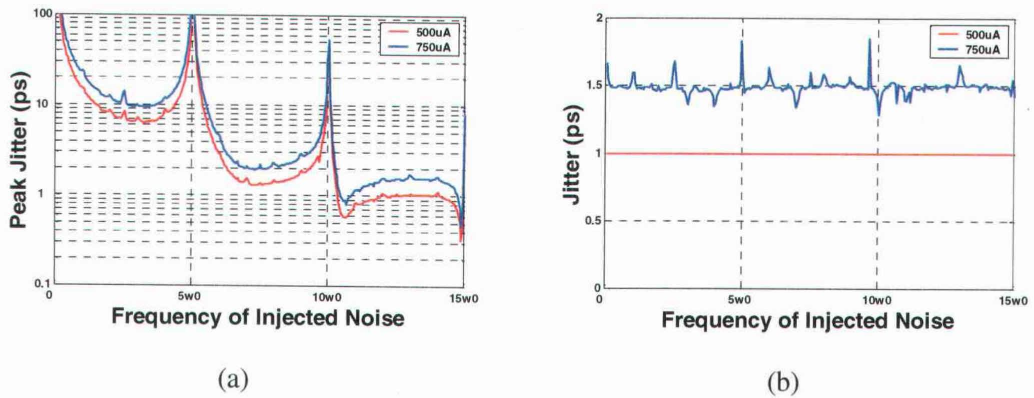


(a)



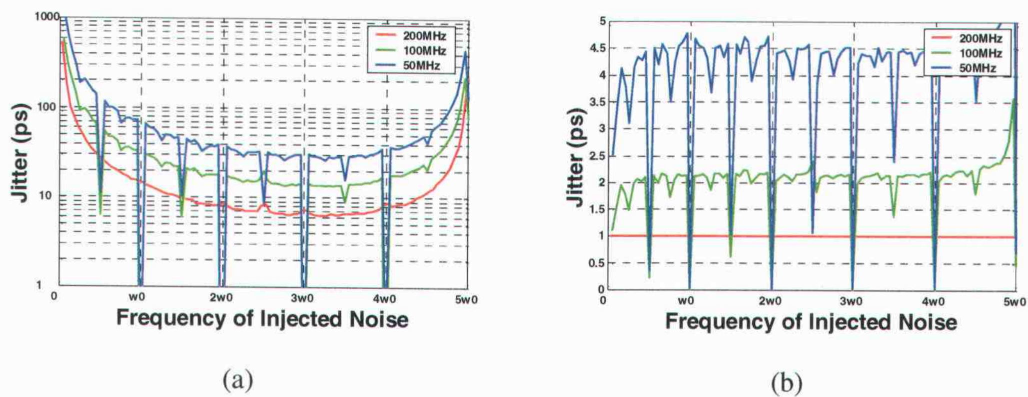
(b)

Figure 3.3 (a) 5-stage oscillator circuit and (b) delay cell with simple substrate model.



(a) (b)

Figure 3.4 (a) The peak jitter due to two different noise current magnitudes is shown. (b) Both curves from (a) are normalized to the magnitude of the 500μA curve. This plot shows peak jitter is a linear function of the injected noise current.



(a) (b)

Figure 3.5 (a) The peak jitter of three oscillators with different oscillation frequencies is simulated. (b) The curves from (a) are normalized to the 200MHz oscillator. This plot shows peak jitter is inversely proportional to the oscillator frequency.

4. TEST CHIP DESIGN AND LAYOUT

To validate the various aspects of the work done in predicting phase noise and jitter, a test chip was designed in the TSMC 0.35μm CMOS process. In all, 16 ring oscillators were designed, each with a specific purpose; each falls into one of two categories. In the first category are oscillators primarily designed to determine the correct flicker noise model, test prediction of phase noise, study layout technique and compare the performance of different oscillator architectures. In the second category, oscillator circuits and layouts are designed to test the results of (3.17) and (3.18) by injecting noise symmetrically and asymmetrically into the circuits and measuring the jitter response. Also, two single-ended ring oscillator (SERO) designs from a 1998 test chip will be shown because the chip contained a unique architecture.

All but one of the differential ring oscillator (DRO) designs, the PMOS pre-drive oscillator, are 3-stage designs represented by Figure 4.1.

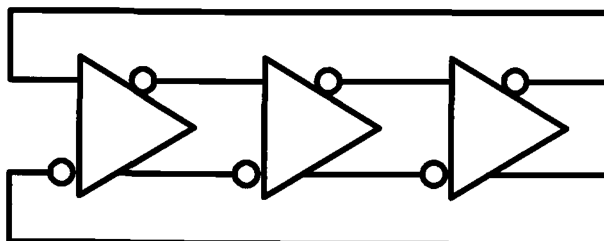


Figure 4.1 Three-stage differential ring oscillator.

4.1. Category 1 Oscillators – Phase Noise

In this category, three single-ended oscillators, the H&L series, were used to study flicker noise, one singled-ended oscillator was used to study a distributed layout technique, and four differential oscillators were used to study architecture performance. The differential oscillator topologies were based on a basic or "vanilla" delay cell (Figure 4.4), a Maneatis load delay

cell (Figure 4.5), a delay cell based on cross-coupled loads (Figure 4.6), and a PMOS pre-drive delay cell (Figure 4.7).

4.1.1. Three H&L series oscillators

As noted in Chapter 1 and Section 2.5, there are three competing flicker noise models, each with different results as illustrated in the example of Figure 2.36. To aid in determining the correct flicker noise model, three different instances of the simple 5-stage single-ended ring oscillator in Figure 2.35 were designed. The measured oscillator flicker noise corners were used to determine the correct noise model and extract the fitting parameters. With this in mind, the NMOS widths chosen were 8μm, 20μm and 49.6μm; the PMOS width is constant at 80μm. In this thesis, these oscillators are referred to as H&L1, H&L2 and H&L3, respectively.

A representative layout of these oscillators is shown in Figure 4.2. The PMOS transistors are at the top of the figure, the NMOS transistors are at the bottom and connections are in the middle. For symmetry reasons, the transistors of each stage are folded and interdigitated with the transistors of other stages. Two dummy transistors are at each end, and the green areas show bulk connections above and below each transistor strip.

4.1.2. Distributed oscillator layout

Although significant work has been published relating circuit design and phase noise, no work has been published showing the influence between layout and phase noise. It is important to know the relationship because phase noise measurements are generally several dB above the simulated values and are usually attributed to "mystery" noise sources unaccounted for in the simulation, or inaccuracy in the models. As an experiment in the layout, the interdigitated layout of Figure 4.2 was rearranged so that each stage was laid out sequentially, as shown in Figure 4.3. The schematic is the same in both cases. In the layout of Figure 4.3, each stage is isolated by a ring of grounded substrate connections that are a minimum of 6.4μm wide, and the NMOS transistors of each stage are separated by a minimum of 28μm. The experiment was to determine which layout is more beneficial-an interdigitated or isolated sequential layout.

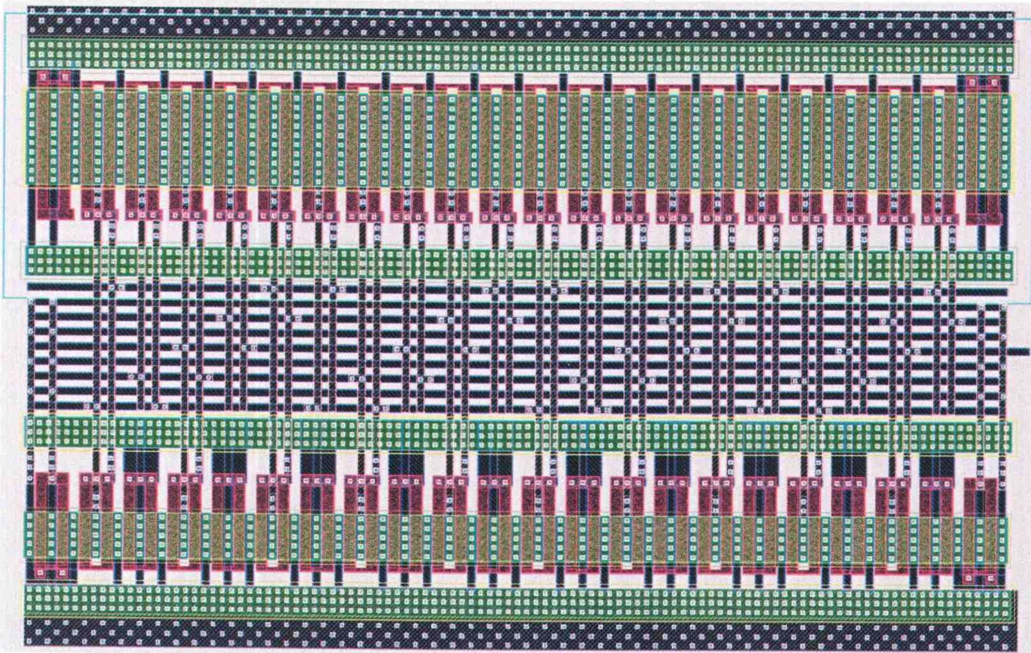


Figure 4.2 Layout of the oscillator in Figure 2.35. The NMOS transistors in each stage are 20μm in width and the PMOS transistors are 80μm.

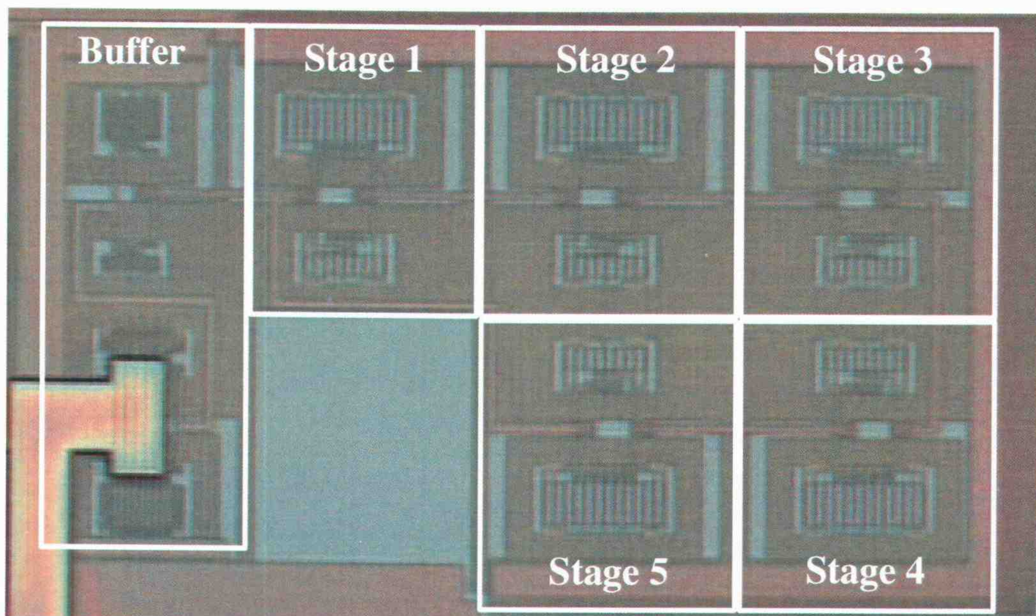


Figure 4.3 Die photo of the distributed oscillator layout.

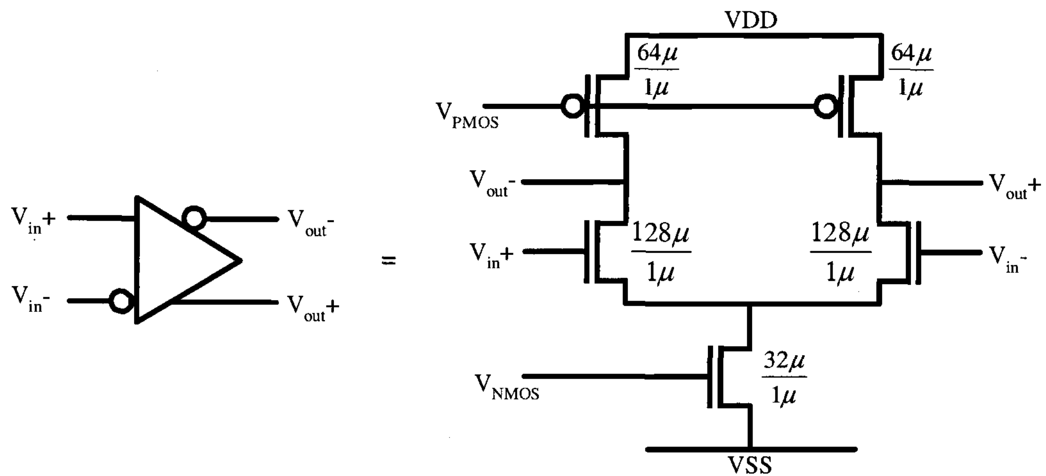


Figure 4.4 A simple or "vanilla" delay cell.

4.1.3. *Vanilla differential*

The "vanilla" circuit is the simplest differential delay cell architecture. As such, it is useful in comparing the performance of other differential delay cell architectures. PMOS and NMOS bias voltages are needed for setting the load impedance and current, respectively. The delay cell with transistor sizes is shown in Figure 4.4.

4.1.4. *Maneatis load delay cell*

In the Maneatis architecture, shown in Figure 4.5 with transistor sizes, a diode-connected PMOS device is added in shunt to an equally sized PMOS device. This pair is referred to as a symmetric load because the I-V characteristics are symmetric about the center of the voltage swing [26], [27]. Non-linear loads can convert common-mode noise to differential mode noise. While still non-linear, the symmetrical loads can be exploited to achieve supply noise rejection. Also, the symmetric loads extend the oscillation frequency range over the vanilla differential circuit [28].

4.1.5. Cross-coupled loads

The cross-coupled load architecture is an extension of the Maneatis delay cell with the addition of cross-coupled transistors. It has been found that the cross coupling can lower the 1/f oscillator noise corner by exploiting single-ended symmetry in the oscillator's waveform [29], [30]. The schematic of the delay cell with transistor sizing is shown in Figure 4.6.

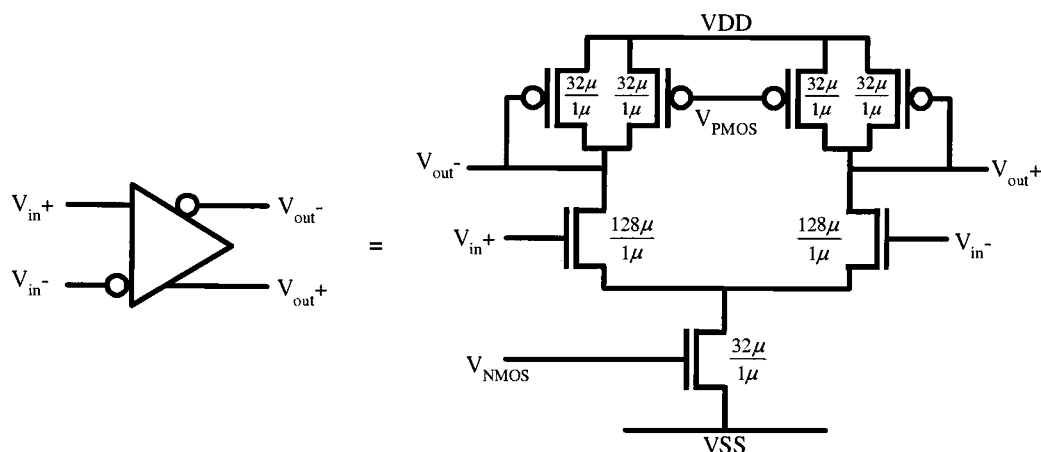


Figure 4.5 Maneatis load delay cell.

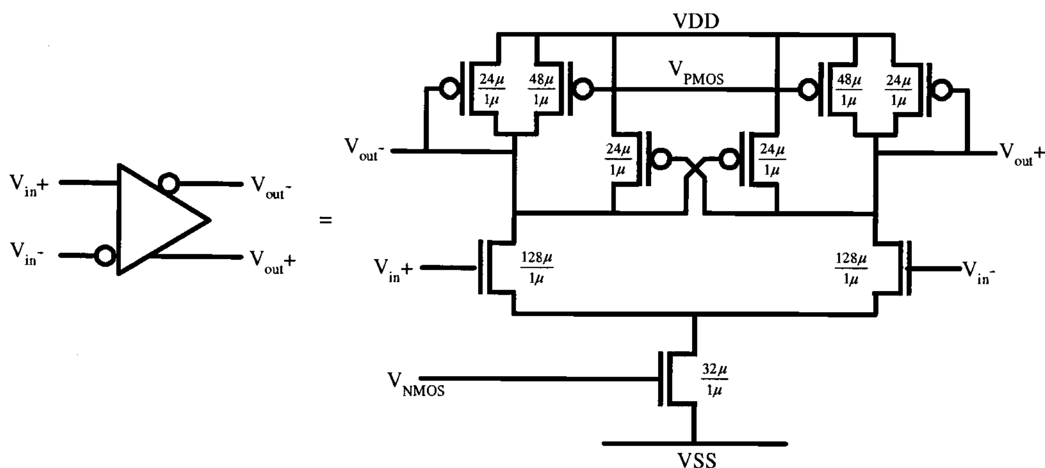


Figure 4.6 Cross-coupled load delay cell.

4.1.6. PMOS pre-drive

The PMOS pre-drive oscillator is a differential oscillator with an architecture shown in Figure 4.7(a) and a delay cell shown in Figure 4.7(b) [31]. Although a differential circuit, it does not rely on a current mirror to fix the power consumption as is the case with the three architectures discussed previously. The current is set by transistor sizing and supply voltage. As such, it provides rail-to-rail oscillation swing and drives all transistors into cutoff during part of each oscillation cycle, both of which are beneficial to phase noise. In each half circuit, the PMOS loads are driven by the signal from the preceding stage and from two preceding stages giving rise to dual delay paths. Frequency tuning is provided by interpolating between the dual delay paths.

Ring oscillators can be classified as saturated and non-saturated [31], depending on the switching characteristics of the delay cell. In the non-saturated type, the transistors in the delay cell never fully switch and are never driven into cutoff, while in the saturated type some or all of the transistors in the delay cell are driven into cutoff. The vanilla differential, Maneatis load and cross-coupled load oscillators are examples of non-saturated oscillators, while the PMOS pre-drive is a saturated oscillator. As such, it is expected to give superior phase noise performance.

4.2. Category 2 - Jitter

Eight oscillators and layouts were designed to test the results of (3.17) and (3.18) by injecting noise symmetrically and asymmetrically into the circuits and then measuring the jitter response. Four oscillators are 3-stage SERO designs and four oscillators are 3-stage DRO designs based on the Maneatis delay cell. The simplified schematic for the SERO is shown in Figure 4.8. This design uses simple inverting delay stages and the oscillation frequency is determined completely by parasitic capacitance. The delay cell of the DRO is shown in Figure 4.9. Its frequency of oscillation is dependent on the NMOS and PMOS bias voltages. All SERO and DRO oscillators have identical schematics. The oscillator's layout determines whether the noise is injected symmetrically or asymmetrically.

(a)

(b)

Figure 4.7 (a) PMOS pre-drive differential ring oscillator and (b) delay cell.

To adequately validate the predictive jitter equations, the jitter response should be measured to injected noise frequencies of at least $2N\omega_0$. It is difficult to inject noise at significant power levels over approximately 600MHz, giving

$$2N\omega_0 = 600MHz \tag{4.1}$$

where N is the number of stages and ω_0 is the oscillation frequency. The minimum number of stages in a ring oscillator is 3, which constrains the oscillation frequency to approximately 100MHz. An oscillation frequency of 80MHz and power consumption of 3.7mW were chosen for the SERO design and the DRO design when biased at a V_{NMOS} of 1.2V and a V_{PMOS} equal to

1.5V. To slow the oscillators, transistor gates were used to add capacitance as shown by the dummy (red) transistors in Figure 4.8 and Figure 4.9.

4.2.1. Supply noise injection

The die photos in Figure 4.10 and Figure 4.11 highlight the difference between symmetric and asymmetric noise injection. In Figure 4.10, a single supply line feeds all 3 oscillator stages. Noise present on the supply line affects all stages equally. In Figure 4.10, however, two supply lines feed the oscillator. This allows a single stage to be affected by supply noise. The layouts for the symmetric/asymmetric DRO cases are very similar and are shown in Appendix C.

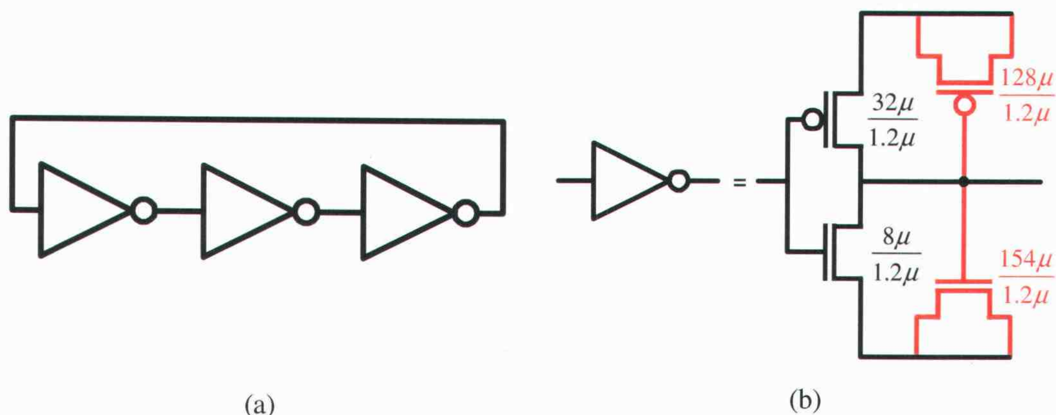


Figure 4.8 (a) Single-ended ring oscillator and (b) delay cell for jitter measurement.

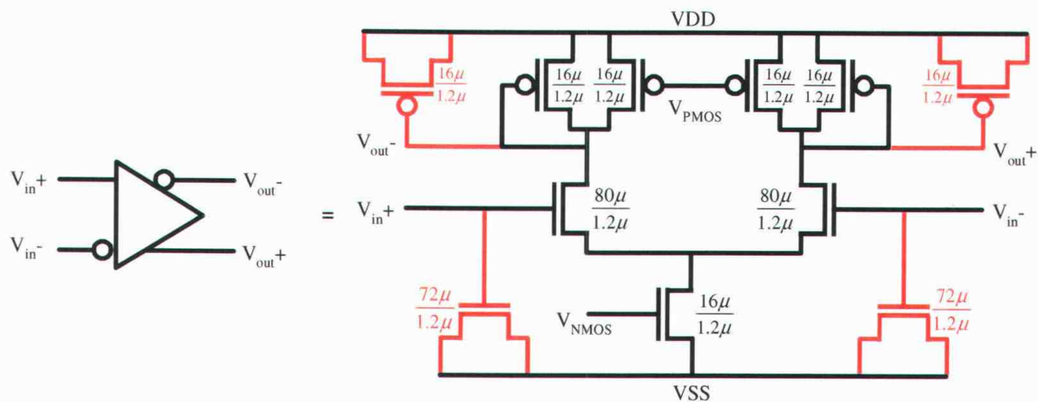


Figure 4.9 Delay cell of the differential oscillators designed for jitter measurement.

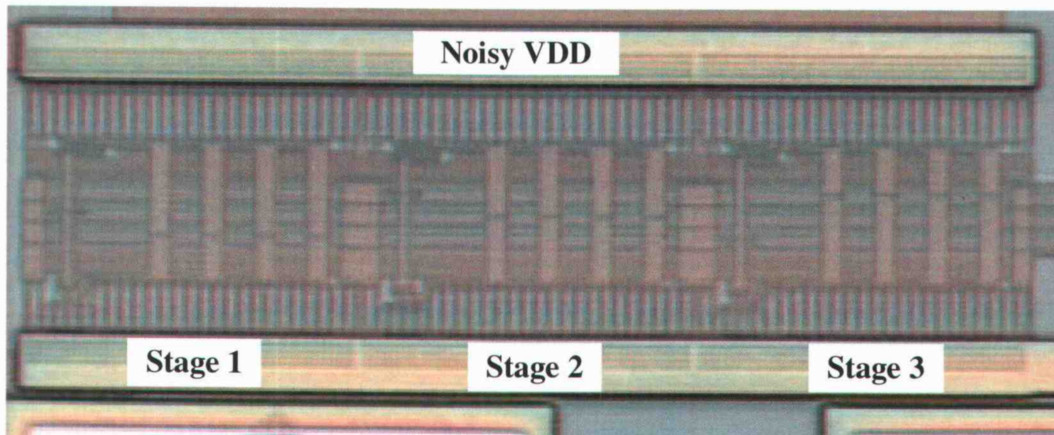


Figure 4.10 Die photo of the single-ended symmetric supply noise injection circuit.

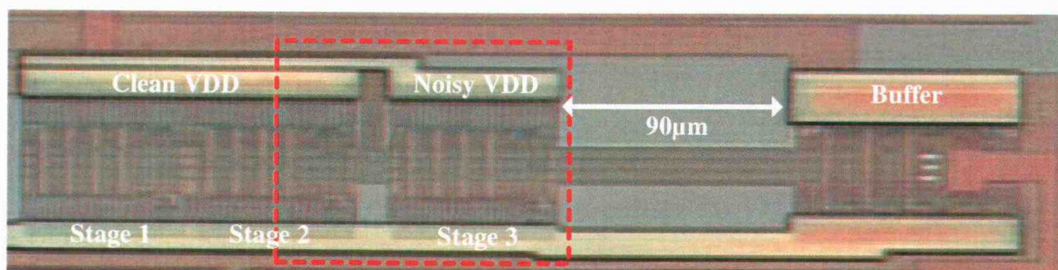


Figure 4.11 Die photo of the single-ended asymmetric supply noise injection circuit. The area inside the dashed red box is shown in Figure 4.12. The space between the oscillator and buffer is 90μm.

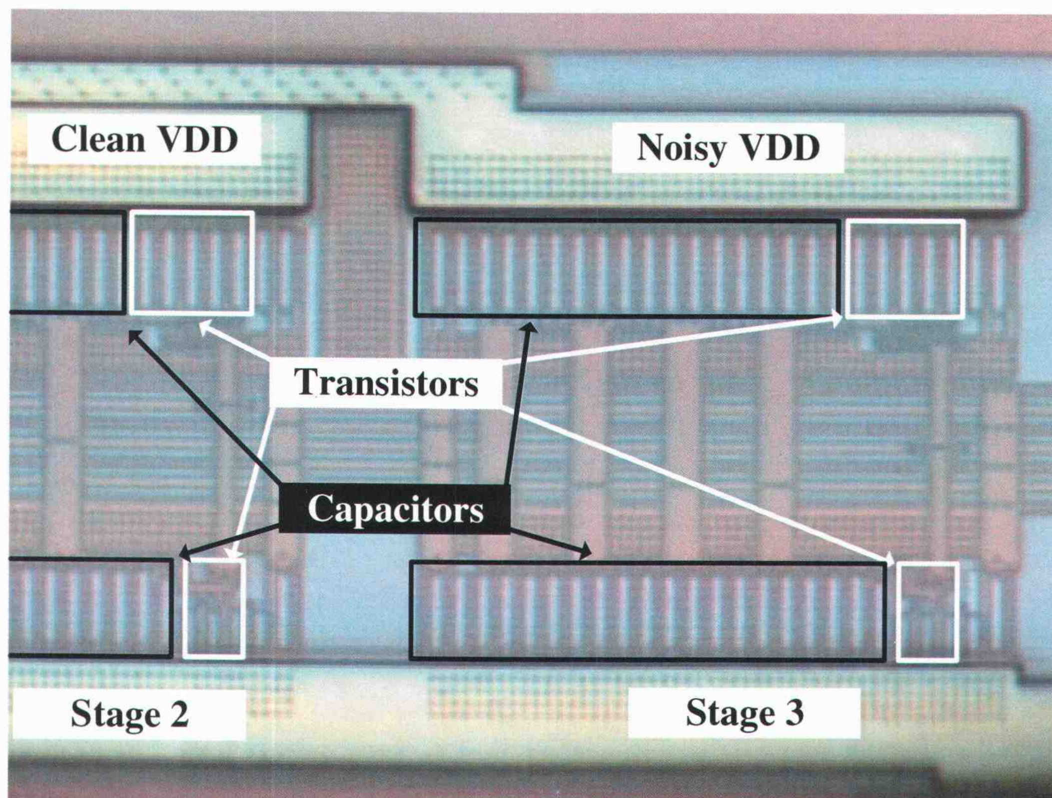


Figure 4.12 Die photo of the single-ended asymmetric supply noise injection circuit showing the separation between the clean and noisy supplies.

4.2.2. Substrate noise injection

To inject substrate noise asymmetrically, noise injectors were placed to primarily affect one stage, as shown in Figure 4.13(a). Noise injectors are small p+ doped regions in the substrate and are placed above and below the oscillator to induce noise current to flow through the oscillator. Figure 4.14 shows the die photo for the single-ended asymmetric substrate layout. The substrate injectors are to the far right, and sit above the transistors in the third stage. The stages are oriented so the transistors in Stages 1 and 2 are located far from the substrate injectors. For symmetric noise injection, injectors were placed to affect all stages, as shown in Figure 4.13(b). Figure 4.15 shows the layout of the single-ended symmetric substrate layout. The layout for the SERO and DRO cases are very similar, except that in the SERO symmetric substrate case the transistors were interdigitated.

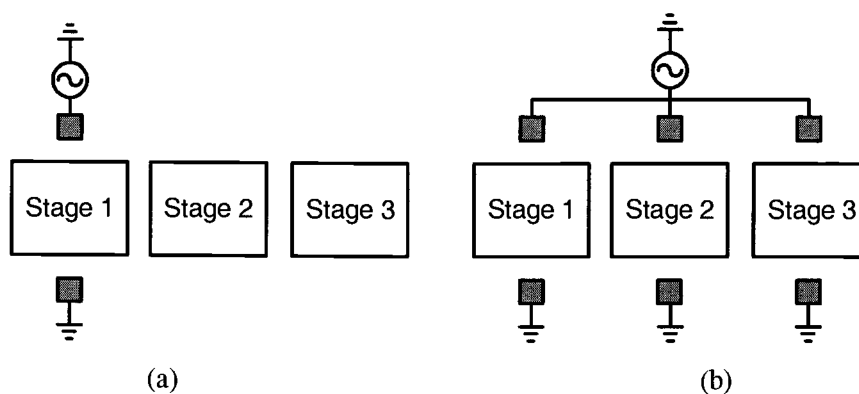


Figure 4.13 Substrate noise is injected (a) asymmetrically and (b) symmetrically.

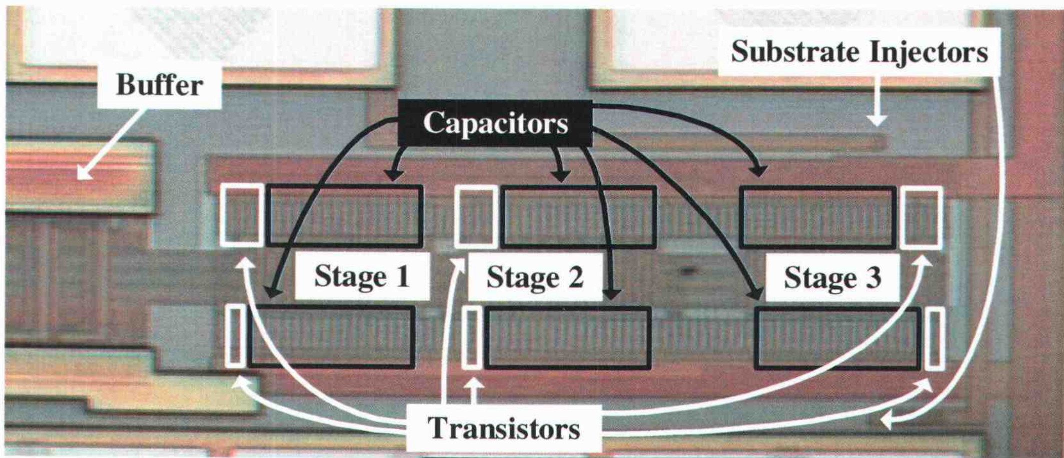


Figure 4.14 Layout of the single-ended asymmetric substrate noise injection circuit.

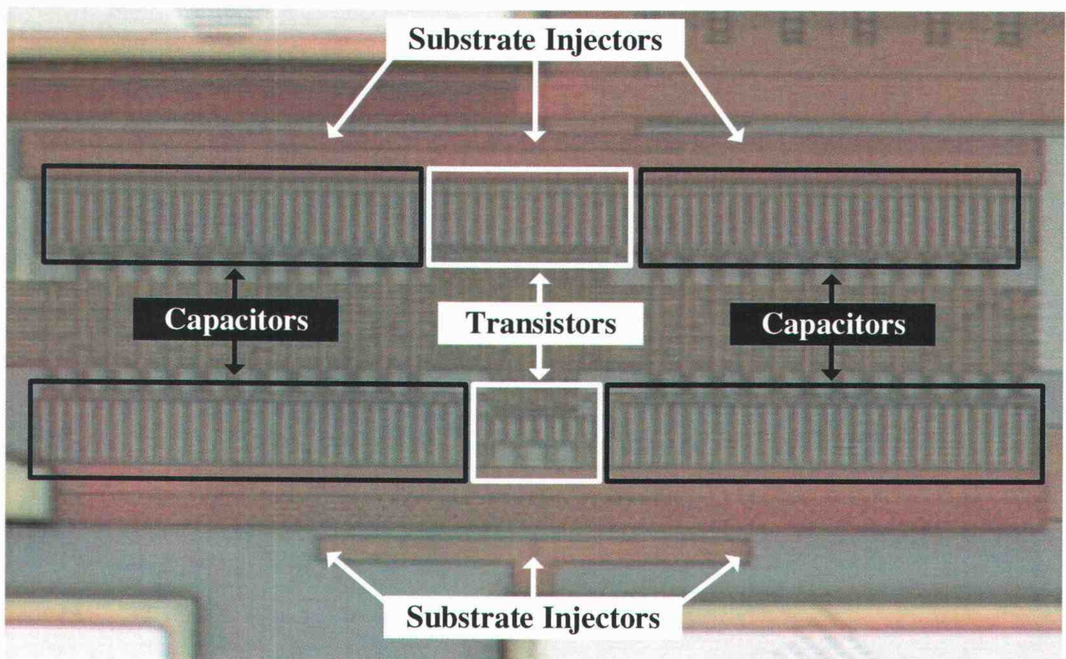


Figure 4.15 Layout of the single-ended symmetric substrate noise injection circuit.

4.3. Output Buffer Design

In system-on-a-chip applications, an oscillator is often directly coupled to the load. In the test chip environment, however, a buffer is needed to isolate the oscillator core from the RF probes and the test equipment. Without a buffer, the RF probes would add a capacitive load to the oscillator and would allow extraneous signals to couple directly into the oscillator. A successful buffer design is one that provides minimal loading on the oscillator core and is capable of driving a strong output signal even at minimal supply voltages and high input frequencies. In the case of the differential oscillators, it is desirable to have the differential-to-single ended conversion performed in the buffer.

In this work there is a wide range of oscillator applications and specifications. Some oscillators have purposely been designed to oscillate at less than 150MHz, while others have a maximum oscillation frequency in excess of 400MHz. When measuring phase noise, it is important that the output of the buffer be within the range of the measurement equipment. For the measurement equipment used in this work, the signal strength must be between -15dBm and 5dBm, referred to 50Ω. That is, over supply voltage and frequency variations, the buffers designed for the measurement of phase noise must drive a 50Ω load between 40mV and 400mV. In the case of jitter, the measurement equipment is limited to signals with a magnitude less than 1.1V. When measuring jitter it is important that the signals are strong in amplitude and have extremely fast rising and falling edges; all extraneous noise occurring near rising and falling edges will degrade the quality of the measurements. By increasing the speed of the transition, noise has less opportunity to interfere with the signal. In phase noise measurements, signal strength and edge rate are less important since the instrument is only sensitive to noise in specific frequency bands.

Buffering the single-ended oscillators is relatively straightforward. Two series-connected inverters, sized progressively larger, were used as shown in Figure 4.16. Buffers can only add white noise [32] to the oscillator's spectrum and, provided the buffer is sized appropriately, the contribution is assumed to be small. Figure 4.18 shows SpectreRF phase noise simulations on the single-ended circuit shown in Figure 2.35; the same circuit with the addition of the buffer is shown in Figure 4.16. The simulation shows a phase noise increase of 0.2dB with the addition of the buffer. To ensure all stages were loaded identically, dummy buffers mimicking the loading of the real buffer were used as shown in Figure 4.20.

Buffering the differential circuits is slightly more challenging. The circuit chosen provides a differential to single-ended conversion as desired and is shown in Figure 4.17. The design is challenging since under certain biasing conditions, some of the differential oscillators have a very high common-mode level, in excess of 2.4V, and a very small voltage swing. Usually under these conditions the oscillator's highest frequency of oscillation is reached. In some cases, the buffer design must be capable of driving the output to an acceptable level under a high common-mode input, small voltage swing and input frequencies in excess of 400MHz. To accommodate the requirements for all the differential oscillators, two implementations of the circuit were used. Figure 4.17 shows the implementation for the low speed differential oscillators designed for jitter applications, while Figure 4.19 shows the implementation used for the high speed circuits. SpectreRF must be used cautiously when simulating buffers. Figure 4.18(b) shows phase noise simulations done in SpectreRF using the circuit in Figure 4.5 with and without the buffer shown in Figure 4.19. SpectreRF shows a lower phase noise by using the buffer, which is an unexpected result.

To obtain fast edge rates, the buffers were chosen to have sizable output driver stages to source and sink large currents. This large power dissipation, however, requires large currents in the on-chip power distribution network and can cause significant inductive ringing and IR drops. To mitigate these drawbacks, the buffers were placed on a power net independent of the oscillator circuits. This also allows supply noise to be independently placed in the oscillator and in the buffer.

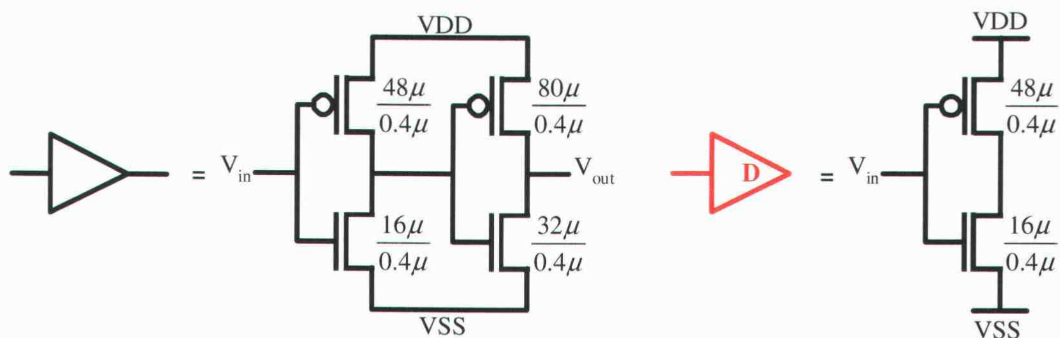


Figure 4.16 Buffer circuit for single-ended oscillators.

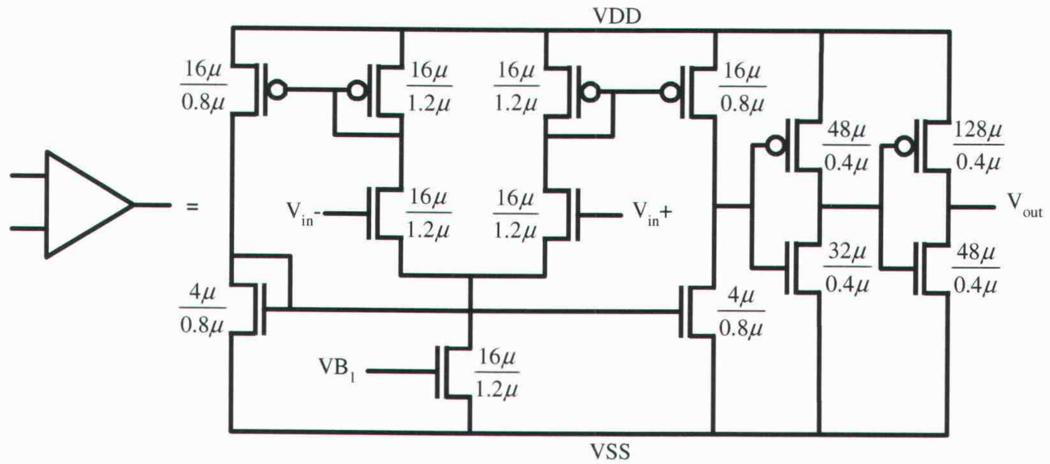


Figure 4.17 Buffer circuit for low speed differential circuits.

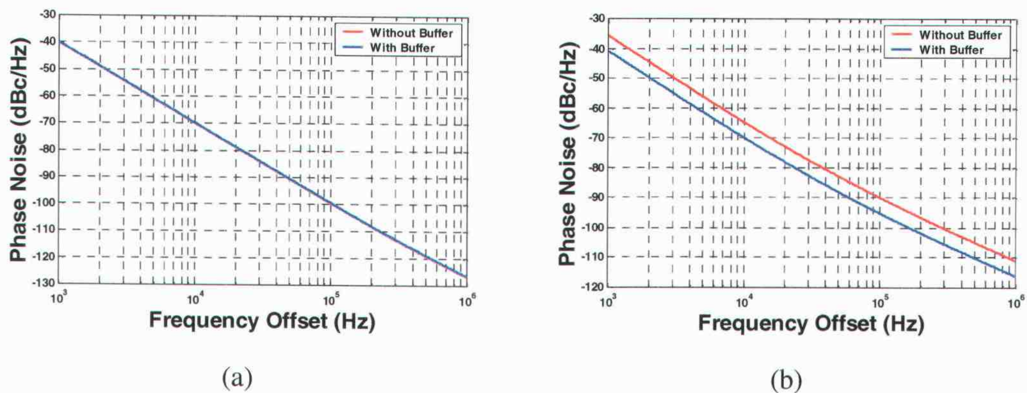


Figure 4.18 SpectreRF simulations show that (a) the buffer in Figure 4.16 increases phase noise by 0.2dB and (b) the buffer in Figure 4.19 reduces phase noise by 5dB.

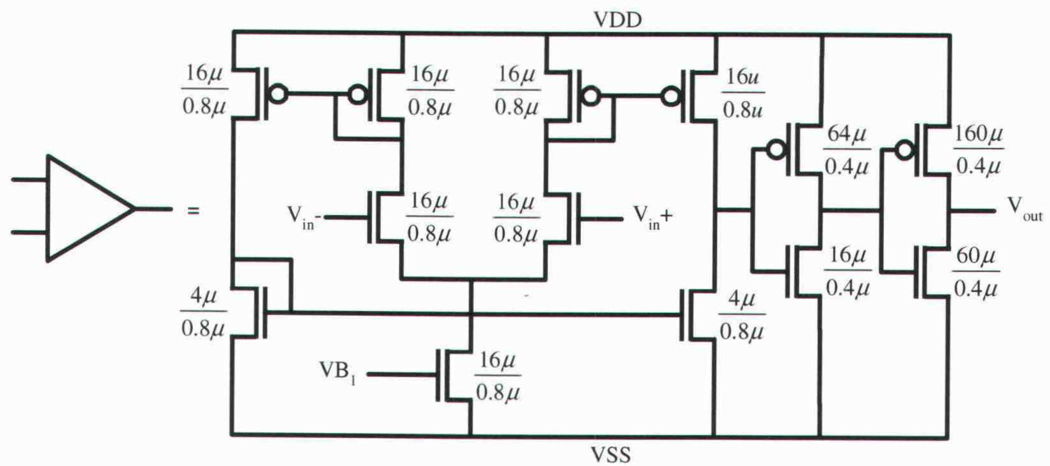


Figure 4.19 Buffer circuit for high speed differential oscillators.

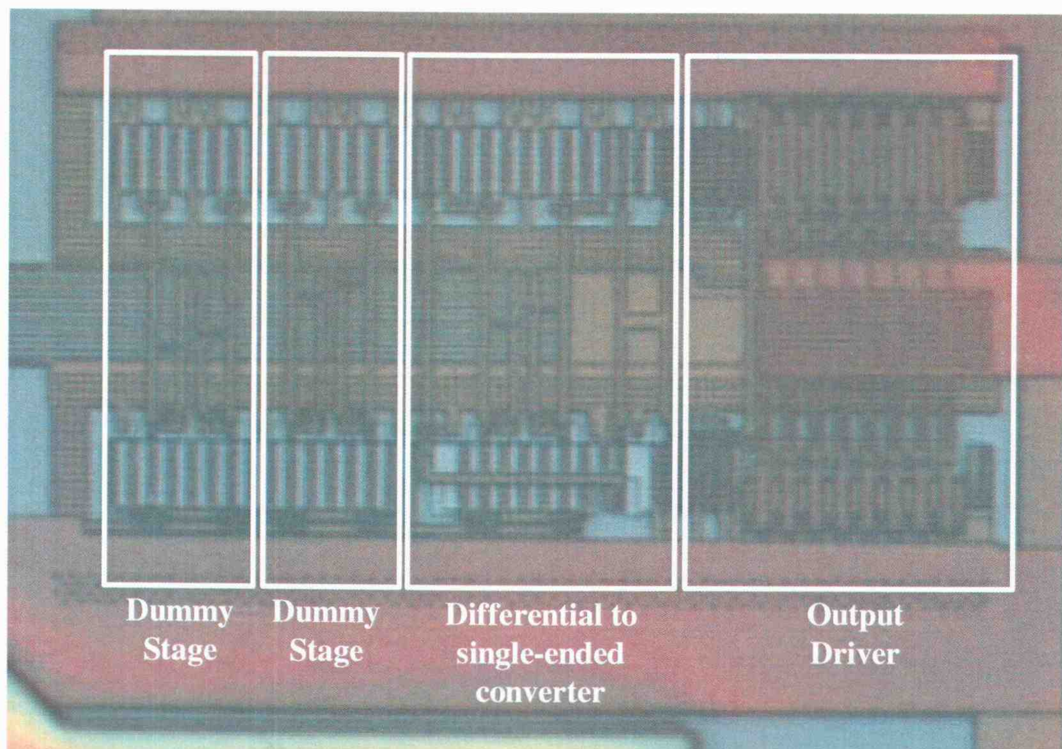


Figure 4.20 Die photo of the buffer for low speed differential circuit applications.

4.4. 1998 Test Chip

In 1998 a test chip with a 5-stage simple ring oscillator circuit shown in Figure 4.22 and a 9-stage, single-ended ring oscillator circuit shown in Figure 4.23 were designed in the TSMC 0.35μm CMOS process and fabricated through MOSIS. In the 9-stage architecture, the PMOS transistor is biased as a current source and a diode-connected transistor limits the output voltage swing. The PMOS device is biased with the voltage-to-current converter shown in Figure 4.23(c). Because the PMOS device acts to limit the current, this is referred to as a current-starved architecture. The 5-stage oscillator is similar to the H&L series oscillators.

The 9-stage current-starved oscillator is included in this work because the number of stages, the biasing and the diode-clamped output make it an architecture unique from the other oscillators presented and thus useful for comparing phase noise simulators. The 5-stage design will be used to help determine the flicker noise parameters of the 1998 process.

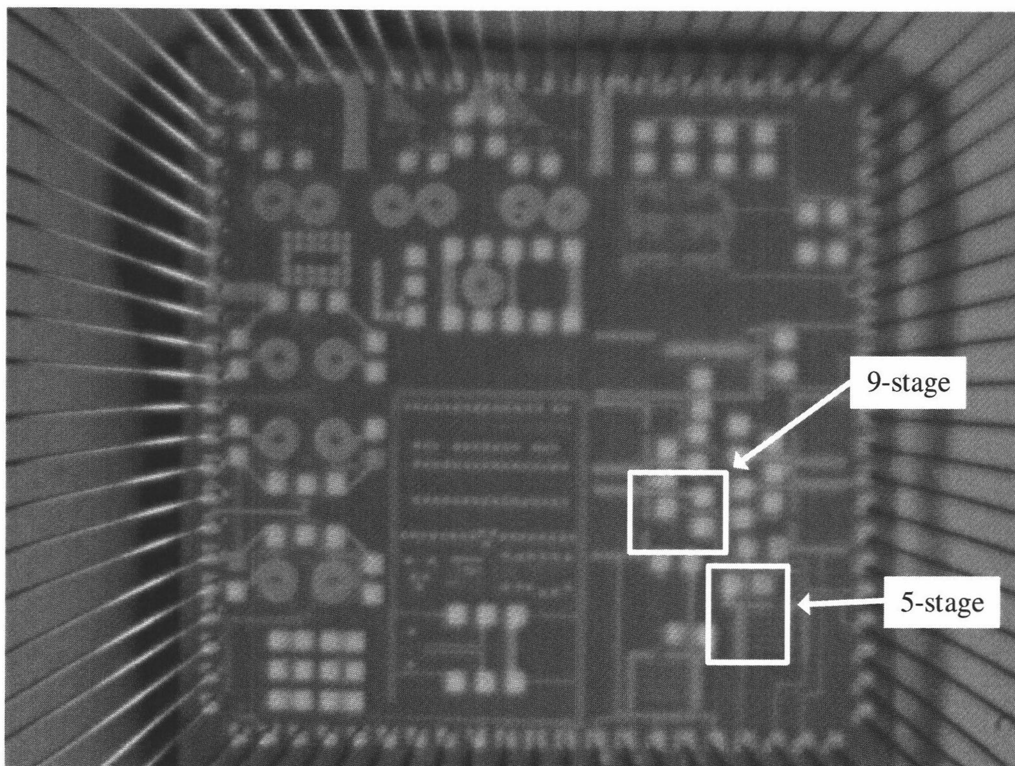
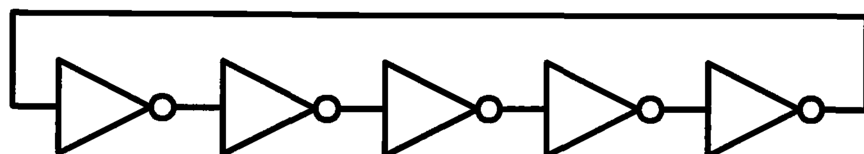
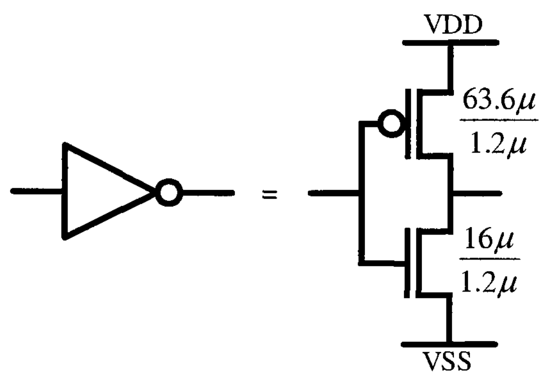


Figure 4.21 Die photo of the chip designed in 1998.

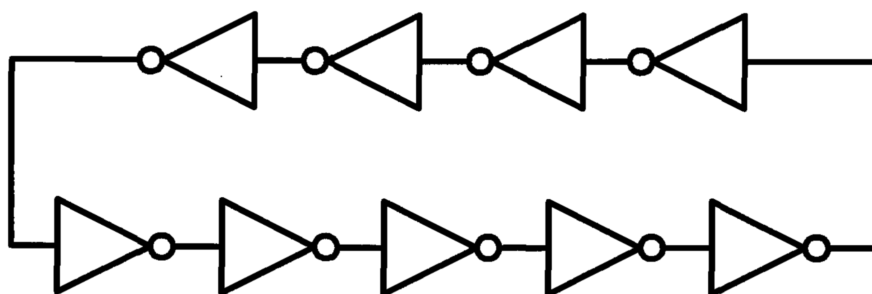


(a)

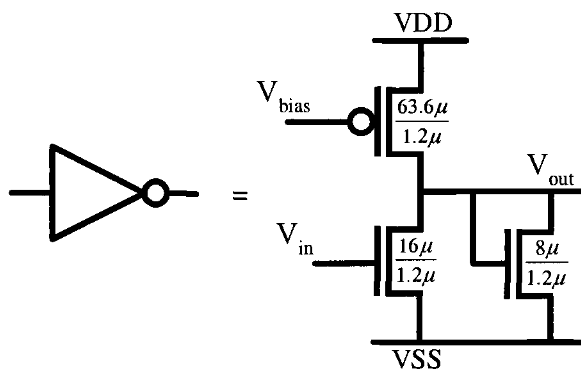


(b)

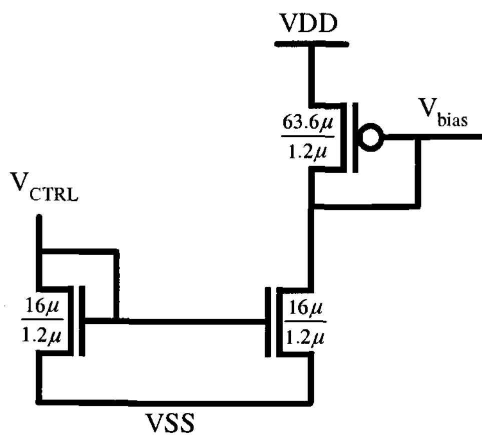
Figure 4.22 (a) A 5-stage ring oscillator, and (b) simple delay cell.



(a)



(b)



(c)

Figure 4.23 (a) A 9-stage ring oscillator, (b) current-starved delay cell and (c) voltage-to-current converter biasing circuit.

5. TEST CHIP MEASUREMENTS

The test chip described in Chapter 4 was fabricated in the TSMC 0.35μm, 4-metal layer CMOS process. A die photo of the entire chip is shown in Figure 5.1. After fabrication, the chip was placed in a DIP40 package. A laboratory at Texas Instruments was used to measure each of the 16 oscillators for phase noise or jitter performance. All measurements were done inside a double-walled screen room to shield against outside electromagnetic interference, and the oscillators were completely powered and biased with battery power. A double-walled screen room is a completely enclosed metal shell inside and electrically isolated from another metal shell. Although a single enclosed metal shell is capable of blocking electric fields, two isolated shells are required to block magnetic fields.

The chip was downbonded, which provides an electrical connection between the silicon backplane of the chip and a pin. During all measurements the pin was grounded. The grounding of the backplane does not affect the operation of the oscillators but significantly influences the network between the substrate injectors and oscillator bulks [37].

5.1. Battery Box

To ensure a clean source of power, free of tones and excess white and flicker noise, large batteries such as gel cell lead acid batteries should be used. While it is possible to use smaller, alkaline batteries, they can have high output impedance and small changes in the drawn current can have substantial changes in the exact supply voltage. If an oscillator has a K_{VCO} from the supply node to the frequency of oscillation of 100MHz/V, a 100μV change in the supply will shift the oscillation frequency 10kHz. In addition it may take some time for the oscillator to settle to a steady state, which may be delayed or impossible to obtain with a high impedance supply. To ensure a steady supply, two 17-AH, 12-volt lead acid batteries were used to power all oscillators, buffer circuits, and biasing through six independent channels. Due to the range of voltages and currents needed, an adjustable voltage source was required for each channel. The circuit used was a simple resistor-divider, with a 3-watt, 10-turn metal wound potentiometer providing the adjustability. To remove any contact noise and filter any

voltage variations, 100,000μF of capacitance was used to smooth the output voltage. To shield from outside noise, the entire power supply was housed in a sealed metal box. In situations where sinusoidal noise was coupled into one supply line, one battery was used to power one channel and the other battery powered the other five channels.

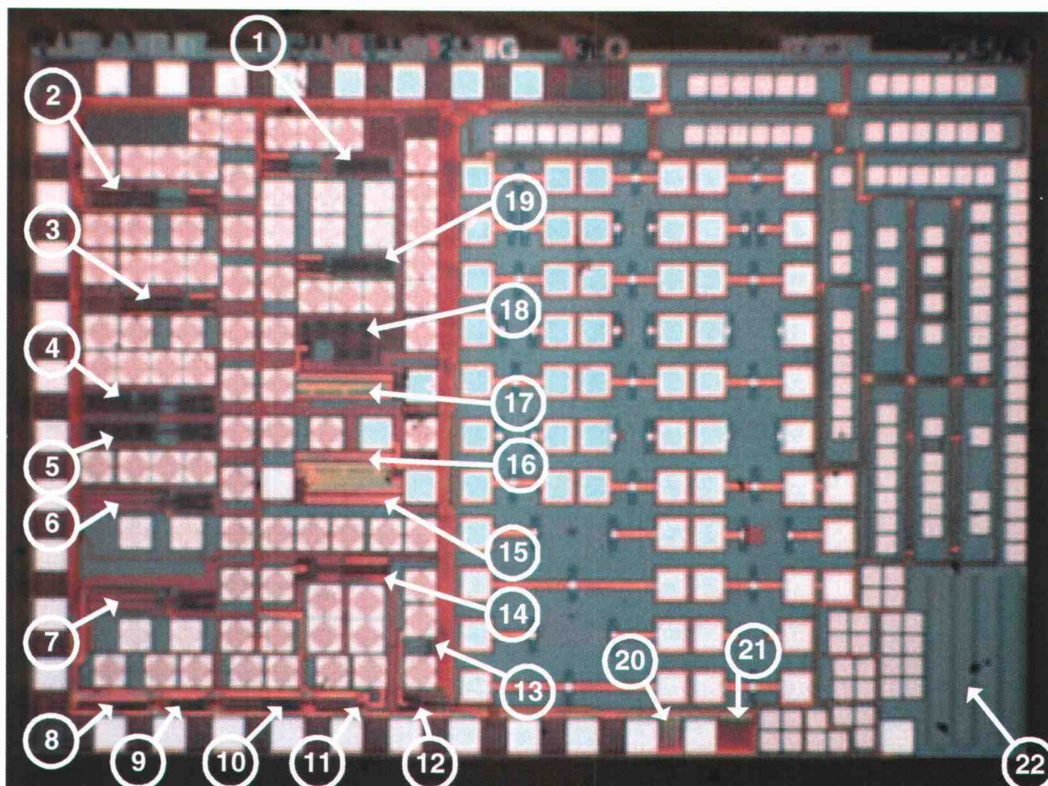


Figure 5.1 Die photo of the entire chip. The circled numbers refer to specific structures and are described in Table 5.1.

Location	Description	Location	Description
1	Single-ended symmetric substrate injection circuit.	12	Differential buffer circuit.
2	Single-ended asymmetric supply noise injection circuit.	13	Differential current biasing circuit.
3	Single-ended symmetric supply noise injection circuit.	14	PMOS pre-drive differential oscillator circuit.
4	Differential asymmetric supply noise injection circuit.	15	Cross-coupled load differential oscillator circuit.
5	Differential symmetric supply noise injection circuit.	16	Vanilla differential oscillator circuit.
6	Differential asymmetric substrate noise injection circuit.	17	Maneatis load differential oscillator circuit.
7	Differential symmetric substrate noise injection circuit.	18	Single-ended distributed layout oscillator.
8	H&L1 series oscillator.	19	Single-ended asymmetric substrate injection circuit.
9	H&L2 series oscillator.	20	912µ /1.2µ NMOS transistor.
10	H&L3 series oscillator.	21	912µ /0.4µ NMOS transistor.
11	Single-ended buffer circuit.	22	SRP structures.

Table 5.1 Description of each oscillator-related structure on the test chip. The location number refers to the die photo in Figure 5.1.

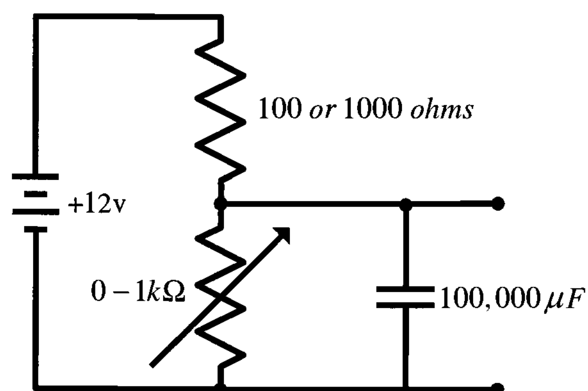


Figure 5.2 Schematic of battery power source.

5.2. Layout Considerations

A popular biasing scheme for differential oscillators is shown in Figure 5.3. In this biasing method, a single current is used to change frequencies. The primary design variable in this circuit is the width of the PMOS transistor. Figure 5.4(a) shows simulated oscillation frequency contours and Figure 5.4(b) shows the simulated waveform amplitude contours for a range of bias currents and a sweep of the PMOS transistor's width. These results are for the high-speed Maneatis load differential oscillator. It can be seen from the simulations that a PMOS width of 35μm gives the best oscillation amplitude for a given current. Additionally, choosing a transistor width where the derivative of the oscillation frequency with respect to the transistor size is zero, i.e. where the frequency contour is flat, could yield a circuit immune to noise added by the biasing circuit.

Although adding this biasing scheme gave an additional feature to test, in cases where it was desired to force the PMOS and NMOS bias lines to specific voltages, it can be seen that the buffer VDD and the PMOS bias lines are no longer isolated but instead have a diode connecting them. It is necessary then to physically sever the wires leading to the PMOS transistor.

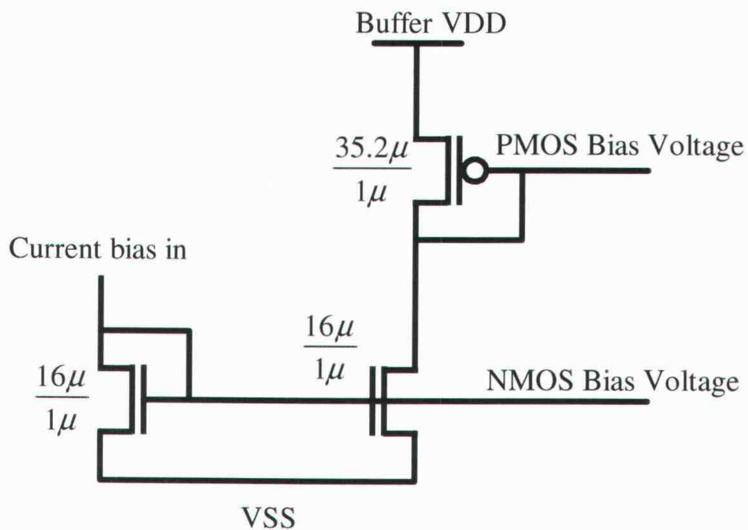


Figure 5.3 A biasing scheme that allows a single current to control the oscillation frequency.

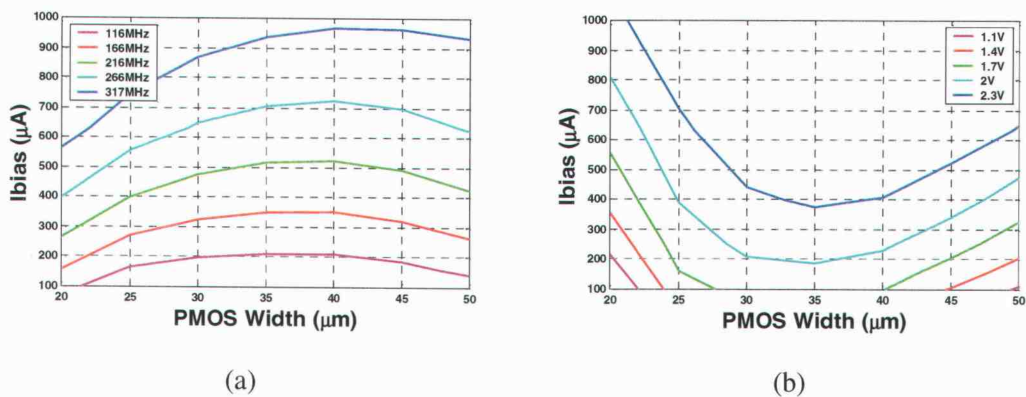


Figure 5.4 (a) Frequency tuning and (b) oscillation amplitude are controlled by the width of the PMOS transistor in Figure 5.3.

A laser was used to cut the wires connecting the PMOS transistor. Figure 5.5 shows a picture of the biasing circuit and cuts made to the buffer VDD wire and the PMOS bias wire. The picture shows several detractions to using a laser. The cuts are not clean, it is difficult to determine if a cut has been made, and the laser causes heat damage to areas around the cut. Wide metal lines are particularly difficult to cut as the metal quickly draws the heat away. In Figure 5.5 the narrowest metal lines are 0.8μm in width.

A better cutting method is to use a focused ion beam (FIB) machine. In a FIB machine, a gas is sprayed over the surface of the die and a beam of ions is shot into the area where a cut is desired. The ions react with the gas to remove metal or oxide. The FIB also has the ability to grow metal lines, although the metal grown is more resistive than the native metal. A cut made by a FIB machine is shown in Figure 5.6. The cut shown is about 1μm wide and about 14μm long and is extremely clean.

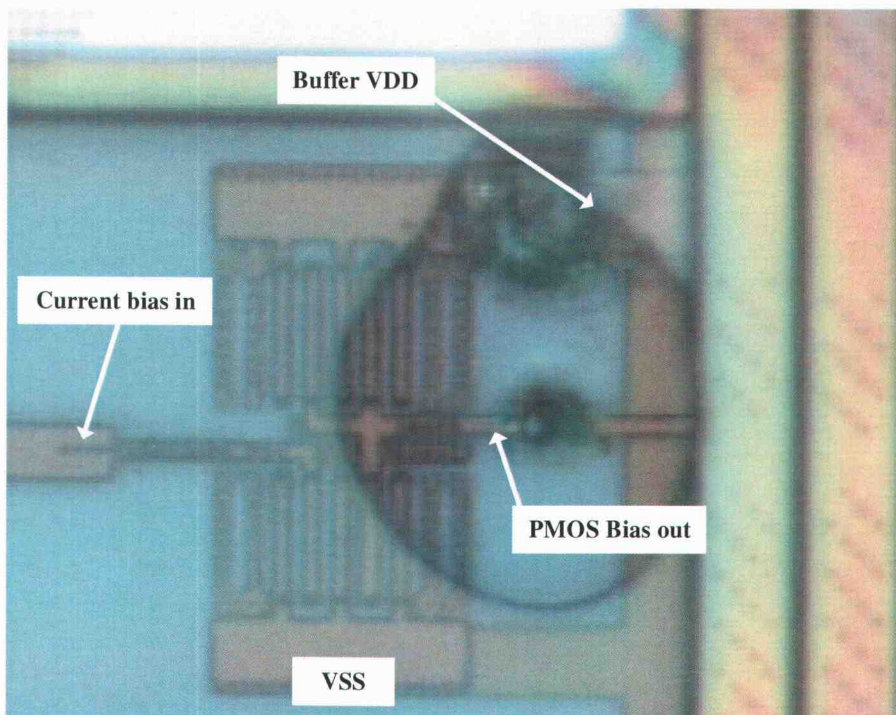


Figure 5.5 Die photo of the biasing circuit in Figure 5.3 after laser cuts.

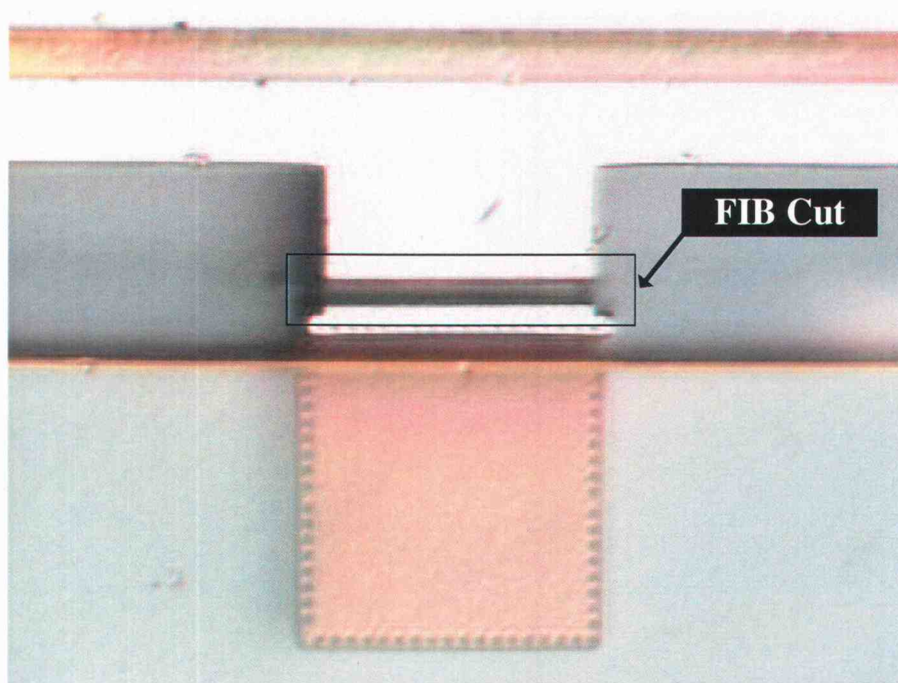


Figure 5.6 Die photo of a 1μm by 14μm FIB cut.

5.3. Measuring Phase Noise

The measurement of phase noise is generally done with one of three methods [33], [34]. The first method is a simple one. The oscillator's noise sidebands can be measured with a spectrum analyzer. Although this method is valid if the spectrum analyzer has better phase noise performance than the device under test (DUT), the approach is limited by the stability of the oscillator. Flicker noise, thermal air currents or other thermal variations cause free running oscillators to slowly vary in frequency. The time constants of the variations are on the order of seconds and the oscillation frequency generally stays close to some mean. For accurate results, the resolution bandwidth (RBW) and video resolution bandwidth (VRBW) of the spectrum analyzer must be set very low which, coupled with a large frequency span, may require 10-30 seconds for the spectrum analyzer to complete a frequency sweep. If the oscillation frequency changes appreciably, the measured noise sideband will be distorted. The distortion is more severe at lower offset frequencies. This method is not suited to applications

where the boundary between the oscillator's $1/f^3$ and $1/f^2$ phase noise regions, ω_{1/f^3}, must be measured.

Another measurement technique is to lock the oscillator to a reference oscillator using a narrow band PLL. The signal from the phase detector, $\theta(t)$, can be analyzed with a baseband spectrum analyzer. High-performance baseband spectrum analyzers have lower noise floors and sharper frequency resolution than their RF counterparts, and the difficulty of a moving center frequency is largely eliminated with the proper selection of the PLL's bandwidth. This method, however, requires a very expensive signal source and a complicated test setup. If the reference oscillator is not properly isolated from the oscillator under test, one source can injection lock to the other. Because the useful phase noise spectrum starts at about 10 times the PLL's bandwidth, this method is also typically not suitable for finding ω_{1/f^3}.

The third method uses an FM discriminator and compares the signal to itself delayed in time. This method also uses a baseband spectrum analyzer but does not require a second signal source or a complicated test setup. Because the delay is created with coaxial cables which have significant loss above 1GHz, this method can only be used to measure oscillators up to 1GHz in frequency. In addition, the delay τ sets the maximum offset frequency from the carrier which, with this method, is typically 1MHz. Measurement equipment using this technique is manufactured by RDL. All phase noise measurement results in this thesis were performed with an RDL NTS-1000A or an RDL NTS-1000B. The differences between the 1000A and 1000B (1000x) are not performance related and both have a claimed accuracy of ±2dB over an offset frequency range of 10Hz – 1MHz. The required input power range is between -20dBm and +5dBm; however, noise in the measurement noticeably increases for power levels less than -10dBm. The NTS-1000x's internal spectrum analyzer uses several resolution bandwidths. The data out of the analyzer is normalized to 1Hz. If the noise spectrum contains spurs narrower than the resolution bandwidth, then the spurs are normalized along with the noise. Since narrow-band spurs should not be normalized, the measured spur amplitude is not representative of the true spur amplitude.

5.4. Phase Noise Measurement Setup & Equipment

The measurement of phase noise due to only device noise was simple and straightforward. The oscillators were powered by the battery box and were coupled directly into a NTS-1000x. DC power and biasing was delivered from the battery box's BNC connectors to the test board's SMA connectors via coaxial cables. Short wires with decoupling capacitors were used to connect from the SMA connectors to the chip's pins. Using twisted pair wires instead of coax was also tried but a significant pickup of noise was noticed. Signals from the oscillators were probed with 50Ω, GSG RF probes. The measurement environment was a CASCADE probe station inside a screen room. Inside the screen room another probe station, a computer and various measurement equipment was used periodically while the phase noise measurements were in progress, which occasionally caused tones in the phase noise spectrums.

In the cases where sinusoidal noise was injected into the supply and substrate, minor changes to the test setup were made. When injecting into the oscillator or buffer supply, a 500μF capacitor was used to capacitive-couple the HP 8664A signal generator into one battery channel. That channel's filter capacitor was reduced from 100,000μF to 10,000μF. In the cases where noise was injected into the substrate, the HP 8664A was directly coupled to the substrate with RF probes. The magnitude of the injected signals was monitored with an HP 8563EC spectrum analyzer.

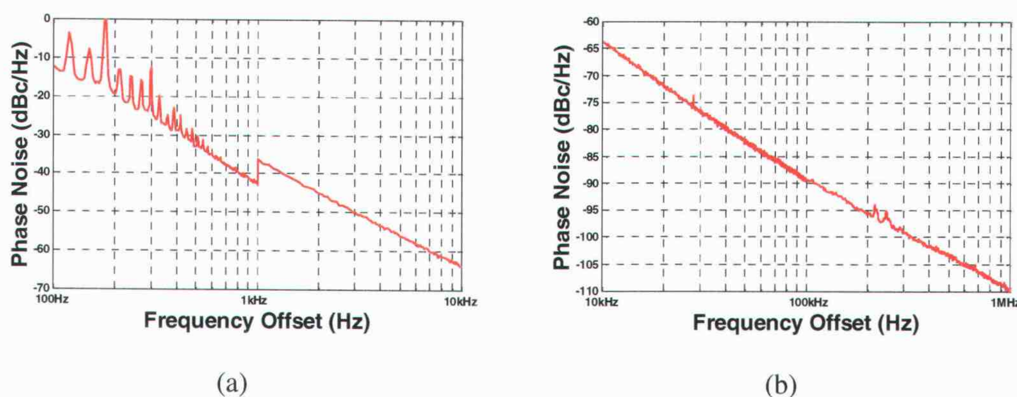
5.5. Phase Noise Measurement and Simulation Results

The phase noise of 10 oscillators from 5 different architectures has been measured over a range of bias and supply voltages. In this section they are compared to simulations from SpectreRF and *isf_tool* using both the direct and indirect methods of calculating cyclostationary noise. Although the NTS-1000x generally gives clean measurements, there are two measurement defects in the instrument. The first is that a small amount of random noise is superimposed onto every measurement, generally making the envelope of the measurement about 2dB. This is from FFT artifacts, noise in the NTS-1000x, and measurement error. The second defect is that the NTS-1000x uses different filters for each decade of frequency offset in the measurement and discontinuities can appear between decades. Flagrant discontinuities often appear at 1kHz which is a known defect of the NTS-

1000x. An example is shown in Figure 5.7(a). Data at less than 1KHz offsets should be discarded in these cases. More subtle discontinuities such as that at 100kHz, shown in Figure 5.7(b), are the typical case.

Although seemingly minor, the random noise and small discontinuities are very disruptive to accurate determination of the flicker noise corner of an oscillator. To smooth the results, all phase noise measurements shown in this work except those taken in 1999 are a composite of the mean and median of between 6 and 128 individual phase noise measurements. Figure 5.8(a) shows a single phase noise measurement and Figure 5.8(b) shows the composite of 20 measurements. In all, the measurement results presented in this work are based on over 2500 phase noise measurements.

As discussed in Chapter 2, phase noise is dependent on thermal and flicker noise sources, and the transfer function between these noise sources and phase noise. Both simulators have intricate means of determining the transfer function, but are dependent on the selection of the thermal and flicker noise models presented in Chapter 1. Although the choice of thermal noise model affects the calculation of cyclostationary noise in the H&L method, in SpectreRF there is little difference in results between the two methods. The correct selection of flicker noise model, however, is a difficult issue. Although the BSIM3v3 model in (1.7) is potentially very accurate because it involves three fitting parameters for each MOSFET region of operation, the fitting parameters for this process are unknown. The two remaining models in (1.5) and (1.6) also have unknown fitting parameters. Companies who require accurate



(a) (b)

Figure 5.7 Filter switching in the NTS-1000x can result in discontinuities between decades. (a) A large discontinuity at 1kHz. (b) A small discontinuity at 100kHz.

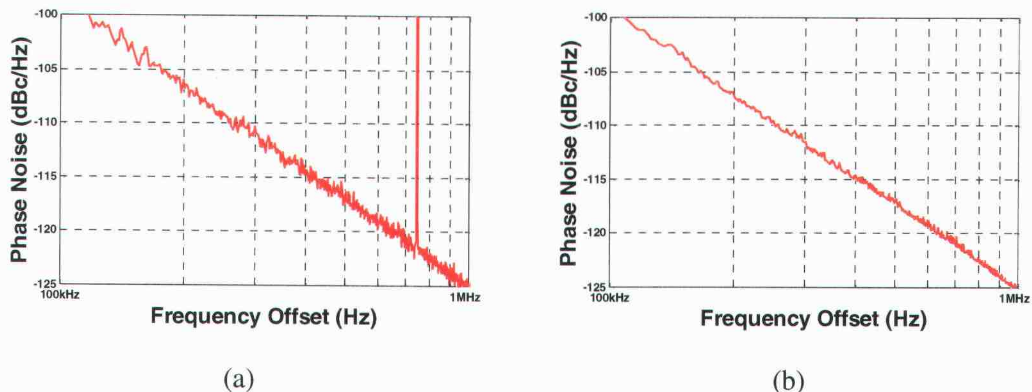
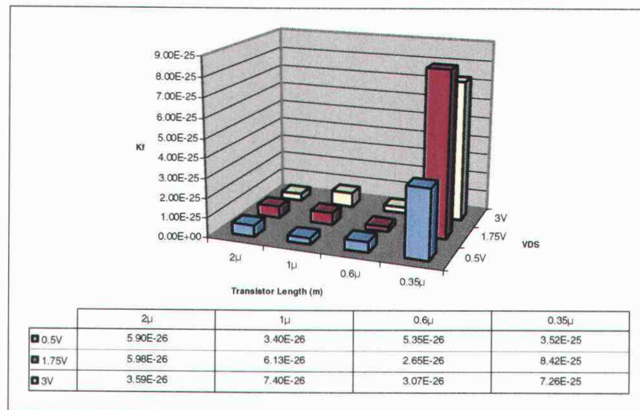


Figure 5.8 (a) Measurements from the NTS-1000x have about 2dB of random noise. (b) By averaging multiple measurements the noise is reduced.

noise measurements generally use very specialized, expensive test equipment to determine the parameters. A simpler method for determining the parameters is to use a spectrum analyzer to measure the noise current, as shown in Figure 5.10 [35]. From the measurements the various fitting parameters can be extracted. This method is relatively simple to implement but has several difficulties to overcome. The amplified noise of the device must be greater than the input noise of the amplifier, the device noise must be greater than the input referred noise of the amplifier, and the channel impedance of the device under test (DUT) must be much less than the input impedance of the LNA. This means only special devices with very large width-to-length ratios can be measured. TSMC flicker noise data published on August 5, 1998 and shown in Figure 5.9 indicate that the fitting parameters are heavily dependent on physical size, so using devices that are significantly different in size than those in the oscillator circuits is futile. The model in (1.6) is associated with the data in Figure 5.9.

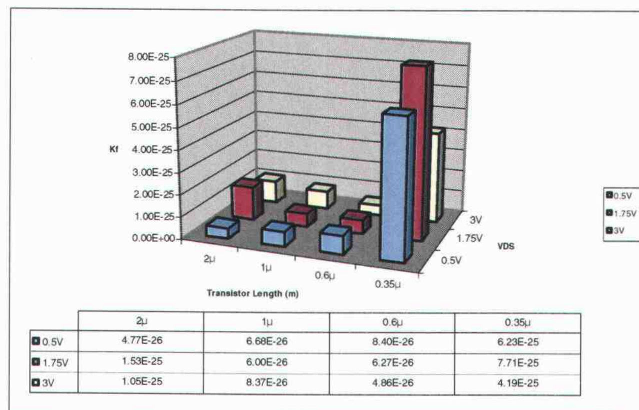
5.5.1. *Determining the flicker noise model*

Because the direct measurement of flicker noise was not possible, an alternate method of determining the correct flicker noise model was devised. To determine the best flicker noise model for test chip #2, simulations using the three H&L series oscillators described in Section 4.1.1 were compared to the measurements. The model and values for the empirical constants that best fit these measurements was chosen as the flicker noise model in this work. For all



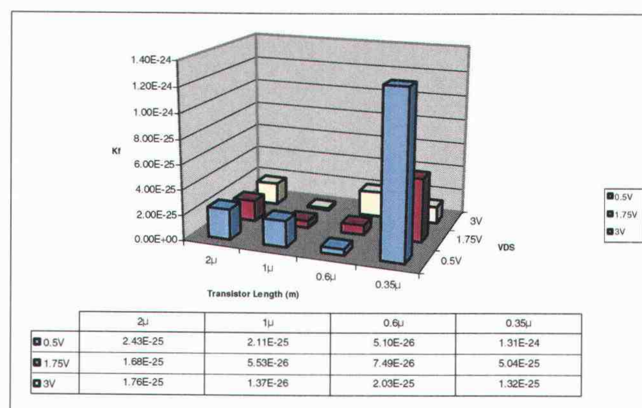
	2µ	1µ	0.6µ	0.35µ
0.5V	5.90E-26	3.40E-26	5.35E-26	3.52E-25
1.75V	5.98E-26	6.13E-26	2.65E-26	8.42E-25
3V	3.59E-26	7.40E-26	3.07E-26	7.26E-25

(a)



	2µ	1µ	0.6µ	0.35µ
0.5V	4.77E-26	6.68E-26	8.40E-26	6.23E-25
1.75V	1.53E-25	6.00E-26	6.27E-26	7.71E-25
3V	1.05E-25	8.37E-26	4.86E-26	4.19E-25

(b)



	2µ	1µ	0.6µ	0.35µ
0.5V	2.43E-25	2.11E-25	5.10E-26	1.31E-24
1.75V	1.68E-25	5.53E-26	7.49E-26	5.04E-25
3V	1.76E-25	1.37E-26	2.03E-25	1.32E-25

(c)

Figure 5.9 TSMC measured K_f values for NMOS transistor sizes of 20µ/2µ, 20µ/1µ 20µ/0.6µ and 20µ/0.35µ with (a) V_{gs} of 0.7V, (b) V_{gs} of 0.95V and (c) V_{gs} of 1.2V.

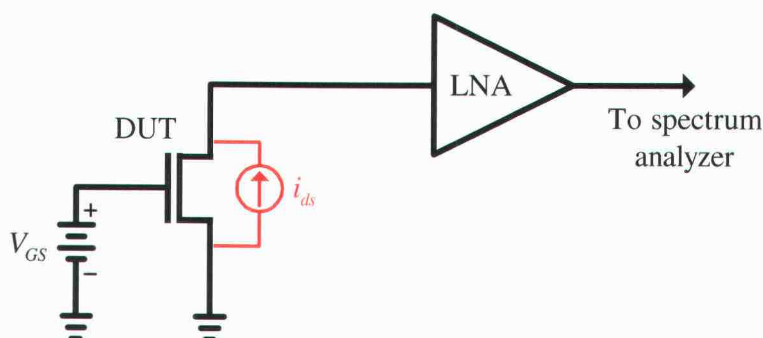


Figure 5.10 MOSFET noise can be measured with an LNA and a spectrum analyzer.

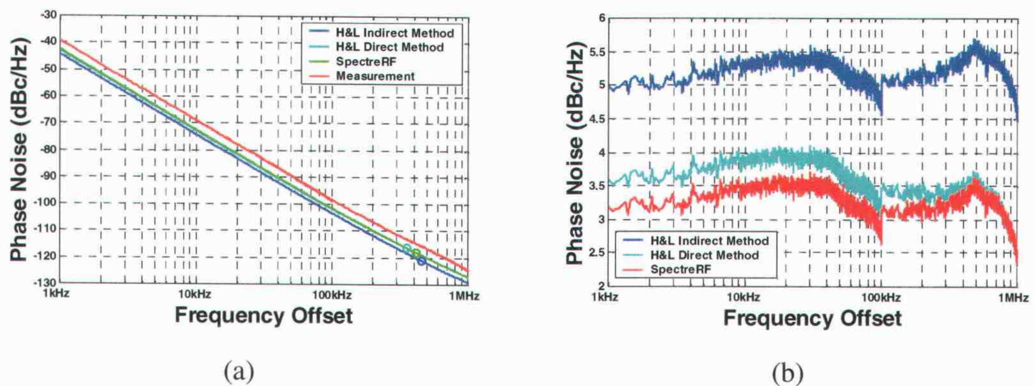
comparisons the parameters *af* and *ef* were chosen to be 1, although TSMC-measured data suggest it could be 0.8 in the NMOS case and 0.7 in the PMOS case. The data, however, is three years old and the process has undergone changes since then, so the data is considered unreliable. Each oscillator was powered with supply voltages of 2.0V, 2.5V, 3.0V and 3.5V, for a total of 12 measurements. A similar procedure was used to determine the best model and K_f values for the first test chip.

The flicker noise model which best fits both test chips was (1.5). The best fit values of K_f for each simulation method and test chip are shown in Table 5.2. This model and the K_f values appear to be a unique solution; the model of (1.6) could not be made to fit measured phase noise trends of either test chip, and no other values for K_f matched the 12 measurements as accurately. Figure 5.11(a), Figure 5.12(a) and Figure 5.13(a) show the simulations versus the measurements for each H&L series oscillator and the simulation methods chosen. Figure 5.11(b), Figure 5.12(b) and Figure 5.13(b) compare the error between the simulation methods chosen and the measurements for each oscillator. Although there are offsets between the measurements and simulations that indicate the amount of noise in the system has been underestimated, the offsets are generally flat across all frequencies. This important result shows that the correct flicker noise model is being used. The remaining 9 of the 12 comparisons are shown in Appendix D. A plot showing the results for all possible simulation methods is shown in Figure 5.15. The 1MHz figure of merit for these oscillators is plotted as contour curves versus supply voltage and transistor width in Figure 5.14. This plot shows little change in the figure of merit for supply voltage changes but some improvement as the

NMOS transistor becomes larger. The improvement is due to the flicker noise corner moving in, not because phase noise due to thermal noise became smaller.

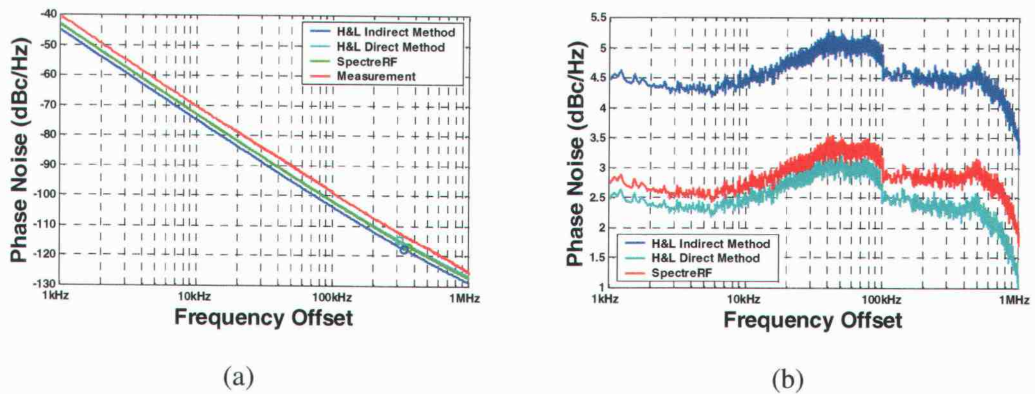
5.5.2. *Characterizing the phase noise due to the buffer*

It is commonly assumed that a buffer's contribution to phase noise is negligible. To confirm this the performance of the single-ended buffer circuit in Figure 4.16 was characterized by injecting a signal from the HP 8664A signal generator and measuring the phase noise out of the signal generator, at the input to the buffer and at the output of the buffer as shown in Figure 5.16(a). The difference between the phase noise at the output of the buffer and the input to the buffer is shown in Figure 5.16(b). Although a number of tones have coupled into the spectrum, the noise added by the buffer is generally less than 1dB. This is consistent with the simulated results in Figure 4.18(a). Because the contribution to the measurements is minor, the phase noise due to the buffer was ignored in simulations.



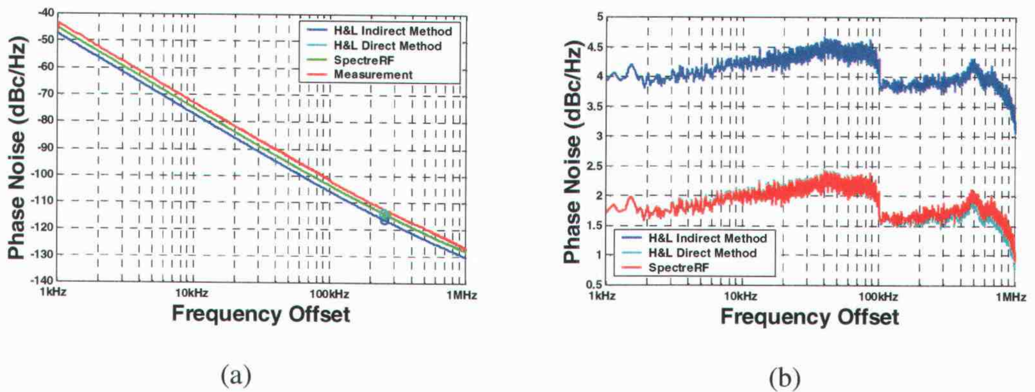
(a) (b)

Figure 5.11 (a) Phase noise performance and (b) error of the HL1 oscillator, VDD=3.0V.



(a) (b)

Figure 5.12 (a) Phase noise performance and (b) error of the HL2 oscillator, VDD=3.0V.



(a) (b)

Figure 5.13 (a) Phase noise performance and (b) error of the HL3 oscillator, VDD=3.0V.

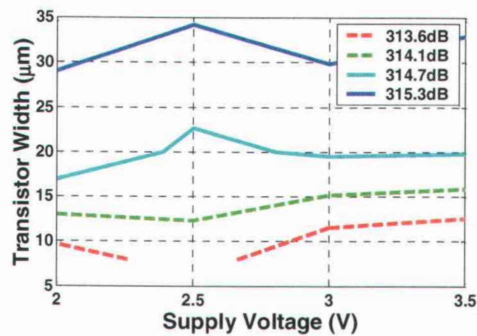


Figure 5.14 The figure of merit versus supply voltage and transistor width in the 5-stage single-ended architecture. Higher numbers show better performance.

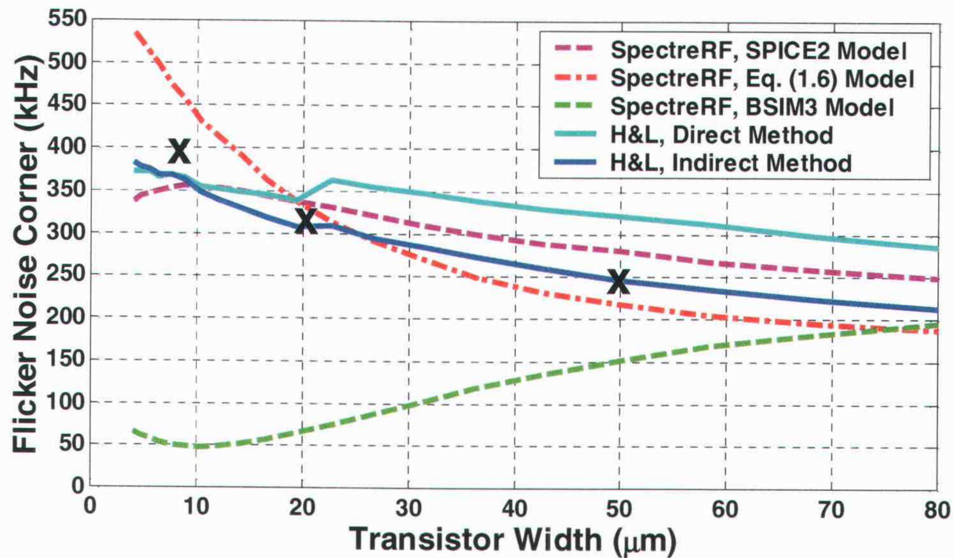
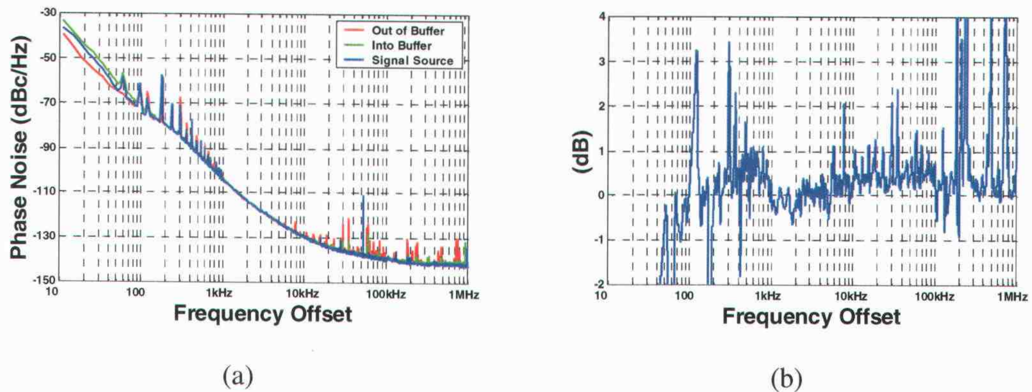


Figure 5.15 The flicker noise corners of all the possible simulation methods versus transistor width for the architecture (H&L series) of Figure 2.25. Flicker noise corner measurements performed on the three H&L series oscillators are denoted with an X. The supply voltage was 3.0V.



(a) (b)

Figure 5.16 The phase noise of (a) the signal source, input of the buffer and output of the buffer, and (b) the difference between the phase noise at the output and input of the buffer

	Chip #1 (1998)		Chip #2 (2001)	
	Kf_{NMOS}	Kf_{PMOS}	Kf_{NMOS}	Kf_{PMOS}
H&L Direct Method	6.7e-28	1.3e-28	12.0e-28	6.0e-28
H&L Indirect Method	5.0e-28	1.0e-28	9.0e-28	2.0e-28
Spectre RF	1.7e-28	0.32e-28	3.0e-28	1.0e-28

Table 5.2 Flicker noise parameters used for each simulation method and test chip.

5.5.3. *Phase noise simulation methodology*

Each simulation result is compared with simulations from SpectreRF using the SPICE2 flicker noise model, and simulations from *isf_tool* using both the direct (Spectre noise simulation) and indirect (GDS_0 extracted from a dc operating point) methods of calculating cyclostationary thermal noise. Flicker noise was calculated using the SPICE2 flicker noise model and K_f values from Table 5.2. The transistor models were those provided by MOSIS for this wafer lot. All simulations neglected the bond wire inductances in series with the supply voltages and grounds and only included parasitic capacitors from the diffusions. Lumped capacitors to ground were used to account for the wiring capacitance.

The measurements show that phase noise due to the buffers is small, and the simulated phase noise results are performed without a buffer in all cases.

For both measurements and simulations the PMOS and NMOS voltages are with respect to ground.

Circles in the phase noise plots are used to indicate the flicker noise corners of each simulation method.

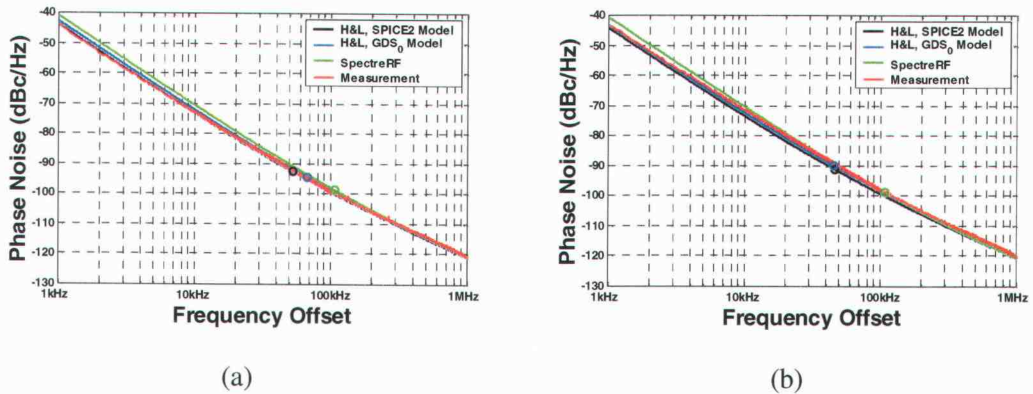
5.5.4. *Typical results for the "vanilla" differential oscillator*

The "vanilla" differential oscillator had a narrow bias range for which the circuit's oscillations were steady enough for phase noise measurements. The phase noise was measured for seven different bias points, and typical simulation and measured results are shown in Figure 5.17. The narrow range for which this circuit oscillates makes this

architecture impractical. Even in Spectre it is difficult to simulate this circuit as it tends to oscillate in its common mode, i.e., as a single-ended circuit. This problem could only be solved by mismatching the switching pair by 0.1μm. All measured results for this oscillator are shown in Appendix E. In almost all cases SpectreRF and H&L are close to the measured values with H&L showing closer agreement than SpectreRF. At two specific bias points in Appendix E, all simulation methods agree strongly but differ significantly from the measurements. Figure 5.19 shows the simulated performance of this oscillator with lines drawn showing bias trends with the least optimal performance. This is the only architecture where SpectreRF predicts higher flicker noise corners than the H&L method.

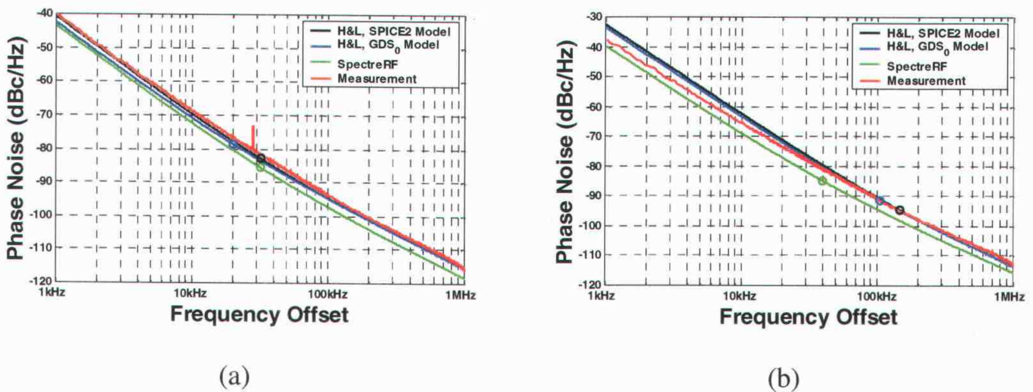
5.5.5. *Typical results for the high-speed Maneatis load differential oscillator*

This circuit oscillated for a wide range of bias, and phase noise was measured for 66 different bias points. Two representative results are shown in Figure 5.18 and complete results are included in Appendix F. In this architecture, both H&L simulation methods accurately predicted the phase noise in the -20dB/dec region, usually within 1-2dB of the measurements and always within 5dB. SpectreRF was less precise, generally underestimating phase noise by 4dB and as much as 7dB. Figure 5.21 shows the 1MHz simulated figure of merit for H&L and SpectreRF as well as the oscillation and amplitude contours. Lines are drawn showing bias trends with the least optimal performance. The figure of merit for this oscillator is approximately 12dB lower than the single-ended H&L series oscillators. This circuit's phase noise performance is inferior to the "vanilla" differential oscillator. No flicker noise corner prediction method exactly matched all measurements, although the H&L indirect method matched a significant portion. Contour plots are used in Section 5.6 to compare the flicker noise prediction results of each method with measurements.



(a) (b)

Figure 5.17 Measurements of the "vanilla" differential oscillator versus simulations for (a) V_{PMOS}=1.7V and V_{NMOS}=1.4V and (b) V_{PMOS}=1.6V and V_{NMOS}=1.5V.



(a) (b)

Figure 5.18 Measurements of the high-speed Maneatis load oscillator versus simulations for (a) V_{PMOS}=1.4V and V_{NMOS}=1.2V and (b) V_{PMOS}=2.0V and V_{NMOS}=1.5V.

5.5.6. Typical results for the low- speed Maneatis load differential oscillator

These measurements are from the circuit designed for symmetrical substrate noise injection. The architecture is the same as the high-speed Maneatis load oscillator but with half the power consumption and capacitance added to slow the frequency of oscillation. Measurements were taken for 17 bias points. Results typical of the simulations and measurements are shown in Figure 5.20 and all results are presented in Appendix G. At small bias currents and low V_{PMOS} voltages the oscillator was not stable enough to give perfect measurement results. This may be because under those conditions the common-mode level is

high and the voltage swing is low, a state the low-speed differential buffer was not designed for. This conclusion stems from the fact that under similar biasing conditions, the high-speed Maneatis oscillator was stable and its buffer was specifically designed for high common-mode and low voltage swing signals.

Ignoring the measurements from biasing conditions that lead to high common-mode and low voltage swing, both H&L simulation methods and SpectreRF show close agreement with the magnitude and flicker noise corner of nearly all measurements. Similar to the high-speed Maneatis results, H&L gives slightly better agreement in both regards.

5.5.7. *Typical results for the cross-coupled load differential oscillator*

The cross-coupled load circuit oscillated for a narrower range of biasing than the Maneatis load circuit, and measurements for 35 bias points were taken. Figure 5.22 shows representative results and all results are presented in Appendix H. Again the H&L methods are usually within 1-2dB of the measurements and never exceed 4dB. SpectreRF is usually within 3dB and never more than 5dB. Figure 5.24 shows the 1MHz simulated figure of merit for H&L and SpectreRF, and the oscillation frequency and amplitude contours. Lines are drawn showing bias trends with the least optimal performance. It can be seen that this method has a better FOM and a wider tuning range than the Maneatis load oscillator. Similar to results from the high-speed Maneatis load oscillator, no method was able to predict the flicker noise corner for all bias points, although the H&L indirect method matched a significant portion. Contour plots are used in Section 5.6 to compare the results of each method.

5.5.8. *Simulation results for the PMOS pre-drive differential oscillator*

The PMOS pre-drive oscillations were not stable enough to measure the phase noise. This circuit demonstrates a benefit of using *isf_tool* to simulate phase noise. Although SpectreRF could not get the circuit to converge during periodic steady state (PSS) analysis, the circuit converges for time domain simulations. Figure 5.26(a) shows the measured oscillation frequency versus control voltage plot, while Figure 5.26(b) shows the simulated results. The shapes are similar but simulations are much higher in frequency, particularly at high control voltages. This is not simply due to extra parasitic capacitance which would translate the entire

curve down. The simulated flicker noise corner and figure of merit as a function of control voltage are shown in Figure 5.26(c) and Figure 5.26(d), respectively.

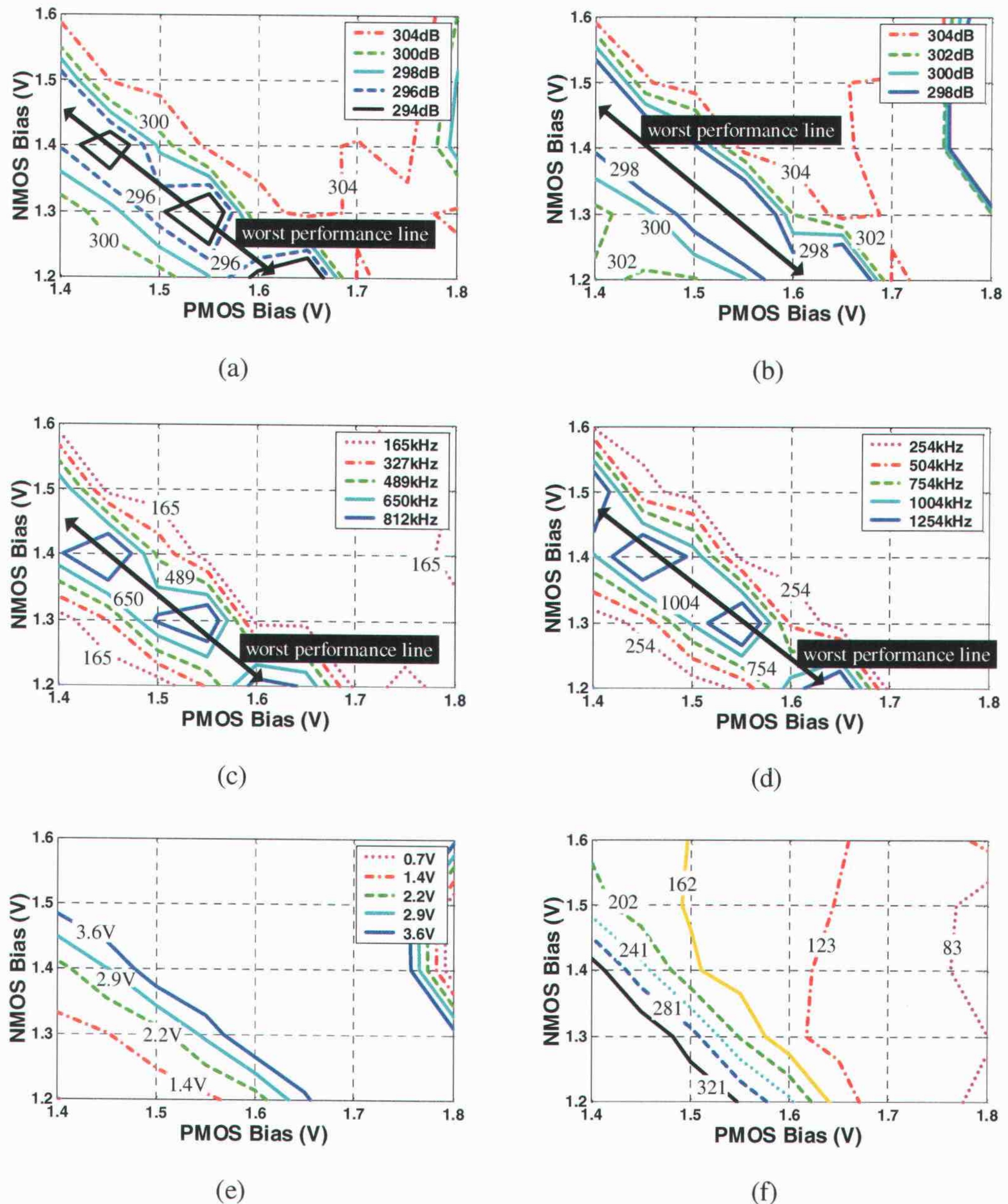


Figure 5.19 The 1MHz offset figure of merit contours predicted by (a) H&L and (b) SpectreRF, flicker noise corners predicted by (c) the H&L indirect method and (d) SpectreRF, (e) the simulated oscillation amplitude contours and (f) the simulated oscillation frequency contours (in MHz) for the "vanilla" differential oscillator.

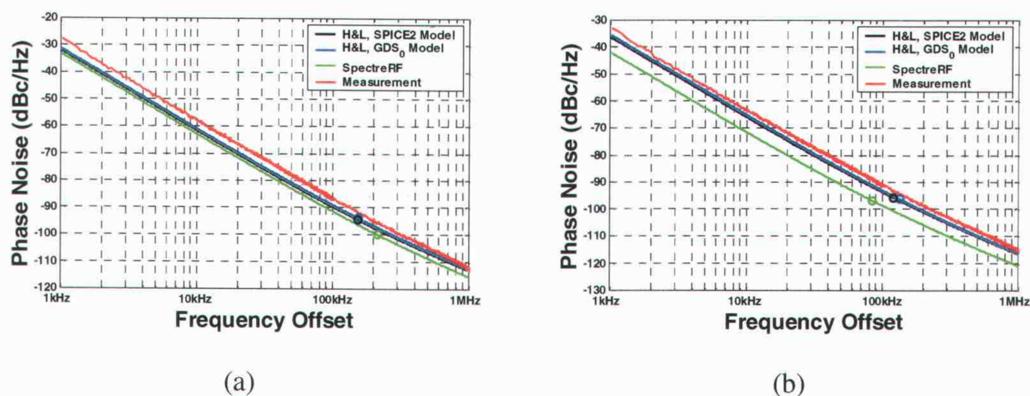


Figure 5.20 Measurements of the low-speed Maneatis load oscillator versus simulations for (a) V_{PMOS}=1.7V and V_{NMOS}=1.2V and (b) V_{PMOS}=1.3V and V_{NMOS}=1.5V.

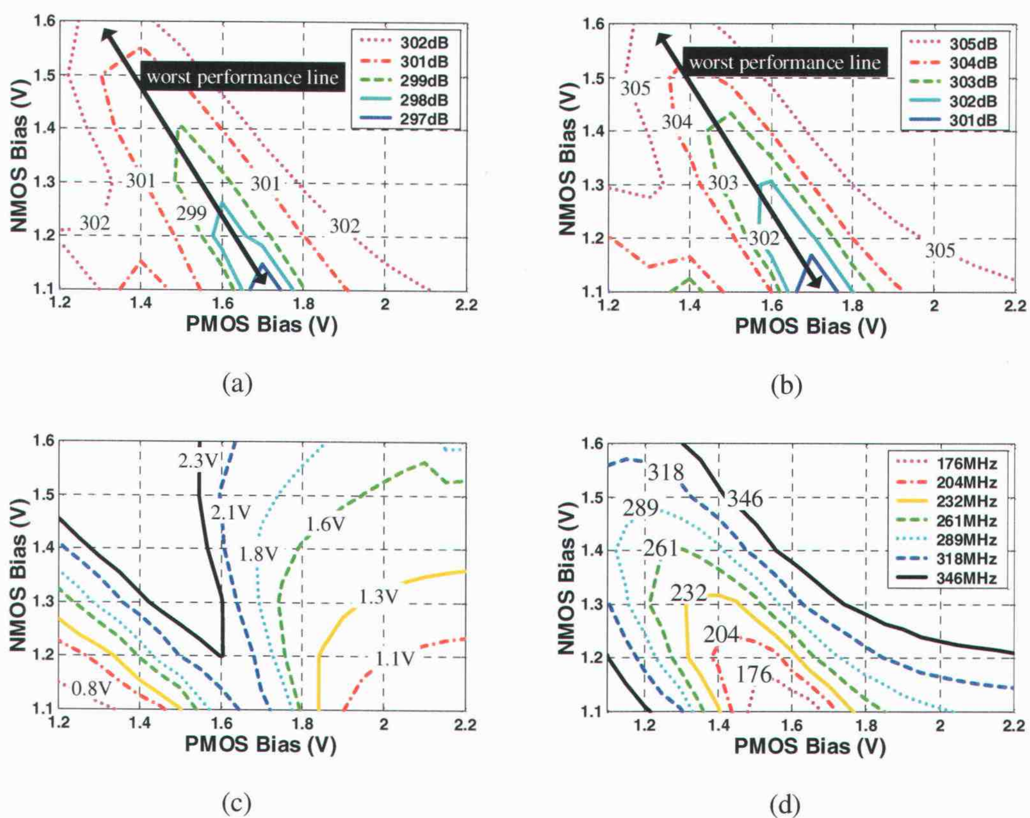


Figure 5.21 The simulated 1MHz offset figure of merit contours predicted by (a) H&L and (b) SpectreRF, (c) simulated oscillation amplitude contours and (d) measured oscillation frequency contours for the high-speed Maneatis load oscillator.

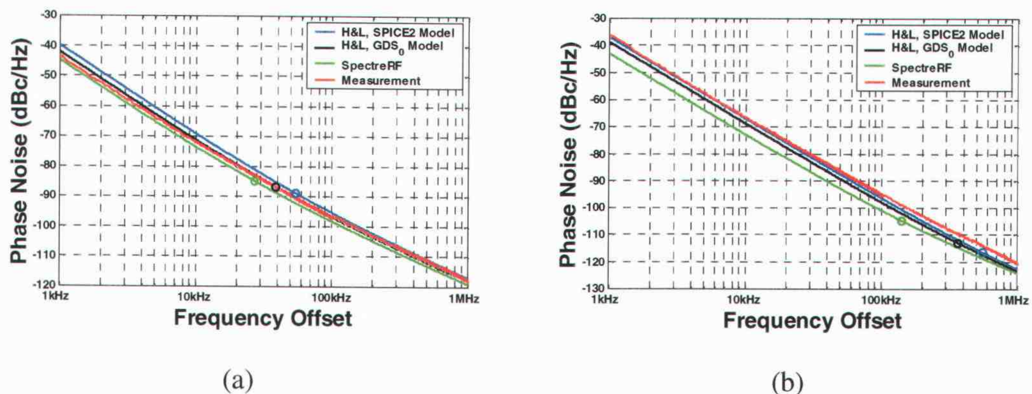


Figure 5.22 Measurements of the cross-coupled oscillator versus simulations for (a) V_{PMOS}=1.5V and V_{NMOS}=1.3V and (b) V_{PMOS}=2.2V and V_{NMOS}=1.5V.

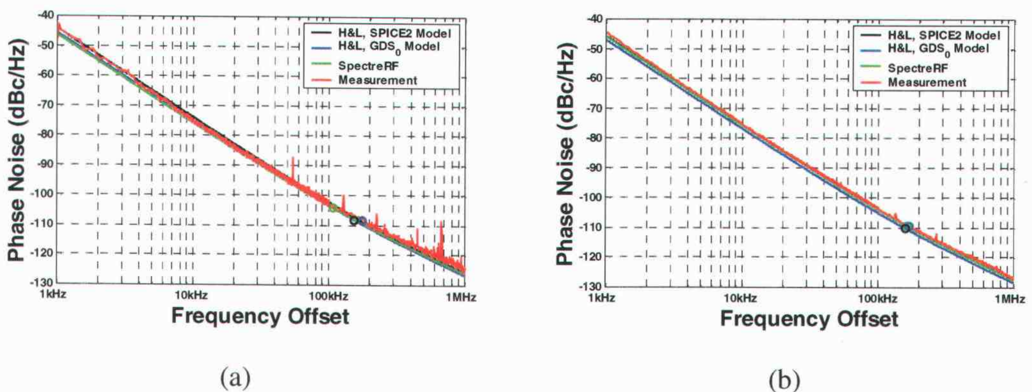


Figure 5.23 Measurements of the single-ended 5-stage oscillator versus simulations for (a) V_{DD}=2.0V and (b) V_{DD}=3.0V.

5.5.9. *Typical results for the 1998 single-ended 9-stage current-starved oscillator*

This oscillator's phase noise was measured at a fixed bias and several supply voltages in 1999 and at a fixed supply voltage and several bias voltages in 2001 for a total of nine measurements. Typical results are shown in Figure 5.25. In this oscillator all the simulation methods are very consistent with each other and accurately predict each measurement. The complete results are shown in Appendix I. The 1MHz figure of merit for this oscillator is shown in Figure 5.27 and it can be seen that this architecture has the poorest phase noise performance. The performance is largely unaffected by change in the control voltage but

decreases with increasing supply voltage. Analysis has shown that the diode-connected device causes significant short circuit current and leads to an over 25dB reduction in the FOM. As the supply voltage increases, the power efficiency decreases which explains the V_{DD} FOM trend.

5.5.10. *Typical results for the 1998 simple, single-ended 5-stage oscillator*

This oscillator was used to help determine the flicker noise model and K_f parameters chosen for this chip. Measurements for five different supply voltages are shown in Appendix J and representative results are compiled in Figure 5.23. Except for a supply voltage of 1.5V, all simulation methods are very consistent with the measurements. This measurement appears to approach a noise floor and may be due to the buffer not being adequately sized to give enough signal strength at low supply voltages.

5.6. Flicker Noise Prediction – Simulations versus Measurements

The choices of K_f and the flicker noise model enabled the measurements of the H&L series oscillators to closely match the simulations from all methods. The above section, however, and the appendices show that in the differential ring oscillators there are substantial differences. This section compares the measured flicker noise corners of the high-speed Maneatis load oscillator and the cross-coupled load oscillator with each simulation technique. Figure 5.28 shows the measured oscillator frequency corner contours of the high-speed Maneatis load oscillator compared to the simulated frequency corner contours predicted by SpectreRF, the H&L direct method and the H&L indirect method. It can be seen that while the shapes of the simulated contours are consistent, they are only generally consistent with the measurements and no simulation method completely matches the magnitude of the measurements. SpectreRF underestimates the corners while both Hajimiri and Lee methods tend to overestimate the corners. The indirect H&L method matches more closely than the direct method. The results for the cross-coupled load oscillator are similar although the simulations closely predict the shape of the contours as shown by Figure 5.29. Again

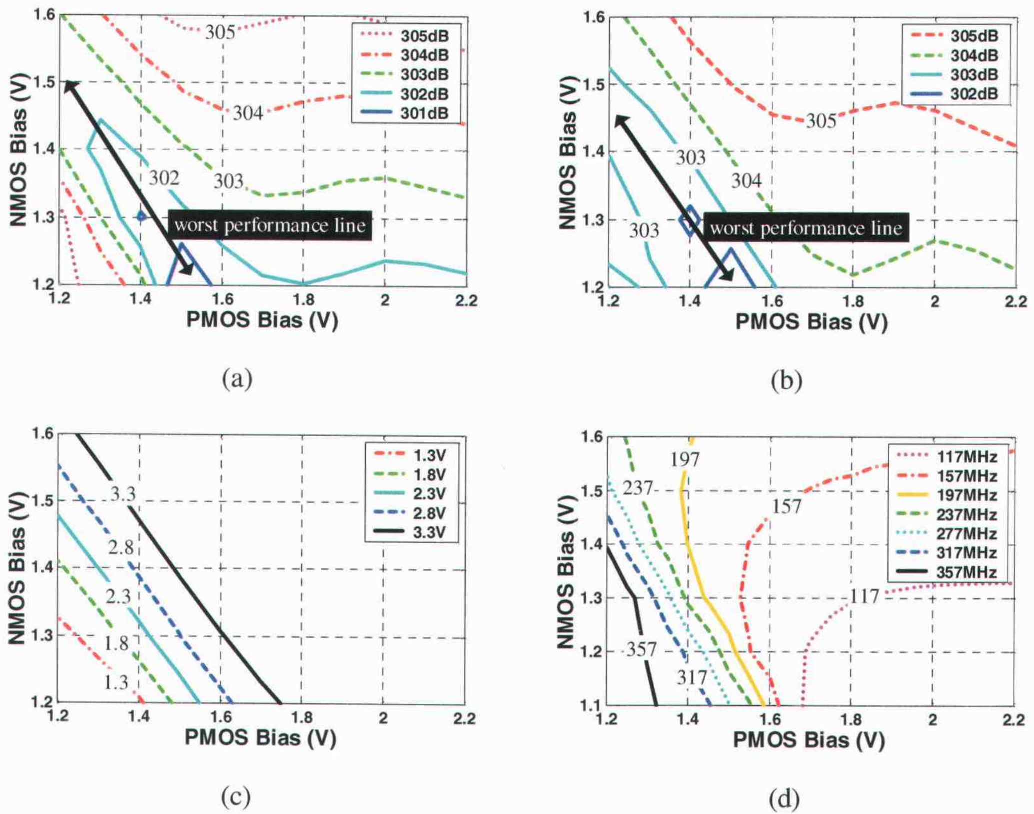


Figure 5.24 The 1MHz offset figure of merit contours predicted by (a) H&L and (b) SpectreRF, (c) simulated oscillation amplitude contours and (d) measured oscillation frequency contours for the cross-coupled load oscillator.

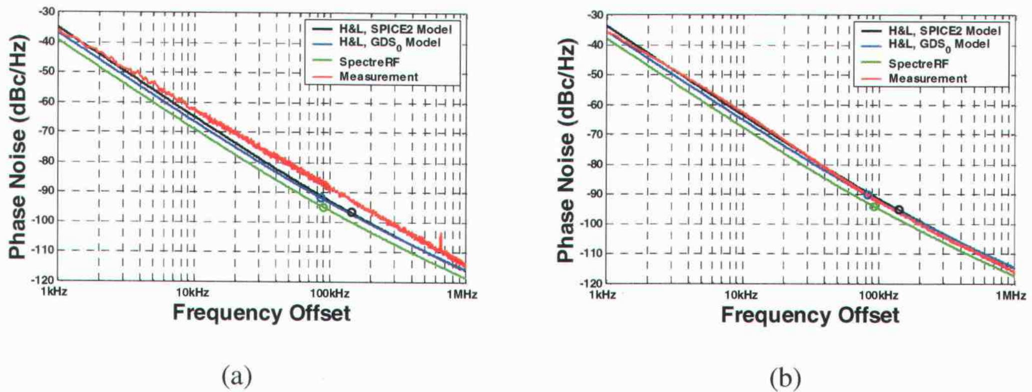


Figure 5.25 Measurements of the 9-stage current-starved oscillator versus simulations for (a) V_{CTRL}=1.24V and V_{DD}=2.0V and (b) V_{CTRL}=1.4V and V_{DD}=3.0V.

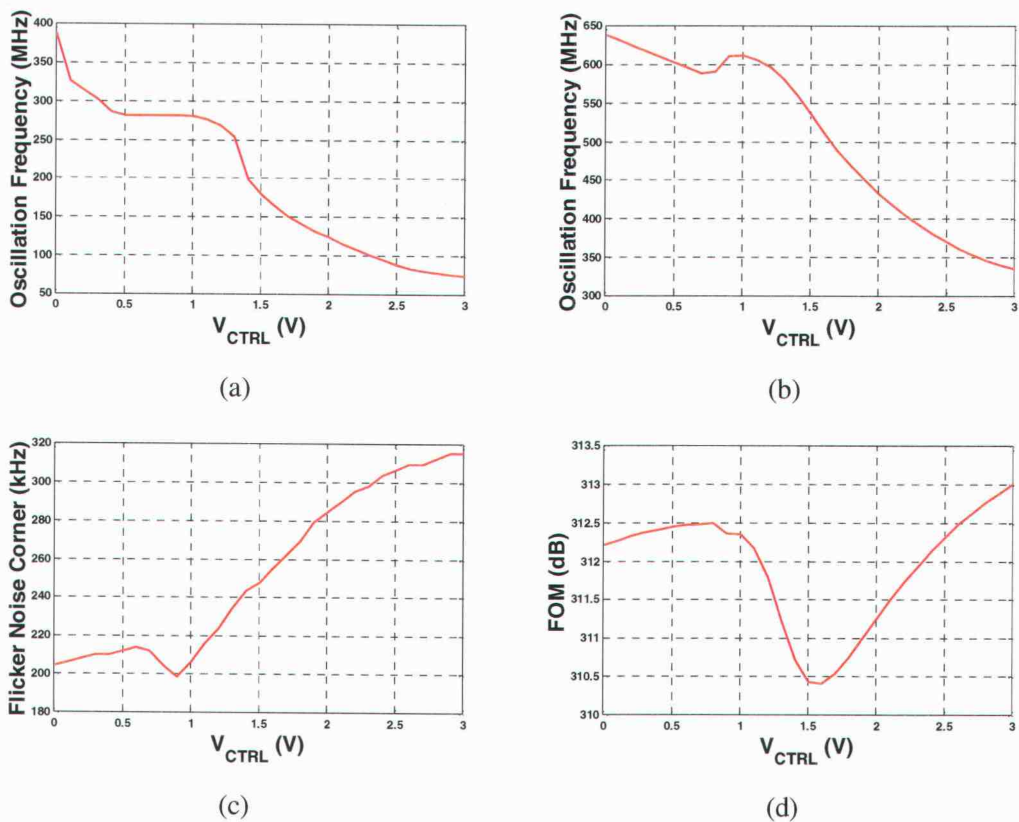


Figure 5.26 (a) The measured and (b) simulated oscillation frequency versus the control voltage of the PMOS pre-drive oscillator. The H&L indirect method was used to find (c) the oscillator flicker noise corner and (d) the figure of merit.

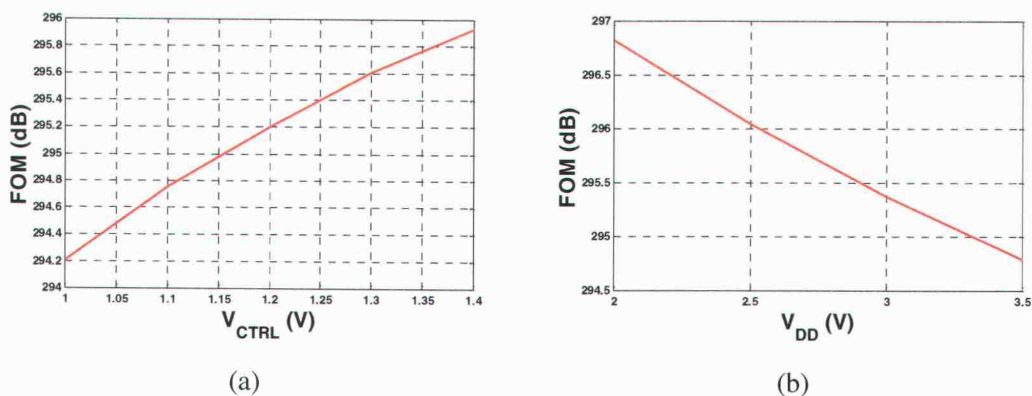


Figure 5.27 (a) The 1MHz figure of merit versus the control voltage (V_{DD} = 3.0V) and (b) the 1MHz figure of merit versus the supply voltage (V_{CTRL} = 1.24V).

SpectreRF underestimates the corner while both Hajimiri and Lee methods overestimate the corner, and again the indirect H&L method matches more closely than the direct method. Of the two methods presented to calculate cyclostationary noise, the indirect method shows better results than the direct method. This is puzzling since the direct method seems more fundamentally sound.

Though no method is perfect in predicting noise corners, all the methods presented can be used to find an oscillator's optimum or least optimum bias points. Also, although the disparity between the simulated and measured noise corners can seem significant in terms of percentages, in reality it is difficult to distinguish between otherwise identical phase noise curves whose flicker noise corners differ by 30%. For this reason the measurement results in Figure 5.28(a) and Figure 5.29(a) have a tolerance of at least ±15%.

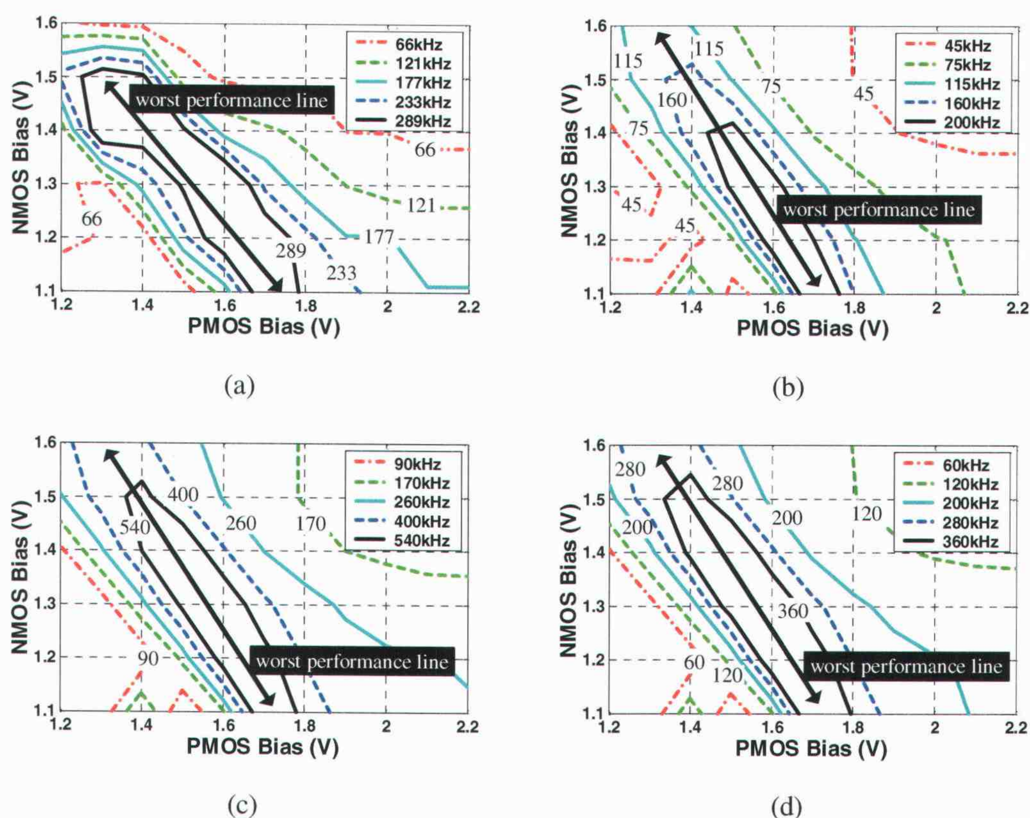


Figure 5.28 The measured oscillator flicker noise corner contours (a) of the high-speed Maneatis load oscillator compared to the simulated flicker noise corner contours predicted by (b) SpectreRF, (c) the H&L direct method and (d) the H&L indirect method.

The disparity between simulations and the measurements could also in part be due to the SPICE2 flicker noise model. It is known that this equation does not perfectly model flicker noise, and at some point it would be surprising if simulations based on this model were consistently accurate in predicting flicker noise up-conversion.

5.7. Layout Experiment Results

The H&L2 series oscillator was laid out in a fully interdigitated layout as shown in Section 4.1.1 and a distributed layout as explained in Section 4.1.2. The oscillator schematics are identical in both cases. The phase noise of both oscillators was measured for several supply voltages as shown in Figure 5.30, Figure 5.31 and Figure 5.32. The distributed layout

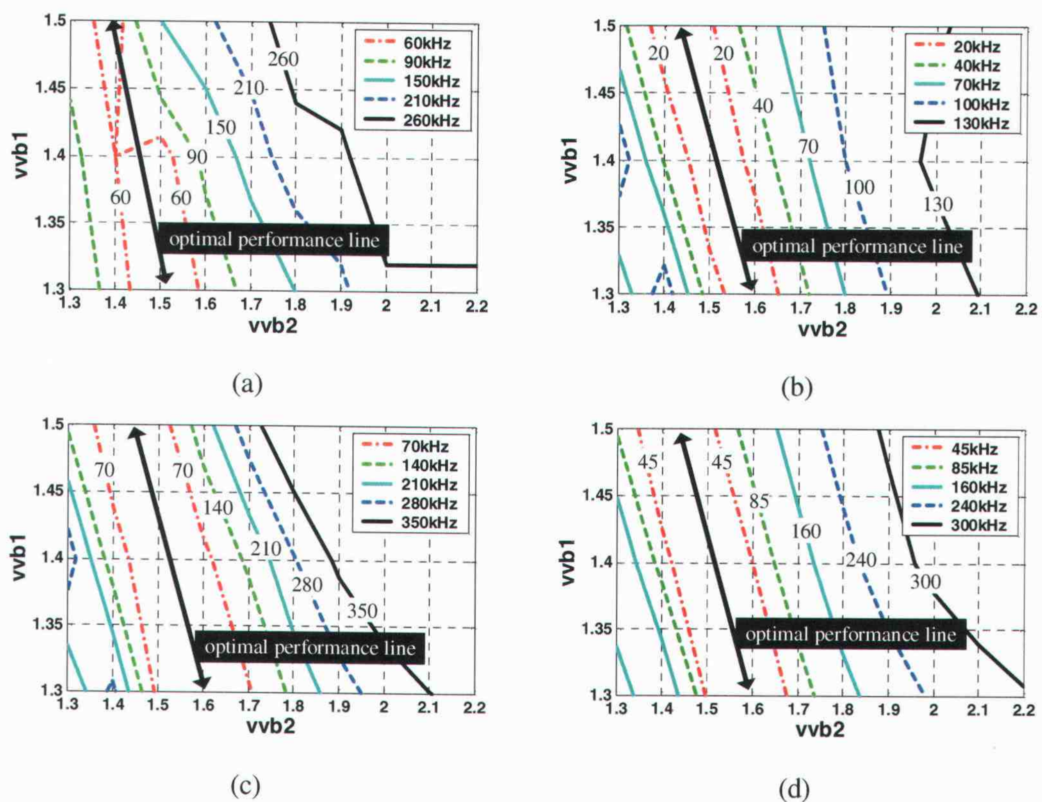


Figure 5.29 The measured oscillator flicker noise corner contours (a) of cross-coupled load oscillator compared to the simulated flicker noise corner contours predicted by (b) SpectreRF, (c) the H&L direct method and (d) the H&L indirect method.

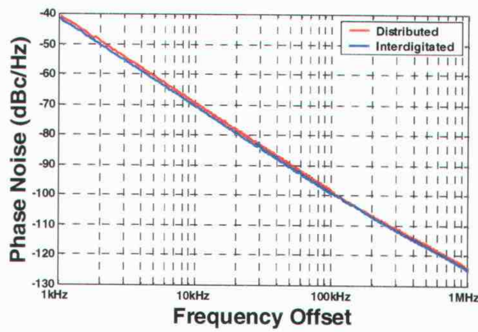
has less parasitic capacitance due to less wiring and thus a higher frequency of oscillation as shown in Appendix I. The frequency difference has been normalized out of the results shown. In general the measurements are within 1dB of each other and indicate a negligible difference in phase noise between the two layout styles.

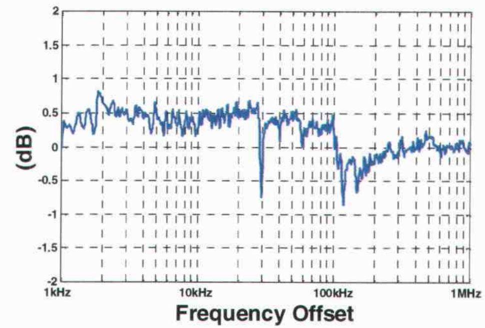
5.8. Phase Noise due to Deterministic Noise

From the Hajimiri and Lee theory it is predicted that interference noise consisting of pure tones will appear in the oscillator's phase noise spectrum as pure tones and will not affect the phase noise at other frequencies. This is contrary to measured results from previous research [36] and was extensively re-measured in this work. Figure 5.33 shows the phase noise in the H&L3 oscillator before and after injecting sinusoidal noise at f_0+*500kHz*, where the measured oscillation frequency was 349.1MHz.

In this figure it can be seen that the addition of a tone at f_0+*500kHz* causes a tone in the phase noise spectrum at f_0+*500kHz* but does not disturb the phase noise at other offset frequencies. The magnitude of the tone is 22.5dB above the reference measurement, but this must be de-normalized with respect to the resolution bandwidth. The true magnitude of the tone is 32.9dB greater, or 55.4dB. In Figure 5.34 the experiment was repeated except noise was injected into the buffer power supply. The results match the previous experiment except the true magnitude of the tone in the phase noise spectrum is 46.9dB. This shows that the phase noise spectrum is less sensitive to noise injected into the buffer.

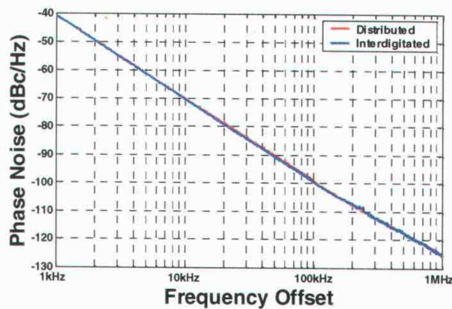
The last supply noise experiment is for the Maneatis load differential oscillator. Here, again noise was injected at f_0+*500kHz* and also at 150MHz. The measured oscillation frequency was 391.4MHz. Figure 5.35 shows the result of the experiment and is consistent with the results of the single-ended circuit. The true magnitude of the tone in the output spectrum is 67.4dB. Although the frequency of oscillation is slightly different from the single-ended counterpart, this accounts for about 1dB of the difference and this example shows the differential circuit to be more sensitive to supply noise at this bias.

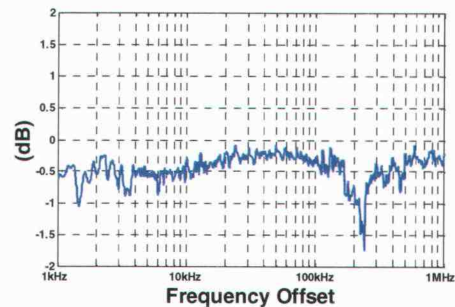




(a) (b)

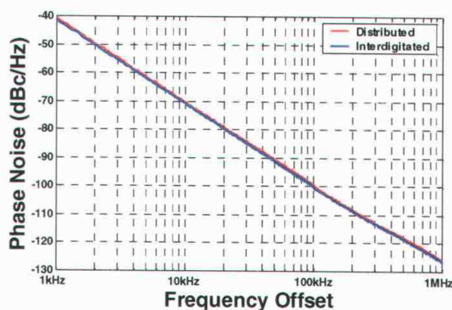
Figure 5.30 (a) The phase noise of the distributed versus interdigitated layout and (b) the difference between them for a supply voltage of 2.5V.

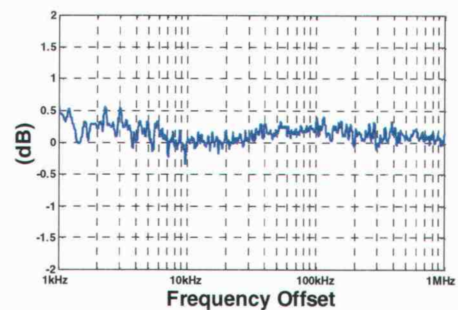




(a) (b)

Figure 5.31 (a) The phase noise of the distributed versus interdigitated layout and (b) the difference between them for a supply voltage of 3.0V.





(a) (b)

Figure 5.32 (a) The phase noise of the distributed versus interdigitated layout and (b) the difference between them for a supply voltage of 3.5V.

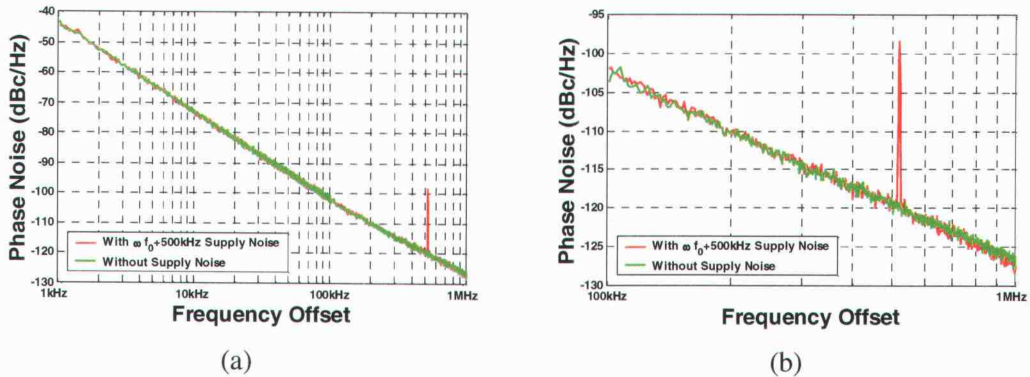


Figure 5.33 Phase noise of the H&L3 oscillator with 100m$V_{p\text{-}p}$ oscillator supply noise injected at f_0*+500kHz* showing (a) the entire spectrum and (b) a single decade of the spectrum.

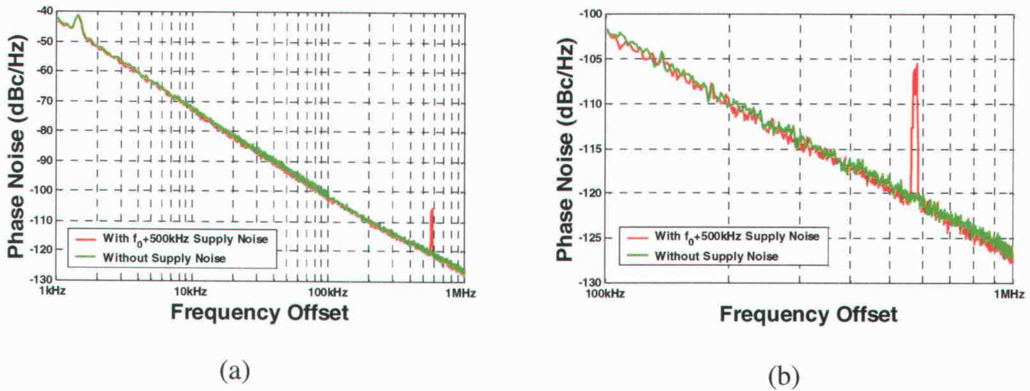


Figure 5.34 Phase noise of the H&L3 oscillator with 100m$V_{p\text{-}p}$ of buffer supply noise injected at f_0*+500kHz* showing (a) the entire spectrum and (b) a single decade of the spectrum.

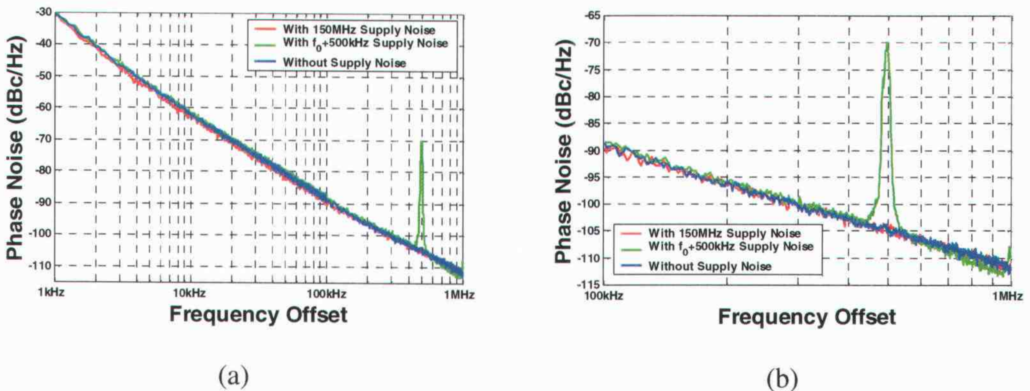


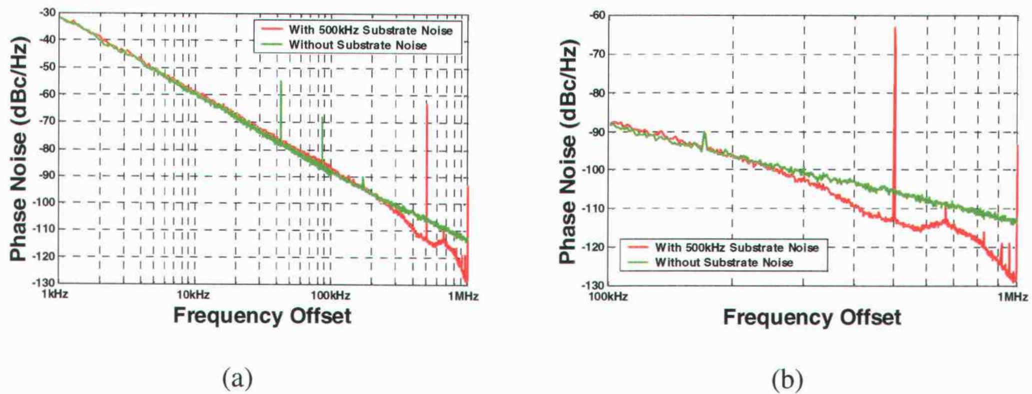
Figure 5.35 Phase noise of the high speed Maneatis load oscillator with 100m$V_{p\text{-}p}$ of supply noise injected at 150MHz and f_0*+500kHz* showing (a) the entire spectrum and (b) a single decade of the spectrum. The bias point was V_{PMOS}=1.8V and V_{NMOS}=1.4V.

The supply noise experiments were repeated for substrate noise injection. Figure 5.36 and Figure 5.37 show the result of injecting 500kHz substrate noise symmetrically and asymmetrically at the same bias point, respectively, and are representative of results obtained at other bias points. In addition to using the low phase noise signal source, a 500kHz band pass filter from Allen Avionics, Inc. was used to filter the source and remove any harmonics or subharmonics. The filter provides 95dB of loss at 1MHz. The result of the signal injection, shown in Figure 5.36, is highly unusual; it shows the phase noise around the frequency of the noise injection and the 2nd harmonic of the noise injection is severely perturbed. It also shows the presence of a strong tone at 1MHz which must be the result of circuit nonlinearities. The true magnitude of the tone above the reference measurement in Figure 5.36 was 75.8dB and in Figure 5.37 it was 53.7dB. The oscillation frequency was 118.5MHz in both circuits.

5.9. Jitter Measurement Setup, Equipment and Analysis

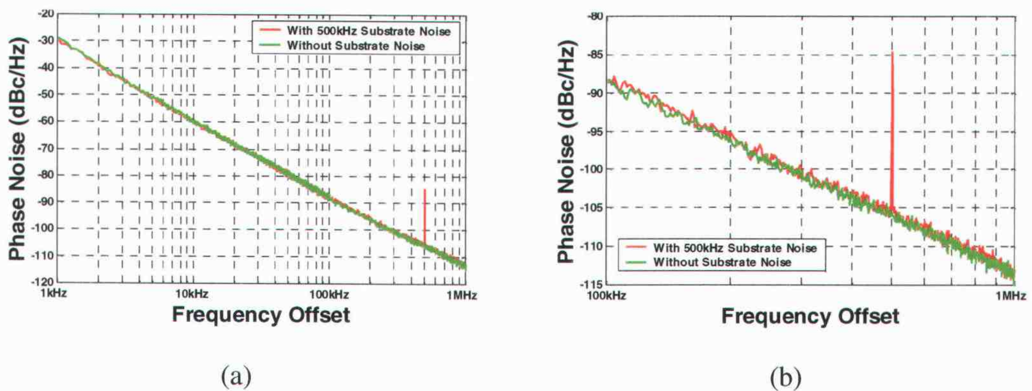
All jitter measurements were taken in a screen room environment with a Wavecrest DTS2079 which has the capability to directly measure absolute jitter. The measurements were converted to peak jitter as defined by (3.5), and all simulation, equation and measurement results shown are in terms of peak jitter unless otherwise noted. As discussed in Chapter 3, when injecting sinusoidal noise, the quantity measured by the DTS2079 is a combination of jitter due to random noise sources such as white and flicker noise, and the jitter imposed by the sinusoid. To separate the effects, reference measurements were taken without the influence of deterministic noise. Figure 5.38 shows a jitter waveform due to only random noise from the single-ended asymmetric substrate injection circuit. A waveform typical of that observed when the oscillator is exposed to deterministic noise is shown in Figure 5.39(a). To obtain the circuit's response to only deterministic noise, the waveform in Figure 5.38 is subtracted from the waveform in Figure 5.39 (a), leaving the result in Figure 5.39 (b). In cases where a reference measurement could not be taken, it can be noted from Figure 5.38 that the reference measurement is nearly linear. The effect of subtracting out the reference measurement can be simulated by de-correlating the measurement from the x-axis.

It can be seen from Figure 5.39 (b) that the magnitude and clarity of the absolute jitter seem to decline with time. This is an artifact of the DTS2079 and the jitter at a small number of oscillation cycles is the most credible.



(a) (b)

Figure 5.36 Phase noise of the low speed Maneatis load oscillator with 200mV$_{p-p}$ of substrate noise injected symmetrically at 500kHz showing (a) the entire spectrum and (b) a single decade of the spectrum. The bias point was V_{PMOS}=1.5V and V_{NMOS}=1.4V.



(a) (b)

Figure 5.37 Phase noise of the low speed Maneatis load oscillator with 200mV$_{p-p}$ of substrate noise injected asymmetrically at 500kHz showing (a) the entire spectrum and (b) a single decade of the spectrum. The bias point was V_{PMOS}=1.5V and V_{NMOS}=1.4V.

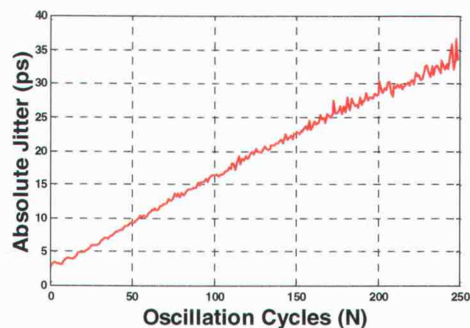


Figure 5.38 Absolute jitter due to random noise sources.

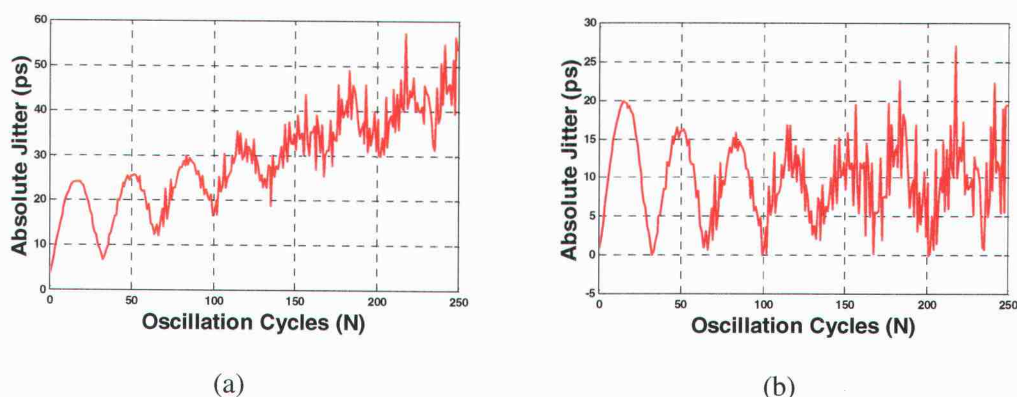


Figure 5.39 (a) Absolute jitter due to both random and deterministic noise sources. (b) The result of subtracting out the absolute jitter due to random noise sources, leaving only the absolute jitter due to the sinusoidal noise injected.

The oscillators were powered by the battery box described in this chapter. When injecting sinusoids into the supply or substrate, an HP 8664A signal generator was used. In the case of jitter due to supply noise, the deterministic noise source was capacitively coupled to the supply. The magnitude of the source was kept constant at –25dBm. In the case of substrate noise injection, a constant signal magnitude of –5dBm was injected into the substrate. The magnitude of the signals injected was monitored with an HP 8563EC spectrum analyzer.

5.10. Substrate Models

The substrate model between the noise injectors and the transistor bulks was assumed to be a simple resistive voltage divider as shown by Figure 5.40 [37], [38]. Although the substrate network consists of capacitive elements as well, it has been shown that these elements can be neglected at frequencies less than 1GHz, which is greater than the frequencies of interest here. Additionally, the substrate network in Figure 5.40(b) shows that for PMOS devices, there is a well capacitance between the n-well and the substrate, along with two voltage divider networks. This implies the PMOS transistors are not significant contributors to substrate-induced noise at low frequencies and they have been neglected in this work.

To determine the values of the resistive elements, the program Extraction of Parasitics for Integrated Circuits [39], version 6, was used to analyze the physical geometry of each layout. This program is only capable of calculating the substrate resistance network between p+

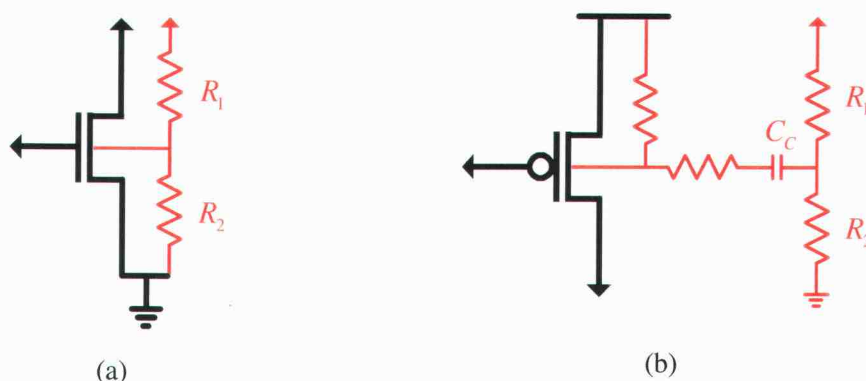


Figure 5.40 This work assumes the substrate networks can be reduced to simple voltage dividers between the noise source and ground. (a) Substrate network for NMOS transistors. (b) Substrate network for PMOS transistors.

contacts in a p substrate; to use the program NMOS transistors were modeled as p+ regions instead of n+ regions. For resistances calculations, EPIC must be provided with the doping profile of the substrate. To accurately determine the doping profile, SRP structures were placed on the chip; after fabrication a chip was sent to Solecon. The doping profile was determined by grinding the surface of the chip and measuring the incremental changes in resistance.

5.11. Jitter Measurement and Simulation Results

5.11.1. Verification of the predictive jitter equations

Each of the eight oscillators' jitter performance due to deterministic substrate and supply noise over a wide frequency range has been measured. In the case of the differential oscillators, jitter due to a 1MHz sinusoid has been measured with symmetric substrate noise injection and asymmetric supply noise injected over a range of biasing conditions. All of the circuits have been simulated for at least 200 cycles with Spectre time domain simulations using the parameters in Table 5.3. The measurements and simulations are compared with the predictive jitter equations developed in Chapter 3.

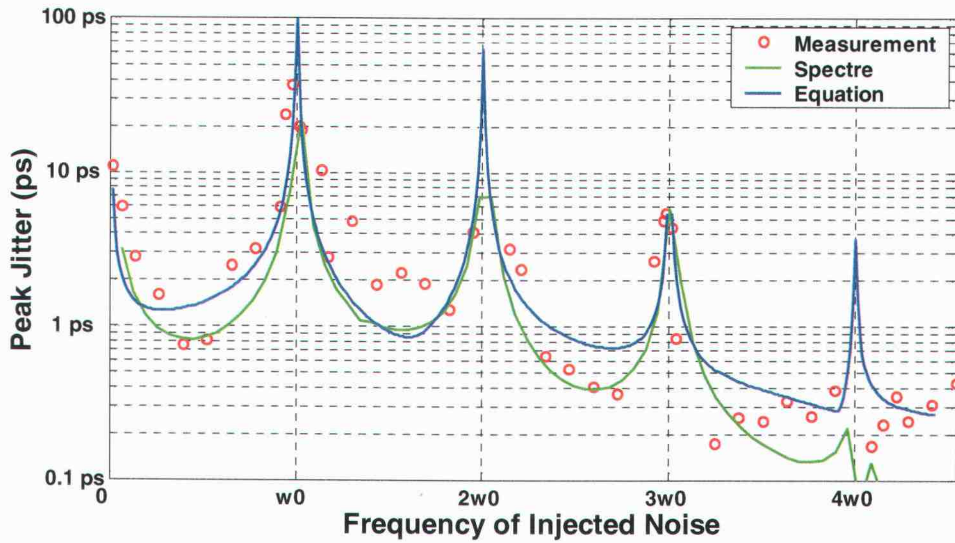


Figure 5.41 Single-ended circuit asymmetric substrate noise injection.

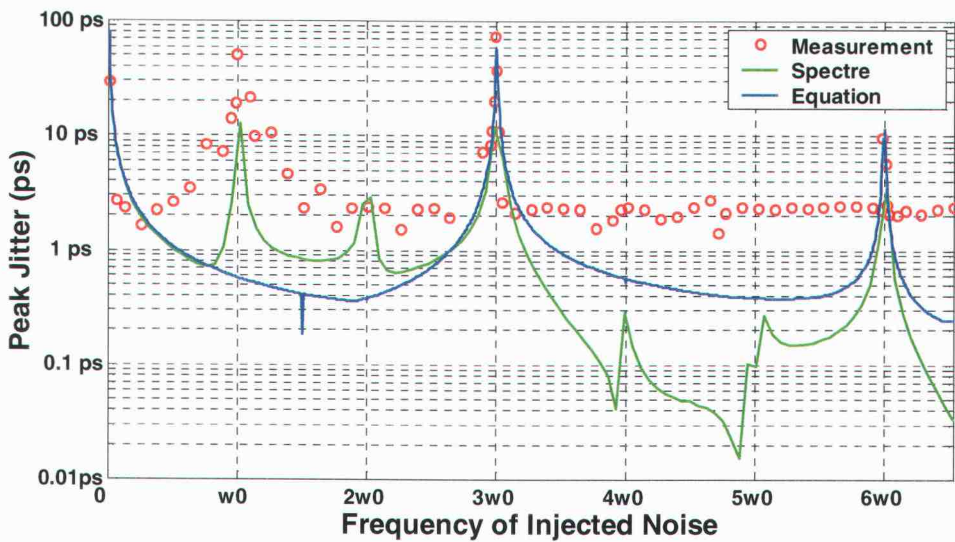


Figure 5.42 Single-ended circuit symmetric substrate noise injection.

Parameter	Value
reltol	1e-9
vabstol	1e-11
iabstol	1e-15
Time step	1ps

Table 5.3 Spectre accuracy settings used for all jitter simulations.

The measured frequency of oscillation for the single-ended ring oscillators was 81MHz. In the differential cases, where the bias point was held constant and the frequency of the injected noise was swept, the bias point was V_{NMOS} = 1.4V and V_{PMOS} = 1.6V. At this bias point, the measured frequency of oscillation was 131MHz.

Figure 5.41 and Figure 5.42 show the result of injecting noise into the substrates of the single-ended ring oscillator circuits. Both measurement results show general agreement with

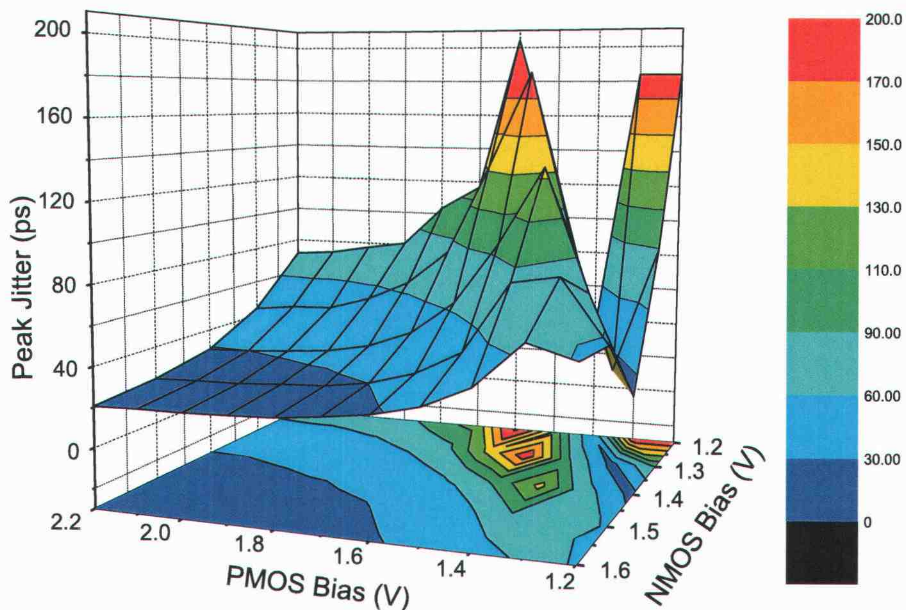


Figure 5.43 2-D sweep of PMOSFET and NMOSFET bias voltages shows that the differential circuit's jitter sensitivity to symmetrically injected substrate noise is bias dependent. The contours are projected on the x-y plane.

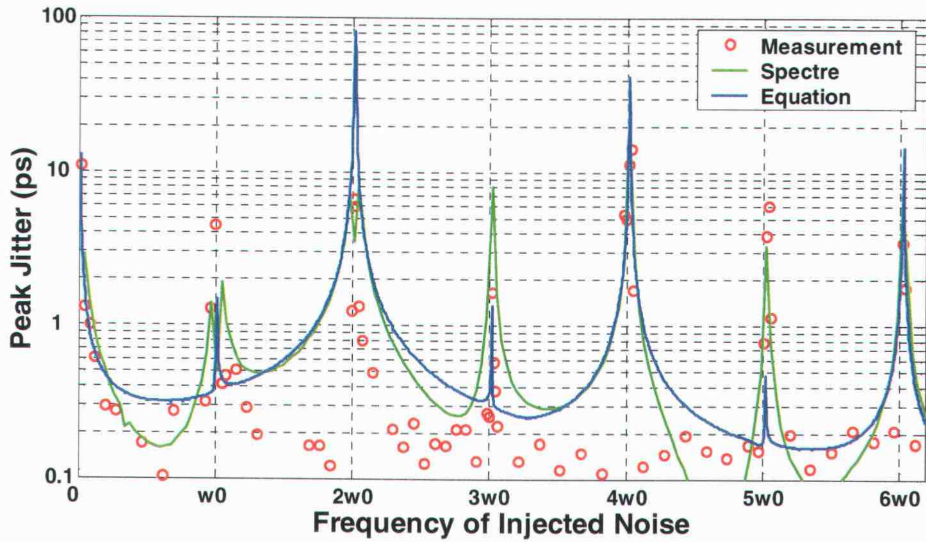


Figure 5.44 Differential circuit asymmetric substrate noise injection.

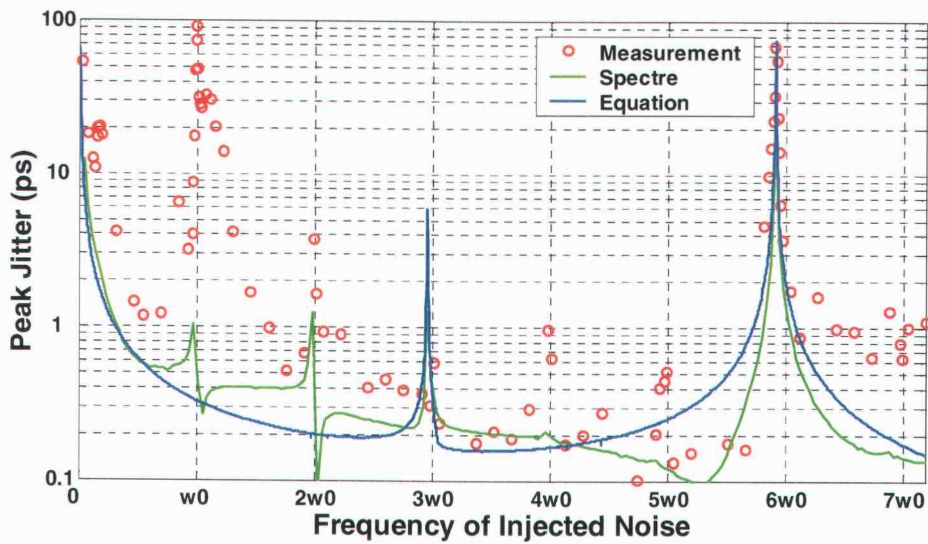


Figure 5.45 Differential circuit symmetric substrate noise injection.

simulations and equations. The symmetric case, however, has substantial peaking at ω_0. This phenomenon is not predicted by either simulations or equations or by placing reasonable asymmetries in the circuit. Peaking at $3\omega_0$ and $6\omega_0$, however is as expected from the equations and simulation. Figure 5.44 and Figure 5.45 show the result of injecting substrate noise into the substrate of the differential circuits. Again, measurements show general agreement with Spectre simulations and equations. Figure 5.45 shows peaking at ω_0, $2\omega_0$, $4\omega_0$ and $5\omega_0$ that is not predicted by simulations of the ideal circuit or equations. Some of the peaks can be accounted for with mismatches in the circuit. Although in these plots the differential circuits reject substrate noise better than the single-ended circuits, the jitter performance of the differential oscillators is dependent on the bias point. One measurement was done by symmetrically injecting a 1MHz sinusoid into the substrate of the differential oscillator and sweeping the bias point of the oscillator with the result shown in Figure 5.43. This figure shows distinct regions where the oscillator is quite sensitive to substrate noise and regions where the oscillator is relatively insensitive to substrate noise. The transitions between these regions can be very abrupt.

The supply noise rejection for the single-ended circuits is shown in Figure 5.46 and Figure 5.47. In general the measurements agree with the simulations and the equations. In Figure 5.47 Spectre does not predict the peak at $3\omega_0$ although this is predicted in the equations. The equations are nearly identical to the measurements.

Figure 5.48 and Figure 5.49 show the jitter results for supply noise injected into the DROs as the bias point is held constant. In Figure 5.48 the equations and simulation both show some deviations from the measurements. Figure 5.49, however, shows substantial differences between the measurements and the simulations and equations. Chapter 6 analyzes the unexpected peaking in the symmetric circuits. As in the substrate injection case, the sensitivity to noise is bias dependent as shown in Figure 5.50. This figure illustrates the oscillator's sensitivity to 1MHz noise versus bias as supply noise is injected asymmetrically.

In nearly all cases, the measurements involving asymmetric noise injection show peaking at integer multiples of ω_0 which is an anticipated result of (3.17). Also, the measurements done where noise is injected symmetrically show peaking at integer multiples of $3\omega_0$ which is an anticipated result of (3.18), for N=3. This validates the predictions of (3.17) and (3.18) for symmetrical versus asymmetrical noise injection.

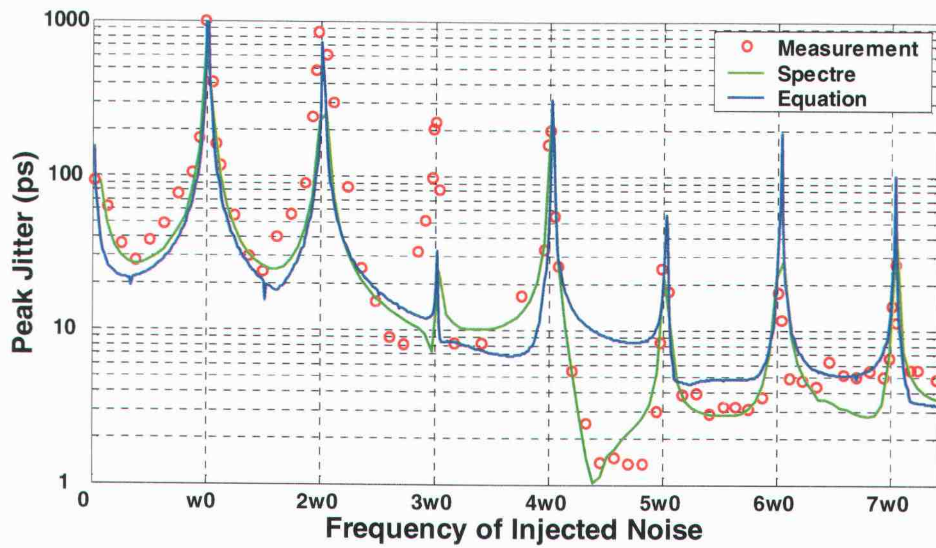


Figure 5.46 Single-ended circuit asymmetric supply noise injection.

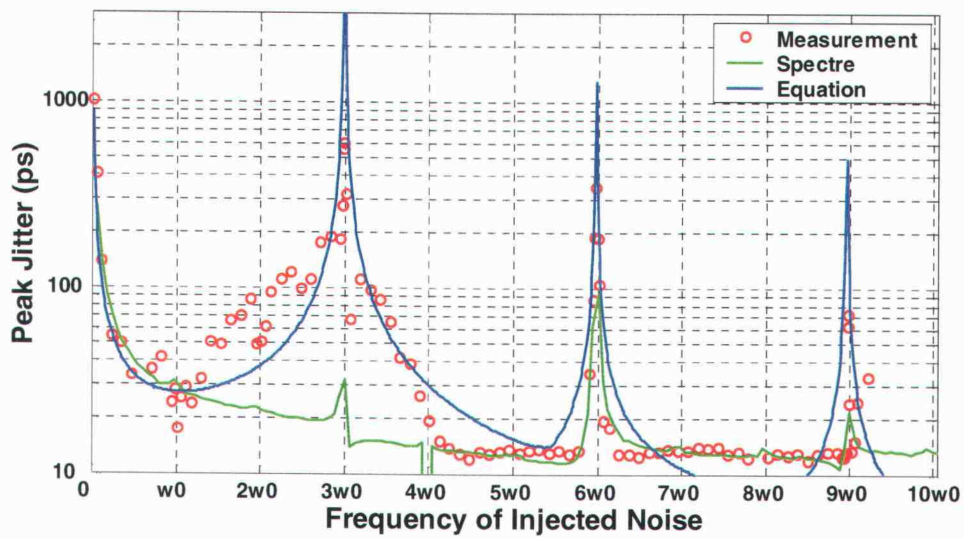


Figure 5.47 Single-ended circuit symmetric supply noise injection.

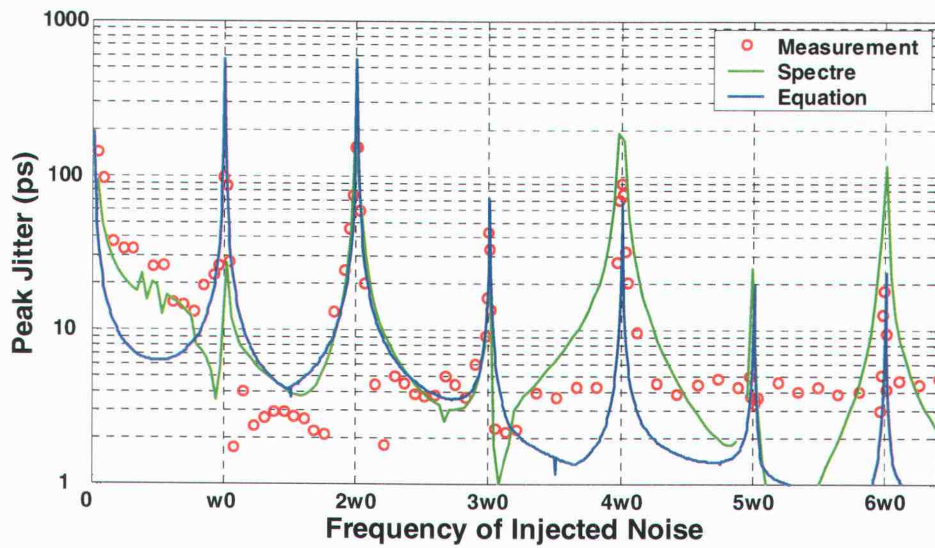


Figure 5.48 Differential circuit asymmetric supply noise injection.

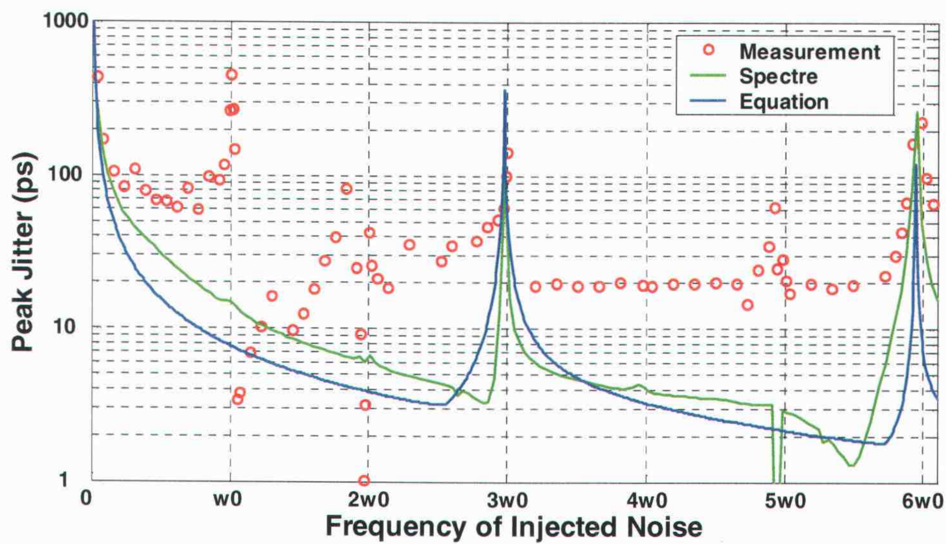


Figure 5.49 Differential circuit symmetric supply noise injection.

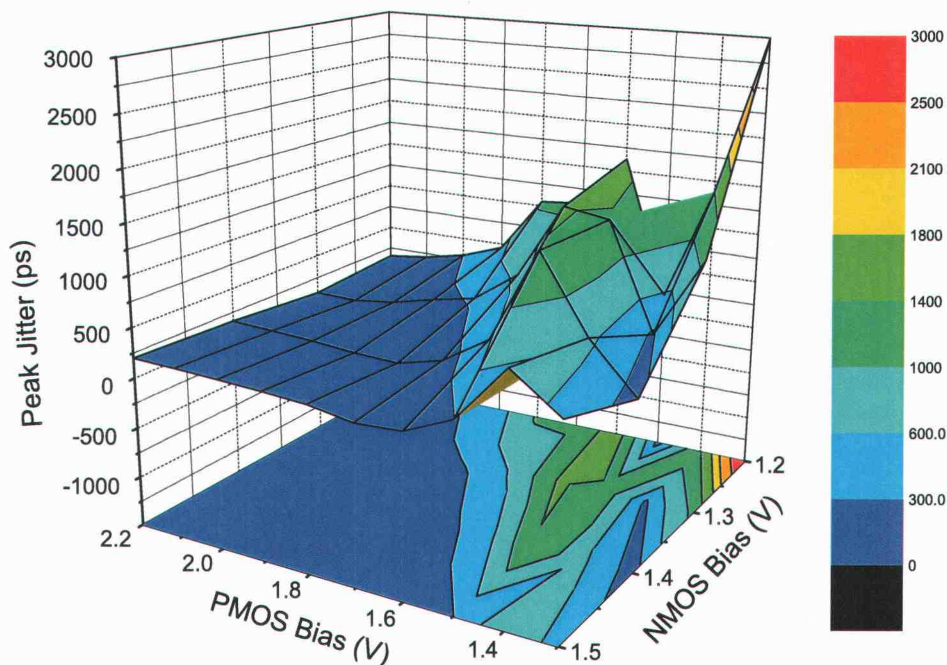


Figure 5.50 2-D sweep of PMOSFET and NMOSFET bias voltages shows that the circuit's jitter sensitivity to asymmetrically injected supply noise is bias dependent. The contours are projected on the x-y plane.

The measurement results consistently show that supply noise dominated over substrate noise even though the injected substrate noise was 10x greater in magnitude. This should be expected, particularly at low frequencies. Low frequency supply noise will modulate the g_m of the transistors, while low frequency substrate noise will modulate g_{mb}. It is typical for g_m to be five times the value of g_{mb}. This is demonstrated in the simple ring oscillator circuit example of Figure 5.51 with an oscillation frequency of 200MHz. In this example, supply noise of constant magnitude is injected directly into the supply and the NMOSFET bulk of each delay cell. The simulated peak jitter is shown in Figure 5.52(a) for each case, and in Figure 5.52(b) the results are normalized to the jitter magnitude of the substrate case. This plot shows that at low frequencies supply noise is 4-6 times more dominant than substrate noise and the ratio generally increases at higher frequencies. The ratio increase at higher frequencies may be due to noise coupling though the parasitic capacitors. At high frequencies, supply noise will

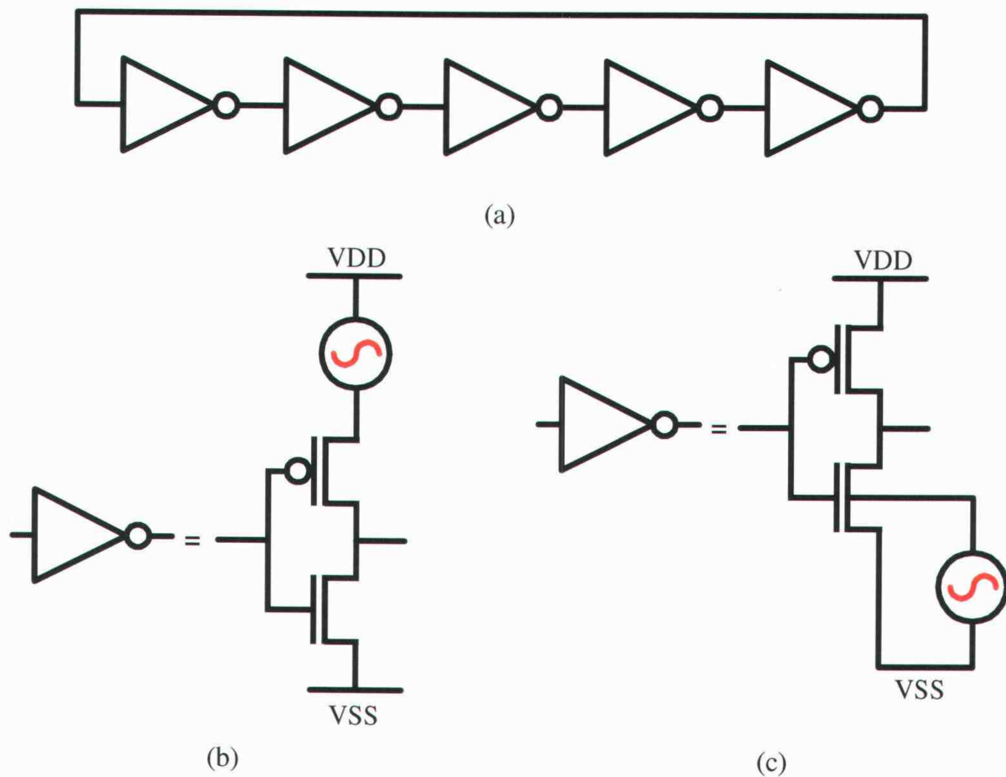


Figure 5.51 (a) 5-stage simple ring oscillator with delay cells wired for (b) supply noise and (c) substrate noise.

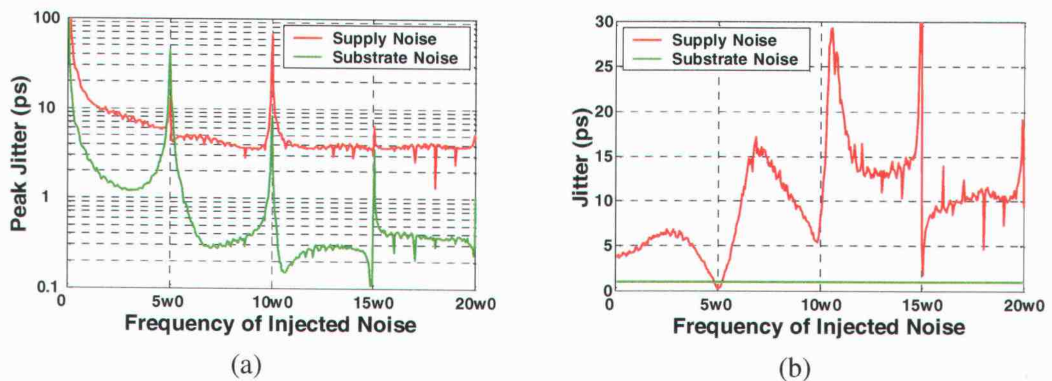


Figure 5.52 (a) Supply and substrate noise simulation results for the delay cells in Figure 5.51(b) and Figure 5.51(c). (b) The curves from (a) are normalized to the substrate noise injection curve.

couple though the parasitic capacitance C_{gs} while substrate noise will couple through the parasitics C_{db} and C_{gb}. The C_{gs} capacitance usually dominates over C_{db} and C_{gb} in MOSFET transistors [40].

An additional surprise in the results is that the differential circuits had jitter performance comparable to the single-ended circuits. Although the plots show the differential circuit to have an edge, the differential circuits' oscillation frequency of 130MHz versus 85MHz for the single-ended circuits gave the differential oscillators an artificial performance boost of 34% as shown in Section 3.4.

Although there is general agreement between the Spectre simulations and the equations, one significant difference between the two methods is time efficiency. The equation-based method required approximately one hour of simulation and MATLAB time for each circuit, whereas direct simulation of each circuit in Spectre® required more than 100 hours of simulation time on a Sun® Ultra 10 workstation.

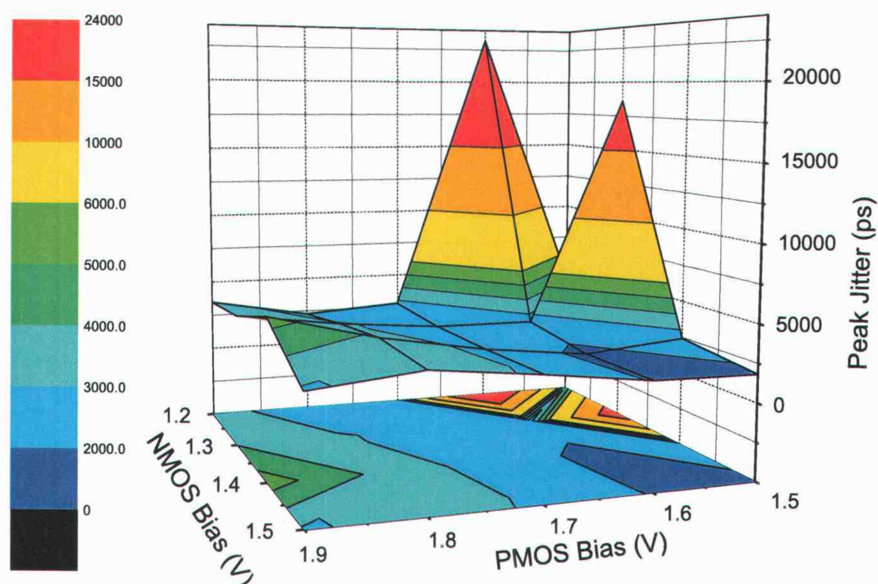


Figure 5.53 Measured peak jitter versus bias point for the "vanilla" differential oscillator. The contours are projected on the x-y plane.

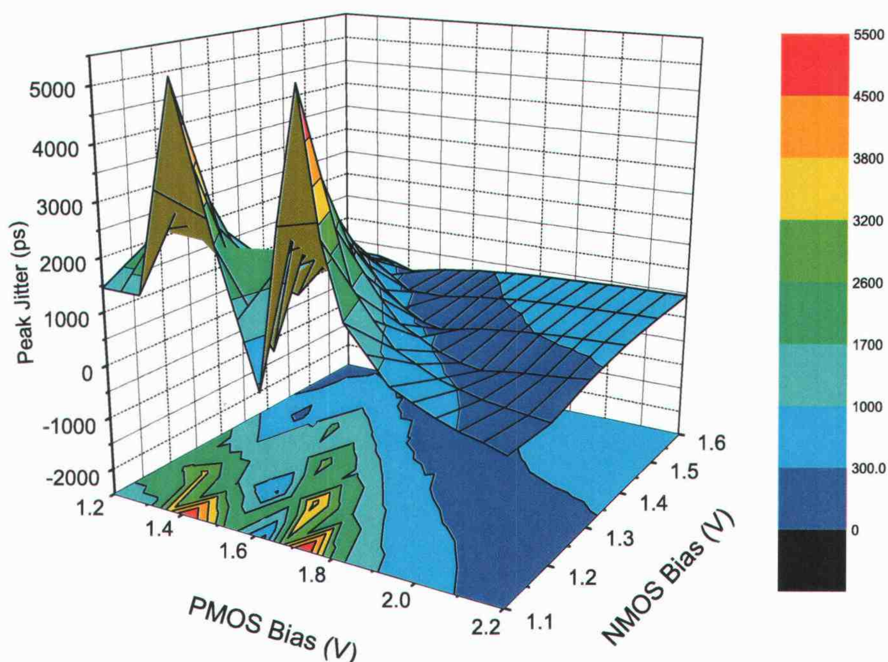


Figure 5.54 Measured peak jitter versus bias point for the Maneatis load differential oscillator. The contours are projected on the x-y plane.

5.11.2. Architecture comparison results

In system-on-a-chip designs, oscillators often share a power supply with a substantial amount of digital circuitry or other blocks that exhibit large transient currents. Through metal IR drops, inductive ringing, capacitive coupling or poor power supply regulation these transient currents induce supply noise which is not white in nature. Even if carefully designed, supply noise can be the dominant source of phase noise and jitter in an oscillator. In an experiment to compare the supply noise rejection performance of three of the differential architectures, the "vanilla" differential, the high-speed Maneatis load oscillator and the cross-coupled load oscillator, a 1MHz, -25dBm sinusoid was applied symmetrically to each oscillator supply and the bias point varied. Figure 5.53, Figure 5.54 and Figure 5.55 show the result for each experiment. The measured results all show distinct trends in the jitter magnitudes that can best be described as mountain ranges or valleys. These results are compared with each other and simulations in Chapter 6.

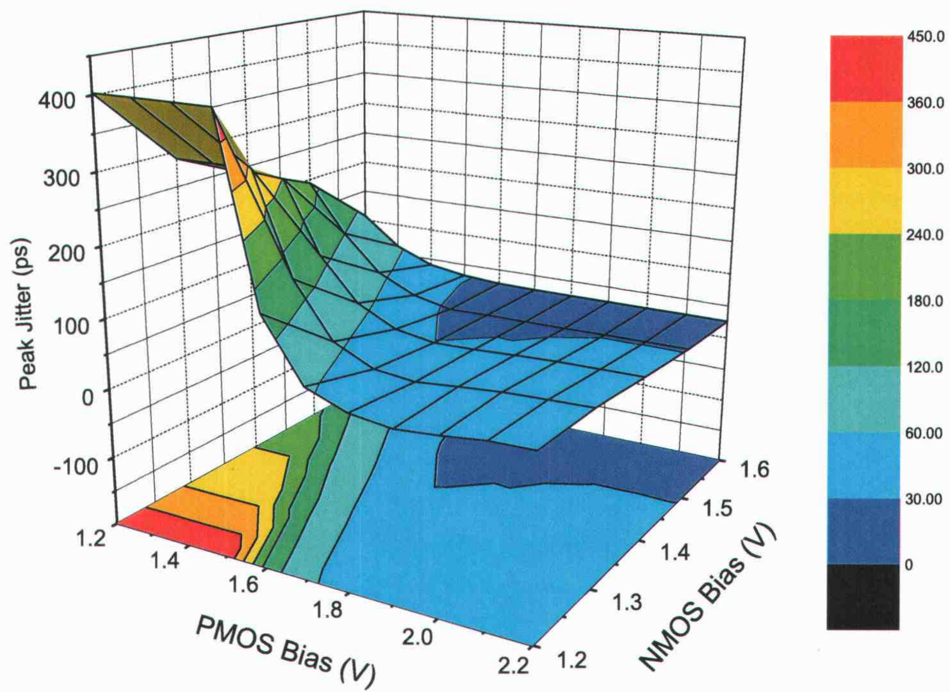


Figure 5.55 Measured peak jitter versus bias point for the cross-coupled load differential oscillator. The contours are projected on the x-y plane.

6. ANALYSIS OF THE JITTER MEASUREMENTS

In this thesis four oscillators were designed for symmetric noise injection to verify (3.18). No physical circuit, however, is perfectly symmetric and the measurements showed peaking not predicted by this equation or the Spectre time domain simulations. This chapter analyzes the effect of asymmetries due to component mismatch and identifies components most sensitive to mismatch. The simulation results presented in Section 6.1 are based on the circuits designed and measured, but in the case of substrate injection simplified substrate networks are used. Section 6.2 studies the architectures of Chapter 5 and compares the results with simulations, while Section 6.3 looks at symmetric and asymmetric noise injection using the jitter metrics cycle jitter and cycle-to-cycle jitter defined in Section 3.1.

6.1. Mismatch in Oscillators

Although MOSFET transistors are designed for specific widths and lengths, limitations in the photolithographic process, ion implantation angles, deviation in acid concentrations or other manufacturing defects cause random variations in each transistor's width and length. These variations ensure that no circuit is truly symmetric and degrade an oscillator's resistance to supply and substrate noise [41]. Dramatic examples of this are simulations of the differential symmetric supply noise injection circuit with mismatches introduced into one stage. The delay cell is shown in Figure 4.9 and the simulation results are found in Figure 6.1. This plot shows that small mismatches in one stage not only increase the jitter "floor" but cause substantial peaking at frequencies other than $N\omega_0$. The most sensitive component to mismatch is the NMOS current source, followed by the PMOS load transistors. The circuit, however, is quite insensitive to mismatches in the switching pair, a result repeated in the analysis of Figure 6.2(a). This plot shows the mismatch analysis done for the differential symmetric substrate noise circuit and is again sensitive to mismatches in the current source, although the jitter "floor" does not increase in this case. Mismatch analysis done on the single-ended symmetric supply noise injection circuit and shown in Figure 6.2(b) reveal that it is nearly impervious to mismatches. The conclusion of this analysis is that supply noise

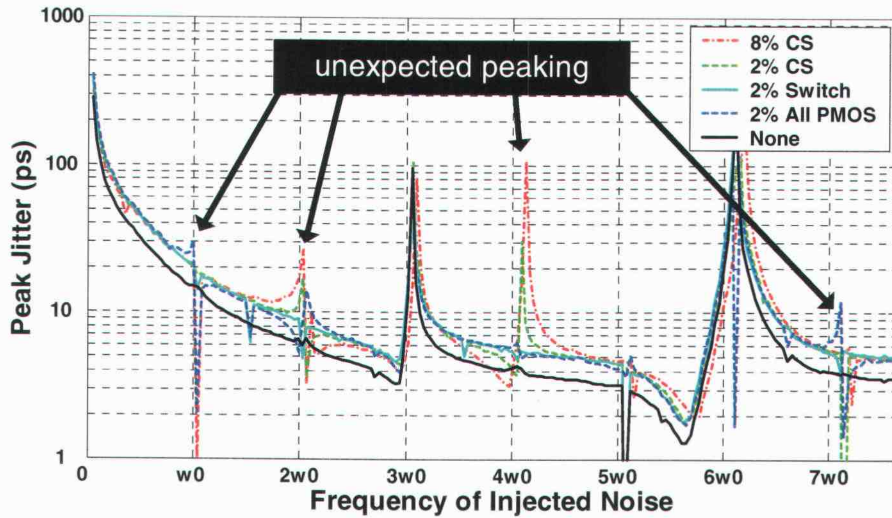
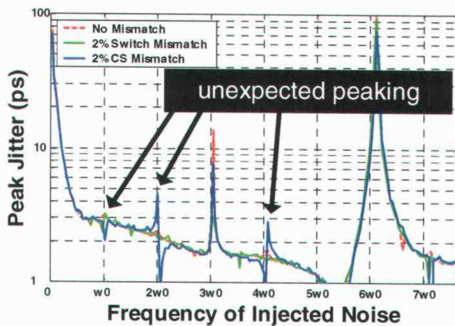
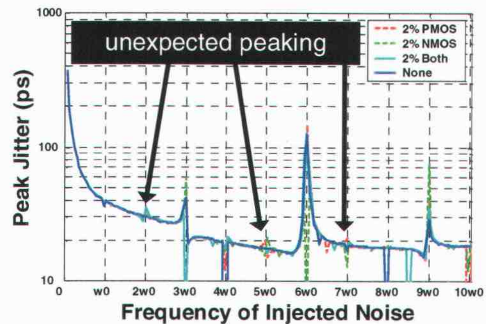


Figure 6.1 Peak jitter response of the differential symmetric supply noise injection circuit when various mismatches exist in one stage of the circuit. The mismatches simulated are increases in the width of the NMOS current source (CS), switching pair (Switch) and one load (All PMOS).



(a)



(b)

Figure 6.2 (a) Peak jitter response of the differential symmetric substrate noise injection circuit when the width of the NMOS current source (CS) and switching pair (Switch) are increased by 2% in one stage. (b) Mismatch analysis of the single-ended symmetric supply noise injection circuit when the NMOS and PMOS transistors are increased by 2% in one stage.

rejection in differential circuits is very sensitive to small component mismatches and every effort should be made to match the PMOS load transistors and the current source transistors of each stage.

6.2. Architecture Comparison and Simulation

In Chapter 5 the measurement results of symmetrically injecting supply noise into the "vanilla" differential, high-speed Maneatis load and cross-coupled load oscillators were presented. This section compares the relative performance of these architectures and presents simulated results. All results are in terms of constant jitter contours. Section 3.4 illustrated

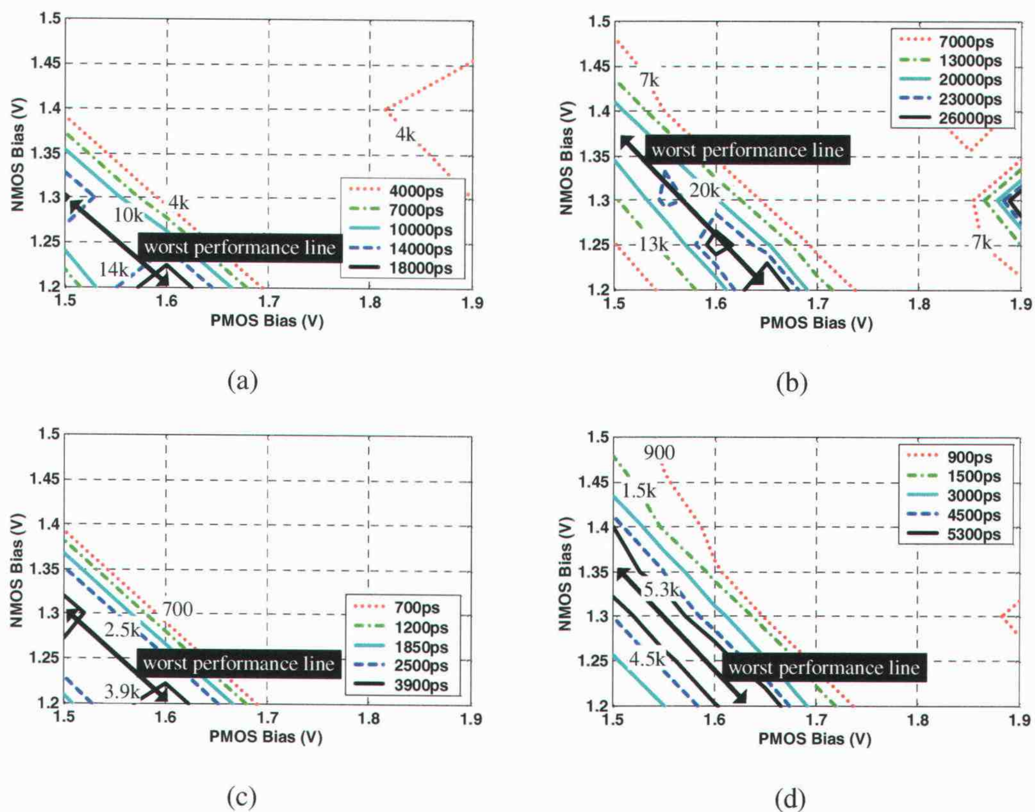


Figure 6.3 The measured peak jitter of the "vanilla" differential oscillator (a) is compared to the simulated peak jitter (b). For fair comparisons to other oscillators the measured peak jitter and the simulated peak jitter are normalized to a 1GHz oscillator in (c) and (d), respectively.

the relationship between peak jitter and the oscillation frequency. To make fair comparisons, the jitter normalization equation (3.20) from Section 3.4 is used to normalize each oscillator and bias point to a 1GHz oscillator. To de-normalize, the normalized value should be divided by the oscillation frequency, in GHz, at that point.

Figure 6.3 shows the measured and simulated results for the "vanilla" differential oscillator. Figure 6.3(a) and Figure 6.3(b) are based on 20 measurements while the corresponding plots in Figure 6.3(c) and Figure 6.3(d) are based on 80 simulations. Although there are far fewer measured data points than simulated points, it can be seen that the measurements agree strongly with the simulations, particularly after normalizing the frequency of oscillation.

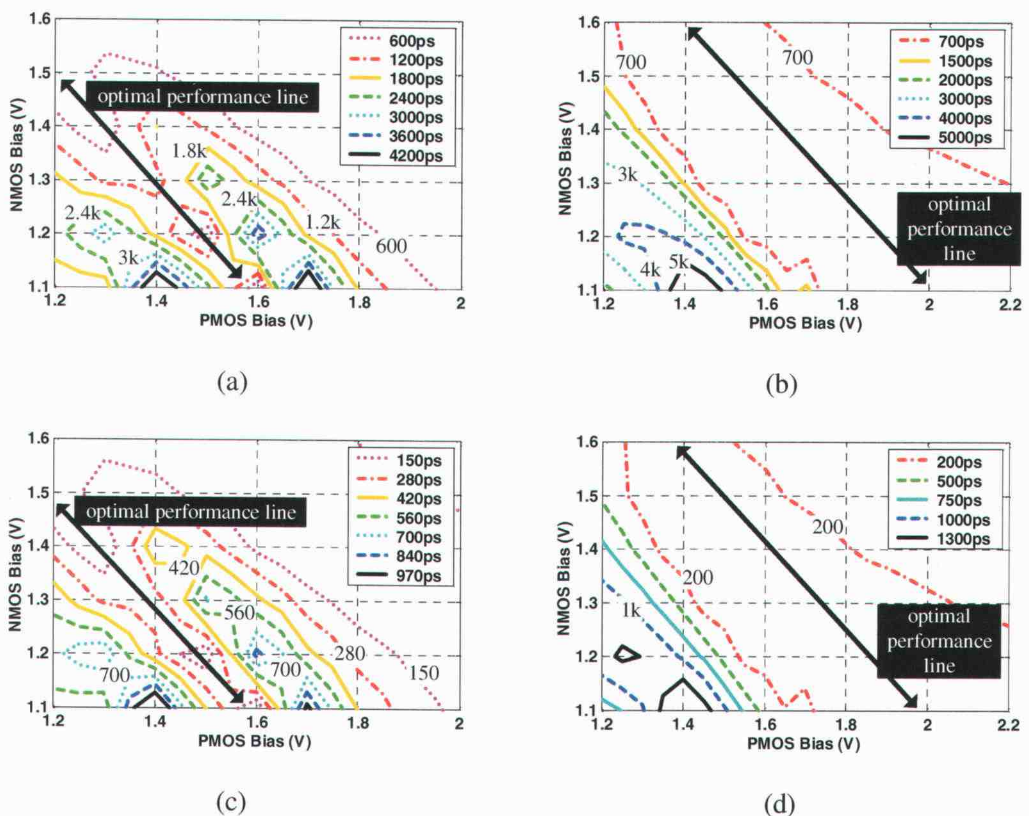


Figure 6.4 The measured peak jitter of the high-speed Maneatis load oscillator (a) is compared to the simulated peak jitter (b). For fair comparisons to other oscillators the measured peak jitter and the simulated peak jitter are normalized to a 1GHz oscillator in (c) and (d), respectively.

The results for the high-speed Maneatis load oscillator are shown in Figure 6.4 and are based on 120 measured data points and 126 simulations. The results for the measurements and simulations are quite different. Although the magnitudes are similar, the measurements have two jitter mountain ranges with a valley between while the simulations have only one. Simulations and measurements show this oscillator to be superior to the "vanilla" differential oscillator.

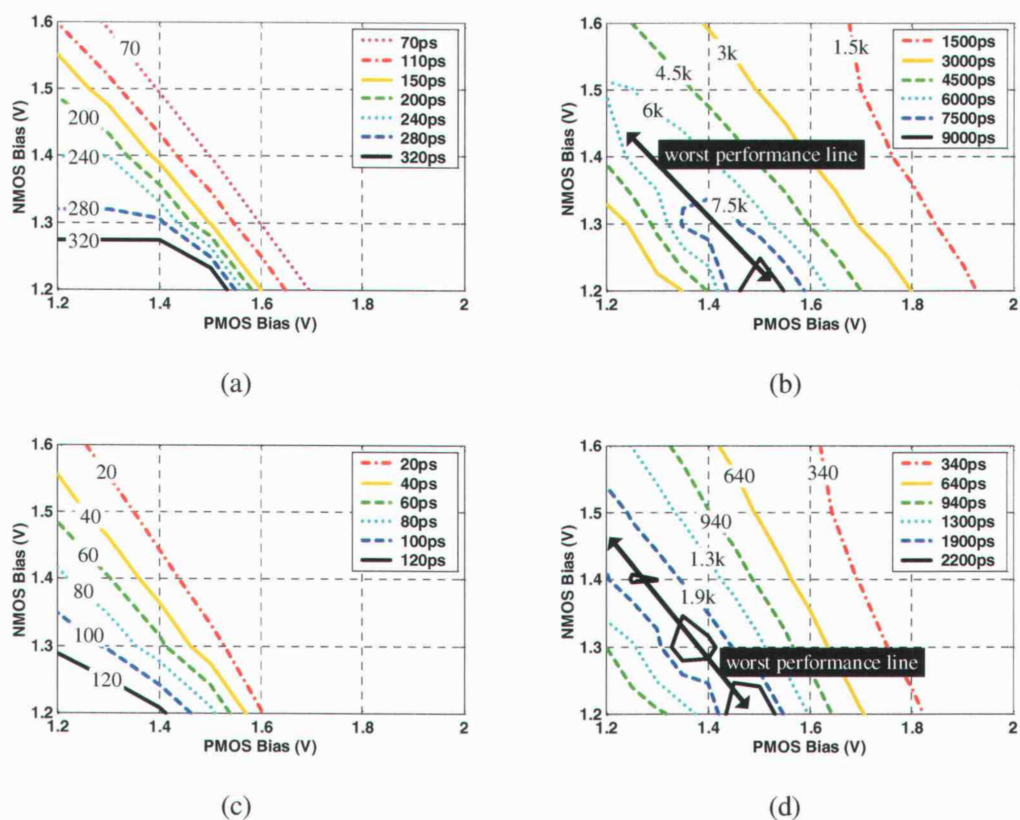


Figure 6.5 The measured peak jitter of the cross-coupled load oscillator (a) is compared to the simulated peak jitter (b). For fair comparisons to other oscillators the measured peak jitter and the simulated peak jitter are normalized to a 1GHz oscillator in (c) and (d), respectively.

In the cross-coupled oscillator, simulations and measurements show very different results. The measured data in Figure 6.5(a) show this oscillator to be extremely resistant to supply noise while the simulations in Figure 6.5(c) show the oscillator to be better than the "vanilla" differential oscillator but worse than the Maneatis load oscillator. During the measurements, the discrepancy between this oscillator and the others was noted and the test setup rechecked. However, the measurement results did not change.

All results, whether based on simulation or measurement, show distinct trends in the jitter magnitudes that can be best described as mountain ranges or valleys. A factor that influences this is the linearity of the PMOS loads [26], [27]. Mentioned previously, non-linearity in the loads can convert common-mode noise into differential-mode noise. Simulations have been performed on each oscillator for a bias point that is very sensitive to noise and a bias point that is relatively insensitive to noise. Representative results are shown in Figure 6.6, Figure 6.7 and Figure 6.8. The dashed line in these plots shows the effective resistance. Although not always true, almost all cases show that highly sensitive bias points have more non-linear PMOS load I-V characteristics than at insensitive bias points. The jitter simulation results showed the Maneatis load oscillator had the best noise rejection, followed by the cross-coupled load oscillator. Analysis of the PMOS load I-V characteristics showed the Maneatis load oscillator to had the most linear I-V characteristics, followed by the cross-coupled load oscillator. This suggests that biasing techniques to exploit load linearity should be developed.

Load impedance linearity analysis cannot be expected to fully explain the bias dependent nature of supply noise sensitivity. The dependence of oscillation frequency on supply voltage could play a significant role, and at high noise frequencies, non-linear C_{gs} capacitance can also be expected to convert common-mode noise to differential-mode noise.

6.3. Other Jitter Metrics

Absolute jitter and peak jitter consider the long term cumulative effects of noise on the zero crossings of an oscillator. It can be argued that in wide-bandwidth PLLs, this is an ill-suited metric because the PLL will tend to correct for long term frequency errors [24]. Cycle and cycle-to-cycle jitter could then be considered more meaningful metrics. While absolute jitter contains the long-term dynamics of jitter, cycle jitter also considers the short-term dynamics and cycle-to-cycle jitter depends completely on the short-term dynamics. In

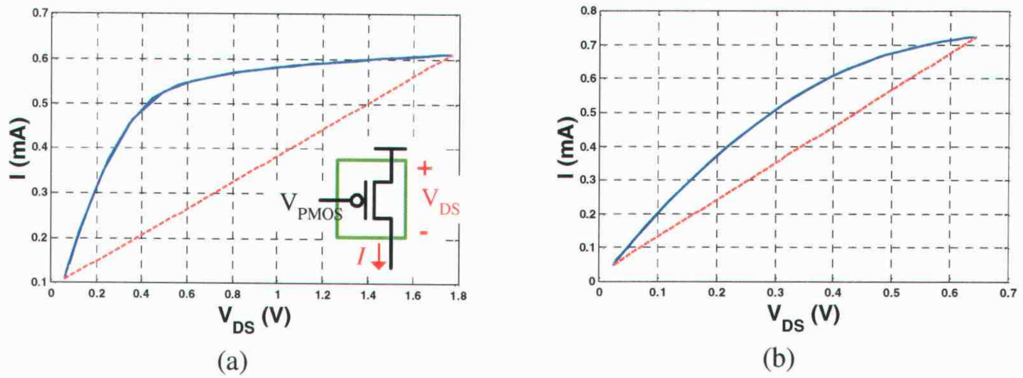


Figure 6.6 I-V characteristics of a PMOS load in the "vanilla" differential oscillator for V_{NMOS}=1.2V and (a) a noise sensitive V_{PMOS}=1.65V and (b) a noise insensitive V_{PMOS}=1.55V.

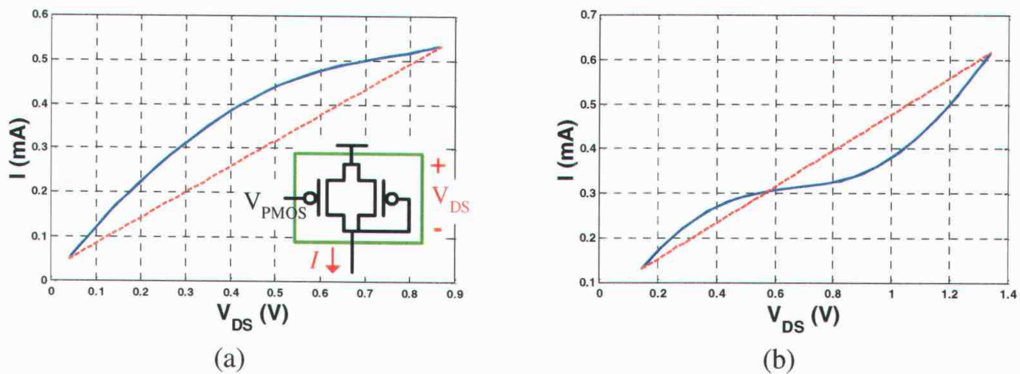


Figure 6.7 I-V characteristics of a PMOS load in the Maneatis load oscillator for V_{NMOS}=1.2V and (a) a noise sensitive V_{PMOS}=1.5V and (b) a noise insensitive V_{PMOS}=1.8V.

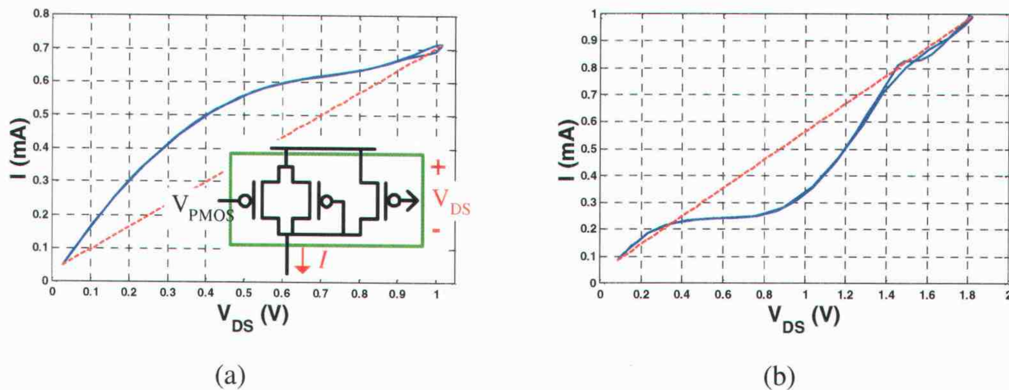
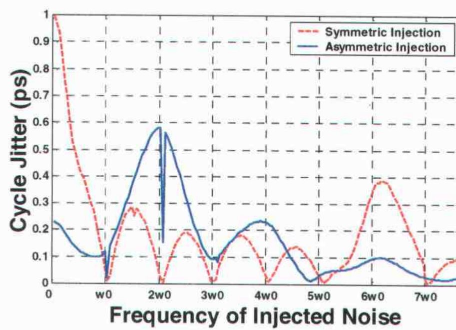
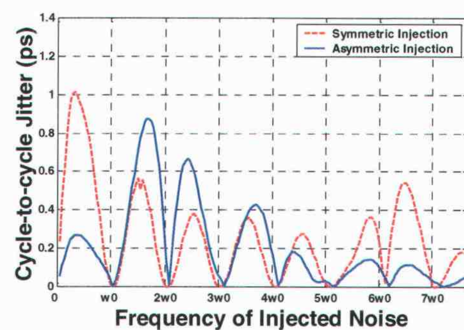


Figure 6.8 I-V characteristics of a PMOS load in the cross-coupled load oscillator for V_{NMOS}=1.1V and (a) a noise sensitive V_{PMOS}=1.4V and (b) a noise insensitive V_{PMOS}=1.6V.

addition to extracting absolute jitter from the Spectre simulations, cycle and cycle-to-cycle jitter have been extracted for both the asymmetric and symmetric differential substrate noise injection cases and the single-ended supply noise injection cases. These results are shown in Figure 6.9 and Figure 6.10, respectively. The symmetric noise injection cases have three times the injected noise power of the asymmetric cases. It can be seen from these figures that as the emphasis is placed more on the short-term dynamics, the difference between symmetric and asymmetric noise injection becomes less and less significant.

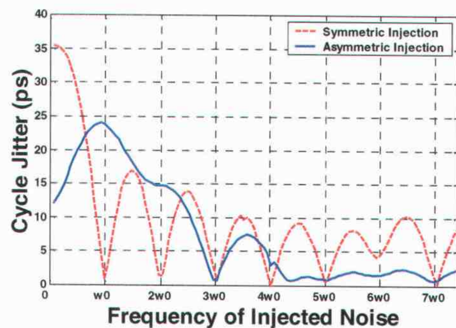


(a)

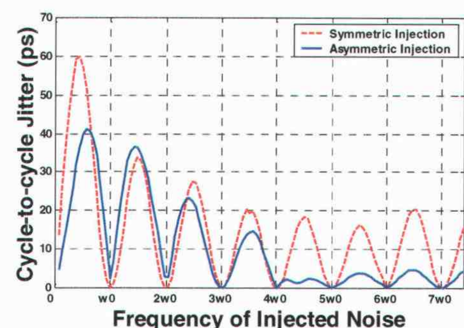


(b)

Figure 6.9 (a) Cycle jitter and (b) cycle-to-cycle jitter for substrate noise that is injected symmetrically and asymmetrically in the differential circuit. The corresponding peak jitter plots are found in Figure 5.47 and Figure 5.46.



(a)



(b)

Figure 6.10 (a) Cycle jitter and (b) cycle-to-cycle jitter for supply noise that is injected symmetrically and asymmetrically in the single-ended circuit. The corresponding peak jitter plots are found in Figure 5.45 and Figure 5.44.

7. TECHNIQUES FOR MINIMIZING PHASE NOISE AND JITTER

Chapters 2 and 3 detail methods developed to predict phase noise and jitter in ring oscillators, and these methods were rigorously verified in Chapter 5. In this chapter these simulation methods and measurements are used to develop techniques to design low phase noise differential oscillators with a high resistance to supply and substrate noise.

7.1. Choosing an Architecture and Scribe Line

Optimizing phase noise performance is a difficult task. As shown in Chapter 5, phase noise, flicker noise up-conversion and supply and substrate noise sensitivities are strong functions of an oscillator's bias "scribe" line as well as architecture selection. Many oscillators use a circuit similar to Figure 7.1(a) to allow a single current to control the oscillation frequency. By changing the current, the PMOS and NMOS bias voltage move along the scribe lines shown in Figure 7.1(b). This figure shows how the scribe lines move as the PMOS transistor width is varied. Although not all VCO circuits will have a bias circuit

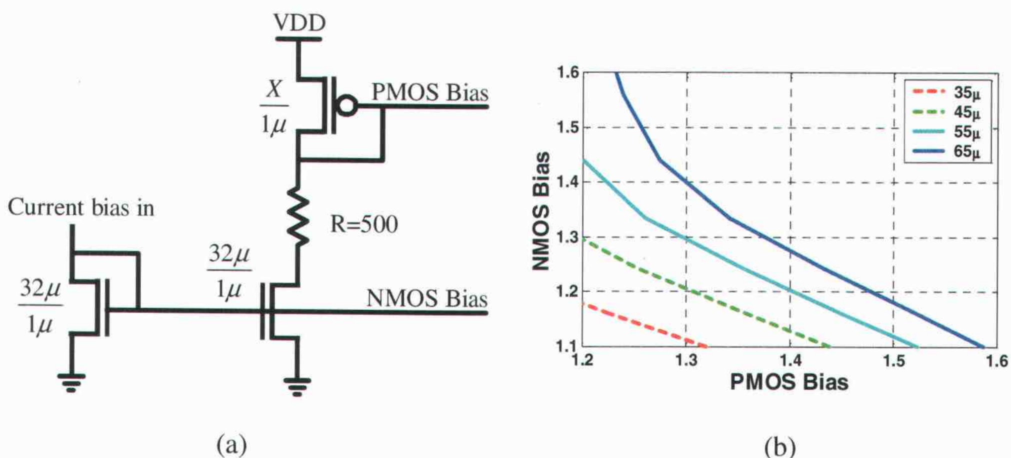


Figure 7.1 (a) A biasing scheme that allows a single current to control the oscillation frequency. (b) Bias "scribe" lines for several PMOS transistor widths as the current is changed from 0.7mA to 5mA.

like Figure 7.1(a), all VCOs will move on a scribe line. Once the architecture is selected, there are concerns other than choosing a biasing circuit and scribe line that minimizes phase noise, flicker noise up-conversion and supply and substrate noise sensitivity. In VCOs it is highly desirable to have a wide and linear VCO tuning range and yet also have a small VCO gain K_{VCO}. K_{VCO} is the incremental change in frequency caused by an incremental change in control voltage or current. High K_{VCO} values significantly amplify noise on the control line and are undesirable. Non-linear frequency tuning is undesirable because it decreases PLL stability and increases PLL lock time. Figure 7.2(a) and (b) show examples of highly non-linear frequency tuning curves. The curve in Figure 7.2(b) would not be permitted in a PLL as it contains a local minimum. If the PLL were to move to the local minimum, it would be unsure of which direction to move to increase frequency. A scribe line must not only be chosen to minimize phase noise, flicker noise up-conversion and supply and substrate noise sensitivity, it must also minimize K_{VCO} and provide linear frequency tuning. With these constraints, Figure 7.3 shows representative scribe lines permitted for the high-speed Maneatis load oscillator and the cross-coupled oscillator. Figure 7.3 shows that the cross-coupled oscillator K_{VCO} is significantly higher than for the high-speed Maneatis load oscillator, which would play a role in the architecture selection process. Using the high-speed Maneatis load oscillator and the bias circuit in Figure 7.1(a) with a PMOS width of 65μm as an example, Figure 7.4 shows that this scribe line is a good tradeoff between tuning range and linearity as well as phase noise, flicker noise up-conversion and supply and substrate noise sensitivity.

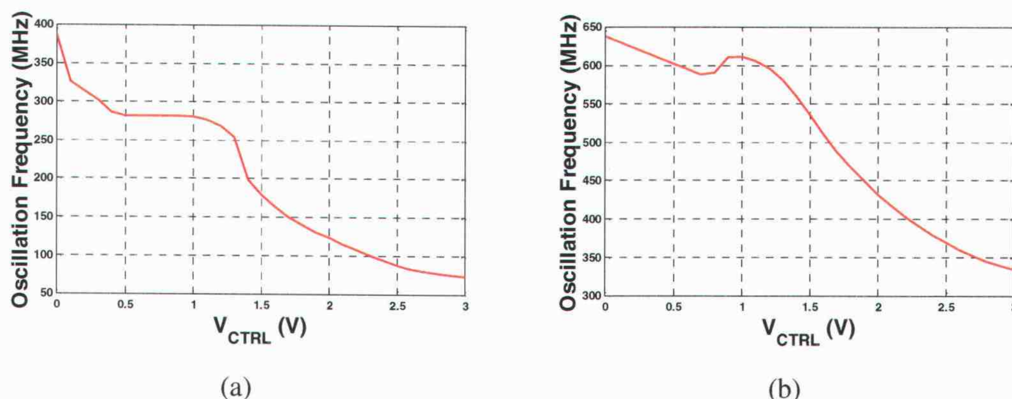
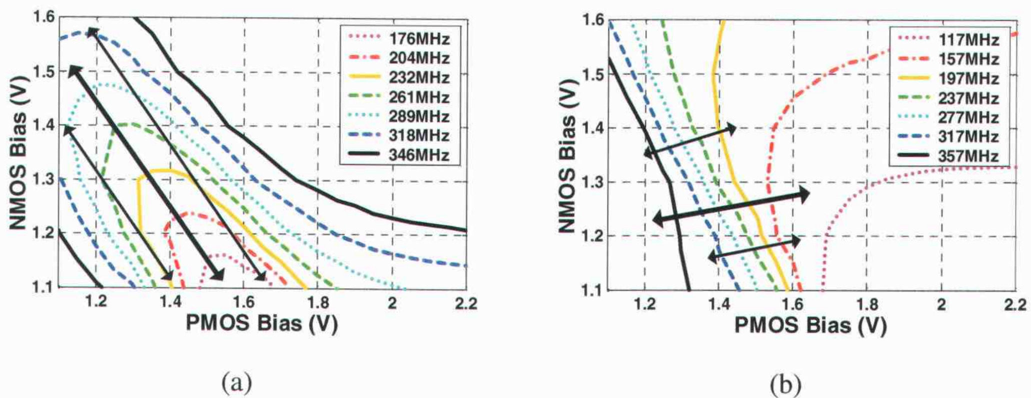
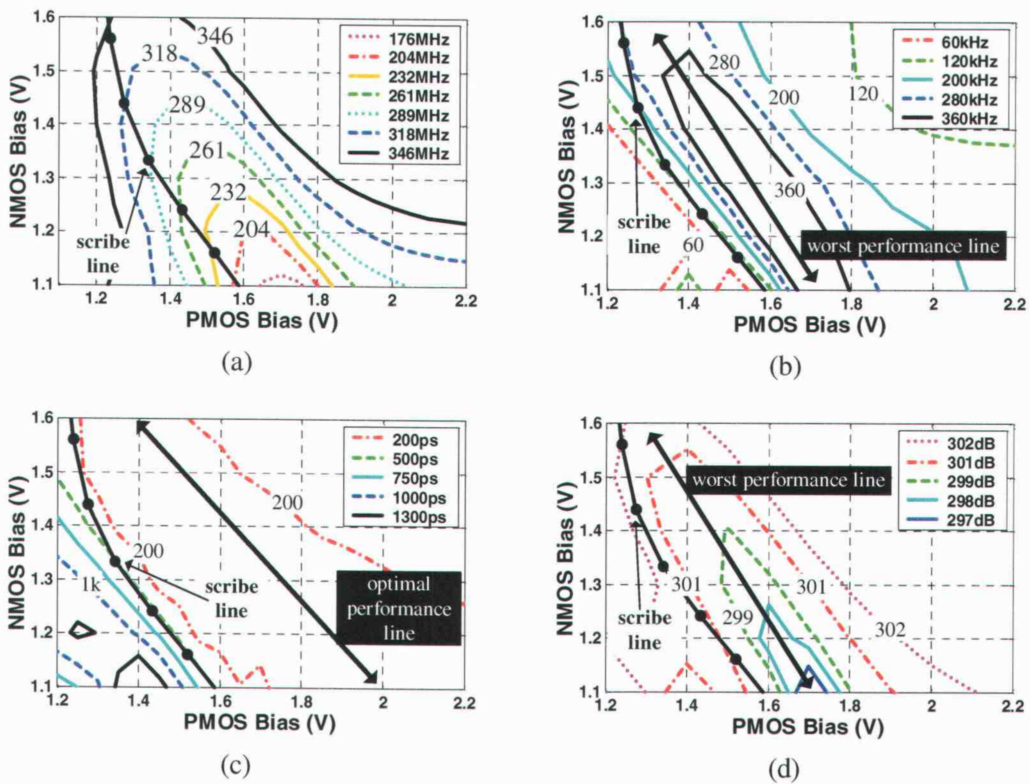


Figure 7.2 (a) The measured and (b) simulated oscillation frequency versus the control voltage of the PMOS pre-drive oscillator.



(a) (b)

Figure 7.3 The measured oscillation frequency contours for (a) the high-speed Maneatis load oscillator and (b) the cross-coupled load oscillator. Wide and linear tuning range is desirable in VCOs which constrains the bias voltages to move as shown by the arrows. The most optimal tuning characteristic is shown in bold.



(a) (b)

(c) (d)

Figure 7.4 The simulated high-speed Maneatis load oscillator (a) oscillation frequency contours, (b) flicker noise corner contours, (c) normalized supply voltage jitter sensitivity contours, and (d) 1MHz figure of merit contours over NMOS and PMOS bias.

7.2. Optimizing Transistor Widths

With initial transistor sizes and an initial scribe line chosen, it is possible to explore whether additional performance can be obtained by changing the transistor sizes. This section examines how the choice of switch width, PMOS load width and the width of the diode-connected PMOS transistor relative to the PMOS current source affects the tradeoffs between tuning range and linearity as well as phase noise, flicker noise up-conversion and supply and substrate noise sensitivity (the performance metrics). The first relationships studied are between the width of the switching pair and the performance metrics as shown in Figure 7.5. These plots show that increasing the width of the switching pair increases supply noise rejection and decreases flicker noise up-conversion. However increasing the switch width

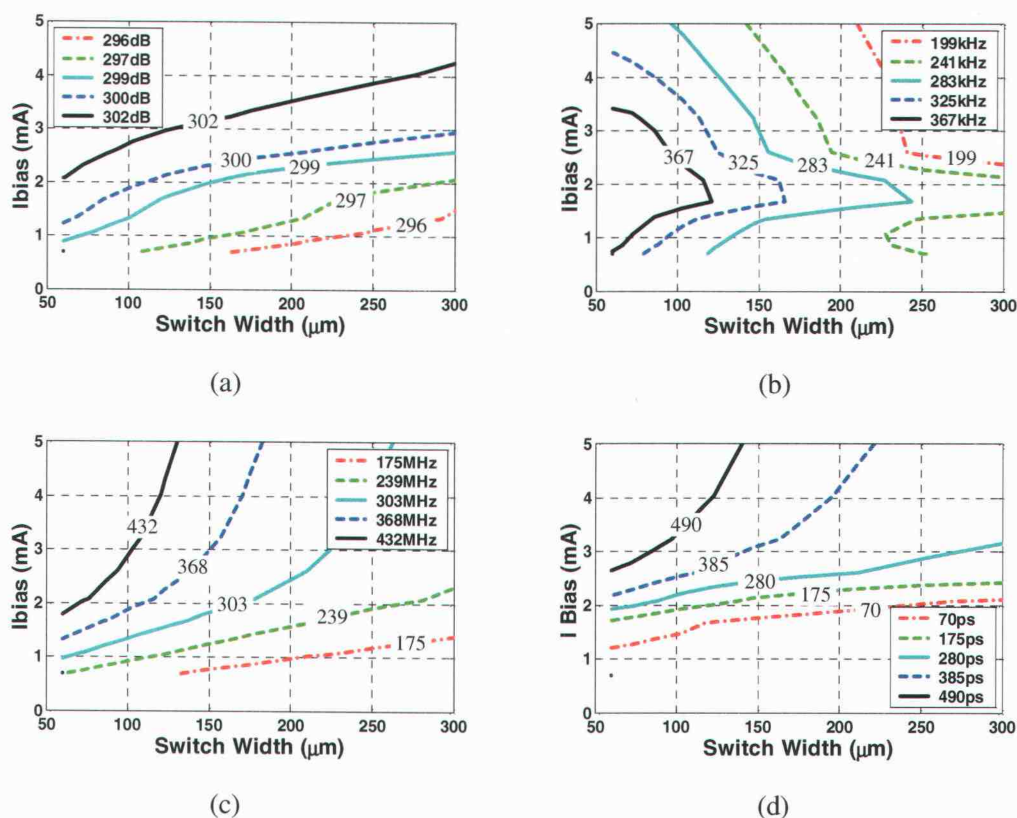


Figure 7.5 The simulated high-speed Maneatis load oscillator (a) 1MHz figure of merit contours, (b) flicker noise corner contours, (c) oscillation frequency contours and (d) supply voltage jitter sensitivity contours normalized to a 1GHz oscillator for the bias scribe line in Figure 7.4 and a sweep of the switching transistor width.

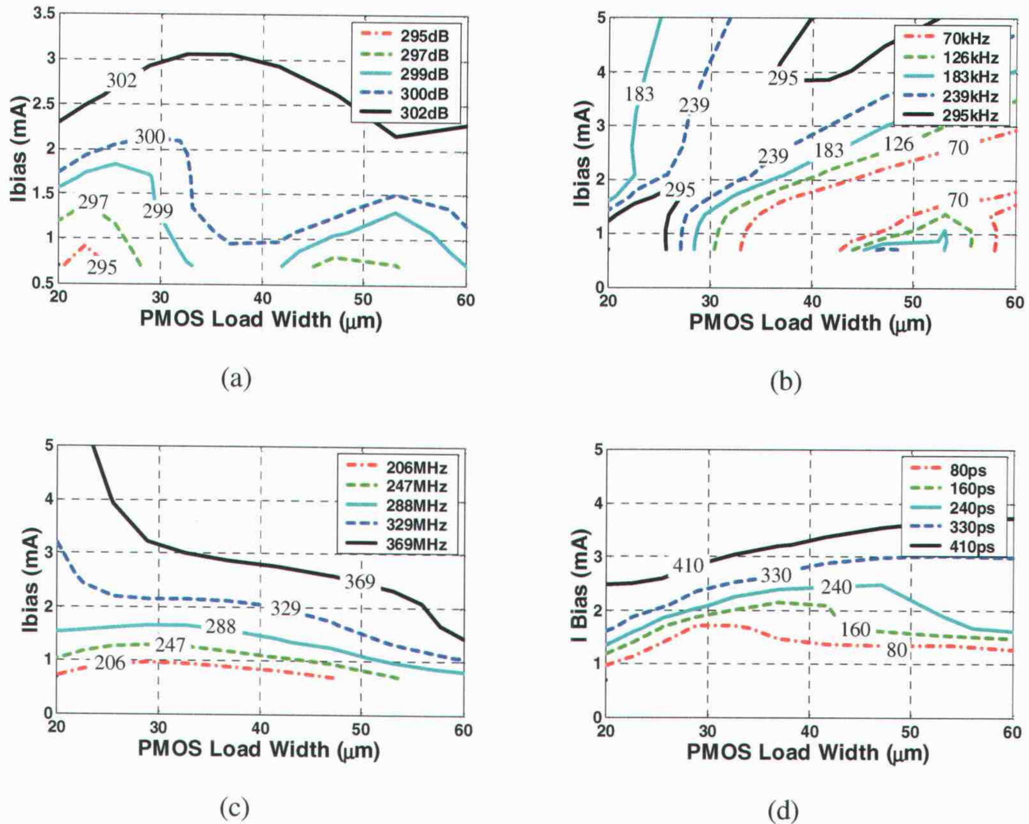


Figure 7.6 The simulated high-speed Maneatis load oscillator (a) 1MHz figure of merit contours, (b) flicker noise corner contours, (c) oscillation frequency contours and (d) supply voltage jitter sensitivity contours normalized to a 1GHz oscillator for the bias scribe line in Figure 7.4 and a sweep of the PMOS load width. The PMOS diode-connected transistor is the same width as the PMOS current source.

decreases tuning range and FOM. The relationships between the PMOS load width and the performance metrics are shown in Figure 7.6. This plots shows that all the performance metrics are generally optimized with a load width between 30μm and 40μm. The last relationships studied are those between the performance metrics and the width of the PMOS diode-connected PMOS transistor relative to the PMOS current source as shown in Figure 7.7. The width of the PMOS current source is held constant at 32μm. These plots show that decreasing the size of the diode-connected transistor increases the FOM, and minimizes flicker noise up-conversion and supply noise sensitivity. The trade off, however, is that the tuning range is drastically reduced.

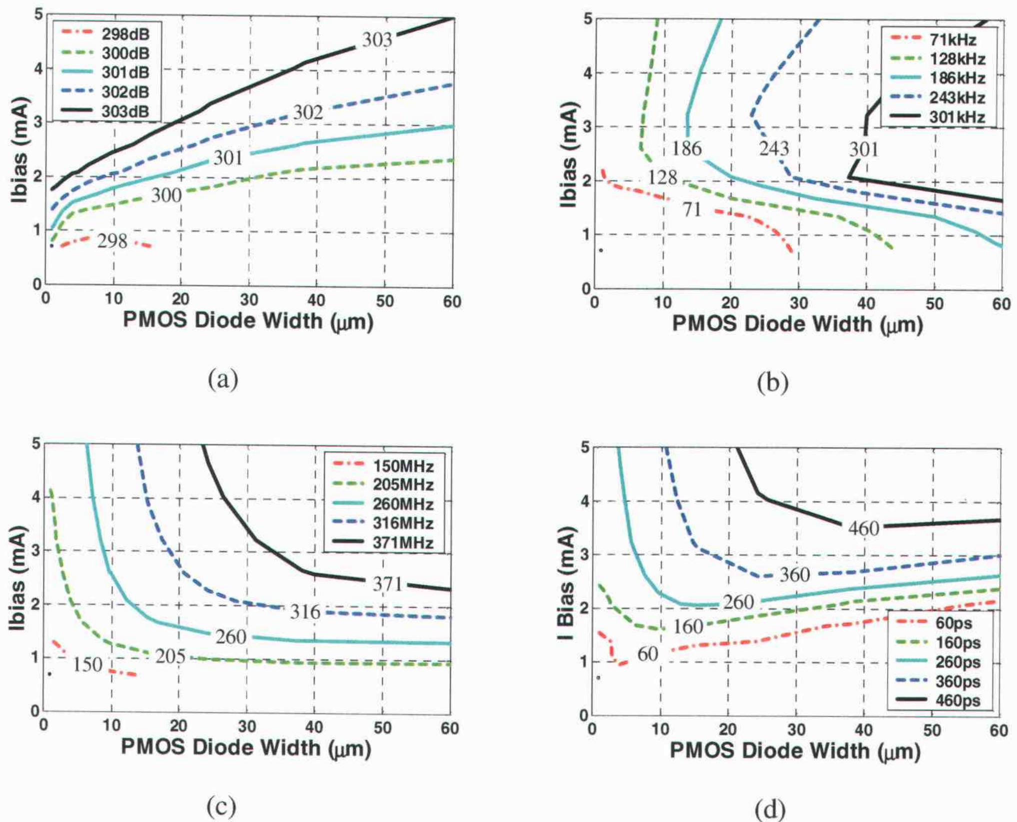


Figure 7.7 The simulated high-speed Maneatis load oscillator (a) 1MHz figure of merit contours, (b) flicker noise corner contours, (c) oscillation frequency contours and (d) supply voltage jitter sensitivity contours normalized to a 1GHz oscillator for the bias scribe line in Figure 7.4 and a sweep of the PMOS diode-connected transistor width. The PMOS current source width is fixed at 32μm.

7.3. Further Circuit Optimization

The preceding sections showed the process of picking an architecture and simulating the performance metrics over all possible bias conditions. From this an initial bias scribe line can be chosen. Additional performance was obtained by studying the relationship between circuit elements and the performance metrics for the chosen scribe line. The next step would be to repeat the process of simulating performance metrics over all possible bias conditions for the new circuit, choosing a new scribe line, and again studying the relationship between circuit elements and the performance metrics for the new scribe line.

8. CONCLUSIONS

This thesis has presented two distinctly different methods of accurately predicting phase noise in ring oscillators: the commercially available SpectreRF and *isf_tool*, a simulator developed in this work from the Hajimiri and Lee theory of phase noise. The results of each approach have been compared with over 2500 phase noise measurements from 10 oscillators and 5 architectures. It was shown that both the *isf_tool* and SpectreRF can be used to accurately predict phase noise in the white noise region, and while neither method consistently predicted the measured flicker noise corners, both captured the flicker noise corner trends. The simulator *isf_tool* was more consistent in predicting phase noise than SpectreRF.

This thesis also studied jitter due to deterministic noise sources and a new jitter metric, peak jitter, was developed to characterize absolute jitter caused by deterministic noise sources. It was shown that ring oscillator circuits respond differently to deterministic noise that is injected symmetrically versus noise that is injected asymmetrically. Asymmetrically injected noise significantly increases absolute jitter at dc and integer multiples of ω_0, while symmetrically injected noise only significantly increases absolute jitter at dc and integer multiples of $N\omega_0$, where N is the number of stages in the ring oscillator. This was shown with Spectre time domain simulations and equations developed to predict absolute jitter due to deterministic noise injected symmetrically and asymmetrically. The simulations and equations were validated with 982 absolute jitter measurements performed on eight single-ended and differential ring oscillator circuits. The equations developed can predict the absolute jitter due to a sinusoidal noise source at any frequency. Absolute jitter considers the long term oscillator jitter dynamics. Spectre simulations show that as the emphasis is placed more on the short-term dynamics, the difference between symmetric and asymmetric noise injection becomes less and less significant

This work has measured the relative phase noise and jitter performance of the different architectures. In a result that may initially appear surprising, the best architecture for phase noise performance is the simple, single-ended architecture, followed closely by the simulated results of the PMOS pre-drive oscillator. Analysis shows that less than rail-to-rail voltage swing oscillators loose a significant portion of their power to short circuit current. These architectures, however, have serious drawbacks for PLL applications when their frequency

tuning characteristics are examined, and of the three architectures examined with more linear frequency tuning characteristics, it was shown that the cross-coupled oscillator had slightly superior phase noise performance compared to the Maneatis load oscillator and significantly better flicker noise up-conversion performance. The "vanilla" differential oscillator was shown to have good phase noise performance but an inadequate tuning range. Jitter measurements and simulations performed on these three architectures over a sweep of bias revealed that sensitivity to supply and substrate noise in differential circuits is heavily bias dependent. It was shown in simulation that the Maneatis load oscillator had generally superior supply noise rejection compared with the cross-coupled load oscillator although in measurements the cross-coupled load oscillator had dramatically better performance. A possible reason why the Maneatis load oscillator was superior in simulations is due to its generally lower K_{VCO} compared to the cross-coupled load oscillator. The "vanilla" differential oscillator had the poorest performance.

Analysis and measurements performed in this work contradict conclusions drawn from the work of others. It is commonly believed that flicker noise up-conversion will be minimized if the oscillator voltage rise and fall times are symmetric. However, measurements, theory and simulations from SpectreRF and *isf_tool* all agree that flicker noise up-conversion in cyclostationary noise processes is generally not minimized by symmetric ISFs, and thus is not minimized by symmetric rise and fall times. Cyclostationary noise processes describe nearly all practical oscillators. Additionally, measurements show that extraneous deterministic noise that couples into the oscillator appears as discrete tones in the phase noise spectrum and does not affect the phase noise at other offsets. Lastly, the results show that differential architectures are not necessarily more resistant to supply and substrate noise than single-ended architectures.

This project included elements of noise modeling and circuit design and is a first step in a difficult subject. More work must be done in both areas to develop better methods to predict flicker noise up-conversion, reduce sensitivity to supply and substrate noise, exploit jitter and phase noise bias dependence, and develop better ring oscillator architectures. Future work should include obtaining the BSIM3 flicker noise parameters and comparing the results of simulations from this model with measurements. Future test chips should include transistors that can be characterized for flicker noise and are representative of transistor sizes in the oscillator designs. The bias dependent nature of both phase noise and jitter should be studied.

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APPENDICES

APPENDIX A. Removing q_{max} from H&L's phase noise equation

Phase noise in the white noise region is given by

$$L\{\Delta\omega\}=10\cdot\log_{10}\left(\frac{\Gamma_{rms}^2}{q_{\max}^2}\cdot\frac{\overline{i_n^2}/\Delta f}{2\cdot\Delta\omega^2}\right). \tag{A1}$$

The impulse sensitivity function (ISF) Γ_{rms} used in this equation is a scaled version of the phase shift due to injecting a charge q_{inj} into an oscillator. The unscaled ISF is calculated by injecting a charge q_{inj} into an oscillator at time t and measuring the resulting phase shift $\Delta\phi(t)$. The unscaled ISF $\tilde{\Gamma}$ is

$$\tilde{\Gamma}(t)=\frac{2\pi\cdot\Delta\phi(t)}{T} \tag{A2}$$

where T is the period of the oscillation. The scaled ISF is

$$\Gamma_{rms}=\left(\frac{q_{\max}}{q_{inj}}\right)\cdot\tilde{\Gamma}_{rms} \tag{A3}$$

where q_{max} is the maximum charge displacement at the injection node. Substituting (A3) into (A1) and canceling q_{max}

$$L\{\Delta\omega\}=10\cdot\log_{10}\left(\frac{\frac{q_{\max}^2}{q_{inj}^2}\tilde{\Gamma}_{rms}^2}{q_{\max}^2}\cdot\frac{\overline{i_n^2}/\Delta\omega}{2\cdot\omega^2}\right) \tag{A4}$$

results in (A5), an equation for phase noise in the white noise region that is independent of q_{max}.

$$L\{\Delta\omega\}=10\cdot\log_{10}\left(\frac{\tilde{\Gamma}_{rms}^2}{q_{inj}^2}\cdot\frac{\overline{i_n^2}/\Delta\omega}{2\cdot\omega^2}\right) \tag{A5}$$

APPENDIX B. Simplifying (2.27)

Equation (2.27), which is the same as (B1),

$$\phi(t)=\frac{1}{q_{\max}}\int_{-\infty}^{t} i(\tau)\left[\sum_{n=0}^{N-1}\Gamma\left(\omega_0\tau+\frac{2\pi n}{N}\right)\right]d\tau \tag{B1}$$

can be expanded by recalling the Fourier expansion for the ISF is given by

$$\Gamma(\omega_0\tau)=\frac{c_0}{2}+\sum_{n=1}^{\infty}c_n\cos(n\omega_0\tau+\theta). \tag{B2}$$

Inserting (B2) into (B1) gives

$$\phi(t)=\frac{1}{q_{\max}}\int_{-\infty}^{t} i(t)\sum_{k=0}^{N-1}\left(\frac{c_0}{2}+\sum_{n=1}^{\infty}c_n\cos\left(n\omega_0\tau+\frac{2\pi nk}{N}\right)\right)d\tau. \tag{B3}$$

Summation from $k=0 \rightarrow N-1$ for the constant term will result in a multiplication by N. The order of the two summations can be changed for the cosine term

$$\phi(t)=\frac{Nc_0}{2q_{\max}}\int_{-\infty}^{t} i(\tau)\,d\tau+\frac{1}{q_{\max}}\int_{-\infty}^{t} i(\tau)\sum_{n=1}^{\infty}\sum_{k=0}^{N-1}c_n\cos\left(n\omega_0\tau+\frac{2\pi nk}{N}\right)d\tau. \tag{B4}$$

In order to do the summation the cosine term can be expressed in terms of exponentials

$$\phi(t)=\frac{Nc_0}{2q_{\max}}\int_{-\infty}^{t} i(\tau)\,d\tau+\frac{1}{q_{\max}}\int_{-\infty}^{t} i(\tau)\sum_{n=1}^{\infty}\sum_{k=0}^{N-1}c_n\left(\frac{e^{j\left(n\omega_0\tau+\frac{2\pi nk}{N}\right)}+e^{-j\left(n\omega_0\tau+\frac{2\pi nk}{N}\right)}}{2}\right)d\tau. \tag{B5}$$

Let x represent the first summation

$$x=\sum_{k=0}^{N-1}c_n\left(\frac{e^{j\left(n\omega_0\tau+\frac{2\pi nk}{N}\right)}+e^{-j\left(n\omega_0\tau+\frac{2\pi nk}{N}\right)}}{2}\right). \tag{B6}$$

The two exponentials can be put into separate summations

$$x=\frac{1}{2}e^{jn\omega_0\tau}\sum_{k=0}^{N-1}e^{j\frac{2\pi nk}{N}}+\frac{1}{2}e^{-jn\omega_0\tau}\sum_{k=0}^{N-1}e^{-j\frac{2\pi nk}{N}}. \tag{B7}$$

It is known that

$$\sum_{n=0}^{N-1}\alpha^m=\frac{1-\alpha^N}{1-\alpha}\ \text{for}\ 1\geq|\alpha|. \tag{B8}$$

By using (B8), x can be rewritten as

$$x=\frac{e^{jn\omega_0\tau}}{2}\cdot\frac{1-e^{j2\pi n}}{1-e^{j\frac{2\pi n}{N}}}+\frac{e^{-jn\omega_0\tau}}{2}\cdot\frac{1-e^{-j2\pi n}}{1-e^{-j\frac{2\pi n}{N}}}. \qquad \text{(B9)}$$

Since $e^{\pm j2\pi n}=1$ for all integer vales of n, numerators in (B9) and therefore x will always be zero, except for when n equals an integer multiple of N. In this case there is a $0/0$ division and L'Hopital's rule can be used to find the limit

$$\frac{\mp j2\pi e^{\pm j2\pi n}}{\mp j\frac{2\pi}{N}e^{\pm j\frac{2\pi n}{N}}}=N. \qquad \text{(B10)}$$

This result means that for integer multiples of N,

$$x=\frac{Ne^{jnN\omega_0\tau}}{2}+\frac{Ne^{-jnN\omega_0\tau}}{2}=N\cos\left(nN\omega_0\tau\right) \qquad \text{(B11)}$$

By substituting x into (B5), a simplified equation for the excess phase $\phi(t)$ is

$$\phi(t)=\frac{Nc_0}{2q_{\max}}\int_{-\infty}^{t}i(\tau)\,d\tau+\frac{1}{q_{\max}}\int_{-\infty}^{t}i(\tau)\sum_{n=1}^{\infty}c_{Nn}\cos\left(nN\omega_0\tau\right)d\tau. \qquad \text{(B12)}$$

The order of the integration and the summation in (B12) can be changed so that

$$\phi(t)=\frac{N\,c_0}{2q_{\max}}\int_{-\infty}^{t}i(\tau)\,d\tau+\frac{N}{q_{\max}}\sum_{n=1}^{\infty}c_{Nn}\left(\int_{-\infty}^{t}i(\tau)\cos\left(nN\omega_0\tau\right)d\tau\right). \qquad \text{(B13)}$$

APPENDIX C Differential supply noise injection circuit die photos

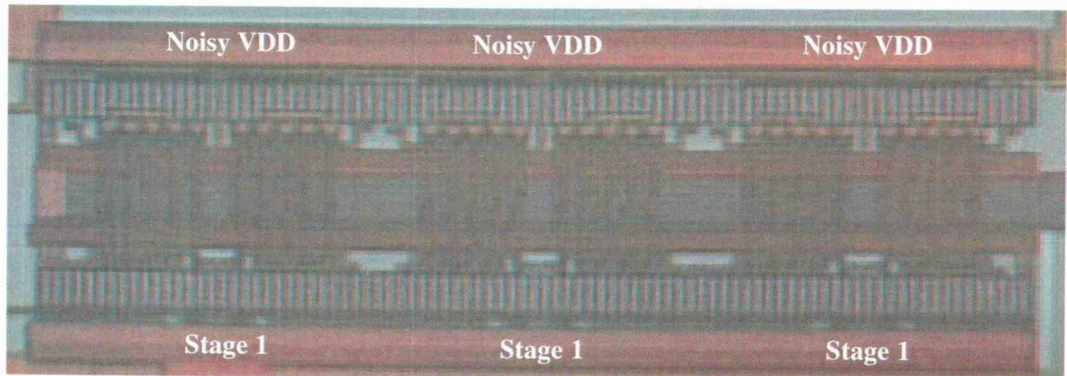


Figure C.1 Differential symmetric supply noise injection.

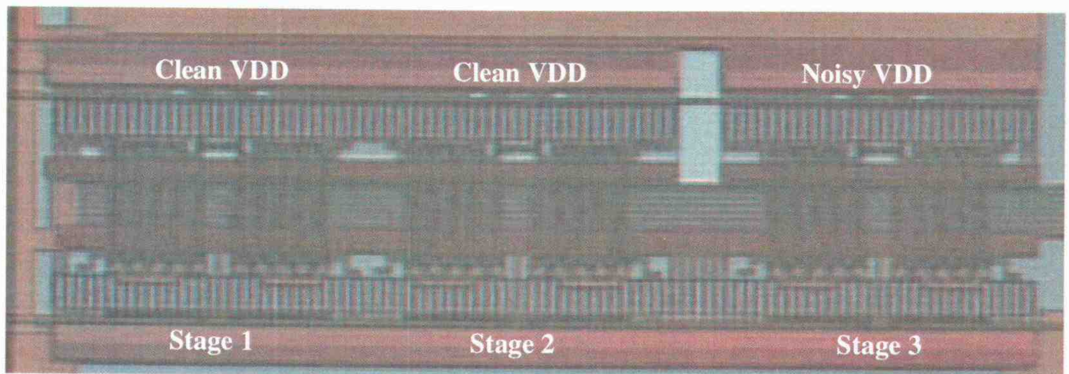
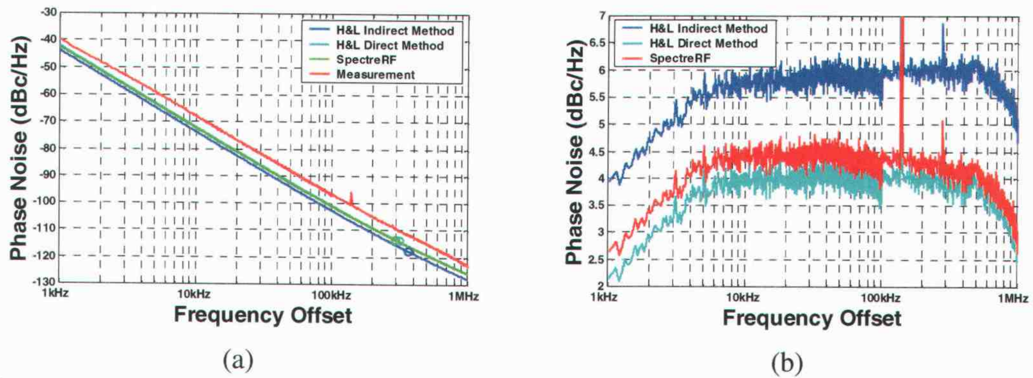


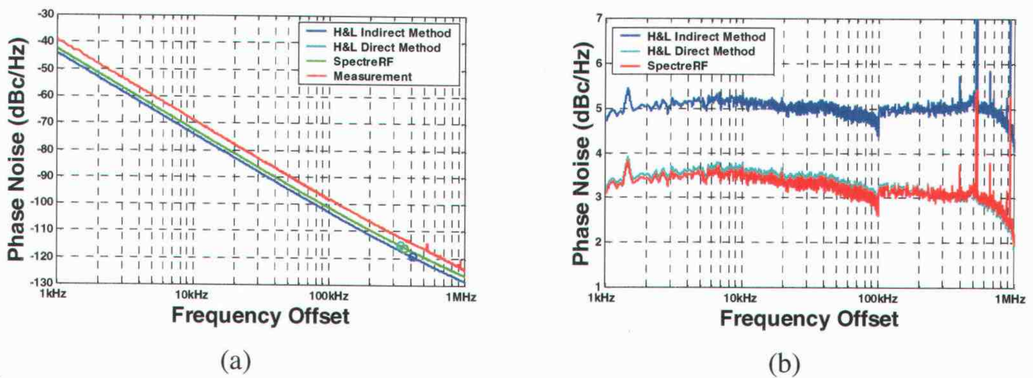
Figure C.2 Differential asymmetric supply noise injection.

APPENDIX D H&L series simulations versus measurements



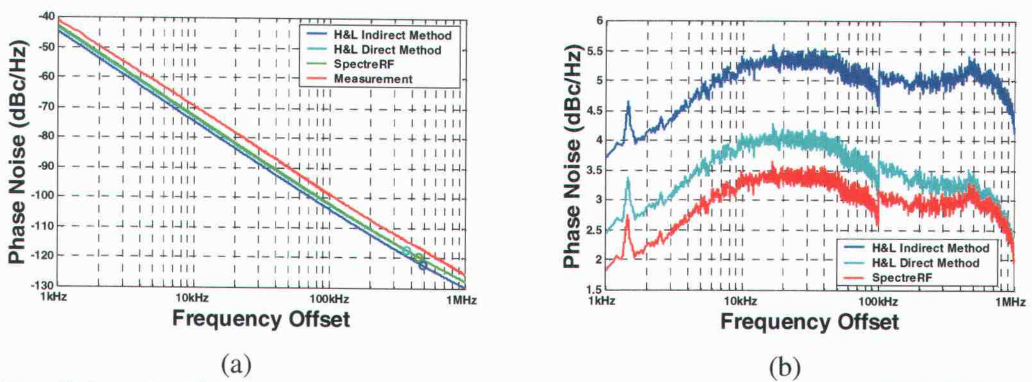
(a) (b)

Figure D.1 (a) Phase noise performance and (b) error of the HL1 oscillator, VDD=2.0V.



(a) (b)

Figure D.2 (a) Phase noise performance and (b) error of the HL1 oscillator, VDD=2.5V.



(a) (b)

Figure D.3 (a) Phase noise performance and (b) error of the HL1 oscillator, VDD=3.5V.

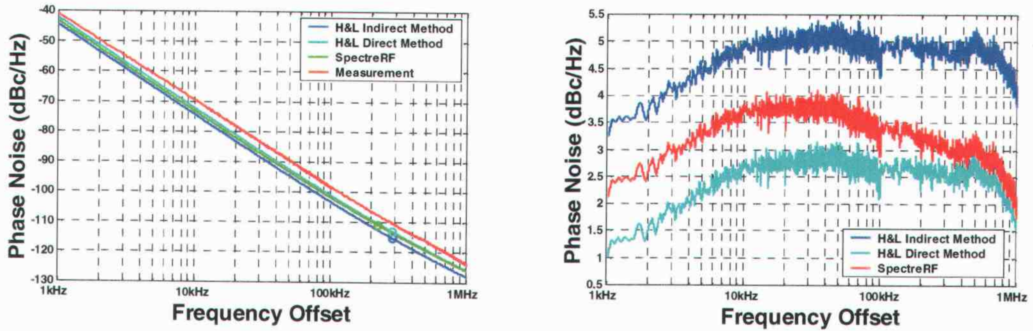
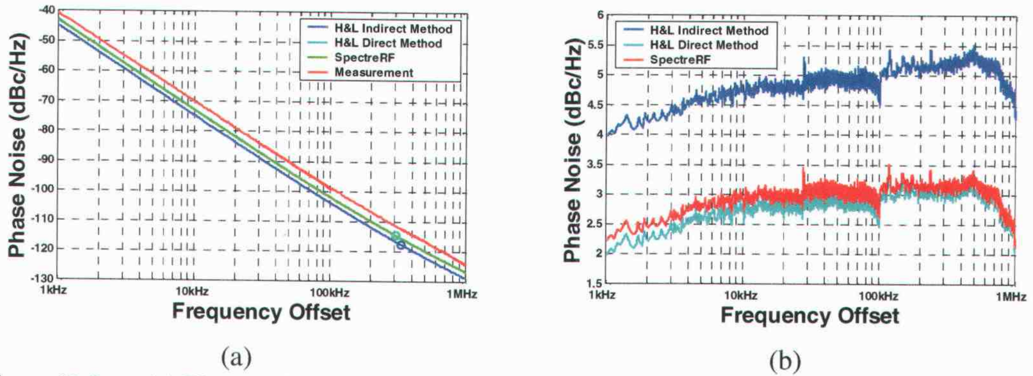
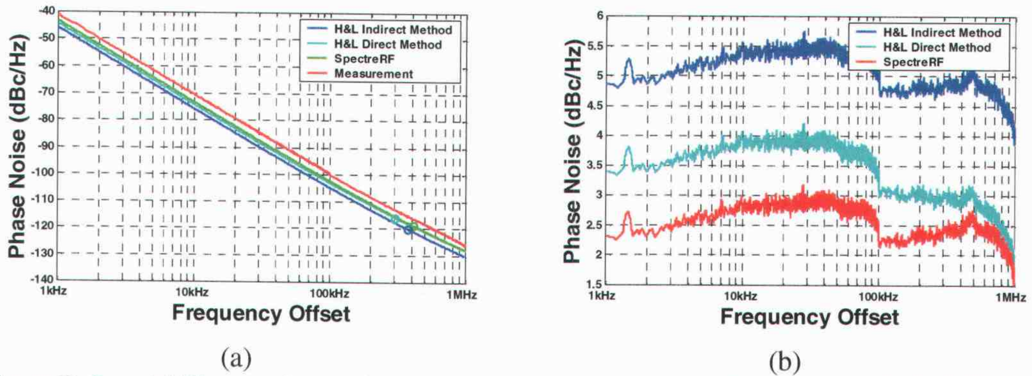


Figure D.4 (a) Phase noise performance and (b) error of the HL2 oscillator, VDD=2.0V.



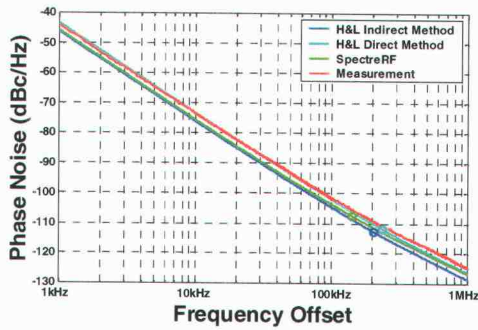
(a) (b)

Figure D.5 (a) Phase noise performance and (b) error of the HL2 oscillator, VDD=2.5V.

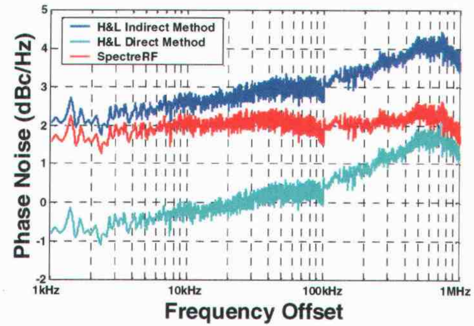


(a) (b)

Figure D.6 (a) Phase noise performance and (b) error of the HL2 oscillator, VDD=3.5V.

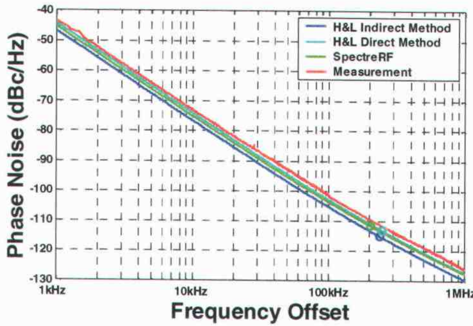


(a)

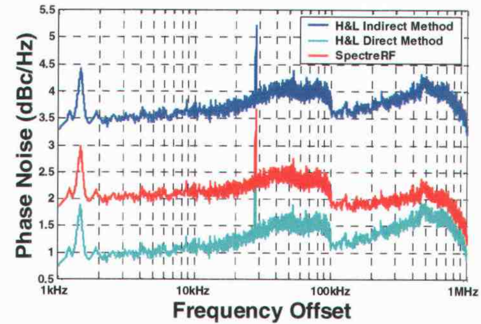


(b)

Figure D.7 (a) Phase noise performance and (b) error of the HL3 oscillator, VDD=2.0V.

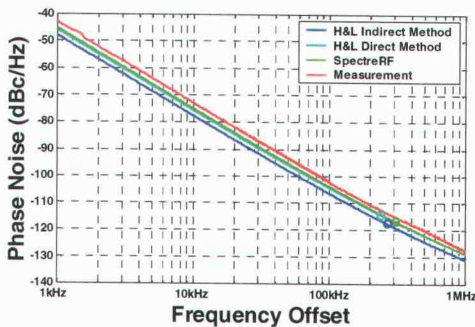


(a)

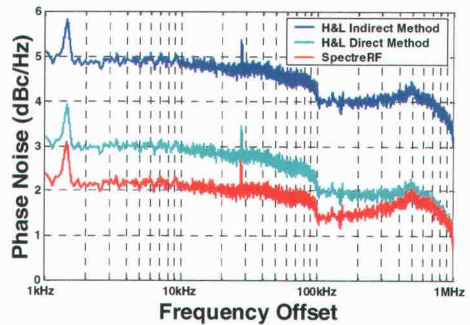


(b)

Figure D.8 (a) Phase noise performance and (b) error of the HL3 oscillator, VDD=2.5V.



(a)



(b)

Figure D.9 (a) Phase noise performance and (b) error of the HL3 oscillator, VDD=3.5V.

APPENDIX E Results for the "vanilla" differential oscillator

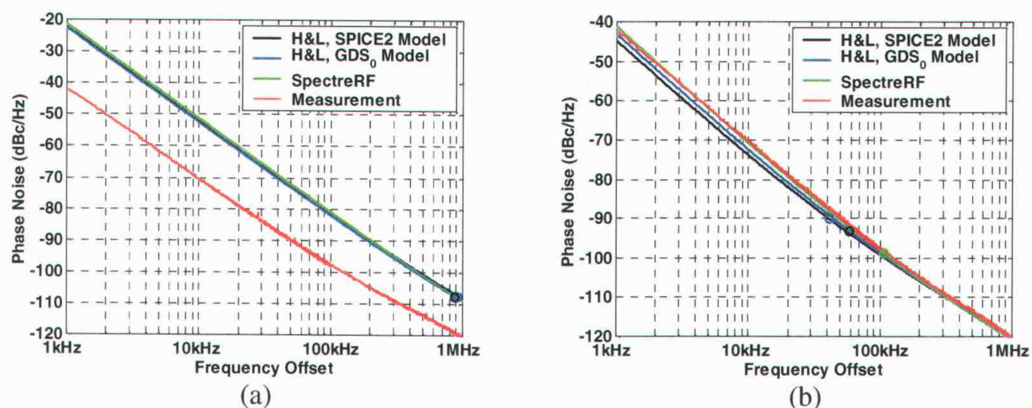


Figure E.1 Measurements versus simulations for (a) V_{PMOS}=1.5V and V_{NMOS}=1.4V and (b) V_{PMOS}=1.6V and V_{NMOS}=1.4V.

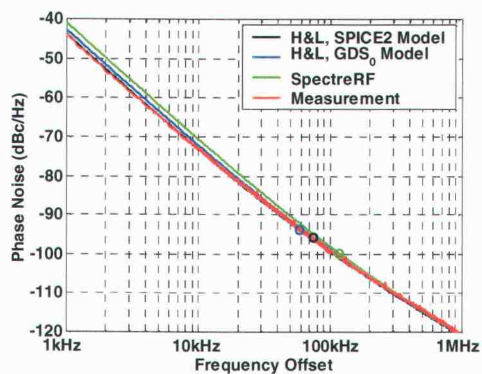


Figure E.2 Measurements versus simulations for V_{PMOS}=1.7V and V_{NMOS}=1.4V.

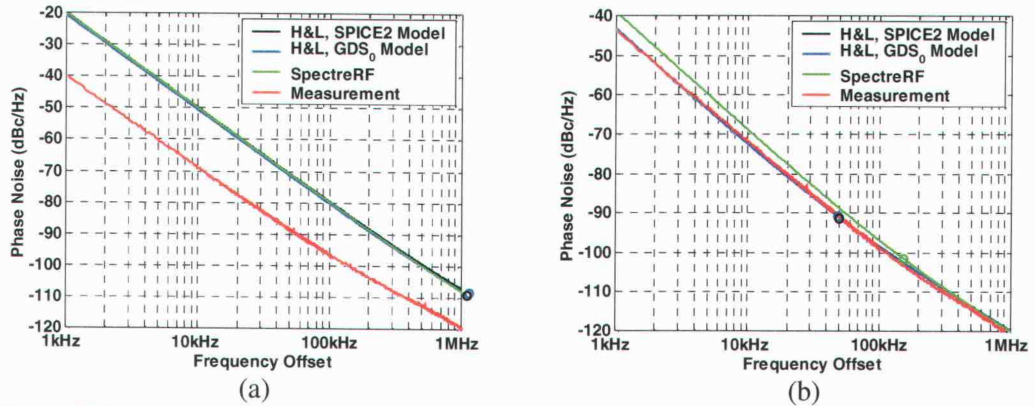


Figure E.1 Measurements versus simulations for (a) V_{PMOS}=1.4V and V_{NMOS}=1.5V and (b) V_{PMOS}=1.5V and V_{NMOS}=1.5V.

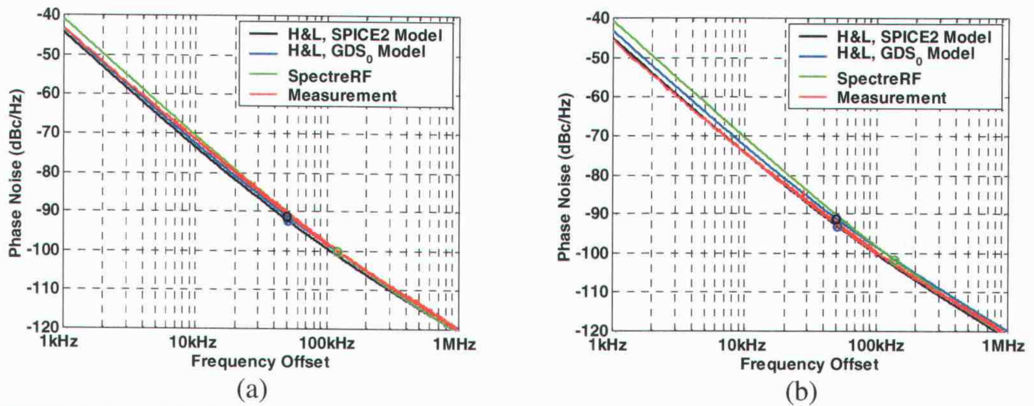
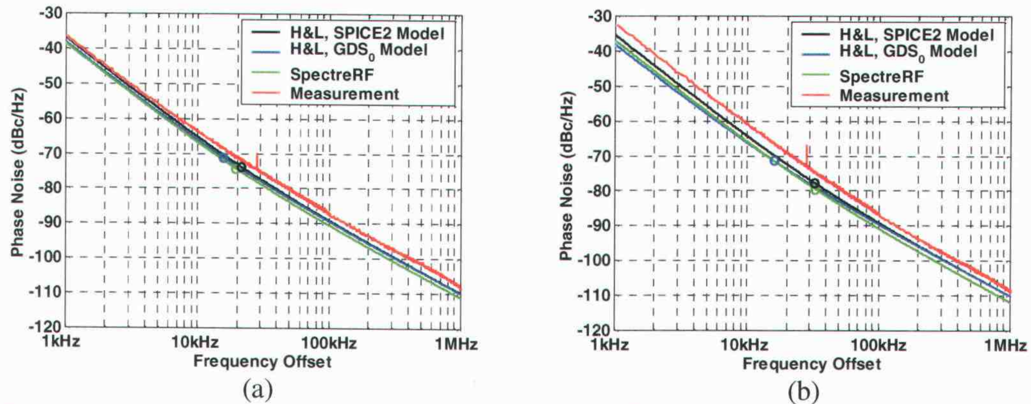


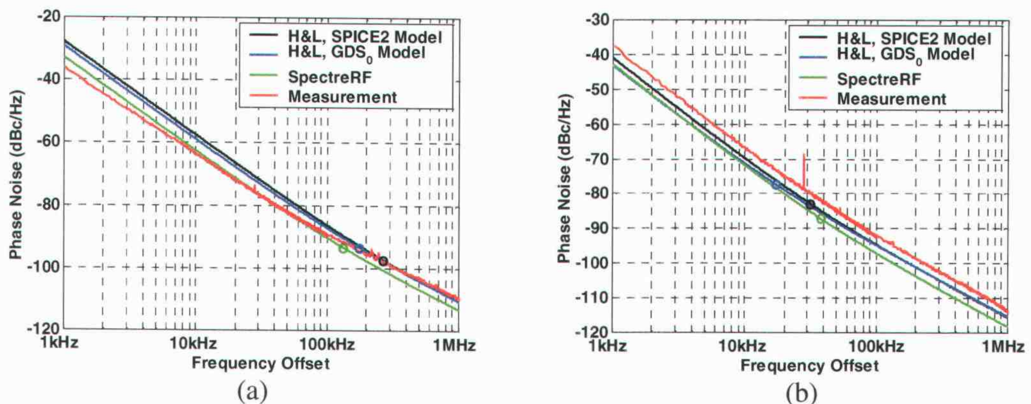
Figure E.2 Measurements versus simulations for (a) V_{PMOS}=1.6V and V_{NMOS}=1.5V and (b) V_{PMOS}=1.7V and V_{NMOS}=1.5V.

APPENDIX F Results for the high speed Maneatis load differential oscillator



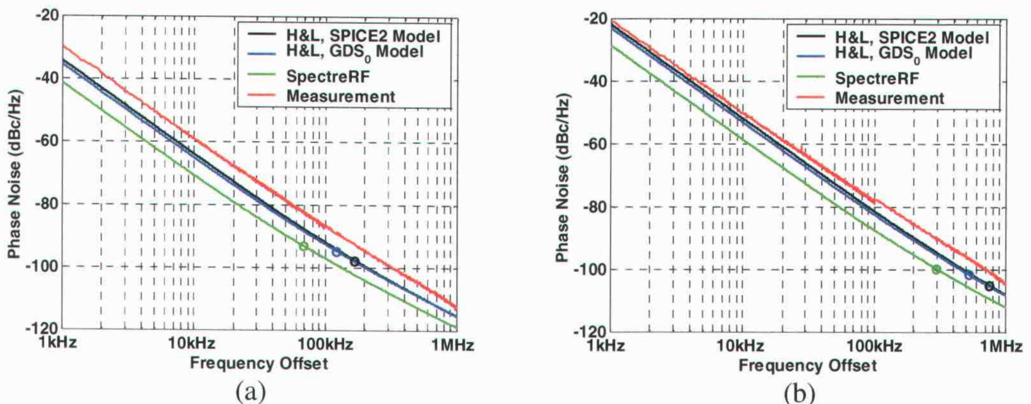
(a) (b)

Figure F.1 Measurements versus simulations for (a) V_{PMOS}=1.2V and V_{NMOS}=1.1V and (b) V_{PMOS}=1.3V and V_{NMOS}=1.1V.



(a) (b)

Figure F.2 Measurements versus simulations for (a) V_{PMOS}=1.4V and V_{NMOS}=1.1V and (b) V_{PMOS}=1.5V and V_{NMOS}=1.1V.



(a) (b)

Figure F.3 Measurements versus simulations for (a) V_{PMOS}=1.6V and V_{NMOS}=1.1V and (b) V_{PMOS}=1.7V and V_{NMOS}=1.1V.

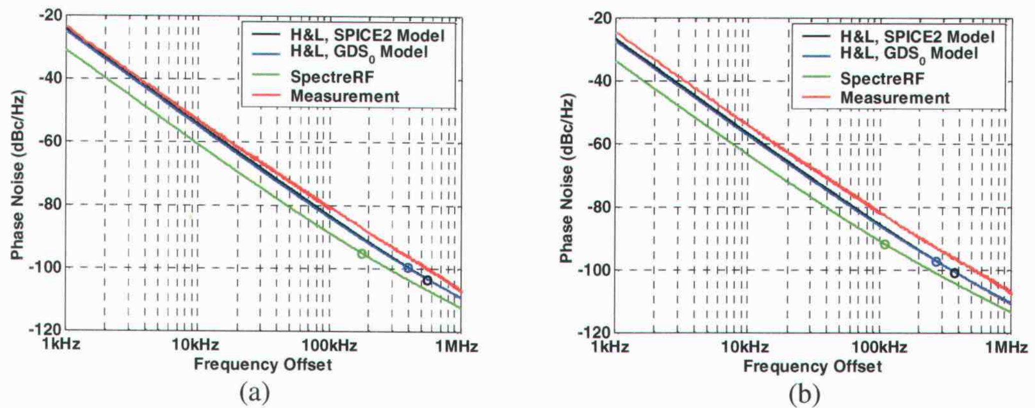


Figure F.4 Measurements versus simulations for (a) V_{PMOS}=1.8V and V_{NMOS}=1.1V and (b) V_{PMOS}=1.9V and V_{NMOS}=1.1V.

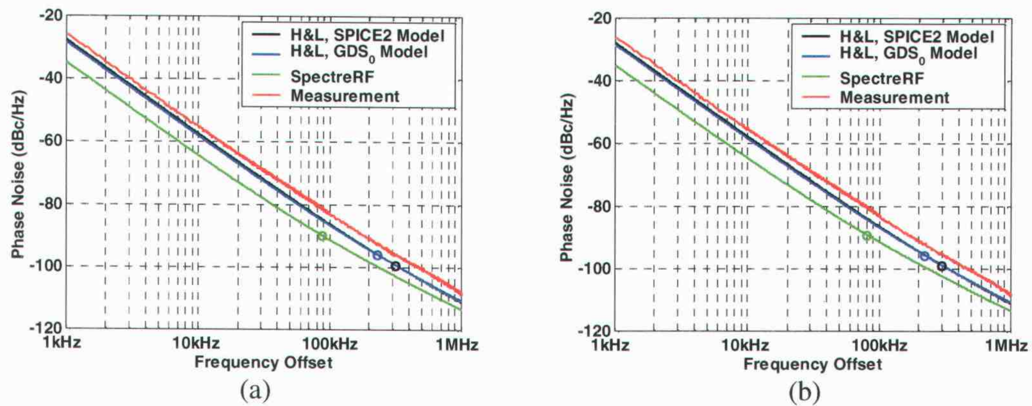


Figure F.5 Measurements versus simulations for (a) V_{PMOS}=2.0V and V_{NMOS}=1.1V and (b) V_{PMOS}=2.1V and V_{NMOS}=1.1V.

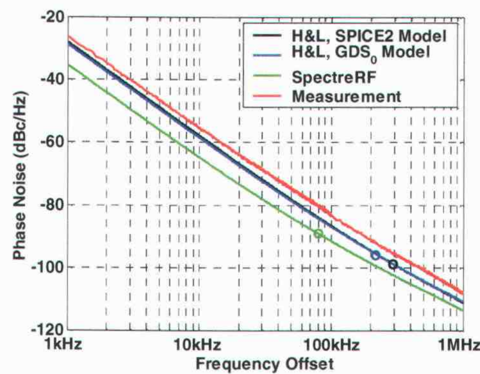
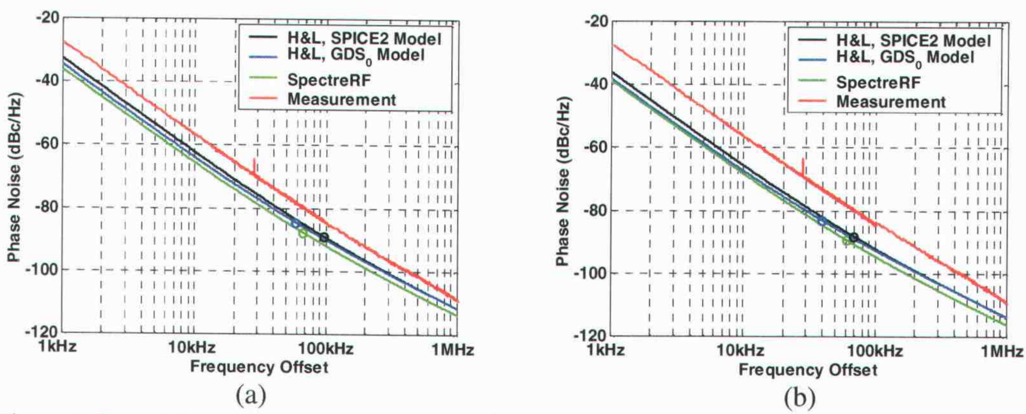
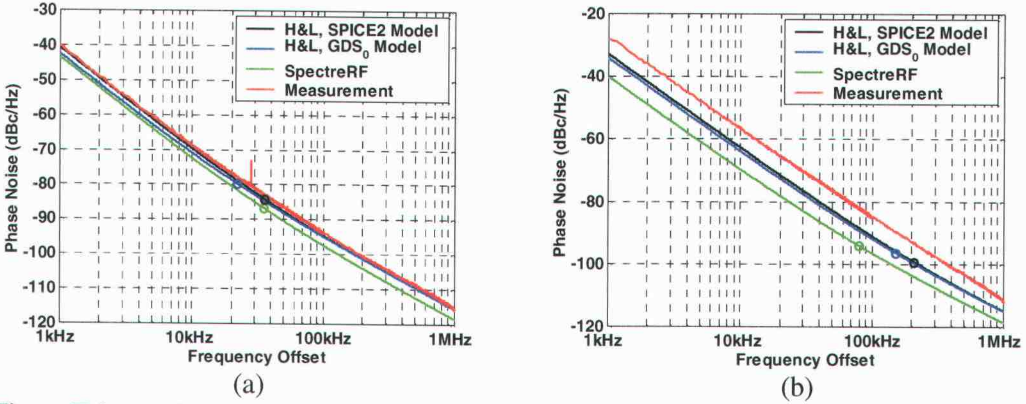


Figure F.6 Measurements versus simulations for V_{PMOS}=2.2V and V_{NMOS}=1.1V.



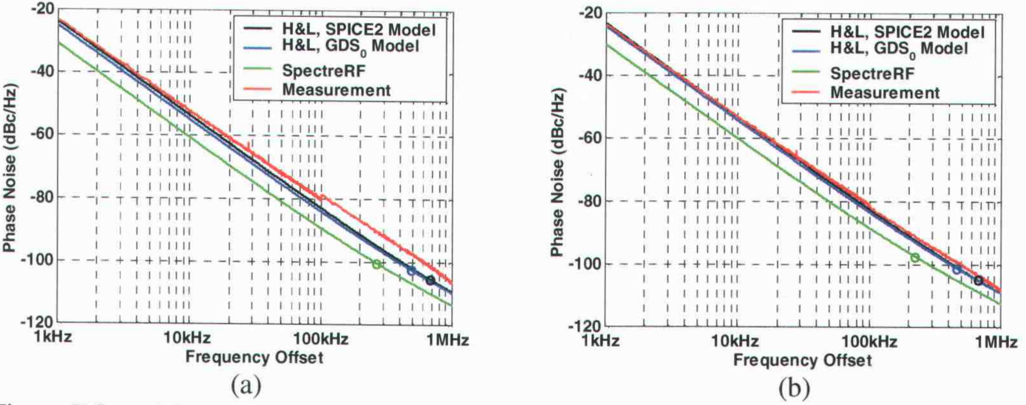
(a) (b)

Figure F.7 Measurements versus simulations for (a) V_{PMOS}=1.2V and V_{NMOS}=1.2V and (b) V_{PMOS}=1.3V and V_{NMOS}=1.2V.



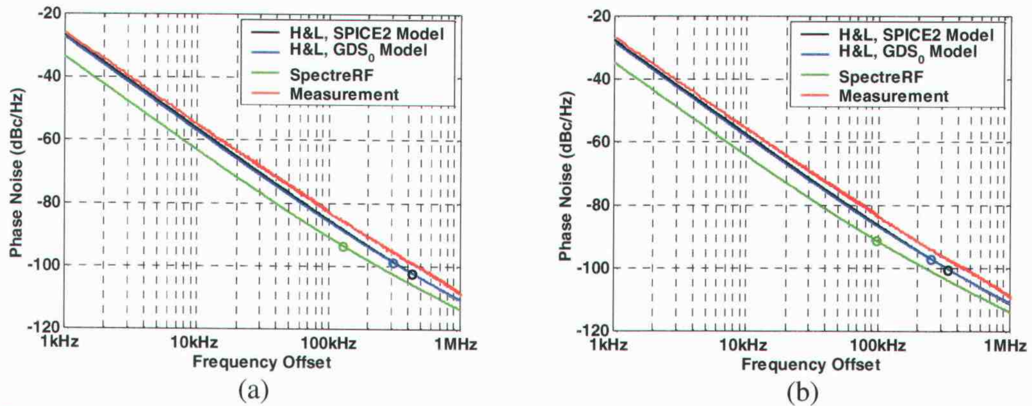
(a) (b)

Figure F.8 Measurements versus simulations for (a) V_{PMOS}=1.4V and V_{NMOS}=1.2V and (b) V_{PMOS}=1.5V and V_{NMOS}=1.2V.



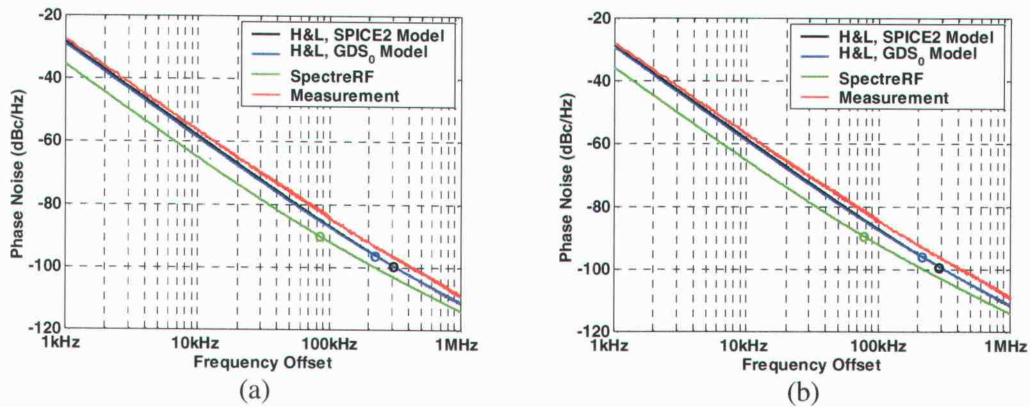
(a) (b)

Figure F.9 Measurements versus simulations for (a) V_{PMOS}=1.6V and V_{NMOS}=1.2V and (b) V_{PMOS}=1.7V and V_{NMOS}=1.2V.



(a) (b)

Figure F.10 Measurements versus simulations for (a) V_{PMOS}=1.8V and V_{NMOS}=1.2V and (b) V_{PMOS}=1.9V and V_{NMOS}=1.2V.



(a) (b)

Figure F.11 Measurements versus simulations for (a) V_{PMOS}=2.0V and V_{NMOS}=1.2V and (b) V_{PMOS}=2.1V and V_{NMOS}=1.2V.

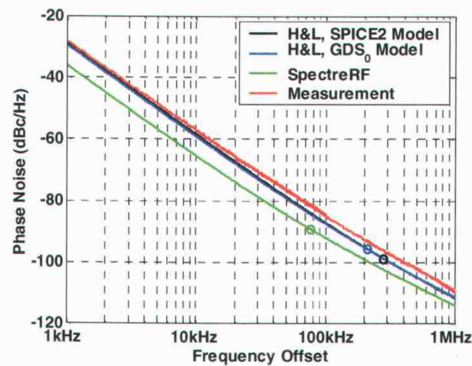


Figure F.12 Measurements versus simulations for V_{PMOS}=2.2V and V_{NMOS}=1.2V.

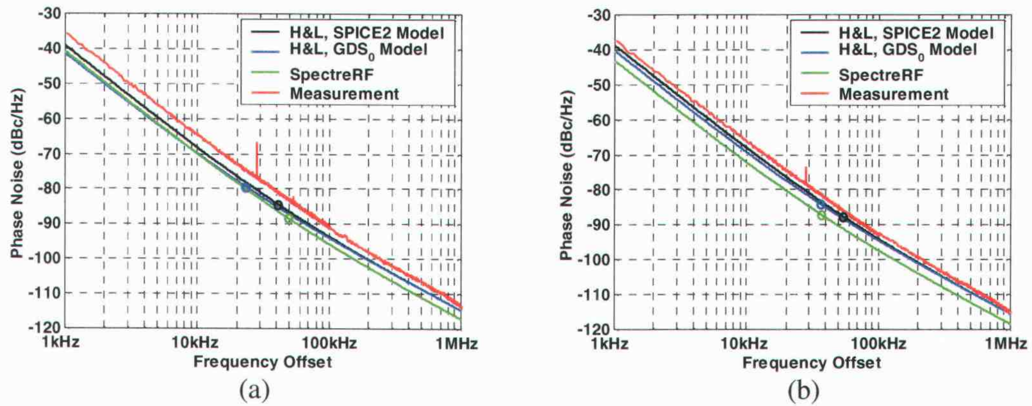


Figure F.13 Measurements versus simulations for (a) V_{PMOS}=1.2V and V_{NMOS}=1.3V and (b) V_{PMOS}=1.3V and V_{NMOS}=1.3V.

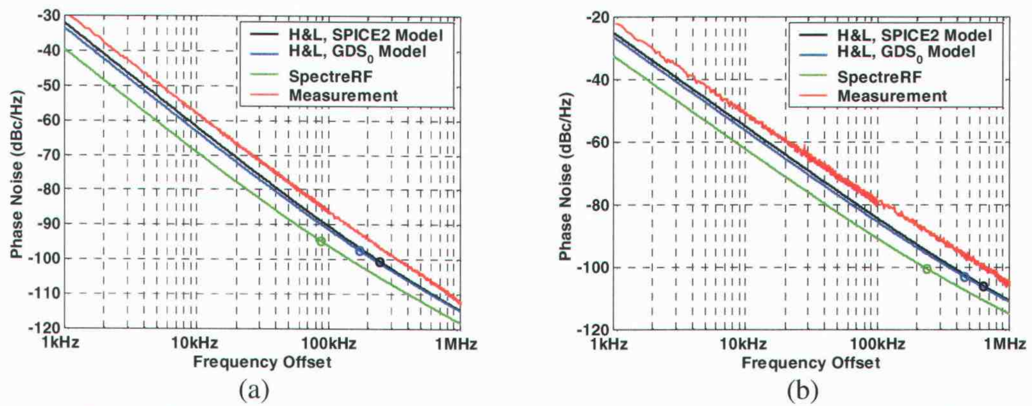


Figure F.14 Measurements versus simulations for (a) V_{PMOS}=1.4V and V_{NMOS}=1.3V and (b) V_{PMOS}=1.5V and V_{NMOS}=1.3V.

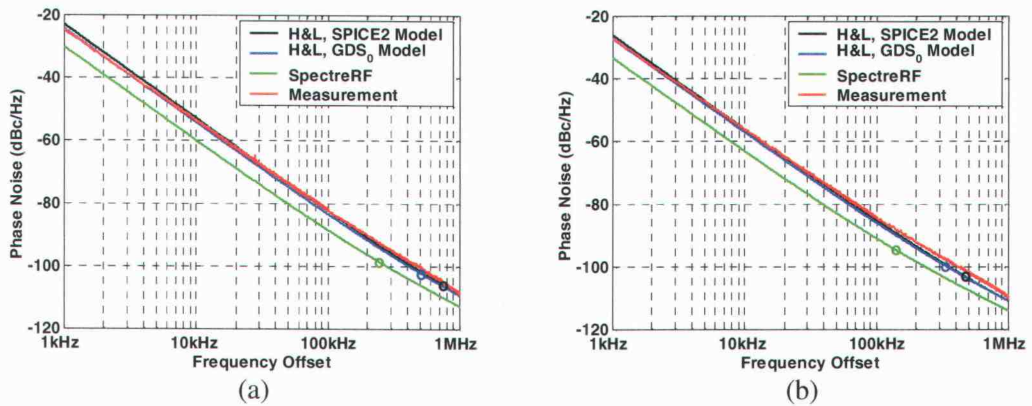


Figure F.15 Measurements versus simulations for (a) V_{PMOS}=1.6V and V_{NMOS}=1.3V and (b) V_{PMOS}=1.7V and V_{NMOS}=1.3V.

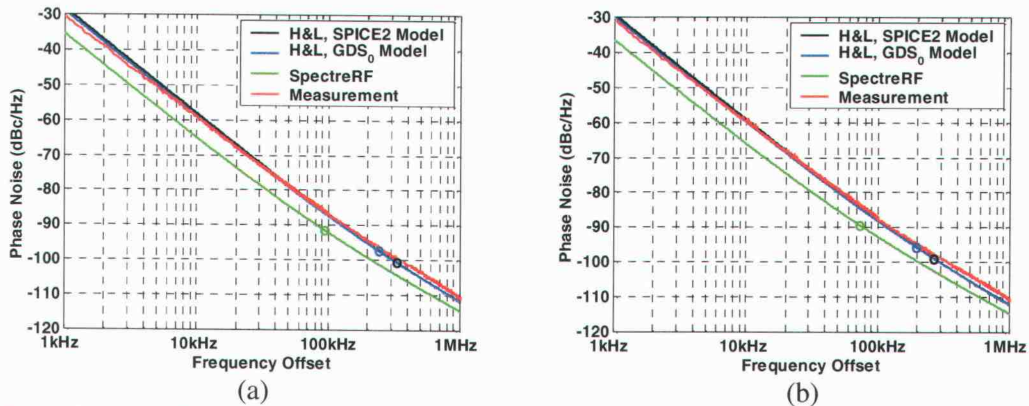


Figure F.16 Measurements versus simulations for (a) V_{PMOS}=1.8V and V_{NMOS}=1.3V and (b) V_{PMOS}=1.9V and V_{NMOS}=1.3V.

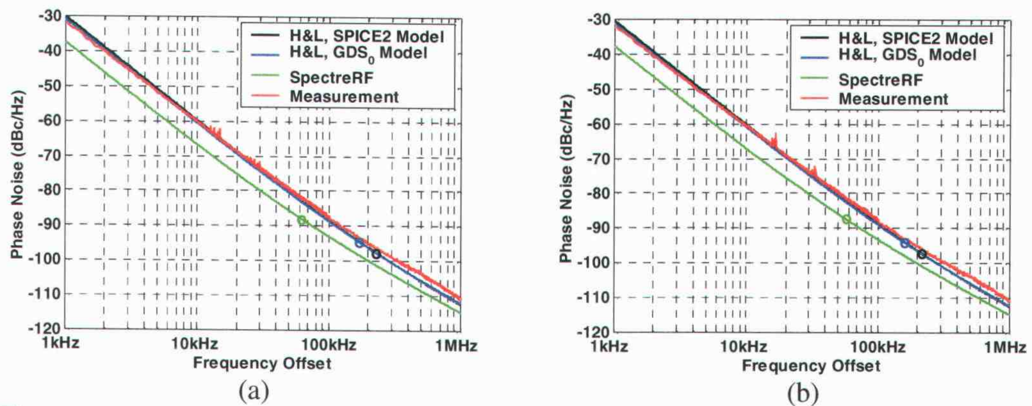


Figure F.17 Measurements versus simulations for (a) V_{PMOS}=2.0V and V_{NMOS}=1.3V and (b) V_{PMOS}=2.1V and V_{NMOS}=1.3V.

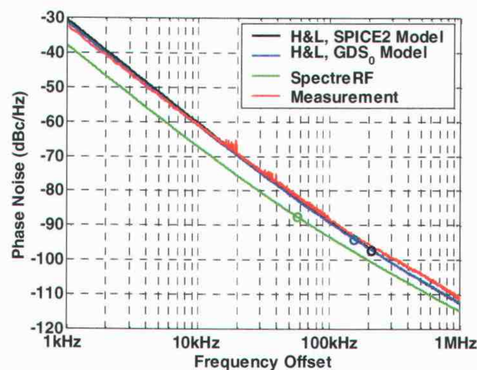
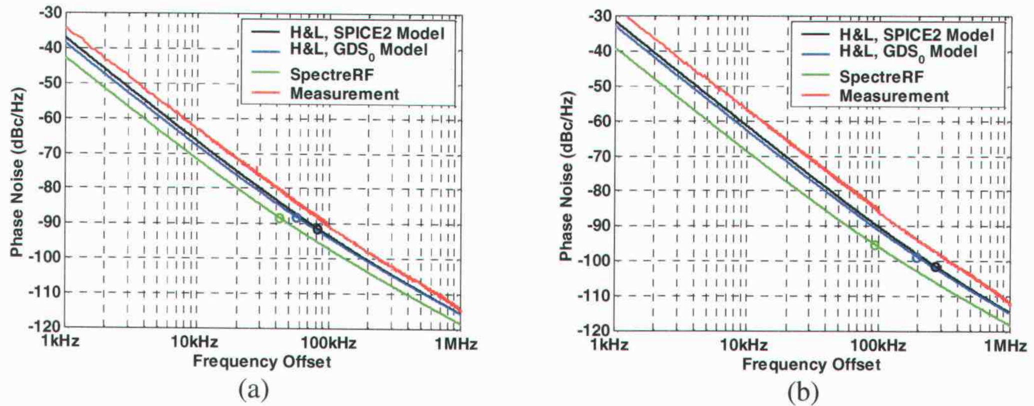
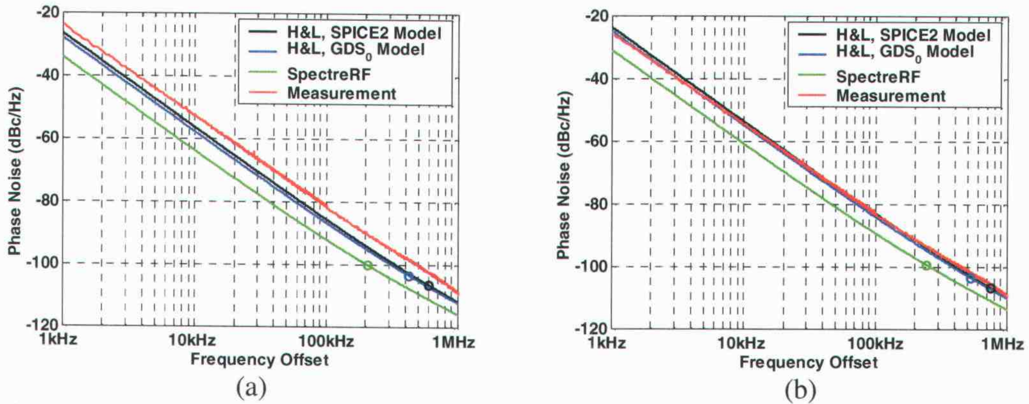


Figure F.18 Measurements versus simulations for V_{PMOS}=2.0V and V_{NMOS}=1.3V.



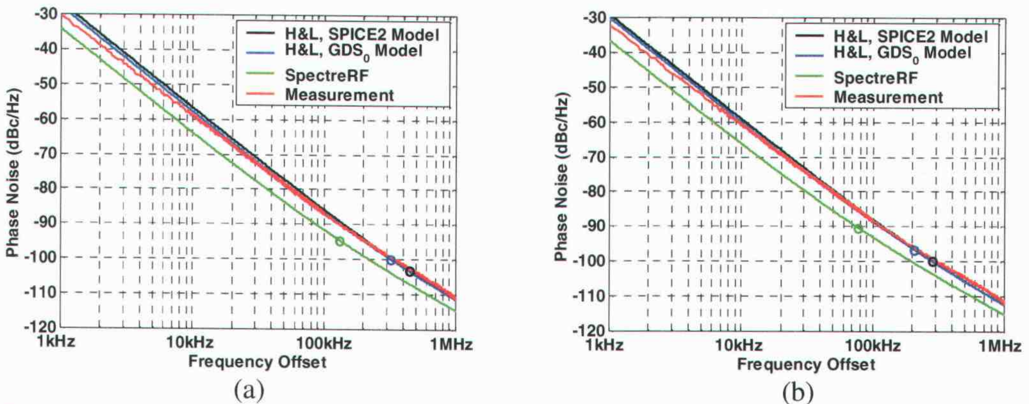
(a) (b)

Figure F.19 Measurements versus simulations for (a) V_{PMOS}=1.2V and V_{NMOS}=1.4V and (b) V_{PMOS}=1.3V and V_{NMOS}=1.4V.



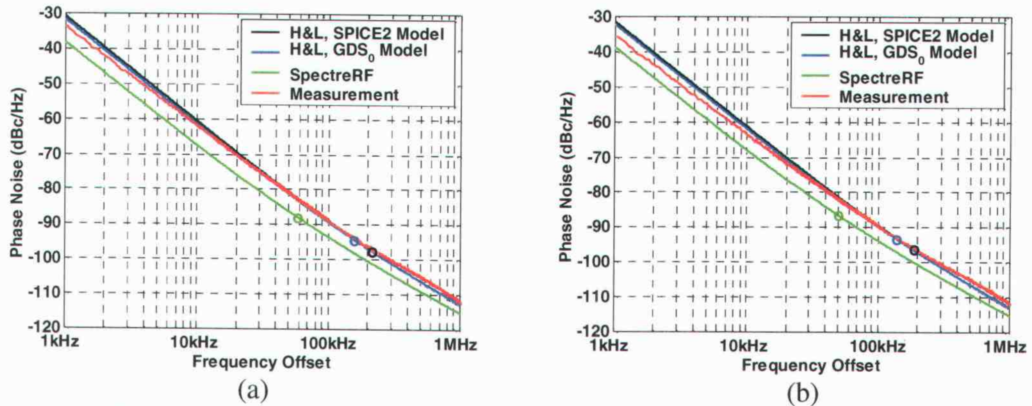
(a) (b)

Figure F.20 Measurements versus simulations for (a) V_{PMOS}=1.4V and V_{NMOS}=1.4V and (b) V_{PMOS}=1.5V and V_{NMOS}=1.4V.



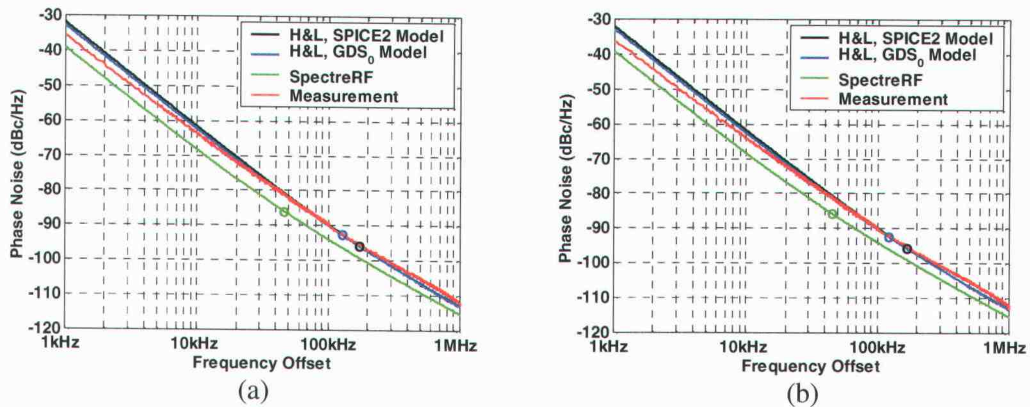
(a) (b)

Figure F.21 Measurements versus simulations for (a) V_{PMOS}=1.6V and V_{NMOS}=1.4V and (b) V_{PMOS}=1.7V and V_{NMOS}=1.4V.



(a) (b)

Figure F.22 Measurements versus simulations for (a) V_{PMOS}=1.8V and V_{NMOS}=1.4V and (b) V_{PMOS}=1.9V and V_{NMOS}=1.4V.



(a) (b)

Figure F.23 Measurements versus simulations for (a) V_{PMOS}=2.0V and V_{NMOS}=1.4V and (b) V_{PMOS}=2.1V and V_{NMOS}=1.4V.

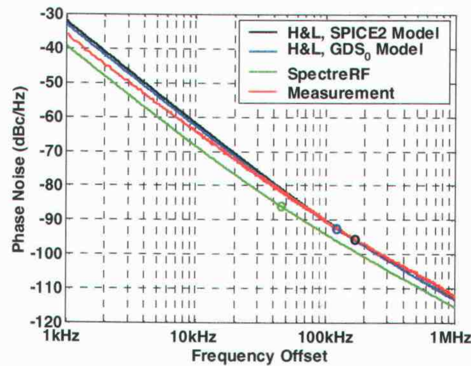


Figure F.24 Measurements versus simulations for V_{PMOS}=2.2V and V_{NMOS}=1.4V.

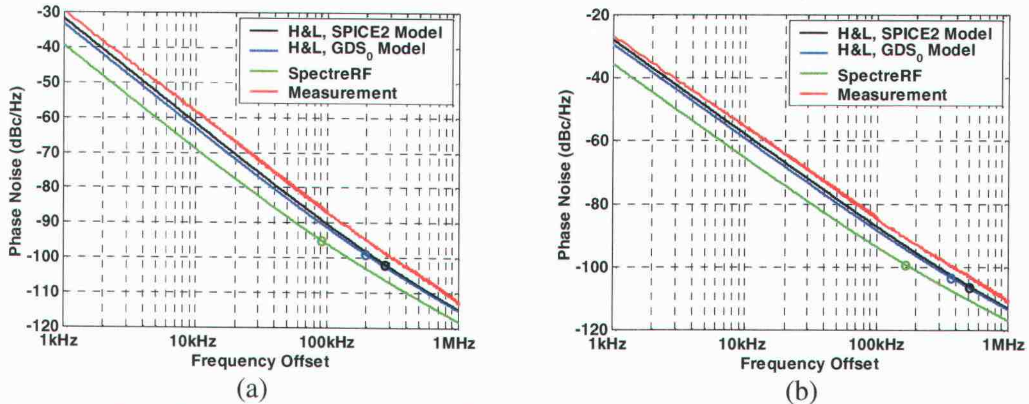


Figure F.25 Measurements versus simulations for (a) V_{PMOS}=1.2V and V_{NMOS}=1.5V and (b) V_{PMOS}=1.3V and V_{NMOS}=1.5V.

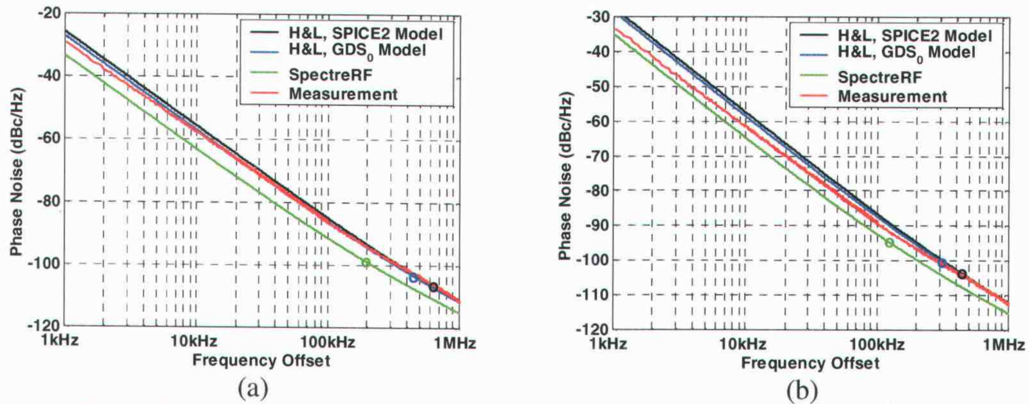


Figure F.26 Measurements versus simulations for (a) V_{PMOS}=1.4V and V_{NMOS}=1.5V and (b) V_{PMOS}=1.5V and V_{NMOS}=1.5V.

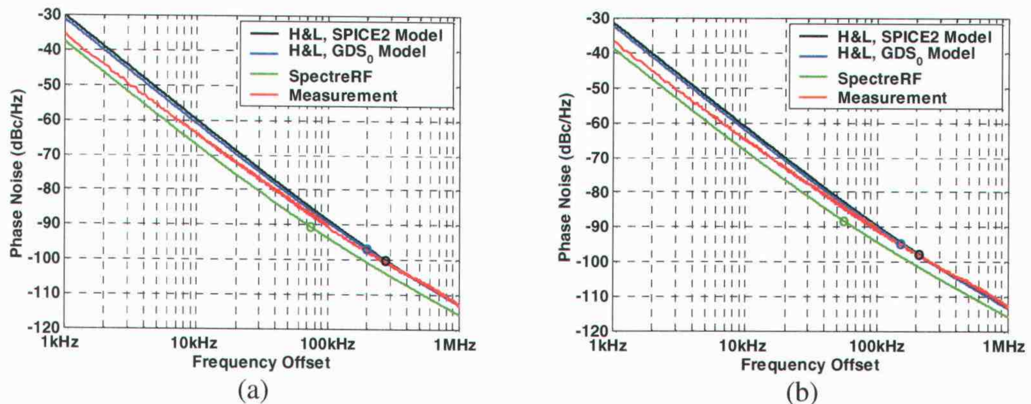
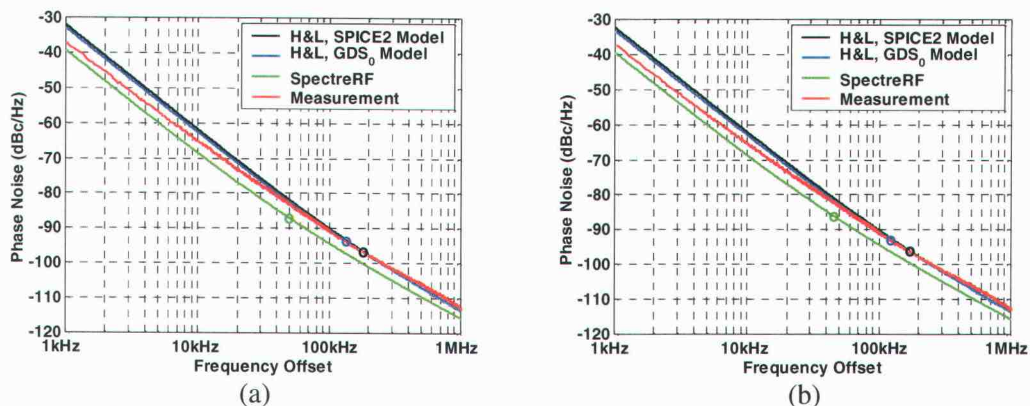
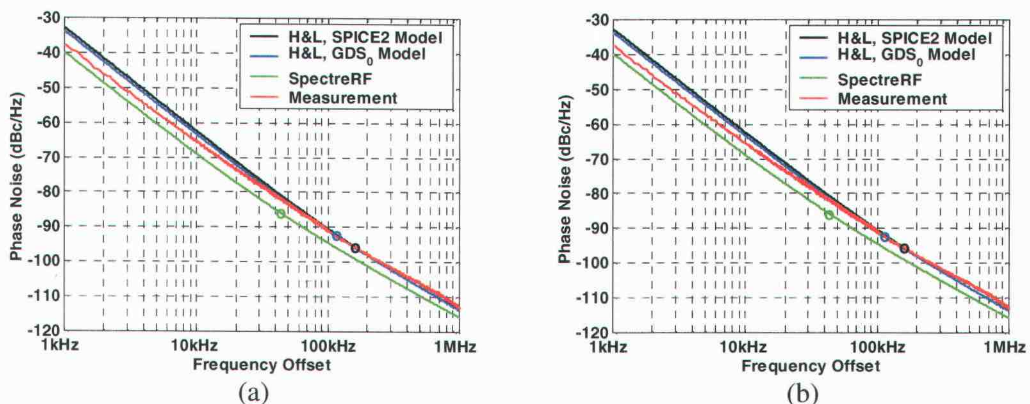


Figure F.27 Measurements versus simulations for (a) V_{PMOS}=1.6V and V_{NMOS}=1.5V and (b) V_{PMOS}=1.7V and V_{NMOS}=1.5V.



(a) (b)

Figure F.28 Measurements versus simulations for (a) V_{PMOS}=1.8V and V_{NMOS}=1.5V and (b) V_{PMOS}=1.9V and V_{NMOS}=1.5V.



(a) (b)

Figure F.29 Measurements versus simulations for (a) V_{PMOS}=2.0V and V_{NMOS}=1.5V and (b) V_{PMOS}=2.1V and V_{NMOS}=1.5V.

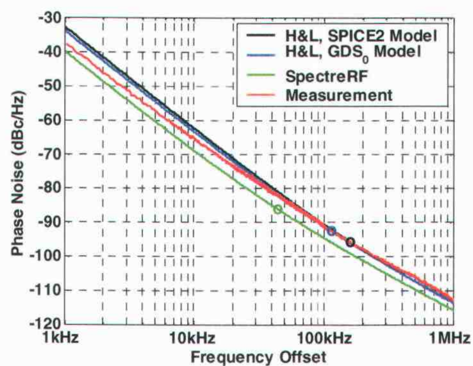


Figure F.30 Measurements versus simulations for V_{PMOS}=2.2V and V_{NMOS}=1.4V.

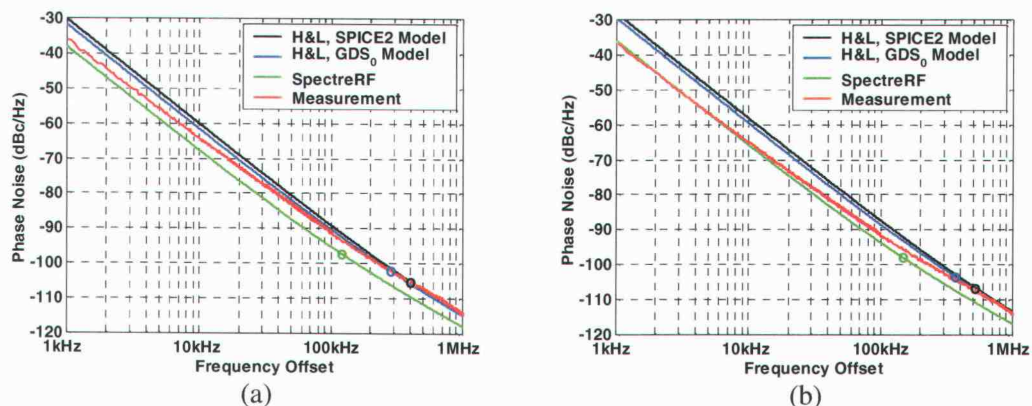


Figure F.31 Measurements versus simulations for (a) V_{PMOS}=1.2V and V_{NMOS}=1.6V and (b) V_{PMOS}=1.3V and V_{NMOS}=1.6V.

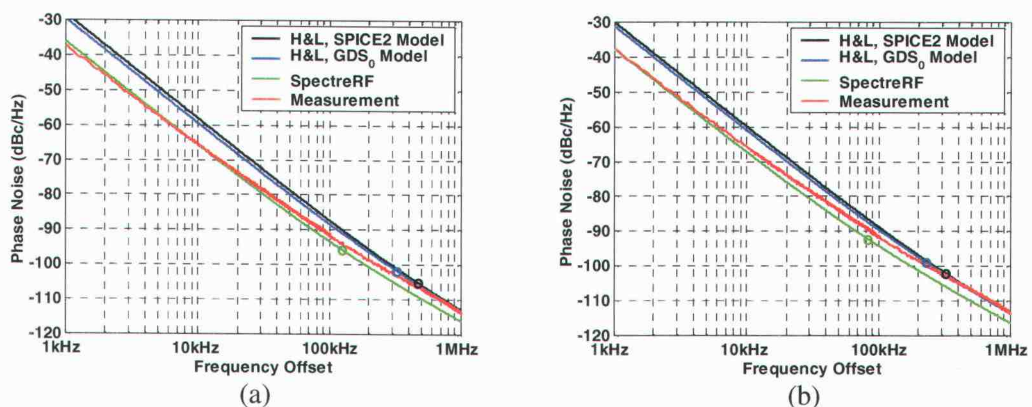


Figure F.32 Measurements versus simulations for (a) V_{PMOS}=1.4V and V_{NMOS}=1.6V and (b) V_{PMOS}=1.5V and V_{NMOS}=1.6V.

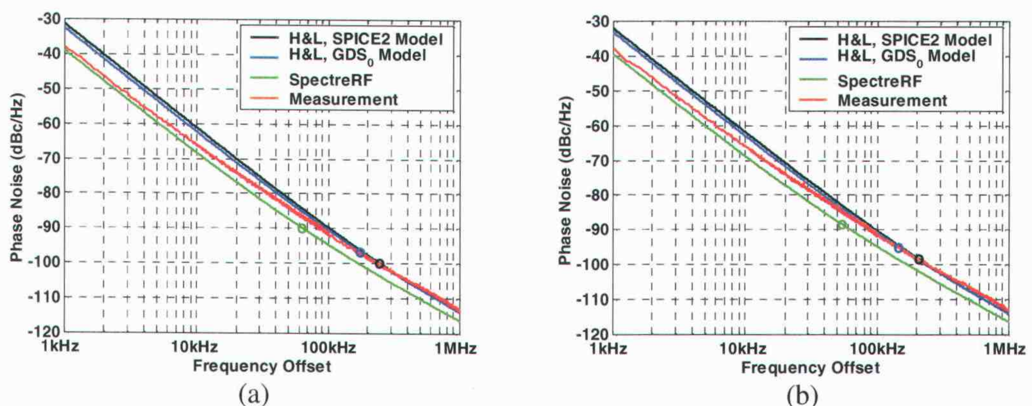


Figure F.33 Measurements versus simulations for (a) V_{PMOS}=1.6V and V_{NMOS}=1.6V and (b) V_{PMOS}=1.7V and V_{NMOS}=1.6V.

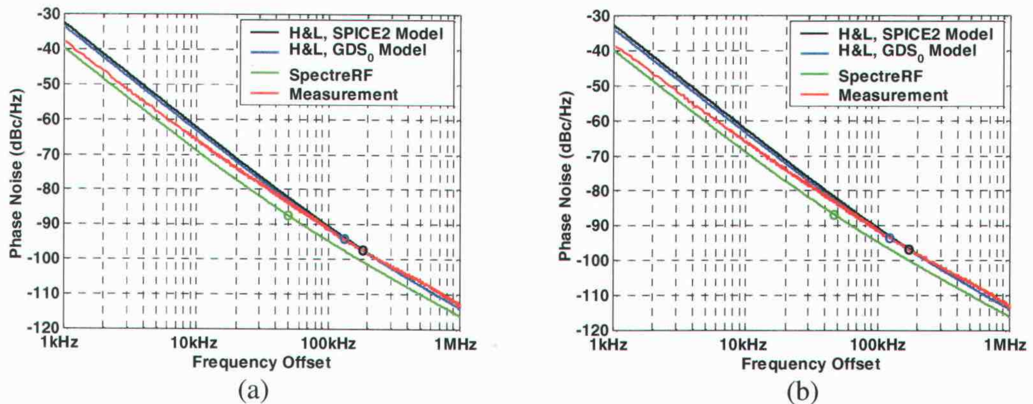


Figure F.34 Measurements versus simulations for (a) V_{PMOS}=1.8V and V_{NMOS}=1.6V and (b) V_{PMOS}=1.9V and V_{NMOS}=1.6V.

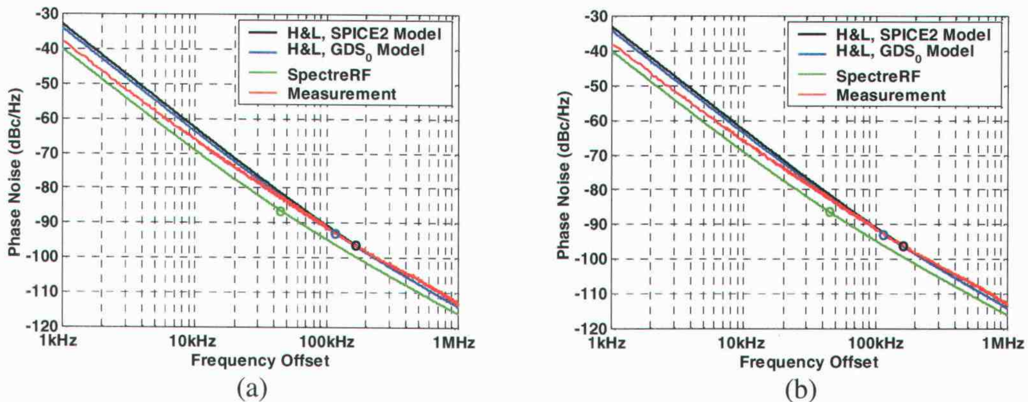


Figure F.35 Measurements versus simulations for (a) V_{PMOS}=2.0V and V_{NMOS}=1.6V and (b) V_{PMOS}=2.1V and V_{NMOS}=1.6V.

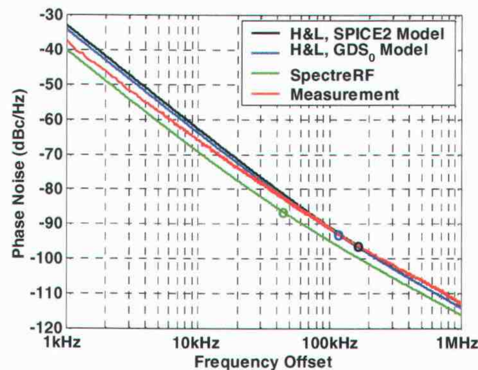


Figure F.36 Measurements versus simulations for V_{PMOS}=2.2V and V_{NMOS}=1.6V.

APPENDIX G Results for the low speed Maneatis load differential oscillator

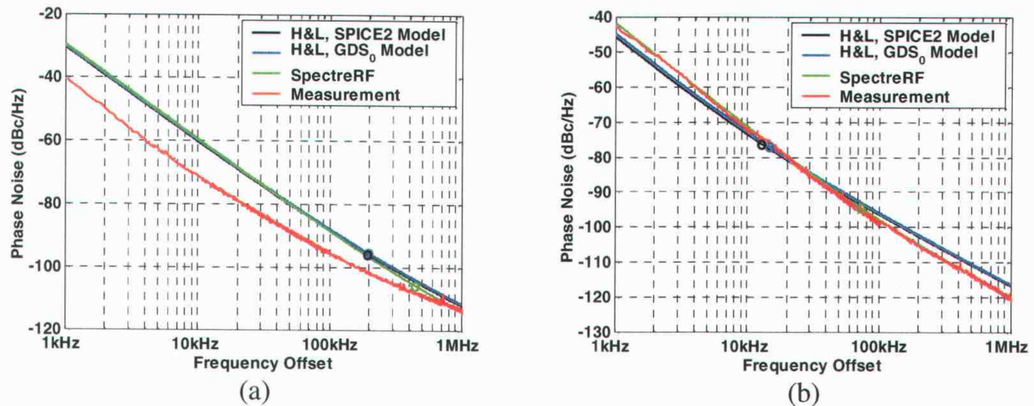


Figure G.1 Measurements versus simulations for (a) V_{PMOS}=1.3V and V_{NMOS}=1.2V and (b) V_{PMOS}=1.4V and V_{NMOS}=1.2V.

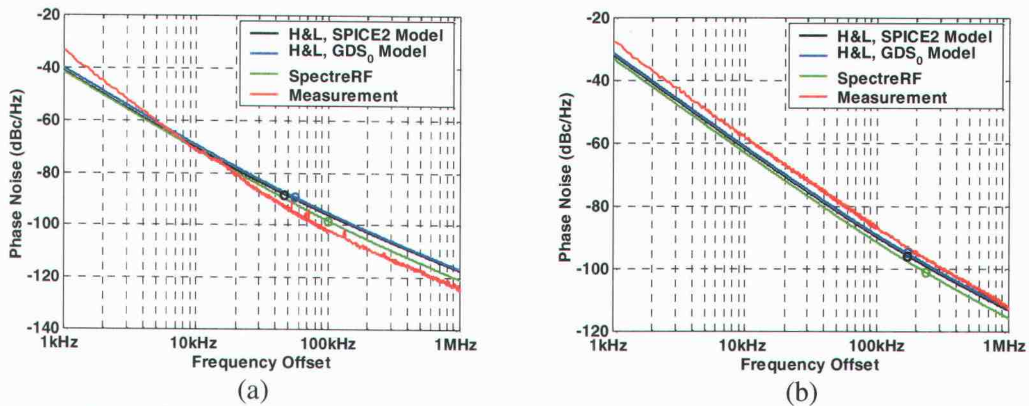


Figure G.2 Measurements versus simulations for (a) V_{PMOS}=1.5V and V_{NMOS}=1.2V and (b) V_{PMOS}=1.7V and V_{NMOS}=1.2V.

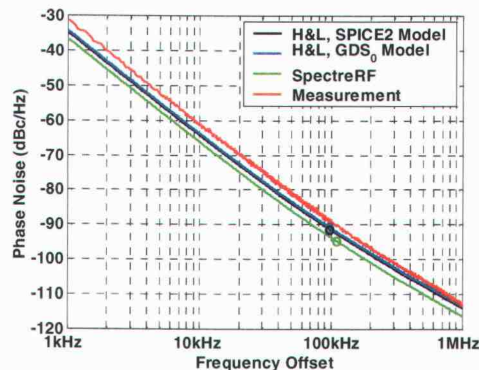
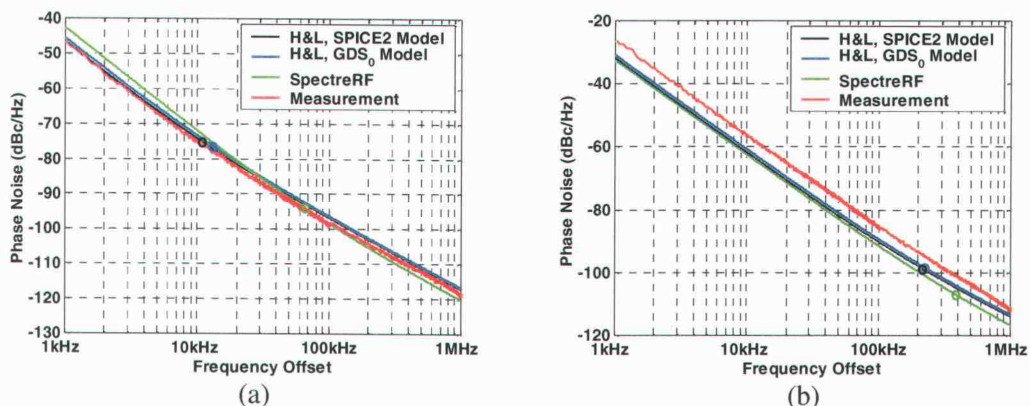
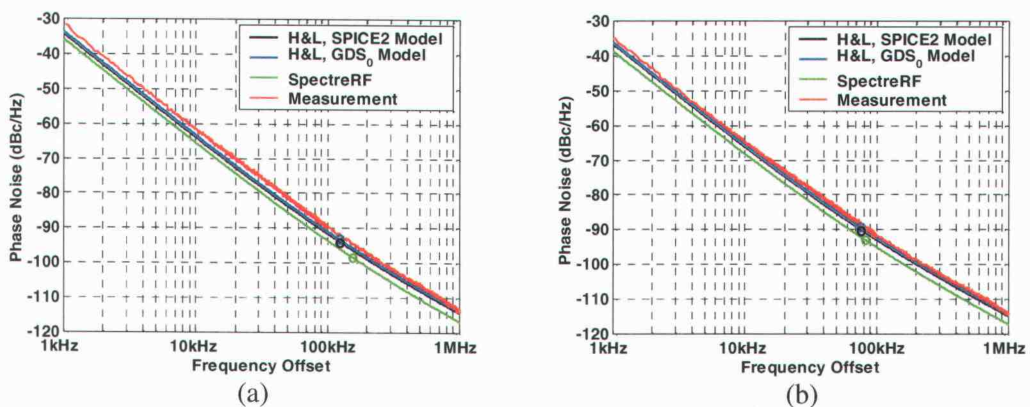


Figure G.3 Measurements versus simulations for V_{PMOS}=1.9V and V_{NMOS}=1.2V.



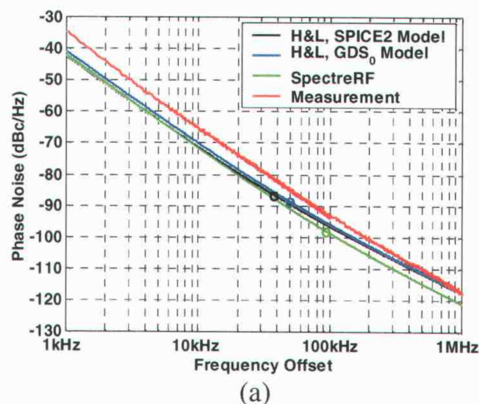
(a) (b)

Figure G.4 Measurements versus simulations for (a) V_{PMOS}=1.3V and V_{NMOS}=1.3V and (b) V_{PMOS}=1.5V and V_{NMOS}=1.3V.

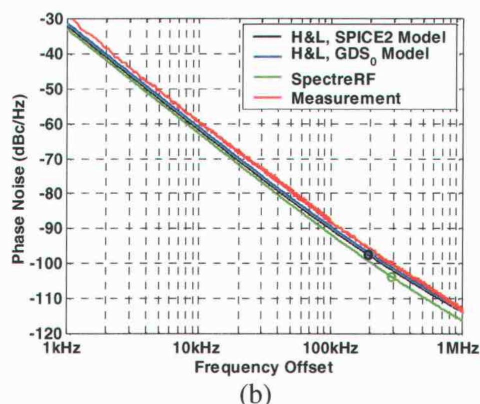


(a) (b)

Figure G.5 Measurements versus simulations for (a) V_{PMOS}=1.7V and V_{NMOS}=1.3V and (b) V_{PMOS}=1.9V and V_{NMOS}=1.3V.

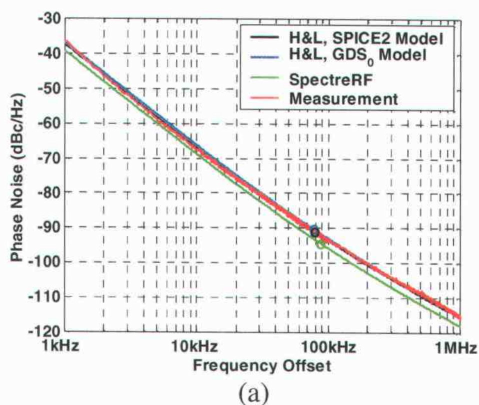


(a)

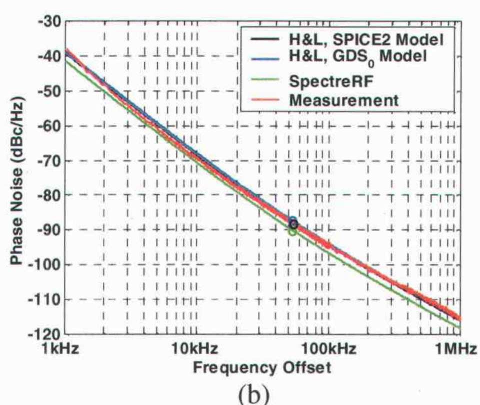


(b)

Figure G.6 Measurements versus simulations for (a) V_{PMOS}=1.3V and V_{NMOS}=1.4V and (b) V_{PMOS}=1.5V and V_{NMOS}=1.4V.

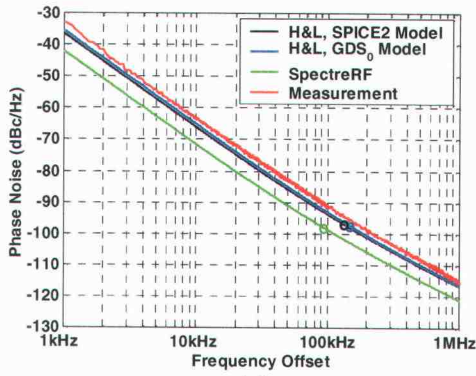


(a)

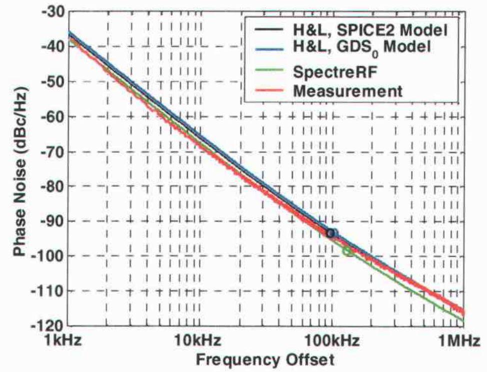


(b)

Figure G.7 Measurements versus simulations for (a) V_{PMOS}=1.7V and V_{NMOS}=1.4V and (b) V_{PMOS}=1.9V and V_{NMOS}=1.4V.

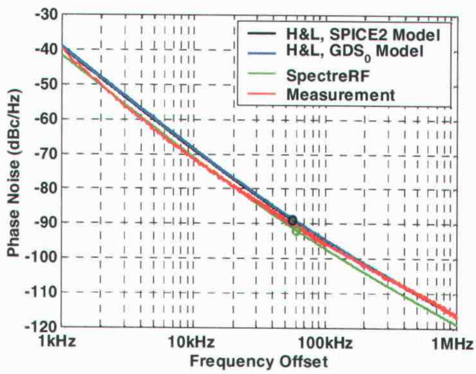


(a)

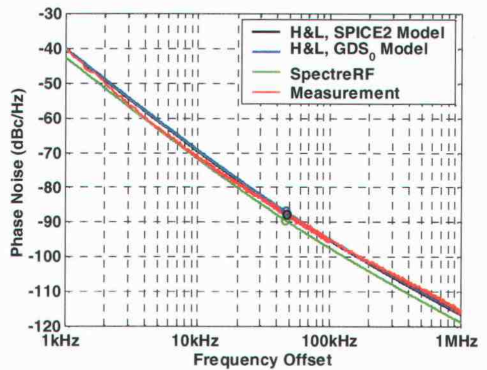


(b)

Figure G.8 Measurements versus simulations for (a) V_{PMOS}=1.3V and V_{NMOS}=1.5V and (b) V_{PMOS}=1.5V and V_{NMOS}=1.5V.



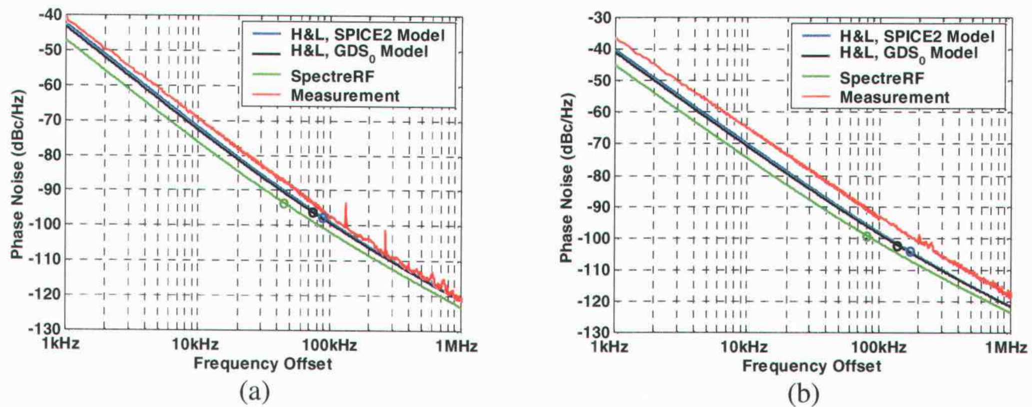
(a)



(b)

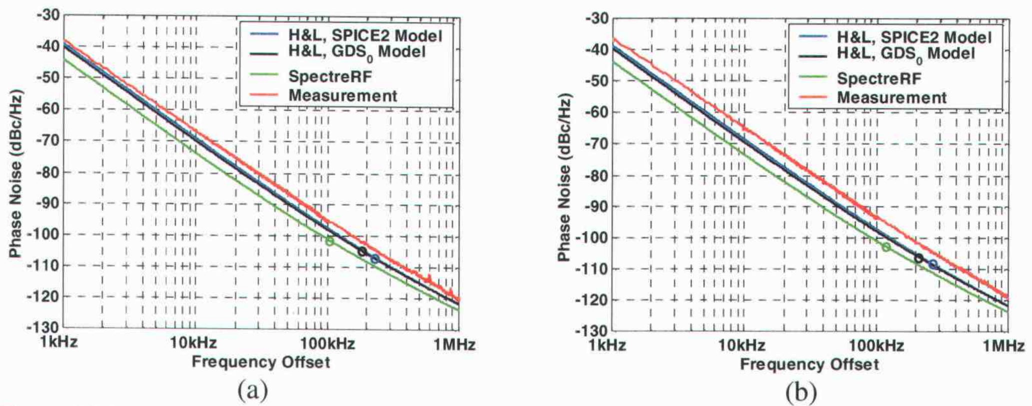
Figure G.9 Measurements versus simulations for (a) V_{PMOS}=1.7V and V_{NMOS}=1.5V and (b) V_{PMOS}=1.9V and V_{NMOS}=1.5V.

APPENDIX H Results for the cross-coupled load differential oscillator



(a) (b)

Figure H.1 Measurements versus simulations for (a) V_{PMOS}=1.8V and V_{NMOS}=1.2V and (b) V_{PMOS}=1.9V and V_{NMOS}=1.2V.



(a) (b)

Figure H.2 Measurements versus simulations for (a) V_{PMOS}=2.0V and V_{NMOS}=1.2V and (b) V_{PMOS}=2.1V and V_{NMOS}=1.2V.

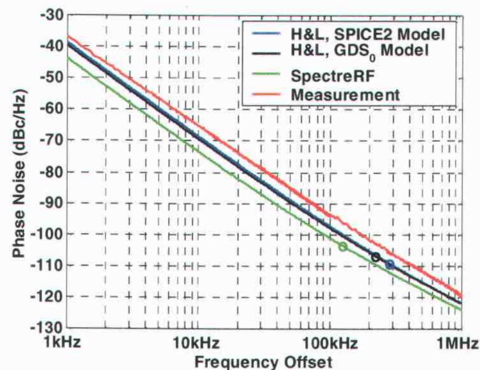


Figure H.3 Measurements versus simulations for V_{PMOS}=2.2V and V_{NMOS}=1.2V.

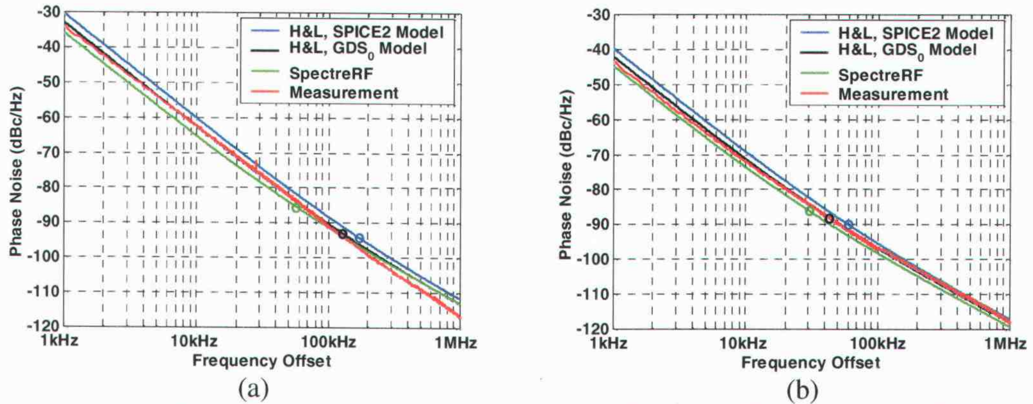


Figure H.4 Measurements versus simulations for (a) V_{PMOS}=1.3V and V_{NMOS}=1.3V and (b) V_{PMOS}=1.5V and V_{NMOS}=1.3V.

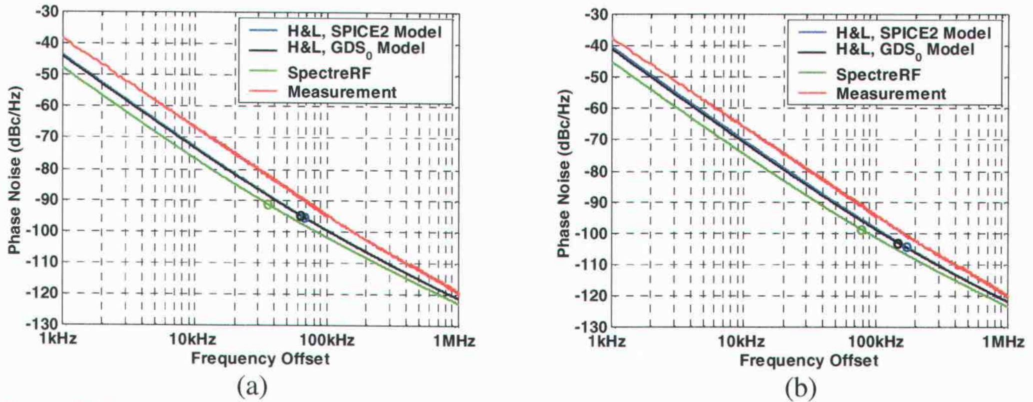


Figure H.5 Measurements versus simulations for (a) V_{PMOS}=1.7V and V_{NMOS}=1.3V and (b) V_{PMOS}=1.8V and V_{NMOS}=1.3V.

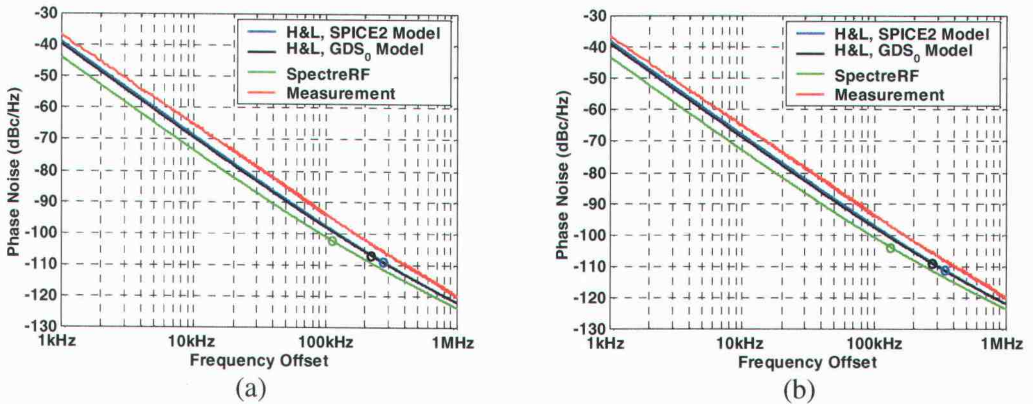
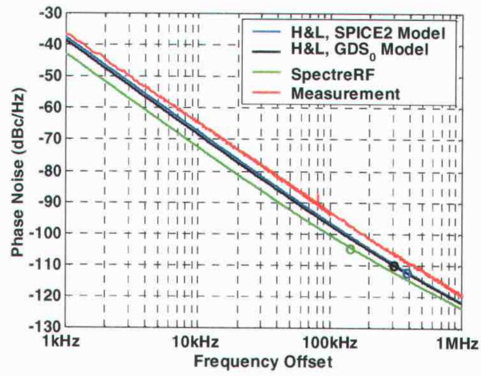
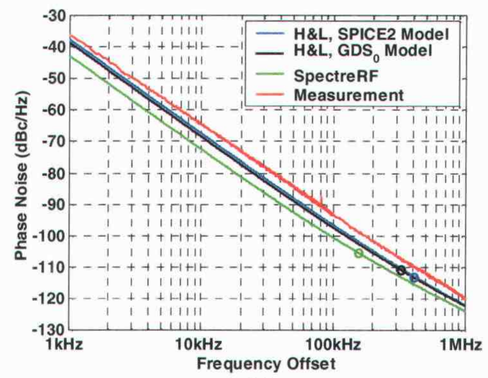


Figure H.6 Measurements versus simulations for (a) V_{PMOS}=1.9V and V_{NMOS}=1.3V and (b) V_{PMOS}=2.0V and V_{NMOS}=1.3V.

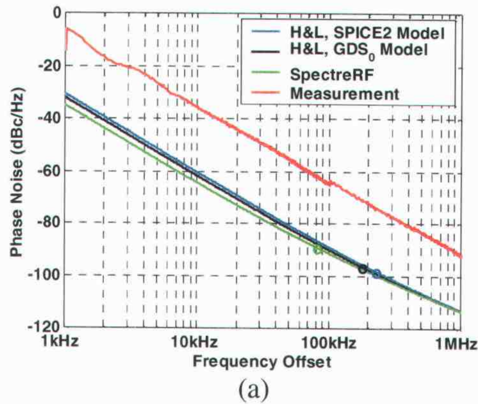


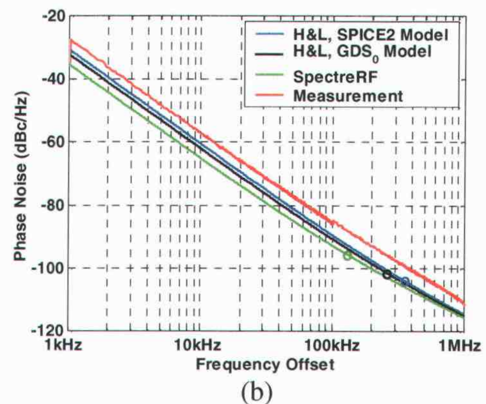
(a)



(b)

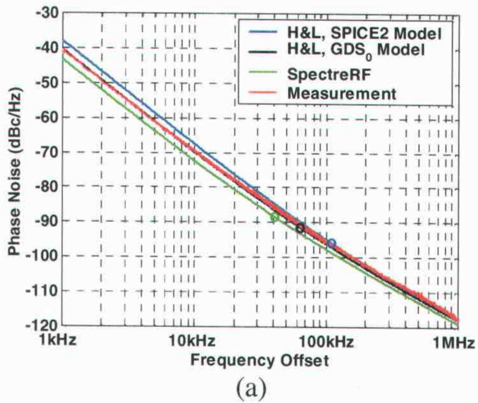
Figure H.7 Measurements versus simulations for (a) V_{PMOS}=2.1V and V_{NMOS}=1.3V and (b) V_{PMOS}=2.2V and V_{NMOS}=1.3V.

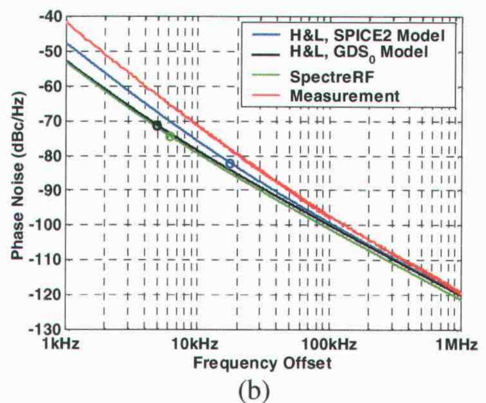




(a) (b)

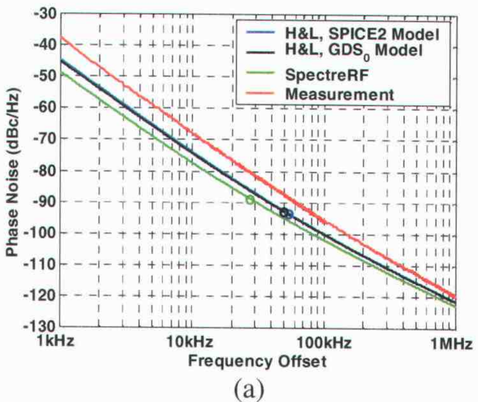
Figure H.8 Measurements versus simulations for (a) V_{PMOS}=1.2V and V_{NMOS}=1.4V and (b) V_{PMOS}=1.3V and V_{NMOS}=1.4V.

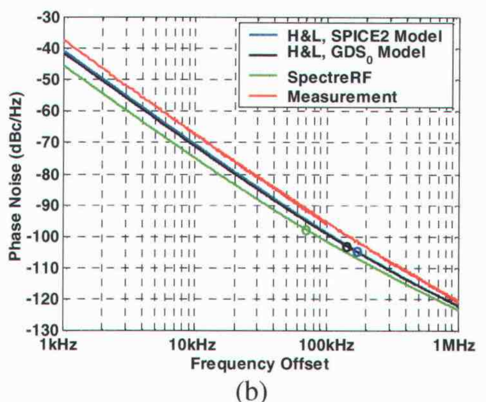




(a) (b)

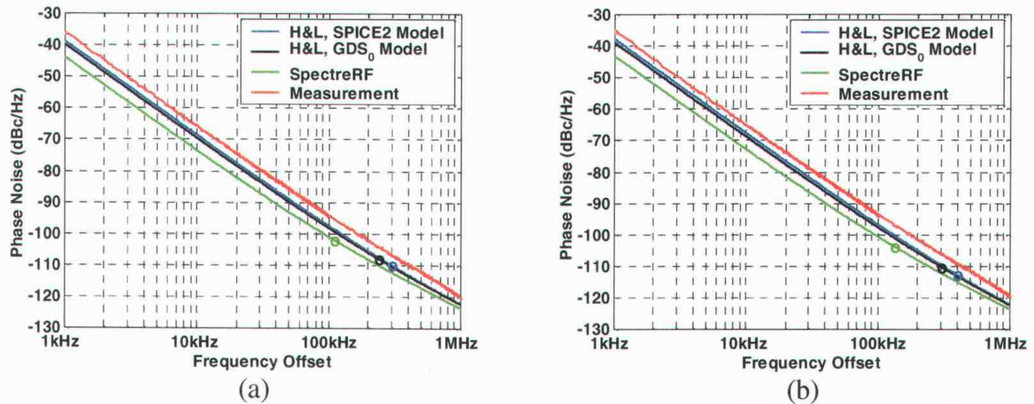
Figure H.9 Measurements versus simulations for (a) V_{PMOS}=1.4V and V_{NMOS}=1.4V and (b) V_{PMOS}=1.5V and V_{NMOS}=1.4V.





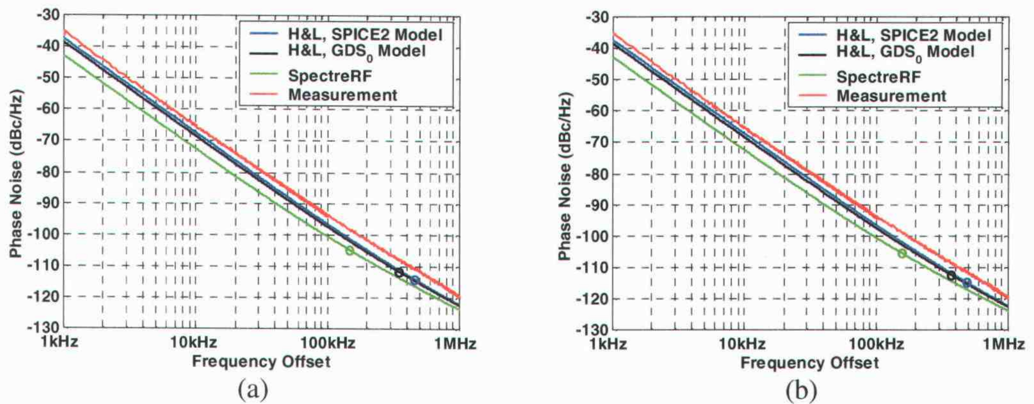
(a) (b)

Figure H.10 Measurements versus simulations for (a) V_{PMOS}=1.6V and V_{NMOS}=1.4V and (b) V_{PMOS}=1.7V and V_{NMOS}=1.4V.



(a) (b)

Figure H.11 Measurements versus simulations for (a) V_{PMOS}=1.8V and V_{NMOS}=1.4V and (b) V_{PMOS}=1.9V and V_{NMOS}=1.4V.



(a) (b)

Figure H.12 Measurements versus simulations for (a) V_{PMOS}=2.0V and V_{NMOS}=1.4V and (b) V_{PMOS}=2.1V and V_{NMOS}=1.4V.

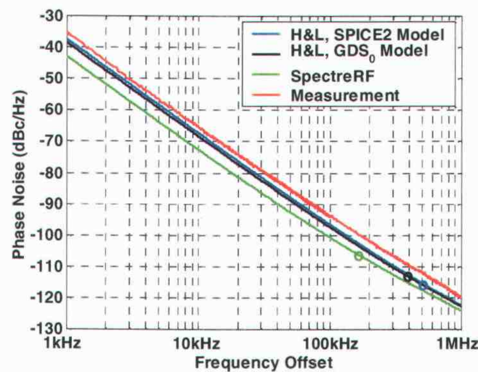


Figure H.13 Measurements versus simulations for V_{PMOS}=2.2V and V_{NMOS}=1.4V.

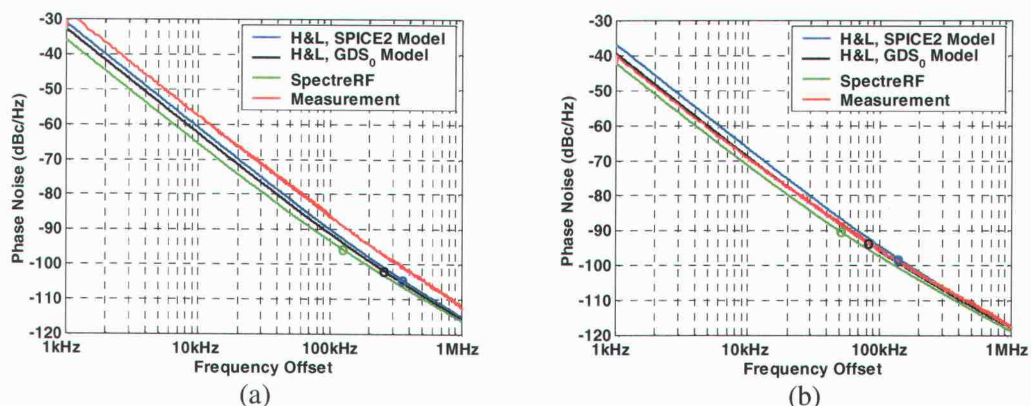


Figure H.14 Measurements versus simulations for (a) V_{PMOS}=1.2V and V_{NMOS}=1.5V and (b) V_{PMOS}=1.3V and V_{NMOS}=1.5V.

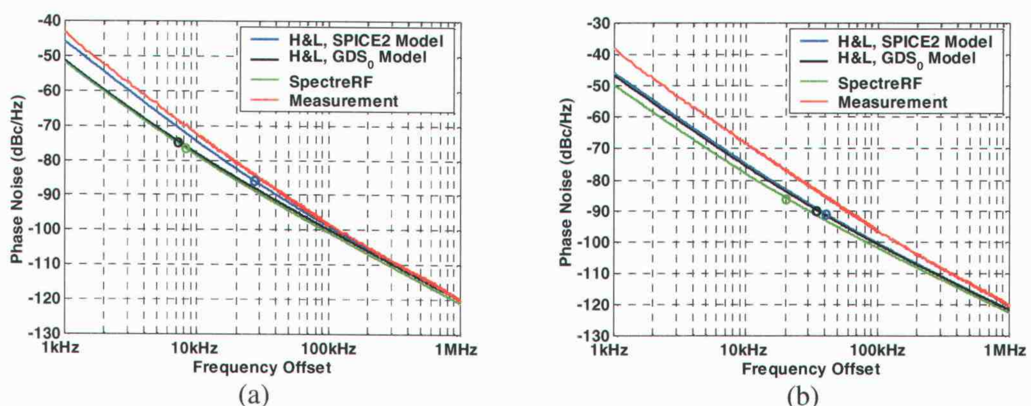


Figure H.15 Measurements versus simulations for (a) V_{PMOS}=1.4V and V_{NMOS}=1.5V and (b) V_{PMOS}=1.5V and V_{NMOS}=1.5V.

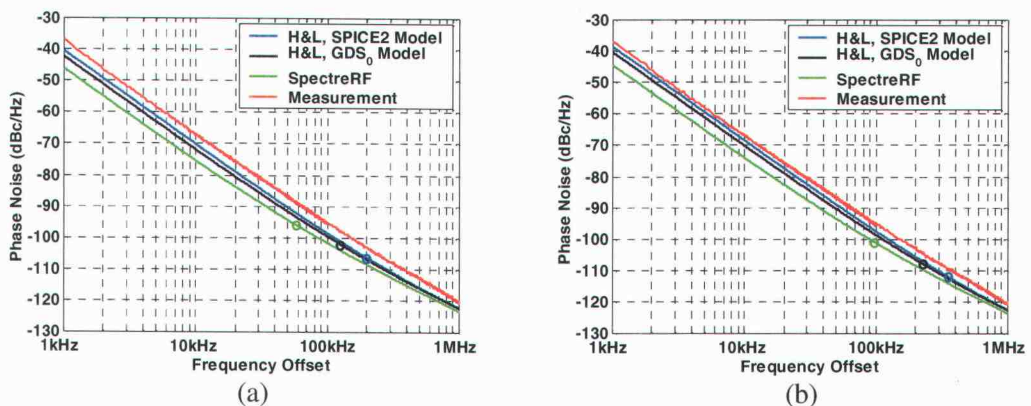


Figure H.16 Measurements versus simulations for (a) V_{PMOS}=1.6V and V_{NMOS}=1.5V and (b) V_{PMOS}=1.7V and V_{NMOS}=1.5V.

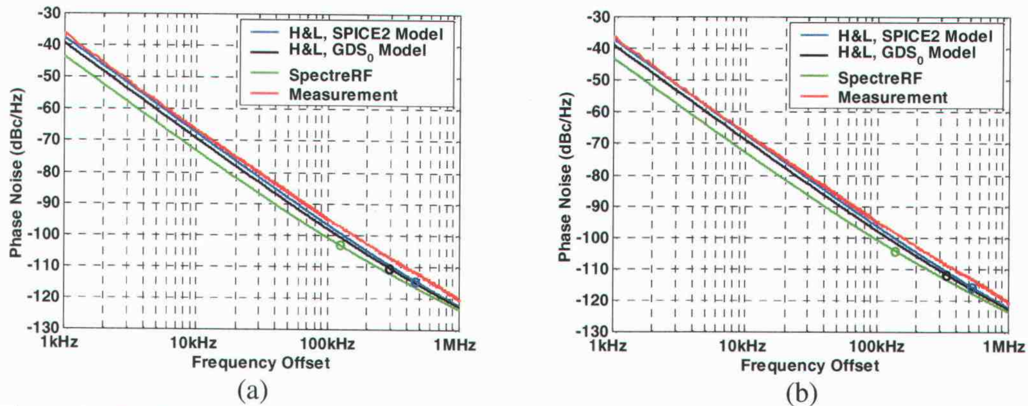


Figure H.17 Measurements versus simulations for (a) V_{PMOS}=1.8V and V_{NMOS}=1.5V and (b) V_{PMOS}=1.9V and V_{NMOS}=1.5V.

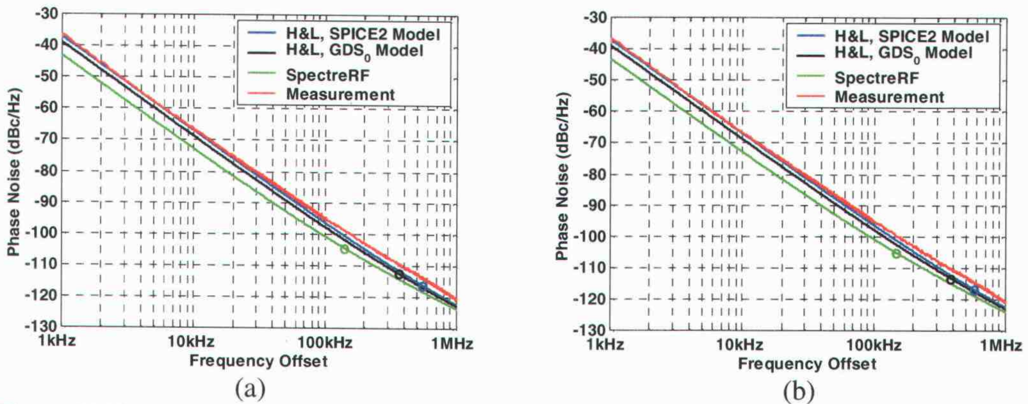


Figure H.18 Measurements versus simulations for (a) V_{PMOS}=2.0V and V_{NMOS}=1.5V and (b) V_{PMOS}=2.1V and V_{NMOS}=1.5V.

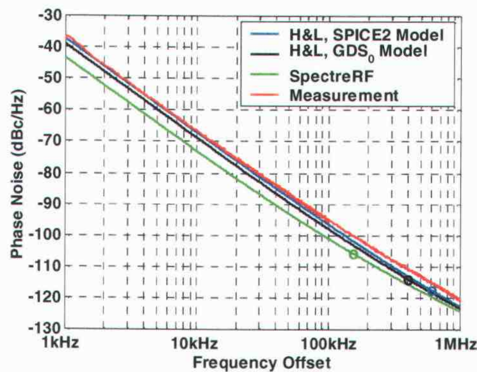


Figure H.19 Measurements versus simulations for V_{PMOS}=2.2V and V_{NMOS}=1.5V.

APPENDIX I Results for the 1998 single-ended 9-stage current-starved oscillator

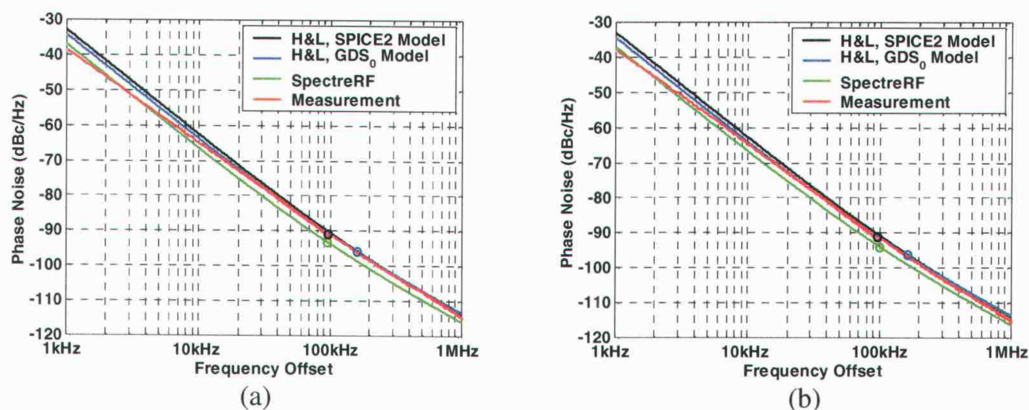


Figure I.1 Measurements versus simulations for (a) V_{CTRL}=1.0V and (b) V_{CTRL}=1.1V.

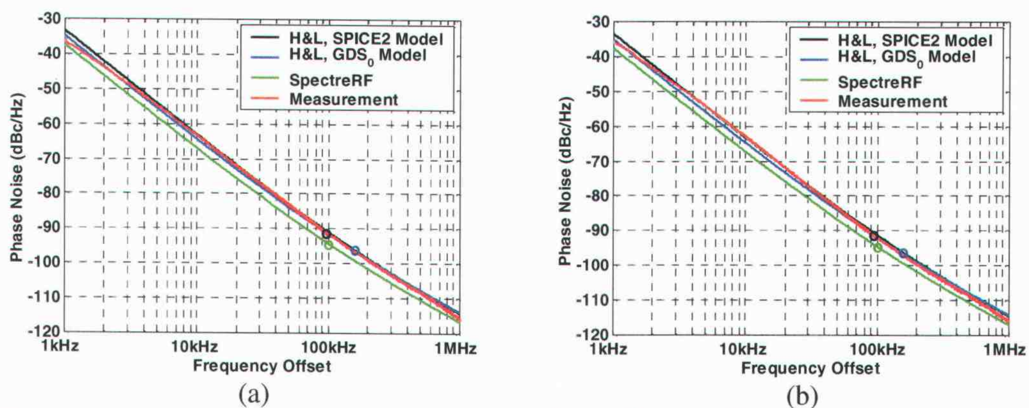


Figure I.2 Measurements versus simulations for (a) V_{CTRL}=1.2V and (b) V_{CTRL}=1.3V.

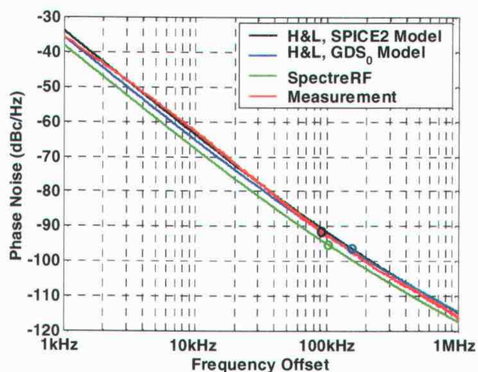
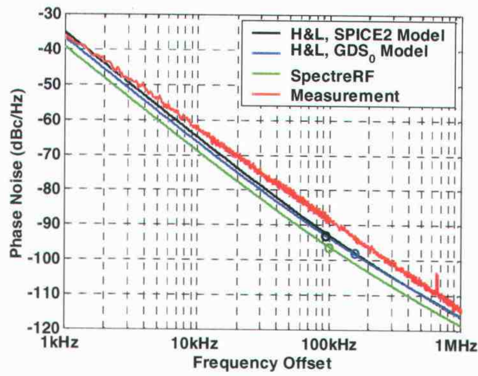
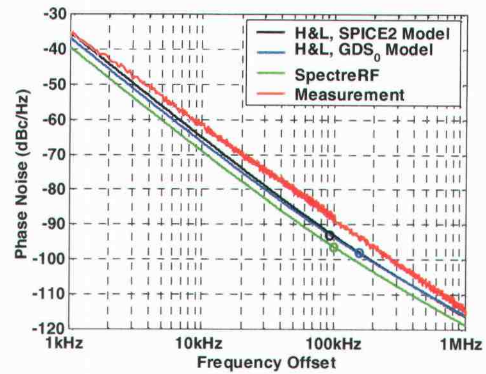


Figure I.3 Measurements versus simulations for V_{CTRL}=1.4V.

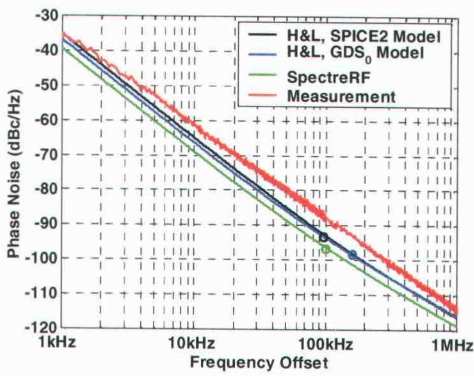


(a)

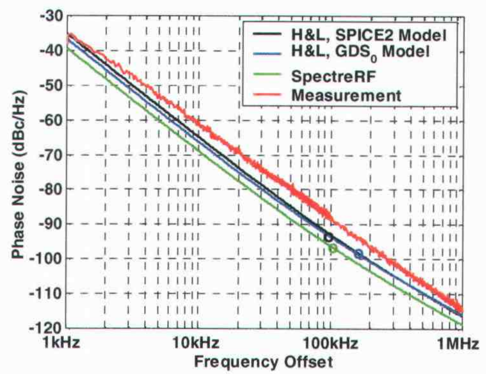


(b)

Figure I.4 Measurements versus simulations for (a) V_{DD}=2.0V and (b) V_{DD}=2.5V.



(a)



(b)

Figure I.5 Measurements versus simulations for (a) V_{DD}=3.0V and (b) V_{DD}=3.5V.

APPENDIX J Results for the 1998 simple, single-ended 5-stage oscillator

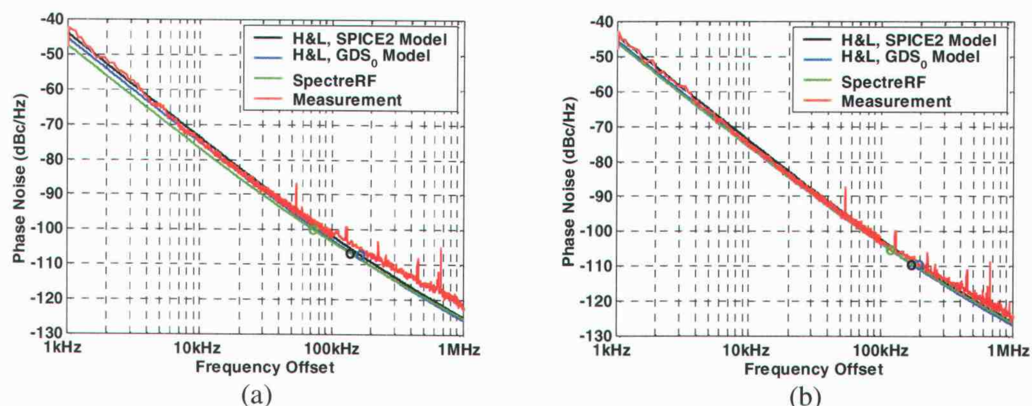


Figure J.1 Measurements versus simulations for (a) V_{DD}=1.5V and (b) V_{DD}=2.0V.

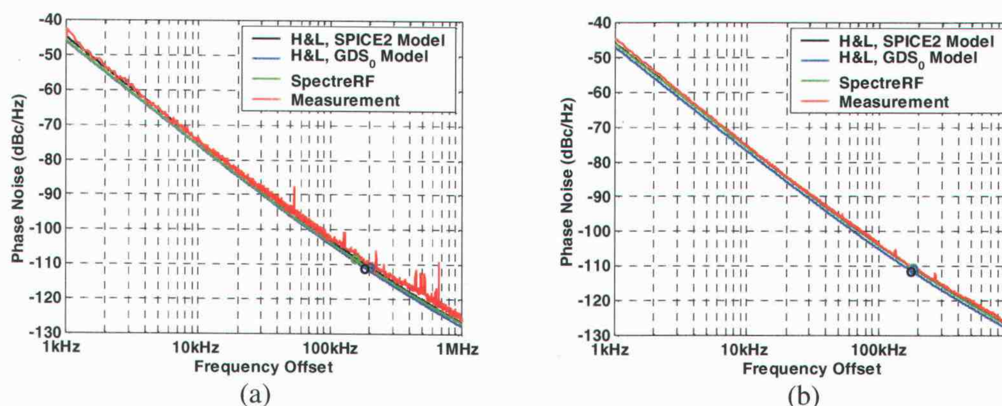


Figure J.2 Measurements versus simulations for (a) V_{DD}=2.5V and (b) V_{DD}=3.0V.

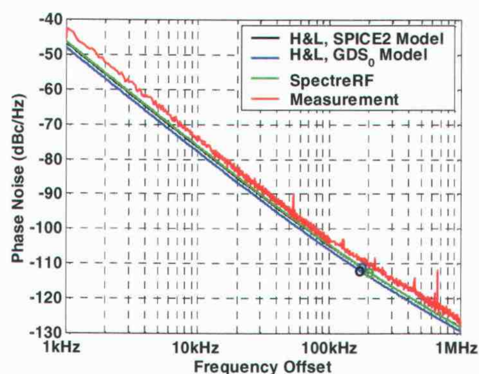


Figure J.3 Measurements versus simulations for V_{DD}=3.5V.

APPENDIX K Measured oscillation frequencies

V_{NMOS} (V)	V_{PMOS} (V)	Simulated (MHz)	Measured (MHz)
1.1	1.10	369.7	-
1.1	1.20	352.4	-
1.1	1.30	332.5	-
1.1	1.40	306.2	236.2
1.1	1.50	258.5	165.2
1.1	1.60	189.3	147.2
1.1	1.70	165.6	188.0
1.1	1.80	202.9	246.8
1.1	1.90	261.2	273.0
1.1	2.00	283.4	286.0
1.1	2.10	293.9	294.2
1.1	2.20	298.2	297.5
1.2	1.10	388.3	347.0
1.2	1.20	366.8	308.1
1.2	1.30	336.6	242.8
1.2	1.40	281.0	197.8
1.2	1.50	229.1	184.0
1.2	1.60	203.9	220.7
1.2	1.70	217.8	279.5
1.2	1.80	282.7	308.1
1.2	1.90	313.1	325.2
1.2	2.00	328.1	335.0
1.2	2.10	336.1	339.9
1.2	2.20	339.4	343.2
1.3	1.10	397.5	320.3
1.3	1.20	363.2	266.4
1.3	1.30	311.7	233.8
1.3	1.40	268.1	222.3
1.3	1.50	242.2	251.7
1.3	1.60	243.3	307.3
1.3	1.70	297.4	338.3
1.3	1.80	336.4	354.6
1.3	1.90	355.3	364.4
1.3	2.00	365.8	371.0
1.3	2.10	371.5	372.6
1.3	2.20	373.8	374.2
1.4	1.10	389.7	295.8
1.4	1.20	345.9	268.1
1.4	1.30	306.2	259.9
1.4	1.40	280.0	282.8
1.4	1.50	274.0	328.5
1.4	1.60	308.4	356.3
1.4	1.70	352.5	372.6
1.4	1.80	374.5	380.0
1.4	1.90	385.8	385.7
1.4	2.00	391.8	388.9
1.4	2.10	394.9	390.6
1.4	2.20	396.1	390.6
1.5	1.10	380.1	305.6
1.5	1.20	343.4	295.8
1.5	1.30	317.2	308.9
1.5	1.40	306.4	341.6
1.5	1.50	321.9	364.4
1.5	1.60	360.8	379.1

V_{NMOS} (V)	V_{PMOS} (V)	Simulated (MHz)	Measured (MHz)	V_{NMOS} (V)	V_{PMOS} (V)	Simulated (MHz)	Measured (MHz)
1.5	1.70	384.8	387.3	1.6	1.40	340.5	366.1
1.5	1.80	396.6	391.4	1.6	1.50	364.1	378.3
1.5	1.90	402.9	395.5	1.6	1.60	388.2	387.3
1.5	2.00	406.3	396.3	1.6	1.70	401.5	393.0
1.5	2.10	408.0	397.1	1.6	1.80	408.8	397.1
1.5	2.20	408.7	397.1	1.6	1.90	413.0	399.6
1.6	1.10	379.5	326.9	1.6	2.00	415.3	401.2
1.6	1.20	353.1	329.3	1.6	2.10	416.5	402.0
1.6	1.30	338.5	345.6	1.6	2.20	424.3	402.8

Table K.1 Oscillation frequencies of the high speed Maneatis load oscillator versus bias.

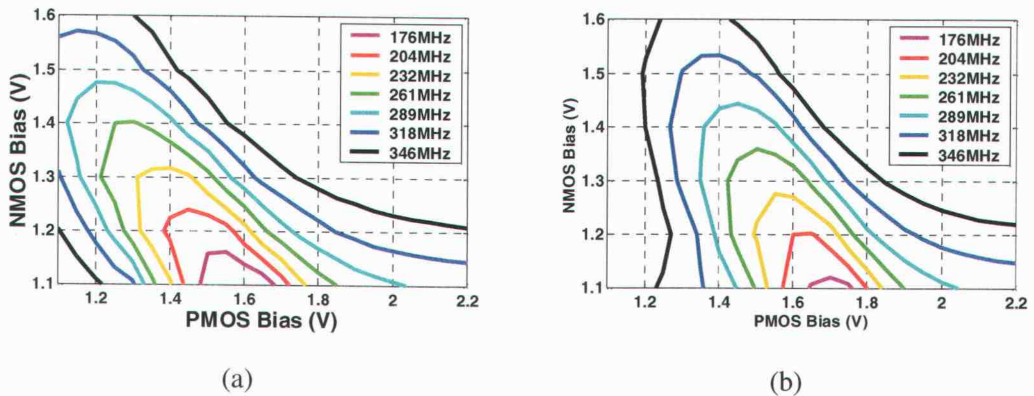


Figure K.1 (a) Measured and (b) simulated oscillation frequencies of the high-speed Maneatis load oscillator.

V_{NMOS} (V)	V_{PMOS} (V)	Simulated (MHz)	Measured (MHz)	V_{NMOS} (V)	V_{PMOS} (V)	Simulated (MHz)	Measured (MHz)
1.1	1.10	357.0	-	1.3	1.60	141.4	139.0
1.1	1.20	334.1	-	1.3	1.70	125.7	125.5
1.1	1.30	311.1	-	1.3	1.80	116.7	118.2
1.1	1.40	286.3	-	1.3	1.90	111.8	114.7
1.1	1.50	252.6	280.0	1.3	2.00	109.5	112.7
1.1	1.60	171.3	180.2	1.3	2.10	108.5	114.7
1.1	1.70	114.8	110.0	1.3	2.20	108.1	112.7
1.1	1.80	94.3	91.3	1.4	1.10	370.4	423.0
1.1	1.90	84.3	82.7	1.4	1.20	324.0	354.2
1.1	2.00	79.3	79.0	1.4	1.30	253.4	256.0
1.1	2.10	77.3	77.2	1.4	1.40	198.1	195.0
1.1	2.20	76.7	77.0	1.4	1.50	166.4	165.0
1.2	1.10	363.8	-	1.4	1.60	148.1	148.5
1.2	1.20	342.0	-	1.4	1.70	137.2	140.0
1.2	1.30	316.6	-	1.4	1.80	130.8	135.0
1.2	1.40	279.0	309.5	1.4	1.90	127.3	132.5
1.2	1.50	196.8	212.7	1.4	2.00	125.5	131.2
1.2	1.60	142.3	137.0	1.4	2.10	124.6	130.5
1.2	1.70	117.3	114.7	1.4	2.20	124.1	130.3
1.2	1.80	104.3	103.3	1.5	1.10	345.5	374
1.2	1.90	97.2	97.7	1.5	1.20	280.9	284.5
1.2	2.00	93.8	95.0	1.5	1.30	226.2	223.6
1.2	2.10	92.4	94.0	1.5	1.40	192.0	191.7
1.2	2.20	91.8	93.7	1.5	1.50	171.4	173.4
1.3	1.10	371.2	437.7	1.5	1.60	158.5	163.7
1.3	1.20	344.6	396.3	1.5	1.70	150.2	156.0
1.3	1.30	302.6	334.7	1.5	1.80	145.0	153.1
1.3	1.40	225.1	226.7	1.5	1.90	141.8	150.2
1.3	1.50	170.1	165.5	1.5	2.00	139.9	149.2

V_{NMOS} (V)	V_{PMOS} (V)	Simulated (MHz)	Measured (MHz)	V_{NMOS} (V)	V_{PMOS} (V)	Simulated (MHz)	Measured (MHz)
1.5	2.10	138.6	147.2	1.6	1.60	169.9	176.6
1.5	2.20	138.0	146.4	1.6	1.70	162.6	171.7
1.6	1.10	307.7	313.8	1.6	1.80	157.5	166.8
1.6	1.20	254.1	253.4	1.6	1.90	154.1	163.5
1.6	1.30	218.1	219.1	1.6	2.00	151.7	161.9
1.6	1.40	195.3	198.6	1.6	2.10	150.2	161.9
1.6	1.50	180.3	185.6	1.6	2.20	149.4	160.3

Table K.2 Oscillation frequencies of the cross-coupled load oscillator versus bias.

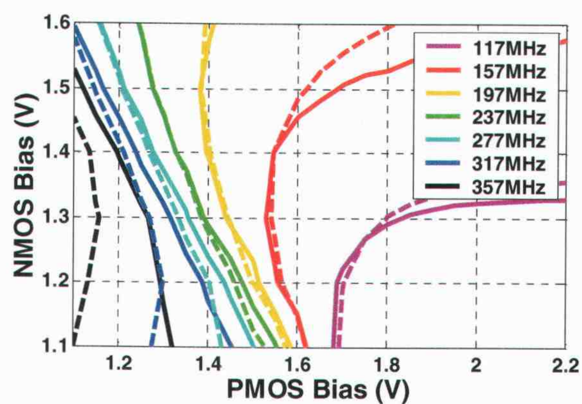


Figure K.2 Measured and simulated oscillation frequencies for the cross-coupled load oscillator. Solid lines show the measured data and dashed show the simulated data.

V_{NMOS} (V)	V_{PMOS} (V)	Simulated (MHz)	Measured (MHz)	V_{NMOS} (V)	V_{PMOS} (V)	Simulated (MHz)	Measured (MHz)
1.2	1.40	399.6	-	1.4	1.80	43.8	89
1.2	1.50	356.5	370.7	1.4	1.90	57.6	65.5
1.2	1.60	250.6	214	1.4	2.00	52.1	45.5
1.2	1.70	97.7	95	1.5	1.40	216.7	188
1.2	1.80	79.5	81	1.5	1.50	158.7	157.5
1.2	1.90	27.1	61	1.5	1.60	132.2	136.5
1.2	2.00	50.3	41	1.5	1.70	111.3	114.5
1.3	1.40	396.5	413.3	1.5	1.80	54.6	90
1.3	1.50	298.7	256.7	1.5	1.90	65.5	67.5
1.3	1.60	128.8	122	1.5	2.00	52.8	49
1.3	1.70	101.7	104	1.6	1.40	193.2	189
1.3	1.80	84.2	86	1.6	1.50	160.9	163.5
1.3	1.90	39.2	63.5	1.6	1.60	136.1	141.5
1.3	2.00	55.6	44	1.6	1.70	113.7	117.5
1.4	1.40	344.1	299.2	1.6	1.80	68.1	91.5
1.4	1.50	167.7	153.5	1.6	1.90	-	69.5
1.4	1.60	128.2	129	1.6	2.00	-	49.5
1.4	1.70	107.6	110				

Table K.3 Oscillation frequencies of the “vanilla” differential oscillator versus bias.

Supply Voltage (V)	Simulated (MHz)	Measured (MHz)
2.0	121.8	123
2.5	162.1	168
3.0	196.9	204
3.5	226.7	230

Table K.4 Measured and simulated oscillation frequencies of the H&L1 oscillator.

(a)

Supply Voltage (V)	Simulated (MHz)	Measured (MHz)
2.0	177.2	179.0
2.5	236.7	241.0
3.0		292.0
3.5	330.9	334.0

(b)

Supply Voltage (V)	Simulated (MHz)	Measured (MHz)
2.0		194.7
2.5		260.7
3.0		315.0
3.5		360.0

Table K.5 Measured and simulated oscillation frequencies of (a) the H&L1 and (b) the distributed oscillator.

Supply Voltage (V)	Simulated (MHz)	Measured (MHz)
2.0	203.2	203
2.5	275.7	277
3.0	338.4	348
3.5	392.3	401

Table K.6 Measured and simulated oscillation frequencies of the H&L3 oscillator.