AN ABSTRACT OF THE THESIS OF

Richard D. Lutz, Jr. for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on July 22, 2005.

Title: Inductors in High-Performance Silicon Radio Frequency Integrated Circuits: Analysis, Modeling, and Design Considerations

Abstract approved: Redacted for Privacy

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Spiral inductors are a key component of mixed-signal and analog integrated circuits (IC's). Such circuits are often fabricated using silicon-based technology, owing to the inherent low-cost and high volume production aspects. However, semiconducting substrate materials such as silicon can have adverse effects on spiral inductor performance due to the lossy nature of the material. Since the operating requirements of many high performance IC's demand reactive components that have high Quality Factor's (Q's), and are thus low loss devices, the need for accurate modeling of such structures over lossy substrate media is key to successful circuit design.

The Q's of commonly available off-chip inductors are in the range of 50-100 for frequencies ranging up to a few gigahertz. Since off-chip inductors must be connected through package pins, solder bumps, etc., which all contribute additional loss and thus lower the apparent Q of an external device, the typical on-chip Q requirement for a given RFIC design is generally lower than that for an off-chip spiral solution. However, a spiral inductor that was designed and fabricated originally in a low loss technology such as thin-film alumina may have substantially

worse performance in regard to Q if it is used in a silicon-based technology, owing to the conductive substrate. For this reason, it is imperative that semiconducting substrate effects be accurately accounted for by any modeling effort for monolithic spirals in RFICs.

This thesis presents a complete modeling solution for both single and multi-level spiral inductors over lossy silicon substrates, along with design considerations and methods for mitigation of the undesirable performance effects of semiconducting substrates. The modeling solution is based on Spectral Domain Approach (SDA) solutions for frequency dependent complex capacitive (i.e. both capacitance and conductance) parasitic elements combined with a quasi-magnetostatic field solution for calculation of the frequency dependent complex inductive (i.e. both inductance and resistance) terms. The effects of geometry and process variations are considered as well as the incorporation of Patterned Ground Shields (PGS) for the purpose of Q enhancement. Proposals for future extensions of this work are discussed in the concluding chapter.

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July 22, 2005

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Inductors in High-Performance Silicon Radio Frequency Integrated Circuits: Analysis, Modeling, and Design Considerations

by

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A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Doctor of Philosophy

Presented July 22, 2005
Commencement June 2006

Doctor of Philosophy thesis of Richard D. Lutz, Jr. presented on July 22, 2005

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ACKNOWLEDGMENTS

First I wish to thank my major professors, Dr. Andreas Weisshaar and the late Dr. Vijai K. Tripathi for providing me with the opportunity to do great research work with them and for giving constant support and encouragement during my years in graduate school.

Thanks is due to Drs. Raghu Settaluri, Tom Plant, Gabor Temes, and Graduate Council Representative Dr. Keith Levien for serving on my graduate committee and reviewing the manuscript.

I also thank my colleagues, Alok Tripathi, Ed Godshalk, Garth Sundberg, Chi-Young Lim and Yeon-Chang Hahm for their encouragement, useful discussions, manuscript review, and contributions to this work.

Many thanks go to Intel Corporation, who awarded me an Intel Graduate Fellowship for the 1998-1999 academic year, and to Agilent Technologies and the Electrical and Computer Engineering Department at Oregon State University for their financial and academic support.

Thanks is due to my father-in-law and mother-in-law, Glenn and Sylvia Kaizuka, for their constant encouragement.

Finally, endless thanks to my wife, Dawn, for her support and inspiration.

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DEDICATION

This thesis is dedicated to the memory of my parents, Richard and Dorothy Lutz, who provided me with the guidance, love and support for me to be successful in my educational endeavors as well as life in general.

INDUCTORS IN HIGH-PERFORMANCE SILICON RADIO FREQUENCY INTEGRATED CIRCUITS: ANALYSIS, MODELING, AND DESIGN CONSIDERATIONS

1. INTRODUCTION

The advent of silicon-based Radio Frequency Integrated Circuits (RFICs) in the communications sector has led to a need for low-cost, small form factor components. To visualize this, consider the evolution of cellular telephone handsets, as shown in Figure 1.1, from the bulky, heavy and expensive phones that were used by a small percentage of the world population in the 1980's, to the small, lightweight phones of today used by millions of people worldwide. On the left side of Figure 1.1 is the Motorola© [1] DynaTAC 8000X, the world's first commercial cellular telephone, which had a retail price of approximately $3,500 and weighed 28 ounces, while the right side shows an example of a modern cellular phone, which typically weighs 3 to 4 ounces and has a retail price in the range of $100 - $200. In addition to reduced-size, low-cost RFIC components, there is also demand within the communications industry for higher levels of integration that result in reduced component count for a given product. One method to lower the component count is to integrate passive devices, such as inductors and capacitors that are often implemented as off-chip components, onto the semiconductor die. This reduces the assembly time and cost for equipment manufacturers. The need to place passive components on an integrated circuit brings about different design issues than for traditional off-chip components owing to the fact that integrated circuits are fabricated on semiconducting substrates (i.e. silicon) rather than

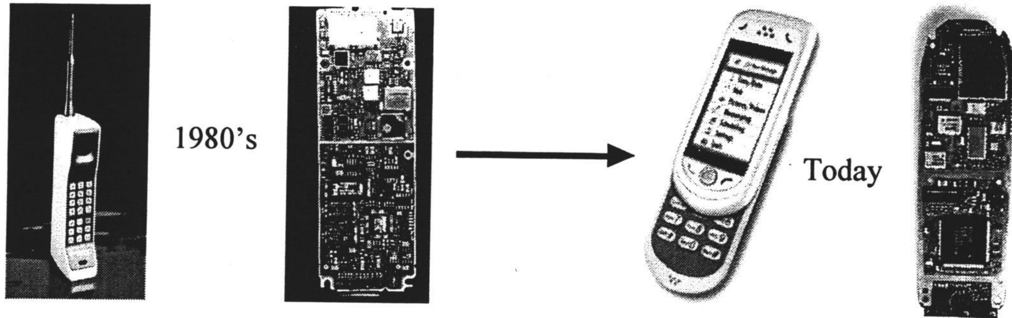


FIGURE 1.1. Evolution of cellular telephone handsets.

low-loss materials such as alumina, duroid or semi-insulating Gallium Arsenide (GaAs). An illustration of a spiral inductor integrated onto a semiconductor die is shown in Figure 1.2.

Quality factor is traditionally defined as the ratio of angular frequency times energy stored to the power loss [2]:

$$Q = \frac{\omega U}{W} \tag{1.1}$$

where U represents the sum of electric and magnetic field energy storage and W is the energy loss per second, or power loss. For purposes of spiral inductors in integrated circuits, the industry-standard definition for Q as a figure of merit is given as

$$Q = \frac{\Im\left[Z_{\text{in}}\right]}{\Re\left[Z_{\text{in}}\right]} \tag{1.2}$$

where Z_{in} is the input impedance of the inductor at a given frequency for the desired operating condition (i.e. single-ended or differential excitation), and $\Im[]$

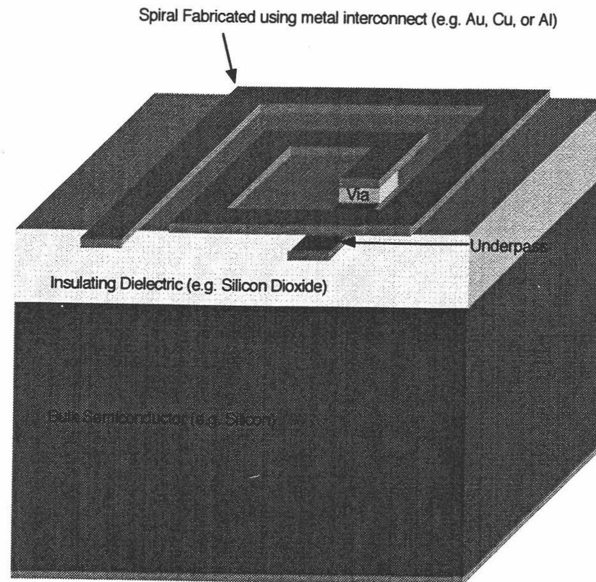


FIGURE 1.2. Example of spiral inductor integrated onto semiconductor die.

and $\Re[]$ denote the imaginary and real parts of a complex number, respectively. This expression is derived from the formula for Q of a series RLC resonant circuit at its resonant frequency, ω_0,

$$Q_{\text{series-RLC}} = \frac{\omega_0 L}{R}. \tag{1.3}$$

Since an inductor is often used as part of a resonant circuit, the ratio of its effective inductance times angular frequency to the effective resistance is indicative of its performance in such a circuit if the resonating capacitor is assumed to be ideal.

High-performance RFICs designed for use in communication devices, such as hand-held units (e.g. cellular telephones) and wireless local area network (WLAN) devices, in general require high Q passive components to enable them to adhere to the strict phase-noise and bandwidth requirements of modern telecom-

munications standards. Hence, the Voltage Controlled Oscillator (VCO) LC tank-circuits and matching networks used in RFICs must use high-Q inductors and capacitors. Often, the limiting factor for RFICs fabricated on silicon is the Q of the inductors, since the on-chip capacitors generally do not interact as much with the silicon substrate. Capacitors are usually of the Metal-Insulator-Metal (MIM) variety, and thus the majority of the electric field is vertical and confined to the upper-layers of dielectric material. Conversely, inductors are traditionally fabricated on-chip using a spiral pattern on the upper layers of metal for the process, resulting in a magnetic field that penetrates deep into the semiconducting substrate below as well as the space above the spiral, which is usually some sort of packaging material such as plastic. Semiconductors contain free charge, and when these charges are moved by the electric fields and electro-motive forces (EMF's) induced by the spiral inductor, the net effect on inductor performance is to lower its Q as a result of the increased power dissipation.

Often, spiral inductors in an RFIC are the most easily recognizable feature on the die, owing to their relatively large size compared to the transistors and other components on the chip. Since the goal of industry is not only to produce high performance chips, but to also offer them to customers at the lowest possible price, the overall size of a silicon chip is, of course, a key concern for semiconductor manufacturers. Methods for reducing the 'real-estate' occupied by on-chip inductors are thus a high priority for the RFIC industry. One way to accomplish such an area reduction is the use of multiple metal layers offered by modern silicon fabrication processes to create 3-D designs that have smaller footprints than typical single-level spirals with the same inductance value.

While the Q's of on-chip inductors are often inferior to off-chip components such as air-coil inductors, the cost savings and simplified circuit design aspects

make on-chip integration attractive to manufacturers. Also, the manufacturing tolerances of on-chip components fabricated in a typical silicon process are generally much tighter than those of external off-chip components, furthering the argument for moving components such as inductors onto the die. Unlike an off-chip inductor, an inductor fabricated on-chip does not require connection through package pins and bondwires, and thus the parasitics associated with using off-chip inductors are eliminated when an on-chip solution is used. This lack of package parasitics translates to a lower on-chip Q requirement than that of an off-chip spiral inductor, since the effective Q on the die of off-chip spirals is lowered by the package parasitic resistance and capacitance. However, the Q's to which on-chip spirals must aspire are still relatively large for high performance chip designs. Hence, accurate modeling and design of on-chip spiral inductors are imperative for ensuring successful RFIC design.

The conventional modeling techniques used for monolithic spiral inductors fabricated in low-loss media are not adequate for spiral inductors in a lossy substrate environment such as silicon. Because silicon is a semiconducting material by nature, there is often significant power loss due to conduction currents in the bulk substrate when a spiral inductor is energized above it. The conduction and displacement currents in the bulk substrate may be decomposed into longitudinal and shunt components and analyzed separately, making the model formulation more straightforward and intuitive. The longitudinal current components result mainly from magnetically induced EMF's by virtue of the magnetic field produced by the spiral inductor, whereas the vertical current components are a product of the vertical electric fields produced by the finite voltage excitation driving the inductor. Thus, for conditions where the substrate dimensions are small compared to wavelength, quasi-magnetostatic and quasi-electrostatic solution techniques may be

applied for the longitudinal and shunt current components respectively. In terms of potentials, the problems reduce to one of magnetic vector potential and one of electric scalar potential. The modeling methodology developed in this thesis addresses the limitations of conventional spiral inductor modeling techniques by including the impact of semiconducting substrates in terms of both longitudinal and shunt substrate current components.

Two methods for enhancing the performance of conventional planar spiral inductors in silicon technology are the implementation of multilevel structures and the use of patterned ground shields. Multilevel spirals make use of the multiple metal level systems offered by most silicon-based fabrication processes and allow a high inductance per unit area to be obtained owing to the high coupling factor between the metal levels where interlayer dielectric thicknesses are on the order of 1-2 microns. Patterned ground shields generally consist of an arrangement of conductive fingers that are orthogonal to the current flow in the inductor and can raise inductor Q by shunting much of the vertical conduction currents through a low loss path rather than through the lossy silicon substrate. The modeling methodology presented in this thesis was used to simulate various structures that utilize these two enhancement methods and evaluate their performance.

Since spiral inductors are such a key component of RFIC design, some of the recent research work has focused on optimization and improvement of inductor performance within various design constraints. The optimization technique presented in [3] relies on the use of extensive experimental data to develop fitting equations for the various spiral inductor model elements that are being optimized. Others have relied solely on experimental data and are able to determine trends in inductor performance through numerous process experiments [4]. Another recently published work includes many of the significant parasitic effects of semi-

conductor processes in the reported modeling tools, allowing for more accurate predictions and optimizations of performance for an array of process variables [5]. This is particularly useful when a semiconductor process is under development and the various process parameters such as doping levels and dielectric thicknesses are constantly changing, which, as a matter of course, leads to variations in inductor performance. Fabrication techniques that utilize air-suspended microstrip technology have been presented in [6] and show significant spiral performance improvement, although the high-volume manufacturability of such a process has yet to be shown. The use of patterned metallization, polysilicon and well/trench structures has also been shown to provide performance enhancements for certain process conditions, as presented in [7] and [8].

Experimental studies presented in [9] and [10] demonstrate design methods that exploit the inherent performance advantages of multilevel interconnect systems that have relatively thick metallization layers, namely constructing spiral inductors that utilize more than one layer of metal, which offers additional degrees of design freedom. The resulting structures are often referred to as dual-level or multi-level inductors. These types of inductors are a main focus of this thesis, particularly in terms of analysis, simulation and design optimization for RFICs. Such dual-level designs have also been fabricated and tested on Gallium Arsenide (GaAs) substrates in [11].

Chapter Two presents modeling techniques for both single and multilevel spiral inductors. Both single and coupled line structures are studied as fundamental components of spiral inductors. The use of a complex virtual ground plane approach is shown to be an efficient way to achieve accurate calculations of the parasitic effects of silicon on inductance and series resistance of microstrip lines and spiral inductor. The importance of inclusion of the so-called eddy-current

effects on inductance and series resistance of spiral inductors over high-loss substrates is examined.

Chapter Three investigates the effects of silicon process and spiral geometry on inductor performance. Specifically, variations in the parameters related to the fabrication process such as bulk resistivity, as well as differing inductor geometries, are considered as 'knobs' in determining a spiral inductor's quality factor and inductance at microwave frequencies.

Chapter Four focuses on design considerations for multilevel spiral inductors versus single level spiral inductors over silicon. The use of multilevel spiral inductors is proposed as another degree of design freedom and is the main focus of the chapter. The relationships between various designs and geometries and performance metrics such as Quality Factor (Q) and usable frequency range are presented.

Methods for mitigation of undesirable effects of silicon on inductor and interconnect performance are presented in Chapter Five. Various configurations and material properties are examined for so-called "patterned ground shields", which electrically shield passive components from semiconducting substrate effects without substantially affecting inductance.

Chapter Six presents conclusions and suggestions for future work in the area of high-performance inductors and other passive components on silicon. The ongoing design challenges faced by the wireless and datacom industries are considered in terms of their future modeling requirements for on-chip passive components.

2. MODELING TECHNIQUES FOR SINGLE AND MULTILEVEL SPIRALS

2.1. Introduction

RFIC designs in lossy media incorporating passive structures, such as microstrip spiral inductors, require modeling techniques that properly address the loss mechanisms involved, particularly those losses due to semiconducting substrate effects. Spiral inductors fabricated in Si-based circuits often have poor quality factors due to high-resistivity metallization and lossy substrates. In addition, substrate currents can adversely affect the inductance of a spiral inductor for certain frequencies and substrate conductivities. Figure 2.1 illustrates these substrate currents. However, because of the low-cost aspects of silicon technology, such structures remain attractive, thus prompting the formulation of accurate modeling and design techniques.

Although an inductor's primary function is to provide magnetic energy storage and a particular reactance at a given frequency, the geometries of spiral inductors fabricated in typical silicon-based technologies, in general, have dimensions such that their so-called 'parasitic' reactances and losses have a substantial impact on the overall inductor performance. Thus, the problem of modeling a spiral inductor in silicon is not one of simply calculating an inductance value from some closed-form approximation, finding the net DC resistance of the metal, and constructing a simple series 'LR' branch to represent the spiral inductor in an equivalent circuit. While the magnetic field is the quantity of interest for a spiral inductor, its interaction with surrounding substrate materials as well as with other parts of the spiral inductor itself give rise to losses that must be properly accounted for. Additionally, because spiral inductors in silicon are typically only

a few microns above a semiconducting material and are also in the presence of other dielectric media such as oxide, the parasitic capacitance terms must also be computed and included in any equivalent circuit model. This is particularly important if the predicted capacitance is expected to cause the inductor to self-resonate near its intended operating frequency. Self-resonance for a spiral inductor is defined as the condition when the inductor's input impedance is purely real, that is, there is zero reactance, neither inductive nor capacitive. The frequency at which this occurs is commonly known in the industry and research community as the self-resonant frequency, f_{SR}. The complicated nature of the electromagnetic fields and corresponding equivalent circuit representations for spiral inductors in silicon are primary reasons that full-wave 3D EM simulators are often employed by engineers and researchers for predicting and analyzing their behavior. However, the computational cost of full-wave solvers in terms of time can often be prohibitive, and thus there is a demand for less-complex, time-efficient modeling solutions for spiral inductors in a semiconducting substrate environment.

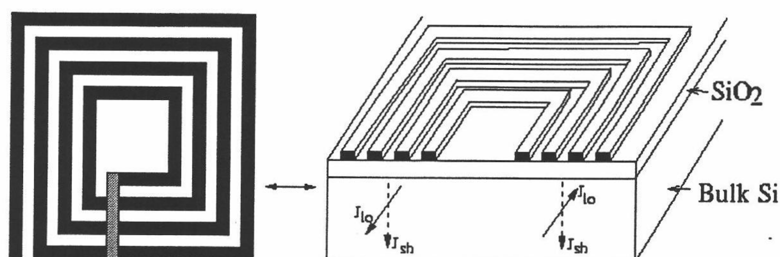


FIGURE 2.1. Substrate currents in Si-SiO_2-based spiral inductor structures.

Numerous design techniques for spiral inductors attempting to improve performance have been proposed and tested, including the use of multiple metallization layers [9, 10], high resistivity substrates [12], as well as air suspended

spirals [13]. One area of focus in this chapter is analysis and modeling of enhanced-inductance/area-ratio multilevel spiral inductors (MLS), such as those being fabricated currently in silicon-based RFICs and GaAs MMICs [10, 14].

Even though a number of experimental results have been reported, accurate distributed models and modeling methodologies for both single and multilevel spiral inductors incorporating all of the conductor and substrate losses and reactive coupling are generally not readily available. Often, as mentioned previously, computationally intensive 3-D EM simulators are invoked to model these structures. The modeling techniques for spiral inductors fabricated on lossy substrates in [9] and [15] address the shunt currents in the silicon substrate and prove to perform quite well for relatively high resistivity substrates such as those found in BiCMOS processes. However, longitudinal substrate currents can have a dominant effect in an environment such as CMOS, where substrate resistivities are on the order of $\rho = 0.01\ \Omega\text{−cm}$ ($\sigma = 10,000$ S/m), as addressed in [16]–[18]. Hence, a general analysis of the substrate effects and development of a modeling technique is necessary for both simple single-level spirals (SLS) as well as more complex multilevel spiral (MLS) structures, such as the designs described in [9], [13].

In this chapter, a complete modeling methodology for single (SLS) and multilevel spirals (MLS) on lossy substrate is presented. Two example structures, a SLS and MLS, are illustrated in Figures 2.2 and 2.3. The multilevel configuration in Figure 2.3 consists of two series-connected spirals and may be viewed as a top level coil, which spirals inward, placed directly on top of an identical coil on the lower level, which spirals outward in the same sense (e.g. clockwise). Such series-connected spirals are often referred to as enhanced inductance spirals, as they yield a substantial increase in base inductance value over a single level spiral of equal area due to the mutual inductance between the two coils, which is often, in

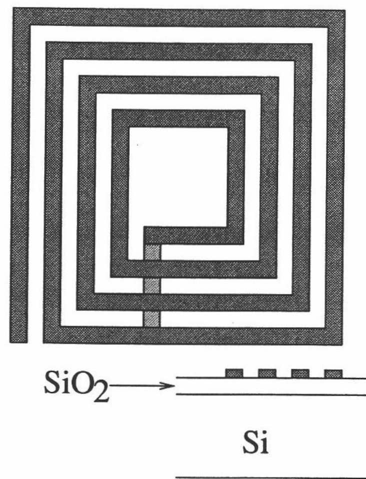


FIGURE 2.2. Example of Si-SiO_2-based single-level spiral inductor structure.

modern IC processes, nearly equal (e.g. 90-95%) to the inductance, L, of one of the coils, as shown in Figure 2.4, and thus $L_{\text{series}} = 2L + 2M =\sim (3.8...3.9) \times L$. The two spirals may also be connected in a parallel configuration, as shown in Figure 2.5, in order to lower series resistance, which effectively makes the spiral thicker and thus have a slightly lower inductance ($L_{\text{parallel}} = [L{+}M]^2/[2L{+}2M)] = [L + M]/2 =\sim (0.95...0.975) \times L$). The modeling methodology presented in this chapter takes into account all significant coupling effects between the different segments of a spiral structure as well as the lossy substrate. In particular, the models consider the substrate skin effect, which leads to higher losses and reduced inductance, especially for heavily doped CMOS substrates.

To briefly summarize the solution methods employed in the following models, a generalized flow-chart is shown in Figure 2.6. For parasitic capacitance/conductance calculations, Spectral Domain Approach (SDA) algorithms are employed that are able to handle multilayer substrates with multiple conductivities. Inductance and resistance calculations are carried out using common partial

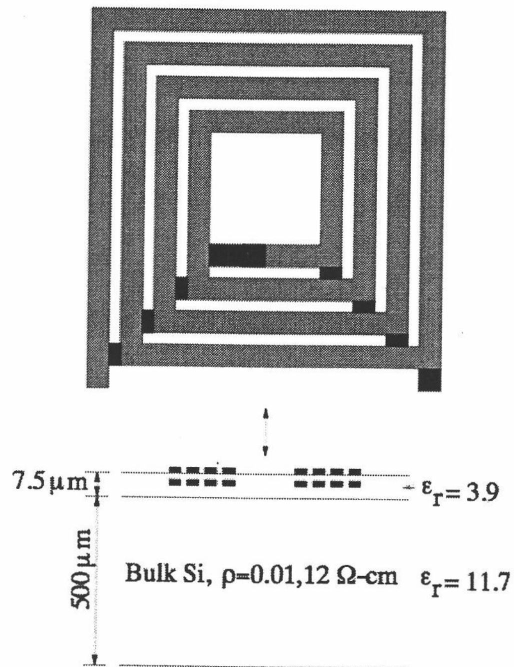


FIGURE 2.3. Example of a two level series-connected spiral inductor on lossy silicon substrate.

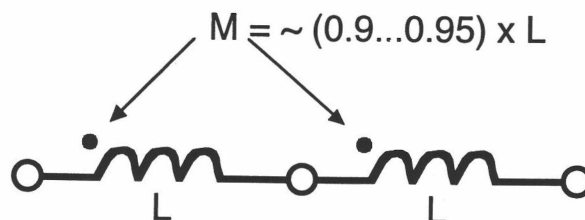


FIGURE 2.4. Schematic representation of series-connected spiral inductor showing typical mutual inductance achievable with modern IC processes.

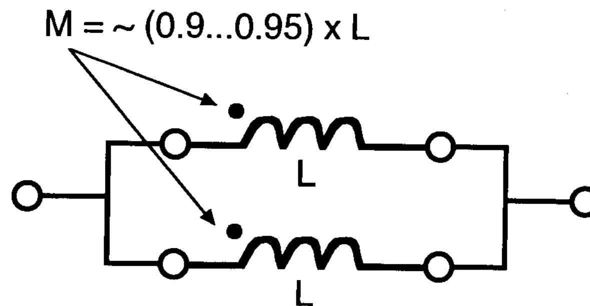


FIGURE 2.5. Schematic representation of parallel-connected spiral inductor showing typical mutual inductance achievable with modern IC processes.

inductance expressions combined with both closed-form skin effect formulae as well as spatial-domain or complex virtual ground plane height techniques [18] in order to include the semiconducting substrate effects. The complete equivalent circuit formulation can be described as a Partial Element Equivalent Circuit (PEEC) [19] type of distributed model, where the spiral inductor is partitioned and the corresponding self and mutual impedance and admittance terms are solved for using the methods outlined above.

The losses in a spiral inductor in silicon are primarily due to finite conductivity metallization and EM interaction with the semiconducting substrate. Because the modeling approach developed here addresses these mechanisms separately, the net effect of each loss component may be analyzed by selectively turning 'on' or 'off' the corresponding parts of the model (e.g. set conductor losses to zero in order to see the effect of longitudinal currents in the semiconductor on effective series resistance).

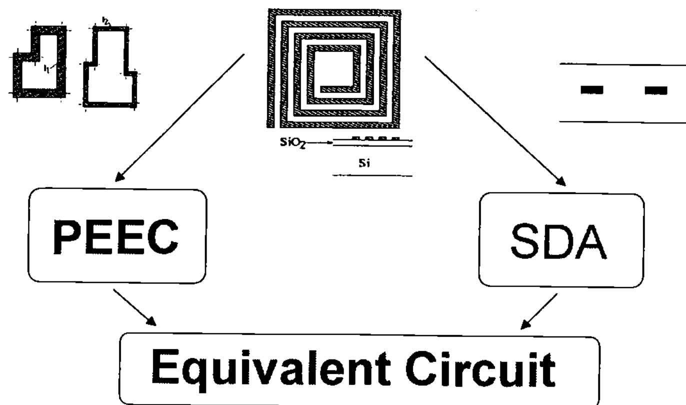


FIGURE 2.6. General flow-chart of spiral inductor modeling technique.

2.2. Limitations of Simple Compact Models for Low-Loss Spiral Inductors

For a general spiral inductor structure above a low-loss substrate, the modeling methodologies are well known and generally consist of simple lumped element equivalent circuits [20]. Partial inductances and capacitances may be determined from closed-form equations [19], [21] and, when included with the strip resistance, form the basis of an equivalent circuit representation for a low-loss structure. Additional losses due to conductor metallization skin depth and imperfect dielectrics may also be easily incorporated.

Likewise, equivalent circuit models for spiral inductors based in Si-SiO_2 systems have been developed for 'high'-resistivity substrates (e.g. 10 S/m) [9], [15]. Typically, the substrate losses are addressed via inclusion of shunt conductances to represent the silicon substrate and associated transverse (shunt) currents. An example of such an equivalent model is shown in Figure 2.7. This type of model proves to be sufficient for conductivities on the order of 10 S/m or less, frequen-

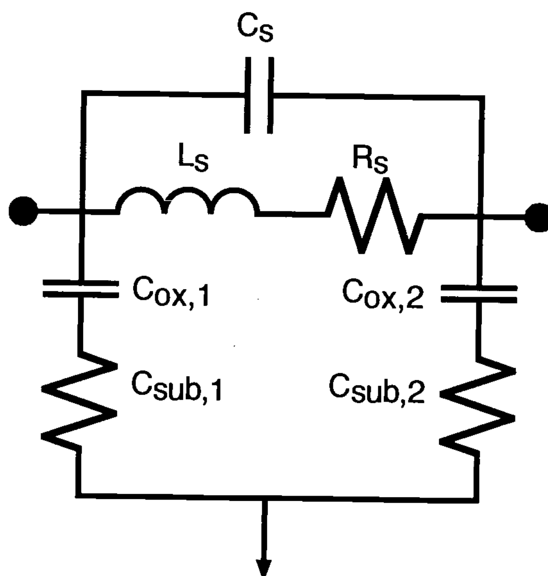


FIGURE 2.7. Simple equivalent circuit for 'high'-resistivity Si substrates.

cies in the low Gigahertz range (i.e. not broadband), and typical semiconducting substrate heights (e.g. $\sim$ 500 μm). However, when the product of conductivity and frequency ($\sigma\omega$) becomes significantly large and the skin depth, $\delta = 1/\sqrt{\pi\mu\sigma f}$, of the semiconducting substrate is small relative to its thickness, such equivalent circuit models for spiral inductors are not adequate. Thus, additional effects, particularly those due to longitudinal substrate currents, must also be addressed and included in an accurate model for these spiral inductors with higher conductivity substrates and frequencies of operation. These effects will be discussed in more detail later in this chapter.

2.3. Why Compact Models Fail for Some Spiral Inductors

In addition to the limitations of previously published models described in the preceding section, compact spiral inductor models also suffer from limitations associated with the overall simplicity of their topology. To best illustrate the limiting factors that cause compact inductor model topologies to fail, consider an ideal transmission line that is represented by a single-π-network. Above a certain frequency, this type of line model breaks down because it does not properly capture the distributed nature of a transmission line. The same can be said for a spiral inductor whose total line length (i.e. when it is "un-coiled") is on the order of a wavelength at its operating frequency. This supports the case for construction of more accurate distributed spiral inductor models. A 'double-π' type model that yields better broadband accuracy was presented in [22]. This may be viewed as a compromise in terms of accuracy versus simplicity between the distributed modeling techniques presented in this thesis and the simple single-π inductor model.

2.4. Fundamental Modeling Techniques for Microstrip Structures on Silicon

Microstrip structures fabricated in conventional silicon technologies are a common component of many mixed-signal and analog integrated circuits. Spiral inductors along with simple single and coupled line structures are a class of microstrip devices. Because of the multiple conductivities and relative permittivities involved in modern silicon processes, the propagation characteristics of even a simple strip of metal are complex functions of frequency. Additionally, the lossy nature of semiconducting substrates at microwave frequencies has added to

the design difficulties. However, if microstrip can be successfully analyzed and modeled for a particular process over a wide range of geometries, then successful RFIC design is possible at frequencies above 1 GHz.

2.4.1. Analysis and Modeling of Single and Coupled MIS Structures

Consider the propagation characteristics of a Si-SiO_2 microstrip configuration as a basic element of the planar spiral inductor, as shown in Figure 2.8. The planar conductor is above a double layer substrate consisting of silicon dioxide (SiO_2, commonly referred to as simply 'oxide' for a silicon based process), over bulk silicon. As described in the literature [23], three fundamental modes, namely, slow-wave, skin-effect, and dielectric quasi-TEM, can propagate in such a system, each having a certain frequency range for a given set of material parameters and geometry. Of particular interest for the case of the microstrip spirals in technologies with relatively low bulk resistivity (i.e. 0.01 Ω-cm) is the skin-effect mode, which is characterized by significant longitudinal, often called 'eddy', currents that serve to increase the effective series resistance and also decrease the net inductance with increasing frequency. Many production CMOS processes today utilize such low resistivity bulk materials.

The skin-effect mode [23] exists when the skin depth, δ, of the substrate material is on the same order as or less than the semiconducting substrate height. The quantity δ is calculated by

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}, \tag{2.1}$$

and represents the depth at which current density in a conductor is reduced to $1/e$ of its value at the surface, as well as the effective thickness of a conductor

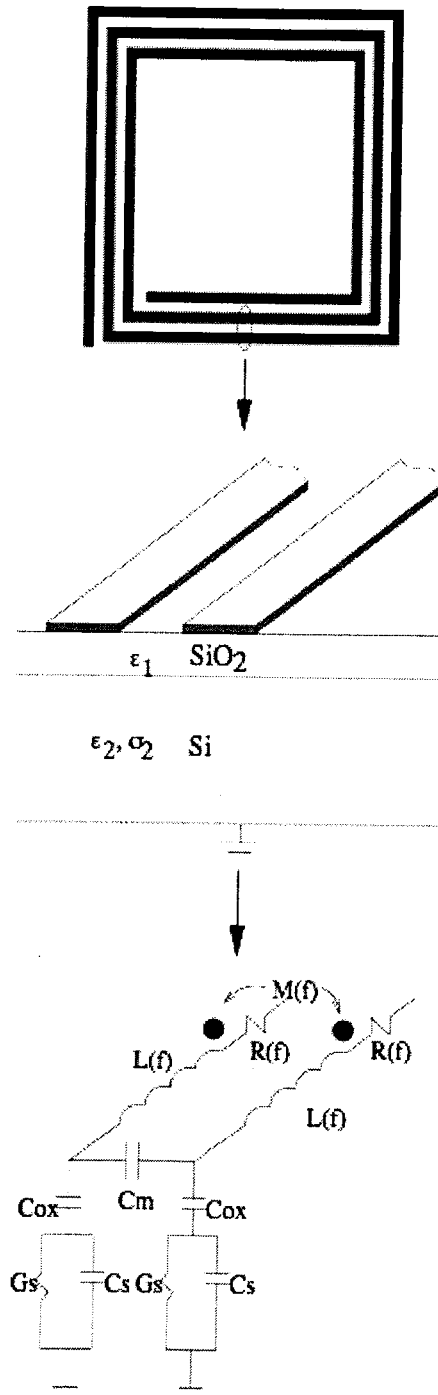


FIGURE 2.8. Equivalent circuit for $Si\text{-}SiO_2$ microstrip coupled lines in skin effect mode.

at a particular frequency for purposes of resistance calculations. In other words, with increasing frequency, the semiconducting substrate begins to behave as a lossy conductor wall and the longitudinal currents, which lower inductance per-unit-length, are closer to the substrate/oxide interface. This in turn yields an inductance and associated loss that are both frequency dependent. An equivalent circuit model for a Si-SiO_2 coupled microstrip line configuration is shown in Fig. 2.8. The capacitances, both shunt and nearest-neighbor line-to-line, and shunt conductances ares determined via a quasi-static Spectral Domain Analysis (SDA) [24] with complex dielectric constants to represent the semiconducting layers. The equivalent shunt elements in the common $C_{ox} - G_s||C_s$, or simply C-G-C, topology may be determined by evaluating the microstrip structure using SDA at one frequency and then calculating the element values of the corresponding equivalent circuit subject to the relationship:

$$G_s = \frac{\sigma_s}{\epsilon_s} C_s. \tag{2.2}$$

The relationship in 2.2 can be derived by examining the formula for capacitance and conductance in terms of the field quantities for charge, current and electric field. Assuming that the silicon/oxide interface is an equipotential plane, a potential difference V may exist between this plane and the ground plane below, as shown in Figure 2.9. The expression for conductance may be written as

$$\begin{aligned} G_s &= \frac{I}{V} \\ &= \frac{\oint_S \mathbf{J} \cdot \mathbf{dS}}{V} \\ &= \frac{\oint_S \sigma_s \mathbf{E} \cdot \mathbf{dS}}{V}, \end{aligned} \tag{2.3}$$

while for capacitance,

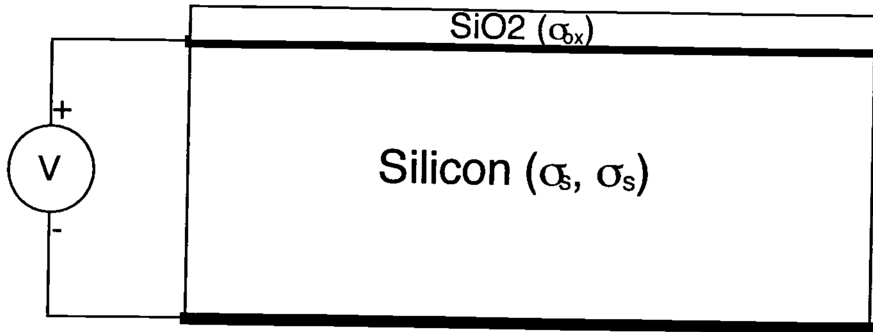


FIGURE 2.9. Illustration of voltage applied across silicon substrate in Equations 2.3-2.4.

$$
\begin{aligned}
C_s &= \frac{Q}{V} \\
&= \frac{\oint_S \mathbf{D} \cdot \mathbf{dS}}{V} \\
&= \frac{\oint_S \epsilon_s \mathbf{E} \cdot \mathbf{dS}}{V},
\end{aligned} \tag{2.4}
$$

and hence,

$$
\begin{aligned}
\frac{G_s}{C_s} &= \frac{\oint_S \sigma_s \mathbf{E} \cdot \mathbf{dS}}{\oint_S \epsilon_s \mathbf{E} \cdot \mathbf{dS}} \\
&= \frac{\sigma_s}{\epsilon_s}
\end{aligned} \tag{2.5}
$$

This C-G-C configuration yields a frequency-dependent total capacitance and conductance that is in good agreement with SDA results over a broad range of frequencies. Distributed series resistances and inductances (including mutual terms) may be calculated using an SDA algorithm [25] or a spatial domain solution [26] (see Appendix B) in conjunction with a modified Partial Element Equivalent Circuit (PEEC) [19] methodology that includes frequency dependence to account for the skin effect mode. The frequency-dependent series resistances incorporate the

skin effect in the finite thickness metallization [27] as well as loss in the semiconducting substrate. The formula used for the metallization skin effect for a conductor of thickness, t, is given by

$$R_{\text{cond.,skin}} = R_{DC} \cdot \Re\left\{ \frac{\gamma t(1 - e^{-2\gamma t} r)}{1 - e^{-2\gamma t}} \right\}, \tag{2.6}$$

where

$$\gamma = \sqrt{j\omega\mu\sigma_{\text{cond.}}} \tag{2.7}$$

$$r = \frac{\eta_0 - \sqrt{j\omega\mu/\sigma_{\text{cond.}}}}{\eta_0 + \sqrt{j\omega\mu/\sigma_{\text{cond.}}}} \tag{2.8}$$

$$\eta_0 = 120\pi \ (\Omega). \tag{2.9}$$

This formula for $R_{\text{cond.,skin}}$ is valid for frequencies at which the skin depth, δ, is less than t, that is, when

$$f \geq \frac{1}{\pi\mu\sigma_{\text{cond.}} t^2}. \tag{2.10}$$

The substrate losses due to longitudinal currents are computed by solving the magnetic vector potential equation in each layer i [26]

$$\nabla^2 A_{zi}(x, y) = j\omega\mu_0\sigma_i A_{zi}(x, y) \tag{2.11}$$

where z is the direction of propagation, subject to the appropriate boundary conditions (e.g. $A_z = 0$ on the ground plane). In the semiconducting substrate region, the current density is computed as

$$J_z(x, y) = -j\omega\sigma_{sub} A_z(x, y) \tag{2.12}$$

Fig. 2.11 shows the current density below the oxide as a function of frequency and depth for a typical Si-SiO$_2$ microstrip structure, as shown in Figure 2.10 with $h_{ox} = 4$ μm, $h_{sub} = 120$ μm, and $\sigma_{sub} = 10^4$ S/m. Similarly, Fig. 2.12 displays the normalized longitudinal current density, $\bar{J}_z$, in a cross section of the substrate

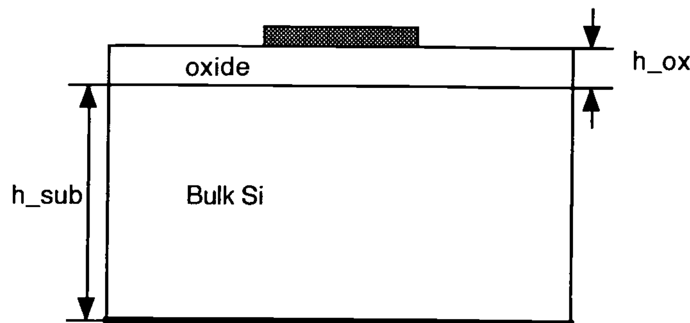


FIGURE 2.10. Example Si-based microstrip showing definition of h_{ox} and h_{sub}.

for various frequencies. It can be deduced that there is current crowding in the vertical dimension at the substrate/oxide interface, and also in the horizontal dimension in the area beneath the strip, as evidenced by the overall magnitude increase of the peak longitudinal substrate current density with frequency.

2.4.2. Complex Virtual Ground Plane Height and Expansion to Multilayer Substrates

As can be deduced from the preceding section, the effect of longitudinal substrate currents on microstrip structures fabricated in semiconducting substrate environments must be accounted for properly. One method for inclusion of the semiconducting substrate's effect on inductance is to utilize the portion of Wheeler's Incremental Inductance Rule [28] relating to inductance, which states that the effective inductance of a device over a conductor is equal to inductance calculated with the assumption that the conductor below is perfectly conducting (i.e. perfect ground plane) plus the increment of additional inductance gained if the conductor wall is receded by $\delta/2$, where δ is the skin depth. Also according

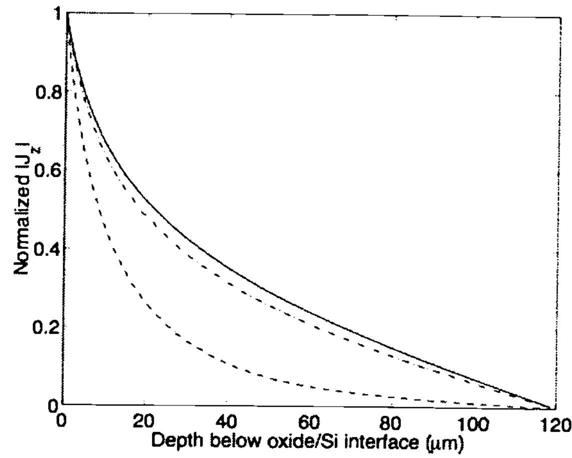


FIGURE 2.11. Normalized longitudinal substrate current density for f= 0.001 GHz (–), 0.1 GHz (-·) and 10 GHz (- -).

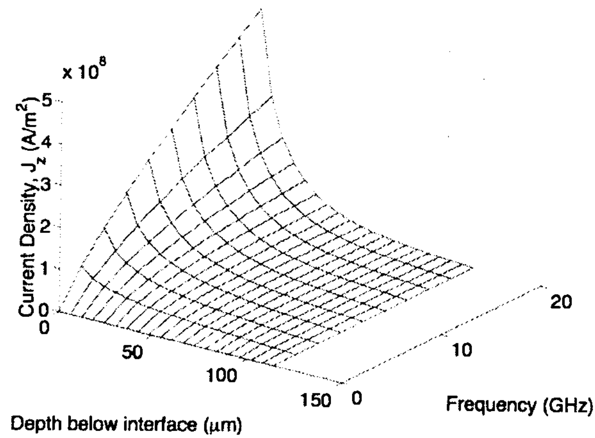


FIGURE 2.12. Longitudinal substrate current density vs. frequency and depth below oxide/Si interface.

to Wheeler's rule, the net increase in resistance is proportional to the change in inductance by the following relationship, $R_s = \omega \Delta L_s$. However, Wheeler's rule is not directly applicable to the 2-D and 3-D problems associated with spiral inductors, since the stated relationship between resistance and inductance does not hold for these complex cases where . But it will be shown that the 1-D parallel-plate waveguide case examined in the proceeding paragraphs is in exact agreement with Wheeler's rule, lending validity to this alternative approach.

While the formulation for solving the frequency-dependent per-unit-length series impedance for a microstrip structure over an insulator/semiconductor (MIS) substrate is a 2-D problem, a simplified 1-D approach for parallel-plate waveguides can provide accurate results through the use of a complex height virtual ground plane [29]. Recall that the magnetic field pattern in the semiconducting substrate can be characterized in terms of a frequency- and spatially-dependent magnetic vector potential function. If the microstrip problem is replaced by an ideal parallel-plate waveguide structure that is partially filled with a semiconducting material, the problem reduces to that of a 1-D magnetic vector potential. This approach is discussed in terms of its application to interconnects in [29] and [30], and is summarized in the following paragraphs. It has also been applied to inductors in [18] and [31], building upon the 'real' virtual ground plane approach developed in [16] and [32].

To derive the "complex height virtual ground plane" approach, first consider the inductance of an ideal air-filled parallel-plate waveguide, as shown in Figure 2.13,

$$L = \mu_0 \left[\frac{h}{w} \right] \tag{2.13}$$

where h and w are the total height and width, respectively. Note that the electric and magnetic fields only have one component each, E_x and H_y, respectively. If the

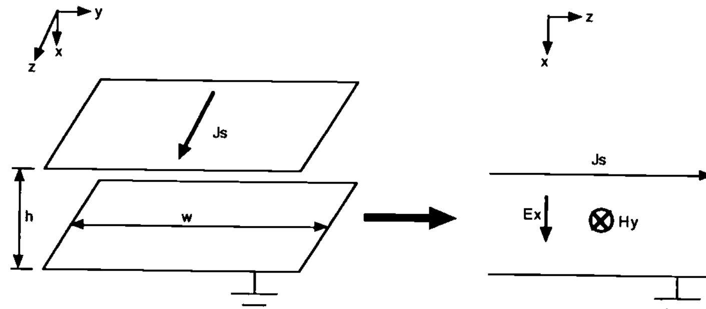


FIGURE 2.13. Ideal parallel-plate waveguide, front and side views.

bottom ground plane is replaced by a semi-infinite semiconducting bulk substrate, as illustrated in Figure 2.14, the net inductance, as well as series resistance due to the substrate's finite conductivity, will now be a function of frequency owing to the non-uniform frequency-dependent longitudinal current distribution in the semiconducting material. This problem may be solved in terms of the magnetic vector potential, in which the semiconducting substrate is replaced by a virtual perfectly conducting ground plane at a distance of α^{-1} below the semiconductor interface [29]. Here α is defined as

$$\alpha = \frac{(1+j)}{\delta}, \tag{2.14}$$

where δ is the skin depth for the semiconducting material, and $j = \sqrt{-1}$.

Upon examination of the preceding formulation, it is clear that as frequency approaches infinity, the net inductance approaches that of the case where the semiconducting substrate is perfectly conducting, since the skin depth is approaching zero. However, note that the distance α^{-1} is complex, which thus implies a complex inductance, or more generally a complex series impedance. Unlike the inductance, which drops and approaches a finite value as frequency goes

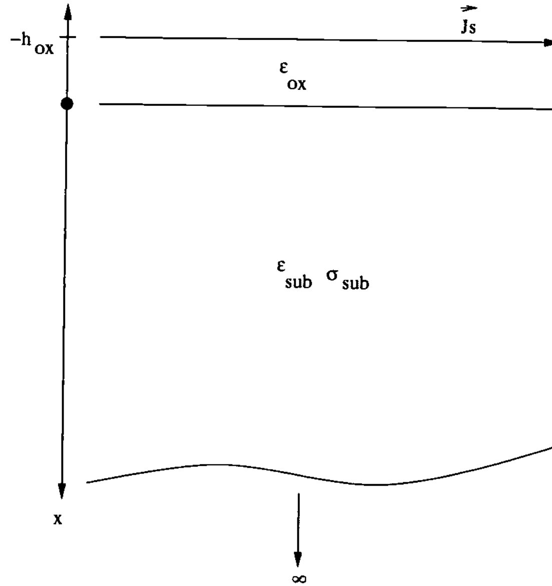


FIGURE 2.14. Parallel-plate waveguide with bottom plate replaced by semi-infinite semiconducting bulk substrate.

to infinity, the net resistance continues to increase as the square-root of frequency and is hence unbounded, as will be shown in the following derivation.

The solution for A_z in the semi-infinite semiconducting substrate is

$$A_z(x)|_{x\geq 0} = \frac{\mu_0 J_s}{\alpha} e^{-\alpha x} \tag{2.15}$$

where J_s is the assumed surface current density on the top plate of the waveguide. The series inductance per-unit-length for a parallel-plate waveguide filled with oxide of height, h_{ox}, may be computed as

$$\frac{L}{l} = \frac{A_z(-h_{ox}) - A_z(0)}{J_s w} \tag{2.16}$$

where

$$A_z(x)|_{x\leq 0} = -\mu_0 J_s x + A_{z0} \tag{2.17}$$

$$A_{z0} = A_z(0). \tag{2.18}$$

The solution for the case of oxide and semi-infinite semiconducting bulk is

$$\frac{L}{l} = \frac{A_z(-h_{ox}) - A_z(\infty)}{J_s w} \tag{2.19}$$

where

$$A_z(x)|_{x \leq 0} = -\mu_0 J_s x + \frac{\mu_0 J_s}{\alpha} \tag{2.20}$$

$$A_z(\infty) = 0. \tag{2.21}$$

This reduces to

$$\begin{aligned} \frac{L}{l} &= \frac{\mu_0 J_s (h_{ox} + \frac{1}{\alpha})}{J_s w} \\ &= \mu_0 \frac{h_{ox}}{w} + \mu_0 \frac{1}{\alpha w} \\ &= \mu_0 \frac{h_{ox}}{w} + (1-j)\mu_0 \frac{\delta/2}{w}. \end{aligned} \tag{2.22}$$

Clearly the solution for the complex series inductance consists of the ideal parallel-plate inductance for a waveguide of height, h_{ox}, plus a term that represents the complex inductance of the semi-infinite bulk semiconducting substrate,

$$\frac{L}{l} = \frac{L_{ox}}{l} + \frac{L_{sub}}{l}. \tag{2.23}$$

Upon examination of the secondary term,

$$\frac{L_{sub}}{l} = (1-j)\mu_0 \frac{\delta/2}{w} \tag{2.24}$$

the complex series inductance term for the semi-infinite substrate is observed to be that of a parallel-plate waveguide of height

$$h_{sub,eff} = (1-j)(\delta/2) \tag{2.25}$$

as shown in Figure 2.15, which is a complex value. Thus, the complex inductance for the entire waveguide may be represented as the solution for two plates

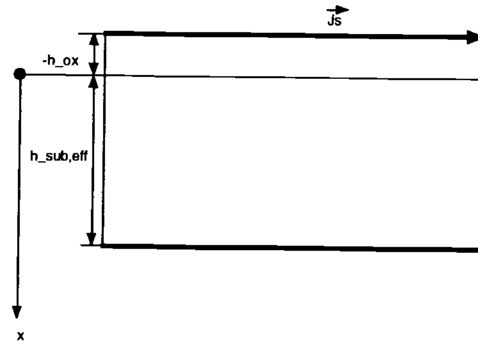


FIGURE 2.15. Illustration of effective substrate height for two-layer Si-filled parallel-plate waveguide.

separated by a complex distance h_{eff},

$$L_{\text{complex}} = \frac{L}{l} = \mu_0 \frac{h_{eff}}{w} \tag{2.26}$$

where

$$\begin{aligned} h_{eff} &= h_{ox} + h_{sub,eff} \\ &= h_{ox} + (1-j)(\delta/2). \end{aligned} \tag{2.27}$$

The resulting net complex series inductance for the entire waveguide may also be written in terms of a complex impedance per-unit-length,

$$Z_s = j\omega L_{\text{complex}} \tag{2.28}$$

$$= j\omega \left[\mu_0 \frac{h_{eff}}{w} \right]. \tag{2.29}$$

When divided into real and imaginary components, the net real inductance and resistance per unit length are computed as

$$\begin{aligned} L_s &= \frac{\Im\{Z_s\}}{\omega} \\ &= \frac{\Im\{j\omega L_{\text{complex}}\}}{\omega} \\ &= \Re\{L_{\text{complex}}\} \\ &= \mu_0 \left[\frac{d + (\delta/2)}{w}\right] \end{aligned} \tag{2.30}$$

$$\begin{aligned} R_s &= \Re\{Z_s\} \\ &= \Re\{j\omega L_{\text{complex}}\} \\ &= -\omega \Im\{L_{\text{complex}}\} \\ &= \mu_0 \omega \frac{\delta/2}{w} \end{aligned} \tag{2.31}$$

As discussed previously, Wheeler's Incremental Inductance Rule states that the contribution to net resistance from a finite conductivity ground plane is computed as

$$R_s = \omega \Delta L_s \tag{2.32}$$

where ΔL_s is the net increase in inductance due to magnetic field penetration into the conducting plane over the inductance of the same structure with a perfectly conducting ground plane. This incremental change in inductance, according to Wheeler's Rule, is equal to the increase resulting from a recession of the perfectly conducting plane by a distance equal to $\delta/2$. For the case of a parallel plate waveguide of height h_{ox} with a semi-infinite semiconducting substrate as the bottom conductor, the inductance will be, according to Wheeler,

$$\begin{aligned} L_s &= \mu_0 \frac{h_{ox}}{w} + \Delta L_s \\ &= \mu_0 \frac{h_{ox} + (\delta/2)}{w}. \end{aligned} \tag{2.33}$$

This is the same result already derived in Eq. 2.30. The net resistance should be, according to Wheeler's rule,

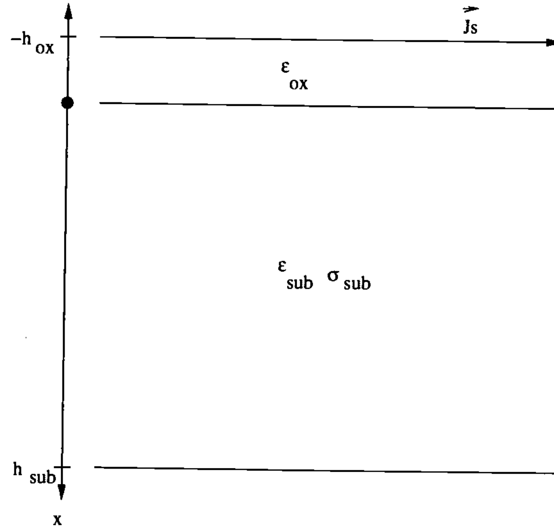


FIGURE 2.16. Parallel-plate waveguide partially filled with semiconducting substrate.

$$R_s = \omega \Delta L_s$$
$$= \omega \mu_0 \frac{(\delta/2)}{w}, \tag{2.34}$$

which is equivalent to Eq. 2.31. Thus, the formulation presented here for a parallel-plate waveguide with a semi-infinite semiconducting substrate as the bottom conductor is consistent with Wheeler's Incremental Inductance Rule.

A more practical case of the parallel-plate waveguide is that of an oxide layer over a finite thickness semiconducting substrate with ground plane on the backside, as illustrated in Figure 2.16. The effective height for this case is [30]

$$h_{eff,\text{groundplane}} = \frac{\delta}{2}(1-j)\tanh\left((1+j)\left(\frac{h_{sub}}{\delta}\right)\right)$$
$$= \frac{1}{\alpha}\tanh\left(\alpha h_{sub}\right) \tag{2.35}$$

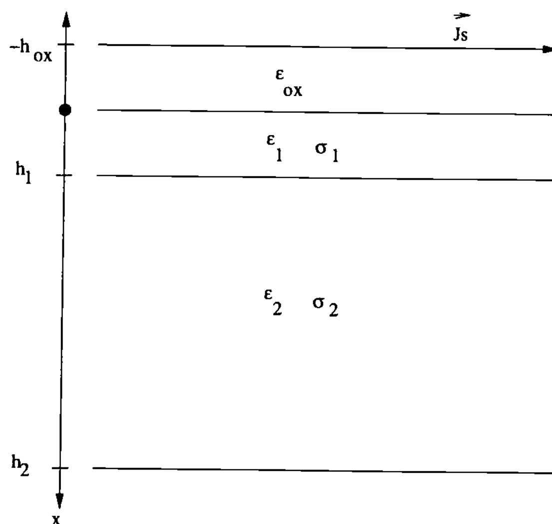


FIGURE 2.17. Parallel-plate waveguide partially filled with 2-layer semiconducting substrate.

Similarly, for the case of two different semiconductor layers, shown in Figure 2.17, the effective height is given by [30]

$$h_{eff,\text{2lyr-semi,groundplane}} = \frac{1}{\alpha_1}\left(\frac{\frac{1}{\alpha_2}\tanh(\alpha_2 h_2) + \frac{1}{\alpha_1}\tanh(\alpha_1 h_1)}{\frac{1}{\alpha_1} + \frac{1}{\alpha_2}\tanh(\alpha_2 h_2)\tanh(\alpha_1 h_1)}\right) \tag{2.36}$$

An examination of the two-layer semiconductor solution in Eq. 2.36 reveals that the equation is of the same form as that of the generalized input impedance of a series of cascaded transmission lines with arbitrary lengths and impedances with the end termination impedance equivalent to a short circuit [30]. As will be shown in the following section, this method can greatly simplify the problem of solving for the series impedance of interconnects over multilayer substrates as is typical in silicon process environments.

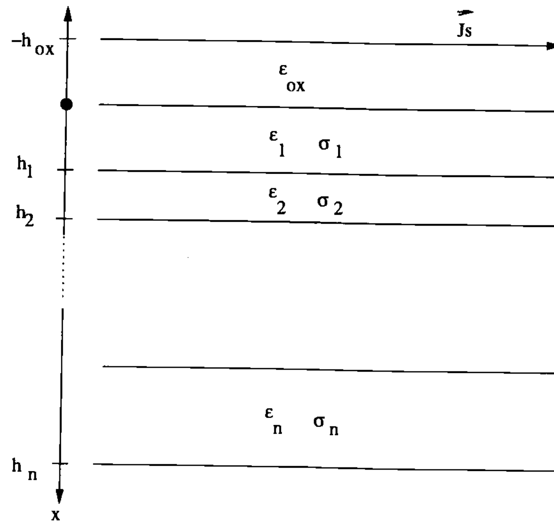


FIGURE 2.18. Parallel-plate waveguide partially filled with N-layer semiconducting substrate.

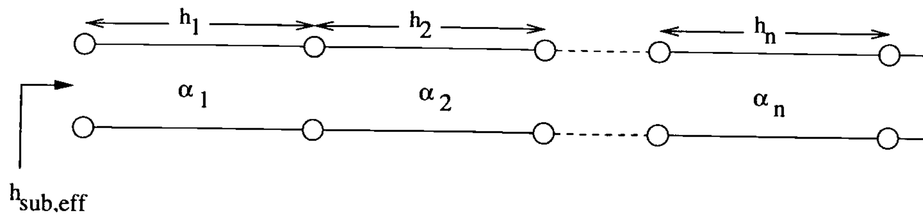


FIGURE 2.19. Illustration of transmission line impedance analogy used for computing h_{eff} for N-layer parallel-plate waveguide.

2.4.3. Using the Complex Virtual Ground Plane to Solve Microstrip Impedance Problems

In general, a microstrip-type structure requires some sort of 2D field solution or a closed-form expression in order to determine its propagation characteristics and line impedance. The technique presented in the previous section employs a ground plane spaced at a complex distance to represent a mutlilayer substrate. Many closed-form expressions already exist for single microstrip and even finite length strips above a ground plane [33]. One of the most common formulations for microstrip is presented in [34] and is given as

$$Z_0 = \frac{60}{\sqrt{\epsilon_e}} \ln\left(\frac{8h}{w} + \frac{w}{4h}\right) \quad \text{for} \quad w/h \leq 1$$

$$= \frac{120\pi}{\sqrt{\epsilon_e}\left[w/h + 1.393 + 0.667 \ln\left(w/h + 1.444\right)\right]} \quad \text{for} \quad w/h \geq 1 \tag{2.37}$$

$$\epsilon_e = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12h/w}} \tag{2.38}$$

If these expressions are evaluated for the case of an air dielectric ($\epsilon_r = 1$), then the inductance per-unit-length is given by

$$L_{\text{p.u.l.}} = \frac{Z_0}{c_0} \quad \text{(H/m)} \tag{2.39}$$

where c_0 is the speed of light in a vacuum. As in the case of the parallel-plate waveguide, the resulting inductance per-unit-length will be complex when the value for h is complex. This is true when there are semiconducting substrate layers present, implying a net series resistance per-unit-length, $R_{\text{p.u.l.}}$. The method for obtaining the frequency-dependent complex inductance for a single microstrip using this closed-form expression for impedance is as follows [29]:

$$L_{\text{p.u.l., complex}}(\omega) = \frac{Z_0\left(w/h(\omega)\right)}{c_0} \quad \text{(H/m)} \tag{2.40}$$

$$L_{s,\text{p.u.l.}}(\omega) = \Re\left\{L_{\text{p.u.l., complex}}\right\} \tag{2.41}$$

$$R_{s,\text{p.u.l}}(\omega) = -\omega\left[\Im\left\{L_{\text{p.u.l., complex}}\right\}\right] \tag{2.42}$$

where $h(\omega)$ is calculated from a formula such as Equation 2.36.

Although it was shown to be equivalent to a complex virtual ground plane height for the 1-D parallel-plate waveguide case, Wheeler's method is not appropriate for the 2-D and 3-D structures analyzed for spiral inductors. As stated previously, the substrate's effect on resistance is not necessarily directly proportional to the product of frequency and relative change in inductance when the electromagnetic fields involved are non-uniform. However, the closed-form expressions available for inductance are able to account for the 2-D or 3-D nature of the structure under analysis, and when combined with a ground plane spaced at a complex distance provide a higher level of accuracy when tested against the SDA algorithm [25] than what is predicted by Wheeler's rule. Additionally, the complex virtual ground plane method is much less computationally taxing and hence faster than SDA for complex inductance of interconnects, since it is used in conjunction with simple closed-form expressions.

The complex virtual ground plane height concept is applicable to coupled line structures as well, which are fundamental building blocks of spiral inductors. This will be discussed in later sections.

2.4.4. Proximity Effects on Resistance for Two Adjacent Lines

In addition to the influence of longitudinal currents in the silicon on effective series resistance of a microstrip, the relatively close proximity of additional metal traces running in parallel can also adversely affect the series loss terms. Figure 2.20 illustrates the current distribution for two parallel microstrips with the same current direction. In this case, a majority of the current flows in the outer edges of each conductor, due to the fact that the effective mutual inductance is

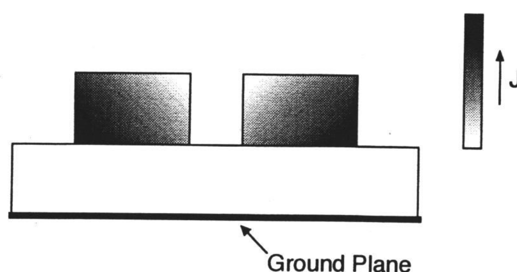


FIGURE 2.20. Current distribution in two parallel lines at high frequency.

largest in the area of the inner edges and thus the impedance in this inner region will consequently be higher relative to the outer edges. The proximity effect can be directly included in the spiral inductor model by subdividing each conductor cross-section into filaments, as demonstrated, for example, in [31]. However, this approach is computationally inefficient. On the other hand, this effect may be included in a coupled line model through the application of an effective complex current penetration depth for each conductor, which results in an effective complex separation distance between the parallel conductors. This method is considered as a topic for future work in Chapter 6.

2.4.5. Partial Inductance Calculations for Rectangular Bars

Since spiral inductors are made up of many finite length sections of metal, it is necessary to have a means for calculating the self and mutual inductances associated with these sections. The method presented by Hoer and Love in [33] for calculating the exact self and mutual inductance of rectangular conducting bars of arbitrary dimension is employed in the following modeling methodologies

and throughout this thesis. It is best summarized by referring to Figure 2.21 and the following expressions:

$$M_b = \frac{1}{bc} \int_P^{P+c} \int_0^b M_t dy_1 dy_2 \tag{2.43}$$

where

$$M_t = \frac{1}{ad} \int_E^{E+d} \int_0^a M_f dx_1 dx_2, \tag{2.44}$$

$$M_f = 0.001 \left[z \ln \left(z + \sqrt{z^2 + \rho^2} \right) - \sqrt{z^2 + \rho^2} \right]_{l_2+l_3-l_1, l_3}^{l_3-l_1, l_3+l_2} (z), \tag{2.45}$$

and

$$[f(z]_{s_2,s_4}^{s_1,s_3} (z) = \sum_{k=1}^{4} (-1)^{k+1} f(s_k). \tag{2.46}$$

Equation 2.45 is the closed-form solution for the mutual inductance between two filaments of current of arbitrary length and spacing, as shown in Figure 2.22. The expression for M_b is recognized to be the Neumann mutual inductance formula

$$M_{12} = 0.001 \int_{l_1} \int_{l_2} \frac{\mathbf{dl_1} \cdot \mathbf{dl_2}}{r} \tag{2.47}$$

integrated over the cross-sections of the two rectangular bars. Equation 2.43 may be computed explicitly by the following formulae [33]:

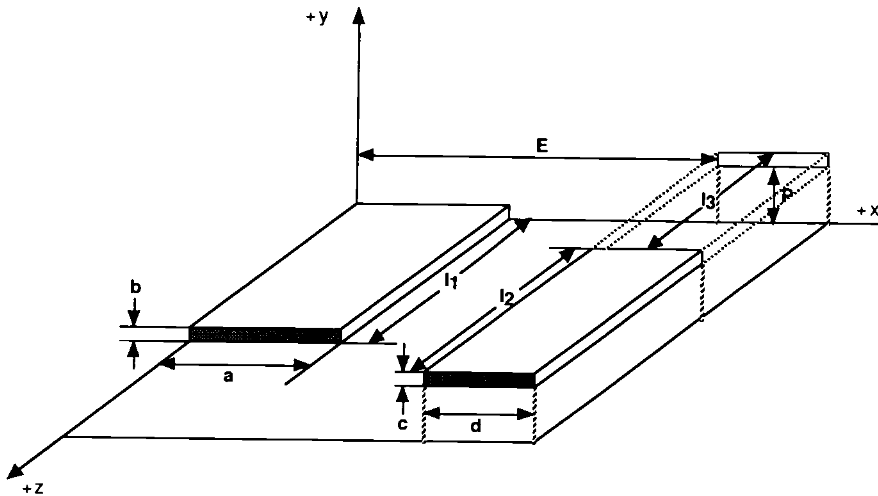


FIGURE 2.21. Two parallel rectangular bars for mutual inductance calculations.

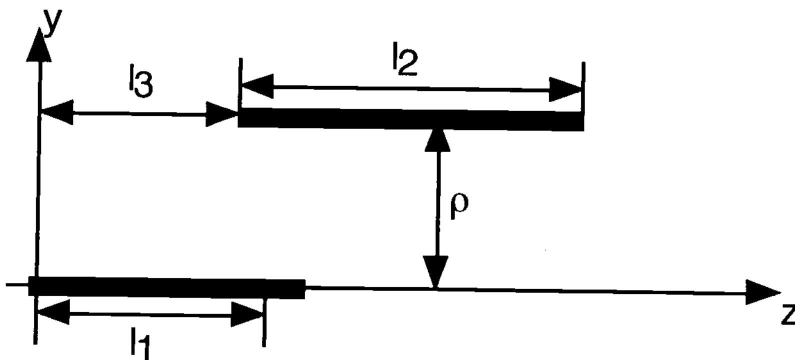


FIGURE 2.22. Two parallel filaments for mutual inductance calculation in Equation 2.45.

$$M_b = \frac{0.001}{abcd}\left[\left[\left[M(x,y,z)\right]_{E+d-a,E}^{E-a,E+d}(x)\right]_{P+c-b,P}^{P-b,P+c}(y)\right]_{l_3+l_2-l_1,l_3}^{l_3-l_1,l_3+l_2}(z) \tag{2.48}$$

$$\begin{aligned} M(x,y,z) = & \left(\frac{y^2z^2}{4} - \frac{y^4}{24} - \frac{z^4}{24}\right) x \ln\left(\frac{x+\sqrt{x^2+y^2+z^2}}{\sqrt{y^2+z^2}}\right) \\ & + \left(\frac{x^2z^2}{4} - \frac{x^4}{24} - \frac{z^4}{24}\right) y \ln\left(\frac{y+\sqrt{y^2+z^2+x^2}}{\sqrt{z^2+x^2}}\right) \\ & + \left(\frac{x^2y^2}{4} - \frac{x^4}{24} - \frac{y^4}{24}\right) z \ln\left(\frac{z+\sqrt{z^2+x^2+y^2}}{\sqrt{x^2+y^2}}\right) \\ & + \frac{1}{60}\left(x^4+y^4+z^4-3x^2y^2-3y^2z^2-3z^2x^2\right)\sqrt{x^2+y^2+z^2} \\ & - \frac{xyz^3}{6}\tan^{-1}\frac{xy}{z\sqrt{x^2+y^2+z^2}} - \frac{xy^3z}{6}\tan^{-1}\frac{xz}{y\sqrt{x^2+y^2+z^2}} \\ & - \frac{x^3yz}{6}\tan^{-1}\frac{yz}{x\sqrt{x^2+y^2+z^2}} \end{aligned} \tag{2.49}$$

$$\left[\left[\left[f(x,y,z)\right]_{q_2,q_4}^{q_1,q_3}(x)\right]_{r_2,r_4}^{r_1,r_3}(y)\right]_{s_2,s_4}^{s_1,s_3}(z) = \sum_{i=1}^{4}\sum_{j=1}^{4}\sum_{k=1}^{4}(-1)^{i+j+k+1} f(q_i,r_j,s_k) \tag{2.50}$$

Equation 2.48 can be summarized as the partial mutual inductance between two rectangular bars of arbitrary dimension and relative position, assuming a uniform current distribution in both cross-sections and one-dimensional current flow in the z-direction (see Fig. 2.21), with assumed return currents at an infinite distance from both conductors. While this may at first seem to be a substantial set of constraints, it is quite applicable to the geometries found in typical spiral inductor structures, where skin depths are still slightly larger than the conductor thicknesses at operating frequencies in the low gigahertz range and current flow is nearly confined to the lengthwise dimension for each straight section being analyzed.

Note that if in 2.48 the values of l_3, E and P are all set to zero, and if $a = d$, $b = c$, and $l_1 = l_2$, then the mutual inductance formula in 2.48 yields the partial self inductance of a rectangular bar with length l_1, width a and thickness

b. This realization provides insight into the meaning of self inductance for a single conducting bar, that it is simply the sum of the mutual inductances between all of the infinitesimal current filaments within the conductor. Clearly, if the conductor is assumed to be a perfect, zero-cross-section filament, this expression is invalid, since the kernel M_f becomes infinite. In this case, Equation 2.48 must be used with caution to ensure that none of the functions are approaching infinity, that is, that relative dimensions are not approaching that of a filament (i.e. $l_1 \gg a, b$).

Because Equation 2.48 is the cornerstone of all of the inductance calculations used in the modeling methodologies in this thesis, it was necessary to generate a programmed form of these expressions to allow them to be implemented in a simulation tool. Matlab© [35] was selected as the script-based language to accomplish this task. Appendix D contains the actual code for this function, aptly named '**mrebar.m**' for '**m**utual inductance between **re**ctangular **bar**s'.

2.5. Distributed Spiral Inductor Models

As stated previously, compact models have limitations in that they are not representative of the distributed nature of spiral inductors whose overall trace lengths are comparable in size with wavelength at their operating frequency. To this end, distributed models have been developed that allow for more accurate modeling and characterization of spiral inductors. This is often the preferred method when inductors are being prototyped and there is little or no measurement data available for the fabrication process being considered. All results in the following sections utilize a virtual ground plane approach, referred to as a modified PEEC approach, to calculate the effect of longitudinal substrate (eddy) currents on inductance, as illustrated in Figure 2.23. This approach was initially developed

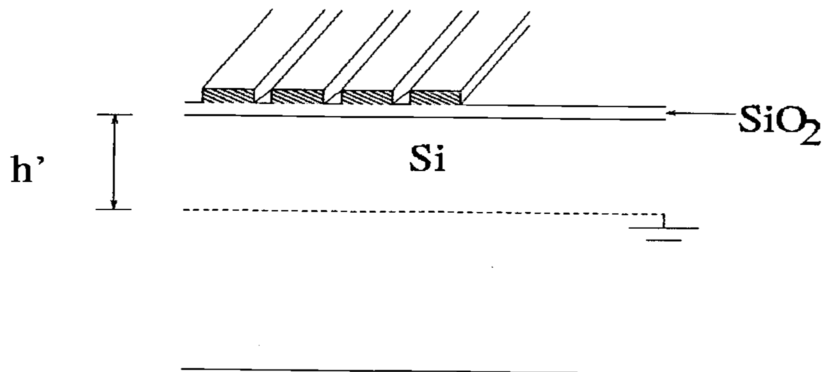


FIGURE 2.23. Illustration of virtual ground plane concept for inductance calculations.

in [16] and [32], and is different than that in [18] and [31] in that it utilizes a virtual ground plane at a real distance for inductance calculations rather than a complex distance that captures both inductive and resistive effects simultaneously. Models utilizing the complex virtual ground plane are presented later in this thesis.

The method for obtaining the effective ground plane height for inductance calculations consists of solving for the equivalent inductance at a given frequency for a single microstrip using the spatial-domain formulation in [26], then calculating the equivalent height, h, of an ideal microstrip with the same per-unit-length inductance in air (i.e. $\epsilon_r = 1$). Given the characteristic impedance of a single line in air with per-unit-length inductance, $L(\omega)$,

$$Z_0|_{\epsilon_r=1}(\omega) = L_{\text{p.}u.l.}(\omega)c_0, \tag{2.51}$$

then

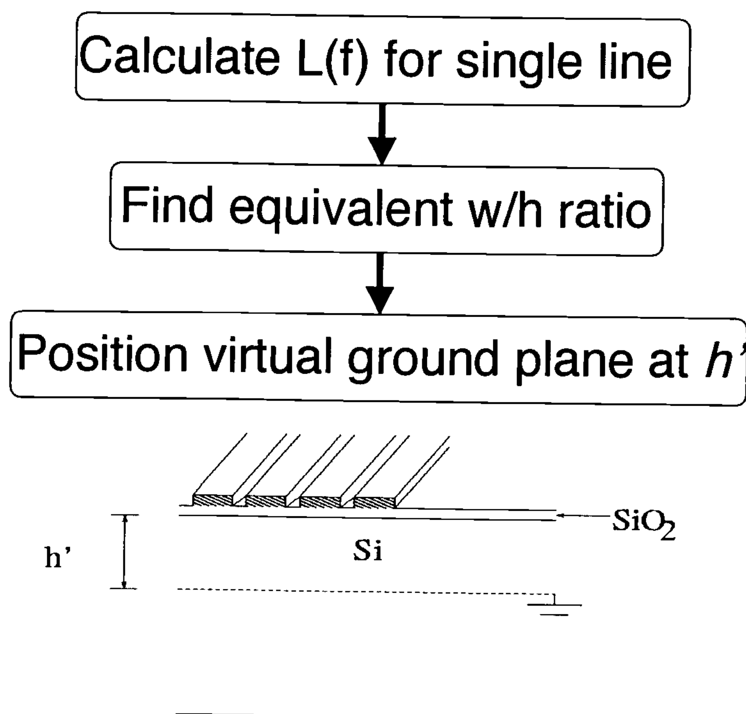


FIGURE 2.24. Flow-chart of virtual ground plane method for inductance calculations.

$$\frac{w}{h} = \frac{8e^A}{e^{2A} - 2} \quad \text{for} \quad w/h < 2 \tag{2.52}$$

$$= \frac{2}{\pi}\left[B - 1 - \ln(2B - 1)\right] \quad \text{for} \quad w/h > 2 \tag{2.53}$$

where

$$A = \frac{Z_0}{60} \tag{2.54}$$

$$B = \frac{377\pi}{2Z_0} \tag{2.55}$$

This method is illustrated by the flow chart in Figure 2.24.

Figure 2.25 shows the schematic representation of a distributed equivalent circuit model for a rectangular spiral inductor over a semiconducting substrate.

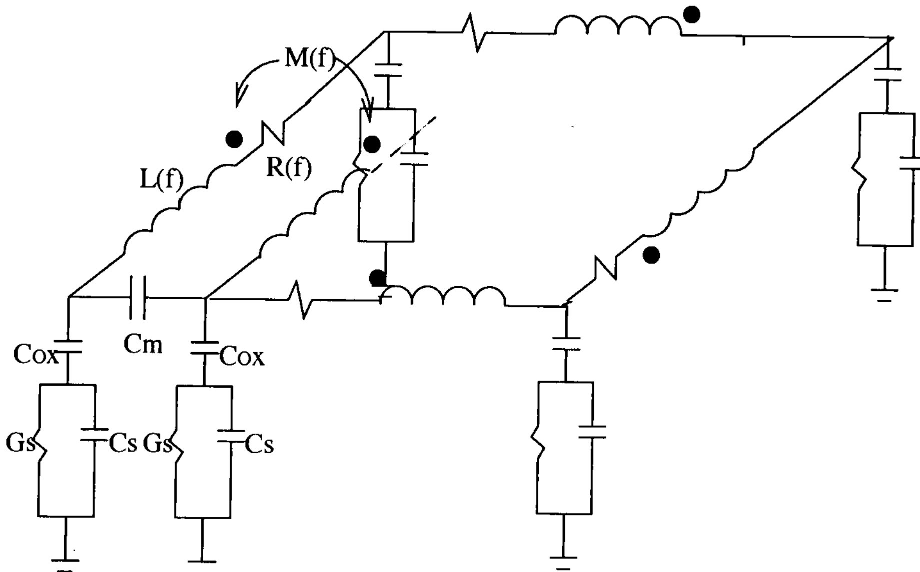


FIGURE 2.25. Distributed equivalent circuit model for spiral inductors.

Given that for even a two-turn spiral, there will be a relatively large number of nodes, it is advantageous to have a robust method for calculating the frequency-dependent input/output characteristics of spiral inductor that can handle any arbitrary number of nodes and also that does not rely on an external SPICE-like simulator, since such a simulator does not handle complex expressions for lumped elements that are frequency-dependent. The modeling engine used to implement the modeling methodology presented in this thesis is a Matlab© [35] program, which allows for testing (during development phases) of various expressions and methods for calculating the composite R, L and C terms that make up the circuit in Figure 2.25. If the circuit is broken down into series impedance (Z_s) and shunt admittance (Y_{sh}) terms, it may be analyzed in terms of a nodal admittance matrix defined by the following equations for an N-turn spiral:

$$\mathbf{Z}_{\mathbf{s,4Nx4N}}(\omega) = \mathbf{R}_{\mathbf{s,4Nx4N}}(\omega) + j\omega \mathbf{L}_{\mathbf{s,4Nx4N}}(\omega) \tag{2.56}$$

$$\mathbf{Y}_{\mathbf{sh,(4N+1)x(4N+1)}}(\omega) = \mathbf{G}_{\mathbf{sh,(4N+1)x(4N+1)}}(\omega) + j\omega \mathbf{C}_{\mathbf{sh,(4N+1)x(4N+1)}}(\omega) \tag{2.57}$$

$$\mathbf{Y}_{\mathbf{n,(4N+1)x(4N+1)}} = \mathbf{A}\mathbf{Z}_{\mathbf{s}}(\omega)^{-1}\mathbf{A}^{\mathbf{T}} + \mathbf{Y}_{\mathbf{sh}} \tag{2.58}$$

where $\mathbf{A}$ is the nodal incidence matrix for the branch admittance matrix $\mathbf{Z}_{\mathbf{s}}(\omega)^{-1}$ and is given by

$$\mathbf{A}_{\mathbf{(4N+1)x4N}} = \begin{bmatrix} 1 & 0 & \cdots & 0 \\ -1 & 1 & \cdots & 0 \\ 0 & -1 & \cdots & 0 \\ \vdots & \vdots & \ddots & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix}. \tag{2.59}$$

Consider the following example of how to solve for the frequency-dependent input impedance of the spiral. Define nodes 1 and (4N+1) as ports 1 and 2, then solve for voltage between ports 1 and 2 when a unity current source is attached across them:

$$\mathbf{Y}_{\mathbf{n,(4N+1)x(4N+1)}}\mathbf{V}_{\mathbf{(4N+1)x1}} = \mathbf{I}_{\mathbf{(4N+1)x1}}, \tag{2.60}$$

where

$$\mathbf{I}_{\mathbf{(4N+1)x1}} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ \vdots \\ -1 \end{bmatrix}. \tag{2.61}$$

Then $\mathbf{V}$ may be solved as

$$\mathbf{V}_{\mathbf{(4N+1)x1}} = \mathbf{Y}^{-1}_{\mathbf{n,(4N+1)x(4N+1)}}\mathbf{I}_{\mathbf{(4N+1)x1}}, \tag{2.62}$$

and the input impedance is simply

$$Z_{\text{in}} = \left(V_{(1)} - V_{(4N+1)}\right), \tag{2.63}$$

since the excitation is a unity current source.

For the modeling methods developed in this thesis, $\mathbf{Z_s}$ contains mutual coupling terms for all sections that are parallel to one another, and $\mathbf{Y_{sh}}$ contains all nearest neighbor coupling capacitances.

Further modeling work has incorporated the virtual ground plane at a complex distance approach [18], [30], [31] presented earlier in this chapter, which results in frequency-dependent inductance as well as resistance. Example simulation results are presented in Chapter 5.

2.5.1. Single Level Spiral Inductor Modeling and Network Reduction

The coupled line model described in this chapter forms the basis for an equivalent circuit model for a complete spiral inductor on lossy substrate. As stated in the preceding section, such a distributed model is constructed by subdividing the structure and computing an equivalent circuit for each straight section (or leg) of length l_m and including the capacitive and inductive coupling terms, using a combination of SDA and modified PEEC techniques, as well as conductor skin effect [27]. This distributed model may become unnecessarily complex for a large number of discretizations, hence, it is desirable to have a means for model reduction [32]. This may be accomplished via construction of an n-section ladder network, as shown in Fig. 2.26, where n is the number of turns. The elements of the ladder network are given by

$$Cox'_k = \left[\sum_{m=(4k-3)}^{4k} l_m\right] \cdot Cox_{\text{p.u.l.}} \tag{2.64}$$

$$Cm'_k = \left[\sum_{m=(4k-3)}^{4k} \frac{(l_m + l_{m+4})}{2}\right] \cdot Cm_{\text{p.u.l.}} \tag{2.65}$$

$$Cs'_k = \left[\sum_{m=(4k-3)}^{4k} l_m\right] \cdot Cs_{\text{p.u.l.}} \tag{2.66}$$

$$Gs'_k = \left[\sum_{m=(4k-3)}^{4k} l_m\right] \cdot Gs_{\text{p.u.l.}} \tag{2.67}$$

$$L'_k(f) = \left[\sum_{i=1}^{4n}\sum_{j=1}^{4n} M_{ij}(f)\right] \cdot \frac{\sum_{m=(4k-3)}^{4k} l_m}{\sum_{m=1}^{4n} l_m} \tag{2.68}$$

$$R'_k(f) = \left[\sum_{m=(4k-3)}^{4k} l_m\right] \cdot R(f)_{\text{p.u.l.}} \tag{2.69}$$

The order of the reduced circuit model is, in general, high enough to sufficiently approximate the response of the original distributed model. The reduced model gives virtually the same performance in the frequency range of interest, which is usually from dc to the first self resonance.

2.5.2. Multilevel Spiral Inductor Modeling

As with the distributed single-level spiral model, the distributed model for multilevel spirals also incorporates a spectral domain approach [25] combined with a modified PEEC formulation [16], [36] to obtain the frequency-dependent distributed series resistance and series inductance components. The distributed capacitances and conductances are computed using a spectral domain approach [24] for multilevel coupled transmission lines on a multi-layered substrate. Each leg or segment of the spiral is modeled in terms of a lumped-element equivalent

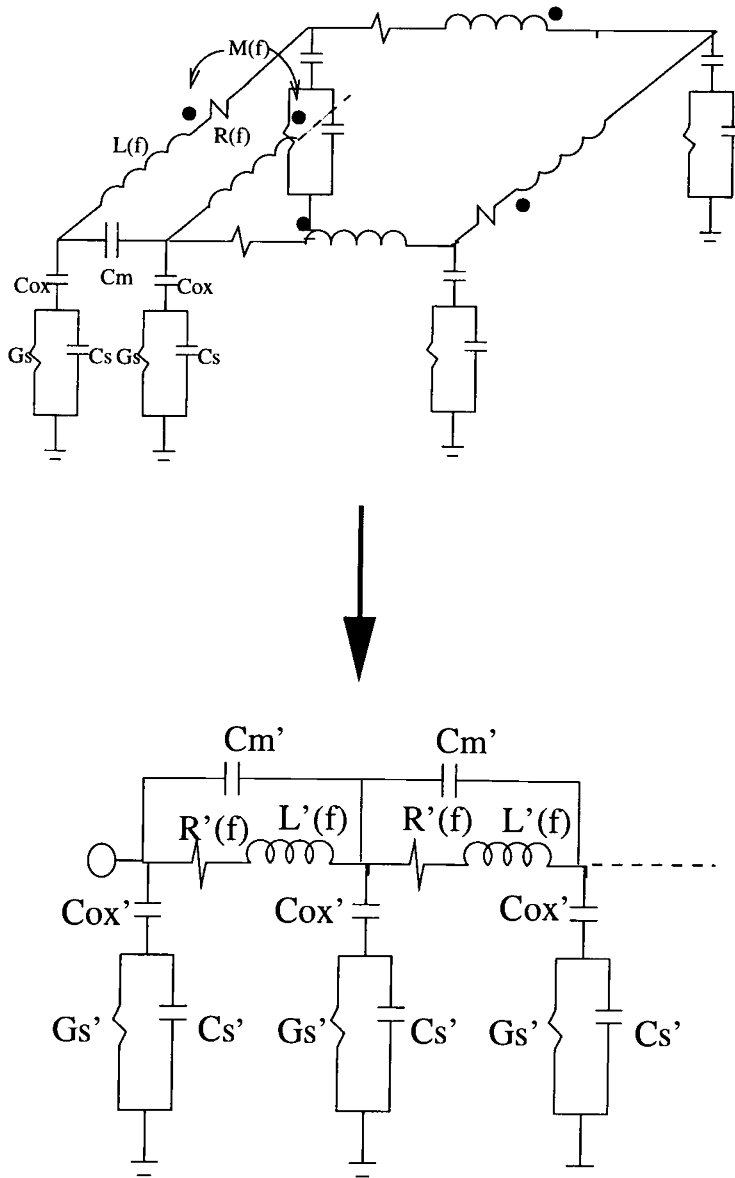


FIGURE 2.26. Distributed model and synthesis of a corresponding ladder network for turns of a spiral inductor.

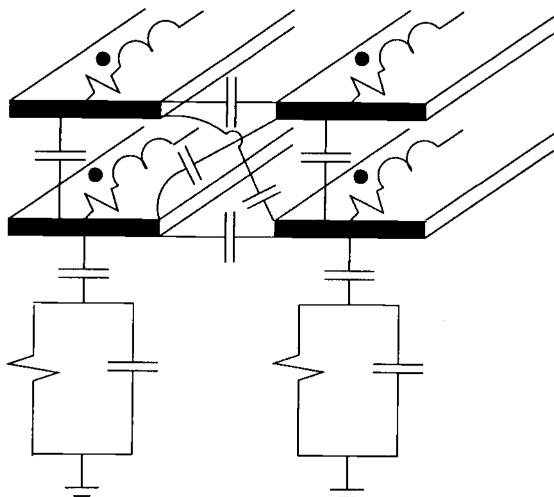


FIGURE 2.27. Equivalent circuit modeling of multilevel structure.

circuit that is appropriately coupled both capacitively and inductively to all other elements of the circuit for which the coupling terms are significantly large. Figure 2.27 illustrates the relationship between the model elements and the physical structure. The shunt elements again utilize the common C-G-C topology. The frequency-dependent self and mutual series resistances and partial inductances incorporate the effects of longitudinal substrate currents, as well as the skin effect in the metallization layers [27].

2.5.3. Application of Complex Virtual Ground Plane Height to Inductors and Mutual Resistance Concept

As presented earlier in this chapter, the virtual ground plane spaced at a complex distance can be used to effectively calculate the series impedance of parallel-plate waveguides as well as microstrip structures. Since the model formulations presented in the previous sections rely on virtual ground planes for

their inductance calculations, it is relatively easy to implement the complex distance approach for the distributed inductor model as well. As with the case of microstrip, the closed-form expressions for inductance between two finite length conducting bars of metal accept complex arguments for distance and return a complex impedance.

Of particular significance to both single and multilevel spirals is the concept of mutual resistance, which provides a higher level of accuracy, particularly over heavily doped substrates where longitudinal substrate currents are significant. Earlier modeling efforts in [16] and [32] did not include mutual resistance terms. Figure 2.28 illustrates the concept for the case of two conductors on two different metallization levels, which is a typical case for multilevel spirals, while Figure 2.29 shows the case of two coplanar lines. The mutual resistance terms for a spiral inductor may be calculated using a two-line spatial domain solution derived in Appendix B from the single line solution in [26]. Alternatively, the complex virtual ground plane height method combined with the closed-form expressions for partial inductance in [33] provides an even more accurate solution since it accounts for the finite lengths of the structures involved.

As an example of mutual resistance in silicon-based microstrip structures, consider a simple two-line microstrip case over a heavily doped substrate (i.e. σ_{Si} = 10,000 S/m) as illustrated in Figure 2.30. If mutual inductance M_{12} between these two lines is complex as a result of the semiconducting substrate below, the net effect at frequency f ($\omega = 2\pi f$) will be a complex mutual impedance

$$\begin{aligned} Z_m(\omega) &= j\omega M_{12} \\ &= j\omega\Re[M_{12}] - \omega\Im[M_{12}], \end{aligned} \tag{2.70}$$

where mutual resistance is given by

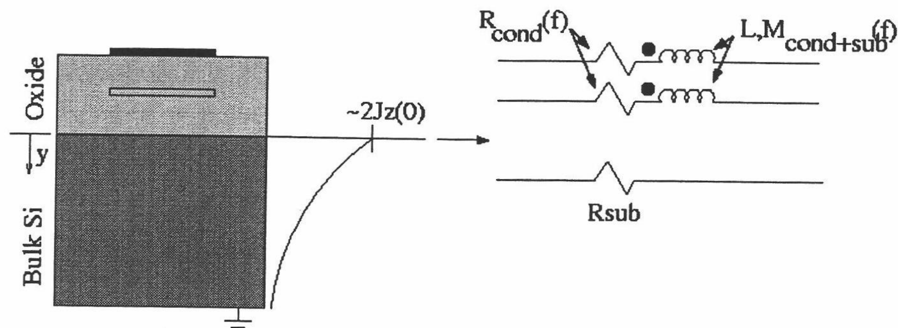


FIGURE 2.28. Illustration of mutual resistance concept for lines above silicon.

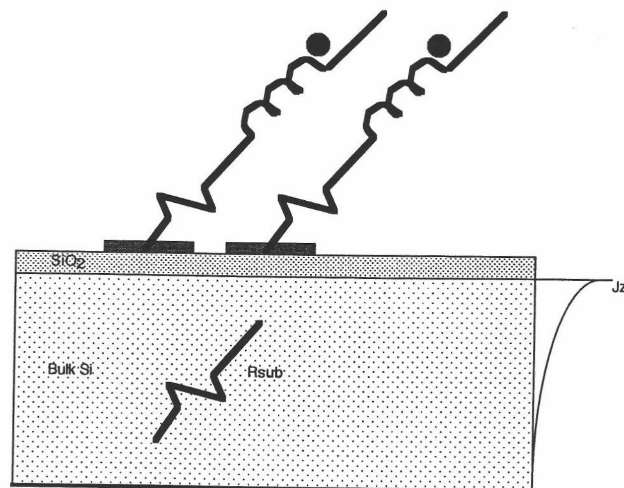


FIGURE 2.29. Additional illustration of mutual resistance concept for coplanar lines above silicon.

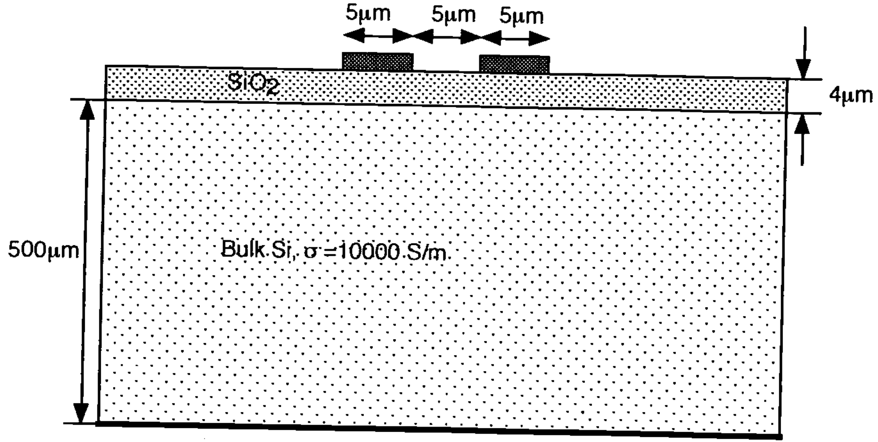


FIGURE 2.30. Example structure for plots in Figures 2.31 and 2.32.

$$R_m = -\omega \Im[M_{12}]. \tag{2.71}$$

A comparison of the net mutual resistance for the lines in Figure 2.30 are shown in Figures 2.31 and 2.32 for both the two-line spatial-domain solution found in Appendix B and the direct application of the complex virtual ground plane height approach. Clearly, the agreement between these two methods is quite good, within 10% across the frequency range for both mutual inductance and resistance, further validating the complex virtual ground plane height application to general microstrip structures.

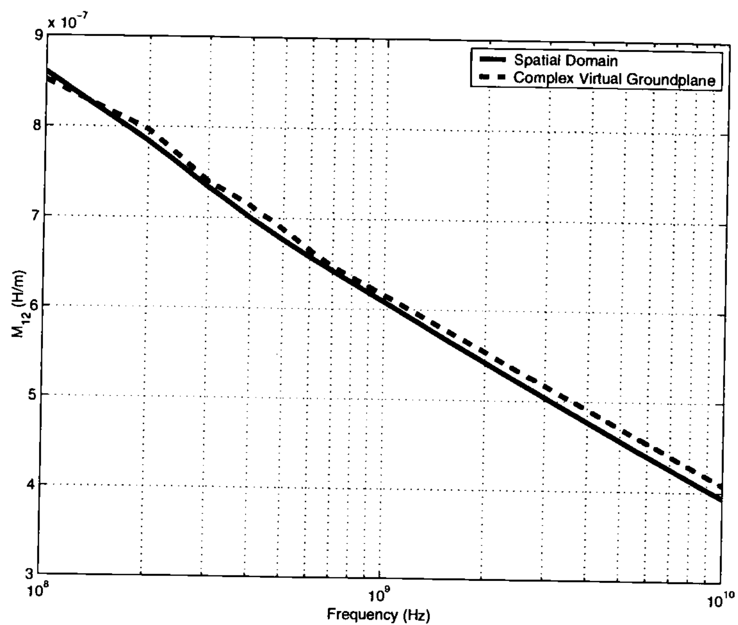


FIGURE 2.31. Mutual inductance for lines in Figure 2.30.

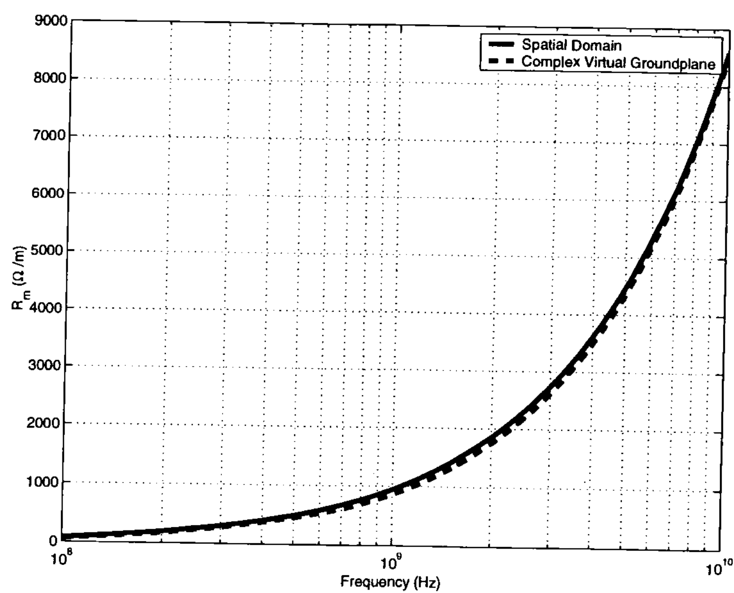


FIGURE 2.32. Mutual inductance and resistance for lines in Figure 2.30.

2.6. Simulation Results for Single and Multilevel Series-Connected Spiral Inductors and Discussion

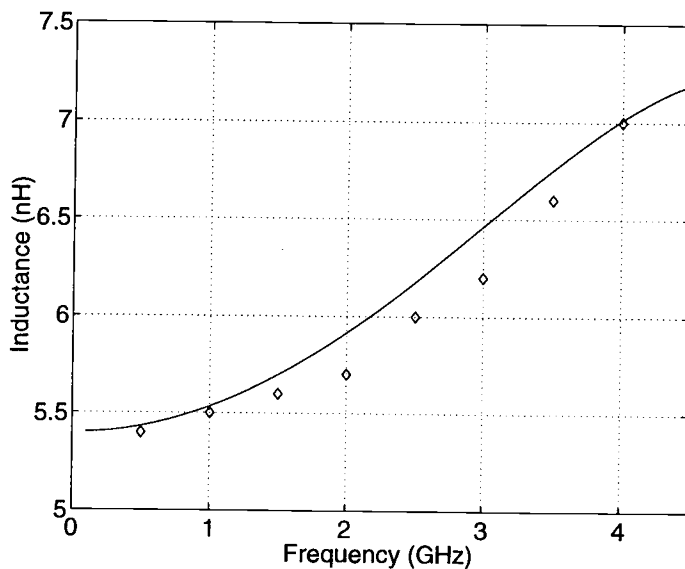
2.6.1. Single Level Spiral Inductors

As an example of a structure with relatively low substrate conductivity, a 5 nH spiral originally studied by Long and Copeland in [15] with $\sigma_{sub} = 10$ S/m is simulated using a model that does not address the skin effect mode (i.e. effects of longitudinal substrate currents are ignored). The model used in this thesis utilizes SDA for capacitance/conductance parasitics, and the resistive parasitics are computed using the conductor skin effect formula from [27]. The results are adequate for this particular structure, as can be observed in Fig. 2.33.

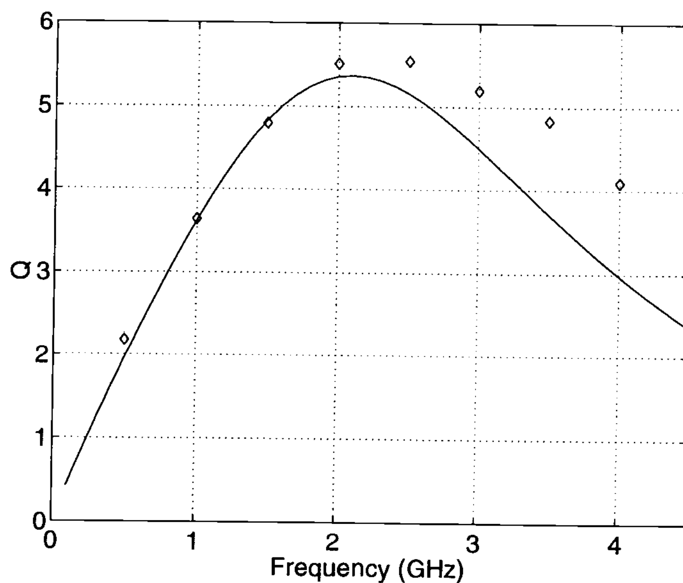
Next, consider a 9.5 turn, 10 nH spiral fabricated in CMOS technology with $\sigma_{\mathrm{Si}} = 10^4$ S/m. Fig. 2.34 shows a comparison of two separate models with measured data [37]. The distributed model (Fig. 2.26) and corresponding ladder network are augmented to properly account for the substrate skin effect through use of a virtual ground plane combined with the spatial domain formulation (see Appendix B) for substrate series resistance. This is in contrast to the model that only includes shunt conductances to represent the substrate losses. It is clear that the inclusion of the substrate skin effect is necessary for accurate modeling of the structure.

2.6.2. Multilevel Spiral Inductors

Figures 2.35 and 2.36 show the inductance and quality factor as functions of frequency for a four turn, two level series-connected spiral inductor over a typical BiCMOS substrate with $\rho = 12$ Ω-cm, as well as for a CMOS substrate with

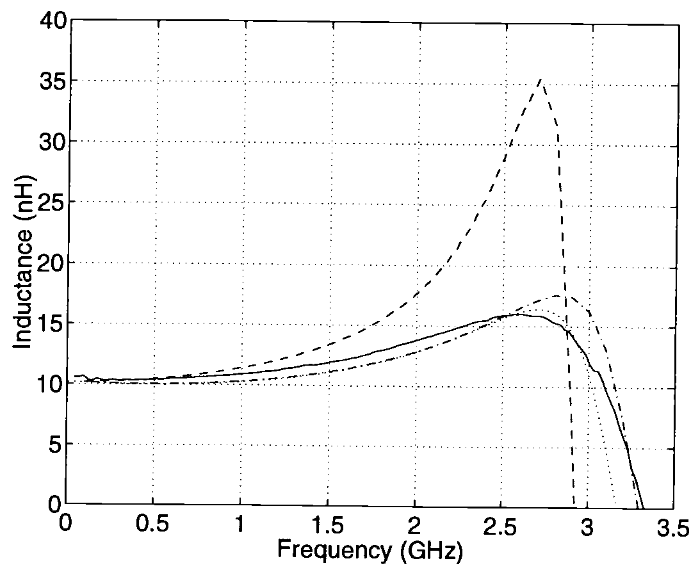


(a)

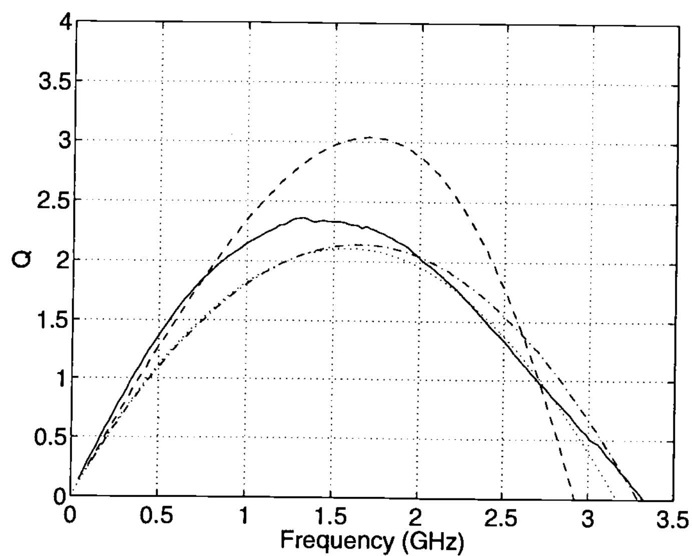


(b)

FIGURE 2.33. Comparison of (a) inductance and (b) quality factor for simulations without Si substrate effects (–) versus measured data (◇) for a 5 nH spiral inductor with $\sigma_{sub} = 10$ S/m [15].



(a)



(b)

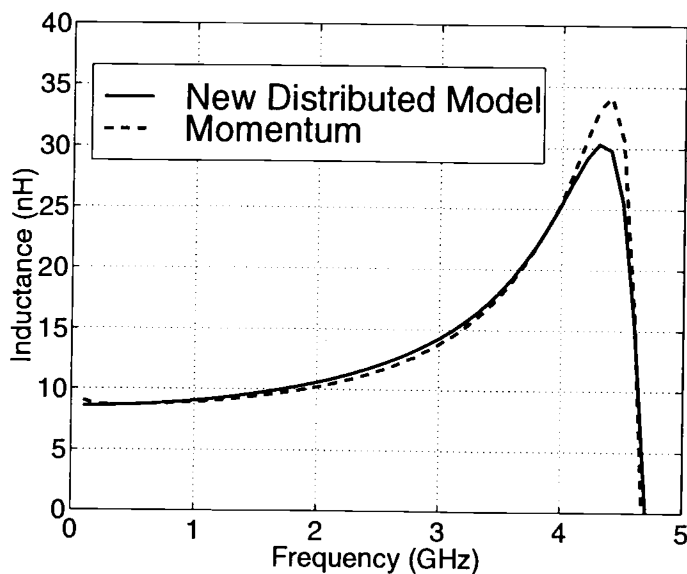
FIGURE 2.34. Comparison of (a) inductance and (b) quality factor for simulations with (-· distributed, ·· ladder) and without (- -) Si substrate effects, versus measured data (–) [37].

ρ = 0.01 Ω-cm, as illustrated in Figure 2.3. In both cases, the lower spiral is located 4.5 μm above the silicon substrate. The dimensions of both spirals are $w = s = 13$ μm and area = 226 × 226 μm^2. The inductance and quality factor were computed using the complete (i.e. all substrate effects included) distributed model described in this chapter and compared with full wave results obtained from Agilent Momentum. In addition, the CMOS substrate example includes results obtained from a distributed model that only accounts for the shunt substrate currents in order to exemplify the need for inclusion of the substrate skin effect for spiral inductors on high conductivity substrates. It is evident that the inductance enhancement from the two-level series configuration, which in this case is an increase in base inductance from ~2.3 nH to~8.8 nH, comes at the expense of a lower self-resonant frequency. However, for a given inductance value, the series resistance of the multilevel series configuration will be reduced, which can be advantageous. Also, in a lossy environment such as in BiCMOS and CMOS technologies, the multilevel structures can often achieve a higher quality factor in the low frequency range than their single level counterparts, as previously noted in [10].

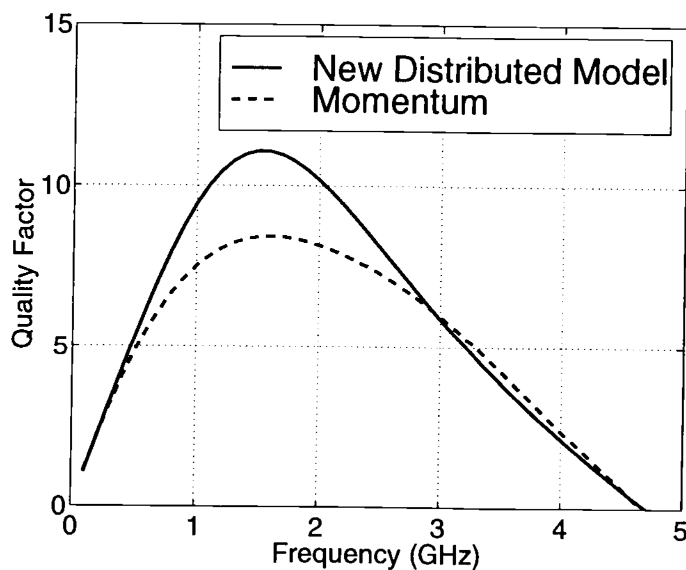
A two-level series-connected spiral fabricated on CMOS (ρ = 0.01 Ω-cm), shown in Figure 2.37, was measured using a 1-port VNA [37]. Figure 2.38 shows the measured data compared with simulation results for the distributed model. Dimensions are: area = 148 × 148 μm^2, w = 10 μm and s = 1.8 μm.

2.7. Parallel-Connected Spirals

A parallel-connected spiral consists of identical spirals placed on multiple metallization layers and shunted together by vias. This design technique makes

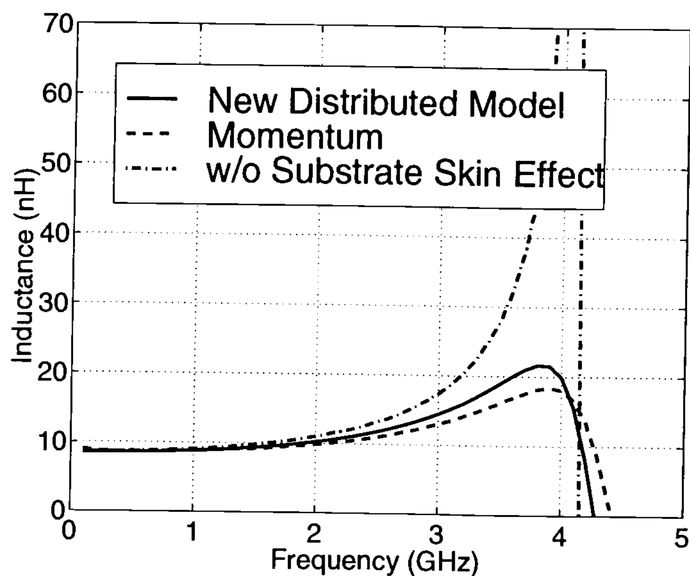


(a)

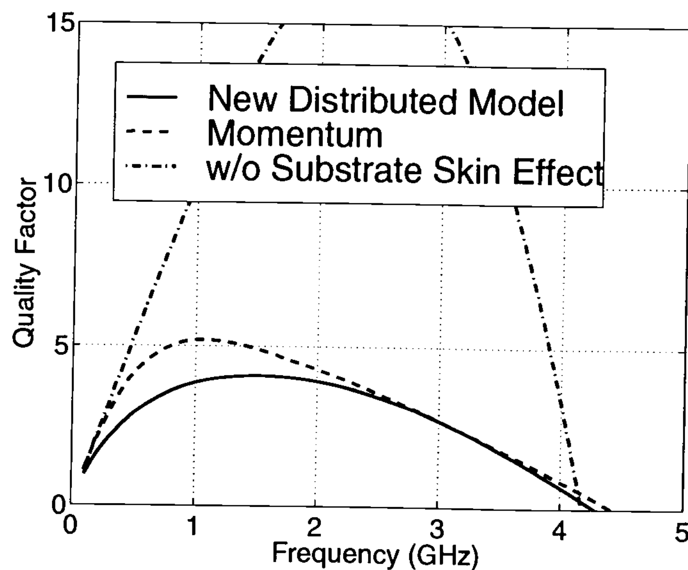


(b)

FIGURE 2.35. (a) inductance and (b) quality factor obtained with the distributed model [36] and HP Momentum [37] for a multilevel spiral inductor in a typical BiCMOS environment ($\rho = 12$ Ω-cm).



(a)



(b)

FIGURE 2.36. (a) inductance and (b) quality factor obtained with the distributed model [36] and HP Momentum [37] for a multilevel spiral inductor in a typical CMOS environment ($\rho = 0.01$ Ω-cm). Results obtained with a distributed model that neglects the substrate skin effect are also shown.

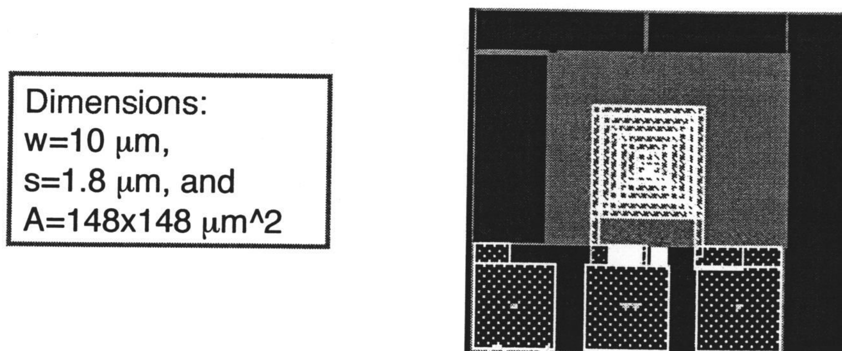
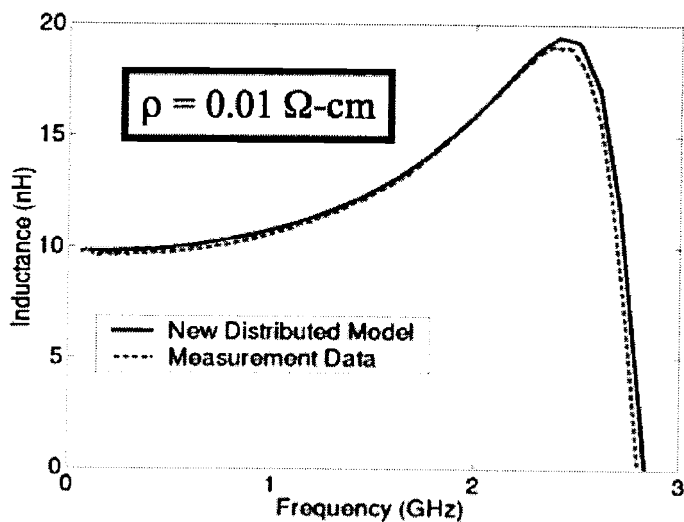


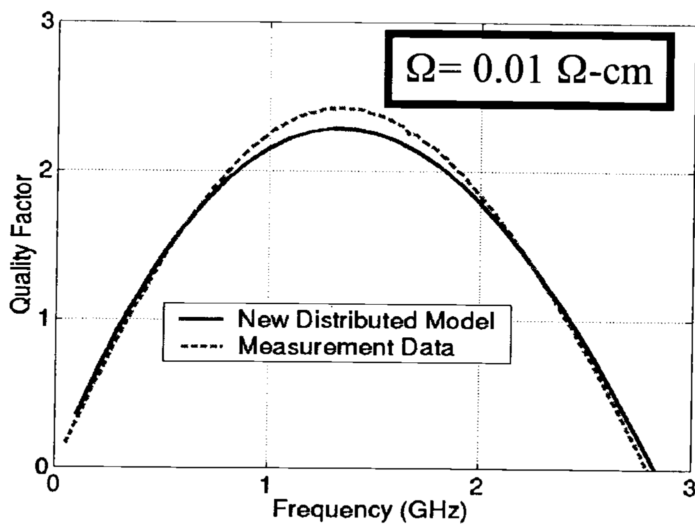
FIGURE 2.37. Measured multilevel spiral on CMOS substrate.

use of a multilevel metallization process to lower overall series resistance by placing multiple layers in parallel, as illustrated in Figure 2.39. The modeling techniques presented in the prior sections is easily extended to this case by simply assigning an effective thickness for the composite spiral equal to the total thickness of all layers being used in the spiral inductor, which is generally a valid approximation provided that the level-to-level spacing is relatively small (i.e. on the order of 1 μm).

Figure 2.40 shows the simulated inductance and quality factor for two eight-turn spiral inductors on a typical BiCMOS substrate ($\rho = 12$ Ω-cm). One of the spirals exists only on the upper metallization layer, and the other structure uses two metallization layers in parallel and shunted together by vias. The total area of both structures is 226×226 μm^2. The width and spacing for both spiral inductor structures are 6 μm, and the heights above the silicon substrate for the two metallization layers are 4.5 μm and 7.5 μm, respectively. The via connections are assumed to be at each corner and are assumed to be perfectly conducting.



(a)



(b)

FIGURE 2.38. (a) inductance and (b) quality factor of a multi-level spiral inductor for the distributed model versus VNA measurement data [37].

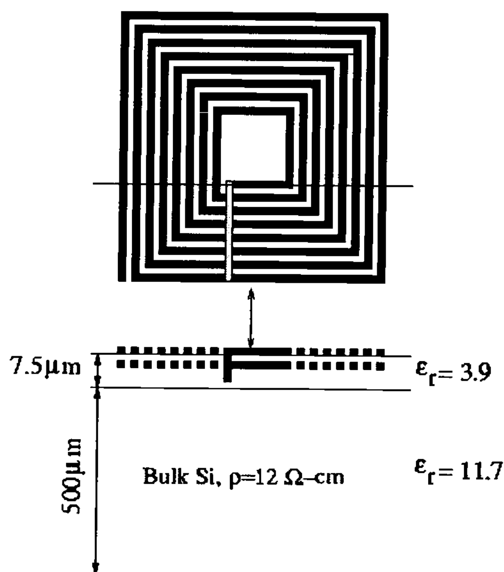
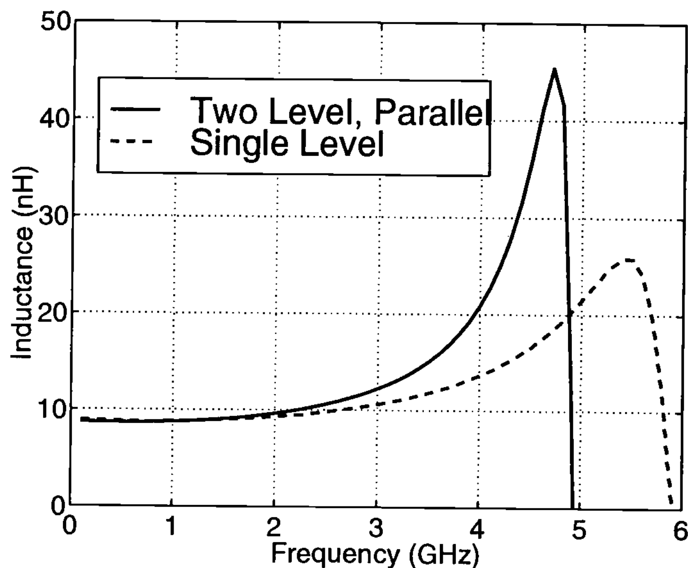
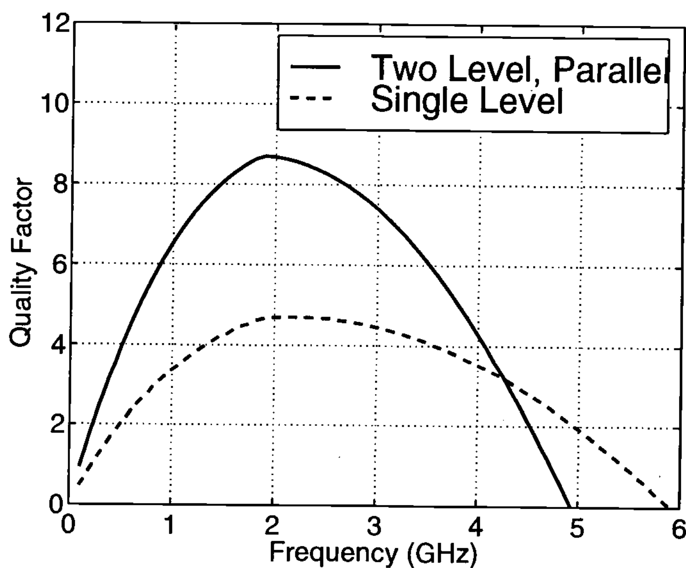


FIGURE 2.39. Parallel-connected spiral inductor used for simulation example.

As expected, the quality factor achieved with the shunted two-level structure is greater than that of the single level counterpart. However, the self-resonant frequency of the parallel-connected spiral is slightly lower, mainly due to the increased shunt oxide capacitance, which results from the lower level being closer to the substrate. The low-frequency inductance values for both structures are virtually identical, indicating that inductance is lowered only slightly by the parallel connection. It should be noted that although the performance improvement is substantial for this example, similar results are not possible if the bulk substrate resistivity is much lower (e.g. $\rho = 0.01$ Ω-cm) since in this case the eddy currents dominate the overall series resistance. Hence, lowering the resistance of the spiral itself through multiple layers connected in parallel will only provide a marginal improvement for low resistivity bulk substrate environments.



(a)



(b)

FIGURE 2.40. Comparison of (a) inductance and (b) quality factor for a two level parallel-connected spiral inductor and a single level spiral in a typical CMOS environment ($\rho = 12\ \Omega$-cm). All results are computed using distributed equivalent circuit models including the substrate skin effect [36].

2.8. Conclusions

In this chapter, a modeling methodology for single- and multilevel spiral inductors on lossy substrates has been presented. It was shown that the proposed model for single-level spiral inductors on lossy substrate is in better agreement with measured data for higher conductivity-frequency products ($\sigma\omega$'s) than previous models, which only address transverse (shunt) currents. It has also been shown that the multilevel series configuration yields a higher inductance/area ratio as well as higher quality factors for low frequencies, although the usable frequency range is reduced as compared to a single-level spiral inductor with the same inductance value. It was shown that in a high conductivity environment, it is necessary to account for the substrate skin effect in order to accurately model spiral inductor structures. In conclusion, it has been demonstrated that both single- and multilevel spiral inductors can be accurately modeled for a wide range of substrate conductivities, including those typically used in CMOS technologies. The proposed modeling methodologies should be very useful in the design of RFICs on silicon substrates, and in particular heavily-doped CMOS substrates.

3. EFFECTS OF SILICON PROCESS AND GEOMETRY VARIATIONS ON INDUCTOR PERFORMANCE

3.1. Introduction

Spiral inductors fabricated in silicon-based integrated circuits often yield poor quality factors due to high-resistivity metallization and/or a lossy silicon substrate. In addition, substrate eddy currents can adversely affect the inductance of a spiral for certain frequencies and substrate conductivities. Because of the low-cost aspects of silicon technology, however, such structures are attractive, especially for RFICs, for which cost must be minimized in order for the semiconductor companies manufacturing such circuits to remain competitive. The need for accurate characterization of silicon-based spiral inductors has prompted the formulation of modeling methodologies that include semiconducting substrate effects, as presented in Chapter 2. This chapter presents analyses of the effects of the silicon substrate on inductor performance in terms of geometry and process variables. The methods in Chapter 2 are applied to simulate the various cases.

3.2. Summary of Semiconducting Substrate Effects on Si-SiO_2 Microstrip

First, the propagation characteristics of a Si-SiO_2-based metal-insulator-substrate (MIS) structure are revisited, since this structure is a basic element of planar spiral inductors. The planar conductor is above a double-layer substrate consisting of oxide over bulk silicon. Due to the finite conductivity of the bulk, both conduction and displacement currents will exist in the substrate. The current distribution in the semiconducting substrate may be decomposed into shunt and longitudinal components resulting from electric and magnetic fields produced

by the conductor, and their respective effects may be analyzed separately. The consequence of the shunt substrate currents is a frequency-dependent p.u.l. shunt admittance $[G(\omega) + j\omega C(\omega)]$, while the longitudinal (eddy) substrate currents contribute to a frequency-dependent p.u.l. series impedance $[R(\omega) + j\omega L(\omega)]$.

As stated above, conduction currents do indeed exist in the semiconducting bulk for a MIS microstrip structure operating above DC. The resistive losses resulting from these substrate conduction currents are generally significant for typical silicon bulk substrate resistivities with operating frequencies in the RF-to-microwave range, and thus need to be included for accurate modeling of planar spiral inductors implemented in a silicon-based MIS environment. Additionally, the frequency dependence of the reactive terms of the shunt admittances and series impedances also need to be incorporated into an accurate spiral inductor model for RFICs. For spiral inductors in RFICs implemented in medium-to-high substrate resisitivity environments (e.g. 10Ω-cm), the main substrate effects are due to shunt currents, while for low substrate resistivities (e.g. 0.01Ω-cm), the longitudinal substrate currents dominate.

3.3. Using Distributed Models to Predict Performance Trends

Because there are many variables involved in a silicon-based fabrication technology, such as the properties of the substrate layers, interlayer dielectrics and metallization layers, it is desirable from a process engineering perspective to be able to predict the performance impact of each of these variables either separately or in various combinations so that the process may be optimized for a given set of initial operating specifications (e.g. an inductor with a Q of at least 15 with outer diameter less than 200 μm at 2 GHz). Additionally, any silicon

process will have natural wafer-to-wafer variations in the dimensions and material properties. The relative impact of these variations are often evaluated by circuit designers to ensure that their products will function within the known tolerances of the process.

Besides optimizing a process and predicting the impact of the relative tolerances, the problem of choosing the best spiral geometry for a given process to meet a particular set of design criteria is also a major task to be undertaken by the circuit designer. As stated previously, the techniques in [3] and [4] are both experimentally-based in terms of how they predict and inductor's performance. However, it is advantageous to have an accurate, reliable method to predict inductor performance in the absence of measured data, which allows for the plotting of various trends such as self-resonant frequency vs. tracewidth, etc. before anything is ever fabricated. This in turn allows for a spiral inductor design to be optimized for a particular application and given silicon process through a sort of virtual prototyping, eliminating the need for costly and time-consuming layout, fabrication and measurement of test wafers.

Fortunately, the distributed modeling methods in Chapter 2 can be used to evaluate all of the variations mentioned in the preceding two paragraphs. For all simulation results presented in the following sections, these distributed models have been used. Capacitance and conductance parasitics are calculated using SDA [24] code for single and coupled microstrip on a multilayer substrate. For inductance and resistance calculations, the PEEC method is used in conjunction with the virtual ground plane at a complex distance approach, which accounts for the effects of a semiconducting substrate. Additionally, closed-form expressions from [27] are used to compute the skin-effect resistance of the conductors themselves and are added to the self-resistance (i.e. on the R-matrix diagonal)

terms. In order to save computation time, the method of subdividing conductors lengthwise to include proximity effects, as was done in [31], is not implemented. As stated in Chapter 2, the development of a simple computationally efficient method for inclusion of conductor proximity effects in spiral inductors is considered as a topic for future research.

3.4. Peak Quality Factor, Self-Resonant Frequency and Other Issues

The distributed equivalent circuit modeling techniques developed in Chapter 2 were found to be quite accurate versus measured data and EM simulations, and, hence, can be used to examine trends in performance versus geometry and process variables. To this end, the proceeding subsections detail results for inductor performance versus substrate properties and spiral geometry. Figure 3.1 shows a typical two turn single-level spiral (SLS) inductor and cross-section with the names of the relevant dimensions for both the inductor and the process variables. The geometry variations are summarized in Table 3.1, with the corresponding figure numbers included for reference purposes. For all cases in the proceeding sections, one micron copper ($t_{\mathrm{Cu}} = 1\mu\mathrm{m}$) was chosen as the metallization. While these results are not to be taken as all-encompassing behavioral trends for all conceivable spiral inductors, they are representative of trends for typical spiral geometries and silicon process variables. A brief discussion on the effects of doped layers and wafer thickness is also included since these two factors can also impact inductor performance.

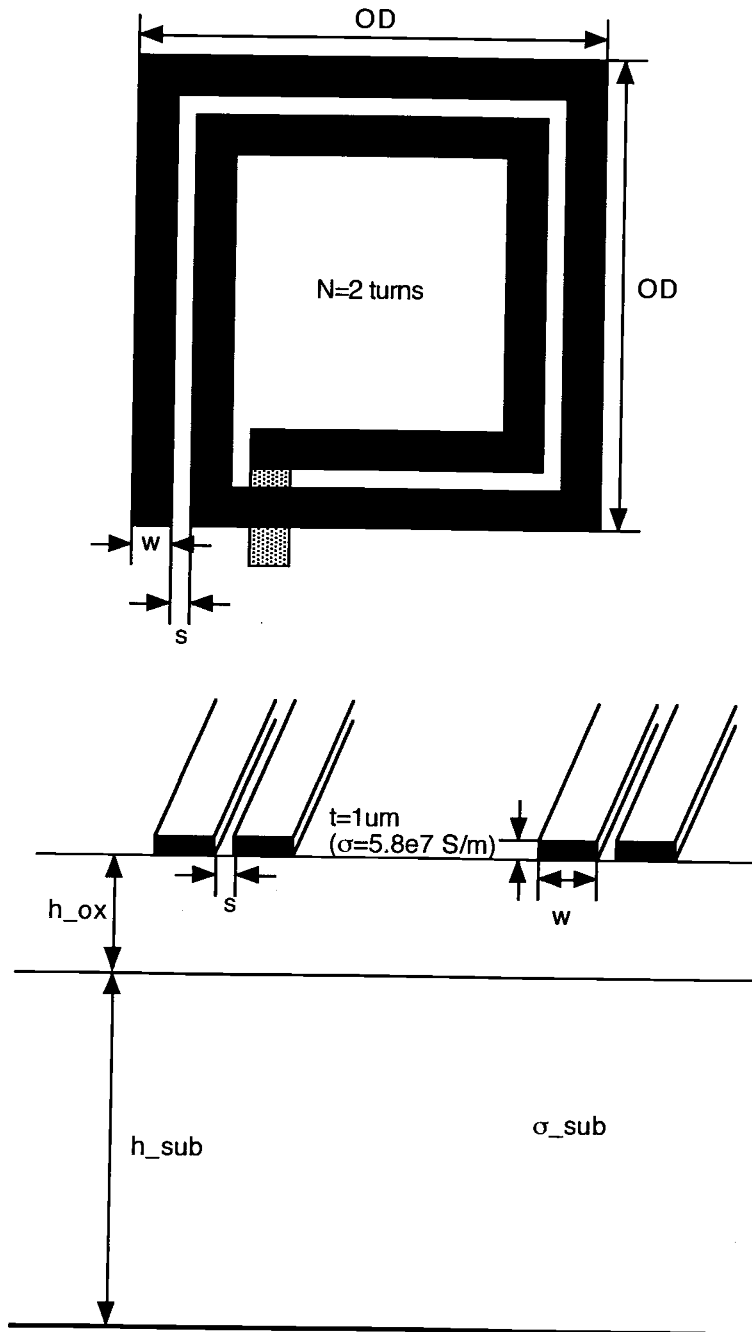


FIGURE 3.1. Example 2-turn SLS and relevant dimensions.

3.4.1. Bulk Substrate Conductivity

To exemplify the effect of finite substrate conductivity on a spiral inductor's frequency-dependent behavior, the peak quality factor (Q_{max}) and self-resonant frequency (f_{SR}) for a typical four-turn spiral inductor as functions of σ_{sub} are examined, as shown in Figure 3.2. As σ_{sub} increases, the initial trend is for peak Q to increase and self-resonant frequency to decrease. This initial behavior is due to lowering shunt losses as well as flatter net shunt capacitance versus frequency, that is, the shunt capacitance remains close to its initial low frequency value over a broader bandwidth that extends to the range of self-resonance, which is approximately 11-17 GHz for this example. However, beyond σ_{sub}=400 S/m, the value of peak Q drops as eddy current losses begin to dominate. The self-resonant frequency picks up as σ_{sub} increases further due to lower net inductance caused by longitudinal eddy currents in the bulk silicon. Using these two criteria, peak Q and self-resonant frequency, as performance metrics, it is clear that a definitive optimum does not exist. In addition, it may be concluded that the finite conductivity of the bulk substrate must be considered and included in any accurate model for spiral inductors in RFICs.

3.4.2. Trace Width and Shunt Capacitance & Conductance

In order to improve Q of an on-chip silicon spiral inductor, a circuit designer may be initially tempted to use the absolute widest traces possible in order minimize resistance. However, wider metal traces increases the inductor's effective plate area in terms of its shunt capacitance to the silicon substrate below, as well as increases line-to-line capacitance. This in turn can lower self-resonant frequency as well as the frequency at which peak Q occurs. Additionally, very

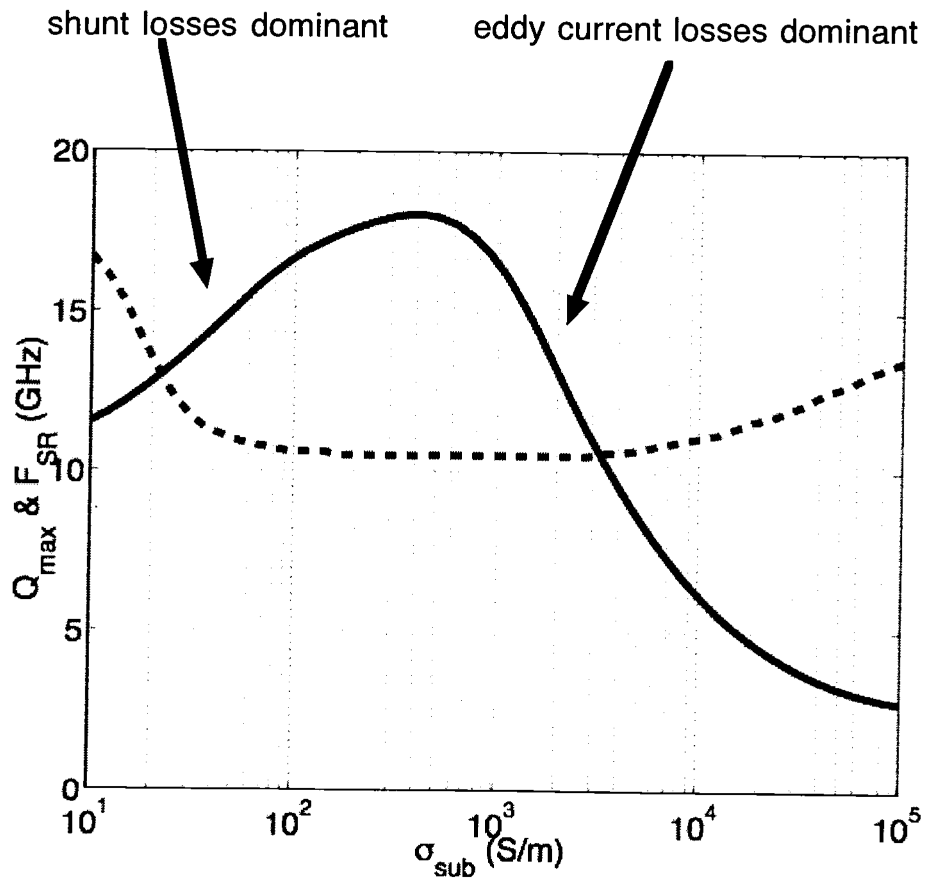


FIGURE 3.2. Q_{max} (solid) and f_{SR} (dashed) vs. σ_{sub} for four-turn SLS inductor.

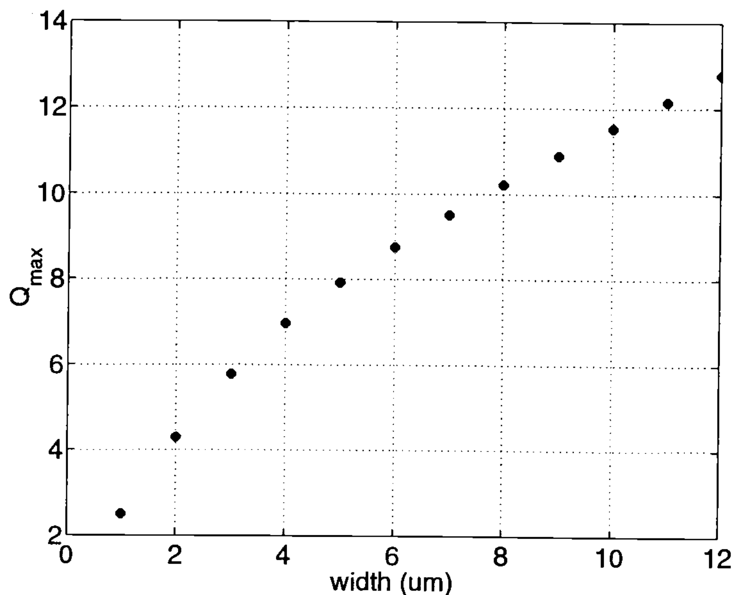


FIGURE 3.3. Q_{max} vs. trace width for OD = 200 μm SLS inductor with constant pitch = 15 μm.

large shunt capacitance can serve to increase vertical electric field losses in the bulk silicon, which counteracts the lowered series loss obtained from the wider metal traces.

Figures 3.3 and 3.4 show the effect of trace width on peak Q and self-resonant frequency for a typical square spiral inductor. In this case, the pitch (width + spacing) was held constant at 15 μm. Thus, the base inductance of the spiral inductor drops with increasing trace width as shown in Figure 3.5, which leads to the initial increase in self-resonant frequency. If the net inductance is held relatively constant by allowing OD to increase sufficiently while still holding the pitch constant, the behavior seen in Figures 3.6-3.8 results.

Note that in both of the preceding examples, the peak Q increased monotonically with line width. However, if the outer diameter is more tightly con-

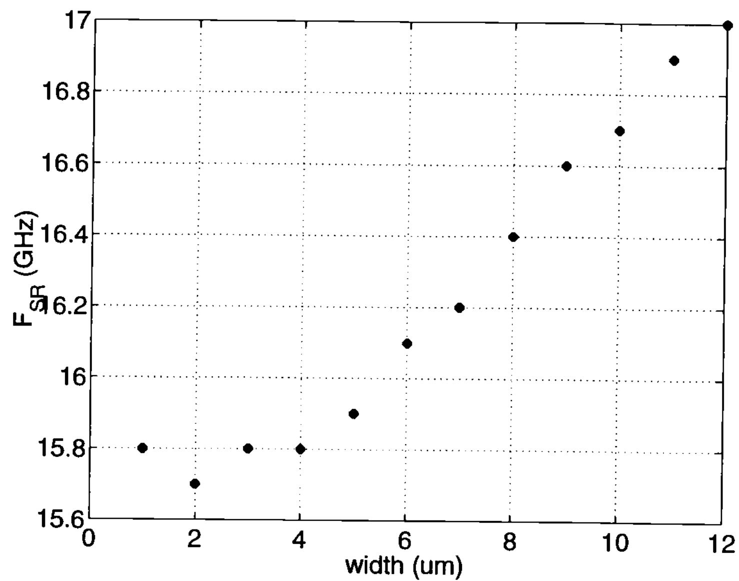


FIGURE 3.4. f_{SR} vs. trace width for OD = 200 μm SLS inductor with constant pitch = 15 μm.

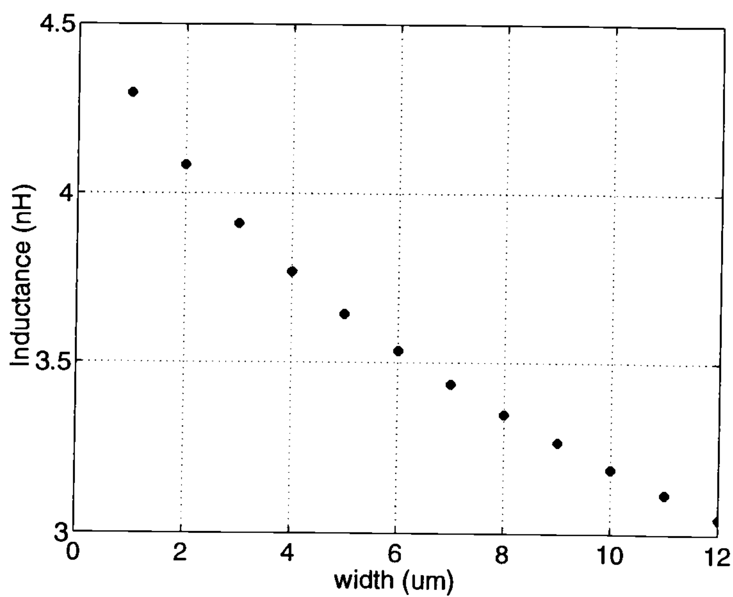


FIGURE 3.5. Inductance vs. trace width for OD = 200 μm SLS inductor with constant pitch = 15 μm.

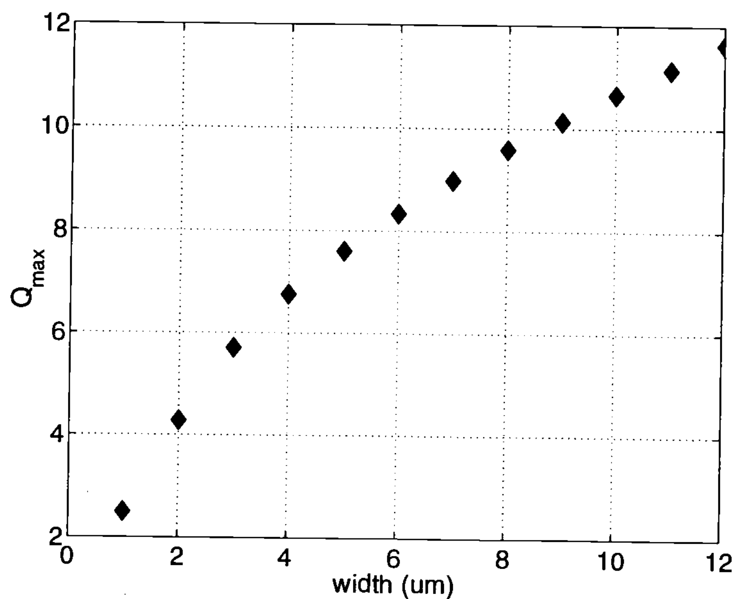


FIGURE 3.6. Q_{max} vs. trace width for approximately constant base inductance SLS inductor with constant pitch = 15 μm.

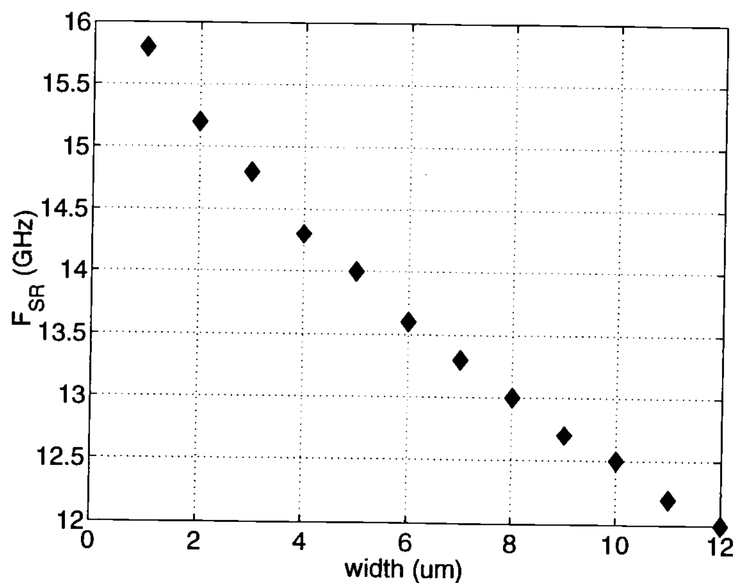


FIGURE 3.7. f_{SR} vs. trace width for approximately constant base inductance SLS inductor with constant pitch = 15 μm.

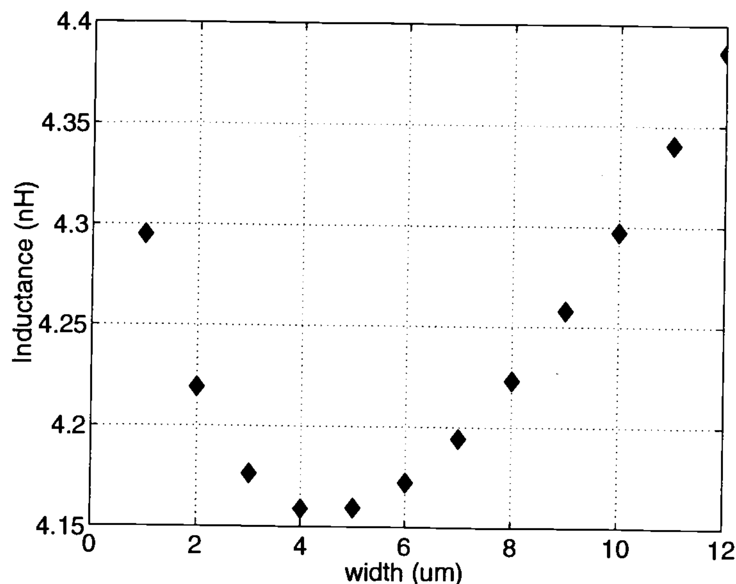


FIGURE 3.8. Inductance vs. trace width for approximately constant base inductance SLS inductor with constant pitch = 15 μm.

strained or even held constant, then spiral inductors with larger trace width will require a greater amount of turns for a given inductance. In this next example, the outer diameter is constrained to be 200 μm and also have nearly constant base inductance equal to approximately 3 nH (see Figure 3.11). The trace-to-trace spacing is held constant at 2 μm, and the number of turns varies from 2.5 to 5.5. The performance is summarized in Figures 3.9-3.13. As expected, the self-resonant frequency decreases with increasing trace width due to rising shunt capacitance, as shown in Figure 3.10. However, note that upon examination of Figure 3.9, the peak in maximum Q does not occur at the end of the sweep as in the previous examples, which is a result of increased shunt losses as the number of turns increases to maintain inductance within the 200 μm OD. Figures 3.12 and 3.13 illustrate another interesting aspect of this example regarding the fre-

TABLE 3.1. Summary of Inductor Geometry Variations.

Case	OD (μm)	Turns	Pitch	Reference Figures
1	200	4	constant	3.3-3.5
2	200-250	4	constant	3.6-3.8
3	200	2.5-5.5	varies	3.9-3.13

quency at which peak Q occurs and the 'Q versus width' behavior as a function of frequency. Observe that the frequency at which peak Q occurs decreases with increasing line width. This suggests that although the maximum Q value is initially rising with increasing trace width, the Q at a particular frequency may not necessarily exhibit this same increase since the Q curve is also shifting in frequency. This phenomenon can be seen in Figure 3.13.

The net shunt capacitance of a planar spiral inductor is generally a strong function of frequency for typical silicon IC processes. This results from the fact that the frequency at which displacement and conduction current magnitudes are equal (i.e. $\sigma_{\text{Si}} = \omega\epsilon$) is in the RF-to-microwave range for bulk substrate conductivities on the order of 10 S/m, which is typical of many production IC processes. Consequently, the net shunt conductance also changes with frequency and contributes to net degradation in Q of a spiral inductor. To summarize this behavior, at low frequencies (i.e. $\omega \ll \sigma_{\text{Si}}/\epsilon$), the net capacitance is predominantly that of the oxide only, and the net shunt conductance is near zero, while at high frequencies (i.e. $\omega \gg \sigma_{\text{Si}}/\epsilon$) the net capacitance is equal to the series combination of the oxide and bulk substrate capacitances and net shunt conductance is nearly

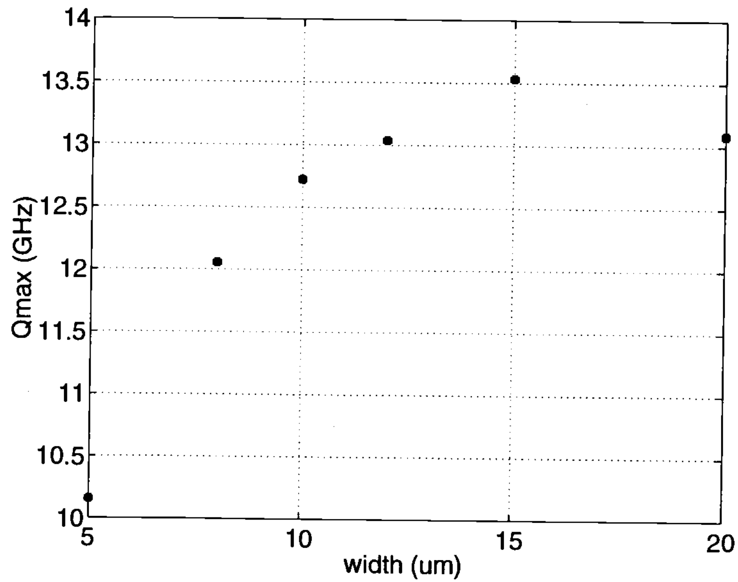


FIGURE 3.9. Q_{max} vs. trace width for OD = 200 μm SLS inductor with s=2μm, variable turns and pitch.

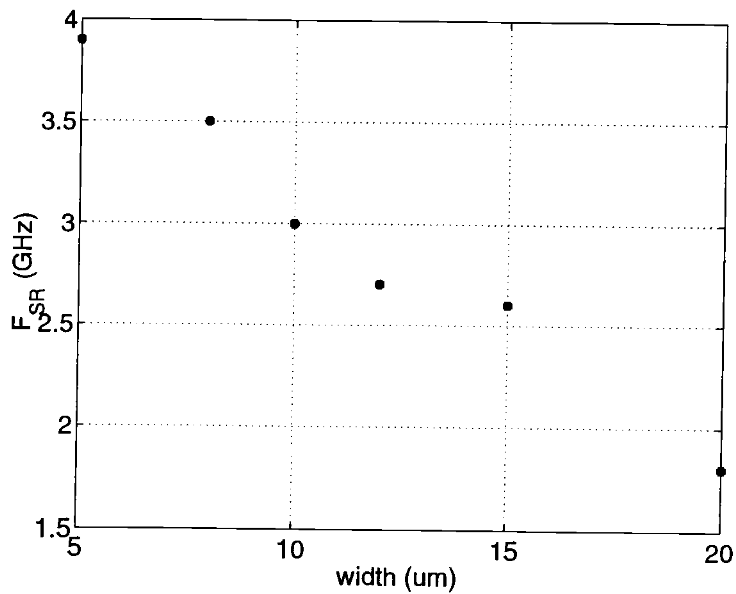


FIGURE 3.10. f_{SR} vs. trace width for OD = 200 μm SLS inductor with s=2μm, variable turns and pitch.

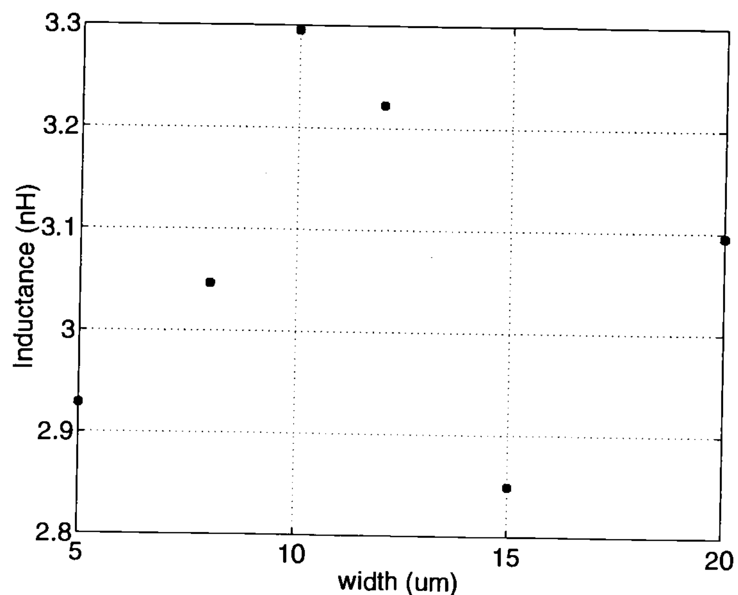


FIGURE 3.11. Inductance vs. trace width for OD=200 μm SLS inductor with s=2μm, variable turns and pitch.

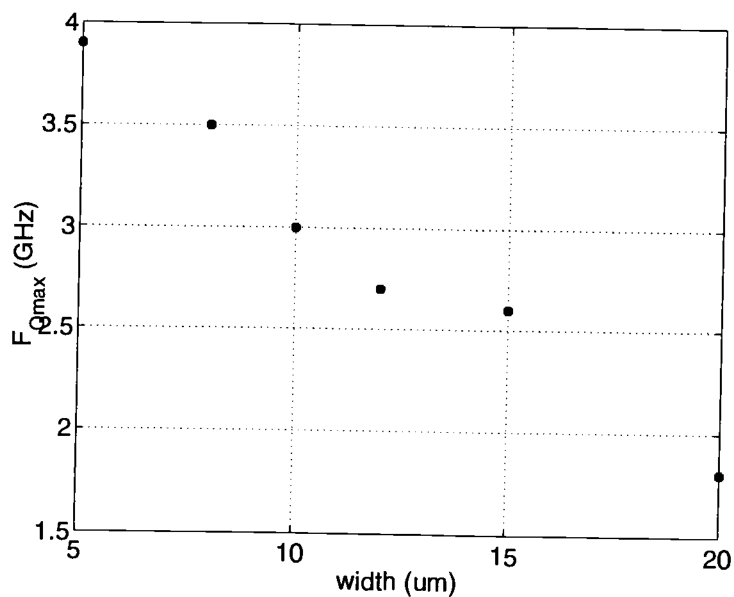


FIGURE 3.12. F_{Qmax} vs. trace width for OD = 200 μm SLS inductor with s=2μm, variable turns and pitch.

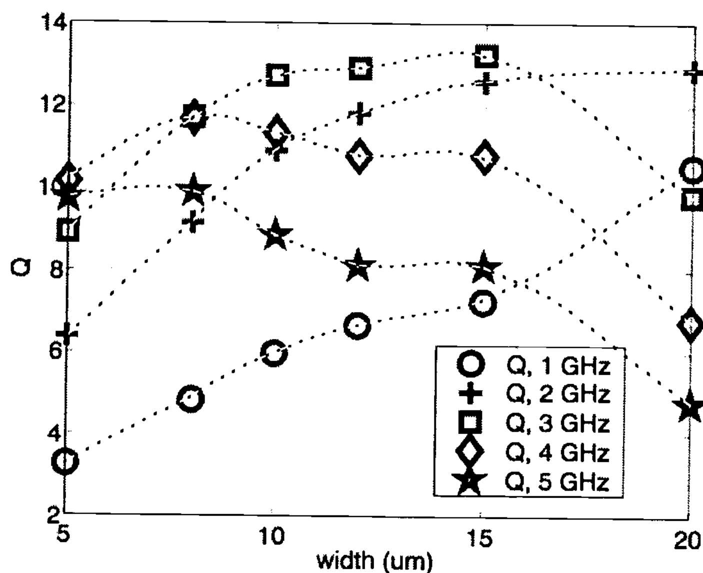
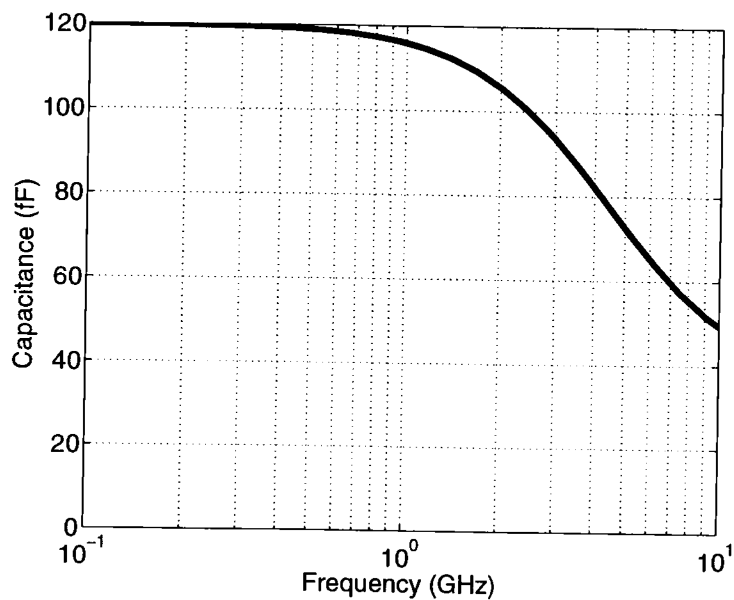
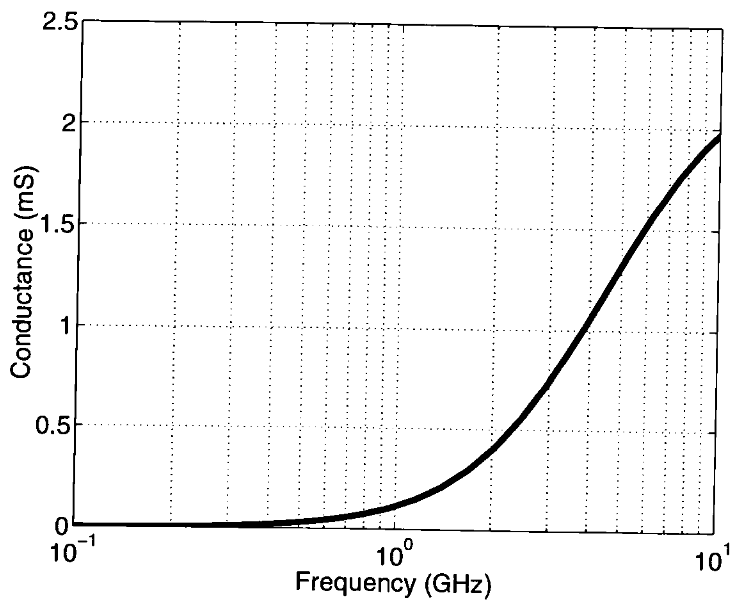


FIGURE 3.13. Q vs. trace width for 1-5 GHz for OD = 200 μm SLS inductor with s=2μm, variable turns and pitch.

equal to the total conductance of the bulk substrate. An example of the frequency dependence of capacitance and conductance for a spiral inductor on 10 Ω-cm bulk silicon is shown in Figure 3.14. In general, a simple C-G-C model topology can accurately represent the bulk/oxide substrate in terms of the vertical electric fields. For the example in Figure 3.14, the capacitance and conductance begin to change substantially in the low gigahertz range. Because this frequency-dependent behavior of the shunt terms is governed by substrate resistivity and oxide height, a design that is optimized in terms of the shunt capacitance and conductance for a particular process and frequency range may not necessarily perform optimally or even satisfactorily on a different silicon process.



(a)



(b)

FIGURE 3.14. a) Capacitance and b) Conductance vs. frequency for a typical spiral inductor on 10 Ω-cm bulk.

Clearly, the effects of the bulk silicon on shunt capacitance and conductance must be considered when designing spiral inductors for on-chip use.

3.4.3. Other Considerations: Wafer Thickness and Active/Doped Layers

Typical silicon wafer thicknesses range from 650 μm down to as thin as 200 μm depending on the intended packaging assembly. Hence, the performance of a spiral inductor, or any large scale passive component for that matter, can be significantly impacted by the thickness of the bulk substrate and the potentially closer proximity to a ground plane. Additionally, because spiral inductors that are fabricated on-chip are almost always in close proximity to active device circuitry, there will often be doped layers present in the substrate region just below the oxide. These layers can range from doped epitaxial layers to implant layers. The net result of this doping is generally a higher conductivity for the layers near or at the top of the substrate stack versus the surrounding bulk silicon. The modeling methodology developed in Chapter 3 can handle variable wafer thickness as well as doped layers in order to investigate their effects on inductor performance.

An example of the effects of doping is shown in Figures 3.15 and 3.16, for the case of a 3μm thick doped epitaxial layer with conductivity of 100 S/m (see Figure 3.17), as simulated using the distributed model from Chapter 2. Clearly, the addition of a doped layer for this example improves Q slightly near its peak, but lowers self-resonant frequency as well.

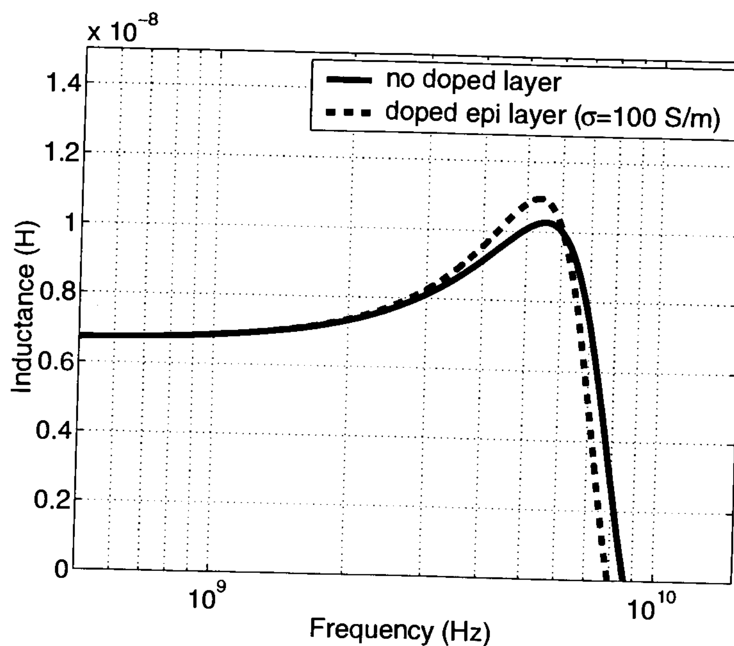


FIGURE 3.15. Inductance for inductor with and without doped epitaxial layer.

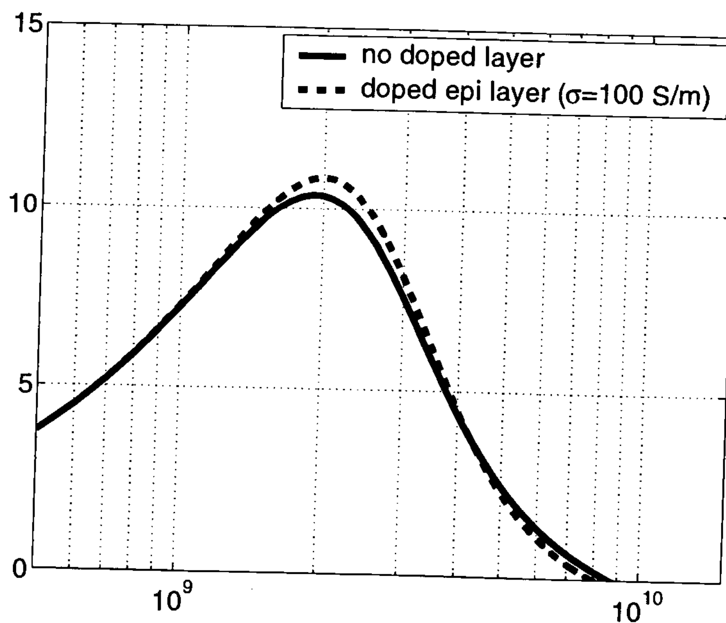


FIGURE 3.16. Quality factor for inductor with and without doped epitaxial layer.

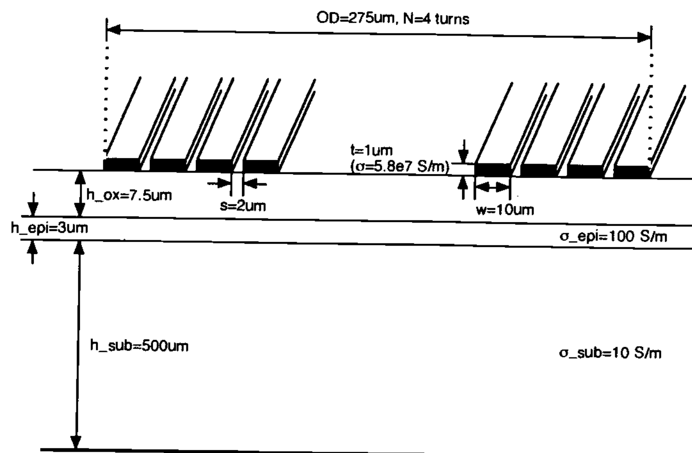


FIGURE 3.17. Cross-section for plots in Figures 3.15 and 3.16.

3.5. Conclusions

The effects of silicon, or any semiconducting material for that matter, on inductor performance have been examined in terms of process parameters and geometries. Due to the many design and process factors involved and their respective performance impacts, the process of optimization for even a simple single-level spiral (SLS) inductor is an arduous task. The plots presented in this chapter provide a solid starting point for an RFIC design project that involves inductors, since often one of the most fundamental tasks of any chip design is floor-planning, and inductors are relatively large in comparison to much of the active device circuitry and, therefore, must be considered early in the design phase.

4. DESIGN CONSIDERATIONS: MULTI-LEVEL VS. SINGLE-LEVEL SPIRAL INDUCTORS

4.1. Introduction

Numerous design techniques for spiral inductors in integrated circuits attempting to improve performance have been proposed and tested, including the use of multiple metallization layers [9, 10]. Multi-level spiral (MLS) inductors can be used to enhance the inductance/area ratios of spiral inductors in silicon-based RFICs and GaAs MMICs [10, 14]. Enhanced inductance can be achieved by judiciously placing multiple spirals on different metallization layers in a series configuration in order to increase the mutual inductive coupling. Further advantages of multi-level spiral inductors implemented in RFICs include higher circuit density, potentially lower series resistance, which increases as a nonlinear function of the number of turns for a single-level spiral (SLS) structure, and improved quality factor.

This chapter investigates multi-level spiral inductor design techniques and their effectiveness in improving the performance of on-chip spiral inductors. The multi-level spiral inductors discussed in this chapter are all in the so-called 'series configuration' where the top-level metallization spirals inward and the bottom-level spirals outward in the same sense, leading to an enhanced inductance through positive mutual inductive coupling. An example structure and the corresponding modeling method are illustrated in Figures 4.1 and 4.2.

The modeling methodology presented in [36] is used as a basis for the analysis of various multi-level spiral inductor configurations. Design issues discussed include self-resonant frequency (f_{SR}) and its relationship to geometrical configuration (e.g. number of metallization levels, conductor width and spacing) as

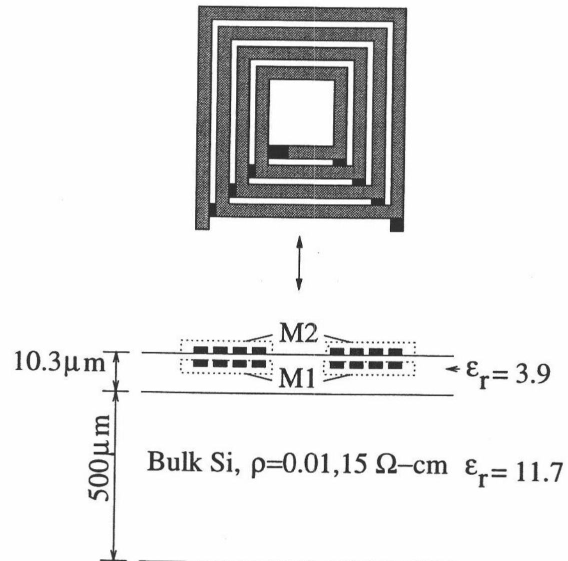


FIGURE 4.1. Example of a two-level series-connected spiral inductor on lossy silicon substrate.

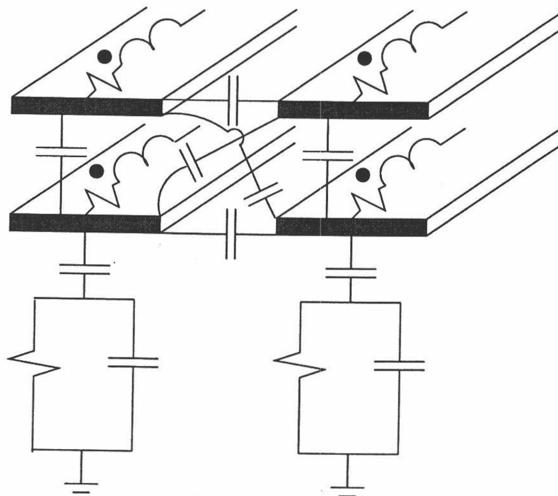


FIGURE 4.2. Equivalent circuit modeling of multi-level structure on lossy substrate.

TABLE 4.1. Summary of Single and Multi-level Inductor Parameters.

Size (mm^2)	No. of Levels	Turns Level	w/s ($\mu m/\mu m$)	L_o (nH)	R_{DC} (Ω)	f_{SR}(GHz)/Q_{max} (ρ_{sub} = 15Ω-cm)	f_{SR}(GHz)/Q_{max} (ρ_{sub} = 0.01Ω-cm)	Reference Figures
0.0256	2	5	10/5	7.91	5.26	5.0/12.5	5.0/4.6	4.3, 4.4
0.0625	1	8	10/5	7.81	6.66	8.9/9.4	6.2/3.1	4.3, 4.4
0.0484	2	7	10/5	20.48	9.94	2.2/9.4	2.2/4.5	4.3, 4.4, 4.8, 4.9
0.1156	1	11	10/5	19.19	12.16	3.5/7.4	3.0/2.7	4.3, 4.4
0.04	2	4	5/2	19.36	15.48	3.3/7.8	3.3/4.7	4.8, 4.9
0.0180	2	9	5/2	19.90	15.27	3.2/8.3	3.2/5.0	4.8, 4.9
0.04	2	4	10/5	11.48	6.69	2.8/9.8	2.9/4.2	4.6, 4.7
				11.18		4.4/11.0 (h_{M1}=6.2μm)	4.4/4.7 (h_{M1}=6.2μm)	
				10.93		5.5/10.2 (h_{M1}=4.2μm)	4.9/4.7 (h_{M1}=4.2μm)	

well as the effects of substrate parameters (e.g. bulk silicon conductivity and oxide thicknesses) on quality factor (Q). Example inductor structures are modeled and analyzed for typical BiCMOS and CMOS processes in order to demonstrate the important characteristics of multi-level spiral inductors as compared to their single-level counterparts. Table 4.1 details the parameters for the various structures studied in the following sections. For all cases, the metallization used is 1.15 μm thick copper, for which the net sheet resistance is approximately 15 m$\Omega/\Box$.

4.2. MLS vs. SLS: Quality Factor

Consider the performance of two MLS/SLS pairs having base inductance values of 8 and 20 nH. The width and spacing are 10 μm and 5 μm, respectively, for all cases. Figure 4.3 shows the simulated performance of the four inductors with a bulk substrate resistivity, ρ_{sub}, of 15 Ω−cm ($\sigma_{sub} = 6.\bar{6}$ S/m). Figure 4.3a shows a large reduction in f_{SR} for both MLS structures, while Figure 4.3b displays

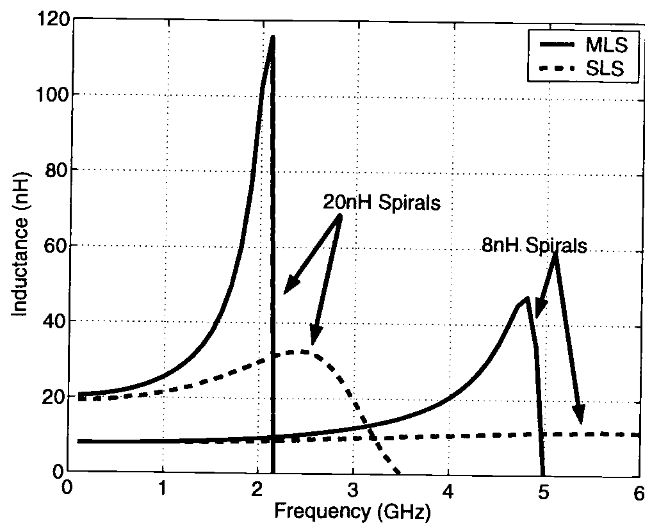
a significant improvement in low frequency Q. Similar results are obtained for the case of heavily-doped silicon substrate with $\rho_{sub} = 0.01$ Ω−cm ($\sigma_{sub} = 10,000$ S/m), with slightly less relative reduction in f_{SR}, as shown in Figure 4.4.

The improvement in quality factor for $\rho_{sub} = 15$ Ω−cm can be attributed to the top-level metallization being partially shielded electrically from the bulk substrate, thus reducing the shunt losses. For the case of $\rho_{sub} = 0.01$ Ω−cm, losses due to substrate eddy currents are typically dominant. Since for a given inductance and width/spacing the SLS is physically longer from end to end than the corresponding MLS, these series losses will have a more detrimental effect on the SLS performance in terms of Q. Also, it should be noted that DC resistance of the MLS is lower for all cases considered here, which can also improve Q.

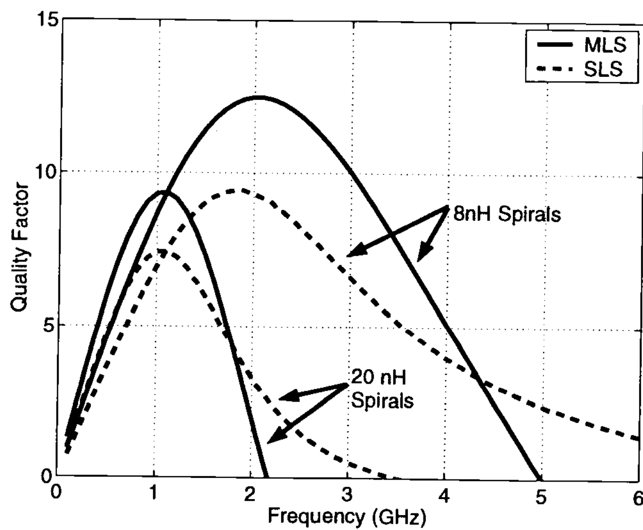
It should be further noted that the relative performance improvements shown here may not always be achievable due to additional factors such as lower metallization levels that often have relatively higher sheet resistances, which could raise the DC resistance of an MLS to a value that is much higher than that of its SLS counterpart. However, for cases where the oxide capacitance is the dominant factor in determining self-resonance, the MLS may not suffer from such a drastic reduction in f_{SR} as demonstrated above, and thus could achieve the same usable frequency range as its SLS counterpart.

4.3. Oxide Heights

In general, it is desirable to fabricate a spiral structure as far away as possible from a semiconducting substrate to minimize losses and in turn maximize performance. Single-level spiral inductors fabricated on upper metallization layers will have lower substrate coupling and consequently reduced loss, while f_{SR}

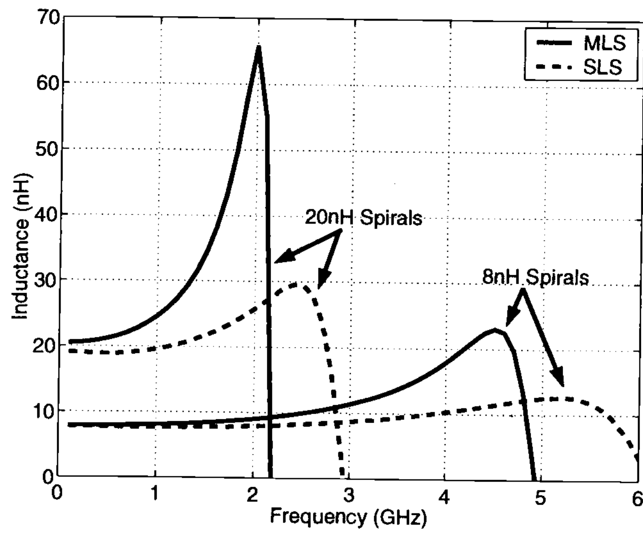


(a)



(b)

FIGURE 4.3. a) Inductance and b) Quality Factor for 8 and 20 nH spiral inductors with $\rho_{sub} = 15\Omega-$cm.



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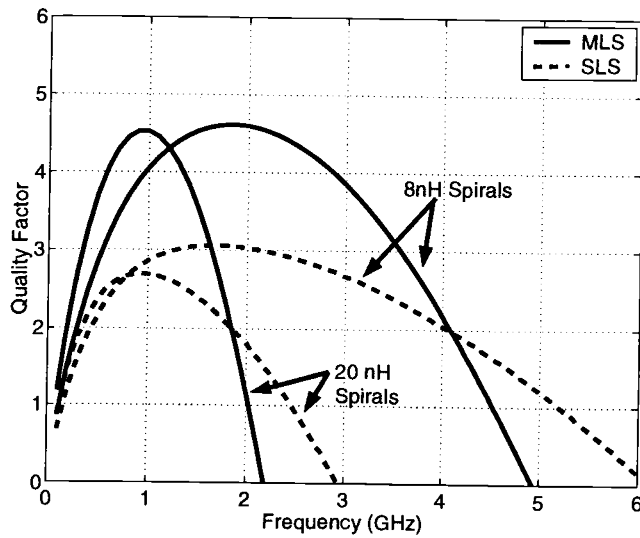


(b)

FIGURE 4.4. a) Inductance and b) Quality Factor for 8 and 20 nH spiral inductors with $\rho_{sub} = 0.01\Omega\text{–cm}$.

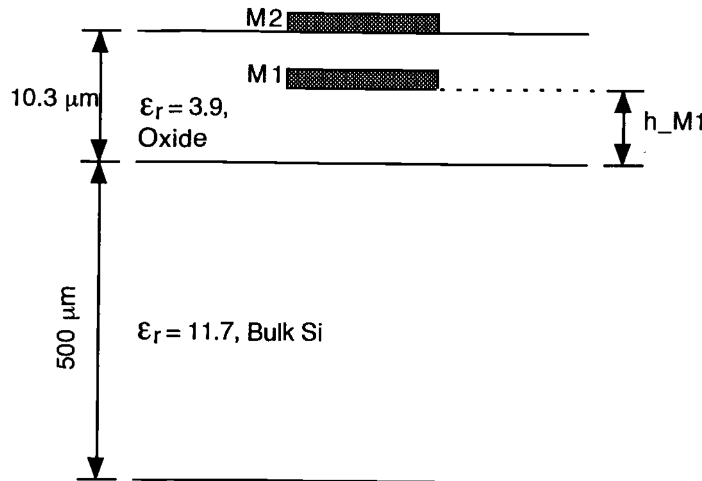
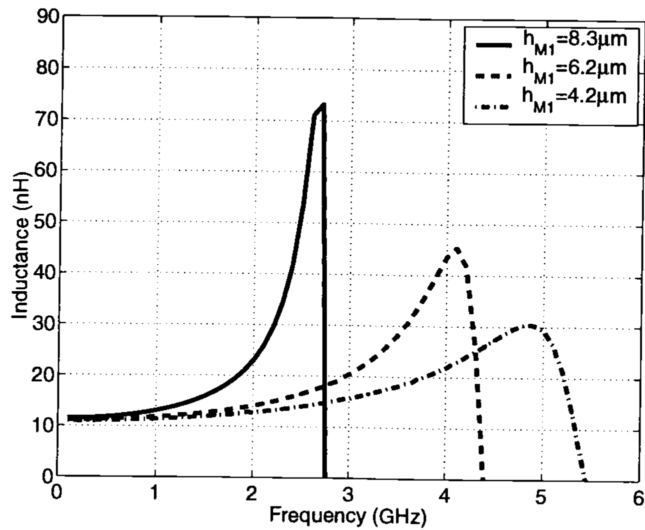
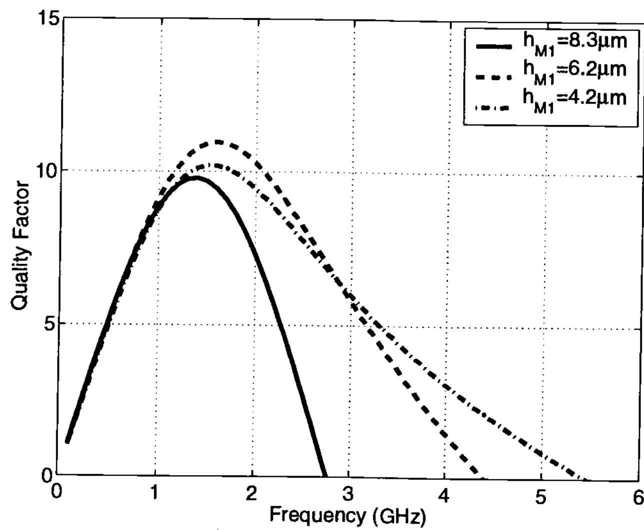


FIGURE 4.5. Illustration of variable M1 height, h_{M1}, for a multi-level spiral inductor.

is observed to increase due to a lower oxide capacitance. However, in the case of multi-level spiral inductors, broadside capacitive coupling between the metallization levels serves to reduce f_{SR} for the case of the series-connected structures under consideration here. Figures 4.6 and 4.7 show the simulated performance of four-turn two-level spiral inductors in various metallization level configurations, where the top metal M2 is at a height of 10.3 μm above the bulk and the height of M1 is the independent variable, h_{M1}, as indicated in Figure 4.5. The metallization level heights and thicknesses are typical of multi-level RFIC (e.g. RF CMOS, BiCMOS) processes. Clearly, maximizing the separation between the upper and lower levels of the spiral inductor leads to a higher f_{SR} as well as some improvement in quality factor, both for $\rho_{sub} = 15$ Ω–cm and $\rho_{sub} = 0.01$ Ω–cm.

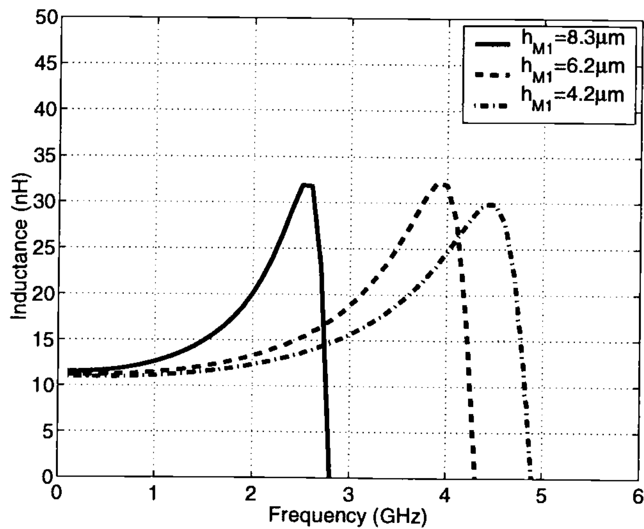


(a)

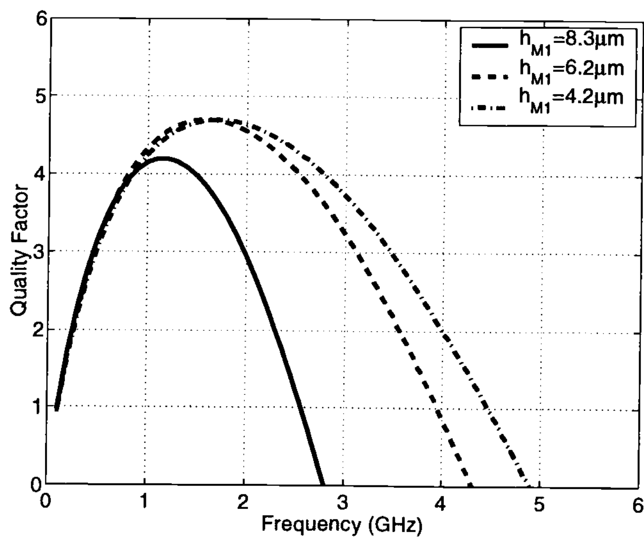


(b)

FIGURE 4.6. a) Inductance and b) Quality Factor for 4-turn spiral inductors with variable M1 height and $\rho_{sub} = 15\Omega\text{-cm}$.



(a)



(b)

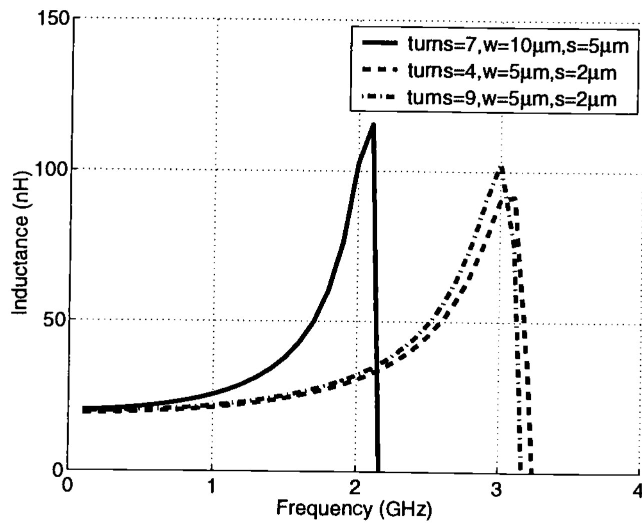
FIGURE 4.7. a) Inductance and b) Quality Factor for 4-turn spiral inductors with variable M1 height and $\rho_{sub} = 0.01\ \Omega\text{–cm}$.

4.4. Conductor Width and Spacing, Footprint

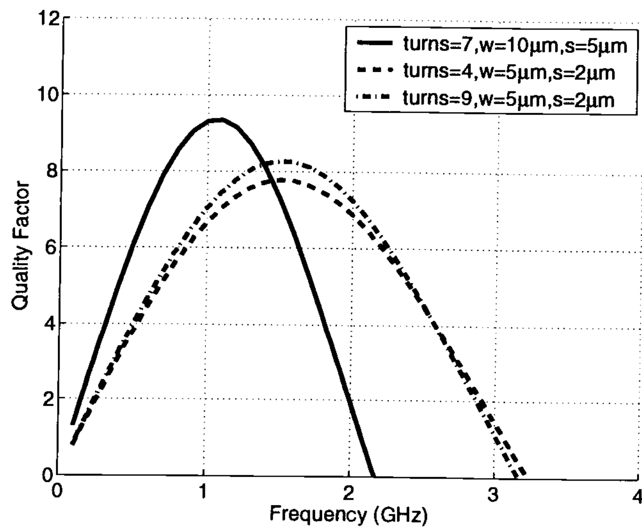
As the base (DC) resistance of an inductor is a design concern, one may be tempted to make the trace width as wide as possible for the technology being used. In this section three multi-level inductors all having a base inductance of 20nH are considered, one with width/spacing = 10/5 μm and the other two with width/spacing = 5/2 μm. The two inductors with identical width/spacing have four and nine turns with corresponding areas 200×200 μm^2 and 134×134 μm^2, respectively. Figures 4.8 and 4.9 show the simulation results for $\rho_{sub} = 15$ Ω−cm and $\rho_{sub} = 0.01$ Ω−cm, respectively. For both substrate resistivities there is a significant reduction in f_{SR} when a larger width and larger spacing are used. The reduced f_{SR} is a result of the larger level-to-level broadside capacitance. However, larger line width yields a higher Q at low frequencies for the case when $\rho_{sub} = 15$ Ω−cm, mainly due to a lower DC resistance and the fact that the shunt losses due to the semiconducting substrate are not large in this low frequency range. When ρ_{sub} is much lower, the losses due to substrate eddy currents can even be significant below 1 GHz, and thus a lowering DC resistance of the spiral inductor in this case has negligible effects on improving Q.

To illustrate the footprint reduction aspects of MLS's, the base (DC) inductance values for square multi-level spiral inductors and their single-level counterparts were computed as functions of footprint size, which is directly proportional to the number of turns in the top metallization level, for two different pairs of width and spacing with turns varying from 3 to 12. From Figure 4.10, it is clear that the MLS yields a much larger inductance for a given area.

In general, the base inductance value for an MLS inductor is almost four times that of an SLS when the two metallization levels used are closely spaced in

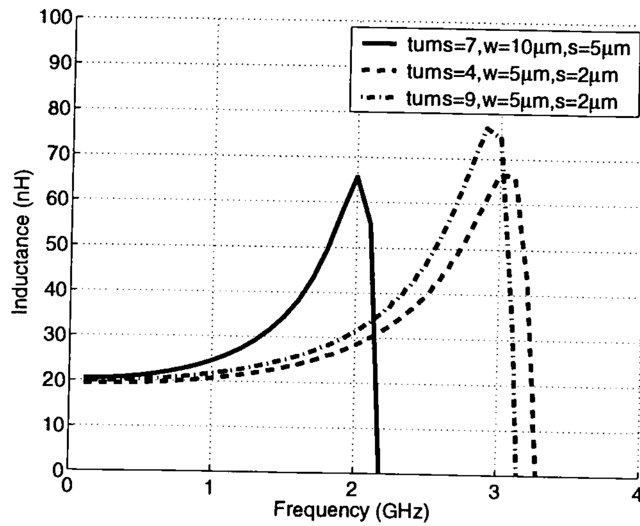


(a)

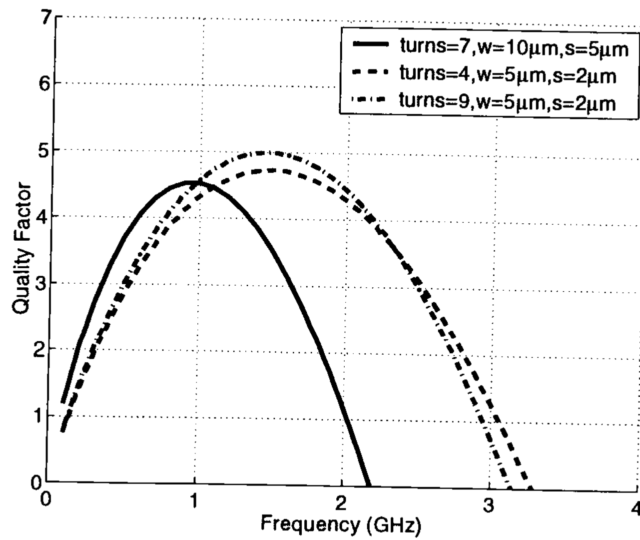


(b)

FIGURE 4.8. a) Inductance and b) Quality Factor for 20 nH spiral inductors with $\rho_{sub} = 15\ \Omega$–cm.



(a)



(b)

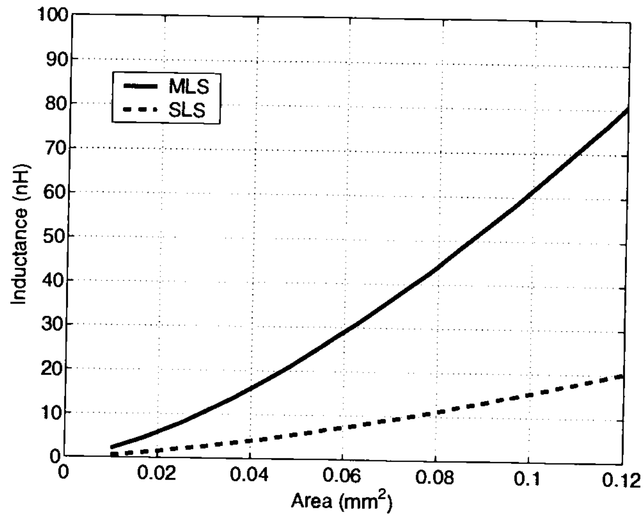
FIGURE 4.9. a) Inductance and b) Quality Factor for 20 nH spiral inductors with $\rho_{sub} = 0.01\ \Omega\text{-cm}$.

the vertical dimension. This can be best explained by considering the fact that for two identical spirals in close proximity to each other, the self inductance and mutual inductance terms are almost equal, thus the total inductance $L_{MLS} = 2L_{SLS} + 2M \lesssim 4L_{SLS}$.

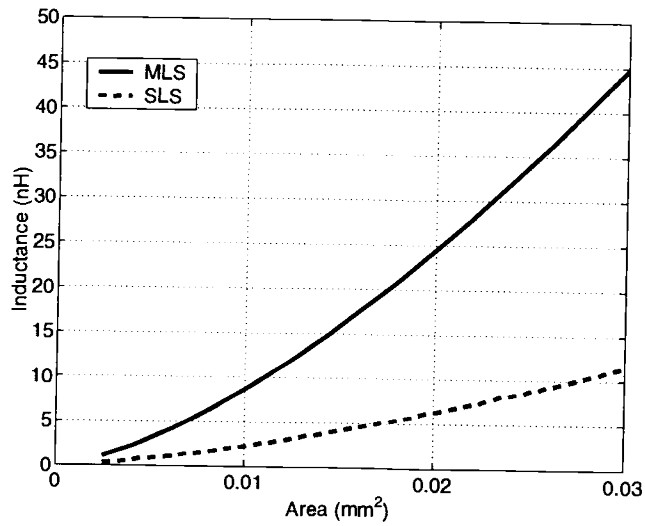
To illustrate the performance improvement of the MLS configuration, Figure 4.11 shows a comparison of multi-level and single-level spiral inductors in terms of their ratios of inductance to DC resistance, L_o/R_{DC} (nH/Ω). Here, both metallization levels are assumed to have a sheet resistance $R_s = 15\ m\Omega/\Box$, as stated previously. Note, however, that in most multi-level processes the lower metallization layers have higher sheet resistivities than the top level metallization, and thus this figure of merit, L_o/R_{DC}, may reduce to that of single-level spiral inductors or even lower, depending on the fabrication process.

4.5. Conclusions

It has been shown that, in comparison with typical single-level structures, multi-level spiral inductors in a 'series configuration' yield higher inductance/area ratios as well as potentially higher quality factors at low frequencies. However, the usable frequency range of series-connected multi-level spiral inductors is generally reduced as compared to single-level spiral inductors with the same inductance value. Smaller line width and pitch allow a higher inductance for a given area to be achieved, but at the expense of increased DC resistance. It was found that the DC resistance is a significant factor in determining low frequency Q for high resistivity substrates, but has little effect on spiral inductors over low resistivity substrates due to high losses caused by substrate eddy currents. In order to increase the usable frequency range of multi-level spiral inductors, maximum

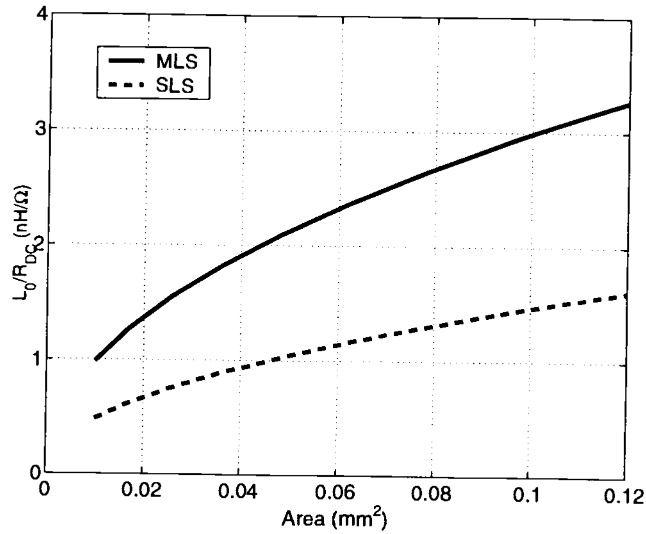


(a)

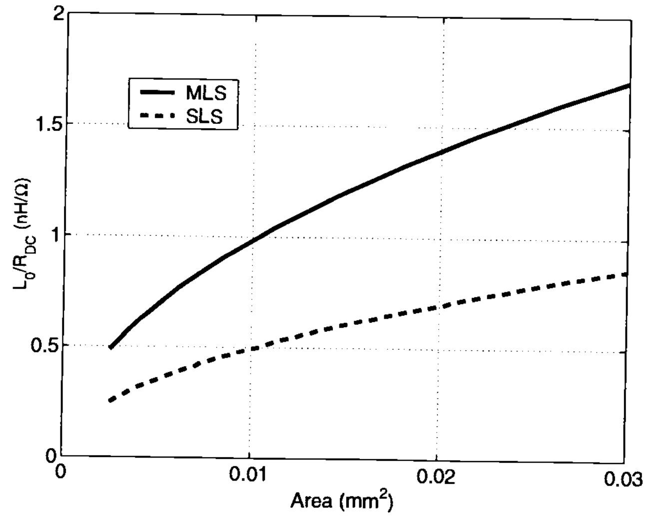


(b)

FIGURE 4.10. Inductance vs. Area for a) w = 10 μm, s = 5 μm, inner length = 25 μm, b) w = 5 μm, s = 2 μm, inner length = 20 μm.



(a)



(b)

FIGURE 4.11. L_o/R_{DC} vs. Area for a) w = 10 μm, s = 5 μm, inner length = 25 μm, b) w = 5 μm, s = 2 μm, inner length = 20 μm (R_s = 15 $m\Omega$/square).

vertical separation between the metallization levels is desired as this will reduce broadside capacitive coupling and thus increase f_{SR}. The analyses presented here are for typical multi-level spiral inductors implemented in BiCMOS and CMOS processes, and should prove to be useful in the design of RFICs.

5. MITIGATION OF UNDESIRABLE PERFORMANCE EFFECTS OF SILICON

5.1. Introduction

The modeling methods presented in the preceding chapters allow a designer to accurately analyze and optimize the performance metrics of silicon-based spiral inductors and interconnects within a given technology (e.g. BiCMOS, CMOS, etc.). However, it is also possible to further improve performance through use of shielding structures that are external, but in close proximity, to spiral inductors and interconnects. While the behavior of on-chip spiral inductors is of critical importance to integrated circuit design, the performance of silicon-based interconnects is also a primary concern [38]. In addition to the conductor loss of the interconnect, the lossy nature of the silicon substrate can give further rise to significant signal attenuation and considerable dispersion in broadband signals. To reduce the effect of substrate loss on the quality factor of on-chip planar spiral inductors, patterned ground shields (PGS) located between the spiral inductor and the silicon substrate have recently been proposed [39], [40]. In this chapter, the use of an orthogonal grid of grounded lines is proposed to significantly reduce loss and signal dispersion on both on-chip interconnects and spiral inductors [41, 42].

In order to study the orthogonal gridded shield, simple interconnect structures are analyzed first, followed by an application of the gridded shield to spiral inductors. The complicated dispersive transmission characteristics of unshielded uniform interconnects on silicon substrate have been studied extensively by experiment (e.g. [23], [43]) and by electromagnetic analysis (e.g. [25], [26]). Here, a full-wave electromagnetic characterization of the shielding effect of the orthogonal

grid of grounded lines on the dispersion and loss characteristics of on-chip interconnects on silicon substrate is presented. Because of the periodic loading of the interconnect by the orthogonal grid, the characteristics of the shielded interconnect structure may be determined in terms of a unit cell [44], which substantially reduces the computational load for full-wave electromagnetic simulation. The unit-cell analysis approach has been applied previously to other periodic slow-wave transmission structures such as periodically loaded transmission lines for velocity matching with electro-optic modulators ([45]- [47]). In the following, the enhanced transmission characteristics of on-chip interconnects with orthogonal gridded shield are demonstrated in terms of the frequency-dependent per-unit-length (p.u.l.) transmission line parameters as well as by the step response of the shielded interconnect. Furthermore, the equivalent circuit model for the shunt admittance of unshielded on-chip interconnects is extended to include the effects of shielding. Finally, the distributed inductor modeling methodology from Chapter 2 is augmented to incorporate the effects of a patterned ground shield (PGS) and thus allow for predictions of performance enhancements resulting from various shield configurations.

5.2. Orthogonal Gridded Shields

Figure 5.1 shows a microstrip-type on-chip interconnect with an orthogonal grid of grounded lines located at the interface between the oxide and the bulk silicon substrate. To provide insight into the objective of such an orthogonal gridded shield, a review of on-chip interconnects without the substrate shielding structure is in order. The characteristics of uniform on-chip interconnects on silicon can be expressed in terms of the frequency-dependent per-unit-length (p.u.l.) line pa-

rameters R, L, G, C. The frequency-dependent behavior of the transmission-line parameters is best explained by considering the low and high frequency limits. Recall from Chapter 3 that in the low frequency limit, the displacement current in the silicon substrate is small compared to the conduction current ($\sigma \gg \omega\epsilon$) and, hence, the shunt capacitance C is given by the oxide capacitance. In contrast, at low frequencies the magnetic fields are unaffected by the presence of the lossy silicon substrate, and the series inductance L is determined only by the configuration of the interconnect and current return path in the ground plane. In the high frequency limit, the shunt displacement currents in the silicon substrate are dominant ($\sigma \ll \omega\epsilon$), significantly lowering the shunt capacitance C. Furthermore, the time-varying magnetic fields in the lossy silicon substrate lead to a strong longitudinal current distribution near the oxide/silicon interface, which causes a significant reduction in the series inductance L and increase in series resistance R. The transitions from the low-frequency L and C values to the high-frequency values occur at different frequencies for L and C and depend strongly on the substrate resistivity. For relatively low bulk resistivities of the silicon substrate on the order of 0.01 Ω-cm ($\sigma_{\text{Si}} \approx 10,000$ S/m), which is typical of analog CMOS processes, the R and L parameters typically exhibit significant variation in the low gigahertz range while C and G remain relatively flat up to frequencies of tens of gigahertz. In contrast, for medium-to-high resistivity substrates on the order of 10 Ω-cm, both C and G vary significantly in the low gigahertz range while L is nearly constant up to frequencies of tens of gigahertz [48], [49].

The objective of the proposed grounded orthogonal grid between the on-chip interconnect and substrate (Fig. 5.1) is to significantly reduce the frequency-dependence of the shunt capacitance parameter C without affecting the series inductance L, as well as reduce shunt loss for substrates with resistivity ρ_{Si} on

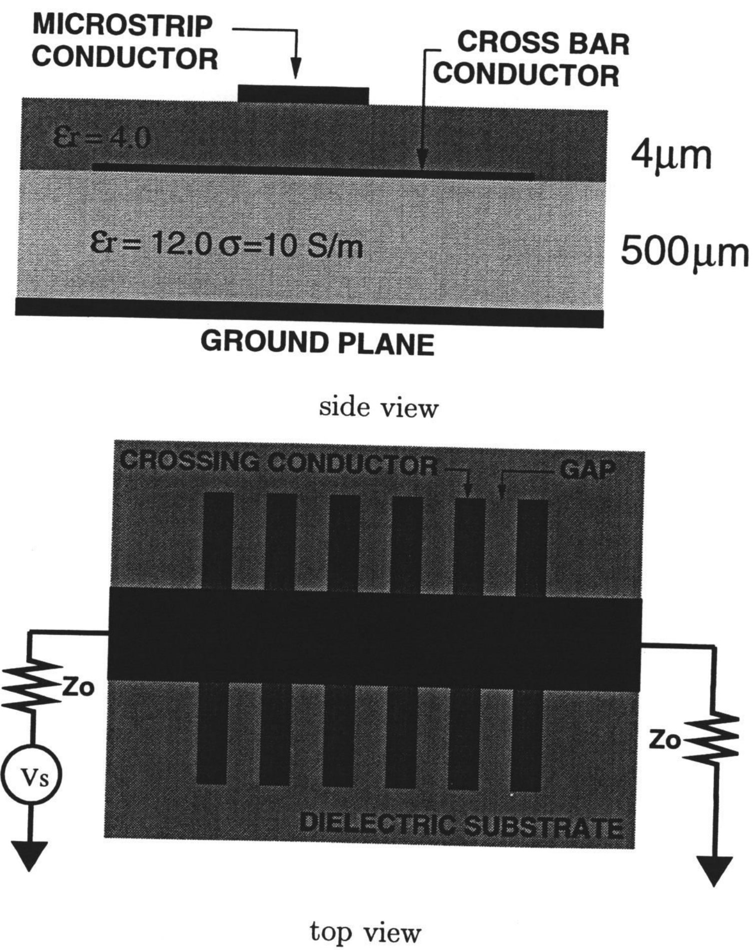


FIGURE 5.1. Orthogonal gridded substrate shielding structure for silicon-based on-chip interconnects.

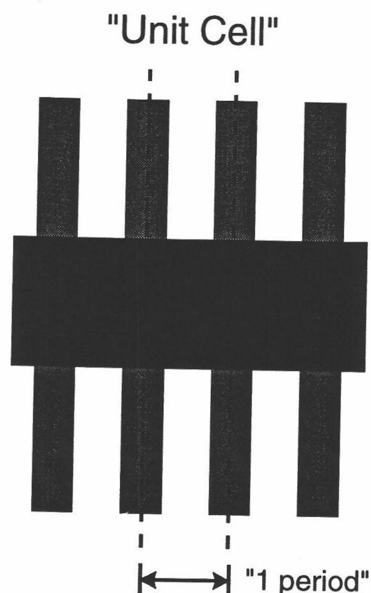


FIGURE 5.2. Definition of unit cell and cell boundaries.

the order of 10 Ω-cm ($\sigma_{\text{Si}} \approx 10$ S/m) and frequencies of operation in the RF-to-microwave range. The grounded orthogonal grid is used to capacitively load the interconnect structure at higher frequencies and effectively extend the 'slow-wave' mode region [23] to higher frequencies while not significantly affecting the series inductance L. As a result, the reduced frequency-dependence of C and reduced shunt loss leads to lower dispersion over a broader bandwidth for on-chip interconnects on silicon substrates with resistivities on the order of 10 Ω-cm that are typically found in modern CMOS and BiCMOS processes used for analog and mixed-signal ICs.

5.2.1. Unit-Cell Analysis

Because the orthogonal shielding lines illustrated in Fig. 5.1 form a periodic grid, the shielded interconnect may conveniently be analyzed in terms of its unit-cell characteristics. Figure 5.2 indicates the unit-cell region of the shielded line structure, corresponding to one period, with boundaries along the center of adjacent crossbars. Since the grid period is much smaller than the wavelength in the frequency range of interest, the interconnect with the gridded shielding structure can be characterized in terms of effective per-unit-length R, L, G, C parameters. The effective R, L, G, C parameters are derived from the $ABCD$ parameters, obtained here with the full-wave planar electromagnetic field solver Agilent Momentum [37]. This field solver is based on a mixed-potential method-of-moments approach. The $ABCD$ parameters of a section of uniform transmission line are

$$A, D = \cosh(\gamma l) \tag{5.1}$$

$$B = Z_0 \sinh(\gamma l) \tag{5.2}$$

$$C = Y_0 \sinh(\gamma l) \tag{5.3}$$

where Z_0 is the characteristic impedance, γ is the propagation constant, and l is the length of the transmission line. From (5.1-5.3) the effective characteristic impedance and propagation constant are then obtained as

$$\gamma = \frac{1}{l} \cosh^{-1} \left[\frac{A+D}{2} \right] \tag{5.4}$$

$$Z_0 = \frac{2B}{D - A \pm \sqrt{(A+D)^2 - 1}} \tag{5.5}$$

Here the length l of the structure under consideration is equal to one period of the orthogonal gridded shield. With (5.4) and (5.5) the effective R, L, G, C parameters are determined as

$$R(\omega) + j\omega L(\omega) = Z_0\gamma \tag{5.6}$$

$$G(\omega) + j\omega C(\omega) = \gamma/Z_0 \tag{5.7}$$

Figures 5.3 and 5.4 show the effective $R(\omega)$, $L(\omega)$, $G(\omega)$, and $C(\omega)$ parameters for unit-cell test structures with different degrees of shielding coverage. The term 'coverage' indicates the fractional amount of bulk substrate that is shielded relative to a solid ground shield, and is defined as

$$c = \frac{w_c}{w_c + s_c} \tag{5.8}$$

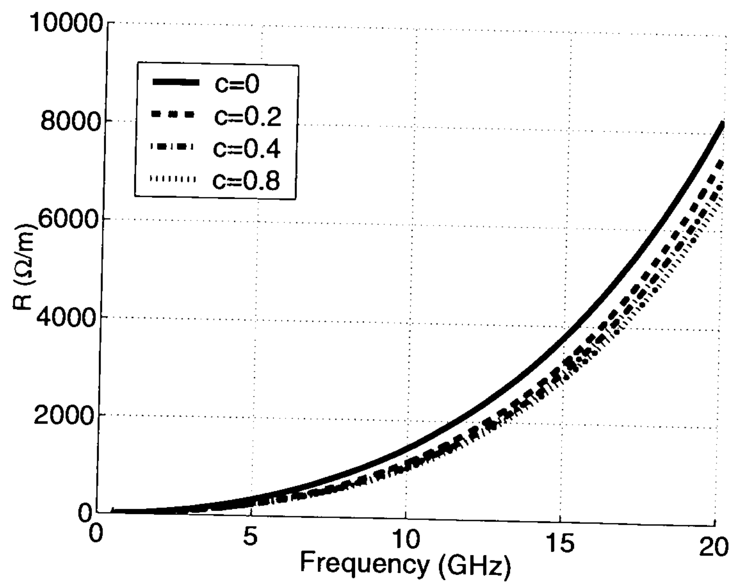
where w_c and s_c are the crossbar width and edge-to-edge spacing, respectively. Thus, a crossing line width of 50 μm with 75 μm edge-to-edge separation corresponds to a fractional coverage of $c = 0.4$ and a unit-cell length equal to 125 μm. The interconnects for these example structures all have a width of $w = 10$ μm with oxide height $h_{\text{ox}} = 4$ μm, which are typical dimensions used in analog IC designs and are amenable to full-wave electromagnetic simulation in the frequency range of interest. The bulk silicon substrate is $h_{\text{Si}} = 500$ μm thick and has a resistivity of $\rho_{\text{Si}} = 10$ Ω-cm. The crossing lines are 50 μm wide and 70 μm long, and are located directly on top of the bulk silicon substrate, as illustrated in Fig. 5.1. Because perfect conductors are used here for all simulation results in order to exemplify the effect of shielding, the only contribution to the series resistance parameter $R(\omega)$ is from the longitudinal current distribution in the bulk Si substrate; hence, $R(\omega = 0) = 0$. In addition, $L(\omega)$ is nearly flat in the frequency range of interest as the longitudinal substrate currents have an insignificant effect on inductance. Also, since perfect conductors are used, there will be no change in inductance due to conductor skin effect.

The results shown in Figs. 5.3 and 5.4 demonstrate that the orthogonal grid shielding structure leads to a significant reduction in capacitance variation

over a broad frequency range while the inductance value is nearly unaffected up to a large fractional coverage. It is further seen that the capacitance variation over frequency is already significantly reduced with a low level of shielding coverage.

5.2.2. Implementation of Orthogonal Gridded Shield

The necessary shielding condition that all crossbars be grounded may be difficult to ensure or implement in standard IC fabrication processes. Figure 5.5 shows a more practical implementation of the proposed orthogonal gridded shielding structure. Here, the crossbars are connected together by a sidebar (this topology will be termed 'sidebar configuration'), which is parallel to the interconnect and grounded only at the ends, as illustrated in Fig. 5.5. For the results presented here, the sidebar is 25 μm in width and is separated laterally from the interconnect by 30 μm edge-to-edge. To demonstrate the validity of the unit-cell analysis approach, a shielding structure consisting of four unit cells is analyzed both in terms of cascaded unit cells described as four-port networks and by full-wave simulation of the entire four-cell structure. Figures 5.6 and 5.7 show a comparison of the effective p.u.l. line parameters computed by both approaches. In addition, results are shown for the unshielded case ($c = 0$) as well as the completely shielded interconnect ($c = 1.0$). It is clear that the presence of the sidebar parallel to the interconnect leads to a noticeable reduction in inductance. This inductance reduction, however, is still much smaller than the approximately 80% reduction for a solid ground shield ($c = 1.0$), as seen in Fig. 5.6. The effect of the sidebar on inductance could be alleviated by placing the sidebar farther away from the interconnect. This, however, could result in an interconnect structure that is too wide for practical use. Also, because a sidebar that is placed farther from



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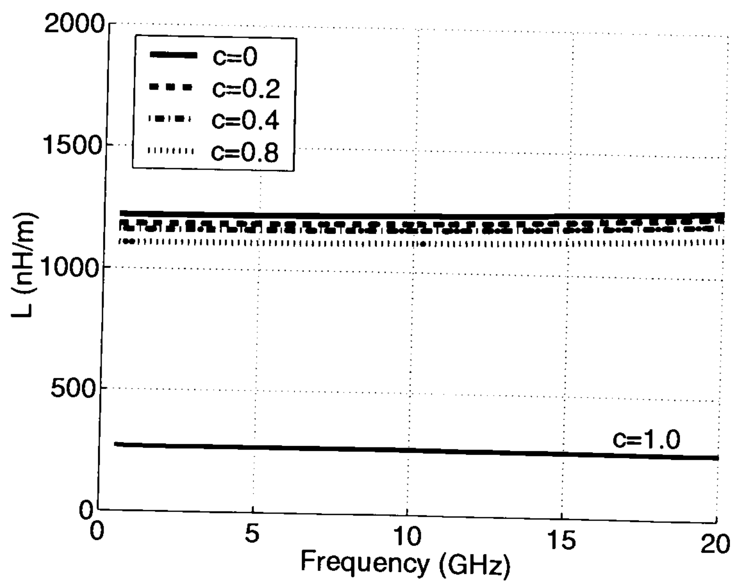
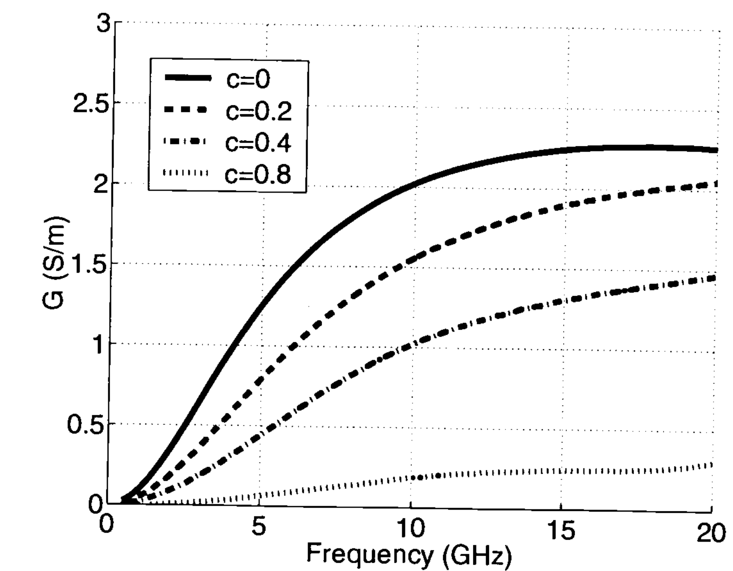


(b)

FIGURE 5.3. (a) Series resistance and (b) inductance p.u.l. for w = 10 μm interconnect with orthogonal gridded shield.



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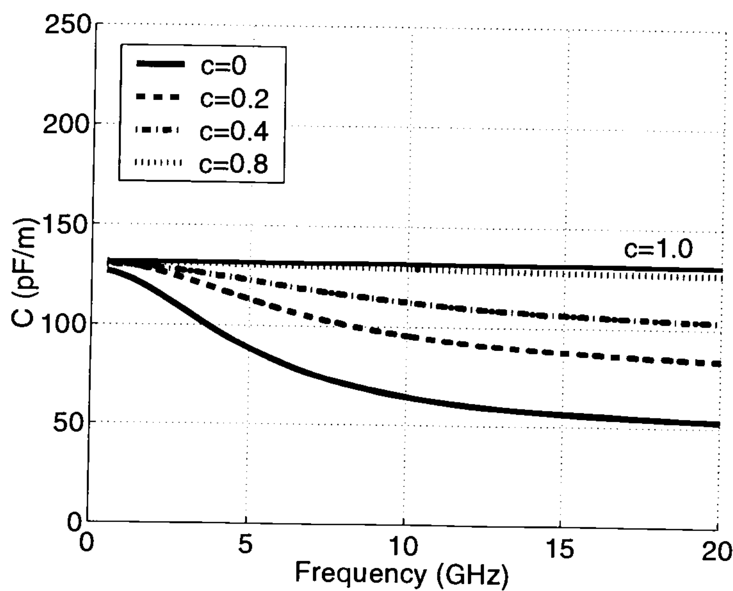


(b)

FIGURE 5.4. (a) Shunt conductance and (b) capacitance p.u.l. for w = 10 μm interconnect with orthogonal gridded shield.

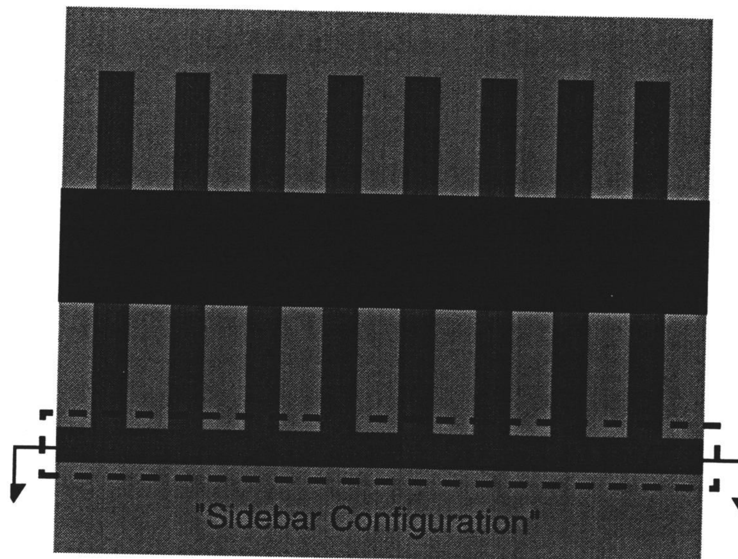


FIGURE 5.5. Practical implementation of orthogonal gridded shield.

the interconnect necessitates the use of longer orthogonal ground lines, the additional inductance and resistance (assuming finite conductivity ground lines) of these longer lines will reduce the effectiveness of the ground shield. To avoid use of a sidebar, each crossbar could be grounded separately by vias.

5.2.3. Equivalent Circuit Model for Effective Shunt Admittance

The use of effective transmission line parameters for the interconnect with substrate shielding suggests a simple extension of the equivalent circuit model of the unshielded interconnect. Since the inductance and resistance parameters are nearly unaffected by the shielding structure, the equivalent circuit for the series impedance of the unshielded interconnect derived from a rational polynomial approximation and described in detail in [48] and [50] can be used. The common $C_{ox} - G_{Si} - C_{Si}$ equivalent circuit topology shown in Fig. 5.8 may be used to

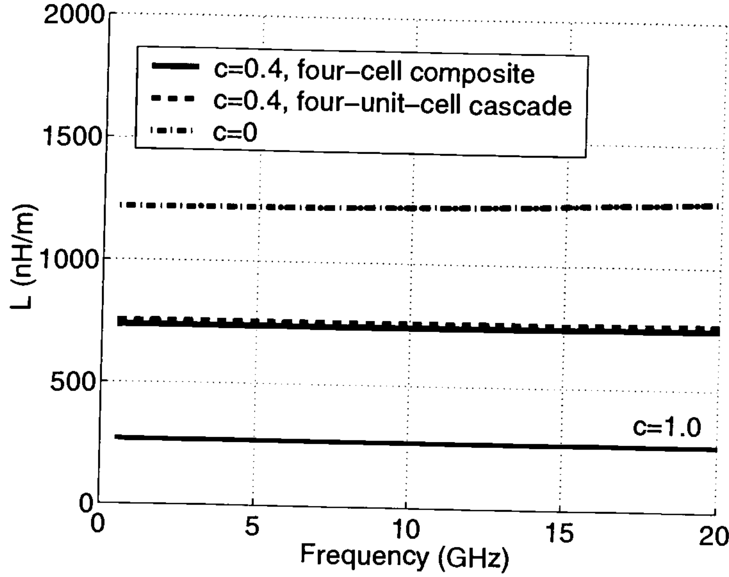
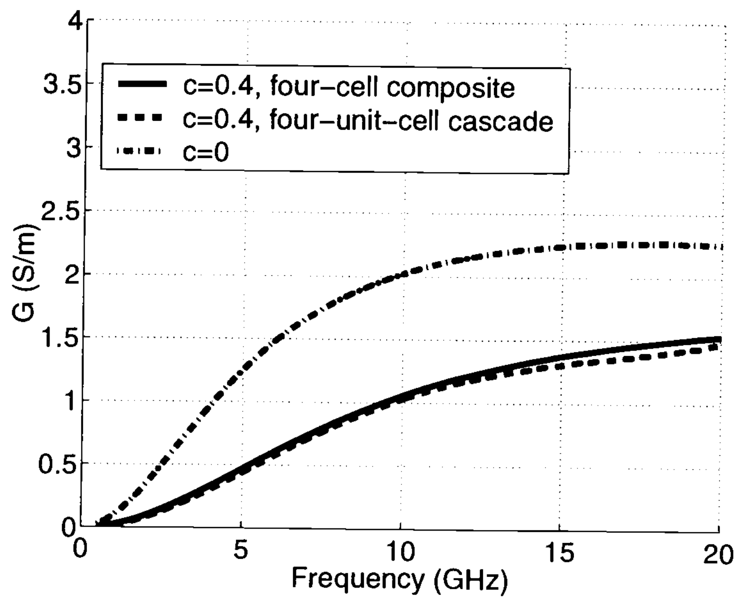


FIGURE 5.6. Inductance p.u.l. for w = 10 μm interconnect with orthogonal gridded shield in sidebar configuration.

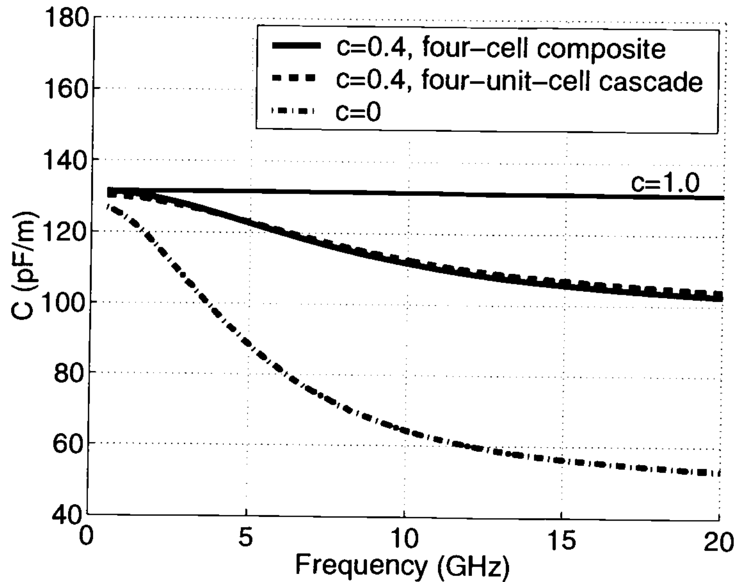
model the shunt admittance for both the unshielded and shielded interconnects. The presence of the grounded orthogonal grid effectively changes the substrate capacitance and conductance while the effect on the oxide capacitance is negligible. Referring to the equivalent circuit shown in Fig. 5.8, the values for the equivalent circuit elements can be directly extracted from the effective p.u.l. shunt admittance.

$$Y_{\text{eff}}(\omega) = G_{\text{eff}}(\omega) + j\omega C_{\text{eff}}(\omega) = \frac{(G_{\text{Si,eff}} + j\omega C_{\text{Si,eff}})j\omega C_{\text{ox}}}{G_{\text{Si,eff}} + j\omega(C_{\text{ox}} + C_{\text{Si,eff}})} \tag{5.9}$$

of the shielded line at a single frequency ω_0 within the range of interest and use of the relationship $C_{\text{Si}}/G_{\text{Si}} = \epsilon_{\text{Si}}/\sigma_{\text{Si}}$. The extracted parameters of the shunt admittance equivalent circuit model are



(a)



(b)

FIGURE 5.7. (a) Shunt conductance and (b) capacitance p.u.l. for w = 10 μm interconnect with orthogonal gridded shield in sidebar configuration.

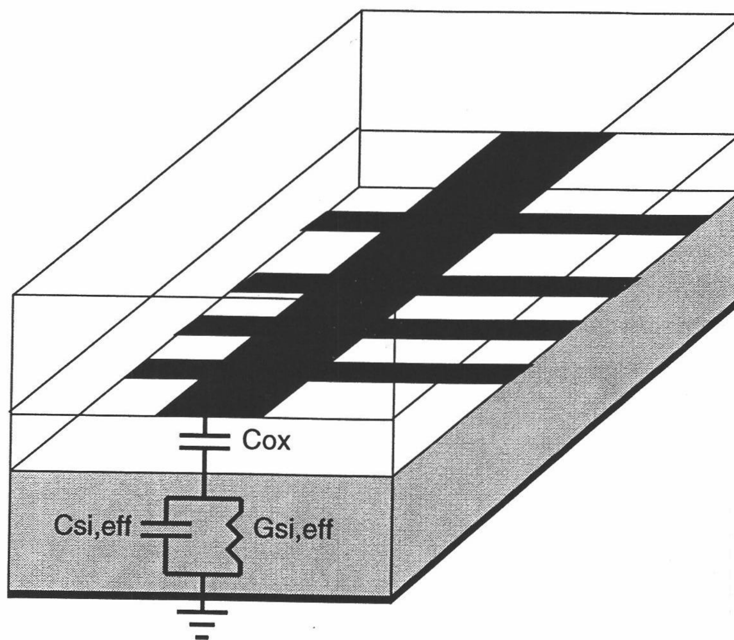


FIGURE 5.8. Equivalent circuit for effective shunt admittance of interconnect with orthogonal gridded shield.

$$G_{\text{Si,eff}}(\omega_0) = \frac{1}{\text{Re}\left\{\frac{1}{G(\omega_0) + j\omega_0 C(\omega_0)}\right\}\left(1 + \left(\frac{\omega_0 \epsilon_{\text{Si}}}{\sigma_{\text{Si}}}\right)^2\right)} \tag{5.10}$$

$$C_{\text{Si,eff}} = \frac{\epsilon_{\text{Si}}}{\sigma_{\text{Si}}} G_{\text{Si,eff}} \tag{5.11}$$

$$C_{\text{ox}}(\omega_0) = \frac{1}{-\text{Im}\left\{\frac{\omega_0}{G(\omega_0) + j\omega_0 C(\omega_0)}\right\} - \frac{\omega_0^2 C_{\text{Si,eff}}}{\left(G_{\text{Si,eff}}^2 + (\omega_o C_{\text{Si,eff}})^2\right)}} \tag{5.12}$$

The values of the resulting model elements are found to be nearly independent of the choice for the matching frequency, ω_0. The equivalent circuit topology described above yields an excellent broadband match to the total frequency-dependent shunt admittance. It is found that the effective substrate capacitance $C_{\text{si,eff}}$ and conductance $G_{\text{si,eff}}$ for the shielded interconnect are significantly higher compared to the unshielded case while the oxide capacitance $C_{\text{ox,eff}}$ ($\approx$ 130 pF/m for the example structures with interconnect width w = 10 μm) is relatively unchanged. Table 5.1 shows the effective substrate shunt conductance $G_{\text{si,eff}}$ for different levels of shielding coverage, c, extracted at 10 GHz. The effective substrate capacitance is directly related to the effective conductance by (5.11). For example, for a coverage of $c = 0.4$ and interconnect width w = 10 μm, the effective substrate capacitance $C_{\text{si,eff}}$ is approximately 360 pF/m.

5.3. Dispersion Characteristics

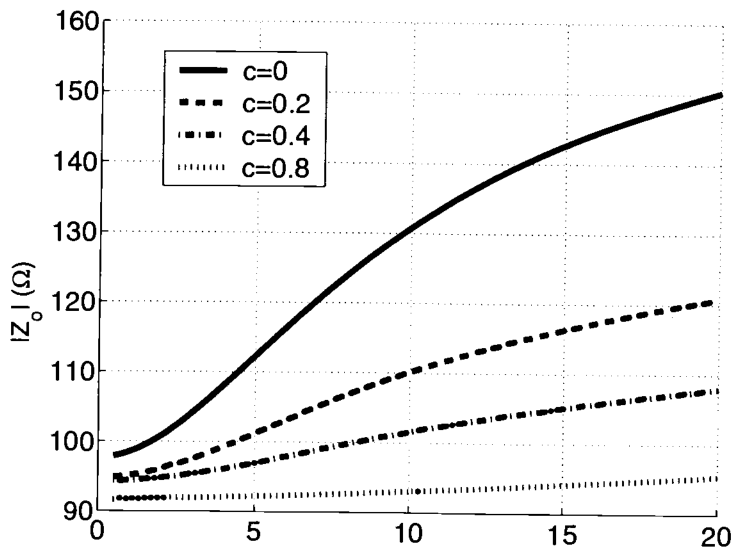
By extending the frequency range of the 'slow-wave' mode, interconnects with orthogonal gridded shield should exhibit lower dispersion for signals with spectral content reaching into the RF/microwave frequency range. Figure 5.9

TABLE 5.1. Effective Substrate Conductance versus Shielding Coverage Extracted using (5.10) at 10 GHz.

Fractional Coverage $\left(c = \frac{w_c}{w_c+s_c}\right)$	$G_{\text{Si,eff}}$ (S/m)	
	w=10 μm	w=50 μm
0	7	9
0.2	17	29
0.4	34	68
0.625	80	164
0.8	243	625

shows the magnitude of the characteristic impedance $|Z_0|$ and phase velocity v_p of an interconnect of width w = 10 μm for different levels of shielding coverage. It is apparent from the flattening of the $|Z_0(\omega)|$ and $v_p(\omega)$ functions for increased shielding coverage that the impedance and dispersion characteristics of the shielded lines are significantly improved over the unshielded case.

Figure 5.10 shows the step response of an on-chip interconnect with different levels of shielding coverage to demonstrate the reduction in signal dispersion in the time domain. The interconnects were matched at the source to the low-frequency characteristic impedance, which is approximately 95 Ω, and terminated in Z_t = 10 kΩ. As expected, a significant improvement in the time-domain response is achieved as a result of shielding.



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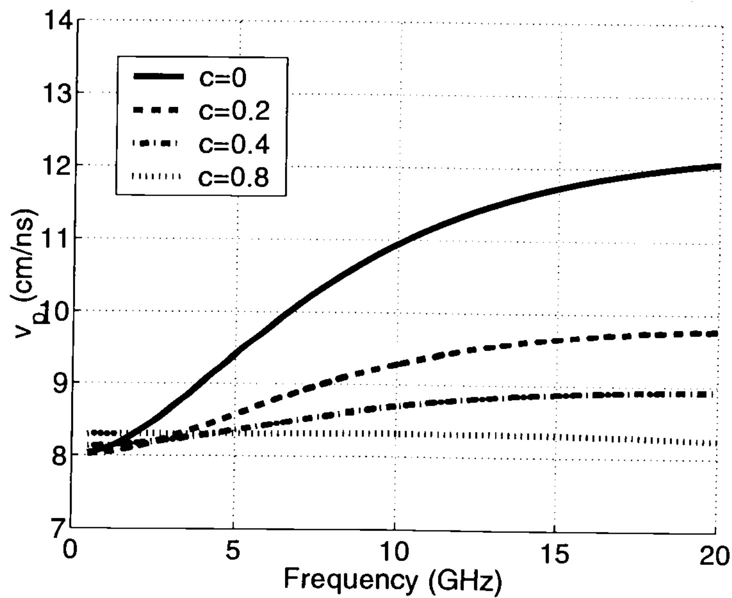


(b)

FIGURE 5.9. (a) Characteristic impedance and (b) phase velocity for interconnects of width w = 10 μm with orthogonal gridded shield.

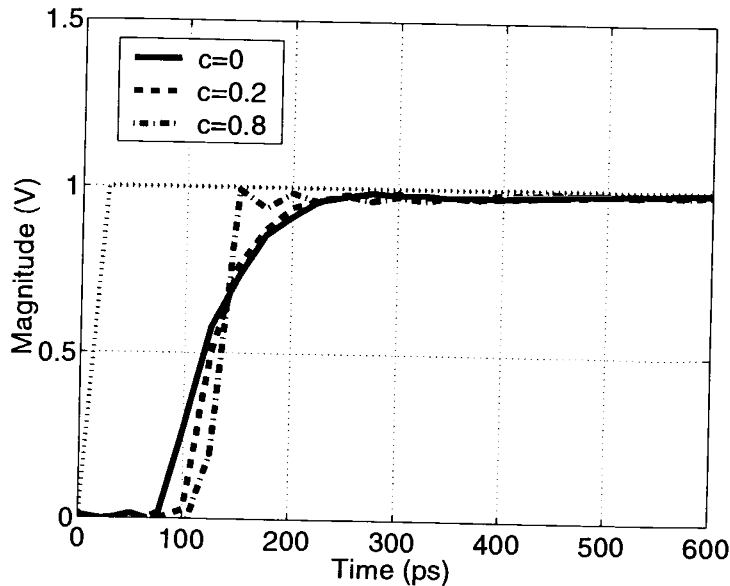


FIGURE 5.10. Comparison of step responses for shielded and unshielded interconnects.

5.4. Application to Spiral Inductors

Just as transmission lines over semiconducting substrates may benefit from the use of orthogonal gridded shields, so may spiral inductors fabricated in silicon technology. To investigate the feasibility of using such shields, several test cases were run using the Agilent Momentum Planar 3D EM simulator. An example structure is shown in Figure 5.11, where the orthogonal gridded shield, or patterned ground shield (PGS), consists of many 'fingers' that are connected to each other by a common ring running around the perimeter. It is important to note that this ring must not be continuous, otherwise the self-inductance of the spiral will be lowered due to inductive loading by the ring. In common practice, a small gap is used to avert this undesired effect.

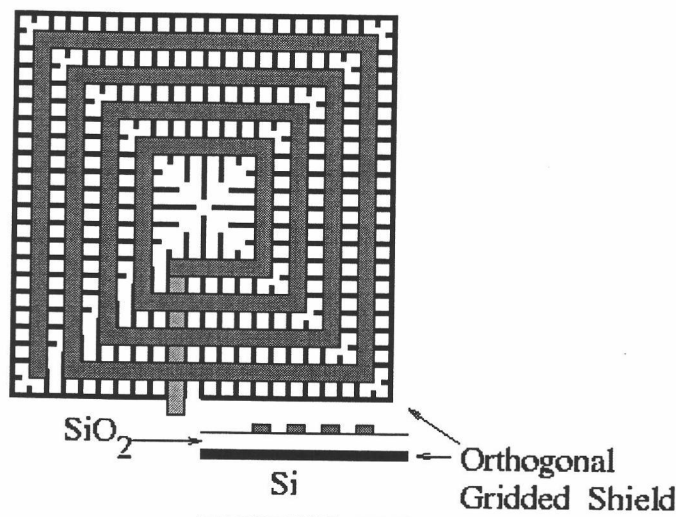


FIGURE 5.11. Example of spiral inductor with patterned ground shield (PGS).

5.4.1. Simulation Examples

Figure 5.12 shows the 4-turn spiral inductor used as a test structure for various shielding cases. The dimensions for this spiral are typical of inductors used in RFICs operating in the 1-6 gigahertz range and fabricated in technologies where the bulk Si resistivity is on the order of 10 Ω-cm.

In Figure 5.13, inductance and Q are plotted for a spiral with and without a gridded shield. The coverage factor, c, for the shielded case is approximately 0.5. There is a significant decrease in the self-resonant frequency for the shielded spiral, as well as an increase in peak Q. As with the interconnects discussed in the previous sections, the net shunt capacitance of the spiral is more constant as a function of frequency and therefore remains close to the DC value of C_{ox}. As a consequence the self-resonant frequency is decreased. Since much of the shunt losses are mitigated by the shield, Q is increased.

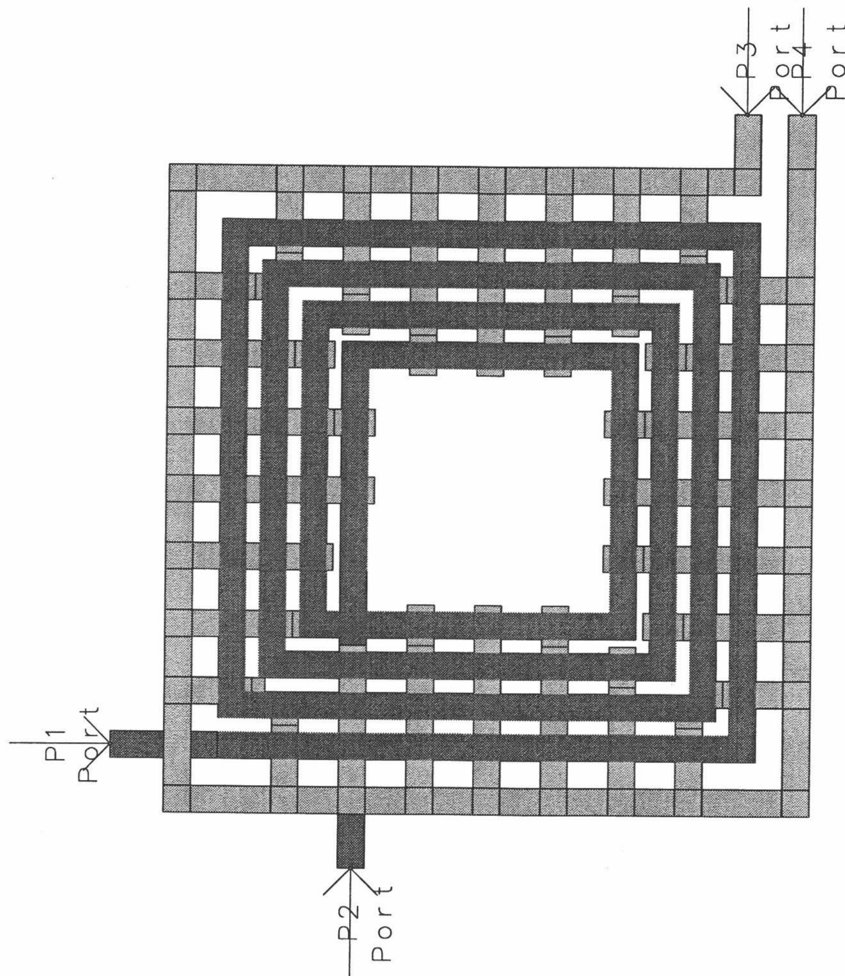
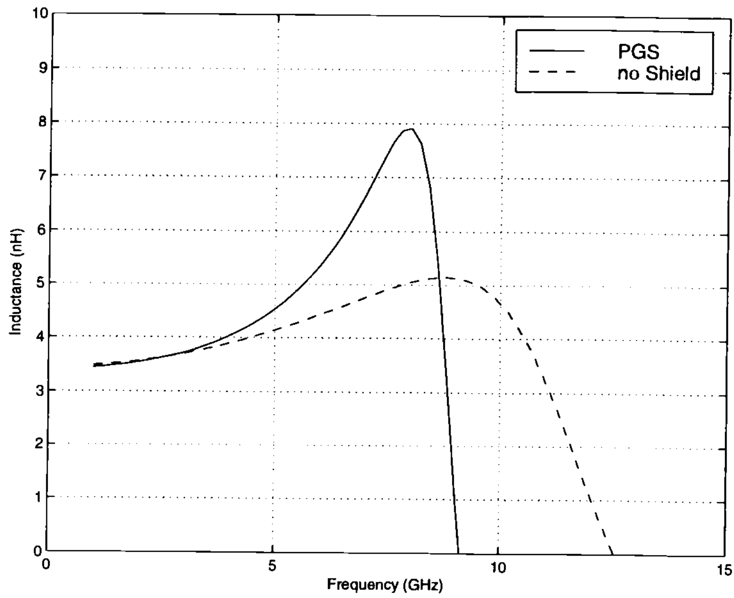
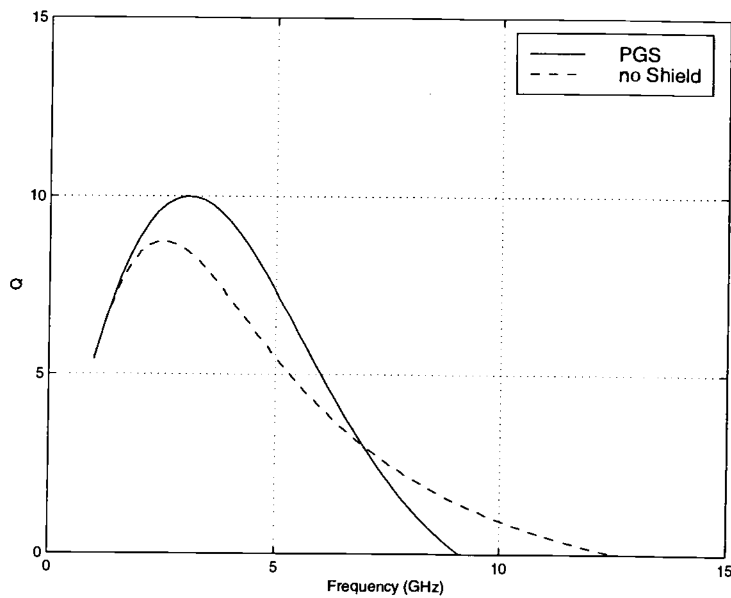


FIGURE 5.12. Example 4-turn spiral inductor with PGS used to test various shielding cases.



(a)



(b)

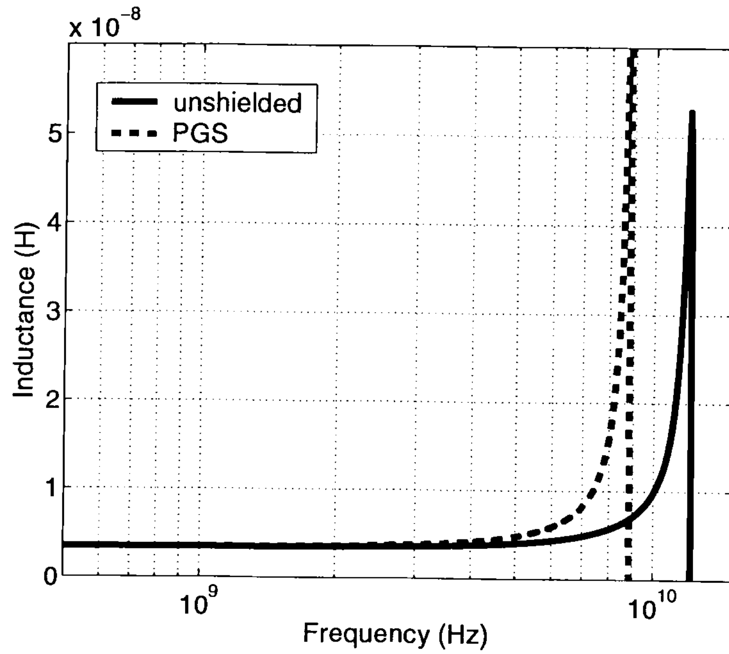
FIGURE 5.13. (a) Inductance and (b) Q for a 4-turn spiral with and without patterned ground shield (PGS).

Figures 5.14, 5.15 and 5.16 show the effect of varying substrate resistivity on the patterned ground shield effectiveness in improving Q for a perfectly conducting shield. As can be observed from these plots, when the resistivity is on the order of 0.01 Ω−cm ($\sigma \approx 10,000$ S/m), the patterned ground shield yields no benefit. This result is intuitive since the dominant substrate loss mechanism for spiral inductors in the RF-microwave frequency range with a very low substrate resistivity (i.e. ≈ 0.01 Ω-cm) is a result of longitudinal or so-called 'eddy' currents in the semiconducting bulk, rather than shunt conduction current. The patterned ground shields only alleviate shunt losses.

Because any patterned ground shield will ultimately be fabricated using some sort of finite conductivity material, it is appropriate to study the effects of such finite conductivity on performance. Figures 5.17 and 5.18 show the inductance and Q for the same example spiral inductor with patterned ground shields of varying sheet resistivity. The case of no shielding is also included as a reference. As observed from the Q plots, a sheet resistivity of 8 Ω/square or higher yields no significant benefit versus a spiral inductor with no shielding. The case of 0.1 Ω/square resistivity is representative of lower metallization layers in a silicon process, whereas 8Ω/square is a typical sheet resistivity for polysilicon layers. Thus, it is important to consider the available material resistivities for a process when deciding to invest the time and effort into developing shielding structures for spiral inductors for which Q's are critical.

5.4.2. Alternative Patterned Ground Shield Configurations

Another configuration for the patterned ground shield is a so-called star pattern, as shown in Figure 5.19. The round shape of such a pattern lends itself



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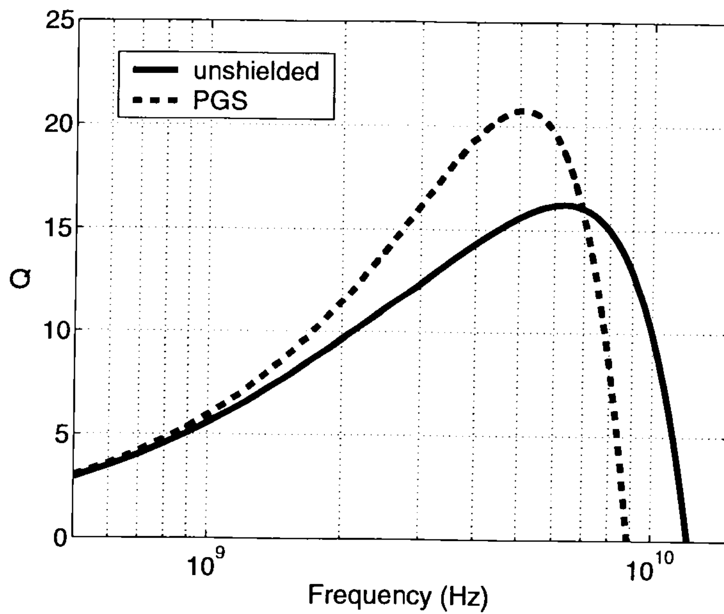
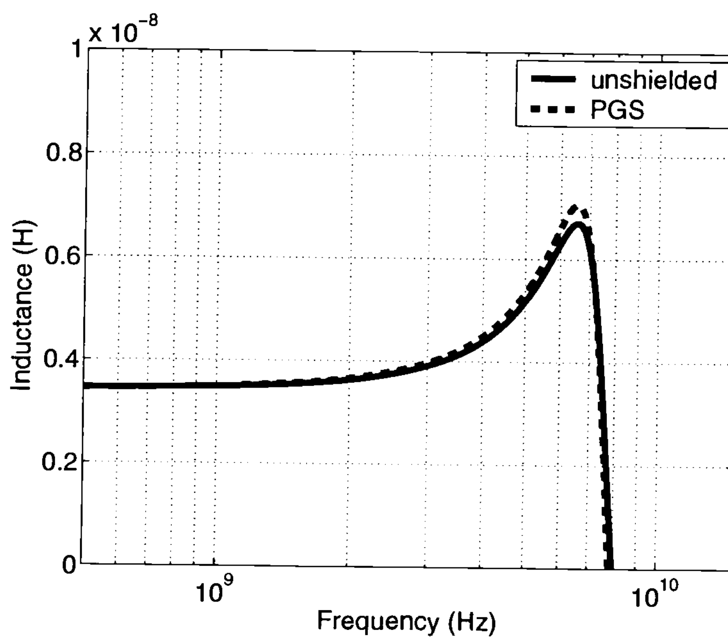


(b)

FIGURE 5.14. (a) Inductance and (b) quality factor for 4-turn spiral inductor with and without PGS, $\rho_{sub} = 1000\ \Omega$-cm.



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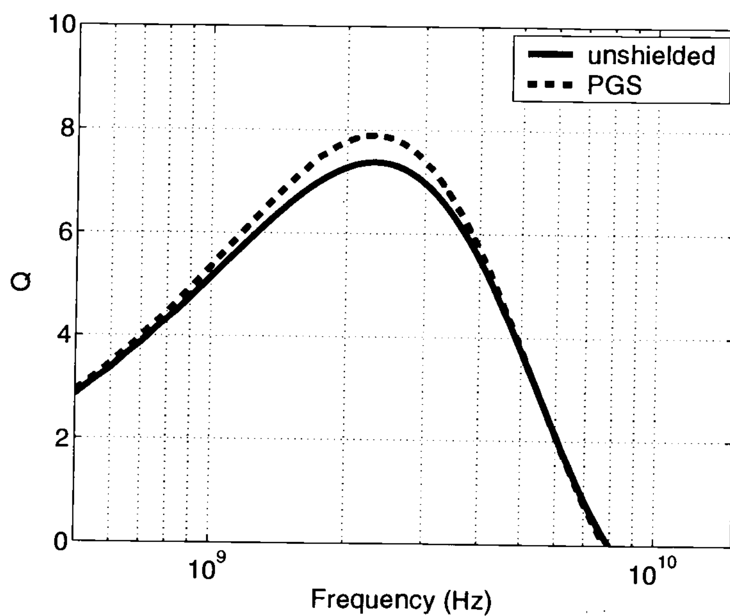
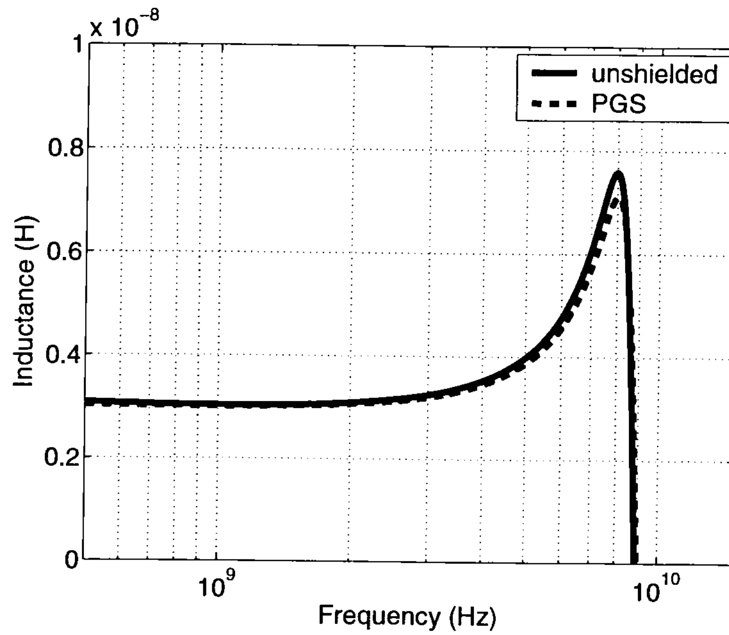
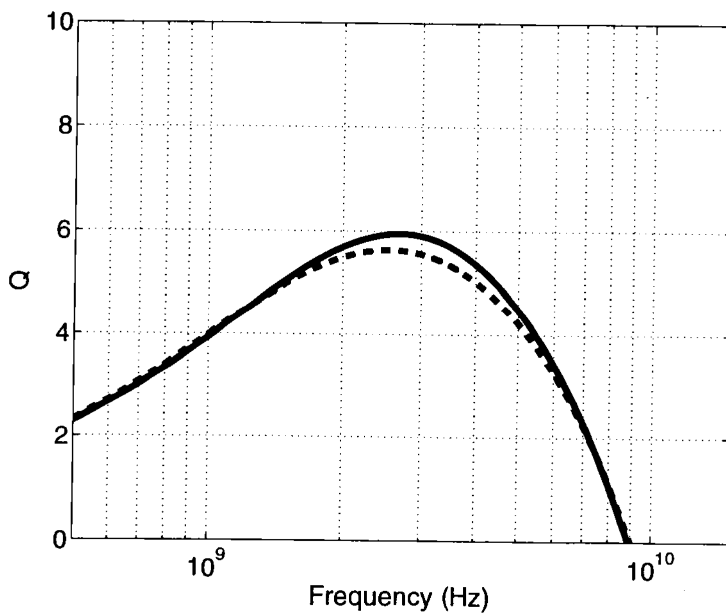


(b)

FIGURE 5.15. (a) Inductance and (b) quality factor for 4-turn spiral inductor with and without PGS, $\rho_{sub} = 1\ \Omega$-cm.

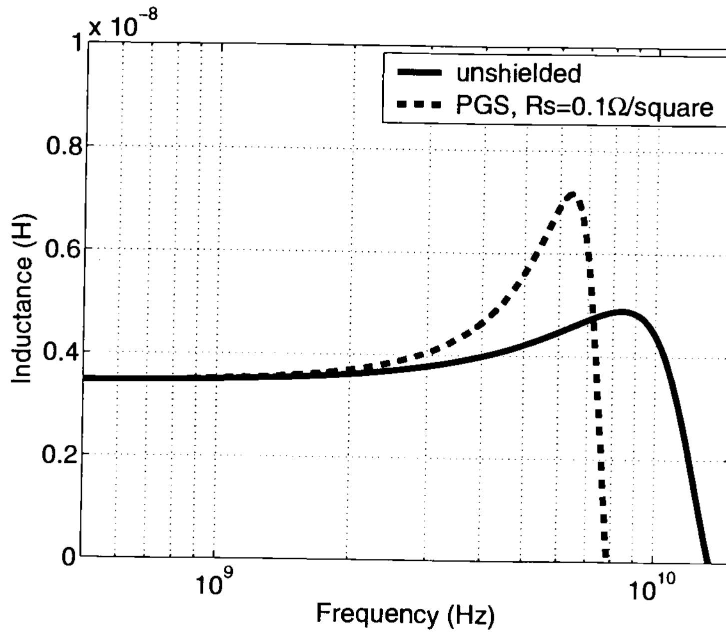


(a)



(b)

FIGURE 5.16. (a) Inductance and (b) quality factor for 4-turn spiral inductor with and without PGS, $\rho_{sub} = 0.01\ \Omega$-cm.



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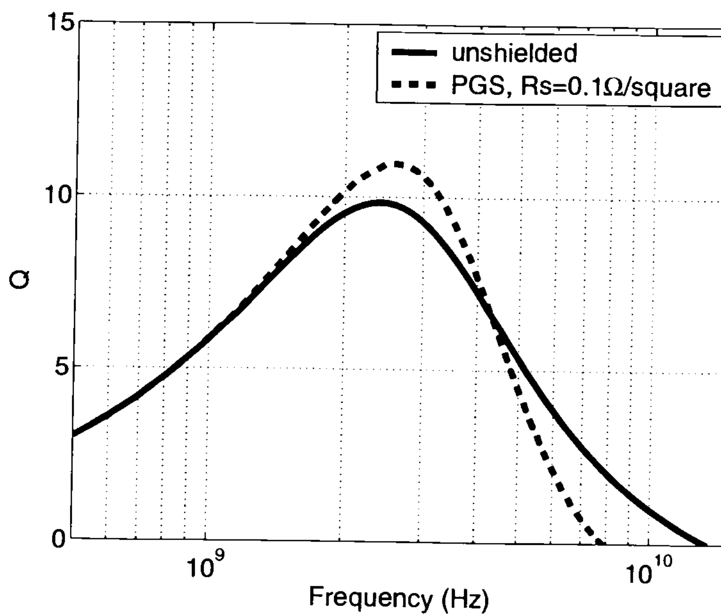

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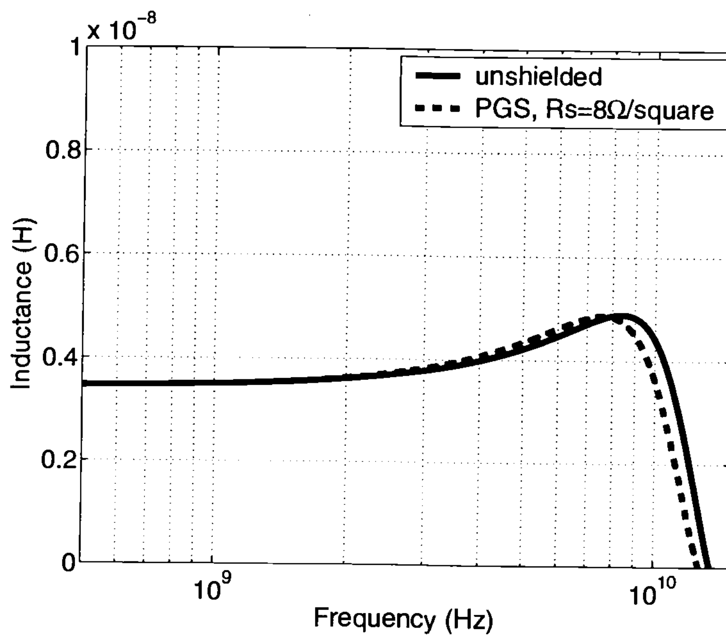
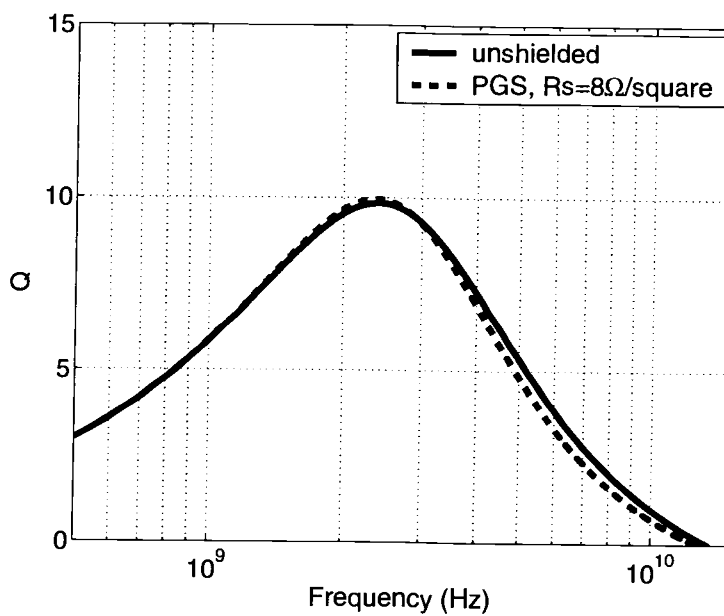
FIGURE 5.17. (a) Inductance and (b) quality factor for 4-turn spiral inductor with and without PGS, $R_s = 0.1\ \Omega$/square.



(a)



(b)

FIGURE 5.18. (a) Inductance and (b) quality factor for 4-turn spiral inductor with and without PGS, $R_s = 8\ \Omega$/square.

to use with circular spiral inductors. Another change relative to the patterned ground shields used in the previous section is the use of a central tap point for the 'fingers', rather than using a circular ring with a gap to connect the 'fingers' together. Figure 5.20 shows the inductance and Q for two different levels of shielding versus a standard unshielded spiral. In this case, the shield is actually located on the lowest metal level and is thus isolated electrically from the silicon substrate.

5.4.3. Modeling the Patterned Ground Shield for Spiral Inductors

The distributed equivalent circuit for single level spiral inductors presented in Chapter 3 may be modified to include the effect of patterned ground shields. As observed for interconnects with an orthogonal gridded shield, the effective semiconducting substrate shunt conductance $G_{\mathrm{Si,eff}}$ is dependent on the relative amount of shielding. A spiral inductor may alternatively be viewed as a collection of coupled interconnects, and thus the behavior of an inductor's shunt conductance when a patterned ground shield is present should be very similar to that observed for shielded interconnects. To investigate this hypothesis, the distributed model from Chapter 3 was modified to emulate the effect of a patterned ground shield on its net substrate shunt conductance. The 4-turn square spiral inductor studied in the previous section is again used as a test vehicle. Since its linewidth is 10 μm and the substrate profile is identical to that used for the interconnect investigation in the previous section, the values in Table 5.1 provide a guide for how to modify the effective vertical substrate conductance for various levels of shielding coverage. Figure 5.21 shows the effective substrate conductivity as a function of shielding coverage normalized to the unshielded value. For the 4-turn square spiral example,

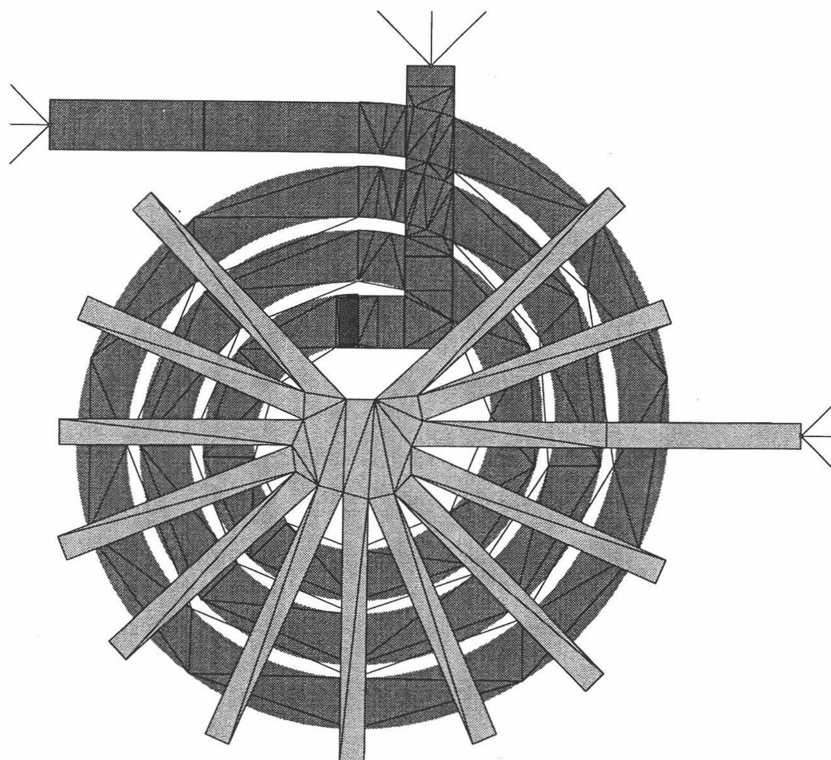
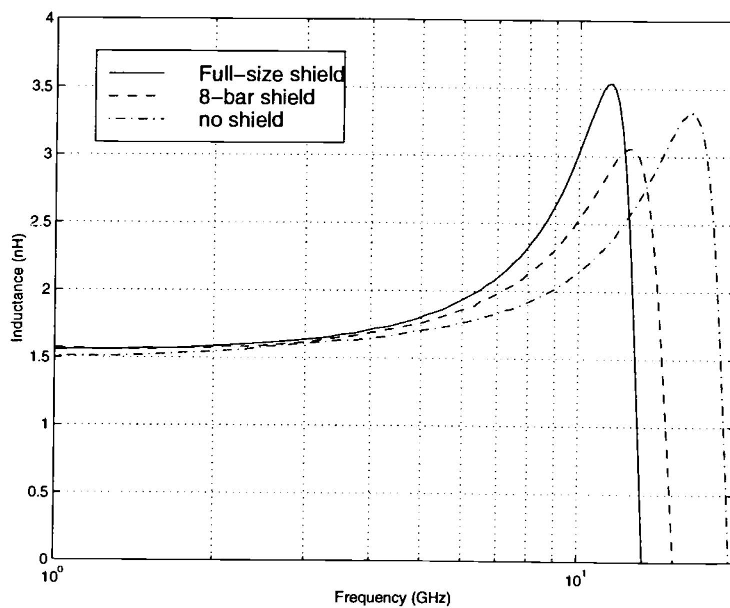
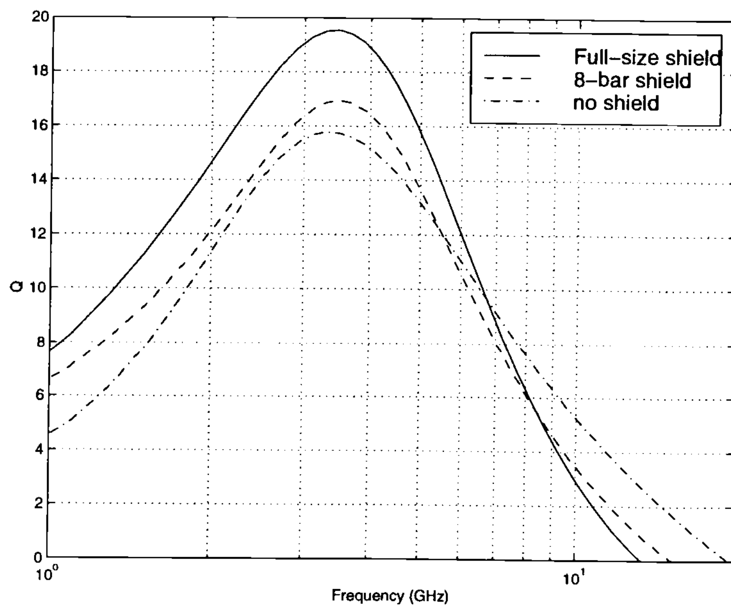


FIGURE 5.19. Example round spiral inductor with star pattern ground shield.



(a)



(b)

FIGURE 5.20. (a) Inductance and (b) Q for a round spiral inductor versus shielding coverage.

the coverage is approximately 50%, and thus the shunt substrate conductance in the distributed model should be multiplied by 6.2 to account for the effect of the patterned ground shield on the vertical substrate loss component. This is easily accomplished since the distributed model's series and shunt terms are calculated separately.

Figure 5.22 shows the simulated inductance and quality factor for the 4-turn example spiral inductor using both Agilent Momentum and the distributed model from Chapter 3 with the shunt substrate conductances appropriately scaled. The net inductance predicted by Momentum is slightly higher than that predicted by the distributed model since Momentum is unable to accurately model the finite conductor thickness and hence uses infinitely thin conductors to represent the inductor. Otherwise, the performance prediction of the distributed model is quite good, with a maximum difference in Q with respect to Momentum on the order of one point for both shielded and unshielded cases.

5.5. Conclusions

It has been demonstrated that an orthogonal grid of grounded lines placed near the oxide/bulk interface can significantly enhance the transmission characteristics of on-chip interconnects on lossy silicon substrates with resistivities on the order of 10 Ω-cm. The characteristics of the interconnect with the periodic shielding structure were extracted from full-wave simulation results for a unit cell. The presence of the orthogonal gridded shield was shown to substantially decrease the frequency dependence of the shunt capacitance while leaving the series inductance nearly unchanged even for a relatively large fractional shielding coverage. The effect of the shielding structure can directly be included in the equivalent cir-

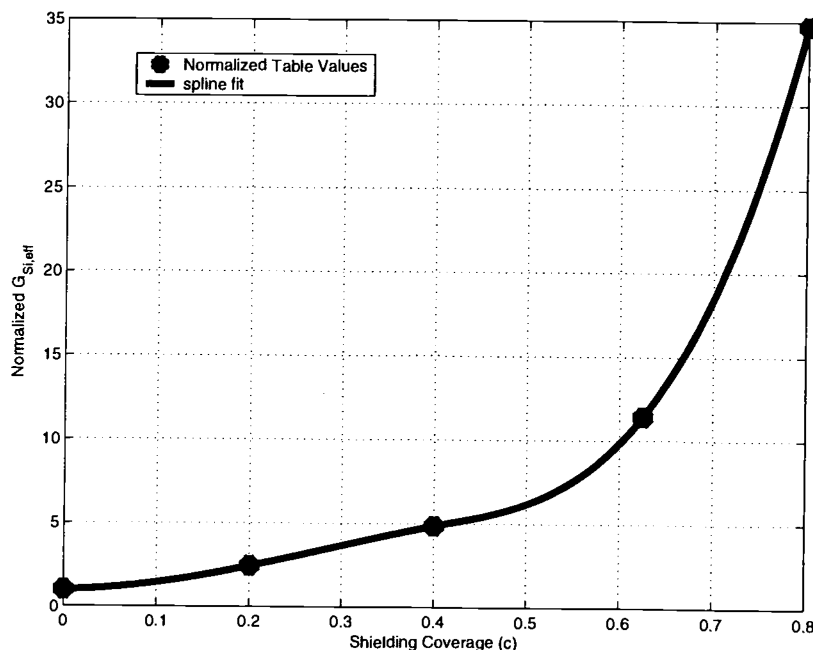
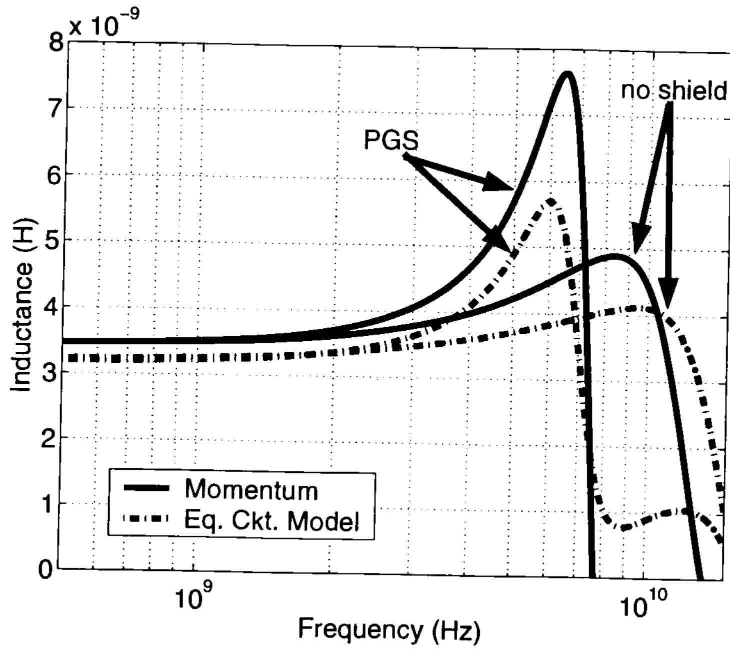


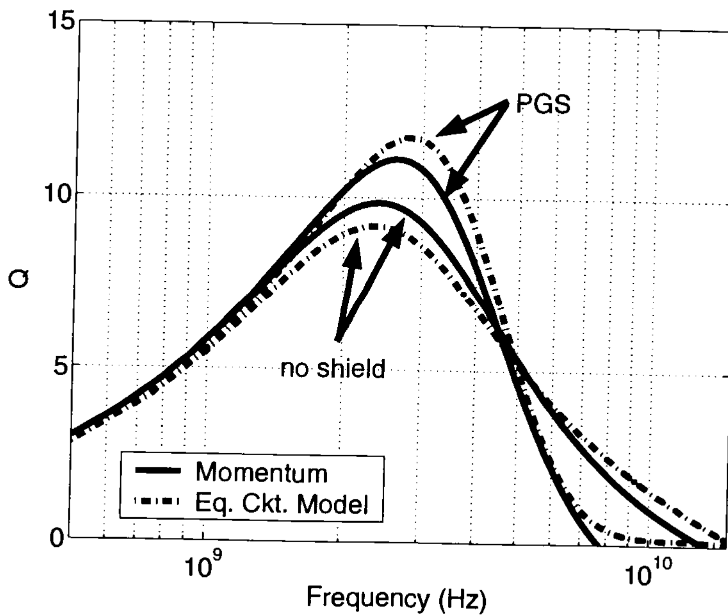
FIGURE 5.21. Normalized Effective Substrate Shunt Conductance for w = 10 μm.

cuit model of the unshielded interconnect in terms of increased effective substrate capacitance and conductance values in the C-G-C shunt admittance topology. On-chip interconnects with orthogonal gridded shielding to reduce the effects of substrate loss should be advantageous for high performance high-speed analog and mixed-signal integrated circuits in silicon technology.

The effects of Patterned Ground Shields on inductor performance were also studied as a natural extension of the work on interconnects over orthogonal gridded shields. Various configurations and process variations were considered and simulation results were presented showing the potential performance enhancements achievable by using ground shields. It was also shown that the effective substrate capacitance and conductance extracted for single lines can also be easily incorpo-



(a)



(b)

FIGURE 5.22. (a) Inductance and (b) quality factor for 4-turn spiral inductor with and without PGS.

rated into the distributed spiral model to provide accurate modeling of shielded spirals. The use of orthogonal shielding structures for spiral inductors can clearly provide a performance advantage in terms of Q for moderate resistivity substrates and low-resistance shields.

6. CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

In the preceding chapters, a modeling methodology was presented for on-chip spiral inductors and applied to various geometries and process parameters, as well as to the use of patterned orthogonal ground shields. This modeling approach was shown to be quite accurate for predicting performance of spiral inductors.

The ability to accurately prototype spiral inductors is of critical importance to the RFIC industry at large. Both design time and time-to-market are critical factors in any semiconductor industry sector, but these are particularly important in areas of high competition and volume such as the telecommunications sector, which includes wireless handsets, Wireless Local Area Network (WLAN) chipsets, as well as fiber optic networking equipment, where first-pass design success is critical. Often, RFIC designs go through many revisions before being put into production for sale to customers. Obviously, if every model being used by a circuit designer was 100% accurate, there would never be a need for additional design turns since the circuit would perform exactly as intended right from the start. Unfortunately, as we all know, in reality the available models for RFIC components, or any electrical component for that matter, are not 100% accurate. However, an improvement in the modeling of relatively large-scale components such as spiral inductors can substantially impact the overall design flow for an RFIC. Often the performance of on-chip inductors at a particular frequency and within a pre-specified chip area need to be known early in the design phase in order to assess the feasibility of the project, since the per-die cost is directly proportional to the chip area.

Because of the relatively large areas occupied by spiral inductors fabricated on-chip, their effects on other adjacent circuitry can be a design concern depend-

ing upon the application. Recall that the magnetic field intensity for a typical inductor does not diminish rapidly with increasing distance, and thus there can be significant magnetic field coupling even across large separations (e.g. 1 mm). There is a need for inductor-to-inductor and inductor-to-device coupling modeling for RFICs in silicon, and this is clearly an area where powerful simulators such as Ansoft's High Frequency Structure Simulator (HFSS) can provide solutions. However, simplified methods of estimating coupling are a potential topic for future work since the circuit designer may not have time or resources to engage a full-wave simulator every time a coupling simulation is needed.

The most commonly simulated environment for spiral inductors and other on-chip passive components is the case of a spiral on top of a dielectric/semiconductor substrate with a ground plane beneath. This situation arises in many common packaging technologies where a so-called 'paddle' is used as a conductive backplane to which the IC die is attached. However, with the advent of new packaging technologies such as Ball Grid Arrays and Flip-Chip, an RFIC die may not necessarily be attached to any sort of conducting plane. In these cases, the ground connections for the chip are brought onto the die through individual solder balls but are not referenced to a ground plane. Thus, the passive components that occupy relatively large areas on the silicon die must be accurately modeled in these new package environments since their respective electromagnetic fields may potentially have a broader influence on performance in the absence of a ground plane that normally provides a degree of shielding. Also, there may be multiple conducting planes that are located off-chip in either a Printed Circuit Board (PCB) or Land Grid Array (LGA) that can have influence on an inductor's performance. Currently, these types of problems are most effectively handled by memory and CPU intensive full-wave simulators like HFSS. If simplifications can

be made, such as assuming only the closest conducting planes in an adjacent PCB are significant for purposes of modeling, then the methods presented in this thesis may be applicable.

In addition to coupling across a die, the topic of proximity effects of the spiraling currents within inductors is also important for further improving the accuracy of the modeling techniques developed here. This concept was illustrated in Chapter 2 and is a topic of interest to the RFIC modeling and design community.

There is a great deal of interest in both academic and industrial communities in the topic of modeling, analysis and design of spiral inductors on silicon. This interest is fueled primarily by a highly competitive marketplace for low-cost, high-performance consumer and commercial telecommunications products that in turn creates a demand for analog integrated circuits that operate at high performance levels in the microwave frequency range and can be fabricated using relatively inexpensive silicon processes. As the sizes of RFIC chips continue to decrease, the importance of accurate modeling of on-chip spiral inductors will be even more pronounced, owing to the need to optimize spiral designs within tighter 'real-estate' constraints. Although on-chip spiral inductors are certainly not the only items requiring accurate modeling in an RFIC design, their complicated frequency-dependent behavior and relatively large-scale electromagnetic aspects warrant a concerted and dedicated modeling effort, as presented in this thesis.

BIBLIOGRAPHY

[1] Motorola (http://www.motorola.com), Schaumburg, Illinois.

[2] S. Ramo, J. Whinnery, T. Van Duzer, *Fields and Waves in Communication Electronics*. New York: John Wiley, 3rd ed., 1994, pp. 258-259.

[3] G. Stojanovic and L. Zivanov, "Comparison of optimal design of different spiral inductors," *24th International Conference on Microelectronics*, Vol. 2 , pp. 613-616, May 2004.

[4] Z. Zhang, Z. Wen, S. Xu, Z. Zhang, G. Chen, and S. Huang, "Optimization of Q factor in spiral inductor on silicon," *Proc. Int. Conf. Solid-State and Integrated-Circuit Technology*, Vol. 1, pp. 251-254, Oct. 2001.

[5] N. A. Talwalkar, C. P. Yue, and S. S. Wong, "Analysis and Synthesis of On-Chip Spiral Inductors," *IEEE Trans. Electron Devices*, Vol. 52 , pp. 176-182, Feb. 2005.

[6] X. L. Wang, X. L. Zhao, Y. Zhou, X. H. Dai, and B. C. Cai, "Fabrication and performance of a novel suspended RF spiral inductor," *IEEE Trans. Electron Devices*, Vol. 51, pp. 814-816, May 2004.

[7] C. A. Chang, S. P. Tseng, J. Y. Chuang, S. S. Jiang, and J. A. Yeh, "Characterization of spiral inductors with patterned floating structures," *IEEE Trans. Microwave Theory Tech.*, Vol. 52, pp. 1375-1381, May 2004.

[8] T. S. Chen, J. D. Deng, C. Y. Lee, and C. H. Kao, "Improved performance of Si-based spiral inductors," *IEEE Microwave and Wireless Comp. Lett.*, Vol. 14, pp. 466-468, Oct. 2004.

[9] J. N. Burghartz, M. Soyuer, and K. A. Jenkins, "Microwave Inductors and Capacitors in Standard Multilevel Interconnect Silicon Technology," *IEEE Trans. Microwave Theory Tech.*, Vol. MTT-44, pp. 100-104, Jan. 1996.

[10] J. N. Burghartz, K. A. Jenkins and M. Soyuer, "Multilevel-Spiral Inductors Using VLSI Interconnect Technology," *IEEE Electron Device Letters*, Vol. 17, pp. 428-430, Sept. 1996.

[11] W.Y. Yin, S. J. Pan, and L. W. Li, "Double-Level Spiral Inductors With Multiple-Via Interconnects on GaAs Substrates," *IEEE Trans. Magnetics*, Vol. 40, No. 3, pp. 1756-1758, May 2004.

[12] J. Lin, L. Zu, R. C. Frye, K. L. Tai, M. Y. Lau, D. Kossives, F. Hrycenko, and Y. K. Chen, "Accurate design of inductors on multi-chip module using

high-resistivity silicon substrate," *Proc. IEEE 1996 Mtg. EPEP*, pp. 187-189, October 1996.

[13] J. Y.-C. Chang, A. Abidi, and M. Gaitan, "Large suspended inductors on silicon and their use in a 2-μm CMOS RF amplifier," *IEEE Electron Device Letters*, vol. 14, No. 5, pp. 246-248, May 1993.

[14] M. W. Geen, G. J. Green, R. G. Arnold, J. A. Jenkins and R. H. Jansen, "Miniature Multilayer Spiral Inductors for GaAsMMICs," *Proc. 1989 IEEE GaAs IC Sym.*, pp. 303-306, 1989.

[15] J. R. Long and M. A. Copeland, "The modeling, characterization, and design of monolithic inductors for silicon RF IC's," *IEEE J. Solid State Circuits*, vol. 32, No. 3, pp. 357-369, Mar. 1997.

[16] R. D. Lutz, Y. Hahm, A. Weisshaar, V. K. Tripathi, A. Grzegorek, W. McFarland and J. Meyer, "Modeling of Spiral Inductors on Lossy Substrates for RFIC Applications," *IEEE 1998 MTT-S Sym. Digest*, Baltimore, MD, pp. 1855-1858, June 1998.

[17] A. M. Niknejad, R. G. Meyer, "Analysis of Eddy-Current Losses Over Conductive Substrates with Applications to Monolithic Inductors and Transformers," *IEEE Trans. Microwave Theory and Tech.* Vol. 49, pp. 166-176, Jan. 2001.

[18] D. Melendy and A. Weisshaar, "A New Scalable Model for Spiral Inductors on Lossy Silicon Substrate," *IEEE 2003 MTT-S Sym. Digest*, Philadelphia, PA, pp. 1007-1010, June 2003.

[19] A. E. Ruehli, "Equivalent Circuit Models for Three-Dimensional Multiconductor Systems" *IEEE Trans. Microwave Theory Tech.*, Vol. MTT-22, pp. 216-221, Mar. 1974.

[20] E. Pettenpaul, H.Kapusta, A.Weisgerber, H.Mampe, J.Luginsland, and I.Wolff, "CAD Models of Lumped Elements on GaAs up to 18 GHz," *IEEE Trans. Microwave Theory Tech.*, pp. 294-304, Vol. 36, Feb. 1988.

[21] H.M. Greenhouse, "Design of Planar Rectangular Microelectronic Inductors," *IEEE Trans. Parts, Hybrids, and Packaging*, Vol. PHP-10, pp. 101-109, June 1974.

[22] A.C. Watson, D. Melendy, P. Francis, Hwang Kyuwoon, and A. Weisshaar, "A comprehensive compact-modeling methodology for spiral inductors in silicon-based RFICs," *IEEE Trans. Microwave Theory Tech.*, Vol. 52, pp. 849-857, March 2004.

[23] H. Hasegawa, M. Furukawa, and H. Yanai, "Properties of Microstrip Line on Si-SiO_2 System," *IEEE Trans. Microwave Theory Tech.*, Vol. MTT19, pp. 869-881, Nov. 1971.

[24] R. T. Kollipara and V. K. Tripathi, "Spectral Domain Analysis of Multiconductor Structures with Rectangular and Trapezoidal Cross Sections," *Microwave and Optics Letters*, John Wiley, Jan. 1990.

[25] A. Tripathi, Y. Hahm, A. Weisshaar and V. K. Tripathi, "Quasi-TEM spectral domain approach for calculating distributed inductance and resistance of microstrip on Si-SiO2 substrate," *IEE Electronics Letters*, pp. 1330-1331, Vol. 34, No. 13, June 1998.

[26] E. Grotelüschen, L. S. Dutta, and S. Zaage, "Full-wave analysis and analytical formulas for the line parameters of transmission line on semiconductor substrates," *INTEGRATION, VLSI J.*, vol. 16, pp. 33-58, 1993.

[27] V.K. Tripathi and N. Orhanovic, "Time-Domain Characterization and Analysis of Dispersive Dissipative Interconnects," *IEEE Trans. Circuits and Systems*, Vol. 39, pp. 938-945, November 1992.

[28] H. A. Wheeler, "Formulas for the skin effect," *Proc. IRE*, vol. 30, pp. 412-424, Sept. 1942.

[29] A. Weisshaar, H. Lan, and A. Luoh, "Accurate Closed-Form Expressions for the Frequency-Dependent Line Parameters of On-Chip Interconnects on Lossy Silicon Substrate," *IEEE Trans. Advanced Packaging*, Vol. 25, pp. 288-296, May 2002.

[30] A. Weisshaar and A. Luoh, "Closed-form expressions for the series impedance parameters of on-chip interconnects on multilayer silicon substrates," *IEEE Trans. Advanced Packaging*,Vol. 27 ,pp. 126-134, Feb. 2004.

[31] D. Melendy, "Modelling of On-Chip Spiral Inductors for Silicon RFICs," *M. S. Thesis*, Oregon State University, November 2003.

[32] R. D. Lutz, "Analysis and Modeling of Planar Microstrip Spiral Inductors on Lossy Substrates," *M. S. Thesis*, Oregon State University, June 1998.

[33] C. Hoer, C. Love, "Exact Inductance Equations for Rectangular Conductors with Applications to More Complicated Geometries," *J. of Research, Natl. Bureau Standards*, Vol. 69C, No. 2, pp. 127-137, Apr.-Jun. 1965.

[34] D. Pozar, *Microwave Engineering*. New York: Addison-Wesley, 2nd. ed., 1993, pp. 185-186.'

[35] The MathWorks, Inc., Natick, Massachusetts.

[36] R. D. Lutz, Y. Hahm, A. Weisshaar, V. K. Tripathi, H. Wu and N. Kanagleka, "Modeling and Analysis of Multilevel Spiral Inductors for RFICs," *IEEE 1999 MTT-S Sym. Digest*, Anaheim, CA, pp. 43-46, June 1999.

[37] Agilent Technologies, Santa Rosa, California (USA).

[38] A. Deutsch, G. V. Kopcsay, P. J. Restle, H. H. Smith, G. Katopis, W. D. Becker, P. W. Coteus, C. W. Surovic, B. J. Rubin, R. P. Dunne, Jr., T. Gallo, K. A. Jenkins, L. M. Terman, R. H. Dennard, G. A. Sai-Halasz, B. L. Krauter, and D. R. Knebel, "When are transmission-line effects important for on-chip interconnections?" *IEEE Trans. Microwave Theory Tech.* , vol.45, No.10, pp.1836-1846, Oct. 1997

[39] J. N. Burghartz, "Progress in RF inductors on silicon — understanding substrate losses," *Proc. 1998 IEEE Int. Electron Devices Meeting*, San Francisco, CA, pp. 523-526, Dec. 1998 USA.

[40] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF IC's," *IEEE J. Solid-State Circuits,* vol.33, pp.743-752, May 1998.

[41] R. D. Lutz, V. K. Tripathi, A. Weisshaar, "Enhanced transmission characteristics of on-chip interconnects with orthogonal gridded shield," *IEEE Electrical Performance of Electronic Packaging, 2000*, Vol. 24, No. 3, pp. 288-293, August 2001.

[42] R. D. Lutz, V. K. Tripathi, A. Weisshaar, "Enhanced transmission characteristics of on-chip interconnects with orthogonal gridded shield," *IEEE Trans. Advanced Packaging, 2000*, 23-25 Oct. 2000, pp. 329-332.

[43] V. Milanovic, M. Ozgur, D. C. DeGroot, J. A. Jargon, M. Gaitan and M. E. Zaghloul, "Characterization of broad-band transmission for coplanar waveguides on CMOS silicon substrates," *IEEE Trans. Microwave Theory Tech.,* vol. 46, pp. 632-640, May 1998.

[44] R. Collin, *Foundations for Microwave Engineering*. New York: McGraw-Hill, 1st ed., 1966.

[45] T. Wang and T. Itoh, "Confirmation of slow waves in a crosstie overlay coplanar waveguide and its application to band-reject gratings and reflectors," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1811-1818, 1988.

[46] M. Yu and A. Gopinath, "High-speed directional coupler modulator with velocity-matched electrode structure," *IEEE MTT-S Int. Microwave Symp. Digest*, Orlando, FL, pp. 255-258, June 1995.

[47] F. Masot, K. A. Remley, R. T. Kollipara, A. Weisshaar, and V. K. Tripathi, "Velocity Matching for Field-Induced Electrooptic Modulators," *IEEE MTT-S Int. Microwave Symp. Digest*, San Francisco, pp. 1441-1444, June 1996.

[48] J. Zheng, A. Tripathi, Y.-C.Hahm, T. Ishii, A. Weisshaar, and V. K. Tripathi, "CAD-oriented equivalent circuit modeling of on-chip interconnects in CMOS technology," *Proc. IEEE 7th Topical Meeting on Electrical Performance of Electronic Packaging(EPEP'98)*, pp.227-230, West Point, NY, Oct.26-28, 1998.

[49] J. Zheng, Y.-C. Hahm, A. Weisshaar, and V. K. Tripathi, "CAD-Oriented Equivalent Circuit Modeling of On-Chip Interconnects for RF Integrated Circuits in CMOS Technology," *IEEE MTT-S Int. Microwave Symp. Digest*, Anaheim, CA, pp. 35-38, June 1999.

[50] J. Zheng, Y. C. Hahm, V. K. Tripathi, and A. Weisshaar, "CAD-oriented equivalent circuit modeling of on-chip interconnects on lossy silicon substrate," *IEEE Trans. Microwave Theory Tech.*, , vol. 48, no. 9, pp. 1443-1451, Sept. 2000.

[51] A. E. Ruehli, "Efficient Capacitance Calculations for Three-dimensional Multiconductor Systems," *IEEE Trans. Microwave Theory Tech.*, Vol. MTT-21, pp. 76-82, Feb. 1973.

[52] A. E. Ruehli and E. Chiprout, "The Importance of Retardation in PEEC Models for Electrical Interconnect and Package (EIP) Applications," *Proc. IEEE EPEP*, pp. 232-234, Oct. 1995.

[53] V. K. Tripathi and R. T. Kollipara, "Quasi TEM Spectral Domain Analysis of Thick Microstrips for Microwave and Digital Integrated Circuits," *Electronics Letters*, pp. 1138-1139, Aug. 1989.

[54] R. T. Kollipara and V. K. Tripathi, "An Efficient Spectral Domain Method for the Dispersion Characteristics of Moderately Thick Microstrip Lines," *IEEE Microwave and Guided Wave Letters*, pp. 100-101, Mar. 1992.

[55] J. P. K. Gilb and C. A. Balanis, "MIS Slow-Wave Structures Over a Wide Range of Parameters," *IEEE Trans. Microwave Theory Tech.*, Vol. 40, No. 12, pp. 2148-2154, Dec. 1992.

[56] V.K. Tripathi, C. Holmes, M. Cochrane, and B. Allen, "A distributed CAD model for microstrip spiral inductors," *European Microwave Conference Digest*, pp. 723-724, September 1993.

[57] Y. Seo and V.K. Tripathi, "Spiral Inductors in RFIC's and MMIC's," *1995 Asia Pacific Microwave Conference Proc.*, Taejon, Korea, pp. 454-457, October 1995.

[58] A. Hill and V.K. Tripathi, "Analysis and Modelling of Coupled Microstrip Bend Discontinuities," *IEEE Int. Microwave Sym.*, pp. 1143-1146, June 1989.

[59] A. Hill and V.K. Tripathi, "An Efficient Algorithm for the 3D Analysis of Passive Microstrip Components and Discontinuties for Microwave and Millimeter Wave Circuits, " *IEEE Trans. Microwave Theory and Tech.* , Vol. 41, pp. 83-91, Jan. 1991.

[60] R. L. Remke and G. A. Burdick, "Spiral Inductors for Hybrid and Microwave Applications," *Proc. 24th Electron Components Conf.*, Washington, D.C., pp. 152-161, May 1974.

[61] J. Müller, H. Thust, and K. H. Drue, "RF-Design Considerations for Passive Elements in LTCC Material Systems," *Intl. Journal Microcircuits and Electronic Packaging*, Vol. 18, pp. 200-206, 1995.

[62] K. B. Ashby, WC Finley, JJ Bastek, S. Moinian, "High Q Inductors for Wireless Applications in a Complementary Silicon Process," *1994 Bipolar/BiCMOS Circuits Tech. Mtg.* pp. 179-182, 1994.

[63] R. D. Lutz, Y. Seo, E. Godshalk, V. K. Tripathi, "Spiral Inductor Design Issues in a Multilayered Medium," *Proc. ISHM Intl. Microelectronics Sym.*, Oct. 1996.

[64] D. Krafesik, D. Dawson, "A Closed-form Expression for Representing the Distributed Nature of the Spiral Inductor," *1986 IEEE MTT Monolithic Circuits Sym. Digest*, pp. 87-91.

[65] E. Frlan, S. Meszaros, M. Cuhai, JS Wight, "Computer Aided Design of Square Spiral Transformers and Inductors, *1989 IEEE Int. Microwave Sym.*, pp. 661-664.

[66] D. Lovelace, N. Camilleri, G. Kannell, "Silicon MMIC Inductor Modeling for High Volume Low Cost Applications," *Microwave Journal*, pp. 60-71, Aug. 1994.

APPENDICES

APPENDIX A. Theory of Partial Inductance

This Appendix provides a detailed analysis of the theory of partial inductance, as presented in [19] and [33] . For an arbitrary conductor of constant cross-section, a_j, around a loop, the magnetic vector potential at a point r_i generated by a current I_j in a loop j may be calculated as

$$\mathbf{A}_{ij} = \frac{\mu}{4\pi} \cdot \frac{I_j}{a_j} \oint_j \int_{a_j} \frac{d\mathbf{l}_j da_j}{r_{ij}} \tag{A1}$$

where $r_{ij} = |\mathbf{r}_i - \mathbf{r}_j|$ and $d\mathbf{l}_j$ is taken along the length of the conductor perpendicular to the cross-section. The assumption made here is that the current density perpendicular to the cross section is uniform. The flux linked by loop i can be calculated from the above expression as

$$\psi_{ij} = \oint_i \int_{a_i} \mathbf{A}_{ij} \cdot d\mathbf{l}_i da_i \tag{A2}$$

where a_i is the constant cross section of conductor loop i. To calculate the mutual inductance

$$L_{ij} = \frac{\psi_{ij}}{I_j} \tag{A3}$$

between loops i and j using (A1) and (A2), the expressions for vector potential and flux linkage are inserted with the result being

$$L_{ij} = \frac{1}{a_i a_j} \cdot \frac{\mu}{4\pi} \oint_i \int_{a_i} \oint_j \int_{a_j} \frac{d\mathbf{l}_i \cdot d\mathbf{l}_j}{r_{ij}} da_i da_j. \tag{A4}$$

This result is similar to the Neumann formula for mutual inductance between two arbitrary filaments of current

$$L_{fij} = \frac{\mu}{4\pi} \oint_i \oint_j \frac{d\mathbf{l}_i d\mathbf{l}_j}{r_{ij}} \tag{A5}$$

where the subscript f stands for filament. In fact (A4) and (A5) are identical when the cross-sectional areas $a_{i,j}$ are zero. It is apparent that averages are being taken

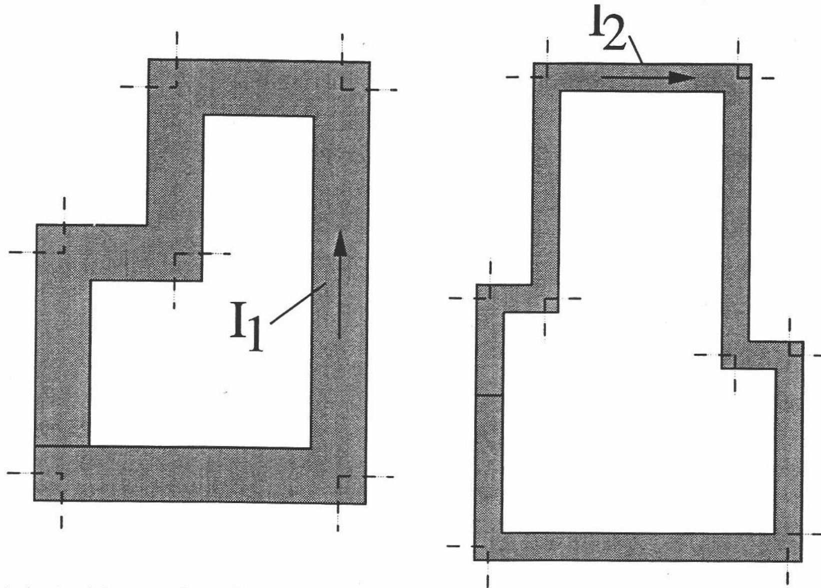


FIGURE A-1. Example of two conductor loops to be analyzed in terms of straight line sections.

in both (A1) and (A2), as both expressions are divided by the cross-sectional area of the conductor involved. Equation (A4) may be combined with (A5) to yield

$$L_{ij} = \frac{1}{a_i a_j} \int_{a_i} \int_{a_j} L_{fij} da_i da_j. \tag{A6}$$

If the conductors forming two loops are analyzed in terms of their respective straight line sections, as shown in Figure A-1, the total inductance may be written in terms of a double summation as

$$L_{km} = \sum_{k=1}^{K} \sum_{m=1}^{M} L_{p_{km}}. \tag{A7}$$

Here the term L_p is introduced to represent the partial mutual or self inductance of the respective conductor sections. The partial inductance for two straight conductors of constant cross sections is calculated using (A4) with the loop integrals replaced by line integrals,

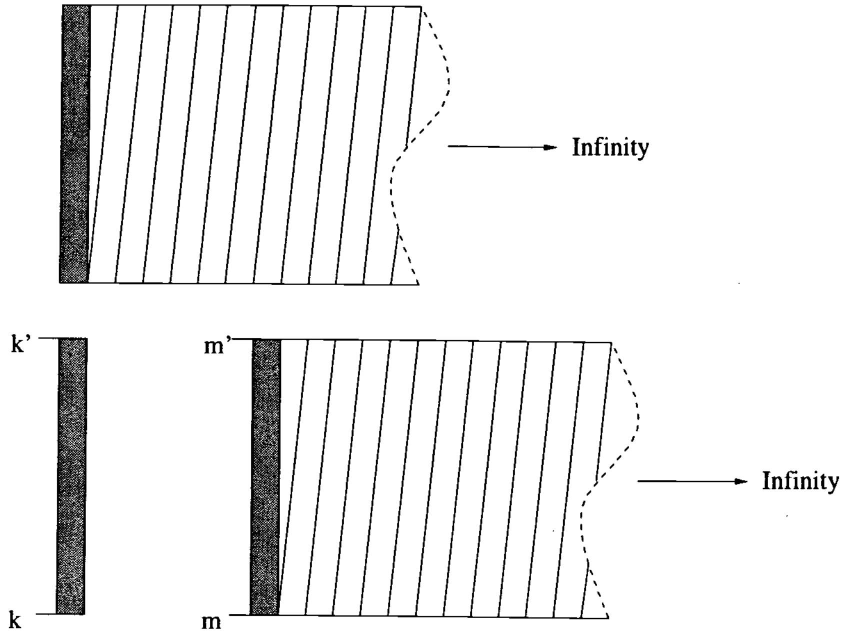


FIGURE A-2. Flux linkage areas associated with self and mutual inductance calculations.

$$L_{p_{km}} = \frac{1}{a_k a_m} \cdot \frac{\mu}{4\pi} \int_{a_k} \int_{a_m} \int_{k}^{k'} \int_{m}^{m'} \frac{d\mathbf{l}_k \cdot d\mathbf{l}_m}{r_{km}} da_k da_m. \tag{A8}$$

The direction of $d\mathbf{l}_{k,m}$ should be in accordance with the assumed current polarity in the loops, which will lead to both positive and negative mutual inductances. To verify this approach, the flux linkage associated with each term in (A7) should be considered. For a partial self inductance term ($k = m$), the region of flux linkage extends from the conductor out to infinity. Likewise, for two conductors k and m, the flux linkage area for partial mutual inductance computations extends from the outside edge of one of the conductors $m(k)$ out to infinity and is also bounded on the edges by lines perpendicular to conductor $k(m)$ and extending from the end points of conductor $m(k)$. These two flux linkage areas are illustrated in

Figure A-2. If a square loop is analyzed purely in terms of flux linkage, we may do the computation with a single surface integral

$$L_{sq} = \frac{1}{I} \int_S \mathbf{B} \cdot d\mathbf{S}. \tag{A9}$$

Likewise, if two parallel conductors of the square loop are analyzed in terms of the flux linkages associated with the self and mutual inductances, it can be deduced that the net area will be that of the square itself (S in (A9)). This is clear upon observation that the flux linkage areas associated with the self inductance terms extend from the conductor to infinity, whereas the area of linkage associated with the mutual terms extends from the conductor of opposing current polarity out to infinity. The difference between these two areas is in fact the area inside the square loop.

APPENDIX B. Expressions for Quasi-Static Magnetic Vector Potential and Their Application to Microstrip Structures

To develop the fundamental equations used in the quasi-static calculation of the magnetic vector potential for an MIS structure, the magnetic field curl expression is used as a starting point

$$\nabla \times \mathbf{H} = \mathbf{J} + \frac{\partial \mathbf{D}}{\partial t}. \tag{B1}$$

If the magnetic vector potential curl equation

$$\mu \mathbf{H} = \nabla \times \mathbf{A} \tag{B2}$$

is substituted for $\mathbf{H}$ in (B1), we obtain

$$\nabla \times \nabla \times \mathbf{A} = \mu \cdot \left[\mathbf{J} + \frac{\partial \mathbf{D}}{\partial t} \right], \tag{B3}$$

which may subsequently be rewritten as

$$\nabla (\nabla \cdot \mathbf{A}) - \nabla^2 \mathbf{A} = \mu \cdot \left[\mathbf{J} + \frac{\partial \mathbf{D}}{\partial t} \right]. \tag{B4}$$

If the divergence of $\mathbf{A}$ is chosen such that

$$\nabla \cdot \mathbf{A} = 0, \tag{B5}$$

which is known as the Coulomb gauge, and displacement current is neglected, then (B4) becomes

$$\nabla^2 \mathbf{A} = -\mu \mathbf{J}. \tag{B6}$$

$\mathbf{J}$ may be rewritten in terms of $\mathbf{E}$ as

$$\mathbf{J} = \sigma \mathbf{E}. \tag{B7}$$

Now, if we recall the curl equations for $\mathbf{E}$ and $\mathbf{A}$,

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{B8}$$

$$\nabla \times \mathbf{A} = \mathbf{B}, \tag{B9}$$

we can write

$$\nabla \times \mathbf{E} = -\frac{\partial}{\partial t} \nabla \times \mathbf{A} \tag{B10}$$

$$\mathbf{E} = -\frac{\partial}{\partial t} \mathbf{A} \tag{B11}$$

Assuming a sinusoidal steady-state solution is desired, we may express $\mathbf{J}$ as

$$\mathbf{J} = -j\omega\sigma \mathbf{A} \tag{B12}$$

which leads us to the final form for (B6) given in Chapter 2

$$\nabla^2 \mathbf{A} = j\omega\mu\sigma \mathbf{A}. \tag{B13}$$

The solutions for A_z for the different regions of a Si-SiO_2 based microstrip structure in the spatial domain (to be given below) are based on the expressions derived in [26] for coplanar structures with no ground plane. Here it is assumed that current only exists along the direction of propagation, the z-coordinate for this case, and thus $\mathbf{A}$ will only consist of a single component A_z. This allows for a solution of a two dimensional scalar potential problem, which simplifies the analysis.

For the non-conducting regions (i.e. air and oxide layers), the z-directed magnetic vector potential must satisfy

$$\nabla^2 A_z(x, y) = 0, \tag{B14}$$

while for conducting regions (i.e. bulk Si substrate)

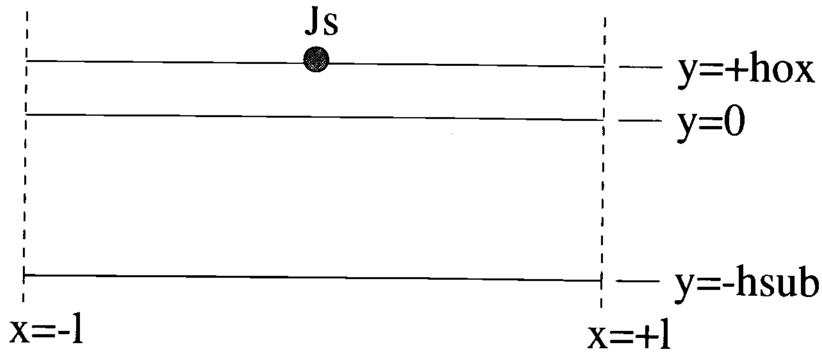


FIGURE B-1. Structure used for solution of magnetic potential.

$$\nabla^2 A_z(x,y) = j\omega\mu\sigma A_z(x,y). \tag{B15}$$

Assuming a line current at $x = 0$ and $y = h_{ox}$, the solutions for A_z in both conducting and nonconducting regions are found by applying appropriate boundary conditions

$$A_z(x, y = -h_{sub}) = 0 \tag{B16}$$

$$\frac{dA_z(x = \pm l, y)}{dx} = 0 \tag{B17}$$

where $\pm l$ are the locations of two symmetric magnetic walls, shown in Figure B-1, which are introduced to simplify the solutions in terms of Fourier series. The solutions in the two regions are

$$A_z(x, y \geq 0) = \frac{\mu_o I}{2\pi} \ln \sqrt{\frac{x^2 + (y + h_{ox})^2}{x^2 + (y - h_{ox})^2}} + \frac{\mu_o I}{l} \left[\frac{E_0}{2} + \sum_{k=1}^{\infty} E_k cos(m_k x) \right] \tag{B18}$$

$$A_z(x, y \leq 0) = \frac{\mu_o I}{l} \left[\sum_{k=1}^{\infty} 2m_k \sinh(q_k(y + h_{sub}))e^{-m_k h_{ox}} cos(m_k x) \right] \tag{B19}$$

where

$$E_k = \frac{q_k \cosh(2q_k h_{sub}) + m_k \sinh(2q_k h_{sub}) - 2q_k}{(q_k^2 + m_k^2)\sinh(2q_k h_{sub}) + 2q_k m_k \cosh(2q_k h_{sub})} \cdot e^{-2m_k h_{ox}} \tag{B20}$$

$$m_k = \frac{k\pi}{l} \tag{B21}$$

$$q_k = \sqrt{m_k^2 + j\omega\mu\sigma} \tag{B22}$$

The infinite summations in (B18) and (B19) are Fourier series representations of the continuous integrals involved when there are no magnetic walls present.

The solution for the magnetic vector potential may then be used to calculate the per-unit-length complex series inductance of a microstrip structure by first averaging A_z over the width of the strip, w_0, assuming a uniform current density in the strip itself, then averaging this result over the same strip to arrive at the solution

$$L_s = \frac{1}{Iw_0^2} \int_{-w_0/2}^{w_0/2} \int_{-w_0/2}^{w_0/2} A_z(x - x')dx'dx. \tag{B23}$$

The expression for the complex mutual inductance between two strips of widths w_0 and w_1 separated by an edge-to-edge distance s is given as

$$L_m = \frac{1}{Iw_1 w_0} \int_{-w_1/2-a}^{w_1/2-a} \int_{-w_0/2}^{w_0/2} A_z(x - x')dx'dx, \tag{B24}$$

where $a = w_0/2 + s + w_1/2$ (a is often referred to as line pitch when w_0 and w_1 are equal). Figure B-2 illustrates the structure under consideration here.

Recognizing that the second term of (B18) represents the contribution of the semiconducting substrate to the overall magnetic vector potential, the expressions for self inductance of a single strip may be written as

$$L_s = L_0 + \frac{\mu_0}{l}\left(\frac{E_0}{2} + \sum_{k=1}^{\infty} E_k \left[\text{sinc}\left(\frac{m_k w_0}{2}\right)\right]^2\right), \tag{B25}$$

where L_0 is the value for L_s when the semiconducting substrate is replaced by a perfectly conducting ground plane. The second term above may be reduced to an equivalent substrate resistance term at a given frequency, ω, as

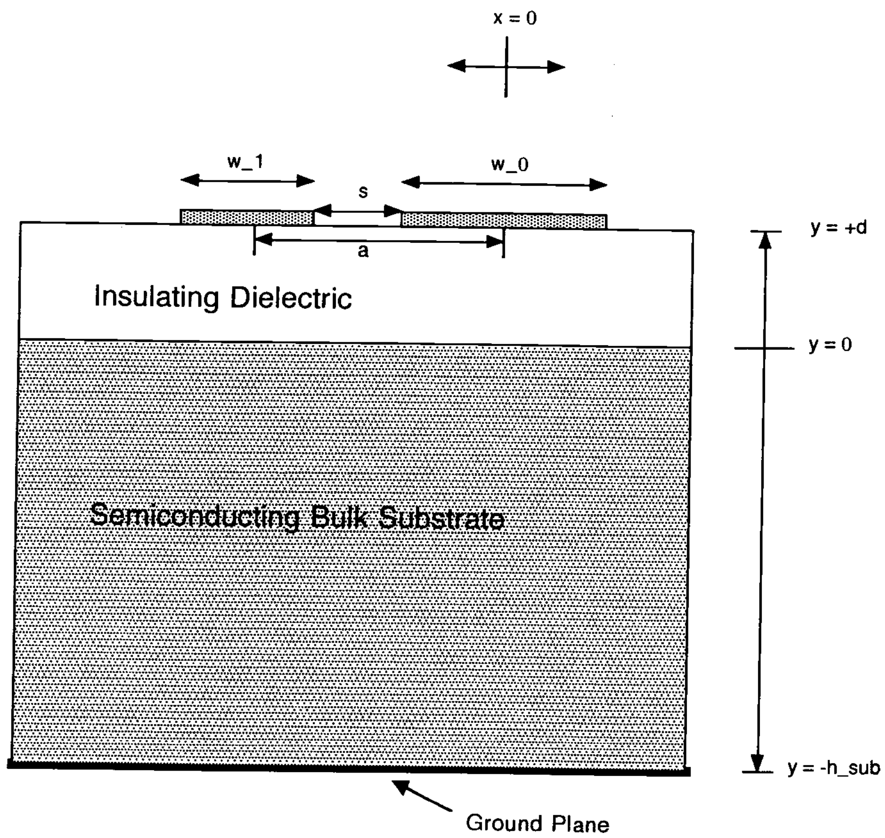


FIGURE B-2. Two-line microstrip structure used for self and mutual inductance calculations.

$$R_{\text{sub}}(\omega) = \Re\left\{ \frac{j\omega\mu_0}{l} \left(\frac{E_0}{2} + \sum_{k=1}^{\infty} E_k \left[\text{sinc}\left(\frac{m_k w_0}{2} \right) \right]^2 \right) \right\}. \tag{B26}$$

Similar expressions may be developed for complex mutual inductance between two strips at separation of $a = w_0/2 + s + w_1/2$,

$$L_m = M_0 + \frac{\mu_0}{l} \left(\frac{E_0}{2} + \sum_{k=1}^{\infty} E_k \text{sinc}\left(\frac{m_k w_0}{2} \right) \text{sinc}\left(\frac{m_k w_1}{2} \right) \cos(m_k a) \right), \tag{B27}$$

where M_0 represents the net mutual inductance when a perfect conducting ground plane is present in place of the semiconductor. The equivalent mutual resistance is given by

$$R_{\text{sub,m}}(\omega) = \Re\left\{ \frac{j\omega\mu_0}{l} \left(\frac{E_0}{2} + \sum_{k=1}^{\infty} E_k \text{sinc}\left(\frac{m_k w_0}{2} \right) \text{sinc}\left(\frac{m_k w_1}{2} \right) \cos(m_k a) \right) \right\}. \tag{B28}$$

A practical implementation of the spatial domain technique presented here was written in Matlab and was found to provide very accurate results when compared with the SDA-based calculations [25] for summations on the order of 1000 terms (i.e. k=0-1000 for m_k, q_k, etc.). A good rule of thumb for choosing the value for l for placement of the virtual magnetic walls was found to be twenty times the sum of all major dimensions (i.e. 20*(w+s+h)). For implementation within a distributed model for spiral inductors, only the resistance terms above are used, with averages taken for mutual resistance between conductors of unequal length, while partial inductances are calculated via the accurate closed-form expressions in [33].

APPENDIX C. Fundamental Explanation of PEEC Modeling

Partial Element Equivalent Circuit (PEEC) [19] models are derived from integral equation solutions based on the summation of all electric field sources within a conductor geometry, and their respective time and spatial dependence, as

$$\frac{\bar{J}}{\sigma} = \bar{E}_o - \frac{\partial \bar{A}}{\partial t} - \nabla\Phi. \tag{C1}$$

The three main computational tasks involved are inductance calculations, capacitance calculations, and network analysis.

Formulation of a PEEC model first requires that a structure be broken down into volume cells, which forms a basis for the nodes in the final PEEC. The unknown quantities (i.e. current and charge) are assumed to be locally constant within their respective cell boundaries, and thus the equivalent circuit element values may be calculated and utilized in solving the integral equation for a single cell or between two cells, the latter applying to mutual inductive and capacitive terms. Inductance and capacitance values may be calculated via the closed-form expressions presented in [33] and [51]. The resulting equivalent circuit model then consists of partial self and mutual inductances and capacitances, with the number of each being determined by the number of nodes and significant coupling terms (L_{pij}, C_{pij}) included.

Time retardation effects may also be included in the PEEC models for geometries having dimensions that are large in comparison to wavelength. For a region with uniform properties ϵ_r, μ_r, the retarded time is given by

$$t' = t - \frac{|\bar{r} - \bar{r}'|}{c}(\epsilon_r \mu_r)^{1/2}, \tag{C2}$$

where $\bar{r}$ and $\bar{r}'$ are vectors from the origin and c is the speed of light. While a retarded PEEC model solver is more difficult to implement due to the delays,

the difference between the retarded and non-retarded solutions may be significant enough to warrant the extra analysis efforts [52]. For EMI problems, the far coupling terms can have appreciable phase lags associated with them when the spectrum of the excitation contains frequencies such that the condition $\tau_{ij} f_{max} \ll 1$ is no longer satisfied, where τ_{ij} is the defined as the time delay of an EM wave (e.g. plane wave) between conductors i and j at frequency f_{max}.

PEEC models that do not include retardation are entirely CAD compatible, as they consist solely of lumped elements with mutual coupling. Thus, any popular circuit simulation tool, such as Libra or MWSpice©, may be used to obtain frequency- or time-domain descriptions for any node in the network.

The PEEC methodology lends itself well to the analysis of multiconductor systems with three-dimensional geometries. Such a class of conductor arrangements includes multilayered lumped elements. Although the standard PEEC methodology can be used to compute both the inductance and capacitances of spiral inductor segments, the use of an alternate efficient and accurate spectral domain technique is proposed in this thesis for the computation of capacitances and conductances associated with structures on semi-conducting silicon substrates [24, 53, 54].

APPENDIX D. Matlab Function Script for Mutual Inductance Between Rectangular Bars

```
function [Mb]=mrebar(l1,l2,l3,E,P,a,b,d,c)

q=[(E-a) (E+d-a) (E+d) E];
r=[(P-b) (P+c-b) (P+c) P];
s=[(l3-l1) (l3+l2-l1) (l3+l2) l3];


Mb=0;
for i=1:4
  for j=1:4
    for k=1:4
       x=q(k);
       y=r(j);
       z=s(i);

       if x~=0&y~=0&z~=0
       Mb=(-1)^(i+j+k+1)* ...
       1e-7/(a*b*c*d)*((y^2*z^2/4-y^4/24-z^4/24)*x* ...
       log((x+sqrt(x^2+y^2+z^2))/sqrt(y^2+z^2))+(x^2*z^2/4-x^4/24 ...
       -z^4/24)*y*log((y+sqrt(x^2+y^2+z^2))/sqrt(x^2+z^2))...
       +(x^2*y^2/4-x^4/24-y^4/24)*z*log((z+sqrt(x^2+y^2+z^2))/...
       sqrt(x^2+y^2))+(1/60)*(x^4+y^4+z^4-3*x^2*y^2-3*y^2*z^2-3*z^2*...
       x^2)*(sqrt(x^2+y^2+z^2))-x*y*z^3/6*atan(x*y/(z*sqrt(x^2+y^2 ...
       +z^2)))-x*y^3*z/6*atan(x*z/(y*sqrt(x^2+y^2+z^2)))...
       -x^3*y*z/6*atan(y*z/(x*sqrt(x^2+y^2+z^2))))+Mb;

       elseif (x==0&y==0&z~=0)|(x==0&y~=0&z==0)|(x~=0&y==0&z==0)
       Mb=(-1)^(i+j+k+1)* ...
       1e-7/(a*b*c*d)*(...
       (1/60)*(x^4+y^4+z^4-3*x^2*y^2-3*y^2*z^2-3*z^2* ...
       x^2)*(sqrt(x^2+y^2+z^2)))+Mb;


       elseif (x==0&y~=0&z~=0)|(x~=0&y==0&z~=0)|(x~=0&y~=0&z==0)
       Mb=(-1)^(i+j+k+1)* ...
       1e-7/(a*b*c*d)*((y^2*z^2/4-y^4/24-z^4/24)*x* ...
       log((x+sqrt(x^2+y^2+z^2))/sqrt(y^2+z^2))+(x^2*z^2/4-x^4/24 ...
       -z^4/24)*y*log((y+sqrt(x^2+y^2+z^2))/sqrt(x^2+z^2)) ...
       +(x^2*y^2/4-x^4/24-y^4/24)*z*log((z+sqrt(x^2+y^2+z^2))/ ...
       sqrt(x^2+y^2))+(1/60)*(x^4+y^4+z^4-3*x^2*y^2-3*y^2*z^2-3*z^2* ...
       x^2)*(sqrt(x^2+y^2+z^2))) ...
       +Mb;


       end;

    end;
  end;
end;
```

FIGURE D-1. Matlab script for calculating M_b, 'mrebar.m'.