AN ABSTRACT OF THE DISSERTATION OF

Lei Zheng for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on August 1, 2018.

Title: Modeling and Design of Interconnects and Passive Components for Millimeter-Wave Integrated Circuits in Silicon

Abstract approved: _____

Andreas Weisshaar

For mmWave Integrated Circuit (IC) design, co-integration of passives can reduce size and power consumption, increase reliability, and reduce overall cost. However, skin and proximity effects in the metallization are aggravated at mmWave frequencies, resulting in increased attenuation and degradation of overall performance. Furthermore, tight integration of passive components (to reduce the die size) poses additional design challenges due to the complicated electromagnetic couplings between the components in close proximity. Other parasitic effects such as dummy metal fill parasitics and substrate eddy current loss, the impact of process variability and uncertainty are also more prominent at mmWave frequencies.

In this thesis, scalable compact modeling techniques based on the Principle of Electromagnetic Similitude and additionally developed methods of complexity reduction are presented. Scalable and compact equivalent circuit models for on-chip microstrip and Coplanar Waveguide (CPW) are developed and validated by both electro-magnetic (EM) simulations and on-wafer measurements. Furthermore, a more general field-based scalable modeling approach for multi-conductor interconnects (e.g., coupled CPWs) and more complicated passives is presented. The field-based approach has been applied and validated for modeling mmWave inductors, including the impact of metal fills and substrate eddy-current effects. Scalable models to capture the magnetic coupling between spiral inductors are presented and a compact layout strategy for reduction of magnetic

coupling is proposed. The scalable and compact models include multi-physics effects such as temperature dependency and can also be utilized to study the impact of the process variations efficiently.

Modeling and Design of Interconnects and Passive Components for Millimeter-Wave Integrated Circuits in Silicon

by

Lei Zheng

A DISSERTATION

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Doctor of Philosophy

Presented August 1, 2018
Commencement June 2019

Doctor of Philosophy dissertation of Lei Zheng presented on August 1, 2018.

APPROVED:

Major Professor, representing Electrical and Computer Engineering

---

Director of the School of Electrical Engineering and Computer Science

---

Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Lei Zheng, Author

ACKNOWLEDGEMENTS

The completion of this thesis was not possible without the support from numerous persons and organizations. First of all, I would like to express my sincere gratitude to my advisor Dr. Andreas Weisshaar. He taught me how to conduct research in a systematic and rigorous way. His insights and ideas into research direction have been invaluable through my Ph.D. program. I thank him for always being patient and supportive during many frustrating times. I have benefited greatly from his advice not only on the academic research, but also on personal life. I would also like to thank him for the financial support through CDADIC research fund. It is my honor and privilege to work under his guidance.

I want to thank Profs. Karti Mayaram, Arun Natarajan and Gabor Temes for being on my program committee. I enjoyed my first analog circuit class ECE522 from Prof. Mayaram and am very impressed by his handwritten notes. I would like to thank Prof. Natarajan for sharing his 67 GHz VNA system. Most of the measurements were done in this system. I also enjoyed his advanced RFIC classes. Thanks go to Prof. Gabor Temes for teaching me the network theory, which is an important part of my thesis. I will miss all his jokes in the classes and CDADIC meetings. Prof. Parmigiani also deserves my sincerest thanks for serving as graduate committee representative.

I sincerely thank my former colleagues Steven Gaskill and Vikas Shilimkar for useful discussions and feedbacks. I would also like to thank Andrew Ferrara and Xuanyi Dong for help with the measurements. Also thanks to my lab mates Dyuti Sengupta, Philip Kness, and Siddarth Rai Mahendra for questions and discussions.

I have been very fortunate to have many friends at OSU. Thank all my friends to make my life at Corvallis so enjoyable - Fan Zhou, Xuanyi Dong, Kai Zhan, Yao Liu, Jian Kang, Hui Zhang, Hongliang Zhang, Jiajia Song, Liping Liu, Yang Xu, Abhishek Agrawal, Sanket Jain and Siladitya Dey.

Finally, I sincerely thank my parents and my elder sister for their unconditional love and support of my studies in the United States. Special thanks to my wife, Jing, who has been supporting and encouraging me for many years, and my daughter, Lixuan, who brings me so much joy and happiness.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

Page

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF TABLES

LIST OF APPENDIX FIGURES

Figure Page

LIST OF APPENDIX TABLES

Chapter 1: Introduction

1.1 mmWave Applications

mmWave systems have a wide range of applications from scientific, military, medical and security to wireless communications. Traditional mmWave systems are used in sectors such as defense and aerospace with low volume production. Over the past decade, commercial applications have fostered the prolification of mmWave technology. The availability of radio spectrum in the 70-90 GHz mmWave bands has led to a broad range of new commercial wireless products and services including advanced automotive radar (Fig. 1.1 [1]) and Internet of Things (IoTs) [2]. Fifth generation ("5G") mobile networks are also stimulating the development of wireless communication systems at mmWave frequencies. The 5G New Radio Standard (NRS) has officially been ratified by 3GPP [3] in 2017. Compared with fourth generation (4G), 5G wireless systems can achieve as high as 10 to 100 times the data rate of 4G with less than a millisecond latency [4]. Development of 5G technologies includes small cell (Fig. 1.2 [5]), full duplex, massive MIMO, beamforming and so on. Major wireless carriers in the United States are expected to provide 5G services by the end of 2018 [6].

Implementations of mmWave systems have also been evolving as integrated circuit (IC) technologies keep advancing. Technology scaling has pushed the cutoff frequencies of on-chip transistors into the mmWave range [7]. In addition, as frequencies go up into the mmWave region, conventional bulky passives like inductors and transformers are also scaled and can be realized in the on-chip metal layers [8] [9]. Due to the small wavelength, development of on-chip distributed couplers [10] and filters [11], and even phased array antennas [12] are possible with affordable silicon area. Both active and passive circuit scaling enables the development of mmWave systems on CMOS processes. Co-integration of passive and active circuits can improve the reliability, lower the power consumption and reduce the cost for mass production.

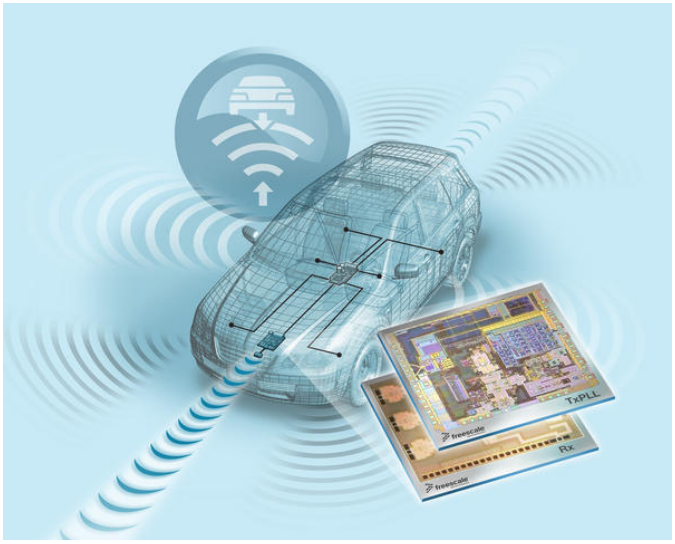

Figure 1.1: Commercialized 77 GHz silicon germanium (SiGe) BiCMOS transmitter for automotive radar (Freescale Semiconductor (now NXP) [1]).

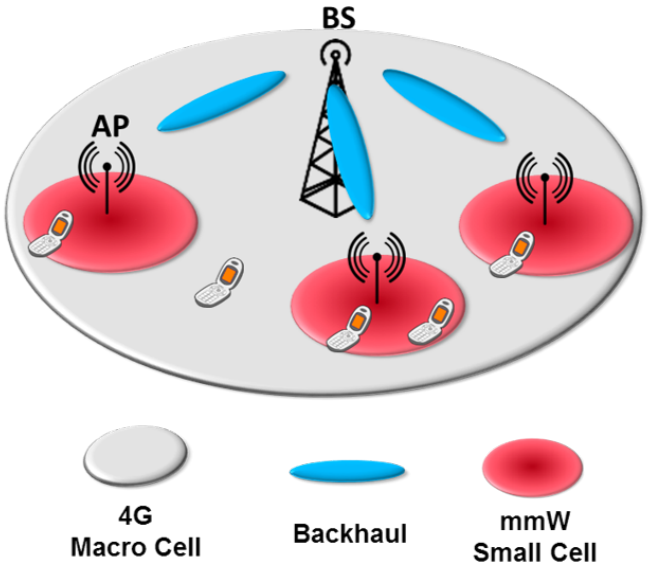

Figure 1.2: 5G wireless communication network concept (from MiWaveS [5]).

1.2 Passive Circuits on Silicon

A brief overview of on-chip interconnects and inductors is given in this section. These structures and components are widely used in Radio Frequency (RF)/mmWave ICs. In this thesis, the efforts are devoted to developing scalable and compact equivalent circuits that include multi-physics effects such as temperature and process variations, metal fill and electro-magnetic (EM) couplings.

1.2.1 On-Chip Interconnects

In RF/mmWave ICs, on-chip interconnects serve mainly two purposes: (i) transmitting and receiving RF signals within or between various functional circuit blocks, and (ii) synthesizing other more complicated passives such as couplers [13], power dividers [14], filters [15], and so on. When transmitting and receiving RF signals, depending on the signaling scheme (i.e., single-ended or differential), on-chip interconnects can be categorized as isolated and coupled transmission lines. For isolated transmission lines (Fig. 1.3), the main on-chip structures used are microstrip, coplanar waveguide (CPW), coplanar stripline (CPS), and stripline. Regarding coupled transmission lines (Fig. 1.4), coupled microstrips and coupled CPWs are the most commonly used structures for differential signaling. The design specifications of the on-chip interconnects are focused on characteristic impedance, attenuation and phase velocity (delay).

The electrical performance of a transmission line can be derived from the $RLGC$ equivalent circuit model of an electrically short section of transmission line of length Δz, where R and L are the per-unit-length series resistance and series inductance, and G and C are the per-unit-length shunt conductance and shunt capacitance parameters (see Fig. 1.5). Since on-chip interconnects are basic building blocks for other complicated passives (e.g., stub matching networks, branch-line coupler, Wilkinson power divider/combiner), it is crucial to develop scalable compact models for on-chip interconnects, which also enable design optimization with active circuits.

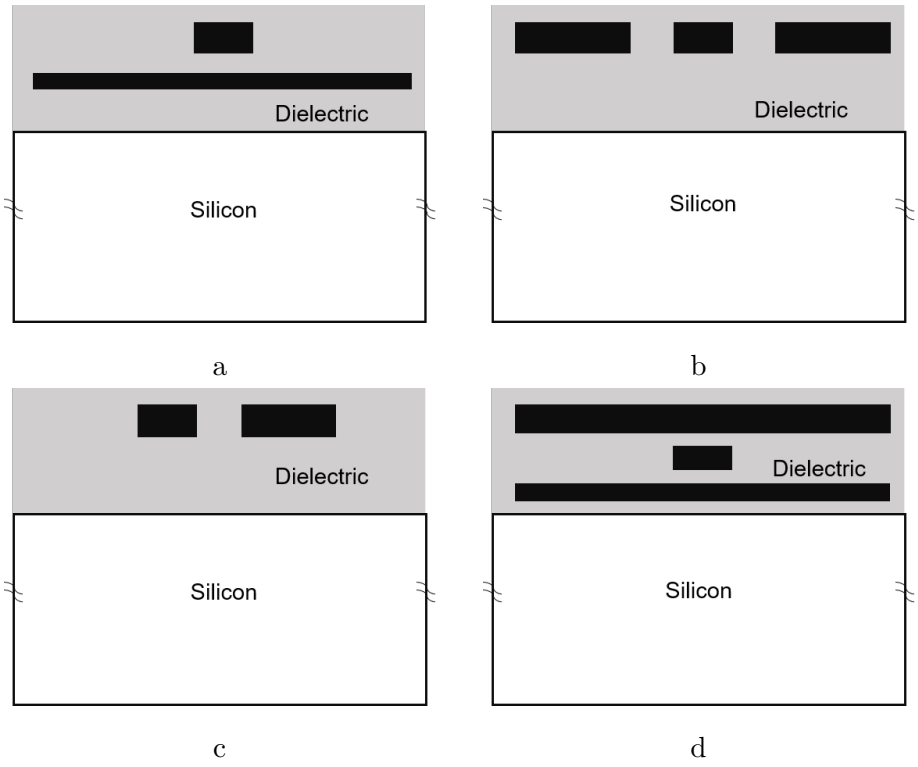

Figure 1.3: On-chip isolated transmission lines: (a) microstrip, (b) coplanar waveguide, (c) coplanar stripline, (d) stripline.

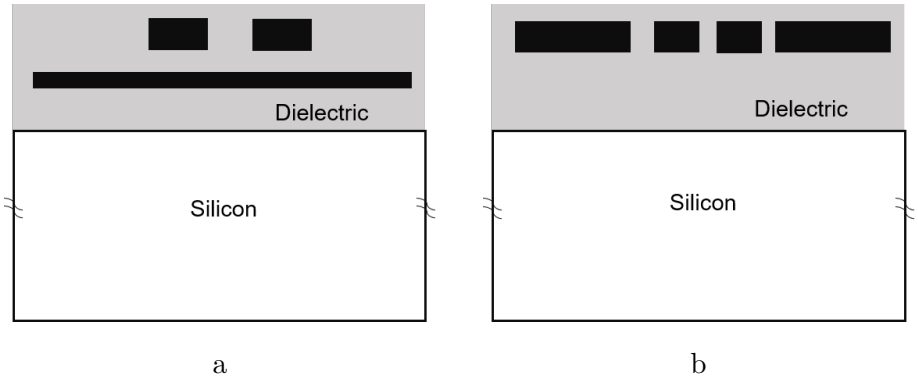

Figure 1.4: On-chip coupled transmission lines: (a) coupled microstrip, (b) coupled coplanar waveguide.

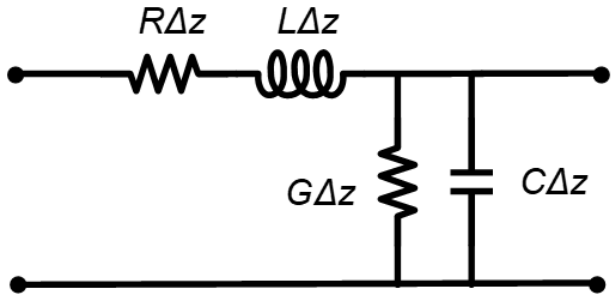

Figure 1.5: *RLGC* equivalent circuit model of an electrically short section of transmission line of length Δz.

1.2.2 On-Chip Spiral Inductors

On-chip spiral inductors, as illustrated in Fig. 1.6, play an important role in RF/mmWave IC designs. They have been widely adopted in many circuit blocks, such as the LC tank in a voltage-controlled oscillator (VCO) [16], inductive degeneration in a low noise amplifier (LNA) [17], transformers [18], baluns, LC matching networks, and lumped LC filters [19]. They are also used to realize the same functionalities as complicated distributed passives such as power dividers/combiners [20], couplers, and phase shifter [21], with much smaller footprint.

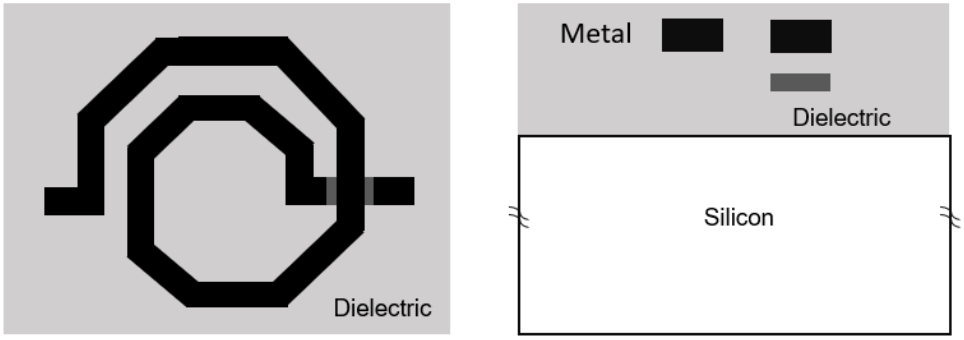

Figure 1.6: Illustration of a typical on-chip spiral inductor: (a) top view; (b) side view.

The electrical performance of on-chip spiral inductors is mainly characterized by three parameters: inductance, quality factor (Q) and self-resonant frequency (SRF). The inductance (pH to nH range) usually is designed by varying inductor size, number of turns, line width and spacing. Achieving large inductance (μH to mH range) on chip is challenging due to impractical size if magnetic materials are not used. The Q of an inductor is the ratio of the energy stored in the inductor to the energy dissipated per cycle [22]. For most cases it is important to optimize the layout to maximize Q whenever possible [23]. The Q limitation is related to ohmic losses in conductors including skin and proximity effects, silicon substrate losses due to displacement currents and eddy currents, and parasitic capacitances within the spiral and between the spiral and the silicon substrate. With increasing operating frequency, there is a point where the capacitance resonates with the inductance resulting in an extremely high impedance, close to an open circuit. This frequency is called the self-resonant frequency or SRF (Fig. 1.7). Operating an inductor near this frequency is avoided since the spiral behaves no longer like an inductor. When designing an inductor, SRF is always chosen much higher than the operating frequency.

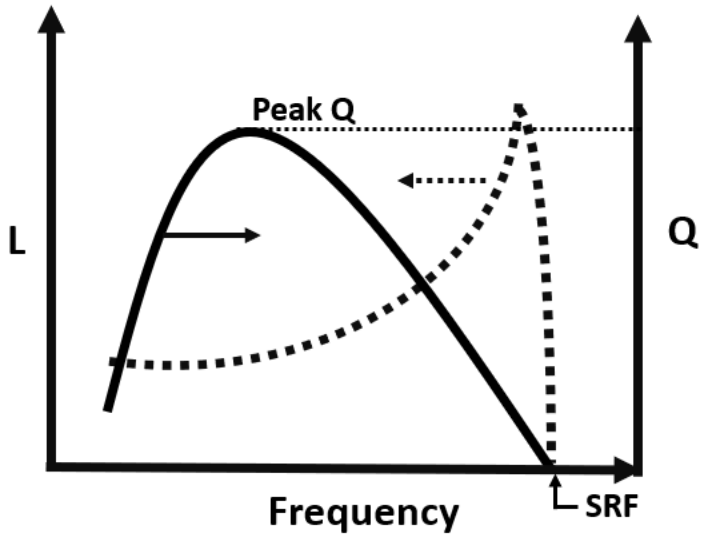

Figure 1.7: Illustration of the frequency-dependent L and Q characteristics of a typical on-chip spiral inductor.

1.3 Challenges in Integration of Passives on Silicon

Operating at mmWave frequencies makes it possible to fully integrate passive components on silicon with the goal to reduce size and power consumption, increase reliability, and reduce overall cost. Furthermore, system-on-chip technology increasingly incorporates a diverse set of functional devices and modules such as sensors, digital logic, and analog-mixed-signal and RF blocks. Even though full integration of passive components is viable in these mmWave frequency bands, high-frequency parasitic effects, such as eddy-current loss in the metallization and silicon substrate loss, are aggravated at mmWave frequencies, resulting in the degradation of the quality of passive components [24]. At the same time, high quality passive components play a key role in circuit design, particularly for low power and low noise circuits. Furthermore, the tight integration of passive components (to reduce the die size) poses additional design challenges due to the complicated electromagnetic coupling between the components and with interconnects in close proximity. Integration of passive components and functionally diverse devices and circuits also poses challenges in terms of interference between various system blocks.

This interference is not limited to electromagnetic coupling but includes other multi-physics effects such as temperature variation. In addition to electromagnetic coupling and other parasitic effects, the impact of process variability, uncertainty, and metal fill is more prominent at mmWave frequencies.

1.3.1 Eddy-current Loss

For on-chip passives in silicon, eddy-current loss exists in the metallization layers as well as in the silicon substrate if heavily-doped digital processes are used [25]. The eddy-current loss in the conductors is caused by skin and proximity effects, where the current density is redistributed non-uniformly due to the time-varying magnetic fields induced by the current itself (skin effect) and/or other current(s) (proximity effect). As illustrated in Fig. 1.8, the current distribution in a semi-infinite conductive space can be solved analytically [26]. The current distribution in the conductive space is formulated as

$$J_z = J_0 e^{-x/\delta} e^{-jx/\delta} \tag{1.1}$$

with

$$J_0 = \sigma E_0. \tag{1.2}$$

E_0 is the applied time-varying electrical field. The parameter δ is the skin depth and is given by

$$\delta = \frac{1}{\sqrt{\pi \mu \sigma f}}, \tag{1.3}$$

where μ is the permeability of the conductor, σ is the conductivity and f is the frequency of interest. The per-unit-length AC resistance is

$$R = \frac{2P}{{I_0}^2}, \tag{1.4}$$

where P is the per-unit-length power loss and I_0 is the total current. Assuming S is the cross-sectional area, the power loss is represented as

$$P = \frac{1}{2} \int_S \frac{{J_z}^2}{\sigma} dS = \frac{1}{2} \int_0^\infty \frac{w {J_z}^2}{\sigma} dx. \tag{1.5}$$

The total current I_0 is given as

$$I_0 = \int_0^\infty w J_z dx. \tag{1.6}$$

From the equations above, we can derive the per-unit-length AC resistance R, which is

$$R = \frac{1}{\sigma} \frac{1}{w\delta}. \tag{1.7}$$

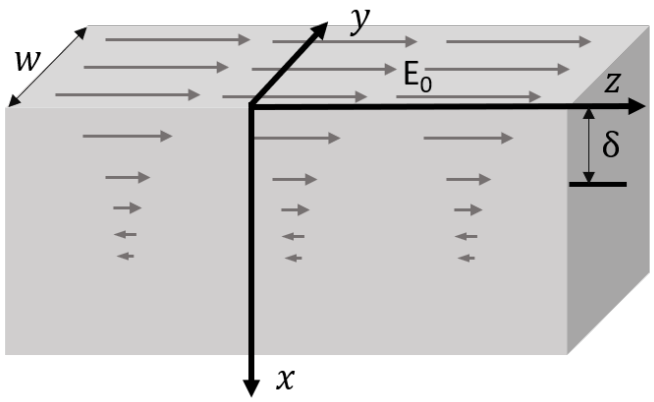

Figure 1.8: Decay of current into conductor (modified from [26]).

R is inversely proportional to the skin depth δ. It is equivalent to the DC resistance (uniform current density) over a depth of δ. As frequency increases, the skin depth will decrease and resistance will increase. As illustrated in Fig. 1.9, a simple model of R for a rectangular conductor at high frequencies can be represented as

$$R = \frac{1}{2\sigma} \left(\frac{1}{(w + t - 2\delta)\,\delta} \right). \tag{1.8}$$

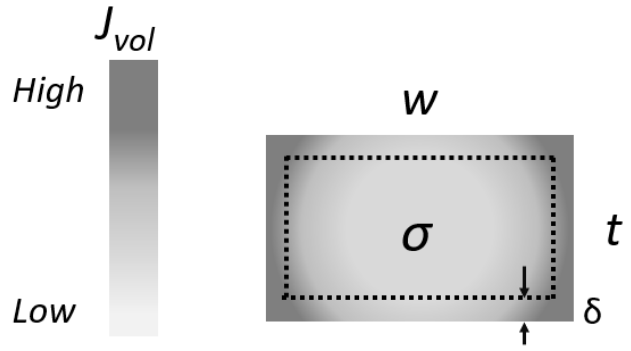

Figure 1.9: Illustration of non-uniform current density in an isolated on-chip trace due to skin effect.

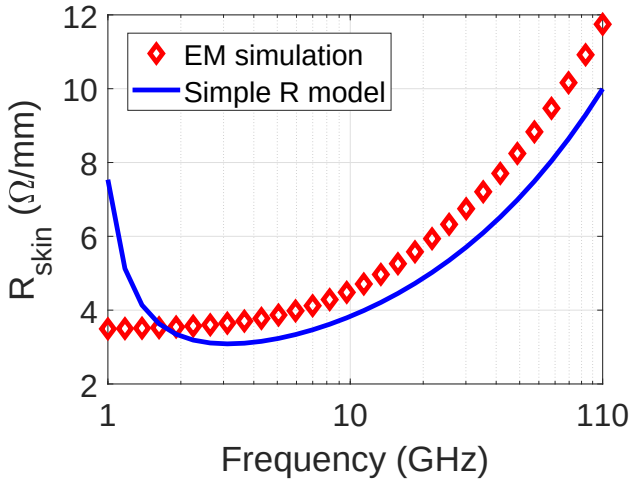

Figure 1.10: Comparison between EM simulation and the simple R model (Eq. 1.8) for a rectangular conductor. The conductor width is 4 μm and the thickness is 2 μm and the conductivity is 3.5×10^7 S/m.

However, this model is not accurate when the skin depth is larger than or comparable with the physical dimensions and does not correctly capture the non-uniform current distribution in the corners, as illustrated in Fig. 1.10. For on-chip metalizations, aluminum and copper are commonly used in CMOS fabrication process. The top metal layers for those processes are thick and have high conductivity. At mmWave frequen-

cies, the skin depth is much smaller than the top metal thickness. For example, the skin depth for aluminum and copper at 60 GHz is 0.34 μm and 0.27 μm, respectively, assuming the conductivity for aluminum is 3.5×10^7 S/m and for copper is 5.8×10^7 S/m. The top thickness is usually several micrometers (μm) for typical RF processes. Thus, the increase of resistance in the metallization from DC to mmWave frequencies due to skin and proximity effects is substantial.

There are well-known methods (e.g., Wheeler's incremental inductance rule [27]) to capture the change of resistance and inductance at high frequencies where the skin effect is fully developed. However, there is still a need for scalable compact models that are not only valid at high frequencies, but also well behaved from low to intermediate frequencies, where the skin effect starts to become important with a skin depth comparable with the conductor geometry dimensions.

For some passive structures that do not have a ground plane underneath to shield the silicon substrate (e.g., CPWs, inductors and transformers), another possible eddy-current loss occurs in the silicon substrate, depending on the silicon resistivity as well as the operating frequency. For most RF processes, the silicon substrate is lightly doped (e.g., 1-100 Ω·cm) so that it behaves like a lossy dielectric substrate, where the skin depth in the silicon substrate is much greater than its physical thickness. In this case, the loss in the silicon substrate is mainly due to displacement current. However, when integrating RF/mmWave circuits in digital processes, the skin depth in the silicon substrate (65 μm at 60 GHz for $\rho = 0.1$ Ω·cm) is much smaller than the substrate thickness (on the order of hundreds of μm), since digital processes typically have low-resistivity silicon substrates (e.g., $\rho < 0.1$ Ω·cm) to prevent latch-up [28]. Thus, the conduction eddy current flowing in the substrate due to the time-varying magnetic field (Fig. 1.11) is not negligible. In this case, not only does the conductor loss of the passive devices need to be taken into consideration, but also the substrate eddy-current loss.

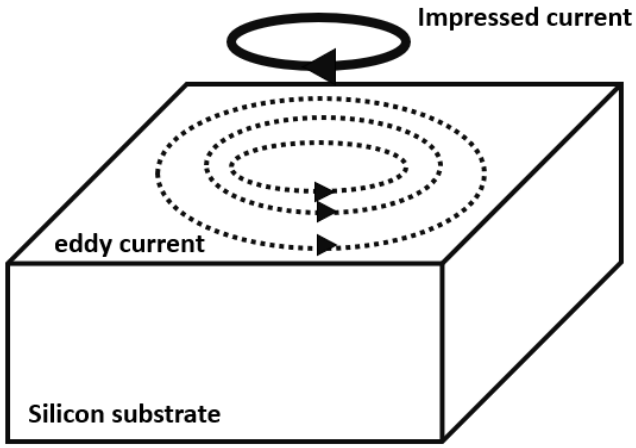

Figure 1.11: Schematic representation of eddy current in silicon substrate (adopted from [29]).

Eddy-current loss in dummy metal fill also needs to be considered for the performance of passives [30], since the insertion of metal fill is necessary for uniformity of the metal density during Chemical Mechanical Polishing (CMP) [31] in advanced IC manufacturing processes. Adding dummy metal fill can help planarize each metal and dielectric layer, reduce the CMP defects, and thus improve the yield. However, the additional metal fill usually degrades the electrical performance of the passive components. One of the biggest issues at high frequencies is the resistive loss. Even though the metal fills are isolated (floating or grounded) (Fig. 1.12), the external magnetic field generated by the excitation current will produce eddy current $\vec{J_e}$ in the metal fill. The eddy current results in a power loss in the metal fills, which can be expressed as [32]

$$P_L = \frac{1}{2}\int_V \frac{\left|\vec{J_e}\right|^2}{\sigma}\, dv. \tag{1.9}$$

where σ is the conductivity and V is the volume of the metal fill. With frequencies extending into the mmWave region, the skin effect in metal fill is fully developed where the skin depth is smaller than the minimum metal fill size, even in metal fill at the lower metallization layers. These additive losses can significantly reduce the Q of a spiral in-

ductor and increase the attenuation of interconnects.

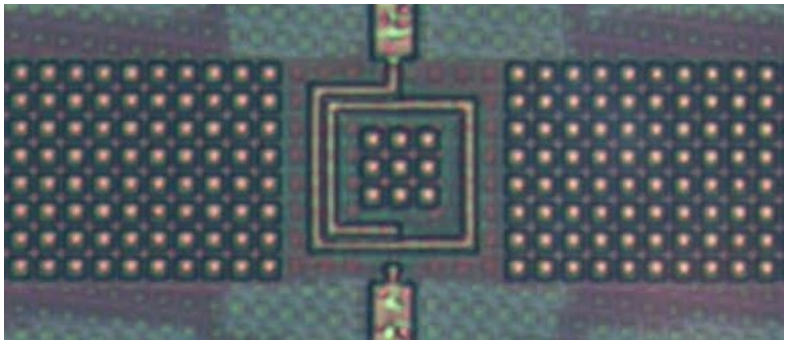

Figure 1.12: A typical on-chip inductor with metal fill.

1.3.2 Electromagnetic Coupling

For RF/mmWave ICs, passive structures typically occupy more than half of the silicon area. There is a need for tighter integration of high quality on-chip passive components to reduce the die size as well as the fabrication cost. This poses significant challenges due to the complicated electromagnetic coupling between components (Fig. 1.13) and coupling to interconnects in close proximity [33]. The electromagnetic coupling mechanism involves both capacitive coupling and magnetic coupling. Traditionally, to reduce the effects of parasitic coupling, a large separation distance is required, which wastes silicon area and increases cost. Large separation sometimes also requires longer interconnects, which introduces additional parasitics and degrades circuit performance. Realization of highly compact layouts while keeping low coupling is a key challenge in compact designs.

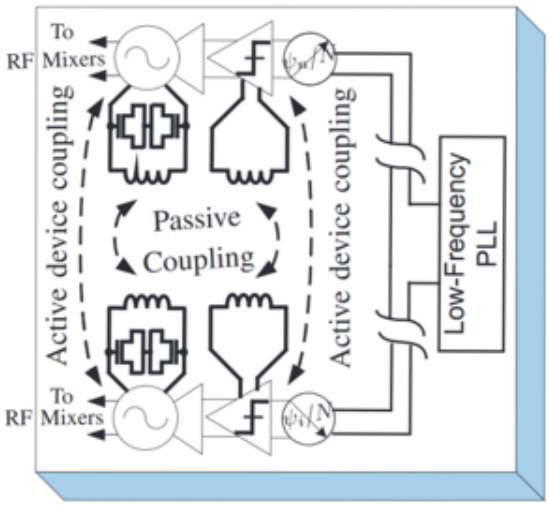

Figure 1.13: Diagram illustrating electromagnetic coupling between example passive circuits (excerpted from [34]).

1.3.3 Process and Temperature Variation

Process variation occurs naturally during the CMOS fabrication processes [35]. For transistors, the variations include physical dimensions such as length, widths and gate oxide thickness. For passives, the related variations mainly consist of inter-layer-dielectric (ILD) thickness, dielectric constant, metal layer thickness and conductivity. In foundry process design kits (PDKs), process variations are given as normal distributions with known mean (μ) and standard deviation (σ) values. To capture the impact of variations on the active circuit performance, circuit designers run analyses for nominal and corner cases with provided model files. However, for passives circuit, the corner cases are usually difficult to determine since the mapping from physical design variation to electrical performance involves many design parameters and complicated EM interactions. The corner cases for physical parameters do not necessarily indicate the corner cases for electrical performance. In addition, on-chip passives also are affected by temperature changes primarily because the conductivity of the metallization is a function of temperature [36]. Depending on the application (e.g., commercial, industrial, or military), the temperature range for electronic devices can be from -55 to 125 degrees Celsius (°C). With such a wide range, the effects of the temperature variation on the passives need to

be included in the model.

1.4 Introduction of Scalable Modeling Techniques

The main challenge of scalable modeling is capturing the frequency-dependent characteristics with many geometrical and material property parameters involved. Those frequency-dependent characteristics include the skin and proximity effects in the conductors and in the silicon substrate, shunt capacitance and conductance in the passivation layer and silicon substrate, and EM couplings between different passives. To model these effects, numerical tools can extract the electrical models, which are usually network parameters (e.g., S, Y or Z parameters) at the frequencies of interest. There are several widely adopted numerical techniques, such as Method of Moments (MoM) [37], Finite Element Method (FEM) [38], Finite-Difference Time-Domain method (FDTD) [39], and Partial Element Equivalent Circuit (PEEC) approach [40], [41]. The advantage of a numerical approach is its capability of computing complicated structures and yet providing very accurate results. However, the drawback is that it involves meshing of structures and matrix calculations, which is usually time consuming and requires large computational resources. Such disadvantage becomes more limiting as frequency goes up into the mmWave range, where the skin depth is much smaller than the physical dimensions. This results in an exponential increase in the number of mesh elements. Furthermore, these tools are not directly compatible with circuit simulation, and not all of the numerical results can be seamlessly used in circuit simulators (e.g., ADS, HSPICE and SPECTRE), especially for broadband signals. In such cases, a further step of fitting the simulated data into an equivalent circuit model needs to be performed. There also exist black box modeling techniques (e.g., model order reduction (MOR) [42], [43]) by fitting the mathematical formulas or equivalent models to the simulated response regardless of the physical structures. Such modeling techniques require no physical information. However, the complexity of the models is high and the models are often not as robust and stable [44] as physical modeling techniques.

Another modeling approach is to develop scalable equivalent circuit models which are directly compatible with circuit simulators. First, the circuit model topologies are proposed based on physical behaviors. The circuit element values are functions of the geometrical and material property parameters, which are usually implemented by closed-

form or empirical expressions. The biggest advantages of this type of modeling technique are (i) that it enables co-simulation/optimization with active circuits without time consuming EM simulations, since the models are derived from equations that can be preprogrammed in the circuit simulator, and (ii) the models are asymptotically stable. The disadvantages of this approach include the limited accuracy and bandwidth of the model due to approximations made during model development. Furthermore, the applicable design dimension range is constrained to achieve a certain accuracy. In terms of scalable equivalent circuit model development, the main challenge is that a large of number of parameters are involved. Hence, the circuit element values are functions of many variables, which makes direct development of closed-form/empirical equations virtually impossible. To make the development of scalable models viable, a reduction of complexity is needed.

1.5 Research Contributions

The goal of this thesis is to develop broadband, process-aware, multi-physics models for on-chip interconnects and passive components to aid in the design of mmWave integrated circuits in silicon. The scalable modeling techniques developed in this thesis for on-chip passives are listed below.

- Systematic scalable modeling approaches are developed for on-chip microstrip and CPW. The equivalent circuit models are suitable for various process nodes with large normalized geometry aspect ratio. The novelty of the techniques is the application of the Principle of Electromagnetic Similitude to reduce the number of variables during model development combined with a Foster network topology to capture the frequency-dependent characteristics with ideal lumped frequency-independent elements. For scalable modeling of a microstrip, we propose a new approach by separately modeling the signal and conductor effects while considering the mutual effects. This greatly reduces the number of variables and makes model development viable. For modeling CPWs, equivalent circuit models for different frequency regions are developed to reduce complexity, and combined to get the fully scalable model. Both scalable models are validated through measurements of fabricated test structures.

- A novel field-based scalable and compact modeling approach is demonstrated for

on-chip multi-conductor interconnects and more complicated passives. This method explores the physical behaviors of the frequency-dependent resistance. Two fundamental phenomena, skin and proximity effects, are modeled with simple closed-form expressions. The procedure of mapping the closed-form expressions to equivalent circuit models is also demonstrated. This approach has been applied to both isolated and coupled transmission lines, as well as on-chip spiral inductors, and has been validated by measurement.

- Our scalable models include multi-physical effects and eddy-current losses in the silicon substrate, as well as in metal fills. The physical modeling process enables capturing the temperature dependency in a simple fashion by scaling the resistance elements. The substrate eddy current loss is augmented in our scalable models for application to low substrate resistivity processes. The metal fill losses in an arbitrary uniform field are modeled as well. Instead of performing time-consuming EM simulations, the scalable models can be used directly to study process variations efficiently and yet accurately.

- Scalable and compact models for magnetic coupling between on-chip spiral inductors are demonstrated. Techniques for minimizing the magnetic coupling are proposed by using the principle of magnetic flux cancellation. Both compactness and high isolation can be achieved through this approach.

1.6 Thesis Overviews

In this thesis, we first discuss the design considerations for on-chip transmission lines. The scalable modeling techniques for microstrip and CPW are presented in Chapter 2. This is followed by a general field-based modeling method for more complicated passives in Chapter 3. Chapter 4 demonstrates the scalable modeling techniques for spiral inductors, including metal fill and substrate eddy current effects. Chapter 5 presents scalable and compact equivalent circuit models for the magnetic coupling between on-chip spiral inductors and proposes a new layout topology to achieve compactness while simultaneously reducing the magnetic coupling. Finally, Chapter 6 provides suggestions for future work and concludes this thesis.

Chapter 2: Design and Modeling of On-Chip Microstrips and CPWs

2.1 Introduction

On-chip microstrips and CPWs have been widely adopted for transmitting signals, in synthesizing filters, impedance matching networks, and so on. They are fundamental building blocks for complicated passives. During RF/mmWave IC design, these passives are usually simulated and optimized in EM simulators, which require extra computational resources and are time-consuming. To enable co-simulation/optimization with active circuit, scalable and compact equivalent circuit models are desired. In this chapter, we present systematic approaches to develop broadband scalable and compact models for on-chip microstrips and CPWs. The models are suitable for a wide range of modern process nodes with large normalized geometry range. We have validated the models through both EM simulations and measurements of fabricated test chips. We also apply the microstrip model to an L-section matching network and a branch line coupler.

This chapter is organized as follows. In Sections 2.2 and 2.3 we discuss the design considerations for on-chip microstrips and CPWs, and we evaluate the performance of the transmission lines (the characteristic impedance, propagation constant and quality factor) for different design choices for example CMOS processes. Then, modeling challenges and approaches in literature are discussed in Section 2.4. Next, in Section 2.5, an overview of proposed scalable modeling techniques is presented. In Sections 2.6 and 2.7, the details of scalable model development for microstrips is explained and model validation is presented as well. Next, we present the scalable model development for CPWs in Sections 2.8 and 2.9. The scalable models include the temperature dependency and can be directly used to study the impact of process variations, as demonstrated in Section 2.10.

2.2 Design Considerations for On-Chip Microstrips

An on-chip microstrip transmission line consists of a metal trace and a ground plane. At mmWave frequencies, the conventional Metal-Insulator-Semiconductor (MIS) structure with back-end metallization is not suitable since the silicon substrate is too thick to suppress surface wave propagation [24]. In a standard RFCMOS or BiCMOS process, metal layers and dielectric layers are stacked up and passivation layers are placed on the top (Fig. 2.1). When designing a microstrip structure, the top thick metal layer is usually chosen as the signal trace, which typically is aluminum or copper with high conductivity; hence, once the ground layer is defined, the height between the bottom ground plane and the signal line is fixed. For the desired characteristic impedance, there exists a unique width for the signal line that fulfills this requirement. Thus, for the possibility of optimization, it is reasonable to consider choosing different metal layers as ground (Fig. 2.2).

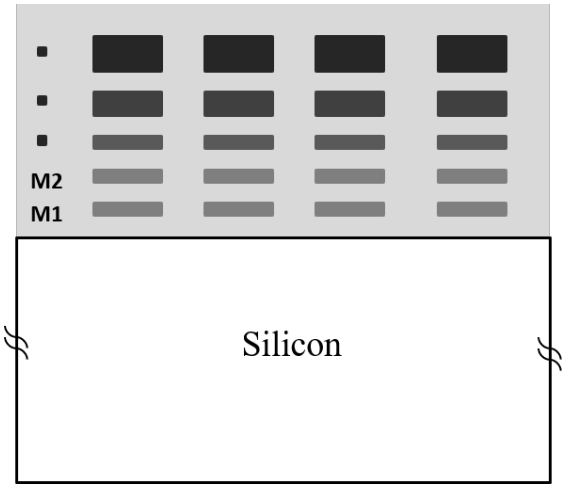

Figure 2.1: Metal layer stackup in IC processes.

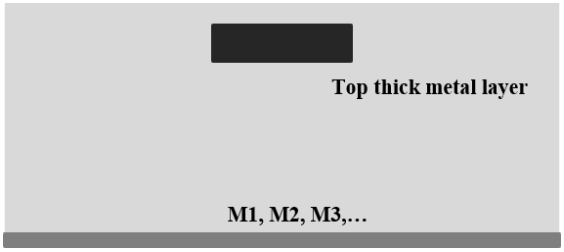

Figure 2.2: On-chip microstrip structure.

For a particular IC process, design rules are specified restrictedly to produce desired yields. This includes restrictions such as the minimal width and the minimal spacing for layout of metal traces. Thus, for microstrip line design, the minimal width limits the maximal achievable characteristic impedance. Figure 2.3 illustrates the maximal characteristic impedance that could be achieved in three different processes (i.e., TSMC 65nm, TowerJazz (Jazz) 130 nm and 180 nm) at 60 GHz.

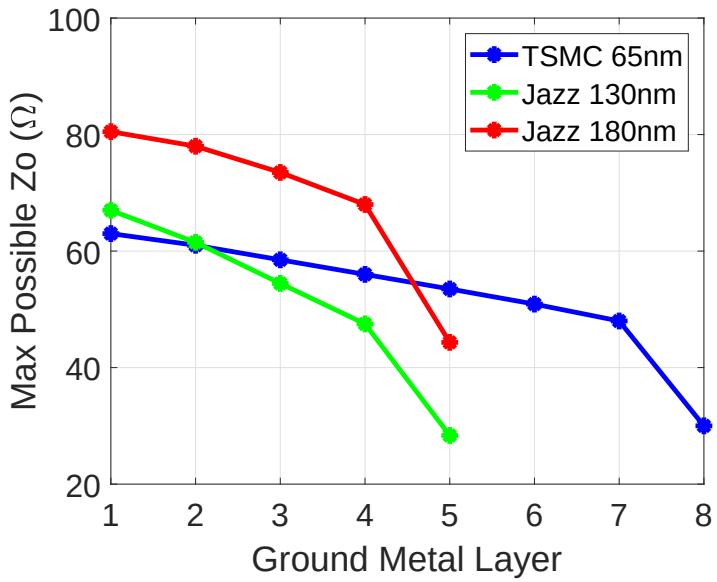

Figure 2.3: Maximal achievable characteristic impedance at 60 GHz in different processes.

To achieve the same characteristic impedance at a certain frequency, the structure

with lower ground metal layer should have a wider signal trace. As a consequence, the cross-section for current flow will be increased and resistance due to the signal trace will be reduced. However, in lower metallization layers, the thickness of the ground as well as the conductivity is usually decreased. This usually leads to an increase in resistance in the ground plane. To evaluate the performance of a microstrip with different ground layers, microstrip lines with different characteristic impedances are designed and simulated in EM simulator Q2D [45] for three different processes (i.e., TSMC 65 nm, TowerJazz (Jazz) 130 nm and 180 nm) at 60 GHz. For each process, M1 is the lowest layer producing the largest microstrip height. As illustrated in Figs. 2.4–2.6, when the ground plane moves closer to the signal line, the attenuation for microstrips designed with 40 Ω, 50 Ω and 60 Ω increases and the quality factor is reduced, while the variation in the phase constant, β, is below 5 %. The attenuation constant, α, and phase constant, β, are the real and imaginary part of the propagation constant, respectively [46], which is given by

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta \tag{2.1}$$

where R, L, G and C are the distributed series resistance, series inductance, shunt conductance and capacitance, respectively [46], and ω is the angular frequency. The quality factor (Q) is [46]

$$Q = \frac{\beta}{2\alpha} \tag{2.2}$$

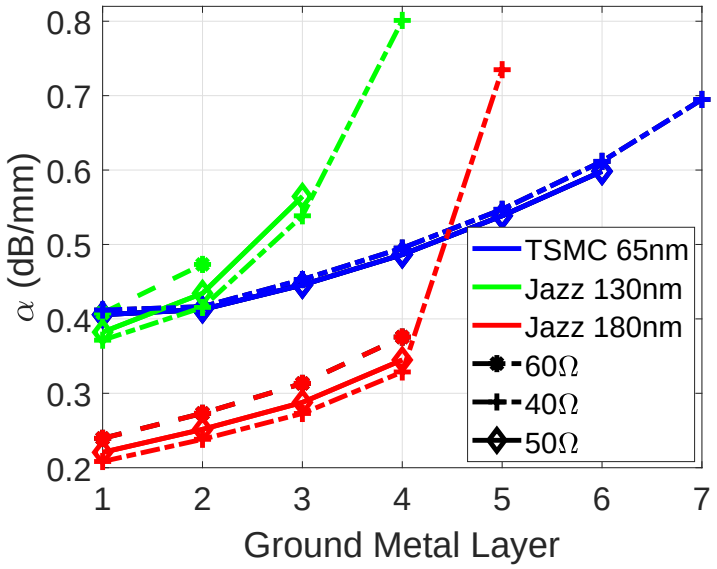

Figure 2.4: Attenuation constant of a microstrip due to conductor skin and proximity effects in three different processes at 60 GHz.

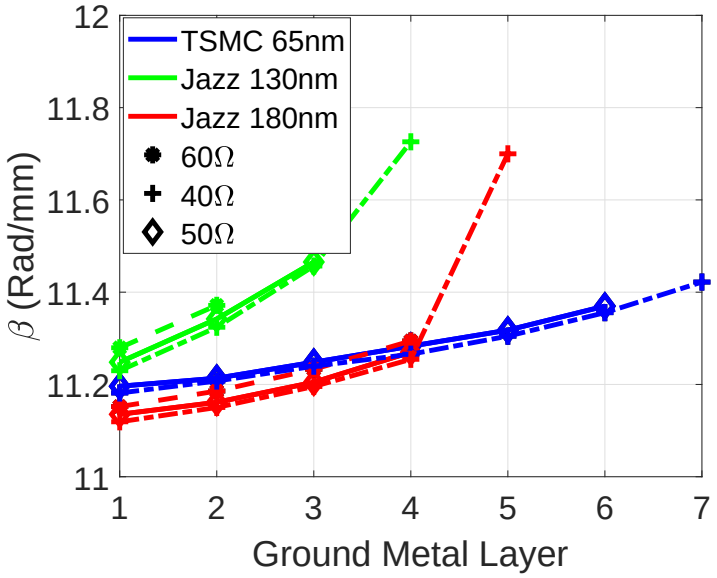

Figure 2.5: Phase constant of a microstrip in three different processes at 60 GHz.

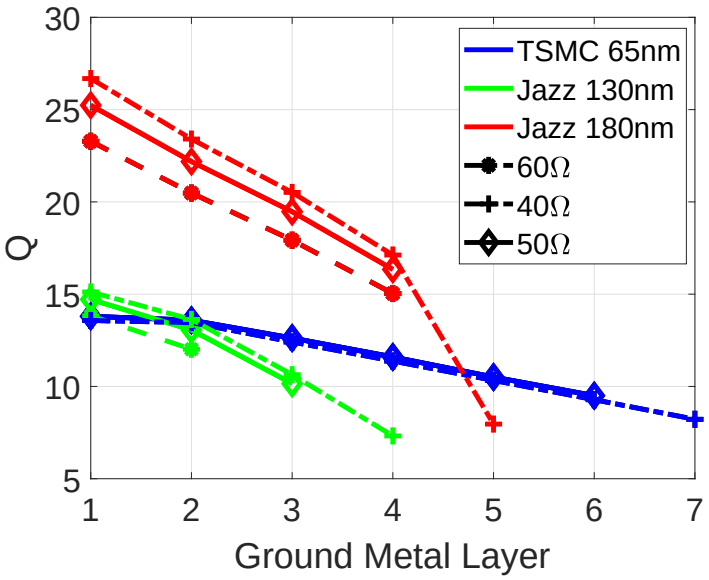

Figure 2.6: Quality factor of a microstrip in three different processes at 60 GHz.

2.3 Design Considerations for On-Chip CPWs

When designing a transmission line with a certain characteristic impedance, CPW is superior to microstrip in controlling the characteristic impedance and achieving high impedance [47]. On the one hand, CPW provides more degrees of freedom (i.e., width of signal line, gap and ground width) compared with microstrip, which enables having different structures with the same characteristic impedance. On the other hand, without a ground metal layer underneath, the magnetic field is not shielded or confined, making a high characteristic impedance easily achievable by enlarging the gap between signal line and the top ground lines.

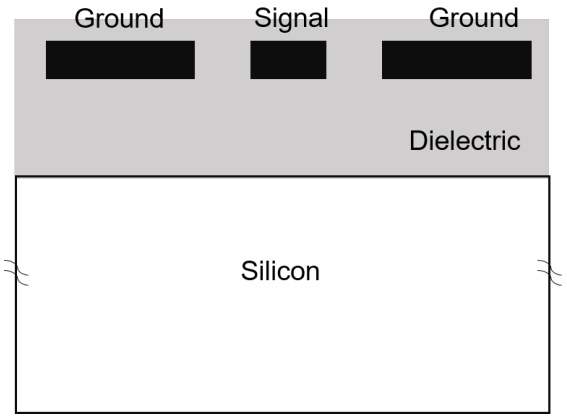

Figure 2.7: On-chip CPW structure.

For CPW, in addition to conductor losses, substrate losses should also be taken into consideration if no ground plane is underneath. Therefore, for optimum design, there is a trade-off between conductor losses and substrate losses. As illustrated in Fig. 2.8, for a given characteristic impedance and assuming the ground conductor width is fixed, a large width of the signal line can decrease conductor loss, but the gap between the signal and ground lines will also be increased to maintain the same impedance. As a result, the field confinement decreases and, hence substrate loss increases. For example, CPW structures with a wide range of signal width and gap are designed in TowerJazz 130 nm RFCMOS and Jazz 180 nm BiCMOS processes. These structures have been simulated in the commercial simulator Q2D [45] from ANSYS. The quality factor and characteristic impedance are plotted in Figs. 2.9 and Fig. 2.10 for the two processes at 60 GHz.

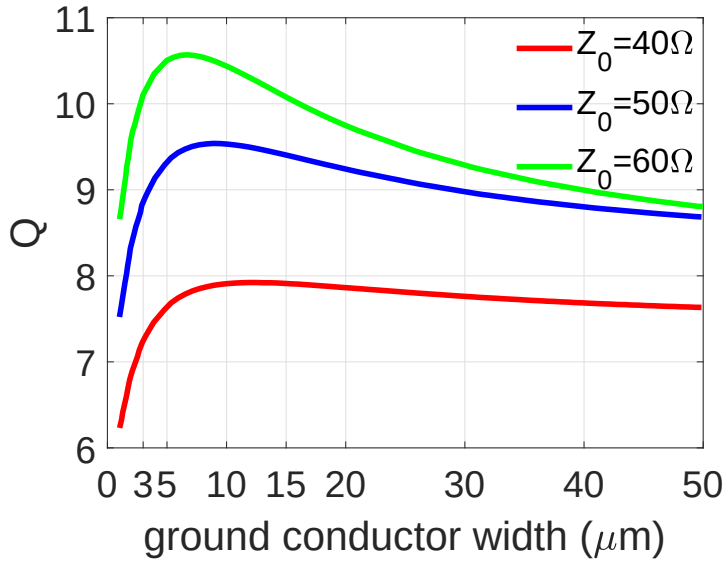

Figure 2.8: Variation of Q for various ground conductor widths, assuming the signal conductor width is fixed.

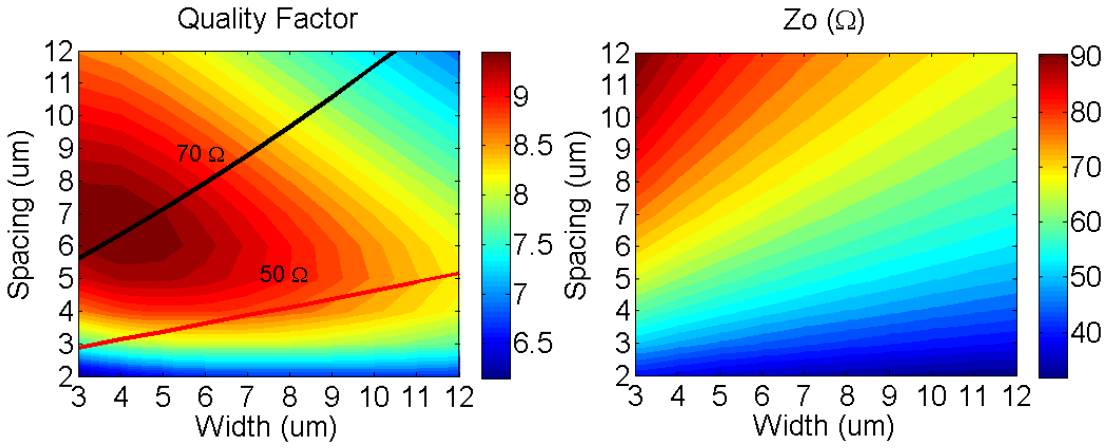

Figure 2.9: Line quality factor and characteristic impedance for different sets of widths and gaps (spacings) in example TowerJazz 130 nm RFCMOS process. Frequency is 60 GHz. Red and black solid lines correspond to 50 Ω and 70 Ω lines, respectively.

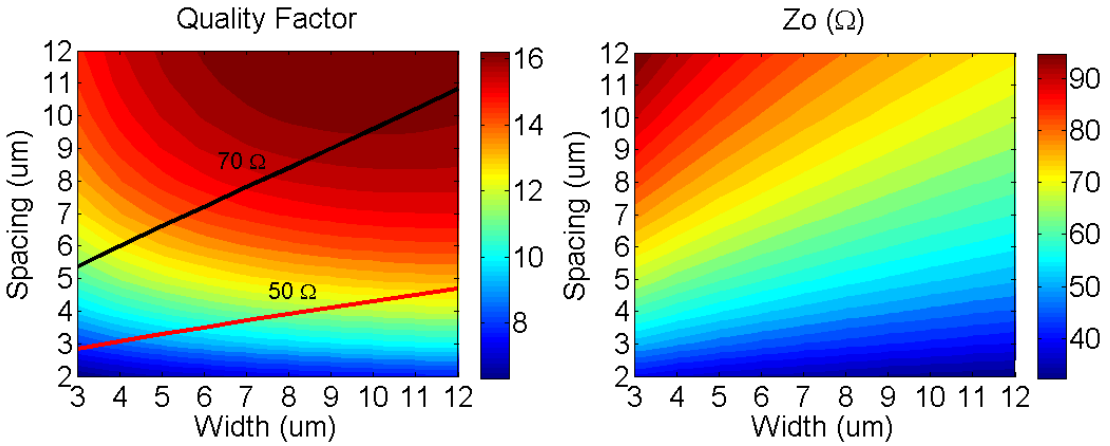

Figure 2.10: Line quality factor and characteristic impedance for different sets of widths and gaps (spacings) in example TowerJazz 180 nm BiCMOS process. Frequency is 60 GHz. Red and black solid lines correspond to 50 Ω and 70 Ω lines, respectively.

2.4 Modeling Challenges and Approaches in Literature

The transmission line characteristics in general depend on a large number of geometrical parameters. Taking an on-chip microstrip as an example, as is illustrated in Fig. 2.11, the per-unit-length R, L, G, C parameters are functions of geometrical parameters (i.e., signal conductor width (w_s), thickness (t_s) and height (h); ground conductor width (w_g), thickness (t_g)) and material property parameters (i.e., conductivity (σ_s, σ_g) of each metal layer, inter-layer dielectric constant (ϵ)), as well as frequency (f). This makes the development of a fully scalable compact model virtually impossible.

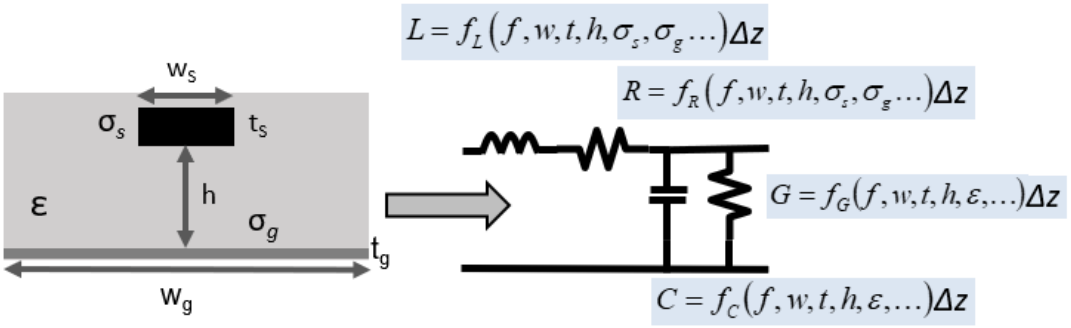

Figure 2.11: Left: microstrip cross-section; Right: $RLGC$ model (Fig. 1.5) of microstrip for a short section length Δz, per-unit-length R, L, G, C parameters are functions of geometrical and material parameters as well as frequency.

The difficulty in scalable modeling for on-chip transmission lines is to capture the frequency-dependent characteristics, which are the per-unit-length series impedance (i.e., resistance and inductance) and the per-unit-length shunt admittance (i.e., capacitance and conductance). For mixed-signal and RF silicon technology with highly resistive silicon substrates [24], the frequency-dependent series impedance at high frequencies is mainly due to the skin and proximity effects in or between conductors. To model the frequency-dependent series resistance and inductance due to the conductors, Kim and Neikirk [48] proposed an RL ladder network to capture the total p.u.l. resistance and the change in p.u.l. inductance for a single round wire. The rules for determining the circuit element values were also discussed. They also extended the model to twin lead and coaxial lines where proximity effects were considered. Unlike round conductors, on-chip interconnects usually are rectangular metal bars or planes where analytical solutions can not be derived rigorously as for round conductors. To address this issue, empirical formulas fitted from optimization tools are preferred. For example, Shi et al. [49] have developed a scalable model for on-chip CPWs, in which a parallel RL network and a parallel CG network are adopted to capture frequency-dependent series impedance and shunt admittance. To determine the circuit element values, empirical formulas were fitted through a customized optimization algorithm. However, the model is not fully scalable and the formulas are only valid for one specific process since only width and length are varied and other process-dependent physical parameters (e.g., metal layer thickness,

metal conductivity, silicon conductivity and so on) are fixed. In other words, with too many parameters involved, it is prohibitive to develop the formulas for the circuit element values directly. Kang et al. [50] established a fully scalable equivalent circuit model for on-chip CPWs up to 110 GHz. A well-developed technique named PEEC (e.g., [51]) was used to extract high-frequency inductance and resistance. However, the PEEC technique involves meshing of the conductors and sparse matrix calculation. At such high frequencies, the skin depth is fairly small when compared with the geometry. To achieve better accuracy, finer mesh elements are always desired, and that leads to a large number of mesh elements, which requires a large amount of computational resources. In addition, matrix calculations make the model inconvenient to be incorporated into circuit simulators (e.g., SPICE, SPECTRE and ADS). Also, matching impedance only at low and high frequency points does not necessarily guarantee a good fit in the transition region from low to high frequencies. Shu et al. [52] attempted to model the series impedance by using the phenomenological loss equivalence method (PEM) [53]. Only the skin effect in the center conductor was calculated while the model did not take the proximity effects and ground conductor loss into consideration. Since the ground conductors play a role in total p.u.l. resistance and inductance, neglecting the ground effects leads to inaccuracy in model performance.

2.5 Overview of Proposed Scalable Modeling Approach

To model the frequency-dependent resistance and inductance for on-chip microstrips and CPWs, we have proposed a systematic scalable modeling approach based on the Principle of Electromagnetic Similitude [54] and the Foster network [55] synthesis. To explain the modeling technique, we take an isolated conductor as an example. As illustrated in the upper left panel of Fig. 2.12, the change of resistance and inductance due to the skin effect is a function of four variables, i.e.,

$$\Delta R = h_R(f, w, t, \sigma) \tag{2.3}$$

$$\Delta L = h_L(f, w, t, \sigma). \tag{2.4}$$

After applying the Principle of Electromagnetic Similitude (upper right panel of Fig. 2.12), the number of variables is reduced to two variables (i.e., w/t, p) and ΔR and ΔL

can be expressed as

$$\Delta R = R_{\rm dc} f_R\left(\frac{w}{t}, p\right) \tag{2.5}$$

$$\Delta L = f_L\left(\frac{w}{t}, p\right). \tag{2.6}$$

In (2.5), $R_{\rm dc}$ is the DC resistance. Variable $p = wt/\delta^2 = wt\sigma\mu_0\pi f$ is the normalized frequency [56], where δ is the skin depth defined as $\delta = 1/\sqrt{\pi f \mu_0 \sigma}$, μ_0 and σ are the permeability and conductivity of the conductor, respectively, and f is the operating frequency. Furthermore, as shown in the lower right panel of Fig. 2.12, we synthesize a Forster network (Fig. 2.13) to capture the frequency-dependency in R and L, which eliminates the normalized frequency p. The resistance and inductance elements in the network are frequency-independent. They are functions of only normalized geometrical parameters. The development of functions $f_R()$ and $f_L()$ will be discussed in the following sections. The number of RL sections can also be increased to achieve better accuracy and larger bandwidth, which will be discussed later. For on-chip microstrips and CPWs, in addition to the aforementioned techniques, we also developed systematic approaches to reduce the complexity of the problem. These techniques will be discussed in the following sections.

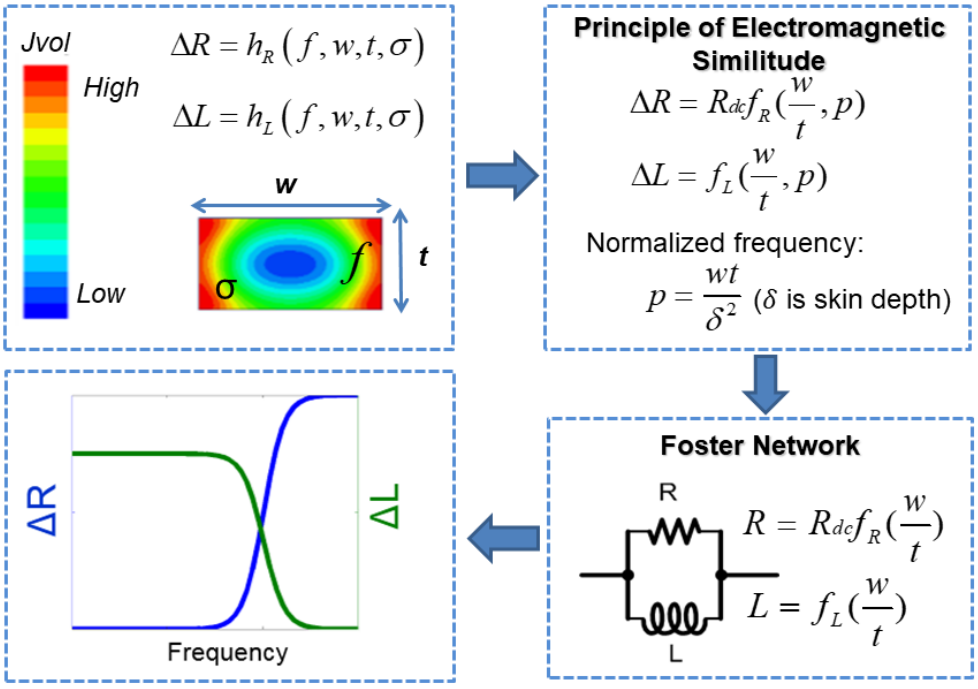

Figure 2.12: Overview of proposed scalable modeling approach.

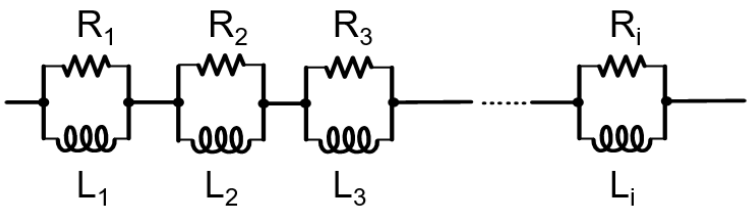

Figure 2.13: A generic RL Foster network.

2.6 Scalable Modeling Approach for On-Chip Microstrips

2.6.1 Approach Overview

To make the development of a scalable model for on-chip microstrips feasible, the complexity of the problem needs to be reduced. To model the shunt C parameter, G can be

ignored since the loss tangent of the silicon oxide is negligible and the silicon substrate is shielded by a sufficiently wide ground plane. This guarantees that C remains frequency independent. For the frequency-dependent resistance and inductance parameter, we have proposed an approach by modeling the change in resistance and inductance for signal and ground conductor separately while considering their mutual influence due to proximity effects in a simplified manner [57] (Fig. 2.14).

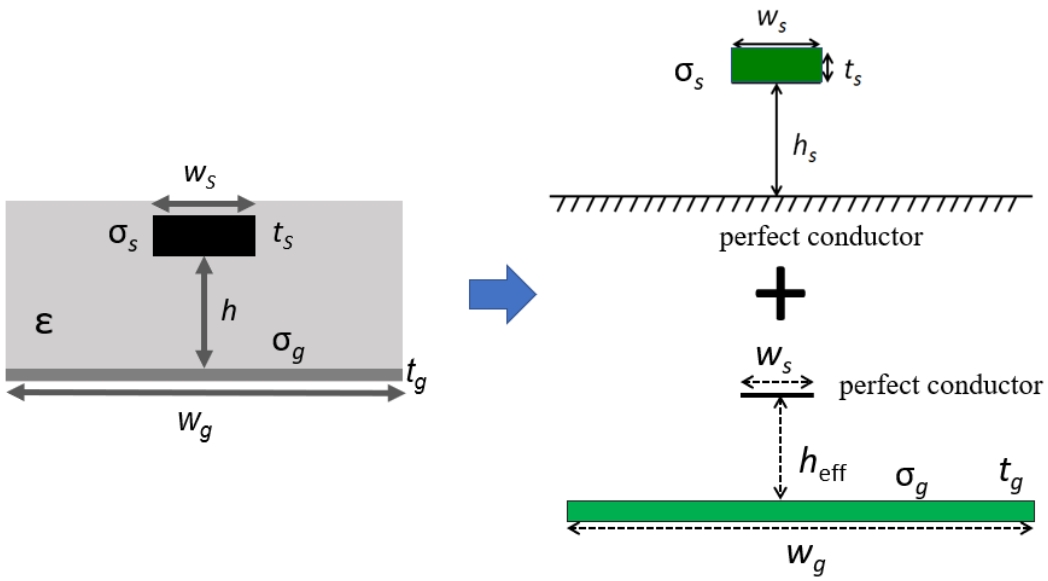

Figure 2.14: Reduction of problem complexity by separating the signal and ground conductor losses while considering mutual effects.

This leads to the network decomposition for the R, L parameters into two networks representing the change in R and L for the signal conductor and the ground conductor, both in the presence of the other conductor, as illustrated in Fig. 2.15. The high frequency inductance L_∞ and total DC resistance R_{dc} parameters are represented separately. We further reduce the number of parameters by assuming a perfect ground conductor of infinite width and conductivity when analyzing the losses in the signal conductor. This simplification has negligible influence on the signal conductor characteristics but leads to a reduction by three parameters associated with the ground conductor on the signal series impedance. Similarly, for modeling the ground conductor characteristics, the sig-

nal conductor is assumed to be a perfect conductor of zero thickness. Each ΔR, ΔL sub-network is a function of several geometrical parameters, conductivity and frequency. As a final step, we develop scalable compact models for each sub-network and combine them as illustrated in Fig. 2.15 to obtain a complete scalable compact model for on-chip microstrips.

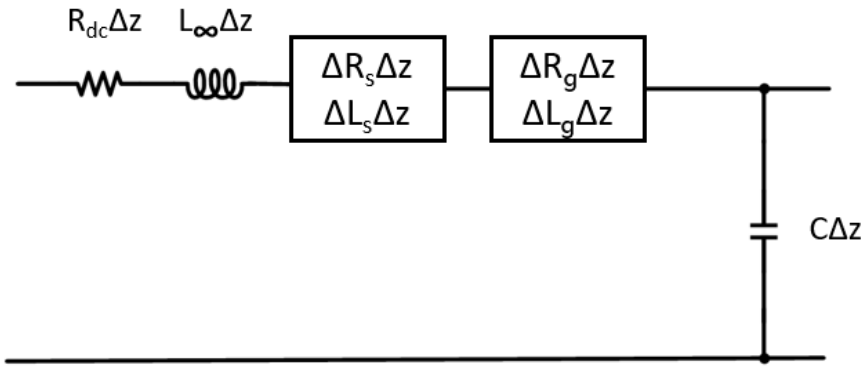

Figure 2.15: Network decomposition model for a short section of microstrip of length Δz.

2.6.2 RL network for Signal Conductor

The increase in resistance and decrease in inductance for the microstrip signal line in the presence of a perfect ground plane (Fig. 2.16) are both due to the skin and proximity effects in the signal conductor. In this case, resistance and inductance are functions of five parameters (w_s, t_s, h_s, and σ_s, and frequency f), which can be expressed as

$$\Delta R_s = G_R\Big(w_s, t_s, h_s, t_s, f\Big) \tag{2.7}$$

$$\Delta L_s = G_L\Big(w_s, t_s, h_s, t_s, f\Big). \tag{2.8}$$

With many parameters, it is prohibitive to develop empirical formulas for $G_R()$ and $G_L()$. To decrease the complexity further, we apply the Principle of Electromagnetic Similitude to reduce the number of independent parameters, as discussed in Section 2.5.

The change in per-unit-length resistance ΔR_s and inductance ΔL_s for the microstrip signal conductor is expressed in functional form with normalized variables as

$$\Delta R_s = R_{\rm dc} G_R\left(\frac{w_s}{t_s}, \frac{h_s}{t_s}, p\right) \tag{2.9}$$

$$\Delta L_s = G_L\left(\frac{w_s}{t_s}, \frac{h_s}{t_s}, p\right), \tag{2.10}$$

where $R_{\rm dc} = 1/(w_s t_s \sigma_s)$. As a further step, the normalized frequency parameter p can be eliminated by synthesizing the ΔR_s, ΔL_s sub-network as a Foster network, as illustrated in Fig. 2.17. By equating the functional form for the ΔR_s, ΔL_s sub-network with the individual elements $R_{\rm si}$, $L_{\rm si}$ of the Foster network, it can be shown that the elements $R_{\rm si}$, $L_{\rm si}$ are simply functions of the two parameters, w_t/t_s and h_s/t_s, and DC resistance $R_{\rm dc}$. Thus, the frequency dependence of ΔR_s, ΔL_s is captured by the Foster network.

$$R_{\rm si} = R_{\rm dc} F_R\left(\frac{w_s}{t_s}, \frac{h_s}{t_s}\right) \tag{2.11}$$

$$L_{\rm si} = F_L\left(\frac{w_s}{t_s}, \frac{h_s}{t_s}\right). \tag{2.12}$$

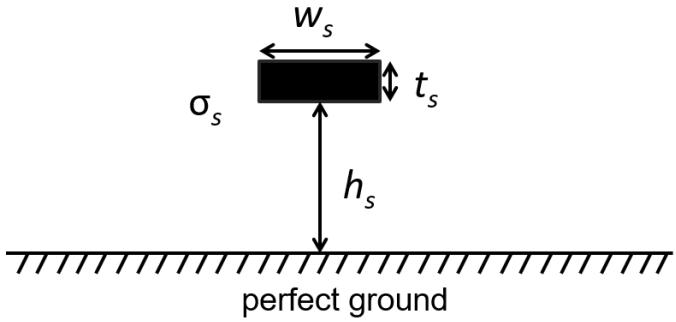

Figure 2.16: Microstrip with perfect ground plane, used for modeling the frequency-dependent signal series impedance.

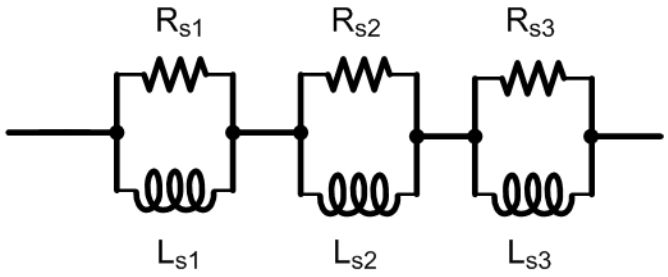

Figure 2.17: RL Foster network for scalable compact modeling of the signal conductor.

To obtain empirical approximations to the functions F_R and F_L, as shown in Fig. 2.18, we first performed extensive quasi-magnetostatic simulations over a wide range of values for w_s/t_s and h_s/t_s to cover practical dimensions for a broad range of process technologies and process nodes. This is achieved by varying w_s and h_s while remaining t_s and σ_s the constant and performing the simulation over a frequency range from DC to an upper frequency $f_{\max}$ (400 GHz). Each discrete set of w_s/t_s and h_s/t_s corresponds to simulated ΔRs and ΔLs over the frequency range of interest. Then, we used a customized Genetic Algorithm [58] to determine the values for each R and L element ($R_{\rm si}$ and $L_{\rm si}$) in the equivalent RL circuit model to obtain the best approximation to the response for both ΔR_s and ΔL_s. Now, we have the equivalent RL circuit models ($R_{\rm si}$ and $L_{\rm si}$) for discrete w_s/t_s and h_s/t_s values. To make the model useful for continuous geometry ranges, the last step is to fit suitable empirical expressions to each element ($R_{\rm si}$ and $L_{\rm si}$) over the 2D parameter space (w_s/t_s and h_s/t_s). The empirical expressions for the resistance parameter $R_{\rm si}$ (i=1,2,3) are of the form

$$R_{\rm si} = \frac{\sigma_o}{\sigma_s}\left(\frac{t_o}{t_s}\right)^2 R_{\rm oi}\left(\frac{w_s}{t_s}, \frac{h_s}{t_s}\right), \tag{2.13}$$

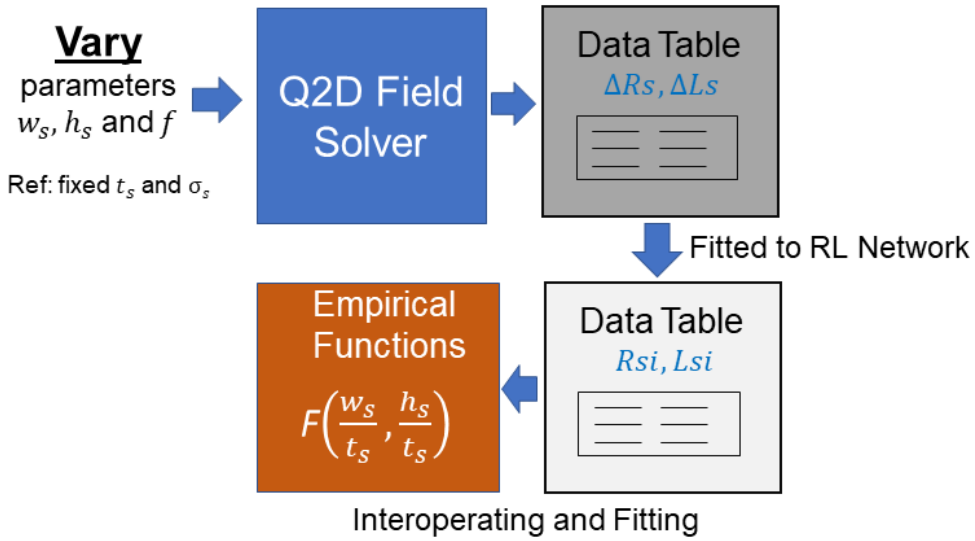

Figure 2.18: Flow diagram of our proposed scalable modeling method.

where we have assumed $t_o = 1\ \mu m$ and $\sigma_o = 6{\times}10^7$ S/m as reference values. The formulas for $R_{\rm oi}(\frac{w_s}{t_s}, \frac{h_s}{t_s})$ are given in Appendix A.1. To determine the inductance parameters $L_{\rm si}$ (i=1, 2, 3) for the signal conductor, we first fit an empirical expression to the pole $p_{\rm oi}$ of each $R_{\rm si}$, $L_{\rm si}$ section of the Foster network. The formulas for $p_{\rm oi}(\frac{w_s}{t_s}, \frac{h_s}{t_s})$ are also provided in Appendix A.1. The $L_{\rm si}$ parameters are given by

$$L_{\rm si} = \frac{R_{\rm oi}\left(\frac{w_s}{t_s}, \frac{h_s}{t_s}\right)}{p_{\rm oi}\left(\frac{w_s}{t_s}, \frac{h_s}{t_s}\right)}. \tag{2.14}$$

To validate our model for the signal conductor, we compared our method for an example microstrip designed in a BiCMOS 180 nm TowerJazz process. The signal conductor is on M6 (top metal) and the width is 6 μm. The ground conductor is on M3, which is assumed perfect. These preliminary results compare the results obtained with the commercially available quasi-electrostatic solver Q2D [45] to our techniques.

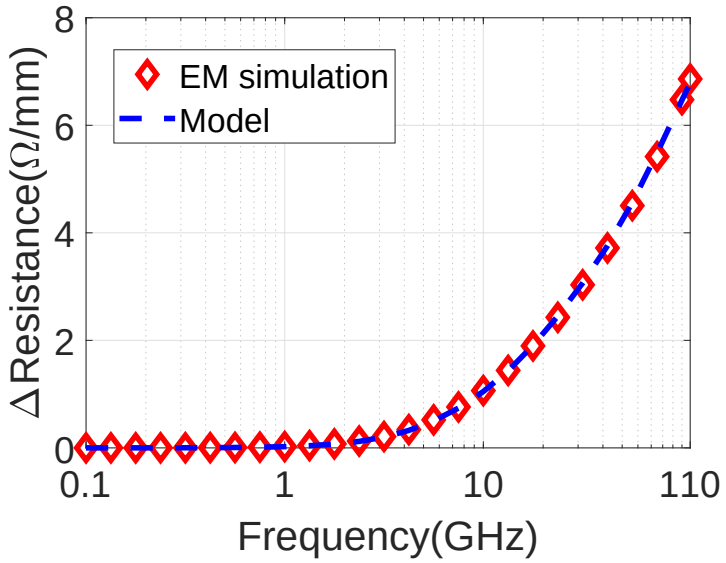

Figure 2.19: Change in per-unit-length resistance for signal conductor up to 110 GHz.

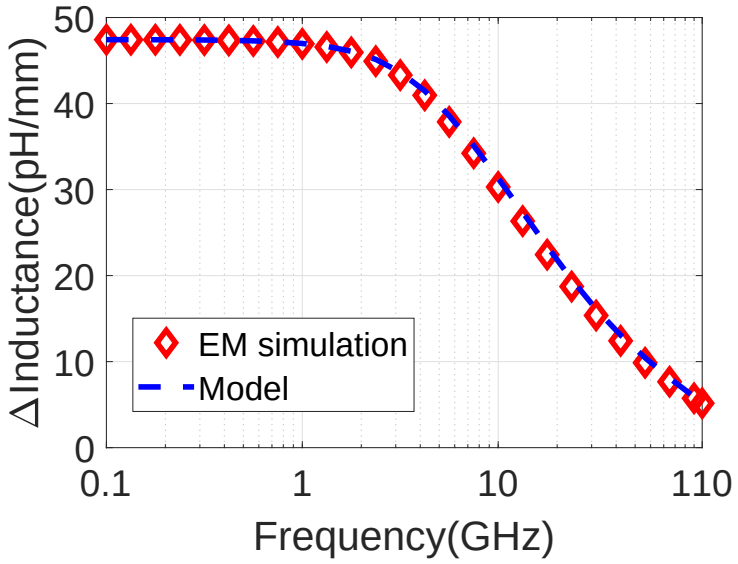

Figure 2.20: Change in per-unit-length inductance for signal conductor up to 110 GHz.

2.6.3 RL network for Ground Conductor

Similar to the signal conductor, we apply a parameter reduction approach to model the change in resistance ΔR_g and inductance ΔL_g corresponding to the ground conductor of the microstrip. The change in resistance and inductance due to the ground conductor in the presence of a signal conductor having infinite conductivity is a function of six parameters (i.e., ground and signal conductor width (w_s, w_g) and thickness (t_s, t_g), ground conductor conductivity (σ_g) and frequency (f)). To systematically reduce the number of parameters, we first assume an effective signal conductor of zero thickness and define an effective height $h_{\text{eff}} = h_s + t_s/2$, as shown in Fig. 2.21.

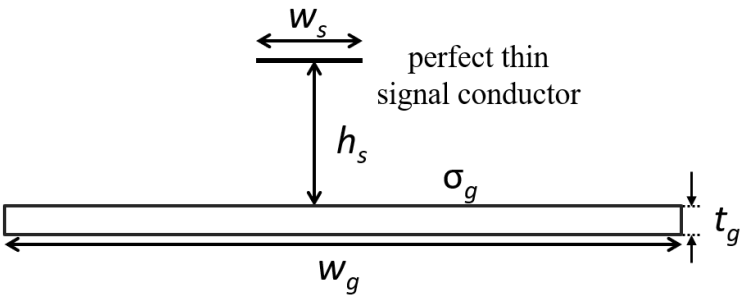

Figure 2.21: Microstrip with perfectly thin signal conductor, used for considering ground series impedance.

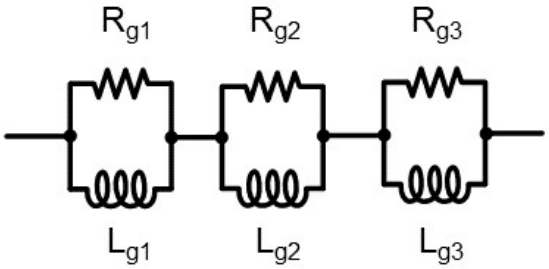

Figure 2.22: RL Foster network for scalable compact model of the ground conductor.

However, we note that the width of the ground conductor affects the total change in inductance and, hence, cannot be neglected in the model. Thus, a total of five parameters are included in the model: the widths of signal and ground conductors (w_s, w_g), the effective signal line height (h_{eff}), the ground conductor thickness (t_g) and the conductivity of ground metal layer (σ_g). To further reduce the complexity of this problem, we note from [59] that the width of the ground conductor does not affect the critical frequency of the frequency-dependent inductance if $w_g > w_s + 6(h_s + t)$ where t is the maximal thickness of the signal and ground conductors. This implies that the poles in the RL Foster network corresponding to the ground conductor (Fig. 2.22) can be assumed to be independent of the ground conductor width for $w_g > w_s + 6(h_s + t)$. Furthermore, with increasing frequency when the skin and proximity effects are well developed, the current distribution in the ground plane is concentrated close to the surface of the ground conductor underneath the signal conductor. Therefore, the ground conductor width can be ignored for modeling the high frequency resistance and inductance. Thus, similar to modeling the signal conductor, the problem is reduced to four parameters, and similitude combined with a Foster network synthesis can be effectively applied to further reduce the problem to two parameters (i.e., w_s/h_{eff}, t_g/h_{eff}) for the elements R_{gi}, L_{gi} of the Foster network shown in Fig. 2.22 together with a simple scaling factor with respect to a reference design. The empirical expressions for the resistance parameters R_{gi} (i=1, 2, 3) are given as

$$R_{\text{gi}}\left(\frac{w_s}{h_{\text{eff}}}, \frac{t_g}{h_{\text{eff}}}\right) = \frac{\sigma_{\text{o1}}}{\sigma_g}\left(\frac{h_o}{h_{\text{eff}}}\right)^2 R_i\left(\frac{w_s}{h_{\text{eff}}}, \frac{t_g}{h_{\text{eff}}}\right), \tag{2.15}$$

where the factor $\frac{\sigma_{\text{o1}}}{\sigma_g}\left(\frac{h_o}{h_{\text{eff}}}\right)^2$ is a scaling factor relative to a reference design with $h_o = 10\ \mu m$ and $\sigma_{\text{o1}} = 5.8 \times 10^7$ S/m. The values of the first two inductance elements ($L_{\text{gi}}(\frac{w_s}{h_{\text{eff}}}, \frac{t_g}{h_{\text{eff}}})$, i=1, 2) in Fig. 2.22 are obtained through the relationship with the RL network's pole as $R_i = p_i L_{\text{gi}}$ (i= 1, 2) together with resistance elements $R_i(\frac{w_s}{h_{\text{eff}}}, \frac{t_g}{h_{\text{eff}}})$($i$=1, 2), which are all given in Appendix A.1. The third inductance element is obtained by enforcing the correct DC inductance of the total network of Fig. 2.15.

$$L_{\text{g3}} = L_{\text{dc}} - L_{\infty} - \sum_{i=1}^{3} L_{\text{si}} - \sum_{i=1}^{2} L_{\text{gi}} \tag{2.16}$$

An analytical formula for $L_{\rm dc}$ of the microstrip is available in [60]. The capacitance formulas in [59] are used to calculate the inductance per unit length in the high frequency limit, L_∞, as $L_\infty = 1/(c_o^2 C_{air})$, where c_o is the speed of light in a vacuum and $C_{\rm air}$ is the capacitance per unit length with air dielectric. We obtain $R_{\rm g3}$ through the relationship with the RL network's pole as $R_3 = p_3 L_{\rm g3}$. The empirical expression p_3 is given in Appendix A.1. To validate our model for the ground conductor, a microstrip designed in a BiCMOS 0.18 μm TowerJazz process is compared with a commercial EM field solver [45]. The signal conductor is on M6 (top metal), which is assumed perfect with zero thickness. The width is 6 μm and the ground conductor is on M3 with a width of 300 μm. Figure 2.23 and 2.24 show a comparison between our scalable model with the EM simulation, which are in good agreement.

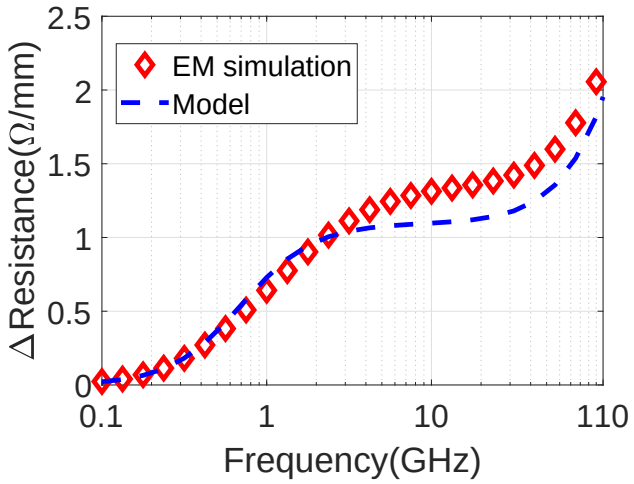

Figure 2.23: Change in per-unit-length resistance for the ground conductor up to 110 GHz.

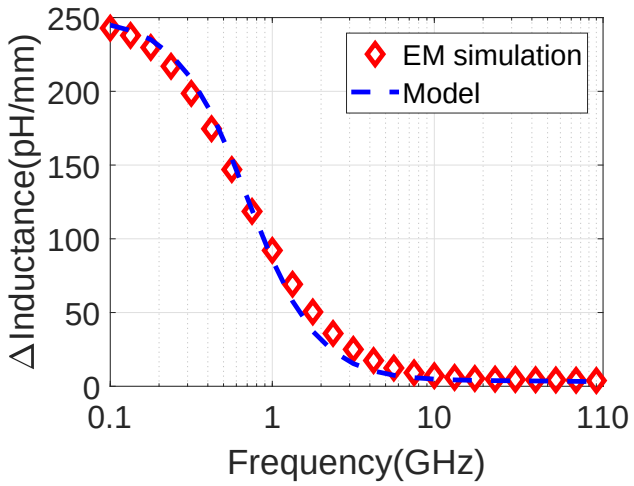

Figure 2.24: Change in per-unit-length inductance for the ground conductor up to 110 GHz.

2.7 Model Validation for On-Chip Microstrip

Figure 2.25 shows the complete scalable equivalent circuit model for a short section of microstrip of length Δz (Fig. 2.26). Similar to the circuit topology shown in Fig. 2.15, the two Foster networks representing the change in resistance and inductance (ΔR, ΔL) corresponding to the signal and ground conductors are cascaded and augmented by the DC resistance $R_{\rm dc}\Delta z$ and the inductance in the high frequency limit, $L_\infty \Delta z$, as well as shunt capacitance $C\Delta z$. The total DC resistance per unit length of the microstrip, including the signal and ground conductors is given by $R_{\rm dc} = 1/(\sigma_s w_s t_s) + 1/(\sigma_g w_g t_g)$. The capacitance formulas in [59] are adopted to calculate the effective permittivity $\epsilon_{\rm eff}$ and the shunt capacitance per unit length $C_{\rm air}$ with air dielectric. The accuracy of these formulas has been verified for a wide range of geometries and dielectric constants.

The effective bandwidth of the scalable model depends on the specific microstrip parameters and the reference design as [57]

$$\text{Bandwidth} = min\left(\frac{\sigma_o}{\sigma_s}\left(\frac{t_o}{t_s}\right)^2, \frac{\sigma_{o1}}{\sigma_g}\left(\frac{h_o}{h_{\rm eff}}\right)^2\right) f_{\rm max}, \tag{2.17}$$

where the reference design with $t_o = 1\ \mu m$, $h_o = 10\ \mu m$, $\sigma_o = 6 \times 10^7$ S/m, and

$\sigma_{o1} = 5.8 \times 10^7$ S/m has been modeled up to the frequency $f_{max} = 400$ GHz.

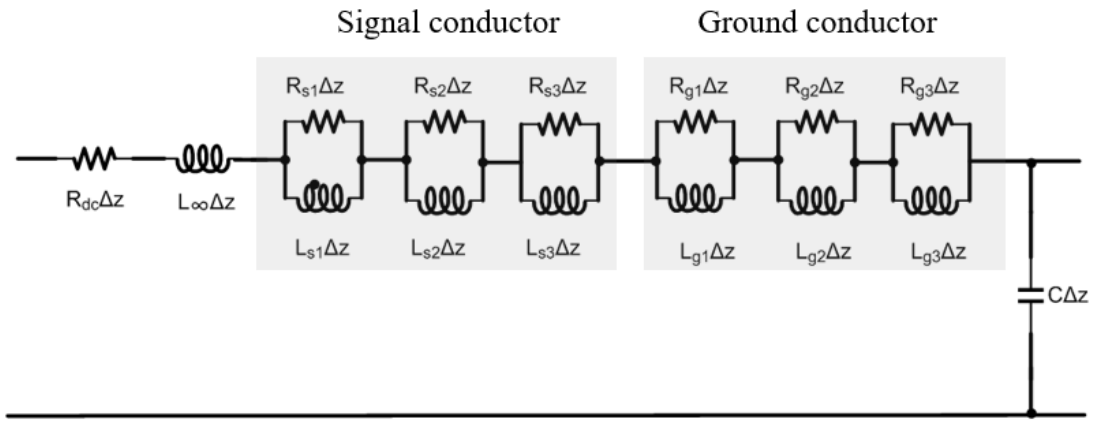

Figure 2.25: Compact scalable broadband model for a short section of on-chip microstrip of length Δz.

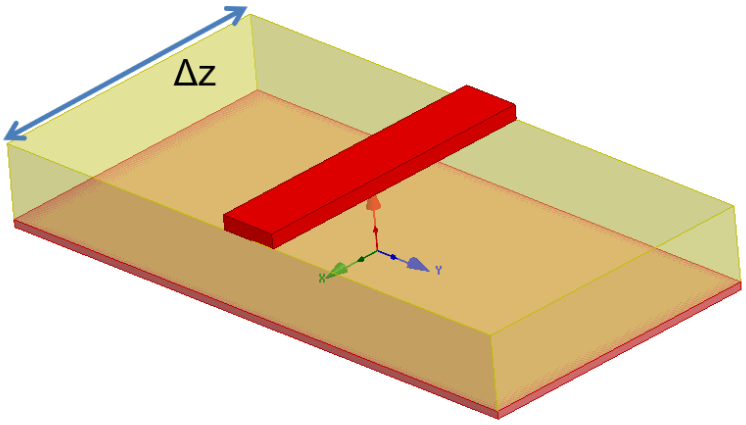

Figure 2.26: A short section of on-chip microstrip of length Δz.

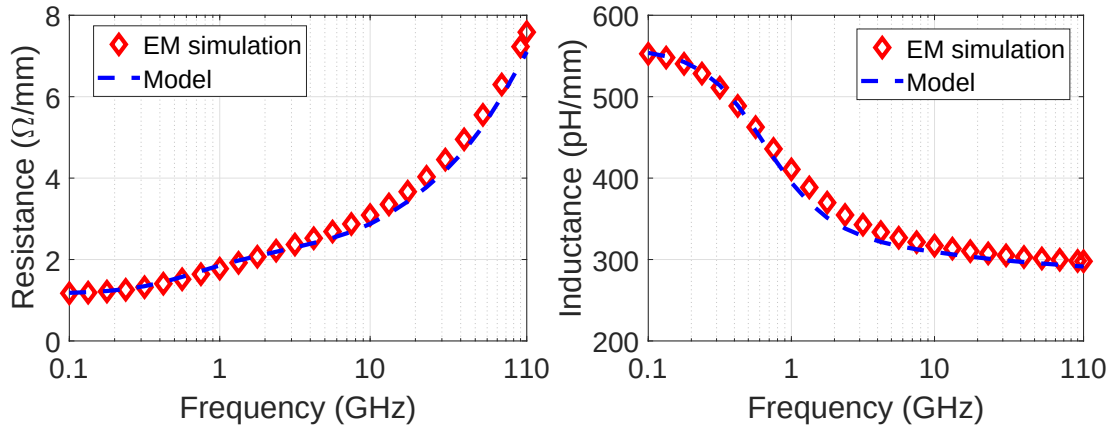

Figure 2.27: Frequency-dependence of per-unit-length resistance and inductance for a on-chip microstrip design up to 110 GHz, the signal conductor is 12 μm wide and is in M6 (top metal layer) and the ground conductor is 300 μm wide and is realized in M3.

We have compared our scalable model for the per-unit-length resistance and inductance parameters of the microstrip with the commercial field solver Q2D for a microstrip design in a BiCMOS 180 nm TowerJazz process (Fig. 2.27). A 50 Ω microstrip fabricated in a BiCMOS 180 nm TowerJazz process has also been measured. The comparison between the measurements and the model is shown in Fig. 2.28.

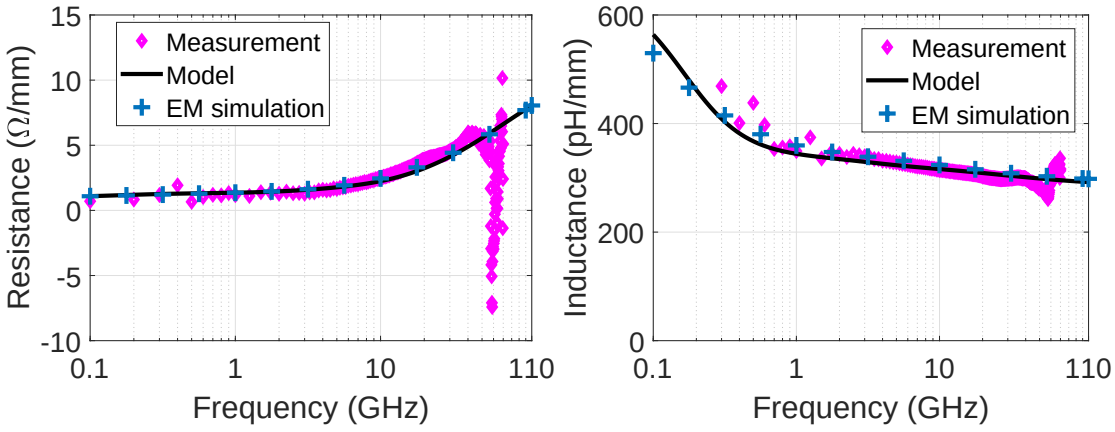

Figure 2.28: Comparison of per-unit-length resistance and inductance obtained with the broadband scalable model and measurements for a 50 Ω microstrip fabricated in a TowerJazz 180 nm BiCMOS process (signal line M6, ground M3).

The model is suitable for aluminum and copper processes with a wide range of normalized geometrical parameters, as listed in Tab. 2.1. Our model was verified with Q2D [45] to be accurate within 10% over the large parameter space. An example HSPICE netlist for microstrip is included in Appendix B.

Table 2.1: Suitable Normalized Geometrical Range

parameter	range
w_s/t_s	0.5-50
h_s/t_s	1-10
w_s/h_{eff}	0-10
t_g/h_{eff}	0.05-0.5

2.8 Scalable Modeling Approach for On-Chip CPWs

2.8.1 Problem Reduction

We have discussed that the challenges of scalable modeling for on-chip microstrip are due to the large number of parameters. This also applies for on-chip CPWs. Our model development focuses on the complicated frequency dependence of the series resistance and inductance due to skin and proximity effects in the conductors from DC up to the mmWave frequency range. For the shunt G, C parameters, suitable models and formulas are readily available (e.g., [61] and [62]). It is generally difficult to capture the frequency-dependent resistance and inductance parameters because of the presence of non-uniform current distributions along the conductor surfaces due to proximity effects, and the inadequacy of the traditional high-frequency surface impedance method for this situation.

As illustrated in Fig. 2.29, the per-unit-length resistance (R) and inductance (L) of a general on-chip CPW are functions of a large number of geometrical parameters (i.e., signal conductor width (w_s), ground conductor width (w_g), conductor thickness (t), and spacing (s)), material property parameters (conductivity (σ)), and the frequency of operation (f)). It is quite challenging to develop a fully scalable compact model with such a large number of parameters. To develop scalable models for the ideal elements of the circuit model in Fig. 2.30, and ultimately for the p.u.l. resistance and inductance param-

eters of a CPW, we first reduce the complexity of the problem by modeling the change in resistance and inductance in two different operating frequency regions [63], namely the 'DC to intermediate frequencies' region and the 'intermediate to high frequencies' region, where the skin and proximity effects are well developed. With this approach we can decompose the network for the p.u.l. resistance R and inductance L parameters into two sub-networks representing the change in R and L in these two regions, as illustrated in Fig. 2.30. Combined with the high frequency p.u.l. inductance L_∞ and the p.u.l. DC resistance $R_{\rm dc}$ parameters, a wideband equivalent circuit model for $R(f)$ and $L(f)$ of an on-chip CPW is obtained. In the next sections, we describe the development of suitable formulas for the circuit elements to make the model scalable with respect to geometrical and material property parameters.

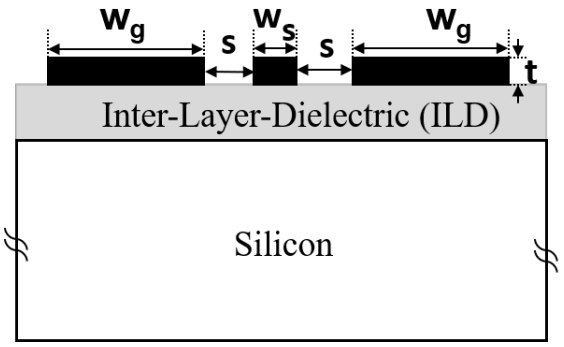

Figure 2.29: Geometry parameters for conductors of on-chip CPW.

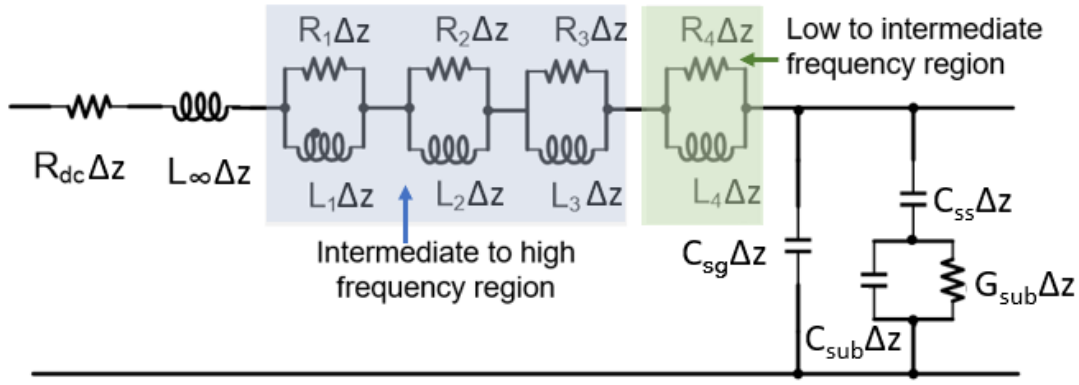

Figure 2.30: Compact broadband model for on-chip CPW for a short length of Δz.

2.8.2 Sub-Network for 'Intermediate to High Frequencies' Region

As for microstrips, the increase in resistance per-unit-length and decrease in inductance per-unit-length up to mmWave frequencies for on-chip CPWs on medium-to-high resistivity silicon substrate are primarily caused by the conductor skin and proximity effects. In this case, p.u.l. resistance and inductance depend on five parameters (w_s, t, s, w_g, σ, and operating frequency f). At sufficiently high operating frequencies, such that the skin and proximity effects are well developed, the currents in the ground conductors crowd at the inner edges close to the signal conductor, as illustrated in Fig. 2.31.

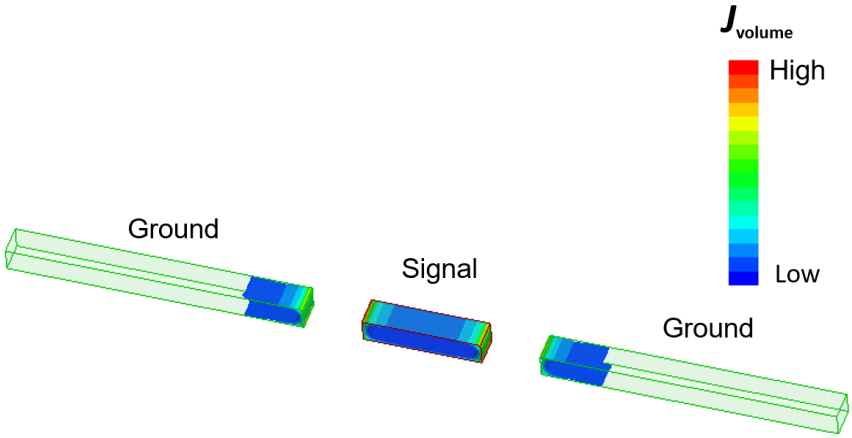

Figure 2.31: Volume current density in an on-chip CPW at 60 GHz.

In this case, the dependence on width of the ground conductors, w_g beyond a minimum width can be neglected in modeling high-frequency resistance and inductance. Applying the Principle of Electromagnetic Similitude, the change in resistance ΔR and inductance ΔL can be expressed in functional form as given below.

$$\Delta R = R_{\mathrm{dc}} G_R \left(\frac{w_s}{t}, \frac{s}{t}, p \right) \tag{2.18}$$

$$\Delta L = G_L \left(\frac{w_s}{t}, \frac{s}{t}, p \right) \tag{2.19}$$

$R_{\mathrm{dc}} = 1/(w_s t \sigma)$ is the p.u.l. DC resistance. Similar to the techniques presented in Section 2.6, a Foster network having elements R_i, L_i is matched to the functional form of the ΔR, ΔL subnetwork, where each of the elements R_i, L_i is only a function of two normalized parameters, w_s/t and s/t (as well as the signal conductor's DC resistance R_{dc} for R_i). The wideband frequency dependence is captured by the Foster network. We have found three RL sections to give sufficient accuracy over the chosen wide frequency and parameter range. For higher accuracy, the Foster network order can readily be increased. The elements of the three RL sections are given in functional form as

$$R_i = R_{\rm dc} F_R\left(\frac{w_s}{t}, \frac{s}{t}\right) (i = 1, 2, 3) \tag{2.20}$$

$$L_i = F_L\left(\frac{w_s}{t}, \frac{s}{t}\right) (i = 1, 2, 3) \tag{2.21}$$

Empirical forms of the functions $F_R(\,)$ and $F_L(\,)$ have been obtained by extensive magnetoquasistatic simulations for a wide range of values of w_s/t and s/t, encompassing practical dimensions for a broad range of process technologies and process nodes. A customized Genetic Algorithm was applied to obtain values for each R_i and L_i element, and suitable empirical expressions were then fitted to each element over the normalized parameter space. The empirical expressions for the resistance parameters R_i $(i = 1, 2, 3)$ are given as

$$R_i = \frac{\sigma_{\rm ref}}{\sigma}\left(\frac{t_{\rm ref}}{t}\right)^2 R_{0i}\left(\frac{w_s}{t}, \frac{s}{t}\right), \tag{2.22}$$

where $t_{\rm ref} = 4\ \mu m$ and $\sigma_{\rm ref} = 6 \times 10^7$ S/m are assumed as reference values. Formulas for $R_{0i}(w_s/t, s/t)$ are given in Appendix A.2. An empirical expression was fitted to the pole p_{0i} of each R_i, L_i section of the Foster network for determining the inductance parameter L_i $(i = 1, 2, 3)$. The formulas for $p_{0i}(w_s/t, s/t)$ are also provided in Appendix A.2. Then,

$$L_i = R_{0i}\left(\frac{w_s}{t}, \frac{s}{t}\right) \Big/ p_{0i}\left(\frac{w_s}{t}, \frac{s}{t}\right). \tag{2.23}$$

2.8.3 Sub-Network for 'Low to Intermediate Frequencies' Region

An additional RL section (R_4 and L_4) is used to capture the frequency-dependent resistance and inductance in the 'Low to intermediate frequencies' range. The inductance L_4 of the fourth section is obtained by enforcing the DC inductance of the overall circuit given in Fig. 2.30.

$$L_4 = L_{\rm dc} - L_\infty - \sum_{i=1}^{3} L_i \tag{2.24}$$

We obtain R_4 through the relationship with the fourth RL section's pole as

$$R_4 = \left(\frac{\sigma_{\text{ref}}}{\sigma}\right)\left(\frac{t_{\text{ref}}}{t}\right)^2 p_{04} \cdot L_4, \tag{2.25}$$

with $t_{\text{ref}} = 4\ \mu m$ and $\sigma_{\text{ref}} = 6 \times 10^7$ S/m as reference values. A suitable empirical expression for p_{04} is given in Appendix A.2. Closed-form formulas for the self and mutual inductances for linear conductors have been derived in [64], which are applied here to calculate the DC inductance of a CPW with finite ground width. An empirical capacitance formula (see Appendix A.2) was also developed to determine the inductance per-unit-length in the high frequency limit, L_∞, as $L_\infty = 1/(c_0^2 C_{\text{air}})$, where c_0 is the speed of light in vacuum and C_{air} is the capacitance per-unit-length with air dielectric.

2.9 Model Validation for On-Chip CPW

We have performed a comprehensive comparison of our scalable model with the quasi-static EM solver Q2D for the per-unit-length resistance and inductance parameters of a CPW for different designs. Figures 2.32 and 2.33 show representative results.

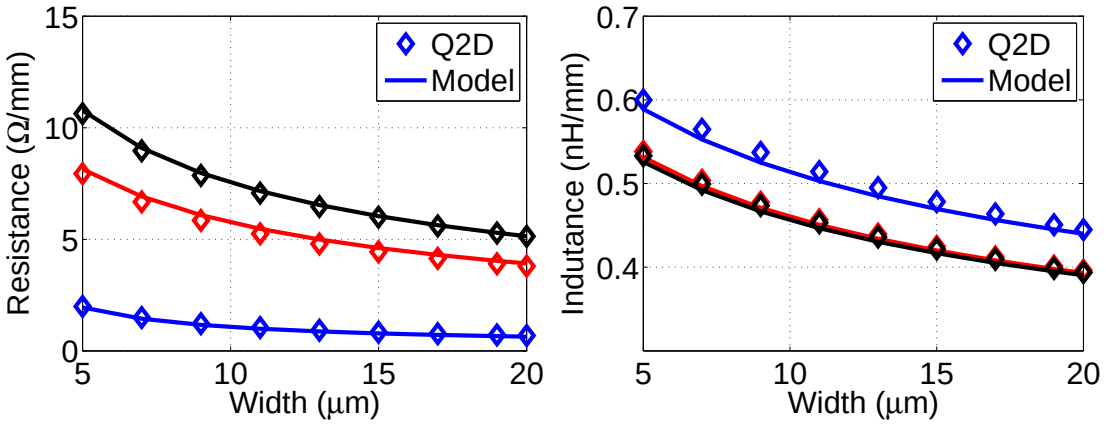

Figure 2.32: Comparison of per-unit-length resistance and inductance obtained with the scalable equivalent circuit model (Model) and EM solver Q2D as function of signal conductor width ($s = 15\ \mu$m, $t = 3\ \mu$m, $w_g = 150\ \mu$m, $\sigma = 3.8 \times 10^7$ S/m). Blue line and symbols are for 1 GHz, red line and symbols for 60 GHz, and black line and symbols for 110 GHz.

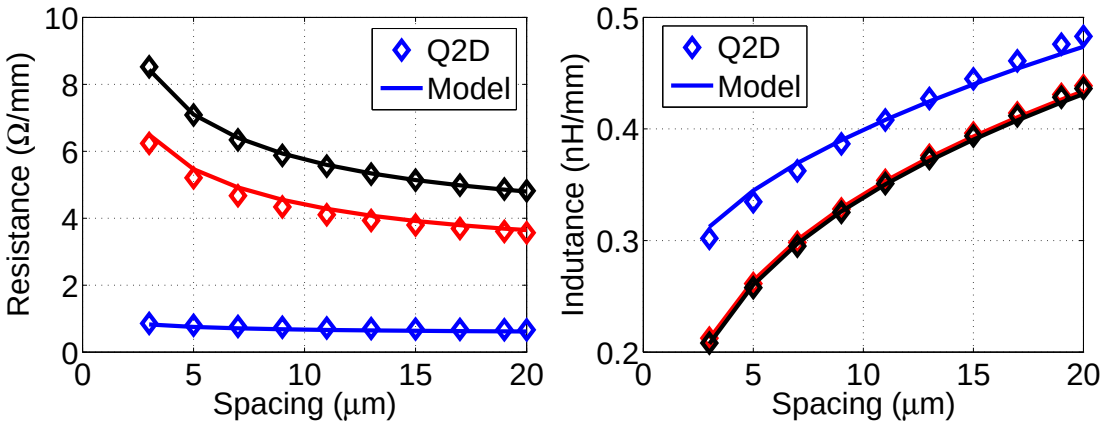

Figure 2.33: Comparison of per-unit-length resistance and inductance obtained with the scalable equivalent circuit model (Model) and EM solver Q2D as function of signal-to-ground conductor spacing ($w = 20$ μm, $t = 3$ μm, $w_g = 150$ μm, $\sigma = 3.8 \times 10^7$ S/m). Blue line and symbols are for 1 GHz, red line and symbols for 60 GHz, and black line and symbols for 110 GHz.

Furthermore, Fig. 2.34 shows a comparison of the frequency-dependent R and L parameters for a representative design with signal conductor width of 20 μm, conductor thickness of 3 μm, ground width of 200 μm, and conductor conductivity of 3×10^7 S/m. Also included in the figure are the results obtained with the mode-matching approach of [65]. Figure 2.35 shows a comparison of our model with the model in the IBM PDK library, as well full-wave simulation using HFSS [66]. In this case the widths of signal and ground conductor are 15 μm and the conductor spacing is 4 μm. The top metal layer in the IBM BiCMOS 8HP process was chosen in this design. When compared with the IBM PDK model [67], our model performs better in capturing the high frequency resistance.

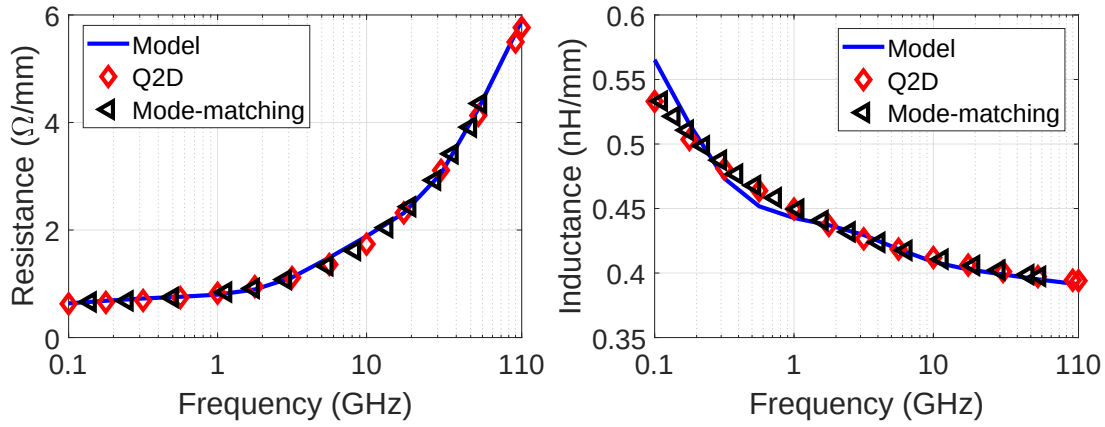

Figure 2.34: Comparison of per-unit-length resistance and inductance obtained with the scalable equivalent circuit model (Model), EM solver Q2D and the mode-matching method [65].

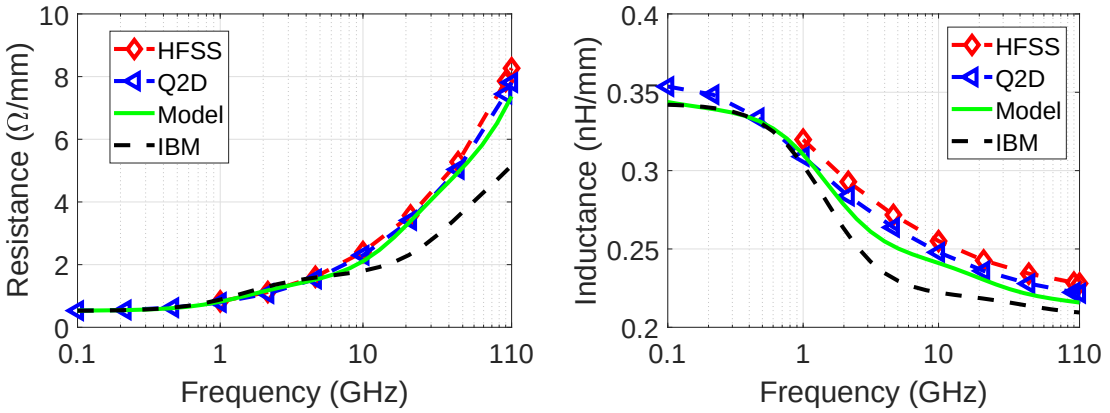

Figure 2.35: Comparison of per-unit-length resistance and inductance obtained with the scalable equivalent circuit model (Model), EM solver Q2D, HFSS and the IBM model from PDK library.

For the same design, we also compared the performance of our model with that in [52]. As illustrated in Fig. 2.36, the model in [52] underestimates the high frequency resistance. This is likely due to neglecting ground effects in the model. Likewise, the high frequency inductance is offset, which is probably caused by the assumption of negligible conductor thickness in the inductance calculation. In all cases our scalable model [68] is in good

agreement with the corresponding EM simulation results.

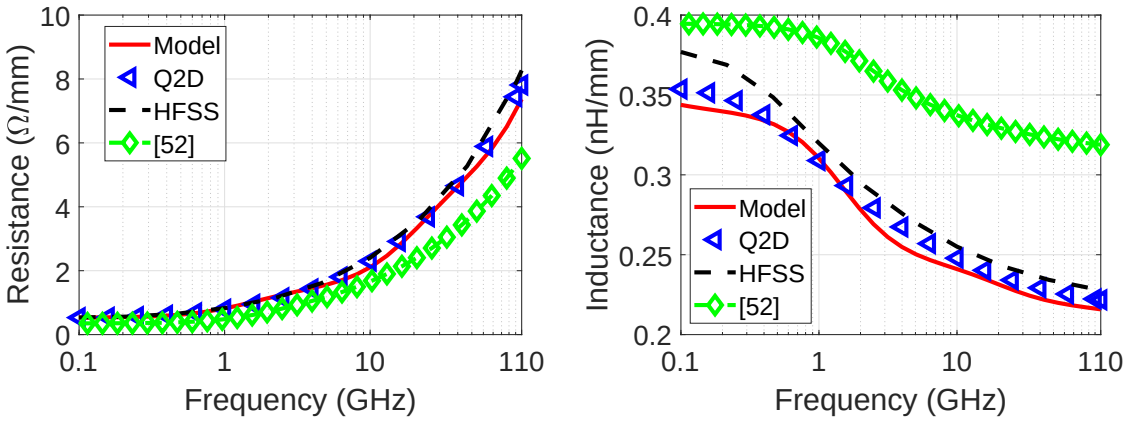

Figure 2.36: Comparison of per-unit-length resistance and inductance obtained with the scalable equivalent circuit model (Model), EM solver Q2D, HFSS and the model in [52].

The scalable RL model of on-chip CPWs is suitable for various process nodes with a large normalized geometry range with signal line width-to-thickness ratios w_s/t between 1 and 15 and spacing-to-thickness ratios s/t between 0.25 and 15. Our model was validated by both rigorous EM simulation and measurements of fabricated test chips. The model can easily be implemented into standard circuit simulators. The accuracy is within 10% over the normalized geometry range, as illustrated in Figs. 2.37-2.39. The error is defined as

$$\text{Error} = \frac{|\text{Scalable Model- EM Simulation Values}|}{\text{EM Simulation Values}} \times 100\% \tag{2.26}$$

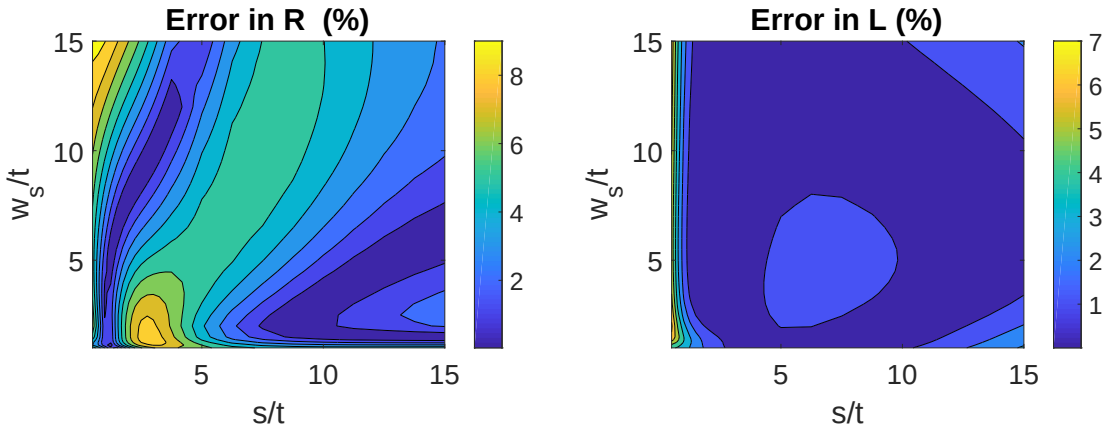

Figure 2.37: RL percent error between the scalable equivalent circuit model and EM solver for wide normalized geometry ranges at 1 GHz.

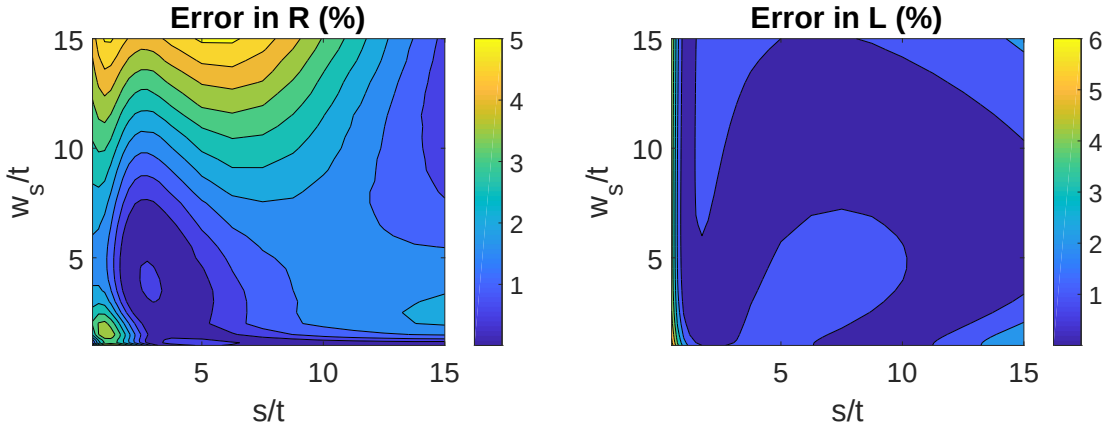

Figure 2.38: RL percent error between the scalable equivalent circuit model and EM solver for wide normalized geometry ranges at 60 GHz.

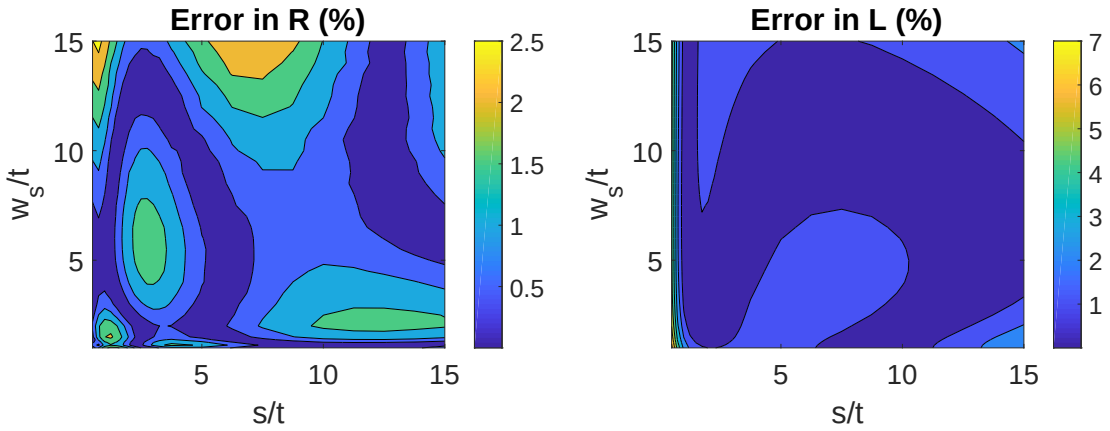

Figure 2.39: RL percent error between the scalable equivalent circuit model and EM solver for wide normalized geometry ranges at 110 GHz.

We have also fabricated test chips in TowerJazz 180 nm SiGe BiCMOS process and 130 nm RFCMOS process. Two test CPWs with different metal thicknesses and dimensions and de-embedding structures have been measured. For CPW in 180 nm process, the width of the signal and ground conductors are both 12 μm. The spacing s is 5 μm. In the 130 nm process, the widths of signal and ground conductors are 6 μm and 12 μm, respectively. The spacing s is 8 μm. The p.u.l. resistance and inductance have been extracted through de-embedded S parameters. The de-embedding process is described in [69]. Comparisons between the model, HFSS simulation, and measurement are shown in Fig. 2.40 and Fig. 2.41. Both the p.u.l. resistance and inductance of the model match well with EM simulation and measurements.

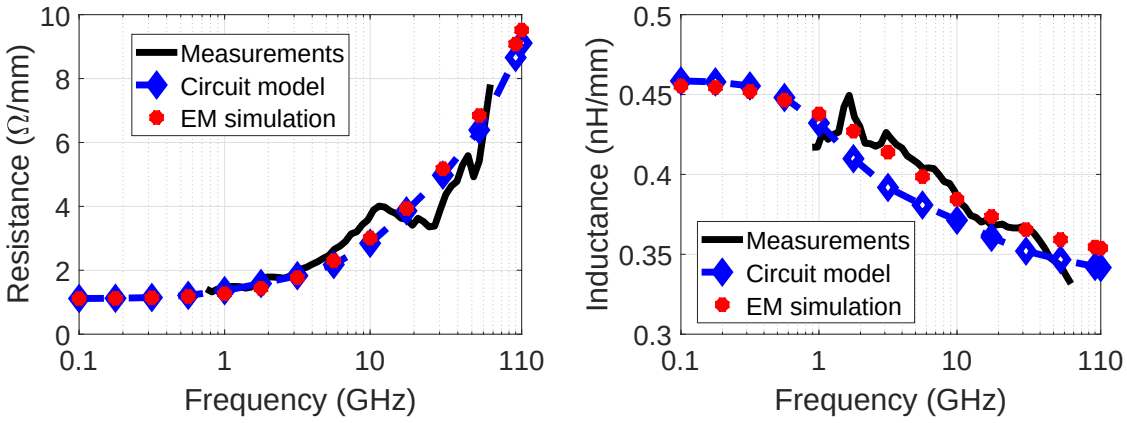

Figure 2.40: Comparison of per-unit-length resistance and inductance obtained with the scalable equivalent circuit model, EM simulation and measurement for example on-chip CPW in TowerJazz RFCMOS 130 nm.

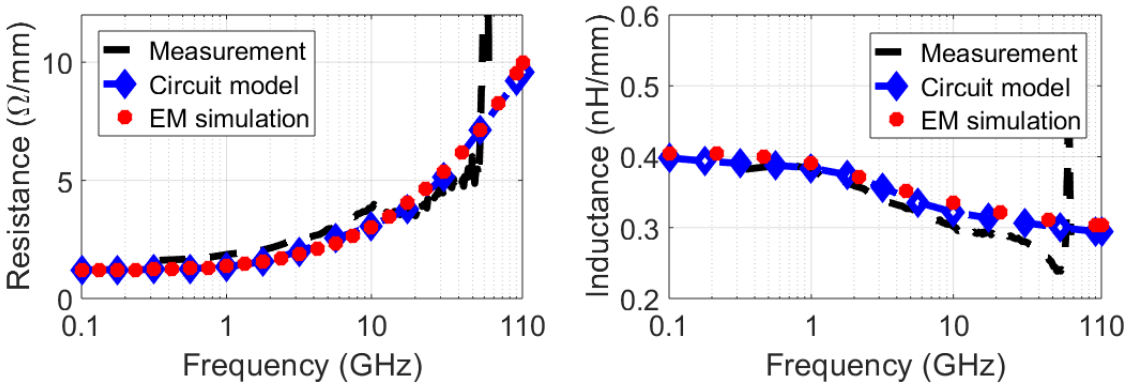

Figure 2.41: Comparison of per-unit-length resistance and inductance obtained with the scalable equivalent circuit model, EM simulation and measurement for example on-chip CPW in TowerJazz BiCMOS 180 nm.

2.10 Scalable Modeling with Multi-physics Effects

The scalable models enable modeling multi-physical effects such as temperature changes [70] and process variability [71] through the mapping from the dimensional and material parameters to the electrical and performance characteristics of the passive components.

To address variability and uncertainty in the physical parameters (dimensions and material properties) in the model, we performed comprehensive Monte Carlo analyses [72] by leveraging our scalable models with the variations in physical parameter input. These analyses provide an intuitive understanding of the severity and impact of variability on the performance of mmWave passive components for a given process as well as different process nodes.

2.10.1 Temperature Effects

For metal layers commonly used in IC processes, such as copper and aluminium, the resistivity is temperature dependent. A linear approximation is typically used [73]:

$$\rho\left(T\right) = \rho_0\left[1 + a\left(T - T_0\right)\right] \tag{2.27}$$

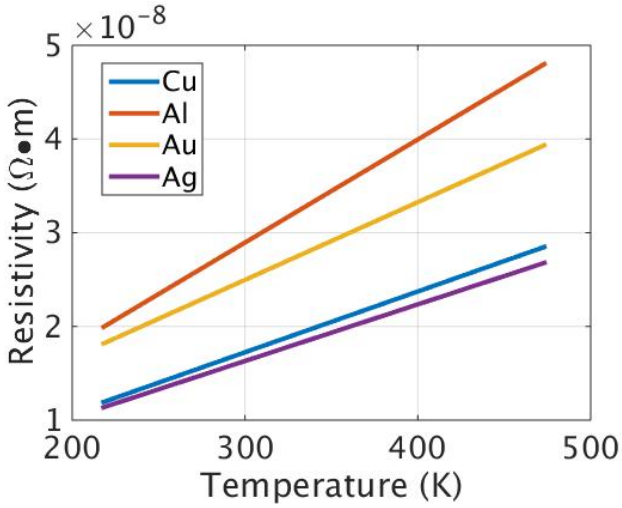

Figure 2.42: Resistivity of different metal changes with temperature.

where ρ_0 is the resistivity at temperature T_0 and a is the temperature coefficient of resistivity. In our equivalent circuit model, if the conductivity of metal changes with temperature, the inductance value will not vary, while all resistance values will be altered based on the relation below:

$$R(T) = \frac{\rho(T)}{\rho_0} R(T_0) \tag{2.28}$$

$R(T_0)$ is the resistance value at temperature T_0, $R(T)$ is the resistance value at temperature T. To verify our model, we take aluminium as example, with a conductivity of 3.5×10^7 S/m at 293 K (20 °C). The temperature coefficient is 0.0039 K^{-1}. Therefore, at 218 K (-55 °C) and 398 K (125 °C), the conductivity for aluminium is 4.94×10^7 S/m and 2.48×10^7 S/m, respectively. For the on-chip CPW, we assuming that the width of the signal conductor is 10 μm, the thickness is 2 μm, the spacing is 4 μm, and the ground conductor width is 100 μm. We implemented our model with the additional temperature dependence. The performance of our scalable model is shown in Fig. 2.43.

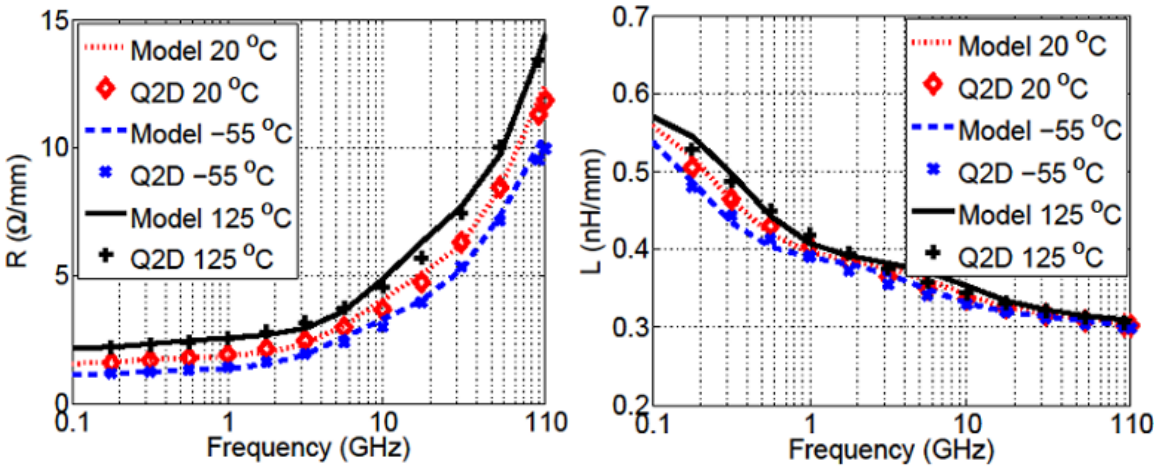

Figure 2.43: Comparison of per-unit-length resistance and inductance obtained with the broadband scalable model and Q2D EM simulation for different temperatures.

2.10.2 Process Variations

By leveraging the scalable modeling, the impact of process variations on the passives can be examined efficiently without performing time-consuming EM simulations. Figure 2.44 shows the flow of this procedure. The process variations are usually given in the IC process PDKs. Variations of physical geometry and material property parameters are mapped to the distributions of circuit element values in the scalable model. In the

end, the performance of the passive component with process variation can be analyzed via Monte Carlo simulations. For example, we have designed a 50 Ω microstrip in a TowerJazz BiCMOS 180nm process. The signal and ground conductor are on M6 and M3, respectively. Figure 2.45 and 2.46 show the distribution of characteristic impedance (Z_0), attenuation constant (α) and phase constant (β) due to the process variations.

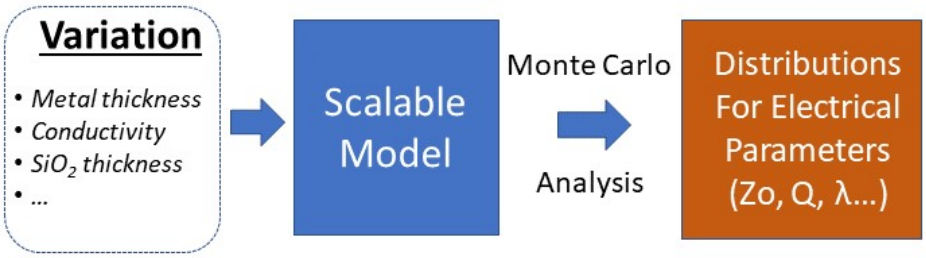

Figure 2.44: Study of process variations through scalable models

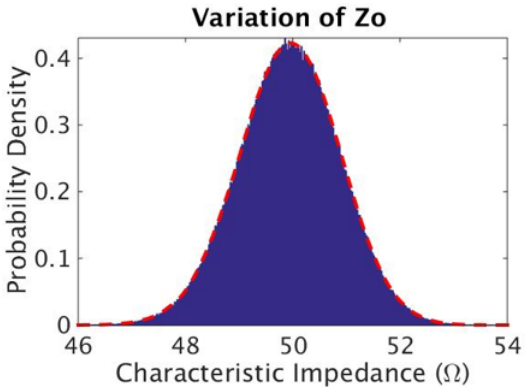

Figure 2.45: Distribution of Z_0 due to process variations for a nominal 50 Ω microstrip in a TowerJazz BiCMOS 180nm process (signal on M6 and ground on M3).

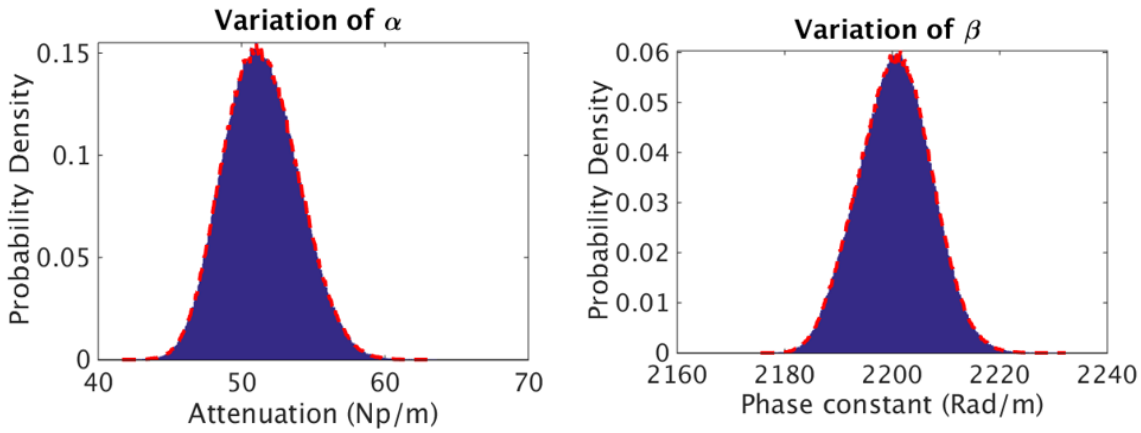

Figure 2.46: Distribution of attenuation constant α (left) and phase constant β (right) due to process variations for a nominal 50 Ω microstrip in a TowerJazz BiCMOS 180nm process (signal on M6 and ground on M3).

We also use our transmission line model as building block for other types of passives. In Fig. 2.47, a single stub matching network was designed and modeled in TowerJazz 180 nm BiCMOS process. A load impedance assumed as 5-j20 Ω was matched to 50 Ω at 60 GHz. The real and imaginary parts of the input impedance are shown in Fig. 2.48. The $\mu \pm 2\sigma$ interval of the input impedance is indicated as well. The distribution of the standing wave ratio (SWR) at input port is illustrated in Fig. 2.49. Similarly, a 60 GHz branch line coupler (Fig. 2.50) was implemented in the same process. Since the branch line coupler only consists of microstrip lines with different impedances, the equivalent circuit model of the coupler is represented for each branch by the micrsotrip equivalent circuit model. The equivalent circuit model (nominal design) matches well with the HFSS simulation, and the impact of process variations is also included in Fig. 2.51.

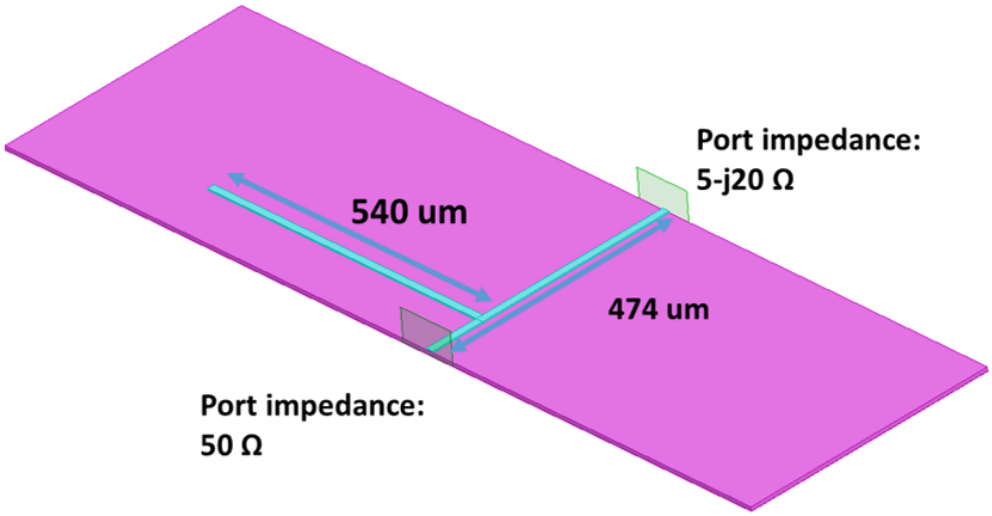

Figure 2.47: Design of a single stub matching network using microstrip in TowerJazz 180 nm BiCMOS process.

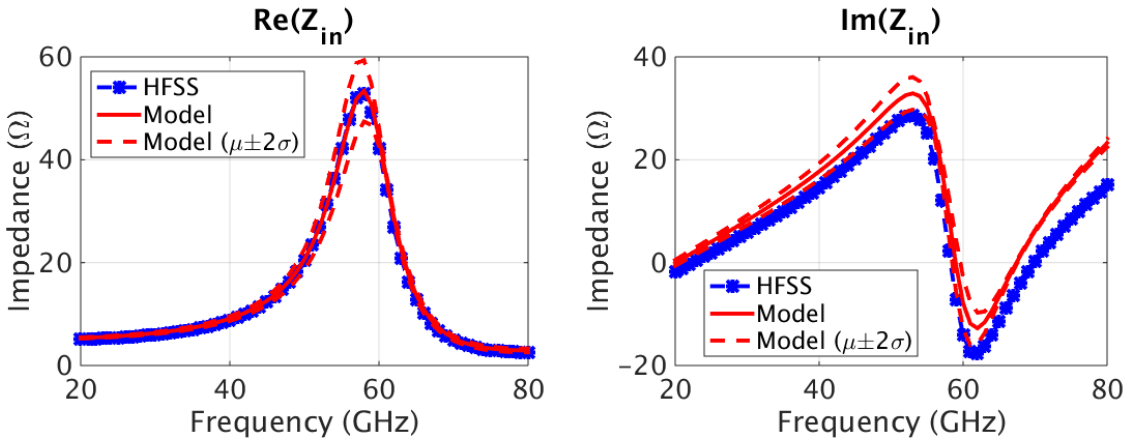

Figure 2.48: Comparison of between HFSS simulation and scalable equivalent circuit model for the single-stub microstrip matching network shown in Fig. 2.47, including the impact of process variations.

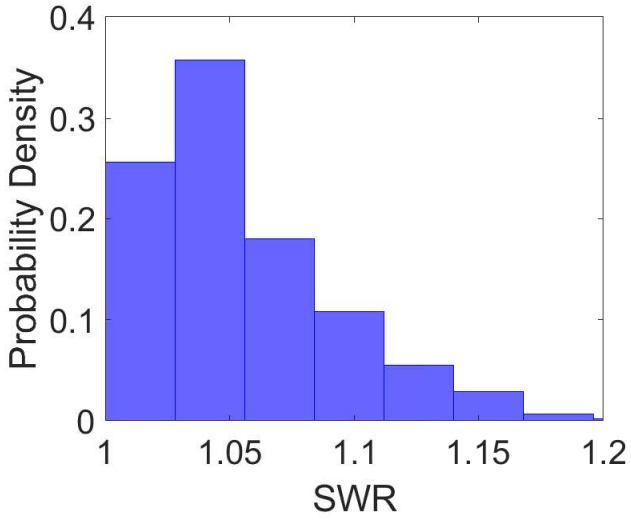

Figure 2.49: Distribution of SWR at input port for the single-stub microstrip matching network shown in Fig. 2.47 due to process variations.

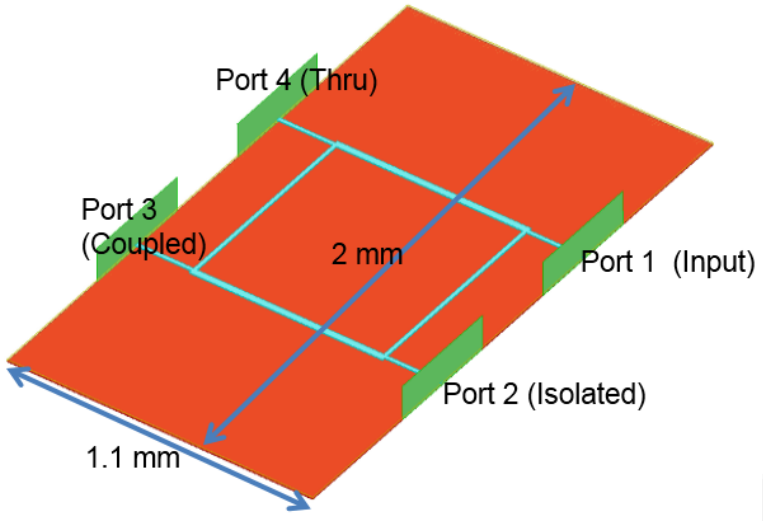

Figure 2.50: Design of a branch line coupler using microstrip in TowerJazz 180 nm BiCMOS process.

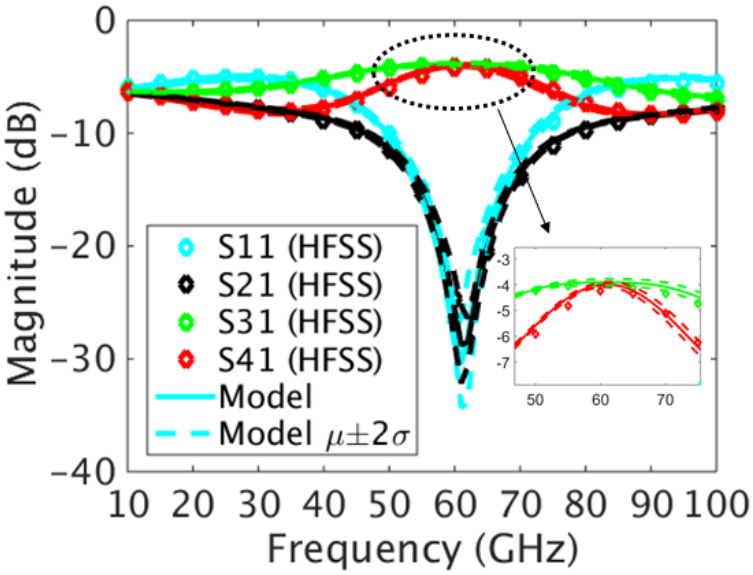

Figure 2.51: Comparison between HFSS simulation and scalable equivalent circuit model for a 60 GHz branch line coupler, including the impact of process variations.

2.11 Conclusion

In this chapter, scalable and compact equivalent circuit models for on-chip microstrip and CPW have been developed and validated by EM simulation and measurement. The models are suitable for various process nodes over broad geometrical parameter ranges. Example HSPICE model netlists for microstrip and CPW are shown in Appendix B.1 and B.2, respectively. Our models incorporate temperature dependency as well. The scalable models have also been applied to more complicated passives (e.g., a single-stub matching network and a 60 GHz branch line coupler). We also have performed Monte Carlo simulation using the scalable models to study the impact of process variations on the performance of passives. To model other more complicated passives, a more general scalable modeling approach is presented in the next chapter.

Chapter 3: Field-based Closed-form Modeling Approach

3.1 Introduction

We have discussed the modeling techniques for single isolated transmission lines (e.g., microstrip and CPW). The key process is to reduce the number of parameters to a certain degree so that development of closed-form formulas is viable. However, for more complicated interconnects with a larger number of conductors than for isolated transmission lines, the number of geometry variables increases quickly so that the approach discussed in Chapter 2 is no longer viable. For example, the coupled CPW has one more signal conductor compared with the isolated CPW, as illustrated in Fig. 3.1. To model the resistance for this extra signal conductor, both the signal conductors' geometry and their relative locations with other conductors need to be taken into consideration. Adding this extra conductor will also affect the frequency-dependent resistance for the other conductors, which needs to be considered in the model.

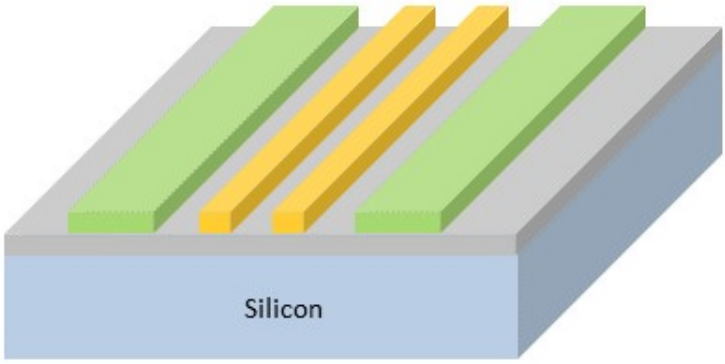

Figure 3.1: On-chip coupled CPWs with four conductors (signal conductors are yellow and ground conductors are green).

In this chapter, we present a systematic approach for modeling the resistive losses

in on-chip interconnects [74]. As discussed in Section 2.4, it is generally prohibitive to directly develop closed-form expressions for the p.u.l. resistance with many parameters involved. In the previous chapter, the key scalable modeling techniques developed for the isolated transmission lines leverages the Principle of Electromagnetic Similitude and adopts a Foster network topology. Such techniques can only reduce the number of parameters by two, i.e., one parameter reduction by using normalized parameters and a variable reduction by implementing the frequency dependence through a Foster network synthesis. For more complicated passives, further reduction of the problem complexity is needed. To address this challenge, we have developed a technique by separately modeling the resistance increase due to the skin and proximity effects on each individual conductor and combining them to obtain the total resistance. The proximity effect is due to the magnetic field generated by the currents in adjacent conductors, which usually is non-uniform across the conductor region. To further reduce the complexity, the non-uniform magnetic field is approximated by an average uniform field. It has been shown that the contributions due to skin effect and proximity effect in rectangular conductors are orthogonal (in a functional sense) [75] if the applied external magnetic field is uniform. Thus, with the uniform magnetic field approximation, we can model the resistance increase due to skin effect and proximity effect separately and combine them to obtain the total frequency-dependent p.u.l. resistance.

This chapter is organized as follows. We first demonstrate the orthogonality of skin and proximity effects in a uniform field environment in Section 3.2. Sections 3.3 and 3.4 present the separate development of closed-form expressions for the skin and proximity losses taking advantage of the orthogonality of their contributions. Next, in Sections 3.5 and 3.6, we apply our techniques to both CPW and coupled CPWs. A mapping technique is proposed in Section 3.7 to derive the equivalent RL circuit model that can be employed in circuit simulators. Our model also includes the substrate eddy current effects in low resistivity substrate, as demonstrated in Section 3.8.

3.2 Orthogonality of Skin and Proximity Effects

If the external applied field is uniform and parallel to the symmetry axis of parallel conductors, the power losses due to skin and proximity effects can be separated due to orthogonality of the two effects [75]. Consider an input current (e.g., I_1) density $\vec{J}_{\text{skin}}$ in

the signal conductor of a CPW, as illustrated in Fig. 3.2. $\vec{J}_{\text{skin}}$ is already non-uniform due to the skin effect. In addition, when an external field $\vec{H}_a$ is applied due to currents in closeby conductors (e.g., I_2), this will cause an additional eddy current $\vec{J}_{\text{prox}}$. The total current density in the signal conductor can be expressed as

$$\vec{J}_{\text{sum}} = \vec{J}_{\text{skin}} + \vec{J}_{\text{prox}}. \tag{3.1}$$

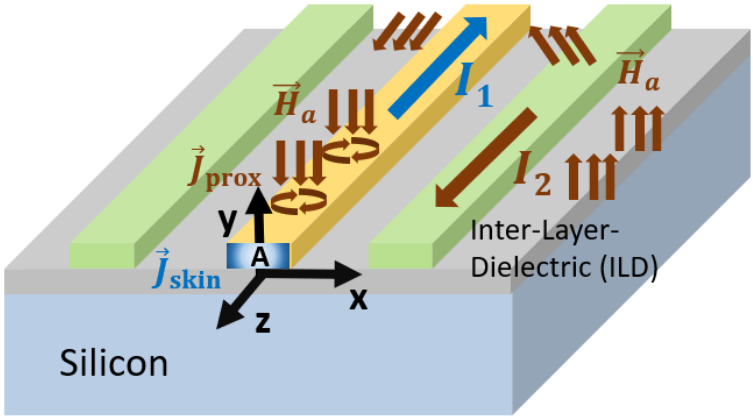

Figure 3.2: Illustration of skin and proximity effects in the signal conductor of a CPW

The non-uniform current density due to the skin effect, $\vec{J}_{\text{skin}}$, is symmetrical about the yz-plane, i.e.,

$$\vec{J}_{\text{skin}}(-x) = \vec{J}_{\text{skin}}(x) \tag{3.2}$$

In contrast, the induced current density due to external field $\vec{H}_a$ is anti-symmetric along the x-axis, i.e.,

$$\vec{J}_{\text{prox}}(-x) = -\vec{J}_{\text{prox}}(x) \tag{3.3}$$

Since $\vec{J}_{\text{sum}}$ is perpendicular to A, the total p.u.l. power loss in the signal conductor is obtained as

$$P_{\text{p.u.l.}} = \frac{1}{2\sigma}\iint_A \vec{J}_{\text{sum}} \cdot \vec{J}^*_{\text{sum}} dA = \frac{1}{2\sigma}\iint_A \left(\vec{J}_{\text{skin}} + \vec{J}_{\text{prox}}\right) \cdot \left(\vec{J}^*_{\text{skin}} + \vec{J}^*_{\text{prox}}\right) dA, \tag{3.4}$$

As discussed before, the induced eddy current ($\vec{J}_{\text{prox}}$) due to an external uniform mag-

netic field is an odd function and the current due to the skin effect ($\vec{J}_{\text{skin}}$) is an even function along the width of the conductor. Therefore, the total power loss can be partitioned into three parts: the power loss due to (i) the skin effect current ($\vec{J}_{\text{skin}}\vec{J}^{*}_{\text{skin}}$), ($ii$) the eddy current induced by the external field ($J_{\text{prox}}J^{*}_{\text{prox}}$), and ($iii$) the mixed current ($\vec{J}_{\text{skin}}\vec{J}^{*}_{\text{prox}} + \vec{J}_{\text{prox}}\vec{J}^{*}_{\text{skin}}$). Since the last term is an odd function, the integral of the mixed current term over the conductor width is zero. The total p.u.l. power loss is given as

$$P_{p.u.l.} = \frac{1}{2\sigma}\iint_A \vec{J}_{\text{skin}} \cdot \vec{J}^{*}_{\text{skin}} dA + \frac{1}{2\sigma}\iint_A \vec{J}_{\text{prox}} \cdot \vec{J}^{*}_{\text{prox}} dA. \tag{3.5}$$

The first and second integrals correspond to skin effect loss and proximity effect loss, respectively.

3.3 Modeling Skin Effect Resistance

We first start with the time-varying applied and response magnetic fields, $\vec{H}_0$ and $\vec{H}_r$ at the cross section of the conductor in the xy-plane. Ignoring the displacement current, the relation between $\vec{H}_0$ and $\vec{H}_r$ can be derived as [76]

$$\vec{H}_0 + \vec{H}_r = \frac{1}{j2\pi f\mu_0\sigma}\nabla \times \nabla \times \vec{H}_r. \tag{3.6}$$

After bringing the constant term $\pi f\mu_0\sigma$ into the curl-curl operator (normalizing the physical dimension in terms of skin depth δ), $\vec{H}_r$ can be represented as

$$\vec{H}_r = |\vec{H}_0|\vec{f}_H\left(\frac{x}{\delta}, \frac{y}{\delta}\right), \tag{3.7}$$

where $\vec{f}_H$ is a unit less vector function. The non-uniform current density $\vec{J}_{\text{skin}}$ is due to the skin effect, whcih $\vec{J}_{\text{skin}}$ can be derived from $\nabla\vec{H}_r$. Since the applied field $\vec{H}_0$ is proportional to the impressed current density $I/(wt)$, $\vec{J}_{\text{skin}}$ can be formulated as

$$\vec{J}_{\text{skin}} = \frac{I}{wt}\vec{f}_J\left(\frac{x}{\delta}, \frac{y}{\delta}\right), \tag{3.8}$$

where $\vec{f}_J$ is unknown unit-less vector function and δ is the skin depth given in (1.3). The p.u.l. power loss P can then be formulated in terms of $\vec{f}_J$ as

$$P = \frac{1}{2}\iint_A \frac{\left|\vec{J}_{\text{skin}}\right|^2}{\sigma} dxdy = \frac{1}{2}\iint_A \frac{I^2}{w^2t^2\sigma}\left|\vec{f}_J\right|^2 dxdy = \frac{1}{2}\frac{I^2}{wt\sigma}\iint_A \frac{1}{wt}\left|\vec{f}_J\right|^2 dxdy. \tag{3.9}$$

The last integral can be further expressed in terms of function G_{skin} as

$$\iint_A \frac{1}{wt}\left|\vec{f}_J\right|^2 dxdy = \frac{\delta^2}{wt} G^2_{\text{skin}}(\frac{w}{\delta}, \frac{t}{\delta}), \tag{3.10}$$

After rearranging the arguments in (3.10) and introducing a new function F_{skin}, which represents the integral above, R_{skin} can be formulated as

$$R_{\text{skin}} = \frac{2P}{I^2} = R_{\text{dc}} F_{\text{skin}}\left(\frac{wt}{\delta^2}, \frac{w}{t}\right), \tag{3.11}$$

where R_{dc} is the p.u.l. DC resistance of the conductor.

To develop a closed-form expression for F_{skin}, the functional form of F_{skin} is based on the behavior of the frequency-dependent resistance. The same functional form (3.12) as in Eq. 8 of [76] is used here, since this form captures the skin effect behavior and it is asymptotically stable. The normalized frequency p is defined as $p = wt/\delta^2$, as discussed in Chapter 2. The development of empirical function F_{skin} is analogous to the one presented in Chapter 2 and is further explained in Fig. 3.3: using a commercial field solver [77], we simulate isolated conductors having different width-over-thickness ratios by varying the width (w) and keeping the thickness (t) and conductivity (σ) constant. The behavior of F_{skin} for different w/t can be captured by normalizing the frequency-dependent resistance with the DC resistance. The next step is to fit the simulated F_{skin} data into (3.12) using a Genetic Algorithm [58], resulting in a data table for the discrete values of coefficient m_i (i=1, 2, 3, 4). As a final step, the data table is fitted into equations that cover a continuous w/t range.

$$F_{\text{skin}} = \frac{m_1 p^2}{\left(m_2 p^{m_3} + 1\right)^{m_4}} + 1. \tag{3.12}$$

The coefficients m_1 to m_4 in (3.12) are fitted as

$$m_1 = 0.0066 \left(\frac{w}{t}\right)^{-0.4456} \tag{3.13}$$

$$m_2 = 0.0279 \left(\frac{w}{t}\right)^{-0.6962} + 0.0175 \tag{3.14}$$

$$m_3 = 1.415 \tag{3.15}$$

$$m_4 = 0.9815 \left(\frac{w}{t}\right)^{0.0087}. \tag{3.16}$$

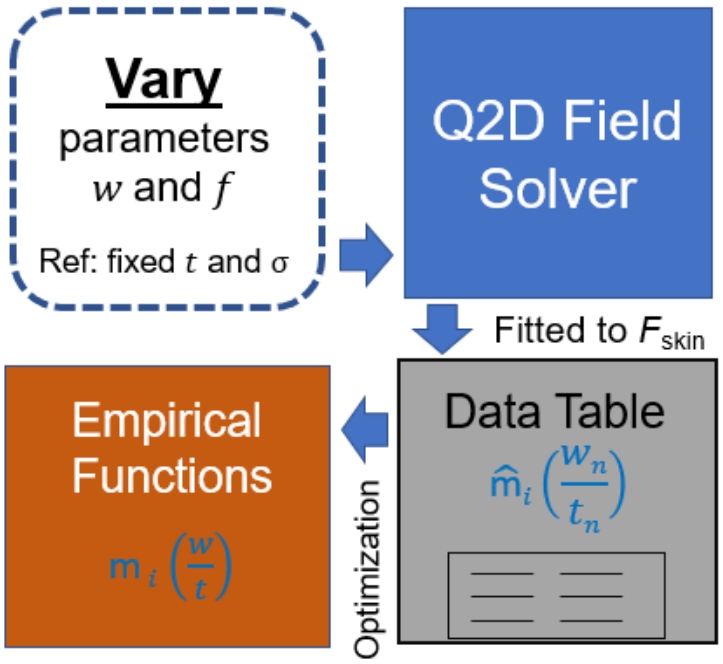

Figure 3.3: Diagram illustrating the development process for obtaining the closed-form expression for skin effect resistance only.

The skin effect formula has been verified through extensive EM simulations. Figure 3.4 shows comparisons between EM simulations and our closed-form formula for different aspect ratios w/t.

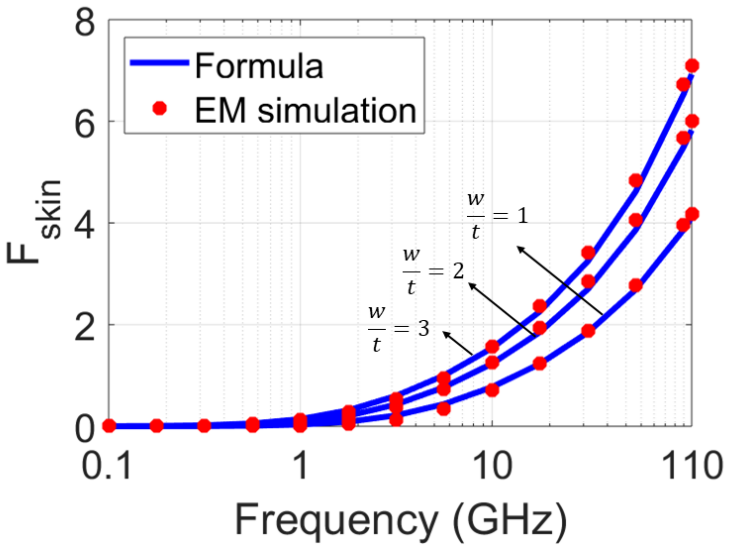

Figure 3.4: Comparison between EM simulations and closed-form formula for F_{skin}.

The formula is suitable for different process nodes, and was developed for width-over-thickness ratio w/t between 1 to 15, and for the frequency range from DC up to 110 GHz. As illustrated in Fig. 3.5, the L2-norm error is below 7% for the geometry range. The L2-norm error is defined as

$$\text{Error} = \frac{\|x_{\text{model}} - x_{\text{sim}}\|_2}{\|x_{\text{sim}}\|_2} \times 100\%, \tag{3.17}$$

where x_{model} is the closed-form expression, x_{sim} is the EM simulation result. $\|\cdot\|$ is the L2-norm [78]. Both x_{model} and x_{sim} are over the frequency range from DC to 110 GHz.

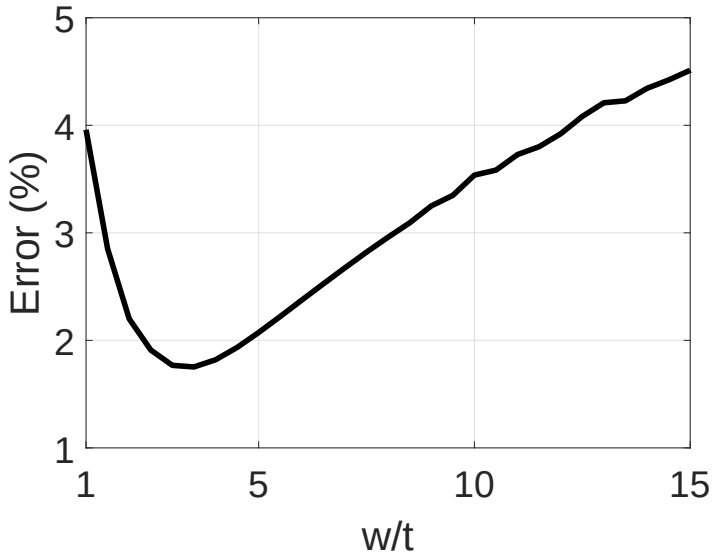

Figure 3.5: L2-norm error over the normalized w/t range for F_{skin}.

3.4 Modeling Resistance Increase due to Proximity Effect

To model the resistance increase due to the proximity effect, we assume the applied magnetic field $\vec{H}_a$ generated by the currents in adjacent planar conductors is uniform. Thus, as discussed in Section 3.2, skin and proximity loss contributions can be separated because of the orthogonality of these two effects. The total power loss p.u.l. is given as

$$P_{\text{total}} = P_{\text{skin}} + P_{\text{prox}} = \frac{1}{2} I^2 \left(R_{\text{skin}} + R_{\text{prox}} \right), \tag{3.18}$$

where I is the excitation current. Similar to the derivation of F_{skin}, the power loss due to the proximity effect is modeled as

$$P = \frac{1}{2} \iint_A \frac{\left| \vec{J}_{\text{prox}} \right|^2}{\sigma} dxdy, \tag{3.19}$$

where $\vec{J}_{\text{prox}}$ is the eddy current due to the external applied magnetic fields $\vec{H}_a$. From (3.6) and(3.7), $\vec{J}_{\text{prox}}$ can be represented as

$$\vec{J}_{\text{prox}} = |\vec{H}_a|\vec{f}_{\text{prox}}\left(\frac{x}{\delta}, \frac{y}{\delta}\right), \tag{3.20}$$

with vector function $\vec{f}_{\text{prox}}$. Similar to the development of F_{skin}, by substituting (3.20) into (3.19), the p.u.l. resistance due to the proximity effect is formulated as

$$R_{\text{prox}} = \frac{\left|\vec{H}_a\right|^2}{\sigma I^2} F_{\text{prox}}\left(\frac{wt}{\delta^2}, \frac{w}{t}\right). \tag{3.21}$$

To approximate F_{prox}, we use the same functional form as for F_{skin}. This form is guaranteed to be asymptotically correct to approximate the frequency-dependent behaviors of the proximity effect, as shown in Fig. 4 in [76]. F_{prox} is given as

$$F_{\text{prox}} = \frac{n_1 p^2}{(n_2 p^{n_3} + 1)^{n_4}}. \tag{3.22}$$

Similar to the development of an empirical formula for F_{skin}, a data set is generated by performing EM simulations in Maxwell [77] over a wide parameter range and fitted into suitable expressions, as shown in Fig. 3.6. Coefficients n_1 to n_4 in (3.22) are fitted as

$$n_1 = 0.2056\frac{w}{t} \times 0.819^{w/t} + 0.0168\frac{w}{t} \tag{3.23}$$

$$n_2 = 0.05 \tag{3.24}$$

$$n_3 = 0.3685 \times 0.8986^{w/t} + 1.1867 \tag{3.25}$$

$$n_4 = 0.1914\left(\frac{w}{t}\right)^{0.2434} + 0.7451. \tag{3.26}$$

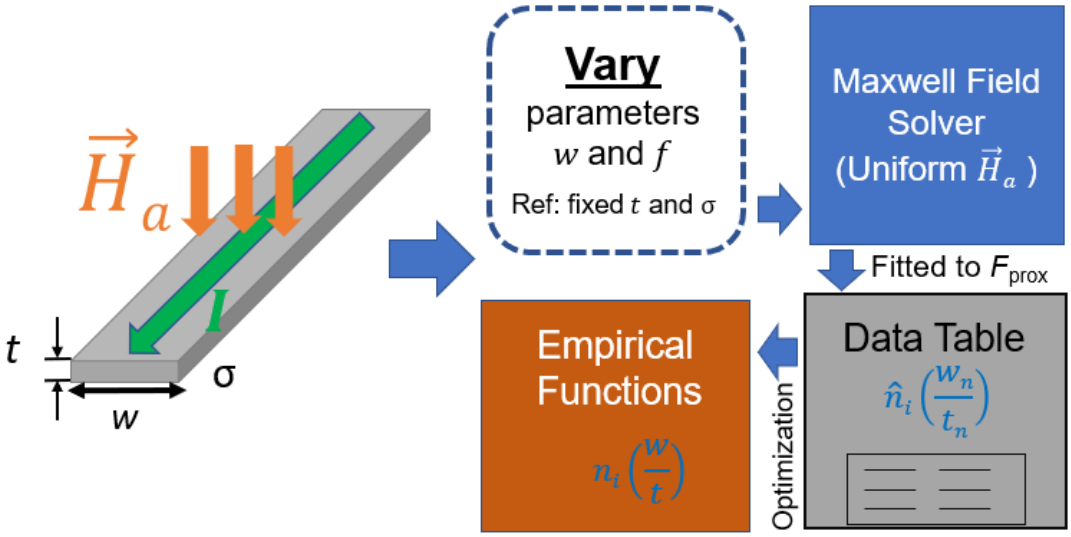

Figure 3.6: Diagram illustrating the development procedure for obtaining closed-form expressions for proximity effect resistance.

F_{prox} is also suitable for different process nodes. It has been developed for the same geometry and frequency range as F_{skin}. The L2-norm error is below 7% for the geometry range, as illustrated in Fig. 3.7. The L2-norm error is defined in (3.17).

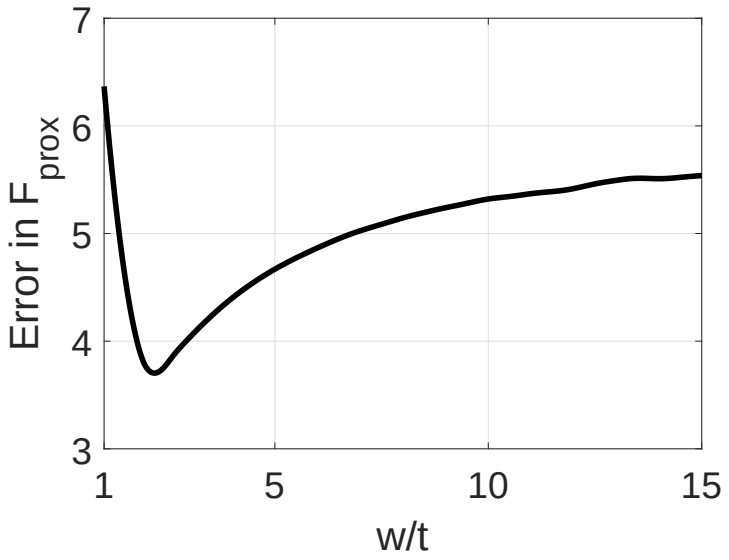

Figure 3.7: L2-norm error over the normalized w/t range for F_{prox}.

3.5 Application to an On-Chip CPW Interconnect

We have applied our systematic modeling methodology to determine the p.u.l. resistance of a representative on-chip CPW interconnect structure. The p.u.l. resistance is obtained as the superposition of the resistance change in signal and ground conductors due to the skin and proximity effects. For the signal conductor, the skin effect and proximity effect are modeled separately under the assumption of an average uniform field. The proximity effect is due to the magnetic field caused by the currents in both ground conductors, as shown in Fig. 3.8. To model the ground conductor resistance, we reduce the complexity of the problem by utilizing the symmetry of the CPW structure, where only one of the ground conductors needs to be considered. The proximity loss in one ground conductor is caused by the magnetic field due to the currents in both the signal conductor and the other ground conductor, as illustrated in Fig. 3.9.

As illustrated in Fig. 3.10, the resistance increase due to the proximity effect in the signal conductor can be calculated from (3.21)-(3.26), where $\left|\vec{H}_a\right|^2 = \left|\vec{H}_{g1} + \vec{H}_{g2}\right|^2$ is the average magnetic field due to the return currents in both ground conductors. $\vec{H}_{g1}$ and $\vec{H}_{g2}$ are due to the currents in the right and left ground conductors, respectively. $|\vec{H}_a|^2$

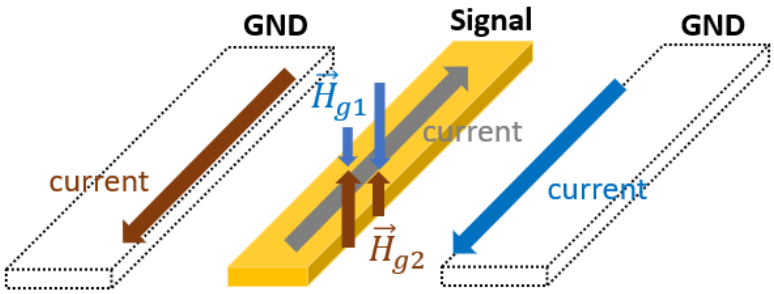

Figure 3.8: Proximity effect in the signal conductor is due to both ground currents.

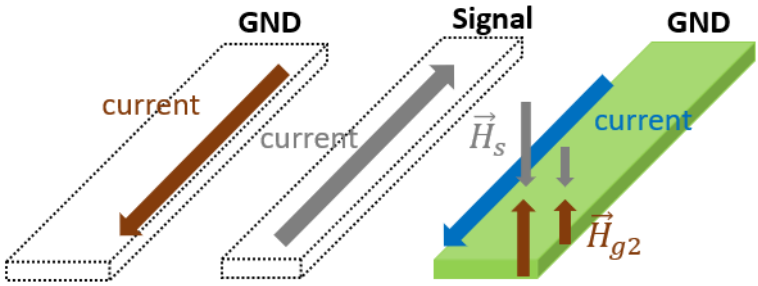

Figure 3.9: Proximity effect in the right ground conductor is due to the signal current and the left ground current.

is approximated as

$$\left|\vec{H}_{g1}+\vec{H}_{g2}\right|^2=\frac{1}{w_s}\int_0^{w_s}\left|\frac{I/2}{2\pi\left(s+x\right)}-\frac{I/2}{2\pi\left(s+w_s-x\right)}\right|^2dx. \tag{3.27}$$

Here we assume the current distribution in each ground conductor is represented as a line current at the inner edge. To capture the increasing resistance due to the conductor skin effect, the formulas developed in Sections 3.3 and 3.4 have been applied.

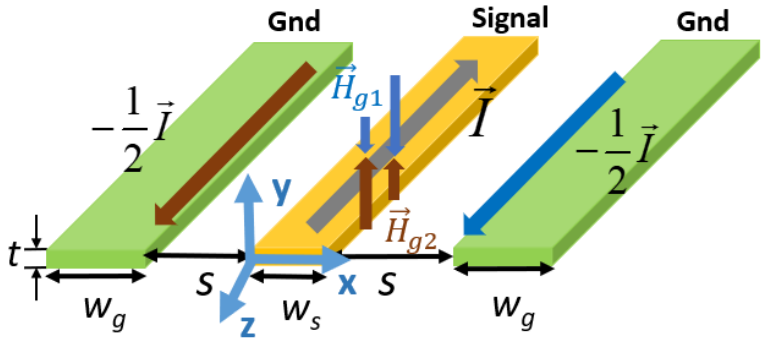

Figure 3.10: Ground conductor current inducing magnetic fields in the signal conductor of the CPW.

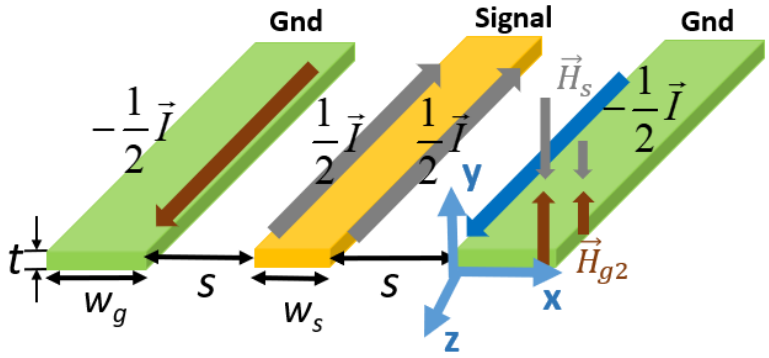

Figure 3.11: Magnetic fields in right-side CPW ground conductor induced by the currents in the signal conductor and the left-side ground conductor.

To calculate the resistance in either of the ground conductors due to the proximity effect, $\left|\vec{H}_a\right|$ is approximated as an average field given as

$$\left|\vec{H}_a\right|^2 = \frac{1}{w_g}\int_0^{w_g}\left|\frac{I/2}{2\pi\left(s+x\right)} + \frac{I/2}{2\pi\left(s+w_s+x\right)} - \frac{I/2}{2\pi\left(2s+w_s+x\right)}\right|^2 dx. \tag{3.28}$$

Here, we assume the current distributions in the other conductors are represented by two line currents placed at the two edges of the signal conductor and a line current at the inner edge of the other ground.

Finally, the total p.u.l. resistance of the CPW can be formulated as

$$R_{\text{p.u.l.}} = \left(R_{\text{skin}}^{\text{signal}} + R_{\text{prox}}^{\text{signal}}\right) + \frac{1}{2}\left(R_{\text{skin}}^{\text{ground}} + R_{\text{prox}}^{\text{ground}}\right) \tag{3.29}$$

We have validated our closed-form expressions for modeling on-chip CPW resistance over a wide parameter range. Figure 3.12 shows the geometry of a test CPW structure, where the width of the ground conductors is 12 μm and the conductor thickness is 3 μm. The single conductor width over the thickness ratio (w_s/t) is varied from 1 to 10. The signal to ground spacing over the thickness ratio (s/t) is also varied from 1 to 10. As shown in Figs. 3.13 to 3.15, the maximum error in $R_{\text{p.u.l.}}$ as compared to EM simulations is below 10% for three example frequencies (i.e., 1 GHz, 60 GHz and 110 GHz). The error is defined in (2.26). The comparison demonstrates the effectiveness of our field-based approach to determine the resistive loss due to skin and proximity effects in coplanar waveguide structures.

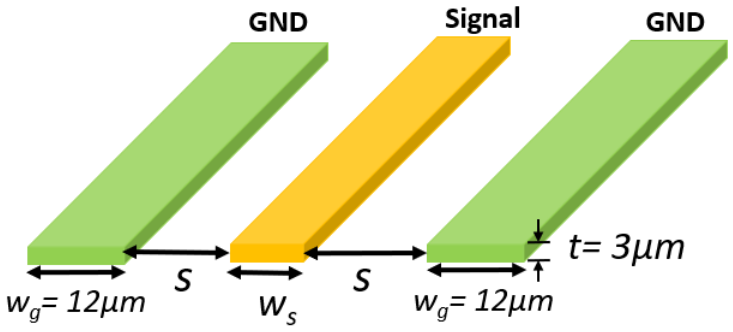

Figure 3.12: Geometry of a test CPW structure.

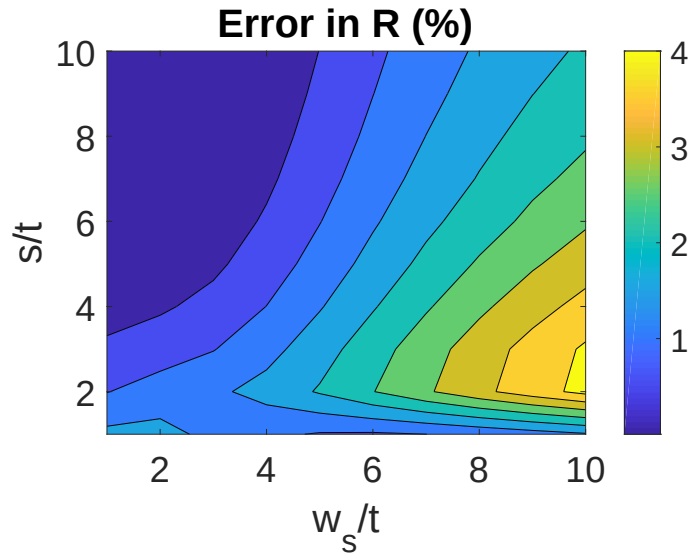

Figure 3.13: Percent error in R between the closed-form formulas and EM simulation at 1 GHz for on-chip CPW shown in Fig. 3.12.

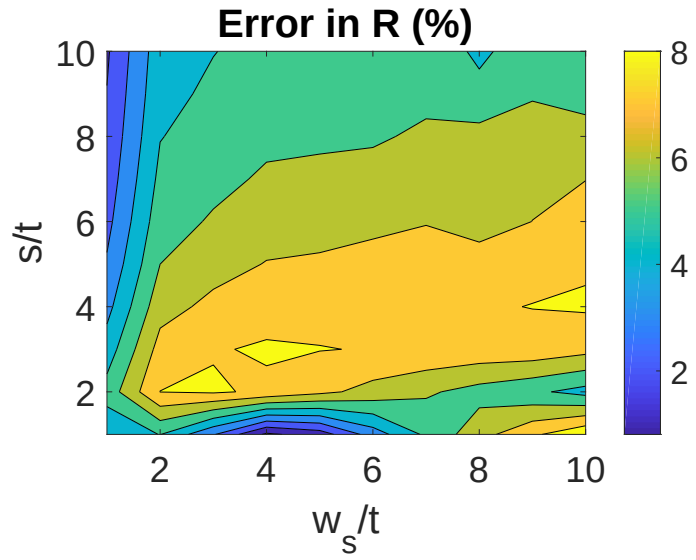

Figure 3.14: Percent error in R between the closed-form formulas and EM simulation at 60 GHz for on-chip CPW shown in Fig. 3.12.

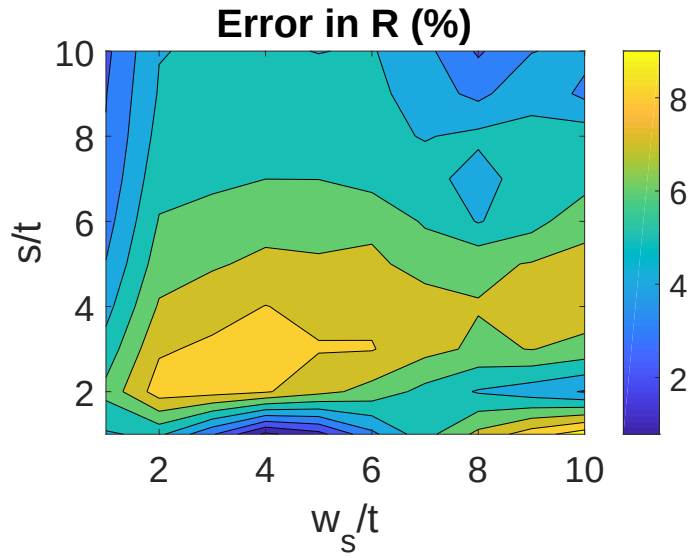

Figure 3.15: Percent error in R between the closed-form formulas and EM simulation at 110 GHz for on-chip CPW shown in Fig. 3.12.

To demonstrate the accuracy and applicability of our scalable modeling approach, we have fabricated a test chip with a CPW structure in a TowerJazz 130nm BiCMOS process and taken on-wafer S-parameter measurements for frequencies up to 67 GHz. The VNA (Agilent PNA U5227A) was calibrated using Short-Open-Load-Thru (SOLT) technique [79] with off-chip impedance standard substrate (ISS). The de-embedding technique from [69] is used. Figure 3.16 shows a comparison of our closed-form formulas and the results obtained with HFSS as well as with the on-wafer measurements. In this case, the width of the signal and ground conductors is 12 μm, and the spacing between the signal and ground conductor is 5 μm. The model shows good agreement with both the measurement and the EM simulation.

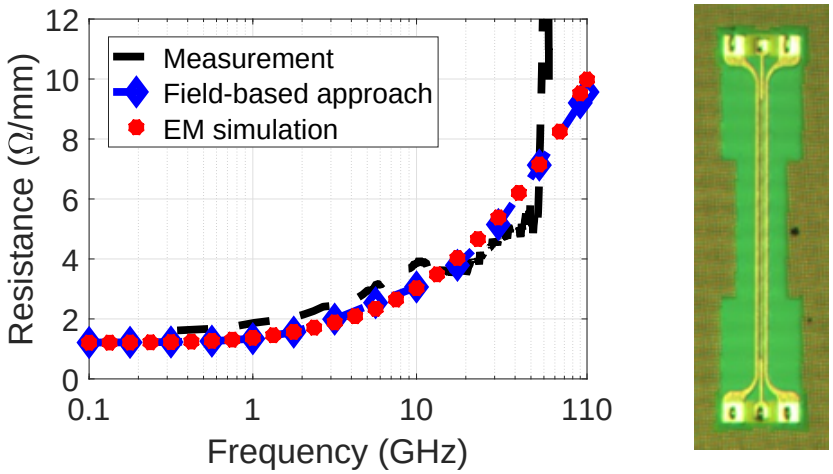

Figure 3.16: Comparison between the closed-form formulas, field solver results and measurements for an on-chip CPW test structure with $w_s = w_g$= 12 μm, s = 5 μm, fabricated in M7 in a TowerJazz 130nm BiCMOS process (right picture).

3.6 Application to an On-Chip Coupled CPW Interconnect

Our approach is also applicable to coupled coplanar waveguides [80]. Similar to a single CPW, we use the symmetry of the structure to reduce the problem complexity. We analyze common and differential modes separately and derive the self and mutual resistance matrix elements based on the common and differential mode resistances. As shown in Fig. 3.17, when calculating the differential mode resistance for the two signal conductors, the problem is reduced to the two-conductor coplanar strip case. The skin effect resistance can be calculated through formulas already developed in Section 3.3. For proximity effect resistance, we observe that the currents are crowding at the inner surfaces. Hence, the $|\vec{H}_a|^2$ field is

$$\left|\vec{H}_a\right|^2 = \frac{1}{w_s}\int_0^{w_s}\left|\frac{I}{2\pi\left(s_s+x\right)}\right|^2 dx. \tag{3.30}$$

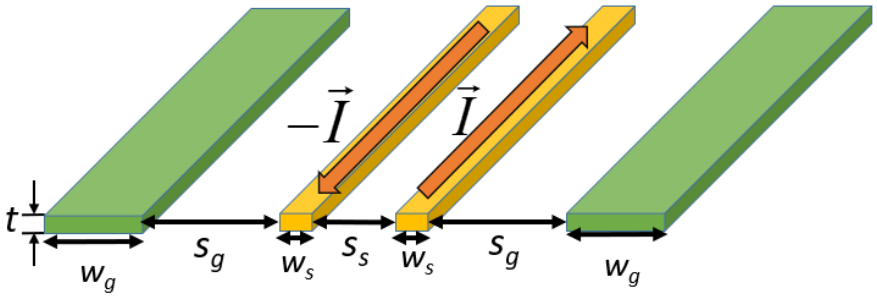

Figure 3.17: Differential mode excitation.

For the eddy-current loss in the ground conductors, the resistance is only due to the proximity effect since there is no impressed current. The proximity effect resistance for the ground conductors can be written as

$$R_{\text{prox}} = \frac{\left|\vec{H}_a\right|^2}{\sigma I^2} F_{\text{prox}}\left(\frac{w_g t}{\delta^2}, \frac{w_g}{t}\right), \tag{3.31}$$

where

$$\left|\vec{H}_a\right|^2 = \frac{1}{w_g}\int_0^{w_g} \left|\frac{I}{2\pi\left(s_g + w_s + x\right)} - \frac{I}{2\pi\left(s_s + w_s + s_g + x\right)}\right|^2 dx. \tag{3.32}$$

When s_s is small compared with $w_s + s_g$, the proximity effect resistance in the ground conductor is negligible compared to the total loss in the signal conductors because of the cancellation of H-fields due to the opposite currents in the signal conductors.

For the common mode resistance, we only need to determine the resistance for one signal conductor and the adjacent ground conductor due to symmetry. As illustrated in Fig. 3.18, the equivalent line current for each signal conductor lies at the outer edge while for the ground conductor it is at the inner edge due to the proximity effect. To calculate the ground conductor proximity effect resistance, $|\vec{H}_a|^2$ can be approximated as

$$\left|\vec{H}_a\right|^2 = \frac{1}{w_s}\int_0^{w_s} \left|\frac{I}{2\pi\left(s_g + x\right)} + \frac{I}{2\pi\left(s_g + 2w_s + s_g + x\right)} - \frac{I}{2\pi\left(2s_g + 2w_s + s_g + x\right)}\right|^2 dx. \tag{3.33}$$

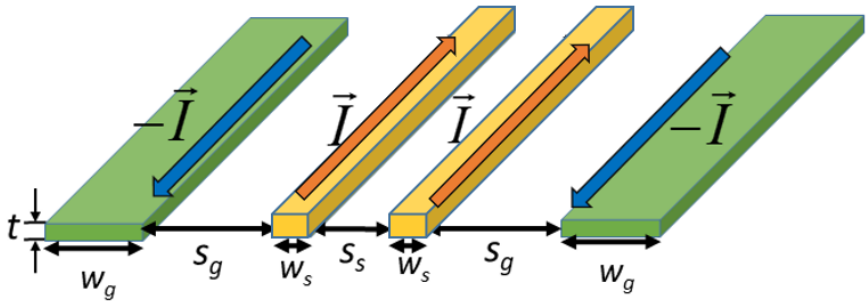

Figure 3.18: Common mode excitation

For the signal conductor resistance due to proximity effect, $|\vec{H}_a|^2$ is approximated as

$$\left|\vec{H}_a\right|^2 = \frac{1}{w_s}\int_0^{w_s}\left|\frac{I}{2\pi\left(w_s+s_s+x\right)}+\frac{I}{2\pi\left(s_g+w_s-x\right)}-\frac{I}{2\pi\left(s_g+w_s+s_s+x\right)}\right|^2 dx. \tag{3.34}$$

For verification, we simulated an example coupled CPW structure shown in Fig. 3.19. As illustrated in Fig. 3.19, the width of the signal and ground conductors is 4 μm and 10 μm, respectively, the thickness is 2 μm, the spacing between the signal and ground conductors is 2 μm, the spacing between the signal conductors is 2 μm, and the conductor conductivity is 3×10^7 S/m. The common mode resistance is the total

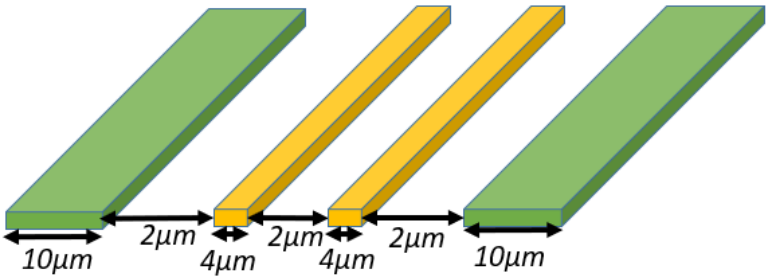

Figure 3.19: Dimensions for a simulated example coupled CPW structure (drawing not to scale).

resistance of both the signal and ground conductors when the two signal conductors are excited with the same voltage. The differential model resistance includes the loss due to the signal conductors as well as the eddy-current loss of the ground conductors. Given

the common and differential mode resistance, the two-port resistance parameters can also be derived based on the following relations:

$$R_{11} = R_{22} = \frac{2R_{\text{common}} + R_{\text{diff}}/2}{2} \tag{3.35}$$

$$R_{12} = R_{21} = \frac{2R_{\text{common}} - R_{\text{diff}}/2}{2}. \tag{3.36}$$

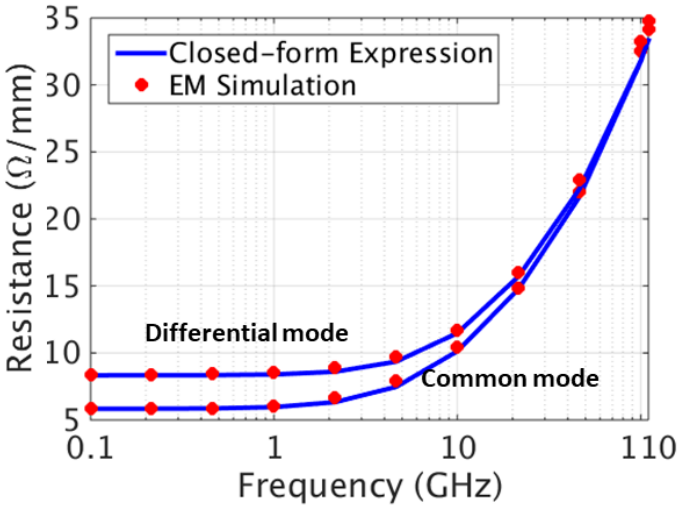

Figure 3.20: Comparison between EM simulation and closed-form expressions of per-unit-length common and differential mode resistance due to both skin and proximity effects in the coupled CPW transmission line shown in Fig. 3.19.

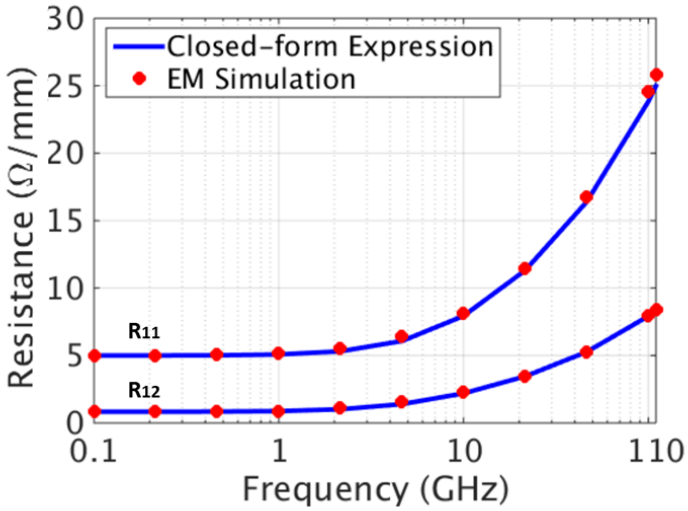

Figure 3.21: Comparison between EM simulation and closed-form expressions for per-unit-length self and mutual resistance due to both skin and proximity effects in the coupled CPW transmission lines shown in Fig. 3.19.

As shown in Figs. 3.20 and 3.21, the resistances obtained with the closed-form expression match well with the EM simulation results. An example coupled CPW was also fabricated in a TowerJazz 130nm RFCMOS process, as shown in Fig. 3.22 On-wafer measurements have been perform using Agilent PNA U5227A up to 67 GHz. The VNA was calibrated using Short-Open-Load-Thru (SOLT) technique [79] with off-chip impedance standard substrate (ISS). The de-embedding technique from [69] is used. Figures 3.23 and 3.24 show comparisons for the common and differential mode per-unit-length resistance and inductance between the scalable model, closed-form expressions, EM simulation, and measurements. In this case, the signal and ground conductors are on M7. The width of the signal and ground conductors is 6 μm and 12 μm, respectively. The spacing between the signal and ground conductors is 8 μm and the spacing between the signal conductors is 5 μm.

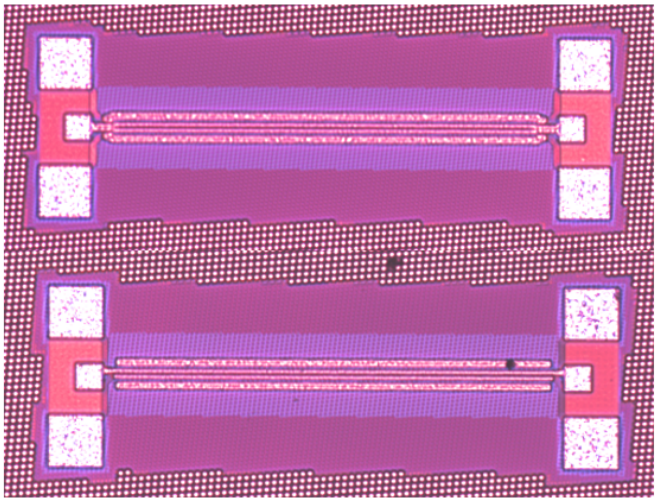

Figure 3.22: Die photo of fabricated coupled CPWs (top for even mode measurement and bottom for odd mode measurement).

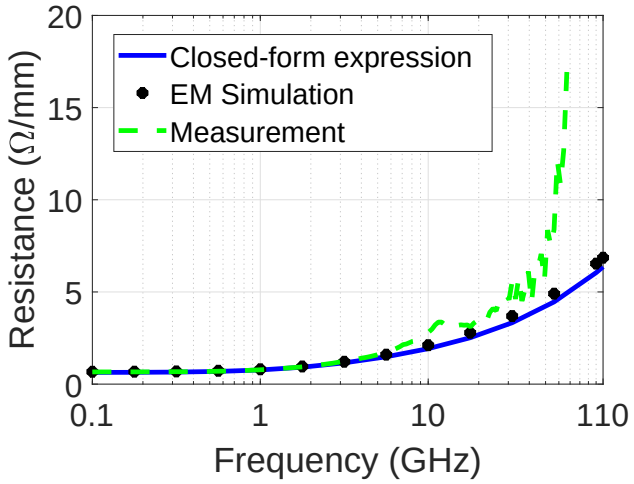

Figure 3.23: Comparison between measurement, EM simulation and closed-form expressions for per-unit-length common mode resistance in the coupled CPW transmission lines with w_s =6 μm, w_g =12 μm, s_s =5 μm and s_g =8 μm; the metal layer is on M7 in a TowerJazz 130nm RFCMOS process.

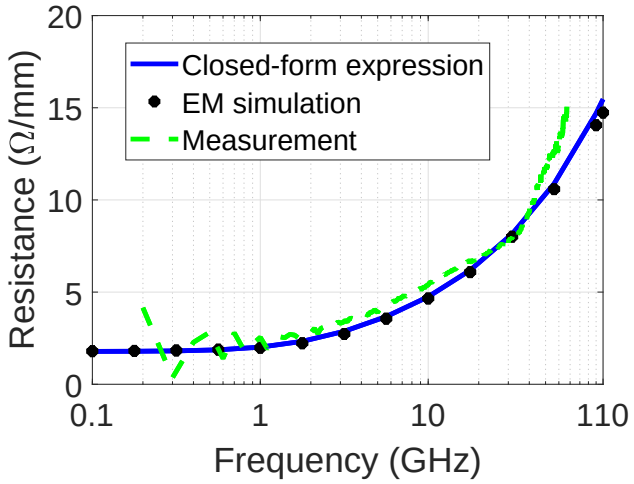

Figure 3.24: Comparison between measurement, EM simulation and closed-form expressions for per-unit-length differential mode resistance in coupled CPW transmission lines with w_s =6 μm, w_g =12 μm, s_s =5 μm and s_g =8 μm; the metal layer is on M7 in a TowerJazz 130nm RFCMOS process.

3.7 Mapping Closed-form Expressions to *RL* Foster Network

To develop an *RL* equivalent circuit model for the frequency-dependent resistance and inductance, we fit the *RL* network (Fig. 3.25) to our calculated frequency-dependent resistance response. One approach is to use optimization algorithms to perform curve fitting with optimum pole locations and minimal orders [81]. However, such procedures require extra resources or tools that may not be directly compatible with circuit simulators. To address this challenge, we fix the poles p_n in the frequency range of interest. The optimum pole locations of the cascaded *RL* sections are relaxed at the expense of minimally increasing the number of *RL* sections (order of the *RL* Foster network). The more *RL* sections are used, the better the overall accuracy that can be achieved. Based on our experimental simulations, four *RL* sections with fixed poles p_i at frequencies 1 GHz, 10 GHz, 50 GHz and 110 GHz were selected and are found to be sufficient to approximate the resistance response with less than 5% deviation from the closed-form expression. Pole p_i is expressed as

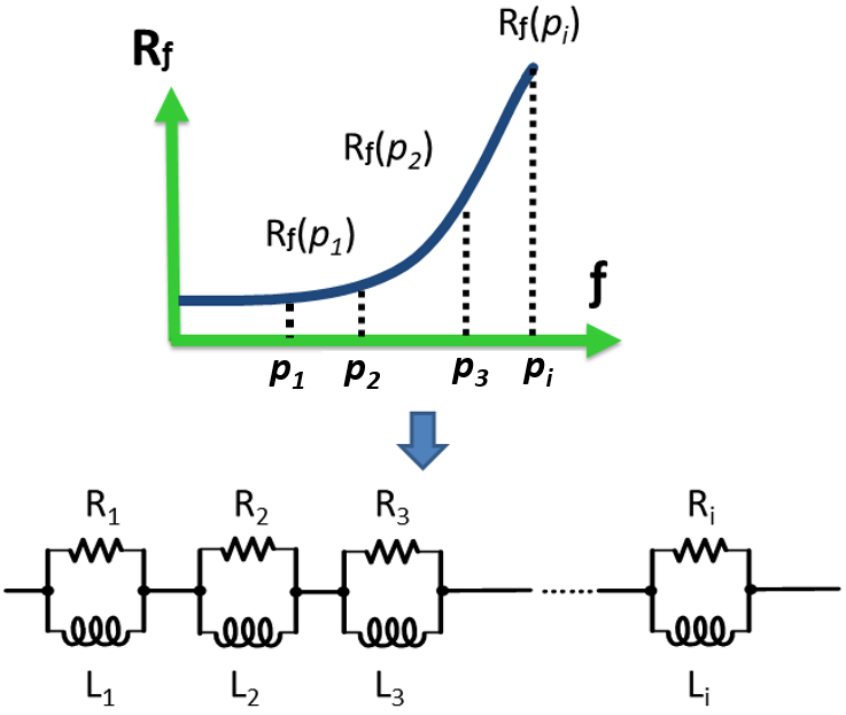

Figure 3.25: Diagram showing the mapping of a frequency-dependent resistance response to an RL network (DC inductance and resistance not shown); each pole p_i corresponds to an RL section.

$$p_i = \frac{R_i}{L_i} \ (i = 1, 2, 3, 4). \tag{3.37}$$

Assuming $R_f(p_i)$ is the total resistance value at pole frequency p_i, we have

$$R_f\left(p_i\right) = R_{DC} + \mathrm{Re}\left[\sum_{m=1}^{M} \frac{j p_i R_m L_m}{R_m + j p_n L_m}\right] \ (i = 1, 2, 3, 4)\,, \tag{3.38}$$

where M is the number of RL sections ($M = N = 4$). The corresponding matrix representation of the equation above can be expressed as

$$\begin{bmatrix} R_f(p_1) - R_{DC} \\ R_f(p_2) - R_{DC} \\ R_f(p_3) - R_{DC} \\ R_f(p_4) - R_{DC} \end{bmatrix} = \mathbf{A} \begin{bmatrix} R_1 \\ R_2 \\ R_3 \\ R_4 \end{bmatrix}, \tag{3.39}$$

where $\mathbf{A}$ is a 4×4 matrix with matrix components given as

$$A_{ij} = \frac{jp_i p_j}{p_j + jp_i} \ (i, j = 1, 2, 3, 4). \tag{3.40}$$

Then

$$\begin{bmatrix} R_1 \\ R_2 \\ R_3 \\ R_4 \end{bmatrix} = \mathbf{A}^{-1} \begin{bmatrix} R_f(p_1) - R_{DC} \\ R_f(p_2) - R_{DC} \\ R_f(p_3) - R_{DC} \\ R_f(p_4) - R_{DC} \end{bmatrix}. \tag{3.41}$$

Note that matrix $\mathbf{A}$ and its inverse only depend on the preselected poles and are independent of the parameters of the conductor; hence, the matrix elements can be precomputed and the equations for the resistor elements can thus be implemented directly in common circuit simulators. The corresponding inductance element values are obtained from the resistances together with the known poles as

$$\begin{bmatrix} L_1 \\ L_2 \\ L_3 \\ L_4 \end{bmatrix} = \begin{bmatrix} p_1 & 0 & 0 & 0 \\ 0 & p_2 & 0 & 0 \\ 0 & 0 & p_3 & 0 \\ 0 & 0 & 0 & p_4 \end{bmatrix} \begin{bmatrix} R_1 \\ R_2 \\ R_3 \\ R_4 \end{bmatrix}. \tag{3.42}$$

The high-frequency inductance L_∞ is derived from the DC inductance by subtracting the inductance elements in the RL Foster network. The DC inductance can be calculated from closed-form formulas for the self and mutual partial inductances for linear conductors [64]. The DC inductance for the inductor can be expressed as

$$L_{DC} = \sum L_{ii} + \sum_{i \neq j} M_{ij}, \tag{3.43}$$

where L_{ii} and M_{ij} are the partial self-inductance of each segment i and partial mutual inductance between segments i and j, respectively. The mutual inductance calculation can be further simplified by utilizing the symmetry of the structure.

We have applied this approach for the development of equivalent RL circuit models for the common and differential modes of the fabricated coupled CPW discussed in Section 3.6. The equivalent circuit model for common or differential mode is illustrated in Fig. 3.26. The complete RL model for coupled CPWs is illustrated in Fig. 3.27. The circuit values for common and differential modes are shown in Tables 3.1 and 3.2, respectively. As shown in Figs. 3.28 and 3.29, the RL circuit model matches well with the closed-form expression calculations. Meanwhile, the inductance response is also captured well by the circuit model, for both common and differential mode.

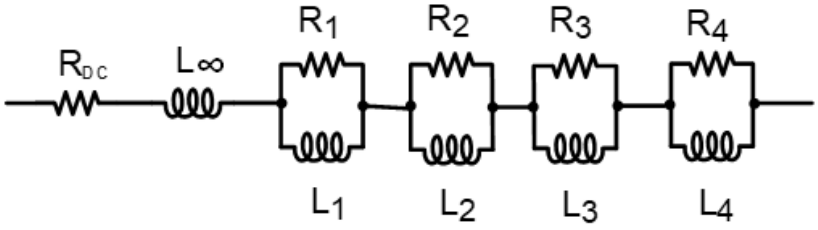

Figure 3.26: RL circuit model for common or differential mode.

Table 3.1: Per-Unit-Length Circuit Element Values for Common Mode

R_{DC}	R_1	R_2	R_3	R_4
0.6	0.23	1.97	1.30	5.05
L_∞	L_1	L_2	L_3	L_4
303.9	36	31.3	3.67	7.3

*unit: pH/mm for L, Ω/mm for R.

Table 3.2: Per-Unit-Length Circuit Element Values for Differential Mode

R_{DC}	R_1	R_2	R_3	R_4
1.79	0.36	4.8	3	12.2
L_∞	L_1	L_2	L_3	L_4
429	57.5	76.8	8.6	17.7

*unit: pH/mm for L, Ω/mm for R.

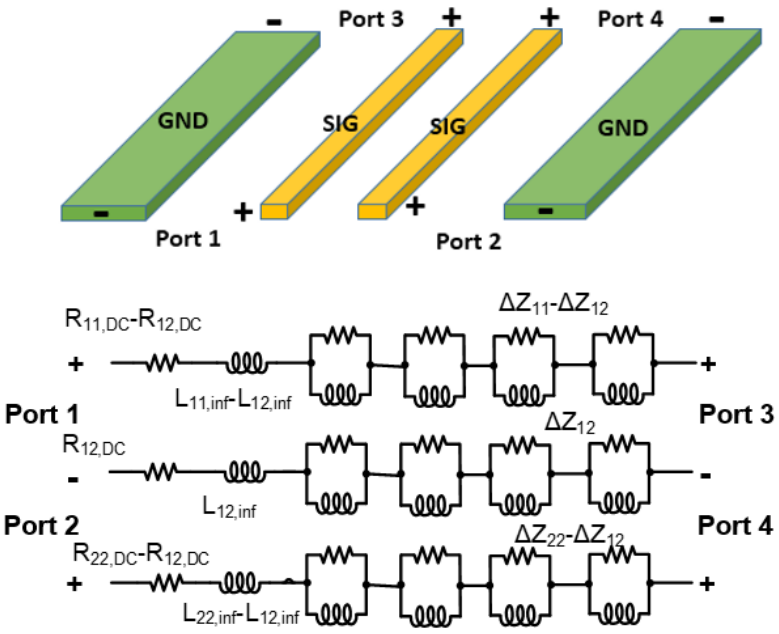

Figure 3.27: Complete RL circuit model for couple CPWs.

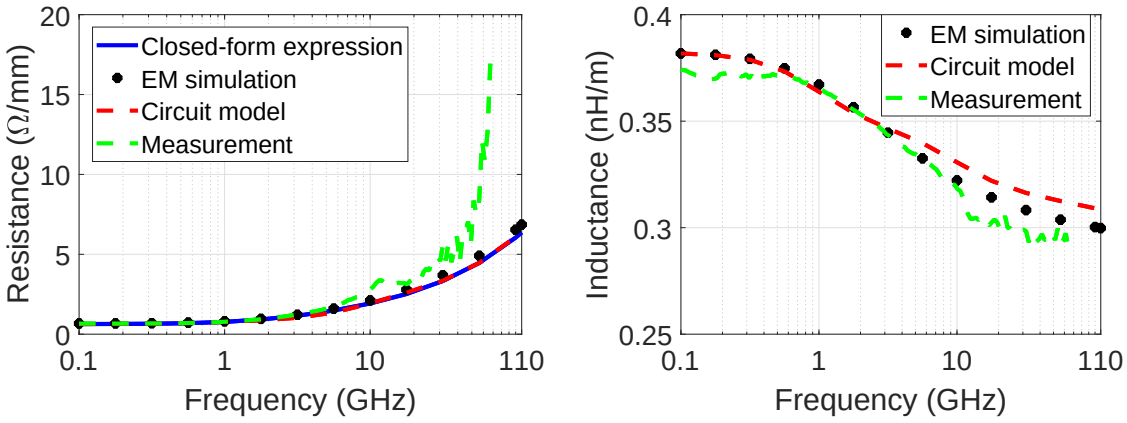

Figure 3.28: Comparison between measurement, EM simulation, closed-form expressions and circuit model for per-unit-length common mode resistance and inductance in coupled CPW transmission lines with w_s =6 μm, w_g =12 μm, s_s =5 μm and s_g =8 μm; the metal layer is on M7 in a TowerJazz 130nm RFCMOS process.

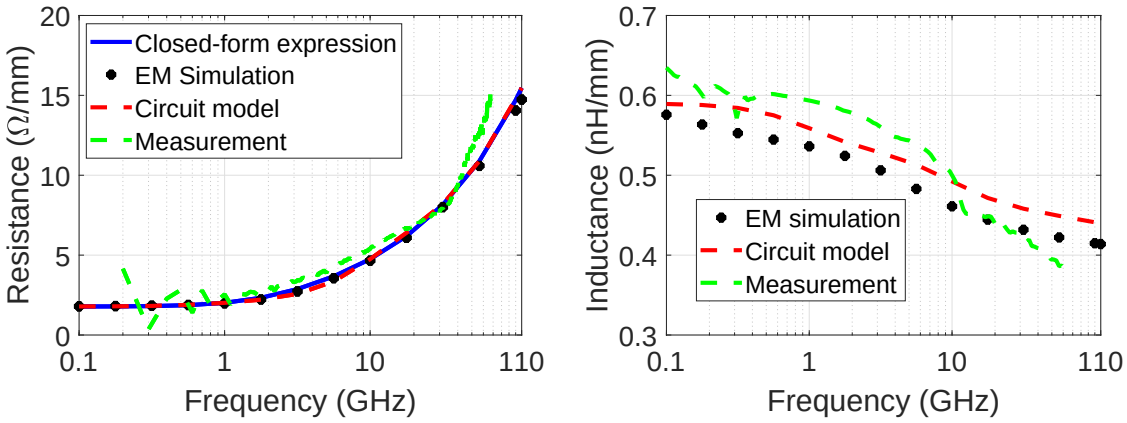

Figure 3.29: Comparison between measurement, EM simulation, closed-form expressions and circuit model for per-unit-length differential mode resistance and inductance in coupled CPW transmission lines with w_s =6 μm, w_g =12 μm, s_s =5 μm and s_g =8 μm; the metal layer is on M7 in a TowerJazz 130nm RFCMOS process.

3.8 Substrate Eddy Current Effects

In addition to conductor loss, eddy current effects will also occur in heavily-doped silicon substrates (on the order of $0.01\Omega\cdot$cm or even less), which are commonly used in digital processes, as discussed in Chapter 1. To include substrate eddy-current loss in our scalable models, the complex image approach [82] [83] is adopted. As illustrated in Figs. 3.30 and 3.31, image conductors are placed below the real inductors at a complex distance $2h_{\text{eff}}$ with opposite currents. These image conductors represent the impact due to the substrate eddy currents in the silicon substrate. With backside metallization, the complex height h_{eff} is given by

$$h_{\text{eff}} = h_{\text{ox}} + \frac{1-j}{2}\delta_{\text{si}} \tanh\left(\frac{(1+j)\,h_{\text{si}}}{\delta_{\text{si}}}\right) \tag{3.44}$$

where h_{ox} is the oxide thickness, h_{si} is the bulk thickness, and δ_{si} is the skin depth of the silicon substrate given in (1.3).

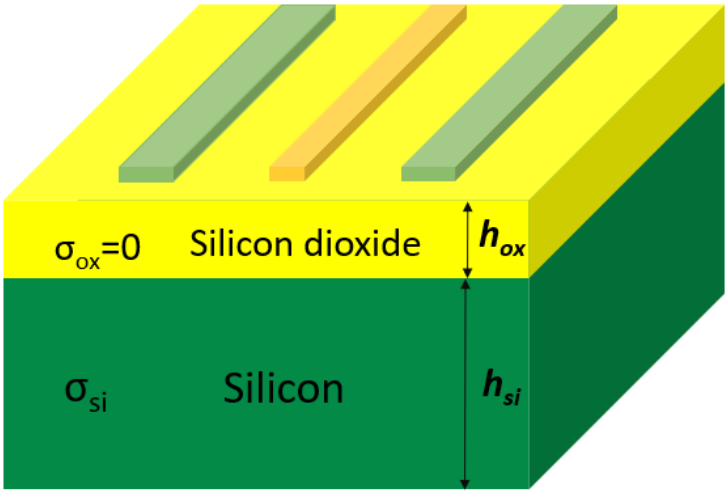

Figure 3.30: An example CPW on lossy silicon substrate.

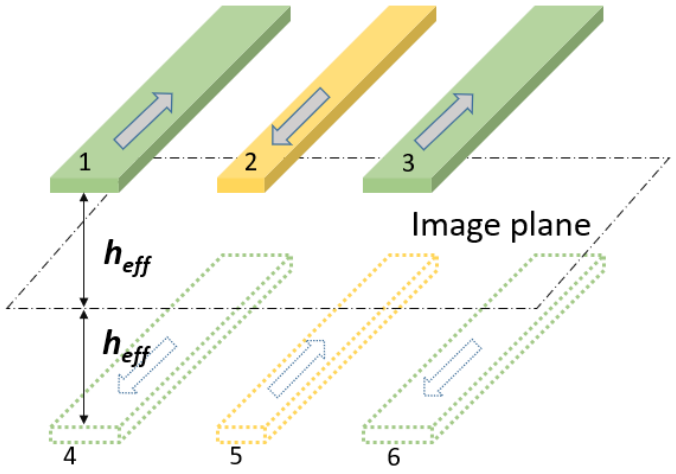

Figure 3.31: Image conductors with opposite current.

The currents of the image conductors are in opposite direction. The complex inductance matrix of the CPW can be formulated as

$$[L_{cf}] = \begin{bmatrix} L_{11} - L_{14} & L_{12} - L_{15} & L_{13} - L_{16} \\ L_{12} - L_{24} & L_{22} - L_{25} & L_{23} - L_{26} \\ L_{13} - L_{34} & L_{23} - L_{35} & L_{33} - L_{36} \end{bmatrix}. \tag{3.45}$$

The partial self and mutual inductances can be derived using e.g., Wheeler's equation. The total loop inductance (L^*_{total}) can be formulated as a linear combination of partial self and mutual inductances through matrix reduction, once the relative current ratios and directions are known. As we can see, L^*_{total} is complex and frequency dependent since the complex distance is frequency dependent. Thus, the frequency-dependent inductance and resistance are obtained as

$$L\left(\omega\right)_{\text{total}} = \text{Re}\left[\text{L}\left(\text{h}_{\text{eff}}\right)^*_{\text{total}}\right] \tag{3.46}$$

and

$$R\left(\omega\right)_{\text{eddy}} = -\omega\text{Im}\left[\text{L}\left(\text{h}_{\text{eff}}\right)^*_{\text{total}}\right]. \tag{3.47}$$

To verify the overall model performance including conductor and substrate eddy-current

losses, we have designed and measured a CPW in TowerJazz CA13 130nm RFCMOS process with low substrate resistivity. The width of the signal conductor is 6 μm. The ground width is 12 μm and spacing between the ground and signal conductor is 8 μm. Figures 3.32 and 3.33 show a comparison between the closed-form expression, HFSS simulation, circuit model and measurement for the frequency-dependent series resistance and inductance due to both conductor loss and the eddy-current loss in silicon substrate. The model and measurement agree well with each other over the broad frequency.

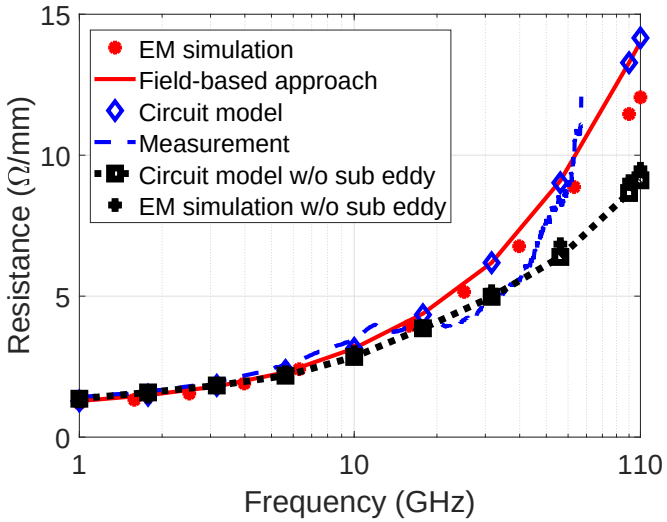

Figure 3.32: Comparison between measurement, EM simulation, closed-form expressions and RL model for per-unit-length resistance for a CPW with/without substrate eddy current effects; for the CPW, $w_s = 6$ μm, $w_g = 12$ μm and $s = 8$ μm.

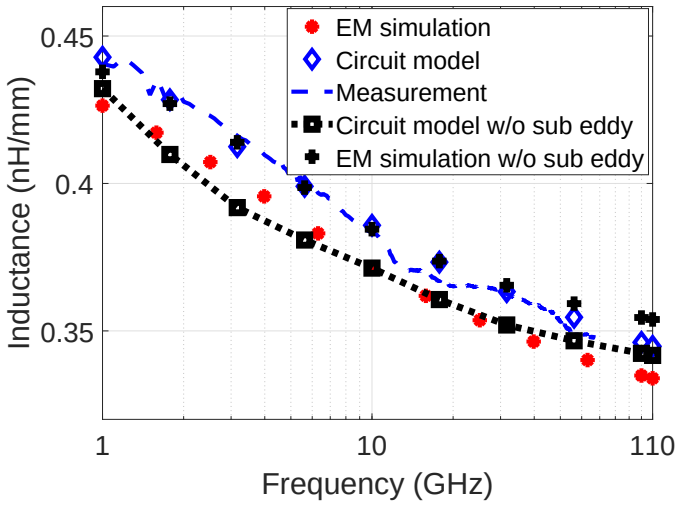

Figure 3.33: Comparison between measurement, EM simulation and RL model for per-unit-length inductance for CPW with/without substrate eddy current effects; for the CPW, $w_s = 6$ μm, $w_g = 12$ μm and $s = 8$ μm.

3.9 Conclusion

In this chapter, we have presented a systematic field-based approach to model the frequency-dependent resistance and inductance for multi-conductor interconnects. Empirical forms for skin effect and proximity effect have been developed for a wide width-over-thickness geometry range from 1 to 15 respectively. The L2-norm error for the empirical formulas is within 7%. We have applied this technique to develop scalable wideband equivalent circuit models for the p.u.l. resistance and inductance for on-chip CPW and coupled CPWs. The error for a wide range of CPWs at three example frequencies (i.e., 1 GHz, 60 GHz and 110 GHz) is below 10%. To validate our models, we also fabricated test chips and performed on-wafer measurements. The models show good agreement with both simulation and measurements of the test chip. The substrate eddy-current effects are also captured using the complex imaging approach. The measurements and model for a test chip fabricated with low-resistivity silicon substrate are shown to match well.

Chapter 4: Scalable Equivalent Circuit Model for On-Chip mmWave Inductors

4.1 Introduction

This chapter presents a fully scalable equivalent circuit model for on-chip mmWave spiral inductors, which are an integral part of mmWave on-chip circuits. This circuit model is directly compatible with standard circuit simulation tools. In the previous chapter, we have developed a systematic modeling methodology to capture the frequency-dependent resistive losses in the conductors of a transmission line due to skin and proximity effects from DC to mmWave frequencies. To develop the scalable model for on-chip spiral inductor, we adopt the commonly used π-topology [84] [85] for on-chip inductors and modify it for scalability and broad bandwidth. In the previous chapter, we already have developed closed-form expressions for the frequency-dependent resistance due to skin and proximity effects, and have mapped these expressions to a Foster RL network consisting of ideal parameterized elements. For the silicon substrate, we adopt the conventional CGC shunt model [86] to capture the frequency-dependent shunt capacitance and conductance. In addition, substrate eddy-current loss and metal fill effects are also included in the scalable model. We have applied the modeling methodology to example on-chip inductors and have validated our models through both full-wave simulations and measurements of a fabricated test chip [87]. Our modeling methodology is suitable for mmWave inductors over a wide geometry range and across different process nodes.

4.2 Circuit Model Topology for On-Chip mmWave Spiral Inductor

The circuit topology of our model for on-chip mmWave spiral inductors (illustrated in Fig. 4.1) is comprised of three parts: a series RL Foster network, two shunt CGC branches, and the port-to-port capacitance C_p. RF/mmWave IC designs usually adopt a process with thick top metal and high-resistivity silicon substrate to reduce loss in the metallization layers and the silicon substrate, respectively. The loss in the metallization

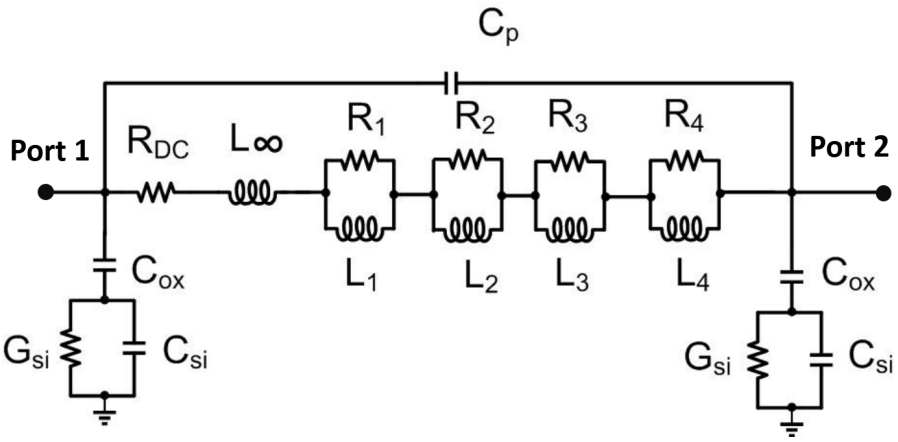

Figure 4.1: Modified π model with Foster RL network.

layers is enhanced due to both skin effect and proximity effects. In the circuit model, the RL Foster network, including a series resistor (R_{dc}) and a series inductor (L_{∞}), captures the frequency-dependent resistance and inductance in the metal wiring. C_p represents the port-to-port capacitance, which models the inter-winding capacitance of the spiral coil. The CGC shunt circuits capture the frequency-dependent capacitance and conductance due to inter-layer dielectric (ILD) and silicon substrate. For typical high-resistivity substrates used for RF/mmWave designs, the substrate acts as lossy dielectric. Eddy-current loss in the silicon substrate is negligible and thus has negligible influence on the frequency-dependent series resistance and inductance. Loss in the ILD is also negligible when compared with silicon substrate loss. Thus, in the CGC model, C_{ox} is the capacitance due to the ILD, which is constant over the frequency range. C_{si} and G_{si} represent the shunt capacitance and shunt conductance, respectively due to the silicon substrate. This model is valid for symmetrical inductor since the two CGC branches are identical. For non-symmetrical inductor, the model topology is still valid but two CGC branch values need to be redistributed. This circuit model for spiral inductor is fully scalable and the circuit elements are frequency-independent, which are functions of geometrical and material parameters.

4.2.1 Modeling Conductor Frequency-Dependent Resistance in Inductors

4.2.1.1 Skin and Proximity Resistances

As for transmission line discussed in Chapter 3, the increased resistance in the spiral due to the conductor skin effect can be expressed in a functional form similar to (3.11) as

$$R_{\text{skin}} = R_{\text{dc}} F_{\text{skin}} \left(\frac{wt}{\delta^2}, \frac{w}{t} \right), \tag{4.1}$$

where here $R_{\text{dc}} = l_{\text{total}}/(wt\sigma)$ and l_{total} is the total conductor length of the spiral inductor.

When multiple parallel conductor segments of on-chip spiral inductors are in close proximity, the resistance increase due to the proximity effect also needs to be taken into account, particularly for multi-turn inductors. Using the field-based approach described in Section 3.4, the resistance equation for proximity effect can be formulated as

$$R_{\text{prox}} = l_{\text{seg}} \frac{\left|\vec{H}_a\right|^2}{\sigma I^2} F_{\text{prox}} \left(\frac{wt}{\delta^2}, \frac{w}{t} \right), \tag{4.2}$$

where l_{seg} is the total length of the conductor segment in which the proximity effect is considered and $\vec{H}_a$ is the average applied magnetic field along the conductor. To model the proximity effect, only the parallel conductors on the same side are considered since they are close to each other, as illustrated in Figs. 4.2 and 4.3. The increasing resistance due to the proximity effect on the parallel conductors on one side of the spiral can be expressed as

$$R_{\text{prox}} = l_{\text{side}} \frac{\left|\vec{H}_a\right|^2}{\sigma I^2} F_{\text{prox}} \left(\frac{wt}{\delta^2}, \frac{w}{t} \right), \tag{4.3}$$

where the average magnetic field is taken as

$$\left|\vec{H}_a\right|^2 = \frac{1}{w} \int_0^w \left| \frac{I}{2\pi (s_1 + x)} \right|^2 dx \tag{4.4}$$

and l_{side} is the length of the parallel segment ($s_2 + w$ or $s_3 + w$). Given the resistance increases in (4.1) and (4.2) due to both proximity and skin effects, the total resistance

of the spiral inductor is obtained as

$$R_{\text{total}} = R_{\text{skin}} + R_{\text{prox}}. \tag{4.5}$$

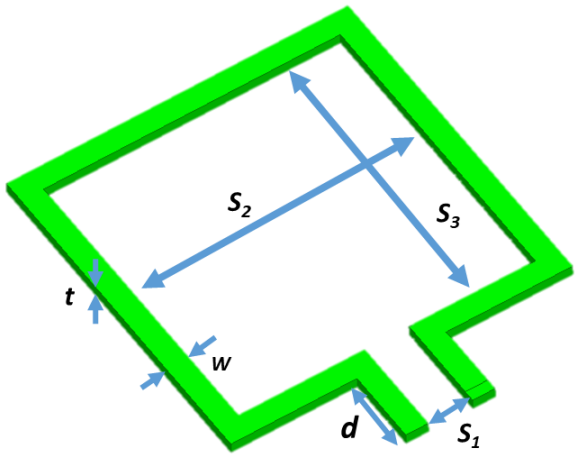

Figure 4.2: Layout for one-turn one-port spiral inductor.

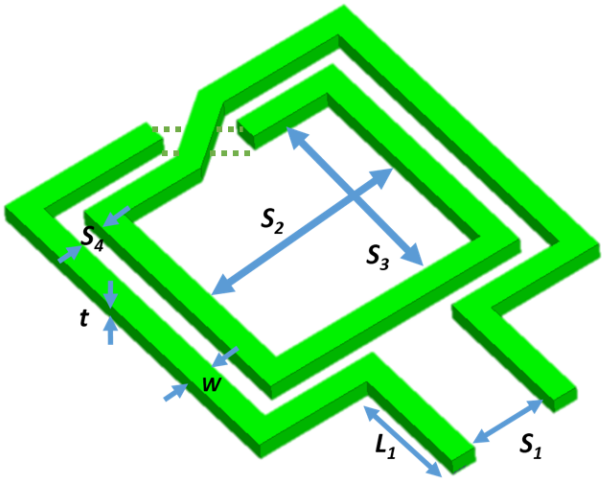

Figure 4.3: Layout for two-turn one-port spiral inductor.

Figures 4.4 and 4.5 show a comparison of our closed-form expressions with quasi-

magnetostatic simulation results (ANSYS Maxwell [77]). For both inductors, the conductor width is 6 μm, the thickness is the same as the top metal layer thickness in a TowerJazz 180 nm BiCMOS process, and the conductor conductivity is assumed to be 3.8×10^7 S/m. Our closed-form formulas match well with the EM simulation.

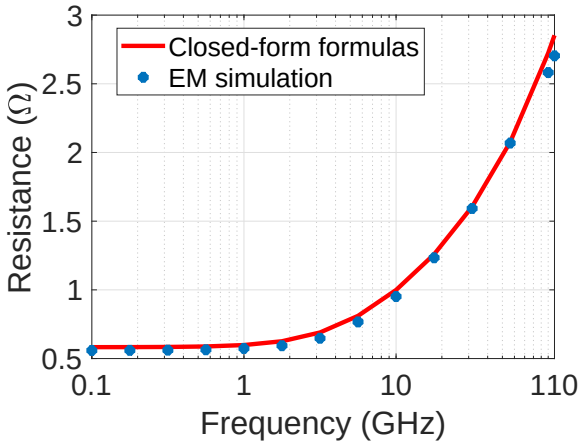

Figure 4.4: Comparison of the series resistance determined by closed-form formulas and EM simulations for a one-turn inductor; the conductor width is 6 μm and size is 70 μm by 70 μm.

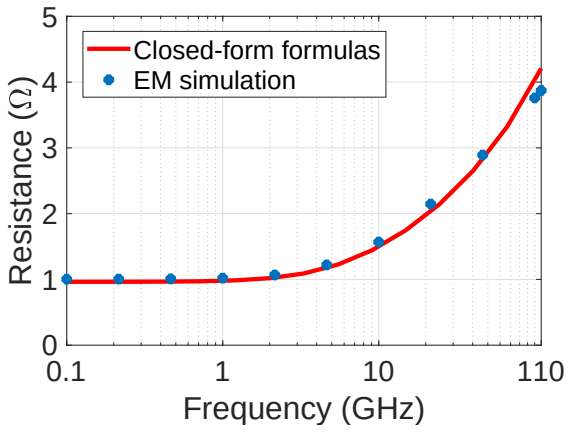

Figure 4.5: Comparison of the series resistance determined by closed-form formulas and EM simulations for a two-turn inductor; the conductor width is 6 μm, inner size is 60 μm by 60 μm and outer size is 70 μm by 70 μm.

After obtaining the frequency-dependent resistance response, the equivalent RL circuit model in Fig. 4.1 is derived using the approach discussed in Section 3.7.

4.2.2 Modeling Silicon Substrate Effect

To capture the frequency-dependent substrate effects, the CGC shunt branch model is derived based on the characteristics of the corresponding metal-insulator-semiconductor (MIS) transmission line [88]. We have adopted closed-from empirical formulas from [89] for the circuit element values with the following parameters: conductor width, w, silicon substrate conductivity, σ_{si}, thickness of the silicon dioxide and silicon substrate, t_{ox} and t_{si}, respectively, and relative permittivity of the silicon dioxide and silicon substrate, ϵ_{ox} and ϵ_{si}, respectively. The parameter l is the total length of the spiral inductor wiring. The two CGC shunt branch networks are identical for spiral inductors with symmetrical layouts. The port-to-port capacitance (or feed-through capacitance), C_p, is mainly due to the port feed line and an under-pass. Several closed-form expressions, such as those given in [90], are available that can be adopted to extract capacitance C_p. The closed-form expressions for the CGC branch elements (Fig. 4.7) implemented in our model are listed below [89]:

$$C_{\text{ox}} = \frac{l \times \epsilon_0 \epsilon_{\text{eff}}\left(\epsilon_{\text{ox}}, t_{\text{ox}}\right)}{2F\left(t_{\text{ox}}, w\right)} \tag{4.6}$$

$$C_{\text{si}} = \frac{l \times \epsilon_0 \epsilon_{\text{eff}}\left(\epsilon_{\text{si}}, t_{\text{si}}\right)}{2F\left(t_{\text{si}}, w\right)} \tag{4.7}$$

$$G_{\text{si}} = \frac{l \times \sigma_{\text{si}}\left[1 + \left(1 + 10t_{\text{si}}/w\right)^{-1/2}\right]}{4F\left(t_{\text{si}}, w\right)} \tag{4.8}$$

$$F(t,w) = \begin{cases} 1/2\pi \ln\left[8\frac{t}{w} + \frac{w}{4t}\right]; \frac{t}{w} \geq 1 \\ \left[\frac{w}{t} + 2.42 - 0.44\frac{t}{w} + \left(1 - \frac{t}{w}\right)^6\right]^{-1}; \frac{t}{w} \leq 1 \end{cases} \tag{4.9}$$

Figure 4.6 shows the equivalent Y-parameter model for on-chip spiral inductor. The shunt capacitance is defined as $\text{Im}(Y(\omega))/\omega$, and the conductance corresponds to $\text{Re}(Y(\omega))$, where $Y(\omega) = Y_{11} + Y_{12} = Y_{22} + Y_{12}$ since the inductor is symmetrical. Figures 4.8 and 4.9 show a comparison of the frequency dependent shunt capacitance and shunt conduc-

tance between the closed-form expressions for one of the CGC branches (two branches are identical), HFSS and Q3D [91] for a test MIS structure in TowerJazz BiCMOS 180 nm process. The spiral is on metal layer M6. The conductor width is 6 μm and the total length of the spiral is 180 μm. In terms of the results, frequency-dependent C and G can be obtained from Q3D directly. For HFSS simulation, the simulated S parameter were converted to Y matrix, from which $Y(\omega)$ was derived.

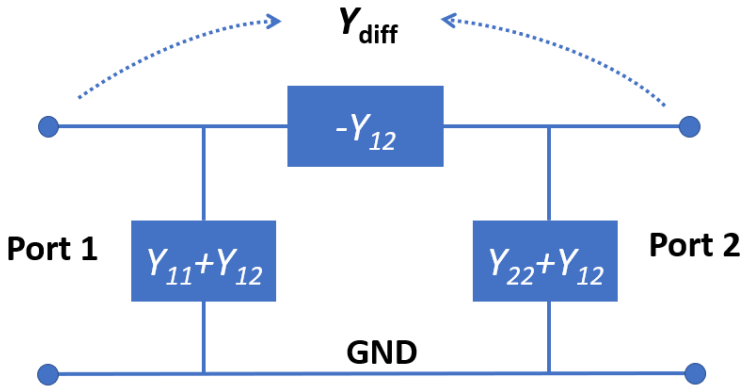

Figure 4.6: Equivalent Y-parameter model for on-chip spiral inductor.

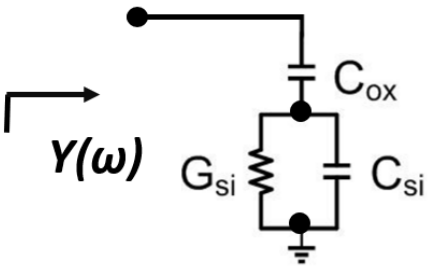

Figure 4.7: Frequency-dependent admittance Y(ω) of the CGC model.

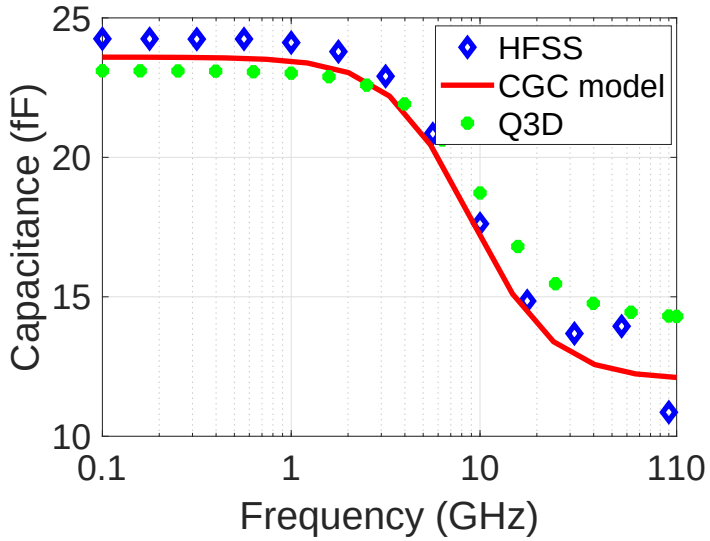

Figure 4.8: Comparison of frequency-dependent shunt capacitance between closed-form expressions for one *CGC* branch and EM simulations (HFSS and Q3D).

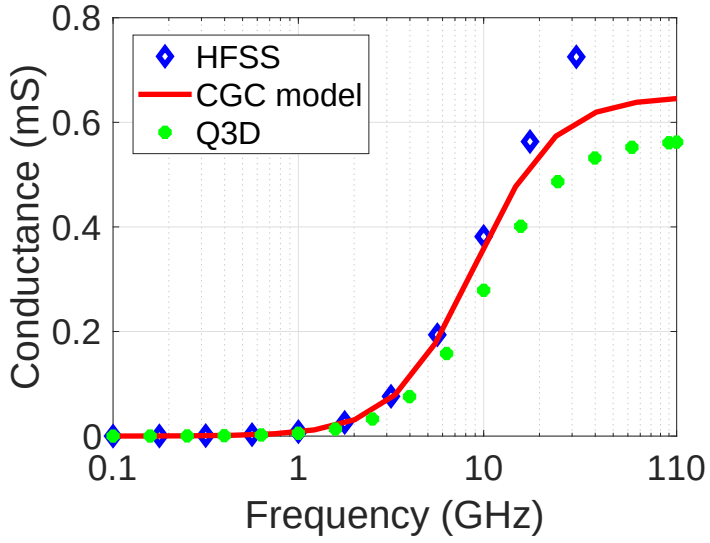

Figure 4.9: Comparison of frequency-dependent shunt conductance between closed-form expressions for one *CGC* branch and EM simulations (HFSS and Q3D).

In additional to $Y(\omega)$, other electrical performance parameters such as resistance, inductance and quality factor Q can also be derived from Y matrix. For differential spiral inductor, R_{12} is defined as

$$R_{12} = \mathrm{Re}\left(-\frac{1}{\mathrm{Y}_{12}}\right). \tag{4.10}$$

L_{12} is

$$L_{12} = \frac{\mathrm{Im}\left(-\frac{1}{\mathrm{Y}_{12}}\right)}{\omega}. \tag{4.11}$$

The differential quality factor Q is expressed as

$$Q = \frac{\mathrm{Im}\left(\frac{1}{\mathrm{Y}_{\mathrm{diff}}}\right)}{\mathrm{Re}\left(\frac{1}{\mathrm{Y}_{\mathrm{diff}}}\right)}. \tag{4.12}$$

For single-ended spiral inductor, R_{11} is defined as

$$R_{11} = \mathrm{Re}\left(-\frac{1}{\mathrm{Y}_{11}}\right). \tag{4.13}$$

L_{11} is

$$L_{11} = \frac{\mathrm{Im}\left(-\frac{1}{\mathrm{Y}_{11}}\right)}{\omega}. \tag{4.14}$$

The quality factor for single-ended spiral inductor is formulated as

$$Q_{11} = \frac{\mathrm{Im}\left(\frac{1}{\mathrm{Y}_{11}}\right)}{\mathrm{Re}\left(\frac{1}{\mathrm{Y}_{11}}\right)}. \tag{4.15}$$

4.3 Model Validation

To validate our scalable model for on-chip spiral inductor, we have fabricated a test chip with a representative inductor in a TowerJazz 130nm RFCMOS process. The inductor is fabricated on metal layer M7 and the width of the conductor is 2.5 μm. The side length is 70 μm. Figures 4.10-4.12 show a comparison between measurement at room temperature, HFSS simulation and scalable model. The inductor was measured in single-ended configuration, where one port of the inductor was connected to the ground. R_{11}, L_{11} and Q are defined from (4.13) to (4.15), respectively. The results obtained with the

scalable model are in good agreement with simulation and measurement.

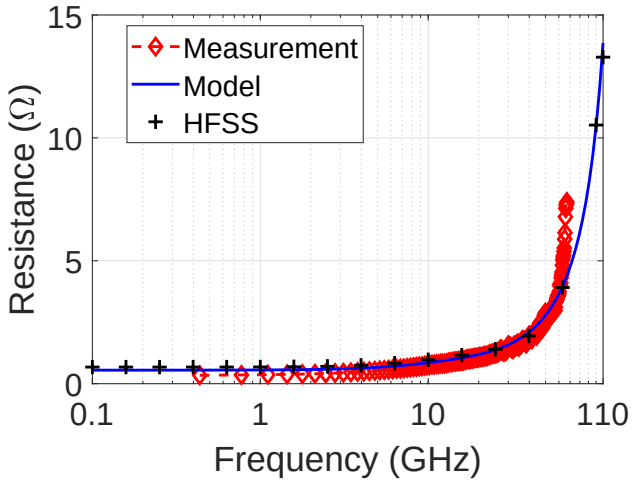

Figure 4.10: R_{11} for the single-ended spiral inductor.

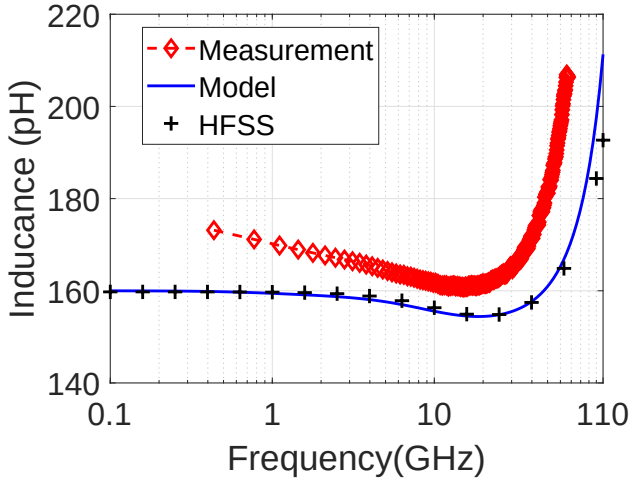

Figure 4.11: L_{11} for the single-ended spiral inductor.

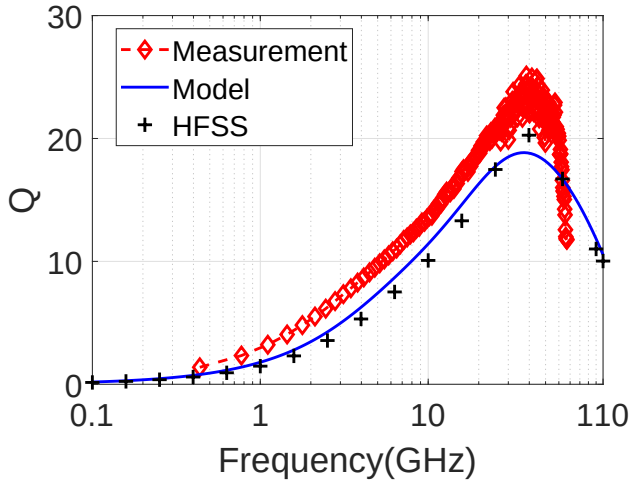

Figure 4.12: Comparisons of quality factor Q_{11}.

4.4 Temperature Effects

Our scalable models can directly capture temperature dependence of the conductor conductivity and its effect on the values of the equivalent circuit elements. As discussed in Section 2.10.1, if the metal conductivity changes due to temperature, the inductance elements in the model remain the same while all resistance values in the series branch of our equivalent circuit model will be altered based on the relation below

$$R_i\left(T\right) = \frac{\rho\left(T\right)}{\rho_0} R_i\left(T_0\right), \tag{4.16}$$

where $R_i(T_0)$ is the resistance value at temperature T_0, and $R_i\left(T\right)$ is the resistance value at temperature T. The dimensional dependences on temperature are negligible since the thermal expansion is insignificant.

We have simulated a test single-turn spiral inductor to evaluate our model's performance at different temperatures. For the test spiral inductor (Fig. 4.2), the width of the conductor is 6 μm, the feed line length d is 20 μm, and dimensions S_1, S_2 and S_3 are 12 μm, 80 μm, and 80 μm, respectively. We have included temperature dependence in our models and have simulated the temperature effects on the spiral inductor characteristics with both our model and a full-wave EM solver (HFSS). R_{12}, L_{12} and Q are defined

from (4.10) to (4.12), respectively. The accuracy of our scalable model as well as the non-negligible impact of temperature changes on the spiral inductor characteristics are illustrated in Figs. 4.13-4.15.

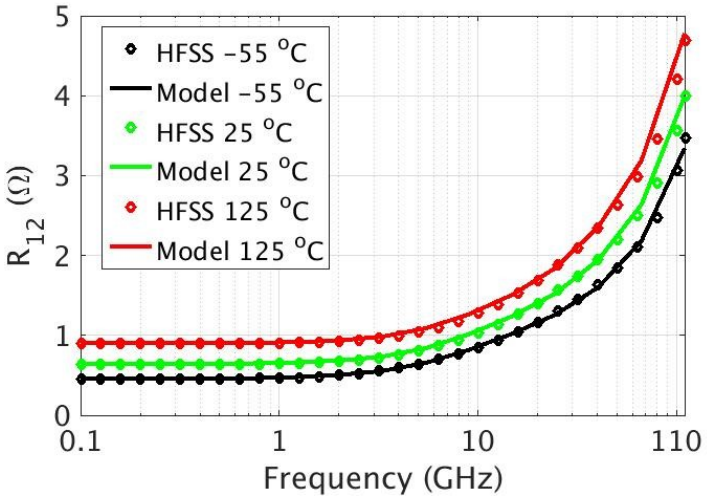

Figure 4.13: Scalable model capturing temperature effect on series branch R_{12} of a spiral inductor; The width of the conductor is 6 μm, the feed line length d is 20 μm, and dimensions S_1, S_2 and S_3 are 12 μm, 80 μm, and 80 μm, respectively.

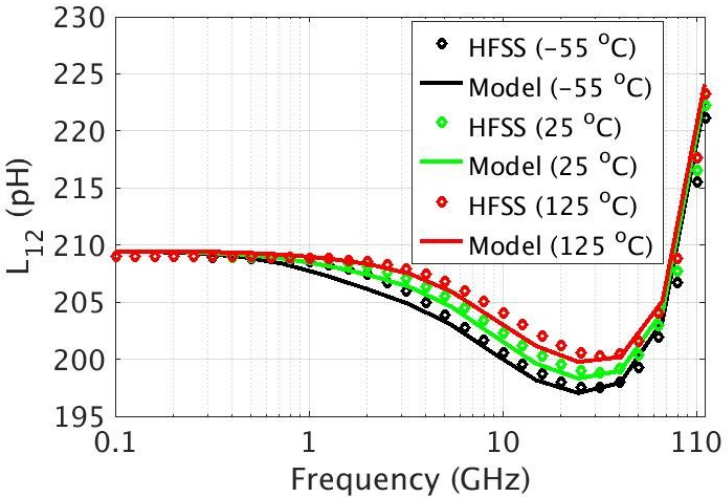

Figure 4.14: Scalable model capturing temperature effect on series branch L_{12} of a spiral inductor; The width of the conductor is 6 μm, the feed line length d is 20 μm, and dimensions S_1, S_2 and S_3 are 12 μm, 80 μm, and 80 μm, respectively.

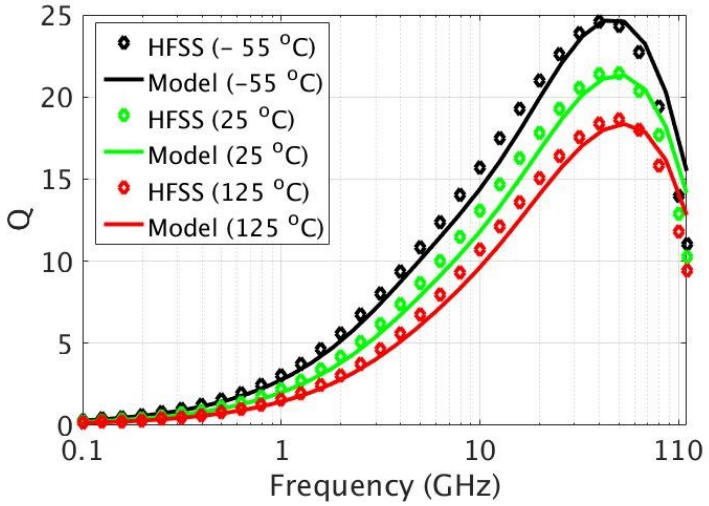

Figure 4.15: Scalable model capturing temperature effect on input quality factor (Q) of a spiral inductor; The width of the conductor is 6 μm, the feed line length d is 20 μm, and dimensions S_1, S_2 and S_3 are 12 μm, 80 μm, and 80 μm, respectively.

4.5 Metal Fill Effects

4.5.1 Closed-form Expressions for Metal Fill Losses

To include power loss in a spiral inductor due to metal fill (Fig. 4.16), not only the fills at top thick metal layers need to be taken into account, but also those in the lower metal layers since the skin depth at such high frequencies is comparable with the lower metal fill size. As illustrated in Fig. 4.17, the total power loss percentage in the lower metal layers (M5-M1) is increased significantly at mmWave frequencies compared with the loss incurred at lower frequencies (1 GHz and 10 GHz). The power loss in lower metal layers needs to be considered for accurate modeling of on-chip spiral inductor with metal fill.

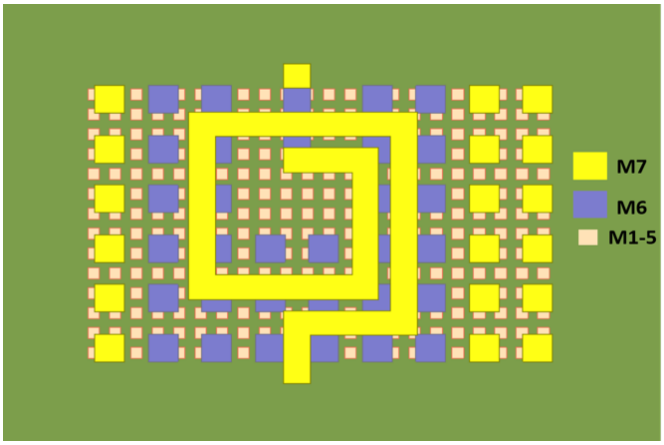

Figure 4.16: Example spiral inductor with 20% metal density and minimum metal fill size.

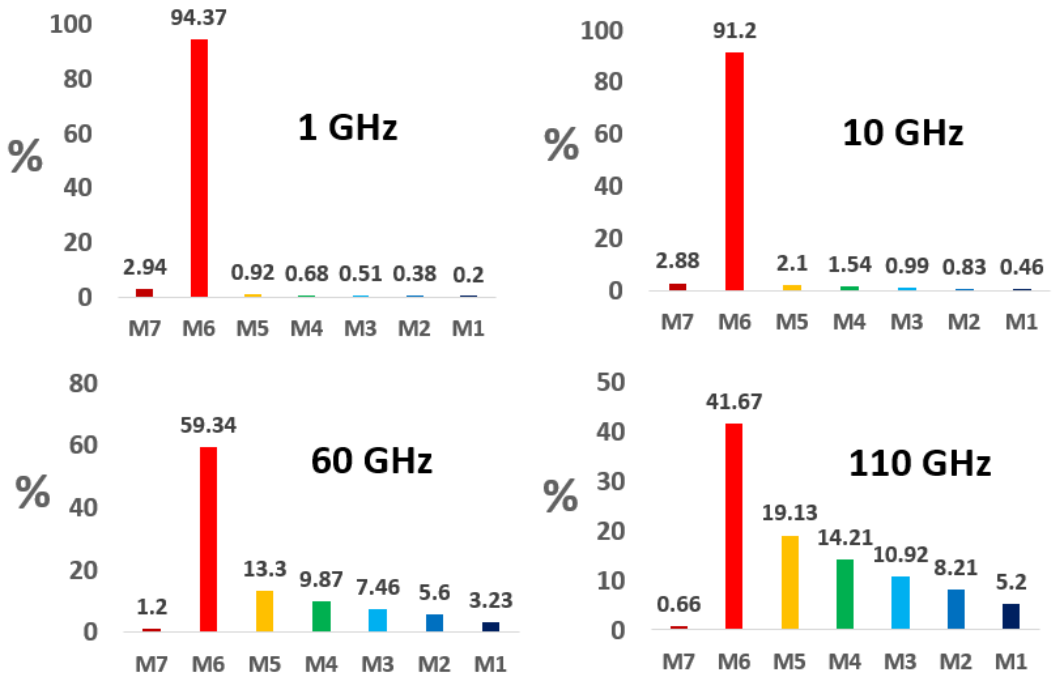

Figure 4.17: Metal fill power loss percentage for different metal layers at various frequencies (i.e., 1 GHz, 10 GHz, 60 GHz and 110 GHz).

To capture the power loss in metal fills, Shilimkar [92] has developed an approach to calculate the loss in a spatially arbitrary uniform magnetic field. This approach is based on the orthogonality of power loss due to the orthogonal magnetic field component, which is explained in Appendix C. The total power loss can be expressed in functional form for each field direction as [92]

$$P = \frac{w}{\sigma}\left[\left|\vec{H}_x\right|^2 G_{xy}\left(t/w, p\right) + \left|\vec{H}_y\right|^2 G_{xy}\left(t/w, p\right) + \left|\vec{H}_z\right|^2 G_z\left(t/w, p\right)\right] \tag{4.17}$$

Here $\vec{H}_x$, $\vec{H}_y$, and $\vec{H}_z$ are the x-, y-, z-direction components of the applied magnetic field towards the metal fill. w is the width of the square fill, t is the thickness, and p is the normalized frequency discussed in Chapter 2. Empirical expression for the G_{xy} function has been developed in [32]. An empirical expression for the G_z function has also been developed in [93] up to 50 GHz. To extend applicable frequency range of the

G_z function to 110 GHz, a new G_z function has been derived. For the development of the new G_z function, we first applied a uniform z-directed magnetic field on the metal fill with various width-over-thickness aspect ratios. Then we determined the power loss through the ANSYS Maxwell field calculator for the frequency range up to 110 GHz. We then approximate function $G_z(t/w, p)$ by a similar empirical expression in [93] with three parameters $k_i(t/w)$ (i=1, 2, 3) as

$$G_z\left(\frac{t}{w}, p\right) = \frac{k_1 p^2}{\left(k_2 p^2 + 1\right)^{k_3}}. \tag{4.18}$$

The empirical expression correctly provides the asymptotic behavior of metal fill loss at low and high frequencies. Discrete parameters $k_i(t_n/w_n)$ (i=1, 2, 3) are obtained by fitting function G_z to an extensive set of EM simulation data over the frequency range from DC to 110 GHz for different thickness-to-width ratios t_n/w_n between 0.015 and 2.78, which covers the size range for older to the most advanced process nodes. Then parameters $k_i(t_n/w_n)$ (i=1, 2, 3) are fitted to continuous t/w range using simple closed-form expressions as

$$k_i = \frac{\sum_{m=0}^{5} p_m^i \left(\frac{t}{w}\right)^m}{\sum_{n=0}^{5} q_n^i \left(\frac{t}{w}\right)^n} \ (i = 1, 2, 3). \tag{4.19}$$

The coefficients for the k_i functions are provided in the table below:

Table 4.1: Coefficients for k_i

	p_0	p_1	p_2	p_3	p_4	p_5
k_1	0	8.20e1	-6.55e1	2.41e1	-3.19	0
k_2	3.05e-5	1.97e-4	1.09e-2	-6.0e-3	9.57e-4	0
k_3	7.56e1	-3.60e1	6.14e1	5.89	3.27e1	-0.322
	q_0	q_1	q_2	q_3	q_4	q_5
k_1	4.90e2	-7.10	8.05e1	1	0	0
k_2	3.53e-1	-4.31e-4	1	-0	0	0
k_3	8.58e1	2.54e1	-1.31e1	6.89e1	2.85e1	1

4.5.2 Loss in Patterned Metal Fill Due to Line Current

To demonstrate this approach, we have applied this technique to a single layer of metal fill (illustrated in Figs. 4.18). Due to symmetry, only half of the metal fills are simulated in the field solver in order to reduce simulation time and memory requirements. The metal fill size is 2 μm $\times$ 2 μm and metal fill is placed with 30 % density. The conductivity is 3.8×10^7 S/m.

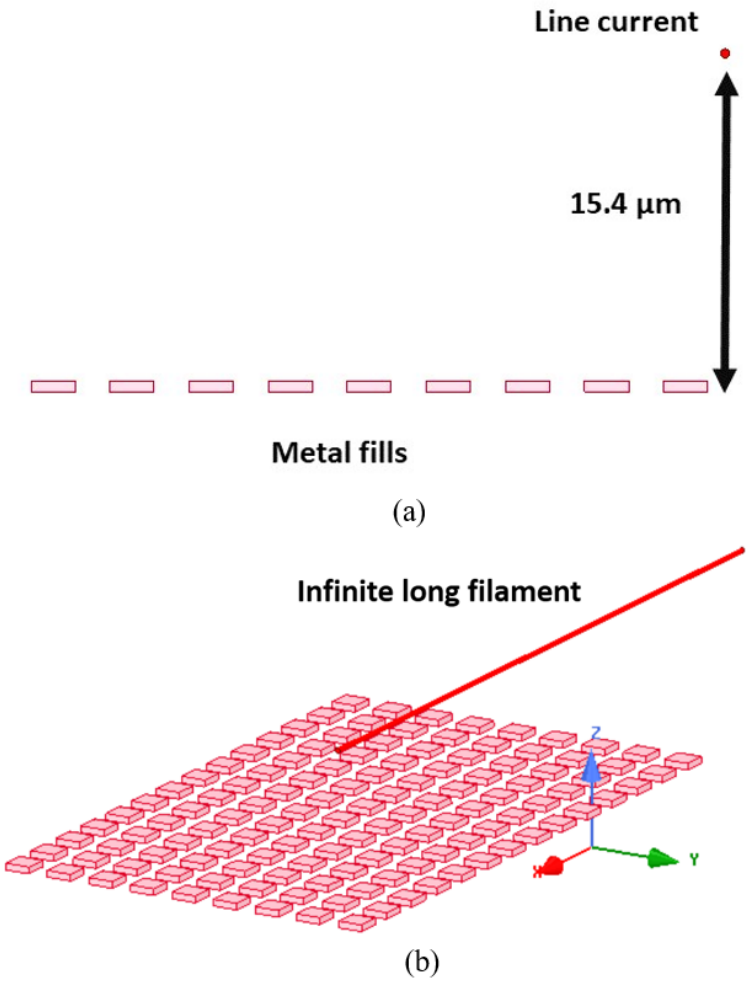

Figure 4.18: Single layer of metal fill under an infinite line current: (a) cross-sectional view, (b) 3D view.

Based on the coordinates of the line current and the metal fills, the magnetic field component along each coordinate axis can be derived through the closed-form expression given above. The power loss in each fill is calculated by [92]

$$P = \frac{w}{\sigma}\left[\left(\left|\vec{H}_x\right|^2 + \left|\vec{H}_y\right|^2\right) G_{xy}\left(t/w, p\right)) + \left|\vec{H}_z\right|^2 G_z\left(t/w, p\right)\right] \tag{4.20}$$

Then, the total power loss is the summation of the loss in each metal fill. Figure 4.19

shows the comparison between our closed-form formulas and EM simulation results by ANSYS Maxwell. ΔR is the increase in resistance due to the power loss in metal fill. The error over the entire frequency range is less than 5%.

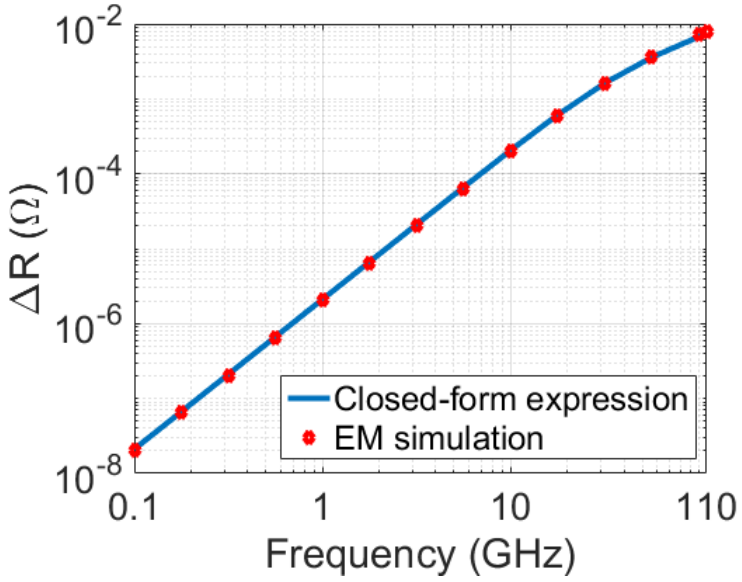

Figure 4.19: Metal fill loss calculated by the closed-form formulas and EM simulation.

4.5.3 General Formulation of H Fields for Spiral Inductors

To capture metal fill loss in spiral inductors, we first need to determine the magnetic fields. For efficient implementation, we discretize the spiral inductor geometry into segments [92] as shown in Fig. 4.20. We approximate each segment as a finite length current filament. The magnetic field at any point in 3D space is estimated using the analytical formula due to line current [46]. Then, we compute the total power loss due to metal fill through our empirical closed-form expressions given in (4.20). We have considered a 1.5-turn spiral inductor with 25 μm $\times$ 25 μm inner dimensions designed in TowerJazz 130nm RFCMOS process. The width of the segments is 4.5 μm and the spacing between turns is 1.5 μm. The metal fill size is 2 μm $\times$ 2 μm and is placed with 30% density on M5. We have limited metal fill to a single layer (M5) due to memory limitations for accurate EM simulations. EM simulation of metal fill loss in all layers

is prohibitive. Figure 4.21 shows a comparison between our model using closed-form expressions and EM simulation results. The model agrees well with the EM simulation results over a broad frequency range up to 110 GHz. It also illustrates that metal fill loss cannot be neglected at mmWave frequencies. Furthermore, in a fabricated spiral, metal fill is placed on all layers, and the associated loss will be significantly higher.

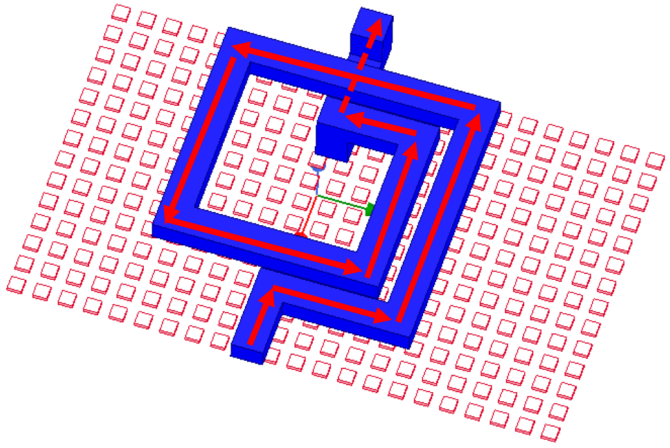

Figure 4.20: Line current approximation in spiral inductor (metal fills underneath).

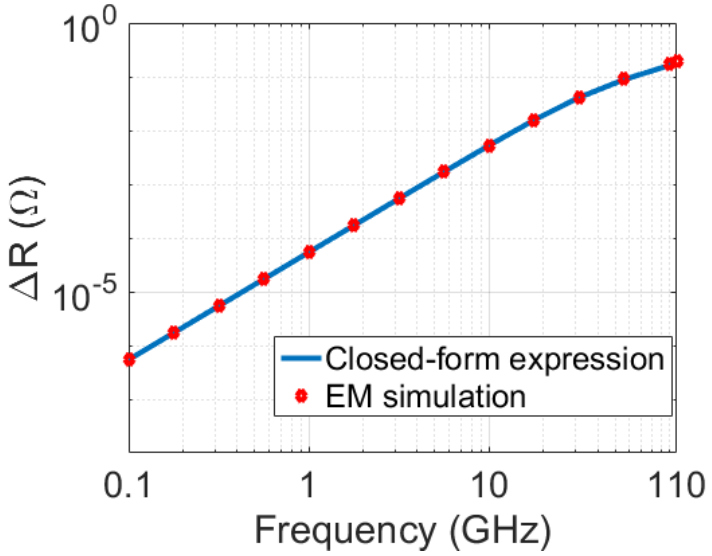

Figure 4.21: Metal fill loss comparison between the closed-form expression and EM simulation.

We have also fabricated a test chip with one-turn spiral inductor designed in TowerJazz 130nm RFCMOS process. The inner dimension is 67 μm $\times$ 67 μm. The width of the segments is 2.5 μm on M7. The metal fill size is 5 μm $\times$ 5 μm and is placed with 25% density on M7 and M6, 2 μm $\times$ 2 μm and 30% density on M5 to M1. Figures 4.22-4.24 are the comparisons between our equivalent circuit model and measurements. Resistance, inductance and Q_{11} are R_{11}, L_{11} and single-ended quality factor, respectively, which are defined in Section 4.3. The model agrees well with the measurement results over a broad frequency range. From Fig. 4.24, it can be clearly seen that metal fill loss is not negligible.

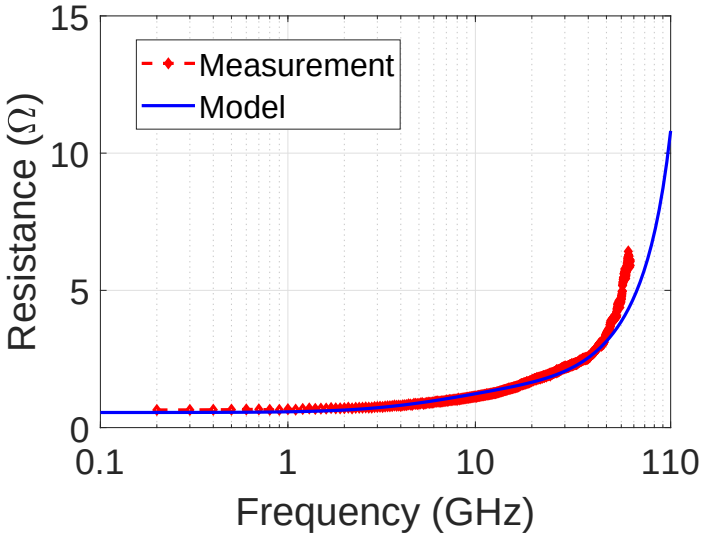

Figure 4.22: Comparison of resistance R_{11} between measurement and scalable model including metal fill effects.

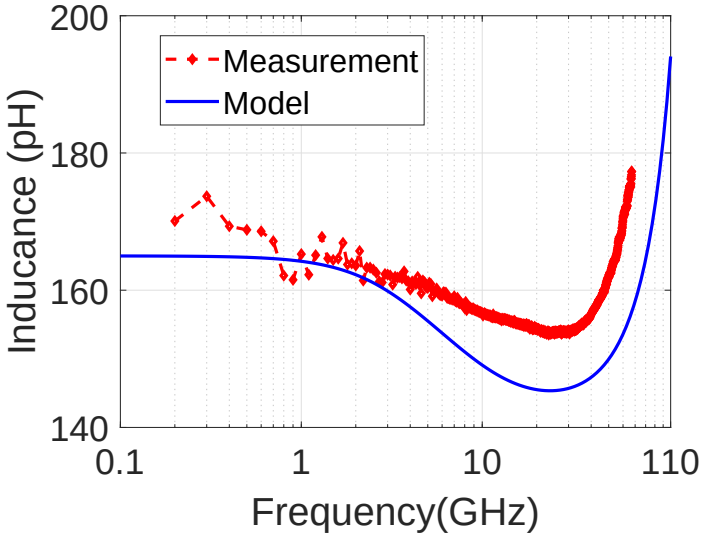

Figure 4.23: Comparison of inductance L_{11} between measurement and scalable model including metal fill effects.

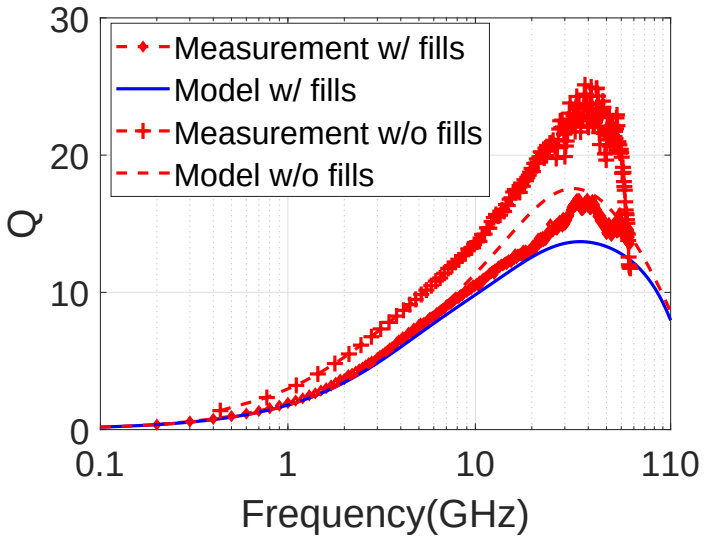

Figure 4.24: Comparison of Q_{11} between measurement and scalable model with and without metal fill effects.

4.6 Substrate Eddy-Current Loss in mmWave Inductors

We have also extended our scalable modeling techniques to capture substrate eddy-current loss using the complex image approach, which was discussed in Section 3.8. To verify our method, we have designed a one-turn spiral inductor with 50 μm $\times$ 50 μm dimensions in TowerJazz CA13 130nm RFCMOS process. The width of the segments is 4.5 μm. Figure 4.26 shows a comparison between the complex image approach and HFSS simulations for the frequency-dependent series resistance R_{11} due to the lossy silicon substrate only. The complex image model agrees well over the broad frequency range up to 110 GHz.

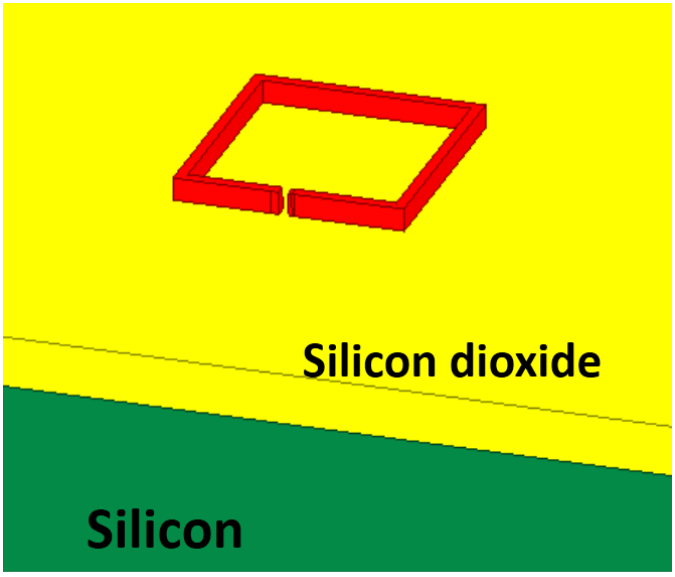

Figure 4.25: Spiral inductor in HFSS simulation setup.

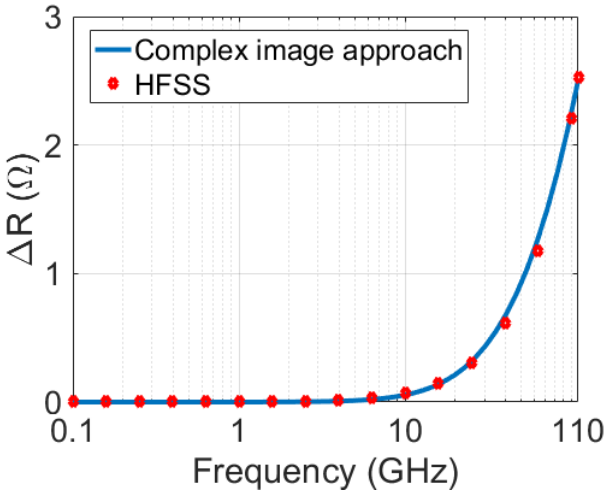

Figure 4.26: Comparison of series resistance calculation between complex image approach and HFSS simulation.

As illustrated in Fig. 4.27, a test chip with an example spiral inductor was also fabricated in TowerJazz RFCMOS 130nm process with low substrate resistivity. The

inductor is on M7. The width of the conductor is 2.5 μm and the side length is 70 μm. Figures 4.28-4.30 show the comparison between measurement and scalable model. Resistance, inductance and Q_{11} are R_{11}, L_{11} and single-ended quality factor, respectively. The one-port measurement was performed up to 67 GHz. One-port Short-Open-Load calibration was used. For de-embedding, open and short pad structures were designed on the chip and on-wafter measurement has been performed as well. Our model matches well with the measurement.

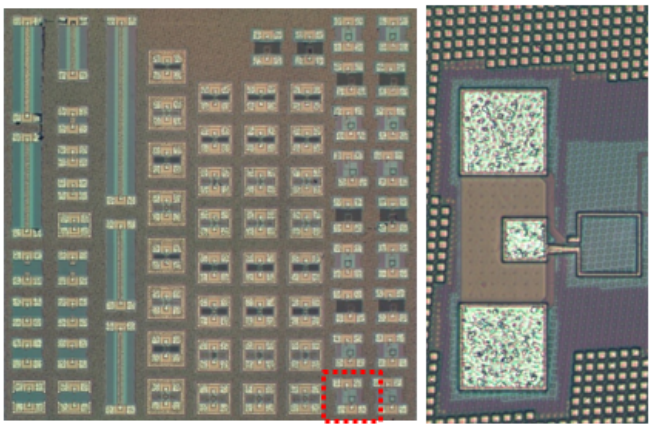

Figure 4.27: Die photo of the test chip and a spiral inductor.

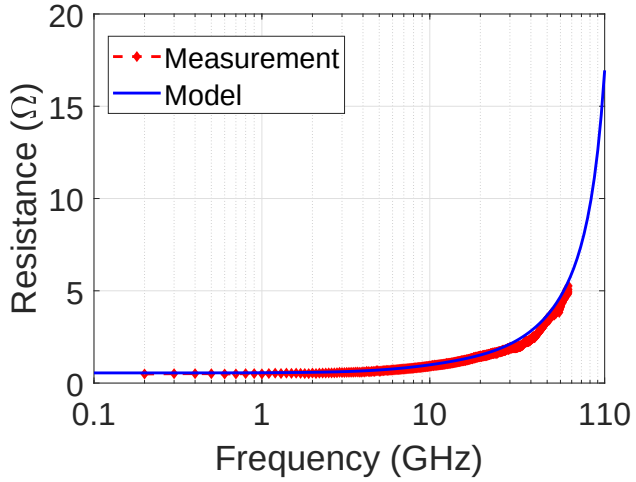

Figure 4.28: Comparison of resistance R_{11} between measurement and scalable model.

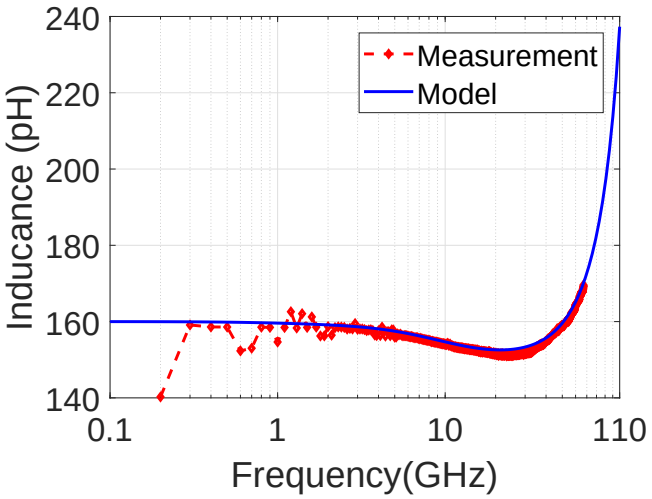

Figure 4.29: Comparison of inductance L_{11} between measurement and scalable model.

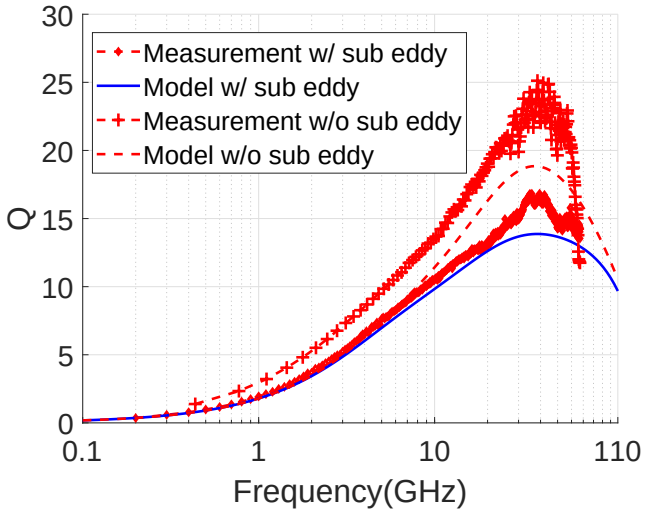

Figure 4.30: Comparison of Q_{11} between measurement and scalable model with and without substrate eddy-current effects.

4.7 Conclusion

In this chapter, we have extended our field-based scalable modeling approach developed in Chapter 3 for transmission lines to an on-chip spiral inductors. The scalable broadband equivalent circuit model topology for inductor is an extension of the traditional π model. Our field-based approach is used to capture the frequency-dependent resistance and inductance due to the skin and proximity effects in metallization layers. The substrate CGC model is adopted from literature [86]. The model also includes temperature dependence by simple scaling the series resistance values. Our model further includes substrate eddy current loss through the complex image approach. In addition, the metal fill loss at all metal layers is captured in our model. The model has been verified through both EM full-wave simulation and measurements of fabricated test structures. The model performance is in good agreement with both EM simulation and on-wafer measurements.

Chapter 5: Scalable Modeling of Magnetic Couplings between On-Chip mmWave Inductors

5.1 Introduction

We have discussed the scalable model for isolated spiral inductors in Chapter 4. On-chip passives, such as spiral inductors, often occupy a large chip area. Hence, compact layouts of spiral inductors are preferred to reduce chip size [94] [95] and cost. However, magnetic coupling between closely spaced spiral inductors may be significant and cannot be ignored [96] [97]. Therefore, it is crucial to capture the magnetic coupling between on-chip spiral inductors to enable parasitics-aware RF/mmWave IC design.

This chapter demonstrates a systematic modeling methodology to capture the broadband magnetic coupling characteristics between on-chip spiral inductors. Isolation improvement techniques to achieve both compactness and high isolation are also proposed. First, we discuss the general behavior of magnetic coupling in Section 5.2. Then, in Sections 5.3, a scalable and compact circuit model is proposed for coupled on-chip spiral inductors, including closed-form formulas for the values of the ideal circuit elements. The validation of the equivalent circuit model is presented in Section 5.4. Following this, techniques for isolation improvement between spiral inductors are presented based on the principle of magnetic flux cancellation in Section 5.5. Finally, we give conclusions in Section 5.6.

5.2 Magnetic Coupling Characteristics of Coupled Inductors

As illustrated in Fig. 5.1, we assume two inductors L_1 and L_2 with mutual inductance M ($M < \sqrt{L_1 L_2}$). The port impedance at both ports is Z_0. The transfer characteristics S_{12} or S_{21} in Laplace domain ($s{=}j\omega$) can be derived as

$$S_{12} = S_{21} = \frac{2sMZ_0}{(L_1L_2 - M^2)\,s^2 + Z_0\,(L_1 + L_2)\,s + {Z_0}^2}. \tag{5.1}$$

Equation (5.1) can be written with a more compact notation as

$$S_{21}(s = j\omega) = a\frac{j\omega}{(j\omega - p_1)(j\omega - p_2)}, \tag{5.2}$$

where

$$a = \frac{2MZ_0}{L_1L_2 - M^2} \tag{5.3}$$

$$p_1 + p_2 = -\frac{Z_0(L_1 + L_2)}{L_1L_2 - M^2} \tag{5.4}$$

$$p_1p_2 = \frac{{Z_0}^2}{L_1L_2 - M^2}. \tag{5.5}$$

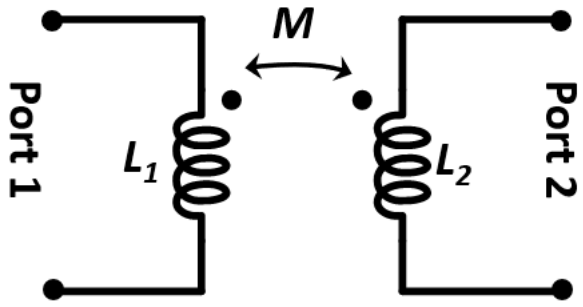

Figure 5.1: Coupled inductors.

The transfer function has two zeros at zero frequency and infinity, and two poles at p_1 and p_2. The response for the transfer function above can be illustrated in Fig. 5.2, by assuming $p_2 > p_1$.

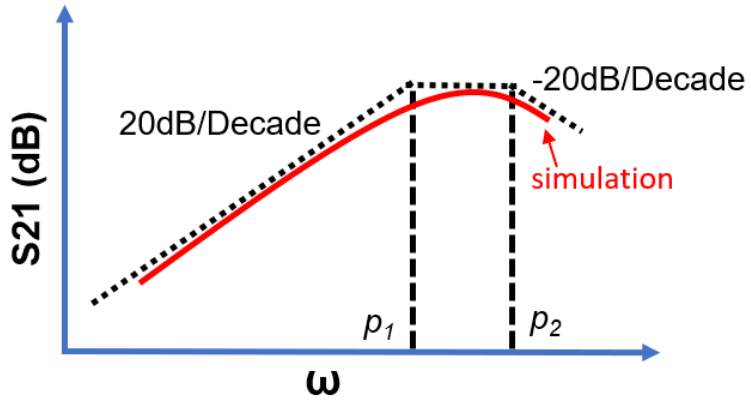

Figure 5.2: Bode plot diagram for magnetic coupling.

5.3 Circuit Model for Coupled On-Chip Spiral Inductors

The circuit model for on-chip coupled inductors is based on the coupled inductor elements. The circuit model topology for coupled on-chip mmWave spiral inductors comprises two isolated spiral inductor circuit models along with a coupled inductor element (Fig. 5.3) [98]. The equivalent circuit model for the isolated inductor was presented in Fig. 4.1 in Chapter 4. The circuit elements are functions of geometrical and material parameters. Since the skin and proximity effects have a negligible effect on the mutual coupling, the magnetic coupling is captured by coupled high frequency inductance element L_∞, with coupling coefficient k. The coupling coefficient k is obtained as

$$k = \frac{M}{\sqrt{L_{\infty 1} L_{\infty 2}}}, \tag{5.6}$$

where $L_{\infty 1}$ and $L_{\infty 2}$ are the high-frequency inductance for spiral inductor 1 and 2, respectively. The capacitive coupling is generally negligible compared to the magnetic coupling and, hence, is ignored in our coupled inductor model.

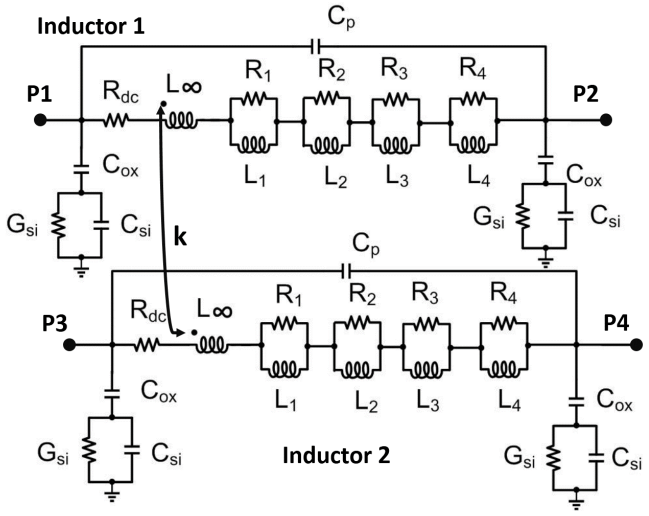

Figure 5.3: Circuit model for coupled on-chip spiral inductors.

5.4 Model Validation

To validate our scalable model, we have fabricated coupled single-turn inductor structures in a TowerJazz 0.18 μm BiCMOS process . We have applied our proposed approach to derive scalable equivalent circuit models for these coupled inductors. In the coupled single-turn inductors, the two spiral inductors are identical to each other. The inductors are on the top metal 6 (M6) with larger thickness and higher conductivity. The width of the conductor is 12 μm, and the side length is $l = 112$ μm. The feed line is 20 μm long and the port spacing s_p is 6 μm.

We first determined the scalable model for a single inductor. The corresponding circuit element values for the single spiral inductor are listed in the table below.

Table 5.1: Circuit Element Values for Single Spiral Inductor

C_{ox}	C_{si}	G_{si}	C_p	R_{dc}	L_∞	L_1
20.25	17.45	1.93	1.5	0.42	226	5.76
L_2	L_3	L_4	R_1	R_2	R_3	R_4
11.06	1.923	2.75	0.044	0.627	0.489	1.90

*unit: Ω for R, pH for L, fF for C, mS for G.

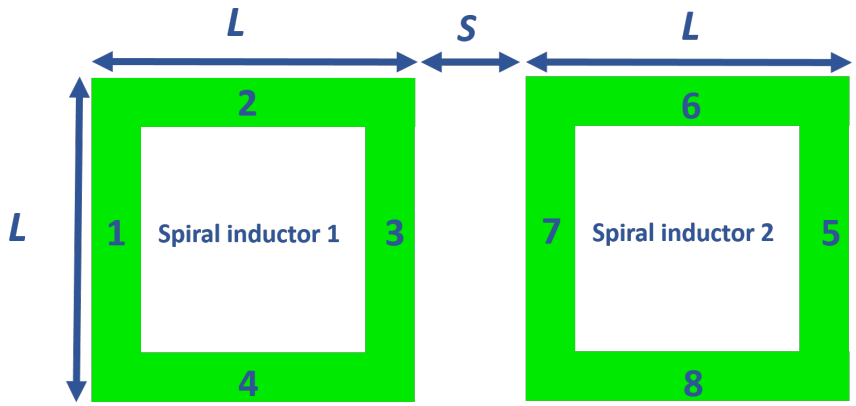

Figure 5.4: Simplified coupled single-turn on-chip inductors in form of closed loops without feed lines.

To derive the coupling coefficient k, each single-turn inductor is approximated as a closed square loop for simplification (multi-turn inductor corresponds to multiple loops), where the feed line is ignored. The top view of the simplified coupled inductors is shown in Fig 5.4. Due to the symmetry and assuming clockwise currents in spiral inductors 1 and 2, respectively, the mutual inductance M can be expressed as

$$M = 2\left(M_{17} + M_{26} - M_{28}\right) - M_{15} - M_{37}, \tag{5.7}$$

where M_{ij} is the partial mutual inductance between segment i and segment j, respectively.

We have fabricated two sets of coupled inductors with different spacing s (10 μm and 20 μm). From (5.6) and (5.7) and using the closed-form expressions for partial

mutual inductances M_{ij} given in [64], the coupling coefficient k is determined as 0.063 and 0.043, respectively. The two-port measurement setup is indicated in Fig. 5.5. For each inductor, one of its terminals is connected to both of the reference ground pads through an under-pass on M5. The ground pads are connected to the silicon substrate.

The comparison between measurements up to 67 GHz, full-wave electromagnetic simulation results, and model performance is shown in Figs. 5.6-5.9. Two-port Short-Open-Load-Through (SOLT) calibration was used. For de-embedding, open and short pad structures were designed on the chip and on-wafter measurement has been performed. The measurements match well with our model and simulation up to 40 GHz. After that, there is a dip on the magnitude of S_{21} for both cases. This might be due to the de-embedding structures, since the Open-Short de-embedding approach was applied and this approach assumes the de-embedding structure should be electrically small to be treated as a lumped equivalent circuit. However, our de-embedding structures include long launching traces connecting the pads to the device under test (DUT). These long traces behave like transmission lines at high frequencies and the lumped model assumption for the Open-Short de-embedding is no longer valid.

In addition to coupled single-turn inductors, we also applied our modeling techniques to coupled two-turn inductors, as illustrated in Fig. 5.10. The inductor size is 70 μm by 70 μm for the outer coil and 50 μm by 50 μm for the inner coil. The trace width is 12 μm and the spacing between the inner and outer coil is 8 μm. The model for the coupled two-turn inductors matches well with the measurements (Figs. 5.11 and 5.12) and HFSS simulation.

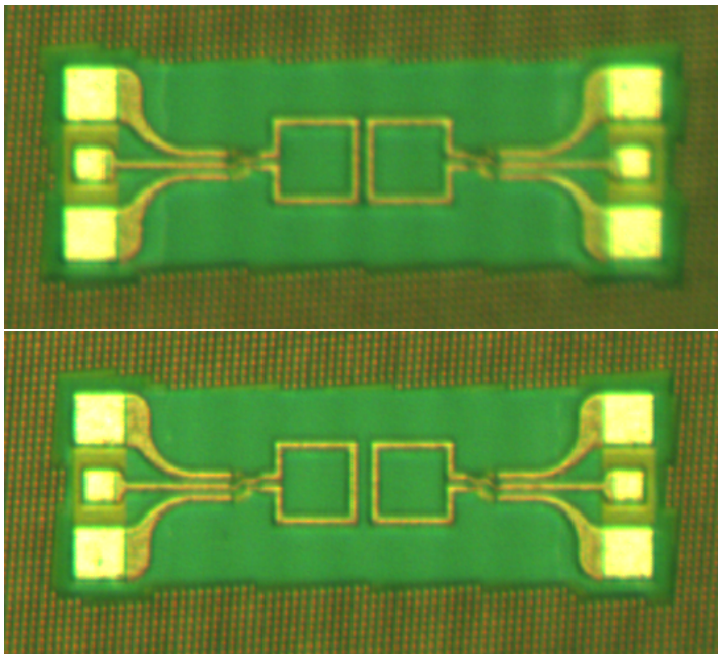

Figure 5.5: Fabricated coupled on-chip spiral inductors with different spacings (top: 10 μm spacing; bottom: 20 μm spacing).

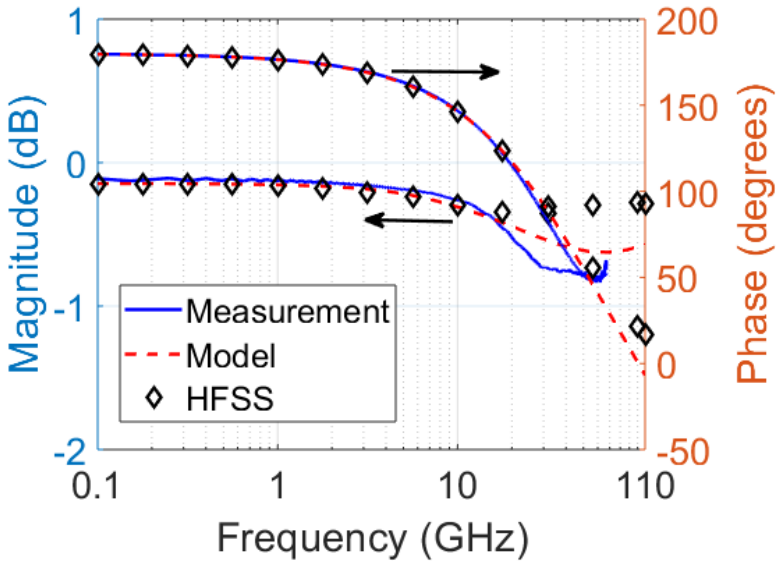

Figure 5.6: S_{11} (S_{22}) for coupled on-chip inductors shown in Fig. 5.5 with spacing 10 μm.

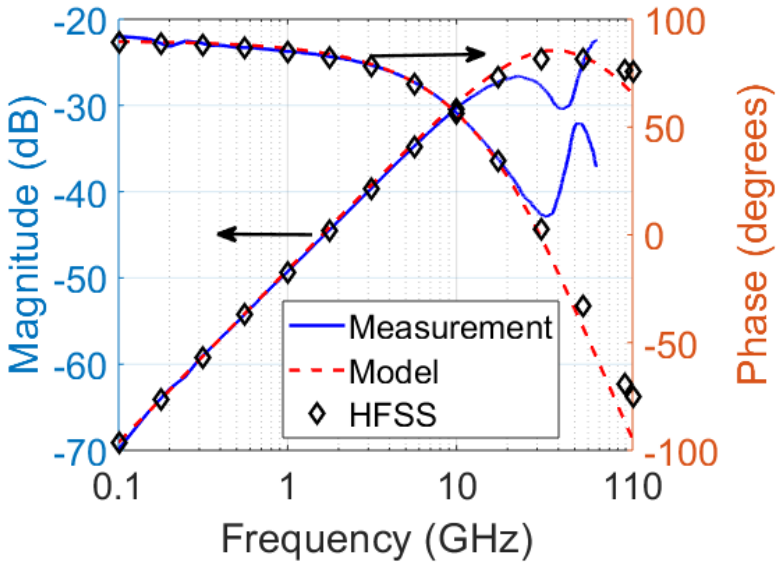

Figure 5.7: S_{21} (S_{12}) for coupled on-chip inductors shown in Fig. 5.5 with spacing 10 μm.

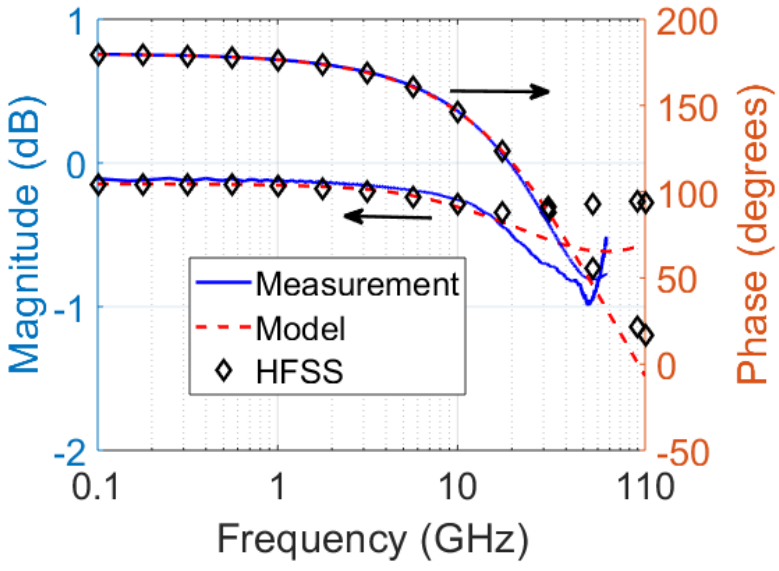

Figure 5.8: S_{11} (S_{22}) for coupled on-chip inductors shown in Fig. 5.5 with spacing 20 μm.

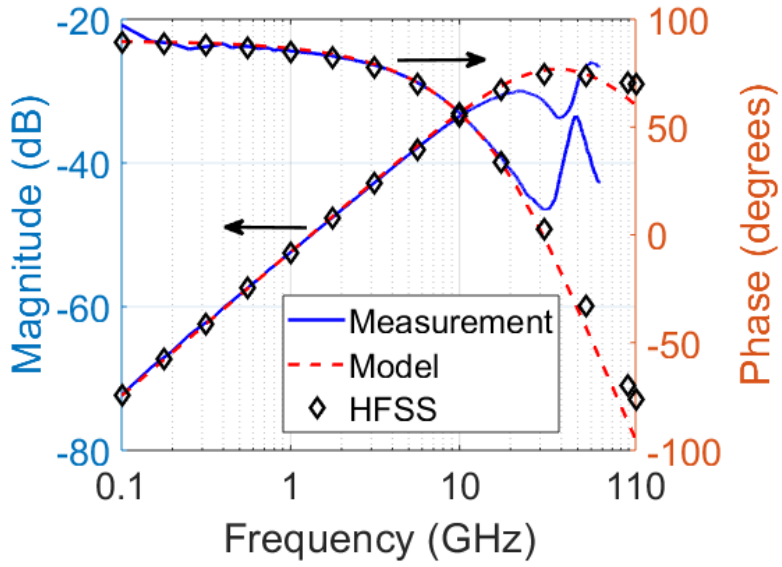

Figure 5.9: S_{21} (S_{12}) for coupled on-chip inductors shown in Fig. 5.5 with spacing 20 μm.

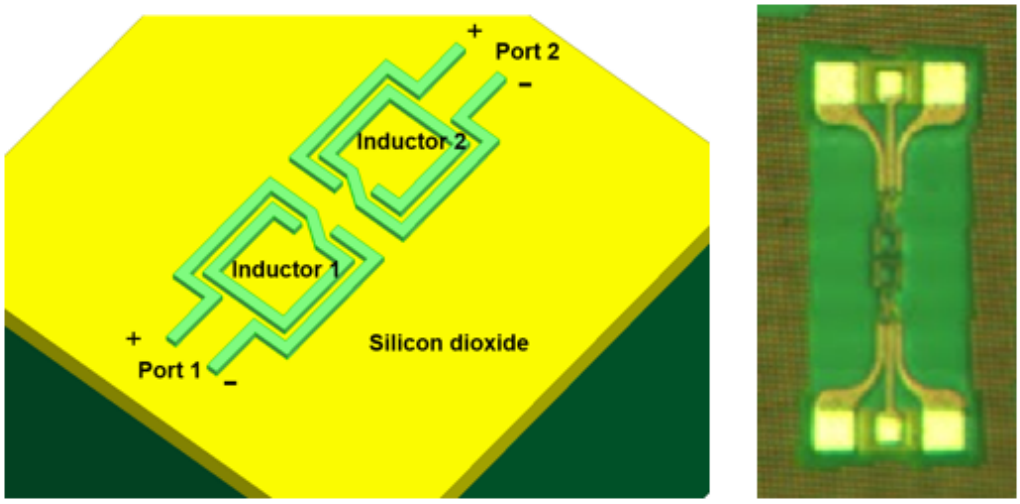

Figure 5.10: On-chip coupled two-turn spiral inductors in HFSS simulation (under-pass not shown) and its die photo.

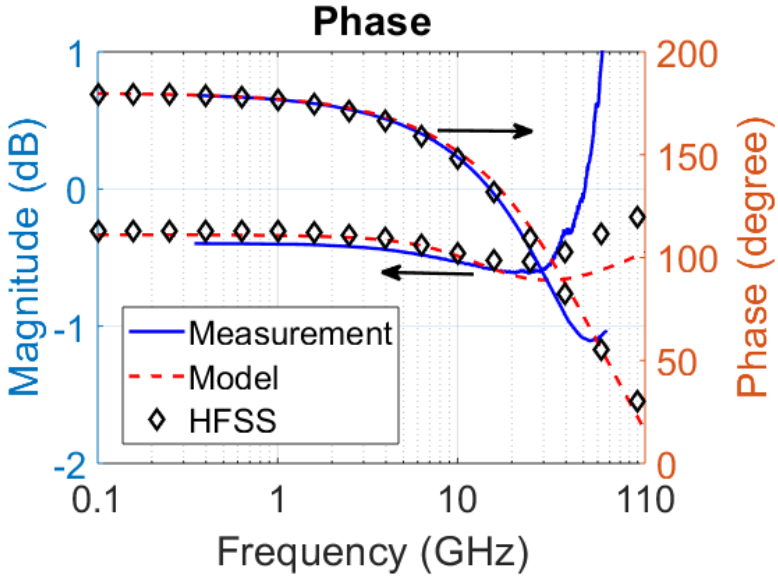

Figure 5.11: S_{11} (S_{22}) for coupled on-chip inductors shown in Fig. 5.10 with spacing 20 μm.

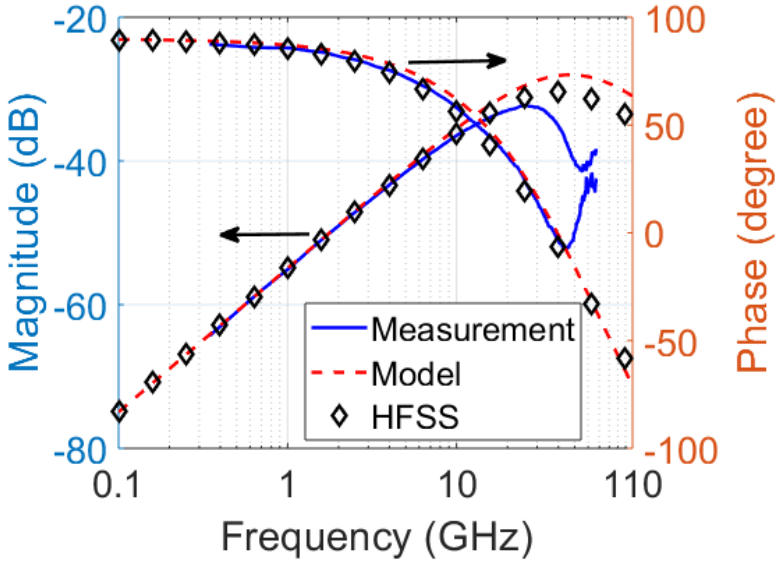

Figure 5.12: S_{21} (S_{12}) for coupled on-chip inductors shown in Fig. 5.10 with spacing 20 μm.

5.5 Isolation Improvement Techniques

Since the mutual inductance causes magnetic coupling due to magnetic flux linkage, we can find a specific overlap of two inductors to have the total mutual flux canceled. Flux cancellation is based on having the same amount of mutual flux but in opposite directions inside of spiral inductor. Similar techniques using the principle of magnetic flux cancellation have been found in [99] [100], but with much large silicon area because the spirals are separated instead of overlapped. Using our proposed flux cancellation strategy with overlapped inductors, both high isolation and layout compactness can be achieved. As illustrated in Fig. 5.13, the different colored regions indicate the opposite magnetic flux directions inside the blue coil. By choosing the proper offset, the mutual inductance can be made close to zero.

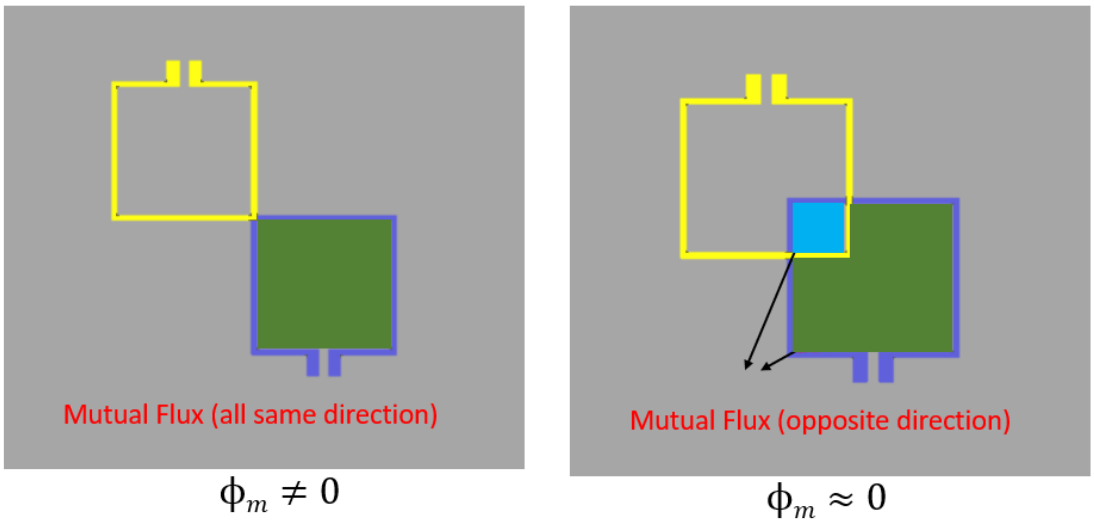

Figure 5.13: Principle of magnetic flux cancellation.

EM simulations have also been performed to validate our technique. Figure 5.14 shows the change of coupling coefficient k with the horizontal offset. The spiral inductors are identical and the coil size is 90 μm by 90 μm. As shown in the figure, there exists an optimal offset where the mutual coupling can be minimized close to zero. From the simulation we can observe this flux cancellation is nearly frequency independent, which means the skin and proximity effects have negligible impact on the external magnetic

field.

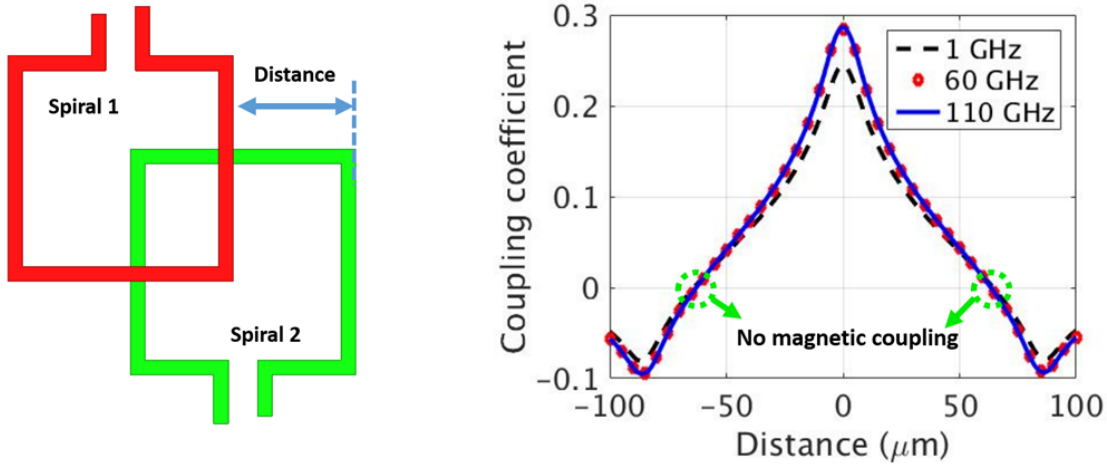

Figure 5.14: Coupling coefficient k versus different location.

To validate our proposed layout strategy for isolation improvement, we have fabricated a test chip in TowerJazz 130 nm RFCMOS process with different coupled inductor layouts. In case 1, two spiral inductors are placed corner to corner. Case 2 has an offset in both vertical and horizontal directions. And in case 3, the two spiral inductors only have a horizontal offset. From the plots we can observe that with overlap the coupling between the spiral inductors is reduced. In all three cases the slop is 20 dB/dec as discussed in Section 5.2. We also observed a dip in cases 2 and 3. This is caused by the interaction of the inductive and capacitive couplings. Since the overlapped inductors have increased mutual capacitance, they behave like a transformer with very small magnetic coupling. Hence, there may exist a transmission zero due to the mutual inductance and capacitance [101]. In terms of the offset between the HFSS simulation and measurements for cases 2 and 3, it is probably caused by coupling between the probing pads, launching structures and spiral inductors. The coupling between the spiral is designed to be very small so that any parasitic coupling becomes dominate. Thus, the additional couplings lead to higher S_{21} than the HFSS simulation results while the traditional Open-Short de-embedding can not capture the parasitic couplings.

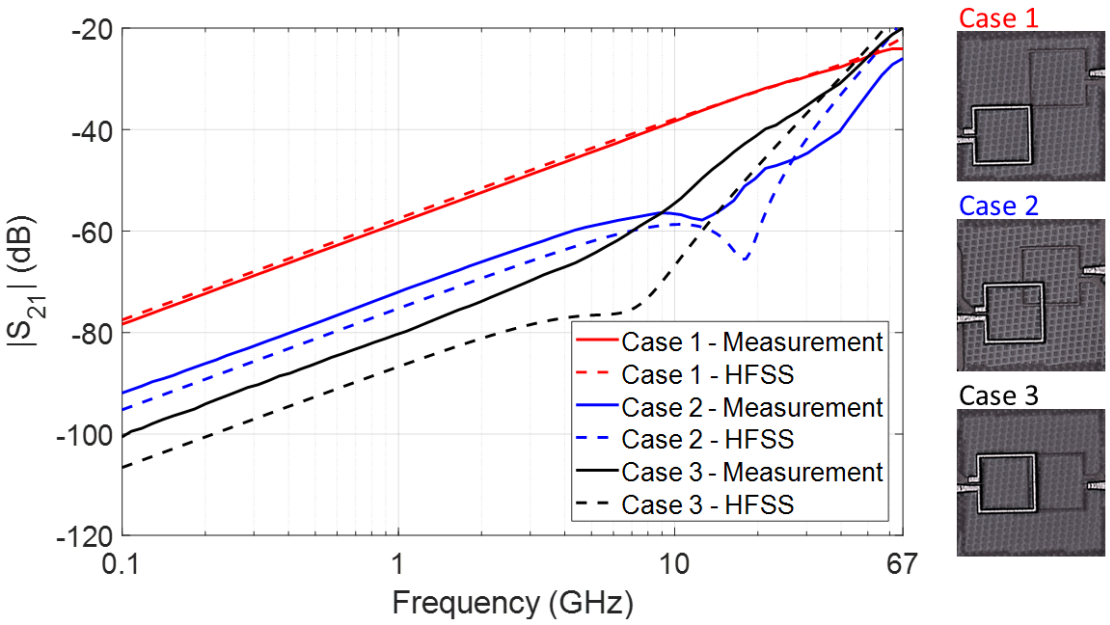

Figure 5.15: Simulated and measured S_{21} for different layouts of inductor pairs.

5.6 Conclusion

In this chapter, we have presented a systematic scalable modeling methodology for capturing the magnetic coupling between on-chip spiral inductors. We have developed the scalable equivalent circuit model with closed-form expressions for the circuit element values, which is compatible with standard circuit simulators. We have verified the model accuracy through both EM full-wave simulation and measurement of fabricated test structures. The comparisons indicate good agreement between model, simulation and measurement for two coupled single-turn spiral inductors with different spacings. We also have proposed layout strategies for isolation improvement based on the principle of magnetic flux cancellation. Test structures have been fabricated and measured to validate our isolation improvement techniques. This flux cancellation technique can be applied to various types of circuits with multiple inductors to achieve both compactness and high isolation. For example, on-chip LC matching networks or filters may adopt this technique to reduce the layout area significantly.

Chapter 6: Summary and Future Work

6.1 Summary

In this thesis, scalable and compact modeling techniques for on-chip interconnects and spiral inductors have been presented. The scalable models capture skin and proximity effects in the conductors as well as substrate eddy current and metal fill loss. The scalable models also capture multi-physics effects such as temperature and process variations.

In the first part of this thesis, we have discussed the design trade-offs for two commonly-used on-chip transmission lines, i.e., microstrip and CPW. Further, we have presented scalable compact modeling techniques for on-chip transmission lines. The scalable equivalent circuit models for microstrips and CPWs are applicable for different IC processes over a large geometrical parameter range. The models have been verified by extensive EM simulations and measurements of fabricated chips. The error for both microstrip and CPW models is within 10% over a wide range of geometries. The models for transmission lines have also been extended to more complicated passives, such as a single-stub matching network and branch line coupler. In addition, temperature and processes variations have also been included in the scalable models.

In the second part of this thesis, we have presented a field-based modeling approach to model more complicated passives, such as coupled CPWs and spiral inductors. This proposed method can handle a larger number of geometrical and material parameters than for isolated transmission lines. The substrate eddy-current effect has also been included using the complex image approach. Further, the field-based approach has been extended to model metal fill loss in an arbitrary uniform magnetic filed. We have validated our field-based modeling techniques by both EM simulations and measurements of fabricated chips.

Finally, a scalable equivalent circuit model for the magnetic coupling between spiral inductors has been presented. The model has been validated by EM simulations and measurements of fabricated coupled inductors with different spacings. In addition, a compact layout strategy for inductor pairs with reduced couplings (high isolation) has

been demonstrated. The strategy is based on the principle of magnetic flux cancellation. Inductor pairs achieving both compactness and high isolation have been fabricated and measured, showing good agreement with EM simulations.

6.2 Future Work

In future work, the modeling techniques can be extended to other passive components such as transformers, capacitors and so on. Future work for passive modeling techniques may include modeling skin and proximity effect resistances due to non-uniform fields, when the field strength on the conductor is significant and the uniform field assumption in our approach is no longer invalid. One possible direction is to decompose the magnetic field with different basis functions and to develop empirical functions for each basis function, respectively. The approach for capturing metal fill loss in this thesis is to model metal fill loss for each metal fill separately and then add the contributions. This approach can achieve higher accuracy, but sacrifices efficiency, especially when a large number of metal fills are present. Approaches with improved efficiency for larger problem areas may be researched in the future.

The compact layout strategy provides a solution for canceling the magnetic coupling only between inductors. As the layout is more compact, the component will become more sensitive to external trace routing. Layout strategies for connecting traces are also needed to preserve the high isolation. In addition, the capacitive coupling needs to be investigated since the overlapping between inductors leads to an increase in the mutual capacitance. Accurate scalable models for the port-to-port capacitance between overlapped inductors need to be developed. Strategies for reduced coupling with compact layouts for other types of passive may also be studied in the future. The principle of magnetic flux cancellation can be further applied to realize other possible functionalities such as six-port devices, duplexers, and so on.

Bibliography

[1] Analog Devices. (2012) Automotive radar transmitter designed for active safety applications. [Online]. Available: https://www.ecnmag.com/product-release/2012/11/automotive-radar-transmitter-designed-active-safety-applications

[2] L. Kong, M. K. Khan, F. Wu, G. Chen, and P. Zeng, "Millimeter-Wave wireless communications for IoT-Cloud supported autonomous vehicles: Overview, design, and challenges," *IEEE Communications Magazine*, vol. 55, no. 1, pp. 62–68, January 2017.

[3] 3GPP. (2017) First 5G NR specs approved. [Online]. Available: http://www.3gpp.org/news-events/3gpp-news/1929-nsa_nr_5g

[4] Huawei Technologies. 5G Vision: 100 Billion connections, 1 ms Latency, and 10 Gbps Throughput. [Online]. Available: http://www.huawei.com/minisite/5g/en/defining-5g.html

[5] MiWaveS. [Online]. Available: http://www.miwaves.eu/

[6] C. Gartenberg. (2017) Verizon says it will have 5G service in five cities by the end of next year. [Online]. Available: https://www.theverge.com/2017/11/29/16717270/verizon-5g-rollout-service-five-cities-sacramento-milimeter-wave

[7] B. Y. Lin, K. H. Tsai, and S. I. Liu, "A 128.24-to-137.00GHz injection-locked frequency divider in 65nm CMOS," in *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, Feb 2009, pp. 282–283,283a.

[8] C. P. Yue and S. S. Wong, "Design strategy of on-chip inductors for highly integrated RF systems," in *Proceedings 1999 Design Automation Conference (Cat. No. 99CH36361)*, 1999, pp. 982–987.

[9] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sept 2000.

[10] H. Ding, G. Wang, K. Lam, D. Jordan, A. Zeeb, A. Bavisi, E. Mina, and B. Gaucher, "Modeling and implementation of on-chip millimeter-wave compact branch line couplers in a BiCMOS technology," in *2007 European Microwave Conference*, Oct 2007, pp. 458–461.

[11] L. K. Yeh, C. Y. Chen, and H. R. Chuang, "A millimeter-wave CPW CMOS on-chip bandpass filter using conductor-backed resonators," *IEEE Electron Device Letters*, vol. 31, no. 5, pp. 399–401, May 2010.

[12] A. Natarajan, S. K. Reynolds, M. D. Tsai, S. T. Nicolson, J. H. C. Zhan, D. G. Kam, D. Liu, Y. L. O. Huang, A. Valdes-Garcia, and B. A. Floyd, "A fully-integrated 16-element phased-array receiver in SiGe BiCMOS for 60-GHz communications," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 1059–1075, May 2011.

[13] H. Ding, G. Wang, K. Lam, D. Jordan, A. Zeeb, A. Bavisi, E. Mina, and B. Gaucher, "Modeling and implementation of on-chip millimeter-wave compact branch line couplers in a BiCMOS technology," in *2007 European Microwave Conference*, Oct 2007, pp. 458–461.

[14] H. Ding, K. Lam, E. Mina, J. Rascoe, D. Jordan, A. Zeeb, and B. Gaucher, "On-chip millimeter-wave library device - scalable wilkinson power divier/combiner," in *2007 Proceedings 57th Electronic Components and Technology Conference*, May 2007, pp. 1246–1251.

[15] S. Luo, C. C. Boon, L. Zhu, M. A. Do, and A. V. Do, "A compact millimeter-wave CMOS bandpass filter using a dual-mode ring resonator," in *2011 International Symposium on Integrated Circuits*, Dec 2011, pp. 270–272.

[16] K. Zhan, J. Kang, G. Wang, T. Kamgaing, R. Khanna, G. Dogiamis, H. Liu, and A. Natarajan, "A low-power FSK/spatial modulation transmitter for mm-wave wireless links," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, June 2017, pp. 801–804.

[17] A. Natarajan, S. Nicolson, M.-D. Tsai, and B. Floyd, "A 60GHz variable-gain LNA in 65nm CMOS," in *2008 IEEE Asian Solid-State Circuits Conference*, Nov 2008, pp. 117–120.

[18] J. Kang, S. Rao, P. Chiang, and A. Natarajan, "Design and optimization of area-constrained wirelessly powered CMOS UWB SoC for localization applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 4, pp. 1042–1054, April 2016.

[19] Z. Q. Zhang, X. P. Liao, and R. Wu, "RF on-chip LC passive bandpass filter based on GaAs MMIC technology," *Electronics Letters*, vol. 46, no. 3, pp. 269–270, Feb 2010.

[20] M. M. Elsbury, P. D. Dresselhaus, N. F. Bergren, C. J. Burroughs, S. P. Benz, and Z. Popovic, "Broadband lumped-element integrated N-way power dividers for voltage standards," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 8, pp. 2055–2063, Aug 2009.

[21] F. Ellinger, U. Mayer, M. Wickert, N. Joram, J. Wagner, R. Eickhoff, I. Santamaria, C. Scheytt, and R. Kraemer, "Integrated adjustable phase shifters," *IEEE Microwave Magazine*, vol. 11, no. 6, pp. 97–108, Oct 2010.

[22] B. Razavi, *RF Microelectronics*. Prentice Hall, 2012.

[23] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, May 1998.

[24] J. R. Long, Y. Zhao, W. Wu, M. Spirito, L. Vera, and E. Gordon, "Passive circuit technologies for mm-Wave wireless systems on silicon," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 8, pp. 1680–1693, Aug 2012.

[25] J. Zheng, V. K. Tripathi, and A. Weisshaar, "Characterization and modeling of multiple coupled on-chip interconnects on silicon substrate," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 10, pp. 1733–1739, Oct 2001.

[26] S. Ramo, J. Whinnery, and T. Van Duzer, *Fields and Waves in Communication Electronics*. Wiley, 1994.

[27] H. A. Wheeler, "Formulas for the skin effect," *Proceedings of the IRE*, vol. 30, no. 9, pp. 412–424, Sept 1942.

[28] R. K. Gupta, I. Sakai, and C. Hu, "Effects of substrate resistance on CMOS latchup holding voltages," *IEEE Transactions on Electron Devices*, vol. 34, no. 11, pp. 2309–2316, Nov 1987.

[29] A. M. Niknejad and R. G. Meyer, "Analysis of eddy-current losses over conductive substrates with applications to monolithic inductors and transformers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 1, pp. 166–176, Jan 2001.

[30] V. S. Shilimkar, S. G. Gaskill, and A. Weisshaar, "Experimental characterization of metal fill placement and size impact on spiral inductors," in *2009 IEEE 18th Conference on Electrical Performance of Electronic Packaging and Systems*, Oct 2009, pp. 101–104.

[31] B. E. Stine, D. S. Boning, J. E. Chung, L. Camilletti, F. Kruppa, E. R. Equi, W. Loh, S. Prasad, M. Muthukrishnan, D. Towery, M. Berman, and A. Kapoor, "The physical and electrical effects of metal-fill patterning practices for oxide chemical-mechanical polishing processes," *IEEE Transactions on Electron Devices*, vol. 45, no. 3, pp. 665–679, Mar 1998.

[32] S. G. Gaskill, V. S. Shilimkar, and A. Weisshaar, "Wide-range closed-form eddy-current loss formula for metal fill," in *19th Topical Meeting on Electrical Performance of Electronic Packaging and Systems*, Oct 2010, pp. 129–132.

[33] R. Amaya, P. H. R. Popplewell, M. Cloutier, and C. Plett, "EM and substrate coupling in silicon RFICs," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1968–1971, Sept 2005.

[34] Y. Soliman and R. Mason, "Experimental results of active and passive isolation techniques for multiple K-band LC-oscillators on silicon ICs," in *Asia-Pacific Microwave Conference 2011*, Dec 2011, pp. 339–342.

[35] K. Agarwal and S. Nassif, "Characterizing process variation in nanometer CMOS," in *2007 44th ACM/IEEE Design Automation Conference*, June 2007, pp. 396–399.

[36] K. Kang, J. Shi, W. Y. Yin, L. W. Li, S. Zouhdi, S. C. Rustagi, and K. Mouthaan, "Analysis of frequency- and temperature-dependent substrate eddy currents in on-chip spiral inductors using the complex image method," *IEEE Transactions on Magnetics*, vol. 43, no. 7, pp. 3243–3253, July 2007.

[37] L. Daniel, O. C. Siong, L. S. Chay, K. H. Lee, and J. White, "A multiparameter moment-matching model-reduction approach for generating geometrically parameterized interconnect performance models," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 23, no. 5, pp. 678–693, May 2004.

[38] Q. Yu and T. W. Holmes, "A study on stray capacitance modeling of inductors by using the finite element method," *IEEE Transactions on Electromagnetic Compatibility*, vol. 43, no. 1, pp. 88–93, Feb 2001.

[39] X. C. Li, J. F. Mao, and M. Swaminathan, "Transient analysis of CMOS-gate-driven *rlgc* interconnects based on FDTD," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, no. 4, pp. 574–583, April 2011.

[40] P. J. Restle, A. E. Ruehli, S. G. Walker, and G. Papadopoulos, "Full-wave PEEC time-domain method for the modeling of on-chip interconnects," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, no. 7, pp. 877–886, Jul 2001.

[41] K. M. Coperich, A. E. Ruehli, and A. Cangellaris, "Enhanced skin effect for partial-element equivalent-circuit (PEEC) models," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 9, pp. 1435–1442, Sep 2000.

[42] L. Daniel and J. Phillips, "Model order reduction for strictly passive and causal distributed systems," in *Proceedings 2002 Design Automation Conference*, 2002, pp. 46–51.

[43] P. Sumant, H. Wu, A. Cangellaris, and N. Aluru, "Reduced-order models of finite element approximations of electromagnetic devices exhibiting statistical variability," *IEEE Transactions on Antennas and Propagation*, vol. 60, no. 1, pp. 301–309, Jan 2012.

[44] A. C. Cangellaris and M. Celik, "Order reduction of high-speed interconnect electrical models: The issue of passivity," in *1998 IEEE Symposium on IC/Package Design Integration*, Feb 1998, pp. 132–137.

[45] *Q2D*, ANSYS, Pittsburgh, PA 15219, USA.

[46] D. Pozar, *Microwave Engineering*. Wiley, 2004.

[47] T. S. D. Cheung and J. R. Long, "Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 5, pp. 1183–1200, May 2006.

[48] S. Kim and D. P. Neikirk, "Compact equivalent circuit model for the skin effect," *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, pp. 1815–1818, 1996.

[49] X. M. Shi, K. S. Yeo, J. G. Ma, A. Do, and E. P. Li, "Scalable model of on-wafer interconnects for high-speed CMOS ICs," *IEEE Transactions on Advanced Packaging*, vol. 29, no. 4, pp. 770–776, 2006.

[50] K. Kang, L. Nan, S. C. Rustagi, K. Mouthaan, J. L. Shi, R. Kumar, W. Y. Yin, and L. W. Li, "A wideband scalable and SPICE-compatible model for on-chip interconnects up to 110 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 4, pp. 942–951, 2008.

[51] A. E. Ruehli, G. Antonini, and L. J. Jiang, "Skin-effect loss models for time-and frequency-domain PEEC solver," *Proceedings of the IEEE*, vol. 101, no. 2, pp. 451–472, 2013.

[52] W. Shu, S. Shichijo, and R. M. Henderson, "A unified equivalent circuit model for coplanar waveguides considering silicon substrate effects," *IEEE MTT-S International Microwave Symposium (IMS)*, pp. 1–3, June 2014.

[53] H. Lee and T. Itoh, "Phenomenological loss equivalence method for planar quasi-TEM transmission lines with a thin normal conductor or superconductor," *IEEE Transactions on Microwave Theory and Techniques*, vol. 37, no. 12, pp. 1904–1909, 1989.

[54] J. A. Stratton, *Electromagnetic Theory*. John Wiley & Sons, 2007.

[55] R. M. Foster, "A reactance theorem," *The Bell System Technical Journal*, vol. 3, no. 2, pp. 259–267, April 1924.

[56] P. Waldow and I. Wolff, "The skin-effect at high frequencies," *IEEE Transactions on Microwave Theory and Techniques*, vol. 33, no. 10, pp. 1076–1082, Oct 1985.

[57] L. Zheng, S. G. Gaskill, and A. Weisshaar, "A scalable wideband equivalent circuit model for on-chip microstrips up to 110 GHz," in *2014 IEEE 23rd Conference on Electrical Performance of Electronic Packaging and Systems*, Oct 2014, pp. 141–144.

[58] C. Karr, D. Stanley, and B. Scheiner, *Genetic algorithm applied to least squares curve fitting*, U.S. Dept. of the Interior, Bureau of Mines, Tech. Rep. RI-9339, Feb. 1991.

[59] F. Schnieder and W. Heinrich, "Model of thin-film microstrip line for circuit design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, pp. 104–110, Jan. 2001.

[60] A. R. Djordjevic and S. K. Tapan, "Closed-form formulas for frequency-dependent resistance and inductance per unit length of microstrip and strip transmission lines," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, pp. 241–248, Feb. 1994.

[61] T. Shibata and E. Sano, "Characterization of MIS structure coplanar transmission lines for investigation of signal propagation in integrated circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 38, no. 7, pp. 881–890, 1990.

[62] F. Stellari and A. L. Lacaita, "New formulas of interconnect capacitances based on results of conformal mapping method," *IEEE Transactions on Electron Devices*, vol. 47, no. 1, pp. 222–231, 2000.

[63] L. Zheng and A. Weisshaar, "Parameterised equivalent circuit model of frequency-dependent resistance and inductance for on-chip coplanar waveguides up to 110 GHz," *Electronics Letters*, vol. 54, no. 16, pp. 986–988, 2018.

[64] G. Zhong and C. K. Koh, "Exact closed form formula for partial mutual inductances of on-chip interconnects," in *Proceedings. IEEE International Conference on Computer Design: VLSI in Computers and Processors*, 2002, pp. 428–433.

[65] H. Klingbeil and W. Heinrich, "Calculation of CPW AC resistance and inductance using a quasi-static mode-matching approach," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 6, pp. 1004–1007, Jun 1994.

[66] *High Frequency Structure Simulator*, ANSYS, Pittsburgh, PA 15219, USA.

[67] D. Goren, M. Zelikson, T. Galambos, R. Gordin, B. Livshitz, A. Amir, A. Sherman, and I. Wagner, "An interconnect-aware methodology for analog and mixed signal design, based on high bandwidth (over 40 GHz) on-chip transmission line approach," *Proceedings of IEEE Design, Automation and Test in Europe Conference and Exhibition*, pp. 804–811, 2002.

[68] L. Zheng and A. Weisshaar, "Scalable and compact modeling of on-chip interconnects from DC to mmWave frequencies," *SRC TECHCON*, 2015.

[69] H. Ito and K. Masuy, "A simple through-only de-embedding method for on-wafer S-parameter measurements up to 110 GHz," in *2008 IEEE MTT-S International Microwave Symposium Digest*, June 2008, pp. 383–386.

[70] K. Kang, J. Shi, W. Y. Yin, L. W. Li, S. Zouhdi, S. C. Rustagi, and K. Mouthaan, "Analysis of frequency- and temperature-dependent substrate eddy currents in on-chip spiral inductors using the complex image method," *IEEE Transactions on Magnetics*, vol. 43, no. 7, pp. 3243–3253, July 2007.

[71] L. Shi, Y. Di, M. Zhao, C. J. Xue, K. Wu, and E. H. M. Sha, "Exploiting process variation for write performance improvement on NAND flash memory storage systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 1, pp. 334–337, Jan 2016.

[72] R. Y. Rubinstein and D. P. Kroese, *Simulation and the Monte Carlo Method.* John Wiley & Sons, 2016.

[73] L. Weiner, P. Chiotti, and A. H. Wilhelm, *Ames Laboratory ISC Technical Reports. 58.*

[74] L. Zheng, A. R. Ferrara, and A. Weisshaar, "Scalable modeling of resistive losses in on-chip interconnects at mm-wave frequencies," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, May 2016.

[75] J. A. Ferreira, "Improved analytical modeling of conductive losses in magnetic components," *IEEE Transactions on Power Electronics*, vol. 9, no. 1, pp. 127–131, Jan 1994.

[76] S. G. Gaskill, V. S. Shilimkar, and A. Weisshaar, "Wide-range closed-form eddy-current loss formula for metal fill," *IEEE 19th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, vol. 19, no. 3, pp. 129–132, Oct. 2010.

[77] *MAXWELL*, ANSYS, Pittsburgh, PA 15219, USA.

[78] A. Sharma, *Linear Algebra*. Discovery Publishing House Pvt. Limited, 2007.

[79] D. K. Walker, R. F. Kaiser, D. F. Williams, and K. J. Coakley, "Lumped-element models for on-wafer calibration," in *56th ARFTG Conference Digest*, vol. 38, Nov 2000, pp. 1–4.

[80] L. Zheng and A. Weisshaar, "Scalable modeling of resistive losses in on-chip interconnects at mmWave frequencies," *SRC TECHCON*, 2016.

[81] B. Gustavsen and A. Semlyen, "Rational approximation of frequency domain responses by vector fitting," *IEEE Transactions on Power Delivery*, vol. 14, no. 3, pp. 1052–1061, Jul 1999.

[82] A. Weisshaar, H. Lan, and A. Luoh, "Accurate closed-form expressions for the frequency-dependent line parameters of on-chip interconnects on lossy silicon substrate," *IEEE Transactions on Advanced Packaging*, vol. 25, no. 2, pp. 288–296, May 2002.

[83] J. Zheng, Y. Hahm, V. K. Tripathi, and A. Weisshaar, "CAD-oriented equivalent-circuit modeling of on-chip interconnects on lossy silicon substrate," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 9, pp. 1443–1451, Sep 2000.

[84] A. M. Niknejad and R. G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF ICs," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1470–1481, Oct 1998.

[85] J. R. Long and M. A. Copeland, "Modeling, characterization and design of monolithic inductors for silicon RFICs," in *Proceedings of Custom Integrated Circuits Conference*, May 1996, pp. 185–188.

[86] A. C. Watson, D. Melendy, P. Francis, K. Hwang, and A. Weisshaar, "A comprehensive compact-modeling methodology for spiral inductors in silicon-based

RFICs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 3, pp. 849–857, March 2004.

[87] L. Zheng and A. Weisshaar, "Compact scalable modeling of mmWave spiral inductors," *SRC TECHCON*, 2017.

[88] D. F. Williams, "Metal-insulator-semiconductor transmission line model," in *51st ARFTG Conference Digest*, vol. 33, June 1998, pp. 65–71.

[89] Y. Eo and R. W. Eisenstadt, "High-speed VLSI interconnect modeling based on S-parameter measurements," *IEEE Trans. Components, Hybrids, and Manufacturing Technology*, vol. 16, no. 5, pp. 555–562, 1993.

[90] F. Stellari and A. L. Lacaita, "New formulas of interconnect capacitances based on results of conformal mapping method," *IEEE Trans. Electron Devices*, vol. 47, no. 1, pp. 222–231, 2000.

[91] *Q3D*, Ansoft Corporation, Pittsburgh, PA 15219, USA.

[92] V. Shilimkar, "Enabling metal-fill-aware design of integrated circuits," Ph.D. dissertation, Oregon State University, 2014.

[93] V. S. Shilimkar, S. G. Gaskill, and A. Weisshaar, "Closed-form expressions for modeling metal fill effects in interconnects," in *2011 IEEE 15th Workshop on Signal Propagation on Interconnects (SPI)*, May 2011, pp. 97–100.

[94] H. Feng, G. Jelodin, K. Gong, R. Zhan, Q. Wu, C. Chen, and A. Wang, "Super compact RFIC inductors in 0.18 um CMOS with copper interconnects," in *2002 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium. Digest of Papers*, June 2002, pp. 443–446.

[95] R. Murakami, T. Ito, K. Okada, and A. Matsuzawa, "An ultra-compact LC-VCO using a stacked-spiral inductor," *IEICE Electronics Express*, vol. 8, no. 7, pp. 512–517, 2011.

[96] K. Kang, C. J. Tan, J. Brinkhoff, J. Shi, and F. Lin, "Coupling effects between on-chip inductors in the millimeter-wave regime," *IEEE Electron Device Letters*, vol. 31, no. 4, pp. 362–364, April 2010.

[97] F. Vecchi, M. Repossi, A. Mazzanti, P. Arcioni, and F. Svelto, "A simple and complete circuit model for the coupling between symmetrical spiral inductors in silicon RF-ICs," in *2008 IEEE Radio Frequency Integrated Circuits Symposium*, June 2008, pp. 479–482.

[98] L. Zheng, A. R. Ferrara, and A. Weisshaar, "Scalable and broadband modeling of coupled on-chip spiral inductors up to 110 GHz," in *2016 IEEE 25th Conference on Electrical Performance Of Electronic Packaging And Systems (EPEPS)*, Oct 2016, pp. 25–28.

[99] N. M. Neihart, D. J. Allstot, M. Miller, and P. Rakers, "Twisted inductors for low coupling mixed-signal and RF applications," in *2008 IEEE Custom Integrated Circuits Conference*, Sept 2008, pp. 575–578.

[100] A. Poon, A. Chang, H. Samavati, and S. S. Wong, "Reduction of inductive crosstalk using quadrupole inductors," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 6, pp. 1756–1764, June 2009.

[101] A. Ghadiri and K. Moez, "Bandwidth enhancement of on-chip transformers using negative capacitance," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 10, pp. 648–652, Oct 2012.

APPENDICES

Appendix A: Closed-form Expressions for Circuit Elements in Microstrip and CPW Model

A.1 Microstrip

For the elements of the signal conductor model,

$$R_{oi} = k_{i1} e^{\left(-k_{i2}\frac{h_s}{t_s}\right)} + k_{i3}\ \Omega/\text{m} \quad (i = 1, 2, 3), \tag{A.1}$$

and

$$k_{ij} = a_{ij}\left(\frac{w_s}{t_s}\right)^{\left(-b_{ij}\frac{w_s}{t_s} - c_{ij}\right)} \quad (i, j = 1, 2, 3). \tag{A.2}$$

a_{ij}, b_{ij} and c_{ij} are listed in the following table

Table A.1: Values for a, b and c

ij	11	12	13	21	22	23
a_{ij}	1.08e4	3.811	6.73e3	1.412e4	3.3	1.839e4
b_{ij}	7.266e-4	5.553e-3	8.474e-4	0	4e-3	2.621e-3
c_{ij}	0.7486	0.337	0.928	1.268	0.198	0.685
ij	31	32	33			
a_{ij}	5.22e4	3.482	4.814e4			
b_{ij}	1.7e-3	3.146e-3	2.177e-3			
c_{ij}	1.1	0.2843	0.69			

For the poles of RL network of the signal conductor,

$$p_{oi} = m_{i1} e^{\left(-m_{i2}\frac{h_s}{t_s}\right)} + m_{i3}\ \text{rad/sec} \quad (i = 1, 2, 3) \tag{A.3}$$

and

$$m_{ij} = x_{1ij}\left(\frac{w_s}{t_s}\right)^{\left(x_{2ij}\frac{w_s}{t_s}+x_{3ij}\right)} - x_{4ij}\left(\frac{w_s}{t_s}\right) + x_{5ij} \quad (i = 1, 2, 3; j = 1, 2, 3). \tag{A.4}$$

The coefficients are listed below:

Table A.2: Values for x

ij	11	12	13	21	22	23
x_{1ij}	4.778e10	2.93e9	1.405e10	0.9086	3.247	27
x_{2ij}	0	0	0	-0.179	-0.02734	-0.1143
x_{3ij}	3.26e-1	1	1	0.624	-0.0537	0
x_{4ij}	0	0	0	0.006115	0	0
x_{5ij}	0	3.37e10	0	0.6074	0.407	0.469

ij	31	32
x_{1ij}	4.56e11	4.32e11
x_{2ij}	0	-0.02246
x_{3ij}	-1.314	-1.206
x_{4ij}	0	1.4655e9
x_{5ij}	1.6e10	4.2e11

and

$$m_{33} = 6 \times 10^{12} \times \left(0.393 - 3.445^{\left(0.0426\frac{w_s}{t_s}-3.95\right)} + 0.246 \times \left(\frac{w_s}{t_s}\right)^{\left(-0.146\frac{w_s}{t_s}-1.667\right)}\right). \tag{A.5}$$

For ground conductor model elements R_i and L_i:

$$R_i = g_{i1}\left(\frac{w_s}{h_{\text{eff}}}\right)^{g_{i2}} + g_{i3} \quad \Omega/\text{m} \ (i = 1, 2) \tag{A.6}$$

and

$$g_{ij} = y_{1ij}e^{\left(-y_{2ij}\frac{t_g}{h_{\text{eff}}}\right)} + y_{3ij} \quad (i = 1, 2; j = 1, 2, 3). \tag{A.7}$$

The coefficients are

Table A.3: Values for y

ij	11	12	13	21	22	23
y_{1ij}	0	0	0	-94.8	0	595
y_{2ij}	0	0	0	10.3	0	13.08
y_{3ij}	-4.512e2	0.5747	2.543e3	-213.4	0.44	826

$$L_i = q_{i1}\left(\frac{w_s}{h_{\text{eff}}}\right)^{q_{i2}} + q_{i3} \text{ H/m} \quad (\text{i} = 1, 2) \tag{A.8}$$

and

$$q_{ij} = z_{1ij}e^{\left(-z_{2ij}\frac{t_g}{h_{\text{eff}}}\right)} + z_{3ij} \quad (i = 1, 2; j = 1, 2, 3). \tag{A.9}$$

The coefficients are

Table A.4: Values for z

ij	11	12	13	21	22	23
z_{1ij}	4.752e-10	0	-2.02e-9	4.624e-9	0	-1.945e-8
z_{2ij}	9.8	0	10.6	6.32	0	5.11
z_{3ij}	-6.08e-10	0.44	2.223e-9	-4.011e-9	0.44	1.756e-8

For the third pole of RL section for the ground conductor,

$$p_3 = u_1\left(\frac{w_s}{h_{\text{eff}}}\right)^{0.44} + u_2 \quad \text{rad/sec} \tag{A.10}$$

and

$$u_i = r_{i1}\left(\frac{t_g}{h_{\text{eff}}}\right)^{r_{i2}} + r_{i3}(i = 1, 2) \quad . \tag{A.11}$$

The coefficients are listed in the table:

Table A.5: Values for r

i	1	2
r_{i1}	-8.616e6	5.967e7
r_{i2}	-1.2	-1.12
r_{i3}	8.616e6	4.32e7

A.2 CPW

For the resistance elements,

$$R_{0i} = \frac{k_{i1}}{1 + k_{i2}\left(\frac{ws}{s}\right)^{k_{i3}}} + \frac{k_{i4}}{1 + k_{i5}\left(\frac{ws}{s}\right)^{k_{i6}}}\ \Omega/\text{m} \quad (i = 1, 2, 3) \tag{A.12}$$

and

$$k_{ij} = a_{ij} + b_{ij}e^{\left(c_{ij}\frac{t}{s}\right)} \quad (i = 1, 2, 3;\ j = 1, 2, 3, 4, 5, 6). \tag{A.13}$$

a_{ij}, b_{ij} and c_{ij} are listed in the following table:

Table A.6: Values for a, b and c

ij	11	12	13	14	15	16
a_{ij}	7.565e3	-6.674	0.256	-6.719e3	-6.045	0.643
b_{ij}	1.222e3	-0.841	0.891	-1.21e3	1.37	-0.348
c_{ij}	-1.042	1.042	0.442	1.268	-1.18	-0.763
ij	21	22	23	24	25	26
a_{ij}	1.13e4	2.496	-3.703e-2	2.156e4	9.191	0.601
b_{ij}	-1.975e3	4.832	-0.768	1.083e4	-2.645	-0.309
c_{ij}	2.607	2.82	-6.294	-0.376	-2.041e-2	-0.205
ij	31	32	33	34	35	36
a_{ij}	6.379e4	7.281	0.598	3.764e4	3.66	0.691
b_{ij}	1.088e5	-5.357	-0.365	-1e5	1.038	-4.671
c_{ij}	-14.436	-1.547	-0.313	-4.588	2.375	-5.953

For the poles of RL network,

$$p_{0i} = \frac{m_{i1}}{1 + m_{i2}\left(\frac{ws}{s}\right)^{m_{i3}}} + \frac{m_{i4}}{1 + m_{i5}\left(\frac{ws}{s}\right)^{m_{i6}}} \text{ H/m} \quad (\text{i} = 1, 2, 3, 4) \tag{A.14}$$

and

$$m_{ij} = x_{ij} + y_{ij} e^{\left(z_{ij}\frac{t}{s}\right)} \quad (i = 1, 2, 3, 4; j = 1, 2, 3, 4, 5, 6). \tag{A.15}$$

x_{ij}, y_{ij} and z_{ij} are listed below:

Table A.7: Values for x, y and z

ij	11	12	13	14	15	16
x_{ij}	2.434e10	2.871	-0.377	-1.285e11	-6.191	0.504
y_{ij}	-1.041e11	5.74	2.473	4.315e10	-6.364	-0.364
z_{ij}	-0.361	-2.26	-0.181	-6.980	-0.715	-4.491
ij	21	22	23	24	25	26
x_{ij}	1.871e11	1.581	1.89	1.411e11	5.453e-3	-0.507
y_{ij}	2.558e11	6.559	-0.666	-7.254e10	3.628	-3.489
z_{ij}	-3.413	-1.164	-0.937	-7.88e-2	-0.808	0.172
ij	31	32	33	34	35	36
x_{ij}	-3.26e12	-5.406	2.073	8.917e11	-0.422	-1.85
y_{ij}	5.01e11	-4.334	1.152	-1.786e11	1.501	-2.702
z_{ij}	6.73e-2	-0.493	-1.457	-9.57e-2	-3.409e-2	5.722e-3
ij	41	42	43	44	45	46
x_{ij}	3.936e8	0.791	1.3	-2.704e8	4.111	-1.124
y_{ij}	-3.406e8	0.1	-1.389	4.889e8	-3.901	0.765
z_{ij}	0.6745	0.171	-1.852	3.905e-2	-0.267	-1.454

For the capacitance formula,

$$C_{\text{air}} = \frac{n_1}{1 + n_2\left(\frac{s}{t}\right)^{n_3}} + \frac{n_4}{1 + n_5\left(\frac{s}{t}\right)n_6} \text{ F/m} \tag{A.16}$$

and

$$n_i = \frac{x_i}{1 + y_i\left(\frac{w_s}{t}\right)^{z_i}} \quad (i = 1, 2, 3, 4, 5, 6). \tag{A.17}$$

x_i, y_i and z_i are listed below:

Table A.8: Values for x, y and z

i	1	2	3	4	5	6
x_i	2.205e-10	0.921	0.732	1.744e-10	9.38	2.615
y_i	4.192	0.459	0.601	8.18e-2	-1.899e-4	0.759
z_i	-0.439	-1.03	-2.39e-2	0.417	-2.564	-5.792e-2

Appendix B: HSPICE Model for Microstip and CPW

B.1 HSPICE Model for Microstrip

```
.SUBCKT microstrip 1 2 0  ws= ts= hs= sigmas=
+wg= tg= sigmag= ereff= length=

$input parameter for the model
$ .PARAM ws=5e-6      $width of signal conductor
$ .PARAM ts=1e-6      $thickness of signal conductor
$ .PARAM hs=10e-6      $height of signal conductor
$ .PARAM sigmas=3e7  $conductivity of signal conductor
$ .PARAM wg=300e-6      $width of ground conductor
$ .PARAM tg=1e-6      $thickness of ground conductor
$ .PARAM sigmag=3e7  $conductivity of ground conductor
$ .PARAM ereff=1   $relative effective permittivity
$ .PARAM length=3e-6  $length of short section

$define constant
.PARAM c0=3e8      $speed of light
.PARAM pi=3.1415926
.PARAM miu0=4*pi*1e-7    $permittivity for vacuum

$ calculate Rdc Linf Cpul
.PARAM eta0 = 'sqrt(4*pi/8.8542e-5)'
.PARAM F1 = '(6+(2*pi-6)*exp(-PWR((30.666*hs/ws),0.7528)))'
.PARAM weq0= '(ws+ts/pi*log(1+4*exp(1)/(ts/hs*PWR(1/
             (tanh(sqrt(6.517*ws/hs))),2))))'
.PARAM Zl0_weq0 = '(eta0/(2*pi)*log(F1*hs/weq0+
```

```
                  sqrt(1+PWR((2*hs/weq0),2))))'
.PARAM Cpul = '(ereff*1/(c0*Zl0_weq0))'
.PARAM Linf = 'ereff/Cpul/c0/c0'
.PARAM Rdc = '(1/ws/ts/sigmas+1/wg/tg/sigmag)'

$define function K4 to calculate Ldc
.PARAM aatan(y,x) = '((y>=0)*(x>=0))*atan(y/x)+((y<0)*(x<0))*
                    (-pi+atan(abs(y/x)))+((y>0)*(x<0))*(pi-
                    atan(abs(y/x)))+((y<0)*(x>0))*(-atan(abs(y/x)))'
.PARAM K4(x, y) = 'POW(sqrt(POW(x,2)+POW(y,2)),4)*cos(4*aatan(y,x))
                  /24*(log(sqrt(POW(x,2)+POW(y,2)))-25/12)
                  -POW(sqrt(POW(x,2)+POW(y,2)),4)*sin(4*aatan(y,x))
                  /24*aatan(y,x)'
$x is the real part, y is the imaginary part
.PARAM Ks_wg_tg= '((4*(K4(wg,0)+K4(1e-30,tg))-2*(K4(wg,tg)+K4(wg,-tg)))
                +1/3*pi*wg*PWR(tg,3))'
.PARAM Ks_ws_ts='((4*(K4(ws,0)+K4(1e-30,ts))-2*(K4(ws,ts)+K4(ws,-ts)))
                +1/3*pi*ws*PWR(ts,3))'
.PARAM a= 'ws'
.PARAM b= 'ts'
.PARAM c= 'wg'
.PARAM d= 'tg'
.PARAM h= 'hs+(ts+tg)/2'
.PARAM Km1= '(-K4((a/2+c/2),(b/2+d/2-h))+K4((a/2+c/2),(b/2-d/2-h))
            +K4((a/2-c/2),(b/2+d/2-h))-K4((a/2-c/2),(b/2-d/2-h)))'
.PARAM Km2= '(K4((a/2+c/2),(-b/2+d/2-h))-K4((a/2+c/2),(-b/2-d/2-h))
            -K4((a/2-c/2),(-b/2+d/2-h))+K4((a/2-c/2),(-b/2-d/2-h)))'
.PARAM Km3= '(K4((-a/2+c/2),(b/2+d/2-h))-K4((-a/2+c/2),(b/2-d/2-h))
            -K4((-a/2-c/2),(b/2+d/2-h))+K4((-a/2-c/2),(b/2-d/2-h)))'
.PARAM Km4= '-K4((-a/2+c/2),(-b/2+d/2-h))+K4((-a/2+c/2),(-b/2-d/2-h))
            +K4((-a/2-c/2),(-b/2+d/2-h))-K4((-a/2-c/2),(-b/2-d/2-h))'
.PARAM Km=  '(Km1+Km2+Km3+Km4)'
.PARAM Ldc = '-2E-7*(1/PWR(ws,2)/PWR(ts,2)*Ks_ws_ts-2/(ws*wg*ts*tg)*Km+
```

```
            1/PWR(wg,2)/PWR(tg,2)*Ks_wg_tg)'

$ signal condcutor R&L
.PARAM k11= '1.08147e4*PWR(ws/ts, (-7.265865e-4*(ws/ts)-0.748582))'
.PARAM k12= '3.81141*PWR(ws/ts, (-5.55321e-3*(ws/ts)-0.3369))'
.PARAM k13= '6.73296e3*PWR(ws/ts, (-8.474357e-4*(ws/ts)-0.9278))'
.PARAM Rs1= '(k11*exp(-k12*(hs/ts))+k13)*6e7/sigmas*PWR((1e-6/ts), 2)'
.PARAM k31= '5.21706e4*PWR(ws/ts, (-1.7e-3*(ws/ts)-1.1))'
.PARAM k32= '3.481797*PWR(ws/ts, (-3.1457e-3*(ws/ts)-0.28434))'
.PARAM k33= '4.814455e4*PWR(ws/ts, (-2.17724e-3*(ws/ts)-0.68979))'
.PARAM Rs3= '(k31*exp(-k32*(hs/ts))+k33)*6e7/sigmas*PWR((1e-6/ts), 2)'
.PARAM k21= '1.41198e4*PWR(ws/ts, (-0*(ws/ts)-1.26808))'
.PARAM k22= '3.303976112*PWR(ws/ts, (-4e-3*(ws/ts)-0.197838))'
.PARAM k23= '1.8394e4*PWR(ws/ts, (-2.62138e-3*(ws/ts)-0.6852))'
.PARAM Rs2= '(k21*exp(-k22*(hs/ts))+k23)*6e7/sigmas*PWR((1e-6/ts), 2)'
.PARAM k1l1= '7.964e-2*PWR(ws/ts,3.26248e-1)'
.PARAM k2l1= '(9.086e-1*PWR(ws/ts,((-1.791265e-1)*ws/ts+6.24e-1))-
            (6.1147e-3)*ws/ts+6.0735e-1)'
.PARAM k3l1= '(0.76)*PWR(ws/ts,(-1.314))+2.6625e-2'
.PARAM k1l2= '1.953125e-3*ws/ts+(2.246e-2)'
.PARAM k2l2= '3.247*PWR(ws/ts,-2.734375e-2*ws/ts-5.37109e-2)
            +4.0722656e-1'
.PARAM k3l2= '2.88086e-1*PWR(ws/ts,(-2.2461e-2)*ws/ts-1.206)-
            (9.7656e-4)*ws/ts+(2.8027e-1)'
.PARAM k1l3= '(2.342e-3)*ws/ts'
.PARAM k2l3= '27*PWR(ws/ts,(-1.1426e-1)*ws/ts)+4.6875e-1'
.PARAM k3l3= '0.39287-PWR(3.445,(4.26e-2*ws/ts-3.95))+2.461e-
            1*PWR(ws/ts,((-1.46e-1)*ws/ts-1.667))'
.PARAM Polefit1='(k1l1*exp(-k2l1*hs/ts)+k3l1)*6e11*6e7/sigmas
               *PWR((1e-6/ts), 2)'
.PARAM Polefit2='(k1l2*exp(-k2l2*hs/ts)+k3l2)*1.5e12*6e7/sigmas
               *PWR((1e-6/ts), 2)'
.PARAM Polefit3='(k1l3*exp(-k2l3*hs/ts)+k3l3)*6e12*6e7/sigmas
```

```
                *PWR((1e-6/ts), 2)'
.PARAM Ls1='Rs1/Polefit1'
.PARAM Ls2='Rs2/Polefit2'
.PARAM Ls3='Rs3/Polefit3'
.PARAM heff='hs+ts/2'
.PARAM Rg1='2.1827e3*(-2.067e-1*PWR(ws/heff,5.747e-1)+1.165)
           *5.8e7/sigmag*PWR((10e-6/heff), 2)'
.PARAM kg11= '-3.2e-10*(-1.485*exp(-9.8*tg/heff)+1.9)'
.PARAM kg12= '2.47e-9*(-0.818*exp(-10.6*tg/heff)+0.9)'
.PARAM Lg1= 'kg11*PWR(ws/heff,0.44)+kg12'
.PARAM kg21= '-6.512e-10*(-7.1*exp(-6.32*tg/heff)+6.16)'
.PARAM kg22= '1.621e-8*(-1.2*exp(-5.11*tg/heff)+1.083)'
.PARAM Lg2= 'kg21*PWR((ws/heff),0.44)+kg22'
.PARAM kg31= '-206*(0.46*exp(-10.3*tg/heff)+1.036)'
.PARAM kg32= '1.14e3*(0.522*exp(-13.08*tg/heff)+0.7244)'
.PARAM Rg2= '(kg31*PWR((ws/heff),0.44)+kg32)*5.8e7/sigmag
            *PWR((10e-6/heff), 2)'
.PARAM Lg3= 'Ldc-Linf-Ls1-Ls2-Ls3-Lg1-Lg2'
.PARAM kp1= '-2.872e7*(0.3*PWR((tg/heff),-1.2)+0.3)'
.PARAM kp2= '1.778e9*(3.356e-2*PWR((tg/heff),-1.12)+2.43e-2)'
.PARAM Poleg='(kp1*PWR(ws/heff, 0.44)+kp2)'
.PARAM Rg3='Poleg*Lg3*5.8e7/sigmag*PWR((10e-6/heff), 2)'

Rdc0 1 4 'Rdc*length'
Linf0 4 5 'Linf*length'
Rss1 5 6 'Rs1*length'
Lss1 5 6 'Ls1*length'
Rss2 6 7 'Rs2*length'
Lss2 6 7 'Ls2*length'
Rss3 7 8 'Rs3*length'
Lss3 7 8 'Ls3*length'

Rgs1 8 9 'Rg1*length'
```

```
Lgs1 8 9 'Lg1*length'
Rgs2 9 10 'Rg2*length'
Lgs2 9 10 'Lg2*length'
Rgs3 10 2 'Rg3*length'
Lgs3 10 2 'Lg3*length'
C   2  0 'Cpul*length'
.ENDS
```

B.2 HSPICE Model for CPW

```
.SUBCKT CPW_MODEL 1 2 0  ws=5e-6 t=1e-6 sigma=3e7
+wg=30e-6 s=10e-6 ereff=1 length=3e-6

$input parameter for the model
$ .PARAM ws=5e-6      $width of signal conductor
$ .PARAM t=1e-6      $thickness of signal conductor
$ .PARAM s=10e-6      $spacing between signal and gournd conductors
$ .PARAM sigma=3e7     $conductivity of  conductor
$ .PARAM wg=30e-6      $width of ground conductor
$ .PARAM ereff=1   $relative effective permittivity
$ .PARAM length=3e-6  $length of short section

$define constant

.PARAM c0=3e8      $speed of light
.PARAM pi=3.1415926
.PARAM miu0=4*pi*1e-7    $permittivity for vacuum

$ calculate Rdc Linf
```

```
.PARAM n1 = '0.73/(1+0.6*PWR(ws/t,-0.024))'
.PARAM n2 = '2.6/(1+0.76*PWR(ws/t,-0.058))'
.PARAM C0= '2.2E-10/(1+4.2*PWR(ws/t,-0.44))/(1+(0.92/(1+
0.46*PWR(ws/t,-1)))*(PWR(s/t,n1)))+1.74E-10/(1+
0.08*PWR(ws/t,0.42))/(1+(9.4/(1-1.9e-
4*PWR(ws/t,-2.6)))*(PWR(s/t,n2)))'
.PARAM Linf = '1/C0/c0/c0'
.PARAM Rdc = '(1/ws/t/sigma+1/wg/t/sigma/2)'

$define functions to calculate Ldc
.PARAM l=1
.PARAM wn = 'ws/l'
.PARAM tn = 't/l'
.PARAM r = 'sqrt(PWR(wn,2)+PWR(tn,2))'
.PARAM aw = 'sqrt(PWR(wn,2)+1)'
.PARAM at = 'sqrt(PWR(tn,2)+1)'
.PARAM ar = 'sqrt(PWR(wn,2)+PWR(tn,2)+1)'
.PARAM asinh(a)='log(a+sqrt(PWR(a,2)+1))'
% compute partial self inductance of signal conductor
.PARAM Ls = 'l*2*miu0/pi*(1/4*(1/wn*asinh(wn/at)+1/tn*asinh(tn/aw)
+asinh(1/r))+1/24*(PWR(tn,2)/wn*asinh(wn/(tn*at*(r+ar)))
+PWR(wn,2)/tn*asinh(tn/(wn*aw*(r+ar)))+
PWR(tn,2)/PWR(wn,2)*asinh(PWR(wn,2)/(tn*r*(at+ar)))
+PWR(wn,2)/PWR(tn,2)*asinh(PWR(tn,2)/(wn*r*(aw+ar)))+
1/(wn*PWR(tn,2))*asinh(wn*PWR(tn,2)/(at*(aw+ar)))
+1/(tn*PWR(wn,2))*asinh(tn*PWR(wn,2)/(aw*(at+ar))))-
1/6*(1/(wn*tn)*atan(wn*tn/ar)+tn/wn*atan(wn/(tn*ar))
+wn/tn*atan(tn/(wn*ar)))-
1/60*((ar+r+tn+at)*PWR(tn,2)/((ar+r)*(r+tn)*(tn+at)*(at+ar))+
(ar+r+wn+aw)*PWR(wn,2)/((ar+r)*(r+wn)*(wn+aw)*(aw+ar))+
(ar+aw+1+at)/((ar+aw)*(aw+1)*(at+1)*(at+ar)))-
1/20*(1/(r+ar)+1/(aw+ar)+1/(at+ar)))'
```

```
.PARAM l=1
.PARAM wn1 = 'wg/l'
.PARAM tn1 = 't/l'
.PARAM r1 = 'sqrt(PWR(wn1,2)+PWR(tn1,2))'
.PARAM aw1 = 'sqrt(PWR(wn1,2)+1)'
.PARAM at1 = 'sqrt(PWR(tn1,2)+1)'
.PARAM ar1 = 'sqrt(PWR(wn1,2)+PWR(tn1,2)+1)'
.PARAM asinh(a)='log(a+sqrt(PWR(a,2)+1))'
% compute partial self inductance of ground conductor
.PARAM Lg = 'l*2*miu0/pi*(1/4*(1/wn1*asinh(wn1/at1)+1/tn1*asinh(tn1/aw1)
+asinh(1/r1))+1/24*(PWR(tn1,2)/wn1*asinh(wn1/(tn1*at1*(r1+ar1)))
+PWR(wn1,2)/tn1*asinh(tn1/(wn1*aw1*(r1+ar1)))+
PWR(tn1,2)/PWR(wn1,2)*asinh(PWR(wn1,2)/(tn1*r1*(at1+ar1)))
+PWR(wn1,2)/PWR(tn1,2)*asinh(PWR(tn1,2)/(wn1*r1*(aw1+ar1)))+
1/(wn1*PWR(tn1,2))*asinh(wn1*PWR(tn1,2)/(at1*(aw1+ar1)))
+1/(tn1*PWR(wn1,2))*asinh(tn1*PWR(wn1,2)/(aw1*(at1+ar1))))-
1/6*(1/(wn1*tn1)*atan(wn1*tn1/ar1)+tn1/wn1*atan(wn1/(tn1*ar1))
+wn1/tn1*atan(tn1/(wn1*ar1)))-
1/60*((ar1+r1+tn1+at1)*PWR(tn1,2)/((ar1+r1)*(r1+tn1)*(tn1+at1)*(at1+ar1))+
(ar1+r1+wn1+aw1)*PWR(wn1,2)/((ar1+r1)*(r1+wn1)*(wn1+aw1)*(aw1+ar1))+
(ar1+aw1+1+at1)/((ar1+aw1)*(aw1+1)*(at1+1)*(at1+ar1)))-
1/20*(1/(r1+ar1)+1/(aw1+ar1)+1/(at1+ar1)))'

% compute partial mutal inductance between ground conductors
.PARAM x1=0
.PARAM y1=0
.PARAM x2='2*wg+ws+2s'
.PARAM y2=0
.PARAM xdif='abs(x1-x2)'
.PARAM ydif='abs(y1-y2)'
.PARAM xq='x1+0.5*wd'
.PARAM yq='y1+0.5*t'
.PARAM xp='x2+0.5*wg'
```

```
.PARAM yp='y2+0.5*t'
.PARAM x1='xq'
.PARAM y1='yq-0.5*t'
.PARAM x2='xq+0.5*ws'
.PARAM y2='yq'
.PARAM x3='xq'
.PARAM y3='yq+0.5*t'
.PARAM x4='xq-0.5*ws'
.PARAM y4='yq'
.PARAM x5='xp'
.PARAM y5='yp-0.5*t'
.PARAM x6='xp+0.5*wg'
.PARAM y6='yp'
.PARAM x7='xp'
.PARAM y7='yp+0.5*t'
.PARAM x8='xp-0.5*wg'
.PARAM y8='yp'

.PARAM h1 = 'sqrt(PWR((xq-xp),2)+PWR((yq-yp),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r11 = 'h1/l'
.PARAM r12= 'r11*r11'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h11 = 'sqrt(g1*g1+r12)'
.PARAM Lp11='(g1*log(g1+h11)-h11)'
.PARAM h12 = 'sqrt(g2*g2+r12)'
.PARAM Lp12='-(g2*log(g2+h12)-h12)'
.PARAM h13 = 'sqrt(g3*g3+r12)'
.PARAM Lp13='(g3*log(g3+h13)-h13)'
```

```
.PARAM h14 = 'sqrt(g4*g4+r12)'
.PARAM Lp14='-(g4*log(g4+h14)-h14)'
.PARAM Mf9='(Lp11+Lp12+Lp13+Lp14)*l*1.0e-7'
.PARAM M9='-2.0*Mf9'

.PARAM h2 = 'sqrt(PWR((x1-xp),2)+PWR((y1-yp),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r21 = 'h2/l'
.PARAM r22= 'r21*r21'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h21 = 'sqrt(g1*g1+r22)'
.PARAM Lp21='(g1*log(g1+h21)-h21)'
.PARAM h22 = 'sqrt(g2*g2+r22)'
.PARAM Lp22='-(g2*log(g2+h22)-h22)'
.PARAM h23 = 'sqrt(g3*g3+r22)'
.PARAM Lp23='(g3*log(g3+h23)-h23)'
.PARAM h24 = 'sqrt(g4*g4+r22)'
.PARAM Lp24='-(g4*log(g4+h24)-h24)'
.PARAM Mf1='(Lp21+Lp22+Lp23+Lp24)*l*1.0e-7'
.PARAM M1='Mf1'

.PARAM h3 = 'sqrt(PWR((x2-xp),2)+PWR((y2-yp),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r31 = 'h3/l'
.PARAM r32= 'r31*r31'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
```

```
.PARAM g4='p'
.PARAM h31 = 'sqrt(g1*g1+r32)'
.PARAM Lp31='(g1*log(g1+h31)-h31)'
.PARAM h32 = 'sqrt(g2*g2+r32)'
.PARAM Lp32='-(g2*log(g2+h32)-h32)'
.PARAM h33 = 'sqrt(g3*g3+r32)'
.PARAM Lp33='(g3*log(g3+h33)-h33)'
.PARAM h34 = 'sqrt(g4*g4+r32)'
.PARAM Lp34='-(g4*log(g4+h34)-h34)'
.PARAM Mf2='(Lp31+Lp32+Lp33+Lp34)*l*1.0e-7'
.PARAM M2='Mf2'

.PARAM h4 = 'sqrt(PWR((x3-xp),2)+PWR((y3-yp),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r41 = 'h4/l'
.PARAM r42= 'r41*r41'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h41 = 'sqrt(g1*g1+r42)'
.PARAM Lp41='(g1*log(g1+h41)-h41)'
.PARAM h42 = 'sqrt(g2*g2+r42)'
.PARAM Lp42='-(g2*log(g2+h42)-h42)'
.PARAM h43 = 'sqrt(g3*g3+r42)'
.PARAM Lp43='(g3*log(g3+h43)-h43)'
.PARAM h44 = 'sqrt(g4*g4+r42)'
.PARAM Lp44='-(g4*log(g4+h44)-h44)'
.PARAM Mf3='(Lp41+Lp42+Lp43+Lp44)*l*1.0e-7'
.PARAM M3='Mf3'

.PARAM h5 = 'sqrt(PWR((x4-xp),2)+PWR((y4-yp),2))'
```

```
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r51 = 'h5/l'
.PARAM r52= 'r51*r51'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h51 = 'sqrt(g1*g1+r52)'
.PARAM Lp51='(g1*log(g1+h51)-h51)'
.PARAM h52 = 'sqrt(g2*g2+r52)'
.PARAM Lp52='-(g2*log(g2+h52)-h52)'
.PARAM h53 = 'sqrt(g3*g3+r52)'
.PARAM Lp53='(g3*log(g3+h53)-h53)'
.PARAM h54 = 'sqrt(g4*g4+r52)'
.PARAM Lp54='-(g4*log(g4+h54)-h54)'
.PARAM Mf4='(Lp51+Lp52+Lp53+Lp54)*l*1.0e-7'
.PARAM M4='Mf4'

.PARAM h6 = 'sqrt(PWR((xq-x5),2)+PWR((yq-y5),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r61 = 'h6/l'
.PARAM r62= 'r61*r61'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h61 = 'sqrt(g1*g1+r62)'
.PARAM Lp61='(g1*log(g1+h61)-h61)'
.PARAM h62 = 'sqrt(g2*g2+r62)'
.PARAM Lp62='-(g2*log(g2+h62)-h62)'
.PARAM h63 = 'sqrt(g3*g3+r62)'
```

```
.PARAM Lp63='(g3*log(g3+h63)-h63)'
.PARAM h64 = 'sqrt(g4*g4+r62)'
.PARAM Lp64='-(g4*log(g4+h64)-h64)'
.PARAM Mf5='(Lp61+Lp62+Lp63+Lp64)*l*1.0e-7'
.PARAM M5='Mf5'

.PARAM h7 = 'sqrt(PWR((xq-x6),2)+PWR((yq-y6),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r71 = 'h7/l'
.PARAM r72= 'r71*r71'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h71 = 'sqrt(g1*g1+r72)'
.PARAM Lp71='(g1*log(g1+h71)-h71)'
.PARAM h72 = 'sqrt(g2*g2+r72)'
.PARAM Lp72='-(g2*log(g2+h72)-h72)'
.PARAM h73 = 'sqrt(g3*g3+r72)'
.PARAM Lp73='(g3*log(g3+h73)-h73)'
.PARAM h74 = 'sqrt(g4*g4+r72)'
.PARAM Lp74='-(g4*log(g4+h74)-h74)'
.PARAM Mf6='(Lp71+Lp72+Lp73+Lp74)*l*1.0e-7'
.PARAM M6='Mf6'

.PARAM h8 = 'sqrt(PWR((xq-x7),2)+PWR((yq-y7),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r81 = 'h8/l'
.PARAM r82= 'r81*r81'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
```

```
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h81 = 'sqrt(g1*g1+r82)'
.PARAM Lp81='(g1*log(g1+h81)-h81)'
.PARAM h82 = 'sqrt(g2*g2+r82)'
.PARAM Lp82='-(g2*log(g2+h82)-h82)'
.PARAM h83 = 'sqrt(g3*g3+r82)'
.PARAM Lp83='(g3*log(g3+h83)-h83)'
.PARAM h84 = 'sqrt(g4*g4+r82)'
.PARAM Lp84='-(g4*log(g4+h84)-h84)'
.PARAM Mf7='(Lp81+Lp82+Lp83+Lp84)*l*1.0e-7'
.PARAM M7='Mf7'

.PARAM h9 = 'sqrt(PWR((xq-x8),2)+PWR((yq-y8),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r91 = 'h9/l'
.PARAM r92= 'r91*r91'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h91 = 'sqrt(g1*g1+r92)'
.PARAM Lp91='(g1*log(g1+h91)-h91)'
.PARAM h92 = 'sqrt(g2*g2+r92)'
.PARAM Lp92='-(g2*log(g2+h92)-h92)'
.PARAM h93 = 'sqrt(g3*g3+r92)'
.PARAM Lp93='(g3*log(g3+h93)-h93)'
.PARAM h94 = 'sqrt(g4*g4+r92)'
.PARAM Lp94='-(g4*log(g4+h94)-h94)'
.PARAM Mf8='(Lp91+Lp92+Lp93+Lp94)*l*1.0e-7'
.PARAM M8='Mf8'
```

```
.PARAM Mgg='abs(M1+M2+M3+M4+M5+M6+M7+M8+M9)/6.0'

.PARAM x1=0
.PARAM y1=0
.PARAM x2='wg+s'
.PARAM y2=0
.PARAM xdif='abs(x1-x2)'
.PARAM ydif='abs(y1-y2)'
.PARAM xq='x1+0.5*wd'
.PARAM yq='y1+0.5*t'
.PARAM xp='x2+0.5*wg'
.PARAM yp='y2+0.5*t'
.PARAM x1='xq'
.PARAM y1='yq-0.5*t'
.PARAM x2='xq+0.5*ws'
.PARAM y2='yq'
.PARAM x3='xq'
.PARAM y3='yq+0.5*t'
.PARAM x4='xq-0.5*ws'
.PARAM y4='yq'
.PARAM x5='xp'
.PARAM y5='yp-0.5*t'
.PARAM x6='xp+0.5*wg'
.PARAM y6='yp'
.PARAM x7='xp'
.PARAM y7='yp+0.5*t'
.PARAM x8='xp-0.5*wg'
.PARAM y8='yp'

.PARAM h1 = 'sqrt(PWR((xq-xp),2)+PWR((yq-yp),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r11 = 'h1/l'
```

```
.PARAM r12= 'r11*r11'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h11 = 'sqrt(g1*g1+r12)'
.PARAM Lp11='(g1*log(g1+h11)-h11)'
.PARAM h12 = 'sqrt(g2*g2+r12)'
.PARAM Lp12='-(g2*log(g2+h12)-h12)'
.PARAM h13 = 'sqrt(g3*g3+r12)'
.PARAM Lp13='(g3*log(g3+h13)-h13)'
.PARAM h14 = 'sqrt(g4*g4+r12)'
.PARAM Lp14='-(g4*log(g4+h14)-h14)'
.PARAM Mf9='(Lp11+Lp12+Lp13+Lp14)*l*1.0e-7'
.PARAM M9='-2.0*Mf9'

.PARAM h2 = 'sqrt(PWR((x1-xp),2)+PWR((y1-yp),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r21 = 'h2/l'
.PARAM r22= 'r21*r21'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h21 = 'sqrt(g1*g1+r22)'
.PARAM Lp21='(g1*log(g1+h21)-h21)'
.PARAM h22 = 'sqrt(g2*g2+r22)'
.PARAM Lp22='-(g2*log(g2+h22)-h22)'
.PARAM h23 = 'sqrt(g3*g3+r22)'
.PARAM Lp23='(g3*log(g3+h23)-h23)'
.PARAM h24 = 'sqrt(g4*g4+r22)'
.PARAM Lp24='-(g4*log(g4+h24)-h24)'
```

```
.PARAM Mf1='(Lp21+Lp22+Lp23+Lp24)*l*1.0e-7'
.PARAM M1='Mf1'

.PARAM h3 = 'sqrt(PWR((x2-xp),2)+PWR((y2-yp),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r31 = 'h3/l'
.PARAM r32= 'r31*r31'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h31 = 'sqrt(g1*g1+r32)'
.PARAM Lp31='(g1*log(g1+h31)-h31)'
.PARAM h32 = 'sqrt(g2*g2+r32)'
.PARAM Lp32='-(g2*log(g2+h32)-h32)'
.PARAM h33 = 'sqrt(g3*g3+r32)'
.PARAM Lp33='(g3*log(g3+h33)-h33)'
.PARAM h34 = 'sqrt(g4*g4+r32)'
.PARAM Lp34='-(g4*log(g4+h34)-h34)'
.PARAM Mf2='(Lp31+Lp32+Lp33+Lp34)*l*1.0e-7'
.PARAM M2='Mf2'

.PARAM h4 = 'sqrt(PWR((x3-xp),2)+PWR((y3-yp),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r41 = 'h4/l'
.PARAM r42= 'r41*r41'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h41 = 'sqrt(g1*g1+r42)'
```

```
.PARAM Lp41='(g1*log(g1+h41)-h41)'
.PARAM h42 = 'sqrt(g2*g2+r42)'
.PARAM Lp42='-(g2*log(g2+h42)-h42)'
.PARAM h43 = 'sqrt(g3*g3+r42)'
.PARAM Lp43='(g3*log(g3+h43)-h43)'
.PARAM h44 = 'sqrt(g4*g4+r42)'
.PARAM Lp44='-(g4*log(g4+h44)-h44)'
.PARAM Mf3='(Lp41+Lp42+Lp43+Lp44)*l*1.0e-7'
.PARAM M3='Mf3'

.PARAM h5 = 'sqrt(PWR((x4-xp),2)+PWR((y4-yp),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r51 = 'h5/l'
.PARAM r52= 'r51*r51'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h51 = 'sqrt(g1*g1+r52)'
.PARAM Lp51='(g1*log(g1+h51)-h51)'
.PARAM h52 = 'sqrt(g2*g2+r52)'
.PARAM Lp52='-(g2*log(g2+h52)-h52)'
.PARAM h53 = 'sqrt(g3*g3+r52)'
.PARAM Lp53='(g3*log(g3+h53)-h53)'
.PARAM h54 = 'sqrt(g4*g4+r52)'
.PARAM Lp54='-(g4*log(g4+h54)-h54)'
.PARAM Mf4='(Lp51+Lp52+Lp53+Lp54)*l*1.0e-7'
.PARAM M4='Mf4'

.PARAM h6 = 'sqrt(PWR((xq-x5),2)+PWR((yq-y5),2))'
.PARAM v = 1.0
.PARAM p = 0.0
```

```
.PARAM r61 = 'h6/l'
.PARAM r62= 'r61*r61'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h61 = 'sqrt(g1*g1+r62)'
.PARAM Lp61='(g1*log(g1+h61)-h61)'
.PARAM h62 = 'sqrt(g2*g2+r62)'
.PARAM Lp62='-(g2*log(g2+h62)-h62)'
.PARAM h63 = 'sqrt(g3*g3+r62)'
.PARAM Lp63='(g3*log(g3+h63)-h63)'
.PARAM h64 = 'sqrt(g4*g4+r62)'
.PARAM Lp64='-(g4*log(g4+h64)-h64)'
.PARAM Mf5='(Lp61+Lp62+Lp63+Lp64)*l*1.0e-7'
.PARAM M5='Mf5'

.PARAM h7 = 'sqrt(PWR((xq-x6),2)+PWR((yq-y6),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r71 = 'h7/l'
.PARAM r72= 'r71*r71'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h71 = 'sqrt(g1*g1+r72)'
.PARAM Lp71='(g1*log(g1+h71)-h71)'
.PARAM h72 = 'sqrt(g2*g2+r72)'
.PARAM Lp72='-(g2*log(g2+h72)-h72)'
.PARAM h73 = 'sqrt(g3*g3+r72)'
.PARAM Lp73='(g3*log(g3+h73)-h73)'
.PARAM h74 = 'sqrt(g4*g4+r72)'
```

```
.PARAM Lp74='-(g4*log(g4+h74)-h74)'
.PARAM Mf6='(Lp71+Lp72+Lp73+Lp74)*l*1.0e-7'
.PARAM M6='Mf6'

.PARAM h8 = 'sqrt(PWR((xq-x7),2)+PWR((yq-y7),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r81 = 'h8/l'
.PARAM r82= 'r81*r81'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
.PARAM h81 = 'sqrt(g1*g1+r82)'
.PARAM Lp81='(g1*log(g1+h81)-h81)'
.PARAM h82 = 'sqrt(g2*g2+r82)'
.PARAM Lp82='-(g2*log(g2+h82)-h82)'
.PARAM h83 = 'sqrt(g3*g3+r82)'
.PARAM Lp83='(g3*log(g3+h83)-h83)'
.PARAM h84 = 'sqrt(g4*g4+r82)'
.PARAM Lp84='-(g4*log(g4+h84)-h84)'
.PARAM Mf7='(Lp81+Lp82+Lp83+Lp84)*l*1.0e-7'
.PARAM M7='Mf7'

.PARAM h9 = 'sqrt(PWR((xq-x8),2)+PWR((yq-y8),2))'
.PARAM v = 1.0
.PARAM p = 0.0
.PARAM r91 = 'h9/l'
.PARAM r92= 'r91*r91'
.PARAM g1='1.0+p'
.PARAM g2='g1-v'
.PARAM g3='p-v'
.PARAM g4='p'
```

```
.PARAM h91 = 'sqrt(g1*g1+r92)'
.PARAM Lp91='(g1*log(g1+h91)-h91)'
.PARAM h92 = 'sqrt(g2*g2+r92)'
.PARAM Lp92='-(g2*log(g2+h92)-h92)'
.PARAM h93 = 'sqrt(g3*g3+r92)'
.PARAM Lp93='(g3*log(g3+h93)-h93)'
.PARAM h94 = 'sqrt(g4*g4+r92)'
.PARAM Lp94='-(g4*log(g4+h94)-h94)'
.PARAM Mf8='(Lp91+Lp92+Lp93+Lp94)*l*1.0e-7'
.PARAM M8='Mf8'

.PARAM Msg='abs(M1+M2+M3+M4+M5+M6+M7+M8+M9)/6.0'

.PARAM Ldc = 'Ls+Lg/2-2*Msg+1/2*Mgg'

$ signal condcutor R&L

.PARAM k11 = '0.26+0.6*exp(0.44t/s)'
.PARAM k12 = '0.64-0.35*exp(-0.76t/s)'
.PARAM R01= '(7.6+1.2*exp(-t/s))/(1-(6.67+0.84*exp(t/s))*(PWR(ws/s,k11)))
-(6.7+1.2*exp(-8.1t/s))/(1-(6-1.4*exp(-1.2t/s))*(PWR(ws/s,k12)))'

.PARAM k21 = '-0.037-0.77*exp(-6.3t/s)'
.PARAM k22 = '0.6-0.31*exp(-0.2t/s)'
.PARAM R02= '(11.3-2*exp(2.6t/s))/(1+(2.5+4.8*exp(2.8t/s))*(PWR(ws/s,k21)))
+(21.6+10.8*exp(-0.38t/s))/(1+(9.2-2.6*exp(-0.02t/s))*(PWR(ws/s,k22)))'

.PARAM k31 = '0.6-0.37*exp(-0.31t/s)'
.PARAM k32 = '0.7-4.671*exp(-6t/s)'
.PARAM R03= '(63.8+109*exp(-14.4t/s))/(1+(7.3-5.4*exp(-1.5t/s))*(PWR(ws/s,k31)))
+(37.6-100*exp(-4.6t/s))/(1+(3.66+10*exp(2.38t/s))*(PWR(ws/s,k32)))'

.PARAM m11 = '-0.38+2.5*exp(-0.18t/s)'
```

```
.PARAM m12 = '0.5-0.36*exp(-4.5t/s)'
.PARAM p01= '(2.4-10.4*exp(-0.36t/s))/(1+(2.9+5.7*exp(-2.3t/s))*(PWR(ws/s,m11)))
-(12.9-4.3*exp(-7t/s))/(1-(6.2+6.4*exp(-0.7t/s))*(PWR(ws/s,m12)))'

.PARAM m21 = '1.89-0.67*exp(-0.94t/s)'
.PARAM m22 = '-0.5-3.6*exp(0.17t/s)'
.PARAM p02= '(18.7+25.6*exp(-3.4t/s))/(1+(1.6+6.56*exp(-1.2t/s))*(PWR(ws/s,m21)))
+(14-7.25*exp(-0.08t/s))/(1+(0.0055+3.6*exp(-0.81t/s))*(PWR(ws/s,m22)))'

.PARAM m31 = '2.1+1.15*exp(-1.46t/s)'
.PARAM m32 = '-1.9-2.7*exp(0.006t/s)'
.PARAM p03= '(-326+50*exp(0.067t/s))/(1-(5.4+4.3*exp(-0.5t/s))*(PWR(ws/s,m31)))
+(89-18*exp(-0.1t/s))/(1+(-0.42+1.5*exp(-0.034t/s))*(PWR(ws/s,m32)))'

.PARAM m41 = '1.3-1.4*exp(-1.85t/s)'
.PARAM m42 = '-1.1+0.8*exp(-1.45t/s)'
.PARAM p04= '(0.04-0.034*exp(-0.67t/s))/(1+(0.8+0.1*exp(0.17t/s))*(PWR(ws/s,m41)))
+(-0.027+0.049*exp(0.04t/s))/(1+(4.1-3.9*exp(-0.27t/s))*(PWR(ws/s,k42)))'


.PARAM L1='R01/p01/1E10'
.PARAM L2='R02/p02/1E10'
.PARAM L3='R03/p03/1E10'
.PARAM R1='R01*6E7/sigma*PWR(4E-6/t,2)'
.PARAM R2='R02*6E7/sigma*PWR(4E-6/t,2)'
.PARAM R3='R03*6E7/sigma*PWR(4E-6/t,2)'
.PARAM L4='Ldc-Linf-L1-L2-L3'
.PARAM R4='1/p04/L4/1E10'

Rdc0 1 4 'Rdc*length'
Linf0 4 5 'Linf*length'
R1 5 6 'R1*length'
L1 5 6 'L1*length'
```

```
R2 6 7 'R2*length'
L2 6 7 'L2*length'
R3 7 8 'R3*length'
L3 7 8 'L3*length'
R4 8 9 'R4*length'
L4 8 9 'L4*length'

.ENDS
```

Appendix C: Power Loss Calculation for Metal Fill in Uniform Magnetic Field in Arbitrary Direction

To account for eddy current loss in the metal fills due to magnetic field in an arbitrary direction, we decompose the applied magnetic field $\vec{H}_a$ at the fill into its three orthogonal components whose directions span the metal fill volume

$$\vec{H}_a = \vec{x}H_x + \vec{y}H_y + \vec{z}H_z. \tag{C.1}$$

The contributions to power loss in the metal fill due to each orthogonal magnetic field component are orthogonal to each other and thus are separable [92]. As shown in Fig. C.1, we can express the eddy-currents in the metal fill due to $\vec{H}_z$ and $\vec{H}_y$ as

$$\vec{J}_1 = \vec{x}f_1(x,y,z) + \vec{y}f_2(x,y,z) \tag{C.2}$$

$$\vec{J}_2 = \vec{x}g_1(x,y,z) + \vec{z}g_2(x,y,z). \tag{C.3}$$

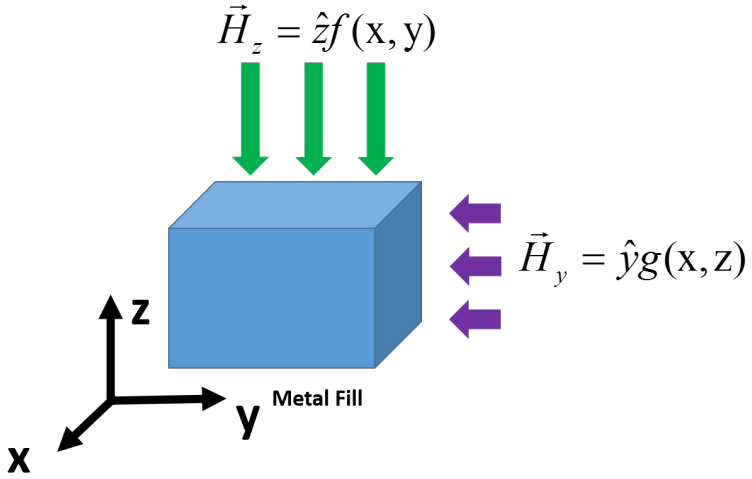

Figure C.1: Decomposition of magnetic field at metal fill.

Assuming $\vec{H}_x$=0, the total power loss can be derived as

$$P = \frac{1}{2}\iiint_V \frac{\left|\vec{J}_1 + \vec{J}_2\right|^2}{\sigma}\, dv = \frac{1}{2}\iiint_V \frac{f_1^2 + f_2^2 + g_1^2 + g_2^2 + 2f_1 g_1}{\sigma}\, dv. \tag{C.4}$$

If the origin of the coordinate system is at the center of the metal fill, based on symmetry we obtain

$$f_1(x, y, z) = -f_1(x, -y, z) \tag{C.5}$$

$$g_1(x, y, z) = g_1(x, -y, z). \tag{C.6}$$

Since $f_1 g_1$ is an odd function along the x-z plane over the volume of the metal fill,

$$\iiint_V \frac{f_1 g_1}{\sigma}\, dv = 0 \tag{C.7}$$

and thus

$$P = \frac{1}{2}\iiint_V \frac{\left|\vec{J}_1 + \vec{J}_2\right|^2}{\sigma}\, dv = \frac{1}{2}\iiint_V \frac{\left|\vec{J}_1\right|^2}{\sigma}\, dv + \frac{1}{2}\iiint_V \frac{\left|\vec{J}_2\right|^2}{\sigma}\, dv. \tag{C.8}$$