AN ABSTRACT OF THE DISSERTATION OF

Hariprasath Venkatram for the degree of Doctor of Philosophy in Electrical Engineering and Computer Science presented on August 20, 2013.

Title: Energy and Area Efficient Techniques for Data Converters

Abstract approved: _____

Un-Ku Moon

Data converters are ubiquitous building blocks of a signal chain. The rapid increase in communication and connectivity devices presents new avenues for pushing the state of the art analog to digital converters. Techniques for improving resolution, bandwidth, linearity and bit-error rate, while reducing the power, energy and area is the motivation for this research. This research focuses on achieving this goal by enabling circuit techniques, architecture techniques and calibration methods. The following techniques are proposed for enabling power, area and energy efficient analog to digital converter techniques.

1. A capacitor switching scheme for successive approximation ADC is introduced to enable 93.4% energy reduction and 75 % reduction in capacitor area as compared to a conventional SAR ADCs.

2. Asynchronous correlated level shifting technique for improving current source linearity and power supply rejection ratio of zero crossing based circuits is proposed. This technique enables asynchronous ADC architectures for energy efficient system.

3. Unified gain enhancement model is proposed to catalogue gain enhancement techniques. Class-A+ and Replicated Parallel Gain Enhancement (RPGe) amplifiers are introduced as parallel gain enhancement techniques for switched capacitor circuits. A prototype pipelined ADC using RPGE amplifier achieves 74.9 dB SNDR, 90.8 dB SFDR, 87 dB THD at 20 MS/s. Built in 1P4M 0.18 μm technology and operating at 1.3 V supply, the ADC consumes 5.9 mW. The ADC occupies 3.06 sq. mm and has a figure of merit of 65 fJ /conversion step. Extracted simulation results of the prototype pipeline

ADC using dynamic RPGE amplifier achieve 74 dB SNDR, 90 dB SFDR, and 85 dB THD at 30 MS /s in a 0.18 μm process. The ADC consumes 6.6 mW from a 1.3 V supply and achieves a figure of merit of 40 fJ/C-S.

4. A low-gain amplifier based V-T converter is utilized along with a TDC to replace the function of flash ADC and the DAC references in a pipeline ADC. The simulated/extracted performance of the chip is 12bit, 100 MHz in 65nm process while consuming approximately 8-9 mA from 1 V supply.

5. A measurement technique for detecting and correcting bit-error rate in ADCs is proposed. This multi-path ADC technique squares the bit-error rate of the ADC without consuming additional analog power. The area increase is negligible compared to the conventional modular redundancy techniques. This technique can be applied to digitally detect and correct single event transients for ADCs. A three-path ADC can restore the ADC performance independent of the input frequency and number of errors in a single path.

6. LMS algorithm is used to estimate the VCO non-linearity by using the VCO as a Nyquist ADC and utilizing a slow but accurate ADC. The simulated ADC performance improves from 5 bits to 7.8 bits by using a second order fit to the VCO non-linearity.

Energy and Area Efficient Techniques for Data Converters

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APPROVED:

Major Professor, representing Electrical Engineering and Computer Science

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I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Hariprasath Venkatram, Author

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Chapter 1. Introduction

1.1 Background

Analog to Digital Converter (ADC) are ubiquitous building blocks of a signal chain. Fig. 1.1 shows typical application of analog-to-digital converters. The design of ADC has its roots in the telecommunication industry. With the advances in the communication, connectivity, automotive, entertainment, space and military applications, the need for high performance, low power, small footprint solutions are all but necessary design constraints. Fig. 1.1 shows the general trend in the use of different data converters for a variety of applications. Classical architectures such as flash, pipeline, integrating, delta-sigma converters, folding and time-interleaved architectures have re-defined their reach with the availability of deep sub-micron process. A detailed tabular column shown in Table. 1.1 provides an insight into the need for resolution, bandwidth, dynamic range and the possible architecture for a given application. It is imperative that the above mentioned parameters of interest must be realized with minimum power, energy and area.

1.2 Organization

The research focus for the thesis is energy and area efficient analog to digital converter techniques and architectures.

In the second chapter, various trade-off in an ADC design are analyzed with an emphasis on calibration and architectural techniques to achieve energy and area efficient design. In particular, deterministic calibration of VCO non-linearity and multi-path ADC technique to build a robust architecture tolerant towards single event effects and bit-error rate.

In the third chapter, circuit techniques are explored in detail achieve energy and area efficiency. To this end, merged capacitor switching energy scheme for SAR ADC, a unified gain enhancement model for amplifiers, class A+ amplifier technique, asynchronous CLS

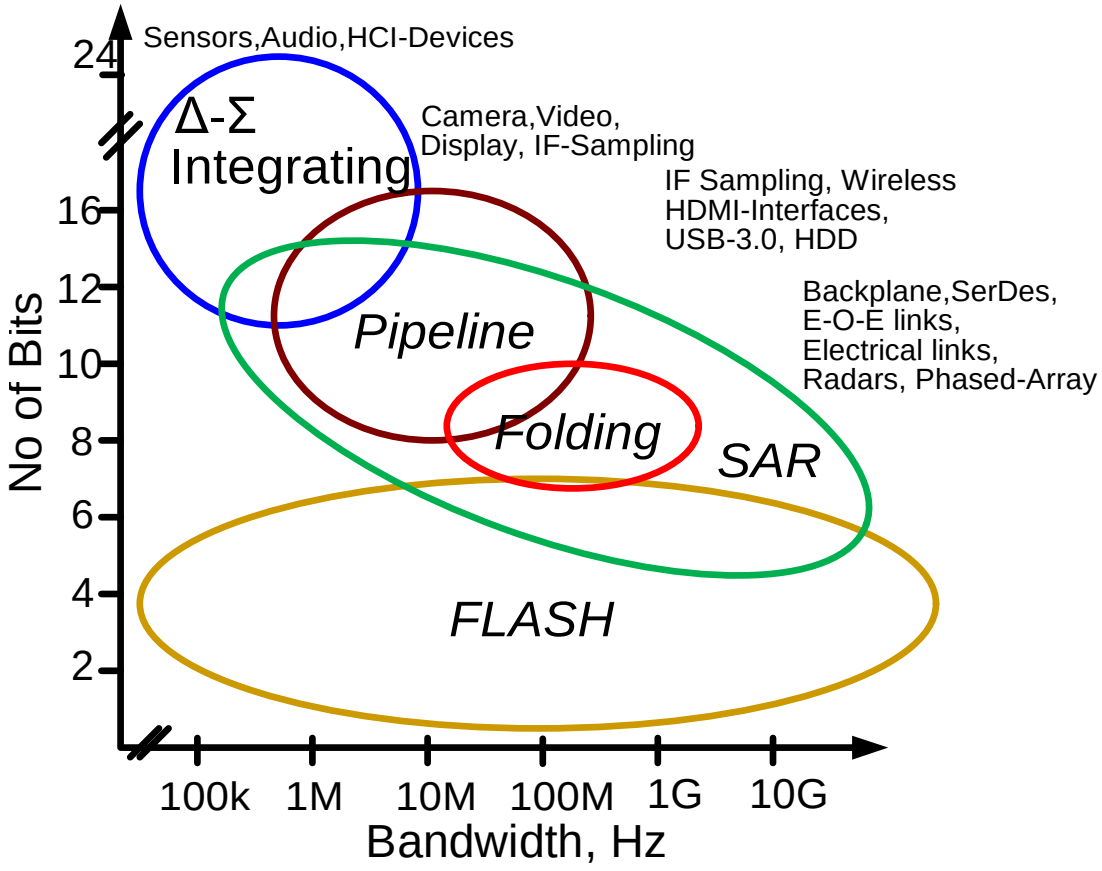


Figure 1.1: ADC Architecture, Resolution vs. Bandwidth

Table 1.1: Architecture and Application

Network	Bandwidth	Resolution/DR	Architecture
Radio, Audio, AM/FM	40 kHz	$\geq$ 16 b, 100 dB	Delta-Sigma
GSM, Bluetooth	135 kHz-500 kHz	$\geq$ 85 dB	Delta-Sigma
UMTS-WCDMA	5 MHz	$\geq$ 65 dB	Delta-Sigma, Pipeline
CDMA	1.25 MHz	$\geq$ 65 dB	Delta-Sigma
DVB-T, T2	8 MHz	$\geq$ 55 dB	Pipeline
Sensor Array	$\leq$ 5 MHz	6-10 b	SAR, Pipeline, Integrating
Medical	$\leq$ 1 MHz	$\geq$ 16 b	SAR, Delta-Sigma
3G/LTE	20-40 MHz	$\geq$ 60 dB	Pipeline, Delta-Sigma
Direct TV	1.5 GHz	$\geq$ 54 dB	Pipeline
802.11 ac/d (WiGiG)	5 GHz	$\geq$ 30 dB	Flash/TI-SAR/Pipeline

technique, replicated parallel gain enhancement technique, dynamic replicated parallel gain enhancement technique are proposed and discussed in detail with prototype and simulation results.

In the fourth chapter, a hybrid time based pipeline ADC amenable towards technology scaling is proposed which utilize both circuit and calibration techniques to realize a power efficient design. Chapter five concludes the thesis with scope for future work.

1.3 Contribution

- Deterministic Calibration of VCO Non-Linearity
- Multi-path ADC Technique for detection and correction of bit-error rate/ single event error
- Unified Gain Enhancement Model
  - Replicated Parallel Gain Enhancement technique amplifier
  - Dynamic RPGE Amplifier
  - Asynchronous CLS technique
  - Class A+ amplifier technique
- Time-to-Digital Converter replacement for flash ADC and capacitor DAC in a traditional pipeline ADC

Chapter 2. Architecture and Calibration Techniques for Analog to Digital Converters

2.1 Introduction

A brief literature survey provides us with the traditional ADC architectures, components and non-idealities [1–7]. The ADC design involves multiple conflicting trade-off shown in Fig. 2.1. In general, area and power are the optimization parameters for a given linearity, bandwidth and noise.

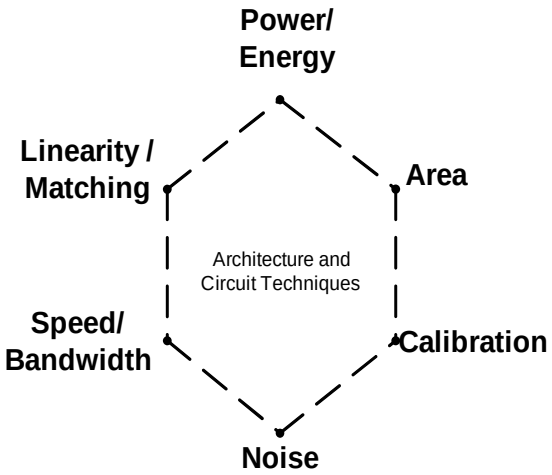


Figure 2.1: ADC Design Tradeoff

Table. 2.1 is a rudimentary list that provides us with the topics to explore new and improved circuit techniques that circumvent, eliminate or tolerate the non-idealities listed for each architecture.

In this chapter, we discuss architecture and calibration techniques to improve the energy and area efficiency of a data converter without sacrificing performance. Deep sub micron CMOS process is prone to variation due to several manufacturing steps. It is not surprising that the components such as resistors, capacitors and transistors also

Table 2.1: Analog to Digital Converter Architectures and Component Limitations

Architecture	Non-Ideality
Flash	matching, reference, offest, timing and jitter.
SAR	matching, settling, reference and (a)synchronous timing.
Folding	offset, matching, nonlinearity and averaging.
Sub-ranging	reference, matching, noise and offset.
Cyclic	offset, matching, finite gain, nonlinearity and jitter.
Pipeline	offset, matching, finite gain, nonlinearity and jitter.
Integrating	offset, matching, timing, noise and nonlinearity.
$\Delta - \Sigma$	stability, delay, matching, jitter and nonlinearity.

experience variation in their parameters. These components are used to realize feedback factor, time constant, current source, transconductance, integrators, reference voltages and amplifiers which are in turn used as building blocks for realizing data converters and filters. In order to meet certain matching, the components must be sized accordingly. Therefore, this design methodology results in an sub-optimal design and it might be impossible to optimize area, power and performance simultaneously. To this end, it is necessary to resort to measurement and correction techniques. In this chapter, a deterministic LMS calibration method for measuring and correcting VCO non-linearity and a Multi-path ADC for detection and correction of single event error (SEE)/ bit-error-rate (BER) are discussed in detail.

2.2 Survey of Calibration Methods

Data Converters are a system built with individual blocks discussed in the previous section. It is worthwhile to consider the different architectures, component mismatches and existing calibration techniques. The following tabular column lists the architecture, non-idealities and calibration methods. The calibration methods can be broadly classified into deterministic, statistical, linear and non-linear methods. Convergence, accuracy, model order, complexity of hardware implementation are the important factors for evaluating or comparing various methods. In particular, deterministic calibration using LMS and split-ADC techniques are utilized to improve the performance.

Table 2.2: Architecture and Non-Ideality

Architecture	Non-Ideality	Technique
Pipeline	Capacitor Mismatch, Non-Linearity	Split-ADC
SAR	Gain Compression	PN Sequence
$\Delta - \Sigma$	DAC Mismatch, Timing	(Non)Linear Error Correction
Folding	Resistor Mismatch, Averaging Error	Deterministic Correction
Time-Interleaved	Gain, Offset, Phase Skew	Look-Up Table
TDC	Delay, Meta-Stability, Dynamic Errors	Phase Skew Estimation
VCO	Nonlinearity	DEM, DWA, Blind Correction

2.2.1 Deterministic LMS fit

Least Mean Square estimation is a deterministic estimation. Given the following model, H, the non-linearity can be estimated from the input and the observed output. Eq. 2.1 shows the generic model equation. Where, $\underline{Y}$ is the observed data, $\underline{\Theta}$ is the model input and $\underline{\underline{H}}$ is the parameters of interest. Eq. 2.2 shows the least mean square estimation of the parameters $\widehat{\Theta_{lms}}$. The line fitting example explains the above model in detail.

$$\underline{Y}=\underline{\underline{H}}.\underline{\Theta} \tag{2.1}$$

$$\underline{\widehat{\Theta}}_{\mathrm{LMS}}= (\underline{\underline{H}}^{\mathrm{T}}\underline{\underline{H}})^{-1}\underline{\underline{H}}^{\mathrm{T}}\underline{Y} \tag{2.2}$$

Given a set of points, $(x_1,y_1), (x_2,y_2).....(x_n,y_n)$, the best fit line using LMS algorithm can be derived as shown in Eq. 2.3. In this setup, "m" is the LMS fit parameter. The parameter m can be evaluated from Eq. 2.2 as given by Eq. 2.4. The above example can be extended to ADCs as explained in [8].

$$\begin{bmatrix} y_1 \\ y_2 \\ . \\ . \\ y_n \end{bmatrix} = \begin{bmatrix} x_1 \\ x_2 \\ . \\ . \\ x_n \end{bmatrix} . [m] \tag{2.3}$$

$$\widehat{m_{LMS}} = \sum_{i=1}^{N} x_i y_i / \sum_{i=1}^{N} x_i^2 \tag{2.4}$$

2.2.2 Split-ADC Calibration Technique

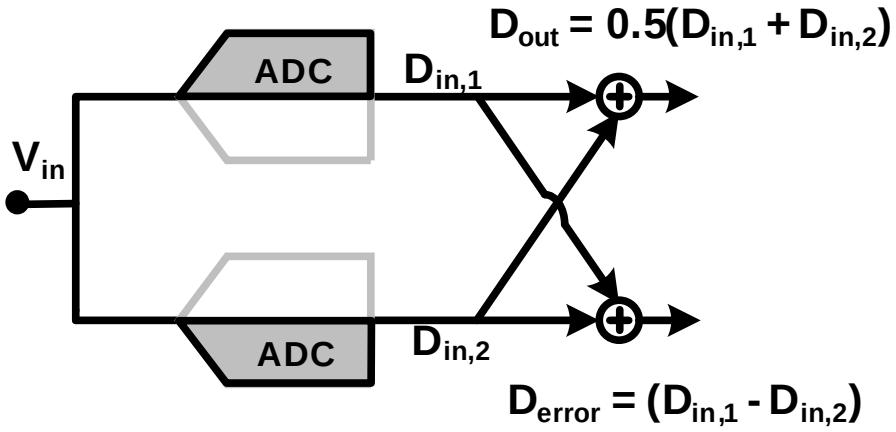


Figure 2.2: Split ADC

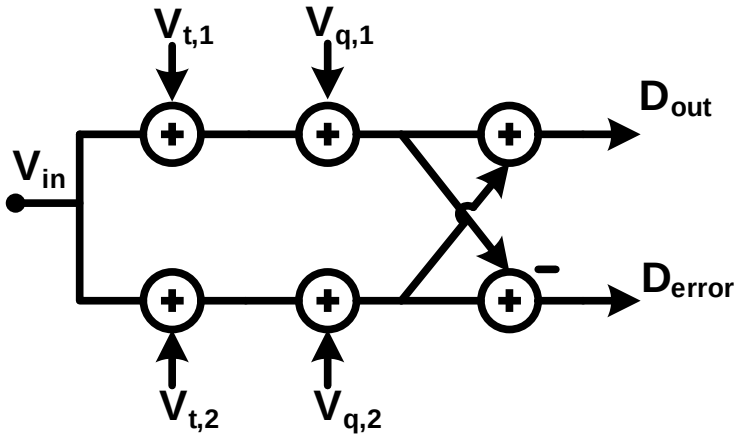


Figure 2.3: Split ADC

Every capacitor and transconductance or opamp is split into two smaller pieces as

shown in Fig. 2.2. The thermal noise power contribution increases by a factor of two due to this scaling. Fig. 2.3 shows the noise model for the split-ADC. $V_{t,1}$ and $V_{t,2}$ represents the thermal noise contribution from the analog section of the split-ADC. $V_{q,1}$ and $V_{q,2}$ represents the quantization noise of the split-ADC. It can be readily observed that the averaged output, D_{out}, has the same signal to noise ratio of the combined ADC.

D_{out} contains the averaged output of the split-ADC and D_{error} contains information about the mismatch between the two channels. The signal content is removed in D_{error} and any anomaly between the channels can be detected from this digital error signal. In this application, along with the mismatch between the two-paths, single event effects and bit-error rates can be detected and corrected. Further details regarding the split-ADC technique can be found in [9] and [10]. The digital section is the overhead for the split-ADC technique. The analog section made up of transconductors, capacitors, and resistors does not increase in area or power.

2.3 Deterministic Calibration of VCO Non-Linearity

2.3.1 Background

The time based ADC architectures are promising in deep-sub micron due to smaller delay generation and large tuning range available from the voltage controlled oscillators (VCO). However, the delay cells and VCO suffer from non-linearity. The linearity of VCO is limited to 5%, which results in a 6 bit resolution, [11]. In order to achieve higher resolution, the linearity of VCO must be improved. In [12], a Nyquist rate VCO based ADC was realized by building a linear VCO. However, the effective number of bits was limited to 8 because of VCO non-linearity. In [11], the VCO was enclosed in a feedback loop to improve linearity. However, this oversampled system requires high frequency sampling clock which limits the maximum oscillation frequency of the VCO. To this end, an attempt is made to measure nonlinear VCO curve using a deterministic calibration technique.

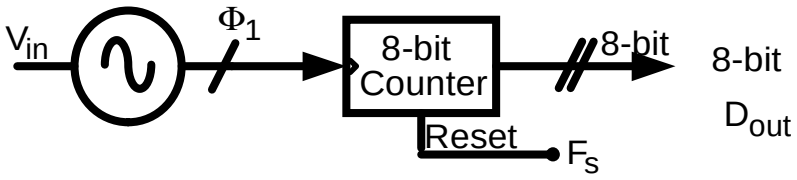


Figure 2.4: VCO Couting ADC

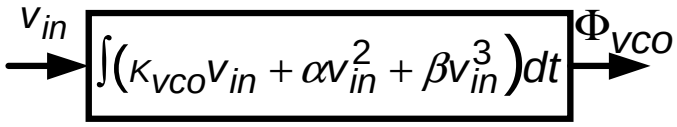


Figure 2.5: VCO Non-Linearity

2.3.2 Limitation of VCO based ADC

The 8-bit time based ADC is shown in 2.4. It consists of a coarse 8-bit converter. The 8-bit coarse converter is implemented with a binary counter clocked by the VCO and reset by the sampling clock The multi-phase VCO was implemented as an 8-stage differential ring oscillator. The conversion of tuning voltage to phase by a VCO is given by Eq. 2.5 for a sinusoidal input. Where, K_{vco} is the VCO gain in Hz/V, is the sampling frequency of the ADC, V_{in} is the amplitude of the input, ω_{in} is the input frequency. The above expression indicates a sinc filtering of the input voltage. This provides an inherent anti-aliasing filter for the input signal, [13].

$$\begin{aligned}\Phi_{\mathrm{vco}}(\mathrm{n}) &= 2\pi \int_{nT_s}^{nT_s+T_s} (\mathrm{K_{vco}v_{in}sin}(\omega_{\mathrm{in}}\mathrm{t})+\mathrm{f_{ref}})\,\mathrm{dt} \\ &= 2\pi\mathrm{K_{vco}T_s v_{in}sin}\left(\omega_{\mathrm{in}}\left(\mathrm{nT_s}+\mathrm{T_s}/2\right)\right).\left(\frac{\sin(\omega_{\mathrm{in}}\mathrm{T_s}/2)}{\omega_{\mathrm{in}}\mathrm{T_s}/2}\right) \\ &= 2\pi\mathrm{K_{vco}T_s v_{in}sin}\left(\omega_{\mathrm{in}}\left(\mathrm{nT_s}+\mathrm{T_s}/2\right)\right).\mathrm{sinc}(\omega_{\mathrm{in}}\mathrm{T_s}/2)\end{aligned} \tag{2.5}$$

The VCO non-linearity can be modeled as shown in Fig. 2.5. Assuming a sinusoidal input, the attenuation provided by VCO for the fundamental and harmonics can be derived as shown in Eq. 2.6. Where, K_{vco}, V_{in}, T_s, ω_{in} have the same meaning as in Eq. 2.5. α, β are the second and third order non-linearity coefficients of the VCO. Phase offset is a collection of terms independent of the input frequency. For an input signal

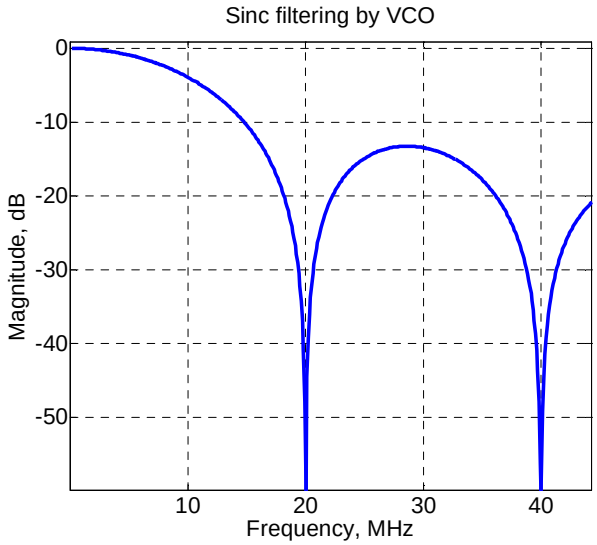


Figure 2.6: Sinc Filter of VCO Input

of 6 MHz, the non-linear VCO will generate harmonics at 12 MHz, 18 MHz and so on. However, the attenuation provided by VCO for 6 MHz, 12 MHz, 18 MHz are -1.5 dB, -6 dB and -18 dB respectively. Thus, the harmonics are attenuated by the sinc filter as shown in Fig. 2.6.

$$\begin{aligned}\Phi_{vco}(n) = {} & 2\pi K_{vco} v_{in} T_s \sin(\omega_{in}(nT_s+T_s/2))\mathrm{sinc}(f_{in}T_s) \\ & + \frac{2\pi\alpha v_{in}^2 T_s}{2}\cos(2\omega_{in}(nT_s+T_s/2))\mathrm{sinc}(2f_{in}T_s) \\ & + \frac{2\pi\beta v_{in}^3 T_s}{4}\sin(3\omega_{in}(nT_s+T_s/2))\mathrm{sinc}(3f_{in}T_s) \\ & + \mathrm{phaseoffset}\end{aligned} \tag{2.6}$$

2.3.3 LMS setup for VCO ADC

The radixes of the ADC are the parameters of interest. A slow but accurate ADC quantizes the input as shown in Fig. 2.7. The output from the slow ADC is compared with the output from the ADC under calibration. This calibration method does not need

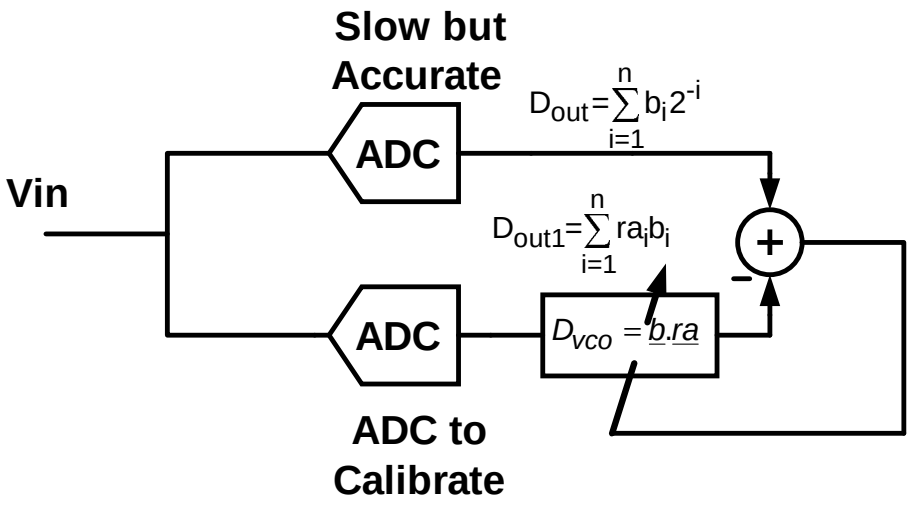


Figure 2.7: Calibration Method

separate calibration signals and can be performed in the background. Since, LMS is a deterministic calibration method; the convergence time for the algorithm is smaller than the correlation based algorithms.

From Eq. 2.6, the output phase of the VCO can be re-written as given in Eq. 2.7. Where, α, β, γ, model the non-linearity of the VCO and $\phi_e(n)$ model the quantization error from the VCO based ADC. Rearranging Eq. 2.7, we get Eq. 2.8. v_{in}, v_{in}^2 is approximated by D_{out} and D_{out}^2 from the slow ADC output decimal code. $\Phi_{vco}(n) + \phi_e(n)$ is obtained from the VCO ADC output code. The VCO characterization is performed as given in Eq. 2.9.

$$\Phi_{vco}(n) = \alpha v_{in} + \beta v_{in}^2 + \gamma v_{in}^3 + \phi_e(n) \tag{2.7}$$

$$v_{in} = \alpha'(\Phi_{vco}(n) + \phi_e(n)) + \beta' v_{in}^2 + \gamma v_{in}^3 \tag{2.8}$$

Where, $D_{out}(1)$,$D_{out}(2)$,....,$D_{out}(n)$ are the output codes from the slow ADC in decimal format. $b_{i,1}$,$b_{i,2}$,...,$b_{i,8}$ are the 8-bit binary output codes from the VCO based ADC. $ra_1, ra_2, \ldots, ra_8$, are the radixes to be estimated for the VCO based ADC. α', accounts for the second order non-linearity from the VCO. $\underline{e}$, represents the error in this model. The error term consists of quantization error, circuit noise and the error in the parameters

to be estimated. The sinc filtering provided by the VCO attenuates the higher order harmonics. Therefore, the higher order harmonics were not modeled in Eq. 2.8. The radixes can be estimated using Eq. 2.2 as shown in Eq. 2.10. The estimated radixes account for the non-linearity in VCO and mismatch in the phase separation of the multi-phase VCO.

$$\begin{bmatrix} D_{out}(1) \\ D_{out}(2) \\ . \\ . \\ D_{out}(n) \end{bmatrix} = \begin{bmatrix} b_{1,1} & . & . & b_{1,8} & D_{out}(1)^2 \\ b_{2,1} & . & . & b_{2,8} & D_{out}(2)^2 \\ . & . & . & . & . \\ . & . & . & . & . \\ b_{n,1} & . & . & b_{n,8} & D_{out}(n)^2 \end{bmatrix} . \begin{bmatrix} ra_1 \\ ra_2 \\ . \\ . \\ ra_8 \\ \alpha' \end{bmatrix} + \underline{e} \tag{2.9}$$

$$\underline{D_{out}} = \underline{\underline{B}}.\underline{ra} + \underline{e}$$

$$\begin{bmatrix} ra_{1,LMS} \\ ra_{2,LMS} \\ . \\ . \\ ra_{8,LMS} \\ \alpha' \end{bmatrix} = (\underline{\underline{\mathrm{B}}}^{\mathrm{T}}\underline{\underline{\mathrm{B}}})^{-1}\underline{\underline{\mathrm{B}}}^{\mathrm{T}}\underline{\mathrm{D}_{out}} \tag{2.10}$$

2.3.4 Simulation Results

An 8-bit VCO based ADC was simulated with a 5-bit linear VCO. The sampling frequency was chosen to be 10 MHz. The VCO tuning range was close to 2.2 GHz. The tuning curve of the VCO is shown in Fig. 2.8. The simulation setup shown in Fig. 2.7 was used for LMS calibration. The LMS setup in Eq. 2.8 was used to calibrate the VCO codes. The estimated VCO transfer curve is shown in Fig. 2.9. The Power Spectral Density (PSD) of the 8-bit VCO ADC before calibration is shown in Fig. 2.10. The SNDR is limited to 5 bits due to the non-linearities present in the VCO. The model in Eq. 2.9 was used to calibrate this VCO based ADC. The calibrated output PSD of the VCO based ADC is shown in Fig. 2.11. The SNDR of the calibrated ADC is 46.7 dB. The improvement in SNDR is close to 2.3 bits.

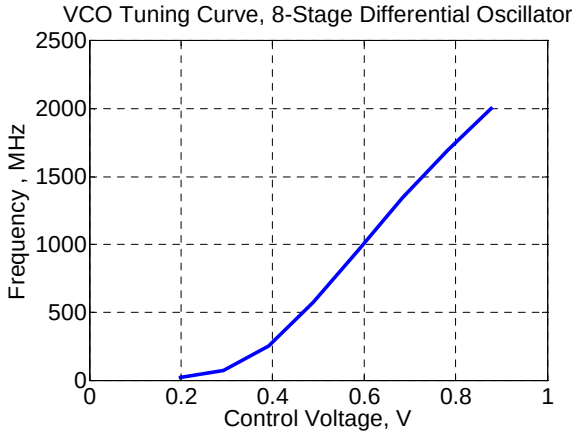


Figure 2.8: Tuning Curve

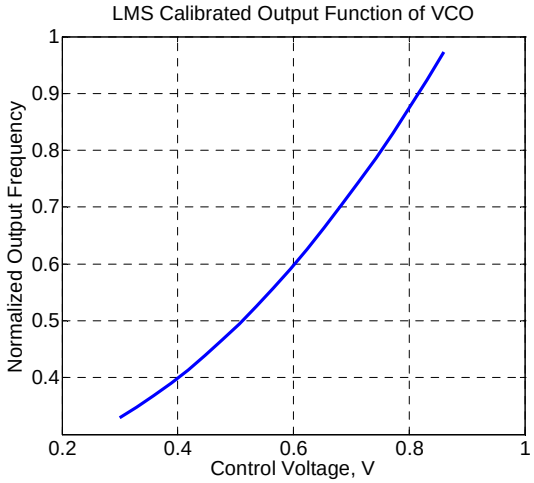


Figure 2.9: LMS Fit

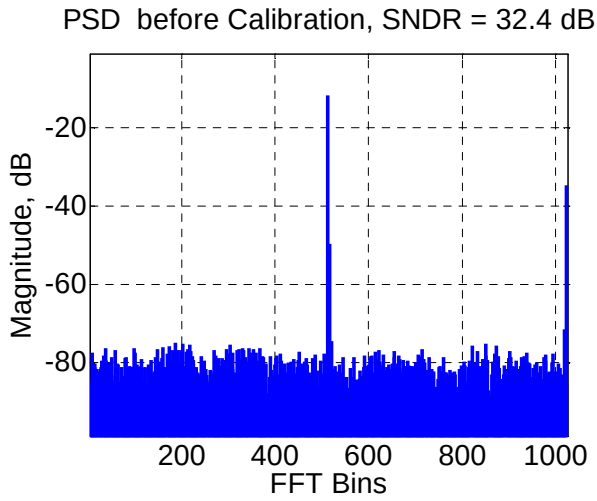


Figure 2.10: PSD Before Calibration

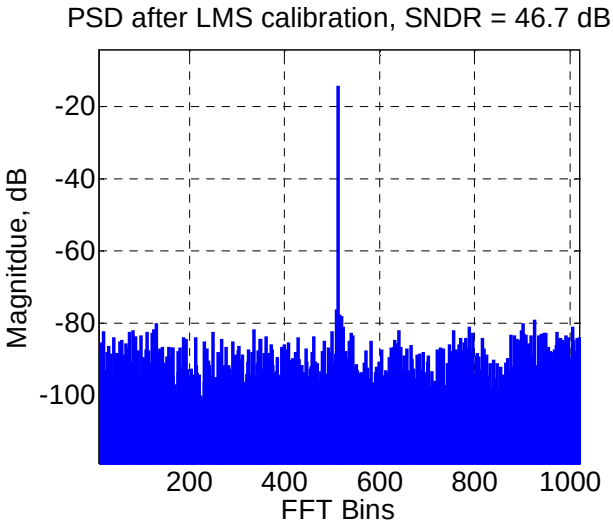


Figure 2.11: PSD After Calibration

2.4 Multi-Path ADC Technique

2.4.1 Background

Data-converters required for space electronics cover frequency ranges from few Hz to several hundreds of MHz and resolution ranges from 6 to 24 bits. No single data-converter architecture can satisfy this requirement in resolution and bandwidth at this juncture. Radiation hardening and BER reduction for such a block provides additional challenges to their design. In particular, single event effect (SEE) such as single event transients and single event upsets significantly degrade performance of the data converters.

Conventional radiation hardening methods for data-converters are architecture specific and often involve extensive simulation of circuit blocks with modified SPICE models, [14–16] and device level simulations. Therefore, it is fair to say that architecture independent radiation hardening and BER reduction techniques for data converters are desirable. Also, high level modeling and simulation methods will enable fast verification of extensive device and circuit simulations. Such techniques will enable reusable and robust design practices for building and testing data-converters. Ideally, these techniques should achieve this without any additional area or power penalty to the data-converter design. To this end, the following sections address the issue of metastability induced bit-error rate, single event error using multi-path ADC and calibration using fractional interpolation, skip and fill, and majority voting calibration techniques.

2.4.2 Mixed Signal Redundancy

In digital system design, triple modular redundancy (TMR) is extensively used for control and data paths to provide radiation hardening against single event upsets. However, this method suffers from area, power and performance penalties. A mixed signal design equivalent to the digital TMR technique is the multi-path ADC technique. This multi-path ADC technique enables a high level modeling, robust detection and correction method for SEE errors in an analog to digital converter. This multi-path ADC technique retains the benefit of digital TMR for radiation hardening and BER reduction without the penalties of analog area, power and performance.

Fig. 2.12 shows the two-path and three-path ADC implementation. The analog

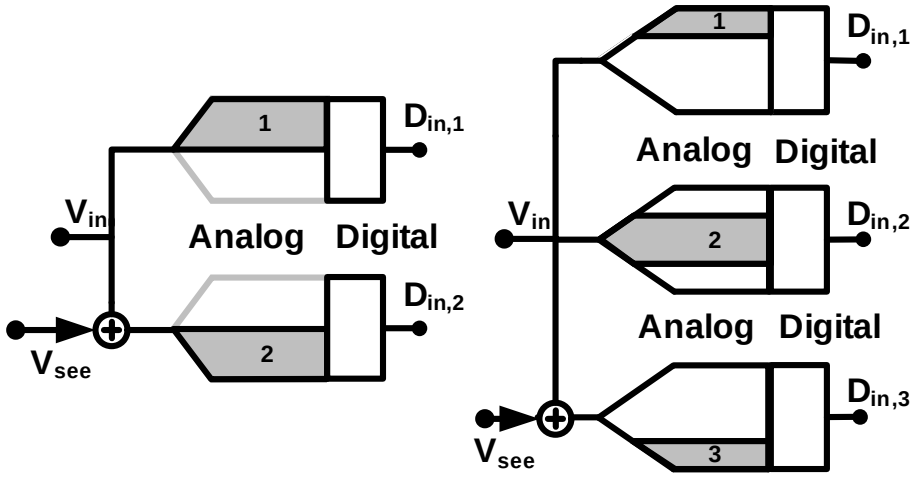


Figure 2.12: Two and Three path ADC

portion of the ADC such as opamps, capacitors and comparators sized for thermal noise are split into equal parts. The two-path ADC is implemented in the same manner as a split-ADC while the three-path ADC is implemented by dividing the analog portion of the ADC into three smaller pieces and replicating the digital section. The shaded region represents the reduced size of each path obtained by splitting the analog blocks of the ADC built for thermal or quantization noise. The combined output of the multi-path ADC is obtained by taking the average of each ADC output ($D_{in,1}, D_{in,2}$,).

The multi-path ADC technique not only allows calibration for gain and offset error but also provides digital detection and correction of single event effects and an improved bit-error rate in ADCs. The detection and correction of single event is achieved by monitoring the digital outputs ($D_{in,1}, D_{in,2}$,) of the multi-path ADC. The multi-path ADC digital output carries information about a single event effect or bit-error rate from all possible internal nodes of the ADC from each path. Therefore, a simple comparison of digital output among the different paths against a digital threshold allows us to detect and correct SEE/BER.

Multi-path ADC technique can be thought of as a mixed signal version of the digital TMR. Thanks to the multi-path ADC technique, the analog section of the ADC does not see any area increase as compared to their digital TMR counterpart. The advantages of the multi-path ADC technique are summarized as follows: 1) Digital detection

mechanism for SEE and bit error rate. 2) Real time correction methods based on digital outputs. 3) The detection and correction methods are independent of data converter architecture making it a robust and re-usable solution.

2.5 Modeling of Single Event Effect in ADC

Literature survey of SEE in analog to digital converter reveals a Gaussian model for SEE from the observed data [17], [18], [19], [20] and [21]. Thanks to the multi-path ADC technique, digital detection of SEE/BER enables fast and accurate high level modeling using this Gaussian model. By studying the digital output, we can monitor the single event error from internal nodes of the data converter that affect the digital output. A conventional technique for studying the single event effects would involve device level simulation or simulation with modified SPICE models[[19], [20]]. In this conventional approach, critical nodes have to be identified and studied extensively through circuit and device simulators. Such methods are time consuming for a bigger system like a data converter and are computationally intensive to study the effects from all the blocks of a data converter. Unlike the conventional method, the multi-path ADC technique is independent of the data converter architecture and is amenable towards existing macro-modeling techniques for analog to digital converter. The digital detection is more efficient than analyzing the single event effects by studying transient voltage or current waveforms at a critical node in a given data converter. In the following sections, system level model for SEE, an application of SEE macro-model in a pipelined ADC, simulation results of SEE in a pipelined ADC and the need for detection and correction methods are explained in detail.

2.5.1 System Level Model for SEE

Fig. 2.13 shows a noise model for the ADC including an SEE noise source. V_{SEE} is a Gaussian random noise source for modeling SEE. V_t and V_q are Gaussian and uniform random noise sources for modeling thermal and quantization noise respectively. The derivation of the random voltage source for single event effect is described in appendix. A. Signal to noise ratio for a given standard deviation (σ_{see}), repetition rate (N_{rep}) and observation window (N_{window}) is shown in Eq. 2.11. The combined signal to noise ratio

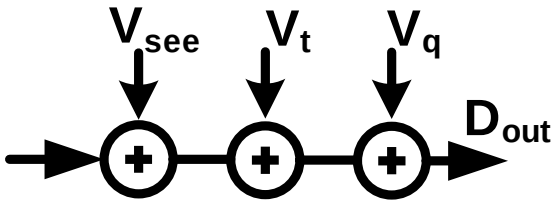


Figure 2.13: Noise Model for SEE in ADC

along with the thermal and quantization noise is shown in Eq. 2.12. Where, $E(Vt^2)$ and $E(Vq^2)$ represent thermal and quantization noise power contribution. As shown in Fig. 2.13, SEE can be modeled as an error voltage source. The error voltage(V_{see}) for a given ADC resolution (n), charge transferred (Q_{see}) and reference voltage (Vref = 1.2 V) is given by Eq. 2.13 and Eq. 2.14.

$$\mathrm{SNR_{SEE}}=\frac{\mathrm{V_{rms}}^2.\mathrm{N_{window}}}{\sigma^2{}_{\mathrm{see}}.\mathrm{N_{rep}}} \tag{2.11}$$

$$\mathrm{SNR_{total}}=\frac{\mathrm{V_{rms}}^2}{\sigma^2{}_{\mathrm{see}}.\mathrm{N_{rep}}/\mathrm{N_{window}}+\mathrm{E}(\mathrm{V_t^2})+\mathrm{E}(\mathrm{V_q^2})} \tag{2.12}$$

$$\mathrm{C_s}=\frac{12\mathrm{kT}.2^{2\mathrm{n}}}{\mathrm{V_{ref}^2}} \tag{2.13}$$

$$\mathrm{V_{see}}=\frac{\mathrm{Q_{see}}}{\mathrm{C_s}}=\frac{\mathrm{Q_{see}}.\mathrm{V_{ref}^2}}{12\mathrm{kT}.2^{2\mathrm{n}}} \tag{2.14}$$

Where C_s is the minimum sampling capacitance in Farad, k is the Boltzmanns constant and T is the temperature in Kelvin. The error voltage plot in Fig. 2.14 shows that the single event effect can saturate an ADC up to 10 bits and significantly reduce the dynamic range above 10-bit resolution. It can be observed from Fig. 2.14, that the commonly used radiation hardening technique of increasing the capacitor value (C_s) to decrease the transient effect will not only increase area and power consumption of the system but also reduce the maximum achievable sample rate of the system.

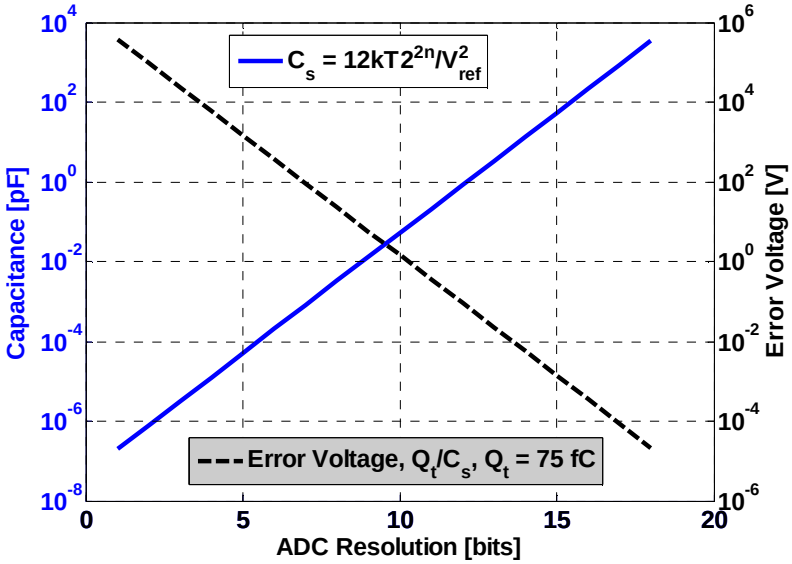


Figure 2.14: Capacitance and Error Voltage vs. ADC Resolution

2.5.2 SEE Model for Pipeline ADC

The single event effect is modeled as a Gaussian random voltage source ($S_0 - S_5$), [20]. The above modeling method is applied to a 12-bit pipelined ADC macro-model to study the single event effects from switches and amplifiers. The 12-bit pipelined ADC consists of five 2.5-bit stages followed by a 3-bit flash ADC as shown in Fig. 2.15. Each stage is made up of a sub-ADC, DAC and an amplifier as shown in Fig. 2.16.

Based on 12-bit noise and matching requirements, the typical input sampling capacitor is 2 pF and feedback capacitor of 500 fF, [22]. A Capacitor scaling factor of 2 is applied for matching considerations for the four stages resulting in feedback capacitors of 250 fF, 125 fF and 62.5 fF for stages 2, 3 and 4 respectively. The fifth stage is a replica of stage-4 with feedback capacitor of 62.5 fF.

Fig. 2.17 shows a generic switched capacitor amplifier used in a pipeline ADC with non-overlapping clock phases (ϕ_1 and ϕ_2). The SEE for the switches can modeled by an equivalent random voltage source ($V_{1,sw}$) and the SEE for the amplifier is modeled by an input referred random voltage source ($V_{1,amp}$). The derivation for the input referred random noise source [23], using the double exponential current source model, is similar

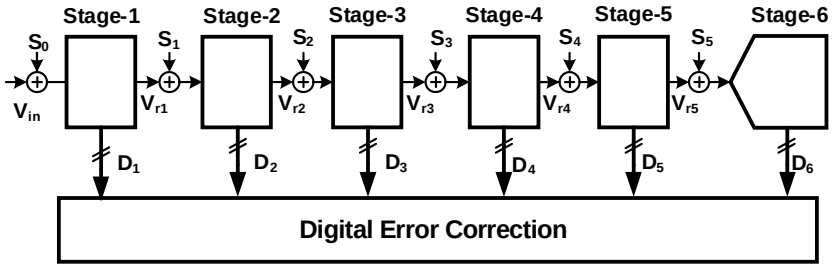


Figure 2.15: Pipeline ADC Model

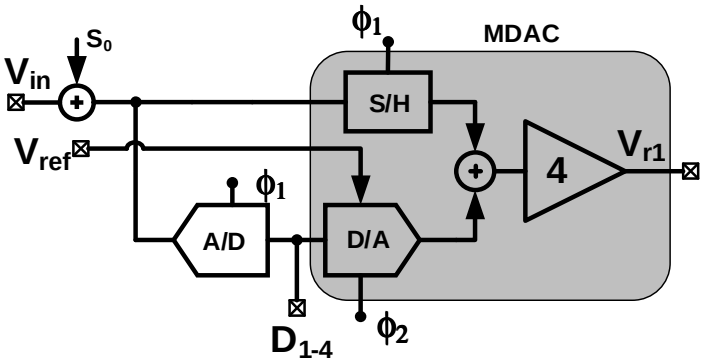


Figure 2.16: Pipeline ADC - Stage 1

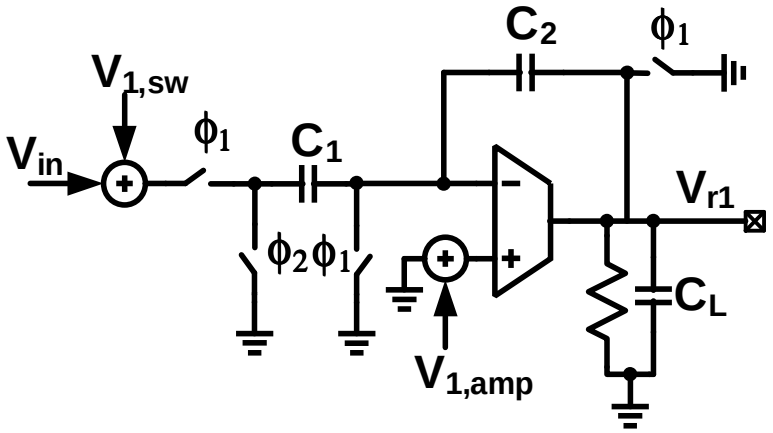


Figure 2.17: Switched Capacitor Amplifier

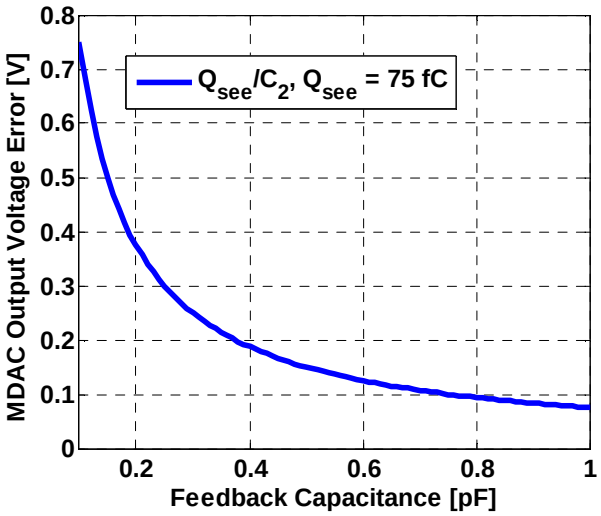


Figure 2.18: MDAC Output Voltage Change due to SEE

to conventional noise analysis. Appendix. B discuss the derivation and limitations of the macro model used. Appendix. B discusses about SEE noise model for an amplifier. Charge conservation at the inverting input terminal of the amplifier is used to derive the output voltage (V_{out}). Eq. 2.15 shows the output voltage of the amplifier with single event error source. Eq. 2.15 is then re-written in terms of charge transferred in Eq. 2.16. From Eq. 2.16, we can observe that the single event effect on the output voltage depends on the feedback capacitance and the net charge transferred by the particles energy. Fig. 2.18 shows the RMS output voltage of an amplifier for a single event effect in one of the sampling switches.

$$\mathrm{V_{out}[n]} = \frac{\mathrm{C_1}}{\mathrm{C_2}}\mathrm{V_{in}[n]} + \mathrm{V_{1,amp}}.\left(1+\frac{\mathrm{C_1}}{\mathrm{C_2}}\right) + \mathrm{V_{1,sw}}.\frac{\mathrm{C_1}}{\mathrm{C_2}} \tag{2.15}$$

$$\mathrm{V_{out}[n]} = \frac{\mathrm{C_1}}{\mathrm{C_2}}\mathrm{V_{in}[n]} + \frac{\mathrm{Q_{see,amp}}}{\mathrm{C_{in,amp}}}\left(1+\frac{\mathrm{C_1}}{\mathrm{C_2}}\right) + \frac{\mathrm{Q_{see,sw}}}{\mathrm{C_2}} \tag{2.16}$$

The above model for the amplifier is used in the MDAC for every stage in the pipeline ADC shown in Fig. 2.18. The voltage magnitude of the single event error source for each stage depends on the random charge transferred and the capacitance of the corresponding pipeline stage Eq. 2.10-Eq. 2.15. Eq. 2.17 shows the error voltage source derived from a

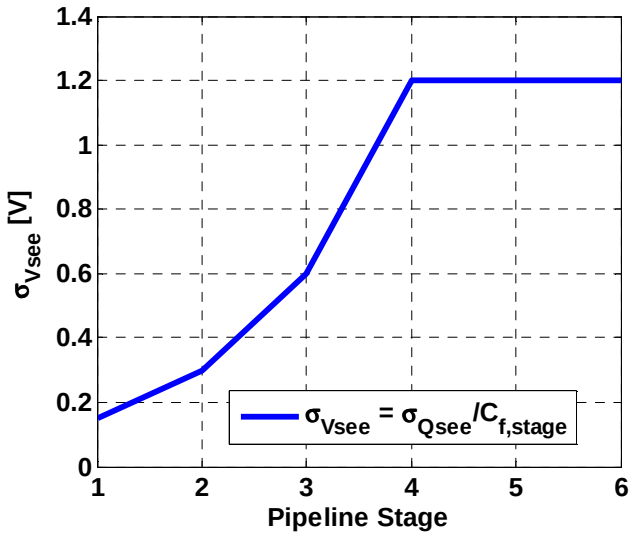


Figure 2.19: Standard Deviation of SEE

single event particles energy source for the different stages of the pipeline ADC ($S_0 - S_5$).

$$\sigma_{\text{see,input}} = \frac{\sigma_{\text{q,see}}}{\text{C}_{\text{f,stage}}.\text{G}_{\text{eff,input}}} \tag{2.17}$$

Where, C_f,stage is the feedback capacitance for each stage (C_{f1-5}) and G_{eff}, input is the input referred gain. It is instructive to note that the capacitor scaling factor of 2 along with the inter-stage gain of 4 reduces the SEE error voltage introduced in the later stages. Fig. 2.19 shows the magnitude of the SEE error voltage source, ($S_0 - S_5$), derived from a Gaussian SEE error voltage source given by Eq. 2.17. Eq. 2.11 can be re-written using Eq. 2.18 to obtain the signal to noise ratio due to the SEE error voltage source. With this error voltage source, Eq. 2.19 can be used to study the degradation in signal to noise ratio due to the SEE error voltage source.

$$\text{E}(\text{V}_{\text{see}}^2) = \sigma_{\text{see,input}}^2 . \frac{\text{N}_{\text{rep}}}{\text{N}_{\text{window}}} \tag{2.18}$$

$$\text{SNR} = \text{V}_{\text{rms}}^2 / \text{E}(\text{V}_{\text{see}}^2) = \frac{{\text{V}_{\text{rms}}}^2 . \text{N}_{\text{window}}}{{\sigma^2}_{\text{see,input}} . \text{N}_{\text{rep}}} \tag{2.19}$$

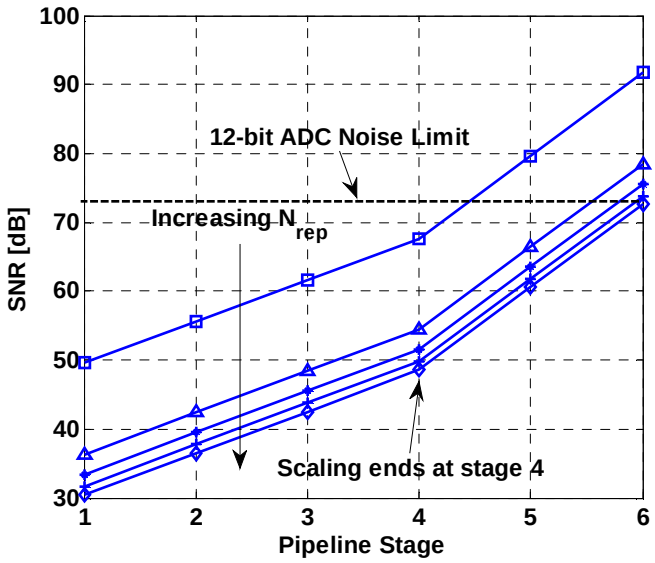


Figure 2.20: SNR for repetition rates 1, 20, 40, 60 and 100 in ADC

The position of the SEE error voltage source in the pipeline ADC, $S_0 - S_5$, and its repetition rate (N_{rep}) was varied to study the effects on the signal to noise ratio. Each sample point in Fig. 2.20 shows average signal to noise ratio of 100 runs. The simulation results were obtained by using the macro-model of Fig. 2.15 in MATLAB and the results obtained closely match the values derived using Eq. 2.19. The simulation results also confirms that the SEE in the later stages of the pipeline ADC has less impact on the SNR as compared to the SEE in the earlier stages. This can be readily observed from Eq. 2.17, Fig. 2.19 and Fig. 2.20. The input referred SEE error voltage, $\sigma_{see,input}$, is reduced by the inter-stage gain, G_{eff}, input, of the pipeline ADC. The SEE repetition rate was also varied to study the effect on SNR with a fixed observation window. Fig. 2.20 shows that even for small repetition rates of the SEE error SNR can significantly lower from the ideal value. This significant reduction in SNR, due to SEE in the signal path, is the motivation for the detection and correction schemes presented in the following sections.

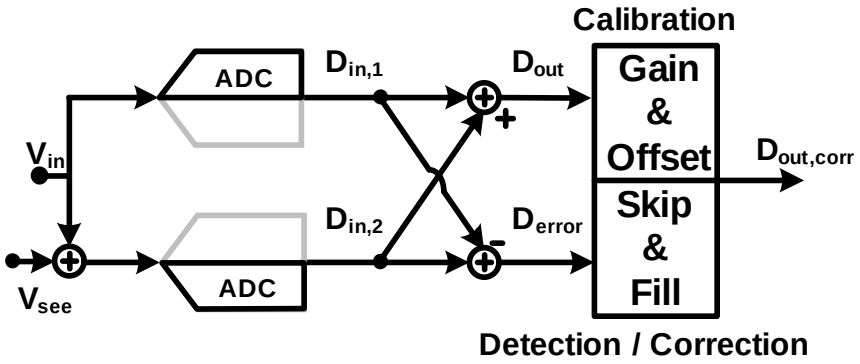


Figure 2.21: Split-ADC with Skip and Fill Correction

2.6 Two-Path ADC with Skip and Fill Correction

By introducing two identical paths using the split-ADC technique, the SEE can be detected by monitoring the digital output, D_{error}, against a digital threshold. Fig. 2.21 shows the implementation of a two-path ADC with skip and fill algorithm, [9] and [10]. D_{error} is used to detect the SEE error and the skip and fill algorithm is used for replacing the corrupt sample. The skip and fill algorithm is a non-linear interpolation algorithm which is superior to the linear interpolation methods in terms of the number of taps required for a given accuracy requirement.

2.6.1 Detection and correction using skip and fill algorithm

The skip and fill algorithm uses a non-linear interpolation method to fill the missing or corrupted sample. The details of the algorithm can be found in [24]. The SEE detection scheme consists of a simple bit by bit logical comparison of D_{error}, against a digital threshold. The skip and fill block receives two digital outputs, D_{error} and D_{out}, from the split-ADC and generates the corrected output, $D_{out,corr}$. If the magnitude of D_{error} is larger than the set digital threshold, the output (D_{out}) is replaced with the interpolated value using (10b). Otherwise, D_{out} is passed on to the output with latency as given by (10a). The interpolation and the SEE error correction is performed only if the SEE error is detected, leading to power efficient use of correction hardware.

$$D_{out,corr}(m) = D_{out}(m) \quad \text{if } D_{error} < 2LSB \tag{2.20}$$

$$= D_{inter}(m) \quad \text{if } D_{error} > 2LSB \tag{2.21}$$

2.6.2 Simulation Results

A 12-bit pipelined ADC macro-model shown in Fig. 2.15 was used in the two-path ADC technique. For the skip and fill correction method, a 40-tap interpolation filter was used with a 4096 sample length observation window. The standard deviation of the SEE error source was 0.4 V. The two-path ADC was calibrated for gain and offset error before simulating SEE errors. The output, D_{error}, used for the SEE error detection, the uncorrected (D_{out}) and corrected output ($D_{out,corr}$) are shown in Fig. 2.22, Fig. 2.23 and Fig. 2.24 respectively. Eq. 2.21 was used to identify and correct SEE errors using the skip and fill interpolation. In order to study the limitations of the interpolation based skip and fill correction scheme, the repetition rate of the SEE error source and the input signal frequency were varied. The resulting signal to noise ratio of the corrected output for the different SEE error repetition rates and the input signal frequency is shown in Fig. 2.25. The accuracy of the interpolated sample decreases with the increase in the input signal frequency. Even for a small SEE error repetition rate, the skip and fill interpolation based SEE error correction bandwidth is limited to 30% of the Nyquist frequency range. Another theoretical limitation occurs when the repetition rate of SEE error is more than 10% percent of the window of observation. In this case, SNR degradation occurs due to uncorrected SEE errors being used for interpolation. These drawbacks can be eliminated by implementing the three-path ADC correction method.

2.7 Three Path ADC Correction Algorithm

SEE is a localized event and the probability of the SEE error equally affecting more than one path in a three-path ADC in the same sample is negligible. The three path ADC technique splits the ADC into three equal smaller parts to perform SEE error detection and correction as shown in Fig. 2.26 and Fig. 2.27. The gain and offset error correction is performed as given by [9]. The SEE error correction is discussed below.

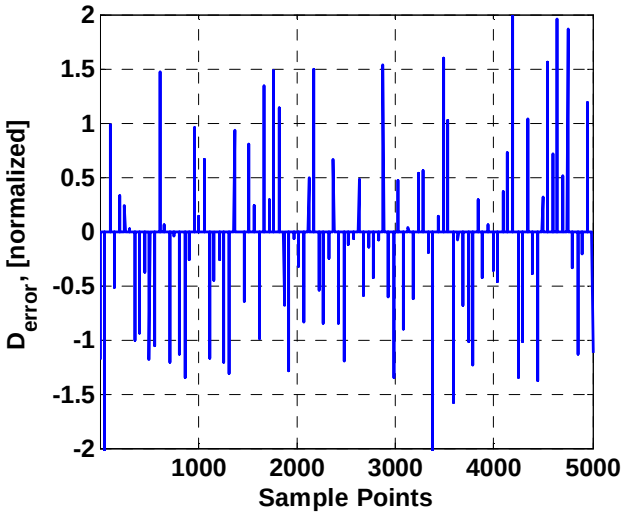


Figure 2.22: D_{error} vs. Sample Points, $N_{rep} = 100$, $N_{window} = 4096$

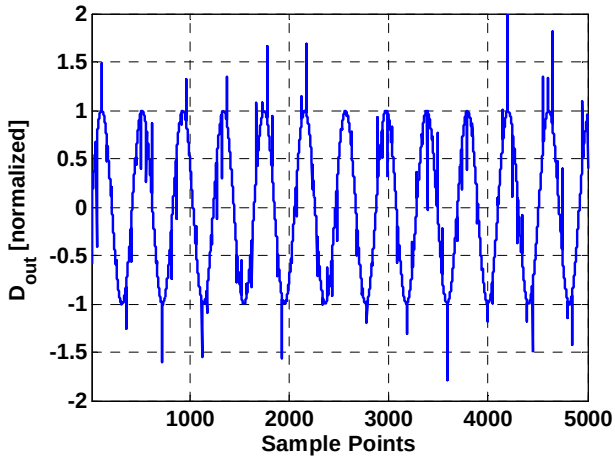


Figure 2.23: D_{out} vs. Sample Points, $N_{rep} = 100$, $N_{window} = 4096$

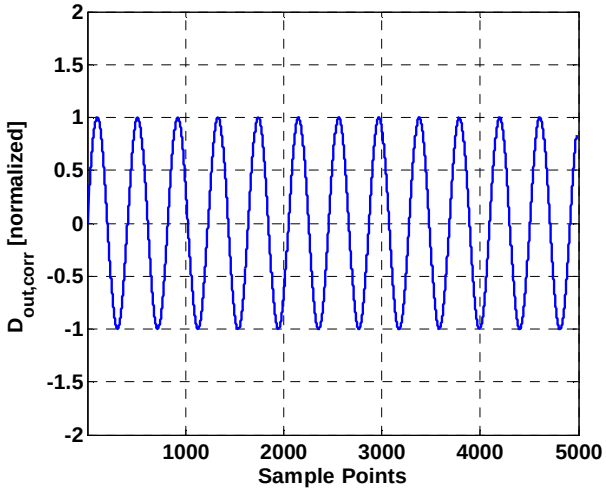


Figure 2.24: $D_{out,corr}$ vs. Sample Points, $N_{rep} = 100$, $N_{window} = 4096$

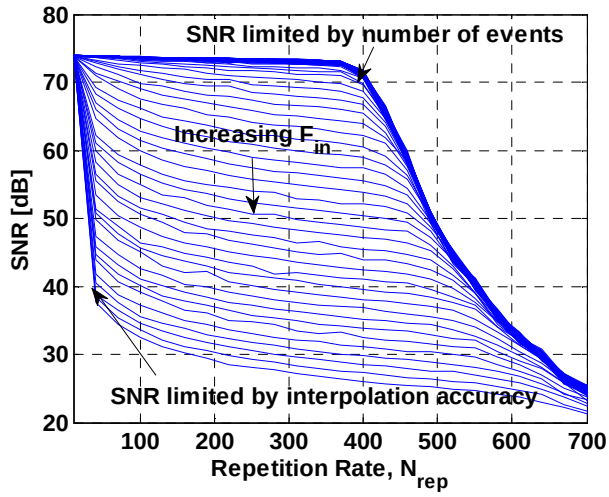


Figure 2.25: Limitations of two-path ADC correction method

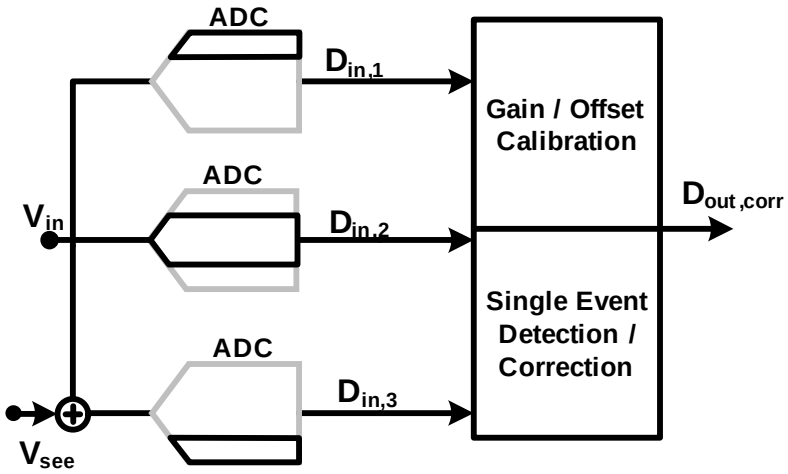


Figure 2.26: Three-path ADC

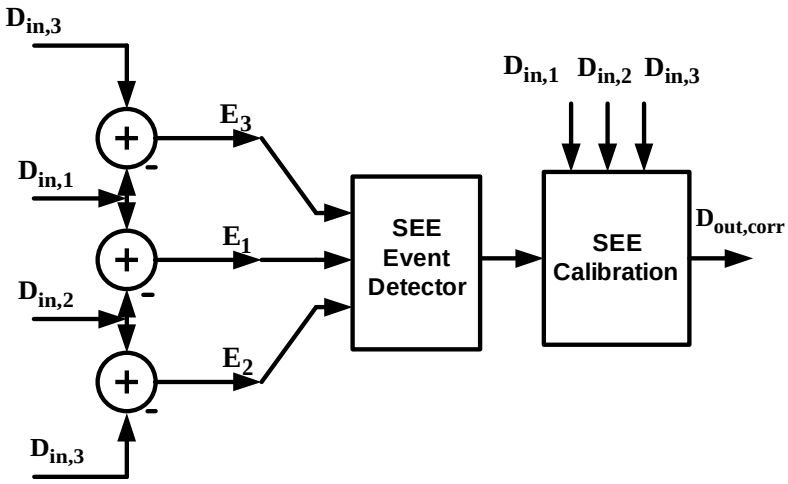


Figure 2.27: SEE Detection and Correction

2.7.1 Correction by Majority Voting

Fig. 2.27 shows implementation of the three-path SEE error detection and correction scheme. SEE error is a localized event and it affects only one of the three paths in the three-path ADC. Therefore, the SEE error detection involves a simple comparison of each of the error terms against a digital threshold which can be programmed for different environments. The minority term among the three error terms provides the two un-corrupted channels. SEE Correction involves dropping the corrupt channel output and averaging the output from the remaining two un-corrupted channels. This correction method can be implemented using simple digital logic and is explained below.

$$D_{out,corr}=\frac{1}{2}\left(D_{in,3}+D_{in,1}\right);E_1,E_2>\ 3LSB,E_3<\ 3LSB \tag{2.22}$$

$$D_{out,corr}=\frac{1}{2}\left(D_{in,1}+D_{in,2}\right);E_2,E_3>\ 3LSB,E_1<\ 3LSB \tag{2.23}$$

$$D_{out,corr}=\frac{1}{2}\left(D_{in,2}+D_{in,3}\right);E_3,E_1>\ 3LSB,E_2<\ 3LSB \tag{2.24}$$

$$D_{out,corr}=\frac{1}{3}\left(D_{in,1}+D_{in,2}+D_{in,3}\right);E_1,E_2,E_3<\ 3LSB \tag{2.25}$$

2.7.2 Simulation Results

For this example, the standard deviation of the SEE error source was 0.4 V and the observation window length was 4096. The SEE error detection threshold for single event effect was arbitrarily set to 2 LSBs. Fig. 2.28 shows the outputs of individual channels. During the first 1500 samples, first channel, D_1, is corrupted. D_2 is corrupted for the next 1500 samples and D_3 is corrupted for the remaining samples in the simulation. Fig. 2.29 shows the error terms generated using Eq. 2.21. The error terms in Fig. 2.29 contains information about the corrupt channel. In particular, the minority term of E2 for the first 1500 samples identifies that the two uncorrupted channels are D_2 and D_3. This can be observed from Fig. 2.29. The corrected output, $D_{out,corr}$, will be the average of D_2 and D_3 as given by Eq. 2.21. The corrected output is obtained from Eq. 2.21 by dropping the corrupted channel is D_1, shown in Fig. 2.30. Similarly, minority terms of E_3 and E_1 show that the corrupted channels are D_2 and D_3 respectively.

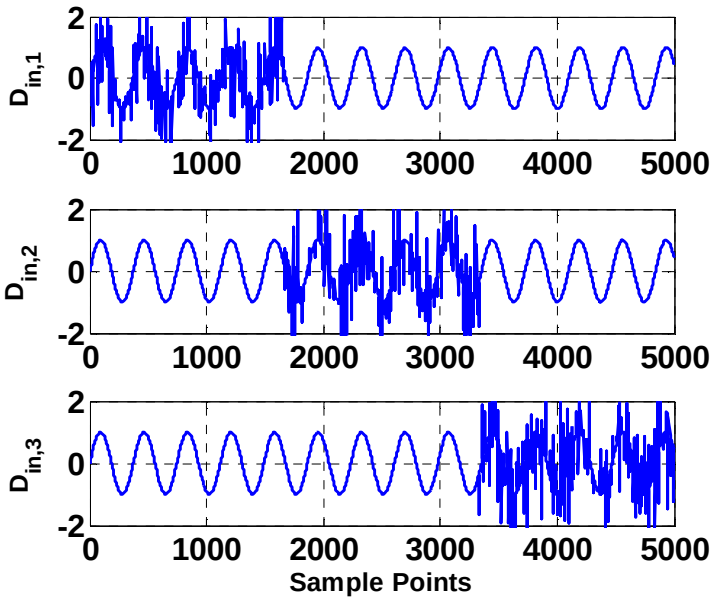


Figure 2.28: Normalized Individual channel outputs

2.7.3 Advantages of Majority Voting based Correction

The advantages of this correction scheme are as follows: effective correction for the entire Nyquist bandwidth, simple digital correction, programmable SEE detection threshold and real-time correction without any latency. Fig. 2.31 shows the corrected output accuracy for different repetition rates. For each repetition rate, N, SNR was obtained by averaging 100 simulation runs.

The artificially high repetition rate was used to point out differences between two-path and three-path ADC correction schemes. Needless to say, input frequency or the repetition rate has no effect on the thee-path ADC correction scheme. The efficacy of this correction scheme can be seen from Fig. 2.31. By dropping one of the corrupt channels, the signal to noise ratio drops by 0.28 bit from its ideal value. This is due to the fact that the noise power from the two channels is $6P_{Nsingle}$, whereas the signal power is $4P_{sig}$. Where, $P_{Nsingle}$ and P_{sig} is the noise and signal power of the single channel ADC respectively. This causes the signal to noise ratio of the corrected output to drop by a factor of 1.7 dB or 0.28 bit from its ideal value. The performance degradation is

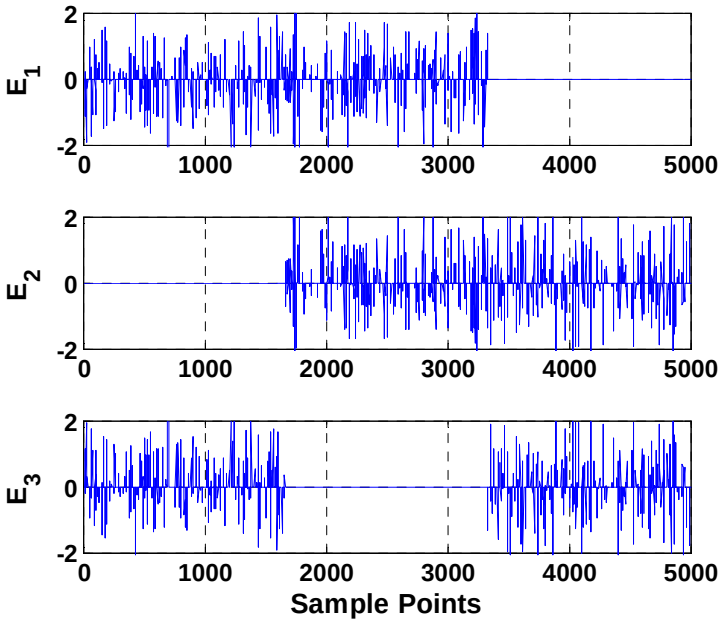


Figure 2.29: Normalized Error outputs

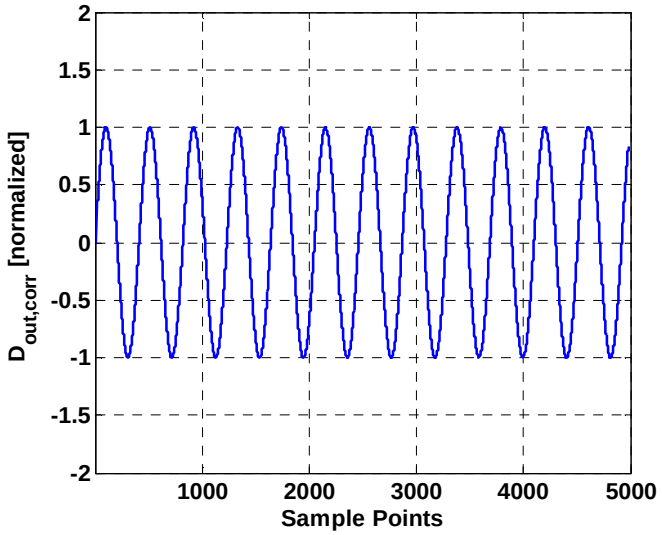


Figure 2.30: Three-Path ADC Corrected Output

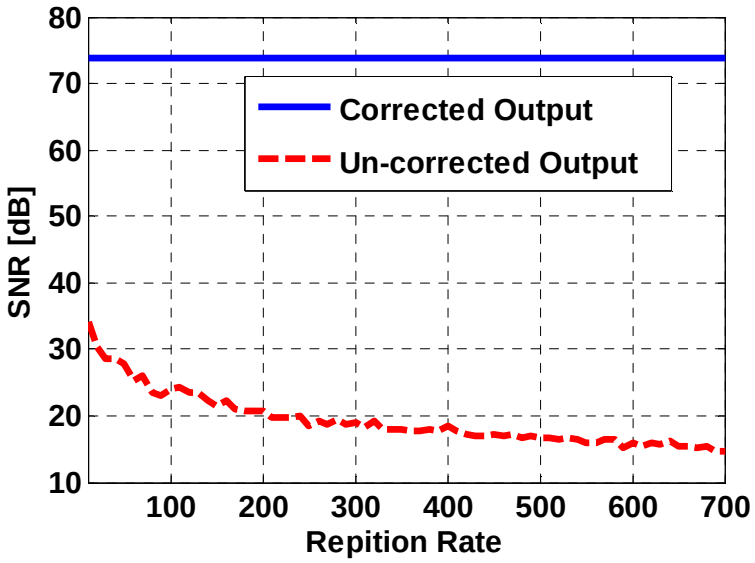


Figure 2.31: SNR vs. Frequency and Nrep = 10 to 700

independent of number of single event errors as compared to two-path ADC correction scheme. The limitation to this correction scheme is that the single event effect cannot happen in more than one channel simultaneously.

2.7.4 Comparison of Single, Two-path and Three-path ADC

Table. 2.3 compares the different aspects of the single, two-path and three-path ADC. Thanks to the multi-path ADC technique, the signal to noise ratio is the same for single, two and three path ADC. The core analog area consisting of resistors, capacitors, transconductors remain the same due to the multi-path ADC technique. The signal and power routing area will marginally increase as compared to the single-path ADC. This routing area increase is marginal as compared to triplicating the initial single path ADC. SEE correction blocks and any digital logic in the single path ADC is the overhead in the multi-path ADC implementation. The fractional interpolation filter used for the two-path ADC and the majority (minority) voting correction block of the three-path ADC is the additional digital hardware required for SEE correction in the multi-path ADC. The

Parameter	Single-Path	Two-Path	Three-Path
SNR w/o SEE	12 b	12 b	12 b
Analog Area	same	same	same
Digital	-	Skip/Fill Logic	Majority Voting Logic
SEE Correction	-	Skip/Fill	Majority Voting
Corr. BW	-	$f_s/4$	$f_s/2$
SNR w/ SEE Corr	$\leq$6 b	12 b	11.72 b

Table 2.3: Summary of Single, Two-Path and Three-Path ADC

two-path ADC along with the SEE correction block restores the performance of the ADC from less than 6 bit without SEE correction to 12 bit for half of the Nyquist bandwidth ($f_s/4$). The three-path ADC with majority voting correction scheme restores the performance for the entire Nyquist bandwidth ($f_s/2$). It is instructive to understand that the correction accuracy and bandwidth offered by three-path ADC cannot be matched by interpolation based correction schemes. The correction accuracy deteriorates rapidly for input frequency above $f_s/4$ and is not favorable for Nyquist rate ADCs.

2.8 Three-Path ADC and Bit-Error Rate Improvement

The comparators in the ADC introduce meta-stable events which manifests as bit-error-rate (BER) [25]. The conventional method to reduce meta-stability induced BER in an ADC is to increase the regeneration time of the comparator or introduce gain-stages before the regenerating latch to increase the input signal range to the regenerative latch [19]. A few architectural changes allow increased regeneration time for the comparator [25], [26], [27]. Redundancy improves meta-stability induced bit-error rate in various pipeline ADC architectures [28] as compared to successive approximation ADC [25] or cyclic/algorithmic ADC. The two-path and three-path ADC technique provides the same improvement as triple modular redundancy without area penalty. The bit-error rate, proportional to $e^{-T_{reg}/\tau}$, is squared and is equal to $e^{-2T_{reg}/\tau}$. In a three-path ADC, the majority voting based correction detects the channel with the bit-error and discards the output from the corrupted channel.

Architecture, n-bit ADC	Bit Error Power
SAR, synchronous [21]	$V_{dd}V_{ref}e^{-T_{reg}/\tau}\left(2^{-2}-2^{-n-2}\right)$
Algorithmic, 1-b/stg, G = 2	$2V_{dd}V_{ref}e^{-T_{reg}/\tau}\left(1-2^{-2n}\right)/3$
Pipeline! [26]	$\frac{GV_{dd}V_{ref}e^{-T_{reg}/\tau}\left(1-G^{-2[n/(m-1)]}\right)}{2(G^2-1)}$
Two-path and three-path pipeline ADC	$\frac{GV_{dd}V_{ref}e^{-2T_{reg}/\tau}\left(1-G^{-2[n/(m-1)]}\right)}{2(G^2-1)}$
Pipeline, look-ahead, [28]	$\frac{GV_{dd}V_{ref}e^{-T_s/2\tau}\left(1-G^{-2[n/(m-1)]}\right)}{2(G^2-1)}$
Two-path and three-path pipeline ADC, look ahead	$\frac{GV_{dd}V_{ref}e^{-T_s/\tau}\left(1-G^{-2[n/(m-1)]}\right)}{2(G^2-1)}$
Pipeline, look-ahead and time-interleaved, [29]	$\frac{GV_{dd}V_{ref}e^{-T_s/\tau}\left(1-G^{-2[n/(m-1)]}\right)}{2(G^2-1)}$

Table 2.4: Bit-Error Rate in ADCs

Chapter 3. Circuit Techniques for Analog to Digital Converters

3.1 Introduction

In the previous chapter, we discussed about calibration methods for non-idealities due to mismatch and process variation. However, these techniques does not necessarily provide the optimal performance. A traditional circuit design solution can be small, simple and more effective in optimizing power, area and performance. In this chapter, circuit techniques for minimizing capacitor switching energy in a successive approximation register (SAR) ADC and a generic amplifier technique to improve loop gain and bandwidth without sacrificing performance are discussed in detail.

3.2 Successive Approximation Register ADC

The SAR ADC implements a binary search algorithm to quantize the voltage/charge quantity into digital bits as shown in Fig. 3.1. The charge sharing technique in MOS technology was introduced by [30] and [31]. As indicated above, this architecture implements a binary search algorithm using a comparator, reference DAC and the stored input signal. By using one comparator sequentially to perform this dichotomous operation, SAR ADC optimizes power and area at the expense of conversion speed [4], [5]. The quick look at Fig. 3.1 with a realistic analog mind can easily identify that the binary or non-binary weighted DAC, charging and discharging of the DAC with reference voltage, input referred noise of the comparator, non-linearity of the input signal path, dynamic offset of the comparator and the high speed timing required as some of the limitations of SAR ADC which inhibit this architecture from achieving high resolution, speed and low power.

3.3 Nonlinear Evolution of SAR ADC Research

In the past, the matching accuracy provided by the MOS technology was poor [30] and limited to 0.1%. This mismatch induced non-linearity of the binary weighted current

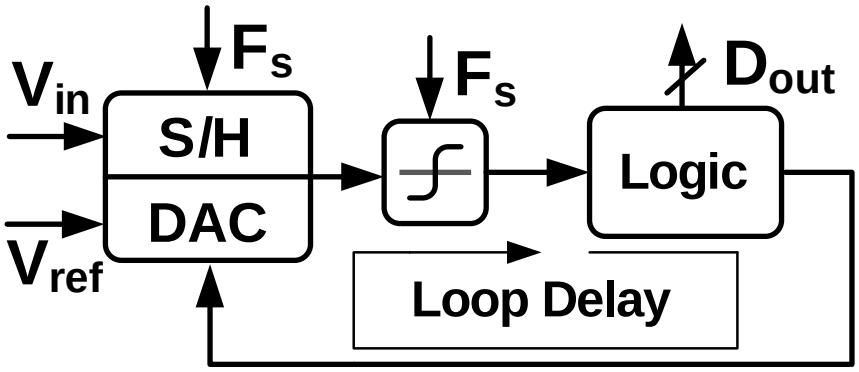


Figure 3.1: SAR ADC

DAC was solved by Plassache [32] using Dynamic Element Matching (DEM). The same problem of element matching was solved by H. S. Lee [33] using a calibration technique to measure and correct the capacitor ratio using a ROM based lookup method. Rossi [34] introduced the idea of using non-redundant capacitor array to relax the matching requirement of the capacitor array. Hammerschmied used a MOS based R-2R current splitter [35] to build a SAR ADC with highly nonlinear MOSFETs and Mortezapour utilized an active S/H and a R-2R reference ladder [36] with similar results. Even though it is attractive to use a resistor ladder to charge the parasitic capacitor to improve the DAC settling time constant and the speed of operation, the poor matching provided by the resistor ($\leq$10 bit) in combination with the static current consumption of the resistor ladder limits the SAR architectures from achieving high resolution and low power. The research topics in SAR ADC during this period were focused mainly on solving the non-linearity of resistor and capacitor matching requirement by DEM, calibration and circuit techniques.

With the evolution of sub-micron technology, the capacitor matching improved along with the popularity of capacitor DAC based SAR ADC. It is instructive to note that the reference capacitor DAC must be accurate to provide static linearity. Therefore, the capacitor area must be large enough to satisfy this requirement. Kuttner [37] used a non-binary capacitor array to relax/decouple this absolute matching accuracy and the static linearity requirement. Kuttner's use of a non-binary capacitor array, corresponding look-up table enabled SAR ADC with 10 bit accuracy and 10 MHz bandwidth. With the

focus shifting towards manipulation of the capacitor array DAC, Ginsburg [38] showed that the capacitor array consumes different energy from the reference supply based on the input. In particular, Ginsburg showed that the "UP" charging cycle is 5 times more efficient than "DOWN" charging cycle and introduced split-capacitor DAC to reduce the switching energy by splitting the MSB capacitor into a binary weighted array at the expense of switching and logic complexity. The deep sub-micron technology confirmed that the capacitor DAC based SAR ADCs with a dynamic comparator provided a ultra low power solution for medium resolution and speed.

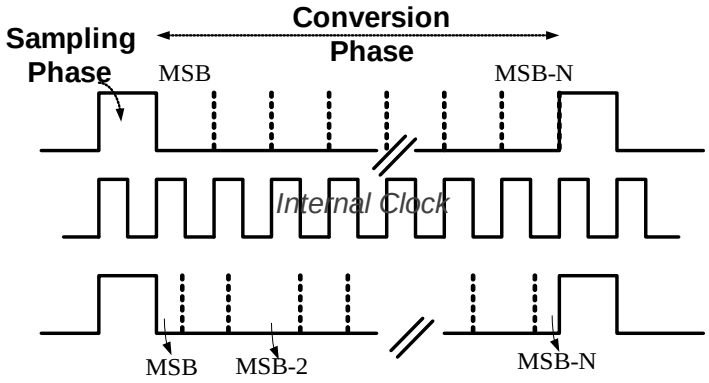


Figure 3.2: Asynchronous Timing

The SAR ADCs mentioned above utilize synchronous timing. Therefore, a high speed clock is necessary. Michael Chen [39] showed that the comparator decision can be used to asynchronously trigger the SAR ADC without the high speed internal clock. This asynchronous switching provides, on an average, twice the operating speed when compared to a synchronous SAR ADC as shown in Fig. 3.2. This leads to a suitable low power architecture. The asynchronous timing for SAR ADC, reduction of switching energy by manipulating reference DAC and the utilization of dynamic comparator lead to a series of low power and medium resolution SAR ADC between 2006-2009 [40], [41], [42], [43], [44], [45] and [46]. However, the above mentioned SAR ADCs achieved low switching energy at the expense of increased complexity to the switching logic, common mode variation of comparator and the number of comparators.

3.4 Merged Capacitor Switching based SAR ADC

A modified Merged Capacitor Switching (MCS) scheme is proposed for the Successive Approximation Register (SAR) Analog to Digital converter (ADC) which minimizes the switching energy of the capacitor array without compromising digital logic/switch complexity or the common mode variation of the comparator. The MCS scheme achieves 93.4% less switching energy as compared to the conventional architecture with 75% less capacitor when compared to a conventional SAR ADC.

3.4.1 MCS Energy Consumption

The energy consumption of a 3-bit MCS capacitor array is shown in Fig. 3.3 and Fig. 3.4. The input is sampled onto the virtual node. The first comparison does not consume any switching energy as compared to the conventional scheme. Further, UP and DOWN transitions are symmetrical and consume equal energy. In particular, UP and DOWN transitions consume energy of $0.5CV_{ref}^2$ J. This efficiency in switching energy translates to decreased power consumption, improved dynamic settling for references and in turn improves the speed of the converter.

3.4.2 DAC Switching Energy Comparison

A single-ended implementation of the proposed 10-bit ADC implementation of MCS SAR is shown in Fig. 3.5. The switching network, number of cycles and the logic complexity is the same as that of a conventional switching scheme. The average energy required for charging and discharging the SAR capacitor array determines the efficiency of the switching scheme. The average switching energy for different switching schemes was compared through a behavioral simulation of a 10-bit SAR ADC. The behavioral simulation of average switching energy for different schemes is shown in Fig. 3.6.

With respect to the conventional switching technique, split-capacitor scheme [38] achieves 37.4% energy savings, energy-saving scheme [41] achieves 58.7% switching energy reduction, set and down scheme [46] achieves 81% energy savings. However, these switching schemes achieve energy savings at the cost of increased switching complexity, common mode variation and matching requirements. The MCS scheme is 93.4% more

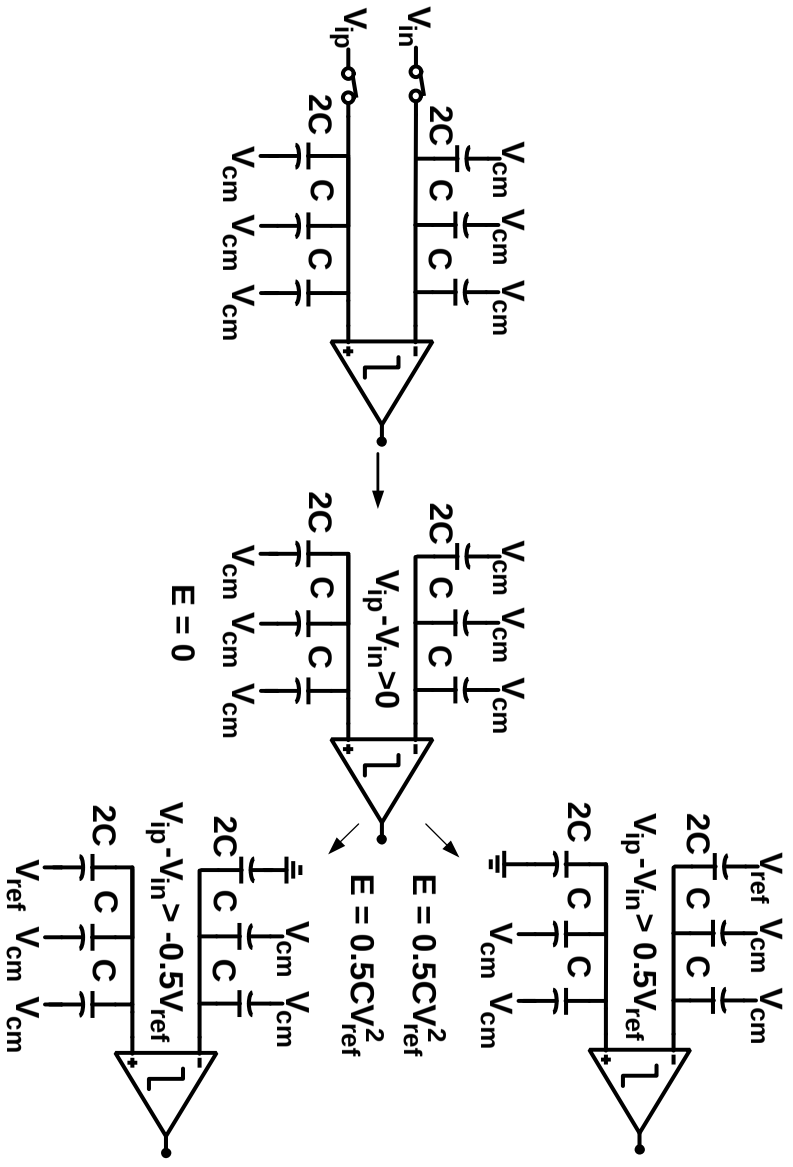


Figure 3.3: MCS Switching Energy-1

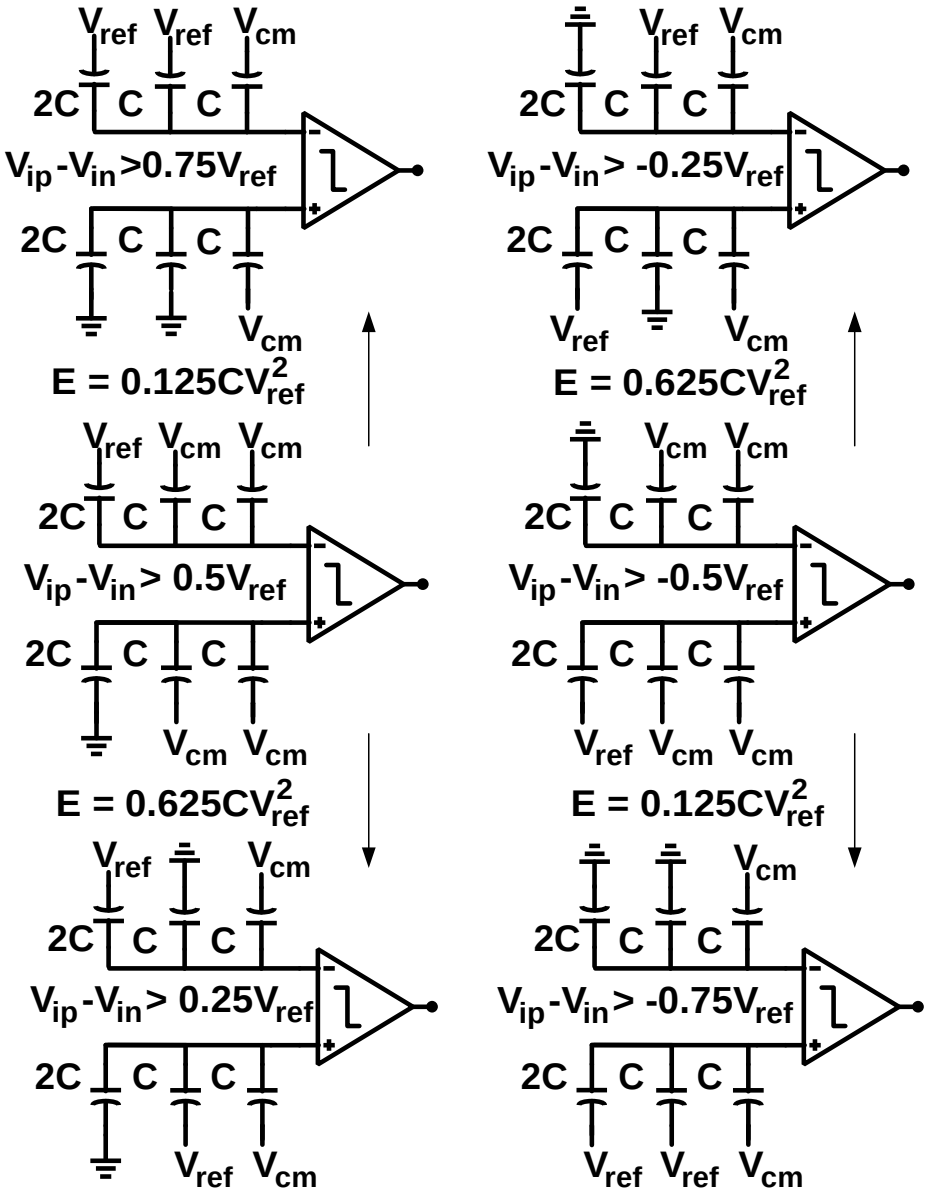


Figure 3.4: MCS Switching Energy-2

efficient than the conventional switching scheme without the above mentioned limitations. In summary, the following equations also verify the above mentioned switching energy for a uniform PDF input.

$$\textbf{Conventional} \quad E_{avg} = \sum_{i=1}^{N} 2^{N+1-2i}(2^i - 1)CV_{ref}^2 \tag{3.1}$$

$$\textbf{Energy Saving} \quad E_{avg} = 3.2^{n-3} + \sum_{i=3}^{n} 2^{n+1-2i}(2^{i-1} - 1)CV_{ref}^2 \tag{3.2}$$

$$\textbf{Set and Down} \quad E_{avg} = \sum_{i=1}^{n} 2^{n-2-i}CV_{ref}^2 \tag{3.3}$$

$$\textbf{MCS} \quad E_{avg} = \sum_{i=1}^{n-1} 2^{n-3-2i} \times (2^i - 1)CV_{ref}^2 \tag{3.4}$$

3.4.3 DAC Matching Requirements

The unit capacitor in the SAR ADC capacitor array is typically limited by the matching requirement. The variation in the unit capacitors were assumed to be Gaussian distributed. Assuming V_{ref} and GND as the reference levels for the capacitor array DAC, Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) requirement for a N bit conventional converter can be derived as follows

$$\mathbf{V_{out}}(n) = \frac{\sum_{i=1}^{n-1}(C_i + \Delta C_i)b_i}{C_{total}} V_{ref} = D_{out}.V_{ref} \tag{3.5}$$

$$\mathbf{DNL(n)} = V_{out}(n) - V_{out}(n-1),\ \mathbf{INL(n)} = V_{out}(n) - V_{ideal}(n), \tag{3.6}$$

$$\mathbf{E(DNL^2)}_{\max} = 2^n\sigma^2,\ \sigma_{\mathbf{DNL},\max} = 2^{n/2}\sigma \tag{3.7}$$

$$\mathbf{E(INL^2)}_{\max} = 2^{n-2}\sigma^2,\ \sigma_{\mathbf{INL},\max} = 0.5 \times 2^{n/2}\sigma \tag{3.8}$$

The above result for INL and DNL requirement is applied to the switching schemes to understand the improved matching accuracy offered by MCS and is tabulated in Table. 3.1.

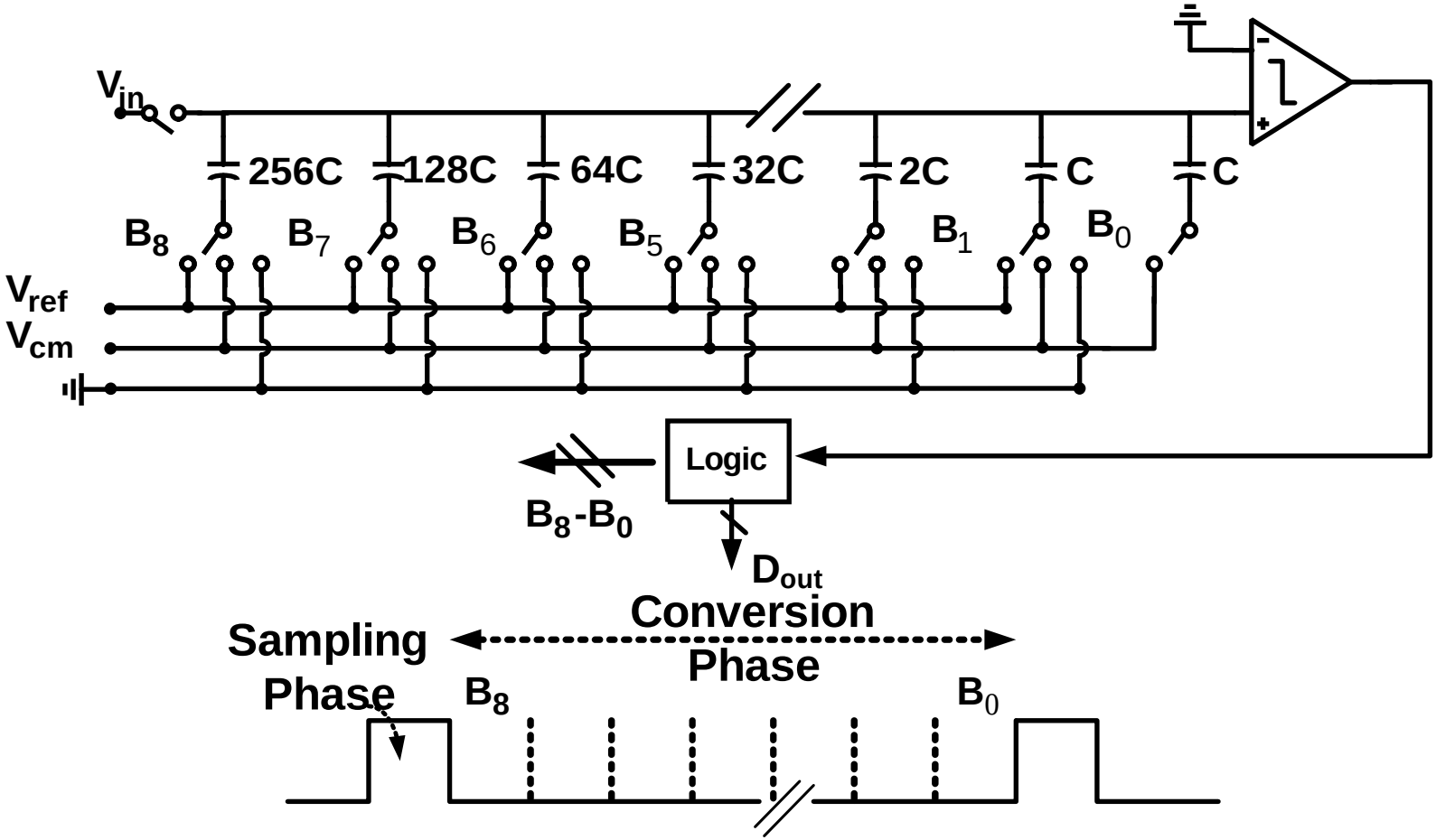


Figure 3.5: 10 bit SAR ADC

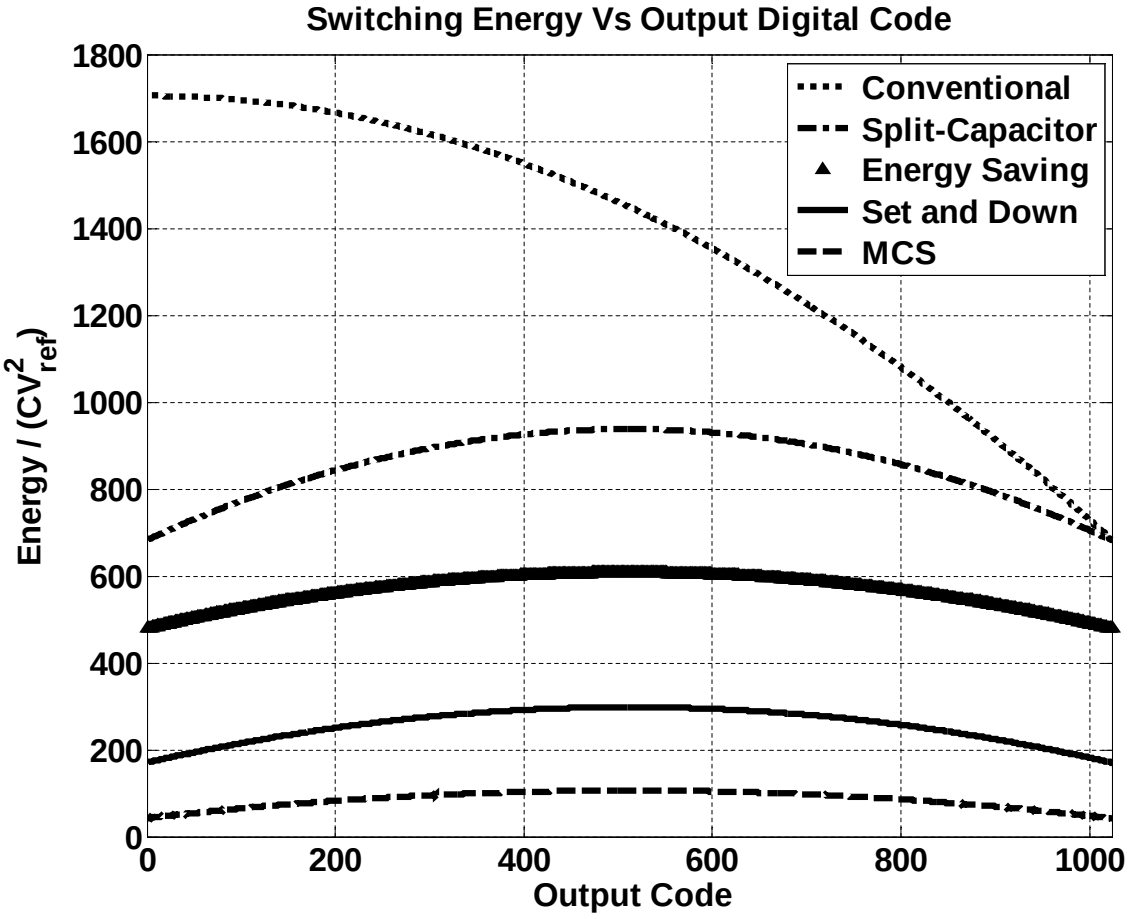


Figure 3.6: DAC Switching energy comparison

Table 3.1: INL and DNL Comparison

Switching Scheme	$\sigma_{INL,max}$	$\sigma_{DNL,max}$
Conventional	16σ	32σ
Split-Capacitor	16σ	$32\frac{\sigma}{\sqrt{2}}$
Energy-Saving	16σ	32σ
Set and Down	16σ	32σ
MCS	$16\frac{\sigma}{\sqrt{2}}$	$32\frac{\sigma}{\sqrt{2}}$

3.5 Ternary SAR

In order to implement a 1.5 bit per comparison, two comparators are required in a pipelined ADC. A 1.5 bit implementation for SAR ADC was proposed by Guerber [47], [27] utilizing a 1-bit TDC and the voltage comparator. This 1.5 bit per comparison using a 1-bit TDC and a voltage comparator improves switching energy by utilizing redundancy to skip comparison within the redundant region. A simplified version of Ternary SAR is shown in Fig. 3.7.

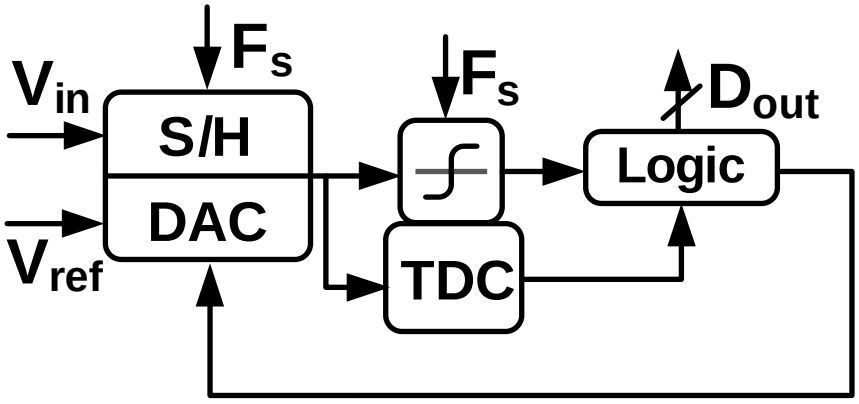
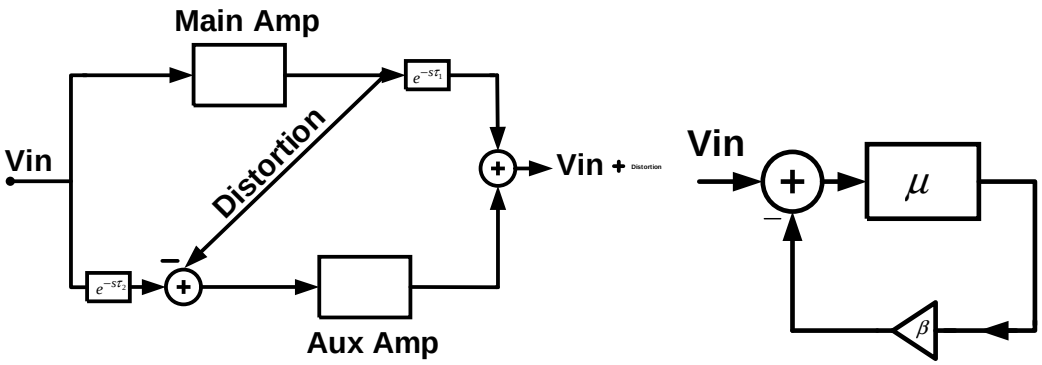


Figure 3.7: Ternary SAR ADC

3.6 Amplifiers

3.6.1 Introduction

The amplifier is the fundamental building block of analog circuit design. H. S. Black is considered to be the pioneer of negative feedback amplifier. Invented in 1927, for building repeaters for telephone communication, the negative feedback amplifiers laid the foundation for feedback and control theory [48] and [49]. Needless to say, the effect of feedback on noise, distortion, sensitivity, impedances, gain and bandwidth are all but second nature to an electrical engineer. Fig. 3.8 represented the state of art in amplifier circuit design in 1927. The lesser known feedforward amplifier and feedback amplifier are the building blocks used by electrical engineers today.



(a) Feedforward Amplifier (b) Feedback Amplifier

Figure 3.8: Feedforward and Feedback Amplifier

The advent of MOS technology and the salient efforts of Dr. Orchard, Dr. Temes, Dr. Nagaraj, Dr. Maloberti, Dr. Martin and Gregorian [22] in discrete-time processing of analog signals through switched capacitor circuits (forward Euler, backward Euler, trapezoidal transforms) paved the way for a rich set of signal processing circuits and amplifier techniques. However, for those who seek to pursue research in amplifiers, the overwhelming number of amplifier implementations and techniques can rather be confusing than providing clarity. The purpose of this section is to identify the underlying principles, ideas and techniques that can be used to understand a wide variety of amplifier techniques available without sacrificing clarity or cerebral acumen.

3.6.2 Summary of Non-Idealities and Circuit Techniques

Elementary feedback theory and circuit design textbooks introduce the concept of gain desensitivity, reduction of distortion, noise, gain-bandwidth product along with amplifier techniques to build the four basic amplifier designs which emulate voltage(current) controlled voltage(current) sources [50], [51], [52], [53], [22], [54], [55]. However, Integrated amplifiers in CMOS are tailor made to a particular application of interest. To this end, each design is unique and requires a thorough understanding of circuit and control theory. The following parameters listed in Table. 3.2 are generally considered for amplifiers in instrumentation, generic filters, data converters, MEMS, automotive, audio, video, ethernet and many other applications. Further, the parameters listed lead to several conventional trade-off such as gain bandwidth product, maximum achievable feedback, swing vs. distortion, noise, offset vs area. The high performance amplifiers which break or push the limits of the above mentioned trade off are broadly classified into continuous time amplifiers and switched capacitor amplifiers. The following tabular column summarizes the amplifier non idealities, continuous time and discrete time techniques used in filters and data converters.

Table 3.2: Amplifier Non-Idealities, Continuous time and Discrete time Techniques

Non-Idealities	Continuous time	Discrete time
Finite-Gain	Cascode	Narrow(wide)band CDS
Bandwidth	Gain Boosting	Parallel CDS
Distortion	Adaptive Biasing	Time-aligned(shifted) CDS
Noise	Multi-Stage Amplifier	Predictive CDS
Offset	Cross Coupling	CLS, Split-CLS
Slew-Rate	Class A+, AB, B, C	Cross-Coupled CLS
	Parallel/Replica Amplifiers	RPGE

3.7 Continuous Time Gain Enhancement

Table. 3.2 summarized the non-idealities and techniques utilized to improve the state of the art in high performance amplifiers. As tabulated, the high performance amplifier techniques can be broadly classified into continuous time and discrete time amplifier techniques. Fig 3.9 shows the continuous time amplifier technique. In this technique,

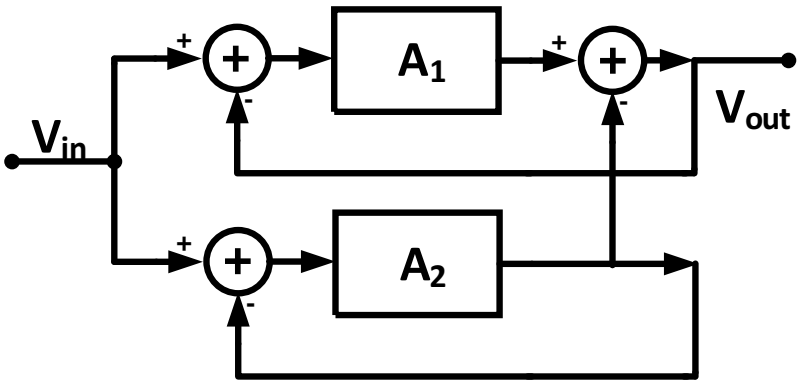


Figure 3.9: Continuous Time Gain Enhancement Model

the main amplifier is A_1 and the parallel/replica amplifier is A_2. With this setup, the resultant input to output equation is given below.

$$V_{out2} = \frac{V_{in}}{\beta}\frac{LG_2}{1+LG_2} \tag{3.9}$$

$$V_{out1} = \frac{V_{in}}{\beta}\frac{1}{1+LG_2}\frac{LG_1}{1+LG_1} \tag{3.10}$$

$$V_{out} = V_{out1} + V_{out2} \tag{3.11}$$

$$= \frac{V_{in}}{\beta}\frac{1+LG_1+LG_1LG_2}{(1+LG_1)(1+LG_2)} \tag{3.12}$$

The salient features of this arrangement is that the main amplifier swing is reduced to the gain error of the parallel amplifier. Also, the final loop gain is approximately the product of individual loop gains. Replica-amplifier, assisted opamp technique and replica class AB/B amplifiers fall into this category, and are described briefly in the following subsection.

3.7.1 Replica Amplifier and Assisted Opamp Techniques

Fig. 3.10 shows the replica amplifier with a main amplifier and a replica amplifier [56]. The replica amplifier is a scaled version of the main amplifier, occupies smaller area and consumes a smaller portion of the main amplifier power consumption. Without any

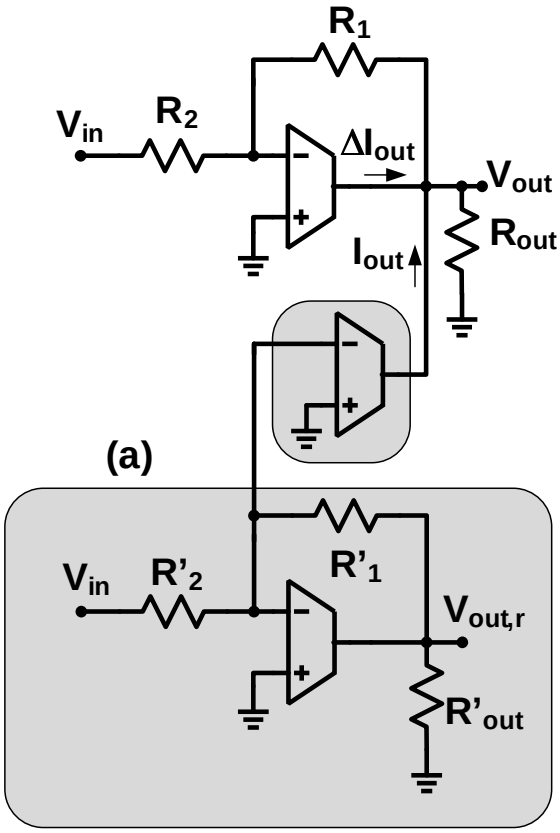


Figure 3.10: Replica Amplifier

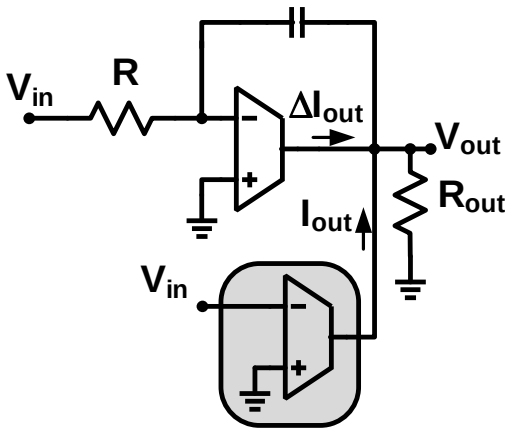


Figure 3.11: Assisted Opamp

mismatch, the coupling transconductor provides majority of the load current except for any distortion. The main amplifier suppresses the distortion current from the replica amplifier. The effective loop gain is the product of the loop gain and the gain error is approximately squared. Fig. 3.11 shows the assisted opamp technique where the transconductor at the output provides the majority of the current(V_{in}/R). The opamp suppresses any mismatch or distortion introduced by the assist transconductor [57].

3.8 Discrete Time Gain Enhancement

The discrete-time gain enhancement technique can be broadly classified into sequential and parallel gain enhancement techniques. Further, the discrete time technique can be classified into input based or output based technique. Fig. 3.12 provides a unified block diagram of discrete time gain enhancement technique. The desired output is obtained at the end of the second phase. The first phase is used to estimate the output. This estimated output is combined either at the input or at the output of the second amplifier in the second phase. It is imperative to note that the charge conservation at the virtual ground is still valid and is the primary reason for the feasibility of this technique. The output at the second phase has similar accuracy as that of the continuous time gain enhancement technique. The effective loop gain is the product of the individual loop gain at the end of second phase.

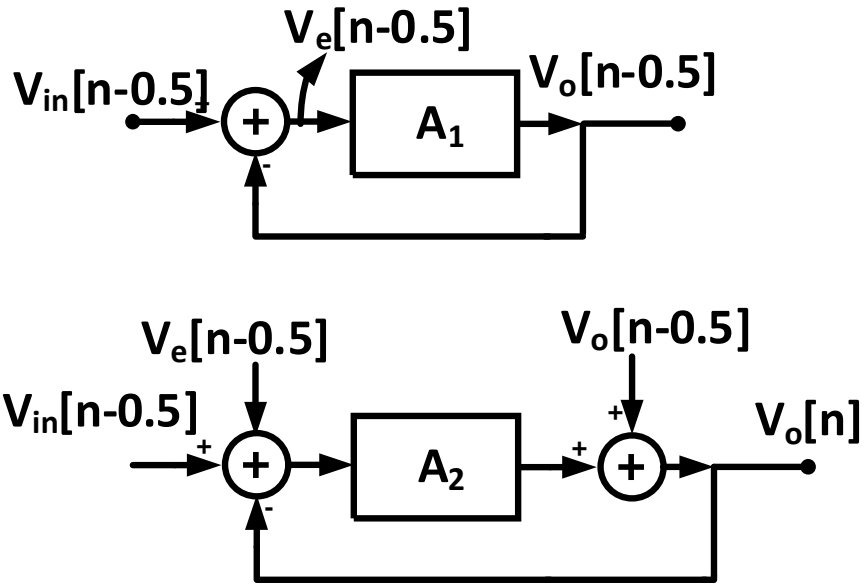


Figure 3.12: Discrete Time Gain Enhancement Model

3.8.1 CDS and CLS Technique

Correlated Double Sampling (CDS) is a input based sequential gain enhancement technique. Fig 3.13 shows the basic narrowband CDS technique. The CDS technique is one of the widely used techniques to improve gain error, offset cancellation and low frequency noise cancellation. Narrowband CDS from the 80's can be found in [58], [59] and [60]. There were several improvements to this technique through 1990's and 2000's such as wideband CDS [61], [62], [63], Predictive CDS [64], Time-shifted CDS, Time-aligned CDS [65] and Parallel CDS [66]. Some of the disadvantages of this technique are the requirement of a three phase clock scheme, frequency dependent gain error, additional capacitors and switches.

Correlated Level Shifting (CLS) is an output based sequential gain enhancement technique. Fig. 3.14 shows the CLS technique. The estimated output is available in the CLS capacitor at the end of the first phase. The level shifting phase provides gain enhancement by driving the output of the opamp to the virtual ground through the level shifting capacitor. In this technique, the level shifting is performed at the output of the opamp with similar improvement to the loop gain. The swing at the output of the

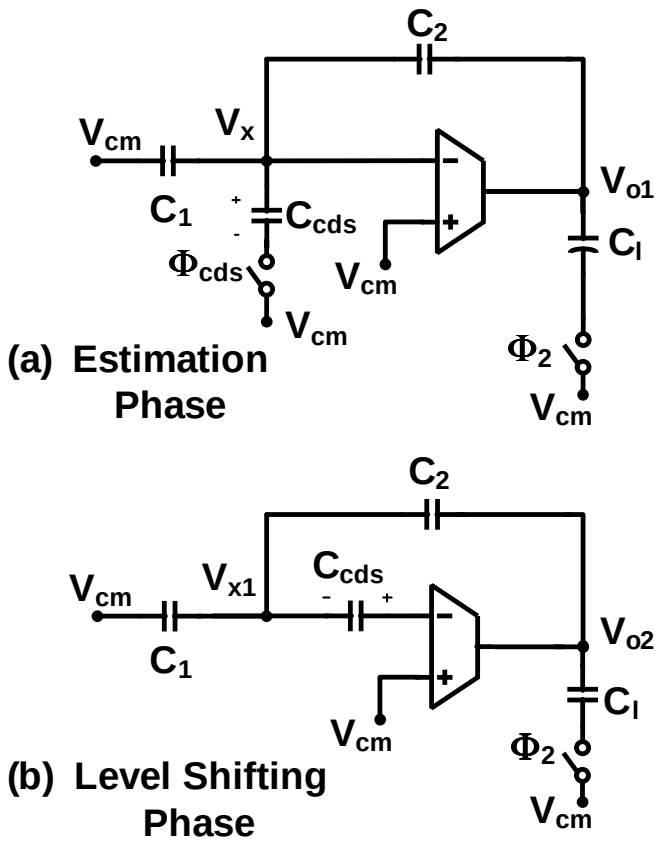


Figure 3.13: Correlated Double Sampling

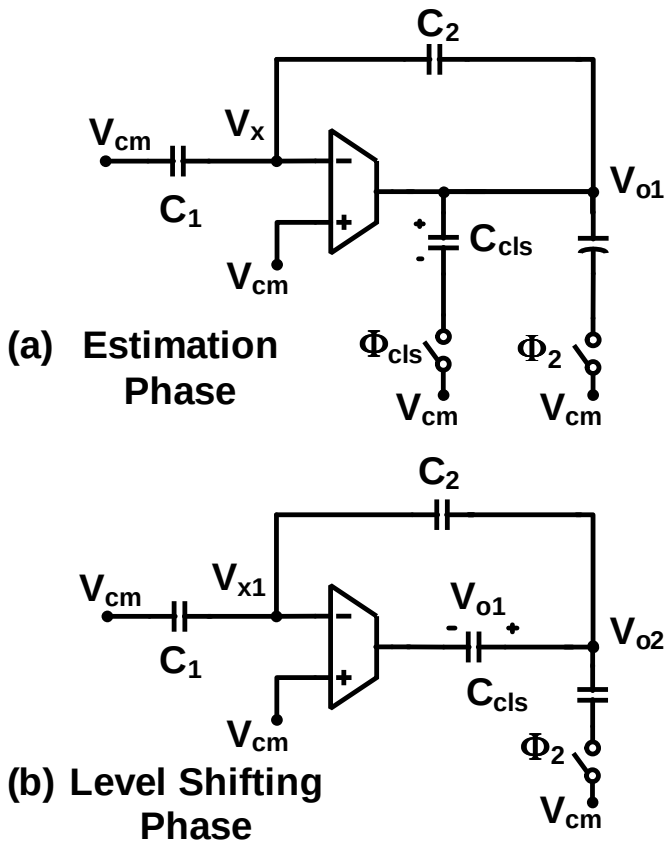


Figure 3.14: Correlated Level Shifting

amplifier is reduced by using CLS and decouples the DC gain vs. swing requirement. Some of the drawbacks of this technique are the requirement of a three phase clock scheme, frequency dependent gain error, additional capacitor load, input referred offset, low frequency noise and switches.

3.9 Asynchronous CLS, Sequential, Output based Gain Enhancement

Asynchronous Correlated Level Shifting technique (ACLS) is proposed as an asynchronous sequential output based gain enhancement technique which utilizes zero-crossing

based circuit. The Correlated level shifting (CLS) technique provides rail-to-rail operation in an opamp based circuit and approximately squares the loop-gain as shown in [67]. However, the three phase clocking scheme, high DC gain requirement in level shift phase, large load capacitor with Class-A type amplifier in estimate phase are detrimental to CLS. These side effects limits CLS from achieving high speed and accuracy while optimizing power and area. The class of zero-crossing based circuits(ZCBC) [68] use a comparator and a current source to provide slew-rate limited charging mechansim to replace the power hungry opamp. However, the ZCBC suffer from signal dependent variation of the current source and overshoot due to the comparator delays as shown in [68].

The purpose of ACLS is to combine the best features of CLS and ZCBC schemes to provide a superior solution when compared against CLS and ZCBC circuits individually. To achieve this performance, ACLS reduces the signal dependent variation of the current source by shifting the current source to a region with more headroom. The increased headroom for the current source can be optimized to provide highly linear current sources with large output impedances. This translates to a large loop-gain in ZCBC and a linear ramp source. This technique is useful in the deep sub-micron technologies, where the voltage headroom for current source is too small to build high gain and high swing opamps.

3.9.1 ACLS Operation

Fig. 3.15 and Fig. 3.16 shows the ZCBC based asynchronous CLS circuit and timing respectively. Fig. 3.17a shows the estimation phase and the level shifting phase of ACLS operation. At the end of estimation phase, the output voltage can be approximated by Eq. 3.13. Where $C_{eff1}=C_{CLS}+C_L+\frac{C_1C_2}{C_1+C_2}$, V_o is the output voltage, r_c is the output resistance of the coarse current source, . C_{eff1} is the effective load capacitance seen by the current source, t_{d1} is the time delay of the comparator at the end of estimation phase. In deep sub-micron technologies, the channel-length modulation causes variation in the current source value and its resistance. This causes non-linearity in 3.13.

Fig. 3.17b shows the level shift phase, where the fine current source is level shifted towards common-mode voltage. At the end of Level Shifting phase, the output voltage can be approximated by Eq. 3.14. Where, $\alpha=\frac{C_{CLS}+C_{eff3}}{C_{CLS}}$,$C_{eff3}=C_L+\frac{C_1C_2}{C_1+C_2}$,$C_{eff2}=\frac{C_{eff3}C_{CLS}}{C_{CLS}+C_{eff3}}$,

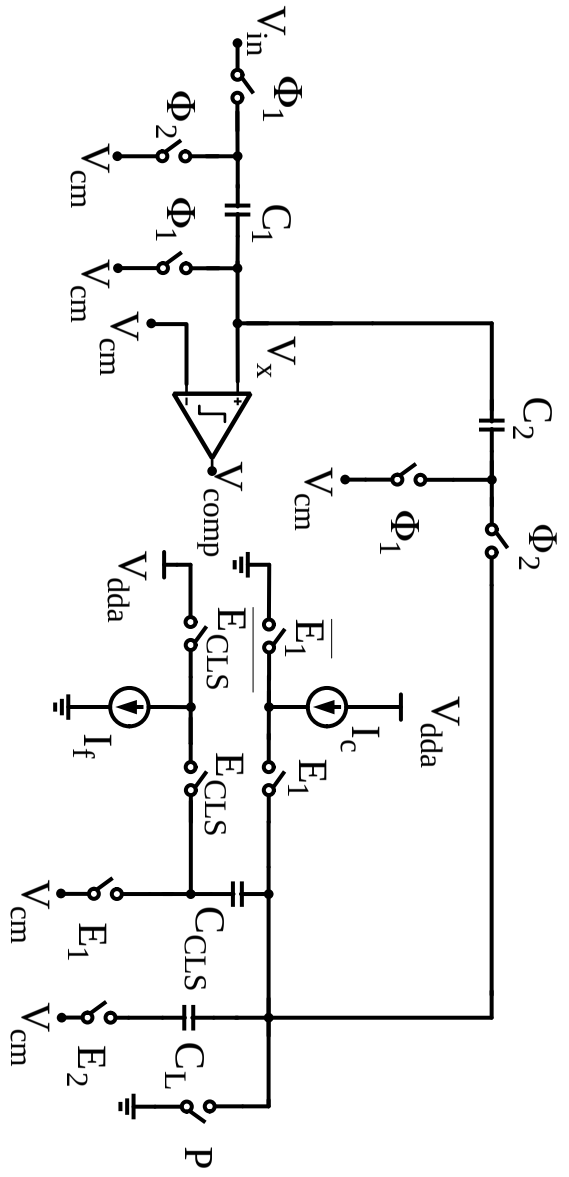


Figure 3.15: Asychronous Correlated Level Shifting Schematic

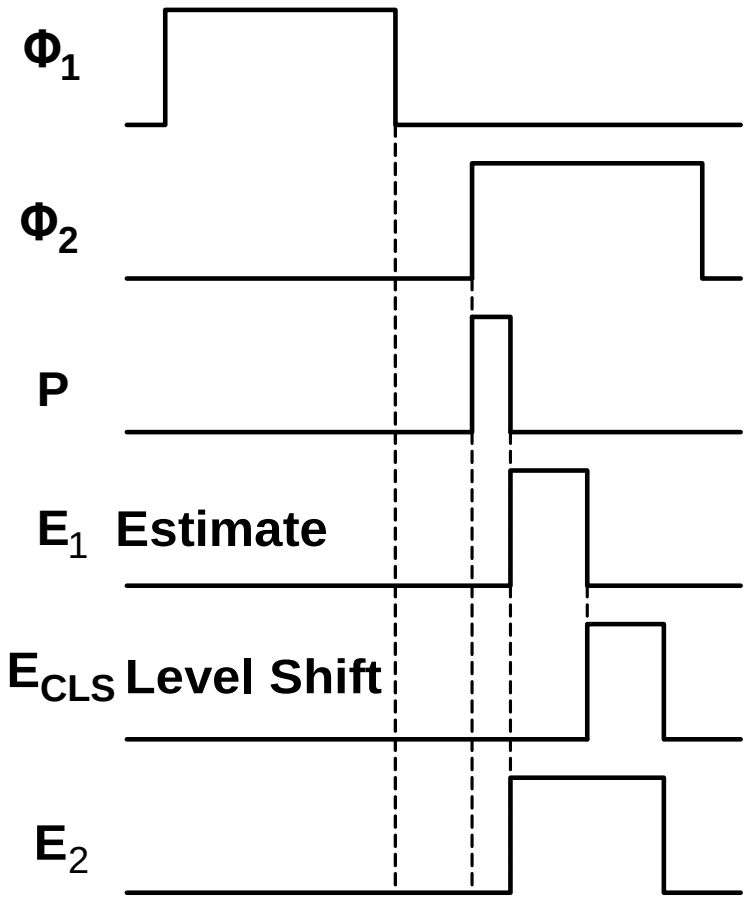


Figure 3.16: Asychronous Correlated Level Shifting Timing

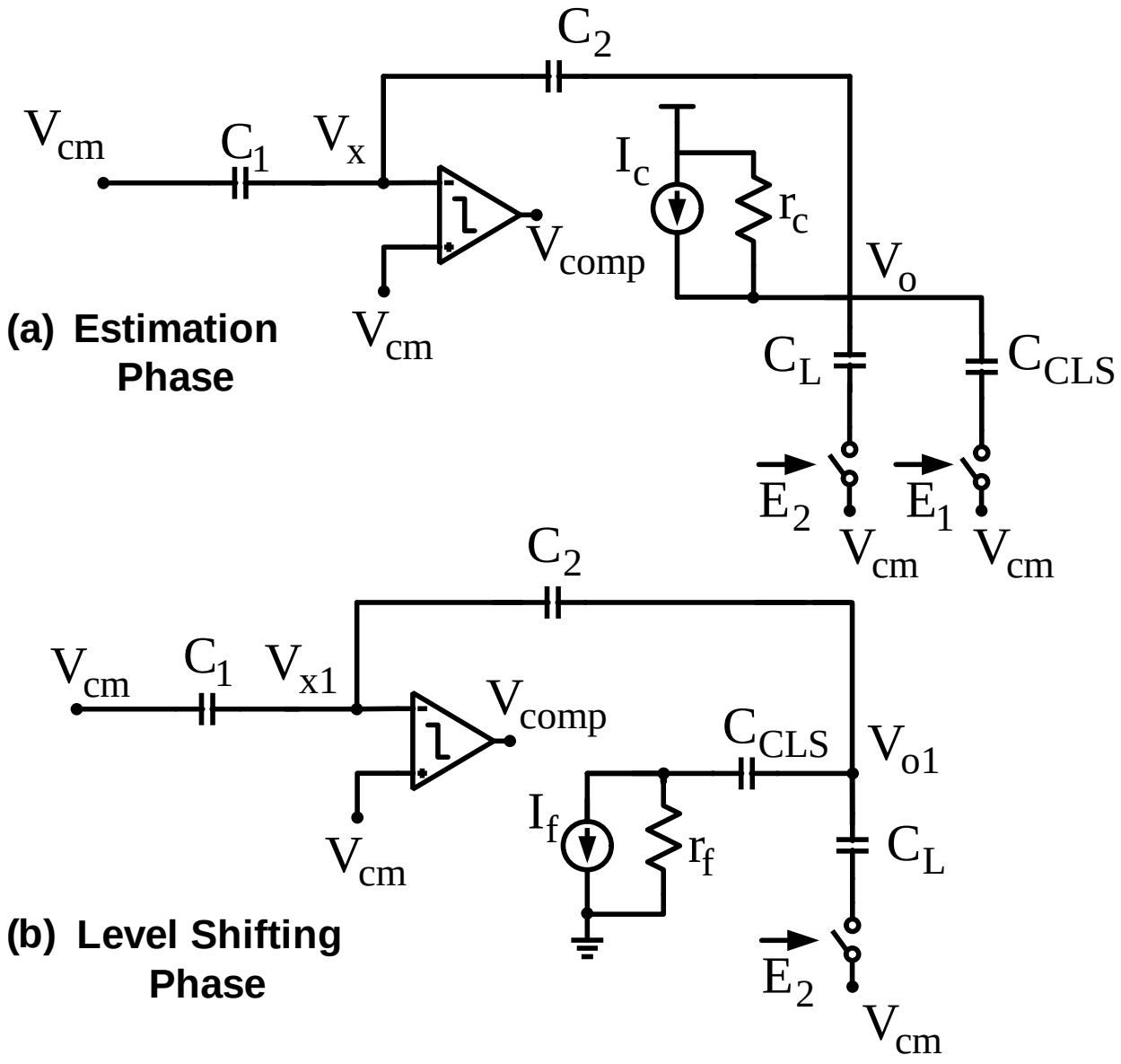


Figure 3.17: ACLS Operation

Table 3.3: Comparison of Opamp and ZCBC CLS

Phase	Opamp LG	ZCBC LG
Estimation	$A_{dc}\beta$	$\frac{r_c C_{eff1}}{t_{d1}}$
Level Shift	$(A_{dc}\beta)^2$	$\frac{r_f C_{eff1}}{t_{d2}} \frac{r_c C_{eff2}}{t_{d1}}$

t_{d2},r_f ,I_f are the corresponding terms for the level shifting phase.

$$V_o \approx \frac{V_{in}C_1}{C_2} \frac{1}{\left(1+\frac{t_{d1}}{r_c(V_o)C_{eff1}}\right)} + \frac{I_c(V_o)t_{d1}}{C_{eff1}} \tag{3.13}$$

$$\begin{aligned} V_{o1} \approx \frac{V_{in}C_1}{C_2}\left(1-\frac{t_{d2}}{r_f C_{eff2}}\frac{t_{d1}}{r_c C_{eff2}}\right) \\ -\alpha\frac{I_f t_{d2}}{C_{eff2}} + \frac{I_c t_{d1} t_{d2}}{r_f C_{eff1} C_{eff2}} \end{aligned} \tag{3.14}$$

3.9.2 Loop Gain Enhancement

According to [67], the opamp based CLS approximately squares the loop gain at the end of level shifting phase. A similar expression for ZCBC is also obtained as shown in Eq. 3.14. The fine current source begins the level-shifting phase with fixed voltage headroom. Thus, the current source can be cascoded to provide large loop gain and the linearity is improved by an order of magnitude. The overshoot caused due comparator delay is given by the second term in Eq. 3.13 and Eq. 3.14. Table. 3.3 provides a side-by-side comparison of opamp based CLS and ZCBC ACLS. Thanks to ACLS, the variation of the fine current source is reduced by an order of magnitude. Thus, the overshoot is largely signal independent. The choice of CLS capacitor is the trade-off between loop-gain enhancement, linearity obtained and speed.

3.9.3 Power Supply Rejection Ratio

The power supply rejection ratio (PSRR) is an important issue due to the mismatch between two current sources in a differential circuit implementation of ZCBC. Fig. 3.18 represents the small signal models for the conventional ZCBC and ACLS based ZCBC. The ACLS based ZCBC provides more attenuation as compared to the conventional ZCBC circuits. However, reducing the CLS capacitor will increase the swing seen by the

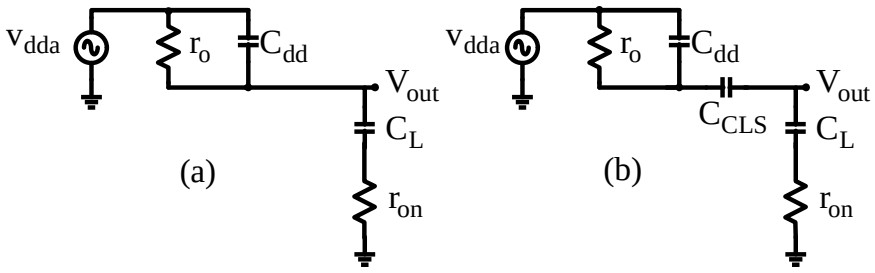


Figure 3.18: PSRR Small Signal Model

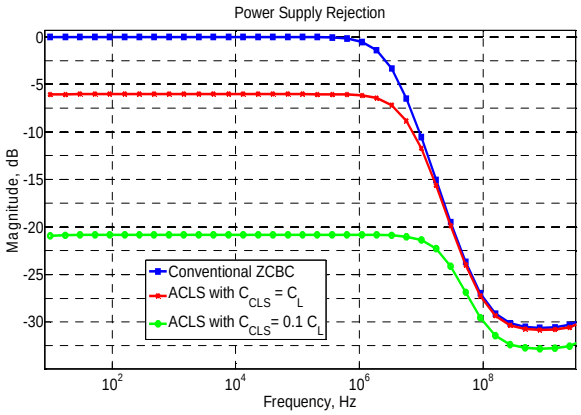


Figure 3.19: PSRR Simulation

fine current source. Fig. 3.19, shows a comparison of PSRR between conventional ZCBC and ACLS based circuits. The PSRR for the conventional ZCBC and ACLS ZCBC is given by equations (5) and (6) respectively. The ACLS ZCBC provides better PSRR and allows an independent control of the PSRR shape through CLS capacitor.

$$\frac{v_o}{v_{dda}} \approx \frac{(1+sC_Lr_{on})(1+sC_{dd}r_o)}{(1+sC_{dd}r_{on})(1+sC_Lr_o)} \tag{3.15}$$

$$\frac{\mathrm{v_o}}{\mathrm{v_{dda}}} \approx \frac{\mathrm{C_{CLS}}}{\mathrm{C_{CLS}+C_L}} \frac{(1\mathrm{sr_oC_{dd}})}{(1+\mathrm{s/p_1})(1+\mathrm{s/p_2})} \tag{3.16}$$

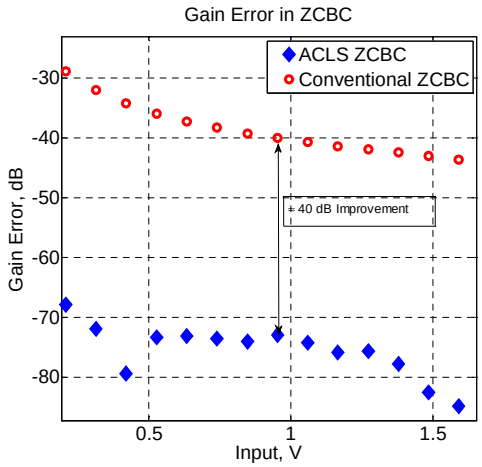


Figure 3.20: Gain Error Comparison

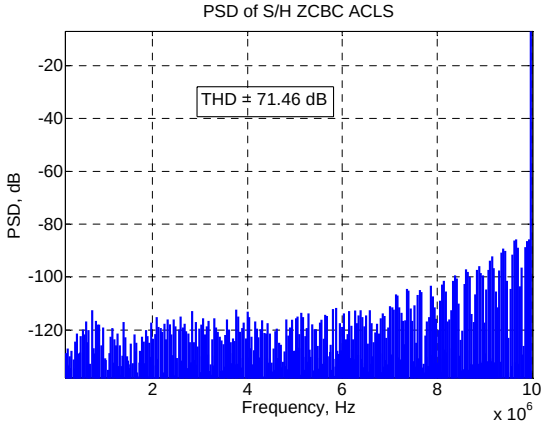


Figure 3.21: PSD of ACLS S/H

3.9.4 Simulation Results

Conventional ZCBC and ACLS circuit were simulated in a S/H configuration. The clock frequency was chosen to be 20 MHz. The comparator bandwidth was chosen to be 2-5 times larger than the clock frequency. The current source was implemented as a single MOSFET transistor. The CLS capacitor was chosen to be the same as the load capacitor. The gain error is shown in Fig. 3.20. The gain error of an S/H block shows 40 dB improvement as compared to a conventional ZCBC. THD simulation result is shown in Fig. 3.21.

3.10 Class A+ Parallel, Output, Positive Feedback based Gain Enhancement

ACLS technique described in the previous section can be described as an asynchronous sequential output based gain enhancement technique using two negative feedback circuits in the estimate and the level shift phase. Class A+ amplifier is a parallel output based gain enhancement technique which is composed of a main negative feedback loop and an auxiliary controlled positive feedback loop. This amplifier technique varies from the conventional amplifier techniques, class A, class AB, class B, shown in Fig. 3.22. The various amplifier architectures shown in Fig. 3.22 are optimized for speed, power, accuracy, signal swing, distortion and area for a given application. The inter-dependant relationship of the above parameters leads to an inefficient design of the amplifier. In this section, we demonstrate a controlled positive feedback approach for the output stage of the two-stage amplifier to relax this dependency on speed, area and power requirements suitable for switched-capacitor amplifier design.

3.10.1 Class A+ Amplifier

The two-stage Class A+ amplifier has the same first-stage as a conventional Class-A amplifier is shown in Fig. 3.23. By utilizing positive feedback, dynamic compensation is achieved for the output stage transconductance. This dynamic compensation for the amplifier relaxes area and power consumption with better settling accuracy and settling time. The reduction in the impedance of output stage and increase in the short-circuit

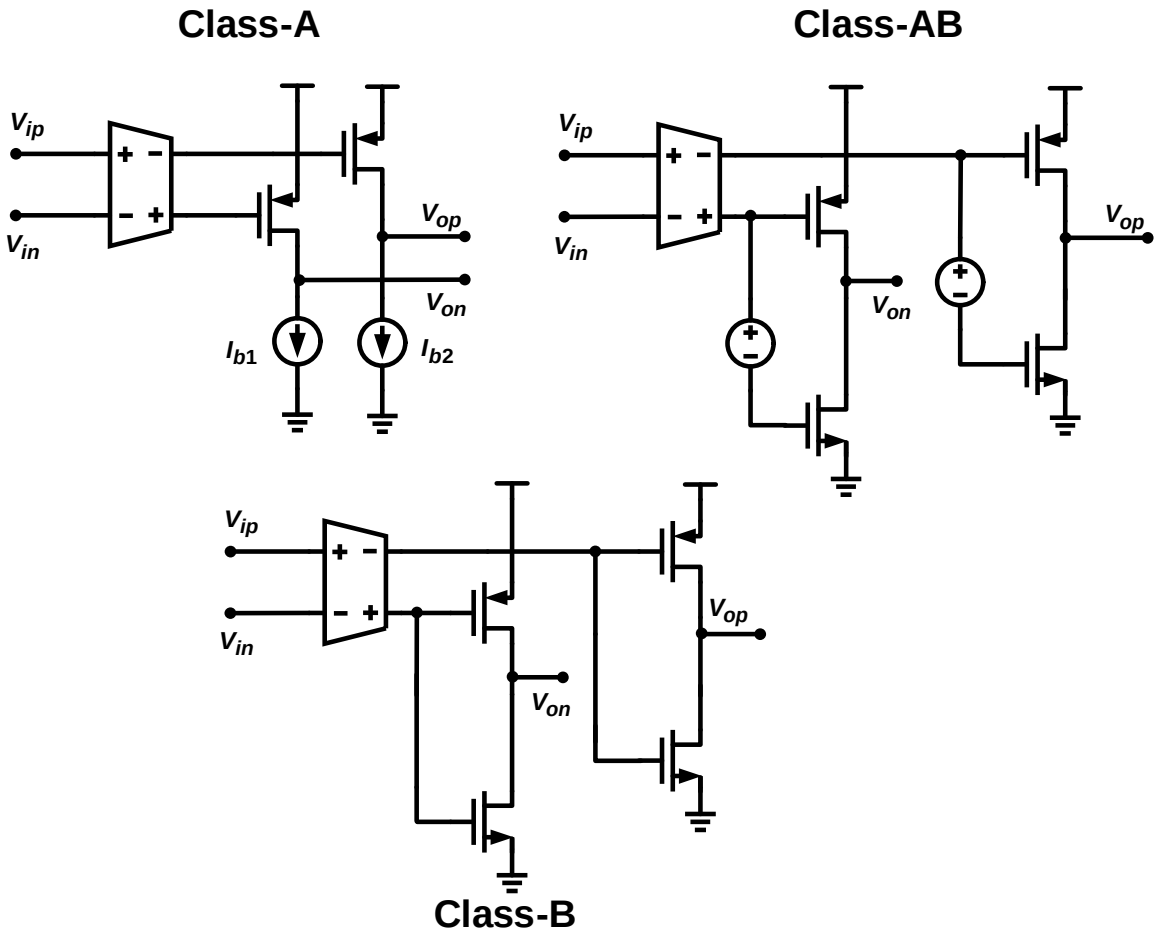


Figure 3.22: Class A, Class AB and Class B

transconductance of the output stage with the positive feedback latch is a design trade-off for a given settling accuracy [69] and [70]. It also decouples the gain bandwidth (GBW) relationship which results in an increased power consumption for the output stage.

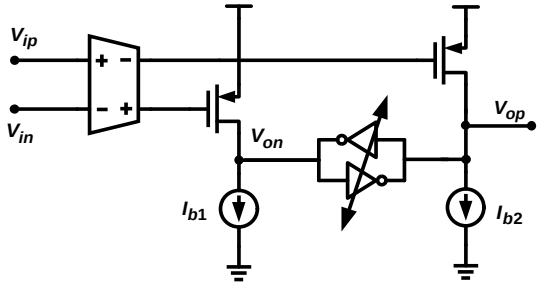


Figure 3.23: Class A+

3.10.2 Class A+ Operation

The Class-A+ amplifier operates in two-phase and is explained as follows. In reset phase, the internal nodes of the latch are reset to known bias voltages of the Class-A amplifier as shown in Fig. 3.24. In amplification phase, positive feedback is applied to the output stage as shown in Fig. 3.24. The positive feedback ratio is set by the capacitor ratio (C_1, C_2, C_3) of the cross-coupled latch. The small signal model shown in Fig. 3.25 for the conventional miller/current buffer compensation is used to show the effect of positive feedback. The positive feedback increases the output stage short-circuit transconductance and decreases output stage impedance for miller compensated (MC) and current buffer (CB) based compensated amplifiers. The open loop transfer function of Miller and Ahuja compensated two stage amplifiers are given by Eq. 3.17 and Eq. 3.18 respectively. The graphical pole-zero location for a compensated two-stage amplifier and the dynamic class A+ amplifier is shown in Fig. 3.26. The non-dominant output pole of the Class-A+ amplifier is moved to higher frequency with the help of positive feedback

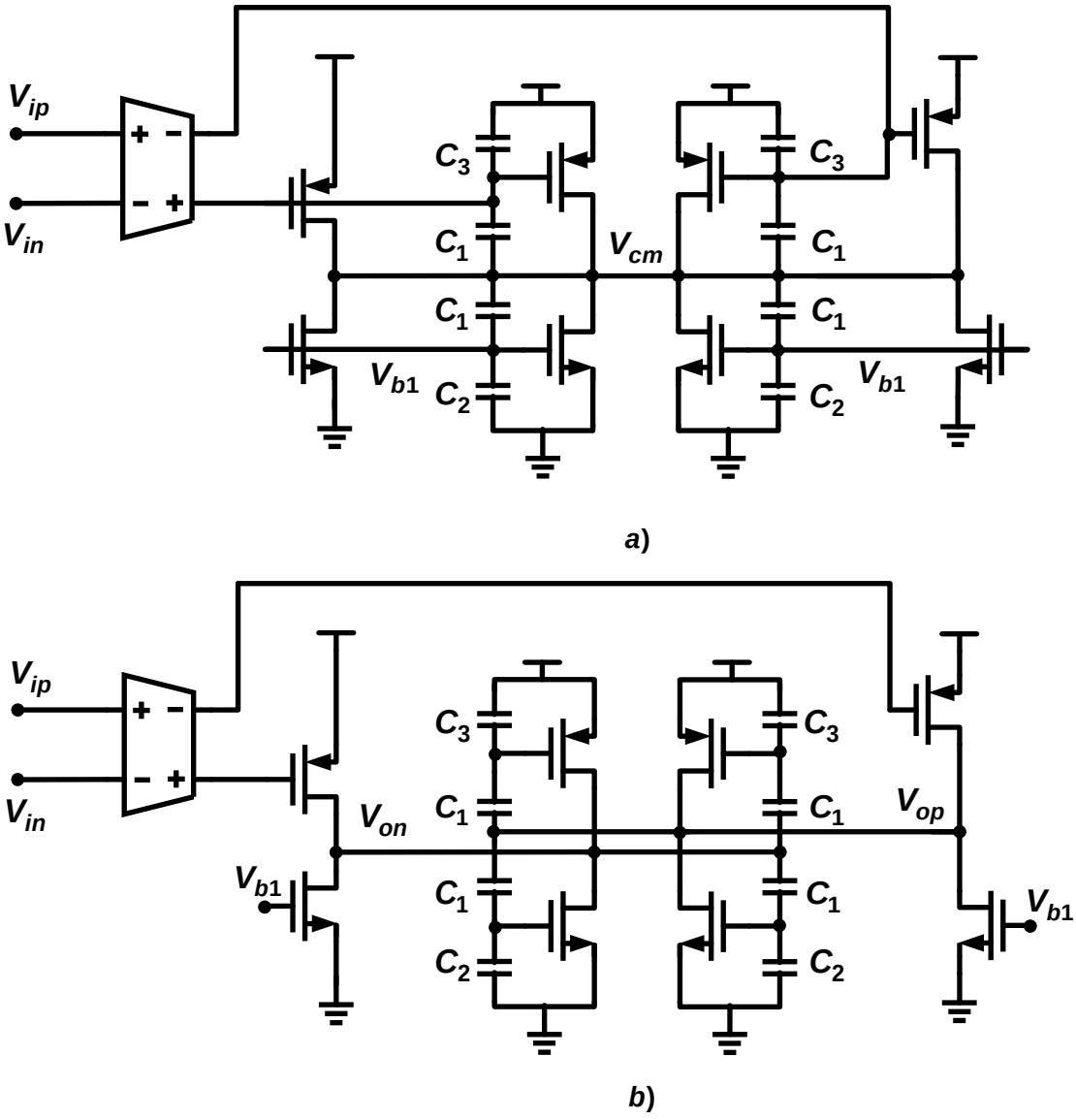


Figure 3.24: Class A+ a) Reset and b) Amplify Phase

latch.

$$\frac{V_o}{V_{in}} = -\frac{g_{m1}(g_{m2} - sC_m)}{s^2(C_1C_L + C_mC_L + C_mC_1) + s(C_Lg_{ds1} + C_1g_{ds2} + C_m(g_{ds1} + g_{ds2} + g_{m2})) + g_{ds1}g_{ds2}} \tag{3.17}$$

$$\frac{V_o}{V_{in}} = -\frac{g_{m1}g_{m2}}{s^2(C_1C_L + C_cC_1) + s(C_Lg_{ds1} + C_1g_{ds2} + C_c(g_{ds1} + g_{m2})) + g_{ds1}g_{ds2}} \tag{3.18}$$

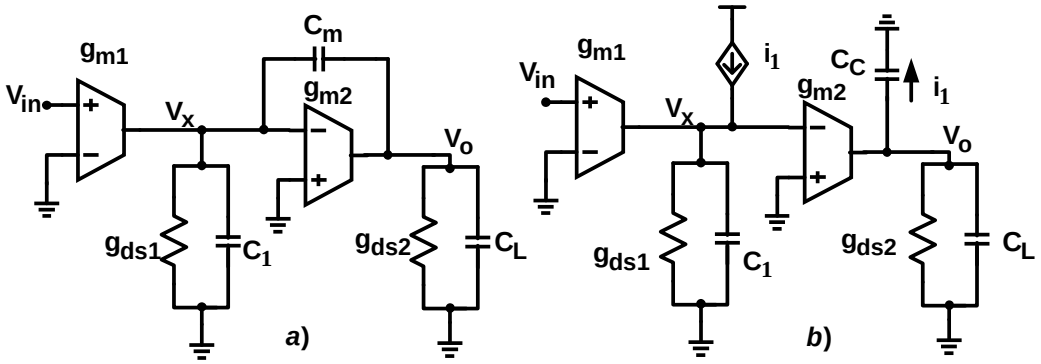


Figure 3.25: Miller and Ahuja Small Signal Models

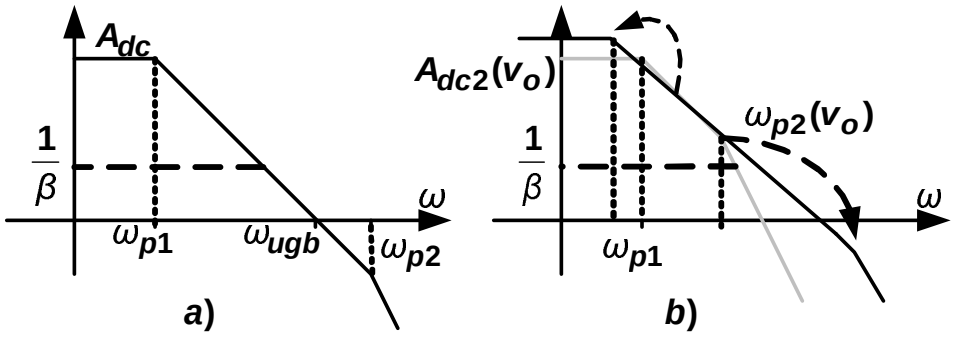


Figure 3.26: Two-Stage and Class A+ Loop Gain Plot

3.10.3 Simulation Results

In a macro-model simulation, Class-A amplifier was modeled as a two-pole system with the non-dominant pole placed at the closed-loop bandwidth frequency with DC-gain of 1000 and feedback factor of 0.5. Class A+ amplifier was modeled as a two-pole amplifier with initial non-dominant pole at half the closed-loop bandwidth frequency whereas, DC-Gain and non-dominant pole vary with output swing. The simulation shows the step response of Class-A+ amplifier change from under-damped closed loop response at the beginning of the step response to improved dynamic and steady state settling accuracy at the end of amplification phase in Fig. 3.27.

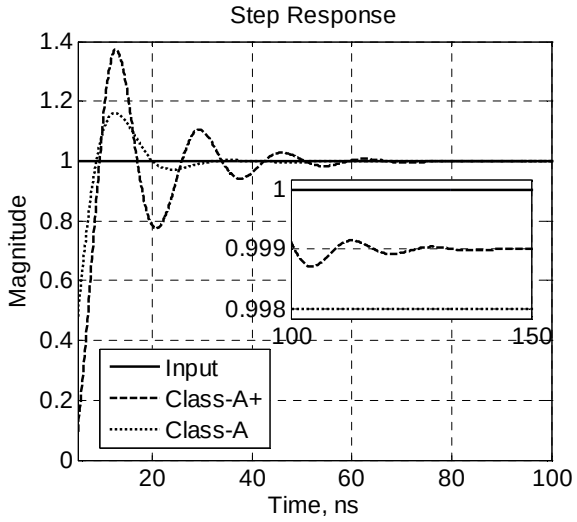


Figure 3.27: Step Response Comparison

The Class-A+ amplifier was compared against an over damped and an under-damped Class-A amplifier. The amplifiers were designed using 0.13 μm CMOS process with 1.2 V power supply. Cascode-compensation based Class-A amplifiers were used for the following comparison. Error amplifier based common-mode feedback was used for common-mode feedback. The above mentioned amplifiers were simulated in a sample and hold (S/H) configuration shown in Fig. 3.28. The S/H circuit was simulated with clock frequency of 20 MHz.

The class-A amplifier has the best stability performance among the amplifiers in

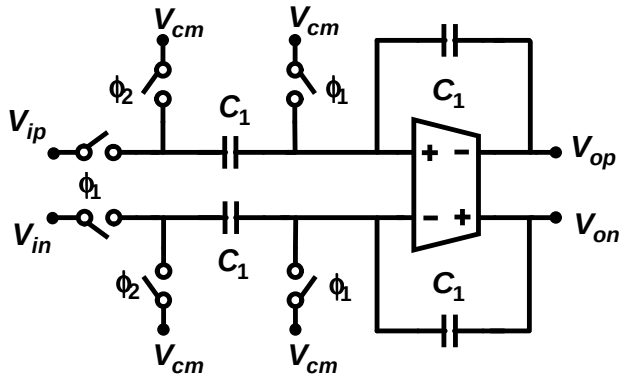


Figure 3.28: S/H Simulation Setup

comparison. The class-A under damped amplifier has 50% reduced output stage devices compared to class-A amplifier and hence degraded stability performance. The class A+ amplifier was designed with 50% reduced output stage as compared to class-A amplifier with cross-coupled latch. Step response of the amplifiers is shown in Fig. 3.29, steady-state setting error is shown in Fig. 3.30 and 0.1% settling time is shown in Fig. 10. The step-response clearly shows the dynamic nature of class A+ amplifier. In the beginning of amplification phase, the class A+ amplifier behaves closer to under-damped class-A amplifier. The positive feedback improves stability and DC-gain of the amplifier.

Settling accuracy is better than a class-A amplifier at the end of amplification phase. Better settling accuracy is achieved with 30% less quiescent current and 50% reduction in the output stage as compared to over damped class-A amplifier design. Since the positive feedback is output signal dependant, settling accuracy for a given settling time was verified across the input signal range. Fig. 3.30 shows % settling error across the entire input range. The class A+ amplifier has better than 10-dB improvement in steady state settling accuracy. Steady state settling accuracy is improved due to the increase in loop gain by positive feedback latch. Similar worst case 0.1% settling time as compared to class-A amplifier is shown in Fig. 3.31. Total Harmonic Distortion (THD) of over-damped class-A amplifier and class-A+ amplifier is shown in Fig. 3.32. The class-A+ amplifier has better than 3 dB THD as compared to a class-A amplifier across the input frequency range. The SFDR performance of class-A+ amplifier is better than 6 dB as compared to class-A amplifier.

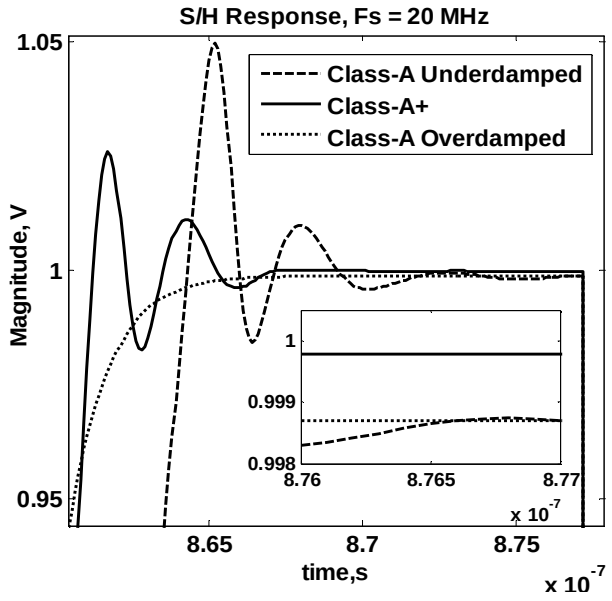


Figure 3.29: S/H Step Response

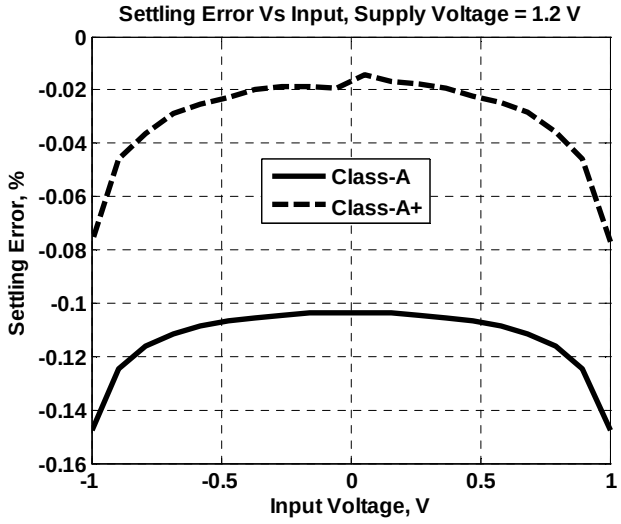


Figure 3.30: Settling Error vs. Amplitude

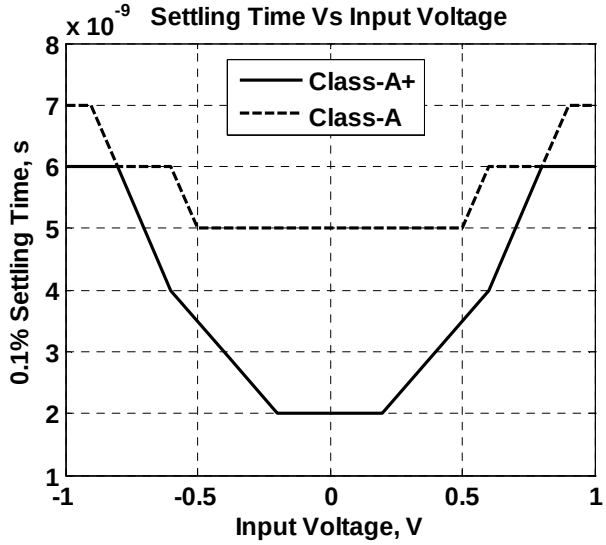


Figure 3.31: Settling Time vs. Amplitude

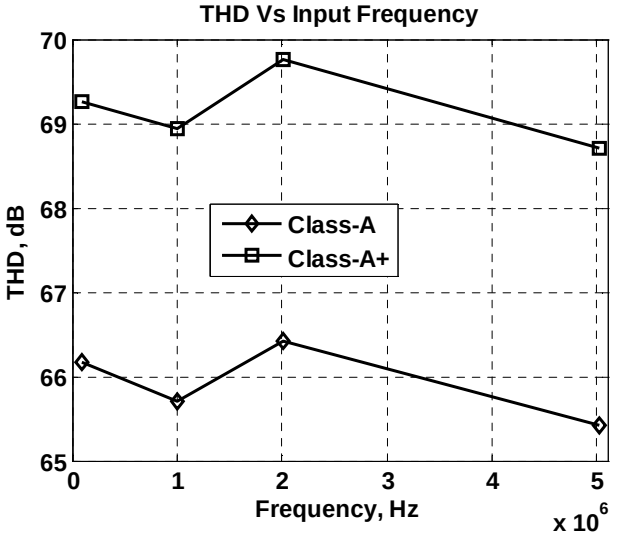


Figure 3.32: T. H. D vs. Frequency

3.11 Unified Gain Enhancement Model

The amplifiers discussed in the previous sections can be categorized into a unified gain enhancement classification chart is shown in Fig. 3.33. CDS, CLS, Replica amplifier, Asynchronous CLS and Class A+ amplifiers can be classified as shown in Fig. 3.33. This classification method not only allows us to categorize available techniques but also allows us to search for new gain enhancement technique methodically.

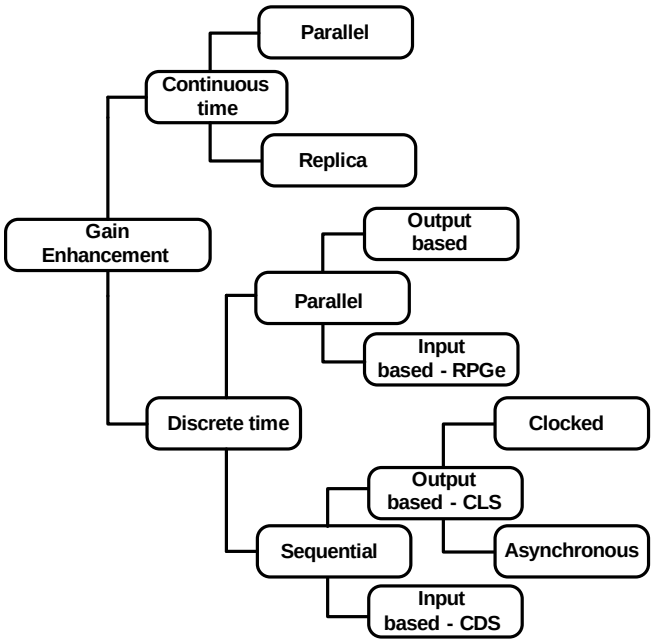


Figure 3.33: Gain Enhancement Model

3.12 Conclusion

In this chapter, we discussed circuit techniques to improve the energy and area efficiency of SAR ADC and pipeline ADC without sacrificing performance. In Chapter 4, a design and verification of pipeline ADC using RPGE amplifier will be discussed in detail as a proof of concept to the parallel gain enhancement technique in switched capacitor circuits.

Chapter 4. Replicated Parallel Gain Enhancement Technique

4.1 Introduction

Gain enhancement, distortion reduction and cancellation techniques are widely used in building high performance amplifiers. A unified gain enhancement classification chart was presented in the previous chapter. The gain enhancement techniques can be classified into continuous time and discrete time gain enhancement techniques. The continuous time gain enhancement technique can be broadly classified into parallel [56] and replica amplifier [57] based techniques. The discrete time gain enhancement techniques can be classified as sequential and parallel gain enhancement techniques based on their operation and implementation. Using this classification method, we identify the advantages and disadvantages of the existing gain enhancement techniques and propose a parallel gain enhancement technique, for switched capacitor circuits, combining the best features of the existing gain enhancement techniques.

In discrete time switched capacitor circuits, the gain enhancement techniques can be broadly classified into sequential and parallel gain enhancement techniques as shown in Fig. 4.1. The gain enhancement technique is classified as a sequential technique when the measurement of gain error and its correction are performed in two different clock phases. This sequential discrete time gain enhancement technique can be further classified into input and output based technique based on the location of the gain error measurement (input or output) and the correction of the measured gain error (input or output). Under this classification, correlated double sampling (CDS) technique [60] will fall under sequential input based gain enhancement technique. The correlated level shifting (CLS) and Split-CLS techniques can be classified as sequential output based gain enhancement technique [67]. The asynchronous sequential output based CLS technique was proposed in [71] and the parallel output based Class A+ amplifier technique was proposed in [72]. In this section, the proposed Replicated Parallel Gain Enhancement (RPGE) technique is a discrete time parallel input based gain enhancement technique for switched capacitor circuits.

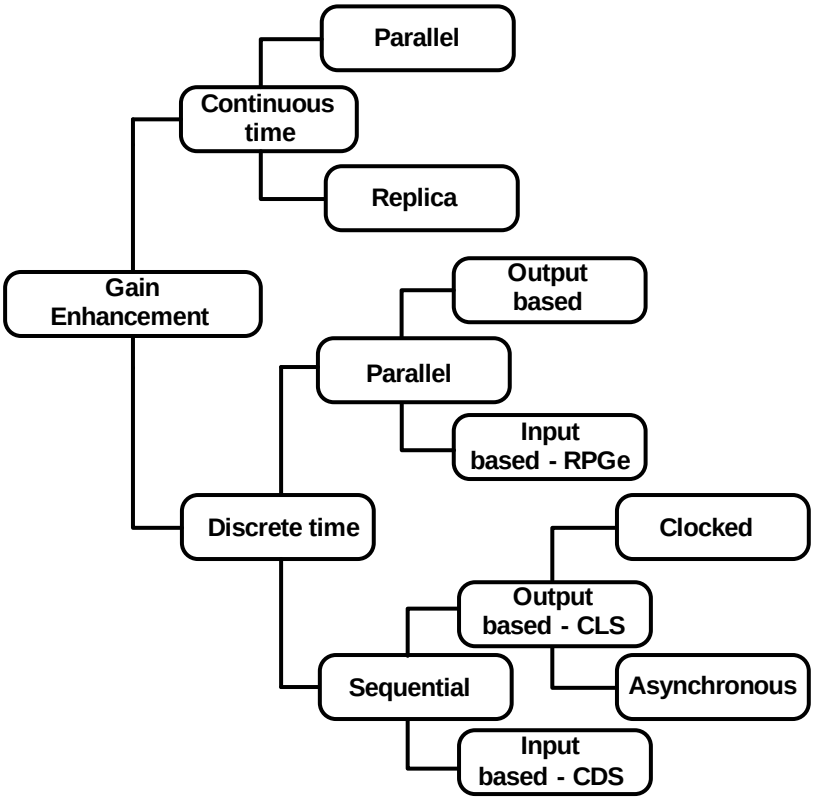


Figure 4.1: Gain Enhancement Model

4.2 Replicated Parallel Gain Enhancement Amplifier

4.2.1 CDS, CLS and Replica Amplifier

Advantages and Disadvantages of Correlated-Double Sampling, Correlated-Level Shifting and Replica Amplifier are summarized to provide insight into the gain enhancement techniques. Replicated Parallel Gain Enhancement Technique combines the best features of the above methods which results in an optimized high gain, bandwidth, low power and noise amplifier.

The sequential input based gain enhancement technique, CDS, is shown in Fig. 4.2. The disadvantages of this technique are : 1) Three phase clock generation 2) Frequency dependent gain enhancement and 3)Switches at the virtual node. The sequential output based gain enhancement technique, CLS, is shown in Fig. 4.2. The disadvantages of this technique are : 1) Three phase clock generation 2) Increased(twice) load capacitor during estimation phase and 3) Low frequency noise cancellation is absent. The replica amplifier is shown in Fig. 4.2. The disadvantages of this technique are : 1) mismatch between the main amplifier and replica amplifier load. 2) input referred offset and noise and 3) Replica amplifier power consumption.

4.2.2 RPGE

The proposed RPGE amplifier is shown in Fig. 4.3. The parallel nature of operation, present in the replica amplifier, transferred to a switched capacitor amplifier would enable the use of an existing two-phase non-overlapping clock, with reduced bandwidth and relaxed settling time requirement for the opamp. Also, the replica load at the input can be smaller (1/4x) than the required C_{cls} capacitor at the output. The output of the amplifier during the level shifting phase in the CLS technique is thus closer to the virtual ground. This important feature allows us to decouple DC-gain and output swing requirements to build an amplifier optimized for gain without the burden of swing requirement. The replicated parallel gain enhanced (RPGe) amplifier shown in Fig. 4.2 combines the above mentioned benefits of reduced bandwidth, settling time requirement, conventional two phase operation, smaller replica capacitor, decoupled DC gain and swing requirements to produce an optimized input based parallel gain enhancement

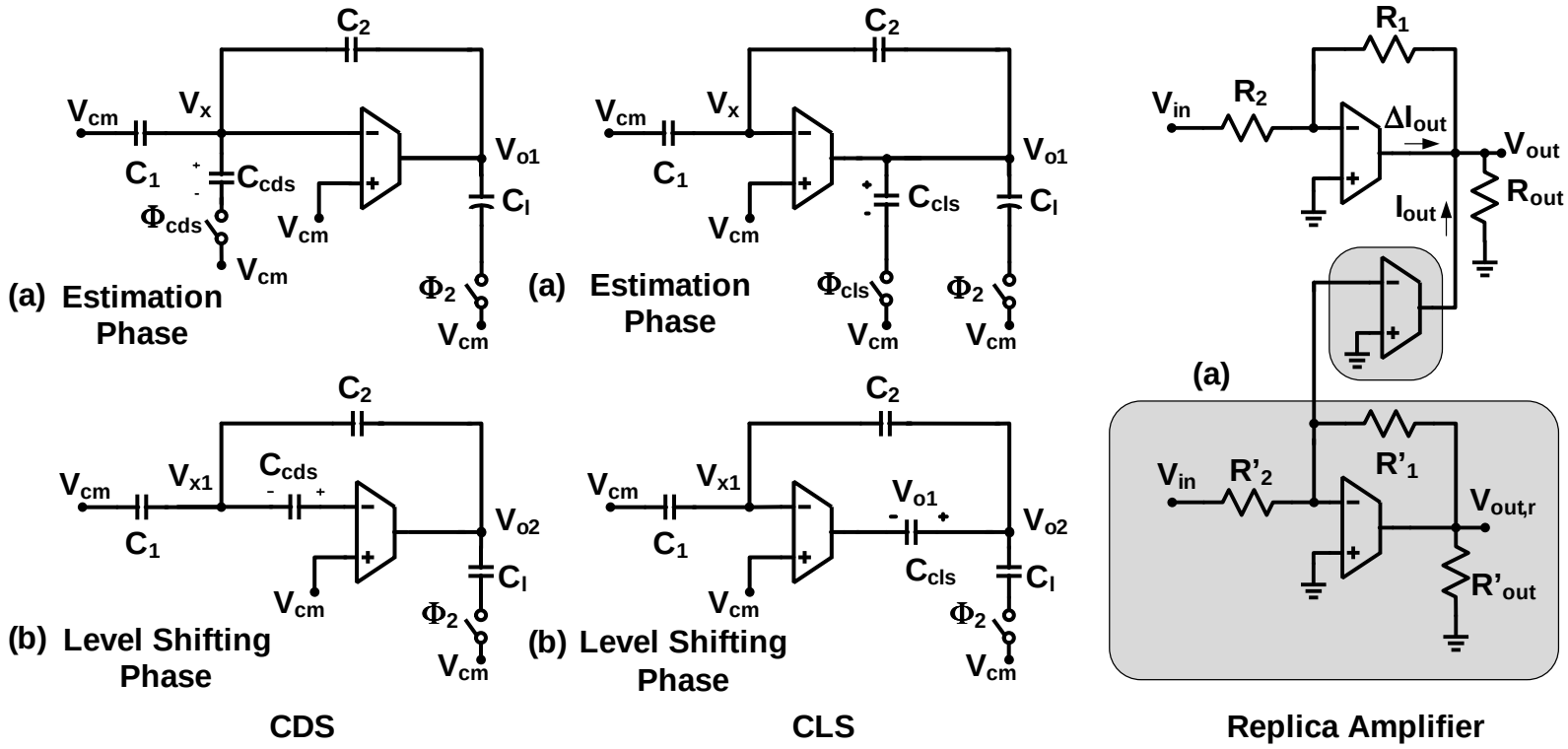


Figure 4.2: CDS, CLS, Replica Amplifier and Gain Assist

amplifier. Fig. 4.2 shows the main loop amplifier in black and the parallel loop amplifier section in the shaded region. The gain of the main loop is set by C_1/C_2 and that of the parallel loop is set by $C_1^{'}/C_2^{'}$. When the gain of the parallel path, $C_1^{'}/C_2^{'}$, is made higher than C_1/C_2, the first stage output (V_y) is forced to move closer to zero as the parallel loop virtual node (V_{x2}) swing increases.

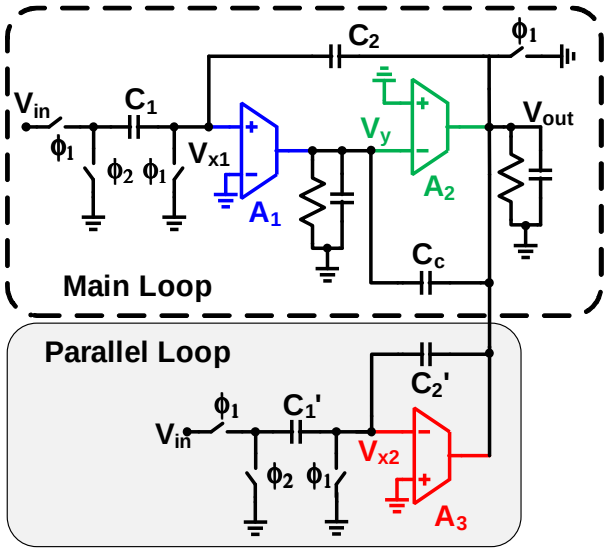


Figure 4.3: RPGE Amplifier

This trend is shown for the internal node voltages, V_y and V_{x2}, in Fig. 4.3. The improved loop gain is obtained from the gain correction/enhancement of second stage by reducing swing at node V_y. The equivalent open loop gain of RPGE amplifier can be made very high in theory by selecting the appropriate parallel path gain and is limited only by the capacitor ratio precision ($C_1^{'}/C_2^{'}$) in a given process. In reality, with non-linear transconductance and limited precision for capacitor ratio, the gain enhancement is at least the product of main loop and the parallel loop ($A_1A_2A_3$). The equivalent loop gain enhancement is shown in Fig. 4b. With ±20% mismatch in the parallel path gain, set by the capacitor ratio $C_1^{'}/C_2^{'}$, the loop gain enhancement is at least 20 dB. The effective loop gain is greater than 100 dB with ±10% mismatch in $C_1^{'}/C_2^{'}$. This is well within the matching accuracy of the on-chip capacitor.

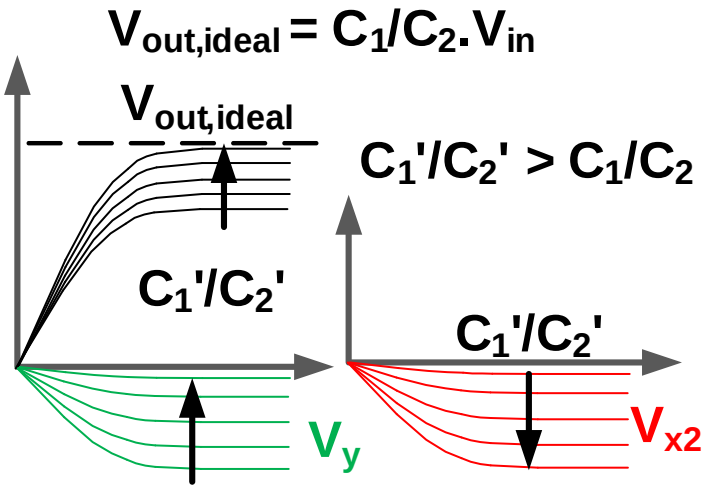


Figure 4.4: RPGE Internal Node Trend

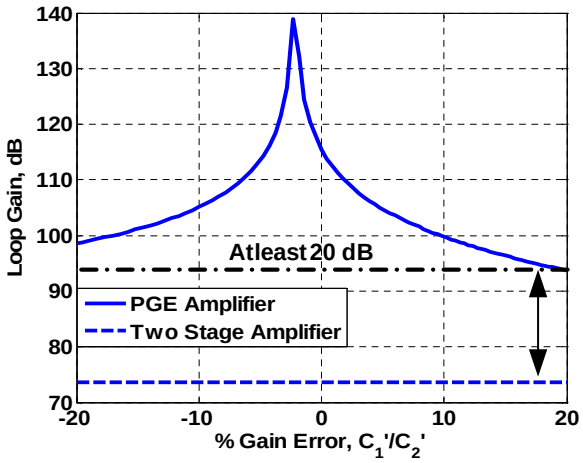


Figure 4.5: RPGE Macro-model simulation Trend

4.3 Pipeline ADC using RPGE amplifier

4.3.1 RPGE amplifier for Pipeline ADC

The RPGe amplifier is an ideal candidate for the high gain, wide bandwidth and high swing amplifier required in a high resolution pipeline ADC. Fig. 4.6 and Fig. 4.7 shows a fully differential switched capacitor RPGE amplifier and a transistor level implementation using a miller compensated two-stage amplifier with RPGE amplifier embedded in the second stage respectively. This implementation, among others, is attractive as it requires only switches and capacitors to implement the RPGE loop shown in the shaded region.

It is instructive to note that the use of this parallel path decouples the swing at the output of the first stage of the amplifier (V_y) and it is less than 5 mV for the entire output voltage range of the amplifier. This allows us to design the first stage for DC-gain and bandwidth without considering swing requirement. Fig. 4.8 shows the effective loop gain enhancement obtained with the transistor level design in Fig. 4.7. The amplifier in Fig. 4.7 was designed for a 2.5 bit MDAC stage in a pipeline ADC with the main path closed loop gain set to GM = 4 and the parallel path closed loop gain set to Gp = 5. Apart from the gain enhancement obtained from the parallel path, the RPGe amplifier can provide a higher output voltage swing as compared to a conventional two-stage amplifier. This is due to the push-pull nature of the PMOS and NMOS output stage as shown in Fig. 4.8. This push-pull nature of RPGE also enables a class-AB like operation of second stage, which allows 50 % reduction in the output stage power consumption and area as compared to a conventional two-stage amplifier.

4.3.2 Comparison of Two-Stage, Feedforward Two-Stage and RPGE

Table. 4.1 summarizes the comparison of performance parameters of a two-stage amplifier, a feed-forward push-pull two-stage amplifier, a two stage amplifier with gain boosted (GB) first stage and the RPGe amplifier. For clarity, the macro-model implementation of the amplifiers is shown in Fig. 4.9

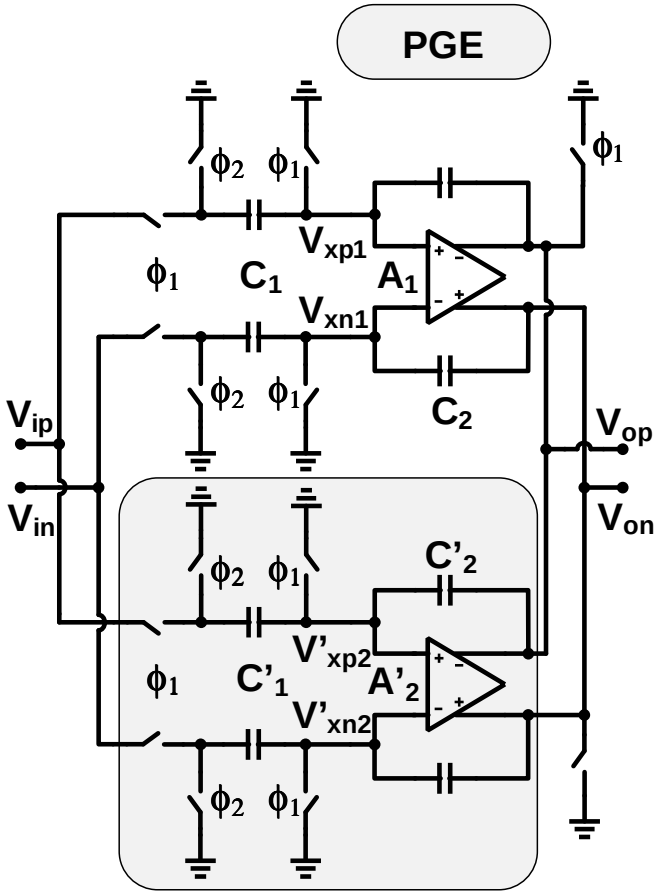


Figure 4.6: RPGE Switched Capacitor MDAC Implementation

Table 4.1: Comparison of Two-Stage, Feedforward, Gain-boosted and RPGE

Amplifier	DC Gain	Swing	Power	Distortion
Two-Stage	A_1A_2	Moderate	Moderate	Moderate
Feedforward Two-Stage	$A_1(A_2+A_3)$	High	Moderate	Moderate
GB Two-Stage	$A_1A_2A_{gb}$	Moderate	High	Low
RPGE	$\geq A_1A_2A_3$	High	Moderate	Low

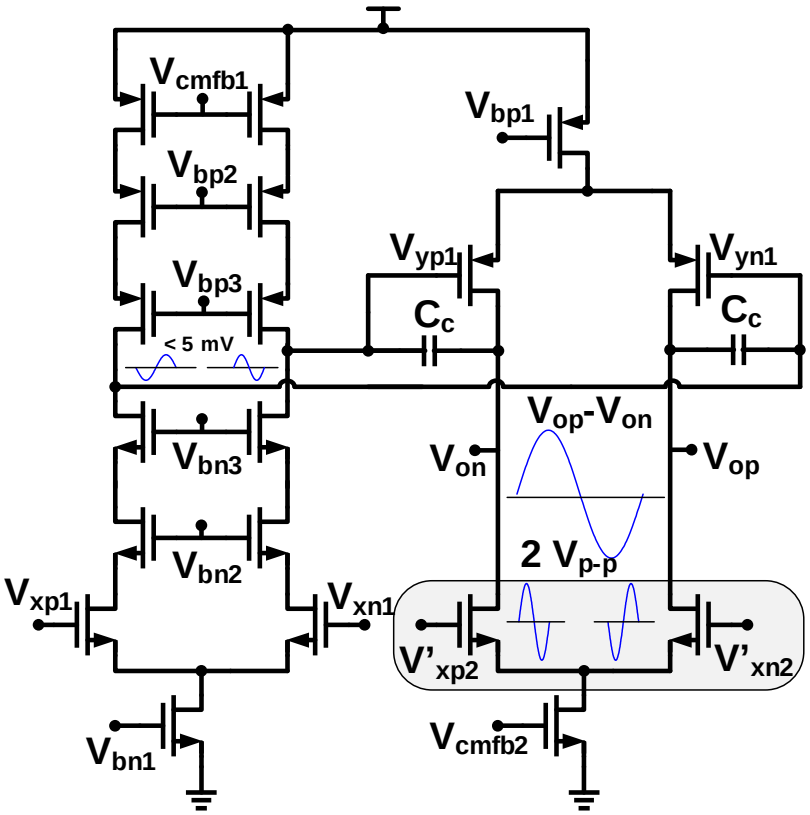


Figure 4.7: RPGE Transistor Level Schematic

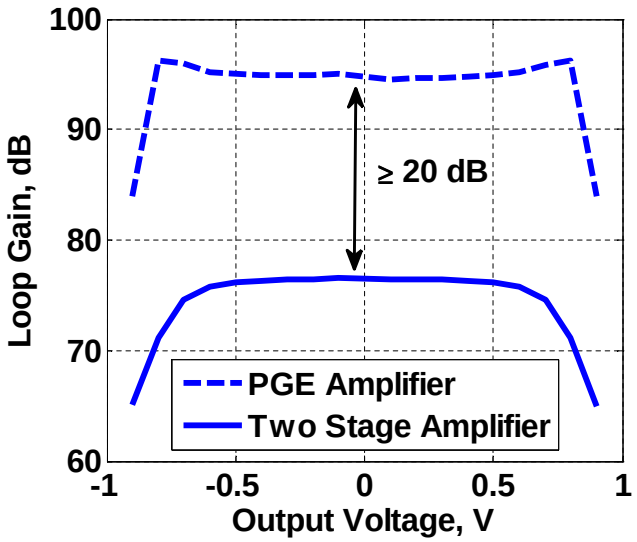


Figure 4.8: RPGE Transistor Level Simulation

4.3.3 13 bit Pipeline ADC System Level Design

In this section, we discuss a few design strategies used in the high resolution thermal noise limited pipeline ADC. As discussed in the previous chapters, noise, linearity, matching, power, area and performance are the optimization parameters in an ADC design. A generic pipeline ADC is shown in Fig. 4.10. However, while building a high resolution ADC($\geq$ 70dB), more often than not, matching requirement and noise budget are the most important factor of the design. In a mature process, it is possible to obtain 12-13 bit matching with careful layout. From Monte-Carlo simulations and previous chip results, 250 fF unit capacitor was sufficient to provide 13 bit matching.

Given that the matching requirement is satisfied, the noise budget must be analyzed to arrive at an optimum design parameter. The input referred noise in a pipeline ADC consists of three major noise sources. Input referred sampling noise, opamp noise and quantization noise are the major contributors. The total input referred noise can be calculated as shown in Eq. 4.1. Where, G is the interstage gain, Xs, is the capacitance scaling factor used in the pipeline ADC between stages and N_{stg}, is the number of MDAC stages in a pipeline ADC. $V_{n,total}, V_{n,opamp}, V_{n,quant}, V_{n,sampling}$ represent the total noise

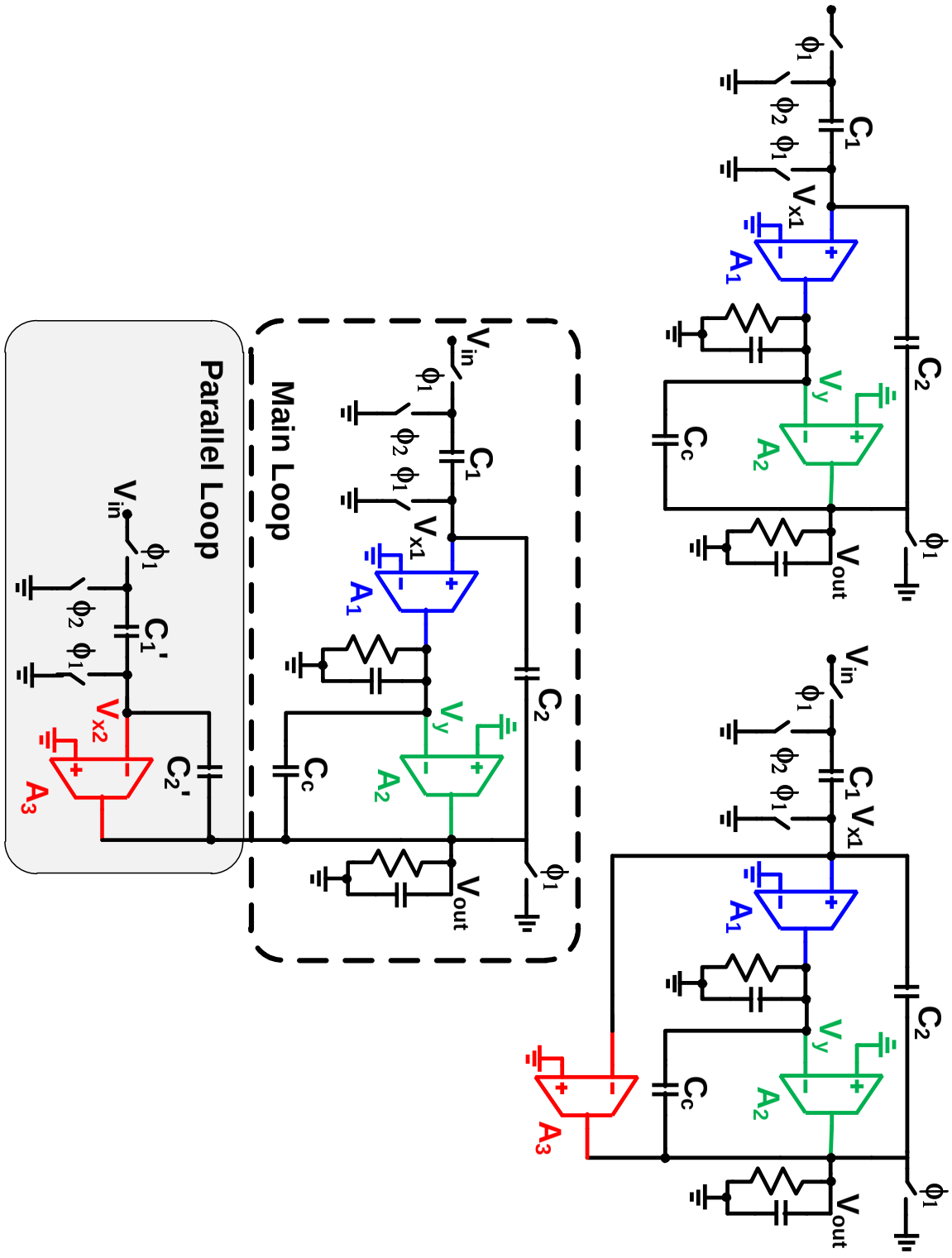


Figure 4.9: Comparison of Two-Stage, Feedforward and RPGE

power of pipeline ADC, opamp, quantization and sampling noise respectively.

$$V^2_{n,total} = \frac{G^2}{G^2 - \text{scaling}} \times \left(1 - \left(\frac{Xs}{G^2}\right)\right)^{N_{stg}} \left(V^2_{n,sampling} + V^2_{n,opamp} + V^2_{n,quant}\right) \quad (4.1)$$

For a 13-bit design, the noise budget was allocated as shown in Fig. 4.11. The sampling noise contribution was 40%, opamp noise contribution was 47.5% and the quantization noise contribution was 12.5%. With this setup, the total first stage capacitance was calculated as shown in Fig. 4.12. Approximately, 2 pF capacitance is required for 12.5-13 bit performance. With 250 fF as unit capacitor for matching requirement and a total of 2 pF for thermal noise requirement suggest that a 2.5 bit MDAC stage as a convenient design choice for this pipeline ADC. The DC-gain and loop bandwidth requirement for the amplifiers in each stage is shown in Fig.4.13 and Fig. 4.14 for completeness.

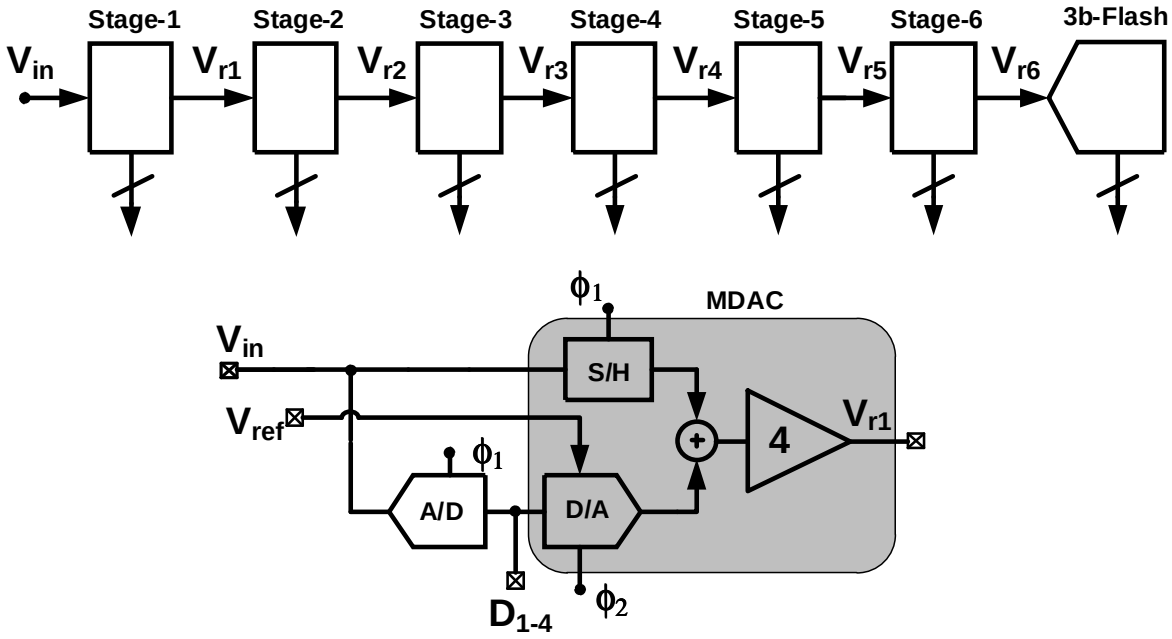


Figure 4.10: Generic Pipeline ADC

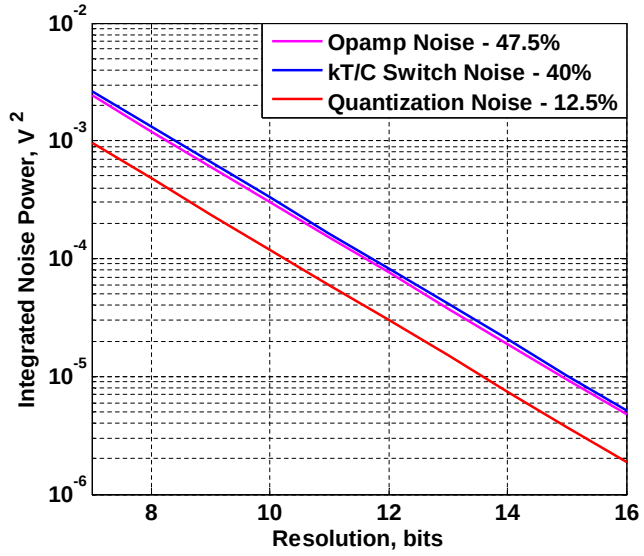


Figure 4.11: Noise Budget for Pipeline ADC

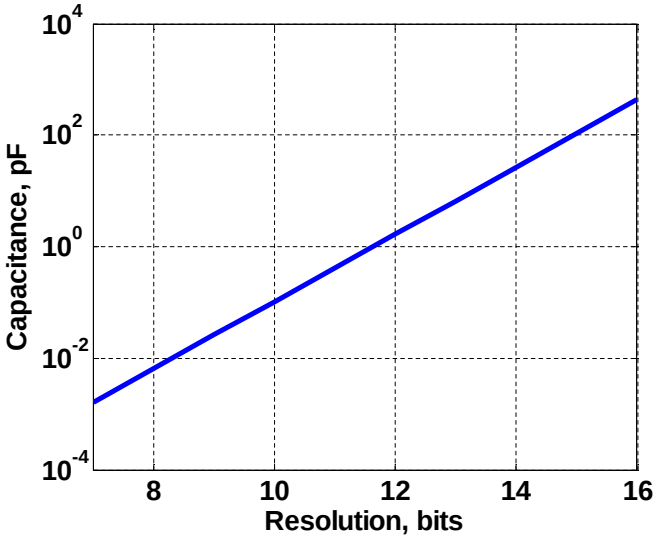


Figure 4.12: First Stage Total Capacitance for 40% Sampling Noise

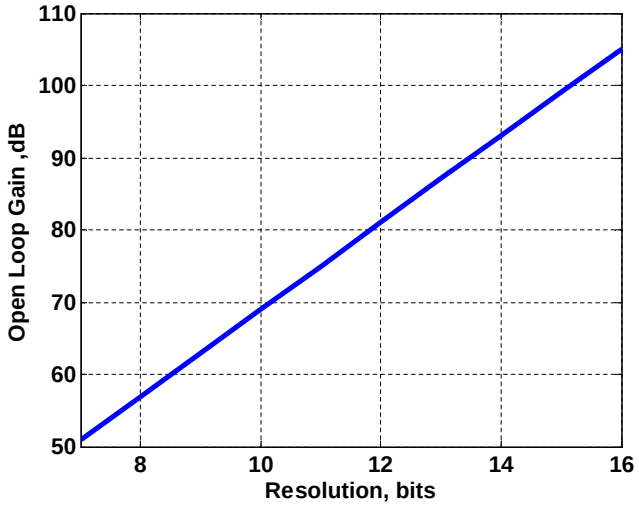


Figure 4.13: DC-Gain Requirement vs. Resolution

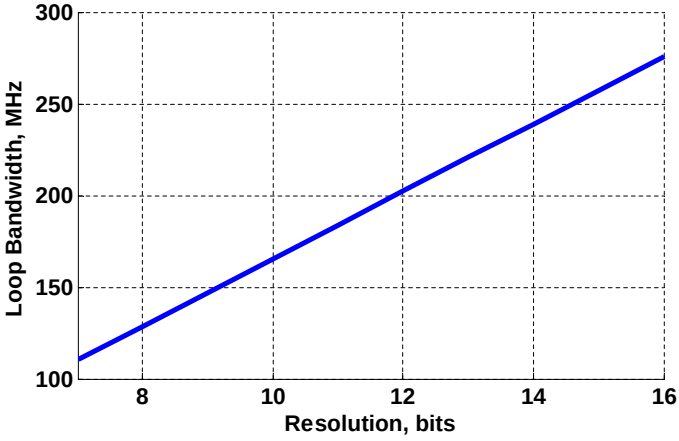


Figure 4.14: Loop Bandwidth vs. Resolution

4.3.4 FLASH ADC

A 9 level Flash ADC is used as a sub-ADC. The switched-capacitor based dynamic comparator and schematic is shown in Fig. 4.15 and Fig. 4.16 respectively. Timing used in Flash ADC is shown in Fig. 4.17. The input referred offset is less than 20 mV and is well within the redundancy range of the MDAC. The input is sampled during ϕ_{1s} and the differential reference voltages V_{refp} and V_{refn} are supplied from a resistor ladder in ϕ_{1ref}. After the non-overlap period and reference subtraction, the latch signal ϕ_{latch} samples the comparator output which is stored in the SR latch. Also, the output of the comparator is reset high and the SR latch output is held until the comparator output is re-evaluated in the next cycle.

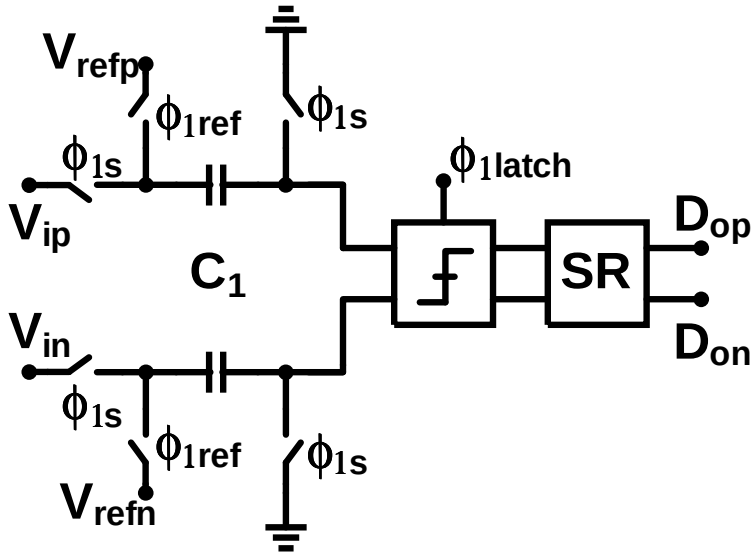


Figure 4.15: Flash Comparator

4.3.5 2.5 bit RPGE MDAC

The six stages of the pipeline ADC consists of 2.5 bit MDAC as shown in Fig. 4.18. RPGE amplifier is used in the MDAC stages and is shown in Fig. 4.19. Capacitor scaling factor of 2 was applied to four stages of the pipeline ADC. The gain of main path is G=4 and the gain of the parallel path is G_p=5. The RPGE amplifier provides DC

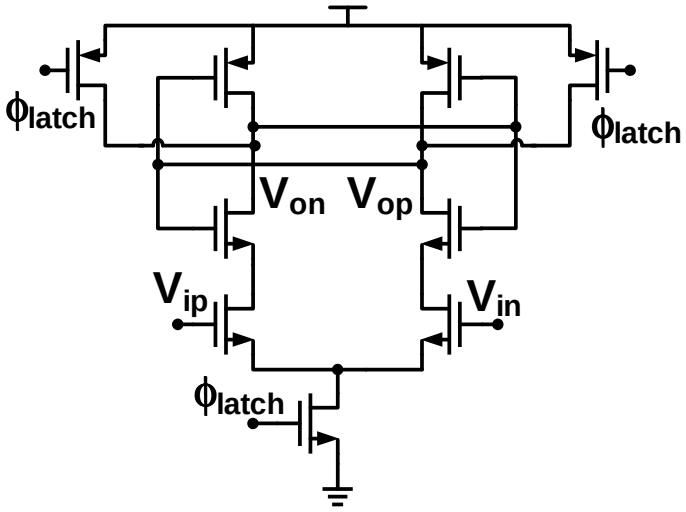


Figure 4.16: Flash Schematic

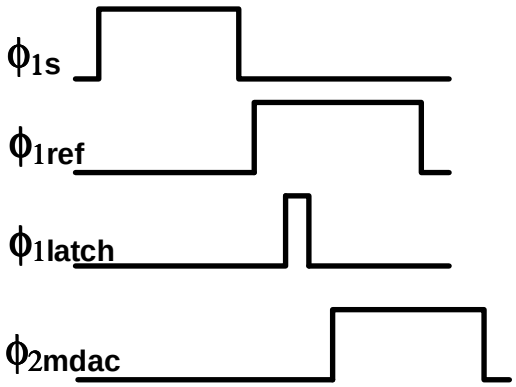


Figure 4.17: Flash Timing

gain of 94 dB and is more than sufficient for the accuracy requirement of 13-bit ADC. However, the non-linearity suppression is better with higher DC gain and the higher DC gain is expected to provide superior THD and SFDR performance.

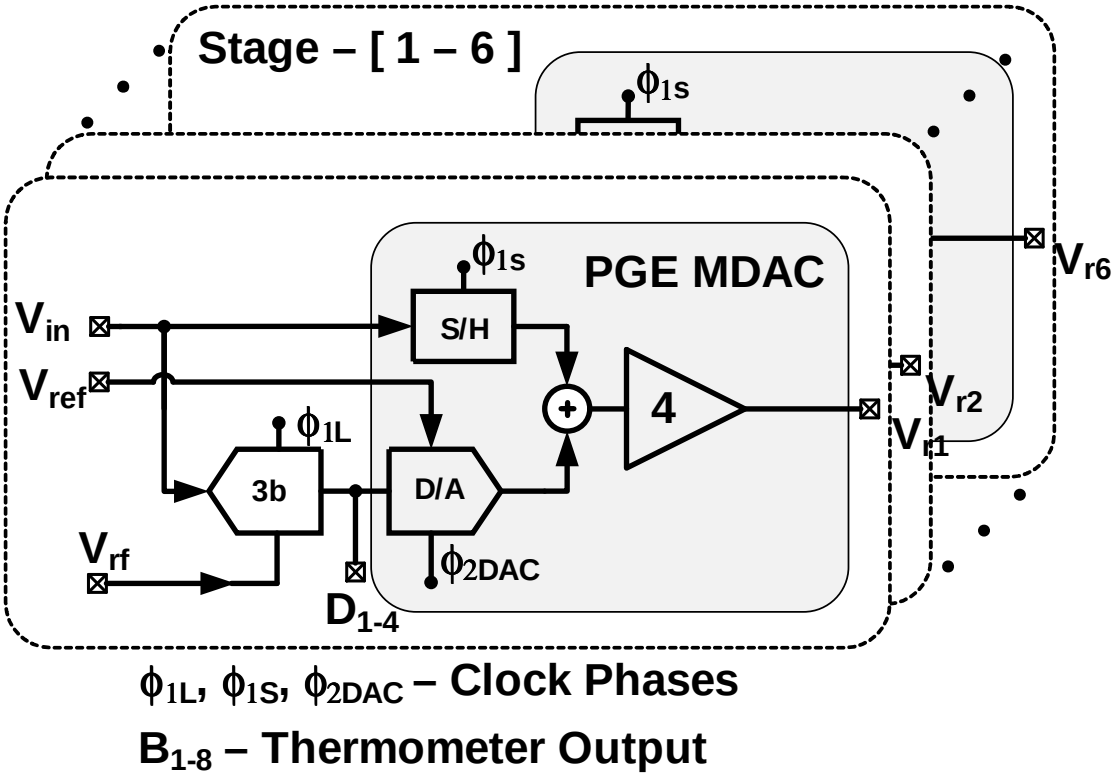


Figure 4.18: MDAC 1-6 Stages

4.3.6 Measurement Results

Built in 1P4M 0.18μm process, the prototype pipeline ADC occupies 3.6 mm x 0.85 mm active area and operates at 1.3 V supply voltage at 20 MHz clock frequency. Fig. 4.20 and Fig. 4.22 shows the single-tone and two-tone test setup. Fig. 4.21 and Fig. 4.23 shows the measured spectrum for a 1 MHz input with 20 MHz clock and two tone test respectively. As shown in Fig. 4.24, the measured 13-bit DNL and INL were +0.75/-0.36 and +0.88/-0.92 LSB respectively. The measured signal to noise and distortion (SNDR), spurious

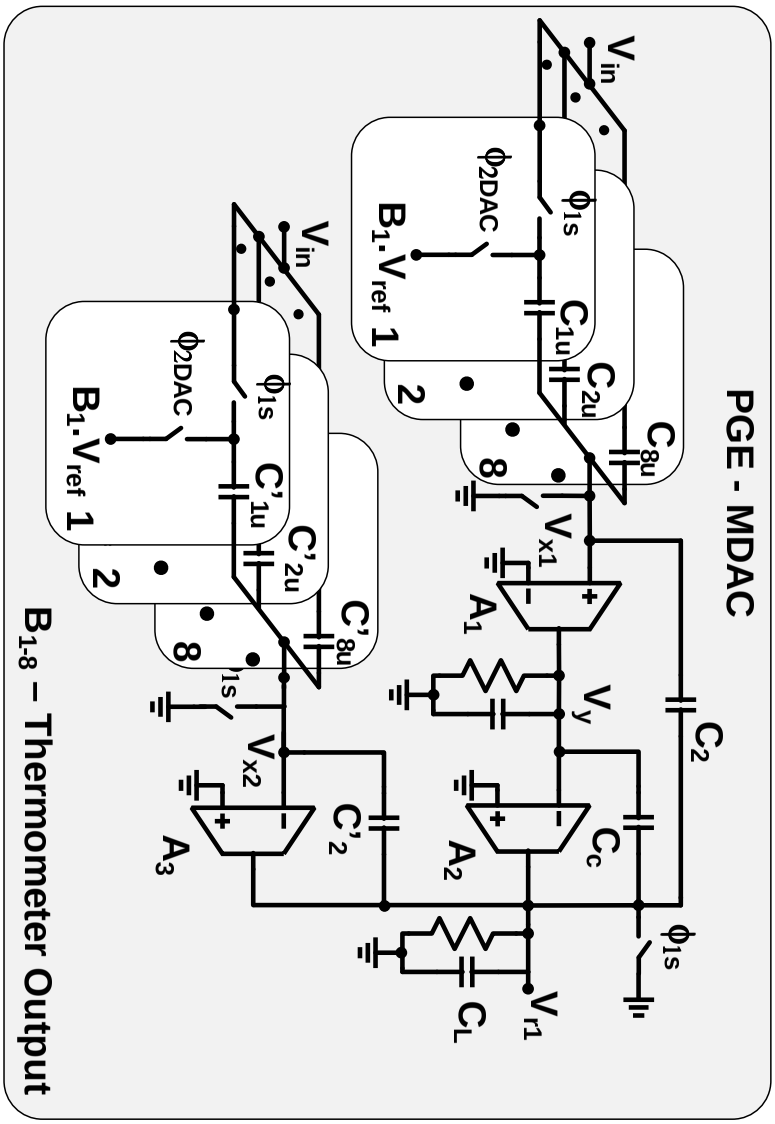


Figure 4.19: RPGE based MDAC

free dynamic range (SFDR) and THD were 74.92 dB, 90.8 dB and -87dB respectively. The reported measurements results are without any form of calibration. The zero-input noise floor is at -76.5 dB and is the expected SNR of the pipeline ADC.

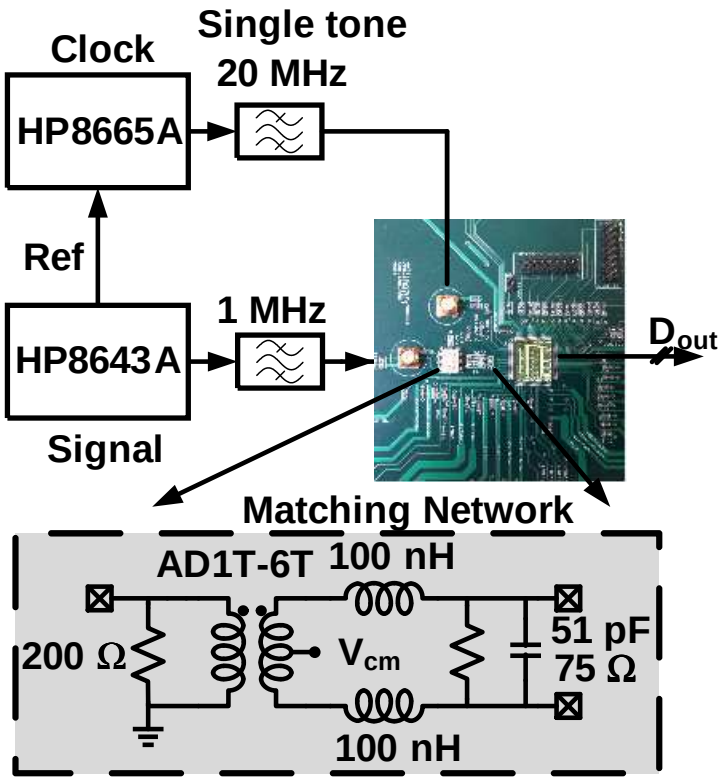


Figure 4.20: Single Tone Test Setup

The measured SNDR, SFDR and THD at 10 MHz Input were 71.3 dB, 88 dB and -86 dB. The SFDR and THD are above 88 dB and -86 dB for the entire 10 MHz bandwidth. The dynamic performance is shown in Fig. 4.25 and Fig. 4.26. The analog portion of power consumption was 4.07 mW. The digital portion consumes 1.83 mW and the total power consumption is 5.9 mW. Fig. 4.27, Fig. 4.28 and Fig. 4.29 show the die-micrograph, performance summary and comparison to other high resolution ADC published in the past 16 years respectively.

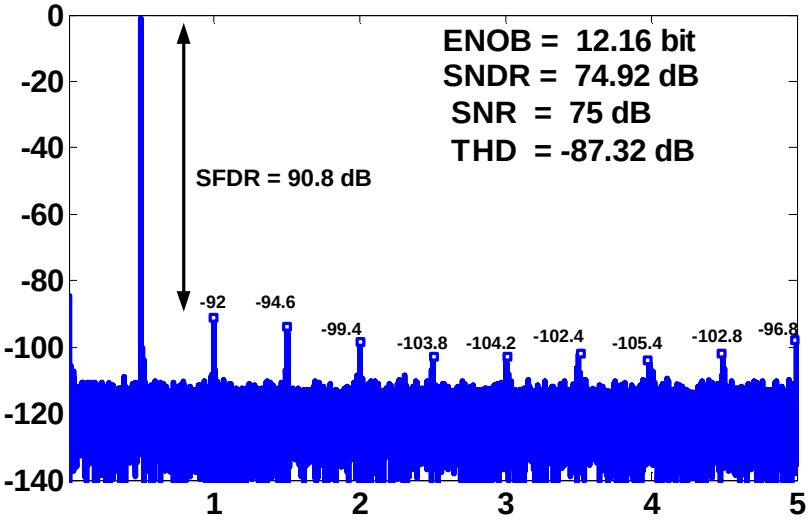


Figure 4.21: RPGE 1 MHz spectrum, Clock Frequency = 20 MHz

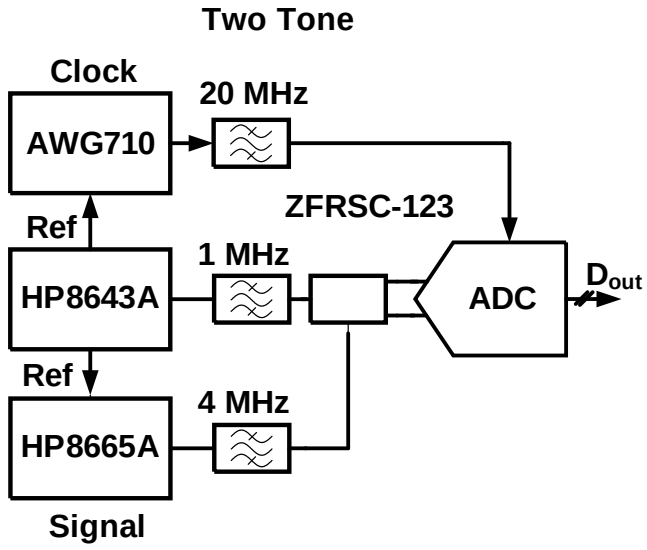


Figure 4.22: Two Tone Test Setup

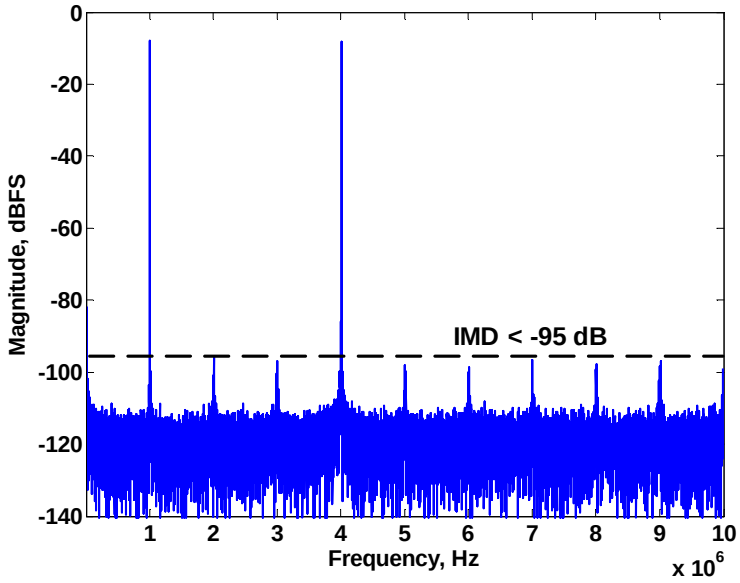


Figure 4.23: Two Tone Test Measurement

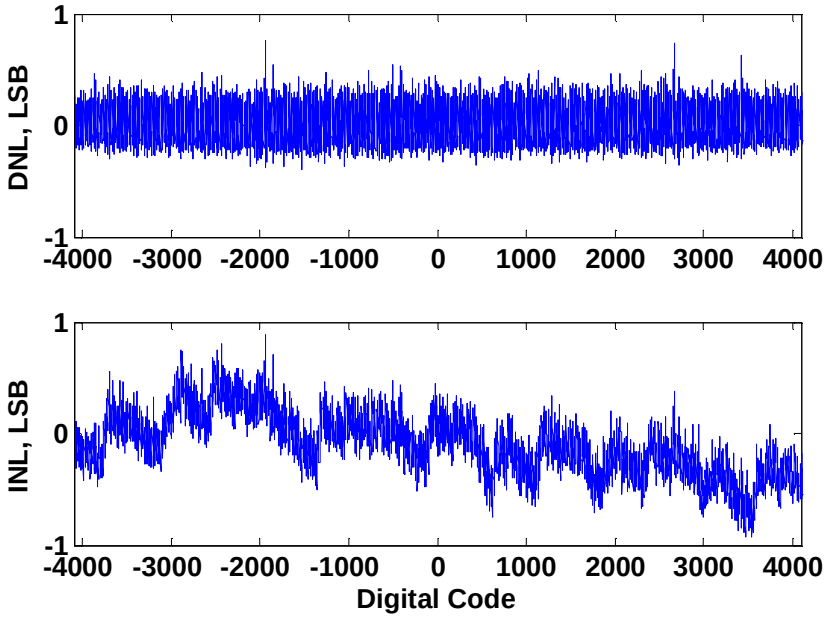


Figure 4.24: 13-bit INL and DNL Measurement

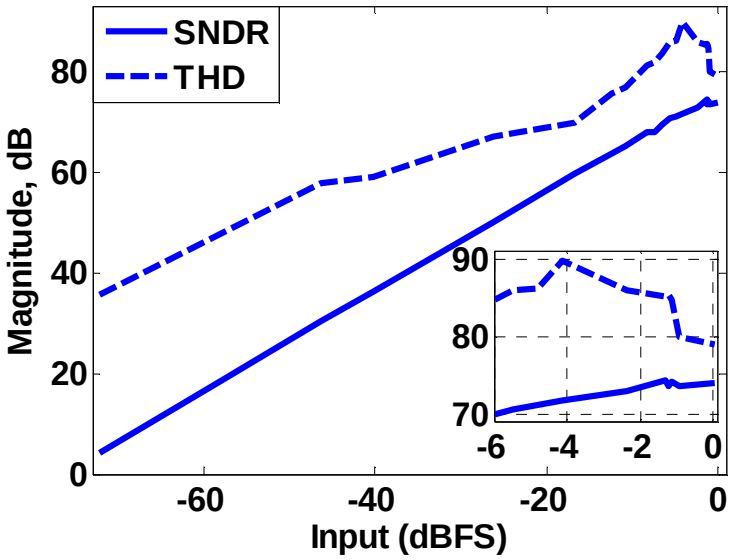


Figure 4.25: Input vs. SNDR and THD

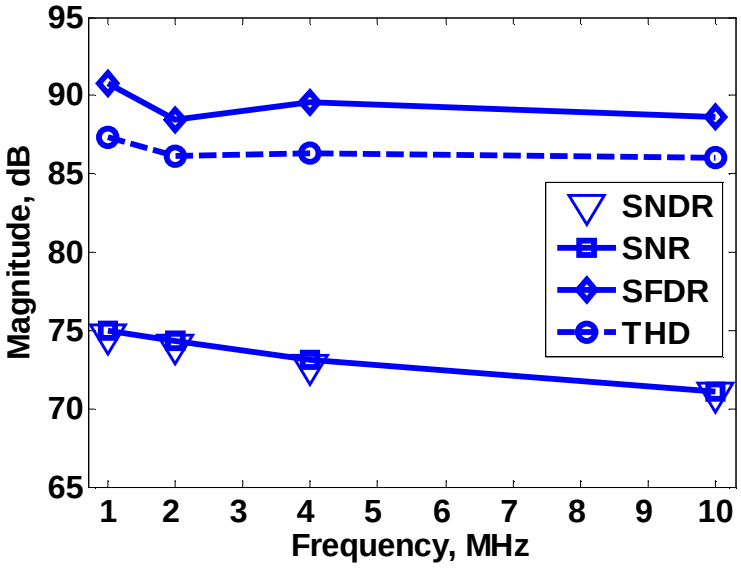


Figure 4.26: Input Frequency vs. SN(D)R, SFDR and THD

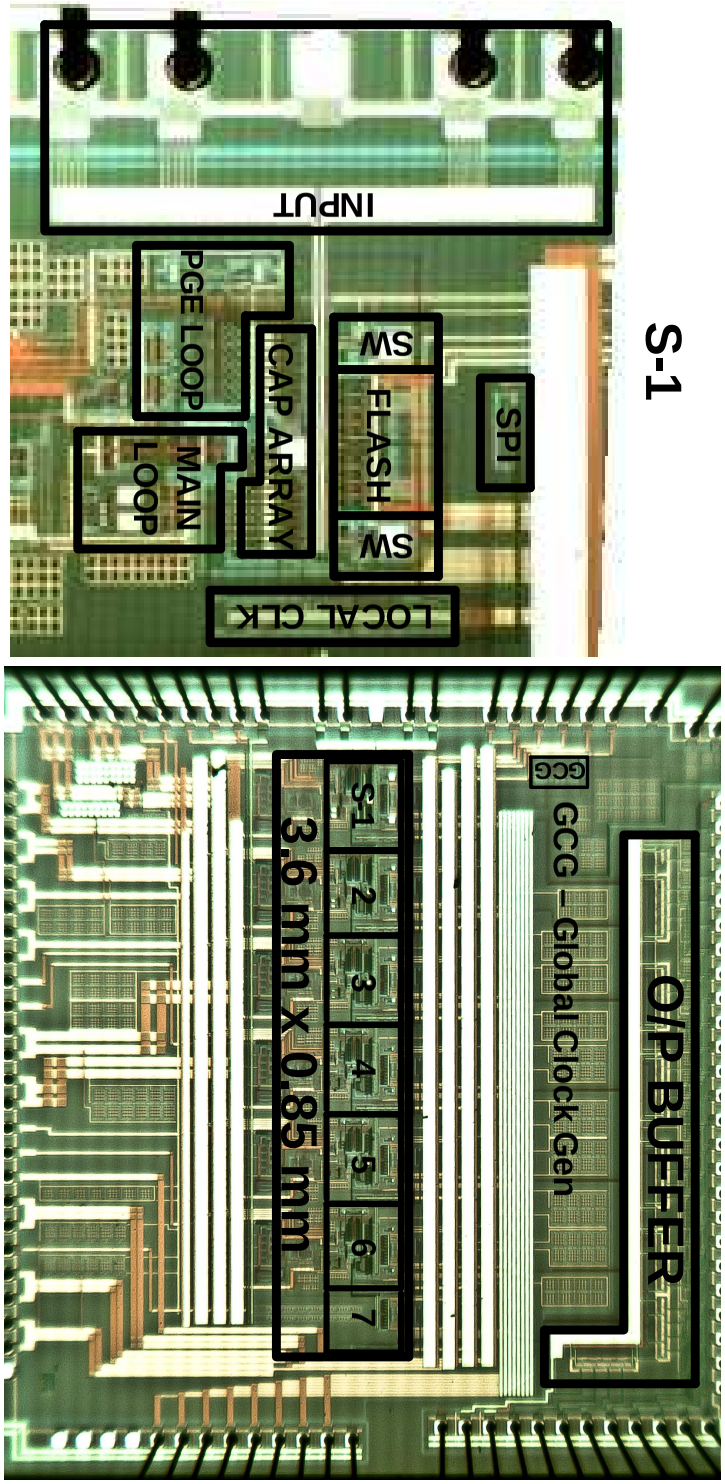


Figure 4.27: Die Micrograph

Parameter	Parameter
Technology	1P4M 0.18 µm
Supply Voltage	1.3 V
Sampling Rate	20 MHz
Input Voltage Range	2.4 V_{p-p}
SNDR/SFDR dB	74.9 dB / 90.8 dB
Power	5.9 mW
Active Area	3.6 x 0.85 sq. mm
FoM	65 fJ/CS
Resolution	13 bit

Figure 4.28: Performance Summary

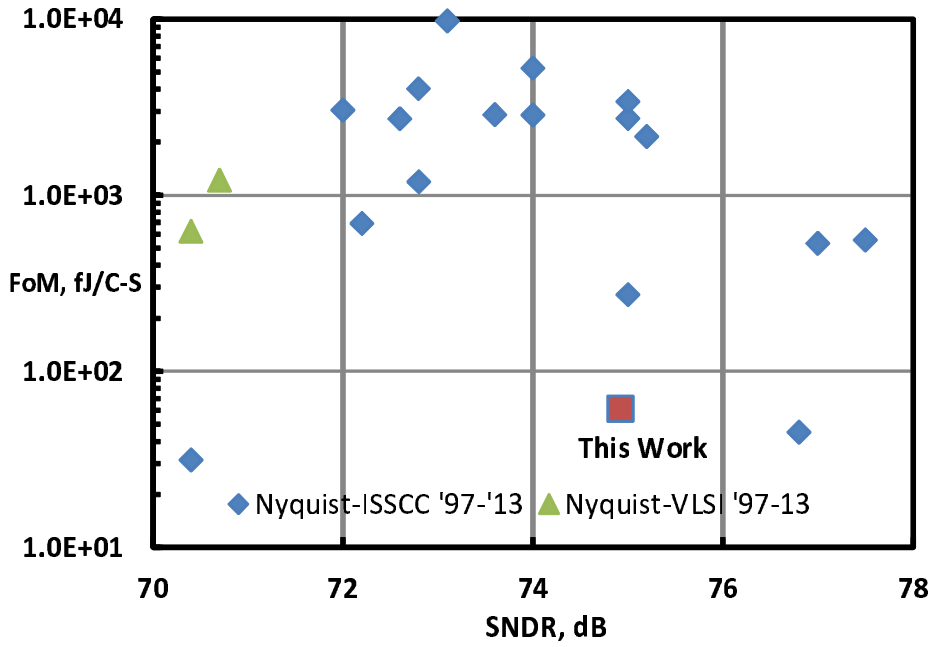


Figure 4.29: Comparison to Nyquist ADC $\geq$ 70 dB SNDR and 5 MHz BW

4.4 Pipeline ADC using Dynamic RPGE

In the previous section, RPGE was used for realizing high resolution pipeline ADC. The RPGE amplifier was constructed using conventional linear amplifier circuits. In this section, we attempt to use a dynamic non-linear amplifier in the parallel gain enhancement technique to break the trade-off between bandwidth vs. power. Dynamic amplifiers were used to provide large DC-gain, wide bandwidth and low power [73] and [74]. By using a dynamic class-AB amplifier along with the RPGE amplifier, the bandwidth of operation is increased by 65% with less than 10% increase in power consumption and area. Thanks to RPGE technique, the DC-gain is still above 94 dB as discussed in the previous section. The RPGE amplifier, dynamic RPGE amplifier and transistor level schematic are shown in Fig. 4.30, Fig. 4.31 and Fig. 4.32 respectively. Thanks to the dynamic amplifier, class AB amplifier combined with the RPGE amplifier provides 65% increase in bandwidth of operation while the area and power increase is less than 15%.

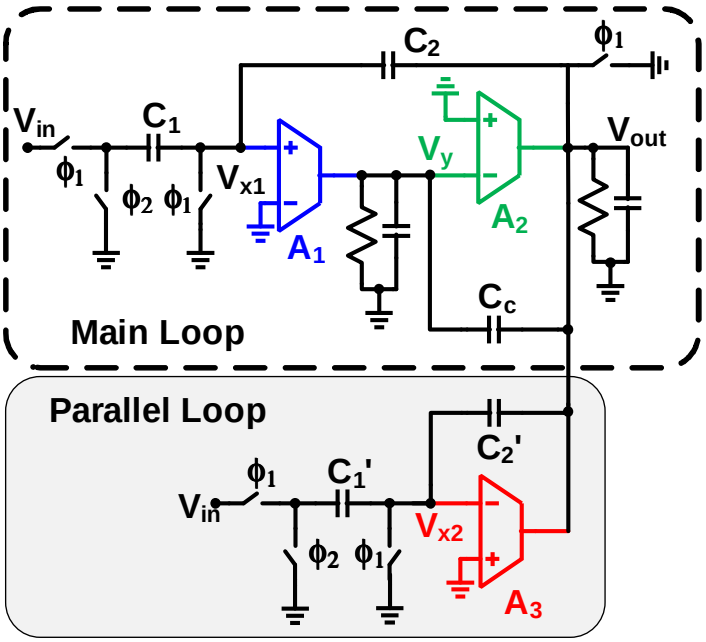


Figure 4.30: RPGE amplifier

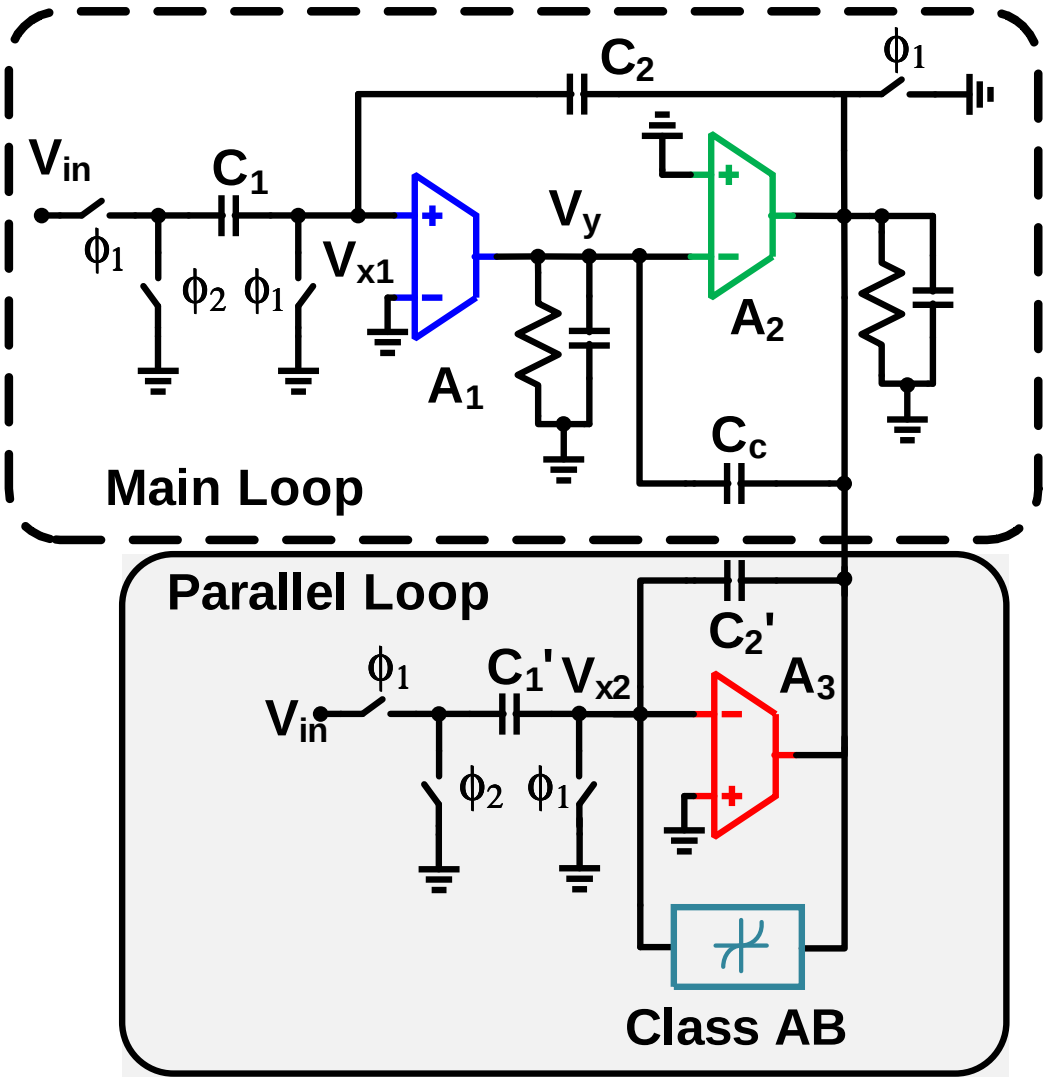


Figure 4.31: RPGE Dynamic amplifier

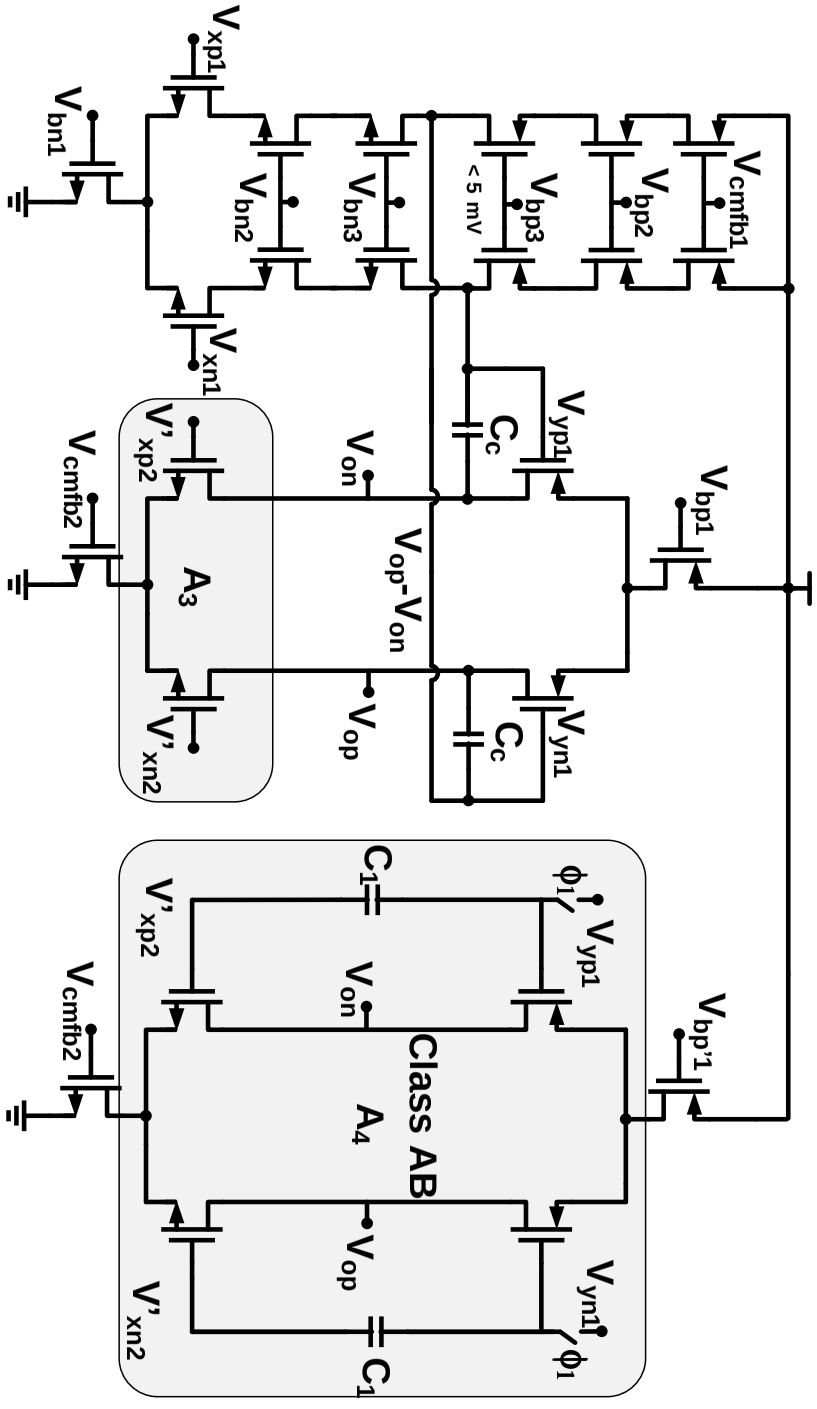


Figure 4.32: RPGE Dynamic amplifier - Schematic

4.4.1 13-bit Pipeline ADC using Dynamic RPGE Amplifier

A 13-bit high resolution pipeline ADC was realized using dynamic RPGE amplifier. A 2.5 bit dynamic RPGE MDAC is shown in Fig. 4.33. The pipeline ADC consists of six stages of 2.5 bit MDAC and a 9 level flash ADC. Built in 0.18μm process, the pipeline ADC consumes 6.6 mW from a 1.3 V supply and occupies 3.85 x 0.85 sq.mm. The clock frequency of operation is 33 MHz and the simulated power spectral density is shown in Fig. 4.35. The simulated performance is 74 dB SNDR/ 88 dB SFDR at 1 MHz input frequency with 33 MHz clock frequency. The layout of the chip in fabrication is shown in Fig. 4.34. The simulated performance summary is given in Fig. 4.36.

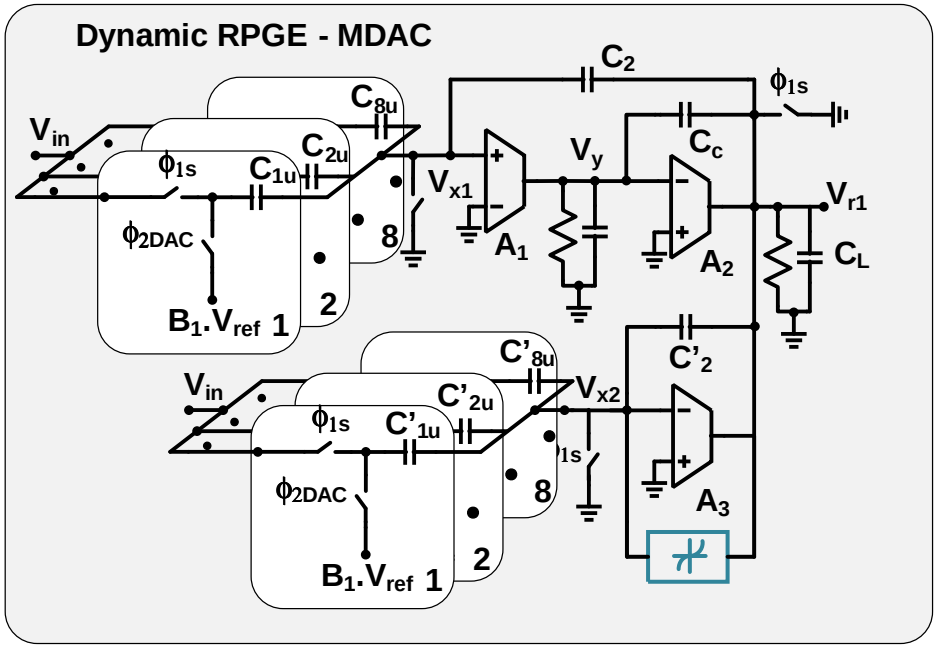


Figure 4.33: Dynamic RPGE MDAC

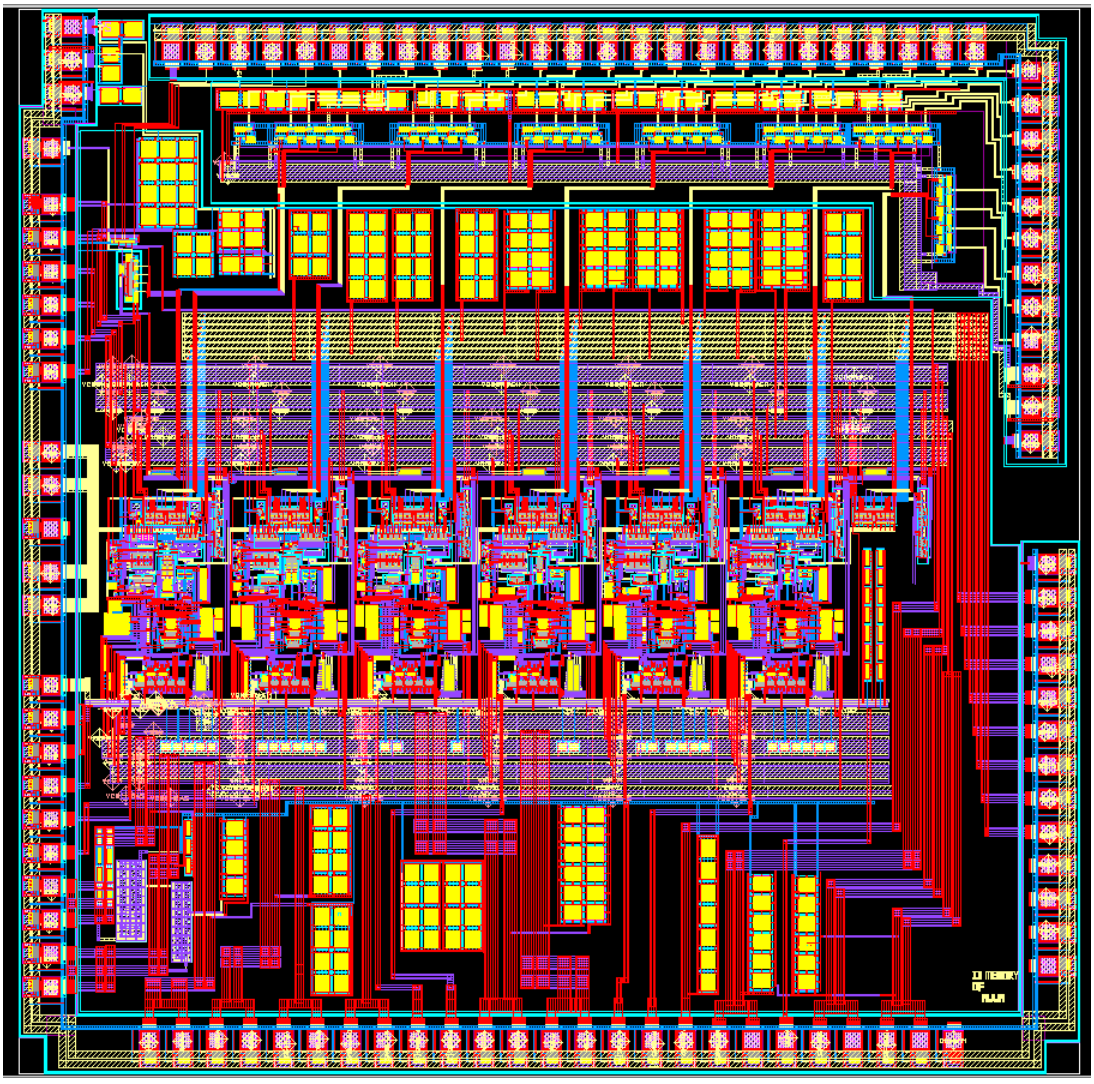


Figure 4.34: Dynamic RPGE Pipeline Layout

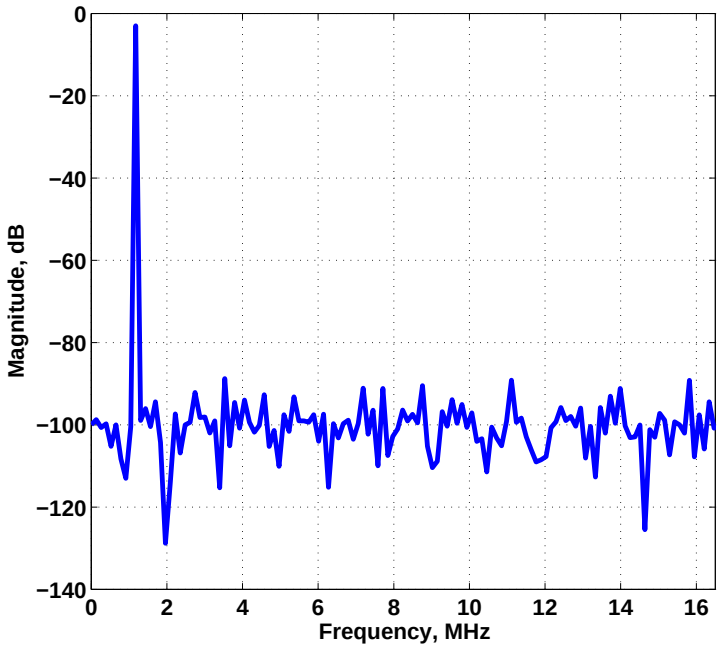


Figure 4.35: PSD of Dynamic RPGE Spectrum, SNDR = 74 dB

Parameter	Parameter
Technology	1P4M 0.18 µm
Supply Voltage	1.3 V
Sampling Rate	33 MHz
Input Voltage Range	2.4 V_{p-p}
SNDR/SFDR dB	74 dB / 88 dB
Power	6.6 mW
Active Area	3.6 x 0.85 sq. mm
FoM	48 fJ/CS
Resolution	13 bit

Figure 4.36: Performance Summary

Chapter 5. Hybrid Voltage-Time Pipeline ADC

5.1 Introduction

In the previous chapters, architecture, calibration and circuit techniques were considered for energy and area efficient ADC design. In particular, pipeline ADC was considered in the context of power efficient design using circuit and calibration techniques to mitigate the non-idealities present due to the CMOS process. In this chapter, we explore a hybrid voltage-time pipeline ADC architecture which takes advantage of the improved time resolution present in the deep sub-micron process. Also, a time-domain quantizer which can be used to replace the flash sub-ADC and the capacitor DAC is introduced to realize this power efficient architecture.

5.2 Hybrid Voltage-Time Converter

The improved time resolution from the deep submicron process offers an opportunity to use a time-digital converter (TDC) as a replacement for flash ADC of the pipeline ADC [75] and [76]. It is also possible to replace flash ADC and capacitor DAC in a traditional pipeline stage using a TDC. However, the mismatch analysis of delay cells in a 65 nm process indicates 5-6 ps of delay variation between delay cells. This mismatch accuracy translates to 6-7 bit matching for a 5 ns period. In order to build a medium-high (10-12 bit) resolution pipeline ADC, either the delay cells must be sized accordingly to improve the matching requirement or a traditional capacitor DAC must be used for the first stage.

In this design, a traditional flash ADC and a capacitor DAC based first stage is used with a hybrid voltage-time converter. This hybrid V-T converter enables the use of low gain, wide bandwidth opamp for a high resolution pipeline ADC as shown in Fig. 5.1. During the residue amplification phase, ϕ_{2dac}, the residue is converted to a time domain signal using a discharging current source(I_{dis}). The zero-crossing detector (ZCD) samples the DLL edges to provide the sub-ADC output. The zero-crossing detector output is

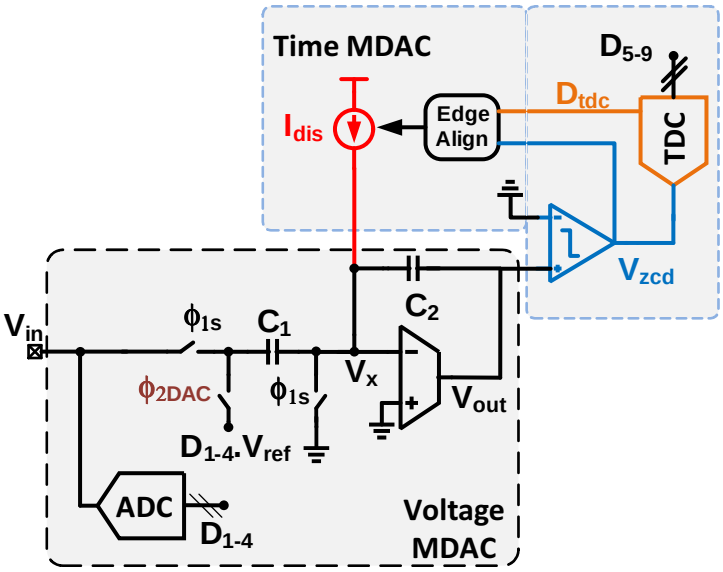


Figure 5.1: Hybrid Voltage-Time Converter

aligned with the next edge of the DLL using a edge align block. This edge aligned signal is used to switch-off the current source. This operation provides the quantization error which is sampled directly onto a capacitor as shown in Fig. 5.1. Thus, the TDC combined with a edge align block can be used to replace a traditional flash ADC and capacitor DAC array. As discussed before, the matching accuracy of the delay line is around 7-bits and is within the accuracy limits of the second stage of the pipeline ADC. The hybrid voltage-time pipeline ADC is shown in Fig. 5.2.

5.3 12-bit Pipeline ADC

The 12-bit pipeline ADC consists of a 3.5 bit traditional MDAC stage with a flash ADC and a capacitive DAC. The hybrid voltage-time converter converts the residue into a time-domain signal which is sampled by a 4-bit TDC and the residue for the next stage is stored in the capacitor.

With one-bit redundancy, the output from four stages are combined to produce a 12-bit output. Linear gain error correction is applied to each stage to eliminate the gain error introduced by the low gain amplifier. Since the zero-crossing is at a fixed voltage

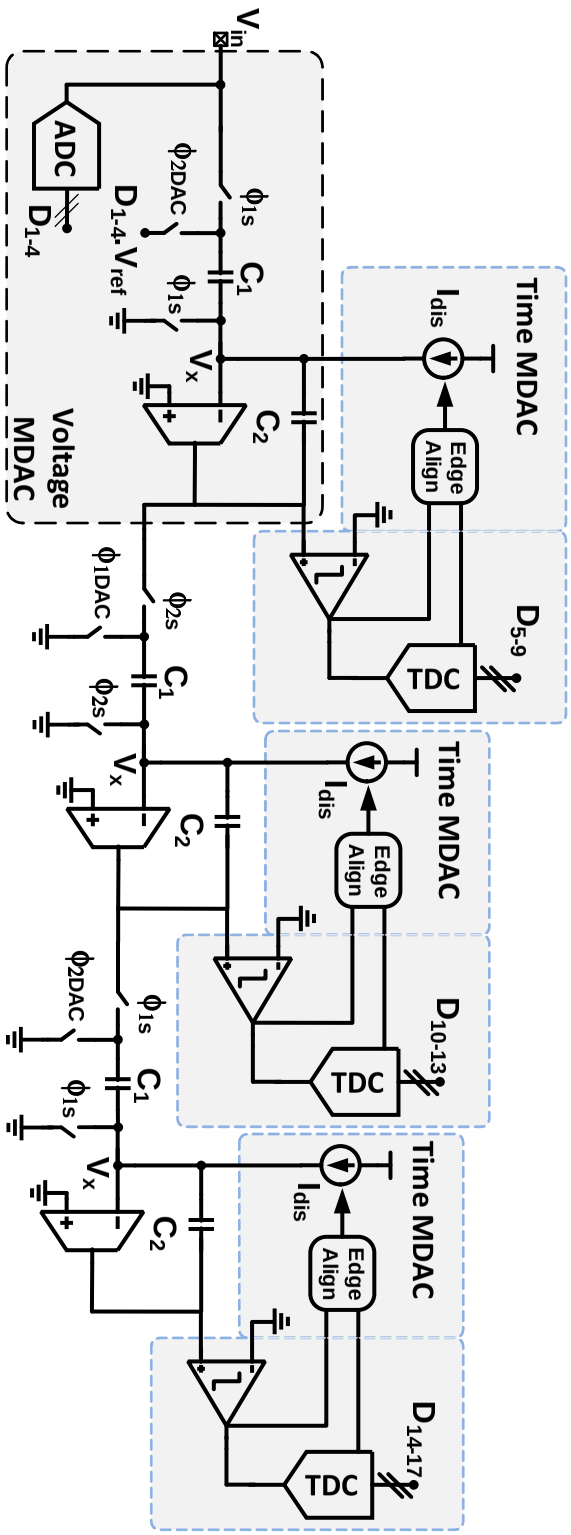


Figure 5.2: Hybrid Voltage-Time Converter - Operation

and is close to the common-mode output of the amplifier, the linear gain error correction is sufficient for the entire output signal range [75].

5.4 Circuit Implementation

5.4.1 Timing and Flash ADC

The first stage of the hybrid pipeline ADC consists of a 3.5 bit flash ADC and a conventional capacitor DAC to realize MDAC operation. The offset of the flash ADC is minimized with a preamp and offset cancellation as shown in Fig. 5.3. The pipeline ADC does not have a S/H and the path mismatch exists between the flash ADC and the MDAC. The sampling period ϕ_1 is split into two parts ϕ_{1s} and ϕ_{1ref} to provide enough time for input sampling and reference sampling. The latch samples the output of the preamp during ϕ_{1latch} and the amplification phase begins after a short interval for the MDAC references to be set by the flash ADC output. This timing diagram for the pipeline ADC is shown in Fig. 5.4.

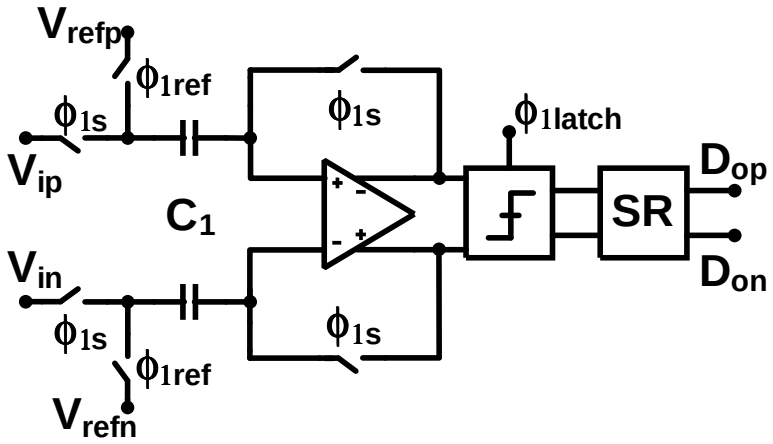


Figure 5.3: Offset Compensated Flash Schematic

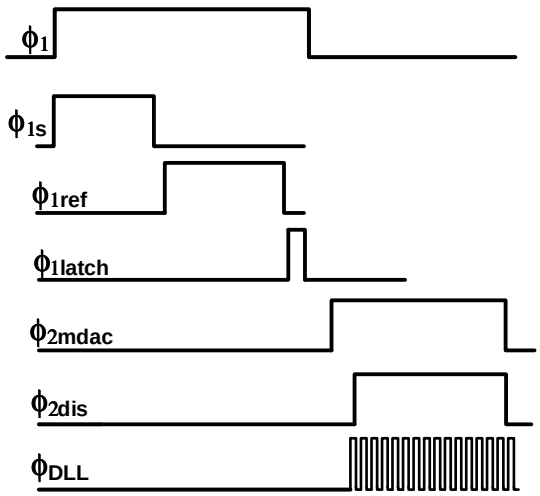


Figure 5.4: Hybrid Pipeline ADC Timing

5.4.2 MDAC and V-T Converter

The hybrid V-T converter enables the use of a low gain, wide bandwidth and non-linear amplifier. The amplifier used is shown in Fig. 5.6. A two-stage amplifier with minimum size transistors are used to provide 40 dB open loop gain. The 3.5 bit stage has a feedback factor of 1/9 which results in a close loop gain of less than 24 dB. Thanks to the V-T converter, the non-linearity of the amplifier does not affect the residue amplification as the zero-crossing event is always at the common-mode of the amplifier output. Thus, a linear gain error correction is sufficient to provide a high resolution(12 bit) first stage. The amplification phase begins during ϕ_{2mdac} as shown in Fig. 5.4. The discharge phase, ϕ_{2dis}, begins after 1τ to avoid any false detection. The discharge current, I_{dis}, connected to the virtual ground of the opamp converts the residue output into a pulse-width modulated time domain pulse which is sampled using a 4-bit TDC using delay-lock loop(DLL) edges as shown in Fig. 5.5.

5.4.3 Zero-Crossing Detector

The continuous time zero-crossing comparator used for zero-crossing detection is shown in Fig. 5.7. The output, V_{OUT}, of the ZCD is reset low during the sampling phase.

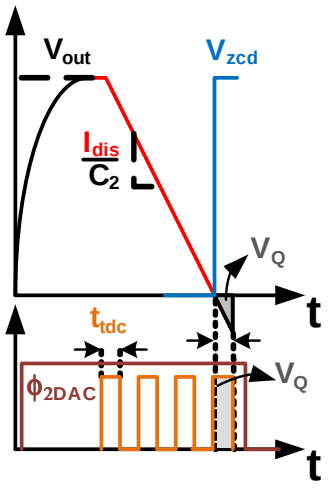


Figure 5.5: Hybrid Voltage-Time Converter - Operation

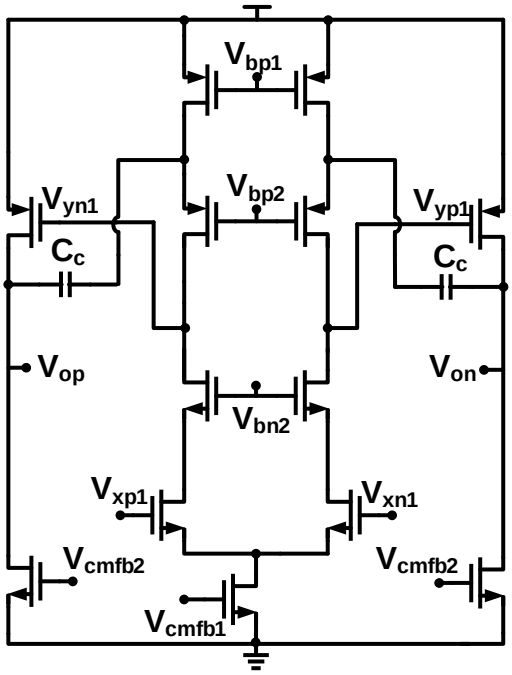


Figure 5.6: Cascode Compensated Opamp

The output of the MDAC is connected to the ZCD through a variable offset correction network to compensate for the static offset. The offset arises due to the non-idealities such as bandwidth limitation of the current source, amplifier and the delay of the sampler in TDC. This switched capacitor network shown in Fig. 5.7 can efficiently correct for the offset than the traditional offset correction methods. The ZCD consists of preamp stage with a clamp which drives the single-ended amplifier to detect the zero-crossing event. The skewed inverter restores the output logic level and this output, V_{OUT}, is stored in SR logic register which is used as the data line for the reduced metastability sampler in TDC.

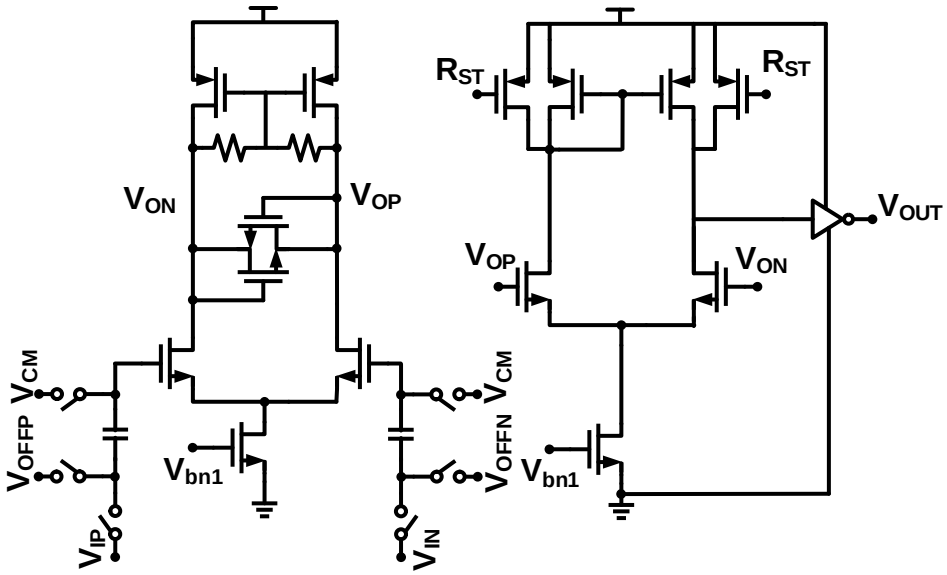


Figure 5.7: Offset Compensated Zero-Crossing Detector

5.4.4 Time-to-Digital Converter and Discharging Current Source

The deep sub-micron process provides improved time resolution. The hybrid pipeline ADC architecture is tailored to take advantage of this improved time resolution. As discussed earlier, a 7 bit linear TDC is possible without any calibration in a 65 nm process which is used for the second stage of the pipeline ADC. The 4-bit TDC shown in Fig. 5.8 replaces the flash ADC and the capacitive DAC in the conventional MDAC stage.

The discharge pulse, ϕ_{2dis} propagates through the delay line and the zero-crossing edge is sampled by this delay line as shown in Fig. 5.8. In order to reduce the metastability window of the flip-flop, the output of successive delay lines sampler (latch and DFF) are used to provide the output which reduces the metastability window. This edge aligned pulses are combined using a "OR" gate which provides the START/STOP signal for the discharging current source. The discharging current source is shown in Fig. 5.9. The discharging current source consists of a p-type and a n-type current source with a common-mode feedback. The current source is source degenerated with a resistor to reduce the effect of the flicker noise. The output of the current source V_{xn} and V_{xp} are connected to the opamp virtual node and is controlled by the "START/STOP" signal provided by the TDC. The linearity of the current source is approximately 9 bits and this translates to a input referred 13-bit linearity. The noise contribution of the current source is discussed in [75] and is accordingly sized to satisfy the noise budget of the 12-bit hybrid ADC.

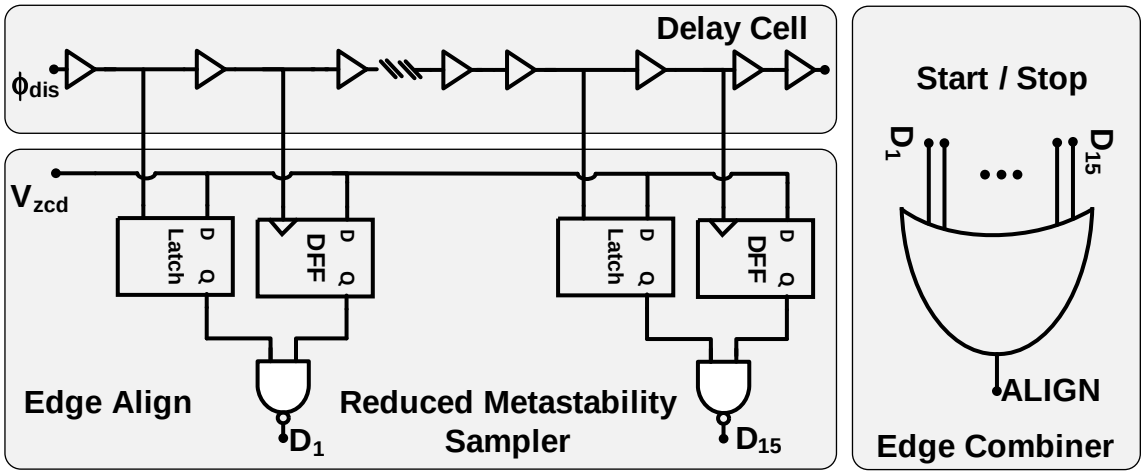


Figure 5.8: Reduced Metastability Time-to-Digital Converter

5.4.5 Summary

The 12-bit hybrid pipeline was built in 1P9M 65nm CMOS process. Simulated at 100 MHz clock frequency, the ADC in fabrication achieves 66 dB SNDR/ 80 dB SFDR from

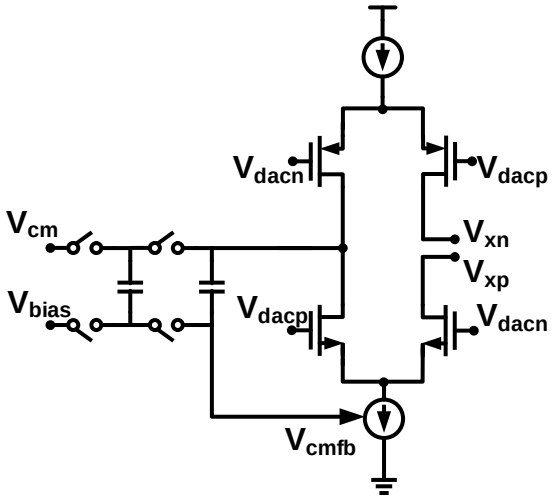


Figure 5.9: Discharging Current Source

a 1 V supply. The hybrid pipeline ADC occupies 1 sq. mm, occupies 1 sq. mm and has a figure of merit of 40 fJ/C-S. The layout of the hybrid pipeline ADC is shown in Fig. 5.10, output spectrum of the ADC with input at -14 dB is shown in Fig. 5.12 and the performance summary is shown in Fig. 5.13.

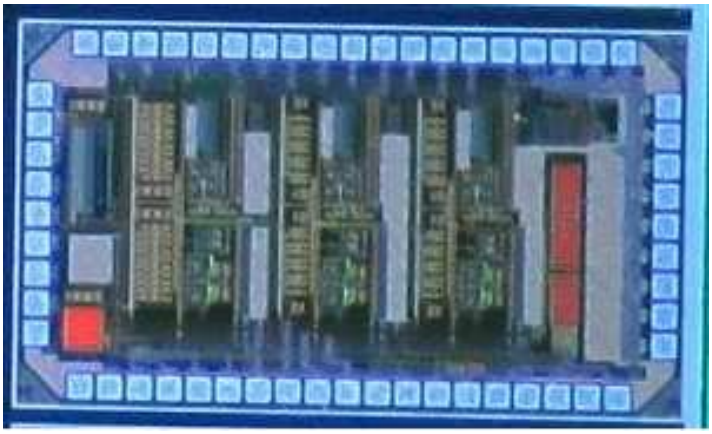


Figure 5.10: Die Micrograph

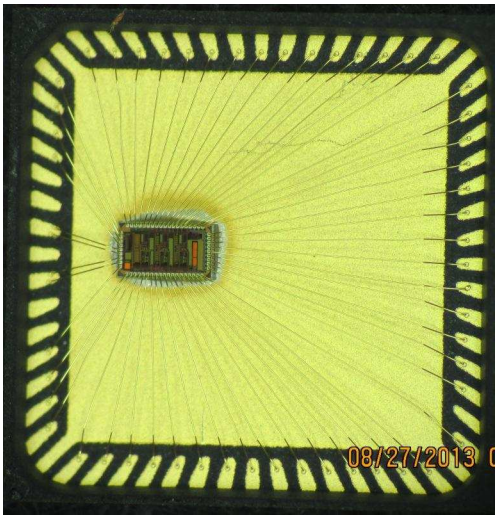


Figure 5.11: Die Micrograph

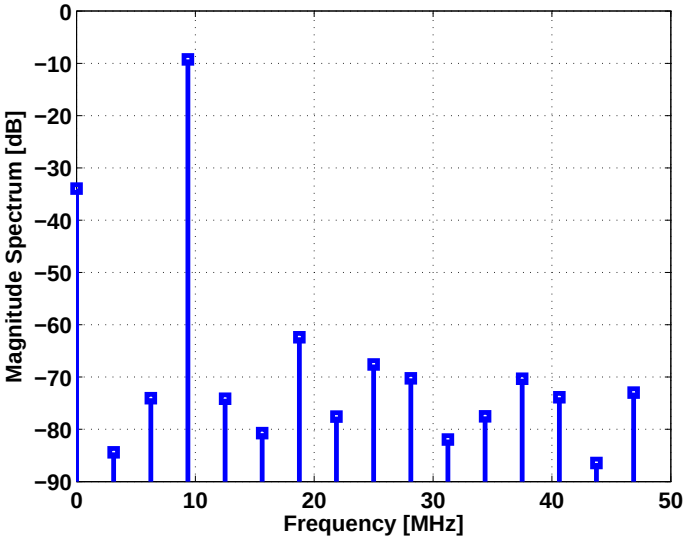


Figure 5.12: Hybrid Pipeline ADC Spectrum, SNDR = 55 dB at -10 dB input

Parameter	Parameter
Technology	1P9M 65nm
Supply Voltage	1 V
Sampling Rate	100 MHz
Input Voltage Range	1.6 V_{p-p}
SNDR/SFDR dB	66 dB / 80 dB
Power	8 mW
Active Area	1 sq. mm
FoM	40 fJ/CS
Resolution	13 bit

Figure 5.13: Performance Summary

Chapter 6. Conclusion

6.1 Summary

Analog to digital converter design trade offs are identified and classified to provide sufficient understanding in choosing either an architectural technique or a circuit technique to improve energy and area efficiency. To this end, two calibration methods were proposed. Deterministic calibration technique to measure and correct VCO non-linearity and Multi-path ADC with skip/fill calibration and majority voting to detect and correct bit-error rate in ADCs. A unified gain enhancement model was proposed to understand the design of high performance amplifiers. Four gain enhanced amplifier techniques were proposed to improve the power efficiency. They are class A+ amplifier, asynchronous CLS technique, replicated parallel gain enhancement technique and dynamic RPGE technique.

Replicated parallel gain enhancement technique and dynamic RPGE were implemented in a pipeline ADC to demonstrate the feasibility. A prototype pipeline ADC built in 0.18 μm, 1P4M process achieves 75 dB SNDR, 90 dB SFDR, -87 dB THD at 20 MS/s from a 1.3 V supply. The pipeline ADC consumes 5.9 mW and achieves a figure of merit of 65 fJ/CS. This ADC is one of very few ADCs in the past 16 years to achieve calibration free, above 70 dB resolution and low power consumption through circuit design. An improved dynamic RPGE amplifier has been implemented in 0.18μm process to demonstrate high resolution and wide bandwidth with improved power efficiency. Extracted simulations of the chip in fabrication indicates 74 dB SNDR, 88 dB SFDR, 85 dB THD at 33 MS/s from a 1.3 V supply. The pipeline ADC consumes 6.6 mW and achieves a figure of merit close to 50 fJ/CS.

A combination of architecture, calibration and circuit technique is utilized to build a hybrid voltage-time pipeline ADC. The TDC is used as a replacement to the flash ADC and capacitor DAC in a conventional pipeline ADC. The simulated/extracted performance of the chip is 11 bit, 100 MHz in 65nm process while consuming approximately 8 mA from 1 V supply.

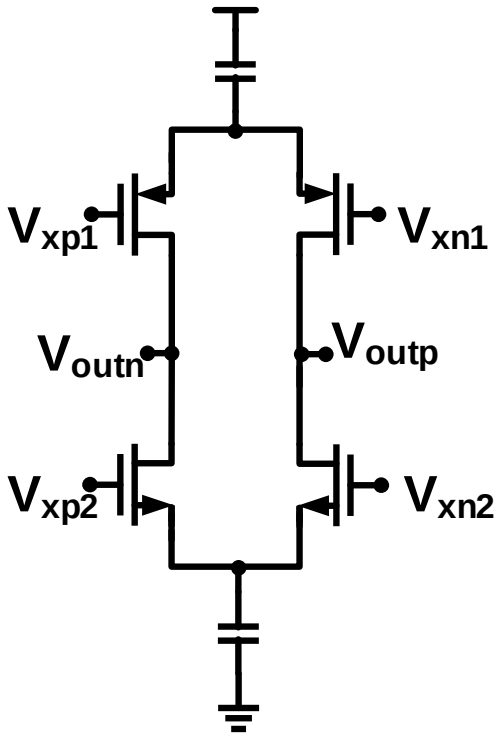


Figure 6.1: Generic Dynamic Amplifier

6.2 Future Work

6.2.1 Dynamic Amplifier

Dynamic amplifiers provide time varying bandwidth and increased DC gain while consuming dynamic power [73]. The dynamic amplifiers, as shown in Fig. 6.1 can be used in combination with the RPGE technique to create a highly efficient wide bandwidth, large DC gain amplifier which can be used either as an amplifier or an integrator to build a pipeline ADC or a delta-sigma ADC respectively.

6.2.2 TDC Calibration

The TDC replacement for the flash ADC and capacitor DAC is limited by the matching accuracy provided by the process and is generally limited to 6-7 bits. In order to build a

14-bit pipeline ADC with the second stage as time domain MDAC, the resolution of the TDC must be close to 10-bits. This architecture will lead a power efficient high resolution, high speed ADC. To enable a 10-bit time domain MDAC, calibration techniques can be used to correct for the mismatch error. One of the calibration techniques such as split ADC or Deterministic calibration or blind calibration is a suitable solution as shown in Fig..

6.2.3 Evaluation of ADC Non-Linearity using Reciprocity Theorem

Understanding component mismatch effects on the performance limitation requires Monte-Carlo simulations and is time consuming. Reciprocity theorem can be used to analyze R-2R DACs, binary weighted capacitor DACs, C-2C DACs, current steering DAC with the creation of adjoint network. This leads to a rapid evaluation and intuitive understanding of the mismatch limitation of each component towards the overall linearity for a DAC under consideration. As an example, reciprocity theorem is explained with an example for R-2R ladder where it is not straightforward to analyze the mismatch effect due to each resistor in the resistor ladder.

$$\begin{aligned} V_{out} &= \frac{R_2}{R_1+R_2}V_1 \\ \Delta V_{out} &= \frac{\partial V_{out}}{R_1}\Delta R_1 + \frac{\partial V_{out}}{R_2}\Delta R_2 \\ \frac{\partial V_{out}}{\partial R_1} &= -\frac{R_2}{(R_1+R_2)^2}, \frac{\partial V_{out}}{\partial R_2} = \frac{R_1}{(R_1+R_2)^2} \end{aligned}$$

6.2.4 Differential Tellegen's Theorem

$$\sum_{k=1}^{N} v_k j'_k = \mathbf{v^T j'}, \sum_{k=1}^{N} v'_k j_k = \mathbf{v'^T j} \tag{6.1}$$

Where v_k, j_k and v'_k, j'_k are the branch voltages and currents of a network N and $\hat{N}$ respectively. If network N changes by a small amount Δ, applying Tellegen's theorem

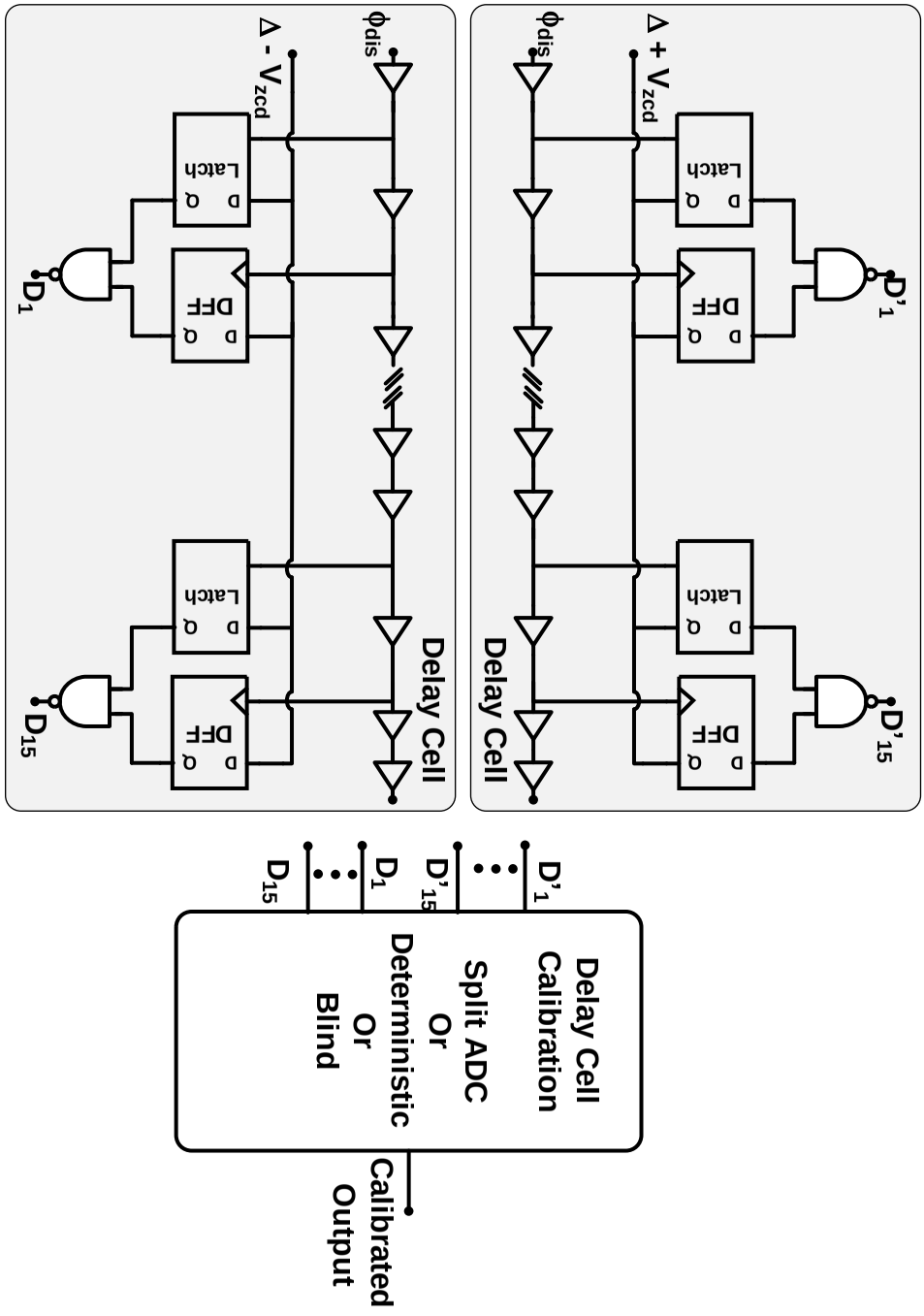


Figure 6.2: TDC Calibration

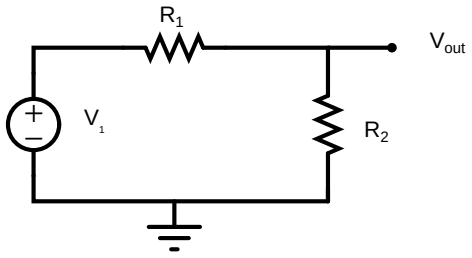


Figure 6.3: Resistor Divider

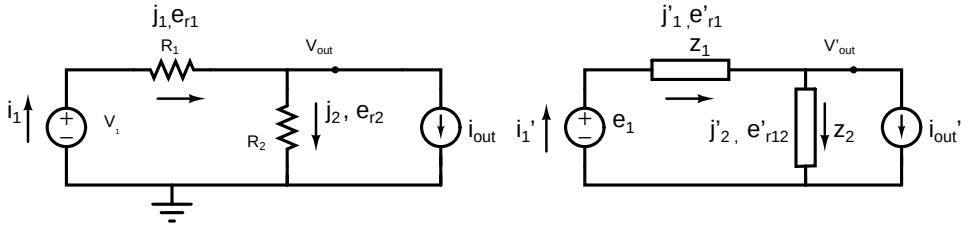


Figure 6.4: Adjoint-Example

to the above network N_Δ

$$(v+\Delta V)^T\hat{j} = 0, \hat{v}^T(j+\Delta j) = 0.$$
$$(v+\Delta V)^T\hat{j} - \hat{v}^T(j+\Delta j) = 0$$
$$\Rightarrow \Delta V^T\hat{j} - \hat{v}^T\Delta j = 0$$

Applying Differential Tellegen's Theorem,

$$\sum\left(\hat{j}\Delta v - \Delta j\hat{v}\right) = 0$$
$$(i_1'\Delta v_1 - e_1\Delta i_1) + (j_1'\Delta e_{r1} - e_{r1}'\Delta j_1)$$
$$+(j_2'\Delta e_{r2} - e_{r2}'\Delta j_2) + (i_{out}'\Delta v_{out} - v_{out}'\Delta i_{out}) = 0$$

To find sensitivity of output voltage to resistor variation,

$$e_{r1} + \Delta e_{r1} = (R_1 + \Delta R_1)(j_1 + \Delta j_1)$$
$$\Delta e_{r1} = R_1\Delta j_1 + \Delta R_1 j_1 + \Delta R_1\Delta j_1$$

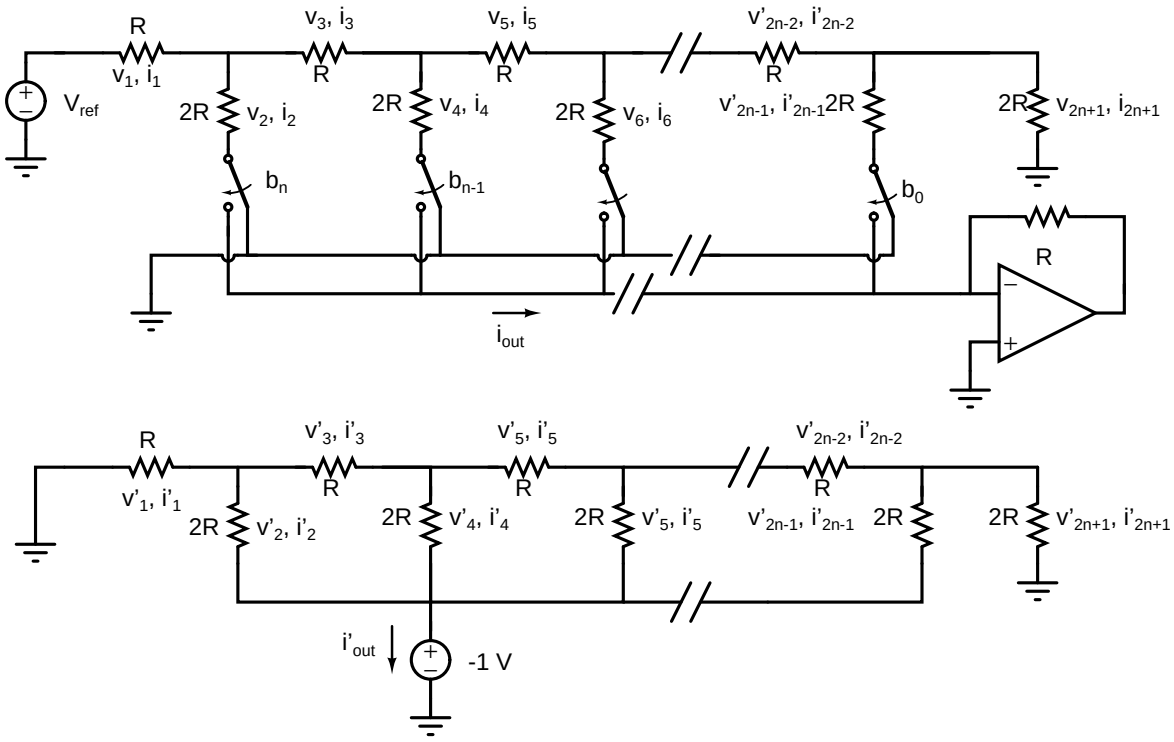


Figure 6.5: R-2R-Example

Neglecting higher order terms, substituting this in the second expression of differential Tellegen's theorem,

$$j_1'\Delta e_{r1} - e_{r1}'\Delta j_1 = j_1 j_1'\Delta R_1 + (j_1' R_1 - e_{r1}')\Delta j_1$$

Observation: Choose the adjoint network such that $j_1' R_1 - e_{r1}' = 0$. For resistor networks, the adjoint is same as the network with de-energized sources

The sensitivity of the output current is a sum of sensitivities of individual resistors. The sensitivities of individual resistors is $j.\hat{j}$, where j and $\hat{j}$ are the branch currents in orginal network and adjoint network. The branch currents in the original network is I,I/2,I/4 and so on. The branch currents of the adjoint network is found as follows. The

nodal equation for adjoint network is given by,

$$\begin{bmatrix} 5 & -2 & 0 & \dots & \dots \\ -2 & 5 & -2 & \dots & \dots \\ 0 & -2 & 5 & -2 & \dots \\ \dots & \dots & \dots & \dots & \dots \\ \dots & \dots & -2 & 5 & -2 \\ 0 & \dots & \dots & -2 & 4 \end{bmatrix} . \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ \dots \\ v_{2n} \\ v_{2n+1} \end{bmatrix} = \begin{bmatrix} -1 \\ -1 \\ -1 \\ \dots \\ -1 \\ -1 \end{bmatrix} \tag{6.2}$$

$$\Delta i_{out} = -\sum_{i}^{2n+1} (j_i \hat{j}_i) \frac{\Delta R_i}{R_i}$$

APPENDICES

Appendix A. Multi-Path ADC Technique

Signal to noise ratio for an ADC with single event Gaussian random noise source is derived as follows. Fig. 2.13 shows the model for the ADC with a single event noise source and quantization noise source. The quantization noise depends on the resolution of the ADC and is uniform. SEE is modeled as a Gaussian noise distribution with standard deviation of σ. Eq. 12 is used to derive the signal to noise ratio with SEE. Where, Vrms is the signal energy and E(X2) is the energy of the random signal X. Eq. 12 can be applied to the quantization noise and Gaussian single event noise source as shown in (12). However, the single event happens only Nrep times in a given observation window, Nwindow. Therefore, the noise energy is scaled by Nrep/Nwindow. Eq. 13 shows the signal to noise ratio for Gaussian and the familiar quantization noise.

$$\mathrm{SNR} = \frac{\mathrm{V}^2_{\mathrm{rms,signal}}}{\mathrm{E}(\mathrm{X}^2)}, \mathrm{E}(\mathrm{X}^2_{\mathrm{uniform}}) = \frac{\Delta^2}{12}, \mathrm{E}(\mathrm{X}^2_{\mathrm{gaussian}}) = \sigma^2 \tag{A.1}$$

$$\begin{aligned} \mathrm{SNR}_{\mathrm{see}} &= \frac{\mathrm{V}^2_{\mathrm{rms}}.\mathrm{N}_{\mathrm{window}}}{\sigma^2_{\mathrm{see}}\mathrm{N}_{\mathrm{rep}}}, \mathrm{SNR}_{\mathrm{quant}} = \frac{\mathrm{V}^2_{\mathrm{rms}}.12}{\Delta^2} \\ \mathrm{SNR}_{\mathrm{combined}} &= \frac{\mathrm{V}^2_{\mathrm{rms}}}{\sigma^2_{\mathrm{see}}.\mathrm{N}_{\mathrm{rep}}/\mathrm{N}_{\mathrm{window}} + \Delta^2/12} \end{aligned} \tag{A.2}$$

Appendix B. Limitations of SEE Model

SEE is modeled as a noise current source shown in Eq. B.1 as shown in Fig. B.1. Where, Q_{see} is the ion charge transferred by the energy particle, α, β, τ are the constants derived from the device model. The sampled voltage on the capacitor C_s is shown in Eq. B.1. Where, i_{see} represents the model for SEE current source, Q_{see} is the random charge transferred from the energy particle, α, β, τ are the constants derived from the device model, C_s is the sampling capacitor and T_s is the sampling rate.

$$\mathrm{i_{see}}=\frac{\mathrm{Q_{see}}}{\tau}\left(\exp(-\alpha.\mathrm{t}/\tau)-\exp(-\beta.\mathrm{t}/\tau)\right) \tag{B.1}$$

$$\mathrm{V_{th}}[\mathrm{nT}_s+0.5\mathrm{T}_s]=\mathrm{V_{in}}[\mathrm{nT}_s+0.5\mathrm{T_s}]+\frac{1}{\mathrm{C_s}}.\int_0^{0.5\mathrm{T_s}}\mathrm{i_{see}}.\mathrm{dt} \tag{B.2}$$

$$\mathrm{V_{see}}\approx\gamma.\frac{\mathrm{Q_{see}}}{\mathrm{C_s}} \tag{B.3}$$

However, SEE current source model is derived from a packet of charge delivered by the energy particle. The integral shown in Eq. B.2 describes the amount of charge transferred to the sampling capacitor. In general, the time constant of the modeled is much smaller compared the sampling-rate used for the system and can be simplified to Eq. B.3. Where, γ is proportionality constant relating the packet of charge delivered by the energy particle and the voltage change V_{see}. As shown in Fig. B.2, this current

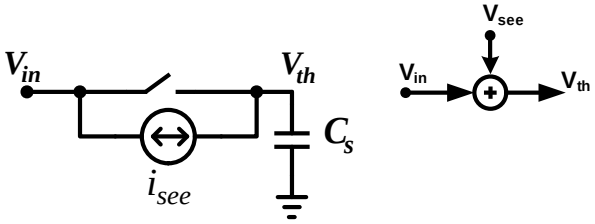


Figure B.1: Sample and Hold with SEE Current Source

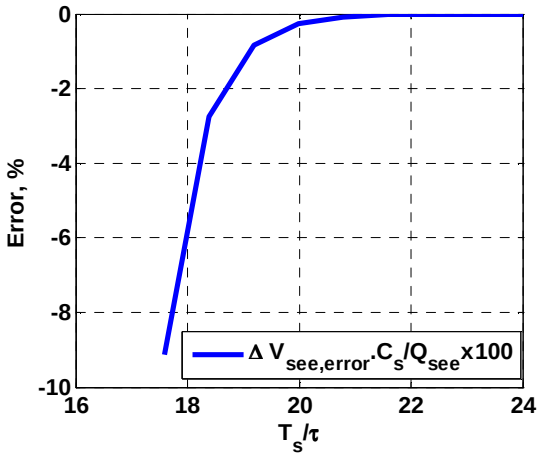


Figure B.2: SEE Model Accuracy

source charges a capacitor for a given sampling period. The voltage change produced by this current source is directly related to the ion charge transferred by the energy particle and this can be derived as shown in Eq. B.4, Eq. B.5 and Eq. B.6.

$$\mathrm{V_{see}}=\frac{1}{\mathrm{C_s}}.\int_0^{0.5\mathrm{T_s}}\mathrm{i_{see}}.\mathrm{dt} \tag{B.4}$$

$$=\frac{\mathrm{Q_{see}}}{\mathrm{C_s}}\frac{\beta-\alpha}{\alpha\beta}+\frac{\mathrm{Q_{see}}}{\mathrm{C_s}\tau}\left(\frac{1}{\beta}\exp(-\beta.0.5\mathrm{T_s}/\tau)-\frac{1}{\alpha}\exp(-\alpha.0.5\mathrm{T_s}/\tau)\right)$$

$$\mathrm{V_{see}}=\gamma.\frac{\mathrm{Q_{see}}}{\mathrm{C_s}}+\Delta\mathrm{V_{see,error}},\gamma=\frac{\beta-\alpha}{\beta.\alpha} \tag{B.5}$$

$$\frac{\Delta\mathrm{V_{see,error}}}{\mathrm{Q_{see}/C_s}}=\frac{1}{\tau}\left(\frac{1}{\beta}\exp(-\beta.0.5\mathrm{T_s}/\tau)-\frac{1}{\alpha}\exp(-\alpha.0.5\mathrm{T_s}/\tau)\right) \tag{B.6}$$

α, β, τ are derived from a specific device under consideration. α, β, τ used for the following discussion are 3, 4 and 12.5 ps respectively. Fig. B.2 shows the error percentage as a function of T_s/τ. It can be observed that for ratios of T_s/τ greater than 20, the error in the approximation of Eq. B.6 is less than 0.25%. In our discussion, we had assumed that the current pulse is ON for the entire sampling period ($0.5T_s$). However, the above discussion indicates that within twenty time constants of the current pulse, 99.75% of

the charge is transferred to the capacitor. In other words, if the sampling period ($0.5T_s$) is larger than 20 time constants, the modeling error is less than 0.25%.

Bibliography

[1] G. Candy, J.; Temes, *Oversampling Delta-Sigma Data Converters:Theory, Design, and Simulation*. Wiley-IEEE Press, 1997.

[2] J. Dallet, Dominique; Machado da Silva, *Dynamic Characterisation of Analogue-to-Digital Converters*, 2005.

[3] M. Gustavsson, J. J. Wikner, and N. Tan, *CMOS Data Converters for Communications*. Springer, 2000.

[4] F. Maloberti, *Data Converters*. Springer, 2007.

[5] G. Manganaro, *Advanced Data Converters*. Cambridge, 2012.

[6] G. Norsworthy, S.; Schreier, R.; Temes, *Delta-Sigma Data Converters:Theory, Design, and Simulation*. Wiley-IEEE Press, 1997.

[7] B. Razavi, *Principles of Data Conversion System Design*. Wiley-IEEE Press, 1995.

[8] Y. Chiu, C. Tsang, B. Nikolic, and P. Gray, "Least Mean Square Adaptive Digital Background Calibration of Pipelined Analog-to-Digital Converters," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 51, no. 1, pp. 38–46, Jan. 2004.

[9] J. Li and U. Moon, "Background calibration techniques for multistage pipelined ADCs with digital redundancy," *... II: Analog and Digital Signal Processing, IEEE ...*, vol. 50, no. 9, pp. 531–538, 2003.

[10] J. McNeill, M. Coln, and B. Larivee, ""Split ADC" architecture for deterministic digital background calibration of a 16-bit 1-MS/s ADC," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2437–2445, Dec. 2005.

[11] M. Z. Straayer and M. H. Perrott, "A 12-Bit, 10-MHz Bandwidth, Continuous-Time Sigma Delta ADC With a 5-Bit, 950-MS/s VCO-Based Quantizer," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, Apr. 2008.

[12] Jaewook Kim and SeongHwan Cho, "A Time-Based Analog-to-Digital Converter Using a Multi-Phase Voltage-Controlled Oscillator," in *2006 IEEE International Symposium on Circuits and Systems*. IEEE, 2006, pp. 3934–3937.

[13] Jaewook Kim, Tae-Kwang Jang, Young-Gyu Yoon, and SeongHwan Cho, "Analysis and Design of Voltage-Controlled Oscillator Based Analog-to-Digital Converter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 1, pp. 18–30, Jan. 2010.

[14] a. L. Sternberg, L. W. Massengill, M. Hale, and B. Blalock, "Single-Event Sensitivity and Hardening of a Pipelined Analog-to-Digital Converter," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3532–3538, Dec. 2006.

[15] P. Fleming and B. Olson, "Design technique for mitigation of soft errors in differential switched-capacitor circuits," *Circuits and Systems ...*, vol. 55, no. 9, pp. 838–842, 2008.

[16] J. Kauppila, "Single event simulation methodology for analog/mixed signal design hardening," *Nuclear Science, ...*, vol. 51, no. 6, pp. 3603–3608, 2004.

[17] S. Buchner and T. Meehan, "Characterization of single-event upsets in a flash analog-to-digital converter (AD9058)," *Nuclear Science, ...*, vol. 47, no. 6, pp. 2358–2364, 2000.

[18] B. Olson and W. Holman, "Evaluation of radiation-hardened design techniques using frequency domain analysis," *... IEEE Transactions on*, vol. 55, no. 6, pp. 2957–2961, 2008.

[19] D. Mavis and P. Eaton, "SEU and SET modeling and mitigation in deep submicron technologies," *Reliability physics symposium, 2007. ...*, pp. 293–305, 2007.

[20] S. E. Armstrong, R. W. Blaine, W. T. Holman, and L. W. Massengill, "Single-event vulnerability of mixed-signal circuit interfaces," *2011 12th European Conference on Radiation and Its Effects on Components and Systems*, pp. 485–488, Sep. 2011.

[21] Y. Boulghassoul, "Applicability of circuit macromodeling to analog single-event transient analysis," *Nuclear Science, IEEE ...*, vol. 50, no. 6, pp. 2119–2125, 2003.

[22] R. Gregorian and G. C. Temes, *Analog MOS integrated circuits for signal processing*. Wiley, 1986.

[23] D. Fulkerson and E. Vogt, "Prediction of SOI single-event effects using a simple physics-based SPICE model," *IEEE Transactions on Nuclear Science*, vol. 52, no. 6, pp. 2168–2174, Dec. 2005.

[24] Un-Ku Moon and Bang-Sup Song, "Background digital calibration techniques for pipelined ADCs," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, no. 2, pp. 102–109, 1997.

[25] J. Eklund and C. Svensson, "Influence of metastability errors on SNR in successive-approximation A/D converters," *Analog Integrated Circuits and Signal ...*, vol. 1, pp. 191–198, 2001.

[26] T. Sundström, C. Svensson, and A. Alvandpour, "A 2.4 GS/s, Single-Channel, 31.3 dB SNDR at Nyquist, Pipeline ADC in 65 nm CMOS," *Solid-State Circuits, ...*, vol. 46, no. 7, pp. 1575–1584, 2011.

[27] J. Guerber, H. Venkatram, M. Gande, A. Waters, and U. Moon, "A 10-b ternary SAR ADC with quantization time information utilization," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 11, pp. 2604–2613, 2012.

[28] T. Matsuura and T. Nara, "A 240-Mbps, 1-W CMOS EPRML read-channel LSI chip using an interleaved subranging pipeline A/D converter," *Solid-State Circuits, ...*, vol. 33, no. 11, pp. 1840–1850, 1998.

[29] S. Guhados, P. Hurst, and S. Lewis, "A Pipelined ADC With Metastability Error Rate¡ 1015 Errors/Sample," *IEEE journal of solid-state circuits*, vol. 47, no. 9, pp. 2119–2128, 2012.

[30] J. McCreary and P. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques. I," *IEEE Journal of Solid-State Circuits*, 1975.

[31] R. Suarez, P. Gray, and D. Hodges, "All-MOS charge-redistribution analog-to-digital conversion techniques. II," *IEEE Journal of Solid-State Circuits*, no. 6, 1975.

[32] H. J. Schouwenaars, "A monolithic 14 bit A/D converter," *IEEE Journal of Solid-State Circuits*, no. 6, pp. 1112–1117, 1982.

[33] H. Lee, D. Hodges, and P. Gray, "A self-calibrating 15 bit CMOS A/D converter," *IEEE Journal of Solid-State Circuits*, no. 6, 1984.

[34] A. Rossi and G. Fucili, "Nonredundant successive approximation register for A/D converters," *Electronics letters*, vol. 32, no. 12, pp. 1055–1057, 1996.

[35] C. Hammerschmied and Q. Huang, "Design and implementation of an untrimmed MOSFET-only 10-bit A/D converter with-79-dB THD," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 8, pp. 1148–1157, 1998.

[36] S. Mortezapour and E. Lee, "A 1-V, 8-bit successive approximation ADC in standard CMOS process," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 4, pp. 642–646, Apr. 2000.

[37] F. Kuttner, "A 1.2 V 10b 20MSample/s non-binary successive approximation ADC in 0.13μm CMOS," in *Solid-State Circuits Conference, 2002. Digest of ...*, 2002, pp. 14–15.

[38] B. Ginsburg and A. Chandrakasan, "An Energy-Efficient Charge Recycling Approach for a SAR Converter With Capacitive DAC," in *2005 IEEE International Symposium on Circuits and Systems*. Ieee, 2005, pp. 184–187.

[39] S. Michael and R. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-m CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2669–2680, 2006.

[40] D. Aksin, M. a. Al-Shyoukh, and F. Maloberti, "An 11 Bit Sub-Ranging SAR ADC with Input Signal Range of Twice Supply Voltage," in *2007 IEEE International Symposium on Circuits and Systems*. Ieee, May 2007, pp. 1717–1720.

[41] Y.-k. Chang, C.-s. Wang, and C.-k. Wang, "A 8-bit 500-KS/s low power SAR ADC for bio-medical applications," in *2007 IEEE Asian Solid-State Circuits Conference*, vol. 2. Ieee, Nov. 2007, pp. 228–231.

[42] J. Craninckx and G. V. D. Plas, "A 65fJ/conversion-step 0-to-50MS/s 0-to-0.7 mW 9b charge-sharing SAR ADC in 90nm digital CMOS," in *Solid-State Circuits Conference, ...*, 2007, pp. 246–248.

[43] B. Ginsburg and A. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS with split capacitor array DAC," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 4, pp. 739–747, 2007.

[44] M. V. Elzakker and E. V. Tuijl, "A 1.9 μW 4.4 fJ/conversion-step 10b 1MS/s charge-redistribution ADC," in *Solid-State Circuits ...*, 2008, pp. 244–246.

[45] V. Giannini and P. Nuzzo, "An 820μW 9b 40MS/s noise-tolerant dynamic-SAR ADC in 90nm digital CMOS," in *Solid-State Circuits ...*, 2008, pp. 238–240.

[46] C. Liu and S. Chang, "A 0.92 mW 10-bit 50-MS/s SAR ADC in 0.13 μm CMOS process," in *VLSI Circuits, 2009 ...*, 2009, pp. 236–237.

[47] J. Guerber, "Time and Statistical Information Utilization in High Efficiency Sub-Micron CMOS Successive Approximation Analog to Digital Converters," Ph.D. dissertation, Oregon State University, 2012.

[48] R. Kline, "Harold Black and the negative-feedback amplifier," *IEEE Control Systems*, vol. 13, no. 4, pp. 82–85, Aug. 1993.

[49] H. Black, "Inventing the negative feedback amplifier: Six years of persistent search helped the author conceive the idea in a flash aboard the old Lackawanna Ferry," pp. 55–60, 1977.

[50] S. Rosenstark, *Feedback amplifier principles*. Macmillan Pub. Co., 1986.

[51] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. Wiley, 2009.

[52] B. Razavi, *Design of Analog Cmos Integrated Circuits*. McGraw-Hill Higher Education, 2001, vol. 2.

[53] T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*. Wiley, 2011.

[54] A. B. Grebene, *Analog integrated circuits*. Wiley-IEEE Press, 1978.

[55] R. G. Meyer, *Integrated-Circuit Operational Amplifiers*. Wiley-IEEE Press, 1978.

[56] P. Yu, "A high-swing 2-V CMOS operational amplifier with replica-amp gain enhancement," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 12, pp. 1265–1272, 1993.

[57] S. Pavan and P. Sankar, "Power Reduction in Continuous-Time Delta-Sigma Modulators Using the Assisted Opamp Technique," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 7, pp. 1365–1379, Jul. 2010.

[58] K. Nagaraj and K. Singhal, "Reduction of finite-gain effect in switched-capacitor filters," *Electronics ...*, vol. 21, no. 15, pp. 3–4, 1985.

[59] K. Haug, F. Maloberti, and G. Temes, "Switched-capacitor integrators with low finite-gain sensitivity," *Electronics Letters*, vol. 21, no. 24, pp. 2–3, 1985.

[60] C. Enz, "High Precision CMOS Micropower Amplifiers," Ph.D. dissertation, 1989.

[61] Y. Huang, P. Ferguson, and G. Temes, "Reduced nonlinear distortion in circuits with correlated double sampling," *Circuits and Systems II: ...*, vol. 44, no. 7, pp. 593–597, 1997.

[62] H. Yoshizawa, Y. Huang, and G. Temes, "Improved SC amplifiers with low sensitivity to op-amp imperfections," *Electronics Letters*, vol. 33, no. 5, pp. 1996–1997, 1997.

[63] H. Yoshizawa and G. C. Temes, "Switched-capacitor track-and-hold amplifier with low sensitivity to op-amp imperfections," *Analog Integrated Circuits and Signal Processing*, vol. 48, no. 3, pp. 267–270, May 2006.

[64] ——, "Predictive Switched-Capacitor Track-and-Hold Amplifier with Improved Linearity," *2007 IEEE International Symposium on Circuits and Systems*, no. 1, pp. 233–236, May 2007.

[65] O. Rajaee, N. Maghari, and U.-K. Moon, "Time-Shifted CDS Enhancement of Comparator-Based MDAC for Pipelined ADC Applications," *2007 14th IEEE International Conference on Electronics, Circuits and Systems*, pp. 210–213, Dec. 2007.

[66] T. Musah, "Low Power Design Techniques for Analog-to-Digital Converters in Submicron," Ph.D. dissertation, 2010.

[67] B. Gregoire and U.-k. Moon, "An Over-60 dB True Rail-to-Rail Performance Using Correlated Level Shifting and an Opamp With Only 30 dB Loop Gain," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2620–2630, 2008.

[68] L. Brooks and H. Lee, "A 12b, 50 MS/s, Fully Differential Zero-Crossing Based Pipelined ADC," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. dec, pp. 3329–3343, Dec. 2009.

[69] M. Schlarmann, S. Malik, and R. Geiger, "Positive feedback gain-enhancement techniques for amplifier design," in *2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353)*, vol. 2. IEEE, 2002, pp. II–37–II–40.

[70] Y. Shimizu, S. Murayama, K. Kudoh, H. Yatsuda, and A. Ogawa, "A 30mW 12b 40MS/s subranging ADC with a high-gain offset-canceling positive-feedback amplifier in 90nm digital CMOS," in *2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers*. IEEE, 2006.

[71] H. Venkatram, B. Hershberg, and U.-K. Moon, "Asynchronous CLS for Zero Crossing based Circuits," in *2010 17th IEEE International Conference on Electronics, Circuits and Systems*. IEEE, Dec. 2010, pp. 1025–1028.

[72] H. Venkatram, T. Oh, J. Guerber, and U.-K. Moon, "Class A+ amplifier with controlled positive feedback for discrete-time signal processing circuits," in *2012 IEEE International Symposium on Circuits and Systems*. IEEE, May 2012, pp. 428–431.

[73] B. Hosticka, "Dynamic CMOS amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 15, no. 5, pp. 881–886, Oct. 1980.

[74] M. Degrauwe and J. Rijmenants, "Adaptive biasing CMOS amplifiers," *Solid-State Circuits, ...*, no. 3, pp. 522–528, 1982.

[75] T. Oh, "Power Efficient Analog-to-Digital Converters using Both Voltage and Time Domain Information," Ph.D. dissertation, Oregon State University, 2013.

[76] M. Gande, "Design Techniques for Time Based Data Converters," Ph.D. dissertation, Oregon State University, 2013.