AN ABSTRACT OF THE DISSERTATION OF

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Un-Ku Moon

Modern day CMOS processes are characterized by voltage scaling and geometry scaling. Geometry scaling helps reduce gate delays, thereby aiding in the design of data converters which use time based processing. Another artifact of geometry scaling is the increase in complexity of digital circuitry available on traditional analog ICs, as digital signal processing could be used to compensate for analog inaccuracies. Calibration assisted analog-to-digital converters(ADCs), software defined radio, digital phase locked loops, etc... have all gained from improvements in the digital processing available on chip. This thesis focusses on data converters which utilize the above features of modern day CMOS processes.

The thesis is primarily divided into two parts. The first part focuses on a technique to convert the time information into a digital word. A high resolution time-to-digital converter (TDC) architecture is proposed which combines the principles of noise-shaping integrating quantizer and charge-pump to build a third-order delta-sigma TDC using a dedicated feedback DAC. Fabricated in a 0.13μm CMOS process, the prototype TDC achieves better than 71dB DR for a 2.8MHz signal bandwidth.

The second part of the thesis proposes a blind digital calibration technique to remove non-linearity in any traditional ADC architectures. The proposed technique uses the concept of downsampling and orthogonality of sinusoidal waves to estimate the harmonic distortion in ADCs and can be used to calibrate multiple harmonics simultaneously. As a proof of concept, the algorithm is demonstrated on a first-order ring oscillator based delta-sigma ADC, whose performance is harmonic distortion limited. Built in 0.13μm CMOS process, the algorithm improves the SNDR of the ADC by 39dB while improving SFDR by 45 dB.

Design Techniques for Time Based Data Converters

by

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I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

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Manideep Gande, Author

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

LIST OF TABLES

DESIGN TECHNIQUES FOR TIME BASED DATA CONVERTERS

CHAPTER 1. INTRODUCTION

1.1 Introduction

Figure 1.1: Role of data converters in everyday life.

In this digital era, communication, health, instrumentation and space electronics enhance our accessibility and information exchange. However, this information exchange happens through the interface between analog world and digital world. Data Converters are imperative for the exchange of information and help in interfacing our communication with the digital world. Analog-to-digital converters and Time-to-digital converters are the two major data converter architectures which steer forward this digital evolution.

Portable, efficient and high performance systems are the nature of today's digital evolution. To this end, some of the latest technology trends are shown in

Fig. 1.2. WiGig, 400 Gbps optical links, highly sensitive physics experiments have created an increasing appetite for data converters that are capable of operating on a wider bandwidth range, while being able to provide high resolution and high linearity, while consuming low power.

Figure 1.2: Application of data converters.

1.2 Motivation

If it can be done in CMOS, it will be done in CMOS.

-Arun Natarajan

The CMOS backend process is the most commonly used digital electronics platform. The reason being near zero incremental device cost/ easy digital-RF integration and the very fact that millions of transistors are available, thereby making digital calibration a viable option. Also, scaling is an integral part of CMOS technology as it helps pack in more transistors, while reducing digital power consumption. However, scaling in deep sub-micron nodes exhibit the general trend

of reduced intrinsic gain and smaller gate delays. This trend is shown in Fig. 1.3. Although the trend is a sign of trouble for conventional voltage based signal processing, it works in favor of data converters that use time based information or are more digital in nature.
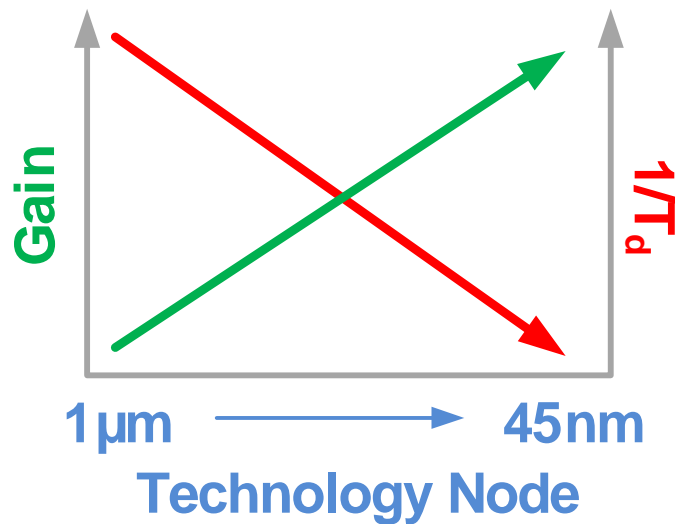
Figure 1.3: Trends in CMOS scaling.

Deep sub-micron CMOS technology provides the user with benefits of reduced gate delay and faster processes, at the cost of reduced voltage headroom and reduced intrinsic gain. Therefore, it is imperative that one looks into alternative design methodologies which take the advantages of the modern processes and make data converters which use time domain signal processing or build data converters which are more digital in nature. This thesis presents two new data converter architectures which utilize the advantages of reduced gate delay available with modern CMOS process. The proposed architectures are also more digital in nature, thereby taking advantage of scaling in CMOS processes.

1.3 Thesis Organization

Chapter 2 introduces some of the basics of Time-to-Digital converters(TDCs), while also giving a peek at attempts made by in the past into improving this field. The merits and demerits of some of the existing architectures are discussed in this chapter.

In Chapter 3, a novel TDC architecture is proposed by combining the properties of noise-shaping quantizer and charge-pump. This proposed architecture makes use of a dedicated feedback path in a TDC, thereby enabling the possibility of building higher order $\Delta\Sigma$ TDCs. The design aspects of the $\Delta\Sigma$ TDC are discussed along with a few important design considerations. This chapter concludes by presenting the measured results of the proposed $\Delta\Sigma$ TDC which is built in 0.13 μm CMOS technology.

In Chapter 4, the effects of nonlinearity on an ADC are studied. One of the many possible ways of combating nonlinearity in ADCs is to use "Digital Calibration". In this chapter, some of the existing nonlinearity calibration algorithms for ADCs are studied, and their shortcomings are discussed.

In Chapter 5, a novel digital calibration algorithm to reduce nonlinearity in ADCs is proposed. The calibration algorithm makes use of downsampling and orthogonality of sinusoid waves to calibrate for nonlinearity in ADCs. This chapter also proves the effectiveness of the proposed algorithm by showing the performance improvement of a VCO based $\Delta\Sigma$ ADC, which are known to be notoriously nonlinear. The VCO based $\Delta\Sigma$ ADC is also built in 0.13 μm CMOS technology.

Chapter 6 summarizes the work presented in this thesis.

CHAPTER 2. BACKGROUND ON TIME TO DIGITAL CONVERTERS

2.1 Introduction

Historically, the basic motivation to synchronize our activities has been one of the main motivations to measure time. Today, measurements of mean lifetime of nuclear particles, particle identification, time-of-flight, timing jitter calculations, instrumentation and communication circuitry etc... require time measurement that are much more precise [1, 2, 3, 4, 5]. Time-to-digital converters (TDCs), as the name suggests, are used to quantize the time interval between two events. Figure 2.1 shows the basic operation of a TDC [6].
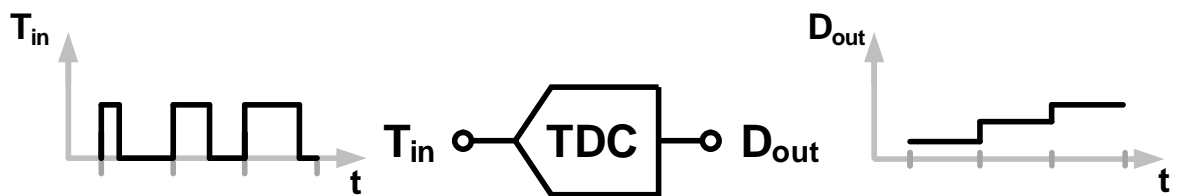
Figure 2.1: Concept of time to digital converter

The input to a TDC is the time interval between two events, and this time interval is quantized and the digital representation of it is given as the output. As shown in Fig. 2.1, the width of the pulse, which is the time input (T_{in}), varies with time; thereby its digital output (D_{out}) also varies proportionally with time. Although Fig. 2.1 represents that the time pulse is synchronized with the sampling

clock edge, this need not be the case in general. An important characteristic of TDC is the minimum time interval which can be measured. This is defined as the resolution of the TDC. Therefore as the resolution of TDC improves, the smaller the time pulse that can be measured by the TDC. Figure 2.2 illustrates some of the terms discussed thus far.
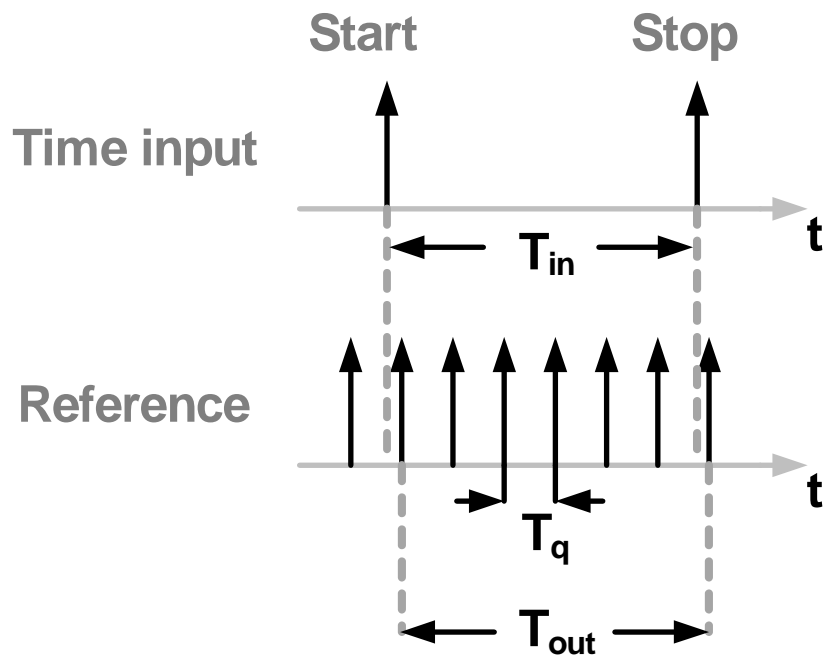
Figure 2.2: Basic TDC operation

The time interval between the two events start (T_{in}) and stop (T_{stop}), which is an analog quantity, is a quantity that needs to measured. One possible way to do this is to divide the time scale into finer references and measure the number of finer reference pulses between the two events. As shown in Fig. 2.2, T_q represents the finer reference pulse width, thereby representing the minimum time width that can be determined by the system, i.e. the resolution of the TDC. The output T_{out} is a integer multiple of T_q, i.e. $T_{out}[n] = k \times T_q$, where k is a digital word, an integer, equalling the number of reference pulse widths in the time event. Therefore, we

can express the input as

$$T_{in}[n] = T_{out}[n] + Q(e) \tag{2.1}$$

where Q(e) is equal to the quantization error. Therefore the digital representation of T_{in} can be written as

$$T_{out} = k \times T_q = T_{in} - Q(e) \tag{2.2}$$

The digital representation of T_{in}, which is k, is obtained from eq. 2.3

$$k = \frac{T_{in} - Q(e)}{T_q} \tag{2.3}$$

In the above example, the TDC resolution is limited by T_q, i.e. a time interval smaller than T_q cannot be measured by the above TDC. With decreasing gate delays in modern day CMOS technology, the resolution achievable by the above kind of TDC improves (i.e. T_q decreases), but this technique has limited uses as it depends on the minimum possible reference width that be accurately obtained.

Many modern applications like energy efficient analog-to-digital converters, wherein the analog voltage is converted to time information that is processed by a TDC to give a digital word [7], and jitter measurement applications [4] where a TDC is used to measure the phase difference between the input reference clock and VCO clock, require sub-pico second TDC resolutions. Therefore, over the years, a great deal of effort has been made in to improve the time resolutions that can be measured.

The remainder of the chapter discusses a few design techniques that help improve the resolution achievable by TDCs.

2.2 Nyquist Rate TDCs

2.2.1 Gate delay TDC

One of the most basic TDC architectures comprises of a chain of delay elements as shown in Fig. 2.3 [8]. This TDC works by counting the number of sequential delays that occur between two rising signal edges (start and stop). One attractive feature of this TDC architecture is that it can be constructed entirely from standard digital gates, thereby enabling the possibility of synthesizing the TDC.
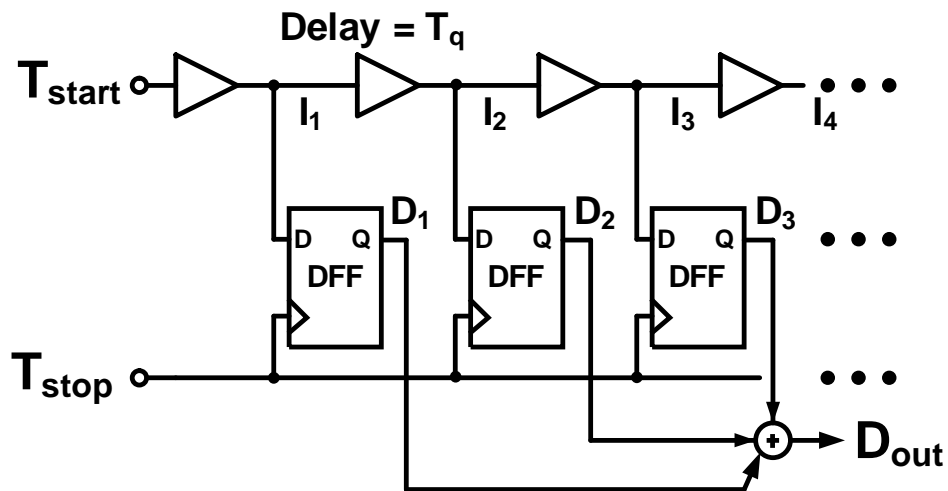
Figure 2.3: Gate delay based TDC.

To explain its operation, the rising edge of the input, T_{start}, which represents the start event, is successively delayed by a series of delay elements, each with delay T_q. Therefore, as shown in the timing diagram Fig. 2.4, the output of the of xth delay cell, I_x, goes high T_q time after I_{x-1} goes high, where T_q is the time delay of the delay element. Therefore in a gate-delay based TDC, the minimum time step that can be measured is equal to T_q,

$$T_{lsb} = T_{q1} - T_{q2} \tag{2.4}$$
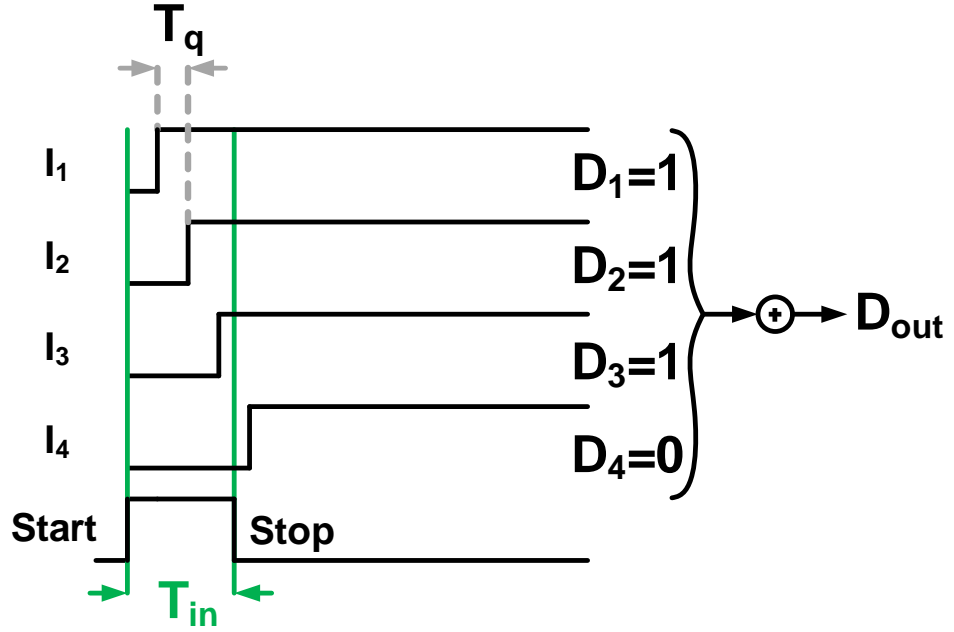
Figure 2.4: Timing for gate delay based TDC.

The delayed outputs of the delay elements act as inputs to D-flip flops(DFFs), which are clocked synchronously with the rising edge of the stop signal, T_{stop}, representing the second event. The thermometer code generated at the register output corresponds to the number of delay elements the input has transitioned during the time interval $T_{stop} - T_{start}$. The TDC digital output $D_{out}[n]$ is then simply equal to the thermometer code i.e.

$$D_{out}[n] = \sum_{i=1}^{N} D_i \tag{2.5}$$

where N is the total number of delay elements in the TDC. The above delay-chain architecture is very digital in nature and offers moderate performance, with the resolution of TDC (T_q) being limited by the minimum delay achievable. With

decreasing gate delays, the above architecture is shown to achieve resolution in the order of tens of pico-seconds.

Another important limitation of the above architecture is the high cost for increase in dynamic range. Increasing the dynamic range of the delay-chain TDC requires a linear increase in the number of delay elements, which inadvertently decreases the sampling rate of the TDC. Although technology scaling will improve the intrinsic delay, the mismatch of delay elements is expected to get worse. This inherently means larger device sizes and larger area and larger power. One alternative solution to the above problem is to use the delay-chain in a wrapped around fashion [9].

2.2.2   Vernier TDC

The Vernier delay technique is one of the very basic time digitization architectures and has been widely used [10, 11, 12, 13]. As shown in Figure 2.5, the vernier TDC works by effectively stretching the input time interval T_{in} by delaying both the start and stop signals with two different delay-chains, whose delay values are nominally different (T_{q1} and T_{q2}).

The start signal is made to pass through a delay chain of delay T_{q1}, the outputs of which are sent to a DFF. The clocks of these DFF's are themselves obtained from a delay chain, whose input is the stop signal. Therefore, the resolution in this case is equal to the relative rate of transitions. As a result, the effective resolution of the Vernier TDC is found to be the difference of the two delays, or more specifically,

$$T_{lsb} = T_{q1} - T_{q2} \qquad (2.6)$$
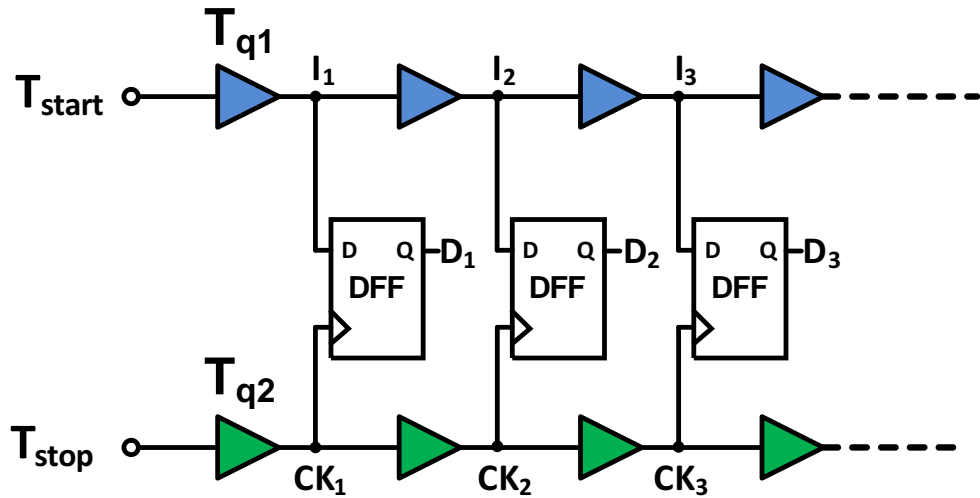
Figure 2.5: Vernier TDC.

Figure 2.6 shows the timing diagram for the vernier TDC. As seen, the vernier technique appears to be able to substantially increase the TDC resolution (as it is the difference between two delays, as opposed to absolute delay like in the gate-delay TDC). However, there are a number of issues that practically limit the resolution. Mismatch between the delay chains provides a bigger problem in a vernier TDC, as the matching now has to be done over two delay lines as opposed to one. Also increasing the dynamic range of a vernier TDC is a bigger problem than a gate-delay based TDC. This can be seen from the following example.

Consider a TDC which can measure a time input of pulse width T_{max}. In a gate-delay based TDC, the resolution with $T_{lsb} = T_{delay}$, the length of the delay chain is given by

$$(\text{Delay chain length})_{gate-delay} = \frac{T_{max}}{T_{delay}} \tag{2.7}$$

For a vernier TDC with $T_{lsb} = T_{delay1} - T_{delay2}$, the number of delay elements
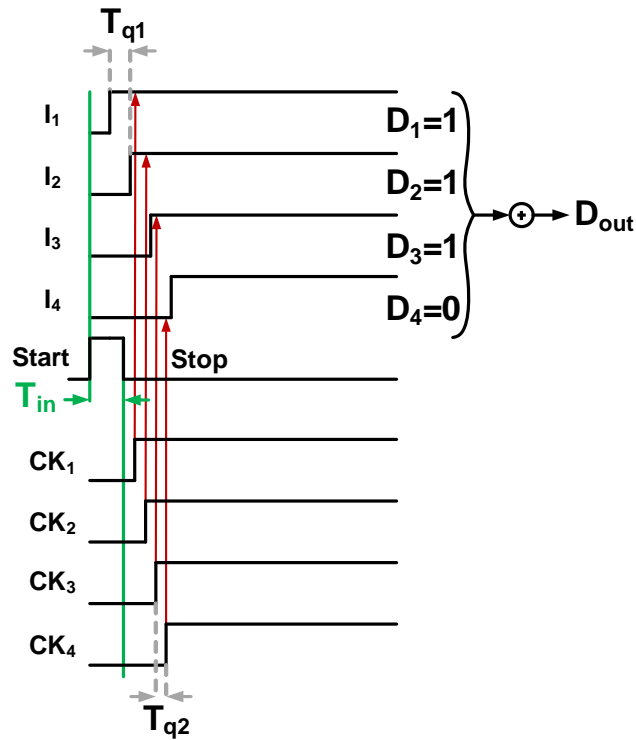
Figure 2.6: Timing diagram for vernier TDC.

required is

$$(\text{Delay chain length})_{vernier} = \frac{T_{max}}{T_{delay1} - T_{delay2}} \tag{2.8}$$

therefore, the length of the delay chain increases with improving resolution of the TDC. Another artifact of the above is the reduction in frequency of operation of the vernier TDC. To mitigate some of these problems, alternative approaches using a ring-based architecture have been proposed [11].

Thus far gate-delay based TDCs and vernier TDCs that are single-step TDC architectures have been described. In the next subsection, multi-step TDC architecture is studied.

2.2.3 Pipeline TDC

Gate-delay based TDCs and vernier TDCs incur a huge penalty when trying to increase the dynamic range of the TDC. An alternative architecture involves using a multi-stage architecture, where the first stage coarsely resolves the time input. The residue is found out using a time subtractor, which is then amplified and sent to the next stage, which repeats the operation, analogous to a pipeline ADC. Figure 2.7 shows a pipeline TDC architecture [14].
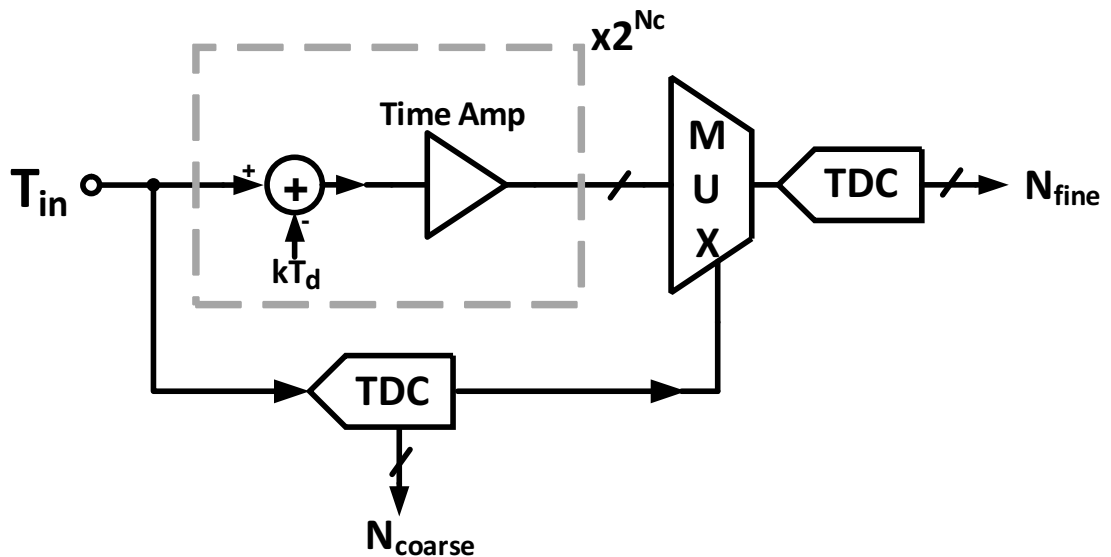
Figure 2.7: Pipeline TDC.

The time input (T_{in}) is sent to a coarse TDC which gives the coarse bits N_c. The coarse value of the time output is now subtracted from the time input and the residue is amplified before being passed onto the next stage. However, unlike voltage, time cannot be stored unless it is converted to other storable quantities such as voltage or current. Therefore every possible time residue is created and amplified using a separate time amplifier. The coarse bits act as a select signal for a MUX, and the appropriate amplified time residue is passed to the next stage(fine

TDC).

The final resolution of the TDC is equal to $T_{fs}/2^N$, where N is the total number of bits resolved in the TDC. The performance of this architecture is limited by the time-amplifier, as it is difficult to build high resolution time amplifiers. Another drawback of this architecture is that the number of time amplifiers required increases exponentially with the number of coarse bits resolved. This therefore increases the power consumption, while also increasing the errors due to mismatch.

2.3   Oversampling TDC

For each of the Nyquist TDC architectures described so far, we have seen that significant effort is required to reduce the TDC resolution below that of a gate-delay, and in each case the cost for doing so is increased complexity. Calibration does generally improve resolution performance in the presence of mismatch, but it comes at an increased cost of power. Therefore, an alternative set of architectures that use the properties of oversampling have been developed to achieve a sub-ps resolution TDCs.

2.3.1   Gated Ring Oscillator based TDC

A gated ring oscillator (GRO) based TDC is similar to that of a ring-based gate-delay TDC, except that in GRO TDC the oscillator ring is switched in accordance with the time input [15, 16].

Figure 2.8 shows a GRO-TDC, in which the Enable pulse switches the ring oscillator ON/OFF, where the Enable pulse represents the time input. In other
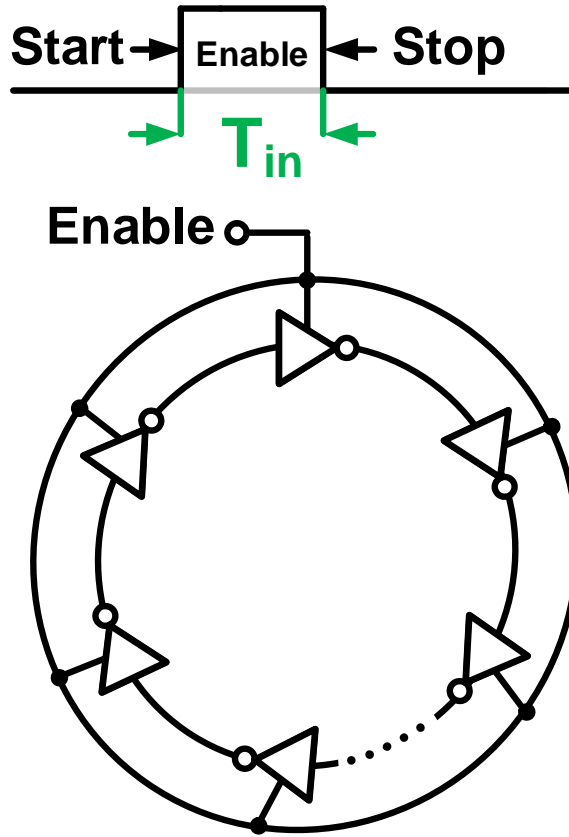
Figure 2.8: GRO based TDC.

words, the amount of time for which the ring oscillator oscillates is equal to the time input (T_{in}). Therefore the output of the GRO TDC is the change in the phase of the ring oscillator, i.e.

$$D_{out} = \phi[n+1] - \phi[n] \tag{2.9}$$

where $\phi[n]$ is the phase of ring oscillator. Since the GRO-TDC is never reset, it preserves the phase at which it stops oscillating for the next cycle as shown in Fig. 2.9. As shown in the figure, the ring-oscillator oscillates at frequency F_1 when Enable is high, and is stagnant when Enable is low. Therefore, ideally the starting

phase of the next clock phase is exactly equal to stopping phase of the previous cycle.
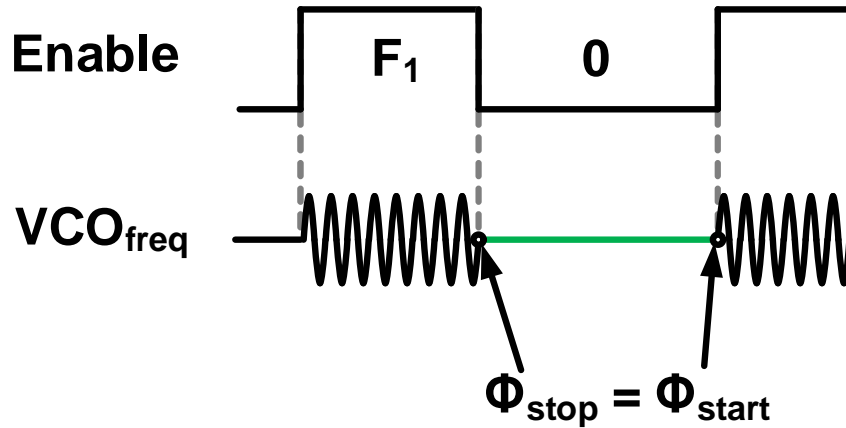
Figure 2.9: Conceptual diagram of GRO based TDC.

By noting that $\phi[n] = \int T_{in} + Q(e)$, and updating eq. 2.9, we get the digital output of the GRO TDC as

$$D_{out} = T_{in} + (1 - z^{-1})Q(e) \tag{2.10}$$

Therefore, the output of the GRO-TDC is input + shaped quantization noise, hence giving us first order noise-shaping. However, this approach is plagued with phase leakage problems as shown in Fig. 2.10.

Ideally, during the off-state of the ring oscillator the phase is preserved. However, in practical situations the phase is not preserved and leakage is observed thereby making it a leaky first order $\Delta\Sigma$ TDC. This problem is addressed in a switched ring oscillator (SRO) TDC, as discussed in the next subsection.
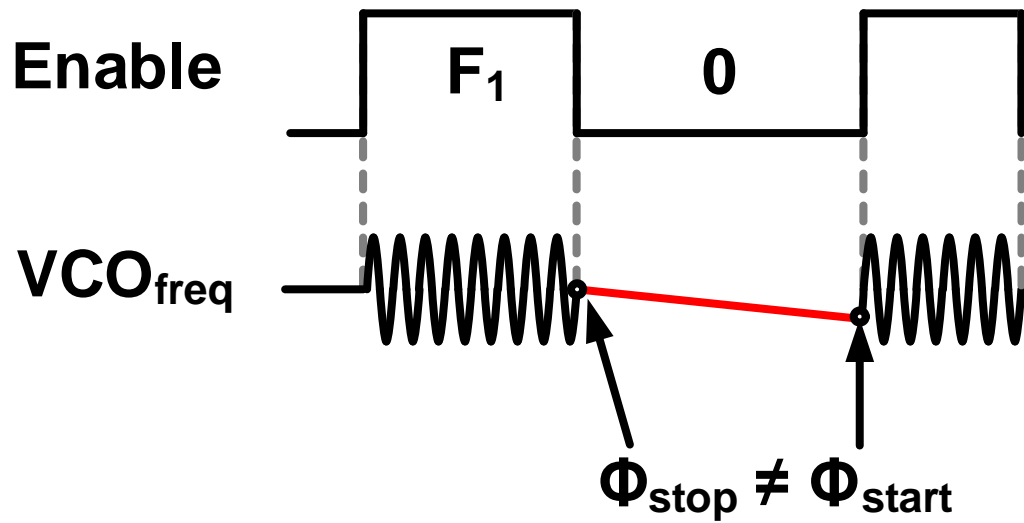
Figure 2.10: Phase leakage in GRO-TDC.

2.3.2 Switched Ring Oscillator based TDC

A switched ring oscillator (SRO) TDC is identical to a GRO-TDC in many aspects, with the main difference being that instead of turning off the VCO during the off state, it is made to oscillate at a lower frequency [17]. Figure 2.11 shows the conceptual diagram of a SRO-TDC.
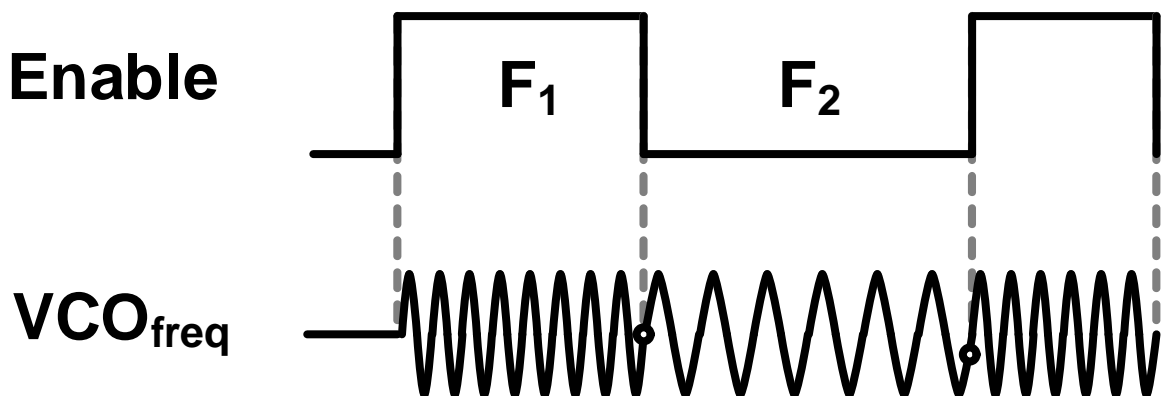
Figure 2.11: SRO based TDC.

The advantage of continuing the oscillation is that the phase leakage problems are reduced. The digital output of the SRO-TDC is also first order noise-shaped [17, 18].

Thus far, only first order noise shaped TDC's are discussed. The next sub-section looks at a higher order $\Delta\Sigma$ TDC.

2.3.3   MASH TDC

In ADCs, multi-stage noise shaping (MASH) architecture is one in which the quantization error from one $\Delta\Sigma$ loop is extracted and sent for processing into another loop, typically another $\Delta\Sigma$ loop. The digital outputs of both the loops are later combined to give a higher order noise shaping (sum of the orders of the two individual loops) [19]. The advantages of the MASH $\Delta\Sigma$ modulator is that higher order noise shaping is achieved with the stability enjoyed by that of a lower order $\Delta\Sigma$ architecture. The concept of MASH ADC can be readily extended to a TDC as implemented by [20] and as shown in Fig. 2.12.

In this TDC architecture, a 3rd order $\Delta\Sigma$ TDC is built using 1-1-1 MASH architecture. The performance of the TDC is, however, limited by noise leakage.

2.4   Summary

One common trait of the $\Delta\Sigma$ TDC architectures is that they lack a dedicated feedback DAC. One reason for the lack of a dedicated feedback DAC is that, unlike voltage, time cannot be stored unless it is converted to other measurable quantities such as voltage or current (which itself adds noise and other nonlinearities in the
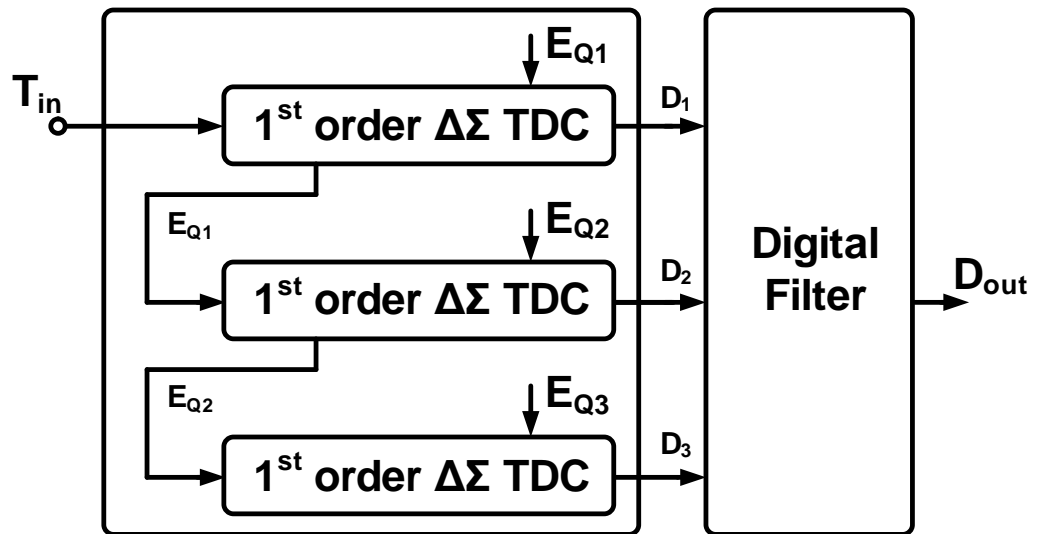
Figure 2.12: 1-1-1 MASH $\Delta\Sigma$ TDC

process of conversion). In the next chapter, we propose a 3rd order $\Delta\Sigma$ TDC which makes use of dedicated feedback DAC and show the measured chip results [21].

CHAPTER 3. CHARGE PUMP BASED $\Delta\Sigma$ TDC

Time to digital converters with sub-ps resolution have found various applications such as high resolution ADC's, phase jitter measurements etc. Oversampling TDCs have emerged as an attractive option and have achieved sub-ps resolution [15, 20, 22]. However, the range of architectures used for oversampling converters are limited since it is difficult to subtract input time from a voltage quantity. Figure 3.1 highlights some of these problems.
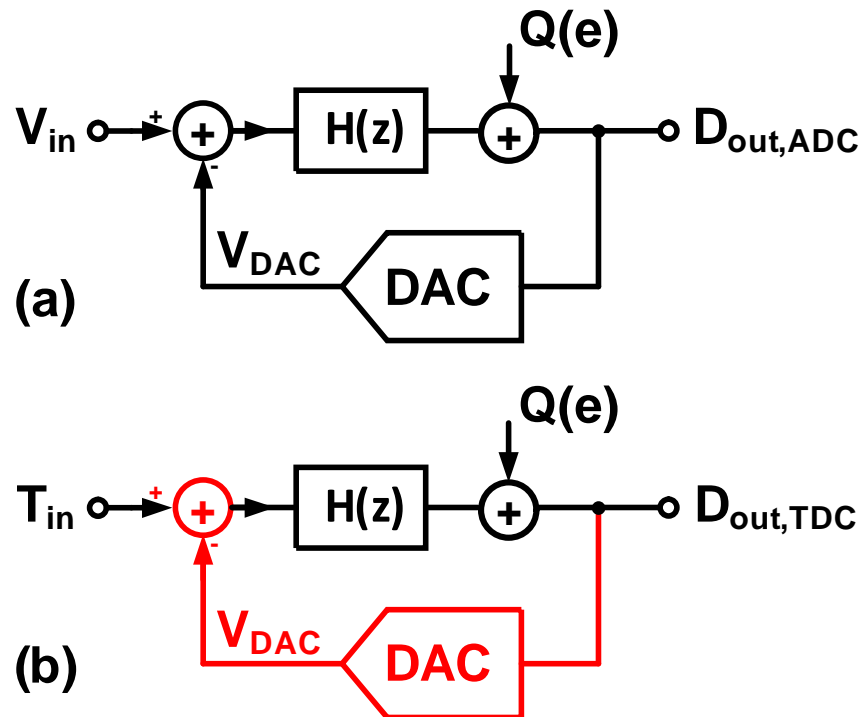
Figure 3.1: Oversampling ADC architecture extended to operate as a TDC.

Figure 3.1 (a) shows a typical oversampling ADC, where H(z) is the loop filter, and Q(e) is the quantization error, and $D_{out,ADC}$ is the digital output of the ADC [19]. The DAC converts the digital output to an analog voltage V_{DAC}. V_{DAC}

is subtracted from the input voltage V_{in}, and the error signal is processed by the loop.

In a oversampling TDC, the analog voltage is replaced by T_{in} as shown in Fig. 3.1 (b). Traditionally, it is difficult to subtract an analog voltage from time input thereby seriously limiting the range of architectures available for oversampling TDCs. Also, with current technology, it is still impossible to directly preserve the quantization error. Instead, the time information has to be converted into another intermediate physical quantity such as voltage or charge. This resulted in developing architectures that do not use a dedicated feedback path like GRO-TDC, SRO-TDC, 1-1-1 MASH [15, 17, 20].

In this half of the project, a novel TDC architecture is proposed that overcomes the problem of subtraction by using a modified dual-slope ADC (noise shaping integrating quantizer) for DAC and a charge-pump as a phase detector, or in other words as a subtractor. The following section starts by discussing the noise shaping integrating quantizer.

3.1   Noise-shaping Integrating Quantizer

A noise shaping integrating quantizer [23, 24] works on a principle similar to that of a dual-slope ADC [25], which in itself can be considered equivalent to a first-order incremental ADC [26]. It acts as quantizer in the $\Delta\Sigma$ loop, while also giving a extra order of noise shaping and above all providing the feedback DAC information in time domain. The operation is discussed in detail in the remainder of this section.

3.1.1   Noise-shaping Integrating Quantizer

The operation of a noise-shaping integrating quantizer (NSIQ) is similar to that of a conventional dual-slope ADC with two key differences: the integrating capacitor is never reset, and the discharging current must disconnect on the next fast-clock edge after the comparator has detected a zero crossing [23]. Figure 3.2 shows the system of NSIQ. The key difference when compared to a dual-slope ADC is the timing control in the feedback path. The operation of NSIQ can be broadly classified into two categories (1) Sampling phase and (2) Discharge phase.
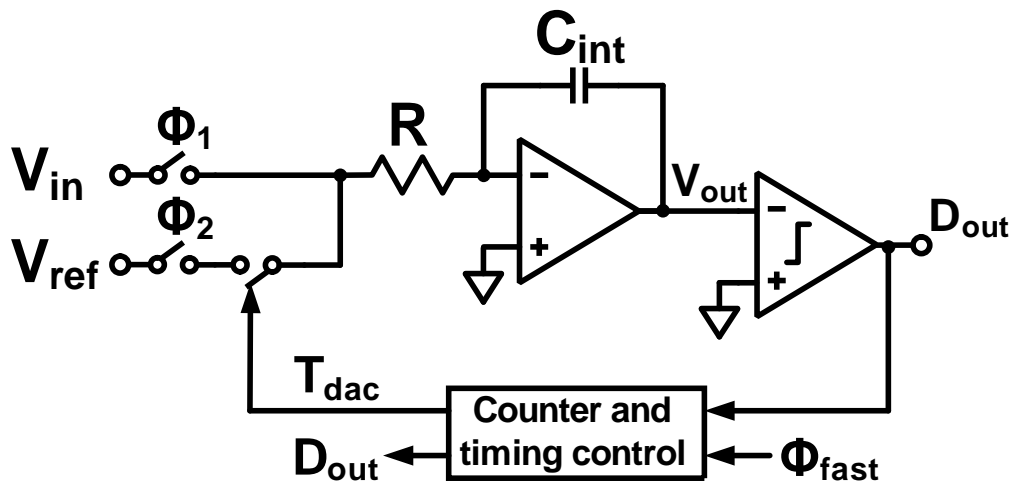
Figure 3.2: Noise-shaping integrating quantizer system.

Input Sampling Phase

Figure 3.3 shows the input sampling phase of the noise-shaping single slope quantizer. The input sampling phase of NSIQ differs from the input sampling phase of a dual-slope ADC in that the integrating capacitor is not reset before the beginning of the sampling cycle (ϕ_1). During this phase, the input is integrated onto the capacitor 'C_{int}' for a fixed duration of time through a resistor of value
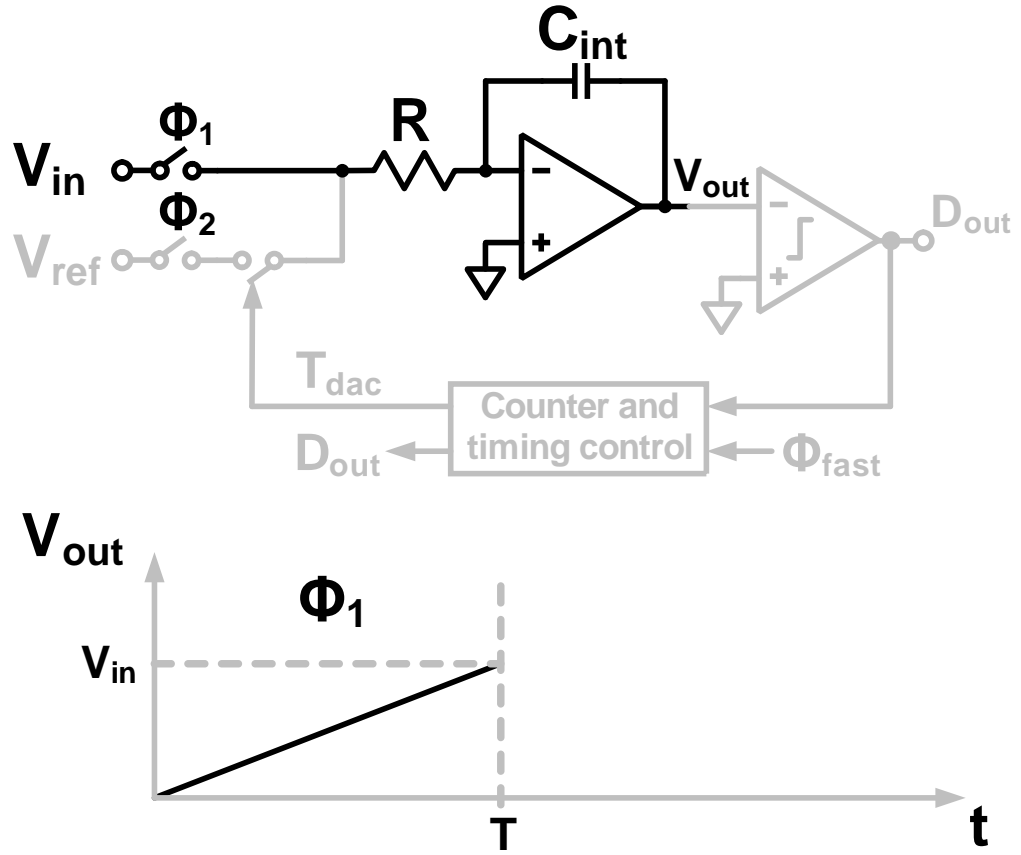
Figure 3.3: Sampling phase of NSIQ.

'R'. Assuming that the time period of integration is T, the voltage at the end of the sampling cycle ϕ_1 is given by

$$V_{out,\phi_1} = \int_0^T \frac{V_{in}}{RC} dt + c \tag{3.1}$$

Note that c is a constant of integration, and is dependent on the initial voltage stored on the capacitor. For a constant input, the above equation is simplified and is given as

$$V_{out} = \frac{V_{in} \times T}{RC} + c \tag{3.2}$$

By scaling $\frac{T}{RC}$ to be equal to one, the voltage at the end of charging phase is given $V_{out} = V_{in}$ as shown in Fig. 3.3. Since the integrating capacitor is not reset, the final output voltage at the end of the sampling phase is dependent on c. In Figure 3.3, the initial value for the first cycle is assumed to be equal to zero.

Discharge Phase

During the discharge phase, the input voltage is disconnected and the capacitor is discharged using a constant reference voltage $-V_{ref}$ via the resistor 'R' until the next fast-clock edge after the comparator has detected a zero crossing.

Figure 3.4 shows the operation of the dual-slope ADC during the discharge phase. The slope of discharge in this case is calculated to be equal to V_{ref}/RC. As shown in Fig. 3.4, the discharging is continued after the zero crossing is detected, until the next fast clock edge. In alternate words, after the zero crossing is detected, the zero crossing edge is synchronized with one of the fast clock edges. This synchronized edge is used to turn off the discharging. By doing this, the negative of quantization error is stored on the integrating capacitor. Therefore, the output voltage at the end of the discharge phase is given by

$$V_{out,\phi_2} = -Q(e) \tag{3.3}$$

As opposed to a dual-slope ADC, the integrating capacitor is not reset, and the value is carried forward to the next phase.

Noise-shaping Integrating Quantizer

Figure 3.5 shows the timing diagram over two cycles for the NSIQ. Assuming that the initial voltage on the integrating capacitor is equal to zero, the voltages during the first cycle are given by eq. 3.4
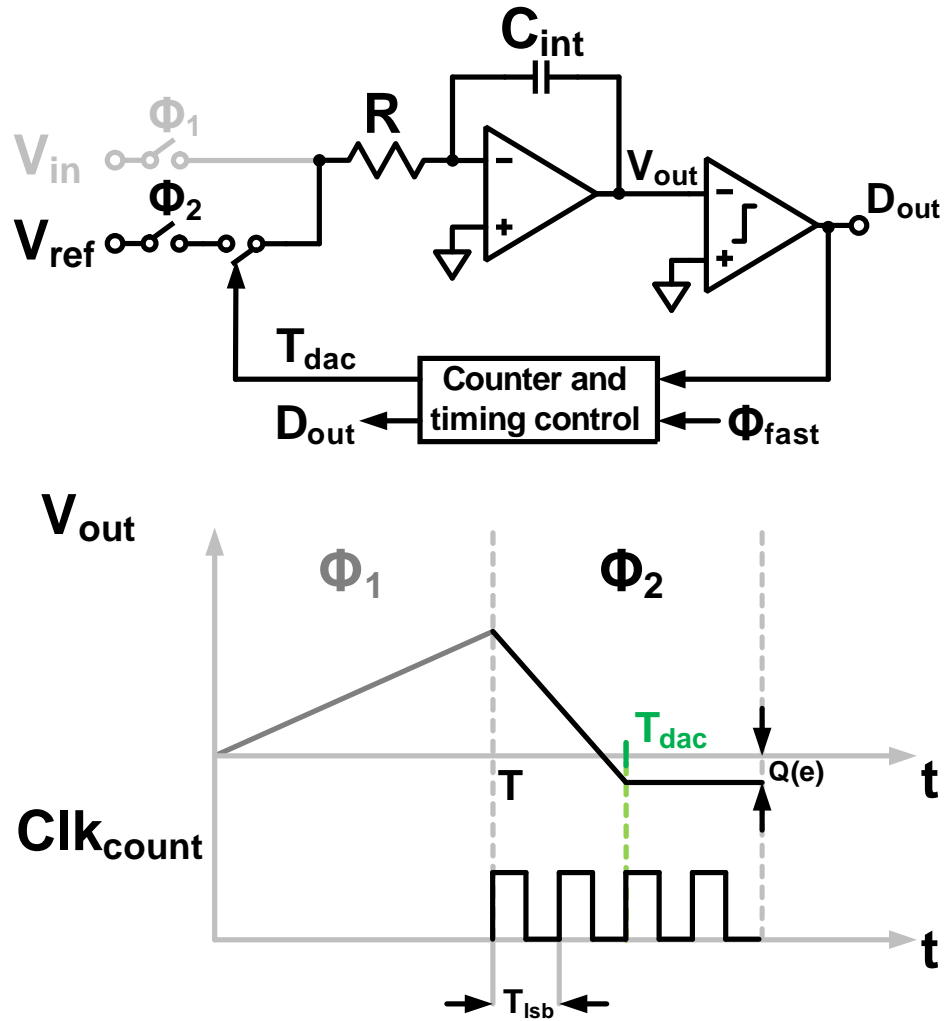
Figure 3.4: Discharge phase of noise-shaping integrating quantizer showing the quantization error being stored at the end of quantization phase.

$$V_{out,\phi_1}[1] = V_{in} \tag{3.4a}$$

$$V_{out,\phi_2}[1] = -Q(e) \tag{3.4b}$$

$$D_{out}[1] = V_{in} + Q(e) \tag{3.4c}$$

Note for the beginning of the second cycle, the voltage on the integrating capacitor is equal to $-Q_e$. Therefore, voltages during the second cycle are given
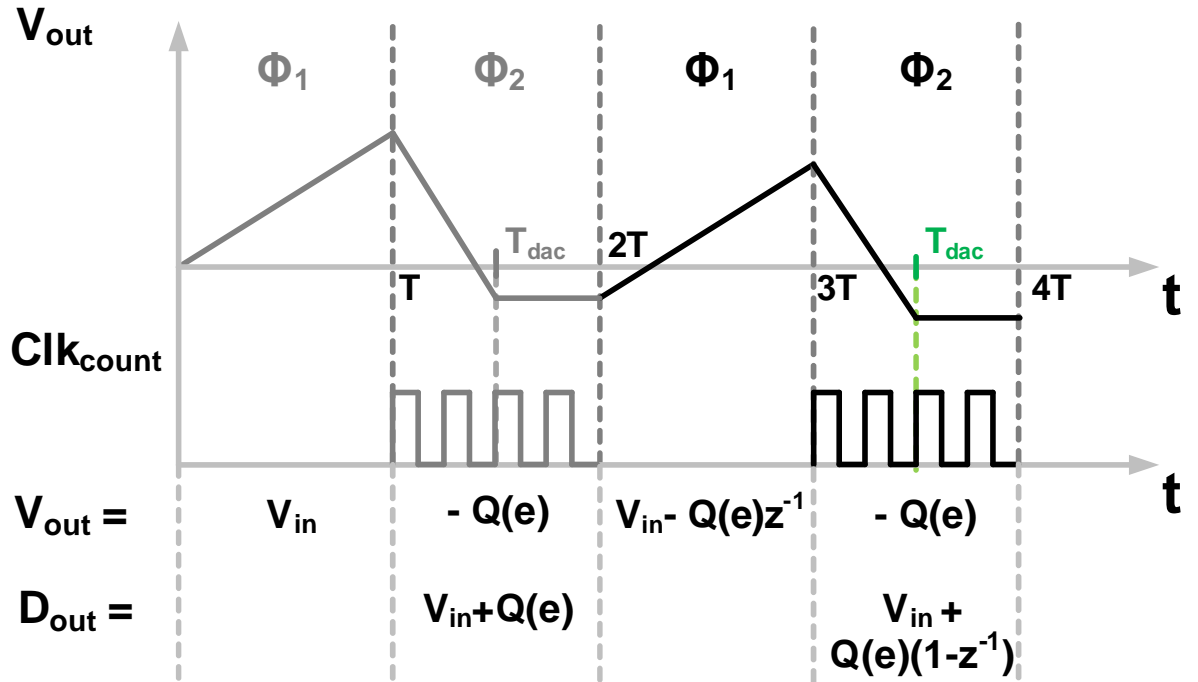
Figure 3.5: Timing diagram showing the operation of NSIQ over two cycles of operation.

by eq. 3.5

$$V_{out,\phi_1}[2] = V_{in} - z^{-1}Q(e) \tag{3.5a}$$

$$V_{out,\phi_2}[2] = -Q(e) \tag{3.5b}$$

$$D_{out}[2] = [V_{in} - z^{-1}Q(e)] + Q(e) \tag{3.5c}$$

$$= V_{in} + (1 - z^{-1})Q(e) \tag{3.5d}$$

From eq. 3.5, it is evident that final digital output shapes the quantization error, and hence we get 1st order noise shaping from the NSIQ.

One more key property of NSIQ is that T_{dac} represents the DAC value in time domain. Therefore, as discussed in next section, a charge-pump is used to

find the phase difference between time input, T_{in}, and T_{dac}. Figure 3.6 shows the equivalent model of the noise-shaping integrating quantizer. The input to the system is an analog voltage V_{in}, and the digital output (D_{out}) is the input + shaped quantization error. Along with the digital output, T_{dac} is also available, which is a time pulse whose width is proportional to D_{out}.
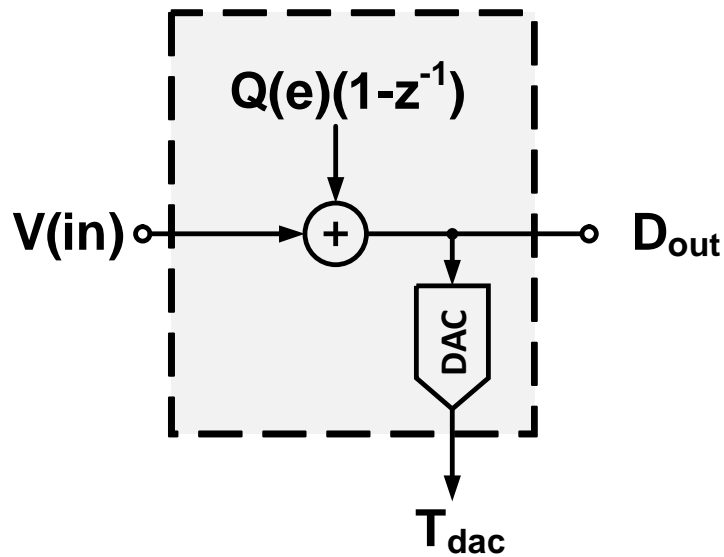
Figure 3.6: Equivalent model of noise-shaping integrating quantizer.

3.2   A 2nd Order Charge-pump Based $\Delta\Sigma$ TDC

3.2.1   Charge-pump as a Phase Difference Integrator

A charge-pump is typically used in a phased locked loop (PLL) to find the phase difference between the reference signal and the output signal - typically designated as UP and DN [27]. As shown in Fig. 3.7, the two signals UP and DN are used to control two switches, which help steer identical currents I_{cp} into or out of a capacitor, thereby integrating the phase difference between the two signals UP

and DN onto the charge-pump capacitance C_{cp}.
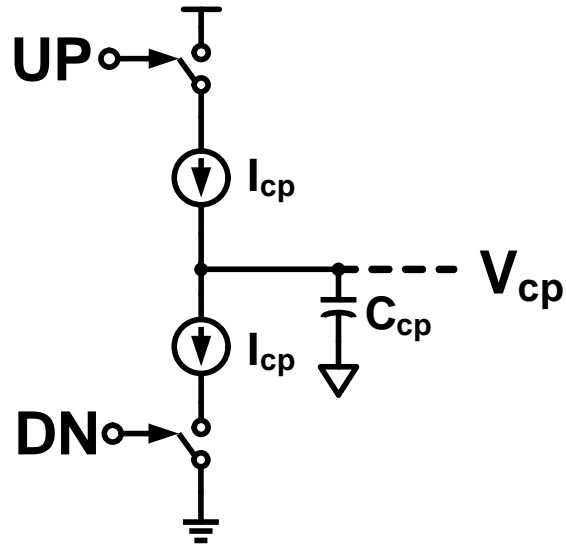
Figure 3.7: Charge-pump as a phase subtractor and integrator.

In each cycle, the time during which the switch is turned on is proportional to the phase difference, hence the charge integrated onto the capacitor is dependent on the phase difference between UP and DN signals. The voltage change on the capacitor during each cycle is given by

$$\Delta V_{cp} = \frac{I_{cp} \times \Delta T}{C_{cp}} \tag{3.6}$$

where ΔV_{cp} is the the change in the charge pump voltage, ΔT is the phase difference between the UP and DN phases, I_{cp} is the charge-pump current and C_{cp} is the integrating capacitor. Capacitor C_{cp} is not reset, thereby acting as an integrator. Therefore, the voltage across the capacitor at the end of any cycle is given by the following equation

$$V_{cp}[n+1] = \Delta V_{int} + V_{cp}[n] \tag{3.7}$$

where $V_{cp}[n+1]$ is the sum of the previous voltage and the change in voltage during the present cycle.

From the above discussion, it is clear that one could use the charge-pump to integrate the phase difference between two time signals. We use this property to build a second-order $\Delta\Sigma$ TDC, as discussed in the following section.

3.2.2 Charge-pump based $\Delta\Sigma$ TDC
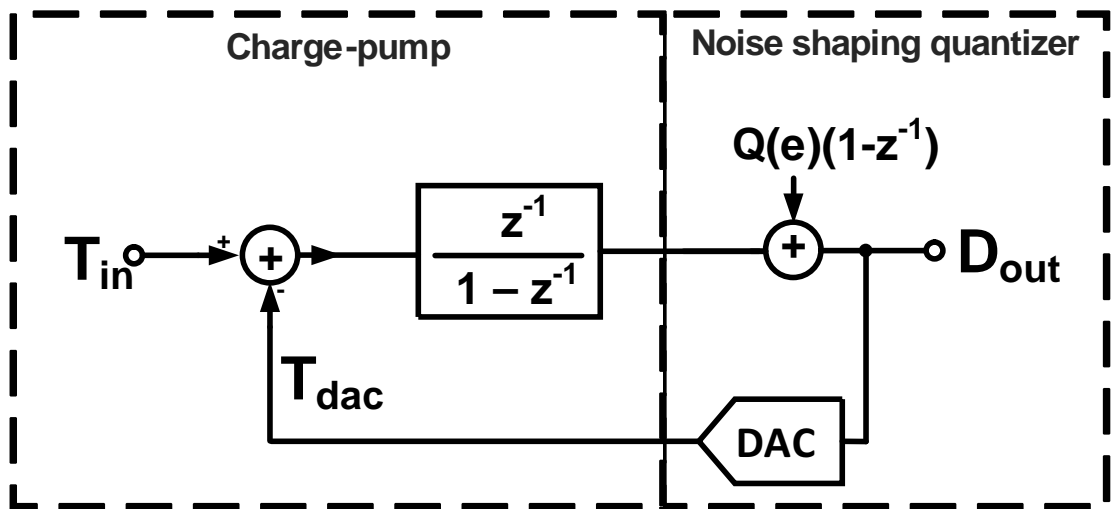
Figure 3.8: 2nd order $\Delta\Sigma$ TDC.

Figure 3.8 shows one possible structure for a second order $\Delta\Sigma$ TDC. It consists of a delayed integrator, giving one order of noise-shaping, and a noise-shaped quantizer which makes it a second order $\Delta\Sigma$ TDC. The input to the TDC is a time input T_{in} and the digital output of the system is D_{out}.

The charge-pump is used to integrate the phase difference between the time-input T_{in} and T_{dac}. A NSIQ is used as a quantizer as it gives one extra order of noise-shaping, while also giving the quantizer DAC value in time domain T_{dac}. The

resulting structure of the second order $\Delta\Sigma$ TDC is shown in Fig. 3.9. The TDC structure is a cascade of a charge-pump and noise-shaping integrating quantizer. The operation of this TDC is very similar to that of a NSIQ and its operation can be broadly classified into two phases (1) Sampling and (2) Discharging.
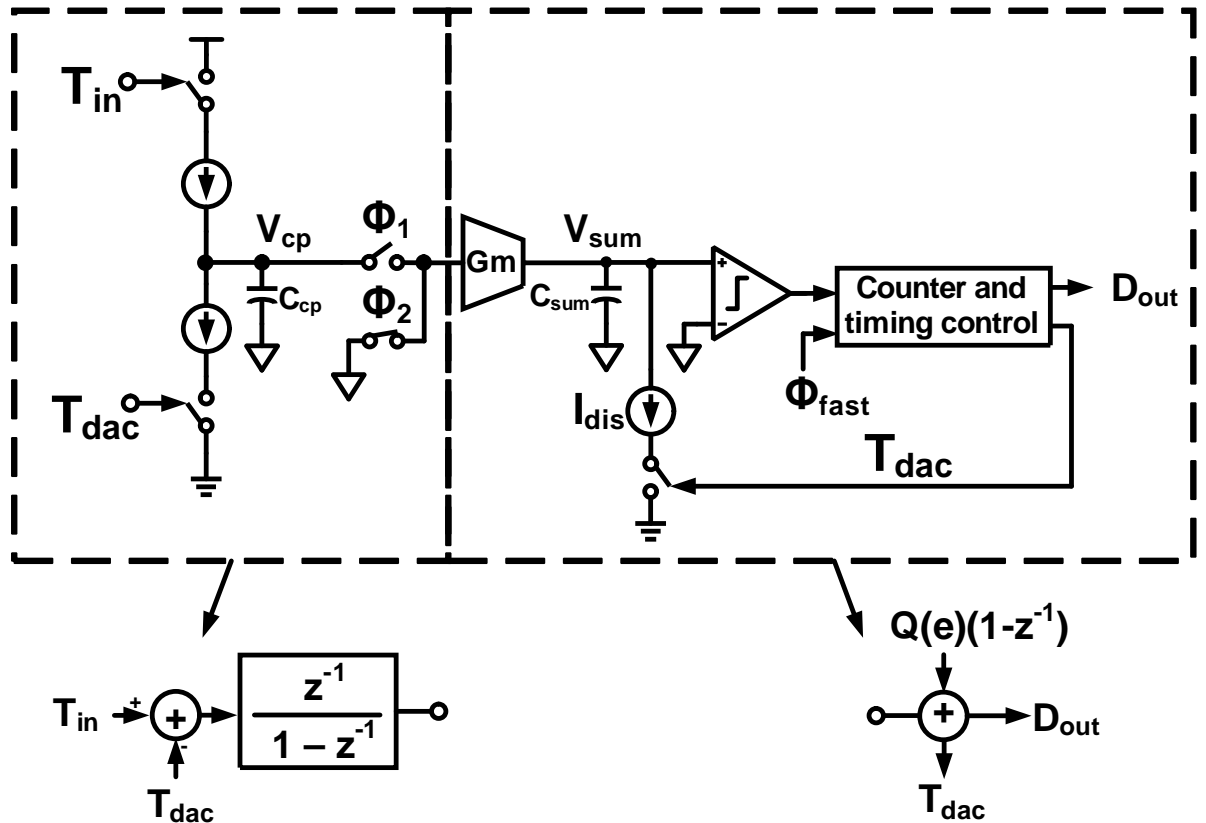
Figure 3.9: 2nd order $\Delta\Sigma$ TDC built using charge-pump and NSIQ.

Sampling Phase

The sampling phase of the TDC is similar to that of the input sampling phase dual-slope ADC, wherein the input of the first integrator is summed on the summing capacitor C_{sum} using a transconductance Gm. This operation happens during phase ϕ_1 as shown in Fig. 3.10.

The summing capacitor is equivalent to the integrating capacitor of the dual
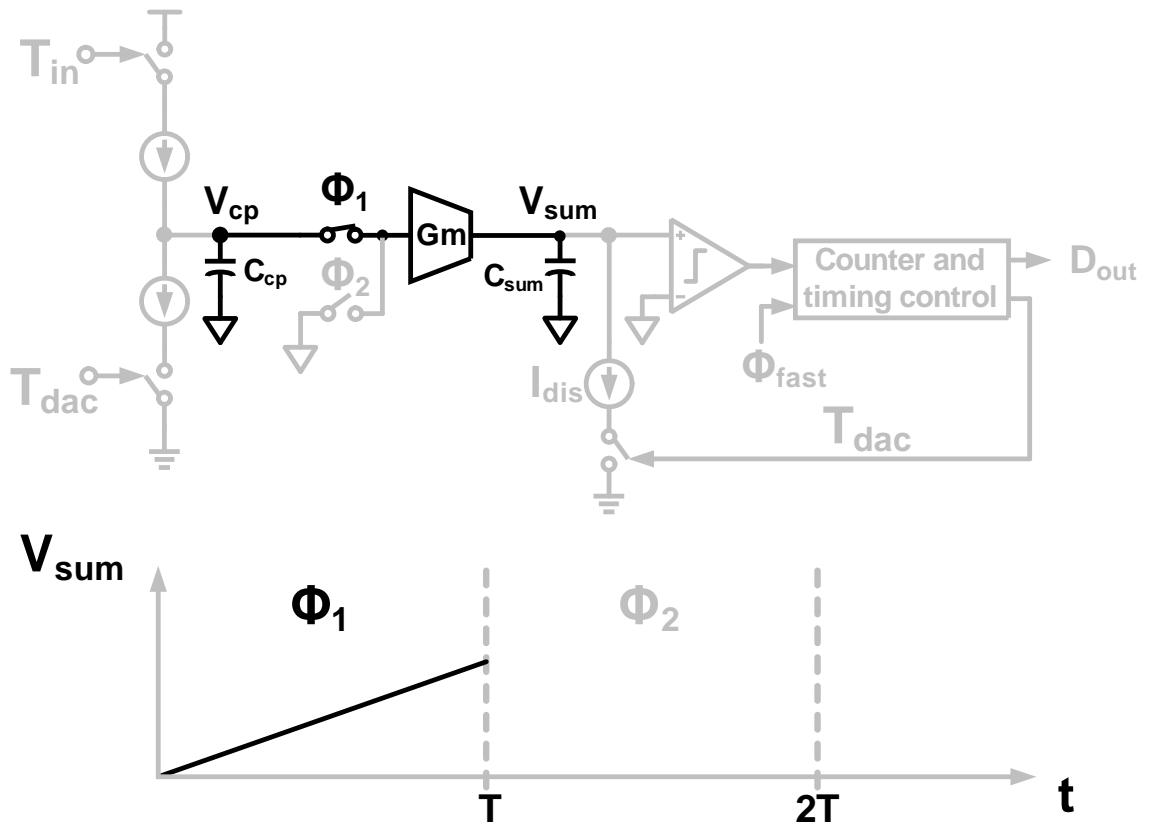
Figure 3.10: Input sampling phase of $\Delta\Sigma$ TDC

slope ADC, and is never reset. The total charge summed onto the summing capacitor during this phase is equal to $I\Delta T$, where I is the current and is equal to $Gm \times V_{cp}$. Therefore, the change in the output voltage is given as

$$\Delta V_{sum} = \frac{Gm\Delta T}{C_{sum}} \times V_{cp} \qquad (3.8)$$

where Gm is the transconductance of the stage, ΔT is the time interval for which the summing happens, which in this case is T (sampling time period/2). If $\frac{Gm\Delta T}{C_{sum}}$ is normalized to one, $\Delta V_{sum} = V_{cp}$. In this case, the output voltage V_{sum} at the end of the sampling phase is given as

$$V_{sum}[n] = -z^{-1}Q(e) + V_{cp}[n] \tag{3.9}$$

where $-z^{-1}Q(e)$ represents the quantization error of the previous cycle. Figure 3.10 also shows V_{sum} voltage as a function of time.

Discharging Phase

The discharge phase of the TDC is similar to that of NSIQ and is shown in Fig. 3.11. The capacitor C_{sum} is discharged, using a constant current source I_{dis} which is disconnected on the next fast-clock edge after the comparator has detected a zero crossing.

The summing capacitor is not reset, thereby storing the quantization error of the stage. The number of fast clock edges for which the discharge happened represents the DAC code, $D_{out}[n]$. Therefore, the voltages at the end of the discharge phase can be summarized as below

$$I_{dis} \times D_{out}[n] = (V_{sum}[n] + Q(e)) \times C_{sum} \tag{3.10}$$

When $I_{dis}C_{sum}$ is scaled to be equal to 1, we get

$$D_{out}[n] = V_{sum} + Q(e) \tag{3.11a}$$

$$= V_{cp}[n] + (1 - z^{-1}) \times Q(e) \tag{3.11b}$$

Note that T_{dac} represents the DAC value in time domain.

A 2nd Order Charge-pump Based $\Delta\Sigma$ TDC

The starting edge of the time input to the TDC is synchronized with rising edge of ϕ_1, while the stop edge of the input occurs asynchronously during ϕ_1. Therefore, during the discharge phase the difference between the DAC value in time
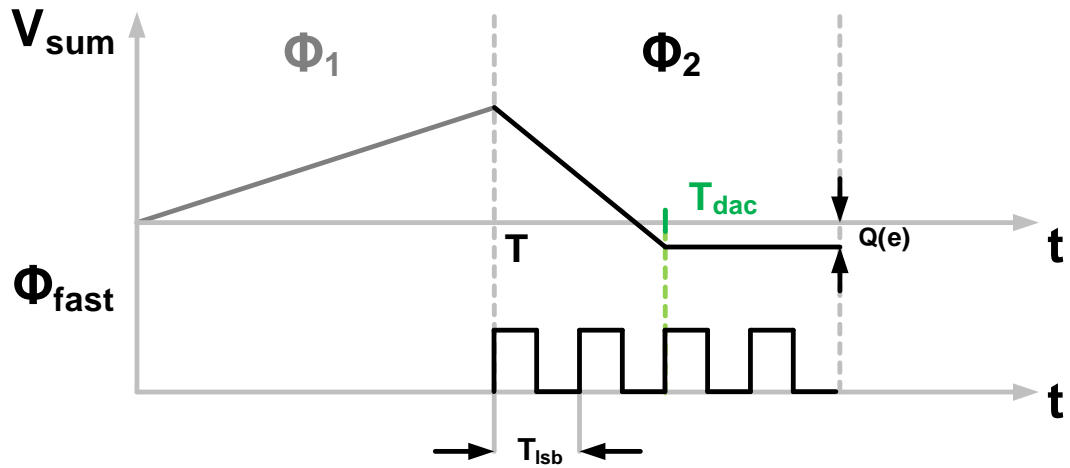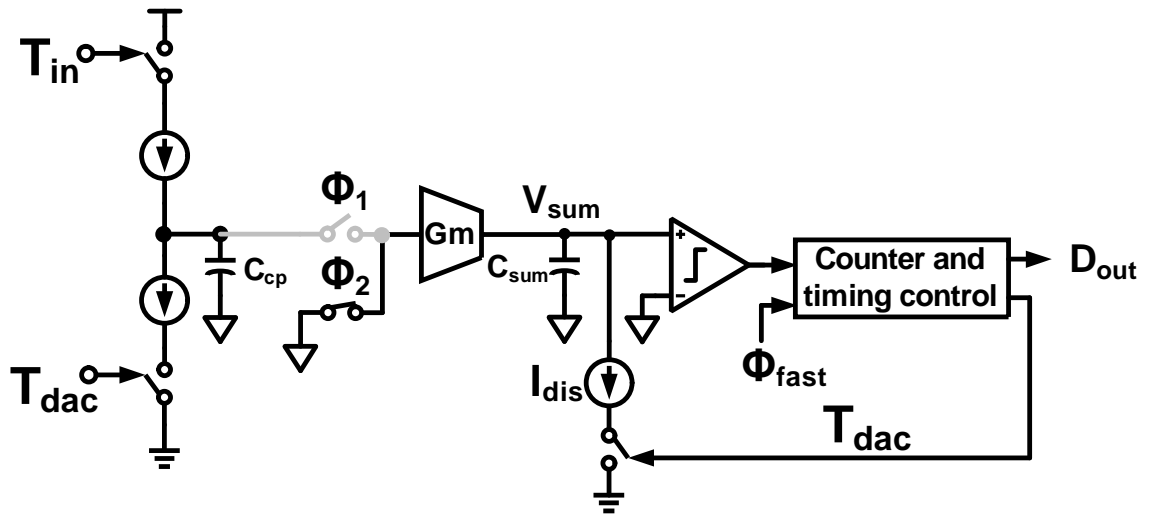
Figure 3.11: Discharge phase of $\Delta\Sigma$ TDC

domain (T_{dac}) and the input (T_{in}) is integrated onto the charge-pump capacitance C_{cp} using the input charge-pump as shown in Fig. 3.11. Therefore, $V_{cp}[n]$ is given by the following equations:

$$V_{cp}[n] = \frac{I_{cp} \times (T_{in}[n-1] - T_{dac}[n-1])}{C_{cp}} + V_{cp}[n-1] \qquad (3.12a)$$

When I_{cp}/C_{cp} is normalized to 1, we get

$$V_{cp}[n] = (T_{in}[n-1] - T_{dac}[n-1]) + V_{cp}[n-1] \tag{3.13a}$$

$$\Rightarrow V_{cp} \times (1 - z^{-1}) = T_{in}[n-1] - T_{dac}[n-1] \tag{3.13b}$$

$$\Rightarrow V_{cp} = \frac{(T_{in} - T_{dac})z^{-1}}{1 - z^{-1}} \tag{3.13c}$$

Therefore, by rearranging the terms of the above equation and using eq. 3.11 while also realizing that $T_{dac} = D_{out}$, we get

$$D_{out}[n] = T_{in}[n]z^{-1} + (1 - z^{-1})^2 \times Q(e) \tag{3.14}$$

Therefore, using a charge-pump and a NSIQ a second-order $\Delta\Sigma$ TDC can be built. The above concept can be extended to build a 3rd order $\Delta\Sigma$ TDC as discussed in the next section.

3.3   A 3rd Order Charge-pump Based $\Delta\Sigma$ TDC

The 2nd order $\Delta\Sigma$ TDC structure discussed above could be extended to operate as a 3rd order $\Delta\Sigma$ TDC by using an extra integrator and a feed-forward path in the loop as shown in Fig. 3.12.

The additional integrator and the feed-forward path shown in Fig. 3.12 are implemented using Gm-C filter as shown in Fig. 3.13

During phase ϕ_2, transconductor Gm_1 integrates the voltage V_{cp} onto capacitor C_2, thereby acting as an integrator. During the same phase, the voltage on C_2 is sensed by transconductor Gm_2 which adds a voltage proportional to the previous value of the onto the summing node V_{sum} along with some portion of the current input value. This therefore reduces the gain required by the direct feed-forward path $(Gm_3 - C_{sum})$.
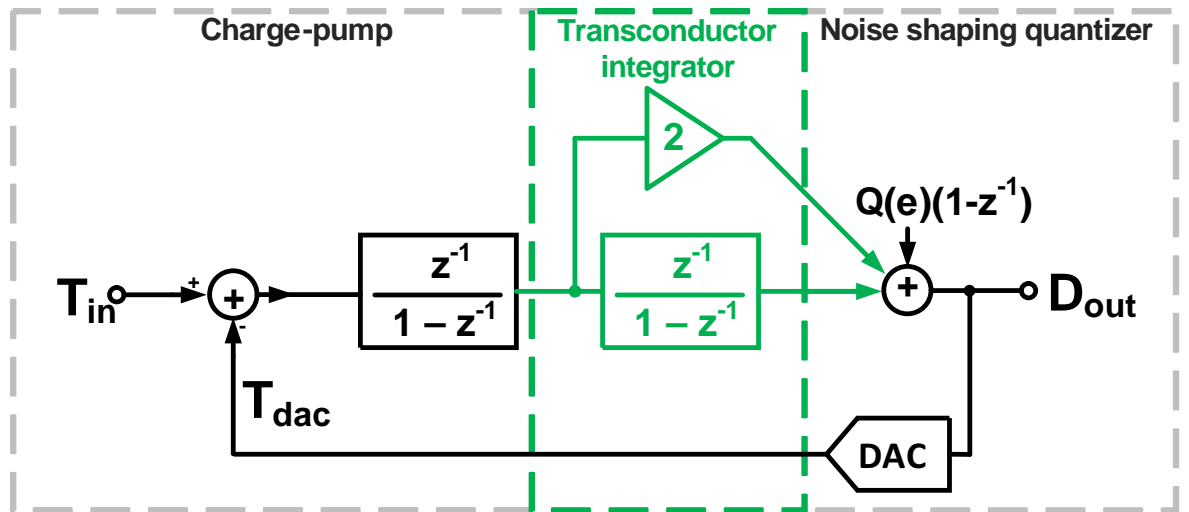
Figure 3.12: Extending the 2nd order $\Delta\Sigma$ TDC to operate as a 3rd order $\Delta\Sigma$ TDC.
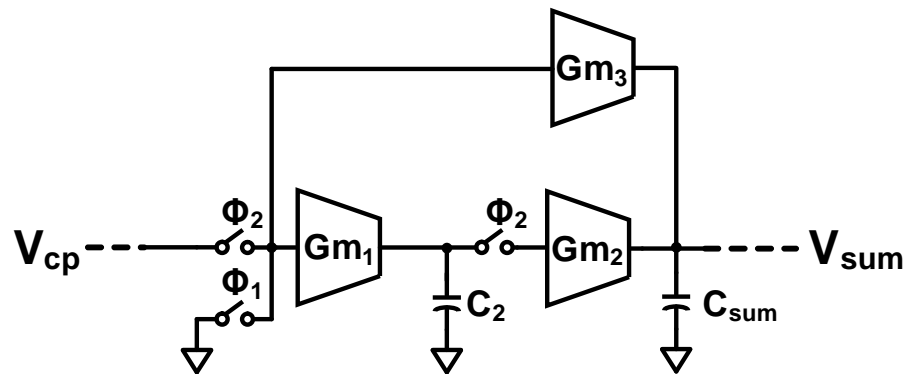
Figure 3.13: Transconductor and feed-forward path using transconductors.

3.3.1 Signal Feed-forward Path

To reduce the amount of signal processed by the loop, and also reduce the amount of distortion caused by the loop components, a input signal feed-forward path is used [28]. In voltage domain, the signal feed-forward path is implemented as shown in Fig. 3.14. The loop filter H(z) processes only the shaped quantization noise, thereby making the architecture immune to distortion by the loop. It has to

be noted that the feedback path has to be delay free for the implementation to be effective. Therefore, a delay is included in the input voltage path, which is later compensated for in the loop.
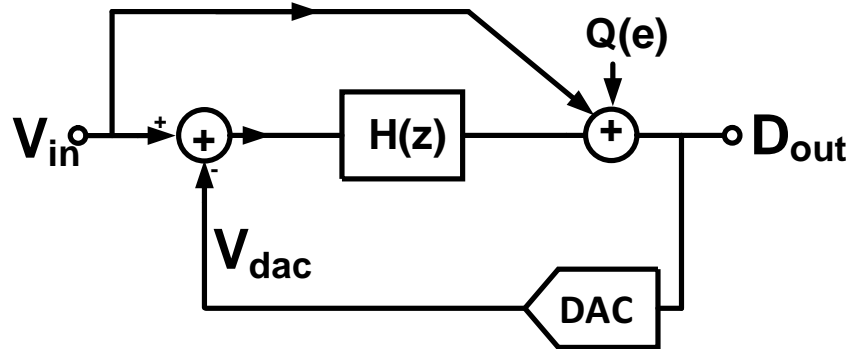
Figure 3.14: Voltage domain low distortion architecture.

However, a direct one-to-one mapping to a TDC is not so straight forward. Using the current technology, it is impossible to delay/store time information accurately. Therefore, an alternative feed-forward path is used in the TDC architecture as shown in Fig. 3.15.
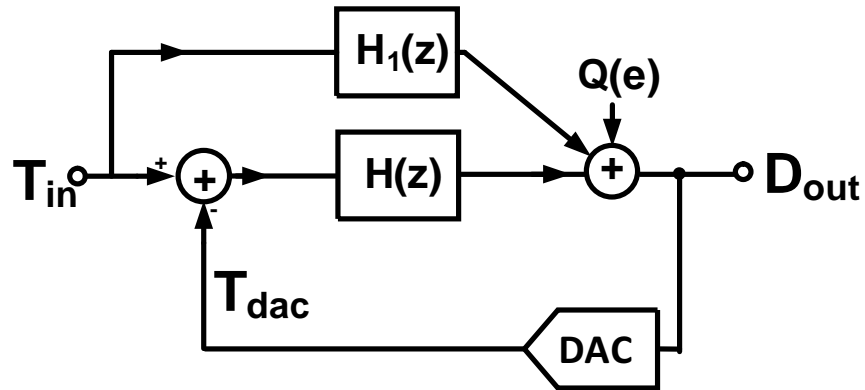
Figure 3.15: Time domain low distortion architecture.

In the feed-forward path shown in Fig. 3.15, the time input is converted to voltage domain using a charge-pump. This voltage is then passed through a low pass filter and added appropriately to the summing capacitor. The timing diagram

and the implementation of the feed-forward path filter is shown in Fig. 3.16. The feed-forward path implements the following transfer function:

$$y[n] = \frac{y[n-1] + x[n]}{2} \tag{3.15a}$$

$$\Rightarrow H_1(z) = \frac{1}{2 - z^{-1}} \tag{3.15b}$$
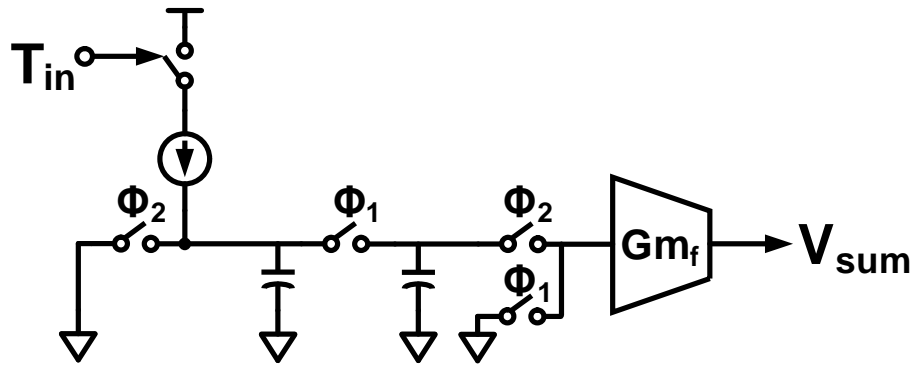
Figure 3.16: Implementation of feed-forward path in TDC.

Since the oversampling ratio of the $\Delta\Sigma$ ADC is 16, the value of $H_1(z)$ was approximated to 1, and Gm_f was designed such that $Gm_f \times T/C_{sum} = 1$.

3.3.2 A 3rd Order Charge-pump Based $\Delta\Sigma$ TDC

By incorporating the extra integrator and the feed-forward path, a 3rd order charge-pump based $\Delta\Sigma$ TDC is built. The final structure of the third-order $\Delta\Sigma$ TDC, which was implemented is shown in Fig. 3.17.

For increasing the stability of the loop, the loop transconductors were designed such that the out of band gain of the modulator was equal to 4 [19]. The quantizer was designed such that the 24 fast clock edges occur during the discharge phase of the TDC, thereby making it a 24-level quantizer.
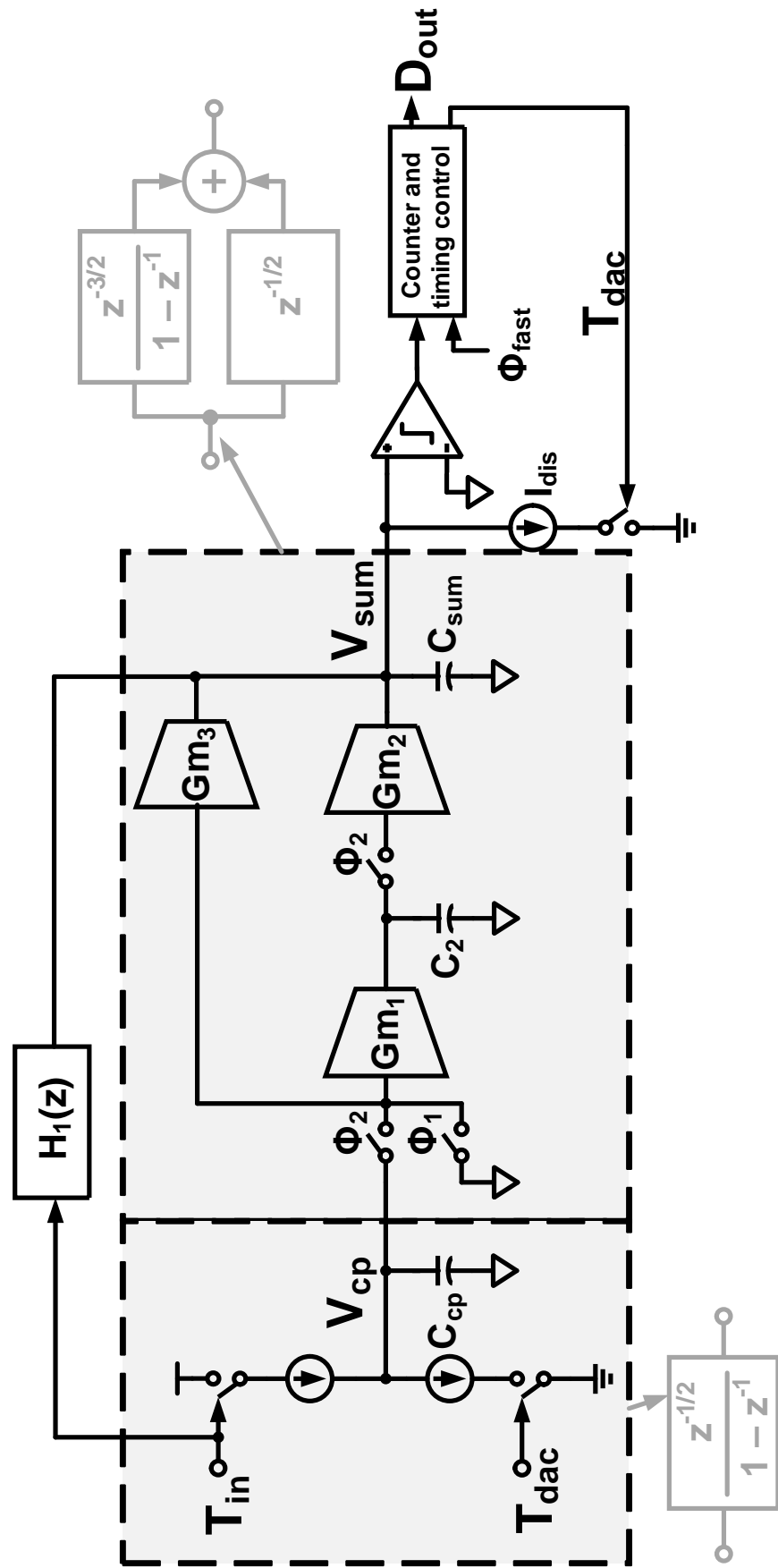
Figure 3.17: A 3rd order charge-pump based $\Delta\Sigma$ TDC.

The next section talks about the circuit level implementation of some of the important blocks in the $\Delta\Sigma$ TDC.

3.4 Circuit Implementation

This section discusses the circuit level implementation of the individual blocks used to build the third order $\Delta\Sigma$ TDC.

3.4.1 Charge-pump

The input charge-pump acts as a time subtractor as well as an integrator. Due to the feed-forward architecture used for the TDC, the main $\Delta\Sigma$ loop only processes quantization error, thereby relaxing the requirements on the loop components considerably. Also, any errors at the output of the charge-pump are first order noise shaped, thereby relaxing the design requirements of the charge-pump.

A current switched architecture for the charge-pump was chosen, with the current of the charge-pump either being pumped into the output nodes (V_{op}, V_{on}), or being directed into the common mode of the system [29]. The inputs to the charge-pump being T_{in} and T_{dac}. A single-ended charge-pump architecture would suffer from NMOS-PMOS mismatch, thereby seriously limiting the achievable SNDR. Therefore, a pseudo differential architecture was used to reduce nonlinearity from the charge-pump, as shown in Fig. 3.18.

Large device sizes were used to reduce the effects of mismatch and also reduce non-linearity due to small channel effects. Noise from the charge-pump is directly proportional to the on-time of the charge-pump and the analysis is done assuming that the charge-pump current sources were "ON" for half the duration of ϕ_1.

A scaled version of the pseudo-differential charge-pump was also used for the discharging current source (I_{dis}), which is used to discharge the summing capacitor.
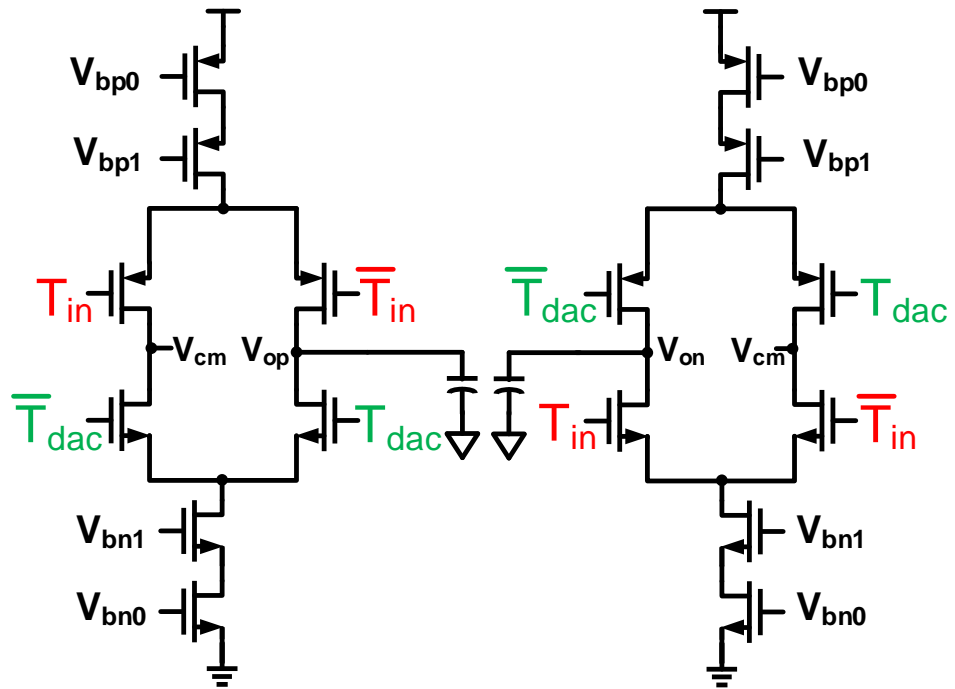
Figure 3.18: Current switched charge-pump.

3.4.2 Transconductors

Since the output of all the transconductors are at least second noise shaped, resistor degenerated transconductors, with wide bandwidth were used in the design [30]. The basic structure of the transconductor is shown in Fig. 3.19

Note that the transconductances of each stage were scaled appropriately based on their respective requirements.

3.4.3 Zero Crossing Detector

In this implementation of the TDC, the direction of discharge is always in the same direction. Therefore, the voltage at which the zero crossing happens is the
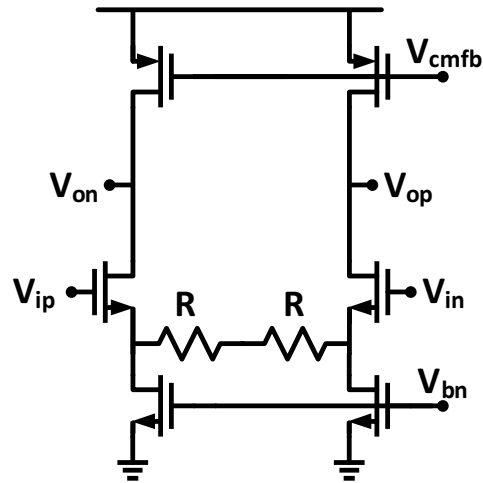
Figure 3.19: Transconductance.

same for all voltage inputs (i.e. a zero detection always happens at a differential input of zero), the zero crossing detector (ZCD) produces a constant time delay. In practice, however, finite ZCD gain and bandwidth result in a signal dependent delay for the ZCD for small inputs [31]. Therefore, in order to minimize these artifacts, a high gain wide bandwidth ZCD was used in the TDC. This ZCD was built by cascading low gain wide bandwidth amplifiers as shown in Fig. 3.20.
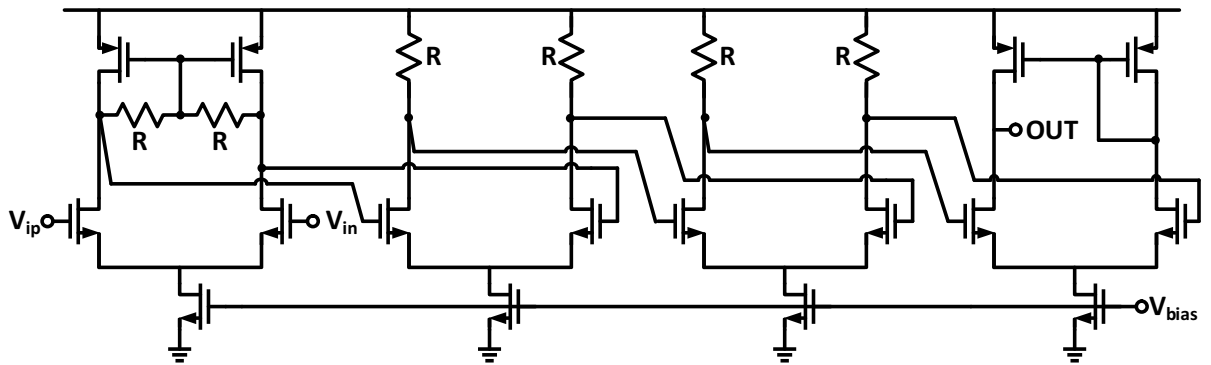
Figure 3.20: Zero crossing detector

Also, note that any signal dependent errors from the ZCD are second order

noise shaped by the loop filter as it occurs only in the later part of the loop. This further relaxes the design requirements on the ZCD.

3.4.4 Fast Clock

The number of fast clock edges in the time interval ϕ_1 directly determines the number of quantization levels of the TDC. Therefore, it is advantageous to increase the frequency of the fast clock as it reduces the signal content which is processed by the loop, thereby stabilizing the loop, while also improving the SQNR. However, it is not practical to inject a high frequency clock onto the chip as it would be difficult to synchronize the beginning of discharge cycle with the beginning of ϕ_1. Therefore, the fast clock is implemented using an on-chip voltage controlled delay line as shown in Fig. 3.21
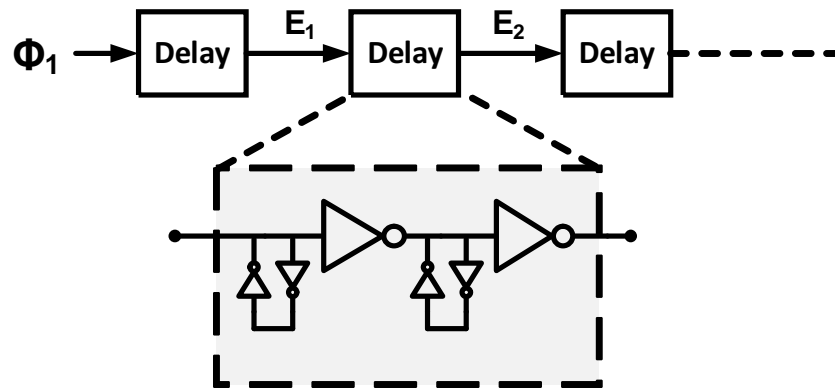
Figure 3.21: Delay line.

The delay line consists of a cascade of delay elements. Each delay element consists of two inverters, whose supply is controlled off-chip, thereby enabling the control on the delay value. The intermediate nodes of the delay element are restored to near full voltage levels using smaller back-to-back connected inverters

as shown in Fig. 3.21. The input to the delay line is the rising edge of ϕ_1, thereby synchronizing the beginning of discharge cycle with beginning of ϕ_1.

In this design, a delay chain of 24-elements was used, thereby making the number of quantization levels equal to 24.

3.4.5   Time to Digital Converter

The main operation of the TDC is to synchronize the zero crossing edge with one of the 24 fast clock edges. The simplest approach to perform this operation is shown in Fig. 3.22 [?].
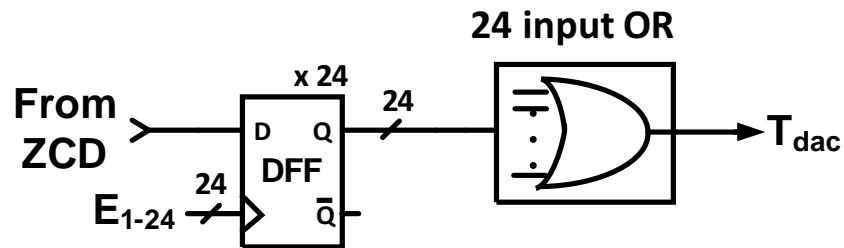
Figure 3.22: Basic time-to-digital converter.

As discussed in the earlier subsection, the fast-clock is implemented using a voltage controlled delay line (VCDL). The 24 edges of the VCDL (E_{1-24}) act as clocks to 24 DFFs. The input to these DFFs is the same, and is got from the ZCD. Once the zero crossing edge occurs, the output of one of the DFFs triggers high synchronously with one of the VCDL edges. The outputs of these 24-DFFs are "OR'ed" using a 24-input OR gate. Thus the output of the OR gate synchronizes the zero-crossing detector edge with one of the VCDL edges.

Unfortunately, the above architecture suffers greatly due to the signal dependent delay of the DFF. This problem is articulated in Fig. 3.23
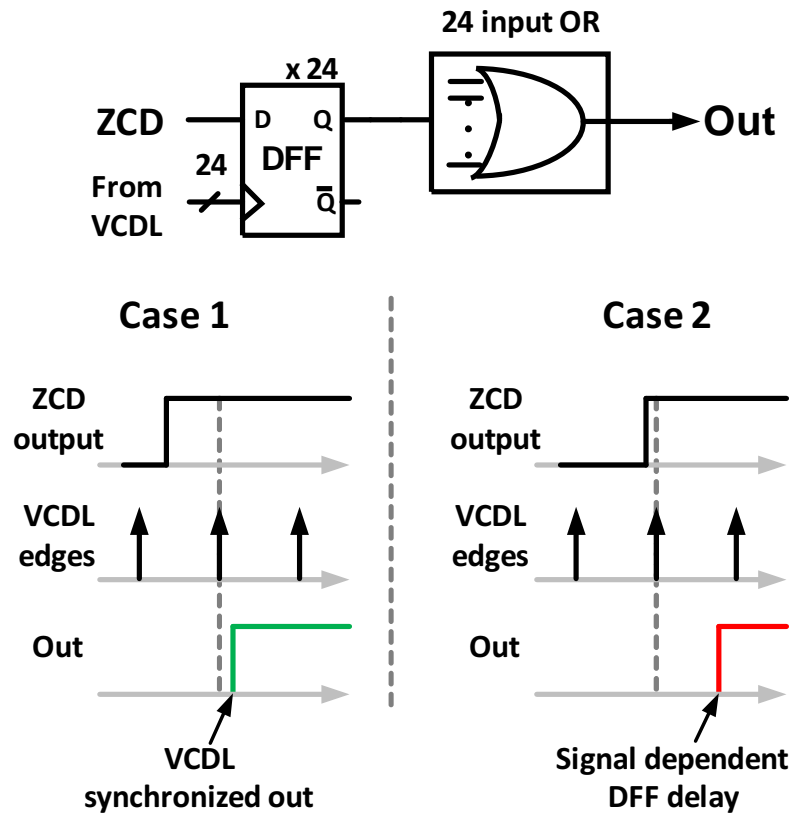
Figure 3.23: Signal dependent delay of DFF.

When the input to the DFF occurs well before a VCDL edge, i.e. well before the setup time of DFF, the delay of the DFF is fixed thereby synchronizing the input with the VCDL edge. This is shown in Case 1 of Fig. 3.23. However, more often than not, the input edge occurs very close to a VCDL edge, thereby making the delay of the DFF signal dependent. Therefore, the output of DFF is no longer synchronous with a VCDL edge, thereby defeating the purpose of the TDC. This phenomenon is shown in Case 2 of Fig. 3.23. Fortunately, an alternative architecture exists which can mitigate the problem of signal dependent DFF delay and this is shown in Fig. 3.24.

The solution makes use of a two level time-staggered DFF and latch [32].
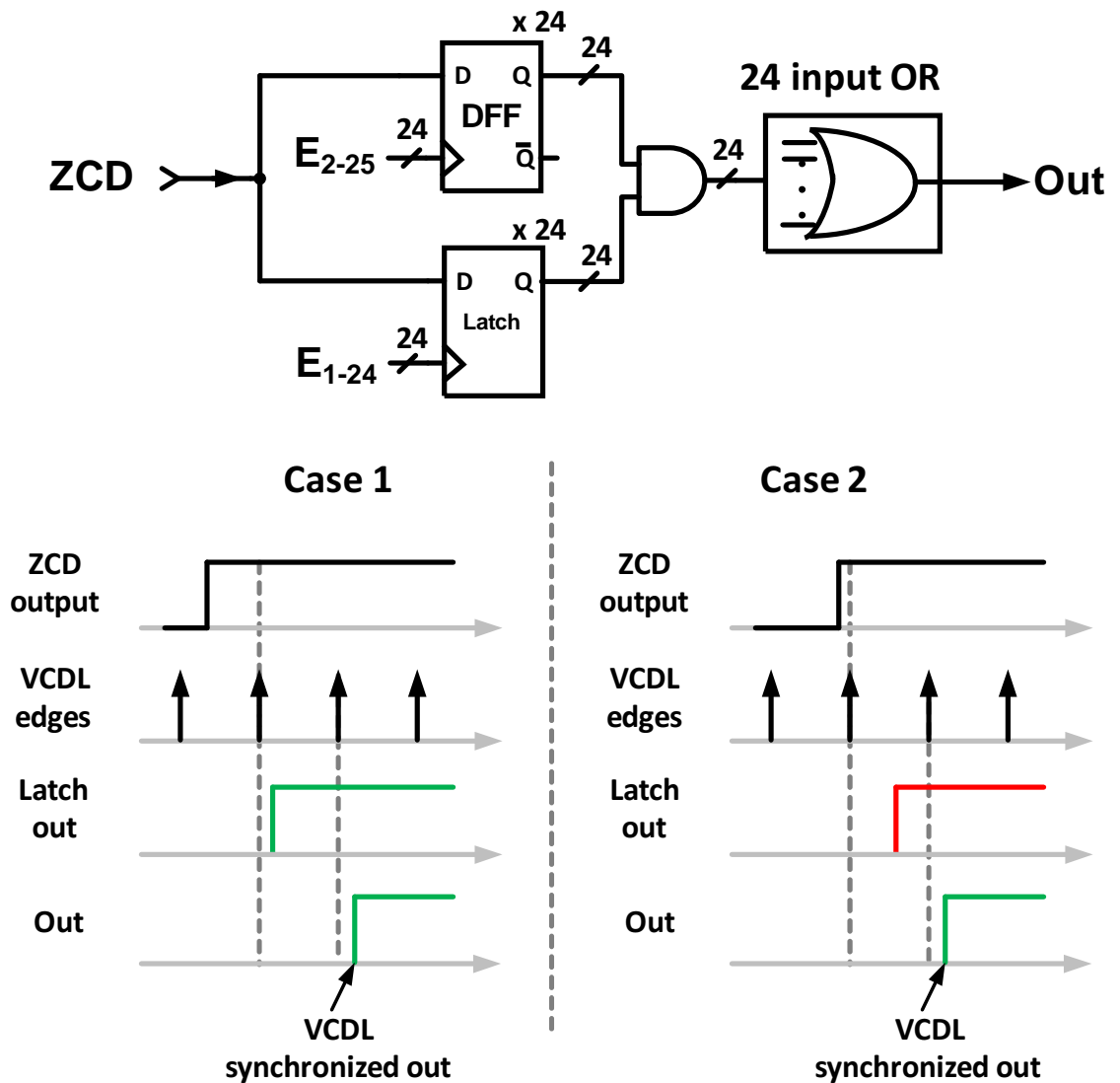
Figure 3.24: (a)Time-to-digital converter. (b) Timing diagram.

The input to the DFF and latch is recieved from the ZCD, while their clocks are time staggered as shown in Fig. 3.24. In case 1, the zero crossing edge is far from the VCDL edge. Therefore, the output of the latch and that of the OR gate are synchronous with a VCDL edge. In case 2, when the zero crossing edge is close to the VCDL edge, the output of the latch suffers from signal dependent delay.

However, the output of OR is still synchronous with a VCDL edge due to time staggering i.e. the DFF triggers only on the next VCDL edge thereby making the output of the AND gate and hence the OR gate synchronous with a VCDL edge. Also, the latches are designed such that the setup time is reduced. Note that the problem of input dependent delay is greatly reduced, but not completely removed [33, 34].

Note that the penalty of using the above time staggering approach is that the architecture introduces one extra delay in synchronizing the zero crossing edge with VCDL edge.

3.5 Non-idealities

The $\Delta\Sigma$ TDC, due to its noise-shaping properties, is immune to some circuit non-idealities and not so immune to others. This section discusses some of the important non-idealities which need to be carefully considered in building the noise-shaping $\Delta\Sigma$ TDC.

3.5.1 Zero Crossing Detector

The zero crossing detector(ZCD) compares the voltage of V_{sum} with zero, and triggers once a zero crossing has been detected. There are two aspects of the zero crossing detector which need to be considered. (1) Comparator noise and (2) Comparator delay.

Comparator Noise

The analysis of the comparator noise is similar to the comparator-based circuits [35], with the main difference being that the reference voltage at which the zero crossing happens and the discharging slope are fixed for all cycles. If the zero crossing happens towards the middle of the fast clock, the noise will have no effect on the performance of the TDC because the discharging will stop only at the next fast-clock edge (shown in green in Fig. 3.25). In the case where the zero crossing edge happens close to the fast-clock edge, the comparator noise could change when the zero crossing happens, and hence the discharge can take place for one extra cycle/ one less cycle. This is shown in red in Fig. 3.25. Note that this phenomenon is equivalent to that of comparator noise in a flash ADC.
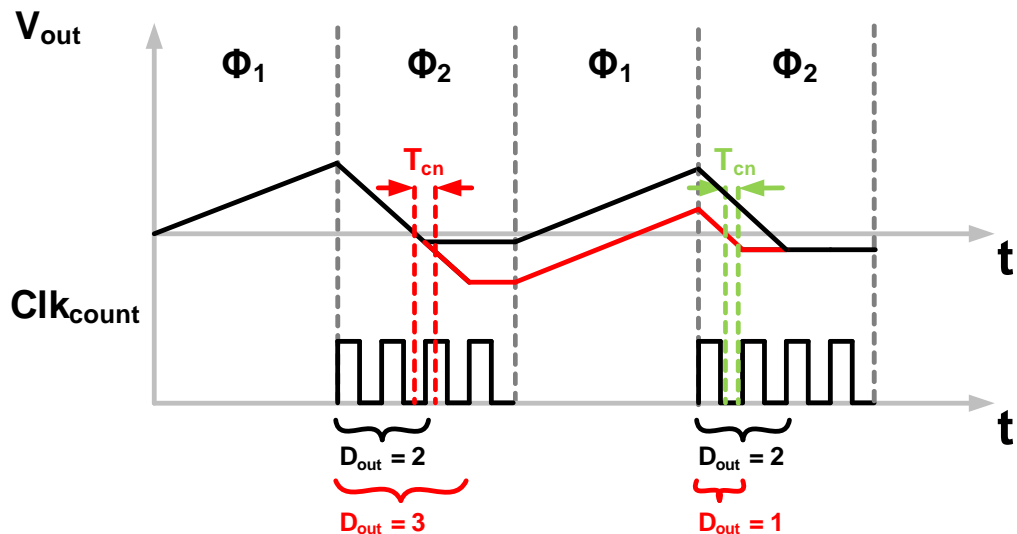
Figure 3.25: Effect of comparator noise on TDC decisions.

In a flash ADC, this would mandate the comparator be designed such that the noise of the comparator be less than LSB/2. Luckily, this is not a big problem in the TDC architecture as the noise in the comparator is added towards the end-of the $\Delta\Sigma$ loop, and hence it is noise shaped. For the above third order system, the

comparator noise is second order noise-shaped. In other words, the comparator noise sees a high pass transfer function, thereby relaxing the design requirements on the comparator and reducing the power consumption. A simple example as shown in Fig. 3.25 illustrates that the error in the dual-slope is high pass filtered i.e. on average the error is removed.

Comparator Delay

The other important aspect, in designing the comparator, is the comparator delay (t_{delay}). The delay acts like a fixed offset since the reference voltage at which the zero crossing happens and the discharging slope are fixed for all cycles. This effect is shown in Fig. 3.26. The signal path in black shows the charging and discharging phases when the comparator is ideal and has zero delay. The curve in red shows the case where the comparator delay is non-zero.
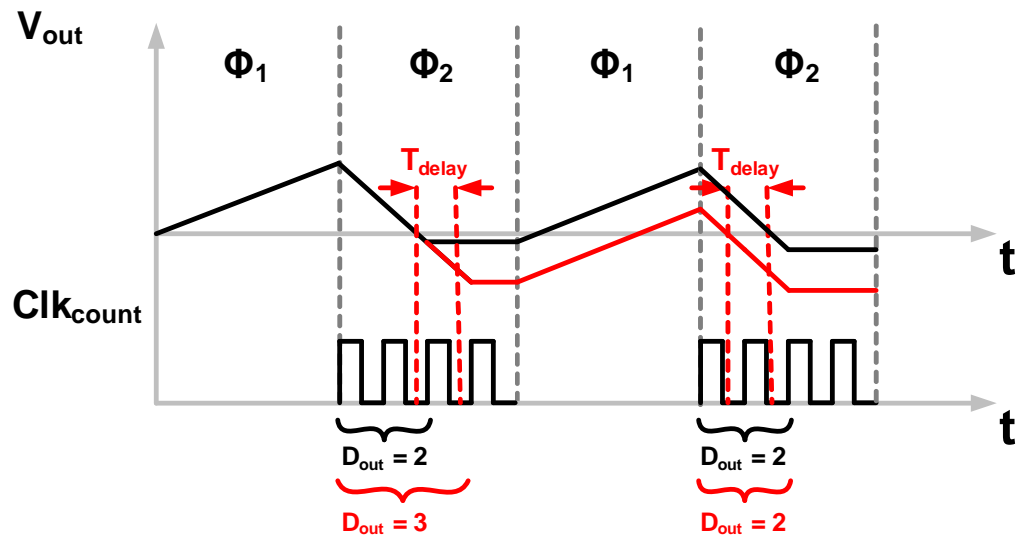
Figure 3.26: Effect of comparator delay on TDC .

However, one interesting effect of comparator delay is observed in Fig. 3.26. Given that the feedback element in the $\Delta\Sigma$ modulator is time information, the

$\Delta\Sigma$ loop ensures that the average value which is feeded back is equal to the average value of the input. Therefore, the value of the comparator delay is absorbed into the loop, and the overall value of D_{out} (in other words T_{dac}) will follow the input T_{in} on the average sense. This interesting property is observed in Fig. 3.26 wherein the value the value of D_{out} is the same after the first cycle onwards. This is because the loop absorbs the delay of the comparator.

3.5.2 Delay Element Mismatch

Delay element forms one of the key blocks in $\Delta\Sigma$ TDC. Since the delay elements are used to build the fast-clock, which are used for counting as well as providing feedback DAC information, any mismatch in them would directly affect the overall performance of the $\Delta\Sigma$ TDC. Mismatch in the delay elements directly translates to mismatch in the time steps. The mismatch in time steps has impact in two different places (1) Mismatch in discharge time steps (2) Mismatch in DAC feedback value.

Mismatch in Discharge Time Steps

Mismatch in discharge time steps is equivalent to mismatch in the flash quantizer typically used in $\Delta\Sigma$ ADCs and is very similar to the effect of comparator noise on $\Delta\Sigma$ TDC. In the case of noise-shaping quantizer, it effectively means the amount of discharge time is not directly proportional to the D_{out}, but instead suffers from mismatch. For example, assume $D_{out} = 2$ corresponds to a time step of width 20ns, then ideally $D_{out} = 3$ would correspond to a time step of width 30ns. But due to mismatches in the delay elements, it could so happen that $D_{out} = 3$ would correspond to a time step of width 31ns. This would mean that the voltage

on the summing node has an error, whose value is proportional to the mismatch in the delay line. Fortunately, as in a conventional $\Delta\Sigma$ ADC, the mismatches in comparator time steps are noise shaped by the loop filter, and therefore have little/no effect on the performance on the overall TDC as shown in Fig. 3.27.
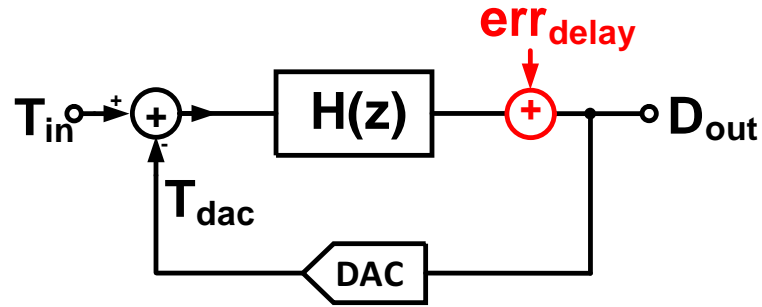
Figure 3.27: Effect of mismatch in discharge time steps

H(z) represents the loop filter in Fig. 3.27 and err_{delay} represents the error due to mismatch in the delay line. H(z) is a low pass filter, therefore the transfer function of err_{delay} due to mismatch in time steps is given by eq. 3.16

$$TF_{err_{delay,time-step}} = \frac{1}{1 - H(z)} \tag{3.16}$$

where $TF_{err_{mismtach}}$ is a high pass filtered, thereby reducing the impact of mismatch in discharge time steps on the overall performance of the TDC.

Mismatch in DAC Feedback Value

Mismatch in delay elements also implies mismatch in the DAC feedback value as the feedback pulse is directly equal to the amount of discharge time. This has a profound impact on the performance of the TDC, as any errors in the DAC feedback value would be directly represented at the output, as it sees a low pass transfer function, thereby massively impacting the overall performance of the TDC. Figure 3.28 illustrates this point.
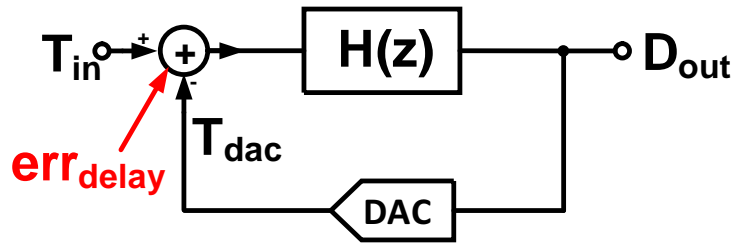
Figure 3.28: Effect of mismatch in DAC feedback path

The transfer function of err_{delay} due to mismatch in the DAC feedback value is give by eq. 3.17

$$TF_{err_{delay,dac}} = \frac{-H(z)}{1 - H(z)} \tag{3.17}$$

where $TF_{err_{delay,dac}}$ is a low pass transfer function, and therefore has a huge impact on the performance of the ADC. Note that the overall transfer function of the mismatch in delay line is obtained by combining equations 3.16 and 3.17.

$$TF_{err_{delay}} = \frac{1}{1 - H(z)} + \frac{-H(z)}{1 - H(z)} \tag{3.18a}$$

$$= 1 \tag{3.18b}$$

The above equation suggests that delay line design is one of the most critical designs for the overall performance of the TDC. Therefore, for this test chip, care has been taken to reduce the mismatch in the delay line to acceptable value. This was done by using larger device sizes (as mismatch α 1/Area) and also making the layout of the delay line as symmetric as possible, thereby reducing the possibility of any deterministic mismatches. Extensive monte-carlo simulations were run to ensure that the overall performance of the TDC is not limited due to the mismatch in delay line. Also, to reduce the effect of dynamic mismatches, huge decoupling

capacitors were used on the delay line supplies.

3.5.3   Clock Jitter

Systems which rely upon continuous time input sampling/continuous time discharging and are synchronized with an external clock are always prone to effects of clock jitter [36]. Continuous time $\Delta\Sigma$ ADCs (CTDSM) are the best examples of systems in which clock jitter has a massive impact on the performance of the ADC [37]. In CTDSM ADCs, the feedback DAC is a pulse whose duty cycle depends on the clock pulse width, thereby any noise in the clock i.e. any jitter present in the clock will directly effect the overall performance of the ADC.

In the case of $\Delta\Sigma$ TDC, the jitter in the main clock has little effect on the performance of the TDC, as it only delays the beginning of the discharge pulse. That is, even though the beginning of discharge pulse is shifted, so are the VCDL edges. Hence the pulse width due to the main clock jitter will not effect the overall performance of the TDC.

However, any noise in the VCDL edges would severely hamper the performance of the TDC, as the noise in the VCDL edges is equivalent to the noise in the feedback DAC. Since any noise in the feedback DAC directly effects the performance of the TDC, care must be taken in the design of the VCDL, such that the noise in the delay line meets the overall specifications of the TDC.

3.6 Measured Results

3.6.1 Test Setup

Time to digital converters are notoriously difficult to characterize. The fundamental reason for this being the inability to generate a clean time input to test the TDC. Therefore, in order to avoid this predicament, a on-chip test setup was used to characterize the performance of the TDC. The on-chip test setup uses a standard dual-slope ADC, in which the zero crossing edge represents the value of input in time-domain. This information was given as an input to the TDC and hence used to characterize the TDC. The other advantage of using the dual-slope ADC for testing is that it synchronizes the time input with the clock edge, thereby easing the efforts of testing. The on-chip dual-slope ADC architecture is shown in Fig. 3.29

During phase ϕ_1, the input along with an offset is summed onto the summing capacitor. Using a constant reference, the summing capacitor is discharged at the beginning of ϕ_2 until the zero crossing edge is detected. The discharge time is directly proportional to the value of input. This time input is used by the TDC. Note that the summing capacitor is reset before the beginning of next cycle ϕ_1.

3.6.2 Measured Results

The TDC achieves a peak SNDR of 67dB and dynamic range of 71dB while consuming 2.58mW (1.3mW analog and 1.28mW digital). This translates to a modulator with 3ps of resolution over a 5.55ns time range with 2.81MHz signal BW. The above numbers are calculated by taking the peak SNDR. Figure 3.30
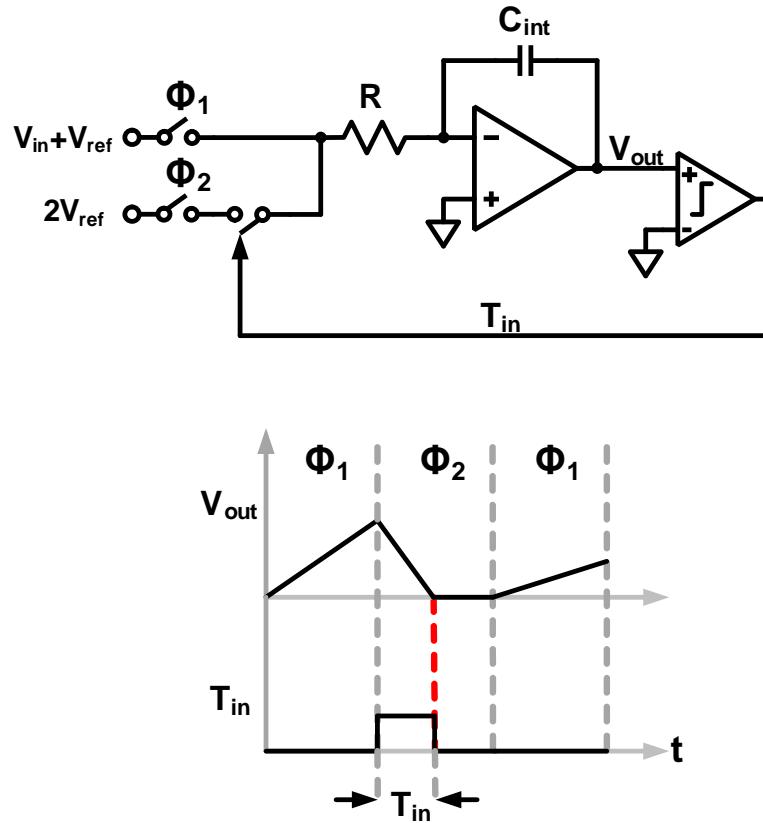
Figure 3.29: Dual slope ADC reconfigured to give time input to the TDC.

shows the frequency spectrum for a large time input. The spectrum shows a dominant second harmonic, which is confirmed as being generated by the on chip V-T converter. Nevertheless, the SNDR includes this second harmonic (without it the SNDR would have been 3dB better).

Figure 3.31 shows the measured spectrum for a small input. The output spectrum for smaller input amplitude and it shows no tonal behavior.

Figure 3.32 shows the measured SNDR vs. input amplitude plot.

The die photo is shown in Fig. 3.33.
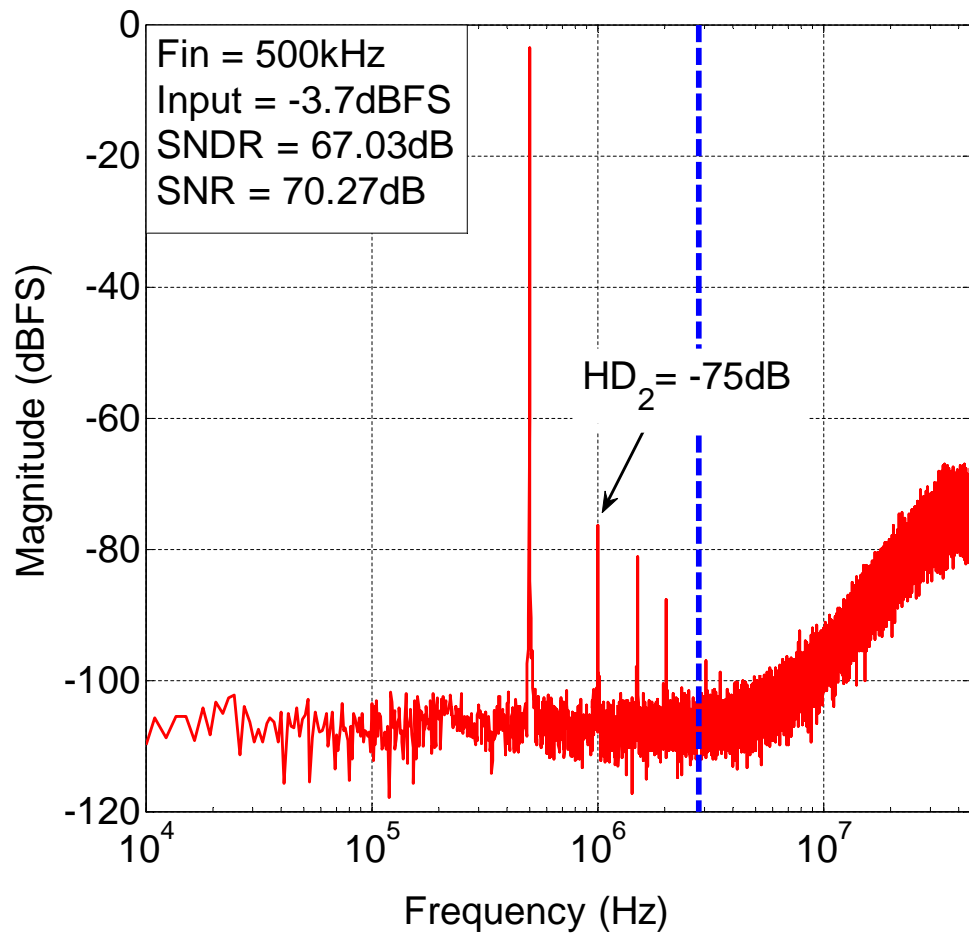
Figure 3.30: Measured spectrum for large input.
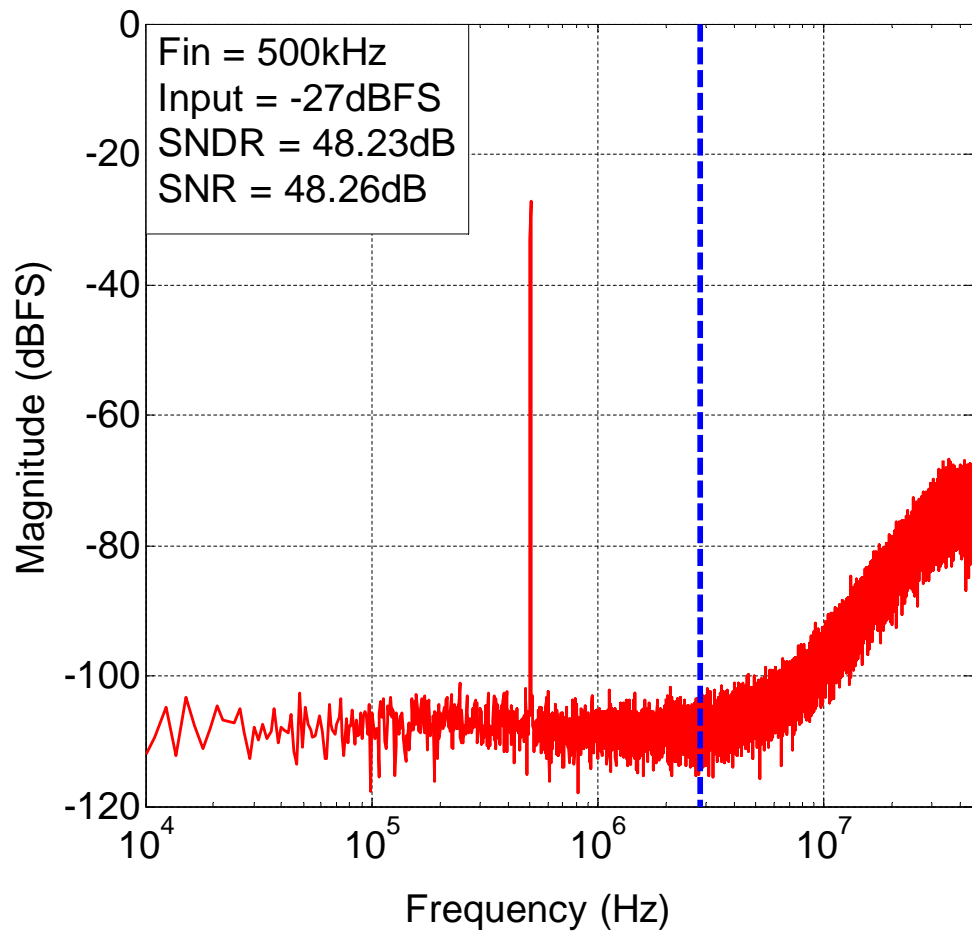
Figure 3.31: Measured spectrum for small input.
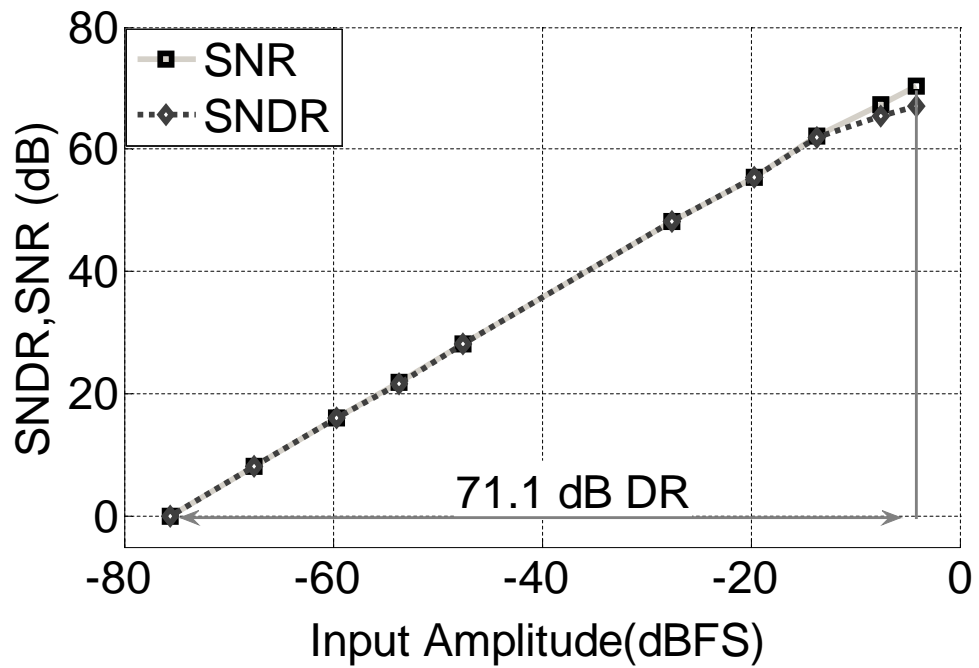
Figure 3.32: SNDR vs. input amplitude.
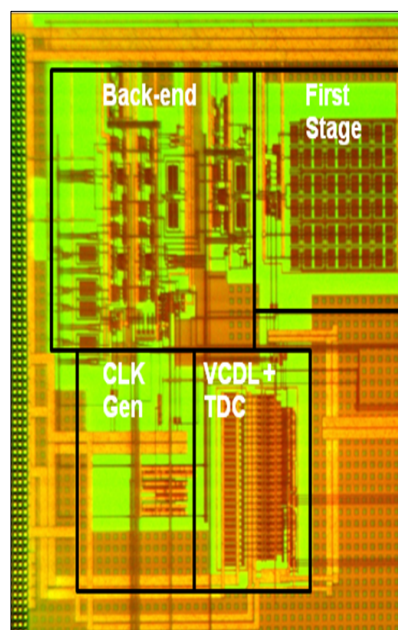
Figure 3.33: Die Photo

3.6.3 Explanation for Observed Harmonic Distortion

As explained in the earlier subsection, the test setup relies on the dual-slope ADC to produce a time input. Therefore, the performance of the TDC would be limited by the performance achievable by the dual-slope ADC. In other words, the TDC would not be able to remove any non-linearity added by the dual slope ADC. This postulation was confirmed by using a simple test setup. This is understood by looking at an interesting property of the dual-slope ADC as shown in Fig. 3.34.
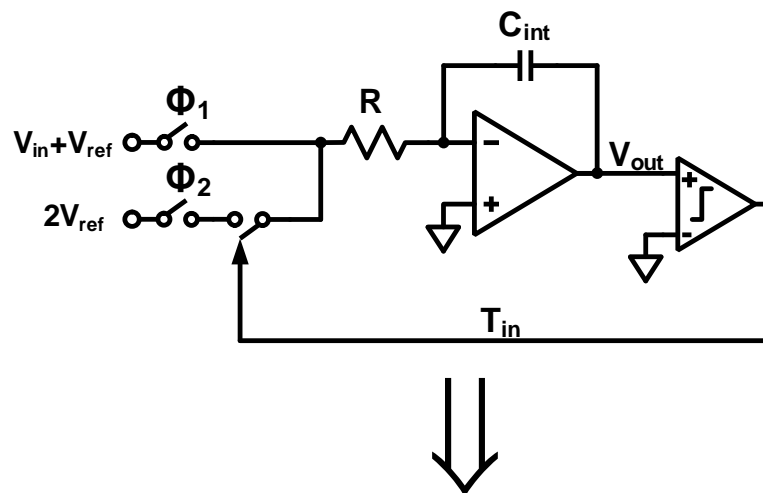
V-T Convertor Operation		
Ref	Input	T_{in}
V_{ref}	V_{ref} 0 $-V_{ref}$	5.55ns 2.77ns 0
0.6 V_{ref}	0.6 V_{ref} 0 -0.6 V_{ref}	5.55ns 2.77ns 0

Figure 3.34: Effect of scaling reference for a dual-slope ADC

When the input and reference are scaled by the same factor, the T_{in} to the dual slope ADC remains unaltered. Therefore by scaling to a lower value, one could reduce the non-linearity from the dual slope ADC, but at the penalty of increased noise. This is exactly depicted from the measured results as shown in Fig. 3.35.

Figure 3.35 shows lower non-linearity for lower reference value thereby confirming the fact that the source of nonlinearity was the test setup, rather the TDC in itself.

Ref = V$_{ref}$

Ref = 0.6V$_{ref}$
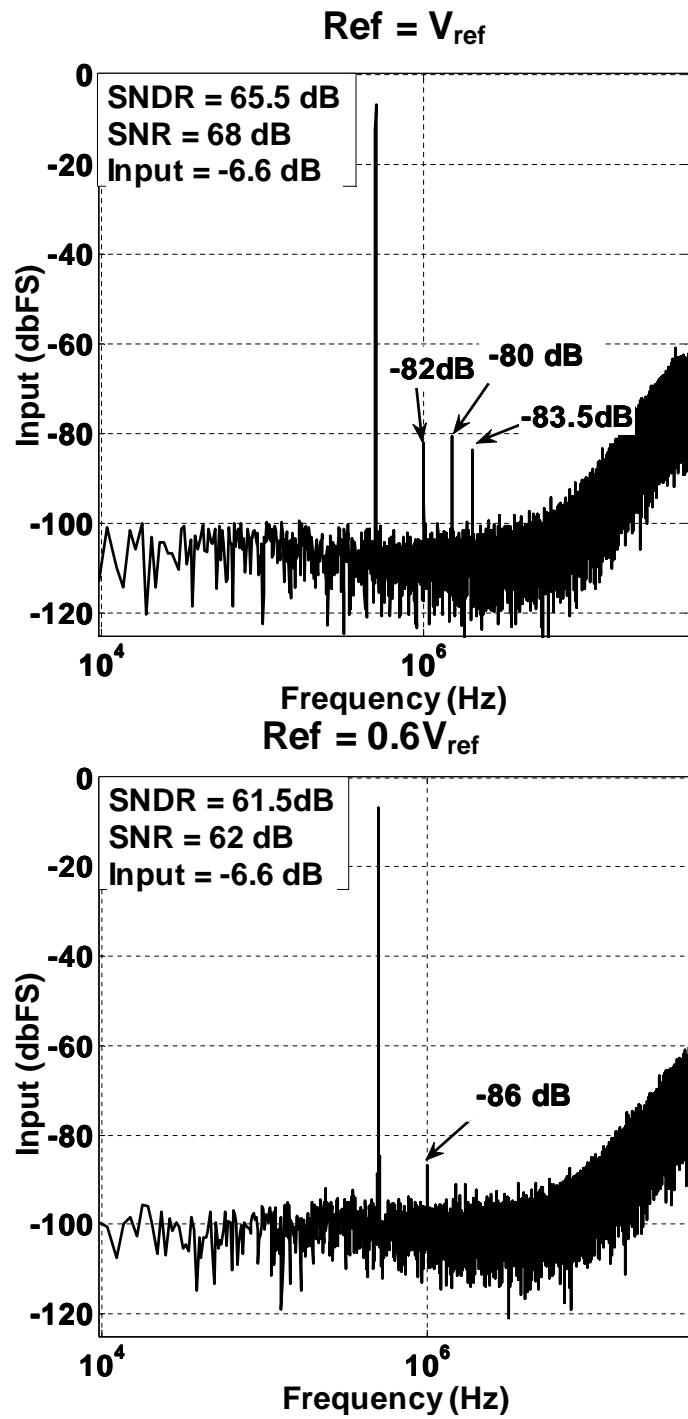
Figure 3.35: Effect on output spectrum by scaling the reference and input in dual-slope ADC

3.7 Summary

In this chapter, a novel TDC architecture is proposed and the measured results are presented. The proposed $\Delta\Sigma$ TDC uses an explicit feedback DAC. The TDC achieves a 3ps resolution over 5.55ns for an input BW of 2.81MHz. Table 3.1 summarizes the performance of the TDC while comparing the performance to other TDCs.

Present day TDCs are limited in peak SNDR performance/characterization due to lack of suitable test equipment. Therefore an alternative figure of merit is proposed. The proposed FOM_{TDC} is give as

$$FOM_{TDC} = \frac{power}{2 * BW * 2ENOB_{DR}} \qquad (3.19)$$

where $ENOB_{DR}$ is ENOB based on the measured dynamic range.

Table 3.1: Summary of performance and comparison with existing architectures

Reference	This Work	[15]	[20]	[22]
Technology	$0.13\mu m$	$0.13\mu m$	$0.13\mu m$	90nm
Supply Voltage	1.2V	1.5V	1.2V	1.2V
Sampling Rate	90MHz	100MHz	50MHz	156MHz
Signal Bandwidth	2.81MHz	1MHz	1MHz	1MHz
Dynamic Range	71dB	95dB	68dB	70dB
Peak SNDR Measured	67.02dB	-	60dB	$\leq$ 50dB
Power	2.58mW	21mW	1.7mW	2.1mW
Area	$0.425mm^2$	$1mm^2$	$0.11mm^2$	$0.11mm^2$
FOM_{TDC}	159fJ/step	200fJ/step	409fJ/step	399fJ/step

CHAPTER 4. BACKGROUND ON DIGITAL CALIBRATION ALGORITHMS FOR NONLINEARITY CORRECTION IN ADCS

4.1   Introduction

In most systems, nonlinearity is an undesired phenomenon in which the output of the system is not linearly related to the input. This phenomenon leads to the creation of new signal frequencies at the output. In case of single tone input, nonlinearity manifests itself as harmonic distortion, while in wideband systems nonlinearity causes harmonic distortion and intermodulation distortion. Equation 4.1 shows a system which suffers from third order non-linearity.

$$y_{out} = \alpha_1 \times x_{in} + \alpha_3 \times x_{in}^3 \tag{4.1}$$

In the above equation, y_{out} is the output of the system, x_{in} is the input, and α_1, α_3 are the linear term and third-order distortion term respectively. For a single tone sinusoid input, the output of the above system has both the input tone as well as third-harmonic term.

In many practical systems, nonlinearity is highly undesirable as it interferes with the existing signal, thereby corrupting the existing signal content. One important example is an RF system, wherein nonlinearity in LNA can result in cross-modulation and intermodulation terms which fall into the signal band, thereby

corrupting the original signal [38].

Most analog circuitry exhibits harmonic distortion to an extent and ADCs are no exception to this. Figure 4.1 shows an example of ADC which suffers from second and third harmonic distortion.
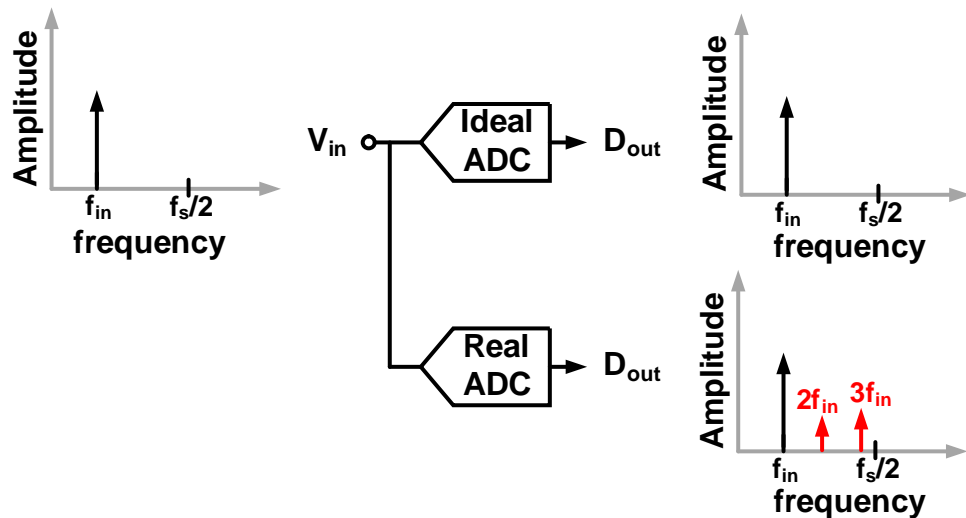
Figure 4.1: Need for calibration.

As shown in Fig. 4.1, when the input to an ideal ADC is a single tone sinusoid, the output is also a single tone sinusoid. If not carefully designed, practical ADCs can suffer from significant nonlinearity, which result in harmonic distortion for a single tone sinusoid. The real ADC shown in Fig. 4.1 suffers from second and third order nonlinearity, thereby the resulting output consists of second and third harmonics along with the original signal tone. This is clearly undesirable and needs to be avoided.

There are a variety of reasons which contribute to non-linearity in any type of ADC. Modern day CMOS processes are characterized by scaling in terms of geometry and supply voltages. Scaling happens with digital design in perspective, thereby complicating the design of high-resolution, high-performance ADCs.

Shrinking geometries tend to reduce the intrinsic gain of MOS transistors, making it difficult to realize high DC gain and wide bandwidth amplifiers. This complicates the design of high performance ADCs. To counter this problem, ADCs which are more digital in nature are being favored in smaller geometry processes. Successive approximation ADCs (SAR) [39, 40] and digitally calibrated ADCs [41, 42, 43, 44, 45, 46] fit the bill perfectly.

Amplifier nonlinearity and capacitor mismatches in pipeline ADCs, capacitor mismatches in SAR ADC, amplifier nonlinearity, quantizer nonlinearity, and DAC nonlinearity in $\Delta\Sigma$ ADCs are a few examples of challenges present in today's ADCs, which if not carefully accounted for could lead to nonlinearity in the system. These issues can be resolved in the analog or digital domain. Analog domain solutions for the above issues include using larger capacitors for better matching or high loop gain, wide bandwidth and low distortion amplifiers [47, 48] or using feedback loops [49, 50, 51, 52], which unfortunately are power intensive and are also becoming increasingly difficult to design in modern day CMOS processes.

On the other hand, reduced gate delays and ease of portability across processes make digital calibration for analog imperfections very attractive in modern day CMOS processes. However, there are only a handful of digital calibration techniques which can remove nonlinearity in ADCs [39, 41, 42, 43, 44, 45, 46]. Note that gain error and capacitor mismatch calibration in pipeline ADCs [53, 54, 55] is different from nonlinearity correction. The remainder of the chapter elaborates on a few prior nonlinearity correction architectures.

4.2 DAC based Calibration Technique

One of the earlier nonlinearity calibration techniques makes use of a dedicated DAC for calibration [45]. The basic structure of the technique is shown in Fig. 4.2.
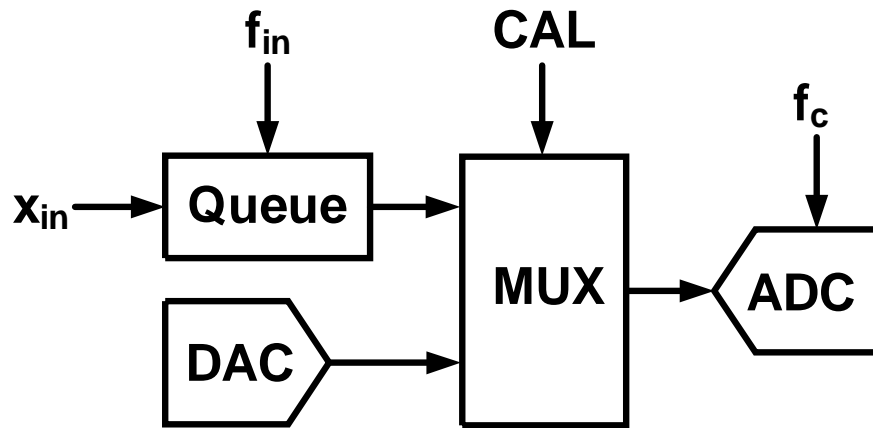
Figure 4.2: DAC based calibration technique.

The calibration technique is similar to the queue-based technique as described in [56]. The input x_{in} is sampled at a rate of f_{in}, while the ADC is clocked at a higher rate f_c, which is necessary for background calibration. The timing diagram for the operation is shown in Fig. 4.3. Impulses in f_{in} indicate instances when the queue begins sampling the input. f_c impulses indicate when the ADC can begin converting a sample. The flag signal FULL indicates the time when the input is available for sampling for the ADC and is held high until the sample is completely transferred to the ADC. Once the signal is transferred to the ADC, the flag FULL is turned low. Since $f_c > f_{in}$, there will be instances when the ADC is ready to convert, but there is no input available (i.e. FULL is low). During these instances, the MUX gives in the DAC value as the input to the ADC which is used to perform the calibration.
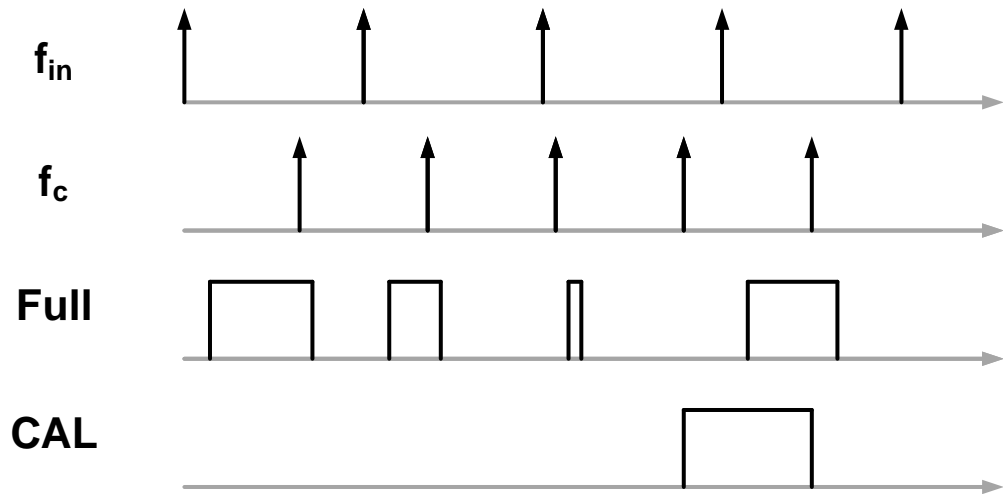
Figure 4.3: Timing diagram for DAC based calibration technique.

The DAC value is assumed to be ideal and is used to calibrate for the nonlinearity. This is done by giving two known DAC codes, DAC_1 and DAC_2, through the DAC to the ADC. If the ADC is ideal, then the difference of the digital output of the ADC is equal to the difference in the DAC codes,

$$err = [D(DAC_1) - D(DAC_2)] - [DAC_1 - DAC_2] \qquad (4.2)$$

The above error is used to estimate the nonlinear distortion coefficient by using a LMS engine and varying DAC_1 and DAC_2 to cover the entire range of the ADC.

This calibration algorithm has multiple drawbacks, as it needs an accurate DAC for calibration. The accuracy requirements on the DAC can be relaxed by using bootstrapping [45]. Also, for background mode, the ADC needs to operate at a higher conversion frequency, thereby leading to a power penalty.

4.3 Split ADC based Calibration Technique

This technique uses the concept of split ADC, wherein the existing ADC is split into near identical halves, and a known offset is given to both the paths as shown in Fig. 4.4 [46].
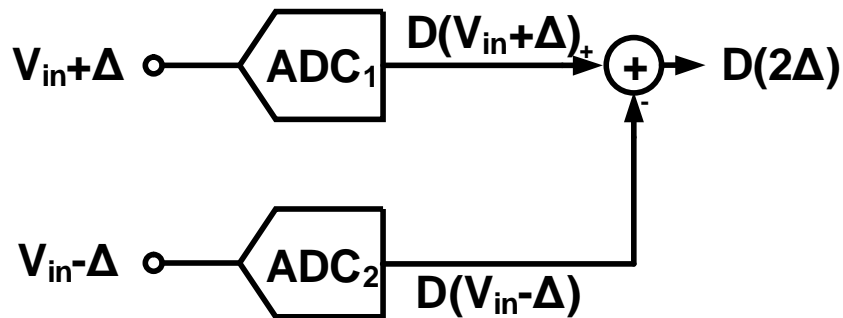
Figure 4.4: Split ADC based calibration technique.

The original ADC is split into two halves ADC_1 and ADC_2. The input to ADC_1 is V_{in} plus a known offset Δ, whereas the input to ADC_2 is V_{in} minus the offset Δ. The sum of the two digital outputs gives the final output of the system. On the other hand, the difference of the two outputs is a fixed word $D(2\Delta)$. In an ideal ADC, which does not suffer from nonlinearity, the value of $D(2\Delta)$ is fixed for all inputs and is equal to $D(2\Delta_{ideal})$. In the case where the ADCs suffer from nonlinear distortion, the value $D(2\Delta)$ varies from the known value. This error (the deviation) from the known value of $D(2\Delta_{ideal})$ could be used to calibrate for nonlinear distortion using an LMS engine.

The above algorithm can be operated in a background mode, and needs the value of Δ to be precisely known. Also, the above algorithm can only be operated to remove odd harmonics, i.e. even harmonic distortion cannot be removed, thereby limiting the range of applications which can use this calibration algorithm.

4.4 Straight line based Calibration Technique

This calibration technique calibrates for second and third order nonlinearity in a pipeline ADC and can be operated in both foreground mode and background mode [44]. For the purpose of calibration, the ADC is modeled as a third order polynomial and is corrected for third harmonic distortion. The basic underlying concept of this calibration technique is shown in Fig. 4.5.
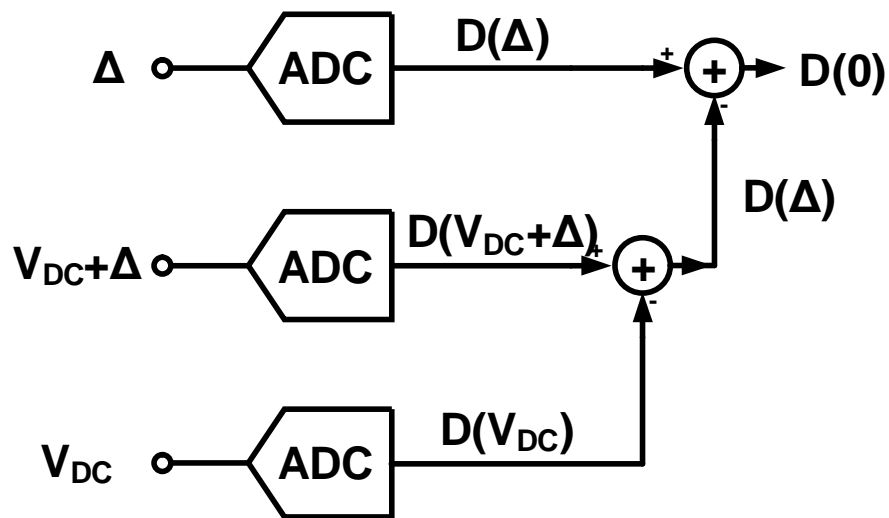
Figure 4.5: Straight line fit based calibration technique.

In the foreground mode, the input to the ADC is varied between V_{DC} and $V_{DC}+\Delta$. Ideally, the difference between the two digital codes $D(V_{DC}+\Delta)-D(V_{DC})$ is equal to a fixed value $D(\Delta)$. But due to nonlinearity present in the system, the difference deviates from the ideal value. Now the value of V_{DC} is varied across the entire input characteristics of the ADC as shown in Fig. 4.6.

The error term, which is given by the equation 4.3, is minimized over the entire range of the ADC by varying V_{DC} to remove 3rd order nonlinearity.
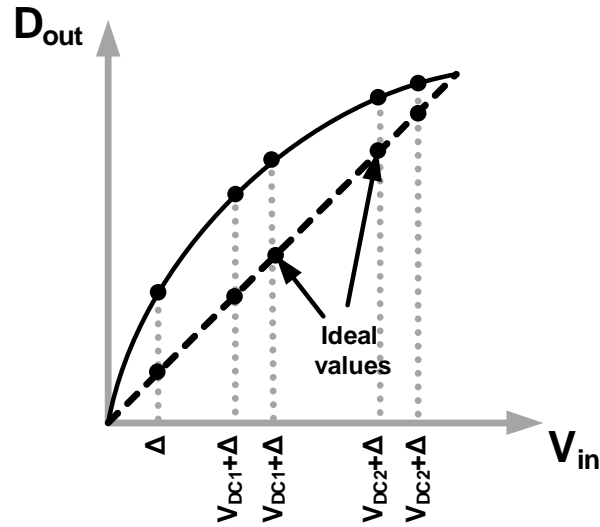
Figure 4.6: Varying V_{DC} over the entire range of ADC to estimate the mean value of the error.

$$\epsilon^2 = \sum_{j=1}^{128} [|D_{DC,j} - D_{DC,j,\Delta}| - D_{out,\Delta}]^2 \tag{4.3}$$

Also note that this calibration algorithm works from the back to the front. i.e. the back-end stages of the pipeline ADC are first calibrated before proceeding onto the front-end stages of the pipeline ADC.

The above algorithm can be extended to operate in background mode by using the skip and fill algorithm [57]. This method disrupts the normal operation of the ADC, and uses the skip and fill algorithm to compensate for the missing input code. As with any skip and fill algorithm, this method has an input frequency limitation.

4.5 Multiple Pseudo-random Number Based Calibration Technique

An interesting property of independent pseudo-random number sequences is that they are orthogonal to each other. i.e., if t_j for j=1,2,3.... represents independent pseudo random number sequences, then

$$\sum t_j \times t_k = \begin{cases} 0 & \text{if } j \neq k, \\ \neq 0 & \text{if } j = k \end{cases} \tag{4.4}$$

This property of pseudo random number sequences can be used to estimate nonlinearity in a ADC [41, 42].
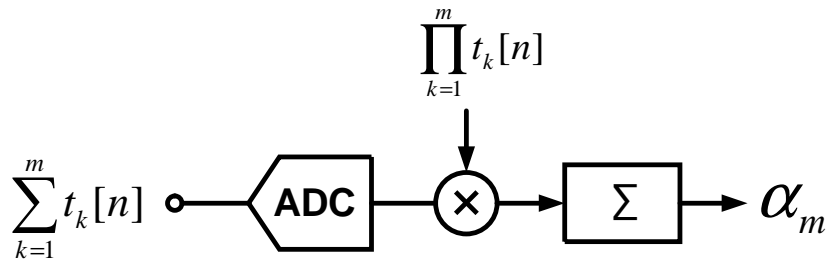
Figure 4.7: Pseudo random number based calibration technique.

Along with the input to the ADC, a sum of two-level independent pseudo-random sequences is given as an input to the ADC as shown in Fig. 4.7. The output of the ADC is multiplied by the product of these pseudo random number sequences to estimate the nonlinearity coefficient.

For example, consider a case where the ADC suffers from third order nonlinearity. In this case, a sum of three independent pseudo-random number sequences (t_1, t_2 and t_3) is added to the input. Since the ADC suffers from third order nonlinearity, the output consists of a term which is a product of the three sequences

$t_1 \cdot t_2 \cdot t_3$, and the coefficient of this term is proportional to the third order nonlinearity. Therefore, by multiplying the output of the ADC by the product of $t_1 \cdot t_2 \cdot t_3$, the third order nonlinear coefficient can be estimated.

The above algorithm can be extended to calibrate for multiple harmonics by multiplying the output with the appropriate sequence. However, the complexity of the algorithm increases with the increase in the nonlinearity order to be estimated. To estimate the fifth-order nonlinearity, five pseudo random number sequences needed to be generated and added to the input. This increases the complexity of the overall algorithm, while also reducing the input range to the ADC, thus making it unsuitable to calibrate for higher order nonlinearity.

4.6   Blind Calibration Based Calibration Technique

The majority of the existing nonlinearity correction architectures need an additional calibration input signal to aid with calibration. Also, some of the techniques described above are specific to an architecture and cannot be generalized to any type of ADC.

In the next chapter we describe a novel blind calibration technique which does not need any external calibration sequence and can be used to calibrate for both even and odd order nonlinearities. The proposed algorithm relies on the properties of downsampling and orthogonality of sinusoidal signals to estimate the harmonic distortion coefficients. The algorithm can be operated in both foreground and background modes to remove even and odd harmonics simultaneously.

CHAPTER 5. BLIND CALIBRATION ALGORITHM FOR NONLINEARITY IN ADCS

5.1 Introduction

In this chapter a blind calibration algorithm is proposed, which corrects for nonlinearity in analog to digital converters (ADCs). The proposed algorithm does not need any external calibration signal and is the first of its kind. The proposed algorithm relies on the properties of downsampling and orthogonality of sinusoidal signals to estimate the harmonic distortion coefficients. The algorithm can be operated in both foreground and background modes to remove even and odd harmonics simultaneously. The algorithm is demonstrated on a first-order ring oscillator based $\Delta\Sigma$ ADC, whose performance is limited due to nonlinearity.

Section 5.2 explains the necessary background for the algorithm and illustrates the working of the algorithm in a single harmonic case in a foreground mode. Section 5.3 illustrates how the algorithm can be extended to operate in background mode. In section 5.4, the algorithm is extended to calibrate for multiple harmonics simultaneously with section 5.5 describing the final architecture. Section 5.6 describes the operation of the implemented VCO based first order $\Delta\Sigma$ ADC. Section 5.7 talks about some of the implemented circuit level blocks with measurement results presented in section 5.8 and the paper being concluded in section 5.9.

5.2   Proposed Algorithm in Foreground Mode
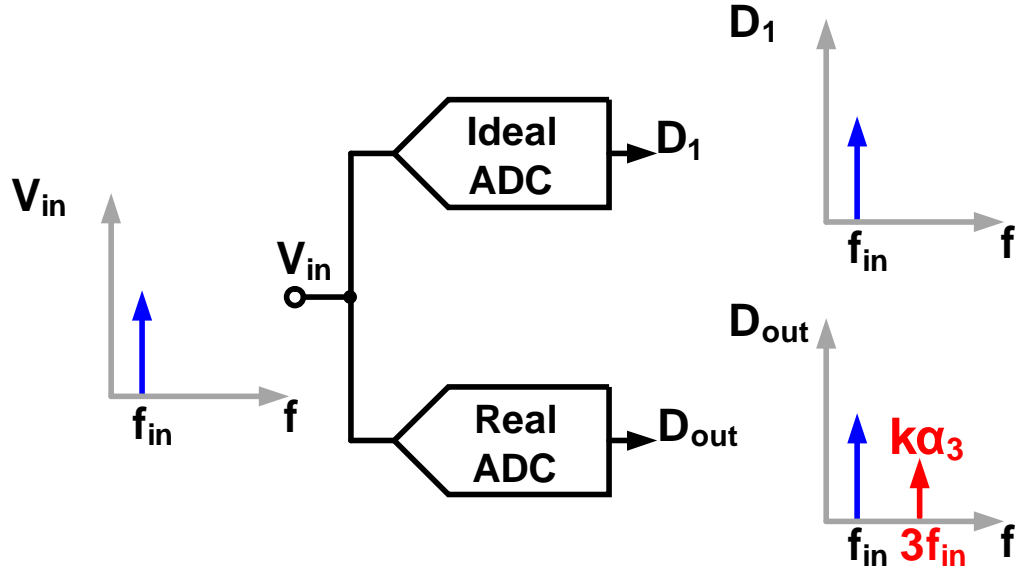
Figure 5.1: Single tone frequency response of ideal and non-ideal ADC.

Figure 5.1 shows the single tone frequency response of an ideal ADC and a non-ideal ADC, which has third harmonic distortion only. As shown, when a sinusoid (of frequency f_{in}) is given to an ideal ADC, the frequency spectrum of its digital output (D_1) consists of a single tone at f_{in}. When the same input is given to a non-ideal ADC which suffers from third order nonlinearity, the output (D_{out}) contains a tone at f_{in} and an additional harmonic distortion component at $3f_{in}$. The assumption that the non-ideal ADC suffers only from third order nonlinearity is for simplicity reasons only. This algorithm is not limited to single harmonic tones and can be used to calibrate for multiple harmonics simultaneously.

For the remainder of this section, the coefficient of distortion is assumed to be α_3. Therefore, the magnitude of harmonic distortion tone at $3f_{in}$ is proportional to α_3 ($k\alpha_3$). The non-ideal ADC is modeled as follows:

$$D_{out} = D(V_{in}) + \alpha_3 \times D(V_{in}^3) \tag{5.1}$$

where D_{out} is the output of the non-ideal ADC, and $D(V_{in})$ is the ideal digital representation of V_{in}. In the above setup, the source of distortion is not important i.e. the distortion could be due to any component in the entire system.

The proposed algorithm relies on two important signal properties (1) downsampling and (2) orthogonality of sinusoidal waves.

5.2.1 Downsampling

Downsampling is the process in which the the sampling rate of a signal is reduced [58]. In the time domain, downsampling leads to dropping of samples, whereas in frequency domain downsampling leads to input spectrum being spread out. If $D_{out}[n]$ represents the output sequence, the sequence which is downsampled by k is obtained by taking every third sample, that is

$$DS_k[n] = D_{out}[kn] \tag{5.2}$$

where $DS_k[n]$ is obtained by extracting every k^{th} sample. Figure 5.2 illustrates the relationship between $DS_3[n]$ and $D_{out}[n]$, where $DS_3[n]$ is obtained by downsampling $D_{out}[n]$ by 3.

Downsampling also affects the frequency response of the downsampled signal. The frequency response of the downsampled output is scaled up by the downsampling factor. This property can be expressed by the following equation,

$$X_{ds}(e^{j\omega}) = X_{out}(e^{j\omega/k}) \tag{5.3}$$
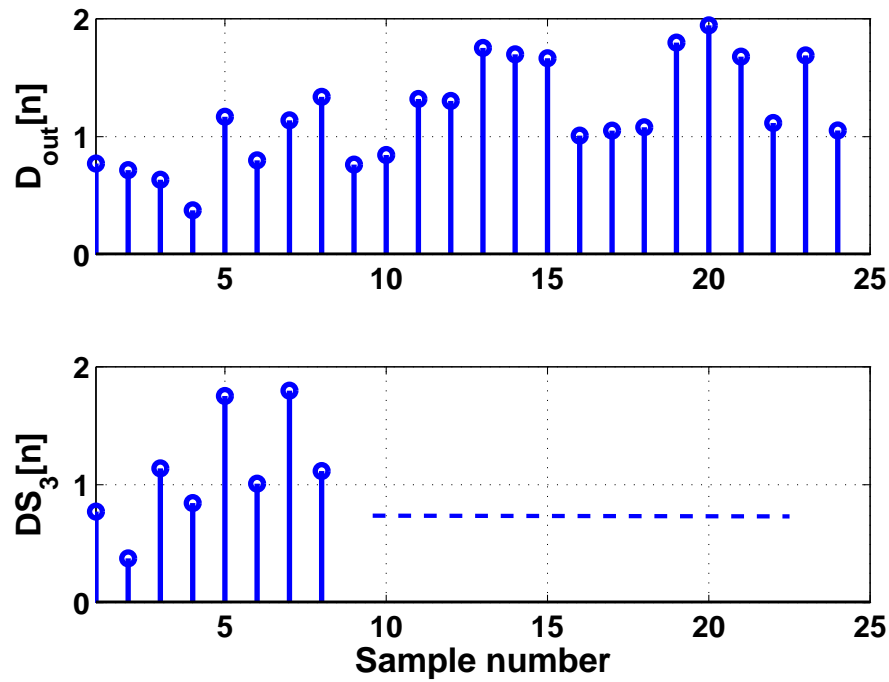
Figure 5.2: Relationship between $DS_3[n]$ and $D_{out}[n]$ in time domain.

where X_{out} is the fourier transform of D_{out} and X_{ds} is the fourier transform of DS_k (obtained by downsampling D_{out} by k). Figure 5.3 illustrates the effect of downsampling in frequency domain. It shows the frequency spectrum of $D_{out}[n]$ and $DS_3[n]$. As shown in Fig. 5.3, the original spectrum of D_{out} has tones at f_{in} and $3f_{in}$, while the downsampled spectrum has tones at $3f_{in}$ and $9f_{in}$. Note that the $3f_{in}$ tone in D_{out} and the $9f_{in}$ tone in DS_3 are due to the harmonic distortion present in the ADC.
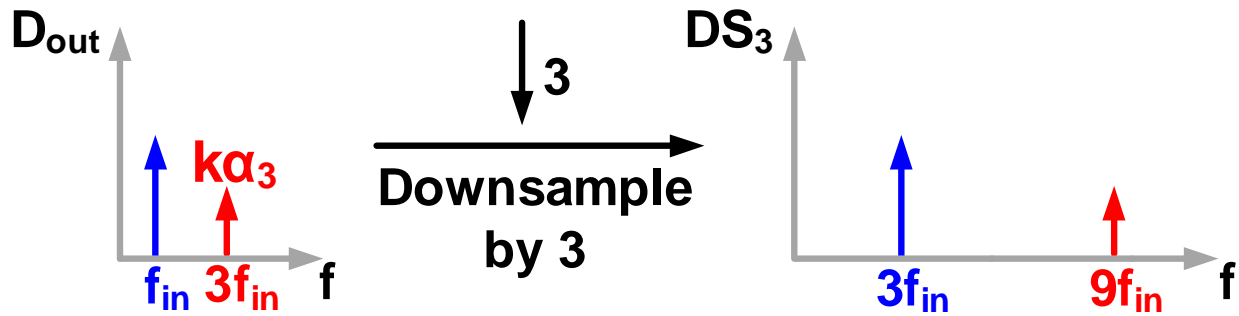
Figure 5.3: Effect of downsampling in frequency domain.

5.2.2 Orthogonality

A key property of sinusoidal waves is that they are orthogonal at different frequencies. In other words, the sum of the product of two sinusoids is zero if the two frequencies are different and is non-zero if the frequencies are same. i.e.

$$\int sin(f_1 t) \times sin(f_2 t) = \begin{cases} 0 & \text{if } f_1 \neq f_2, \\ \neq 0 & \text{if } f_1 = f_2 \end{cases} \tag{5.4}$$

This can be obtained by using the following identity

$$2sin(x) \cdot sin(y) = cos(x - y) - cos(x + y) \tag{5.5}$$

Using the property that the average of a sinusoid is equal to zero, when the above sum is integrated, the left hand side of the equation is non-zero if and only if x = y. Else the average is zero. Similarly, this property can be extended to discrete sinusoid waves, and the property is shown in eq. 5.6.

$$\sum_{n=1}^{N} sin(f_1 n) \times sin(f_2 n) = \begin{cases} 0 & \text{if } f_1 \neq f_2, \\ \neq 0 & \text{if } f_1 = f_2 \end{cases} \qquad (5.6)$$

where N is the frequency of repetition. The above equation can be reworded as: the sum of product of two sinusoids is equal to zero if the frequencies are different and is equal to non-zero if the frequencies are the same. An alternative way of looking at the above property is that the product of two sinusoids of same frequencies has a component at DC, while the product of two sinusoids of different frequencies does not have any component at DC.

5.2.3 Proposed Algorithm

Combining the properties of downsampling and orthogonality of sinusoid waves, the coefficient of the third harmonic distortion (α_3) is estimated. This is done by taking the running average of the product of the two digital bit streams D_{out} and DS_3. As shown in Fig. 5.4, when there is a third harmonic distortion term present in the ADC, the running sum product of D_{out} and DS_3 has a component at DC, whose magnitude is proportional to α_3.

Using this information, the third harmonic distortion term can be extracted using an LMS based engine. The error term of the LMS engine is given as

$$err = \sum \left(D_{cal}[n] \times DS_3[n] \right) \qquad (5.7)$$

where D_{cal} is the updated calibrated signal and err is the error for the LMS engine. The error term is zero if and only if the calibrated output D_{cal} and the downsampled output DS_3 do not have any common sinusoid in their digital streams. The simplified update equations for the LMS engine are given in eq. 5.8
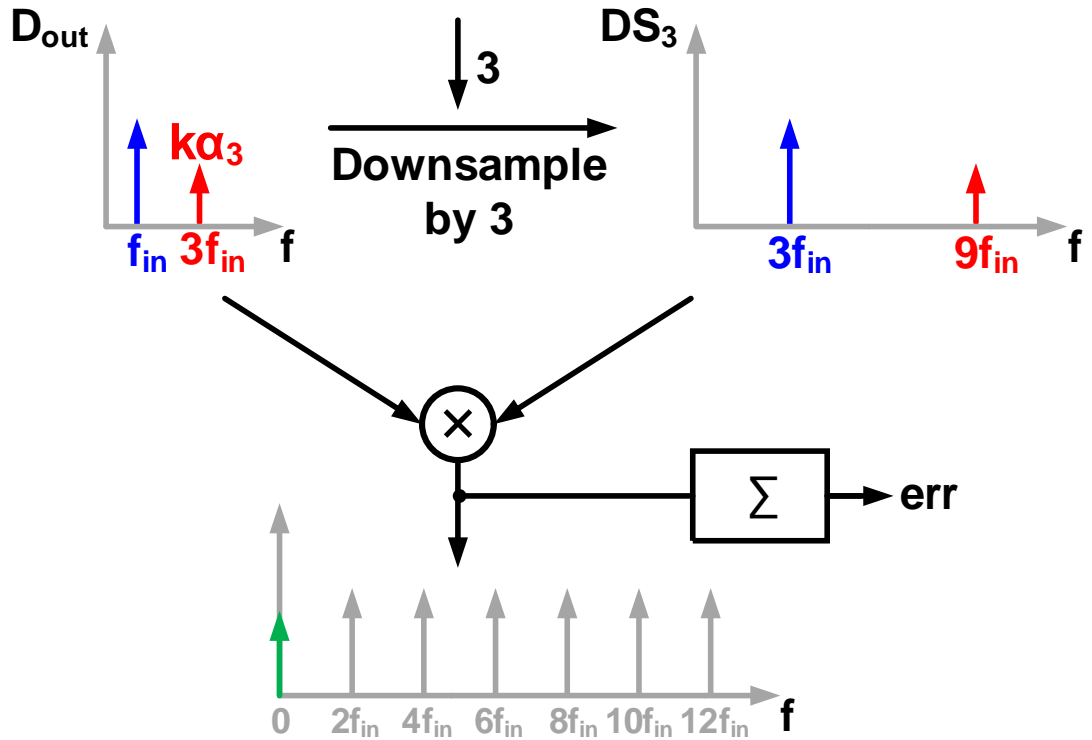
Figure 5.4: LMS engine.

$$D_{cal}[n+1] = D_{out}[n] - \alpha_3[n] \times D_{out}^3[n], \tag{5.8a}$$

$$\alpha_3[n+1] = \alpha_3[n] - \mu \times err \times DS_3[n] \tag{5.8b}$$

where $\alpha_3[n+1]$ represents the updated value of α_3 and $D_{cal}[n+1]$ is the updated value of D_{cal}. The value of α_3 settles only when $err = 0$, and this happens only when the non-linearity in the system is removed. The above proposed foreground calibration engine is visually illustrated in Fig. 5.5.

Therefore, the final calibrated sequence is given as

$$D_{cal} = D_{out} - \alpha_{3,stable} \times D_{out}^3, \tag{5.9}$$
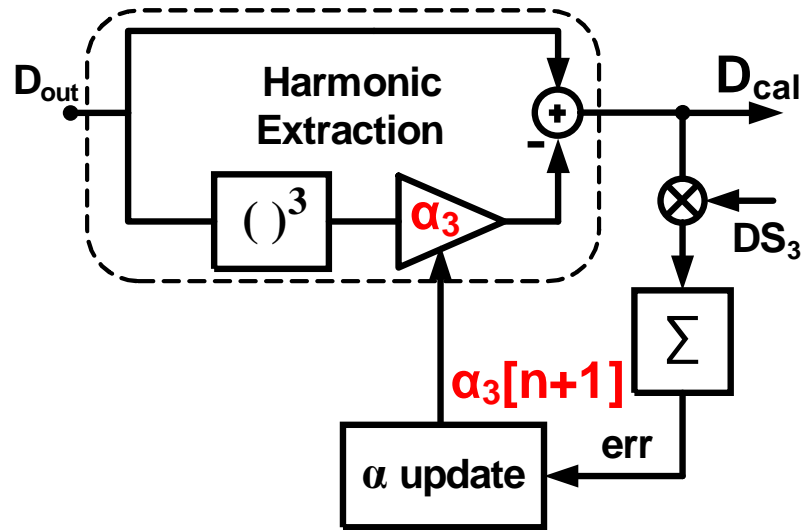
Figure 5.5: Update engine used to perform the LMS operation to estimate the nonlinearity coefficient.

5.3 Background Calibration

The algorithm discussed so far needs a clean sinusoid input and can be operated in a foreground fashion. In many cases, this could be a problem as generating a clean input sinusoid needs expensive laboratory equipment. Consider the case where the input itself has a third harmonic term present in it, as shown in Fig. 5.6.
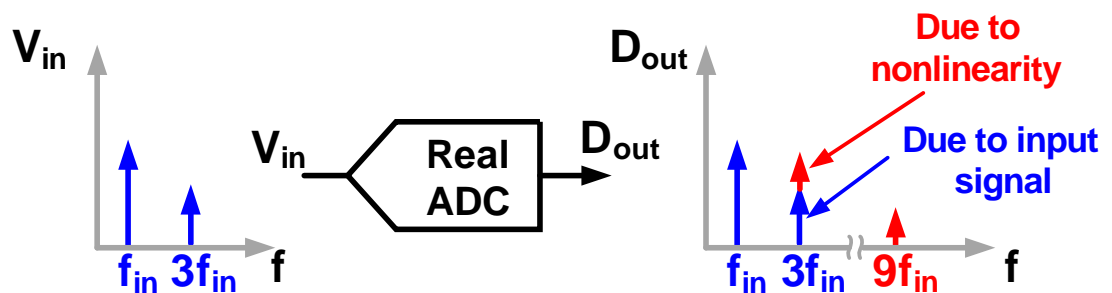
Figure 5.6: Limitations of foreground calibration technique.

The input has frequency terms f_{in} and $3f_{in}$. When such an input is passed through an ADC, which suffers from third order nonlinearity, the output spectrum has terms at $f_{in}, 3f_{in}$ and $9f_{in}$. However, the tone at $3f_{in}$ has components due to the input and nonlinearity. Unfortunately, the foreground calibration technique cannot distinguish between signal and nonlinearity, and when used to calibrate for third order nonlinearity, it removes both the signal and nonlinear distortion. This is clearly a problem and is not desirable, as illustrated in Fig. 5.7.
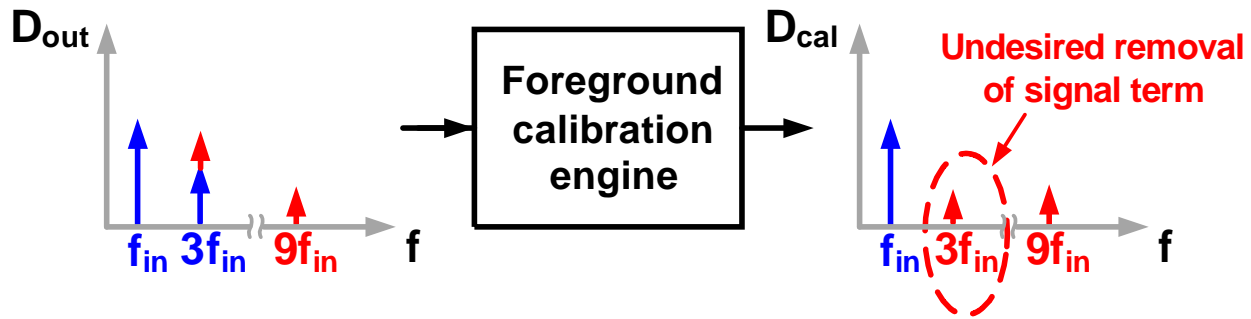
Figure 5.7: Illustration of limitation of foreground calibration technique.

Fortunately, an alternative solution exists, which can be used to make the algorithm operate in the background mode. The above algorithm can be made to operate in a background mode by removing the signal component from the output digital stream and dealing only with the harmonics. As shown in Fig. 5.8, this is done by splitting the original ADC into two parts and applying input V_{in} to one ADC and an approximately scaled version of V_{in} (e.g. $V_{in}/2$) to the other ADC. By doing so, the linear component of the input is scaled by a linear factor, whereas the harmonic distortion part is scaled by a different factor. Therefore, the digital stream D_{out} - $2D_{By2}$ does not have any input signal component present in it, but only has the harmonic distortion terms present in it. Therefore, by taking the average of the product of the above obtained signal free stream and

the downsampled stream (DS_3), the third harmonic distortion coefficient can be estimated. The finite accuracy of the scaling by 2, in this example, can also be merged into the LMS engine.
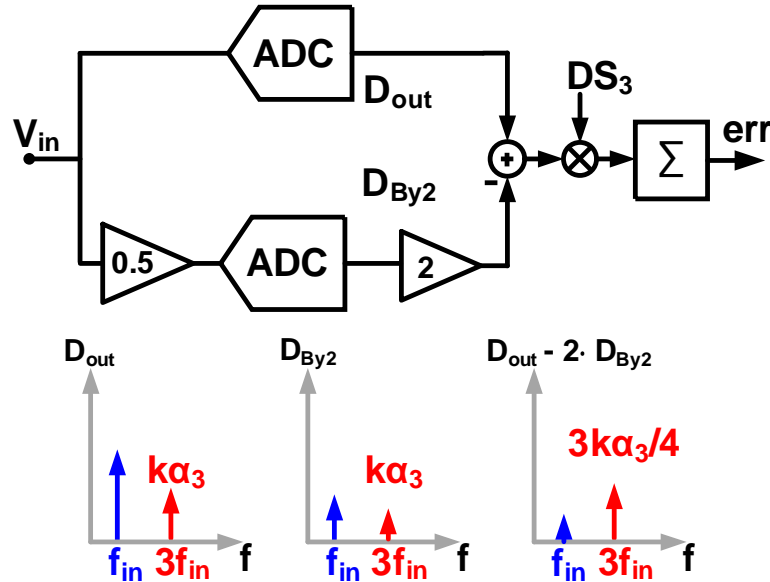
Figure 5.8: Removal of signal term from the input signal by using two ADCs with scaled inputs.

The updated error equation for background calibration is given as

$$err = \sum \left(D_{nosig}[n] \times DS_3[n] \right) \tag{5.10}$$

where D_{nosig} is the digital output which does not have any signal component in it. The update equations for the LMS engine are given as

$$D_{cal}[n+1] = D_{out}[n] - \alpha_3[n] \times D_{out}^3[n], \tag{5.11a}$$

$$D_{calby2}[n+1] = D_{By2}[n] - \alpha_3[n] \times D_{By2}^3[n], \tag{5.11b}$$

$$D_{nosig}[n+1] = D_{cal}[n+1] - 2 \times D_{calby2}[n+1], \tag{5.11c}$$

$$\alpha_3[n+1] = \alpha_3[n] - \mu \times err \times DS_3[n] \tag{5.11d}$$

The above equations are shown visually in Fig. 5.9
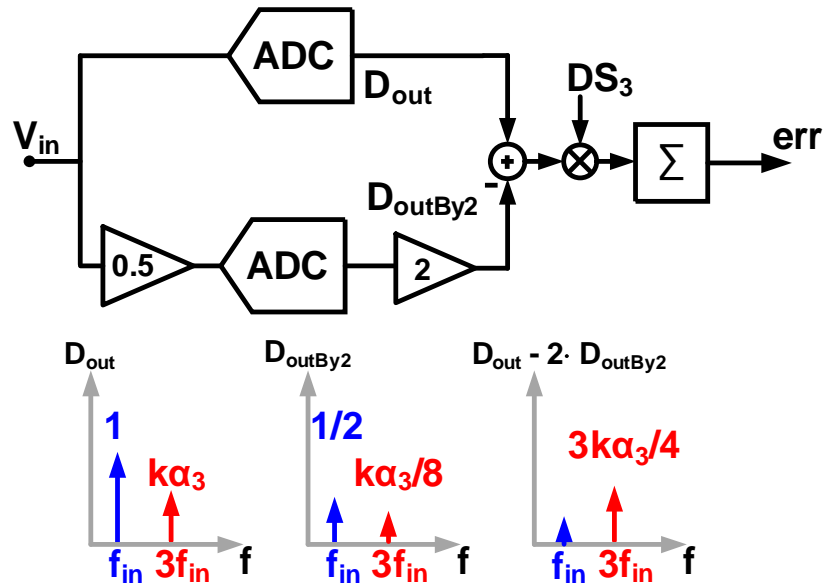
Figure 5.9: System update equations in background calibration mode.

Therefore, the final calibrated sequence obtained from background calibration is given as

$$D_{cal} = D_{out} - \alpha_{3,stable} \times D_{out}^3, \tag{5.12}$$

5.4 Calibration for Multiple Harmonics

The above algorithm can be extended to calibrate for multiple harmonics. This is done by using multiple downsampled streams, which are created by downsampling the output stream by the nonlinear factor which needs to be estimated, and then performing the above calibration operation in unison.

For example, assume that the ADC suffers from both k_1 and k_2 order nonlinearity. Two new digital streams (1) digital stream downsampled by k_1 (DS_{k1})

and (2) digital stream downsampled by k_2 (DS_{k2}) are created. The sum of the product of the sequences D_{nosig} (the sequence from which the signal component is removed) and DS_{k1} gives a term proportional to err_{k1}, whereas the product of the terms D_{nosig} and DS_{k2} gives a term proportional to err_{k2}. Note that the estimation of both the coefficients happens simultaneously, i.e. the modified update equation is

$$D_{cal}[n+1] = D_{out}[n] - \alpha_{k1} \times D_{out}^{k1}[n] - \alpha_{k2} \times D_{out}^{k2}[n] \tag{5.13}$$

The final calibrated sequence is given by

$$D_{cal} = D_{out} - \alpha_{k1} \times D_{out}^{k1} - \alpha_{k2} \times D_{out}^{k2} \tag{5.14}$$

5.5 Final System Architecture

Figure 5.10 shows the final architecture of the complete ADC. The core ADC consists of two ADCs with input to the first being V_{in} and the input to the second being $V_{in}/2$. The digital outputs from the ADCs are then sent to the calibration engine, which are used to estimate the harmonic distortion coefficients. Once the coefficients are estimated, the coefficients are stored in memory. The ADC now returns to normal operation, and the output of the ADC is corrected for harmonic distortion using eq. 5.14. The digital engine is operated using 15-bit precision words and is implemented off-chip in software.
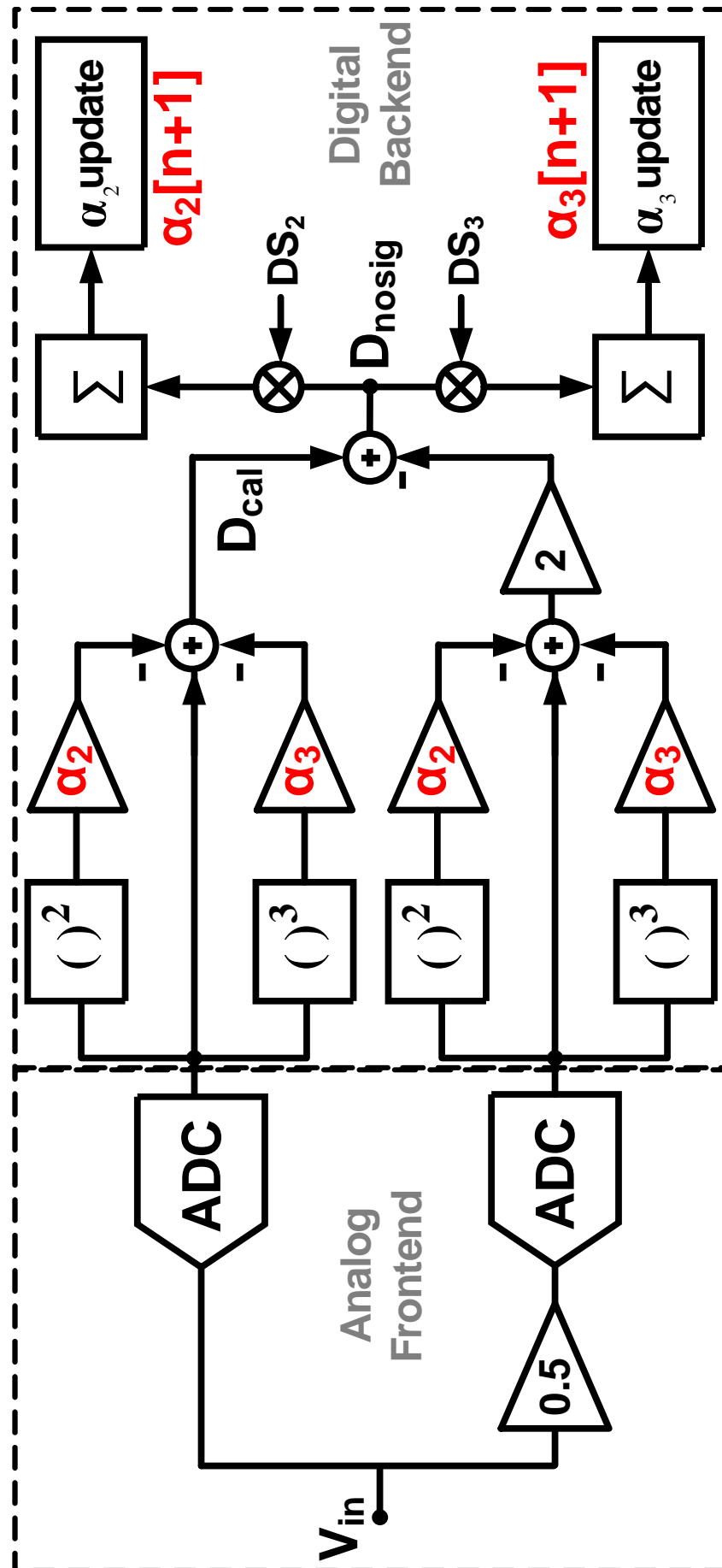
Figure 5.10: Background calibration architecture implemented.

5.5.1   Example Nyquist Converter

In this subsection, the calibration algorithm is explained for a nyquist data converter. Assume that the ADC suffers from second and third order nonlinearity. Figure 5.11 shows the frequency spectrum of such a ADC without calibration.

SNDR= 90.4642dB

SNDR= 45.0473dB
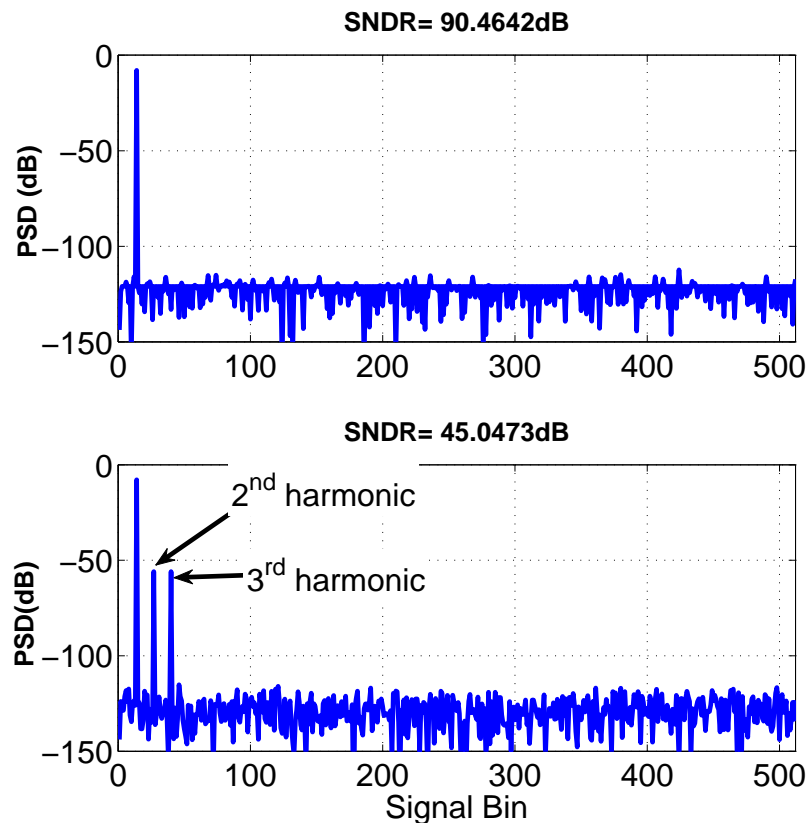
Figure 5.11: Uncalibrated spectrum of ADC suffering from 2nd and 3rd order non-linearity.

As expected, for a single tone sinusoid input, the input FFT has a single impulse, while the output has a tone at f_{in} plus additional harmonic distortion terms at $2f_{in}$ and $3f_{in}$, thereby limiting the SNDR to 45dB. Therefore, the output of the ADC can be modeled as

$$D_{out} = D(V_{in}) + \alpha_2 \times D(V_{in}^2) + \alpha_3 \times D(V_{in}^3) \qquad (5.15)$$

where $D(V_{in})$ is the ideal representation of the input voltage, and α_2, α_3 are the coefficients of second and third order nonlinearity respectively. The above ADC is calibrated for second and third harmonics using the blind calibration algorithm. The calibrated spectrum is shown in Fig. 5.12.
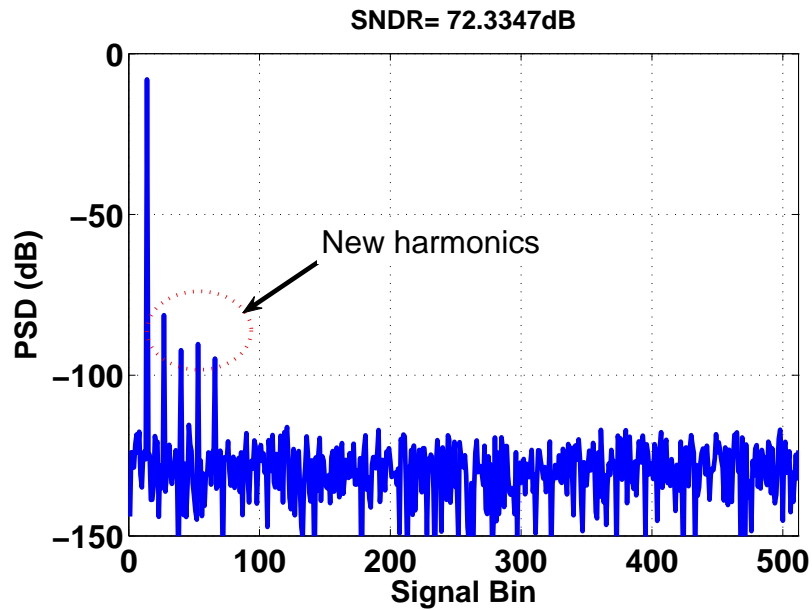
Figure 5.12: Spectrum of ADC after calibrating for 2nd and 3rd order nonlinearity.

Clearly, from Fig. 5.12, one can observe that calibrating for 2nd and 3rd order nonlinearity causes other distortion terms. This can be explained by looking at the final calibrated spectrum

$$D_{cal} = D_{out} - \alpha_2 \times D_{out}^2 - \alpha_3 \times D_{out}^3 \qquad (5.16)$$

Since D_{out} has second and third harmonics, D_{out}^2 and D_{out}^3 would create additional higher order harmonics (4th and 5th). Therefore, to optimize the performance of the ADC, the ADC is calibrated for second, third, fourth and fifth harmonics.

The final calibrated spectrum is shown in Fig. 5.13 and the coefficient settling is shown in Fig. 5.14.

SNDR= 89.512dB
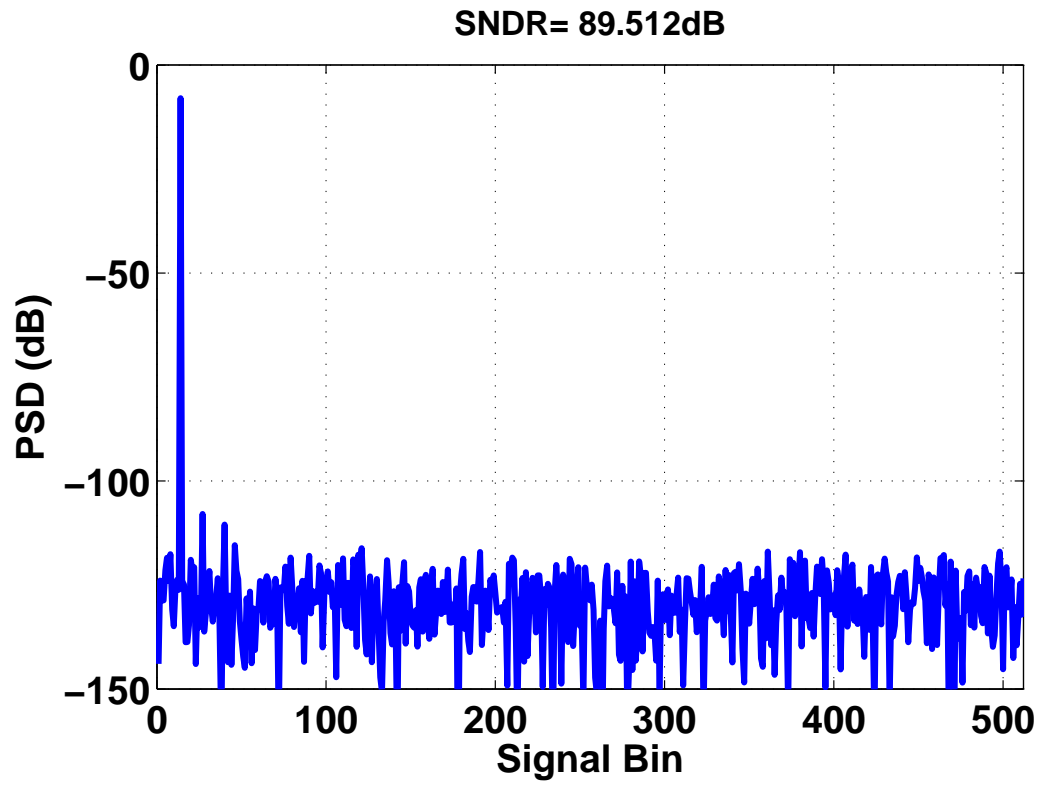
Figure 5.13: Spectrum of ADC after calibrating for $2^{nd}, 3^{rd}, 4^{th}$ and 5th order non-linearity.
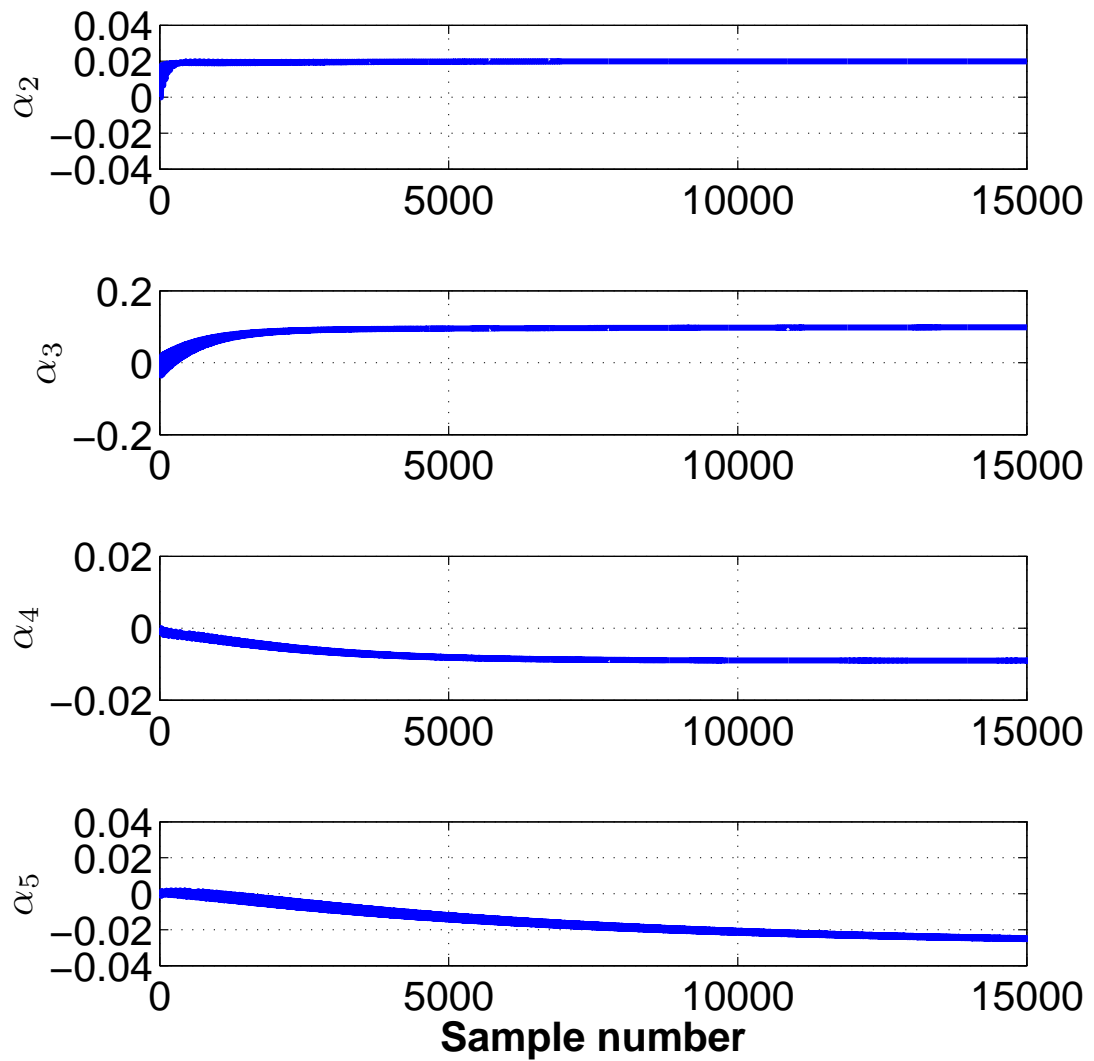
Figure 5.14: Settling of $2^{nd}, 3^{rd}, 4^{th}$ and 5th order coefficients.

The next case considers a multi-tone input in which the second tone is a third harmonic of the first tone, therefore making it an ideal candidate for the blind calibration algorithm. The frequency spectrum of the input and the corresponding un-calibrated output spectrum of the ADC are shown in Fig. 5.15.
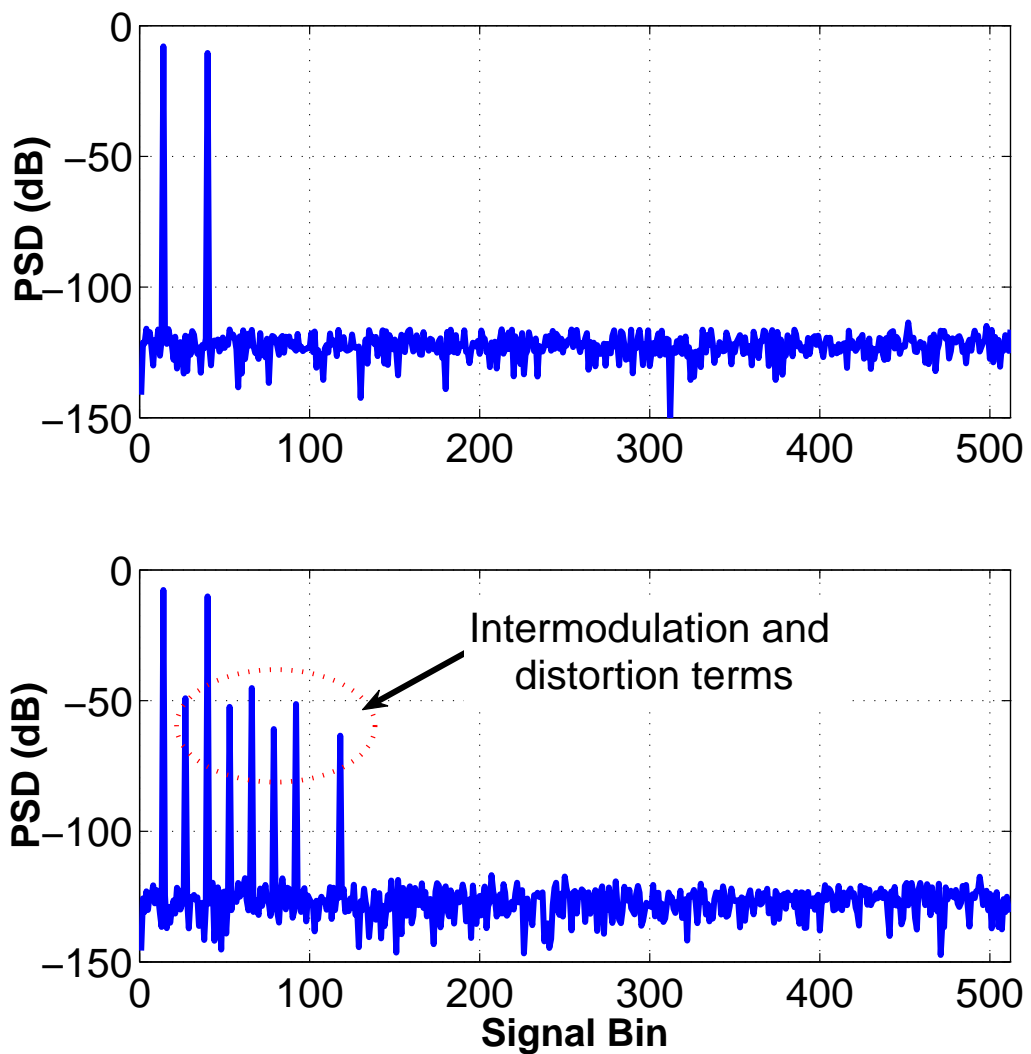
Figure 5.15: Input and un-calibrated output spectrum for multi-tone input, with second tone being a harmonic bin of the first tone.

As expected, the input has two tones while the output has tones at the input,

and well as tones which are a result of intermodulation and cross-modulation. Upon calibrating for $2^{nd}, 3^{rd}, 4^{th}$ and 5th order nonlinearity, the resulting spectrum is shown in Fig. 5.16.

Note that the intermodulation distortion terms can be further reduced by using higher precision for the calibration engine and by calibrating for higher order nonlinear terms.
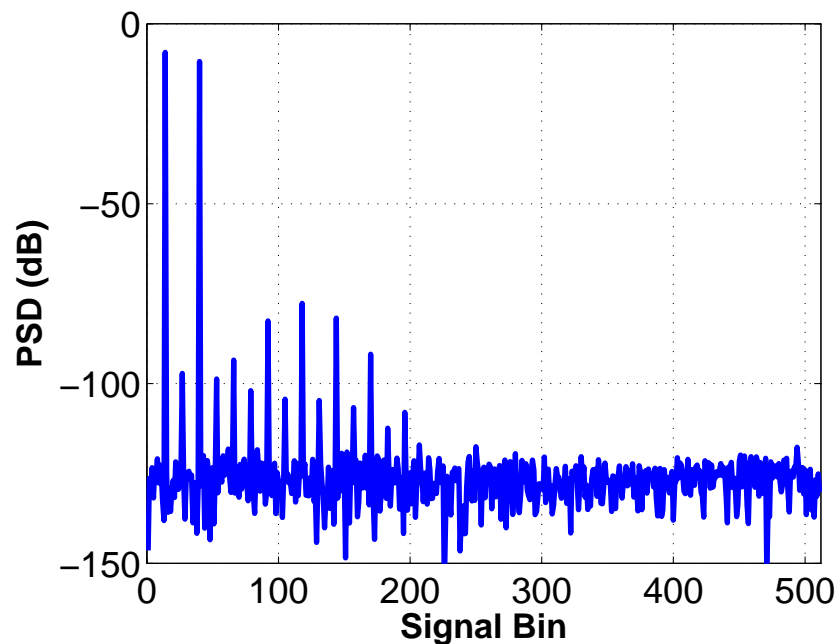
Figure 5.16: Calibrated spectrum for multi-tone input.

5.6   VCO Based $\Delta\Sigma$ ADC

By definition, phase is equal to the integral of frequency. In other words, one could estimate the frequency of oscillation of an oscillator by differentiating its phase. A voltage controlled ring oscillator (VCO) is an oscillator whose oscillation frequency is controlled by the input voltage. Therefore, the phase of the

VCO contains information about the integrated value of the oscillation frequency. Consequently, by differentiating the phase, one could obtain the average value of the oscillation frequency and hence the input voltage, as the oscillation frequency is proportional to the input voltage for a VCO [41, 50, 52, 16]. Figure 5.17 shows a generic VCO whose output frequency of oscillation is a function of its input. As the input voltage of the oscillator increases, the frequency of oscillation also increases.
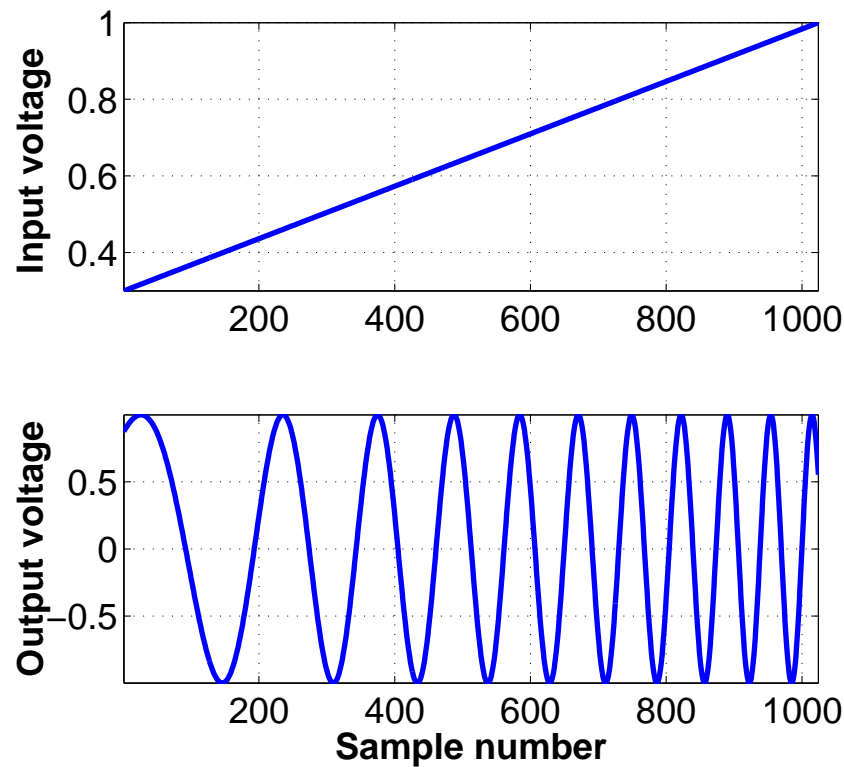
Figure 5.17: Oscillator whose output frequency is a function of input voltage.

The instantaneous oscillation frequency of the VCO is given as

$$f_{VCO}(t) = f_c + K_{VCO}V_{in}(t) \tag{5.17}$$

where f_c is the VCO center frequency and K_{VCO} is the VCO gain and V_{in} is the input voltage. The phase quantizer quantizes the VCO phase at clock frequency f_s, i.e. at time intervals of nT_s, where n =0,1,2,3 ... The phase output of the VCO is given as

$$\phi[n] = \int_0^{nT_s} f_{VCO}(t)dt \tag{5.18}$$

where ϕ is the phase of the VCO. Note that the output phase of the VCO never saturates, and ideally it could be kept track of by taking wrapping into consideration. The phase detector quantizes the value of the phase, thereby adding a quantization error along the operation. Therefore, the output phase of the oscillator is given as

$$\Phi_q[n] = \int_0^{nT_s} f_{VCO}(t)dt + Q_e[n] \tag{5.19}$$

where Q_e is the quantization error associated with the discrete phase detector, and Φ_q is the output phase. Next, the instantaneous value of the frequency is given by differentiating the phase value. Since the output phase is discrete, differentiation in digital domain is performed using the high pass filter $1 - z^{-1}$. Therefore, the output frequency of the VCO is given as

$$F_{out}[n] = \Phi[n] - \Phi[n-1] \tag{5.20a}$$

$$= \int_{(n-1)T_s}^{nT_s} f_{VCO}(t)dt + (1 - z^{-1})Q_e \tag{5.20b}$$

where F_{out} is the quantized output frequency of the oscillator. One interesting property which can be observed from eq. 5.20 is that the quantization error is first-order noise shaped. This can be clearly observed by examining Fig. 5.18.

Since the instantaneous frequency is directly proportional to the input voltage, the quantized frequency value is directly proportional to the input i.e.
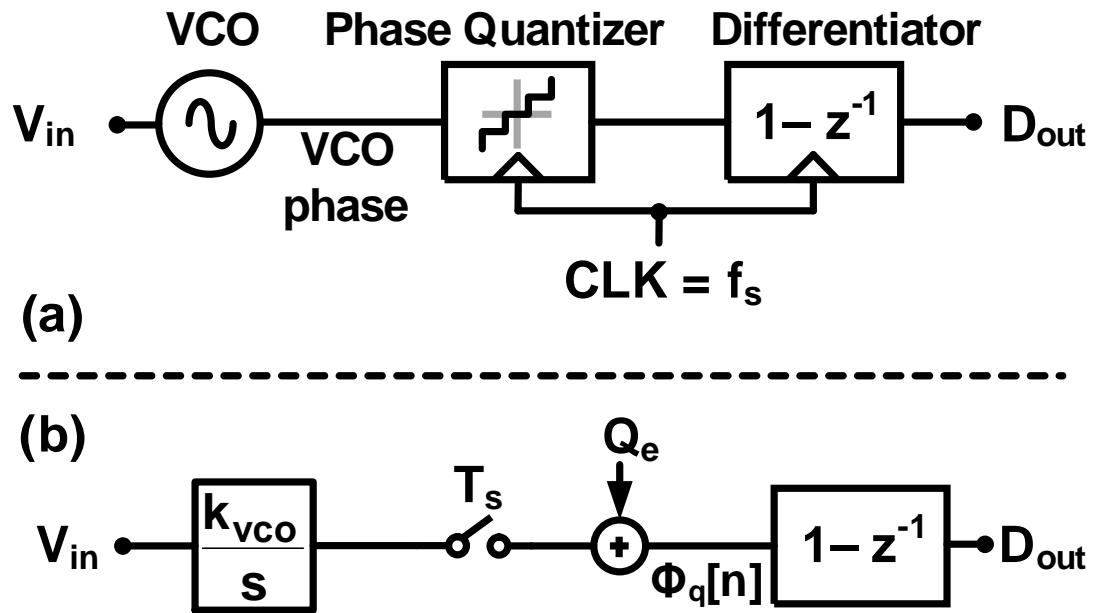
Figure 5.18: Model diagram of VCO.

$$D_{out}[n] = \int_{(n-1)T_s}^{nT_s} V_{in}(t)dt + (1 - z^{-1})Q_e \qquad (5.21)$$

As a result, the digital output of the $\Delta\Sigma$ ADC is input + shaped quantization error. The operation of the VCO in time domain can be understood by analyzing Fig. 5.19. The input voltage (V_{in}) was assumed to be constant; therefore, the VCO oscillates at a fixed frequency. The phase of the VCO is quantized using the count signal, and D_{out} equals the number of rising VCO edges in a given phase, thereby differentiating the output phase. An intuitive way to understand the shaped quantization noise is that the incomplete part of phase oscillation of one clock cycle is completed in the next clock cycle, thereby the next phase starts off from the $-Q(e)z^{-1}$. This is illustrated in the red part of the figure.

Although the above analysis shows a simple way of implementing an ADC, it has to be noted that the accuracy of the ADC is determined by the linearity
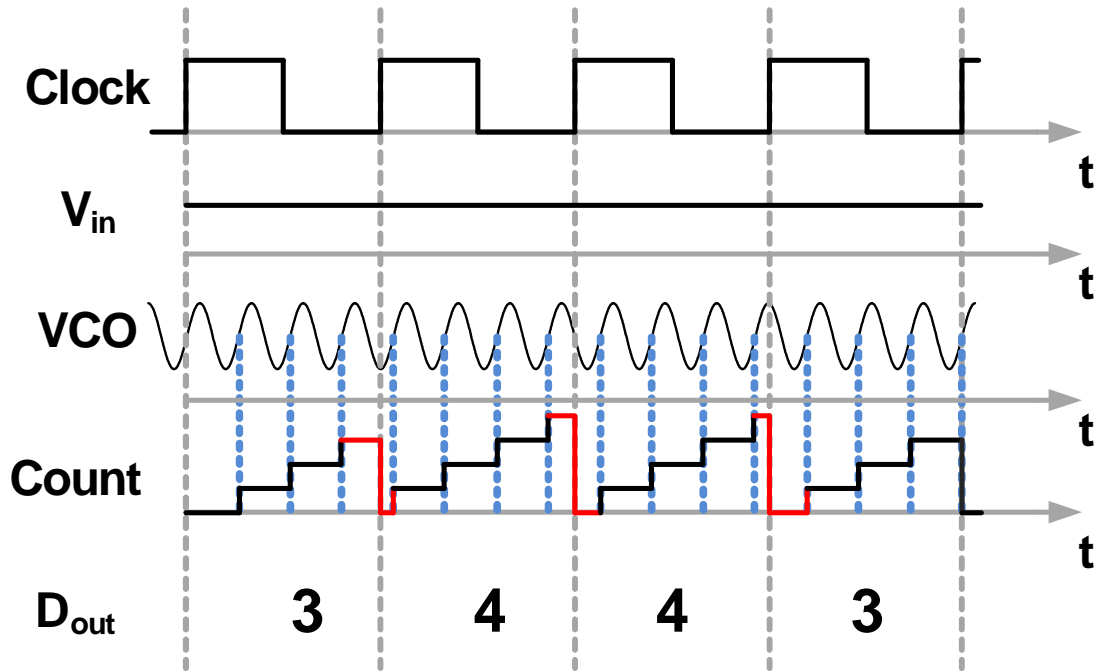
Figure 5.19: Illustration of first order noise shaping in VCO.

of the voltage to frequency conversion. Unfortunately, the voltage to frequency conversion i.e. K_{vco} of the VCO is highly nonlinear. Consequently, any ADC built using a VCO as quantizer needs to suppress the nonlinearity of the VCO [50].

Since the VCO based $\Delta\Sigma$ ADC is highly nonlinear, it has been chosen to show the effectiveness of our proposed nonlinear calibration algorithm.

5.7   Circuit Implementation

5.7.1   Supply Controlled VCO

The VCO was made using a 15-cell ring oscillator built using standard cell inverter blocks. The supply of the inverter cells is directly controlled by the input

of the system, thereby making it a supply controlled VCO, as illustrated in Fig. 5.20. Also, most of the cells used in the design are standard cell blocks, thereby making the design highly scalable with modern day CMOS processes.
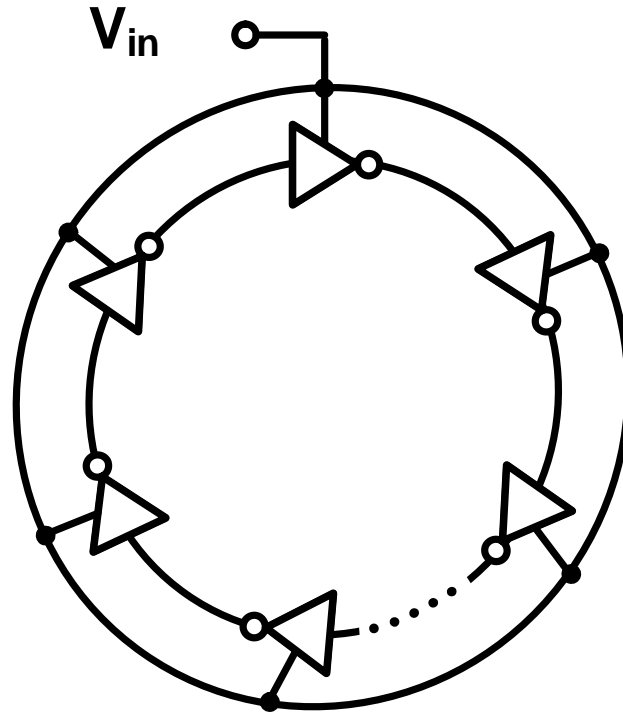
Figure 5.20: Voltage controlled ring oscillator.

One advantage of the ring oscillator based $\Delta\Sigma$ modulator is that it avoids the use of dedicated feedback DAC. This makes the architecture less sensitive to clock jitter when compared to conventional $\Delta\Sigma$ modulators. However, jitter-induced due to ring sampling is high pass noise shaped by $1\text{-}z^{-1}$, as the sampling occurs after the integration is performed [41].

When designing the VCO, special attention should be placed on the phase noise of the VCO. The phase noise of the ring oscillator is 1/f dominated and hence is low pass in nature. The phase noise is high pass shaped by the differentiator, i.e. the phase noise is subjected to a high pass transfer function of $(1\text{-}z^{-1})$; as a result,

the noise contribution to the ADC is predominantly white. Therefore, taking this effect into consideration, the ring oscillators were designed such that the in-band noise contribution to the VCO is below 78dB, for a signal BW of 5MHz.

5.7.2   Phase Quantizer

The phase quantizer was built using a symmetrical sense-amplifier flip-flop(SAFF), which is shown in Fig. 5.21 [59].
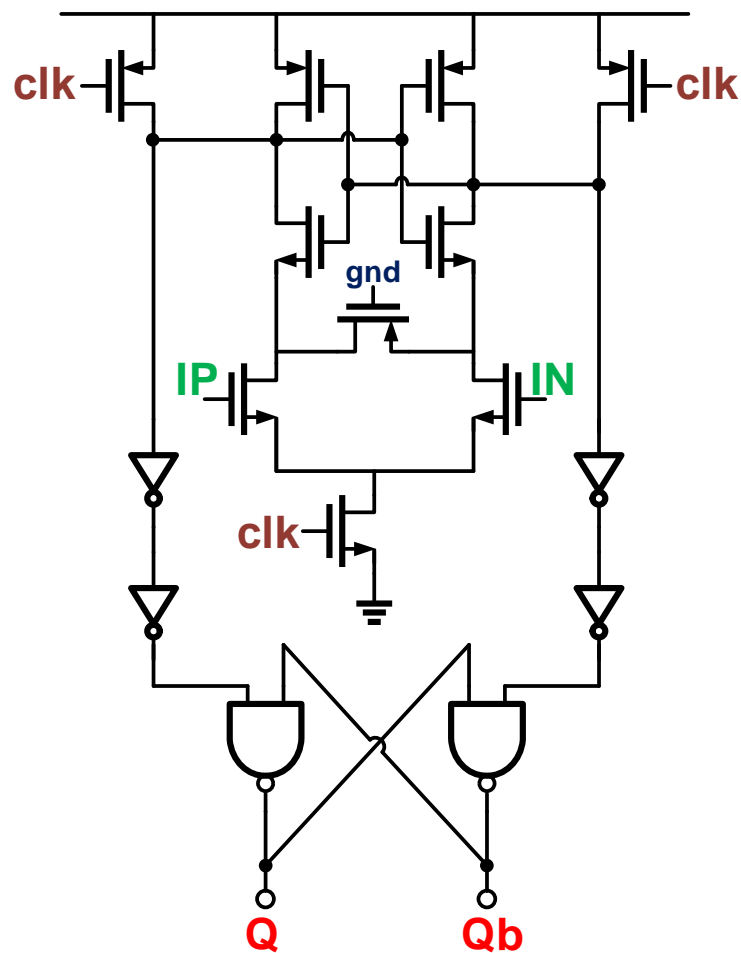
Figure 5.21: Sense amplifier flip-flop.

The SAFF was built so that it is symmetrical with respect to both the inputs. The SAFF latches onto $IP - IN$ at the rising edge of clk. The positive feedback latch amplifies $IP - IN$ into a digital code, which is sensed using the Set-Rest (SR) latch. The output Q is passed onto the phase differentiator.

5.7.3 Phase Differentiation

The range of oscillation frequency of the VCO to operate as an ADC is limited by the architecture of the phase differentiator used. This is because of the unique property of the phase of the VCO. Though the VCO acts as a open loop integrator, the phase of the VCO never saturates. This is because the phase wraps around and is recounted. Therefore, as long as phase wrapping is taken into account, the limits on the oscillation frequency of the VCO are non-existent. In this design, a simple ex-or phase detector, as shown in Fig. 5.22, was used to act as a phase differentiator.

$\Phi_q[n-1]$	$\Phi_q[n]$	out
0	0	0
0	1	1
1	0	1
1	1	0
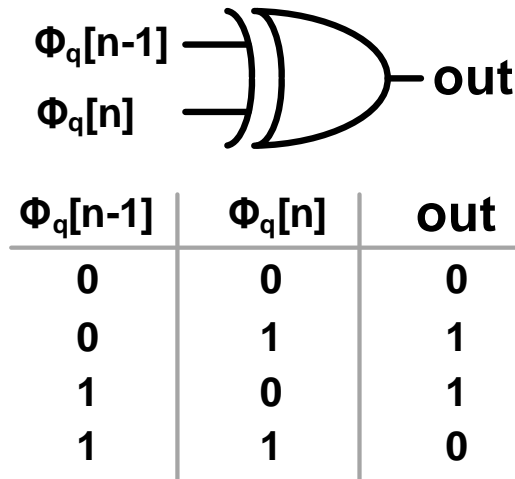
Figure 5.22: Ex-or phase differentiator.

The ex-or phase detector is nothing but an ex-or gate. It compares the

current quantized phase with the previous quantized phase, and any difference in the quantized phase is counted as 1. It can be proven that the ex-or phase detector places the limit on the oscillation frequency to half the sampling frequency [60], i.e. for proper functioning of the ADC,

$$f_{vco,max} - f_{vco,min} = f_{clk}/2 \qquad (5.22)$$

where $f_{vco,max}$ is the maximum oscillation frequency of the VCO, $f_{vco,min}$ is the minimum and f_{clk} is the clock sampling frequency. In this design, the VCO was designed to oscillate between $f_{clk}/2$ and f_{clk}.

5.8   Measured Results

The performance of VCO based first-order $\Delta\Sigma$ ADC is harmonic distortion limited, thereby making it an ideal candidate for the proposed algorithm. The prototype ADC consists of two versions of the VCO $\Delta\Sigma$ ADC. One ADC processes regular input, while the other processes a scaled version of the input. An off-chip transformer was used for creating a scaled version of the input.

Built in $0.13\mu m$ CMOS, the prototype ADC occupies an area of $0.055mm^2$. The ADC operates at a sampling frequency of 450MHz with an OSR of 64, resulting in a signal bandwidth of 3.51MHz. A rounded square wave signal (i.e. an arbitrary signal) is given as the input to both the ADCs, and the second and third harmonic distortion coefficients are estimated. The non-linearity correction is then performed using the above obtained coefficients.

Figure 5.23 shows the output spectrum for a 1MHz sinusoid input before calibration. Before calibration, the SNDR of the ADC is harmonic distortion
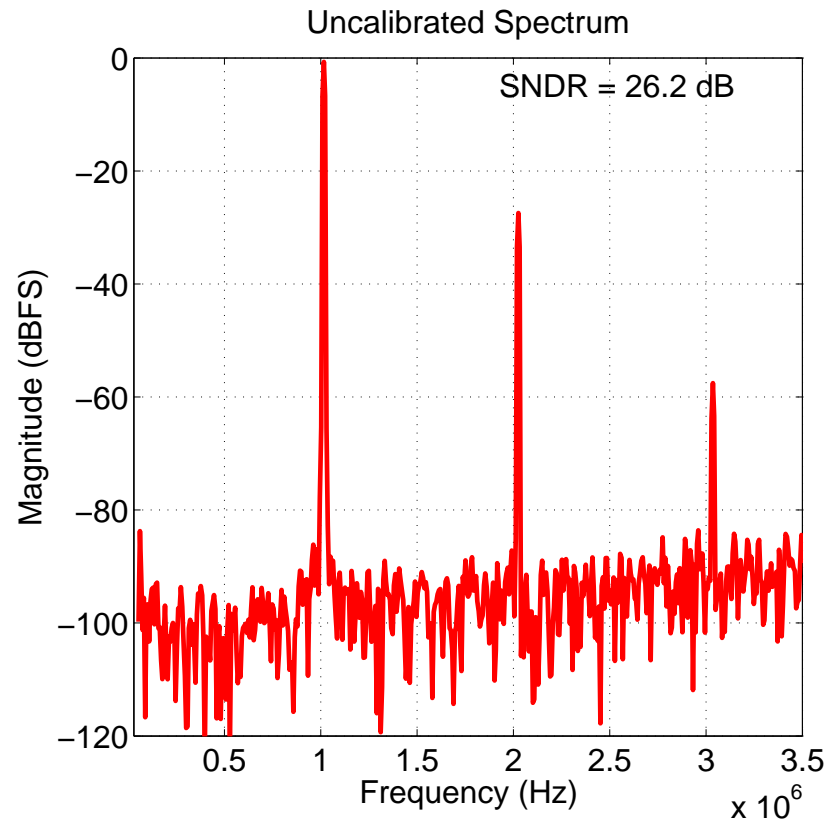
Figure 5.23: Measured spectrum before calibration.

limited and is equal to 26dB. The spectrum after calibration is shown in Fig. 5.24.

After calibration, the SNDR of ADC improves to 65dB. The power consumption of this ADC was 1.65mW resulting in an FOM of 161 fJ/C-S. The limited FOM is due to a design oversight and can be improved easily. Figure 5.25 shows the SNDR vs. input amplitude for the ADC. The chip micrograph of the ADC is shown in Fig. 5.26.
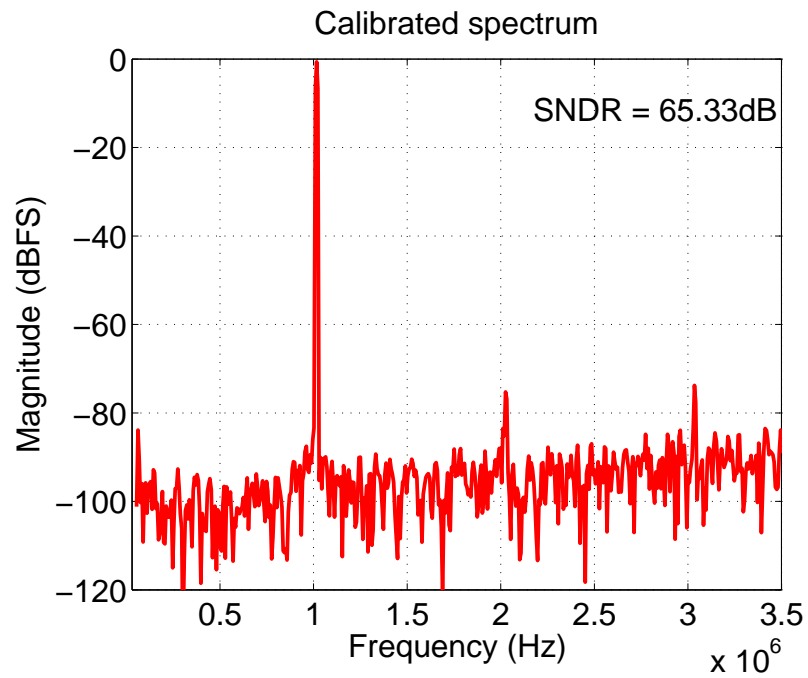
Figure 5.24: Measured spectrum after calibration.

5.9 Summary

In this chapter, a blind calibration algorithm is proposed which can be used to reduce nonlinearity in ADCs. The proposed algorithm can be applied to any ADC architecture in general, and can be used to remove both even and odd harmonics. The successful operation of the algorithm was demonstrated for a VCO based first order $\Delta\Sigma$ ADC. Table 5.1 summarizes the performance of the ADC.

Table 5.1: Summary of performance

Parameter	Value
Technology	$0.13\mu m$
Supply Voltage	1.2V
Sampling Rate	450MHz
Signal Bandwidth	3.5 MHz
SNDR Before Calib.	26dB
SNDR After Calib.	65dB
Power	1.65mW
Area	$0.055mm^2$
FOM	162fJ/step
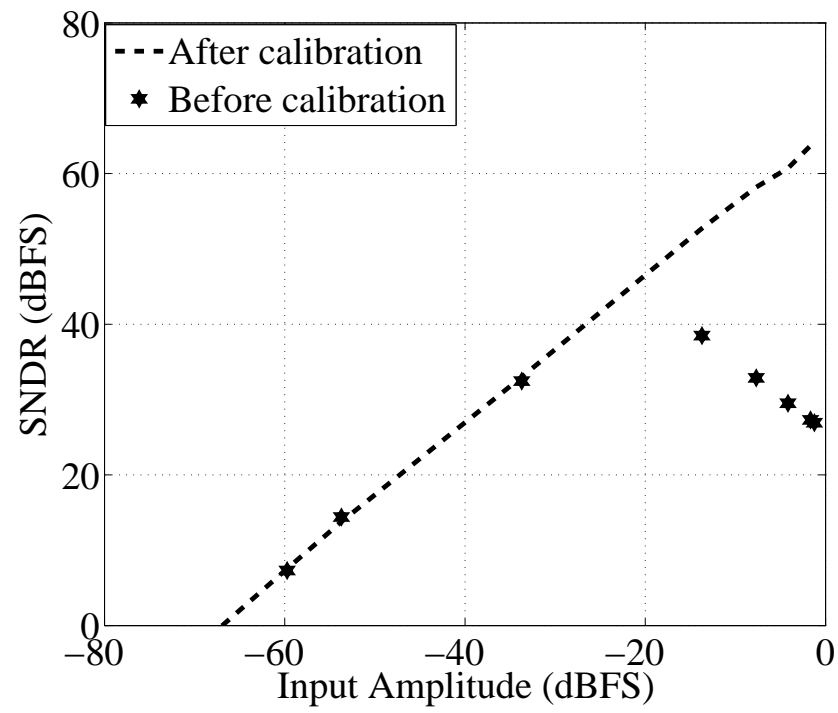
Figure 5.25: SNDR vs. input amplitude.
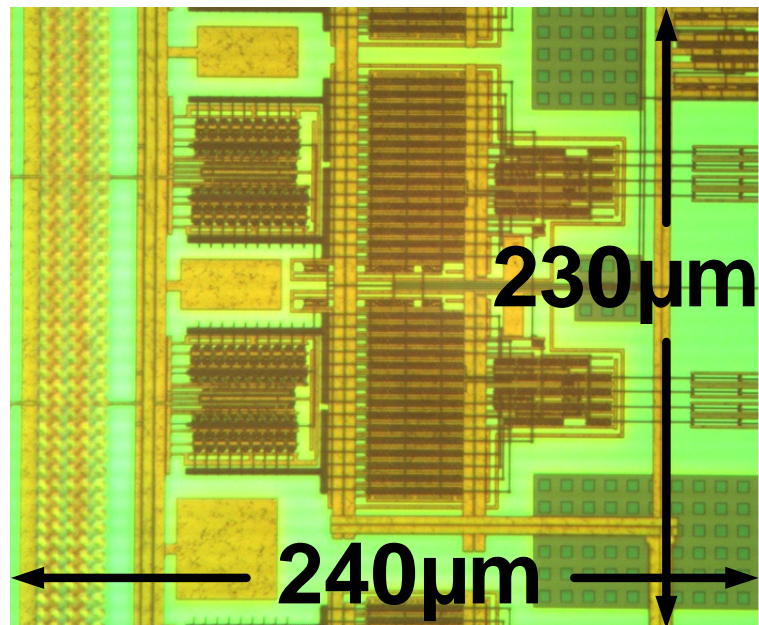
Figure 5.26: Chip micrograph.

CHAPTER 6. CONCLUSION

Deep sub-micron CMOS technology provides the user with benefits of reduced gate delay and faster processes, but at the same time it throws in many challenges due to reduced voltage headroom and reduced intrinsic gain. Therefore, it is imperative that one looks into alternative design methodologies which take the advantages of the modern processes. Data converters which make use of time domain signal processing or build data converters which are more digital in nature tend to utilize these benefits. This thesis presents two new data converter architectures which try to take advantages of these modern day CMOS processes.

In Chapter 2, the fundamentals of the operation of time-to-digital converters (TDCs) were discussed. This chapter also looked at some of the existing TDC architectures in order to give a better understanding of the limitations of the TDC.

In Chapter 3, a new delta-sigma TDC architecture was proposed. The architecture combines the properties of a noise-shaping quantizer with a charge-pump to build a single loop higher order $\Delta\Sigma$ structure. Taking advantage of the decreased gate-delay, this architecture was shown to help reduce the power consumption, while also improving the performance achievable by TDCs. This chapter concluded by presenting the measured results of the proposed $\Delta\Sigma$ TDC which is built in 0.13 μm CMOS technology.

In Chapter 4, the effects of nonlinearity on ADCs was studied. This chapter also presented a brief study on the existing digital nonlinearity calibration algorithms for ADCs, while talking about the merits and demerits of these architecture.

In Chapter 5, a novel blind calibration algorithm was proposed, which can be used to reduce nonlinearity in ADCs. The proposed algorithm can be applied to any ADC architecture in general and can be used to remove both even and odd harmonics simultaneously. The successful operation of the algorithm was demonstrated for a VCO based first order $\Delta\Sigma$ ADC, which is known to suffer from nonlinear distortion. Also, VCO based ADC being highly digital in nature makes the entire design of the ADC highly portable with modern day CMOS processes. This chapter concludesd by presenting the improvements achieved by using the calibration algorithm on the VCO based $\Delta\Sigma$ ADC, which was built in 0.13 μm CMOS technology.

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