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Abstract approved:_____

Un-Ku Moon

As advanced wired and wireless communication systems attempt to achieve higher performance, the demand for high resolution and wide signal bandwidth in their associated ADCs is strongly increased. Recently, time-domain quantization has drawn attention from its scalability in deep submicron CMOS processes. Furthermore, there are several interesting aspects of time-domain quantizer by processing the signal in time rather than only in voltage domain especially for power efficiency. This research focuses on developing a new architecture for power efficient, high resolution ADCs using both voltage and time domain information.

As a first approach, a new ΔΣ ADC based on a noise-shaped two-step integrating quantizer which quantizes the signal in voltage and time domains is presented. Attaining an extra order of noise-shaping from the integrating quantizer, the proposed ΔΣ ADC manifests a second-order noise-shaping with a first-order loop filter. Furthermore, this quantizer provides an 8b

quantization in itself, drastically reducing the oversampling requirement. The proposed ADC also incorporates a new feedback DAC topology that alleviates the feedback DAC complexity of a two-step 8b quantizer. The measured results of the prototype ADC implemented in a 0.13µm CMOS demonstrate peak SNDR of 70.7dB (11.5b ENOB) at 8.1mW power, with an 8x OSR at 80MHz sampling frequency.

To further improve ADC performance, a Nyquist ADC based on a time-based pipelined TDC is also proposed as a second approach. In this work, a simple V-T conversion scheme with a cheap low gain amplifier in its first stage and a hybrid time-domain quantization stage based on simple charge pump and capacitive DAC in its backend stages, are also proposed to improve ADC linearity and power efficiency. Using voltage and time domain information, the proposed ADC architecture is beneficial for both resolution and power efficiency, with MSBs resolved in voltage domain and LSBs in time domain. The measured results of the prototype ADC implemented in a 0.13µm CMOS demonstrate peak SNDR of 69.3dB (11.2b ENOB) at 6.38mW power and 70MHz sampling frequency. The FOM is 38.2fJ/conversion-step.

Power Efficient Analog-to-Digital Converters using Both Voltage and Time Domain Information

By

Taehwan Oh

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Major Professor, representing Electrical and Computer Engineering

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

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Taehwan Oh, Author

ACKNOWLEDGEMENTS

In spring 2009 on the airplane flying to the U.S. from Korea, I was anxious and hopeful about starting my Ph.D work. Coming back to graduate school after spending almost seven years in industry was a big challenge for me. Since then, after four years of being a Ph.D student, the anxiety was turned into the satisfaction through the relationships I have made with the smart people here at Oregon State University and the nice people here in beautiful community, Corvallis, OR. I cannot imagine having reached this moment without help from the people around me.

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TABLE OF CONTENTS

Page

TABLE OF CONTENTS (Continued)

Page

TABLE OF CONTENTS (Continued)

Page

LIST OF FIGURES

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF TABLES

Table Page

POWER EFFICIENT ANALOG-TO-DIGITAL CONVERTERS USING BOTH VOLTAGE AND TIME DOMAIN INFORMATION

CHAPTER 1. INTRODUCTION

The recent popularity of mobile systems has made power consumption of the system one of the key performance parameters in various applications. Furthermore, the recent trend with system-on-chip's (SoC) are merging several functions into a single chip and in line with technology scaling. Since by definition SoC integrates a large number of analog blocks, the power efficiency of those analog blocks as well as digital circuits that service those analog blocks become very important in the SoC circuit design paradigm.

Among the various analog blocks embedded into modern systems, analog-to-digital converters (ADC) play an important role in interfacing the real world to the digital signal and are important to the overall system performance. With the advances in wired and wireless communication systems, the demand for high resolution and wide signal bandwidth with low power consumption in their associated ADCs is even further increased.

1.1 Nyquist ADC versus oversampling ADC

Fig. 1.1 shows the general comparison between a Nyquist and an oversampling ADC which can be classified by the ratio of sampling and signal frequency. For a high resolution ADC, the delta-sigma modulator has become a popular architecture for the last few decades. Due to the oversampling nature of a delta-sigma ADC, this architecture suffers from limited signal bandwidth without having a prohibitively high sampling rate. On the other hand, for a wide signal bandwidth up to the Nyquist-rate, the pipelined ADC architecture has many advantages with regard to its wide signal bandwidth and reasonable power efficiency with a medium resolution; however, it is not easy to achieve high resolution comparable to the delta-sigma architecture without requiring excessively large power consumption. Therefore, it is always a challenge in ADC design to obtain a high resolution and wide signal bandwidth, while maintaining low power consumption. Achieving these goals pose a significant and interesting challenge in circuit design, especially in the context of submicron CMOS scaling.

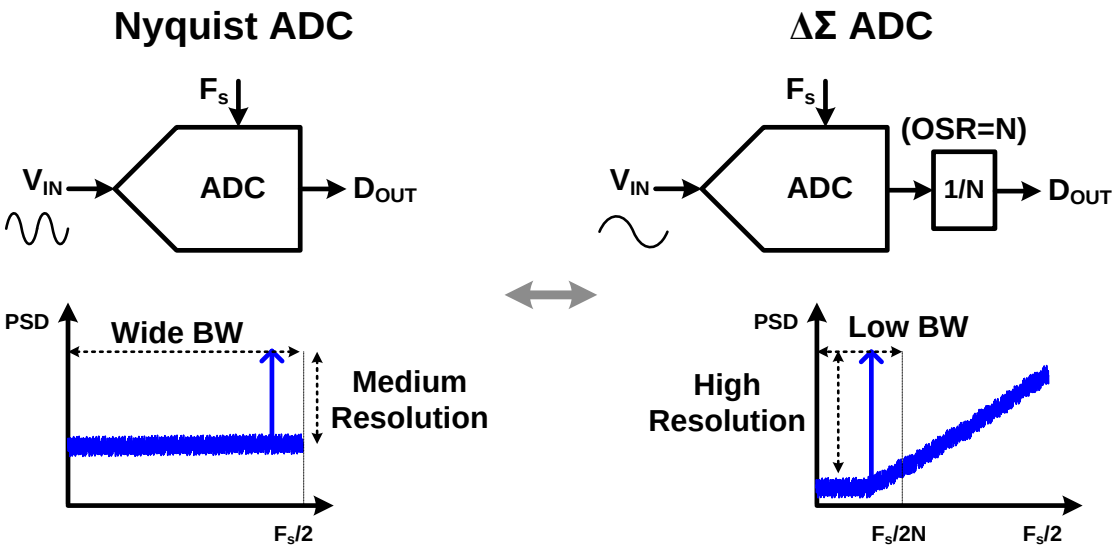

Figure 1.1: Comparison between Nyquist ADC and oversampling ADC

1.2 ADC architecture versus performance

Fig. 1.2 shows the ADC performances with different ADC architectures which have been published in recent papers [1]. In this figure, ADC performances are represented by the signal-to-noise and distortion ratio (SNDR) and signal bandwidth. There is a clear trade-off between the resolution and bandwidth. Each ADC is also grouped as a Nyquist or oversampling ADC based on the type of conversion. While many high speed ADCs (> 1 GHz) are based on flash architecture, most of ADCs with high resolution (> 80dB SNDR) are based on an oversampling architecture. However the overlapped region in Fig 1.2 which covers the resolution of 10b ~ 12b effective number of bit (ENOB) and the signal bandwidth of 1MHz ~ 100MHz can be achieved based on either Nyquist or oversampling ADC.

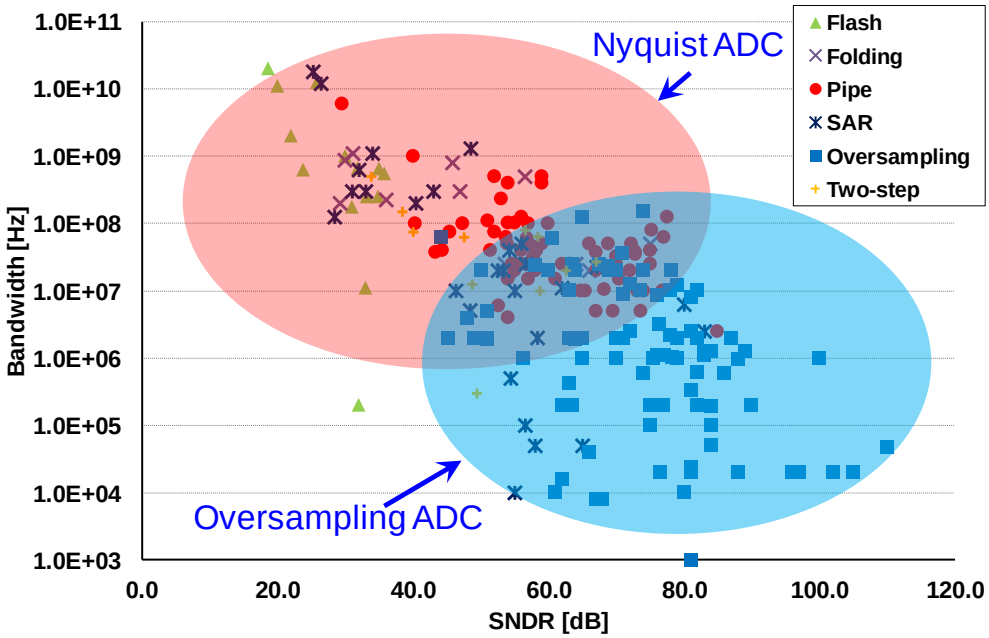

Figure 1.2: ADC performance versus architectures

In general, pipeline or SAR type architectures are employed as a popular architecture for Nyquist ADCs. However to achieve the target resolution of interest (12b ENOB), both architectures need an expensive residue amplifier which is usually not power efficient. Even in the SAR type ADC with a two-step architecture, an amplifier with large gain is required for the residue amplification [2]. Furthermore, a scaled CMOS process with a low supply voltage makes it difficult to design a large gain amplifier with low power consumption and/or reduces the effective signal swing resulting in increased power consumption from the larger devices.

In the case of an oversampling architecture, the design requirement for the amplifier can be relaxed compared to the Nyquist ADC due to the noise-shaping characteristic. However to achieve wide signal bandwidth, the required oversampling ratio (OSR) should be minimized which leads to a higher modulator order for the same signal-to-quantization noise ratio (SQNR) or the sampling rate should be increased for the same OSR [3]. In general, both strategies (higher order or sampling rate) result in increased power consumption of the ADC.

This research will develop new ADC architectures with a special focus on power efficiency. For the target specification of interest (12b ENOB with minimum power consumption) we will introduce two different ADCs based on both Nyquist and oversampling architectures. Chapter 2 will start by comparing the characteristics of data conversion in voltage and time domain signal processing and review the conventional ADCs which use a time domain signal for data conversion. Chapter 3 will propose a delta-sigma ADC based on the two-step integrating quantizer which uses both voltage and time domain quantizers with an inherent noise-shaping property. Chapter 4 will propose a Nyquist ADC utilizing a time based pipelined architecture which improves the power efficiency and allows a higher signal

bandwidth by using both voltage and time domain information. Chapter 5 will then conclude this research and compare the design result with other state-of-the art ADCs. This chapter will also describe some potential future work.

CHAPTER 2. USING VOLTAGE AND TIME DOMAIN SIGNALS FOR ANALOG-TO-DIGITAL CONVERSION

For analog-to-digital conversion, the conventional ADCs which use voltage information for quantization have been widely used for decades. In general, signal processing in voltage domain such as addition, subtraction, and multiplication are trivial in the voltage domain by utilizing an amplifier [4]. Usually the accuracy of these operations can be improved by employing an amplifier with high gain. However, it is more and more challenging to design the amplifier with high gain in advanced technologies due to the reduced intrinsic gain of the devices. It is also noted that the scaled supply voltage for the advanced technologies makes it harder to design it for a given signal swing or leads to reduced signal swing, which results in increased power consumption for the same SNR requirement.

Recently, time domain quantization has drawn attention compared to the conventional voltage domain quantization due to its scalability benefits in recent deep submicron CMOS process [5], [6]. It also has potential for high speed/low power consumption from its operation based on more digital-like blocks. However, it is not easy to process the signal solely in time domain due to the lack of an amplifier with high gain versus the signal processing in voltage domain.

In this chapter, we will review some analog-to-digital converters which use the time domain signal for the data conversion, specifically focusing on high resolution while consuming low power consumption.

2.1 Data conversion using time domain information

Fig. 2.1 compares the conventional flash type ADC in voltage domain to the flash type time-to-digital converter (TDC) in time domain [5]. Both are very similar except that the ADC compares the input signal with the voltage reference and the TDC compares the input signal with the time reference. One difference between the time domain quantizer and voltage domain quantizer is that the time comparator compares the digital signal (up to VDD) with the logic threshold (usually VDD/2) while the voltage domain comparator compares the input signal with the reference voltage which can be smaller than the supply (VDD) in general. As shown in paper [6], the power efficiency of the time domain quantizer can be improved further over the voltage domain quantizer especially with advanced processes for the thermal noise limited design. Similar to the case of the conventional flash ADC in voltage domain, the resolution of the flash type TDC is also limited and the power consumption increases exponentially with the TDC resolution. To efficiently increase the resolution in time domain, many innovative TDC architectures have been proposed [7]-[15].

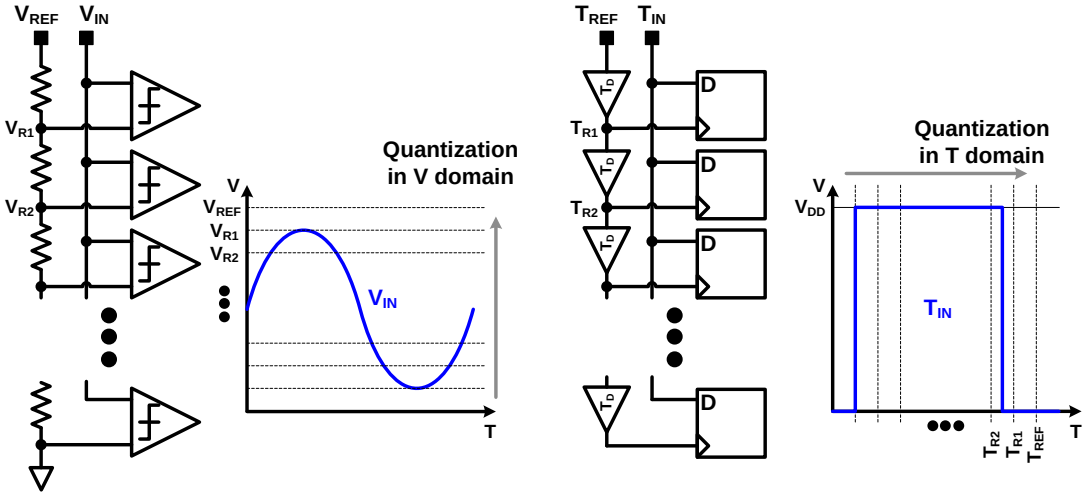

Figure 2.1: Flash type ADC vs. TDC

2.1.1 Vernier delay line based TDC

In a flash type TDC, the time resolution is determined by the minimum delay of the single delay cell which is used for the time reference generation. The resolution of this TDC can be improved by a Vernier delay line shown in Fig. 2.2 [9]. This technique is based on a Vernier principle. Using the delay difference between upper and lower delay cells, the possible range of the measured time T_O is

$$n \cdot \Delta T < T_O < (n+1) \cdot \Delta T \tag{2.1}$$

where ΔT is the delay difference T_{D1}-T_{D2}. Therefore by using a small delay difference between T_{D1} and T_{D2}, the resolution of this TDC can be increased compared to the TDC using single delay cell. However, the area of the Vernier delay line based TDC increases linearly with the TDC resolution and the delay cell should match well for high resolution.

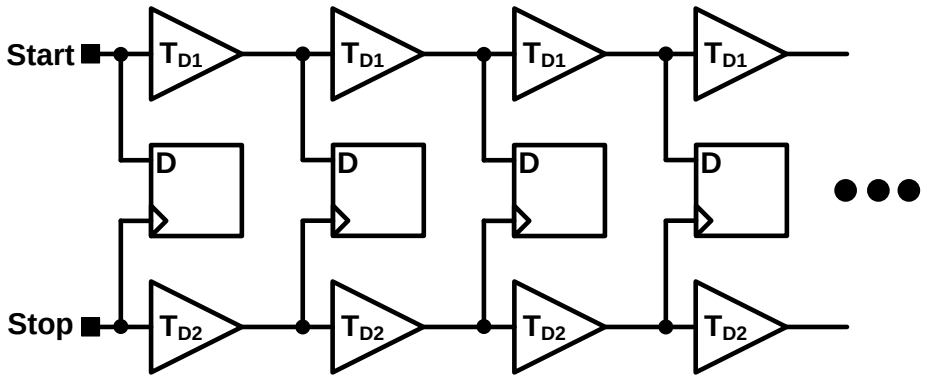

Figure 2.2: Vernier delay line based TDC

2.1.2 VCO based ADC

Fig. 2.3 (a) shows the general VCO-based quantizer. The VCO output frequency depending on the input is quantized by the digital logic in time domain. Due to its digital-like operation, this VCO based ADC can work at high speed with low power consumption. It also has a 1^{st}-order shaping of its quantization noise, which can improve the resolution, especially in an oversampled system [10]. As shown in Fig. 2.3 (a), the truncation error of the current counting edge is accounted in the following clock cycle. The quantization error is

$$error[n] = q[n] - q[n-1] \tag{2.2}$$

which provides a first-order shaping of the quantization error by the quantizer itself. However the non-linear characteristic between the input voltage and output frequency of the VCO limits the resolution. This limitation of the VCO based ADC can be improved by using it as a multi-bit quantizer in a delta-sigma modulator loop as shown in Fig. 2.3(b) [11]. Here the non-linearity of the VCO based ADC can be shaped by the loop filter. Although the nonlinearity of the VCO quantizer is shaped by the loop filter, this ADC still suffers from large harmonic distortion for high resolution applications.

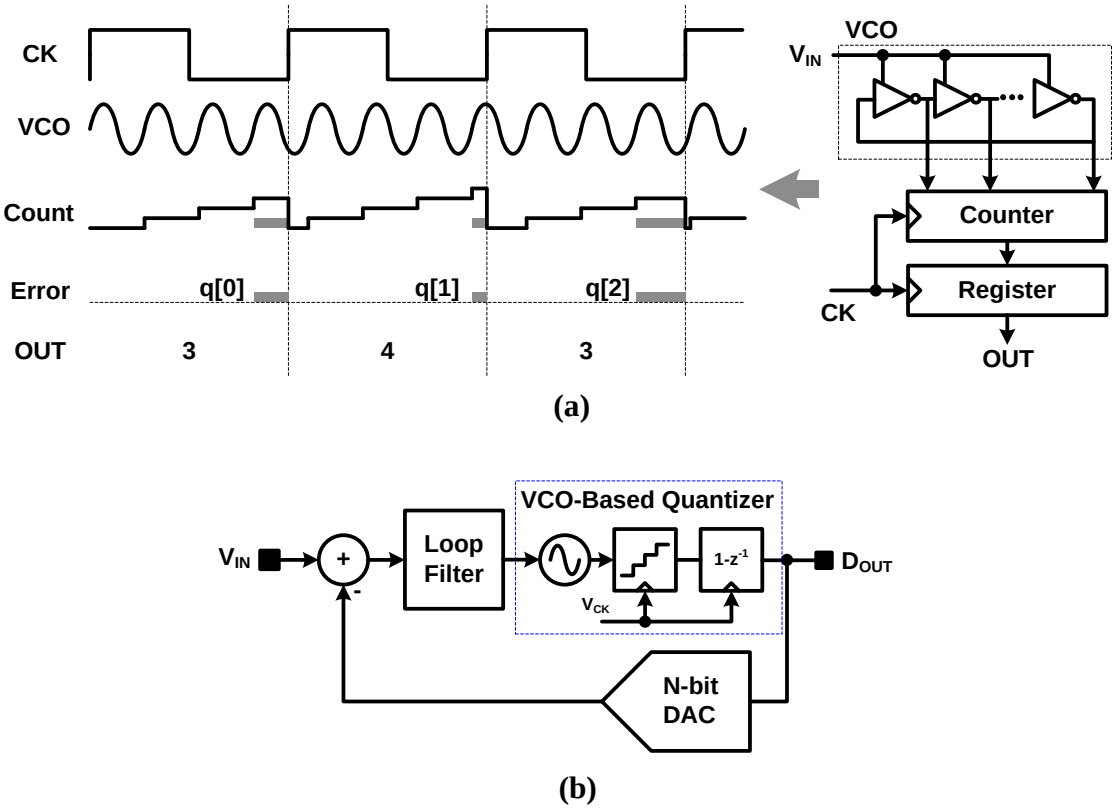

Figure 2.3: VCO based ADC (a) VCO based quantizer and (b) delta-sigma modulator with VCO-based quantizer

2.1.3 Multi-step TDC based on time amplifier

Similar to the case of the conventional ADC in voltage domain, the resolution of the TDC can be increased by using residue amplification in a multi-step architecture. In Fig. 2.4, the resolution is increased based on a two-step architecture with coarse and fine TDCs [12]. In this architecture, the time amplifier which uses the signal dependent delay in a meta-stable operation of the SR latch is used [13]. As analyzed in the paper [12], the small-signal gain in time domain of this amplifier is

$$A = \frac{2C}{g_m T_{off}} \tag{2.3}$$

where g_m is the transconductance of a NAND gate during the meta-stable operation and C is the output capacitance. The resolution of the two-step TDC is mainly limited by the non-linearity of the time amplifier. Another TDC with a pipelined architecture which uses similar type of time amplifier as a residue amplification is proposed but it requires a complex calibration for high resolution [14].

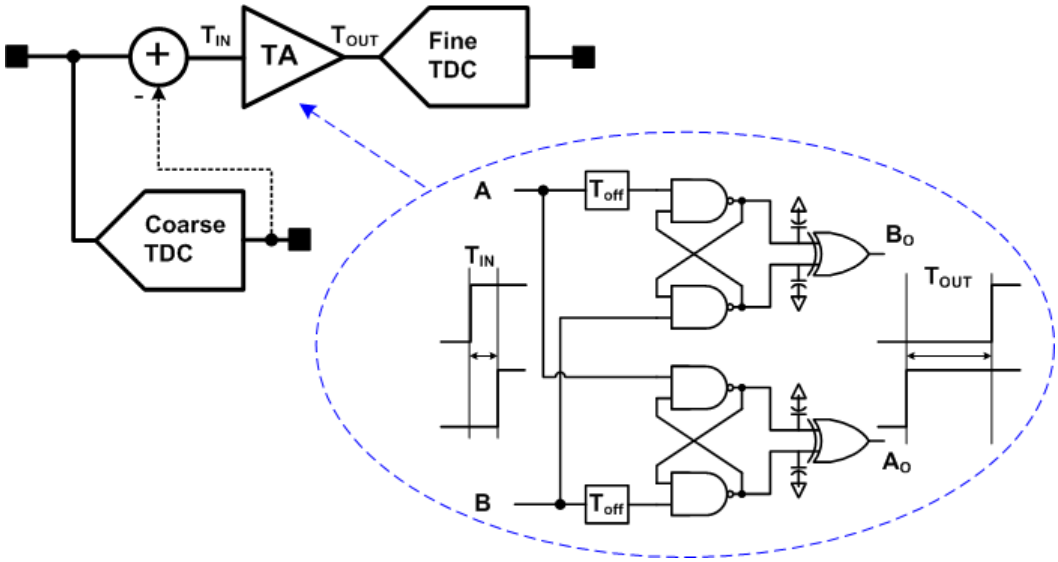

Figure 2.4: Multi-step TDC based on time amplifier

2.1.4 Algorithmic TDC with a current mode time amplification

Fig. 2.5 shows a power-efficient ADC using time amplification based on current mode operation [15]. In this architecture, the equivalent time amplification is done by measuring the time required to charge a capacitor with different current values. With a fixed time window T_{CK}, the input time is measured with the fixed current I_{IN}. Then it is quantized/amplified based on a different fixed current I_{REF}. The measured quantization error T_{Q1} in the first cycle is quantized/amplified again with I_{REF} in the next cycle. Then the next quantization error T_{Q2} is measured. This algorithmic ADC repeats the same operation to get the final quantization error. In this scheme, the gain of the time amplifier is defined by the current ratio between the input current and the reference current for the charging operations with matched capacitors. Therefore, the amplified time output is

$$T_{OUT} = \frac{I_{IN}}{I_{REF}} T_{CK} \tag{2.4}$$

This ADC shows good power efficiency due to the time based amplification method. However it has a limited linearity due to the V-T conversion at the input of the ADC and shows the limited performance only at low frequency due to the algorithmic architecture.

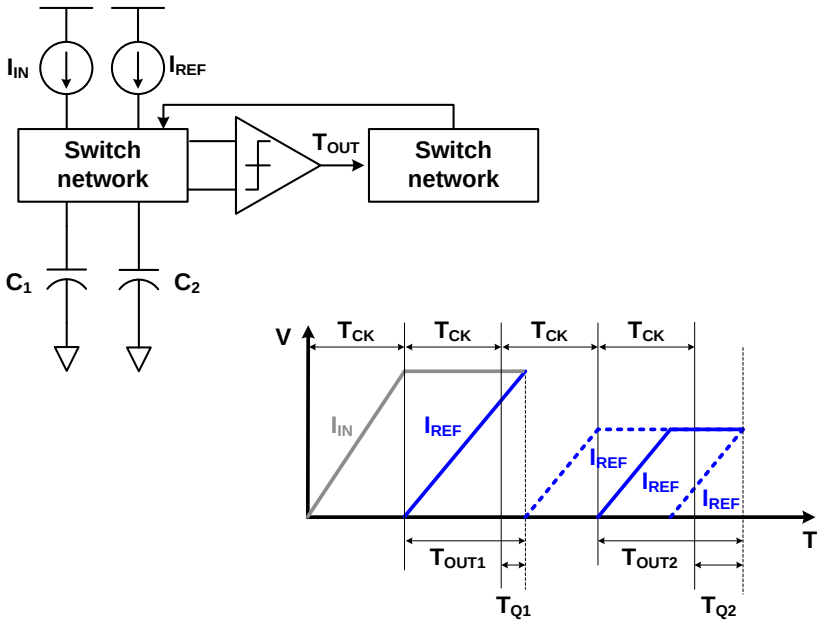

Figure 2.5: Algorithmic TDC with current mode time amplifier

2.2 Further usage of time and voltage domain information

As we reviewed in this chapter, there have been many efforts to increase the resolution in time domain while achieving low power consumption. The accuracy of the TDC can be improved with time amplification, but the resolution of the TDC is limited and not yet comparable to the resolution of the ADC in voltage domain. However, there are many interesting aspects using the time domain information as well as the voltage domain information in data conversion in conjunction with each other, which will be explored in later chapters of this dissertation. In the next two chapters, new ADC architectures will be proposed, which use the voltage and time domain information to achieve high resolution and efficient power consumption.

CHAPTER 3. A SECOND-ORDER DELTA-SIGMA ADC USING NOISE-SHAPED TWO-STEP INTEGRATING QUANTIZER

In the past two chapters, we have described the data converters which use the time domain information for high resolution with low power consumption. In this chapter, we will take a closer look at the usage of the time domain information as well as the voltage domain information in the contents of delta-sigma modulator for high resolution with good power efficiency. For this, we will start by taking a brief review of the noise-shaped integrating quantizer. Then the proposed noise-shaped two-step integrating quantizer is explained. After that, the proposed ΔΣ ADC incorporating the noise-shaped two-step integrating quantizer and studies some key aspects of the proposed ADC are presented. The implementation details and considerations of non-idealities are followed in later of this chapter, respectively. Finally, measurement results are provided. This design was initially published in [16] and most of the text in this chapter is based on [17].

3.1 Motivation

With an increasing demand to process a large amount of data in mobile communication systems, higher resolution and bandwidth is necessary. ADCs in these systems need to provide such performance with minimal power consumption for portable systems. Delta-sigma ADCs which are based on oversampling are suitable candidates for high resolution and medium signal bandwidth. In order to achieve high resolution and wide signal bandwidth in an

oversampled ADC, either the sampling frequency should be increased or the modulator should provide more efficient noise shaping. The former will result in increased power consumption whereas the latter might result in instability and/or reduced dynamic range. On the other hand, it is possible to increase the number of quantization levels which in turn will reduce both the in-band and out-of-band quantization noise power, resulting in improved signal-to-noise ratio (SNR) and improved stability, enabling the possibility to reduce the oversampling ratio (OSR) requirement.

There have been many different approaches to use a high resolution quantizer in delta-sigma ADCs [18]-[21]. However, those ADCs need expensive analog components [18]-[19] or complex digital calibration [20]-[21] to match the analog and digital transfer functions. In order to utilize a high resolution quantizer and to reduce power consumption at the same time, the number of active components (e.g. operational amplifiers) should also be minimized. Recently, several innovative quantizers in ΔΣ ADCs which provide an extra order of noise-shaping have been proposed [11], [22]-[23]. However, it is difficult to achieve high resolution and low power consumption with these quantizers due to the inherent non-linear characteristic of voltage controlled oscillator (VCO) [11] and/or limited time resolution [22]. The noise-shaped two-step quantizer shown in [23] can easily achieve higher resolution than other quantizers but it consumes more power from its large residue gain and complex error feedback. In addition to the above mentioned issues, the complexity of the feedback DAC path in ΔΣ ADC with a high resolution quantizer also should be resolved, because the high resolution of quantizer makes it difficult to implement its feedback DAC and corresponding dynamic element matching logic [24].

A new two-step integrating quantizer with inherent noise shaping is proposed. The proposed quantizer not only obtains high resolution from the two-step quantization but also provides a first-order noise shaping by means of quantization error feedback. By minimizing the residue gain in the first step and employing time-domain quantization in the second step, the power consumption of this quantizer is reduced. The benefits of the proposed two-step quantizer are explored in a second-order ΔΣ ADC with a first-order loop filter [16]. The proposed structure also alleviates the design difficulties in feedback DAC path with an 8b two-step quantizer. This is done by employing separated feedback paths topology which utilizes capacitive and analog residue DACs.

3.2 Noise-shaped two-step integrating quantizer

3.2.1 Noise-shaped integrating quantizer

The noise-shaped integrating quantizer is shown in Fig. 3.1 [25]. This structure is based on the conventional dual-slope ADC with a modified discharging phase: the discharging is terminated at the next clock edge after the zero-crossing. By doing so, the quantization error is stored in the integrating capacitor. In the next charging/sampling phase, the capacitor is not reset before charging, which will result in the quantization error to be subtracted from the input. Thus, this quantizer provides a first-order noise shaping. This quantizer can be used as a multi-bit quantizer in a standard oversampling ADC, providing an extra order of noise shaping. Furthermore, it can also work as an active adder which makes it attractive to use it in

the delta-sigma modulator. The main drawback of this technique is the limited quantizer resolution due to the high speed requirement of the counting clock.

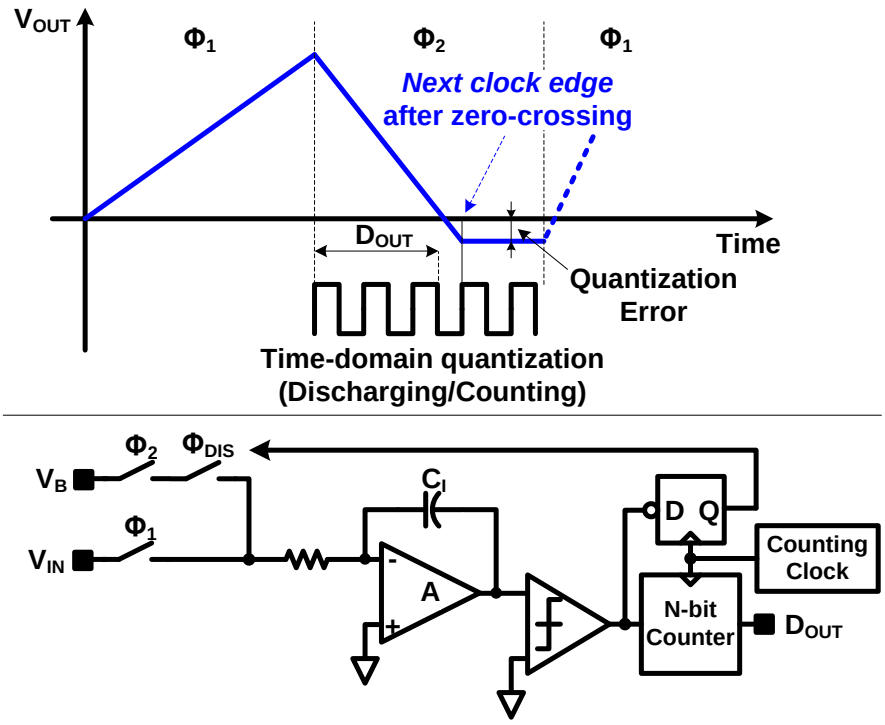

Figure 3.1: Noise-shaped integrating quantizer

3.2.2 Proposed two-step integration quantizer

Fig. 3.2 shows the proposed two-step noise-shaped integrating quantizer. This quantizer is similar to the conventional two-step quantizer (or a single stage of a conventional pipelined ADC [26]) with a multiplying-DAC (MDAC), except that it utilizes time-based quantization for the fine quantization. This quantizer consists of a coarse flash sub-ADC (FLASH), an MDAC, a zero-crossing detector, a fine time-to-digital converter (TDC), and additional circuitry for discharging operation.

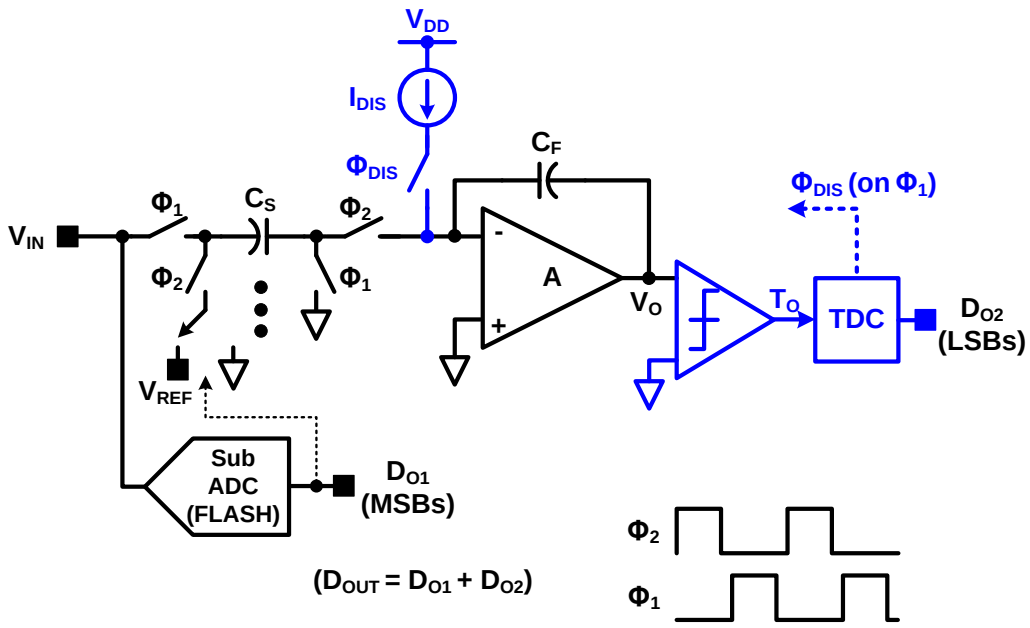

Figure 3.2: Proposed noise-shaped two-step integrating quantizer

The operation principle of the proposed quantizer is shown in Fig. 3.3. The sampled input signal is quantized in the sampling phase Φ_1 by the sub-ADC. During amplification phase Φ_2, the DAC subtracts the corresponding reference from the sampled input signal depending on the output code from the sub-ADC. Shown in Fig. 3.3, the coarse quantization error E_1 remains at the output of the residue amplifier at the end of Φ_2 as a residue signal with an equivalent gain of 1. During the next sampling/discharging phase Φ_1, the sampling capacitor is disconnected from the virtual ground to sample the next input signal. At the same time, the residue output (E_1) in voltage domain is discharged and it is quantized by the TDC. After this step, the fine quantization error E_2 is preserved on the feedback capacitor of the MDAC amplifier as a voltage signal (similar to the noise-shaped integrating quantizer) [25]. During the next conversion step (next Φ_2), the stored quantization error is inherently subtracted from

the next input sample, providing first-order quantization noise shaping. Finally, D_{OUT} is obtained after the two-step quantization.

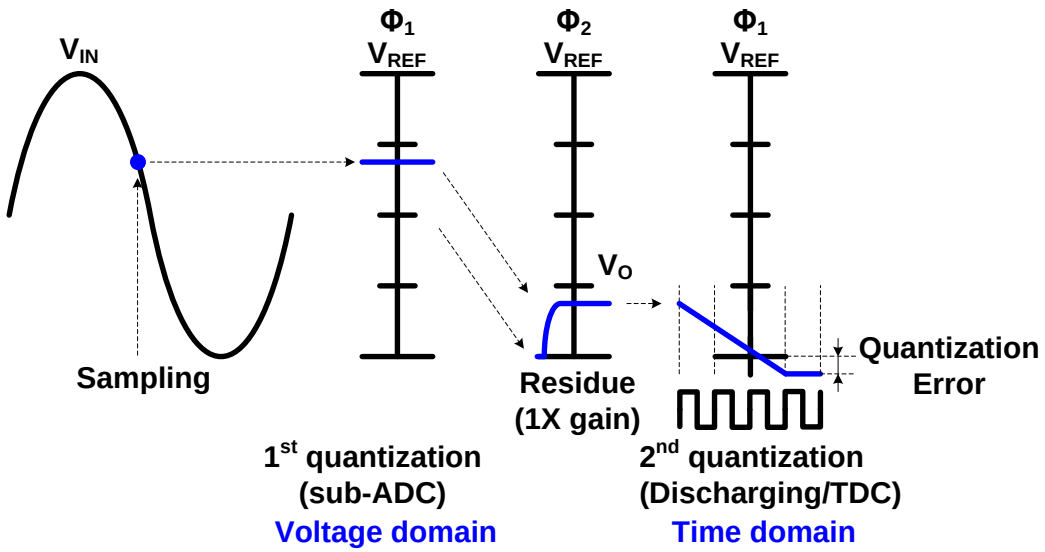

Figure 3.3: Operation of the proposed two-step quantizer

To analyze the linearized model of the proposed quantizer, Fig. 3.4 is provided. The coarse and fine quantization errors, i.e. E_1 and E_2, are generated from each quantizer after two-step quantization. The feedback of fine quantization error E_2 to the input illustrates the subtraction of the previous sample of quantization error from the current one. This is an inherent property of the noise-shaped discharging quantizers. Under ideal condition, the first-step quantization error E_1 will be completely cancelled, and the digital output of the proposed two-step quantizer in Z-domain will be

$$D_{OUT}(z) = V_{IN}(z) + (1 - z^{-1})E_2(z). \tag{3.1}$$

The simulated output spectrum of this quantizer is shown in Fig. 3.4(b) and it is compared to that of the traditional two-step ADC. It is evident from this figure that the proposed quantizer provides the first-order noise shaping for the fine quantization error, resulting in drastic SQNR improvement in the lower frequency range.

This structure has several advantages over the traditional quantization method. First, it can resolve a large number of bits, (because of the two-step quantization), without being penalized with a significant additional power consumption as in conventional flash quantizers. Second, due to the unity residue gain, the amplifier has only a small output swing requirement and can be designed for low power and high linearity under a low supply voltage. Third, the jitter requirement of the TDC portion of the circuit is relaxed compared to that of the conventional TDC-only quantizer [27] for the same total quantization levels, as illustrated in Fig. 3.5. In this example, 4b quantizer is used. It can be seen that the proposed quantizer has 4 times larger LSB in time than the conventional TDC, which relaxes the design requirement, and subsequently reduces the power consumption of the time-reference circuitry. Therefore, the proposed ADC is less sensitive to the counting clock jitter in the quantizer, which allows using a coarse PLL/DLL to be used to generate these edges. However, the sampling clock jitter follows the same criteria as in any regular discrete time ΔΣ ADC. Finally, the proposed quantizer provides an extra order of noise shaping with minimal modification from the conventional quantizer. Therefore the proposed quantizer is a good candidate to be used in high order ΔΣ ADCs. Also the embedded adder-operation in the MDAC of the proposed quantizer can provide more advantage, especially in ΔΣ ADCs with a feed-forward architecture. This will be described later.

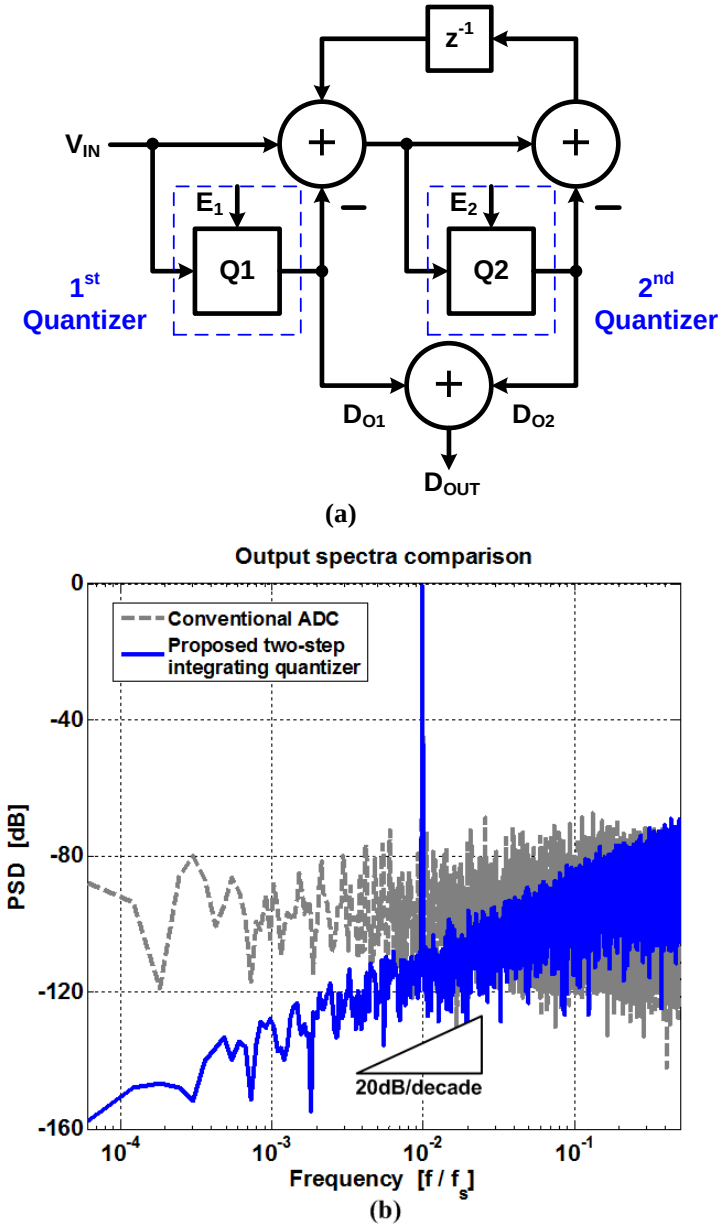

Figure 3.4: Proposed two-step quantizer: (a) linearized model and (b) behavioral model simulation

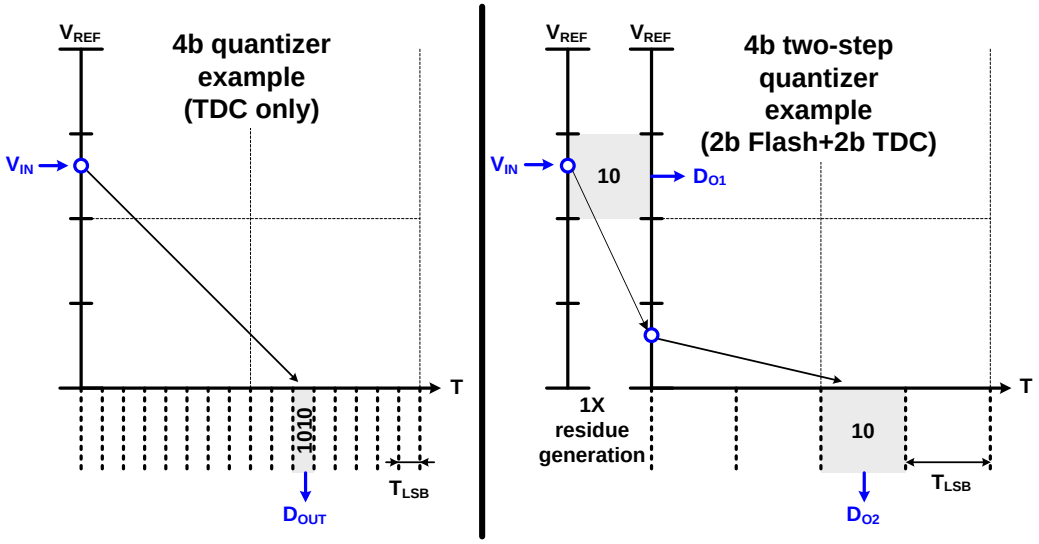

Figure 3.5: Jitter sensitivity comparison of the proposed two-step quantizer vs. TDC only quantizer

3.3 Proposed ΔΣ ADC with two-step integrating quantizer

Fig. 3.6 shows the proposed ΔΣ ADC employing the proposed noise-shaped two-step integrating quantizer. It consists of a first-order loop filter, two-step integrating quantizer including an MDAC, a 5b flash sub-ADC, a zero-crossing comparator, a 4b TDC, and a digital correction logic (DCL). After the two-step quantization, the final 8b digital output is generated from the DCL with 1b redundancy between the coarse and fine quantizers. As in a conventional pipelined ADC, the decision error from the coarse quantizer up to +/- 4 LSBs is easily corrected with the error correction scheme based on the 1b redundancy [28]. This ADC also adopts the well-known feed-forward architecture to process mostly the quantization noise in the loop filter [29]. The added error feedback ($-z^{-1}E_2$) generated from the discharging of the coarse quantization error and time-domain quantization will cancel E_1 (coarse quantization error) and leaves only E_2 in the loop and in the final digital output. With an extra order of

noise shaping from the quantizer, the proposed ΔΣ ADC has a second-order NTF using only first-order loop filter. The proposed ADC can achieve SQNR over 80dB at low OSR of 8 owing to the high resolution of 8b from the proposed two-step quantizer. In this section, the details of the modulator loop and the quantizer are discussed.

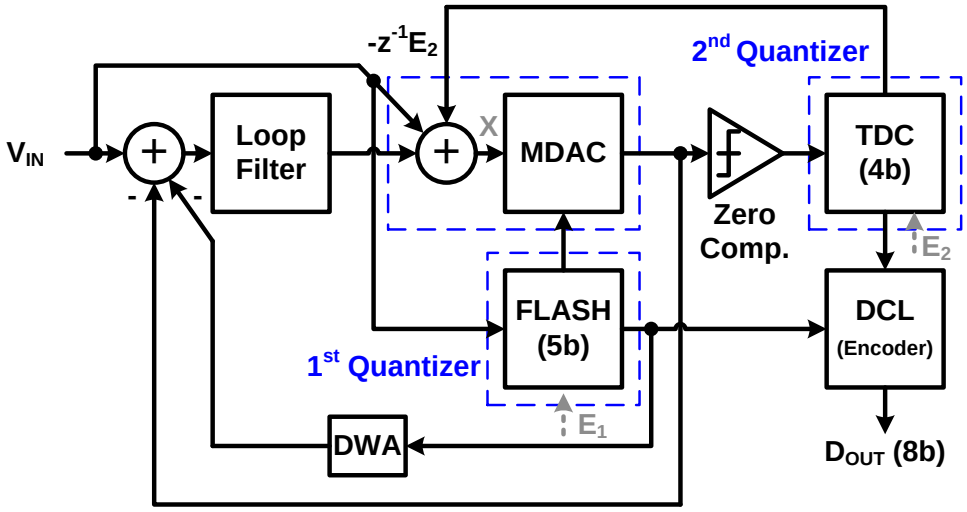

Figure 3.6: Proposed second-order discrete-time ΔΣ ADC incorporating the noise-shaped two-step integrating quantizer

3.3.1 Feedback DAC

One of the main limitations in the design of a ΔΣ ADC is the accuracy of the global feedback DAC path. In ΔΣ ADCs with a large number of quantization levels, the required elements and the complexity in the feedback DAC path are increased exponentially. Furthermore, the commonly used dynamic element matching technique such as data-weighted averaging (DWA) will worsen the matter. In a given ADC design, the multiple gate delay from the DWA can also limit the conversion speed especially if it utilizes a narrow time window for the DWA operation [30].

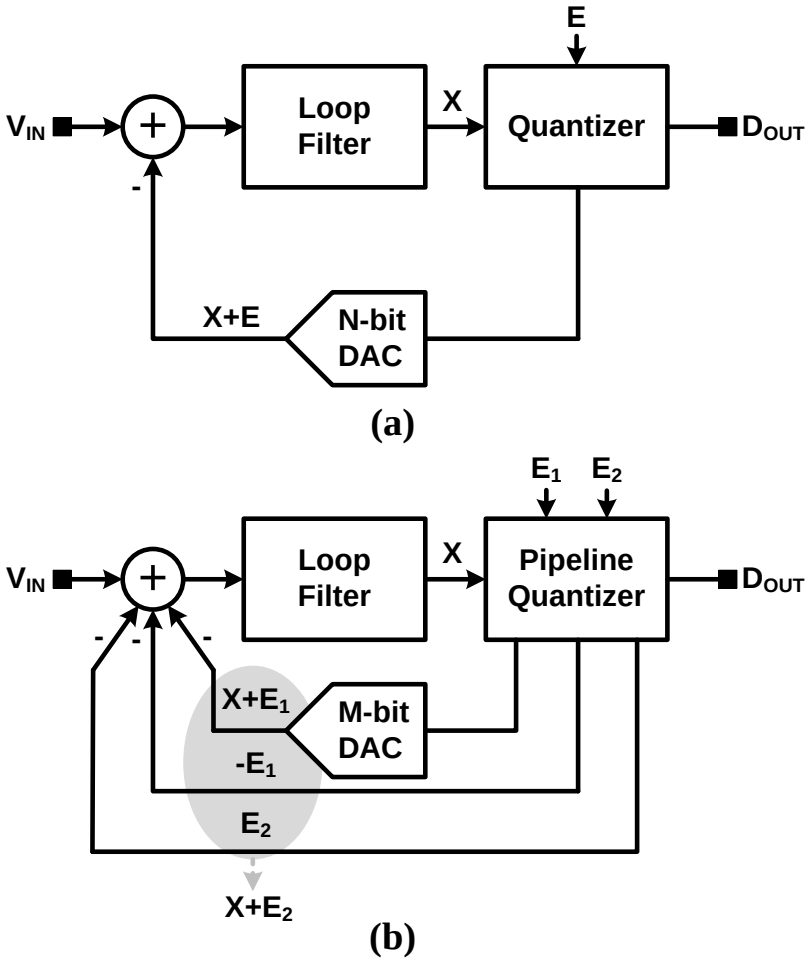

Figure 3.7: Conventional feedback DAC configuration with multi-bit quantizer: (a) general feedback topology and (b) separated feedback topology in [31]

To alleviate these problems, an improved feedback topology based on separated feedback paths [31] is proposed. Fig. 3.7(a) shows the conventional feedback method for a multi-bit quantizer. Compared to the conventional feedback for multi-bit quantizers, the separated feedback method shown in Fig. 3.7(b) utilizes only MSBs from the first pipeline stage in its main feedback DAC path. The coarse quantization error E_1 is cancelled in the analog domain by providing the analog residues from the first and final pipeline stages which represent the

coarse and fine quantization errors (E_1 and E_2) in the additional feedback paths. After E_1 cancellation, the signal equivalent to V_{IN}-($X+E_2$) is integrated onto the integrating capacitor, where X is the input signal of the pipeline quantizer. Because only MSBs are used in the main/global DAC path, the complexity of the global feedback path is reduced significantly in this feedback method. This separated feedback topology can be easily adopted in an ADC with a high resolution quantizer as long as the analog residues of E_1 and E_2 are accessible.

Fig. 3.8 shows the feedback topology used in the proposed ADC. Because both analog residues (E_1 and E_2) are available from the MDAC after residue generation and discharging/time-domain quantization, the simple separated feedback method can be adopted in the proposed ADC. Hence, instead of providing all the digital outputs from the quantizer to operate the feedback DAC, only the MSBs from the 5b sub-ADC operate the global feedback DAC. As a result, only 5b DWA logic is required in MSB feedback path.

To simplify the feedback path even further, the LSBs (4b TDC output) are fed back in analog form by subtracting the output of the MDAC after both residue amplification and discharging phases. This will effectively subtract ($-E_1+E_2$) using a single capacitor and results in the cancelation of E_1 in the loop filter. After E_1 is cancelled, the proper signal is integrated onto the integrating capacitor. Fig. 3.9 shows the details of the proposed feedback method. One of the interesting advantages of this structure over [31] is the reduced slew-rate requirement of the MDAC and the first integrator of the modulator. This is due to the fact that the analog residue E_2 is generated by the linear discharging at the output of the MDAC. Hence, the analog feedback which drives the first integrator of the modulator does not encounter a fast slewing/settling behavior.

To minimize the gain mismatch between the two feedback paths (MSBs DAC & analog residues), two matched capacitor sets are used. The matching requirement is also relaxed by the resolution of the first quantizer. For instance, if the ADC needs 12b linearity and the resolution of the first quantizer is 5b, the required matching accuracy between two paths is about 7b (without considering OSR), which is not difficult to achieve. With a higher OSR, the matching requirement is relaxed even further. Because a single capacitor is used for the two residue feedbacks in the proposed topology, there would be no gain mismatch between the coarse and fine residue paths.

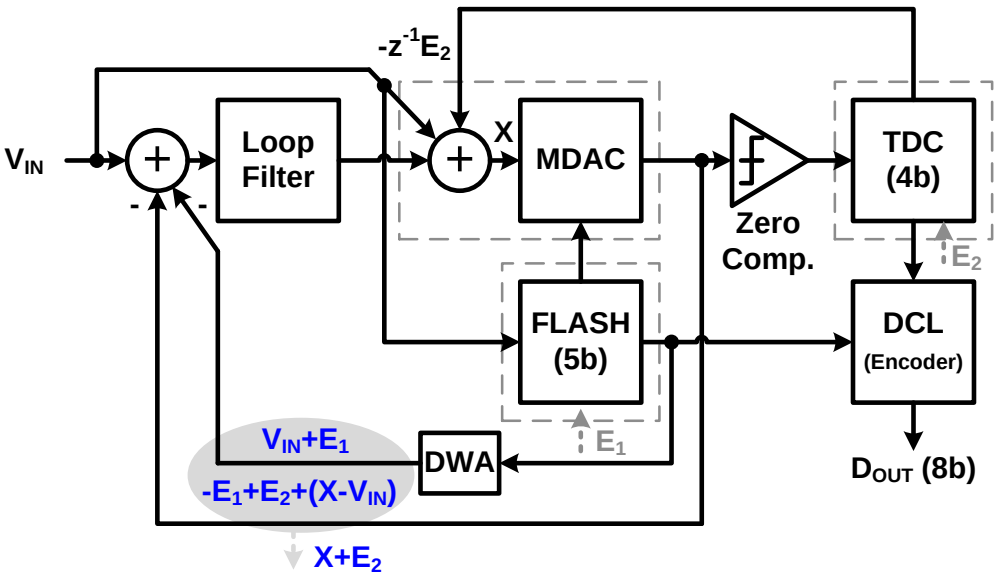

Figure 3.8: Feedback configuration of the proposed ADC employing the separated feedback topology

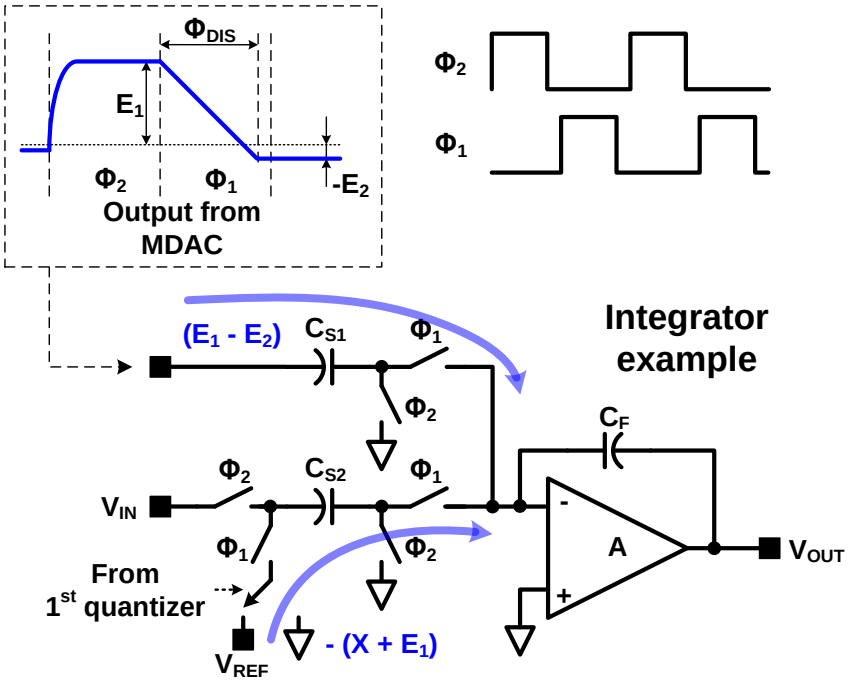

Figure 3.9: Implementation example in an integrator of the proposed separated feedback topology

3.3.2 Uni-directional discharging

To quantize the coarse quantization error in time domain and store the resulting fine quantization error onto the integrating capacitor, the residual charge on the virtual ground after the residue amplification must be discharged. In this work, we use uni-directional discharging as shown in Fig. 3.10. The non-zero delay in the discharging loop manifests as a fixed time offset which does not produce a signal dependent error in this uni-directional discharging scheme. This delay will add a fixed offset in the DAC path, which does not affect the ADC performance. Even though this offset reduces the signal range of the second quantizer, it can be easily corrected by providing an equal offset with an opposite polarity. The accuracy of this offset correction is relaxed by the redundancy range of the two-step quantizer. Although by

doing so the range of signal swing will be doubled at the MDAC output, it is not difficult to achieve the required swing due to the small residue gain of 1 in the proposed two-step quantizer.

To implement the uni-directional discharging with zero-crossing detection for the entire signal swing (+/- 8 LSBs), a fixed offset up to half of the MDAC output swing should be added to guarantee that the MDAC output is always greater than zero. In other words, the output of the MDAC at the end of the amplification phase should be above the comparator reference for proper discharging. Therefore, a voltage offset of up to 8 LSBs of the fine quantizer is added through the offset correction capacitor in the MDAC during the residue amplification phase. As a result, the residue output is always discharged to a differential zero without changing the polarity, which makes it easy to detect the zero-crossing with a simple zero-crossing comparator. In a nominal condition without the decision error from the coarse quantizer, the MDAC output swing ranges are from 4 LSBs to 12 LSBs as show in Fig. 3.10. The rest of the signal ranges, 0 to 4 LSBs and 12 to 16 LSBs are used for the error correction with 1b redundancy.

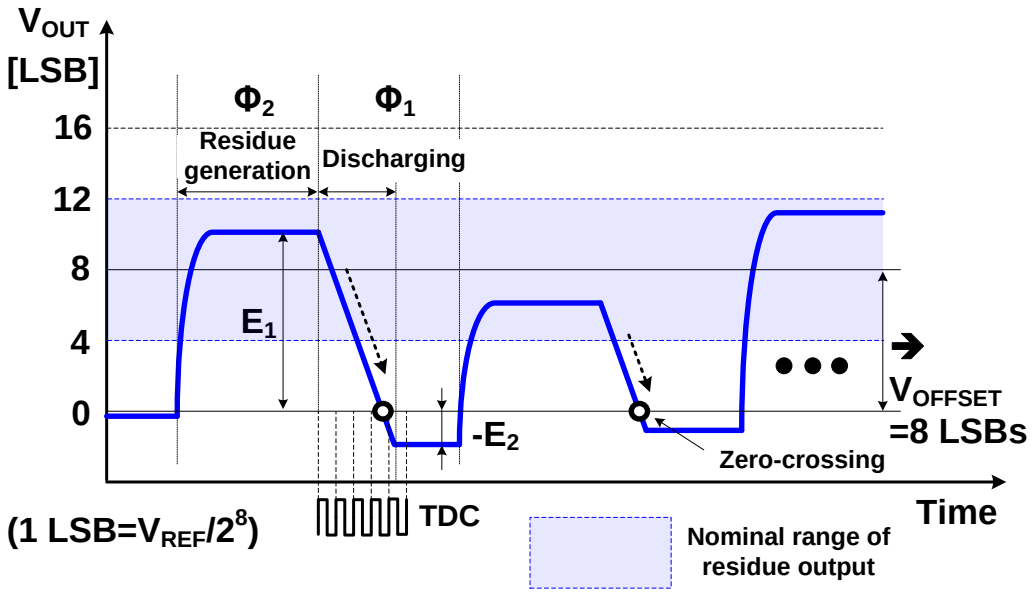

Figure 3.10: Uni-directional discharging of the proposed quantizer employing 1b redundancy between the coarse and fine quantizers. The shaded area shows the nominal range of the MDAC output (+/- 4LSBs) without the decision error from coarse quantizer (5b FLASH)

3.3.3 Quantizer input configuration

One important characteristic of this ADC is that the integrator does not drive the flash quantizer, thus the amplifier power is further reduced [31]. Fig. 3.11 shows the signal summation paths and the input configuration of the two-step quantizer. This configuration is made possible by the small output of the integrator (loop-filter) by combining the low-distortion structure with a very large number of quantization levels. In the low-distortion architecture, the output of the loop filter only contains filtered quantization error. Therefore, this output will be very small regardless of the input signal, if a high resolution quantizer is employed. Hence, in the proposed structure, the path from the loop-filter's output to the input of the flash ADC can be removed, assuming that the loop-filter's output is significantly smaller than the input signal. This brings forth an important advantage: the amplifier in loop

filter has the benefit of driving less capacitive load; by avoiding to drive the input capacitance of the flash ADC and its associated routing. Because the flash ADC only has one input signal which is from the feed-forward path (i.e. the input signal of the modulator), the input of the flash ADC is different from the input of the MDAC which has all required signals as the input. However, this signal difference between the MDAC and FLASH paths can be absorbed by the redundancy of the two-step quantizer, as long as the total error is contained within the available redundancy range. Simulation shows that the signal difference between the two sampling paths is around +/- 1.5 LSBs (1 LSB = $2.4V_{P\text{-}P}/2^8 = 9.375mV_{P\text{-}P}$). If the error from the first quantizer is larger than the designed 1b redundancy range (+/- 4 LSBs), it can saturate the second quantizer. In this case, the modulator loop can become unstable. Therefore, in the flash ADC design, the reduced redundancy range should be considered with care.

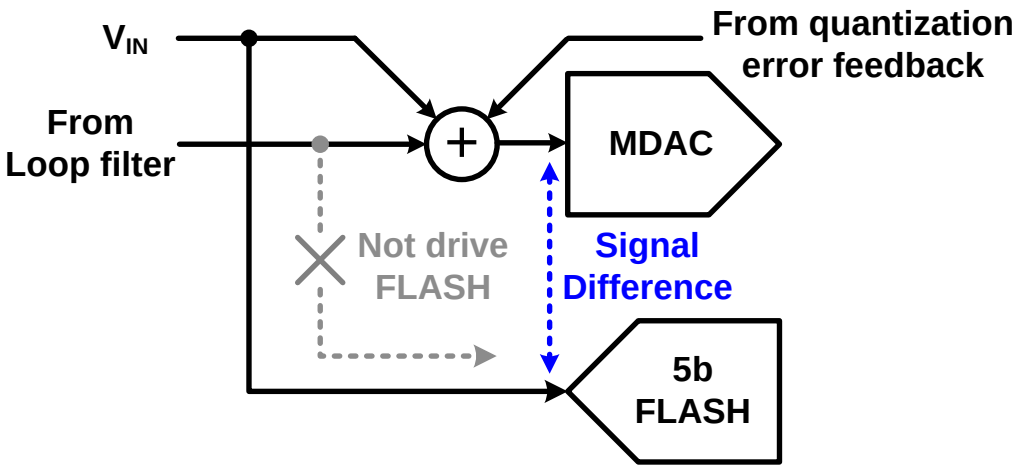

Figure 3.11: Quantizer input configuration of the proposed ΔΣ ADC

3.4 Circuit implementation

3.4.1 Flash quantizer

To minimize the comparator offset in the 5b flash quantizer, each comparator employs a two stage pre-amplifier incorporating an auto-zeroing scheme as shown in Fig. 3.12. The Monte-Carlo simulation results indicate that the designed comparator has +/- 3σ input referred offset voltage of less than +/- 6mV, which is equivalent to a quarter LSB of the 5b flash.

In addition to the error from the comparator offset, any error from sampling aperture mismatch in the feed-forward input signal between the flash ADC and the MDAC paths can also reduce the allocated 1b redundancy range. Therefore, the comparator operates with the same sampling phase Φ_2 as in the MDAC to minimize any sampling inaccuracy/mismatch between the flash ADC and the MDAC paths. This also helps to alleviate the common problem found in ADCs without a dedicated sample-and-hold amplifier [32]. Therefore, the flash ADC generates its digital output at the *next* sampling phase Φ_2, which produces an additional delay of half clock cycle in the DAC path of the MDAC. This is different from the conventional flash quantizer generating no additional delay in its digital output without using the dedicated sampling phase. This additional delay can be easily corrected in the MDAC path by providing the same delay, which will be explained later. The dedicated time for the sampling provides enough time for the pre-amplification before the comparator decision, which enables the pre-amplifier to consume less power.

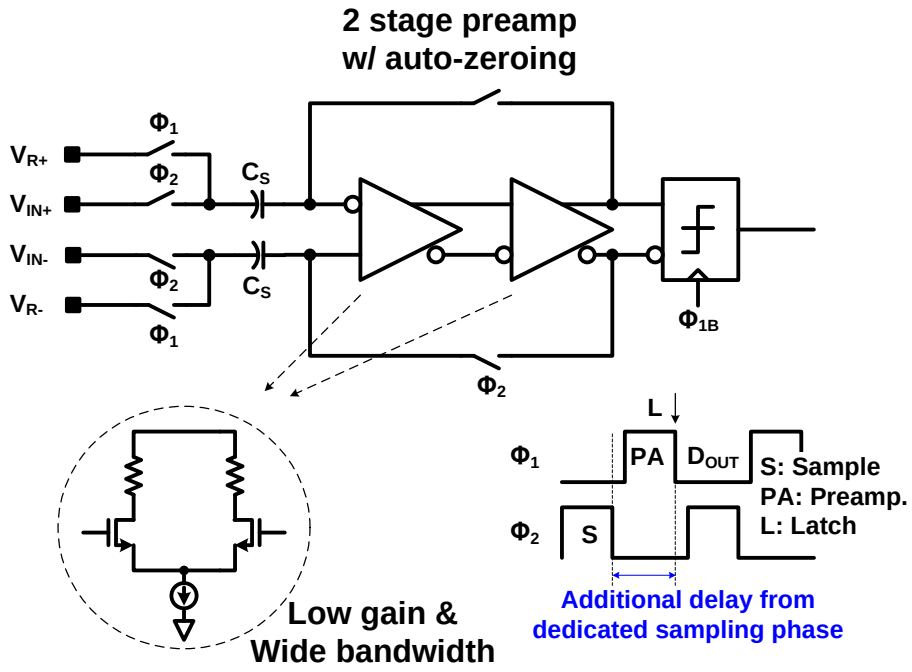

Figure 3.12: Comparator in 5b FLASH employing a two-stage pre-amplifier

3.4.2 Multiplying Digital-to-Analog Converter (MDAC)

Fig. 3.13 shows the implemented MDAC. The number of capacitors for a 5b DAC operation is reduced by a factor of two (16 capacitors instead of 32 capacitors) by using the merged capacitor switching scheme [33]. The residue charge after the amplification phase is discharged with a fixed current source in this work.

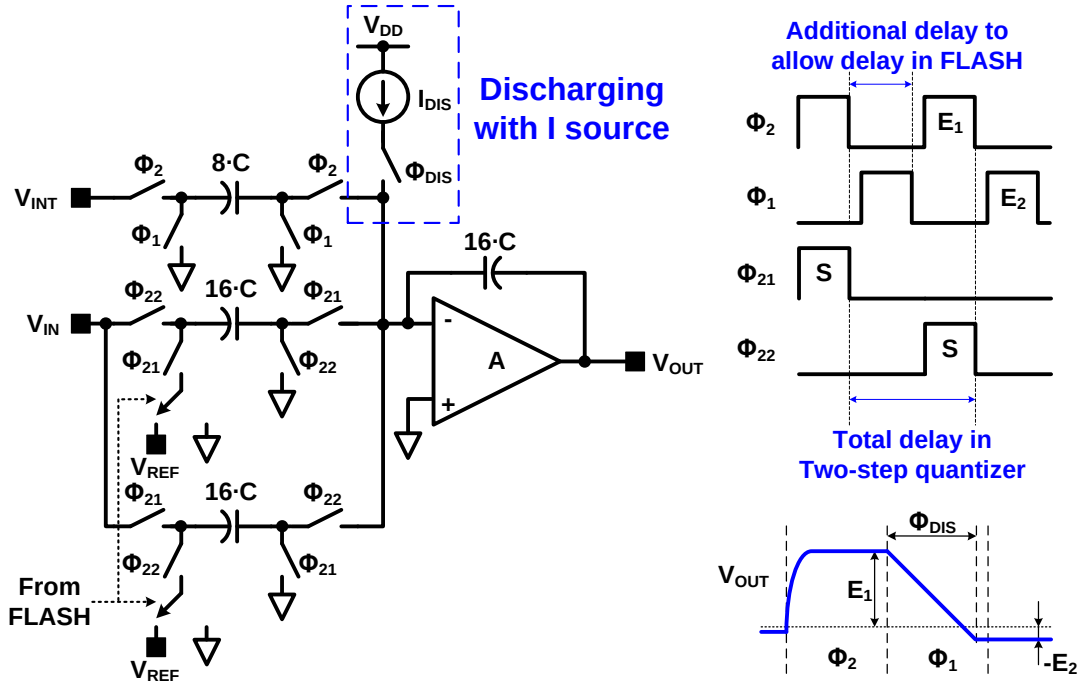

Figure 3.13: Multiplying DAC (MDAC) in the two-step quantizer (drawn as single-ended for simplicity)

To compensate the delay in the global feedback DAC path from the flash ADC, an extra set of capacitors providing a half cycle delay are employed. Therefore, the proposed quantizer generates one clock cycle delay to provide the coarse output (in digital bits) and fine output (in analog residue), after the two-step quantization. Because the fine quantization error E_2 is generated during Φ_1, the half clock phase Φ_2 can be used for the DWA operation of the coarse digital output. As a result, the 5b DWA has sufficient time for operation.

3.4.3 Integrator

The implemented first-order discrete-time loop filter is shown in Fig. 3.14. As explained earlier in this paper, the feedback DAC path is implemented with two separate DAC paths, a capacitive DAC path for the MSBs and an analog residue path for the LSBs. Also the number

of capacitors in the 5b MSB DAC path is also reduced by a factor of two (16 capacitors) similar to the MDAC capacitor array. The one cycle clock delay from the two-step quantizer is compensated by providing the same amount of delay in its input path using an extra set of capacitors. As explained earlier, the matching between the two DAC capacitors can be easily achieved with a careful layout for the targeted performance (approximately 7b matching required for 12b linearity). The total input capacitance is 900fF (C_{unit}=56fF). For low power consumption, a simple common source amplifier with an open loop dc gain of 25dB is used to satisfy the minimum gain requirement (20dB) of the integrator.

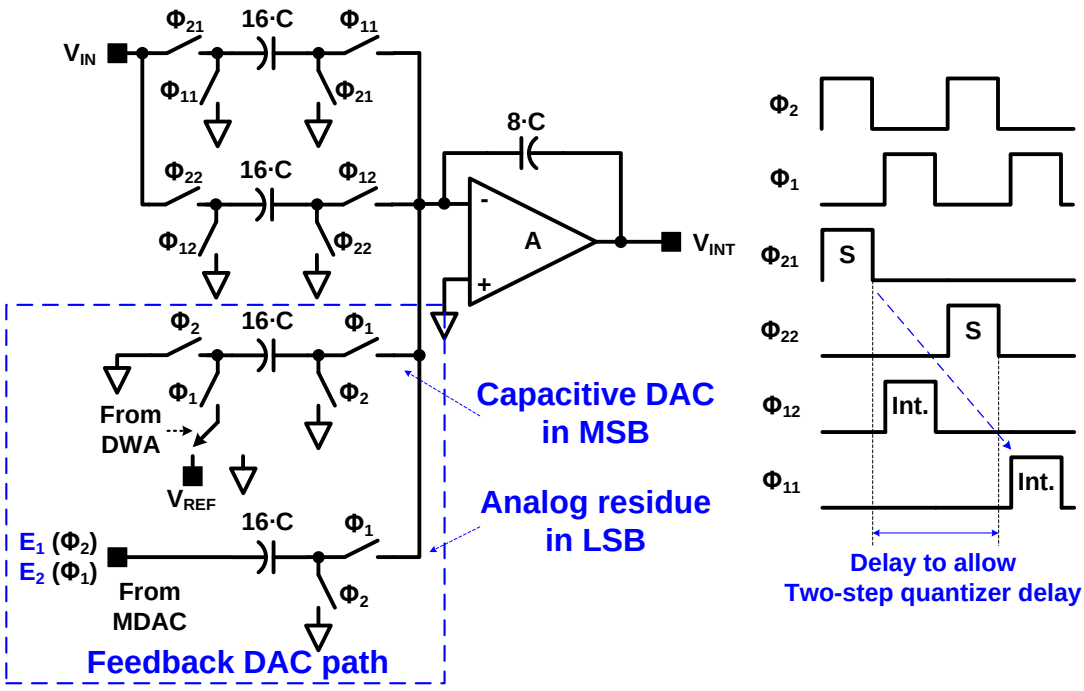

Figure 3.14: The front-end integrator of the modulator (drawn as single-ended for simplicity)

3.4.4 Zero-crossing comparator

Because of the uni-directional discharging scheme, the zero-crossing comparator always detects the same input voltage (differential zero) which produces a constant time delay. However, in practice, there is a signal dependency in the comparator delay due to finite comparator gain and bandwidth. This error is increased with smaller input signals [34]. To minimize the signal dependent portion of the comparator delay under a small input signal from the unity residue gain, a high gain and wide bandwidth comparator is employed. As shown in Fig. 3.15, this architecture is based on multiple cascaded stages with low gain and wide bandwidth.

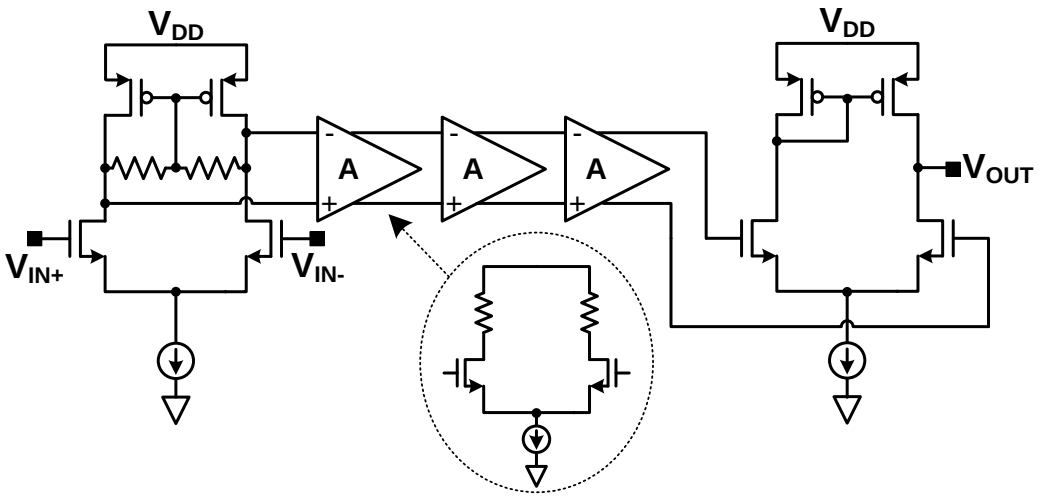

Figure 3.15: Continuous-time zero-crossing comparator

3.4.5 Time-to-Digital Converter (TDC)

Fig. 3.16 shows the proposed 4b TDC based on a simple flash type TDC architecture using D-FFs as time comparators [5]. It consists of a VCDL generating the time references, two-stage D-FFs as time comparators, and logic circuitry to generate a discharging pulse (Φ_{DIS}) and the 4b digital output.

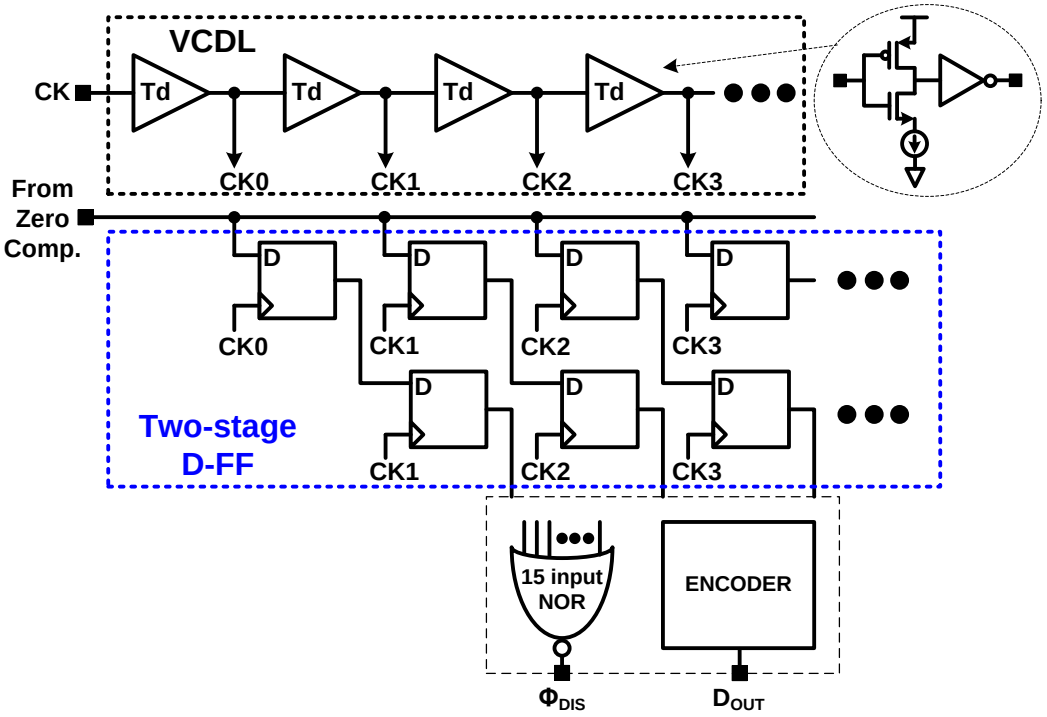

Figure 3.16: Time-to-digital converter (TDC)

In the proposed ADC, the discharging pulse from the TDC must be synchronized with the TDC time reference to provide proper noise shaping. However, the signal dependent delay of the D-FF is usually caused by the meta-stable condition due to a small time difference between the data input and clock input. Because the discharging pulse is generated based on

D-FF outputs, the signal dependent delay from the time comparator should be resolved especially when the time reference for the TDC is relatively small compared to the delay from the D-FF. Fig. 3.17 compares the two different time comparator architectures for different timing situations. In case 1, if the time difference between data input and clock reference is large enough, the delay from the D-FF is smaller than 1 LSB (in time) and almost constant. Then, the discharging pulse Φ_{DIS} is synchronized with the time reference CK1 in the time comparators of both the single and two-stage D-FF. However in case 2, if the delay from the D-FF is larger than 1 LSB (can occur when the data and clock edge are close), the signal T0 would be dependent on the delay from the D-FF in the single-stage D-FF case as shown in Fig. 3.17(a). Therefore Φ_{DIS} which is based on T0 depends on the signal dependent delay (it will not depend on the time reference) which would be problematic in the proposed ADC.

On the other hand, in the two-stage D-FF shown in Fig. 3.17(b), the Φ_{DIS} is still synchronized with the time reference because the delayed D-FF output in the first stage is detected by the second-stage D-FF with the next time reference CK2. Although there is a decision error in the two-stage case, this is not a critical problem; this decision error appears as an added quantization error and will be shaped/suppressed by the loop filter. Even though there is a possibility that the same problem occurs in the second stage D-FF (if the D0 and CK1 is on the same condition generating large delay), the probability is greatly reduced in the two-stage case versus the single-stage case. Therefore, the two-stage D-FF architecture is employed in the proposed TDC as a time comparator.

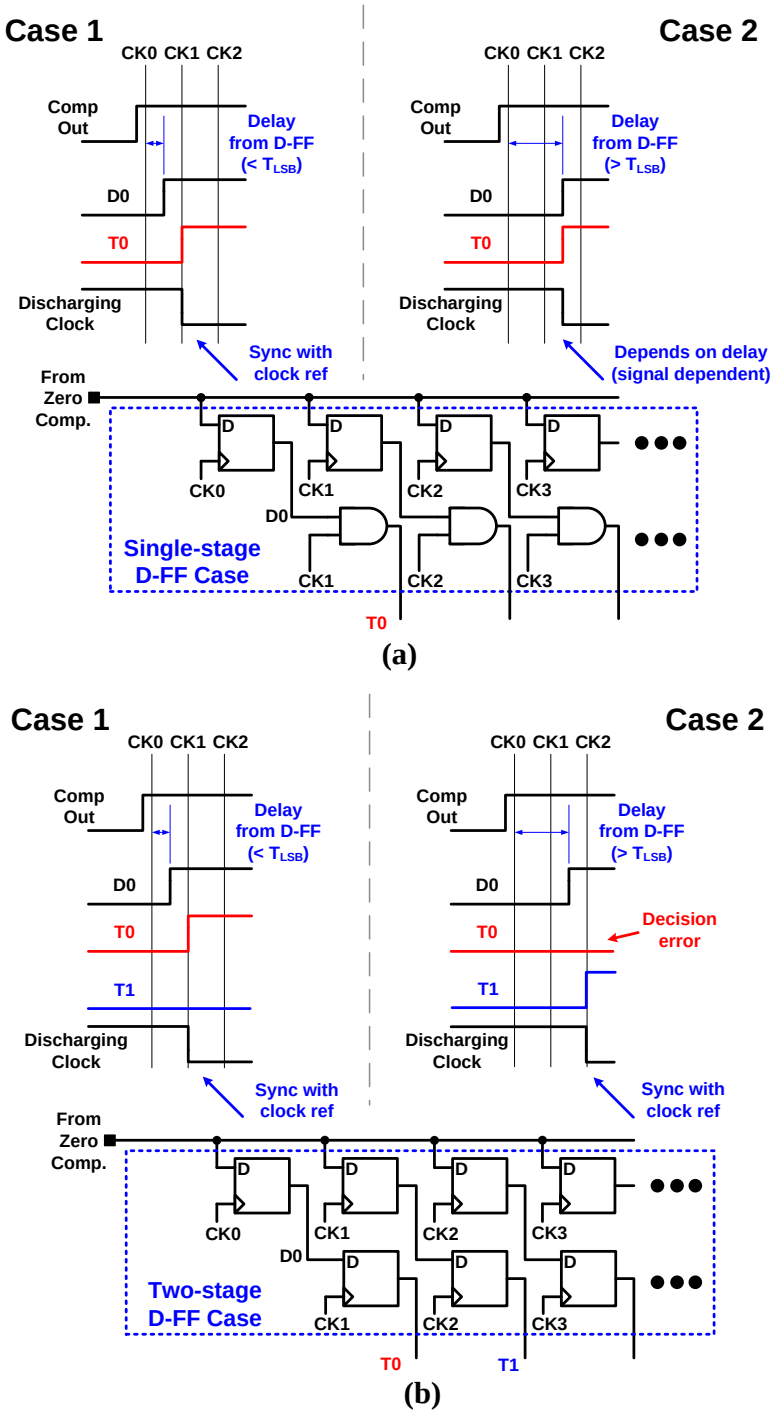

Figure 3.17: Comparison of two time comparator architectures considering different timing scenarios: (a) single-stage D-FF and (b) two-stage D-FF

3.5 Consideration of non-idealities

3.5.1 Noise

In the proposed ADC design, the noise from each block should be properly taken into account. This is because the ADC noise performance is affected not only by the noise from the integrator but also by the noise from the analog residue path. By adopting the separated feedback topology, the noise from the discharging current source and residue amplifier (in the MDAC) directly affect the noise performance of the ADC during the DAC operation. However, the noise induced error from these sources during the discharging phase is shaped by the loop filter because the noise induced error is processed by the fine quantizer itself and is fed back to the input through the DAC path (as an analog residue) at the same time.

Nevertheless, the noise induced error *after* the zero-crossing (such as counting clock jitter) is not processed by the fine quantizer and will appear directly at the ADC output through the residue feedback path, without being shaped by the loop filter.

3.5.2 Jitter from time reference

The jitter from the time reference in the two-step quantizer also affects the noise performance of the ADC. Although the proposed two-step quantizer has a reduced jitter sensitivity compared to the conventional TDC-only quantizer as explained earlier in this paper, the time reference should be designed with care. The jitter from the time reference in the fine time-domain quantizer affects not only the digital output of the fine quantizer, but also the DAC path of the ADC. Therefore, the jitter induced error *after* the zero-crossing directly affects the ADC noise performance through the feedback path for analog residue. By adopting

a voltage controlled delay line (VCDL) as a time reference generator, the jitter induced error from the external clock source can be minimized because the time reference from each delay cell has a fixed delay regardless of the jitter of the input clock. In this case, the jitter of the time reference is only affected by the jitter generated in each delay-cell and related logic circuitry for discharging control, which is usually much smaller than the jitter from an external clock source.

3.5.3 Signal path/gain mismatch

The mismatch error between the two signal/DAC paths in the MDAC is shaped by the loop filter because the error is processed by the fine quantizer and is fed back to the input through the DAC path at the same time. The calculated ADC output with the mismatch in the signal and DAC paths is derived as in the following equations. If we assume the mismatch error between the two paths in the MDAC as α_{Cmis}, which is injected at $F_S/2$, then the input of the 2nd quantizer (residue output of the MDAC) in the time-domain and Z-domain is

$$e_1(n)[1+\alpha_{Cmis}(-1)^n] \Rightarrow E_1(z)+\alpha_{Cmis}E_1(-z) \tag{3.2}$$

where $e_1(n)$ is the coarse quantization error. Note that the $(-1)^n e_1(n)$ term is transformed to $E_1(-z)$ based on the scaling property of the Z-domain transformation. Then the final output of ADC in Z-domain is

$$D_{OUT}(z) = V_{IN}(z) + \frac{(1-z^{-1})}{1+H(z)}E_2(z) - \frac{1}{1+H(z)}\alpha_{Cmis}E_1(-z) \tag{3.3}$$

where *H(z)* is the transfer function of the loop filter. As expected, the mismatch error is shaped by the loop filter. Therefore this error is not critical in the proposed ADC. However, the signal gain between the residue output in voltage domain and its representation through the discharging/quantization in time domain should be matched. The gain mismatch, between the analog residue (feedback in voltage domain) and its digital value (quantized in the time-domain by the fine quantizer) results in the leakage of the coarse quantization. This leakage directly appears at the ADC output. In this case, the calculated ADC output in Z-domain is

$$D_{OUT}(z) = V_{IN}(z) + \frac{(1-z^{-1})}{1+H} E_2(z) - \alpha_{gain} E_1(z) \tag{3.4}$$

where α_{gain} is the equivalent gain error between the voltage and time domain paths of the proposed quantizer. From equation (4), the coarse quantization leakage due to the gain mismatch is directly shown at the ADC output without any suppression. In this design, the allowed gain mismatch is approximately less than 1% (7b matching for 12b linearity without considering OSR).

3.6 Measurement results

The prototype ADC was implemented in a 0.13µm CMOS process. Fig. 3.18 shows the die photograph of the fabricated prototype [16]. The active area is 0.37mm^2 (593µm by 616µm). In the prototype measurement, the gain mismatch (between the voltage domain and the time domain in the two-step quantizer) is corrected by the following calibration procedure. First,

the time reference from VCDL is set based on the sampling frequency. Second, with a given time window for discharging in the MDAC, the gain error is measured from the INL (integral non-linearity) measurement of the two-step quantizer. Then this gain error is corrected with an external trimming of the discharging current to minimize the gain error. Although this gain mismatch is controlled with an external trimming of the discharging current in this prototype, a simple trimming block which traces the gain relation between the voltage and time domain in the background can be added to compensate for the PVT variation.

Fig. 3.19 shows the measured output spectrum of the 8b two-step quantizer as a standalone ADC at the 80MHz sampling rate and 500kHz input frequency with -0.1dBFS signal power. The measured SNDR is 66.8dB at an OSR of 8. The 20dB/decade slope of the quantization noise demonstrates the inherent first-order noise shaping of the proposed two-step quantizer. The measured output spectrum of the entire ΔΣ ADC for the same condition is shown in Fig. 3.20. The prototype ADC shows the second-order noise shaping for the quantization noise with a first-order loop filter and has a peak SNDR of 70.7dB while consuming 8.1mW from 1.2V supply. The SNDR of the prototype ADC with the loop filter shows less improvement than anticipated, compared to the case with an 8b quantizer alone. We believe that the transient noise from the discharging current source limits the noise performance of the entire ADC. This is because of the uni-directional discharging which uses PMOS and NMOS current sources as a single-ended configuration. This can be improved by employing the architecture with a better supply rejection such as supply regulated current source. Proper design correction/enhancement may improve SNDR by about 10dB, which is close to the thermal noise limitation of this ADC design. The measured dynamic range with different input amplitudes is shown in Fig. 3.21. Due to the high resolution quantizer of 8b, the proposed

ADC shows a fully stable operation up to -0.1dB of the full scale input. The calculated figure-of-merit (FOM) of this prototype ADC at 5MHz signal bandwidth is 280fJ/conversion-step. The measured SNDR at a 160MHz sampling rate (10MHz signal bandwidth) is 67.4dB, which is degraded due to the speed limitation of the residue amplifier in the MDAC during the residue generation. Table 3.1 summarizes the measured performance of the prototype ADC.

Table 3.1: Performance summary

Process	**0.13µm CMOS**	
Supply	**1.2V**	
Input	**2.4V_{P-P}**	
Fs	**80MHz**	**160MHz**
OSR	**8**	**8**
Signal BW	**5MHz**	**10MHz**
SNDR	**70.7dB**	**67.4dB**
Power	**8.1mW (Analog: 5.0mW, Digital: 3.1mW)**	**12.6mW (Analog: 5.7mW, Digital: 6.9mW)**
FOM*	**280 fJ/C-S**	**330 fJ/C-S**
Area	**0.37mm^2**	

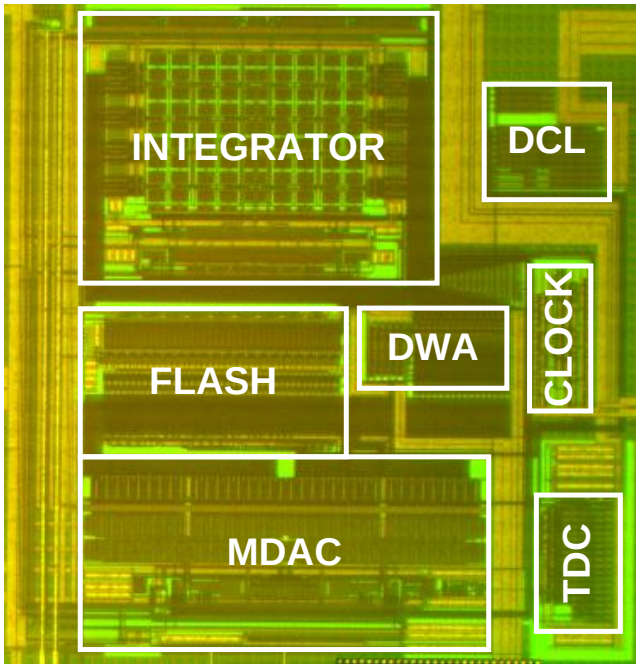

Figure 3.18: Prototype ADC in 0.13µm CMOS process (0.37mm^2=593µm by 616µm)

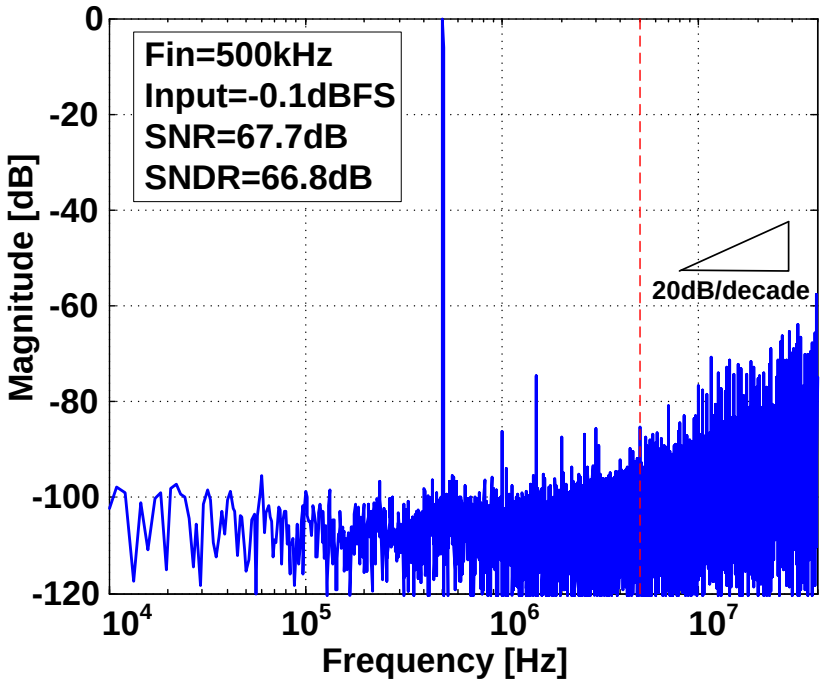

Figure 3.19: Measured output spectrum with 8b two-step quantizer alone

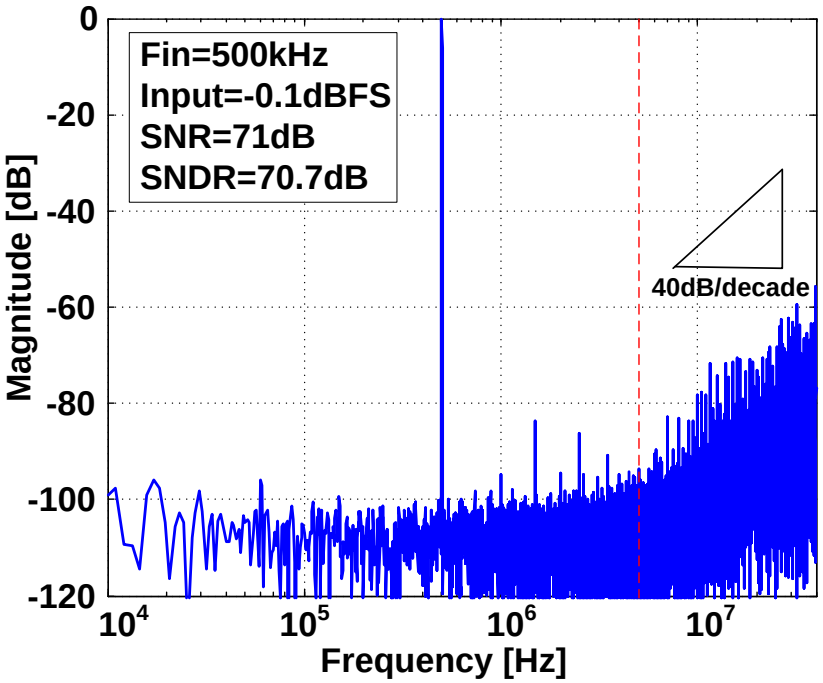

Figure 3.20: Measured output spectrum with entire ΔΣ ADC

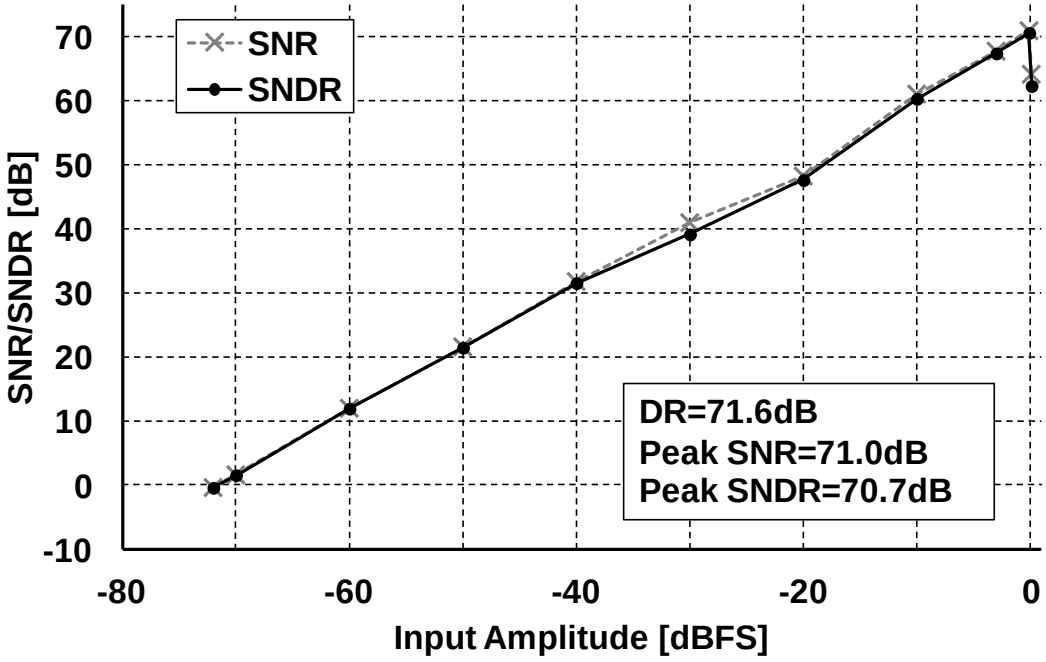

Figure 3.21: Measured dynamic range of the prototype ΔΣ ADC

CHAPTER 4. A TIME-BASED PIPELINED ADC

In addition to the previous research, based on the two-step integrating quantizer, another power efficient ADC architecture suitable for high resolution and wide input bandwidth which also use both voltage and time domain information will be introduced in this chapter.

4.1 Motivation

Although the delta-sigma ADC introduced in the previous chapter benefits from an extra order of noise shaping based on time based quantization, which results in low power consumption, the architecture still battles an inherent limitation. It is difficult to achieve wide signal bandwidth due to the oversampling nature. From this point of view, Nyquist conversion architecture should be considered, which may prove to be a more efficient path for wide signal bandwidths. Naturally, achieving higher resolution will become more challenging. As we introduced in chapter 1, both oversampling and Nyquist architecture are available to achieve our target resolution of interest (12b ENOB). In general, the possible Nyquist ADC architecture for such purposes is the pipelined or SAR architecture. Although SAR architecture shows good efficiency, it still needs power hungry residue amplifier to achieve high resolution, which is less power efficient. While there are many ways to increase the ADC resolution via calibration of linear errors, it is also not easy to correct nonlinear amplifier

errors. Furthermore, the nonlinearity error becomes worse with process scaling, due to the difficulty in maintaining a moderate signal swing at lower supply voltage.

One important advantage of the two-step quantizer in previous chapter is that it can be configured easily to work with a lower residue gain, which would provide a small signal swing. This is desirable for low power/voltage operation in the residue amplifier. Unlike the previous architecture which uses the quantization error in voltage domain for error feedback (to benefit from the extra order of noise-shaping in the oversampling system), in the Nyquist operation, it is required to quantize further for higher resolution. Without proper modification, this would require an expensive (power hungry) residue amplifier.

To continue to improve ADC performance and efficiency, the benefits of the two-step integrating quantizer which uses the voltage and time domain information will be further explored.

4.2 Utilizing time domain information for high resolution ADC

As explored in chapter 2, time domain quantization has drawn attention in recent deep submicron CMOS process as a good candidate for power efficient ADC architecture. To increase the resolution in time domain, the time amplifier is employed in [12]-[14]. However, these approaches need complex calibration to correct the time amplifier nonlinearity. Other approaches using a linear current source for time amplification in analog-to-digital conversion have been reported in [15], [35]-[37]. Although these ADCs show power-efficient conversion through time-domain signal processing without an expensive residue amplifier, they are

restricted in performance, offering either low frequency [15] or limited resolution [35]-[37]. The proposed architecture in this chapter demonstrates an efficient way to utilize time domain information as well as voltage domain information to achieve low power, high speed, and accuracy in analog-to-digital conversion.

4.2.1 Time domain amplification

Efficiently resolving bits and pipelining the quantization requires robust residue amplification in time domain. Fig. 4.1 shows one possible way to achieve such residue amplification similar to the time amplification [15]. Based on a simple charge pump, we may obtain time amplification with different slopes applied for charging and discharging. By measuring the discharging time for the zero-crossing utilizing a current source with different ratio, the input time can be amplified. In this example, the amplified output time with the gain of 4 is calculated based on the following equation.

$$T_{OUT} = \frac{4I}{I} T_{IN} = 4T_{IN} \tag{4.1}$$

Similar to the conventional pipelined ADC, this time-amplification scheme can be applied to process and pipeline the time-domain signal. Shown as in Fig. 4.2, the quantization error in time domain can be generated by taking the difference between input and DAC signal in time. The quantization error (residue) is amplified and used in the following stage as an input signal in time. With proper time amplification, further/continued quantization is possible in the time-domain pipelined stages to extract higher resolution.

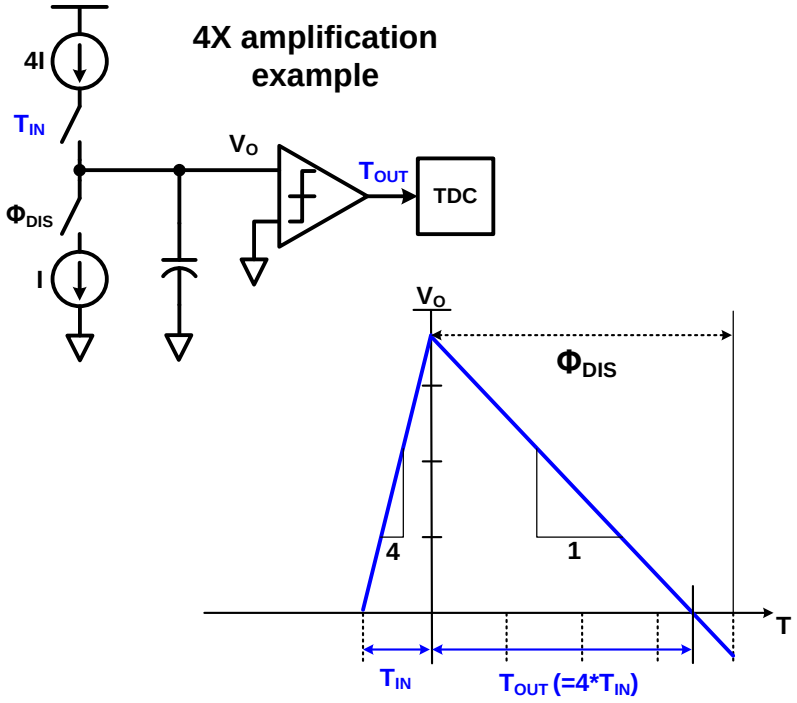

Figure 4.1: Example of the time amplification using charge pump

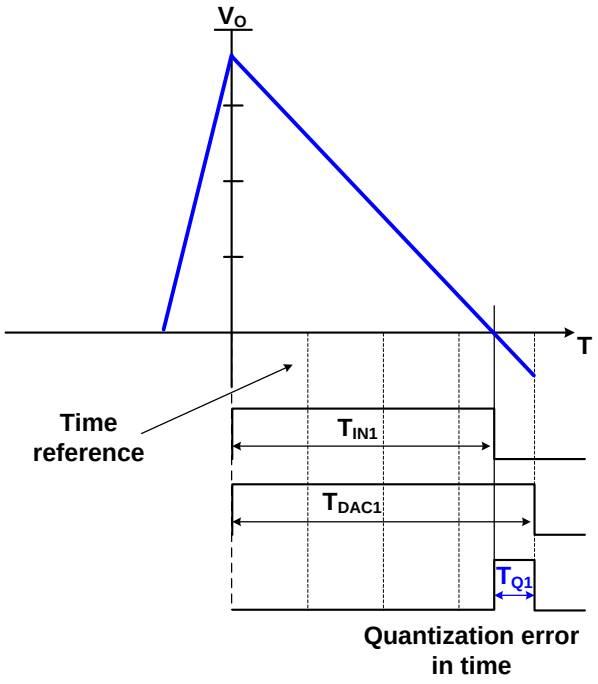

Figure 4.2: Time domain quantization

4.2.2 Time domain pipelining

Fig. 4.3 shows the example of a time domain pipeline stage for the pipelined TDC based on the time domain amplification. It consists of a sub-TDC for time domain quantization, a charge pump, a zero-crossing comparator, and other blocks for time residue generation. After the reset phase, the time input (T_{IN}) is quantized by the sub-TDC which generates the digital output and DAC pulse (T_{DAC}) for residue generation. As shown in Fig. 4.4, T_{DAC} is generated according to T_{IN} from the time reference (T_{REF}) after quantization. Then, the time residue (T_{DAC}-T_{IN}) is amplified by 4 with a different current ratio of 4:1 for charging and discharging in this example. After the zero-crossing comparison, the time output (T_{OUT}) is generated for further quantization in the next pipeline stage. With time residue amplification and its simple open loop configuration, further/continued quantization is possible as a pipelined TDC to extract higher resolution with relatively low power consumption.

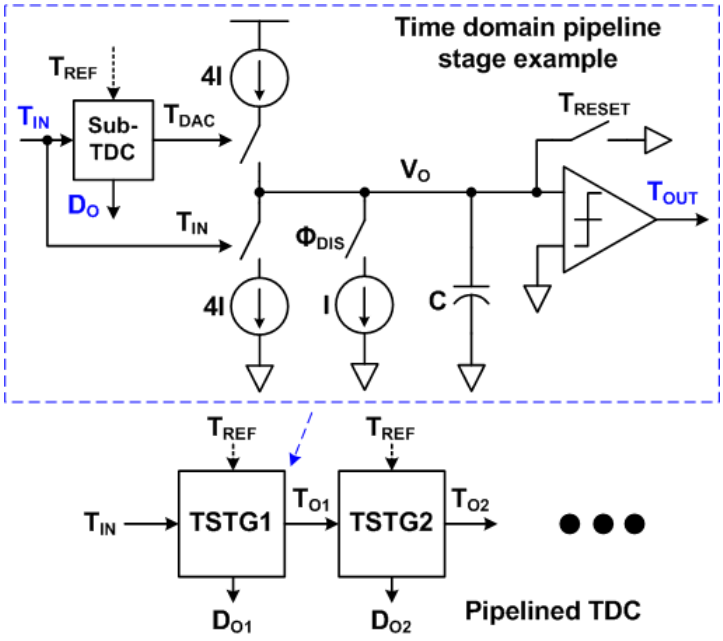

Figure 4.3: Pipelined TDC with time domain pipeline stage

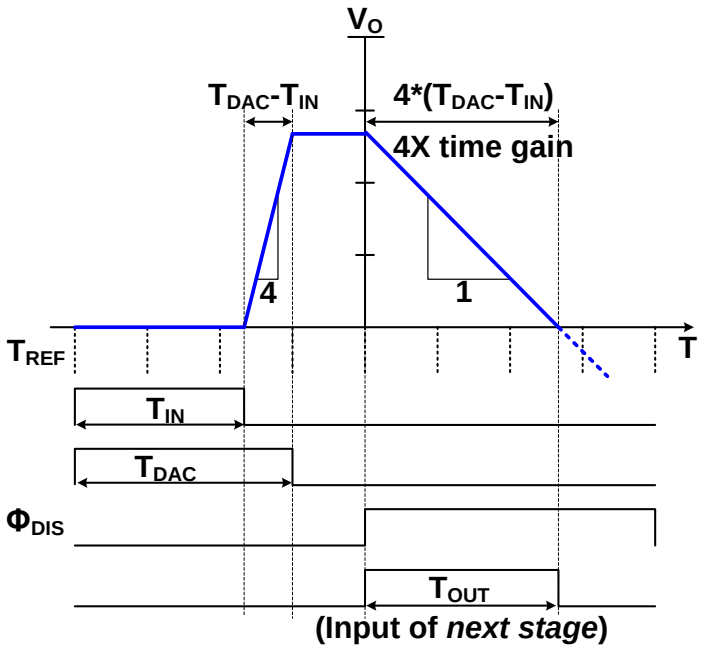

Figure 4.4: Time residue amplification and quantization of the time domain pipeline stage

4.3 Proposed pipelined ADC

In this section, we will show the proposed pipelined ADC using the time-domain amplification concept as a power efficient ADC architecture.

4.3.1 ADC architecture

Shown in Fig. 4.5 is the proposed time-based pipelined ADC. It consists of a conventional 4b MDAC and FLASH in voltage domain, a zero-crossing comparator for V-T conversion, four time-based pipeline stages (TSTGs) and a final 2.5b TDC for backend pipelined stage, and other supporting blocks. With a 1b redundancy between the pipeline stages, the ADC generates the final 14b digital output after the conversion. V-T trimming block which provides coarse current reference to MDAC and TSTGs traces the relation between the voltage and

time domain gain. V-T gain is also tuned externally in analog domain and the finite gain error in each stage is corrected by a simple off-chip radix calibration in digital domain. For sub-TDCs time reference, a voltage controlled delay line is employed.

The main features of the proposed ADC as follows. First, a high resolution and wide signal bandwidth can be attained with the pipelined Nyquist ADC architecture. Second, a power-efficient and simplest amplifier can be used for linear V-T conversion in the first stage based on the proposed V-T conversion which will be explained in the following section. Third, a simple charge pump based pipelined architecture is employed for low power consumption. Finally, the accuracy requirement of the backend pipelined TDC in time domain is relaxed by the resolution of the first stage in voltage domain which is easier to achieve high accuracy than the time domain in general. As a result, it is able to take advantage of the unique benefits of utilizing both the voltage and the time domains, by processing MSBs in voltage domain and LSBs in time domain.

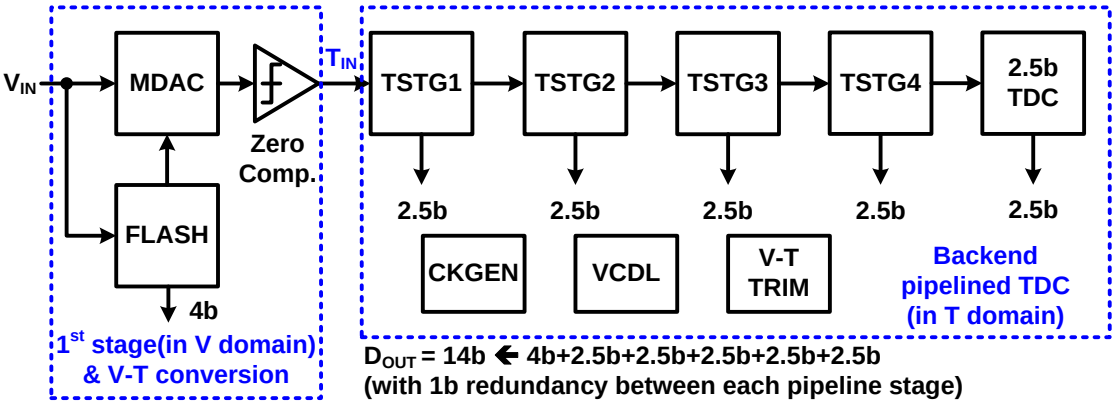

Figure 4.5: Proposed time based pipelined ADC

4.3.2 V-T conversion

To process the signal in time, the initial input to the first stage of ADC in voltage domain should be converted to time domain. In a conventional V-T conversion using charge integration method as in dual-slope ADC shown in Fig. 4.6, an amplifier with high gain is typically required to provide an accurate virtual ground for charging reference for high accuracy of the time domain output [38].

In a conventional V-T conversion using the two-step quantizer shown in Fig. 4.7, the sampling capacitor C_S is disconnected from the virtual ground to sample the next input signal for two-phase operation [16]. Because only the transferred residue charge on the feedback capacitor C_F is used to measure the discharging time for zero-crossing, the accuracy of the charge transfer affects this V-T conversion process. The residue output in voltage domain after the amplification phase is

$$V_O = \frac{C_S}{C_F}(V_{IN} - V_R) \cdot \frac{A\beta}{1 + A\beta} - \frac{I_{DIS} \cdot T_O}{C_F} \tag{4.2}$$

where A is the open loop dc gain of the amplifier and β is the feedback factor. Then, the time domain output at zero-crossing in discharging phase is

$$T_O = \frac{C_S}{I_{DIS}}(V_{IN} - V_R) \cdot \frac{A\beta}{1 + A\beta} . \tag{4.3}$$

Therefore, any nonlinear error from the amplifier directly affects the time domain output in this V-T conversion. As a result, we need a high gain/linear amplifier also in this V-T conversion.

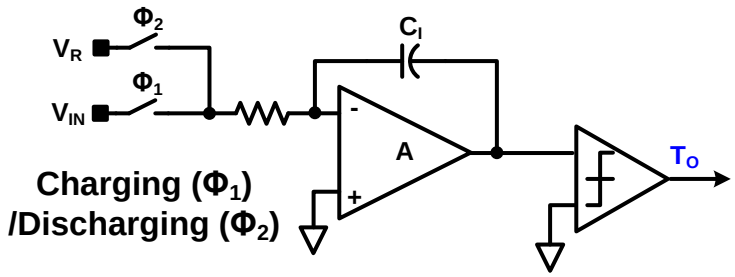

Figure 4.6: Conventional V-T conversion (Dual-slope ADC)

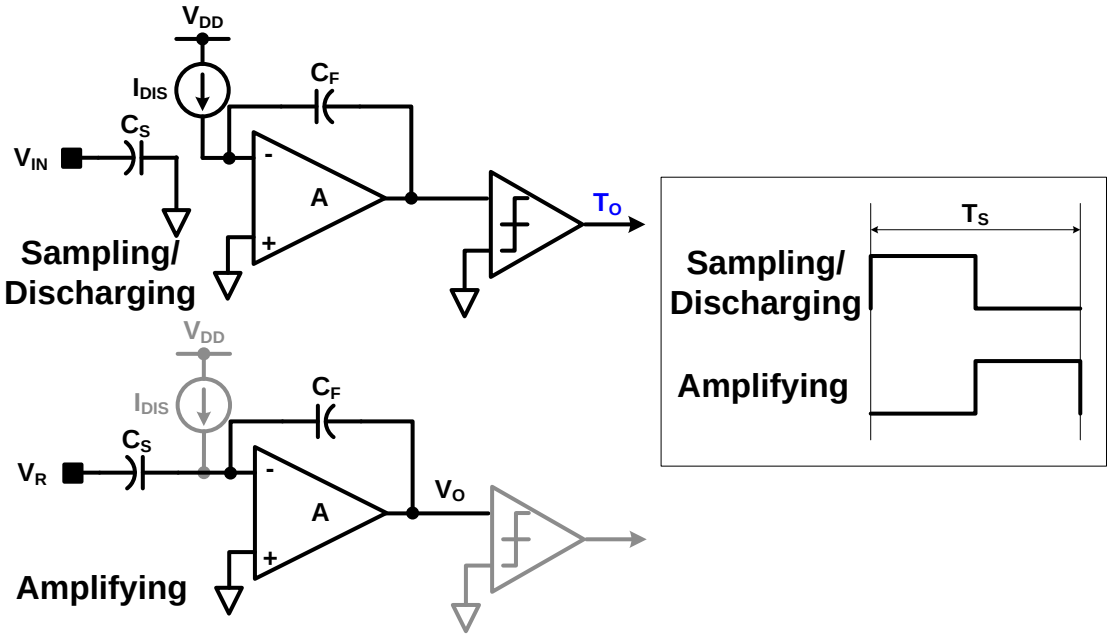

Figure 4.7: Conventional V-T conversion (Noise-shaped two-step integration quantizer)

Fig. 4.8 shows the proposed V-T conversion which alleviates the stringent amplifier requirements on gain and linearity. In the proposed solution, which operates in three phases, the charge stored in both sampling and feedback capacitors is discharged together. Because there is no charge loss on both capacitors and discharged together to measure the time for zero-crossing, the time-domain output at zero-crossing is always linear regardless of the amplifier non-idealities, as long as the current source is linear [39]. The residue output after the amplification phase in this case is derived as the following equation.

$$V_O = \left[\frac{C_S}{C_F}(V_{IN} - V_R) - \frac{I_{DIS} \cdot T_O}{C_F} \right] \cdot \frac{A\beta}{1 + A\beta} \tag{4.4}$$

As you can see, the residue output in voltage domain is affected by the amplifier characteristic even in this amplification. However the time domain output at zero-crossing in discharging phase is

$$T_O = \frac{C_S}{I_{DIS}}(V_{IN} - V_R). \tag{4.5}$$

Now, the output T_O is always linear regardless of the characteristic of the amplifier in the proposed V-T conversion. Another intuition to understand this linearity is that the zero-crossing on the amplifier output is always detected at the same voltage (for the differential zero), which means that there is no signal dependency in time domain output at zero-crossing moment. Therefore, a low gain/linearity amplifier can be allowed in the proposed V-T

conversion. The bandwidth of the amplifier only affects the time delay during discharging, which is mostly signal independent. Although it should operate in three phases, the time for amplification can be minimized because we don't need full settling of the residue output in voltage domain. In the linearity simulation shown in Fig. 4.9, the time output after the discharging phase shows a superior linearity compared to the voltage output of the amplifier after amplification (prior to discharging) with a simple common source amplifier which has an open loop dc gain of just 24dB.

This simple method for V-T conversion provides significant advantages as follows. First, the output swing of the amplifier (input swing of comparator) can be maximized, which makes it easy to design the zero-crossing comparator for low power. This provides strong advantage especially in recent CMOS process with low supply voltage. Second, a cheap (small and low power) amplifier with very low gain could be employed for V-T conversion. Even though the amplifier sees a reduced feedback factor in this case and less time for settling because of three-phase operation (needs more bandwidth), it benefits from a significant net improvement from being able to use much simpler amplifier architecture. Also the power saving of the residue amplifier is significant if this V-T conversion is employed in the first pipeline stage, because the first stage amplifier in the pipelined ADC is most power hungry block.

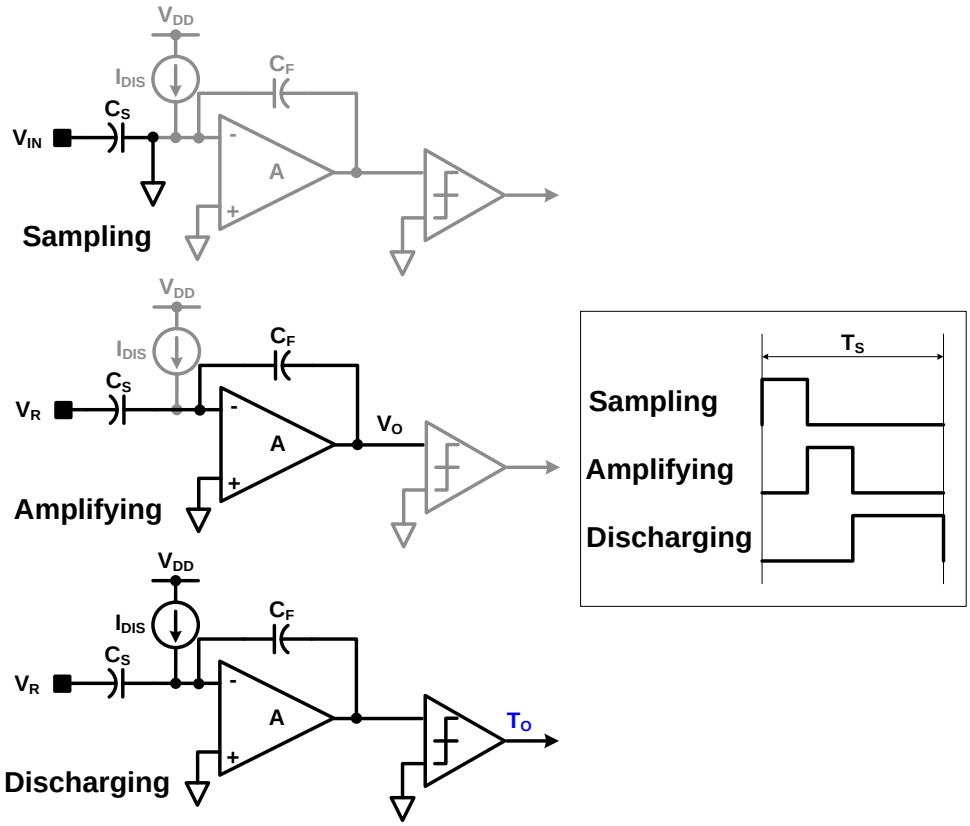

Figure 4.8: Proposed V-T conversion (Three phase operation)

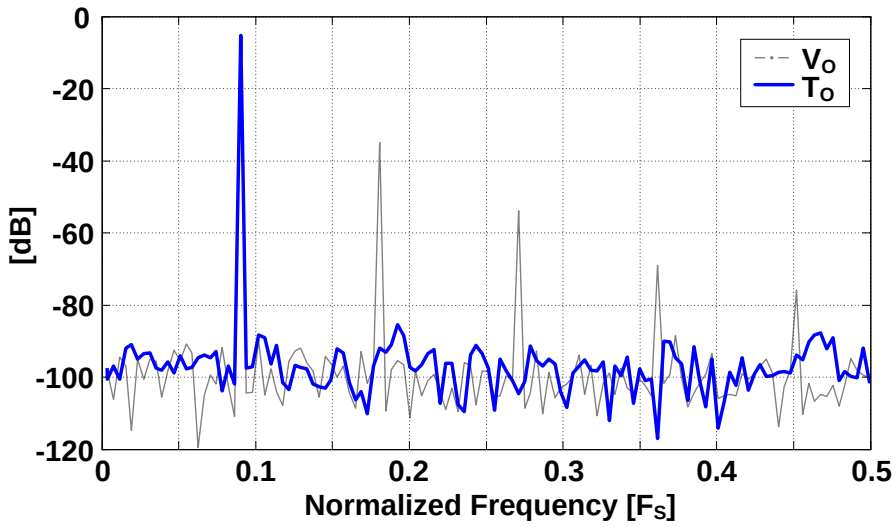

Figure 4.9: Linearity simulation of the proposed V-T conversion using a residue amplifier with 24dB open loop dc gain (Voltage domain output in gray and time domain output in blue)

4.3.3 Hybrid time domain stage

Even though the pipelined TDC based on the time domain pipeline stage in section 4.2 can possibly provide low power consumption, it also has many major error sources such as the nonlinearity of the current source, the noise of the comparator, and the jitter of the time reference. Although, other error sources can be treated as design trade-offs, the jitter of the time reference will directly limit the pipelined TDC performance for high SNR. For example, the linearity of the DAC pulse in the time-domain quantization is critical in achieving high accuracy, similar to DAC linearity in a conventional pipelined ADC, because the linearity of DAC directly affects the TDC linearity.

Fig. 4.10 shows two possible methods to generate the time reference. Either a high frequency clock from an oscillator or a delay line from DLL is typically employed as a time reference. However both methods require high accuracy, which adds to complexity. In general, the high frequency clock generation suffers from the clock jitter and can consume a large amount of power. In order to achieve N-bit SNR, the required jitter tolerance in the time reference is less than $1T_{LSB}$ of the N-bit TDC resolution, which is not easy to achieve in high resolution cases with fine time reference [40]. Also DLL has a limited linearity due to its delay cell mismatch [41]. Even though the jitter induced error or nonlinearity from the time reference can be calibrated, it requires complex calibration algorithm and extra power consumption [42].

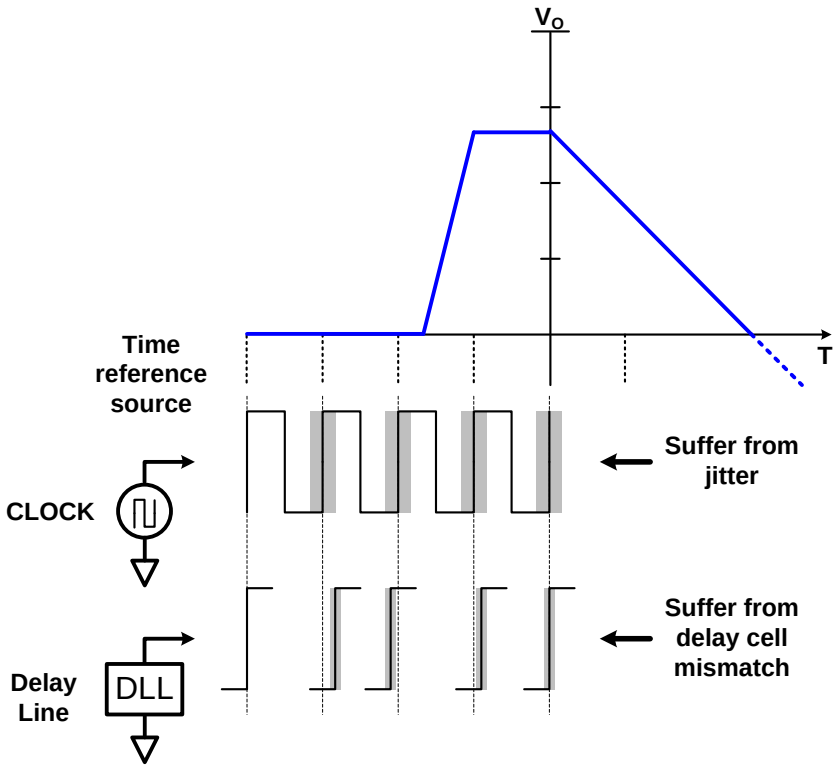

Figure 4.10: Problem in time reference generation

To solve the problem efficiently, we propose a hybrid time-domain quantization stage as shown in Fig. 4.11. The proposed hybrid stage employs a capacitive DAC for charge subtraction instead of using a DAC pulse. The linearity of DAC now only depends on capacitor matching, which is not difficult to achieve. Time-domain error sources such as jitter or delay mismatch now only affect the linearity of TDC quantizer and it is relaxed with the given redundancy between stages. With a conventional error correction scheme which usually is employed to correct comparator error in a pipelined ADC, the time reference error up to ½ LSB can be corrected by the 1b redundancy between the pipeline stages [28]. Fig. 4.12 illustrates the operation of the proposed stage. Initially, all capacitors are reset to the positive

reference. In charging phase, capacitors are charged by a fixed current (4I) based on the time input. At the same time, sub-TDC quantizes the time input and generates a corresponding thermometer code for the DAC operation, sequentially. In next phase, the stored charge on the capacitors (which represents the residue) is discharged by a different current ratio (I) for residue amplification. After the zero-crossing, the amplified time residue output is passed on to the next pipelined stage.

The comparison of two different time amplification methods is shown in Fig. 4.13. In case of the amplification using a dual slope (charging and discharging), the linear current source is required and the residue gain is not well defined due to the different type of current source (PMOS and NMOS type) for the amplification. However in a single slope case (using two charging slopes) similar to [15], the same type of current source is used for amplification. Now, the residue gain only depends on the matching of the same type of current source which is well defined with a careful layout. In this case, the linearity of the current source can be maximized with a proper common mode control. Although twice the capacitors are required in the single slope case, it provides many advantages in real implementation which use a low supply voltage. In case of the amplification using a dual slope, it is difficult to get a required signal swing with high linearity, which results in an increased capacitance for the same SNR with a smaller signal swing. Therefore the amplification method using a single slope is employed in this work.

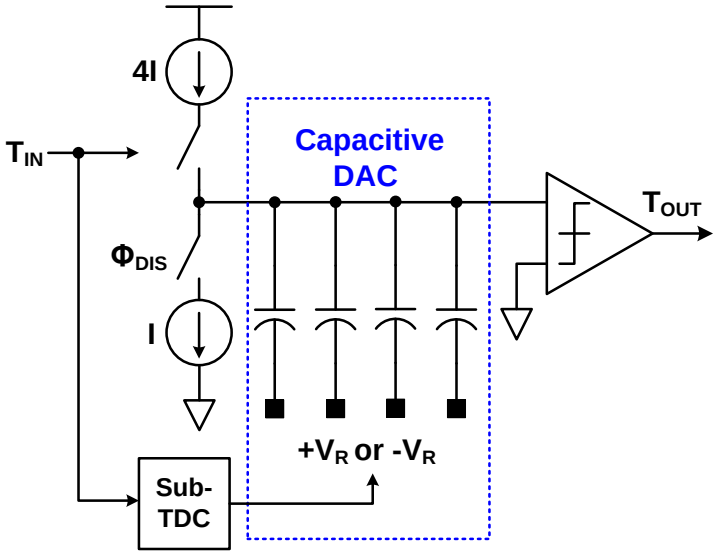

Figure 4.11: Proposed hybrid time domain stage

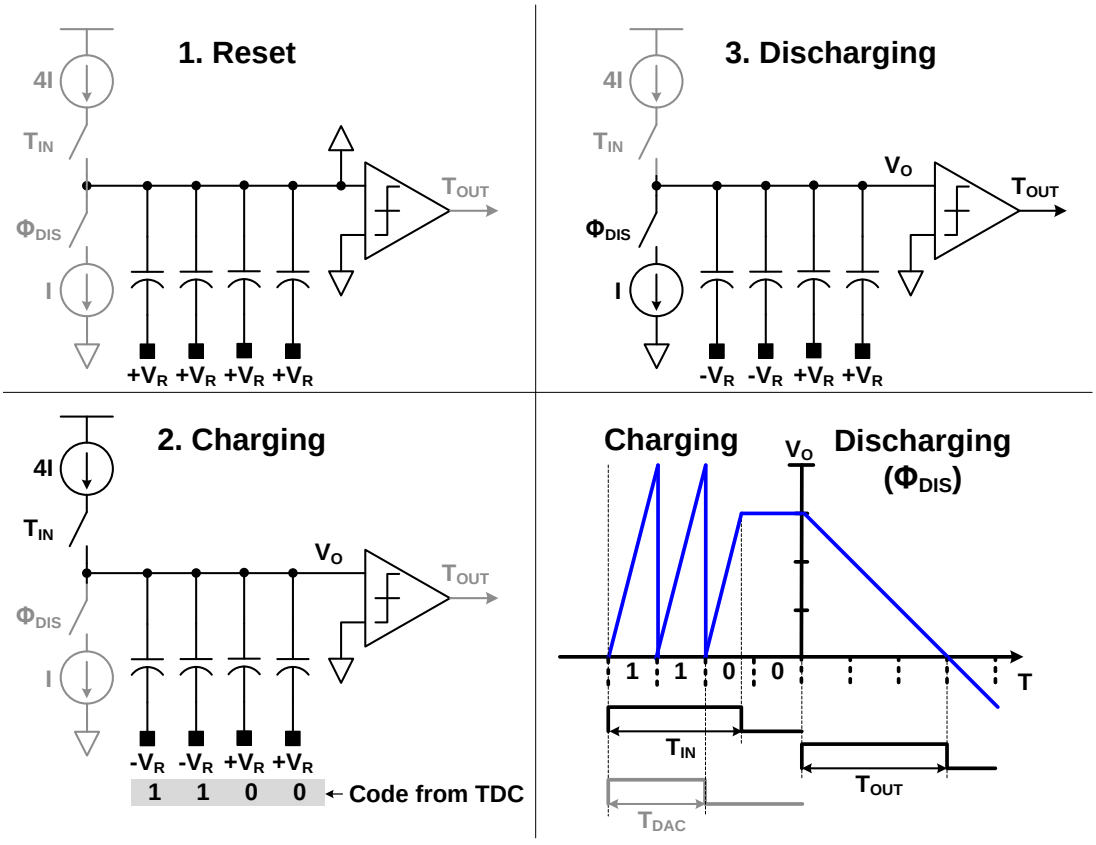

Figure 4.12: Operation of the proposed hybrid time domain stage

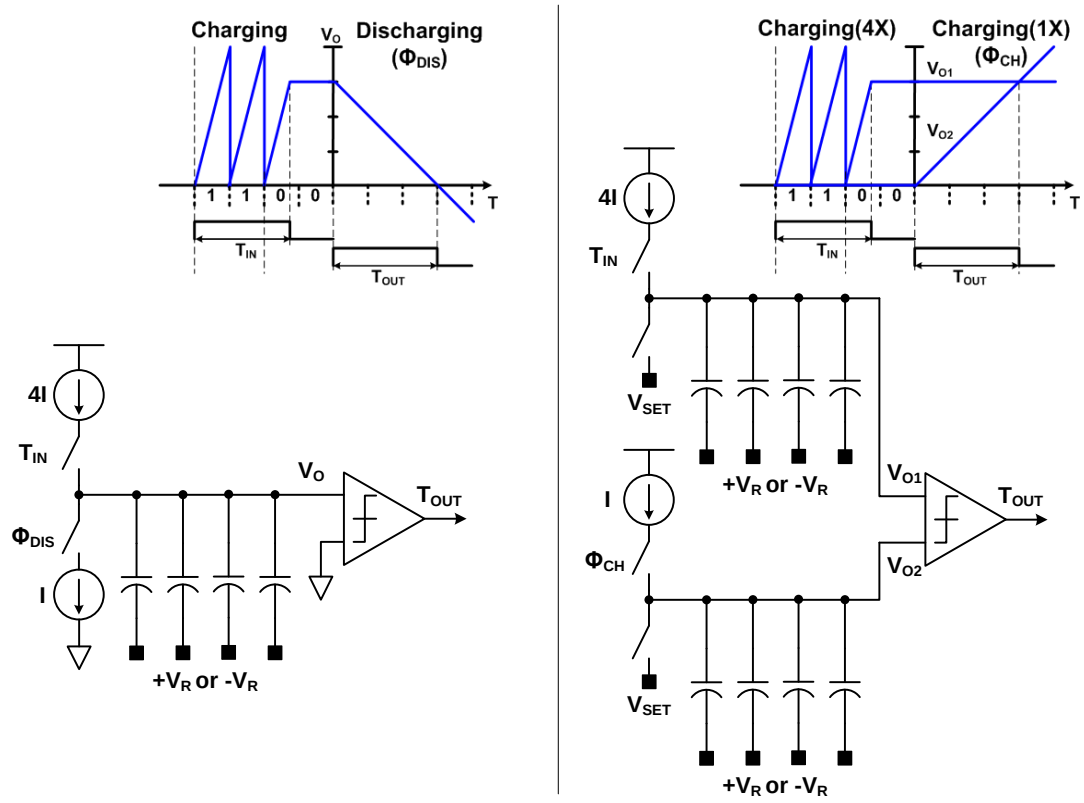

Figure 4.13: Comparison of two different implementation of the time amplification with dual slope (charging and discharging) and single slope (two charging)

4.4 Circuit implementation

4.4.1 Multiplying Digital-to-Analog Converter (MDAC)

Fig. 4.14 shows the first stage MDAC in the proposed ADC. The proposed MDAC is similar to the conventional MDAC except the additional blocks for discharging and V-T conversion. It consists of capacitors and switches for sampling and DAC operation, a residue amplifier, a discharging current source, and a zero-crossing comparator. Similar to the MDAC in the two-step quantizer in the previous chapter the number of sampling capacitor for DAC operation is reduced by half based on the merged capacitor switching technique (8 capacitors

for 4b operation) [33]. Note that there is an additional path providing a fixed offset up to half of MDAC output swing, which guarantees that the MDAC output is always larger than zero for the uni-directional discharging

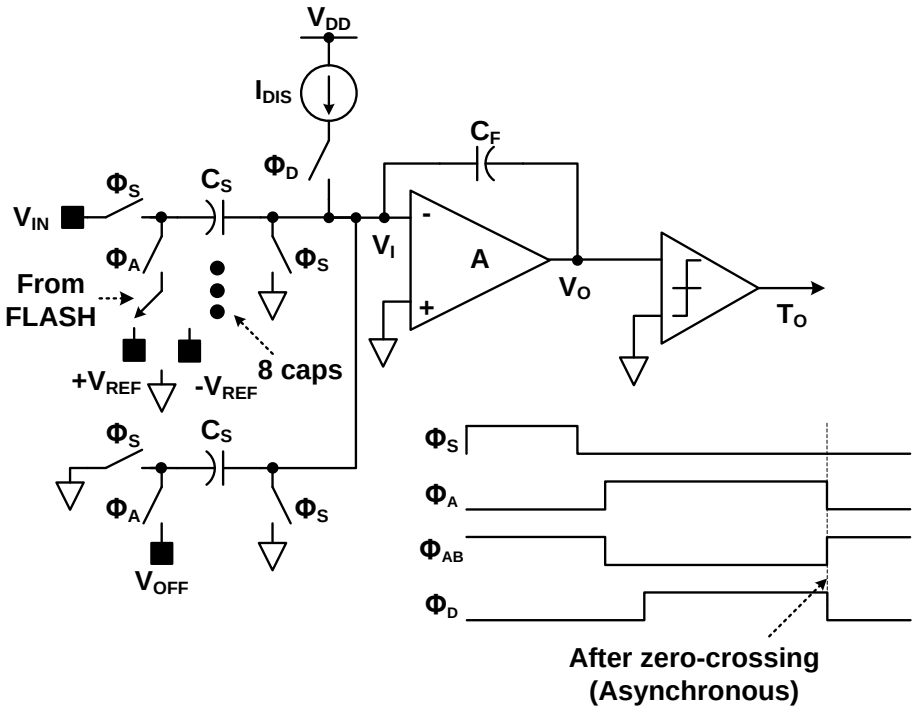

Figure 4.14: Multiplying digital-to-analog converter (MDAC) incorporating the proposed V-T conversion based on low gain of 24dB switched residue amplifier

One main feature of the proposed ADC is the alleviated amplifier requirement with the proposed V-T conversion in the first stage (MDAC). As we explained in section 4.3.2, the simple switched amplifier which has only 24dB DC gain is employed as shown in Fig. 4.15. The proposed amplifier only operates in amplifying/discharging phase based on switched operation for low power consumption. Also, it drives small load capacitance (zero-crossing comparator) in the proposed architecture. Because the first stage residue amplifier is the most power consuming block in conventional pipelined architecture, this simple amplifier structure

incorporating small load capacitance reduces ADC power consumption significantly. The power consumption of the amplifier is further reduced by turning it off asynchronously after zero-crossing.

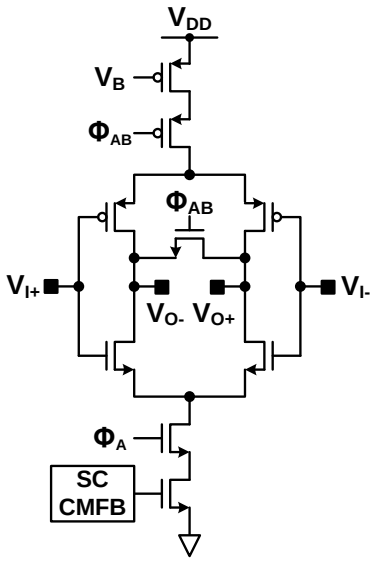

Figure 4.15: Switched residue amplifier with a dc gain of 24dB in MDAC

4.4.2 Time domain pipeline stage (TSTG)

Fig. 4.16 shows the implemented hybrid time-domain stage which adopts a pseudo differential configuration for better supply noise immunity. It consists of capacitors and switches for charging and DAC operation, current sources for two charging slopes, sub-TDC with 2.5b, and a zero-crossing comparator. Note that the comparator with 4 inputs is employed for a pseudo differential operation of the time amplification. The common mode levels of current sources and comparator input are controlled separately using the coupling capacitor, C_C, to maximize the linearity of current source. Therefore, the current variation during the capacitive DAC operation is minimized in this implementation. Because the parasitic

capacitance on the output node of the current source and on the input node of comparator is signal dependent, the linearity of the proposed stage is mainly limited by these parasitic capacitances. However as explained in section 4.2.3 the accuracy requirement of this TDC stage is relaxed by the resolution of the first stage in voltage domain in the proposed ADC.

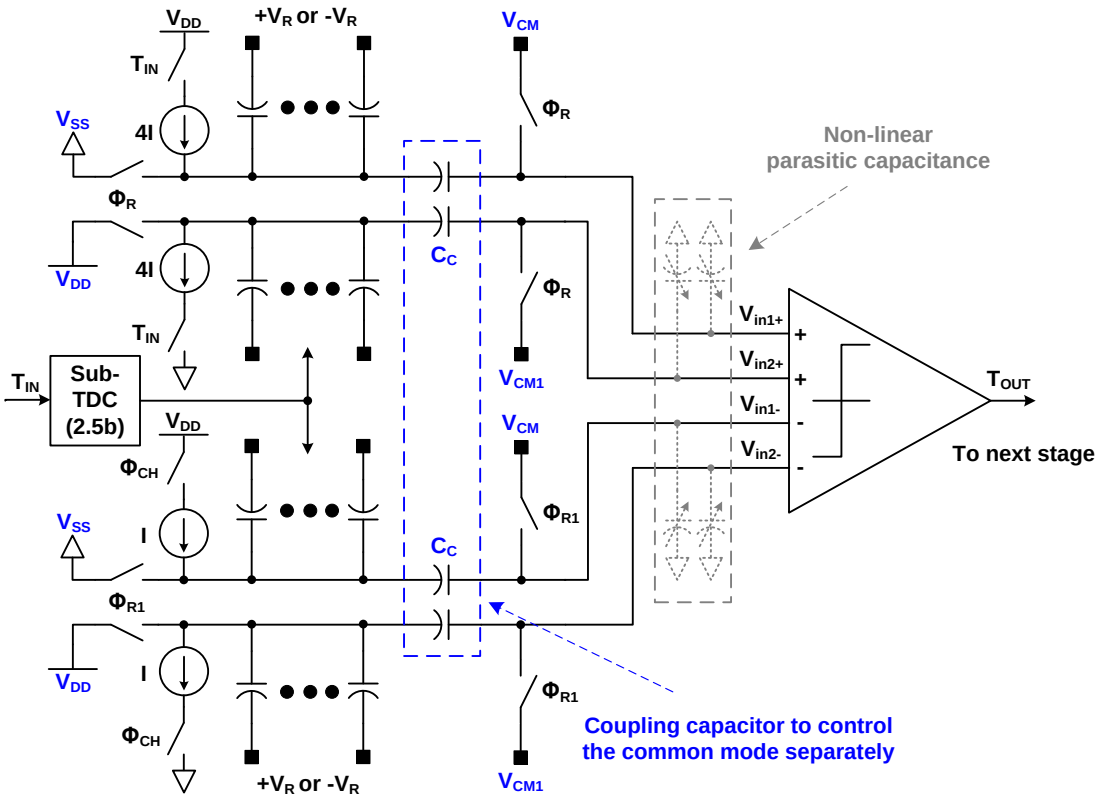

Figure 4.16: Implementation of the time domain pipeline stage (TSTG)

4.4.3 Switched charge pump in TSTG

The detailed schematic of the charge pump in TSTG is illustrated in Fig. 4.17. The time residue gain is simply defined by the device ratio of two PMOS transistors in current source. In the proposed charge pump, the dedicated reset phase, Φ_{R1} and Φ_{R2}, allows the current

source to be settled to the bias point from the turned-off condition before the actual charging. The current source is switched off completely after the charging to reduce power consumption. Therefore, the only charge during the two charging phase is used for the operation without any static charge from charge pump. The power consumption is reduced further by switching off asynchronously after zero-crossing.

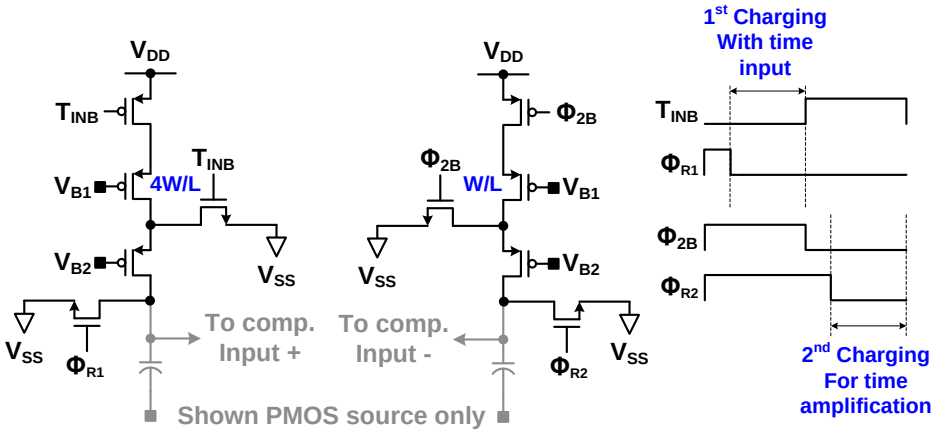

Figure 4.17: Switched charge pump (Shown PMOS current source only for simplicity)

4.4.4 Switched zero-crossing comparator in TSTG

Fig. 4.18 shows the proposed zero-crossing comparator employed in TSTG. Similar to the case in charge pump, the comparator is completely turned off asynchronously after zero-crossing detection to reduce power consumption. In the proposed time domain pipeline stage, the linearity is limited by the signal dependant parasitic capacitance on the comparator input node. During the 1st charging phase, the comparator is turned-off because the comparator is not used for comparison. However any voltage change on the floating node from the turned-off transistor causes the parasitic capacitance change, which results in the nonlinear error

during the charging operation. This problem is solved by adopting the additional switched in dotted box from Fig. 4.18 which makes the input parasitic capacitance constant.

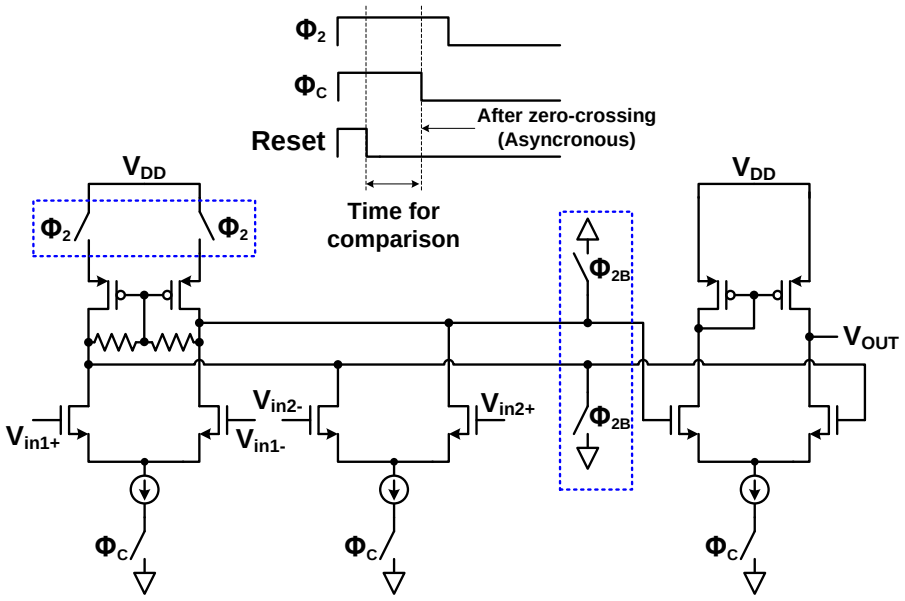

Figure 4.18: Switched zero-crossing comparator

4.4.5 V-T gain trimming circuit

In the proposed ADC, the effective voltage-to-time conversion gain depends on the capacitance and current value with a given voltage reference and time reference for discharging. However these values are not well defined in real implementation. The V-T trimming circuit shown in Fig. 4.19 provides a coarse current reference for MDAC and TSTGs. With a same voltage and time reference, the trimming circuit traces the correct current value for discharging for a replica capacitor used in MDAC and TSTG1. However due to the matching accuracy of this replica path, the V-T gain is also tuned externally in analog domain

and the finite gain error after the tuning in analog domain is corrected by a simple off-chip radix calibration in digital domain.

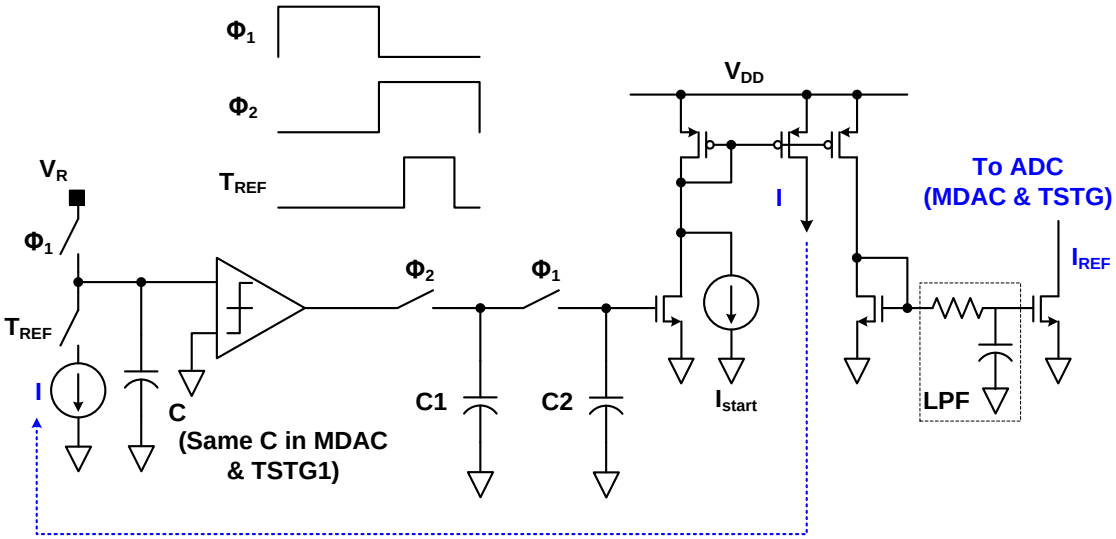

Figure 4.19: V-T gain trimming circuit

4.5 Consideration of non-idealities

In this chapter, we will review about the two main non-idealities, noise from discharging current source and time delay from zero-crossing comparator, in the proposed time based ADC which limits the performance.

4.5.1 Noise

In the proposed ADC, the integrated noise from the current source in first stage MDAC dominates the noise performance, which is directly related to the ADC resolution. Fig. 4.20 shows the noise model to analyze the noise performance of MDAC. If we assume the bandwidth of the amplifier is much higher than the switching time for discharging (W_u >>

1/T_D), the voltage accumulated on feedback capacitor C_F is derived as follows, where the power spectral density (PSD) of the current source I_{DIS} is $4kT\gamma g_m$.

$$\overline{V_{on}^{\,2}} = \frac{1}{C_F^{\,2}} \int_0^{T_D} \overline{I_{DIS}^{\,2}}\, dt = \frac{\overline{I_{DIS}^{\,2}}}{C_F^{\,2}} T_D \tag{4.7}$$

If we assume a random walk process of the integrated noise on the capacitor [34], the output noise is

$$\overline{V_{on}^{\,2}} = \frac{2kT\gamma g_m}{C_F^{\,2}} T_D. \tag{4.8}$$

Therefore, the equivalent input-referred noise is derived as following equation by dividing the signal gain.

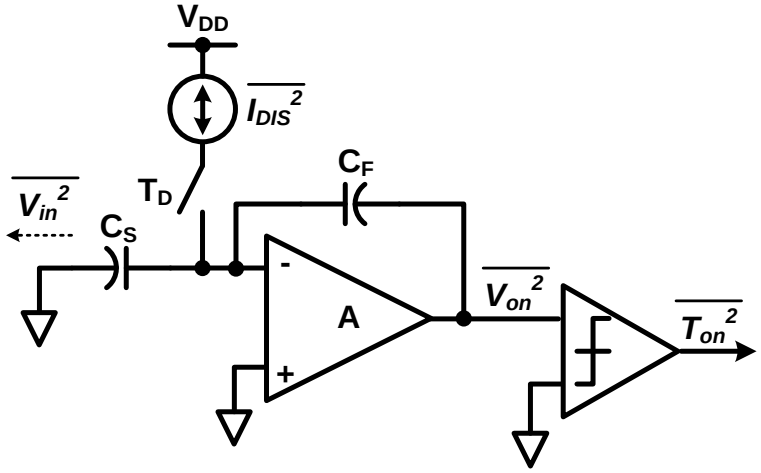

Figure 4.20: Integrated noise model for the current source in MDAC

$$\overline{V_{in}^{\,2}} = \overline{V_{on}^{\,2}} \cdot \left(\frac{C_F}{C_S}\right)^2 = \frac{2kT\gamma g_m}{C_S^{\,2}} T_D \tag{4.9}$$

In equation (4.9), the current value for the discharging in a given time window is fixed based on the ADC reference voltage and sampling capacitance ($I_{DIS} \cdot T_D = C_F \cdot V_{REF}$), the input-referred noise can be derived as follows.

$$\overline{V_{in}^{\,2}} = \frac{2kT\gamma g_m}{C_S^{\,2}} T_D = \frac{2kT\gamma g_m}{C_S^{\,2}} \cdot \frac{C_F V_{REF}}{I_{DIS}} \tag{4.10}$$

Because the ratio between C_S and C_F is the residue gain of the MDAC, this equation can be re-formulated as follows.

$$\overline{V_{in}^{\,2}} = \frac{2kT\gamma}{C_S} \cdot \frac{1}{G} \cdot \frac{2V_{REF}}{V_{eff}} \tag{4.11}$$

where g_m is $2I_{DIS}/V_{eff}$, G is the residue gain, and V_{eff} is the effective voltage of the current source. As you can see, the input referred noise from current source is affected by the sampling capacitance, the residue gain, and the ratio between the ADC reference range (or signal range) and the effective voltage of the current source. With a given signal range, this noise can be minimized with a maximized effective voltage of the current source under a given supply voltage. Also we can reduce this noise by increasing the residue gain (by resolving more bits from the first stage). Even though the proposed ADC requires a larger sampling capacitance than the conventional pipelined ADC for the same SNR performance due to this additional noise from the discharging current source, the benefits of the proposed

architecture in terms of the power consumption and linearity in real implementation are significant especially under the condition with low supply voltage.

4.5.2 Delay from zero-crossing comparator

The dynamic range of the proposed time domain stage is mainly limited by the delay from zero-crossing comparator. Fig 4.21(a) shows the residue plot of TSTG with 2.5b resolution. The error correction range with 1b redundancy is $T_{REF}/4$ in ideal case. However, the error correction range in the case with a comparator delay (in red curve in Fig 4.21) is reduced due to the delay. If this delay is longer than $T_{REF}/4$, the residue output will saturate the next stage, which is problematic. Therefore the delay should be minimized compared to the time reference. Fig 4.21(b) compares the two residue plots with and without delay correction. The delay can be corrected by subtracting the same amount of delay in time reference as a time offset as shown in blue curve in Fig. 4.21(b). By shifting the decision point of the sub-TDC, the time residue output can be located in the nominal range which allows the error correction as the ideal case.

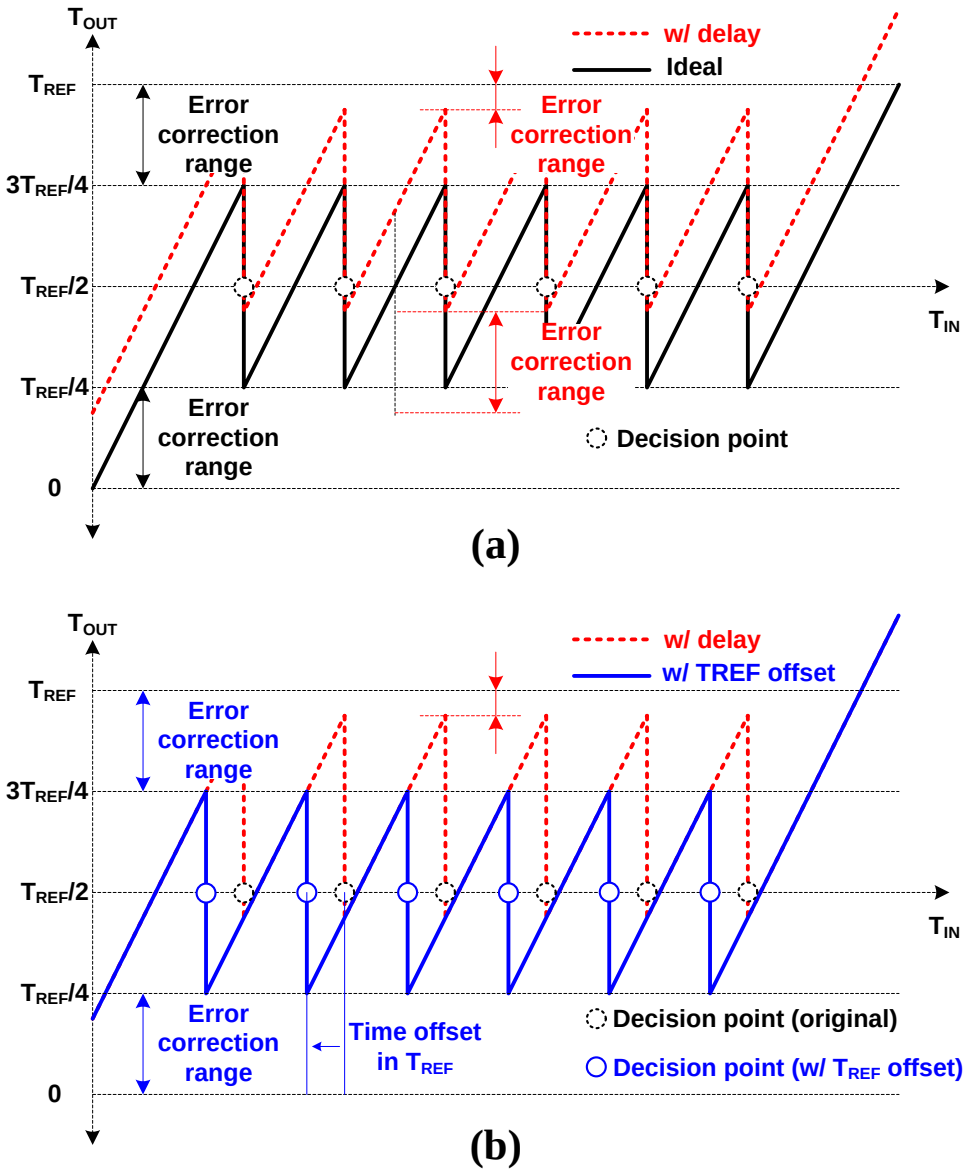

Figure 4.21: Residue plot of TSTG (a) with comparator delay and (b) with delay correction by injecting time offset in time reference

4.6 Measurement results

The prototype ADC was implemented in a 0.13μm CMOS process. Fig. 4.22 shows the die photograph of the fabricated prototype [43]. The active area is $0.5mm^2$ (1095μm by 460μm). Fig. 4.23 shows the measured DNL and INL graph. The measured DNL and INL at 11b level are +/- 0.78 LSB and +/- 0.79 LSB, respectively. Fig. 4.24 shows the measured output spectrum at the 70MS/s sampling rate and 1MHz input frequency. The measured SNDR and SFDR are 69.3dB and 80.6dB, respectively, while consuming 6.38mW under 1.3V supply. Due to the proposed V-T conversion in the first stage of the pipelined ADC, the input range is maximized up to near rail-to-rain of $2.4V_{p-p}$ for the maximum SNR performance while achieving high linearity of more than 80dB SFDR at the same time. The measured output spectrum with 20MHz input frequency is shown in Fig. 4.25. The measured SNDR and SFDR are 65.2dB and 75.9dB, respectively. Note that the output data of the ADC is downsampled by a factor of 4 for test purpose in Fig 4.24 and 4.25. The measured SNDR versus different input frequencies is shown in Fig. 4.26. The measured dynamic range with 1MHz input signal is shown in Fig. 4.27, which is 72.6dB with a -0.1dB of the full scale input. The calculated peak FOM with a 1MHz input frequency is 38.2fJ/conversion-step. Table 4.1 summarizes the measured performance of the prototype ADC.

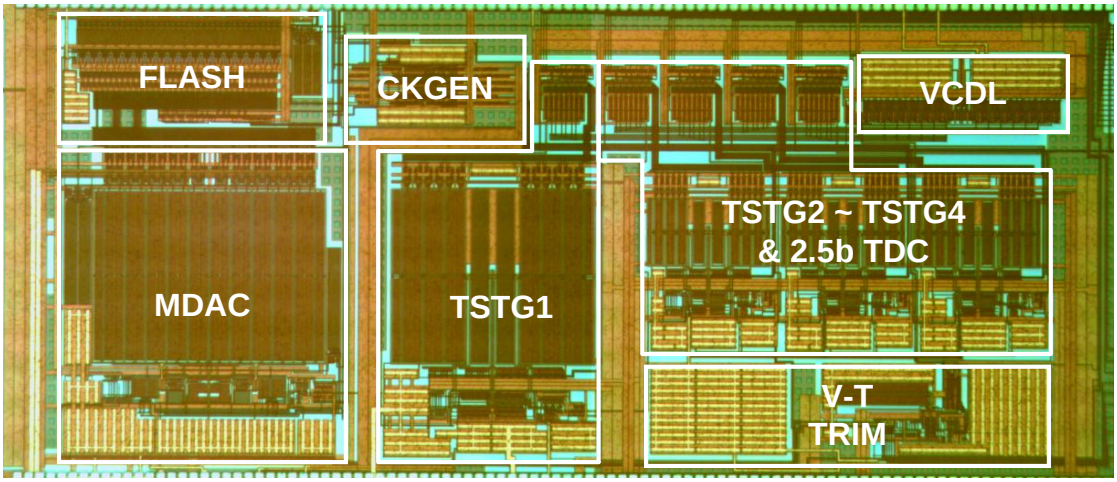

Figure 4.22: Chip photo of the prototype ADC in 0.13µm CMOS

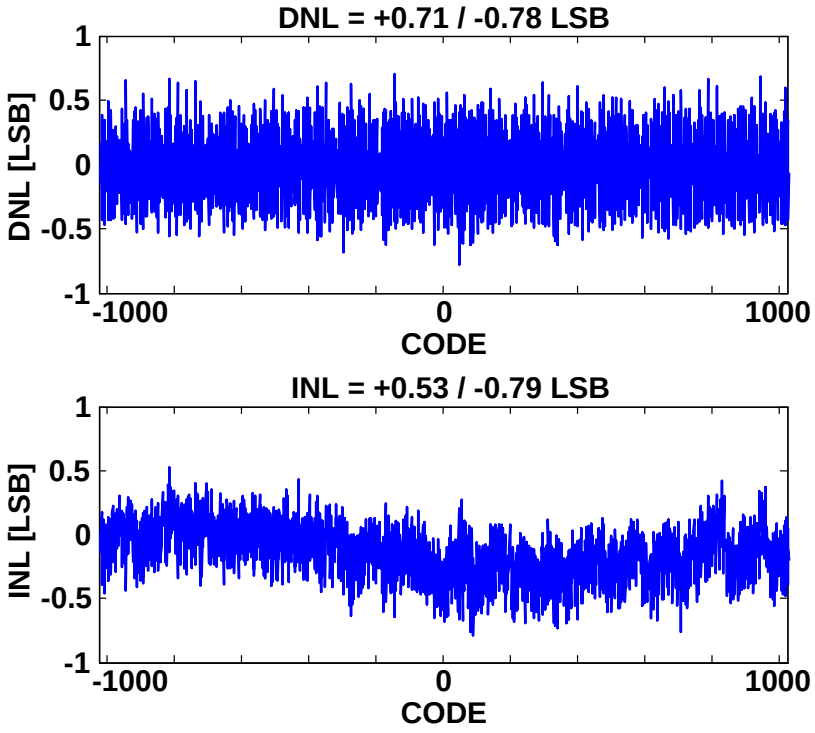

Figure 4.23: Measured DNL and INL

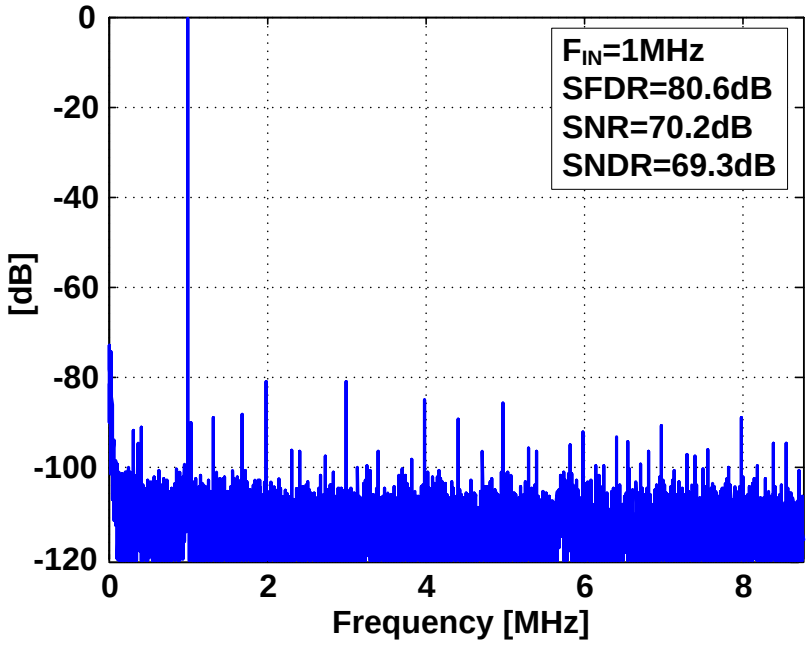

Figure 4.24: Measured output spectrum (@F_{IN}=1MHz, downsampled by a factor of 4)

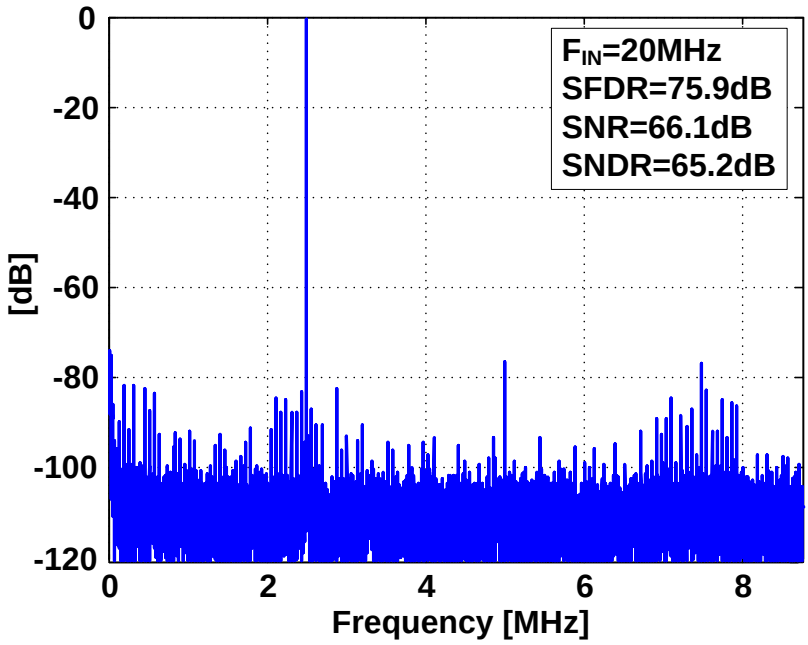

Figure 4.25: Measured output spectrum (@F_{IN}=20MHz, downsampled by a factor of 4)

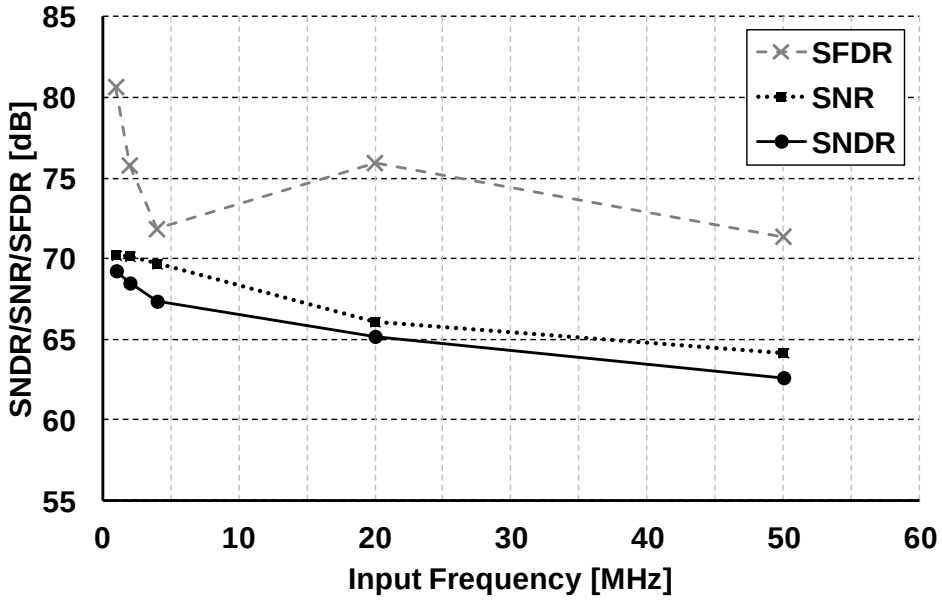

Figure 4.26: Measured SNDR vs. input frequency

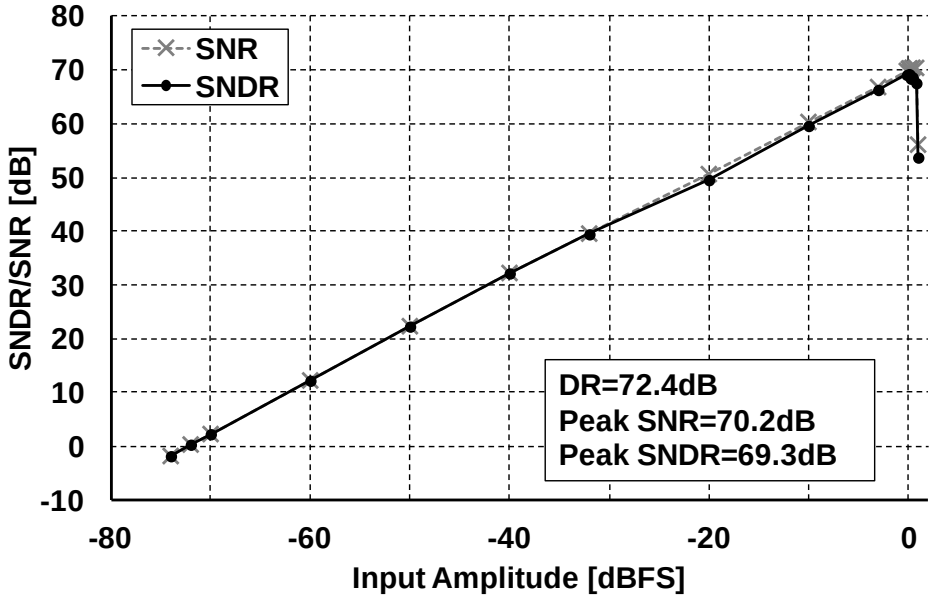

Figure 4.27: Dynamic range of the proposed ADC

Table 4.1: Performance summary

Process	**0.13µm CMOS**		
Supply	**1.3V**		
Input	**2.4V_{P-P}**		
Fs	**70MS/s**		
Power	**6.38mW**		
Area	**0.5mm^2**		
SNR	**70.2dB (@F_{IN}=1MHz)**	**66.1dB (@F_{IN}=20MHz)**	**64.2dB (@F_{IN}=50MHz)**
SNDR	**69.3dB (@F_{IN}=1MHz)**	**65.2dB (@F_{IN}=20MHz)**	**62.6dB (@F_{IN}=50MHz)**
FOM	**38.2fJ/C-S (@F_{IN}=1MHz)**		

CHAPTER 5. CONCLUSIONS

The research work shown in this dissertation focused on developing new power efficient ADC architectures using both the voltage domain and the time domain information. New ideas were verified with prototype implementations and performance measurements. This section will summarize this research and discuss possible future works.

5.1 Summary

In this dissertation, two different approaches to achieve high resolution (12b ENOB) with good power efficiency based on oversampling and Nyquist ADC architecture were discussed. The first delta-sigma ADC employs noise-shaped two-step integrating quantizer which uses time domain quantizer for an extra order of noise shaping. It also incorporates a new feedback method which allows the utilization of a high resolution quantizer in the delta-sigma loop without increased complexity. The proposed architecture enables high resolution and wide signal bandwidth, which is difficult to achieve in a conventional second order system.

In the second approach, the quantization error in time is processed by the pipelined TDC at Nyquist rate for a higher signal bandwidth instead of achieving an extra order of noise shaping like an oversampling ADC. Due to the simple structure of the pipelined TDC based on the charge pump instead of an expensive residue amplifier, it provides efficient conversion with low power consumption. The proposed ADC also adopts a new voltage-to-time conversion

scheme in the first stage to process the input signal in voltage domain. With the proposed V-T conversion, the proposed ADC can utilize a very low gain amplifier in the first stage MDAC as a residue amplifier which is the most power hungry block in pipelined ADC. Table 5.1 compares the recent published state of the art Nyquist ADC with SNDR above 62dB (10b ENOB), sampling rate above 50MHz, and figure of merit (FOM) below 100fJ/C-S [44]-[48]. As shown in table, the proposed ADC (second approach in this dissertation) shows a very competitive FOM among the recent published ADCs with similar specifications. The FOM of the proposed ADC can be improved further with an advanced CMOS process.

In conclusion, the research in this dissertation shows a new approach using both time domain and voltage domain signals in analog-to-digital conversion. By using time domain signal processing as a supplementary method to the conventional voltage domain signal processing, high resolution and low power consumption can be accomplished. The proposed architectures have strong advantages particularly in recent sub-micron CMOS processes, not only from the scaling benefit but also from using a low-gain residue amplifier with low power consumption (in the first approach). It also has a benefit of utilizing a low open loop gain amplifier with maximum signal swing (in the second approach) which can be difficult to design with a low supply voltage.

Table 5.1: Performance comparison

	This work	Morie [ISSCC'13]	Kapusta [ISSCC'13]	Brooks [ISSCC'09]	Chu [VLSI'10]	Lee [VLSI'10]
Process [nm]	**130**	**90**	**65**	**90**	**90**	**65**
Arch.	**Pipeline (TDC)**	**SAR**	**SAR**	**Pipeline (ZCBC)**	**Pipeline (ZCBC)**	**SAR (Two-step)**
F_S [MHz]	**70**	**50**	**80**	**50**	**100**	**50**
Peak SNDR [dB] ($@F_{IN}$)	**69.3 (@1MHz)**	**71 (@1MHz)**	**73.6 (@5MHz)**	**62 (@10MHz)**	**65 (@24MHz)**	**65.5 (@4MHz)**
Power [mW]	**6.38**	**4.2**	**31.1**	**4.5**	**6.2**	**3.5**
Peak FOM [fJ/C-S]	**38.2**	**28.7**	**99.6**	**87.5**	**42.8**	**45.5**

5.2 Future work

While this research shows new ADC architectures based on utilizing both voltage and time domain signal processing, it also can lead to a few interesting architectures that use a time domain quantizer.

The delta-sigma ADC architecture using the two-step integrating quantizer can be improved further. As explained earlier, the speed of the delta-sigma ADC is limited by the residue amplifier (in MDAC) which drives the sampling capacitor for the analog residue feedback. Fig. 5.1 shows the modified approach using PWM feedback. In this approach, the LSB feedback signal is fed back to the loop filter in time domain instead of feeding back the analog residue in voltage domain. Since the residue amplifier doesn't drive the sampling capacitor, the power consumption of the amplifier can be significantly reduced. Also, the

feedback factor of the amplifier in the loop filter is improved. Therefore, this modified approach will improve the power efficiency of the delta-sigma ADC or it can further increase the sampling rate.

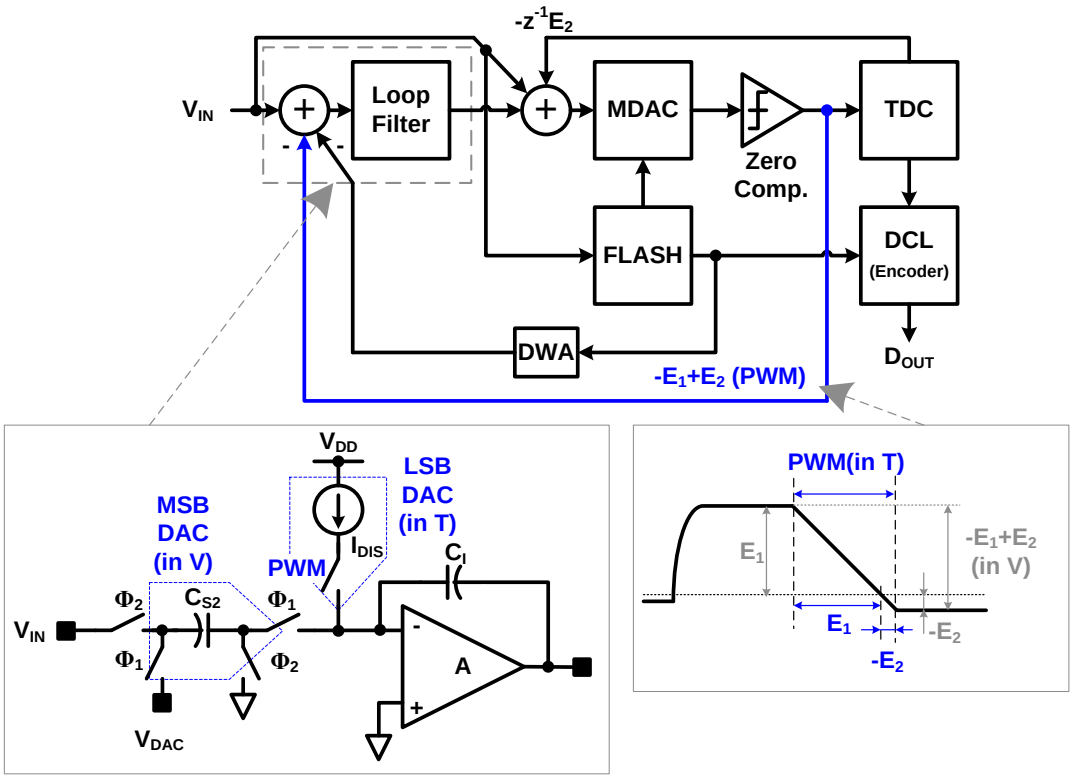

Figure 5.1: Improved delta-sigma architecture using PWM feedback

The proposed V-T conversion with a coarse quantizer (MDAC and FLASH) in the second approach can alleviate the V-T conversion problem that can limit the TDC performance in a general TDC design [49]. Since the proposed architecture enables the use of a low gain amplifier for the V-T conversion with high linearity, the proposed V-T conversion stage can be used as a first stage of any TDC architecture. Fig. 5.2 shows the generalized architecture

with the proposed V-T conversion stage. Although the proposed Nyquist ADC shows good power efficiency based on the charge-pump based backend stage, the power efficiency of the backend TDC can be improved further incorporating more digital-like blocks (such as a VCO quantizer). This can be a power efficient architecture particularly in an advanced CMOS process such as 65nm or less. In this generalized architecture, to build a more power efficient backend TDC with any type of time domain quantizer, either in Nyquist or oversampling rate will be an interesting research topic.

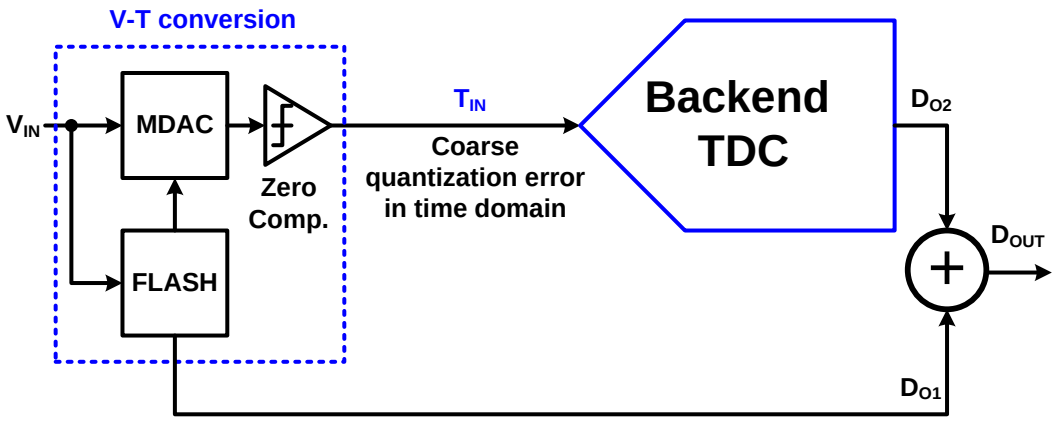

Figure 5.2: Generalized architecture with the proposed V-T conversion block

Meanwhile, the V-T gain mismatch of the proposed architecture in this dissertation should be calibrated accurately. While this calibration is done in foreground by external trimming and digital radix calibration in this dissertation, the background calibration is more preferable to address the PVT variation and the robust operation. Additional research to build a background calibration algorithm will also be an interesting research topic.

5.3 Acknowledgements

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