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Pavan Kumar Hanumolu

Voltage controlled oscillator (VCO) based ADC is an important class of time-domain ADC that has gained widespread acceptance due to their several desirable properties. VCO-based ADCs behave like an open-loop continuous time $\Delta\Sigma$ modulator and achieve excellent resolution by first order noise shaping the quantization error. However, the SNDR of an open-loop VCO-based ADC is severely distortion limited by the voltage-to-frequency tuning characteristics of the VCO. This work examines various techniques that have already been proposed to overcome the VCO tuning non-linearity problem. Two new VCO-based ADC architectures, that overcome the limitations of the conventional approaches, are proposed. In the first approach, the ADC is linearized by forcing the VCO to operate at only two operating points using a front-end two level modulator. With this technique, the linearity is improved without using either a multi-bit feedback DAC or calibration. Fabricated in a 90 nm CMOS process, the prototype ADC achieves better than 71 dB SFDR and 59.1 dB SNDR in 8 MHz signal bandwidth while consuming 4.3 mW power. The ADC achieves a figure of merit of 366 fJ/conv-step, which is

comparable with other state of the art time based ADCs. In the second approach, the need for a front-end two level modulator is obviated using linearizers, which introduce an inverse of VCO's voltage to frequency characteristics in the signal path. A deterministic digital calibration unit runs continuously in the background and builds the inverse voltage to frequency transfer function. Implemented in a 90nm CMOS process, this on-chip calibration improves SFDR of the prototype ADC from 46 dB to more than 83 dB. The ADC consumes 4.1 mW power and achieves 73.9 dB SNDR in 5 MHz signal bandwidth resulting in an excellent figure of merit of 101 fJ/conv-step.

Linearizing Techniques for Voltage Controlled Oscillator Based Analog to Digital Converters

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Sachin B Rao

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Director of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Sachin B Rao, Author

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CHAPTER 1. INTRODUCTION

CMOS technology scaling has enabled the integration of very large scale systems on a single chip, where bulk of the signal processing is performed efficiently in the digital domain. However, since the real world signals are analog in nature they need to be converted to the digital domain. This conversion is done using analog to digital converters (ADCs). ADCs thus form the indispensable bridge between the 'real world' and the 'digital world' which exist in almost every electronic system. Figure 1.1(a) shows an example ADC application in a typical radio-frequency (RF) receiver system. The low noise amplifier (LNA), mixer and filter form the RF

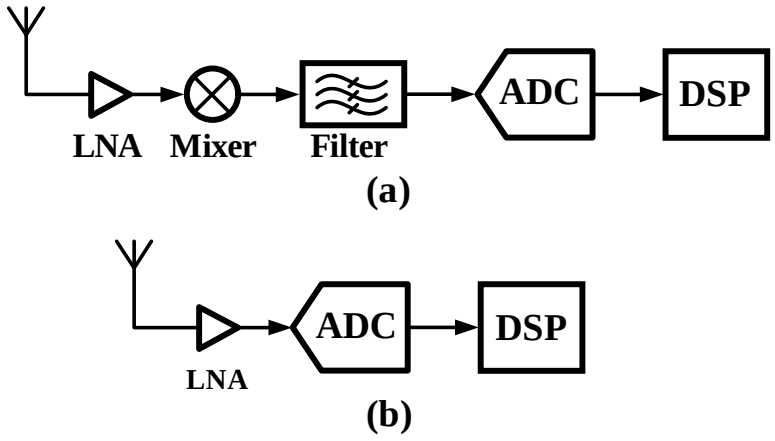

Figure 1.1: Simplified architecture of the RF receiver employing ADC. (a) Down converting receiver. (b) Direct sampling receiver.

section of the system which down-convert the received signal to base-band. The ADC then converts the base-band signal to digital domain. Most of the remaining signal processing including decoding, compression, storage etc., is performed in digital-domain using the digital-signal-processor (DSP). Recently in more advanced systems, the RF section is simplified by directly digitizing the received RF signal using a high performance ADC as shown in Fig. 1.1(b). In such systems, entire signal processing including the RF demodulation is performed in the digital domain by a high-speed DSP. To reduce system cost in such applications, it is highly desirable to integrate both the ADC and DSP on a single chip. To reduce system power and improve performance, the DSPs are implemented in the most advanced technology nodes, thereby forcing even the ADCs to be designed in such technology nodes.

1.1 Effect of Technology Scaling

As CMOS technology continues to scale, faster and smaller transistors have been realized, which significantly reduce power consumption in digital circuits. However, the transistor's intrinsic gain, headroom and leakage currents have progressively degraded. These factors negatively impact analog circuits such as ADCs, and their power consumption does not scale accordingly. In fact, for a given signal to noise ratio, in a thermal noise limited scenario, the power consumption of analog ciruits is higher in an advanced technology node. This is mainly because of the reduced supply voltage and reduced signal swing [1]. In addition to this, conventional high-performance voltage-domain ADCs, such as pipelined-ADC, $\Delta\Sigma$-ADC etc., require high-gain and high-bandwidth operational amplifiers (op-amps) [2]. Due to reduced intrinsic gain and headroom, realizing such high-performance op-

amps is becoming increasingly difficult. These factors have forced designers to invent new ADC architectures and circuit design techniques that take advantage of technology scaling and reduce power consumption.

Time-domain analog to digital conversion is one such technique that benefits from miniaturization and improved transistor speed. Contrary to conventional voltage domain ADCs which perform voltage quantization, time-domain ADCs perform quantization in time. Therefore, these ADCs take advantage of faster clock and improved time resolution in advanced technology nodes. It can be shown that a time-domain flash ADC consumes relatively much less power when compared with a voltage-domain flash-ADC, especially at higher resolution [3]. Because of these advantages, time-domain ADCs have recently become popular and various such ADC architectures have been invented.

1.2 Scope of this work

Among different time-based ADC architectures, voltage controlled oscillator (VCO) based ADCs are very attractive and possess several desirable properties. While retaining all the benefits of other time-based ADCs, VCO-based ADCs achieve high resolution without employing analog building blocks such as op-amps, comparators, precision references etc., which suffer from technology scaling. However, the performance of open-loop VCO-based ADCs are severely distortion limited by the VCO tuning non-linearity. This work focuses mainly on developing new techniques to improve the linearity of VCO-based ADCs. After a brief review of various time-based ADC architectures, advantages and limitations of existing VCO-based ADC architectures are discussed. Two new VCO-based ADC architectures, that overcome the limitations of conventional approaches are presented.

Measurement and simulation results are provided to validate both the proposed architectures.

1.3 Thesis Organization

The thesis is organized as follows. Chapter 2 discusses various time-domain ADC architectures. Chapter 3 introduces VCO-based ADC and discusses the advantages and limitations of prior-art VCO-based ADC architectures. In Chapter 4, a technique to linearize the VCO-based ADC by operating it at only two points on the tuning curve is presented. A new background calibration scheme is presented in Chapter 5. Finally, Chapter 6 provides a brief summary and concludes this research work.

CHAPTER 2. TIME DOMAIN ANALOG TO DIGITAL CONVERTER ARCHITECTURES

Time-domain analog to digital converters (ADCs) differ from voltage-domain ADC in that they quantize the input signal using time as the reference quantity. Since quantization is performed in time domain, these ADCs take advantage of improved time resolution in finer technology nodes. Therefore, they have emerged as an attractive alternative to conventional voltage-domain ADCs, especially in the the last few years. Various types of time-domain ADC architectures have been developed over the years. This chapter briefly discusses different time-domain ADC architectures, their advantages, disadvantages and performance limiting factors.

Figure 2.1 shows a simplified version of one of the earliest time-domain ADCs [4, 5]. A pulse width modulator (PWM) produces an output pulse whose width is

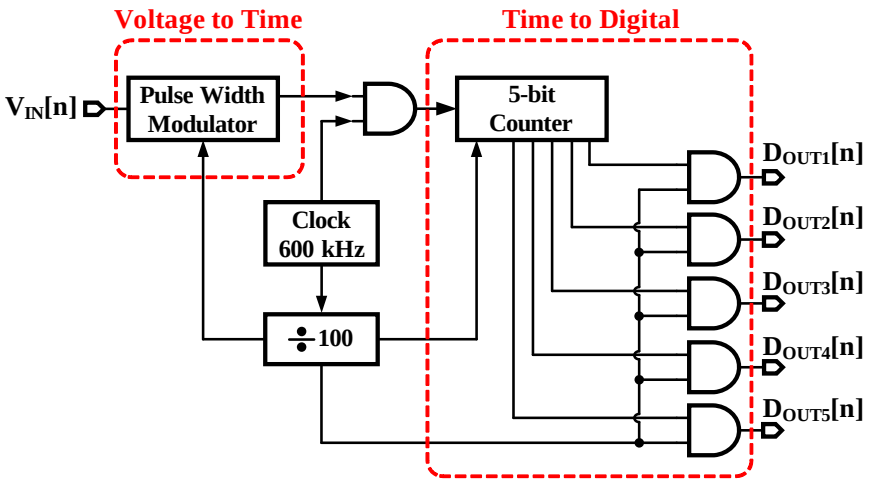

Figure 2.1: Simplified block diagram of first patented time-domain ADC.

proportional to the sampled input signal, $V_{IN}[n]$. The PWM therefore acts as a

voltage-to-time converter (VTC). The 5-bit counter measures the width of the VTC output pulse by counting total number of clock edges of the 600 kHz clock when the PWM output is 'high' and gives a digital output, $D_{OUT}[n]$. The counter thus acts as a time-to-digital converter (TDC). In the above example, since the quantization step corresponds to one time period of the 600 kHz clock, the resolution this ADC is limited by the 600 kHz clock. Due to technology scaling, multi giga-hertz clock frequencies can be realized at relatively low power. The resulting improved time resolution leads to improved ADC resolution.

All time-domain ADCs have the general structure shown in Fig. 2.1 and contain a VTC and a TDC. The VTC converts the input voltage signal to a time signal and the TDC quantizes the time signal to give a digital output. These ADCs differ by employing different VTC and TDC architectures. The rest of the chapter discusses different time-domain ADC architectures. Section 2.1 discusses recent developments in integrating ADCs. Time-domain ADCs that use high-resolution and high-sampling rate TDCs are discussed in Sec. 2.2 followed by a discussion of voltage-to-frequency conversion based ADCs in Sec. 2.3.

2.1 Integrating ADC

A simple block diagram of a single-slope integrating ADC is shown in Fig. 2.2(a). It's operation is explained with the waveforms shown in Fig. 2.2(b). During the sampling phase, Φ_S, the input is sampled on to the integrating capacitor C_I. In the counting phase, Φ_C, the integrating capacitor is discharged with a constant current source, I_D. The counter is enabled at the beginning of Φ_C and it counts till the integrating capacitor is fully discharged. A reset phase is applied to remove any residual charge on the capacitor before the start of next sampling phase. With

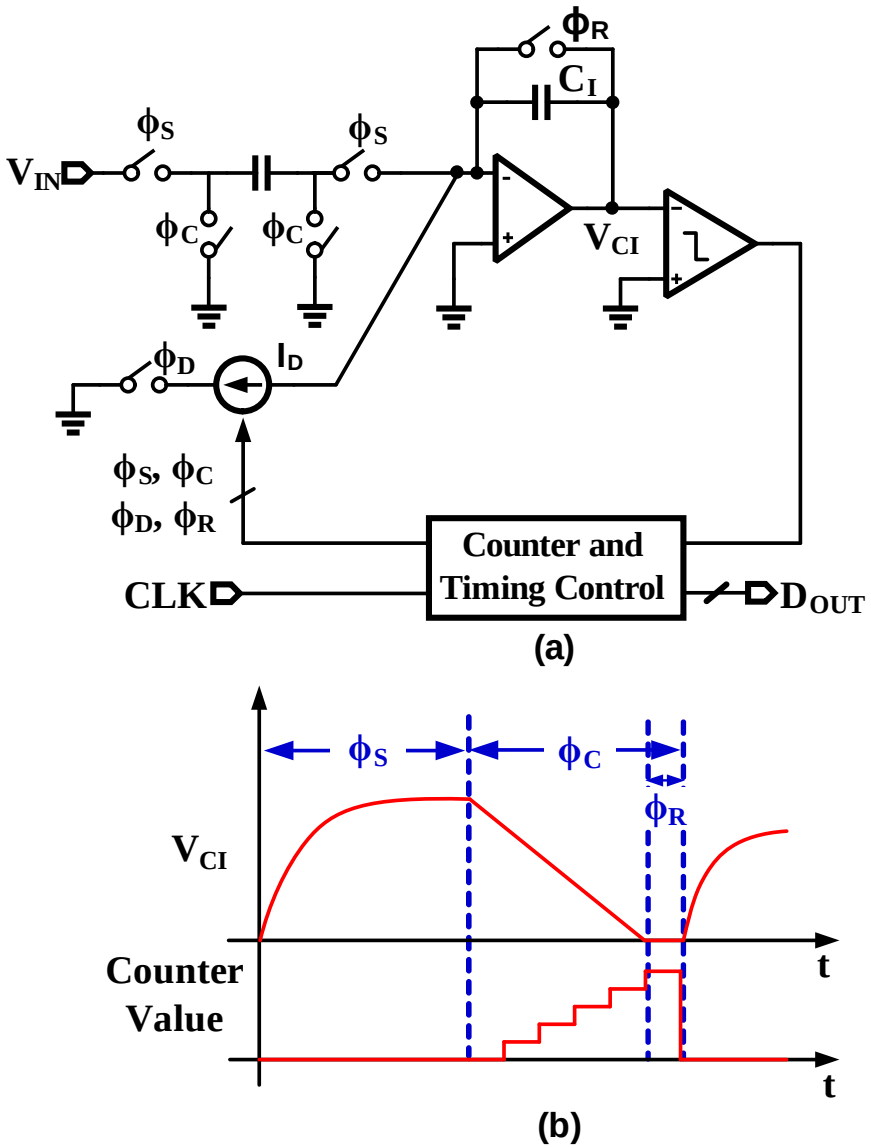

Figure 2.2: Single slope ADC. (a) Simplified block diagram. (b) Time domain waveforms.

this operation, the counter value at the end of each count phase is given by,

$$D_{OUT}[n]\frac{T_S I_D}{C_I} = V_{IN}[n] + E_Q[n] \tag{2.1}$$

where $D_{OUT}[n]$ represents the ADC output and T_S represents period of the counter reference clock, CLK. $0 \leq E_Q[n] < \frac{T_S I_D}{C_I}$ represents the quantization noise.

Though this ADC has a relatively simple implementation it requires a large conversion time. Assuming equal durations for Φ_S and Φ_D, the time taken by this ADC to resolve N-bits is given by,

$$T = 2^{(N+1)}T_S \tag{2.2}$$

which indicates that the conversion time varies exponentially with the desired ADC resolution. Nevertheless, this architecture can be used in low speed applications where monotonic or high-resolution output is desired.

2.1.1 Multi-slope Integrating ADC

To improve the conversion time of the single slope ADC, various architectural changes have been employed. Figure 2.3(a) shows the simplified block diagram of a multi-slope ADC [6]. As opposed to the architecture shown in Fig. 2.2, multiple current sources I_{D1}, I_{D2} and I_{D3}, have been employed in this implementation. The operation can be explained using the waveforms shown in Fig. 2.3(b). During Φ_S, the operation is similar to single slope ADC and the input is sampled on to the integrating capacitor C_I. The count phase, Φ_C, begins by enabling current source I_{D1} which discharges C_I. Once completely discharged, I_{D1} is disabled at the next rising edge of the reference clock, CLK. During this time the counter determines the total number of clock edges to give a digital output, n_1. Since I_{D1} is disabled only at the rising edge of the reference clock, the quantization noise from this measurement is stored in C_I as shown in Fig. 2.3(b). Next, in a similar way, n_2 is obtained by measuring the stored quantization noise by enabling I_{D2}. Since I_{D2} has smaller magnitude and opposite polarity to that of I_{D1}, finer resolution is obtained in this step. The above procedure is repeated till all the current sources

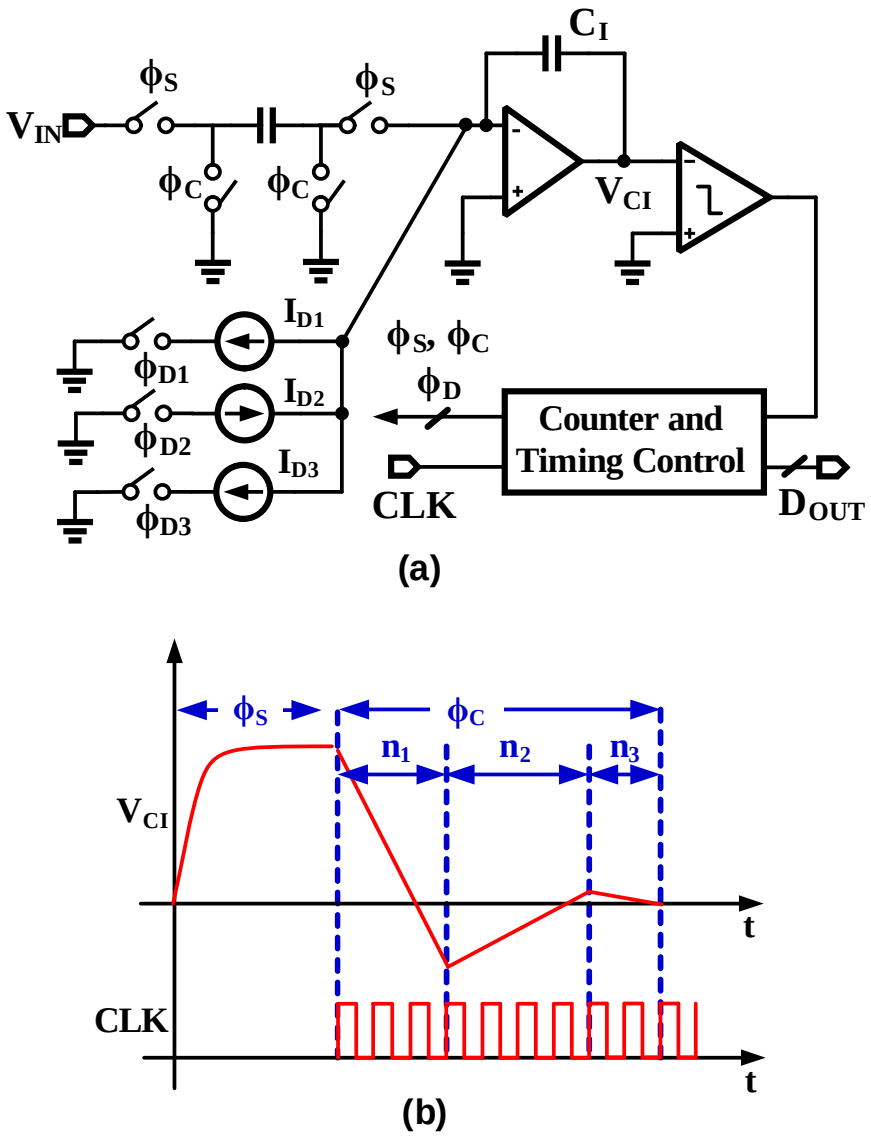

Figure 2.3: Multi slope ADC. (a) Simplified block diagram. (b) Time domain waveforms.

are successively enabled and disabled. The resolution of this ADC is $N = N_1 + N_2 + N_3$, where N_1, N_2 and N_3 are total number of bits resolved by I_{D1}, I_{D2} and I_{D3}, respectively. The worst case convergence time of this ADC is given by,

$$T = (2^{N_1} + 2^{N_2} + 2^{N_3})T_S \tag{2.3}$$

which is much smaller than a single-slope ADC. Though multi-slope ADC results in much faster conversion time, the requirement of multiple current sources is an important drawback. Mismatch between these current sources results in non-linearity and non-monotonic behavior and limits the ADC performance.

2.1.2 Sub-ranging Integrating ADC

Another architecture that improves the conversion time employs sub-ranging techniques [7]. Figure 2.4(a) shows the simplified block diagram of a sub-ranging time-domain ADC. The sub-ranging algorithm is demonstrated with the time-domain waveforms shown in Fig. 2.4(b). An input current, I_{IN}, charges the capacitor C_1 for one reference clock period, T_{CLK}. The counter determines the number of clock cycles taken by a reference current, I_{REF}, to charge another capacitor C_2 (= C_1) to the same voltage as that on C_1. Once the voltage on C_2 equals to that on C_1, the counter value, which represents the MSBs, is read and both the capacitors and the counter are reset. Next, by charging C_1 till the end of the next clock edge, the complement of residue, T_{RESB}, can be stored on C_1. Each sub-ranging phase involves charging C_2 till its voltage equals that of C_1, resetting C_1 and charging it again till voltage across it equals that of C_2. This process amplifies the residue by 2, in time, as shown in Fig. 2.4(b). The number of rising edges of CLK in each sub-ranging phase represents the amplified residue from the previous sub-ranging phase. In the actual implementation of this technique, the time taken to resolve N bits is given by,

$$T = (5N)T_S \tag{2.4}$$

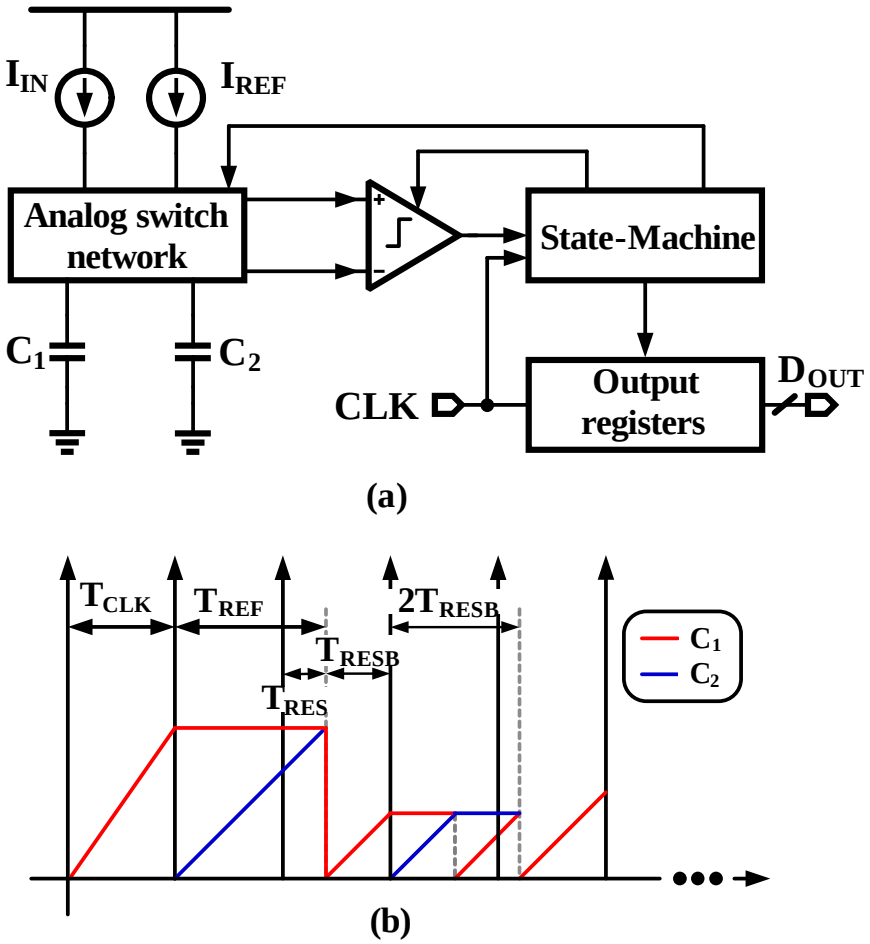

Figure 2.4: Subranging time domain ADC. (a) Simplified block diagram. (b) Time domain waveforms.

where the multiplication by 5 comes from a special algorithm used to avoid very small time residues in each sub-ranging phase. Though the above technique greatly reduces the conversion time, it requires a highly linear voltage to current converter to convert input voltage to current, I_{IN}. Furthermore, the performance is affected by the comparator delay, and charge injection from the switch network.

2.1.3 *Noise shaping Integrating ADC*

With simple modifications to the single-slope ADC shown in Fig. 2.2 quantization noise shaping can be achieved. Figure 2.5(a) shows the modified ADC [8].

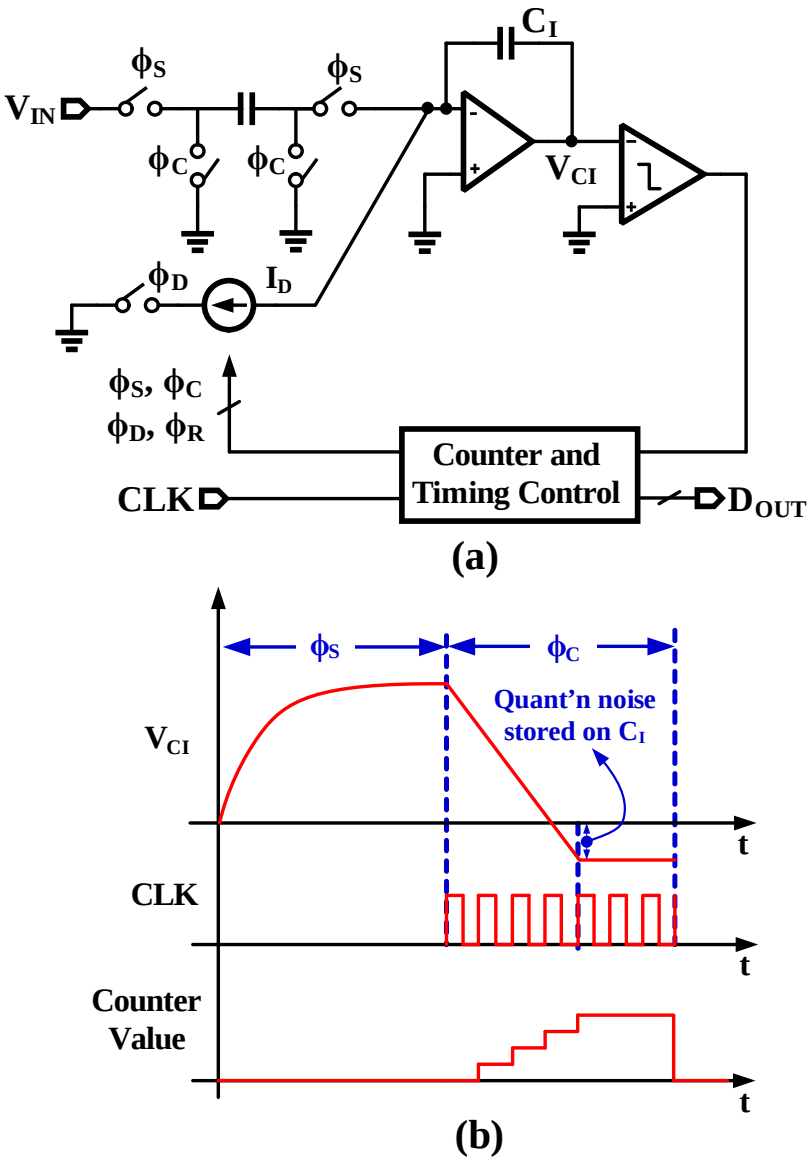

Figure 2.5: Noise shaping integrating ADC. (a) Simplified block diagram. (b) Waveforms depicting noise-shaping integrating ADC operation.

Here, instead of disabling the current source immediately after V_{CI} is completely

discharged, it is disabled at the next rising edge of the reference clock as shown in Fig. 2.5(b). Consequently, the quantization noise is stored in the capacitor C_I. By avoiding the reset phase for the integrating capacitor, the stored quantization noise can be used in the next clock period to obtain first order noise-shaping [8]. Though good resolution is obtained at a relatively higher speed, compared with other types of time-domain ADCs, these techniques are not suited for very high speed applications.

2.2 Delay-line based ADC

The integrating ADCs discussed in the previous section are suitable for high resolution, low speed applications. In applications where high speed, but medium resolution (6 - 10bits) is desired, delay-line based analog to digital converters are used. Architecturally, these ADCs are similar the one shown in Fig. 2.1, but instead of counters, they employ CMOS delay-line based time-to-digital converters (TDC). Such TDCs are also employed in digital phase locked loops (PLLs) to replace the phase frequency detectors. Improvements in the process technology and scaling have led to the development of high-speed, high-resolution and low-power TDCs.

Figure 2.6(a) shows a simple delay-line based TDC that digitizes the time difference, $T_{IN}[n]$, between the rising edges of START and STOP signals [9]. The START pulse edge is applied to the delay line and the state of the delay elements is captured at the rising edge of STOP. Since it takes a time, τ_d, for the START pulse edge to propagate through one delay element, the captured value in the flip-flops represent a thermometer encoded representation of the input pulse width $T_{IN}[n]$.

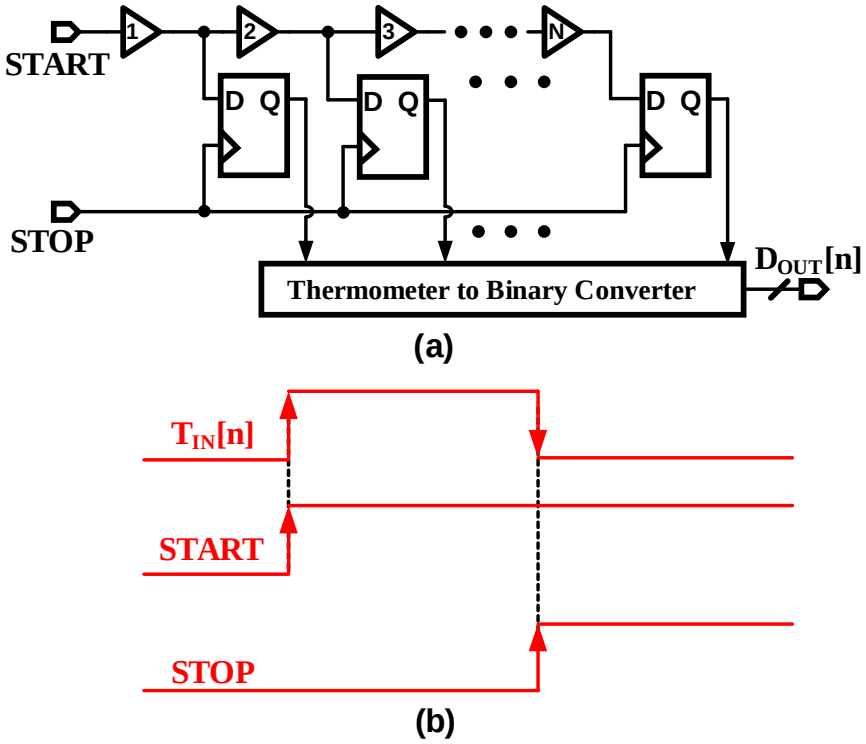

Figure 2.6: Delay line based TDC. (a) Block diagram. (b) Time domain waveforms.

The TDC output, $D_{OUT}[n]$, can be expressed as,

$$T_{IN}[n] = D_{OUT}[n]\tau_d + T_Q[n] \tag{2.5}$$

where $0 \leq T_Q[n] < \tau_d$ represents the quantization noise in time. Since this TDC consists of only inverters and flip-flops and does not require any precision references it is easy to design. Furthermore, since the buffer delay, τ_d, reduces with process scaling, the resolution of this TDC improves with technology scaling. When used in an ADC, the START and STOP pulses are generated from a voltage to time converter. A pulse width modulator or an asynchronous $\Delta\Sigma$ modulator may be used as a voltage to time converter [10].

Though the TDC-ADC discussed above is easy to implement and is scaling friendly, it suffers from two main drawbacks. First, its dynamic range is limited by

the number of stages (delay cells) in the delay line. A large dynamic range would require a large number of stages, thereby complicating the design. For example, a 10-bit dynamic range would require as many as 1024 delay elements. Second, ensuring good matching between all these delay elements across PVT corners is a very difficult design task.

2.2.1 Two-step TDC based ADC

The low dynamic-range problem associated with basic TDC discussed in the previous section can be overcome by employing a two-step TDC as shown in Fig. 2.7(a) [11]. The associated time domain waveforms are shown in Fig. 2.7(b). The voltage-to-time conversion is performed by a continuous time comparator by comparing the input to a ramp signal. A 5-bit counter acts as a coarse quantizer and quantizes the time, T_C, into 5 MSBs. A 32-stage delay line quantizes the time, T_F, into 4-bit LSBs. The final output is obtained by subtracting the MSBs from the LSBs to get $T_M = T_C - T_F$. In order avoid very small T_F, one additional reference clock (CLK) period is added to both T_C and T_F. Since the two times are subtracted after digitization, the added reference clock period cancels and does not have any impact on the final output. By operating the TDC at 400mV supply, the power consumption is limited to only 7 μW while operating at 1MHz sampling rate. The power consumption of the entire ADC (including the ramp generator) is 14 μW resulting in a figure-of-merit (FOM) of 97 fJ/conv-step.

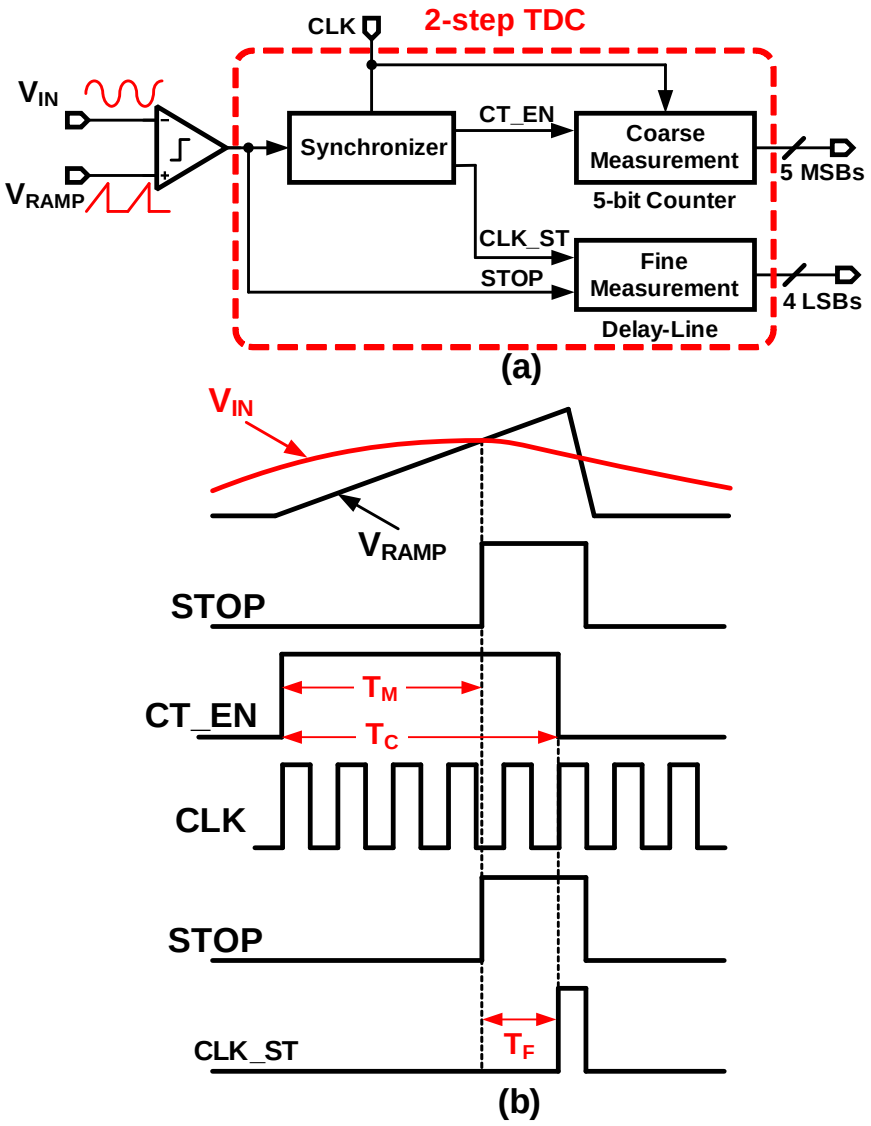

Figure 2.7: Two-step TDC based ADC. (a) Simplified block diagram. (b) Timing diagram.

2.2.2 Oversampling TDC based ADC

Using the two-step TDC architecture, improving the SNDR further would be difficult as the linearity of the voltage-to-time converter and matching between

delay-cells would start to limit the performance. In another design approach, the performance of the TDC-ADC has been improved using a $\Delta\Sigma$ loop as shown in Fig. 2.8 [12]. Since the loop filter high-pass shapes any error introduced in the

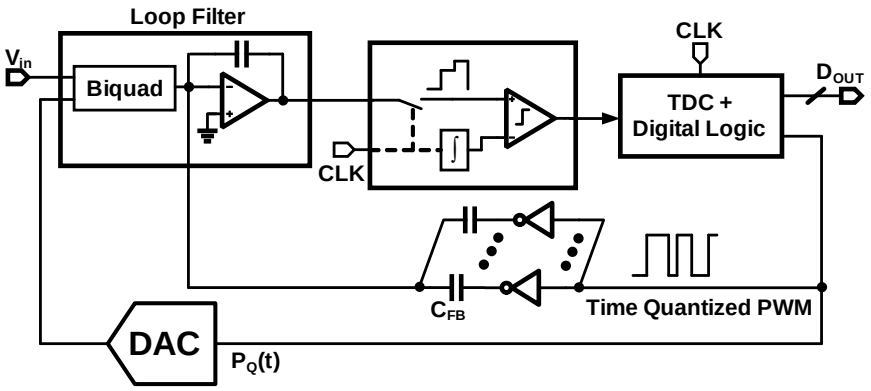

Figure 2.8: High resolution TDC-ADC using a $\Delta\Sigma$ loop.

TDC-ADC, the linearity requirement of the voltage-to-time converter is greatly reduced. For example, since a 3rd order loop filter is used in [12], a voltage-to-time converter with only 35 dB SNDR is sufficient to achieve an overall SNDR better than 70 dB. Furthermore, since quantization is performed in time-domain, as many as 50 quantization steps can be obtained in the 65nm CMOS process, thereby reducing the quantization noise. The large number of quantization steps would have complicated the feedback DAC design in a conventional $\Delta\Sigma$ modulator. This problem is circumvented in this design by generating a 1-bit PWM feedback pulse from the TDC. Though the PWM feedback DAC is highly linear due to the absence of multiple elements in the DAC, it imposes a stringent matching requirement (800 fs-rms) on the delay-stages in the TDC that are used to generate the feedback pulse. However, it should be noted that this matching requirement is a result of PWM feedback and not due to the application of TDC-ADC as a quantizer in a $\Delta\Sigma$ loop.

2.3 Voltage-to-Frequency Conversion Based ADC

The earliest voltage-to-frequency conversion based ADC (VFC-ADC) was described in a US patent [13]. Figure 2.9 shows a simplified block diagram of one such VFC-ADC [5].

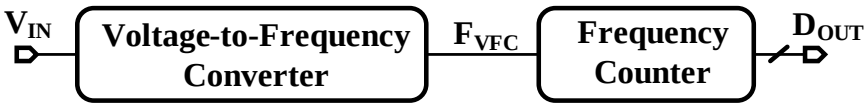

Figure 2.9: Voltage to frequency conversion based ADC.

Voltage to frequency converter is used to convert the analog input to an output frequency, F_{VFC}. This frequency is converted to digital representation using a frequency counter, which periodically determines the total number of rising edges (pulses) in the VFC output [14]. The digital output, $D_{OUT}[n]$, is therefore given by,

$$D_{OUT} \propto F_{VFC} \propto kV_{IN} \tag{2.6}$$

which indicates that the digital output is proportional to input, V_{IN}, if the VFC output frequency is proportional to V_{IN}. Since these ADCs consume very less power and are monotonic, they have been used in telemetry applications where the VFC and frequency counter need not be located physically close to one another.

Traditionally, current steering multi-vibrator based VFCs or charge-balance VFCs have been used to achieve high linearity. Consequently such ADCs had been used in application requiring 12 - 14 bit linearity. However, more recently CMOS based ring-oscillators have been employed to improve resolution and achieve wide bandwidth [15]. Such VFC-ADCs are also known as voltage-controlled-oscillator based ADC (VCO-based ADC). VCO-based ADCs offer a number of advantages over other types of time-domain, and voltage-domain ADCs and therefore are

highly desirable. In addition to being scaling friendly, these ADCs obviate the need for a front-end VTC. Furthermore, they achieve excellent resolution by first order noise shaping the quantization noise. In the next chapter, implementation details of a VCO-based ADC, their properties, advantages and limitations are discussed.

CHAPTER 3. OVERVIEW OF VCO-BASED ADCS

A simplified block diagram of high sampling rate ring VCO-based ADC is shown in Fig. 3.1(a) [15]. The analog input, $V_{in}(t)$, controls the delay of each inverter and sets the oscillation frequency of the N-stage ring-oscillator.

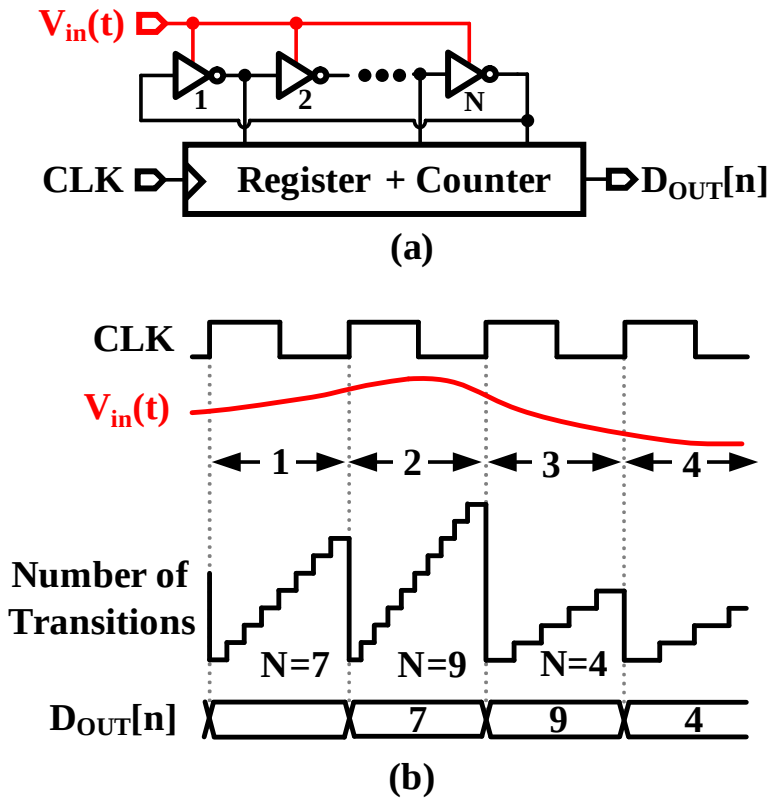

Figure 3.1: VCO-based quantizer. (a) Simplified block diagram. (b) Representative waveforms.

The digital output, D_{OUT}, is obtained from the register and counter by determining the total number of inverters that undergo a transition in each period of the reference clock, CLK. The operation of this ADC can be understood with the waveforms shown in Fig. 3.1(b). During the reference clock period 1, V_{in} sets the

delay such that seven inverters in the ring-oscillator undergo a transition resulting in $D_{OUT} = 7$. During the clock period 2, V_{in} has increased which reduces inverter delay resulting in nine transitions and therefore $D_{OUT} = 9$. Similarly, in the subsequent clock period 3, $D_{OUT} = 4$. The digital output during each reference clock period can be expressed as,

$$D_{OUT} = \frac{T_S}{t_d\left(V_{in}\right)} \tag{3.1}$$

where T_S is the reference clock period, and $t_d\left(V_{in}\right)$ is the input voltage dependent delay of each inverter. For a simple N-stage ring-VCO shown in Fig. 3.1(a), the oscillation frequency is related to $t_d\left(V_{in}\right)$ as,

$$f_{VCO}\left(V_{in}\right) = \frac{1}{2Nt_d\left(V_{in}\right)} \tag{3.2}$$

Therefore,

$$D_{OUT} = \frac{T_S}{t_d\left(V_{in}\right)} = 2NT_S f_{VCO}\left(V_{in}\right) \tag{3.3}$$

From the above equations,

$$D_{OUT} \propto V_{in} \text{ if, } f_{VCO}\left(V_{in}\right) \propto V_{in} \tag{3.4}$$

which confirms that the digital output indeed represents the analog input. Rigorous analyses of VCO-based ADCs have already been performed by others [15, 16, 17, 18, 19]. In the following sections some important properties will be briefly discussed .

3.0.1 Quantization noise shaping

VCO-based ADC provide first-order noise shaping to the quantization error. Consider the simplified functional block diagram shown in Fig. 3.2(a) [16, 17]. Here, the ring oscillator acts as a voltage-to-phase (V-to-P) converter which inte-

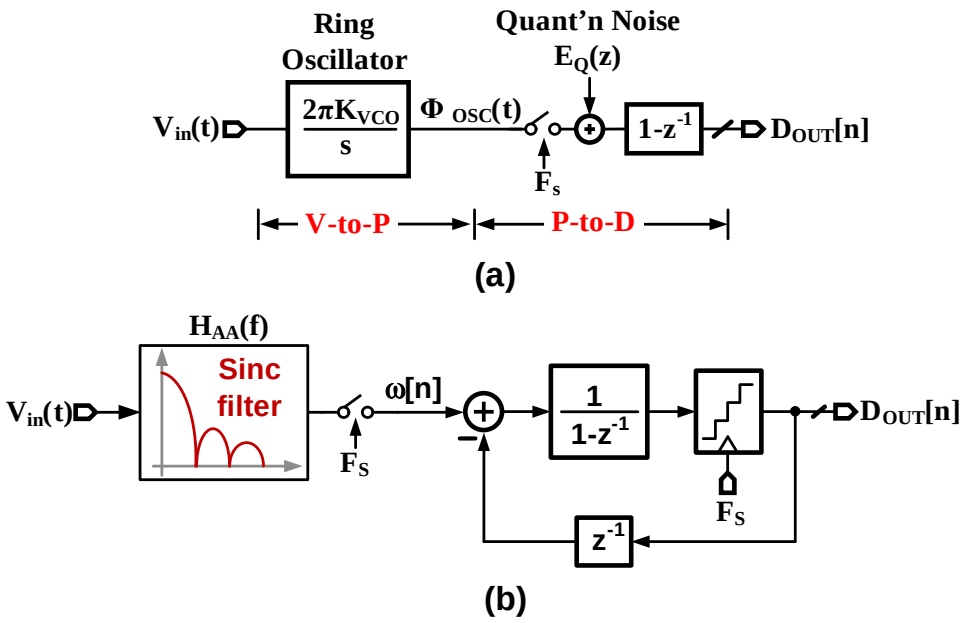

Figure 3.2: Modeling of VCO-based ADC. (a) Simplified functional block diagram of VCO-based ADC. (b) VCO-based ADC model with anti-aliasing filter and $\Delta\Sigma$ modulator.

grates the input voltage to produce an output phase, $\Phi_{OSC}(t)$, with a VCO gain K_{VCO}. The quantizer and digital differentiator model the process of determining the total number of inverters that undergo transition in every period of the reference clock. Since the input voltage sees a continuous time integration and a digital differentiation, there is no net integration or differentiation and the input appears at the output in digital form. However, since the quantization noise, $E_Q(z)$, sees only a differentiator, it is first order noise shaped at the ADC output. Consequently, this ADC benefits from oversampling and achieves an excellent resolution.

3.0.2 Anti-aliasing property

It can be shown that the models in Fig. 3.2(a) and Fig. 3.2(b) are mathematically equivalent [19]. Therefore a VCO-based ADC is equivalent to a $\Delta\Sigma$ modulator with a front-end anti-aliasing filter. The transfer function of this filter is given by,

$$\mathrm{H_{AA}(f)} = \mathrm{K_{VCO}} e^{-\mathrm{j}2\pi \mathrm{T_S f}} \frac{\sin(\pi \mathrm{T_S f})}{\pi \mathrm{f}} \tag{3.5}$$

which indicates that the ADC provides first order anti-aliasing to the input signal. Intuitively, in the small signal model shown in Fig. 3.2(a), since sampling is performed after a continuous time integration of the input, aliasing high frequency contents are suppressed relative to the low frequency input signal. Therefore, the ADC provides first order anti-aliasing to the input signal.

3.0.3 Effect of sampler metastability and offset

Compared with a voltage-domain ADCs such as a Flash-ADC, VCO-based ADCs exhibit improved sampler metastability behavior. In a flash-ADC, as the resolution of ADC is increased the voltage swing at the samplers reduce, thereby increasing the probability of metastable behavior. However, in a VCO-based ADC, the voltage swing at the input of the samplers is independent of the ADC resolution. Therefore, the probability of metastable behavior is significantly lower. It can be shown that, a N-bit VCO-based ADC is 2^{N} times less likely to encounter a metastable event [20].

Sampler offsets in a flash ADC changes the reference voltage and results in non-linearity. It can also lead to missing codes in higher resolution ADCs. A

VCO-based ADC is robust to such offset errors. Since these errors are introduced in the samplers, the digital differentiator first order noise shapes such errors and improves the ADC performance [18].

3.1 Effect of VCO tuning non-linearity

Though VCO-based ADCs have several desirable properties, their signal to noise and distortion ratio (SNDR) is severely limited by VCO tuning non-linearity. This can be understood with the simplified functional block diagram shown in Fig. 3.3. This model is similar to the one shown in Fig. 3.2(a), but here the V-to-

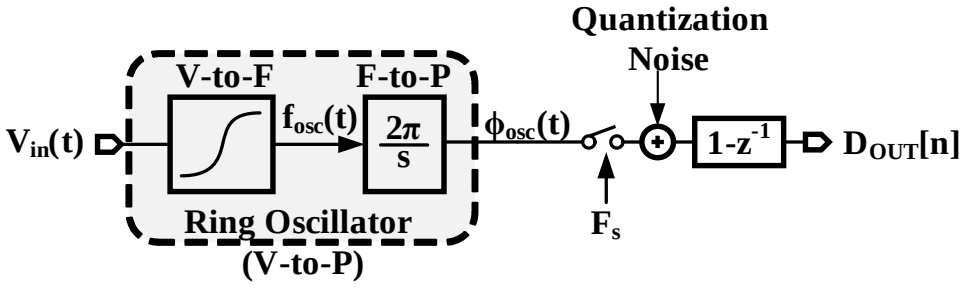

Figure 3.3: Simplified model of VCO-based quantizer.

P conversion within the ring-oscillator is divided into two separate steps, voltage to frequency (V-to-F) and frequency to phase (F-to-P) conversions. Since V-to-F transfer characteristic of a ring oscillator is highly non-linear, significant distortion is introduced in the V-to-F conversion. The simulated output spectrum of an open loop VCO-based quantizer with 16 ring-elements is shown in Fig. 3.4. The resulting SNDR and SNR are 23.7 dB and 66.5 dB, respectively, for an over-sampling-ratio (OSR) of 40. Since other error sources such as quantization noise, sampler offset errors etc., are suppressed by the digital differentiator, the V-to-F non-linearity forms the biggest bottleneck in achieving good SNDR from an open VCO-based

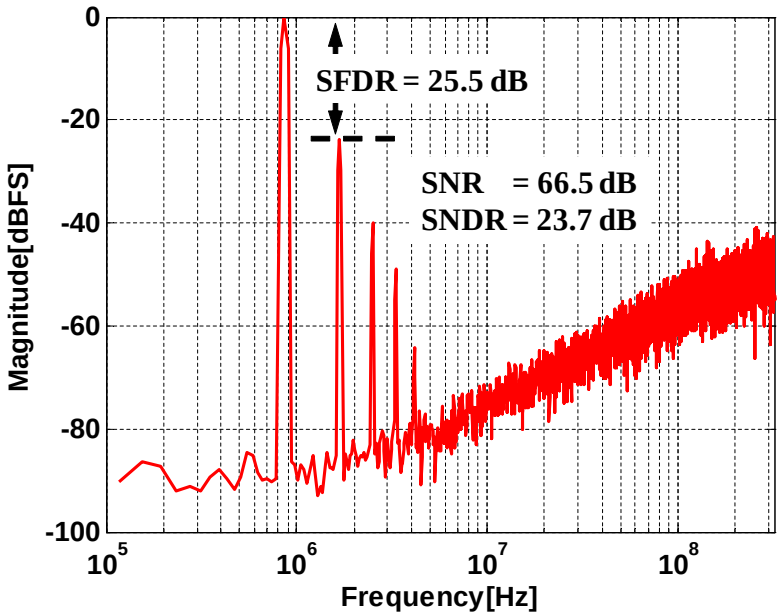

Figure 3.4: Output spectrum of open loop VCO-based ADC.

ADC.

3.2 Prior-art VCO-based ADC architectures

Various design techniques have already been proposed to overcome the VCO tuning non-linearity and improve the ADC performance. This section briefly discusses such prior-art VCO-based ADC architectures and appreciate their advantages and disadvantages.

3.2.1 *Linear VCO-based ADC using ΔΣ loop*

In [17, 21], the VCO quantizer is linearized by placing it inside a continuous-time ΔΣ loop as shown in Fig. 3.5. The negative feedback loop suppresses the

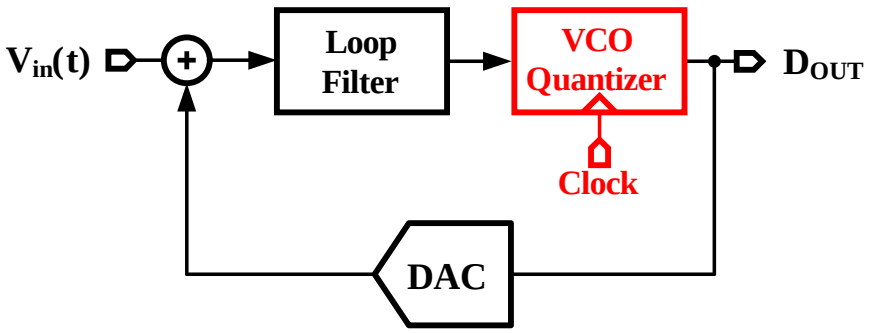

Figure 3.5: Schematic of VCO-based ADC in a delta sigma loop.

VCO non-linearity approximately by the gain of the loop filter. The improved spurious-free-dynamic-range (SFDR) given by,

$$\mathrm{SFDR_{OUT,CL}} \approx \frac{\mathrm{SFDR_{VCO,OL}}}{|1 + \mathrm{L(s)}|} \tag{3.6}$$

where $\mathrm{SFDR_{OUT,CL}}$ and $\mathrm{SFDR_{VCO,OL}}$ represent the SFDR with and without the negative feedback loop, respectively, and L(s) is loop filter gain. Though this technique improves the ADC performance, a high order loop filter is required to sufficiently suppress VCO non-linearity. To understand this, consider the typical loop filter gain as a function of frequency as shown in Fig. 3.6. The loop filter gain decreases at higher frequencies and the gain at the band edge, for a loop filter with non optimized zeros, can be approximated as [22],

$$|\mathrm{L(s)}| \approx \left(\frac{\mathrm{OSR}}{\pi}\right)^{\mathrm{N}} \tag{3.7}$$

which indicates that the problem is especially severe at low OSR. For example, from Eq. 3.6, to improve the SFDR from 25 dB to more than 75 dB the loop

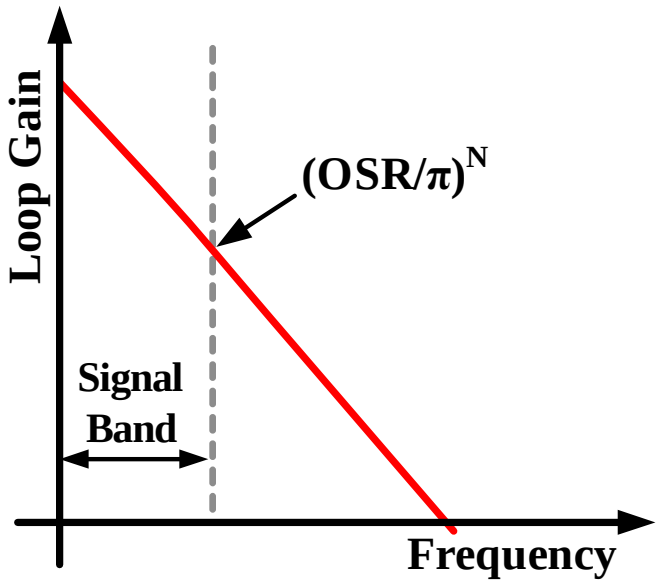

Figure 3.6: Loop filter gain vs. frequency.

filter must provide more than 50 dB gain within the signal-band. A 3rd-order filter would be sufficient to achieve this with an OSR of 40, however with an OSR of 40 a 4th order loop filter would be required [20]. Stabilizing a higher order feedback system poses many challenges and typically incurs a power penalty. Furthermore, even with a high order loop filter, the ADC performance continues to be limited by the VCO tuning non-linearity rather than the quantization noise. For example, the 2nd-order loop filter used in [17] results in a 3rd order noise shaping for the quantization noise. As a result, the peak SNDR is distortion limited to 65 dB even though the peak SQNR is more than 100 dB.

3.2.2 *VCO-based ADC with phase output*

By using VCO phase instead of its frequency as the output quantity, the loop filter requirements are greatly relaxed [23]. Figure 3.7 shows a simple im-

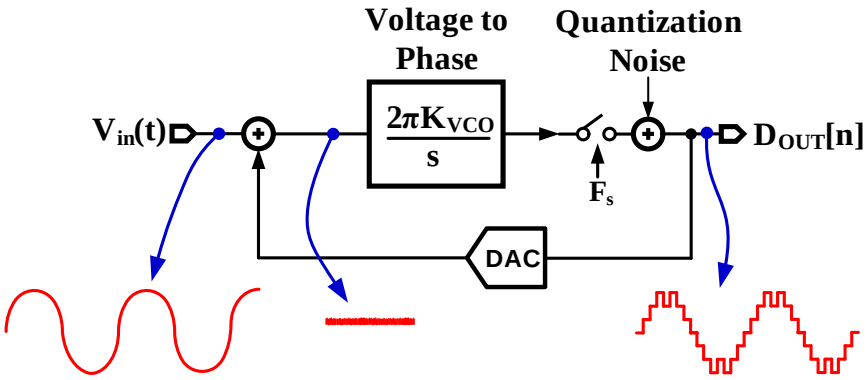

Figure 3.7: Basic structure of VCO-based ADC with phase output.

plementation of one such VCO-based ADC. Here, instead of differentiating the quantized VCO phase, it is directly used as the output quantity and is fed back to the input using a feedback DAC. Therefore, the VCO quantizer behaves like an integrator with large gain within the signal band, thereby minimizing the signal swing at the VCO input. With small signal swing at the VCO input, only a small section of the non-linear tuning is exercised which automatically improves the linearity. Using the basic structure shown in Fig. 3.7, a 4^{th}-order continuous time $\Delta\Sigma$ modulator was realized in [23]. The performance is no longer limited by the VCO tuning non-linearity and the ADC achieved an SNDR of 78 dB in a 20 MHz signal bandwidth.

3.2.3 *Residue canceling VCO-based ADC*

While the architecture in Fig. 3.7 uses feedback, a feed-forward architecture can also be used to minimize the signal swing at the input of the VCO quantizer as shown in Fig. 3.8 [24]. Here, a two-step quantizer is employed such that the

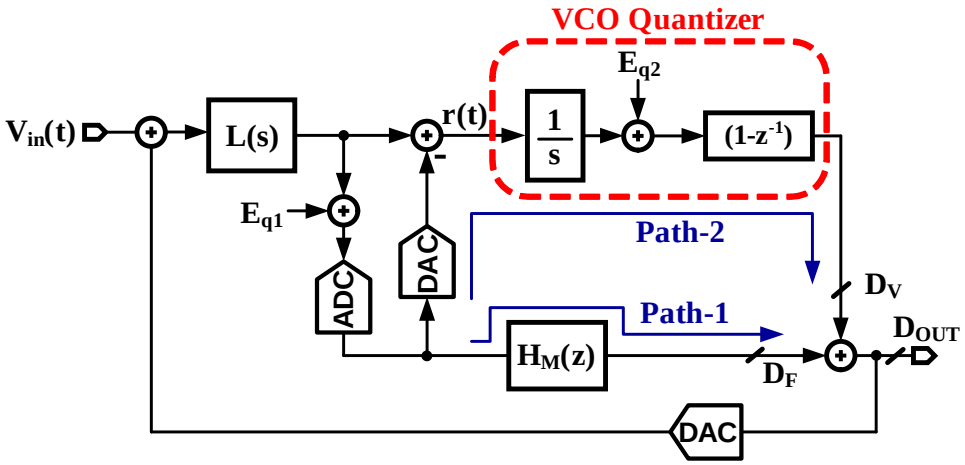

Figure 3.8: Simplified block diagram of residue canceling VCO-based ADC.

VCO-based quantizer process only the residue from the first stage. Consequently, it's input signal swing is minimized leading to a highly linear behavior. Filter, $H_M(z)$, ensures that the first stage residue has the same transfer function through the two the paths, thereby canceling it at the final ADC output. Gain mismatch between the two paths is first order noise shaped by the loop filter. Therefore, the final ADC output contains only the shaped quantization noise of the VCO-based quantizer. Using a first order loop filter, second order quantization noise shaping is obtained.

Two-step ADCs with VCO-based ADC at the second stage, similar to the quantizer in [24] have also been proposed in [25, 26]. In [25] a 5-bit flash ADC is used in the first stage followed by a second stage VCO-based ADC. In [26] a

1-1 MASH is realized with a 1st-order discrete-time $\Delta\Sigma$ in the first stage, followed by the VCO based second stage. Furthermore, multi-rate sampling is employed to maximize the benefits of the VCO-based ADC. Though both these techniques mitigate the VCO non-linearity problem by minimizing the voltage swing at the VCO, they are sensitive to variations in the VCO gain across PVT corners [24].

3.2.4 VCO-based ADC with calibration

All the VCO-based ADC architectures discussed so far require a multi-bit feedback digital-to-analog converter (DAC). Since the DAC is in the feedback path, its linearity directly determines the linearity of the entire ADC. Realizing a highly linear, multi-bit DAC is a very challenging design task and increases system complexity and typically incurs a power penalty [27]. Various calibration techniques have been successfully employed for VCO-based ADCs [28, 19, 29]. These techniques perform analog to digital conversion in an open loop manner and obviate the need for a multi-bit DAC.

In [28], foreground calibration is employed to correct VCO tuning non-linearity as shown in Fig. 3.9. When in calibration mode, the ADC is disconnected

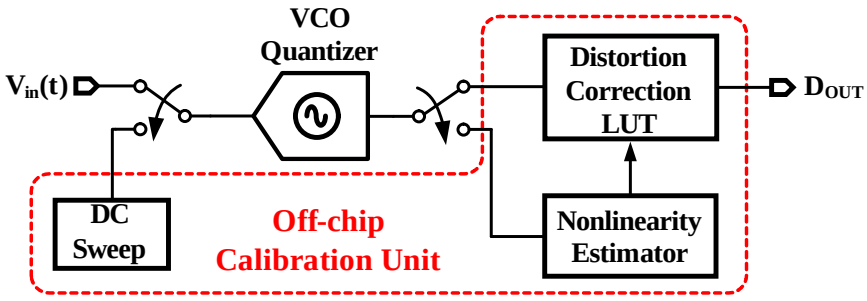

Figure 3.9: VCO-based ADC with off-chip foreground calibration.

from the signal path and different DC voltages are applied to its input. Based on

the resulting output the the non-linearity is determined and it is used to correct the output when the ADC is connected back to the signal path. While this technique improves linearity, the calibration is performed off-chip and it requires an accurate external voltage source to perform DC sweep. Furthermore, since calibration is performed in the foreground, this technique is sensitive to PVT variations.

The sensitivity to PVT variations is minimized using statistical background calibration as shown in Fig. 3.10 [19, 29]. Here, a third order polynomial is assumed

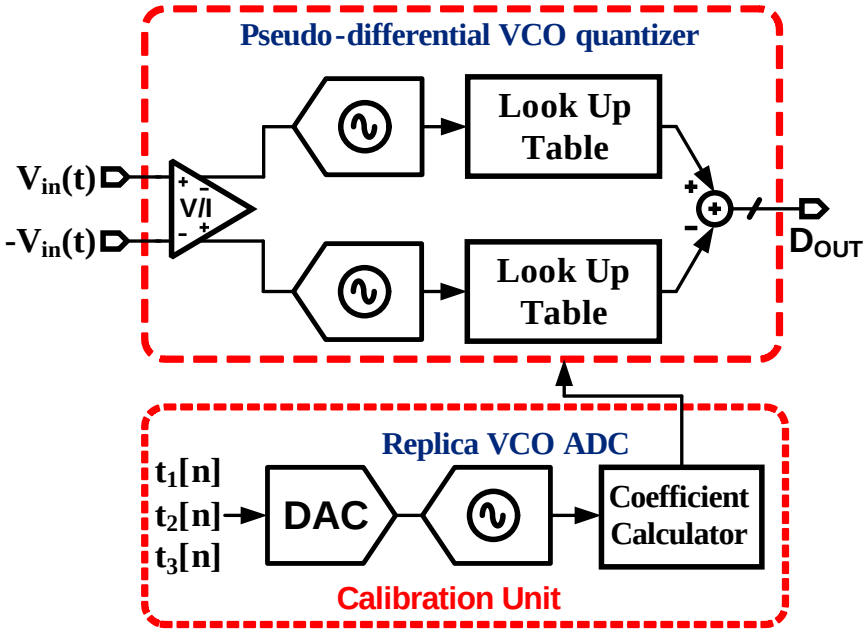

Figure 3.10: Block diagram showing background calibration of VCO-based ADC.

to represent the VCO's V-to-F transfer characteristics. Three psuedo-random sequences $t_1[n]$, $t_2[n]$ and $t_3[n]$ are applied to a replica VCO, and a calibration unit consisting of multipliers and correlators determine the coefficients of the V-to-F polynomial. The estimated coefficients are used to correct the output of the main VCO quantizer. The first version of this ADC required a high-performance, linear front-end voltage to current (V-to-I) converter which consumed significant power [19]. However, this requirement was overcome in the second version by

calibrating even the V-to-I non-linearity [29]. Though this technique effectively improves the ADC performance, the calibration unit corrects only the second and third order harmonic terms. Furthermore, the calibration unit employs a multi-bit DAC which needs to be highly linear.

In the following chapters, two new VCO-based ADC architectures are presented that simplifies the design of linear VCO-based ADCs. In the first approach, the ADC is linearized by operating it at only two points on the non-linear VCO tuning characteristics. The second approach employs a new background calibration technique to linearize the ADC. Both techniques avoid the stability issues associated with a continuous-time $\Delta\Sigma$ loop and obviate the need for a multi-bit feedback DAC. The implementation details of the first technique are discussed in the next chapter.

CHAPTER 4. LINEAR VCO-BASED ADC USING TWO LEVEL OPERATION

4.1 Proposed Architecture

The genesis of the proposed architecture can be explained using the VCO's V-to-F transfer characteristics shown in Fig. 4.1. In a conventional VCO-based

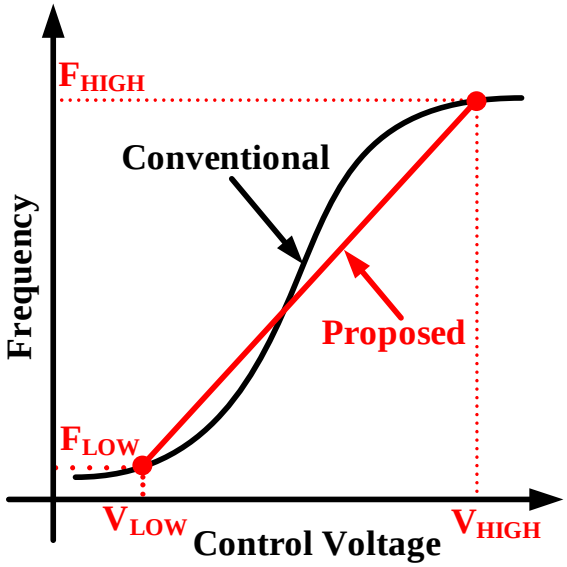

Figure 4.1: Illustration of the basic idea of the proposed architecture.

ADC, the analog voltage input spans the entire non-linear tuning curve which causes frequency output to be severely distorted. We propose to improve the linearity by exercising only two points corresponding to frequencies F_{HIGH} and F_{LOW} on the non-linear tuning curve. This two level operation results in a V-to-F

gain given by,

$$K_{VCO,2-level} = \frac{(F_{HIGH} - F_{LOW})}{(V_{HIGH} - V_{LOW})} \tag{4.1}$$

which is linear. Consequently, the detrimental impact of VCO non-linearity on the ADC performance is eliminated.

The block diagram of the proposed VCO-based ADC that takes advantage of the two-level operation discussed above is shown in Fig. 4.2 [30]. It consists

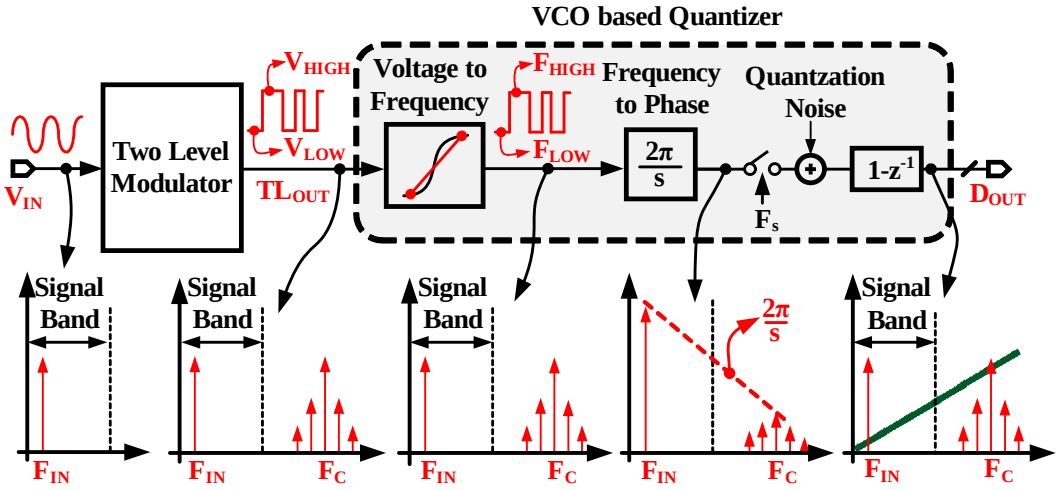

Figure 4.2: Proposed VCO-based ADC architecture.

of a two-level-modulator (TLM) that converts the analog input signal, V_{IN}, to a two level signal, TL_{OUT}. The TLM output drives the tuning port of VCO and forces it to operate at only two frequencies thus, ideally, eliminating the impact of its non-linearity. The phase sampler and the digital differentiator within the VCO quantizer form a frequency-to-digital converter that digitizes the VCO output frequency and generates the ADC output, D_{OUT}.

The representative spectra in Fig. 4.2 highlight the linear behavior and quantization noise shaping property of the proposed architecture. By an appropriate choice of TLM architecture (see Sec. 4.2), it is ensured that the two-level output contains only the input signal with no other modulation tones in the signal band.

Because VCO acts only as a V-to-F converter by mapping V_{HIGH} and V_{LOW} voltages to F_{HIGH} and F_{LOW} frequencies, respectively, it does not alter the spectrum of the TLM output. In other words, the spectrum of the VCO output frequency is only a scaled version of the TLM output. Since VCO phase (rather than its frequency) is sampled in a VCO quantizer, the spectrum of the VCO output frequency is integrated. This integration suppresses the high frequency tones relative to the signal and provides anti-aliasing. Quantization of the sampled phase introduces quantization noise. The spectrum at the final ADC output shows that the quantization noise is 1^{st}-order shaped due to the digital differentiator. Thus, by operating the VCO at only two levels, a linear VCO-based ADC is realized while retaining its noise shaping properties. The trade-offs and considerations involved with the design of two level modulator and the VCO quantizer are discussed in the following sections.

4.2 Two level modulator design considerations

Since the two level modulator is at the front-end of the proposed ADC, it needs to satisfy the linearity requirement of the entire ADC. Pulse width modulation (PWM) is used to realize the two level modulator. While PWM can effectively convert the analog input to a two level signal, the linearity of the pulse width modulated output differs widely depending on whether the input is uniformly sampled or naturally sampled. Next, we will briefly review the distortion performance of the two well known PWM schemes.

4.2.1 *Uniform sampling PWM*

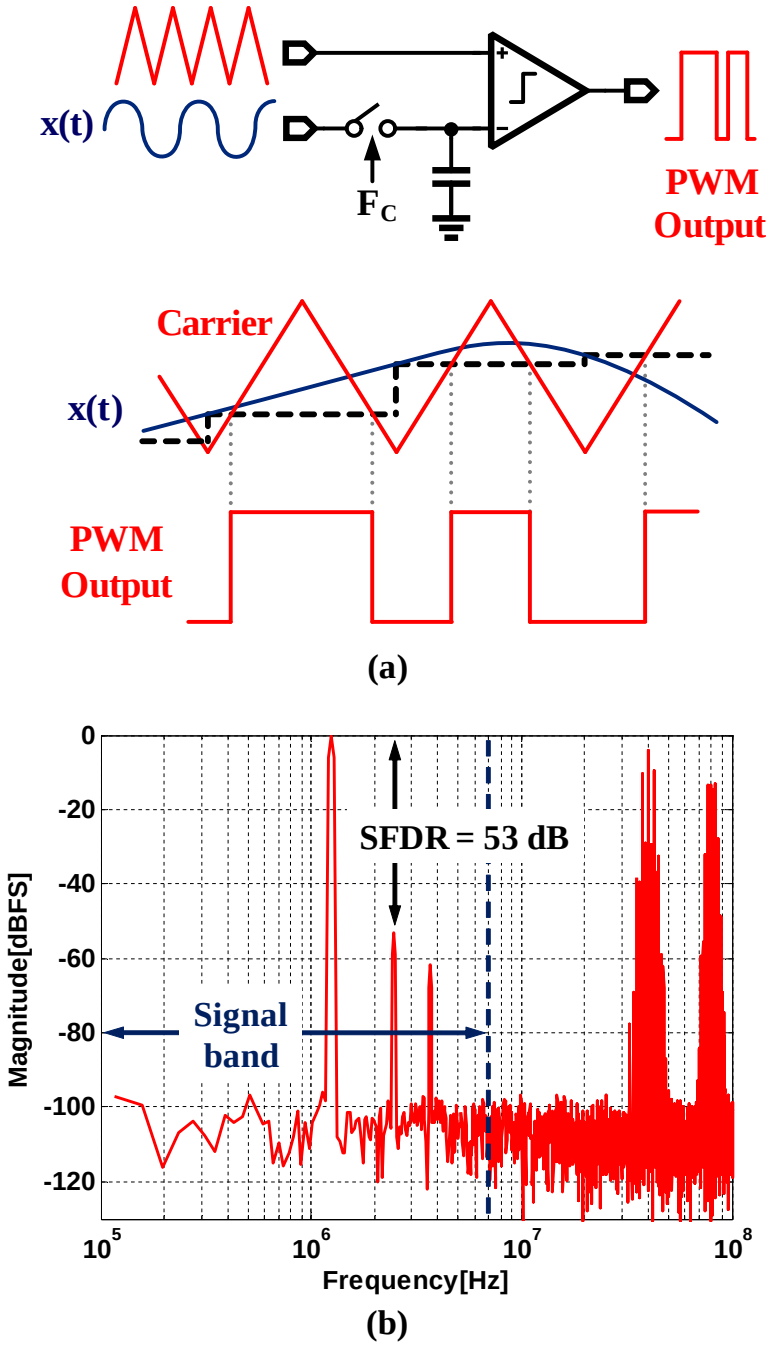

Figure 4.3: Uniform sampling pulse width modulation. (a) Basic block diagram and principle of operation. (b) Output spectrum with sinusoidal input.

Figure 4.3(a) shows a simple pulse width modulator implementation where the input, x(t), is sampled at a rate F_C and compared with a triangular wave (also called carrier) to produce a two level output [31]. The pulse width of the two level output within each carrier period is proportional to the sampled input, $x(nT_C)$ i.e.

$$T_{PWM}(n) = \frac{T_C}{2}\left(1 - \frac{x_{in}(nT_C)}{A_C}\right)$$

where $T_{PWM}(n)$ represents the pulse width during n^{th} carrier period and T_C and A_C represent the carrier period and amplitude, respectively. Since the output pulse width depends on uniformly sampled input, this PWM scheme is called uniform sampling pulse width modulation. While uniform sampling is a linear process, the resulting pulse width modulated output suffers from distortion. Figure 4.3(b) shows the output spectrum for a 1.2 MHz sinusoidal input. Within the signal band, it contains harmonic tones of the input and outside the signal band it contains higher order inter-modulation tones around the carrier frequency and its harmonics. The high frequency inter-modulation tones can be filtered out by a low-pass filter. However, harmonic tones in the signal band degrade SFDR to 53 dB. It is important to note that these harmonic tones are inherent to uniform sampling pulse width modulation and they are not a result of non-ideal circuit behavior [32].

4.2.2 Natural sampling PWM

The inherent non-linearity associated with the above architecture is eliminated by naturally sampling the input signal. Figure 4.4(a) shows a simplified block diagram of a natural sampling pulse width modulator wherein, instead of uniformly sampling the input signal, it is directly compared with the triangular

carrier. Since an explicit input sampler is absent, the output pulse width during

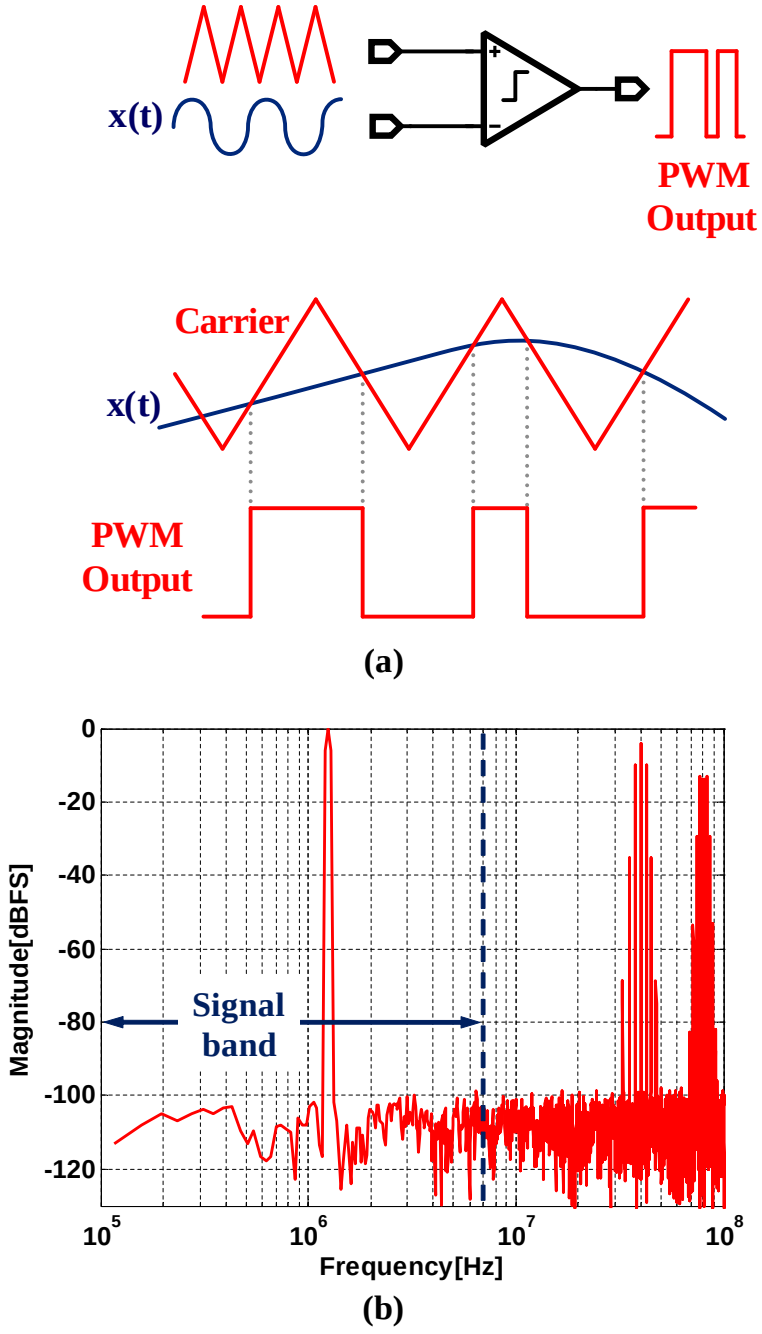

Figure 4.4: Natural sampling pulse width modulation. (a) Basic block diagram and principle of operation. (b) Output spectrum with sinusoidal input.

each carrier period depends on instantaneous values of the input when the com-

parator output undergoes a transition, as depicted by the waveforms in Fig. 4.4(a). For a sinusoidal input, the naturally sampled PWM output can be decomposed as (using the general expression derived in [32]),

$$PWM_{OUT,NS}(t) = Msin(2\pi f_{in}t) - \sum_{k=odd}\left(\frac{4}{k\pi}\sum_{n=even} J_n(\frac{k\pi M}{2})cos(2\pi(kF_C + nf_{in})\right) + \sum_{k=even}\left(\frac{4}{k\pi}\sum_{n=odd} J_n(\frac{k\pi M}{2})sin(2\pi(kF_C + nf_{in})\right) \quad (4.2)$$

where M represents the modulation index equal to the ratio of input signal amplitude to carrier amplitude and $J_n(x)$ represents the n^{th} order Bessel function of 1^{st} kind. Equation 4.2 clearly shows that the input harmonic tones are absent in natural sampling PWM output. However, like the uniform sampling PWM, it contains inter-modulation tones at even or odd multiples of f_{in}, around F_C and its harmonic frequencies. Though theoretically there are an infinite number of such inter-modulation tones, their magnitude decays rapidly with increasing 'k' and 'n' as governed by the values of the bessel function. Therefore, if F_C is set high enough, the inter-modulation tones that extend into the signal band correspond to large values of 'n' and have negligible impact on the targeted linearity. The simulated output spectrum for a 1.2 MHz sinusoidal input shown in Fig. 4.4(b) confirms the absence of harmonic tones. Because natural sampling PWM is inherently linear and exhibits better distortion performance, it is employed in this work.

4.2.3 Two level modulator implementation

The natural sampling PWM shown in Fig. 4.4(a) has simple implementation and is inherently linear, however, non-ideal circuit behavior introduces distortion. For example, in the single ended implementation shown in Fig. 4.4(a), the com-

parator input common mode varies with the amplitude of input signal and the triangular carrier. Consequently, its transition delays become signal dependent re-

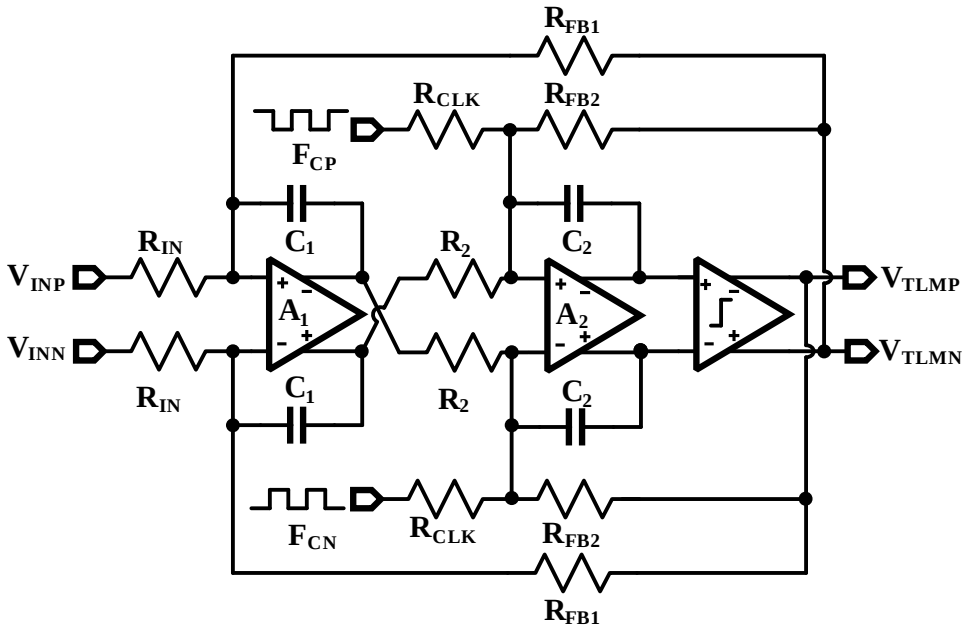

Figure 4.5: Block diagram of a fully differential two level modulator.

sulting in distortion. Simulations indicated that the linearity of this single-ended implementation is limited to about 40 dB. Furthermore, the triangular carrier needs to be generated on-chip since providing it from an off-chip source would render this architecture not very useful.

Figure 4.5 shows the complete block diagram of the two level modulator used in the proposed ADC. It consists of a second order loop filter realized with two active-RC integrators, and a comparator. The second integrator along with the comparator realize natural sampling pulse width modulator. Triangular carrier is generated by integrating the square wave carrier clock at the second integrator [33]. Because the implementation is fully differential, the input common mode of the comparator is independent of the input signal. Consequently, atleast to a first order, the comparator transition delays are independent of input signal and the

carrier thereby improving the overall linearity. Any residual distortion either due to the comparator or due to non-ideal carrier is suppressed by the loop filter. The simulated transistor level output spectrum, shown in Fig. 4.6, indicates that the linearity of this stage is about 85 dB. The circuit implementation details of the operational amplifiers and comparator are discussed in Section 5.1.

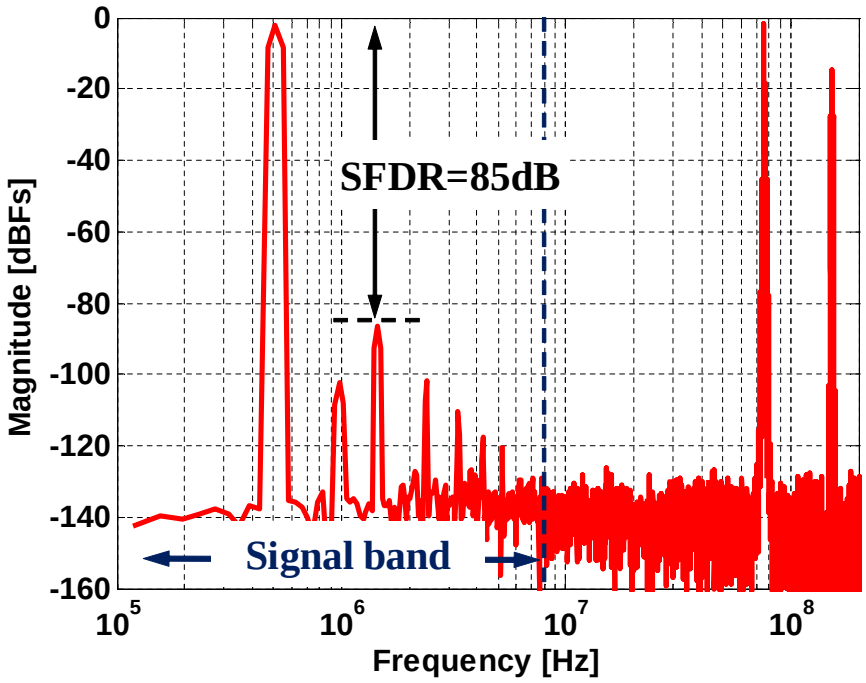

Figure 4.6: Simulated two level modulator output spectrum.

At this point it is important to identify difference between the architecture in Fig. 4.5 and a 2^{nd}-order 1-bit continuous time $\Delta\Sigma$ modulator. The difference lies in the behavior of the last stage in each modulator. The last stage in a $\Delta\Sigma$ modulator consists of a 1-bit quantizer which would introduce quantization noise. Therefore a large oversampling ratio would be required to push the quantization noise out of the signal band and achieve good signal to noise ratio (SNR). On the contrary, since natural sampling PWM is used in Fig. 4.5, there is no source of quantization

noise. Therefore good SNR can be achieved with reasonably low oversampling ratios. For example, while the two level modulator achieves better than 78 dB SNR with an oversampling ratio of 8, the SNR of a 2^{nd}-order 1-bit $\Delta\Sigma$ modulator is limited to only around 40 dB [22]. Obviously, the $\Delta\Sigma-$ modulator would directly give out digital output, but the two level modulator output needs to be processed by a VCO quantizer to get the digital bits.

4.2.4 Choice of carrier frequency

The choice of carrier frequency, F_C, in Fig. 4.5 is governed both by the characteristics of the two level modulator and the VCO quantizer. For the simple natural sampling PWM (see Fig. 4.4(a)), as discussed F_C should be set high enough such that the magnitude of the inter-modulation tones is negligible within the signal band. In the presence of negative feedback loop around the pulse width modulator as shown in Fig. 4.5, additional distortion terms are introduced [34]. For a given loop filter order, the magnitude of these additional distortion depends on the relative values of signal bandwidth and F_C, such that higher F_C results in lower distortion. These factors set a lower bound on F_C. Simulations indicted that $F_C \geq 75$ MHz is sufficient to achieve better than 75 dB distortion. While the two level modulator sets the lower bound, the upper bound on F_C comes from the characteristics of the VCO-quantizer as discussed in Sec. 4.3.1.

When the two level modulator output is sampled by the VCO quantizer, the inter-modulation tones present around the sampling frequency, F_S, and its harmonics alias into to the signal band. However, as discussed in Sec. 4.1, since the VCO quantizer samples the VCO phase, high frequency inter-modulation tones are suppressed relative to the signal before being sampled, thereby minimizing the

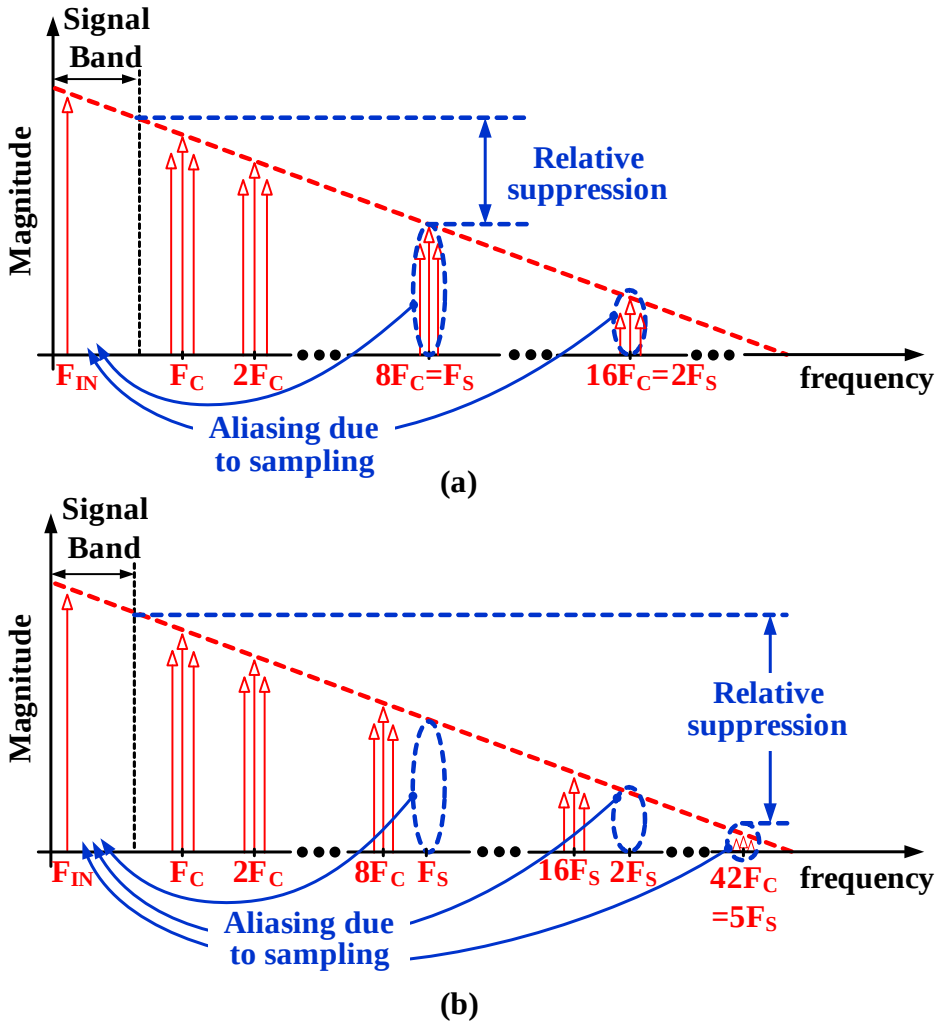

Figure 4.7: Aliasing of inter-modulation tones. (a) Carrier frequency is harmonically related to sampling frequency. (b) Carrier frequency is harmonically not not related to sampling frequency.

ill-effects of aliasing. Tones at higher frequencies are suppressed to a greater extent as shown in Fig. 4.7(a). If F_C and F_S are not harmonically related, the tones that alias into the signal band correspond to very high frequencies and are therefore greatly attenuated. For example, if F_C = 80 MHz and F_S = 640 MHz, inter-modulation tones around the 8^{th} harmonic of F_C(= 640 MHz) alias into the signal band as shown in Fig. 4.7(a). However, if F_S is not an integer multiple of F_C

(F_C = 76.2 MHz, F_S = 640 MHz), the inter-modulation tones that alias into the signal band correspond to 3.2 GHz, which is much higher than the sampling frequency of 640 MHz. Consequently, these tones are attenuated to a greater extent as depicted in Fig. 4.7(b). Thus with the right choice of F_C and F_S, benefits due to the anti-aliasing property of VCO-based quantizer can be maximized.

4.3 VCO quantizer design considerations

4.3.1 VCO quantizer response time

The upper bound on F_C is set by the speed with which VCO quantizer responds to a two level input. Until now the V-to-F conversion within the VCO is assumed to be instantaneous. However, in practice this conversion takes a finite time due to the limited bandwidth of the VCO. To gain more insight, consider a simple current starved VCO architecture shown in Fig. 4.8(a). The input volt-

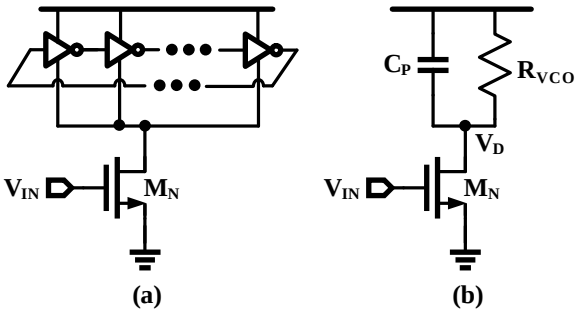

Figure 4.8: Current starved VCO. (a) Block diagram. (b) Equivalent model.

age controls the current through transistor, M_N, which in turn changes oscillation frequency. Figure 4.8(b) shows an equivalent model of the current starved VCO, where C_P represents the parasitic capacitance at the drain node and R_{VCO} represents the equivalent resistance looking into the inverter ring. Capacitance C_P and

R_{VCO} introduce a parasitic pole, ω_p, and modify the VCO transfer function to,

$$H_{VCO}(s) = \frac{K_{VCO}}{1 + \frac{s}{\omega_p}} \tag{4.3}$$

and

$$\omega_P = \frac{1}{C_P R_{VCO}} \tag{4.4}$$

where K_{VCO} represents the ideal V-to-F transfer characteristic. Pole at ω_p sets the VCO bandwidth and modifies its response to the two level input signal as shown in Fig. 4.9. The response of an ideal VCO is depicted in Fig. 4.9(a). The output frequency transitions are instantaneous and the VCO operates only at F_{HIGH} and F_{LOW} resulting in the desired linear behavior. Figure 4.9(b) depicts the response of a practical VCO. Due to finite VCO bandwidth, the frequency transitions are not instantaneous and it takes a finite time for the output frequency to transition from F_{HIGH} to F_{LOW} and vice-versa. During time period 1, the input pulse width is wide enough for the VCO to complete the transition. However, during time period 2, due to the narrow input pulse, the VCO fails to reach F_{HIGH} and the final operating point depends on the input pulse width. Thus, depending on the input pulse width, different points on the K_{VCO} curve are excited leading to non-linear behavior. The linearity improvement of the proposed ADC therefore depends on the relative magnitudes of VCO bandwidth, ω_p, and the minimum input pulse width, T_{MIN}. For the proposed two level modulator with sinusoidal input, T_{MIN} is given by

$$T_{MIN} = \frac{T_C}{2}\left(1 - \frac{A_{IN}}{A_C}\right) \tag{4.5}$$

where A_{IN} and A_C represent the amplitudes of the input and the carrier, respectively and T_C represents the carrier period. The simulated SFDR as a function of the product $\omega_P T_{MIN}$ is shown in Fig. 4.10. For very small $\omega_P T_{MIN}$, since the VCO output frequency fails to reach the desired final value in every carrier period,

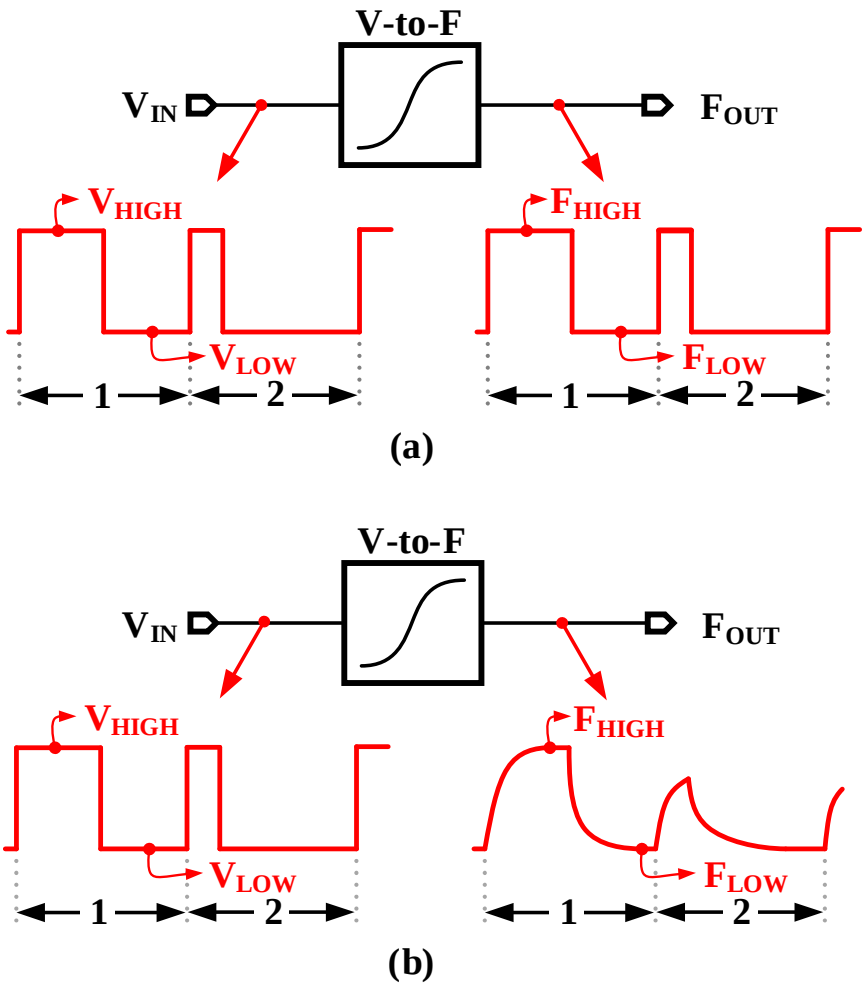

Figure 4.9: VCO response to a two level input. (a) Ideal VCO response. (b) Practical VCO response.

the linearity degrades to that of a conventional open loop VCO quantizer. The linearity improves as ω_P is increased with respect to T_{MIN} and to achieve an SFDR better than 75 dB, $\omega_P > (4/T_{MIN})$ is required. From Eq. 4.5, for $F_C = 80$ MHz and -1.5 dB input, the required VCO bandwidth is about 650 MHz. If F_C is increased, the required VCO bandwidth also increases, thus setting the upper bound on F_C.

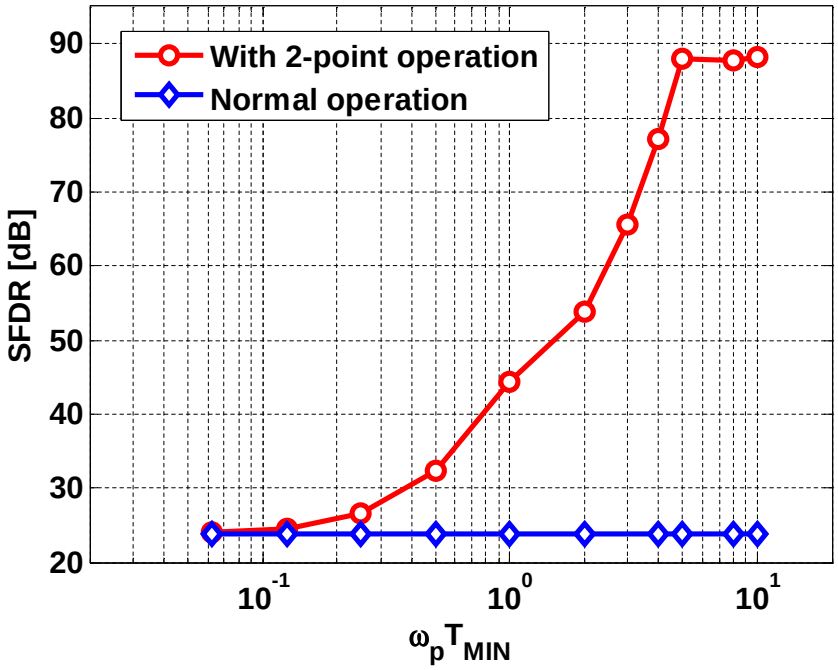

Figure 4.10: Simulated SFDR vs. $\omega_P T_{MIN}$.

4.3.2 VCO quantizer architecture

Wide bandwidth VCO can be realized by directly switching the supply voltage of the inverter ring as shown in the Fig. 4.11. When the input is high, V_{HIGH}

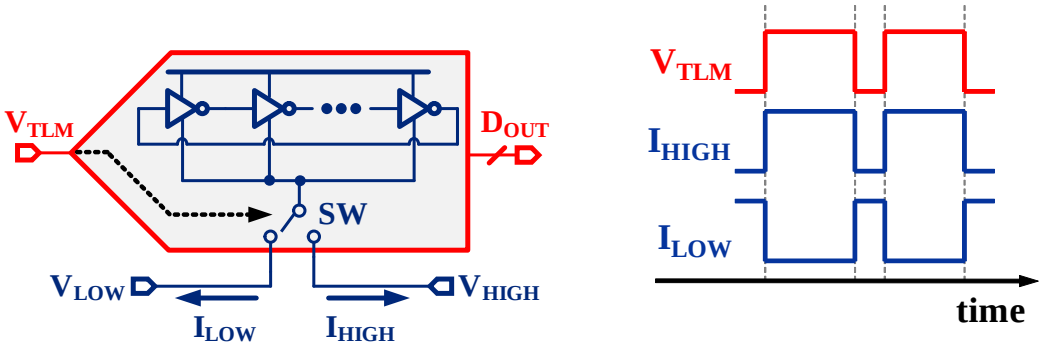

Figure 4.11: Schematic and waveforms for a single ended wide bandwidth VCO.

is connected to the ring oscillator and when it is low, V_{LOW} is connected to the oscillator. The signal path pole, ω_p, for this VCO is given by,

$$\omega_P = \frac{1}{C_P(R_{VCO}||R_{SW})} \tag{4.6}$$

where R_{SW} represents the switch resistance. By reducing the switch resistance, R_{SW}, the bandwidth can be maximized. The representative waveforms, for currents I_{HIGH} and I_{LOW} drawn from V_{HIGH} and V_{LOW}, respectively, are also shown in Fig. 4.11, indicating that the currents have the same profile as the input two level voltage signal. The sharp I_{HIGH} and I_{LOW} current pulses impose stringent speed and slewing requirements on the buffers that drive V_{HIGH} and V_{LOW}.

The high speed and slewing requirements are relaxed using a pseudo-differential quantizer architecture as shown in Fig. 4.12. The positive and negative half cir-

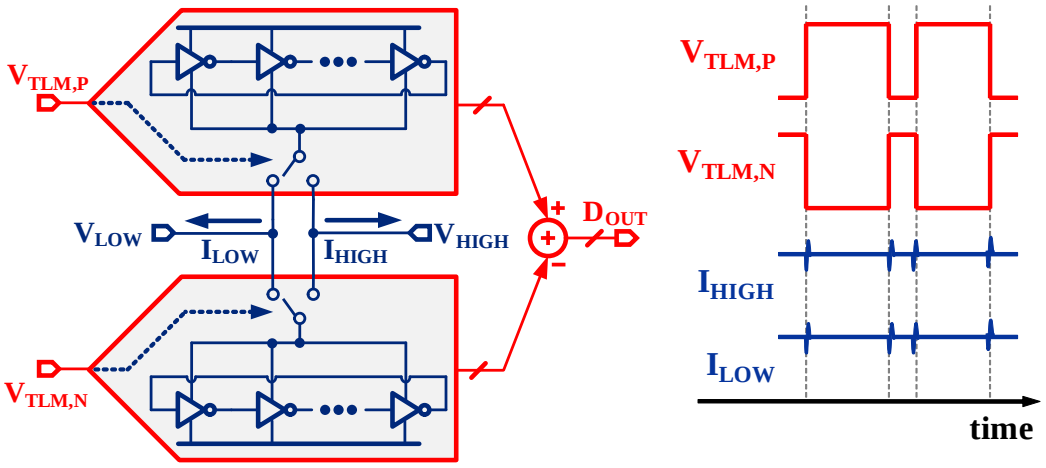

Figure 4.12: Schematic and waveforms for a pseudo-differential wide bandwidth VCO.

cuits process the complimentary two level signals denoted by $V_{TLM,P}$ and $V_{TLM,N}$, respectively. The digital outputs from the positive and negative half circuits are subtracted to get the final output, D_{OUT}. Since the two level input signals are complimentary, V_{HIGH} and V_{LOW} are always connected to one of the two half circuits. Therefore, to an extent that the two half-circuits match, currents I_{HIGH}

and I_{LOW} remain constant thereby relaxing the speed and slewing requirements on the V_{HIGH} and V_{LOW} buffers. Other benefits of pseudo-differential architecture include improved SNR and linearity. Since the signal in each half circuit is correlated, signal power at the ADC output increases by 6 dB. However, due the random nature of noise, the noise power increases by only 3 dB. This results in a net 3 dB improvement in SNR at the ADC output. Furthermore, since the half circuits processes complimentary signals, the even order harmonic terms from each half circuit cancel at the final ADC output resulting in improved linearity.

4.4 Circuit Design Details

4.4.1 Operational amplifier and comparator

The circuit design details of the loop filter and comparator used in the two level modulator (TLM) are discussed here. The TLM loop filter is implemented with two active-RC integrators since they achieve better linearity than a $G_M - C$ integrator. Figure 4.13 shows the operational amplifier used in the active-RC

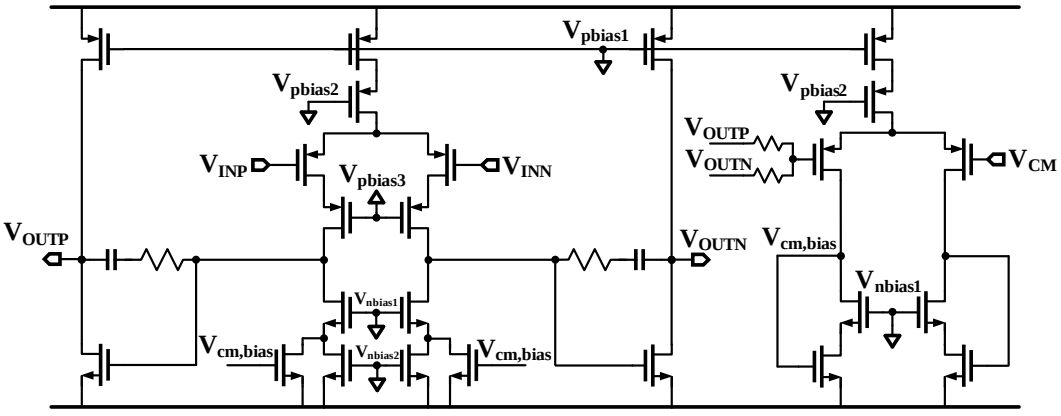

Figure 4.13: Opamp architecture used in NSPWM.

integrator. It employs a two stage Miller compensated architecture wherein the output common mode is set by controlling the current through the first stage. The

Table 4.1: Performance summary of the operational amplifier

Supply Voltage	1.3 V
DC Gain	62 dB
Unity Gain Bandwidth	1.4 GHz
Power	0.9 mW

performance of the operational amplifier is summarized in Table 4.1.

The comparator architecture is shown in Fig. 4.14. It consists of two gain

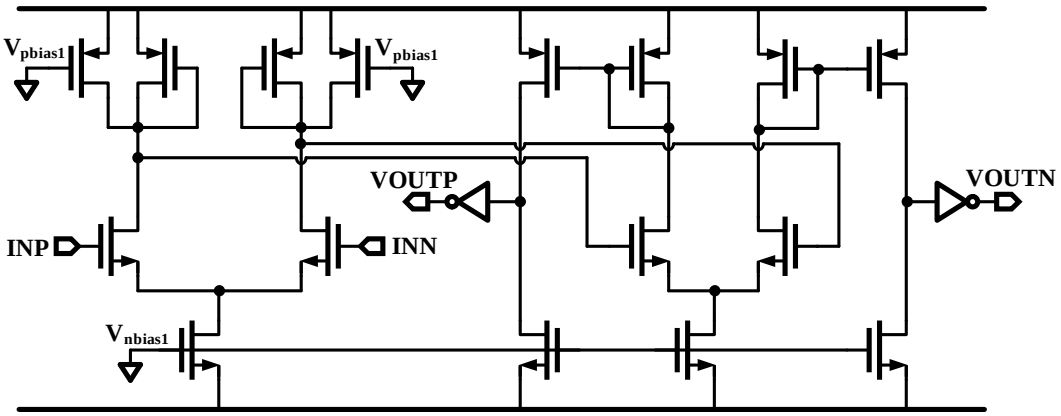

Figure 4.14: Comparator architecture used in NSPWM.

stages. The first stage acts as a pre-amplifier and provides additional gain which helps improve the sensitivity of the comparator. The second stage output is passed through inverters to obtain rail-to-rail output swing. Operating from a 1.3 V supply and with 80 MHz carrier frequency, the comparator consumes about 0.3 mW power.

4.4.2 VCO phase sampler

Phase samplers are used within the VCO quantizer to sample and quantize the VCO phase. Figure 4.15(a) shows a conventional implementation where the ring-VCO phases denoted by P_{H1}, P_{H2} etc., are sampled by an array of sense-amp flip-flops [23]. Here, quantization is performed by comparing these phases to a reference voltage, V_{REF}. If V_{REF} is not at the center of the voltage swing of the VCO phases, it results in non-uniform quantization steps [19]. This is elucidated with the waveforms in Fig. 4.15(b), where phases P_{H1}, P_{H2}, P_{H3} and P_{H4} corresponding to four consecutive delay stages in the ring-VCO. Since V_{REF} is at the lower half of the phase swing, the quantization steps arising from the phases going low, such as P_{H2} and P_{H4} are wider than the quantization steps arising from the phases going high such as P_{H1} and P_{H3}. In practice, since the voltage swing at these phases varies with the input signal, it is difficult to set V_{REF} at the center. Though error due to non-uniform quantization is first order noise shaped by the digital differentiator that follows the phase sampler, it can be eliminated with an improved phase sampler. Figure 4.16(a) shows the improved phase sampler used in this design. Instead of inverters, pseudo-differential delay cells are used in the ring VCO. Furthermore, V_{REF} is eliminated by feeding the sense-amp flip-flops with complimentary phases available from the pseudo-differential delay cells. Since in this implementation quantization steps are defined by two complimentary phases, the resulting quantization steps are uniform as depicted by the waveforms in Fig. 4.16(b).

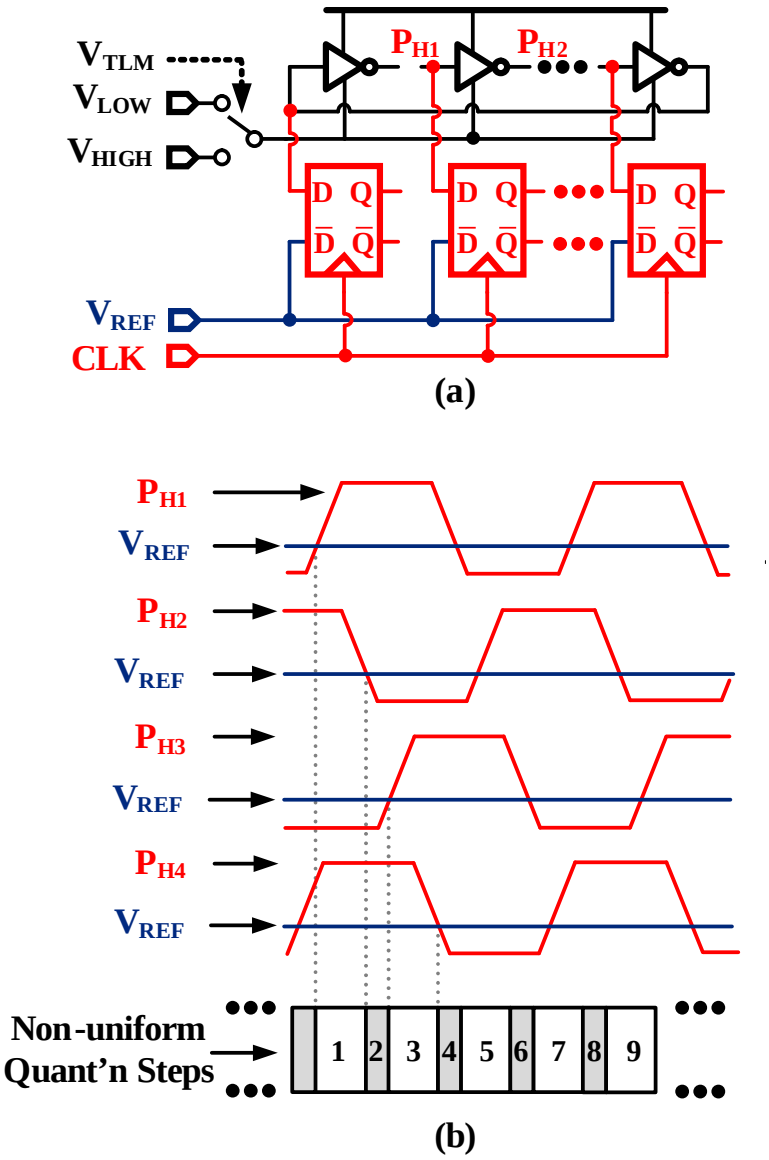

Figure 4.15: Conventional phase sampler. (a) Simplified block diagram. (b) Phase waveforms depicting non-uniform quantaization steps.

4.4.3 Complete VCO Quantizer

Figure 4.17 shows the complete VCO quantizer architecture. As discussed earlier, it consists of two identical half circuits each digitizing complimentary two

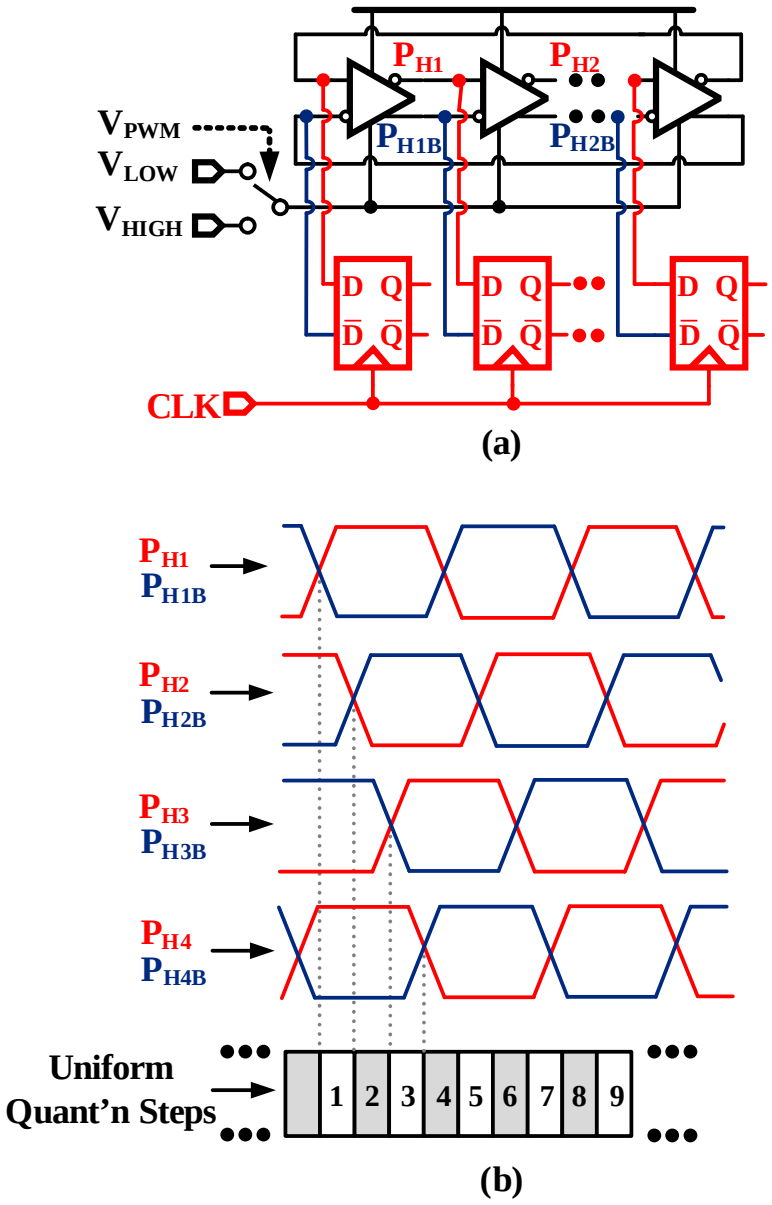

Figure 4.16: Proposed pseudo-differential phase sampler. (a) Simplified block diagram. (b) Phase waveforms depicting uniform quantization steps.

level input signals, V_{TLMP} and V_{TLMN}, generated by the two level modulator. Each half circuit consists of a 16-stage ring oscillator formed with pseudo-differential delay cells. The pseudo-differential delay cells are realized using resistively coupled

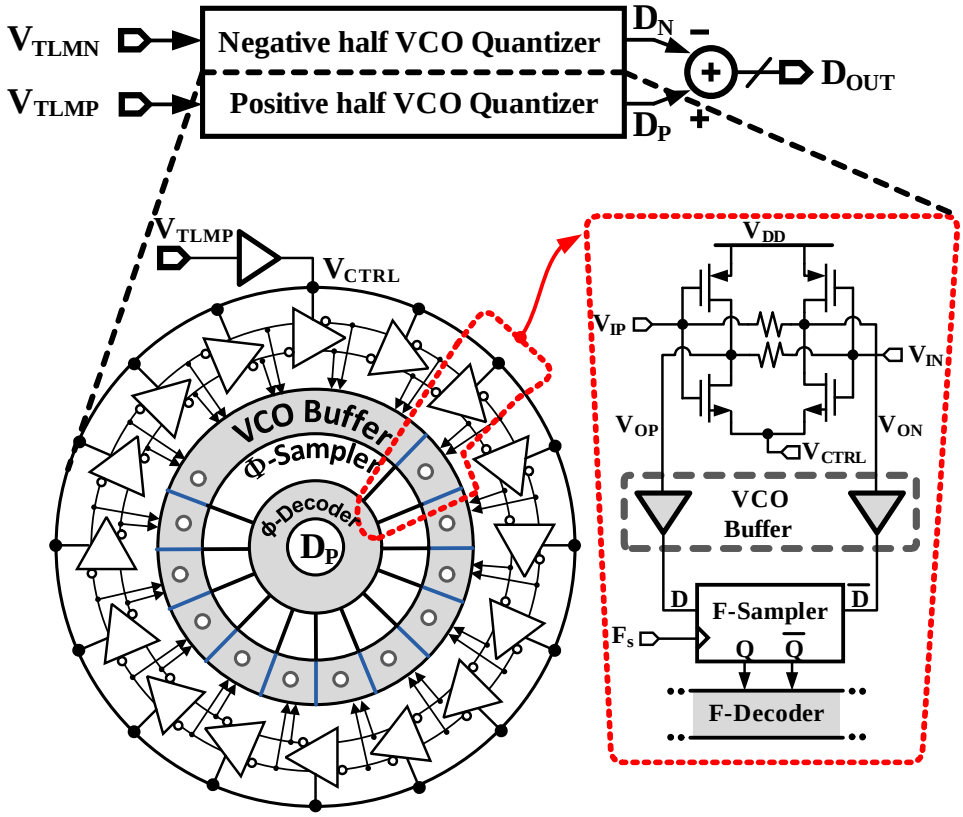

Figure 4.17: Complete VCO quantizer architecture.

inverters as shown in Fig. 4.17. A buffer stage isolates the VCO from kick-back noise caused by phase sampler. The sense-amp flip-flop used in the phase sampler is identical to the one discussed in [35]. The phase decoder (Φ-decoder) maps the sampled VCO phase from the positive and negative half circuits to binary numbers, D_P and D_N, respectively. Finally, the outputs of the two half circuits are digitally subtracted to get the ADC output, D_{OUT}.

4.5 Measured Results

The prototype chip was fabricated in 90nm CMOS process and it occupies an active area of about 0.1mm^2. Figure 4.18 shows the die micro-graph of the prototype chip. The chip was packaged in a 48 pin TQFP package.

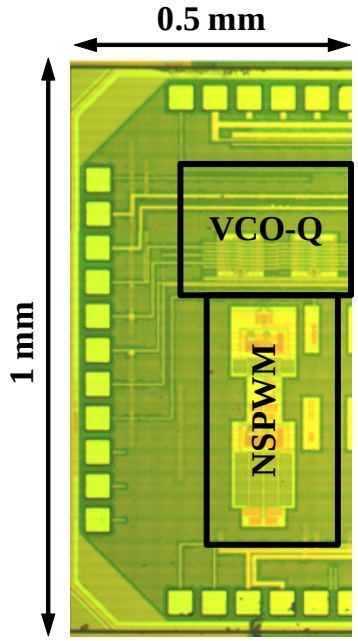

Figure 4.18: Die micrograph.

The analog building blocks such as the two level modulator operate from a 1.3 V supply voltage and all the digital blocks including the VCO quantizer operate from a 1 V supply. The sampling clock and carrier clock are provided using external clock sources. The sampling clock frequency, F_S, and the carrier frequency, F_C, are set to 640 MHz and 76.2 MHz, respectively. This choice of F_S and F_C ensures that they are not harmonically related and therefore suppress the aliasing higher order inter-modulation tones to a greater extent as discussed in Sec. 4.2.4.

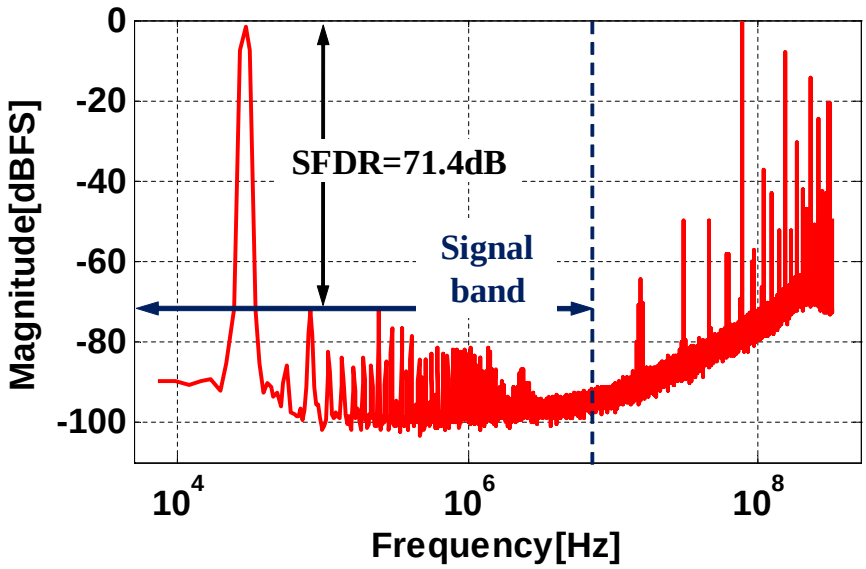

Figure 4.19: Measured output spectrum.

The measured output spectrum of the prototype ADC for a $1.15V_{p-p,diff}$ input is shown in Fig. 4.19. A 2^{18} point FFT was averaged 16 times to plot this spectrum. An excellent SFDR of 71.4 dB is observed which validates the effectiveness of the proposed two-level operation. Tones observed at frequencies outside the signal band correspond to the carrier frequency and aliased higher order inter-modulation tones of the two-level signal. These tones should be filtered by the digital decimation filters that follow the $\Delta\Sigma$ modulator. Harmonic tones, though below -71.4 dBFs, are also observed within the signal band. Interestingly, these tones extend up to very high orders and they are unlikely to be caused by VCO non-linearity. Simulations indicated that these tones are most likely caused by noise on the supply and references caused due to excessive bond-wire inductances and insufficient on-chip decoupling capacitors.

Figure 4.20(a) shows the simulated output spectrum with a 2.5 nH bond-wire

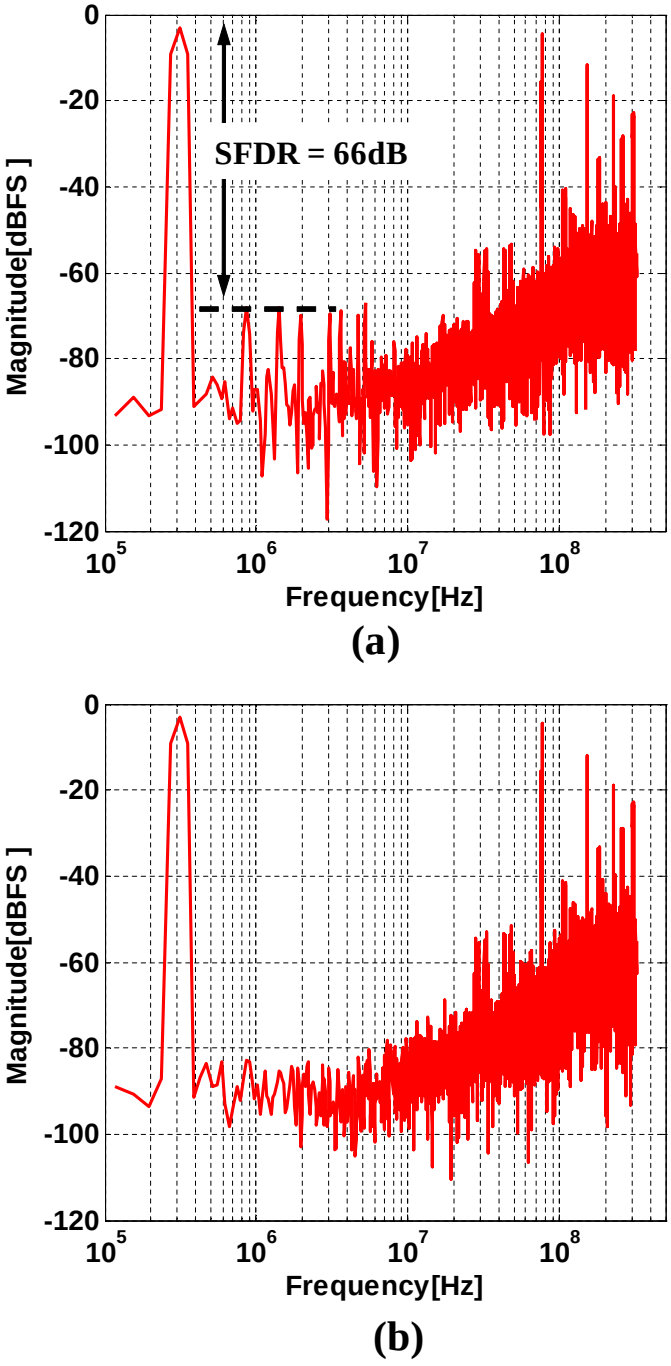

Figure 4.20: Simulated output spectrum with supply parasitics. (a) 2.5nH bond-wire inductance. (b) 0.5nH bond-wire inductance.

inductance. Since 1mm × 1mm die is relatively much smaller than the 7mm × 7mm 48-pin package, 2.5 nH bond-wire inductance is a reasonable estimate.

This output spectrum shows similar in-band higher order harmonic tones that degrade the SFDR to 66 dB. However, if the bond-wire inductance is reduced to 0.5 nH, the in-band harmonic tones disappear. These simulations indicate that the performance of this ADC can be improved further by using a different package with lower parasitics or by adding more on-chip decoupling capacitors on the sensitive nodes. The measured SNDR and SNR, over 8 MHz signal bandwidth, for various input signal amplitudes is shown in Fig. 5.23. The ADC achieves a peak SNDR and SNR of 59.1 dB and 63.1 dB, respectively and the dynamic range is 65.6 dB.

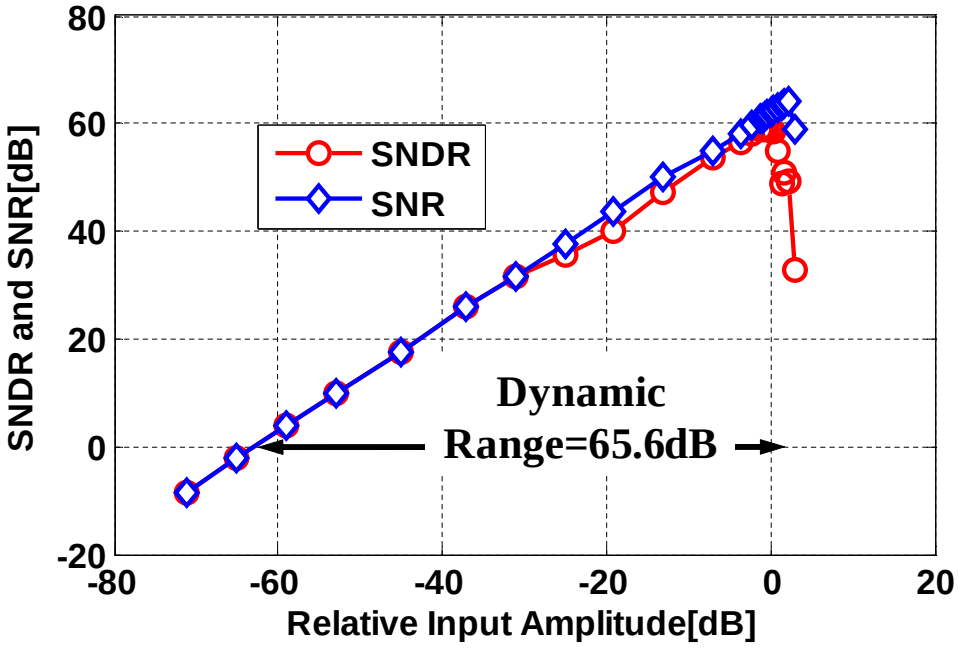

Figure 4.21: Measured SNDR and SNR vs. input amplitude.

The ADC consumes a total power of 4.3 mW. The analog blocks consume 2.3 mW while the digital blocks consume 2 mW. The figure of merit (FOM) cal-

culated as,

$$\text{FOM} = \frac{\text{TotalPower}}{2 \times \text{Bandwidth} \times 2^{\text{ENOB}}} \tag{4.7}$$

is found to be 366 fJ/conv-step. Table 4.2 summarizes the performance of this

Table 4.2: Performance summary and comparison

Reference	[17]	[31]	[23]	[24]	[29]	This Work
Technology	0.13 μm	65 nm	0.13 μm	90 nm	65 nm	90 nm
Bandwidth [MHz]	10	20	20	10	20.3	8
Sampling rate [MHz]	950	250	900	600	1300	640
Multi-bit feedback DAC	Yes	Yes	Yes	Yes	No	No
Calibration	No	No	Yes	No	Yes	No
SNR [dB]	86	62	81	80.5	70	63
SNDR [dB]	72	60	78	76.6	69	59.1
Power [mW]	20	10.5	87	16	11.5	4.3
FOM [fJ/conv-step]	500	319	330	145	123	366
Active area [mm^2]	0.42	0.15	0.45	0.36	0.075	0.1

ADC and compares it with other state of the art time-based ADCs. It indicates that this ADC achieves good linearity and FOM without using either a multi-bit feedback DAC or calibration.

CHAPTER 5. BACKGROUND CALIBRATION OF VCO-BASED ADC

Though the VCO-based ADC presented in the last chapter is highly linear, it requires a front-end two level modulator to convert the analog input signal to a two level signal. In addition to consuming more than half the total ADC power, it needs to be as linear as the entire ADC. Furthermore, the two level modulator introduces additional thermal noise and degrades the figure of merit. Since the ADC employs analog building blocks such as op-amps and comparators, it does not fully benefit from the 'digital' nature of the VCO-based ADC. Therefore, it is desirable to improve the linearity of VCO-based ADCs without using such front-end two level modulators. In this chapter a background calibration architecture is presented to linearize the VCO-based ADC. Contrary to other background calibration architectures that assume a third order polynomial to represent the V-to-F tuning characteristic [19, 29], the proposed architecture makes no such assumption about the V-to-F characteristics and it corrects all the non-linear terms. In addition to having a simple implementation, it results in faster convergence time.

5.1 Proposed Architecture

Consider the system shown in Fig. 5.1(a) with an input to output transfer function given by,

$$y_{out}(t) = f(x_{in}(t)) = a_0 + a_1 x_{in}(t) + a_2 x_{in}^2(t) + \cdots + a_n x_{in}^n(t) \qquad (5.1)$$

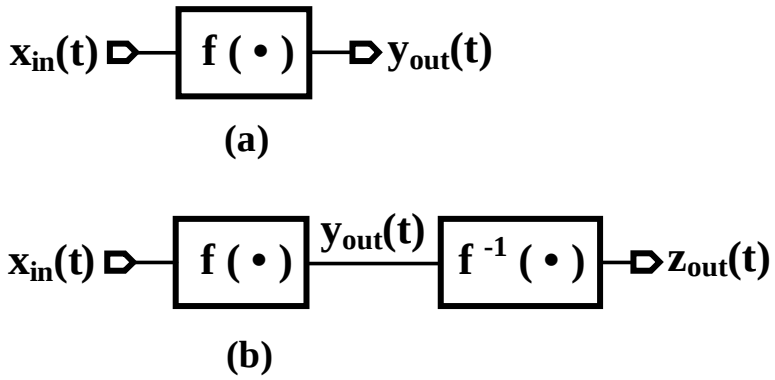

Figure 5.1: Figure depicting the basic idea. (a) A general non-linear system. (b) Linear system realized with cascaded inverse systems.

where $x_{in}(t)$ and $y_{out}(t)$ represent the input and output, respectively, and a_0, a_1, ..., a_n are constants. If any one of the constants a_2, a_3, ..., a_n has non-zero value, it results in harmonic distortion. However, if this system is cascaded with a second system that has an inverse transfer function, as shown in Fig. 5.1(b), the non-linearity is eliminated. The final output of the cascaded system is given by,

$$z_{out}(t) = f^{-1}(y_{out}(t)) = (f^{-1}(f(x_{in}(t))) = x_{in}(t) \tag{5.2}$$

which is linear and distortion free. The above linearizing technique forms the basis of the proposed architecture.

Figure 5.2 shows the simplified block diagram of the proposed architecture. The VCO converts the analog input voltage, V_{IN}, to frequency, F_{VCO}. The phase-sampler, encoder and digital differentiator realize a frequency-to-digital (F-to-D) converter and convert F_{VCO} to a 5-bit digital output, D_{VCO}. Like in a conventional VCO-based ADC, due to the non-linear V-to-F conversion, D_{VCO} suffers from significant distortion. The linearizer corrects this distortion by introducing an inverse V-to-F transfer function in the signal path as discussed earlier. To do so, the linearizer maps D_{VCO} to a non-linearity corrected output, D_{LIN} using a

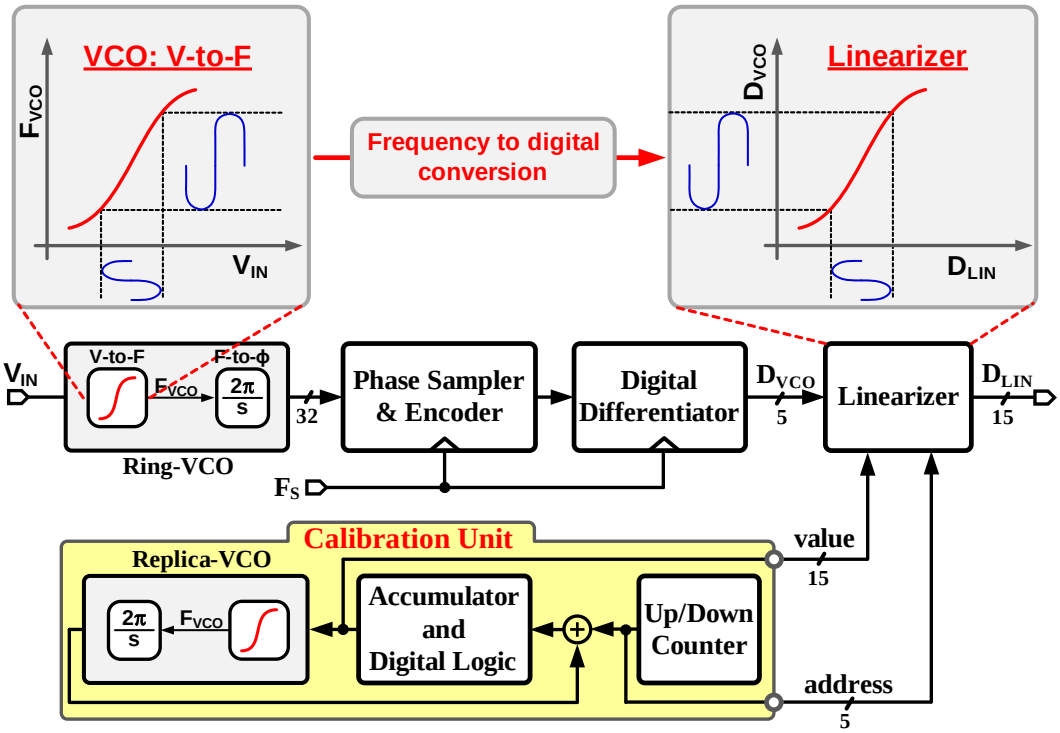

Figure 5.2: Simplified block diagram of the proposed architecture.

look-up-table (LUT). The calibration unit runs in the background and builds the inverse V-to-F transfer function using a replica-VCO. Since the calibration unit runs continuously, it tracks variations in process, voltage, and temperature thereby resulting in a system that is robust to such errors. A deterministic background calibration is employed in this ADC. It's implementation details are discussed in the following section.

5.1.1 Proposed Calibration Unit

To understand how the calibration unit determines the correct LUT contents, we note that in the VCO-based ADC shown in Fig. 5.2, the non-linearity is

mainly introduced in V-to-F conversion. However, unlike the V-to-F conversion, frequency-to-digital (F-to-D) conversion is linear. Therefore, for a given digital output, D_{VCO}, the VCO oscillation frequency, F_{VCO} can be precisely determined. For example, consider N-delay stage VCO-based ADC and the associated waveforms shown in Fig. 5.3. Here, the register and counter represent the frequency

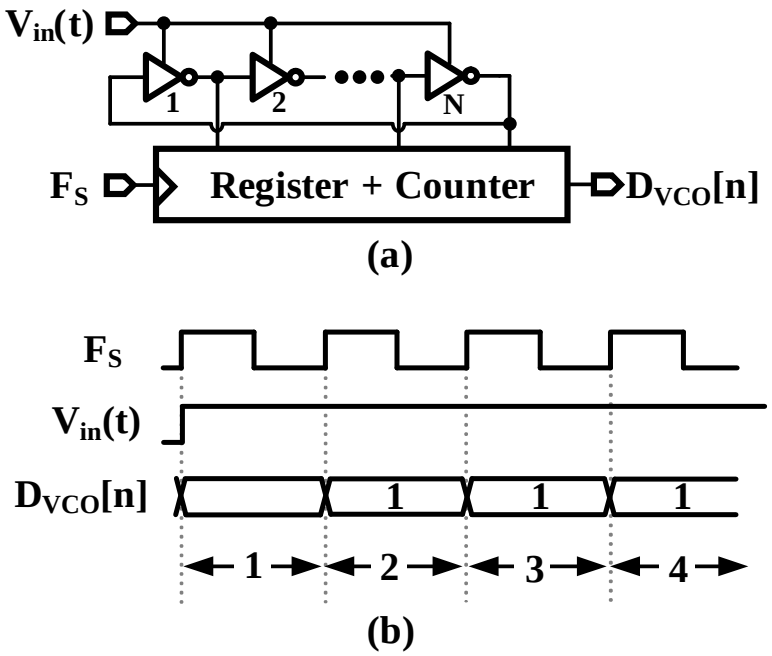

Figure 5.3: N-delay stage ring VCO. (a) Simplified block diagram. (b) Waveforms depicting $D_{OUT}[n] = 1$.

to digital converter. $V_{IN}(t)$ is a constant, which is set such that $D_{VCO} = 1$. It indicates that during every clock period, T_S, of the sampling clock, exactly one delay stage undergoes transition. This implies that the delay of each stage is T_S. Therefore, the frequency of oscillation of this N-delay stage ring-VCO is given by,

$$F_{VCO} = \frac{1}{2Nt_d} = \frac{F_S}{2N} \tag{5.3}$$

where t_d represents the nominal delay of each stage. In general, the relationship between the VCO oscillation frequency and the digital output is given by,

$$F_{VCO} = \left(\frac{F_S}{2N}\right) D_{VCO}. \tag{5.4}$$

By determining the input voltage that causes the VCO to oscillate at F_{VCO}, the inverse V-to-F transfer function can be constructed. This is done in the calibration unit by forcing a replica-VCO to oscillate at F_{VCO} and the corresponding input voltage, in digital form, is stored in the LUT.

The simplified block diagram of the calibration unit used in this design is shown in Fig. 5.4. It employs a highly digital frequency-locked-loop (FLL) where

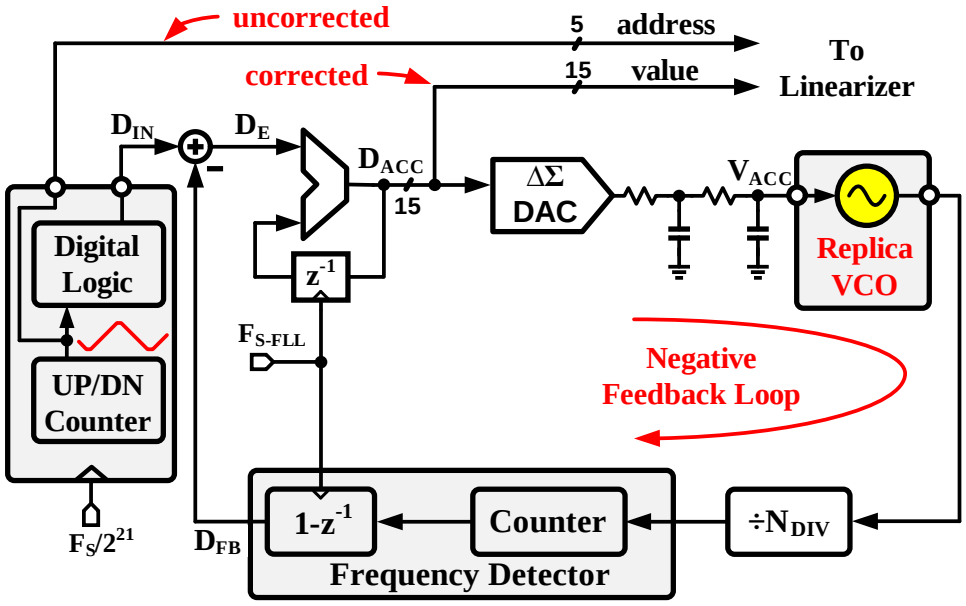

Figure 5.4: Simplified block diagram of the proposed calibration unit

a negative feedback loop sets the replica-VCO oscillation frequency in accordance with the digital input code, D_{IN}. The replica-VCO output frequency is first divided by N_{DIV} using a ripple divider. The counter and the digital differentiator $(1 - z^{-1})$ form a frequency detector. It detects the divided replica-VCO frequency

by continuously counting the total number of rising edges in each period of the FLL reference clock, F_{S-FLL}. Since the counter is never reset in this frequency detector, the frequency detection error approaches zero with time. Consequently, the frequency detector output, D_{FB}, precisely represents the divided replica-VCO frequency. The divided replica-VCO frequency is given by $F_{DIV-VCO} = D_{FB}F_{S-FLL}$. The accumulator integrates the difference between the detected frequency, D_{FB}, and D_{IN}. A slow, but accurate $\Delta\Sigma$-DAC converts the accumulator output, D_{ACC}, to analog voltage, V_{ACC}, that drives the tuning port of the replica-VCO. In steady-state, the negative feedback loop forces $D_{FB} = D_{IN}$ and the replica-VCO oscillation frequency is given by,

$$F_{VCO} = D_{IN}N_{DIV}F_{S-FLL}. \tag{5.5}$$

By a correct choice of D_{IN}, N_{DIV} and F_{S-FLL}, the replica-VCO can be forced to operate at all the desired frequencies determined using Eq. 5.4. For example, in this implementation since the digital output, D_{VCO}, is 5-bit wide, Eq. 5.4 results in 32 F_{VCO} values. Therefore, with $F_{S-FLL} = F_S/2^{10}$ and $N_{DIV} = 8$, $D_{IN} = 4n$ (where n = 0, 1, ... , 31) locks the replica-VCO to all the desired frequencies. DINGEN block, consisting of a 5-bit Up/Down counter and combinational logic circuits, cyclically generates the desired D_{IN} values. For each D_{IN}, sufficient time is provided for the feedback loop to attain a steady-state. The accumulator output in steady-state represents the desired VCO input in digital form. This is stored in the LUT using the address provided by the DINGEN block, to realize the inverse V-to-F transfer function.

To fully realize the benefits of the above architecture, D_{ACC} must accurately represent the replica-VCO input, V_{ACC}. The circuit design and implementation details of the DAC and other building blocks in the calibration unit are discussed in Sec. 5.2.

5.1.2 *Pseudo-Differential Architecture*

While the architecture shown in Fig. 5.2 effectively linearizes the VCO-based ADC, it's benefits can be maximized by employing a pseudo-differential structure. Figure 5.5 shows the complete architecture of the proposed VCO-based ADC. The differential inputs, V_{INP} and V_{INN} are digitized separately by the positive and

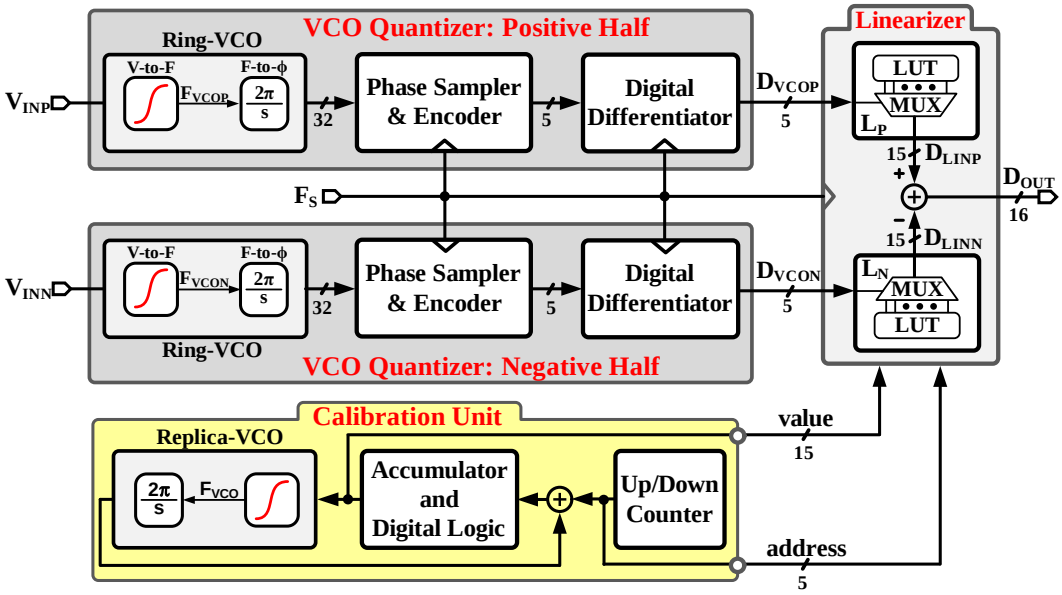

Figure 5.5: Simplified block diagram of the pseudo differential VCO-based quantizer.

negative half circuits to produce distorted outputs D_{VCOP} and D_{VCON}, respectively. Linearizers, L_P and L_N, remove distortion introduced in the VCOs of each half circuit resulting in digital outputs, D_{LINP} and D_{LINN}. The outputs of each half circuit are then digitally subtracted to get the final ADC output, D_{OUT}.

The pseudo-differential architecture results in improved signal to noise ratio (SNR) and linearity [19]. Since the input signal processed in each half circuit is differential, they are correlated and therefore the total signal power at the final ADC output increases by 6 dB. However, the noise in each half-circuit is uncorrelated

due to it's random nature and the noise power at the final ADC output increases by only 3 dB. This results in a net 3 dB improvement in SNR of the pseudo-differential ADC. The improvement in linearity occurs because, the even order harmonics of the input signal, due to V-to-F nonlinearity of VCO, have same magnitudes and signs at the output of each half circuit. Consequently, these harmonic terms cancel at the final ADC output. It should be noted that the improvement in linearity is limited by the extent to which the two half circuits match and the improvement in SNR comes at the cost of increased power consumption and area. However, since some blocks such as calibration unit, LUT, clock buffers etc., can be shared between the half circuits, the power overhead is not doubled. Furthermore, simulated and measured results indicate that the two half circuits match sufficiently to improve linearity. Therefore, the advantages of pseudo-differential architecture far outweigh it's disadvantages.

5.2 Circuit Design Details

This section discusses the circuit design details of important building blocks in the signal path such as VCO-based quantizers, linearizers, etc., and the calibration unit.

5.2.1 VCO-based quantizer

The complete architecture of the pseudo-differential VCO-based quantizer is shown in Fig. 5.6. For simplicity only the positive half circuit is shown with more detail. The VCO used in each half-circuit consists of a current starved architecture

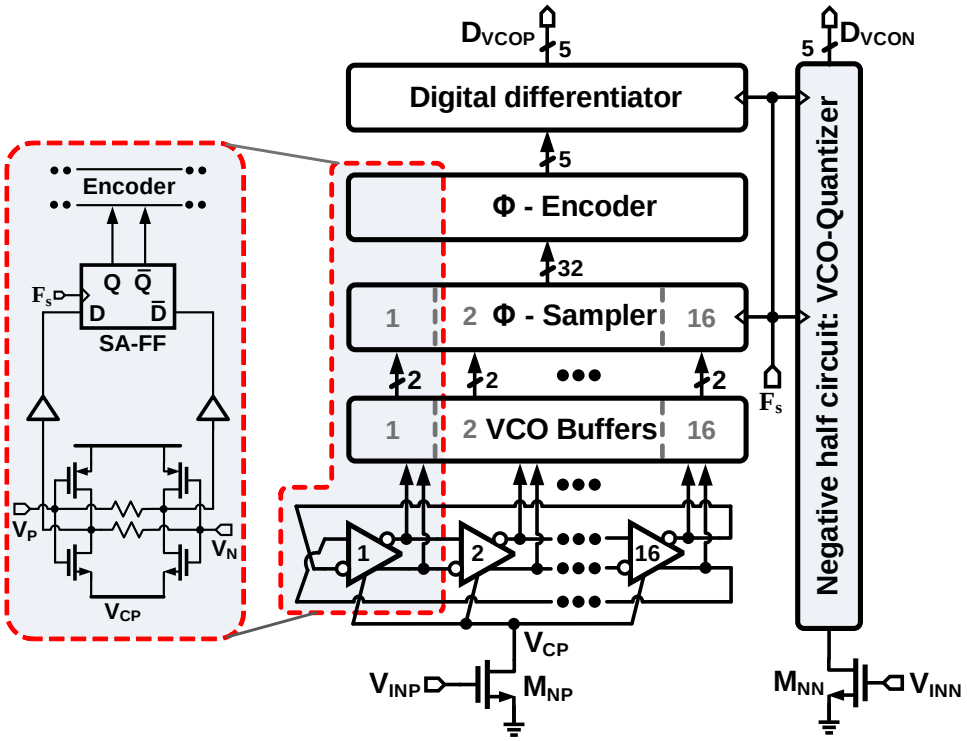

Figure 5.6: VCO-based quantizer architecture.

with 16 delay stage ring oscillator. Each delay stage consists of two inverters that are resistively coupled. The inputs to the VCO, V_{INP} and V_{INN}, control the current through transistors M_{NP} and M_{NN}, respectively, to set the VCO oscillation frequency. Since the inputs directly control the gates of the transistors, it provides a high input impedance, at least at low frequencies. Good layout practices are adopted to ensure that the mismatch between the VCO phases are minimized. The buffered oscillator phases, in each half circuit, are sampled by the phase-sampler which consists of an array of 16 sense-amplifier flip-flops. The buffer stage isolates the ring-VCO from the sampling kick-back noise and loading effects of the flip-flops. The output of the phase sampler has CMOS voltage levels and represents the quantized VCO-phase. This output is 16 bit (32 bit using complimentary values)

wide and is encoded to a 5-bit binary number using the phase encoder which consists of combinational logic. To get the quantizer output, the phase samples must be differentiated. This is done in the digital differentiator by subtracting the current and previous samples of the binary encoded phase using a 5-bit digital subtracter. Two's-complement representation is used in this subtraction due to it's ease of implementation. The simulated output power spectrum of this VCO-

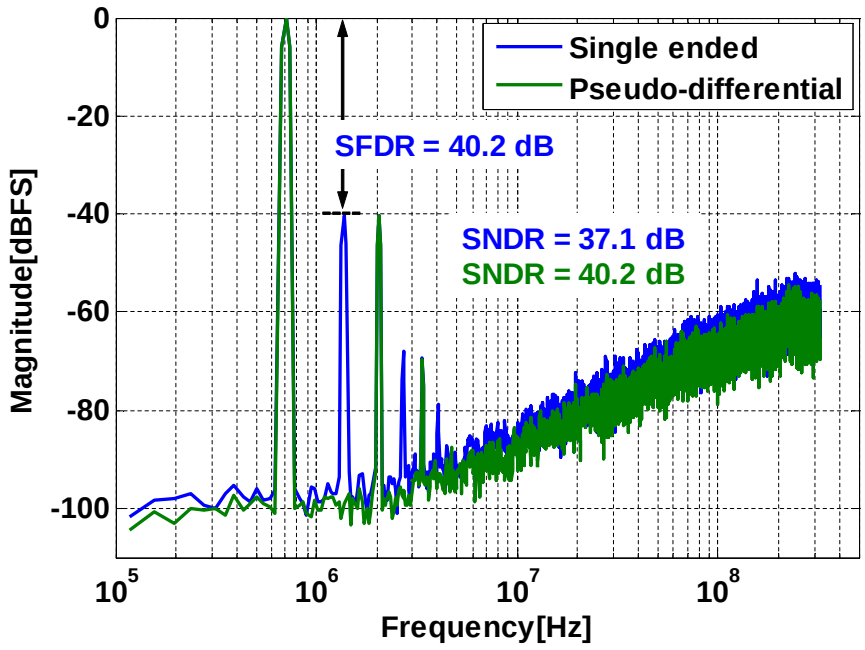

Figure 5.7: Simulated output power spectral density of the VCO-based quantizer.

based ADC with a sampling clock frequency of 640 MHz is shown in Fig. 5.7. With single-ended implementation, the ADC output contains both even and odd harmonic tones and the SNDR is limited to about 37 dB. However, with pseudo-differential implementation, the even order harmonics cancel and the ADC achieves an SNDR of about 40 dB.

The simulated voltage to frequency (V-to-F) tuning characteristics of the VCO used in each half circuit is shown in Fig. 5.8(a). It covers a wide tuning

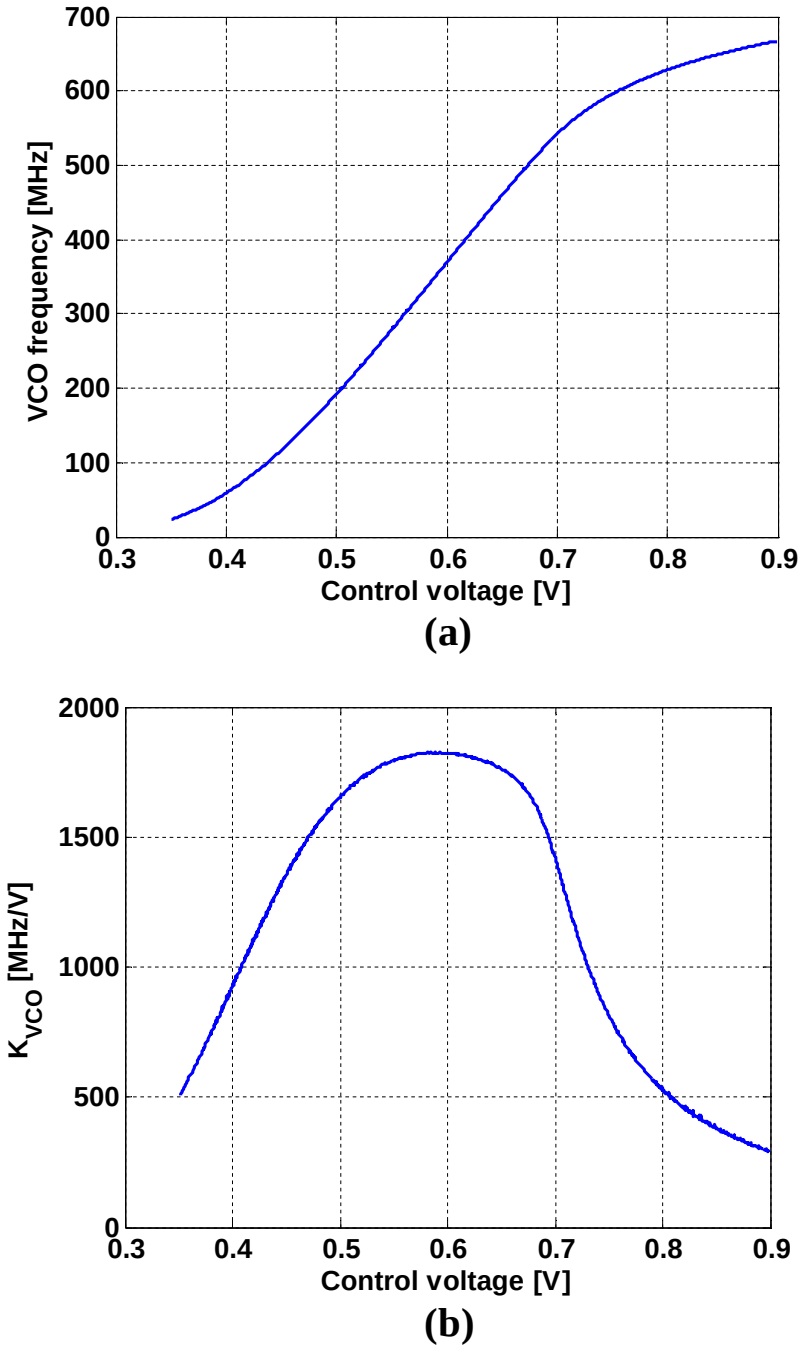

Figure 5.8: Simulated VCO characteristics. (a) Voltage to frequency tuning characteristics. (b) VCO gain (K_{VCO}) vs. control voltage.

range from close to 0 to 660 MHz. Since the phase-encoder does not take care of phase rollover, the VCO oscillation frequency range is limited to 0 - F_S which is 0 - 640 MHz in this implementation. For control voltage (V_{INP}/V_{INN}) greater than 0.7 V, and control voltage less than 0.45 V, the V-to-F tuning characteristic becomes grossly non-linear. This is because, at the higher end current control transistor M_{NP} (or M_{NN}) enters triode region and at the lower end it approaches cut-off region. Between these extreme ends ($0.45\ V \leq V_{INP}, V_{INN} \leq 0.7\ V$), the control transistor operates in saturation region and the V-to-F tuning curve appears relatively linear. However, even in this region the VCO gain (K_{VCO}) varies by more than 20% as depicted in Fig. 5.8(b) and limits the achievable SNDR as shown earlier in Fig. 5.7. The simulated phase noise of the VCO is shown in Fig. 5.9. It has a $1/f^3$ corner frequency of about 200 kHz above which the phase noise rolls off at -20 dB/decade. To determine the magnitude of thermal noise, the phase noise is input referred by dividing it with the VCO's voltage to phase transfer function (K_{VCO}/s). The root mean squared value of the thermal noise obtained in this manner is about 8.6 μV in 5 MHz signal bandwidth. For a 400 $mV_{pp,diff}$ input, the phase noise limits the SNR to about 81 dB.

5.2.2 Calibration Unit

Most of the calibration unit building blocks, except the replica-VCO and DAC, are digital in nature. The replica-VCO is placed physically close to the VCOs in the signal path and is architecturally identical to other VCOs in the signal path. Care is taken to ensure that the all the VCOs have identical terminal parasitic resistances and capacitances. The feedback path in the calibration unit consists of level-shifter, divider and digital frequency detector. The output of

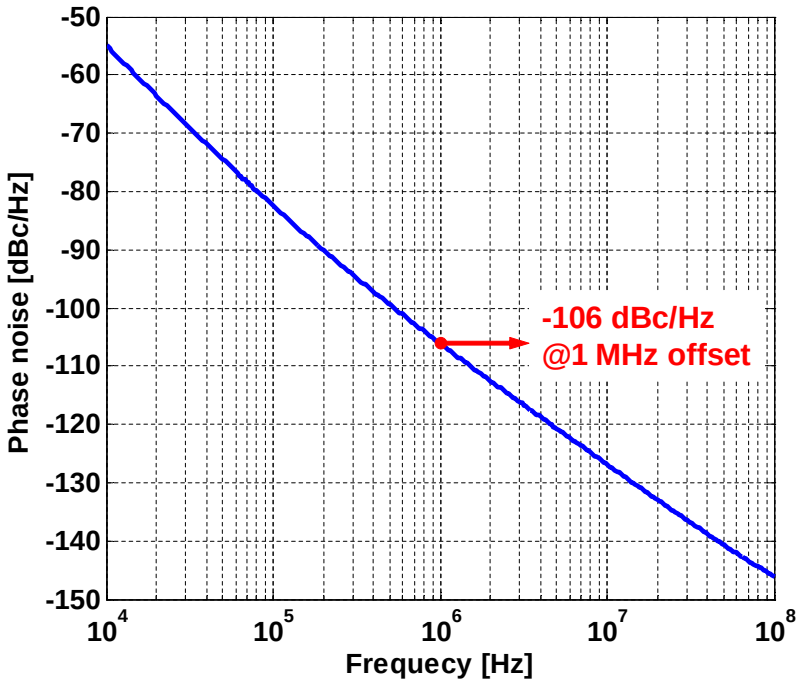

Figure 5.9: Simulated VCO phase noise.

the replica-VCO is converted to CMOS voltage level with level shifters as shown in Fig. 5.10(a). A ripple counter type divider using three flip-flops, as shown in Fig. 5.10(b), is used to divide the replica-VCO output. The frequency detector consists of a 10-bit counter and a digital differentiator as shown in Fig. 5.10(c). The counter determines the number of rising edges of the divider output. The differentiator finds the difference between the current and the previous counter outputs to determine the total number of rising edges in every period of the FLL reference clock, F_{S-FLL}. Since the counter updates at the rising edge, to avoid metastability, the differentiator clock is re-timed with the falling edge of the divided replica-VCO clock. Due to two's complement representation, the subtracter takes care of counter rollover and it need not be reset.

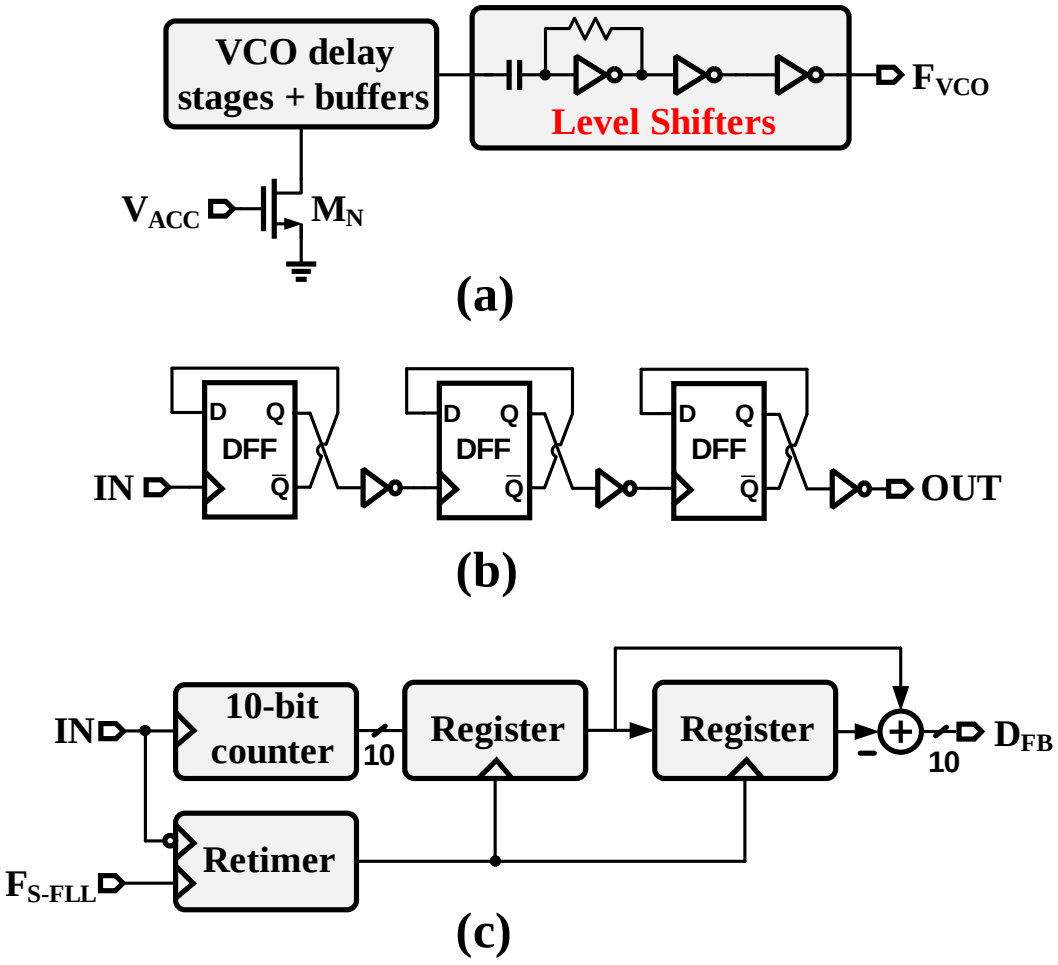

Figure 5.10: Blocks in calibration unit feedback path. (a) AC coupled level shifters. (b) Frequency divider. (c) Frequency detector.

The 15-bit DAC (see Fig. 5.4), which converts the accumulator output, D_{ACC}, to a analog voltage, V_{ACC}, forms a critical building block of the calibration unit. Since errors in this DAC directly affect the accuracy of distortion corrected codes, it needs to satisfy the linearity requirement desired from the entire ADC. Achieving a highly linear 15-bit DAC can be a very challenging design task. However, since the accumulator updates at a very slow rate ($F_{S-FLL} = F_S/2^{10} = 625$ kHz), $\Delta\Sigma$ DAC can be easily employed. Figure 5.11 shows the architecture of the DAC

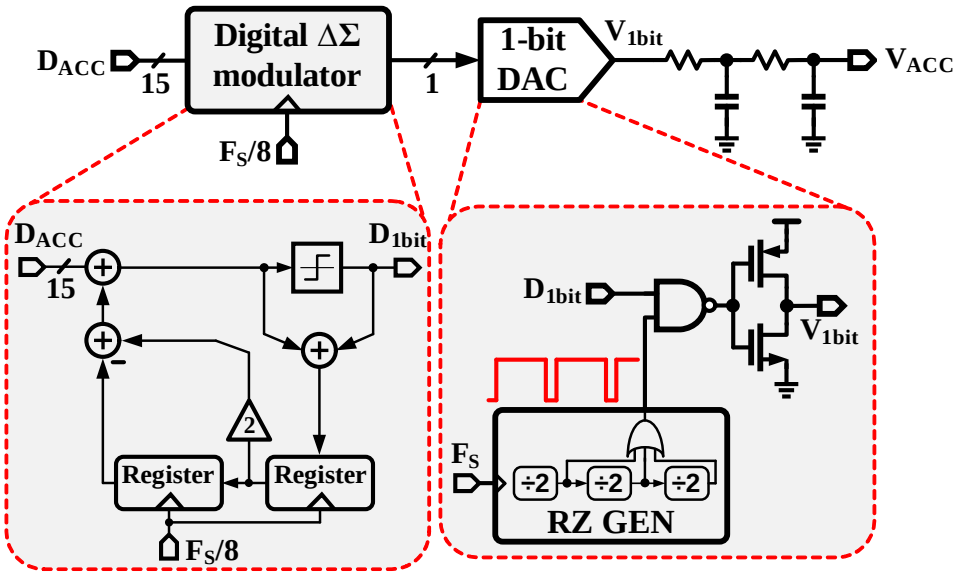

Figure 5.11: Schematic of 1-bit ΔΣ DAC.

used in this implementation. A second order digital ΔΣ modulator truncates the 15-bit D_{ACC} to a 1-bit data stream which drives a 1-bit DAC. An error feedback architecture is used to implement the digital ΔΣ modulator due to it's ease of implementation. A passive low pass filter suppresses the shaped truncation error to generate a voltage, V_{ACC}. Though an ideal 1-bit DAC is inherently linear, non-idealities such as unequal rise/fall times in the DAC output results in non-linearity. To minimize the impact of this dynamic non-linearity, a modified return-to-zero DAC (RZ-DAC) is employed. An input 'high' is represented by an output pulse which remains high for only 7/8 clock period of the ΔΣ clock, and for an input 'low' the DAC output remains low for the entire clock period. Compared with traditional RZ-DAC, which uses 50% duty-cycle output pulse, this modified implementation allows increased output dynamic range for given DAC reference voltages. For example, with 0 V and 1.2 V references, the proposed DAC output can range between 0 V - 1.05 V. However, if a conventional RZ-DAC is used, the

output voltage range is only 0 V - 0.6 V.

5.2.3 Linearizers

Figure 5.12 shows the simplified structure of the linearizer. It consists of a

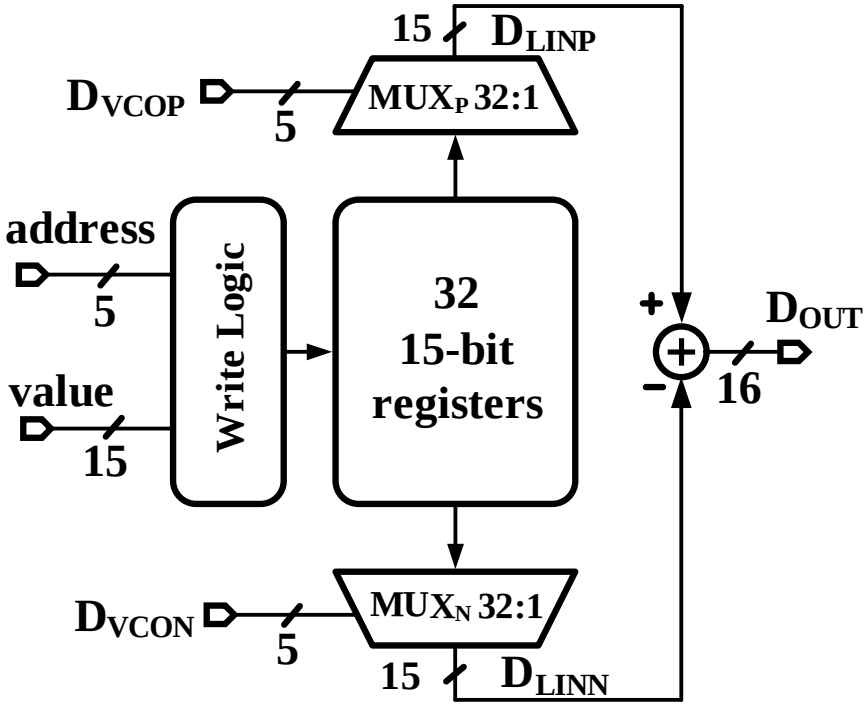

Figure 5.12: Implementation of the linearizer.

bank of 32, 15-bit registers, that is common to both half-circuits, and it stores all the distortion corrected codes. Using the address and data obtained from the calibration unit, the write logic continuously updates this memory bank. Two output multiplexers, MUX_P and MUX_N, read the memory bank contents using the quantizer outputs D_{VCOP} and D_{VCON}, respectively, as the address. The multiplexer outputs are subtracted with a 15 bit carry look ahead subtracter to get the ADC output.

Due to the highly digital nature of the proposed ADC, schematic and layout of most of the building blocks in the calibration-unit, linearizers, adders/subtractors etc., are easily obtained from corresponding high level description language using a standard digital flow.

5.3 Design Considerations and Non Ideal Effects

In this section, the impact of various non-ideal effects such as mismatch, dynamic non-linearities etc., are studied.

5.3.1 Effect of replica-VCO mismatch

In the proposed architecture, since the inverse V-to-F transfer function is obtained from the replica-VCO, the effectiveness of distortion correction would depend on the matching between the signal path VCOs and replica-VCO. Mismatch in the threshold voltage of the current control transistor of the VCO (eg. transistor M_{NP}) causes fixed offset in it's V-to-F transfer characteristics. The proposed architecture is immune to such offset errors. This is because, it shifts the detected inverse transfer function curve to the left or right parallel to the x-axis, as shown in Fig. 5.13(a). Consequently, the linearity improvement remains unaffected and it results only in a DC offset in distortion corrected ADC output. Contrary to offset error, gain error in the V-to-F transfer function shifts the detected inverse transfer function along the y-axis and directly impacts the linearity improvement as shown in Fig. 5.13(b). Such gain errors, for example, can be caused by the mismatches in the mobility or width/length of the current control transistor. As

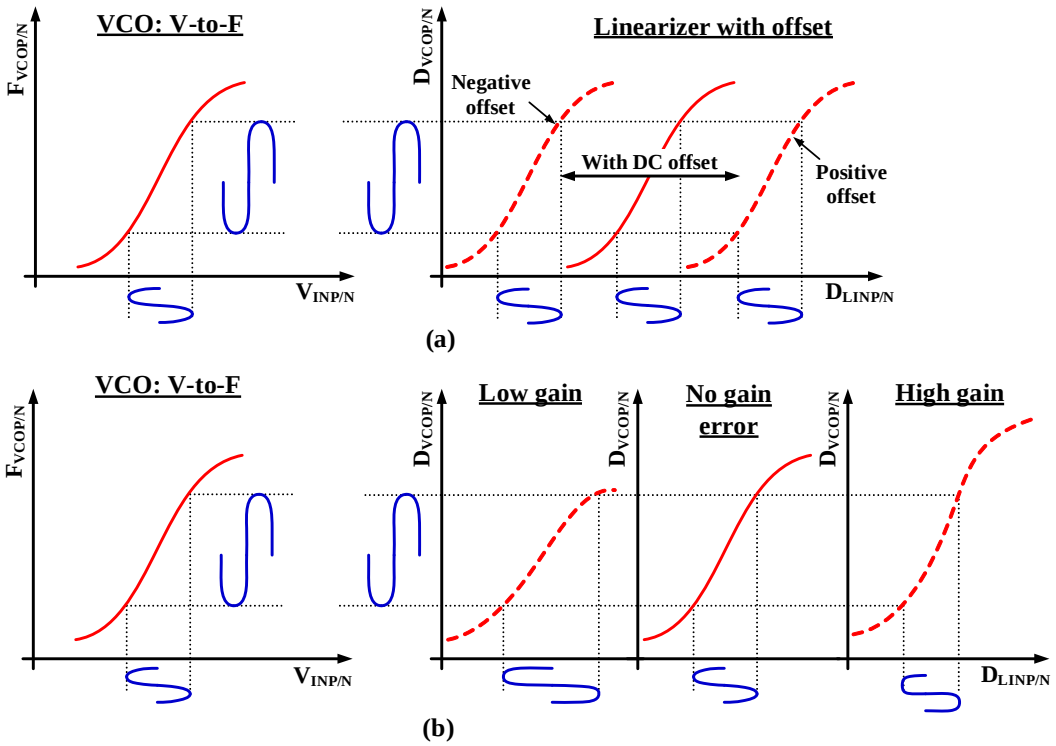

Figure 5.13: Effect of mismatch between the VCOs. (a) Manifestation of offset mismatch. (b) Manifestation of gain mismatch.

shown in the figure, either a high or low a gain cause distorted ADC output.

To determine the overall impact of mismatch due to gain and offset errors, Monte-Carlo simulations were performed. Figure 5.14(a) shows the simulated SNDR in 5 MHz bandwidth for 100 Monte-Carlo runs with and without the proposed calibration. it's mean and variance are 75 dB and 0.24 dB, respectively. Figure 5.14(b) shows the Monte-Carlo results for SFDR, which has a mean and variance of 84 dB and 2.4 dB, respectively. Since the SNDR is limited by quantization noise and thermal noise rather than harmonic tones, it's variance is smaller than that of SFDR. These results indicate that if the target SNDR is around 75 dB - 80 dB (or lower), proposed ADC provides sufficient correction even in the presence of mismatches.

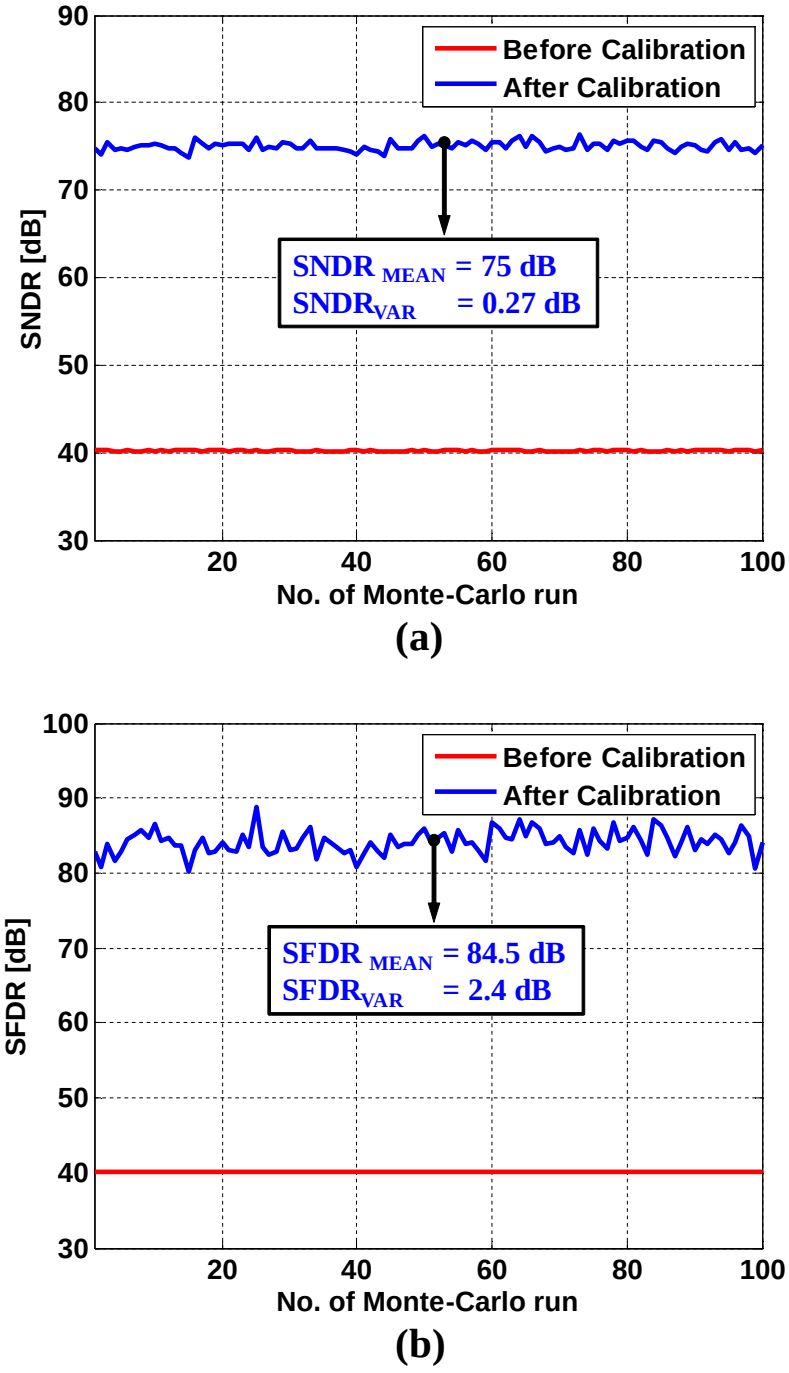

Figure 5.14: Monte-Carlo simulation results. (a) SNDR in 5 MHz bandwidth. (b) SFDR in 5 MHz bandwidth.

5.3.2 Effect of Dynamic Non-Linearity

While determining the inverse V-to-F transfer function in the calibration unit, sufficient time is provided for the feedback loop to settle before changing D_{IN}. Hence the proposed calibration unit determines the 'static' inverse V-to-F transfer function of the replica-VCO. Since the inputs of the VCOs in the signal-path change rapidly, it's dynamic behavior is not captured by the calibration unit which results in dynamic non-linearity and may affect distortion correction. To

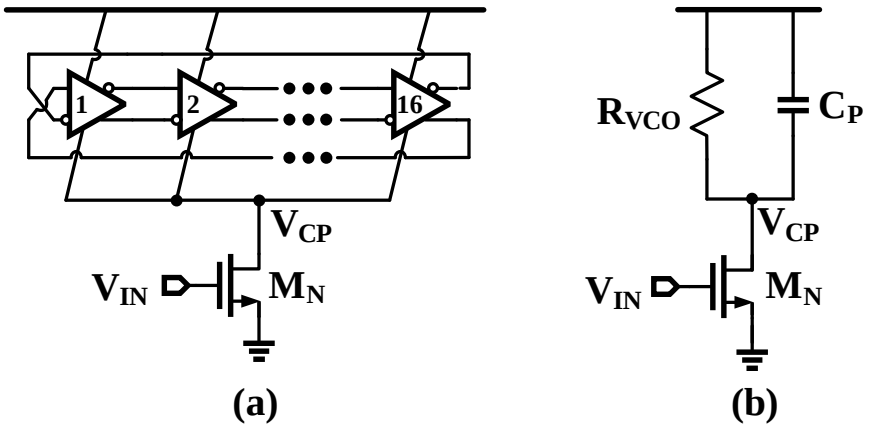

Figure 5.15: Dynamic behavior VCO. (a) Schematic of current starved VCO. (b) Approximate small signal model.

gain more insight into the dynamic behavior, consider the current starved VCO and it's equivalent small signal model as shown in Fig. 5.15. In the small signal model, C_P represents the sum of all the terminal and parasitics capacitances on the drain node of the current control transistor, M_N, and R_{VCO} represents the resistance looking into the VCO ring. Capacitance C_P introduces a parasitic pole, ω_p ($= 1/(R_{VCO}C_P)$), which slows the VCO response. Since both R_{VCO} and C_P vary with the VCO frequency (input signal dependent), and this pole is introduced after the non-linearity of the transistor, it results in dynamic non-linearity. Simulations

indicated that in this implementation ω_p is much greater than the signal bandwidth of 5 MHz, therefore the dynamic non-linearity effects are negligible.

For wide bandwidth ADCs, special care may be required to push ω_p further out and minimize it's impact. To this end, C_P should be reduced by adopting good layout practices to minimize the parasitic capacitances on drain node of M_N. Parasitic pole frequency, ω_p, may also be increased by minimizing R_{VCO}. This can be achieved by operating the VCO between $0.5F_S$ - $1.5F_S$ (or F_S - $2F_S$), instead of operating it in the range of 0 - F_S as in this implementation. This is because, R_{VCO} decreases as the VCO frequency is increased and therefore a higher VCO frequency results in lower impedance looking into the VCO ring [36]. This can also be seen with the voltage settling behavior at the drain of M_N for a negative input step applied at 100 ns, as shown in Fig. 5.16. Case-1 corresponds to the drain

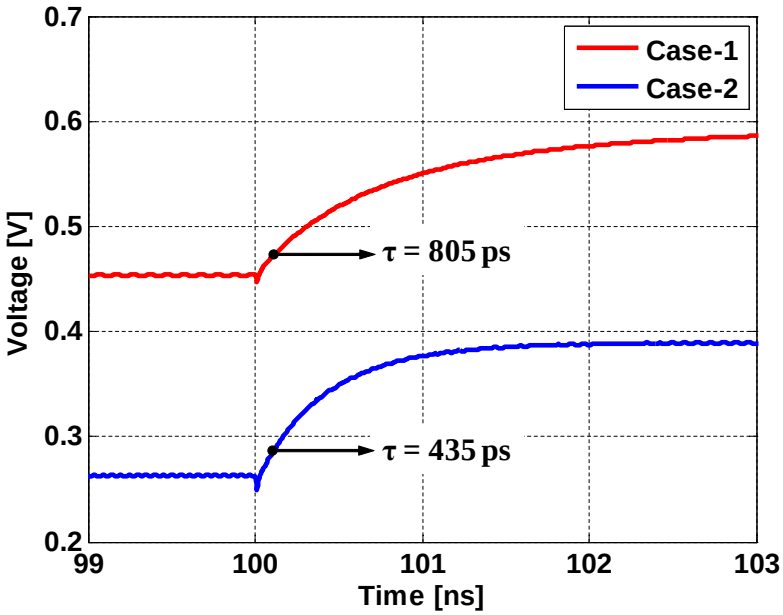

Figure 5.16: Voltage settling at the drain node for a step input at 100 ns.

voltage for VCO frequency change from 300 MHz to 100 MHz, and for case-2 the

frequency changes from 600 MHz to 400 MHz. In both cases the frequency change is 200 MHz, however due to higher VCO frequency in case-2 the settling is much faster indicating that ω_p is larger.

5.3.3 *Effect of finite point correction*

Since VCO's tuning characteristics is a continuous function, only a continuous inverse V-to-F transfer function can perfectly linearize the system. However, in the proposed ADC, the inverse V-to-F transfer function is determined only at a finite set of frequencies (given by Eq. 5.4). It is instructive to determine the effect of this finite point correction on the ADC performance.

Consider the distortion correction with only four calibrated points as shown in Fig. 5.17. Perfect correction is obtained only for the inputs corresponding to the

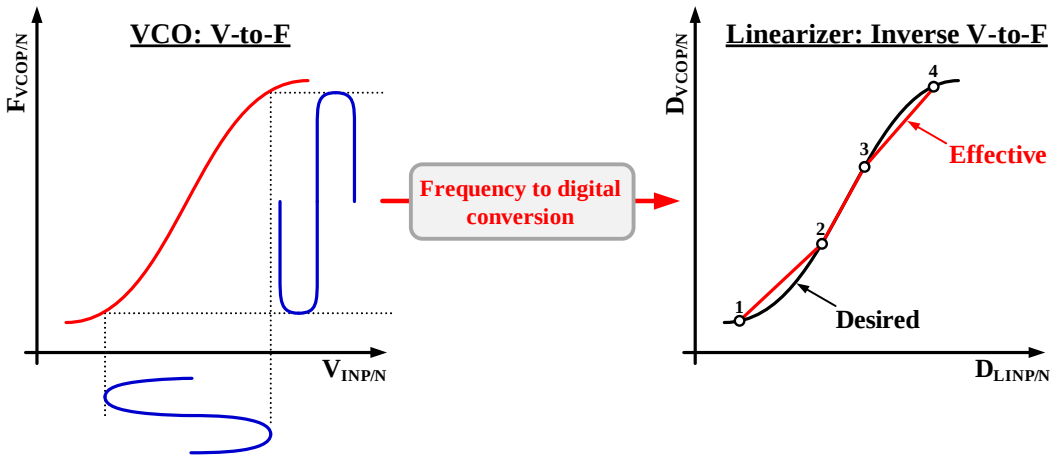

Figure 5.17: Effect of finite point calibration on distortion correction.

four calibrated frequencies. If the input lies in between two calibrated points (say 1 and 2), due to $\Delta\Sigma$ operation of the VCO-based quantizer, it's output toggles between the two points (i.e. 1 and 2) such that the average corresponds to the

VCO frequency. Consequently, the inverse V-to-F transfer function is represented by a straight line joining to consecutive calibrated points as shown in Fig. 5.17. The resulting integral-non-linearity (INL) for different number of calibration points is qualitatively represented in Fig. 5.18. It indicates that the INL is zero only at

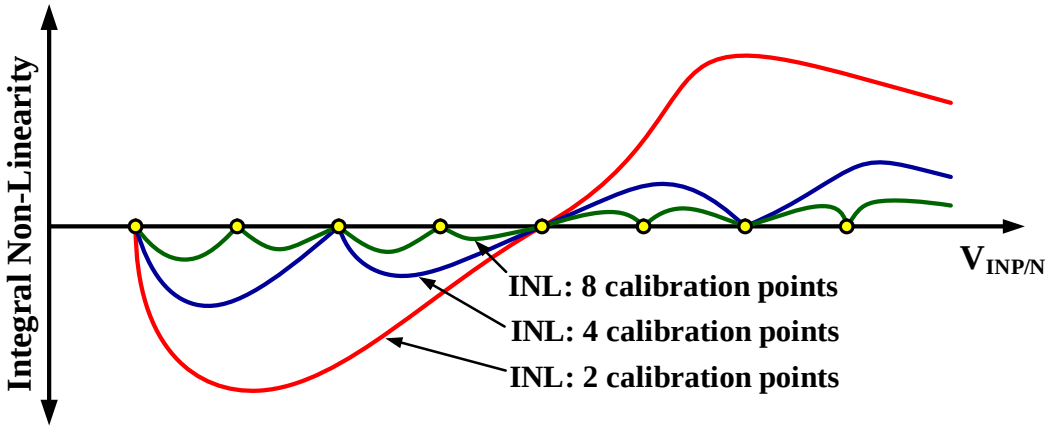

Figure 5.18: Representative integral-non-linearity for different calibration points.

the calibrated points, therefore a lower number of calibrated points degrades the linearity performance of the system. In this implementation, 32 calibration points are used as it was found to be sufficient to achieve better than 80 dB linearity.

5.4 Measured Results

Figure 5.19 shows the die-micrograph of the proposed ADC. The ADC is fabricated in a 90nm CMOS process and it occupies an active area of about 0.16mm^2. All the building blocks shown in Fig. 5.5 including the calibration unit, linearizers etc., are implemented on-chip. The chip is packaged in a 60 pin QFN package.

An external clock source provides one 640 MHz master clock reference which is used as the sampling clock in the VCO-based ADC. All the other clock references used in the calibration unit such as F_{S-FLL} and $F_S/2^{21}$ clock references (see Fig. 5.4)

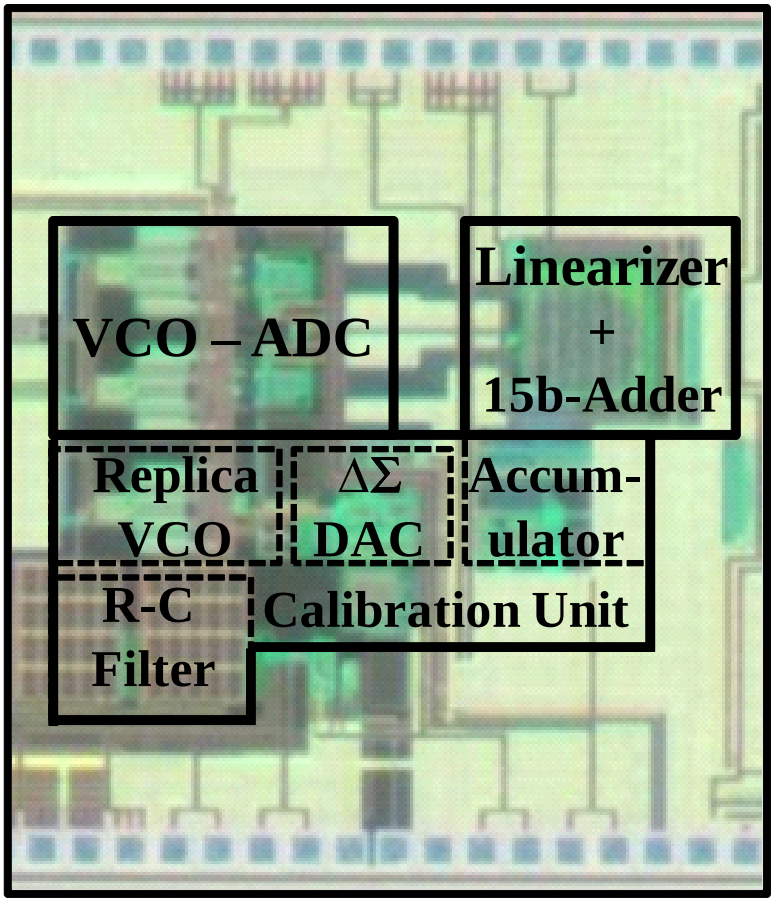

Figure 5.19: Die photograph of the proposed ADC.

are derived on-chip by dividing the 640 MHz master clock. The analog building blocks such as the VCO and the RZ-DAC operate from a 1.2 V supply and all the remaining circuits are digital in nature and they operate from a 1 V supply. Various test modes have been implemented to measure the ADC output with and without on-chip calibration and to capture the output of the accumulator used in the digital FLL.

The measured output of the accumulator used in the calibration unit is shown in Fig. 5.20. As D_{IN} is changed cyclically by the DINGEN block, the feedback loop forces the replica-VCO to operate at different frequencies. Consequently, the accu-

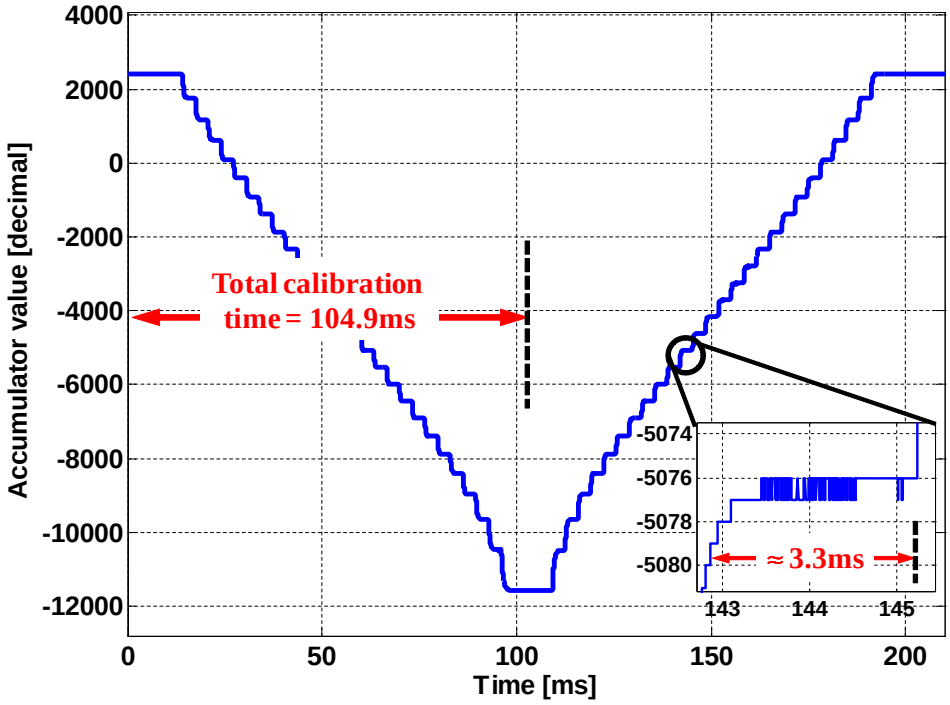

Figure 5.20: Measured accumulator output as replica-VCO locks to different frequencies.

mulator output also changes cyclically to drive the replica-VCO with the correct tuning voltage. Due to an inversion within the $\Delta\Sigma$ DAC, higher accumulator output corresponds to a lower DAC output and vice-versa. Since this inversion results only in a sign change in the final ADC output, the linearity correction remains unaffected. Since D_{IN} is changed every 3.28 ms (corresponding to $F_S/2^{21}$ clock), it takes about 104.8 ms to cycle through all D_{IN} values and get the first set of look-up-table (LUT) contents. The inset in Fig. 5.20 shows that the settling behavior for one particular D_{IN}. In steady-state, the accumulator output toggles between two codes.

The measured output power spectral density of the ADC with 400 $mV_{pp,diff}$,

500 kHz sinusoidal input is shown in Fig. 5.21. To plot this spectrum a 2^{15} point

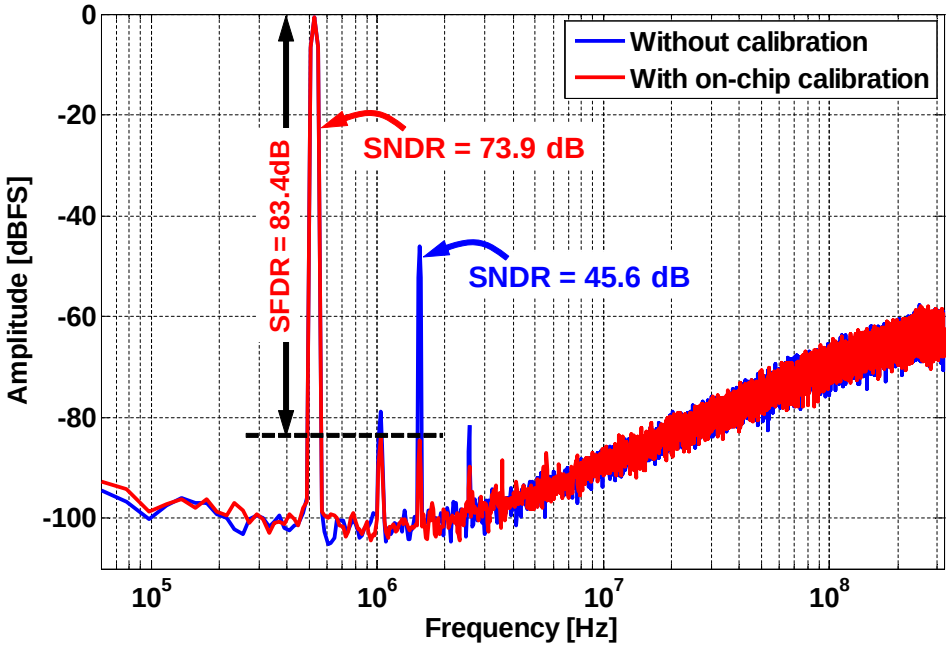

Figure 5.21: Measured ADC output power spectral density with and without background calibration.

FFT is averaged 16 times. Without calibration the ADC achieves a peak SNDR of 45 dB in 5 MHz signal bandwidth. Due to the pseudo differential ADC architecture, the even order harmonics are minimized and the SNDR is limited mainly by the third order distortion. However, once the background calibration is enabled the proposed calibration algorithm improves the SFDR of the ADC from 45.6 dB to more than 83 dB and it achieves an SNDR of 73.9 dB in 5 MHz signal bandwidth. The performance of this ADC with a two tone input is shown in Fig. 5.22. For this measurement two sinusoidal input tones at 500 kHz and 1 MHz, each with half the full scale input amplitude, is applied to the ADC. Figure 5.22(a) shows the measured output power spectrum without calibration. Due to the V-to-F nonlinearity, the output spectrum contains many inter-modulation tones. However, as shown in Fig. 5.22(b), when the on-chip calibration is enabled the linearity

of the ADC improves thereby significantly reducing the magnitude of the inter-modulation tones. This measurement confirms that the proposed calibration works effectively even for multi-tone inputs. The measured SNR and SNDR for different input amplitudes is shown in Fig. 5.23. The ADC achieves a peak SNR and SNDR of 75.4 dB and 73.9 dB, respectively, and the dynamic range is 77 dB. Near the peak performance, the SNR and SNDR for different input frequencies are also shown in Fig. 5.23. For a 2 MHz input, since the third harmonic falls outside the signal band, the SNDR is better than that for 1 MHz and 500 kHz input.

Table 5.1 summarizes the performance of the proposed ADC and compares it with other state of the art time based ADCs. It consumes a total power of 4.1 mW with all the analog blocks such as the VCOs and the RZ-DAC together consuming about 1.2 mW and all the digital blocks such as linearizers, phase samplers etc., consuming about 2.9 mW. The figure of merit (FOM) for this ADC is calculated as,

$$\text{FOM} = \frac{\text{TotalPower}}{2 \times \text{Bandwidth} \times 2^{\text{ENOB}}}. \tag{5.6}$$

The ADC achieves an FOM in the range of 92-110 fJ/conv-step for different input frequencies. This FOM is the best among all time-based ADCs. Furthermore, since more than 70% of the power is dissipated in digital circuits, this FOM is expected to improve significantly in finer CMOS technologies.

Table 5.1: Performance summary and comparison

Reference	This work			[17]	[23]	[31]	[24]	[29]
Process	90 nm			0.13μm	0.13μm	65 nm	90 nm	65 nm
Bandwidth [MHz]	5			10	20	20	10	20.3
Sampling rate [MHz]	640			950	900	250	600	1300
Input frequency [MHz]	0.5	1	2	1	2	3.9	1	1
SNDR [dB]	73.9	73	74.7	72	78	60	76.6	69
SNR [dB]	75.4	75.4	75.4	86	81	62	80.5	70
Power [mW]	4.1			40	87	10.5	16	11.5
Active area [mm^2]	0.16			0.42	0.45	0.15	0.36	0.075
FOM [fJ/conv-step]	101	112	92	500	330	319	145	123

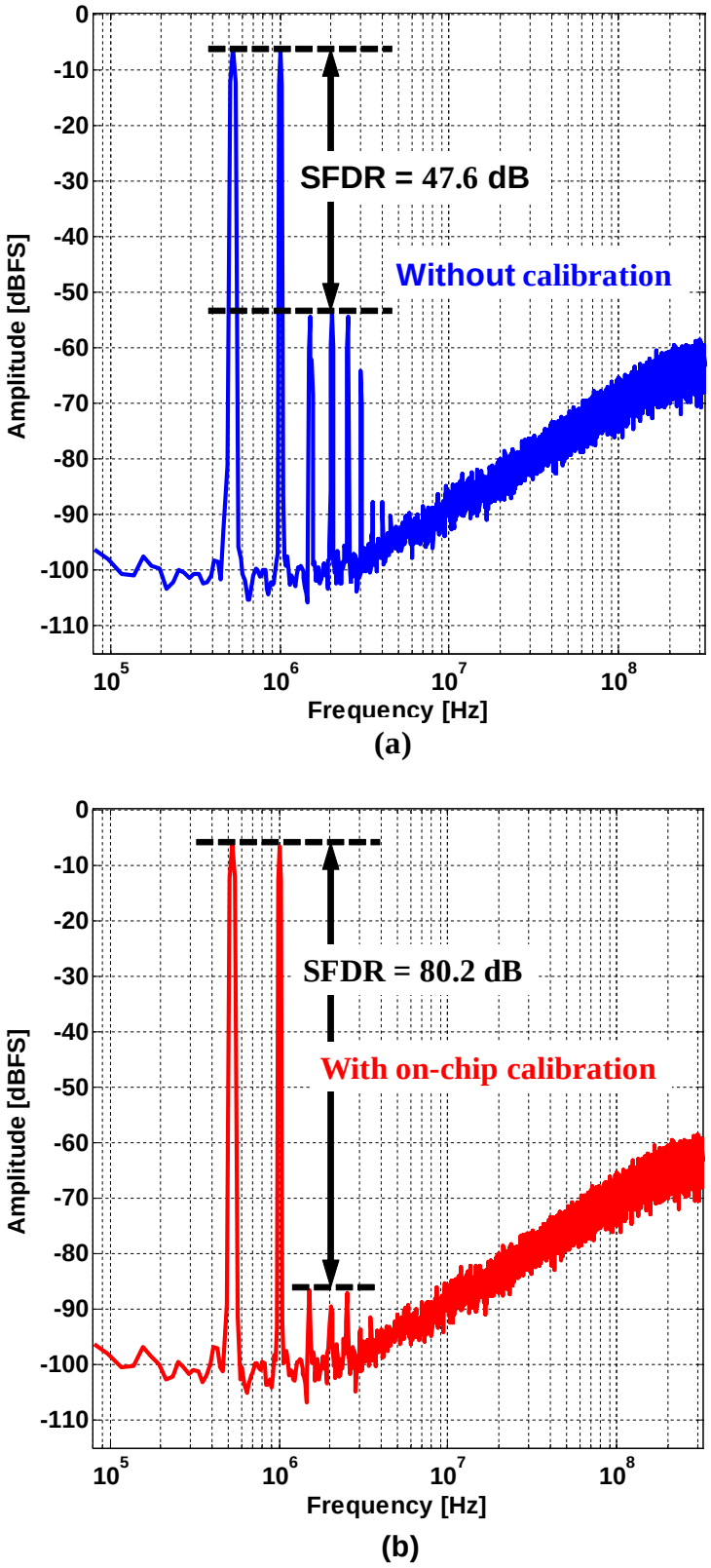

Figure 5.22: Measured ADC output power spectral density with two tone input. (a) Without calibration. (b) With background calibration.

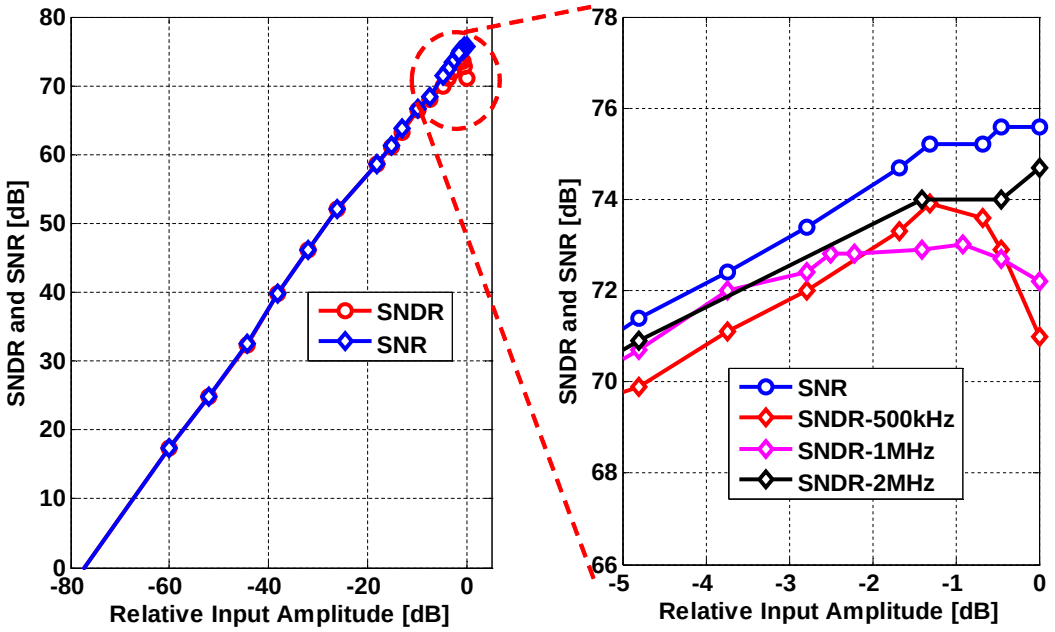

Figure 5.23: Measured ADC SNR and SNDR vs. input amplitude.

CHAPTER 6. CONCLUSION

In this work, two new VCO-based ADC architectures have been discussed. To improve the distortion performance of VCO-based ADCs, the first technique explores an interesting approach wherein the VCO is forced to operate at only two frequencies on the non-linear K_{VCO} characteristic. To this end, a two level modulator is used to first convert the analog input signal to a two level signal which is then digitized using a VCO-based ADC. A natural sampling pulse width modulator is used as the two level modulator in this implementation. Unlike other forms of pulse width modulation, a natural sampling pulse width modulator is inherently linear and does not use an explicit sampler thereby simplifying the design. Furthermore, since this two level modulator does not introduce any quantization error, its design is mainly governed by the targeted ADC linearity. The proposed ADC, in addition to being linear, retains the advantages of other VCO-based ADCs and provides first order noise shaping to the quantization error. Due to the anti-aliasing properties of the VCO-based quantizer, the aliased higher order tones are suppressed. Measured results from a prototype IC, fabricated in 90 nm CMOS process, demonstrated the linearity improvement and validated the proposed two level operation. Compared with conventional approaches, since the proposed two level signal is spectrally dense even at very high frequencies, the proposed architecture may be more susceptible to parasitics on the supply, and cross talk between different blocks. However, this problem can be mitigated by using a better package or improving the on-chip isolation. The linearity and figure of merit of this ADC is comparable to other state of the art VCO-based ADCs. Innovative circuit design

techniques that can realize a two level signal while consuming lower power can further improve the performance of this ADC.

One definite disadvantage of the first technique is the requirement of a linear front-end two level modulator. In addition to using analog building blocks such as op-amps, comparators etc., the two level modulator consumes significant power which may not scale with the CMOS process. In the second technique, the requirement of the two level modulator is obviated by digitally calibrating the distorted output. Calibration is performed by introducing an inverse V-to-F transfer function in the signal path. To find the inverse V-to-F transfer function, the proposed technique uses a feedback loop and forces a replica-VCO to oscillate at predetermined set of frequencies. The proposed replica-VCO based calibration is very effective for VCO-based ADCs, mainly because of two reasons. First, since errors due to offsets and other circuit imperfections are first order noise shaped, they do not affect the final ADC output. Consequently, unlike in a voltage-domain ADCs, such errors need not be calibrated in this ADC. The only significant source of non-linearity is voltage to frequency tuning characteristics. Since the V-to-F characteristic match well between VCOs in a given chip, a replica-VCO can be used to extract the inverse V-to-F characteristics. Second, since the output quantity of a VCO-based ADC represents VCO's frequency, rather than a voltage quantity, the calibration unit can be implemented in a highly digital manner with infinite loop gain at DC, perfect frequency dividers and well defined digital inputs. If such a feedback loop were to be implemented for a voltage-domain ADC, very high gain amplifiers and precision input references would be required thereby incurring a power penalty. Simulation results indicated that mismatch between replica-VCO and signal path VCOs may limit the distortion correction, and the proposed ADC is most suitable for achieving about 12 to 13 effective number of bits. Though this

ADC targets 5 MHz signal bandwidth, in more advanced technology nodes, much wider signal bandwidth can be achieved. Measured results from the prototype chip shows good linearity improvement and validates the efficacy of the proposed architecture. Since this architecture avoids using analog building blocks, there are no additional sources of noise in the signal path. Therefore, the ADC achieves very good figure of merit with a relatively small input signal amplitude. If this ADC is employed in a system where the ADC noise is the limiting factor, the ability to work with small input signal amplitudes eases the design of the stages that precede VCO-based ADC.

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