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Title: Time and Statistical Information Utilization in High Efficiency Sub-Micron CMOS Successive Approximation Analog to Digital Converters.

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Un-Ku Moon

In an industrial and consumer electronic marketplace that is increasingly demanding greater real-world interactivity in portable and distributed devices, analog to digital converter efficiency and performance is being carefully examined. The successive approximation (SAR) analog to digital converter (ADC) architecture has become popular for its high efficiency at mid-speed and resolution requirements. This is due to the one core single bit quantizer, lack of residue amplification, and large digital domain processing allowing for easy process scaling. This work examines the traditional binary capacitive SAR ADC time and statistical information and proposes new structures that optimize ADC performance. The Ternary SAR (TSAR) uses the quantizer delay information to enhance accuracy, speed and power consumption of the overall SAR while providing multi-level redundancy. The early reset merged capacitor switching SAR (EMCS) identifies lost information in the SAR subtraction and optimizes a full binary quanitzer structure for a Ternary MCS DAC. Residue Shaping is demonstrated in SAR and pipeline configurations to allow for an extra bit of signal to noise quantization ratio (SQNR) due to multi-level redundancy. The feedback initialized ternary SAR (FITSAR) is proposed which splits a TSAR into separate binary and ternary sub-ADC structures for speed and power benefits with an inter-stage encoding that not only maintains residue shaping across the binary SAR, but allows for nearly optimally minimal energy consumption for capacitive ternary DACs. Finally, the ternary SAR ideas are applied to R2R DACs to reduce power consumption. These ideas are tested both in simulation and with prototype results.

Key Words: SAR ADC, TSAR, Ternary SAR, Residue Shaping, EMCS, FITSAR, R2R DAC

Time and Statistical Information Utilization in High Efficiency Sub-Micron CMOS Successive Approximation Analog to Digital Converters

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APPROVED:

_____

Major Professor, representing Electrical and Computer Engineering

_____

Director of the School of Electrical Engineering and Computer Science

_____

Dean of the Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

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Jon Guerber, Author

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The journey of my education has not been propelled by my own power. Rather, it's been guided, shifted, and directed by many who have worked to influence my environment and understanding of the world. As Issac newton famously said "If I have seen further, it is only by standing on the shoulders of giants." I'd like to take a few pages and thank some of the giants that have lifted me along my journey (in no particular order). Some of them had long-term interactions with me and some were brief insights that stuck with me, but they all channeled me into the path I'm on today.

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1. INTRODUCTION

Since the dawn of time, man has been trying to quantify the world. Time is naturally divided by sunrises and sunsets, but man further sub-divided it into hours and minutes. Temperature, quantized by freezing and boiling points, is further categorized in degrees. Goods are weighted by ounces and pounds, only to have that digitized weight be further broken down into a monetary value of dollars and cents. We intrinsically know that by approximating a continuous signal into a numerical or digital one, we can greatly improve the efficiency of our lives, but as we try and divided more complex signals with greater accuracy, the question often is how can efficiently perform this approximation.

Electronics has arisen as a tool to not only execute this division efficiently through analog to digital converters (ADCs), but also to perform the necessary math on those approximations millions of time faster than a human could. Some of applications we all use of these ADCs are shown in fig. 1. While ADCs enable much of our human-electronic interaction, the cost of these computations is energy and in a world where we want to have all the electronic tools available in every location of our lives, energy often become the limit of our devices.

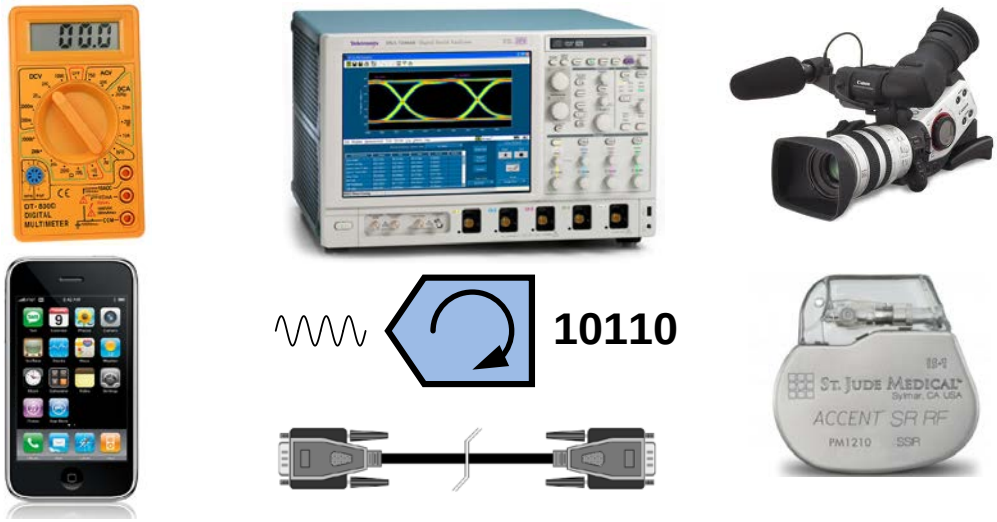

Figure 1.1: Examples of devices with analog to digital conversion

This thesis will examine the development of general purpose ADCs that are optimized for energy efficiency through the use of information that is typically discarded during the conversion process. Chapter 2 will start by examining the structure, history, and recent

developments of the SAR ADC, which is the current leader in ADC energy efficiency and will be the foundation of this work. Chapter 3 will then propose the ternary SAR which takes parasitic time information from the SAR comparator and uses it to increase the efficiency, accuracy, and speed of the traditional SAR. Chapter 4 will dive into the topic of residue shaping which was revealed in chapter 3, but has performance benefits for any multi-stage ADC by simply examining the statistics of the internal stages. Chapter 5 will then introduce a structure that emulates the benefits of the ternary SAR, but without using a time comparator, which can be useful in products where little redesign is required or in low resolution structures. Chapter 6 then puts many of these ideas together in the feedback initialized ternary SAR to make an optimized 2 stage ADC that improves on the ternary SAR efficiency by about a factor of 3. Some of these ideas from this chapter will then be shown in the context of R2R DACs in chapter 7, where power consumption per code is minimized. Chapter 8 will then conclude the work and describe some proposed and potential future work. References can be found in chapter 9.

2. THE SAR ADC

The successive approximation analog to digital converter (SAR ADC) provides a high-efficiency method for translating continuous real-world signals into digital bits for processing. While there are speed and resolution limitations with the structure, the substantial power savings that can be gained make the SAR achieve one of the best measures of efficiency for all ADCs. This chapter will introduce the concept of analog to digital conversion, show how the SAR fits into the set of ADC varieties, and then analyze the SAR ADC, its optimized variation the MCS SAR, and other recent state of the art developments.

2.1 Analog to Digital Conversion

In our world today, it's difficult (if not impossible) to translate real world information, such as temperature, volume, and pressure, directly into the 1s and 0s used in digital processing. However the benefit that is gained from this translation is extraordinary. Digital processing speeds are in the multi GHz range and digital ubiquity and portability have never been higher. A number of applications such as medical devices, communications equipment, audio/video recording, sensor networks, and many others depend on this processing for their functionality.

This section will investigate the process of analog to digital conversion by first defining the specifications that ADCs are compared with and then looking at top level ADC architectures and how they meet some of the given specs. Many of these definitions will be explained as they are critical for the understanding of the rest of the thesis.

1.1.1 ADC Specifications

When selecting an ADC for a given application, there are a number of block level input and output specifications that must be considered. Generically these can be broken up into accuracy, speed, power, and cost considerations and a some of the more common ones are shown in table 1. In this section we'll define a number of the important parameters that will remain useful throughout this work.

Specification	Units	Typical Value	Description
SNR	dB	66	Signal to Noise Ratio – Measure of Accuracy
SNDR	dB	60	Signal to Noise and Distortion Ratio
ENOB	Bits	10	Effective Number of Bits (6.02*SNDR + 1.76)
SFDR	dB	75	Spurious Free Dynamic Range – Distortion Level
Sample Rate	MS/s	20	Sampling Interval / ADC Operating Speed
Bandwidth	MHz	10	Maximum Input Frequency for Ideal Reconstruction
Power	Watts	75.2	Power From Supply for Operation at Max Sample Rate
Supply Voltage	Volts	1.2	Potential of Local ADC Power Supply
INL / DNL	LSBs	1 / 0.5	Integral Non-Linearity / Differential Non-Linearity
Area	mm²	0.1	ADC Chip Die Area
Technology	µm	0.13	Smallest Feature Length of Fabrication Process
Figure of Merit (FOM)	fJ/CS	20	Measure of Efficiency = Power / [(2^ENOB)*(2*Bandwidth)]

Table 2.1: Common ADC specifications with typical values for a 12b, 20MHz SAR ADC

1.1.1.1 Accuracy

The ADC is a converter in the sense that it converts a signal from the analog to the digital domain. How well these two domains match defines the accuracy of the ADC. Typically the accuracy is defined as a ratio of the input signal power and the noise or distortion power.

The most intrinsic source of noise is simple the rounding error from assigning a digital bit to a given analog input range. This is known as the quantization error. The quantization error for a given digital bin can be as small as zero when the input is directly in the bin center and $V_{LSB}/2$ when the input is on the bin edge. This makes the quantization noise power the following [1]:

$$NP_{RMS} = \sqrt{\frac{1}{V_{BIN}} \int_0^{V_{BIN}} \left[V_{LSB} \left(\frac{v}{V_{BIN}} - \frac{1}{2} \right) \right]^2 dV_{BIN}} = \frac{V_{BIN}}{\sqrt{12}} \tag{1.1}$$

Where V_{BIN} is the output bin sampling interval corresponding to the quantization bin of the ADC. The most fundamental ADC accuracy definition is the signal to quantization noise ratio (SQNR) which is the ratio of the input signal power to the quantization noise power defined in (1.2). This results in the following:

$$\mathrm{SQNR} = 20\log_{10}\left(\frac{V_{FS}}{2\sqrt{2}}\cdot\frac{\sqrt{12}\left(\mathrm{NLev}\right)}{V_{FS}}\right) \;=\; 20\log_{10}\left(\mathrm{NLev}\right)+1.76 \tag{1.2}$$

Where NLev is the number of levels in the ADC output and V_{FS} is the full-scale range of the ADC input. In terms of the number of bits:

$$\mathrm{SQNR} = \;6.02\mathrm{N}+1.76 \tag{1.3}$$

Where N is the number of inherent bits in the ADC. This would be the end of the story if the only error source was quantization noise. However it isn't and the other dominant error source is thermal noise, which is present in all electronic circuits. A more general accuracy definition is the signal to noise ratio (SNR) where noise is defined as all generic noise sources such as thermal noise and quantization error. Finally, often an ADC will have distortion which is an error that is correlated to the input signal. When this error source is combined with the other noise sources we get the signal to noise and distortion ratio (SNDR). This is the main accuracy specification used to define the quality of the ADC conversion. It can also be formulated in the effective number of bits (ENOB) with the following equation:

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{1.4}$$

A final dynamic accuracy specification that will be useful for this document is the spurious free dynamic range (SFDR) which is defined as the ratio of the signal power to the largest distortion term power.

In addition to the signal power based accuracy definitions, there are a number of static linearity definitions that define the accuracy of the output quantization bins of the ADC. The first is the differential non-linearity (DNL). This parameter is defined for each individual output code and is the difference between the current code output bin voltage and the previous code. In a typical ADC, you want this DNL to be less than the half of the voltage of an ideal LSB. The integral non-linearity (INL) is similarly defined as the difference between the current output code and an output code in an ideal output code spaced ADC. This can also be thought of as the cumulative sum of the DNL errors up to the current bin.

1.1.1.2 Bandwidth

The frequency of input that the ADC can convert to digital domain with no reconstruction losses is the input bandwidth. This is separate from the other speed requirement of the sample rate which is the speed with which the ADC is clocked. In a nyquist converter (like the typical SAR ADC), the input signal bandwidth is simply ½ the sample rate since the nyquist theorem [2] states that a signal must be sampled at a minimum of twice per period for non-lossy reconstruction. In oversampled converters, the bandwidth can be some factor times smaller than the (sample rate)/2 requirement due to the internal feedback structure. This bandwidth factor is called the oversampling rate (OSR).

1.1.1.3 Power

The amount of power that an ADC draws is a vital number for many modern applications. If the ADC is in portable devices, sensor nodes, or medical electronics, it's important that the power be minimized to reduce battery sizes, make the device more portable, and allow functionality in energy harvesting settings. Typically the power is measured in watts, and is defined as the average current drawn from the supply times the given ADC supply voltage. In SAR ADCs, energy is also often examined where energy (J) is simply the charge used times the supply or the power multiplied by some time window. Also in capacitive and digital systems (sometime SAR ADCs) power can be calculated dynamically as derived below:

$$P_{VDD} = I * V_{DD} = \frac{Q}{T} V_{DD} = \frac{\alpha C_T V}{T} V_{DD} = \alpha C_T {V_{DD}}^2 f \tag{1.5}$$

Where α is the capacitance activity factor (what percentage of the total capacitance is switched in each cycle) and f is the switching frequency of the capacitance.

In the digital world, energy consumption has been rapidly decreasing as the number of computations per joule has been doubling nearly every 1.5 years [3]. In the ADC world however, the number of samples per joule is only doubling about every 3.3 years, making ADCs more and more of a bottleneck in the power balance of portable electronics [4]. This is one of the reasons for the focus on the SAR ADC structure as it provides a mid-range ADC conversion with significantly improved efficiency.

1.1.1.4 Cost

Depending on what your role is, perhaps the most important of all ADC parameters is cost. The three main components of the ADC cost include design effort, die area, and fabrication costs.

These all relate to SAR ADCs as the structure tends to have a low design time since there are few analog blocks, have a small die area due to the cyclic nature, and are able to be fabricated in a variety of digital and analog processes with no special devices. Also calibration plays a role in many modern ADC designs and background calibration techniques can reduce the trim time during fabrication.

1.1.1.5 Figure of Merit

In order to properly compare various types of ADCs, an efficiency benchmark called the figure of merit (FOM) was created in [1]. The commonly accepted FOM is defined as the following:

$$FOM = \frac{P_{VDD}}{\left(2^{ENOB}\right)\left(2 * BW\right)} \tag{1.6}$$

Where the bandwidth is typically the maximum input bandwidth however this BW term is sometimes debated.

1.1.2 ADC Varieties

Due to the wide range of ADC specifications, there are a number of ADC architectures that are designed to most efficiently meet each requirement. Fig. 1 [5] shows a number of example specifications plotted in terms of their resolution and bandwidth needs. The most common ADC varieties employed to meet the required bandwidth and accuracy specifications are shown in fig 2. This figure is of course approximate, as there is both overlap in many of the specifications (multiple architectures can meet a given spec) and debate among ADC designers where the boundaries should lie.

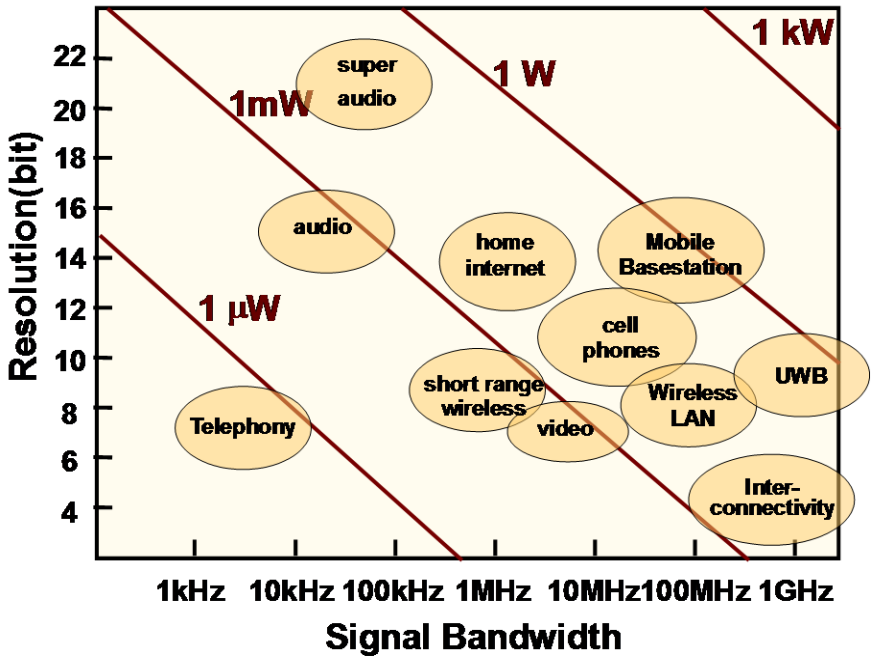

Figure 2.2: ADC applications vs. resolution and bandwidth

ENOB / BW	100 HZ	1k Hz	10k Hz	100k Hz	300k Hz	1M Hz	3M Hz	10M Hz	30M Hz	100M Hz	300M Hz	1G Hz	3G Hz
18	INC	INC	ΔΣ	ΔΣ	ΔΣ	ΔΣ	ΔΣ	ΔΣ	Pipe	Pipe	Pipe	Pipe	Pipe
17	INC	INC	ΔΣ	ΔΣ	ΔΣ	ΔΣ	ΔΣ	ΔΣ	Pipe	Pipe	Pipe	Pipe	Pipe
16	INC	INC	ΔΣ	ΔΣ	ΔΣ	ΔΣ	ΔΣ	ΔΣ	Pipe	Pipe	Pipe	Pipe	Pipe
15	SAR	SAR	SAR	SAR	SAR	SAR	Pipe	Pipe	Pipe	Pipe	Pipe	Pipe	Pipe
14	SAR	SAR	SAR	SAR	SAR	SAR	SAR	Pipe	Pipe	Pipe	Pipe	Pipe	Pipe
13	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	Pipe	Pipe	Pipe	Pipe	Pipe
12	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	Pipe	Pipe	Pipe	Pipe
11	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	Pipe	Pipe	Pipe	Pipe
10	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	Pipe	Pipe	Pipe
9	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	Pipe	Pipe	Pipe
8	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	Pipe	Pipe
7	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR	Pipe	Pipe
6	F	F	F	F	F	F	F	F	F	F	F	F	F
5	F	F	F	F	F	F	F	F	F	F	F	F	F
4	F	F	F	F	F	F	F	F	F	F	F	F	F

Figure 2.3: Generally used ADC variety for given resolution and bandwidth specifications

The most common ADC topologies are the Flash, SAR, Pipeline, Delta Sigma, and Incremental. Others that have been regularly used over the past few years include the dual slope, folding and interpolating, algorithmic, binary search, and voltage controlled oscillator (VCO) or counting based structures. The flash is the most fundamental of all the ADC types consisting of a string of comparators with the negative input tied to the input voltage, and the positive side tied to a reference voltage. This converter is a single stage, thus it has a large bandwidth, but requires 2^N comparators meaning that is quickly loses its energy efficiency for larger resolutions. The rest of the ADC types are essentially special feedback loops that can be formed around the basic flash converter.

The pipeline takes a small flash converter and subtracts the analog input from the digital flash output. This analog output residue is then multiplied by the stage flash resolution. This forms a pipeline stage where the input is an analog input voltage, and the output is the digital bits from the flash and the analog residue voltage. This architecture increases the energy efficiency and speed of the flash since only 2*N comparators (in a 1 bit case) are now required (however, amplifiers are now needed). This architecture will be discussed in detail when the idea of residue shaping is addressed later in the thesis.

The delta sigma ADC also uses a flash (or other low resolution ADC) as the central quantizer unit, however adds integrating feedback around the quantizer. By adding this feedback in such a way that the output quantization error is shifted to a high frequency and the input is contained to a low frequency, the output resolution can be dramatically increased by filtering out the high frequency noise digitally. This make the architecture have the ability of achieving very high accuracy but only at lower input bandwidths. By resetting the integrators with a very low bandwidth, an extremely accurate incremental ADC can be formed. These two structures won't be discussed in detail in this thesis, however more information on this structure can be found in [6]-[7].

While not shown in fig. 4, the counting ADC (dual slope, VCO, or delay line) is important for this work. The counting ADC converts the input voltage first into a time by either setting the input as the control voltage of a VCO, delay line or RC integrator. By counting the resulting time value (cycles in a VCO, inverters in a delay line, or zero crossing time in a dual slope) a digital flash-like value is obtained. Like a flash though, 2^N data latches are required, but these can be made

with low energy or noise shaping properties. Time domain quantization will be described later in this thesis.

2.2 Successive Approximation Converters

The SAR ADC is so named because the input signal is quantized by using steps of successive approximations (the register part come from how early ADCs were built). However, the successive approximation method goes back much farther than with the ADC. By looking not only at these roots and the evolutions of the electrical SAR, we can learn about not only how the SAR functions, but why today it has become the converter of choice for high efficiency mid-range conversions.

2.2.1 The Successive Approximation Algorithm

Successive approximation is a method that has been used for generations and is a concept that today we teach our children when they are young. To illustrate the method imagine you are asking a friend to guess a number between 1 and 100. Once you guess a number your friend will tell you if you are too high or too low and you must keep guessing until you get the number exactly (no decimal places here). If you are too busy for silly games, how will you guess the number the fastest? The answer is, assuming you have no additional information, to first guess 50. This is because after the first guess, your range of possible values for the guessed number is cut exactly in half. Having ½ times as many numbers to guess is the minimum possible range decrease you can have, for example a guess of 55 would mean the lower guessing range is not half but 55/100 which could require more guessing time. Thus the method with the shortest worst case guessing time is to always guess a number halfway inbetween the range of numbers that you know have not been eliminated.

While the example of guessing a number seems childish, this problem did arise many times throughout history and perhaps the most important (because money was involved) was in the historic problem of the scales. The scales question involves an ideal set of two pans balanced inbetween a fulcrum (think scales from the middle ages). To measure things, an item was placed on one of the pans and weights were placed in the other pan. Initially, the scale was tipped towards the side with the item and weights were placed on the opposite side until the scale tipped to the weights side. Then smaller weights could either be added to the item side or subtracted from the weights side in an effort to make both pans equal. This could be a very

time consuming process especially when things like expensive spices were being accurately measured. Thus the question arose, how can an unknown item's weight be measured with the fewest number of steps?

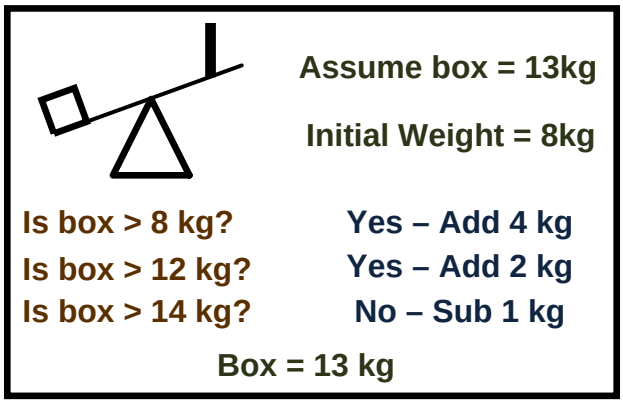

Figure 2.4: Successive approximation manifested though historic weight determination

This question remained formerly unsolved until the mathematician Tartaglia tackled it in 1556 [8]. Tartaglia was a French self-taught scholar who was the son of a low class delivery man [9]. Thus while he published many great theoretical works, he had a knack for also solving everyday practical problems, such as analyzing the trajectory of cannonballs, optimizing the recovery of sunken ships, and solving the problem of the weights and scales. Tartaglia's solution is known as feedback subtraction or optimized successive approximation. He proved that for an unknown item whose upper weight limit was bounded, the minimal number of steps needed to determine the weight to a given accuracy was to simply start with a weight equal to exactly ½ of the full-scale range weight of the unknown item [10]. Then if the scale tips in favor of the item still, a weight of exactly ¼ the full-scale max weight is added to the test weight side, and if the scale does not tip towards the item in question, the ½ weight is removed and the ¼ weight is placed on the test side. Essentially, Tartaglia was describing a method where after each guess of ½ the known range is made, the feedback of the polarity of the scale tilt allows him to know whether to add or subtract the next test weight of ½ the previous test weight. Thus by having a set of test weights of 1/(2^N) (binary weighted) tartaglia could determine the weight of an item to within N bit accuracy in only N steps. This is illustrated in an example in fig. 5. This became the standard method of solving for the weight of an unknown item for centuries and is used to day in the electrical SAR ADC. It should also be noted that Tartaglia published a somewhat mysterious second proof that if the weigher had the ability to place weights on either side of the

scale after a comparison, then the optimal test weight distribution is 1/(3^N). While implementing the binary feedback subtraction is simple, figuring out how to implement this ternary feedback has been a constant thought of the author and often distracts him as he tried to sleep.

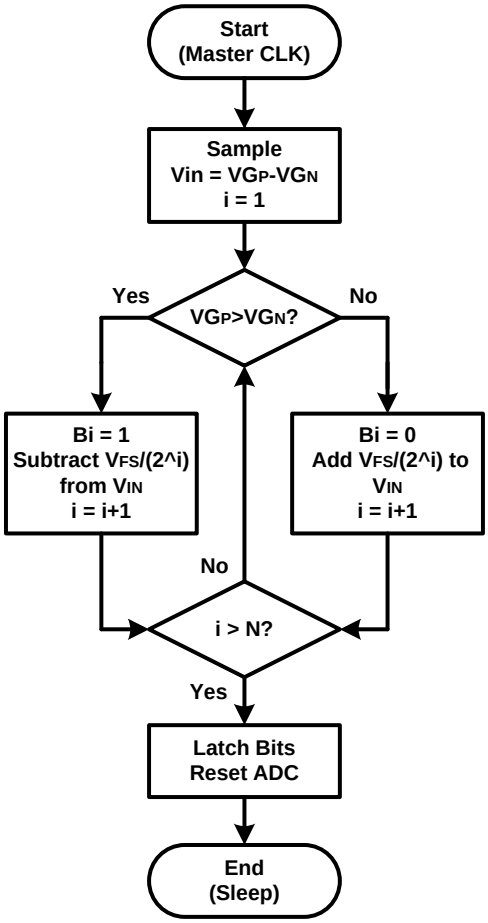

Figure 2.5: SAR ADC operational flowchart

2.2.2 Electrical Successive Approximation

While the idea of feedback subtraction in the marketplace has existed for centuries it was not until the advent of modern electronics in the 1940s that people started to apply the successive approximation algorithm to analog to digital conversion. Really the problem in the electrical domain has many similarities. There is an unknown electrical potential (box) that must be converted to a discrete value (converted to digital) and the tools we have to perform this

conversion include comparators (scales) and a feedback digital to analog converter (test weights).

The generic electrical SAR ADC flow chart is shown in Fig. 4. In the electrical domain, the input signal voltage must first be sampled onto the ADC virtual ground nodes. This can either be in the voltage or current domains, but today is typically done in with voltages on sampling capacitors. After this the sampled input is quantized or compared, telling whether the input is larger or smaller than a reference or, in the case of a differential SAR, determining the input polarity. After this first comparison, the bit is recorded in the SAR and the feedback subtraction DAC will either add or subtract from the input signal a voltage (or current) equal to half of the input full-scale range. Then the cycle of comparison, bit recording, and feedback subtraction continues, with each cycle's full-scale input range decreasing by a factor of 2. After the full accuracy has been determined, the SAR will stop. For a 1b per stage SAR, this happens after N stages where N is the resolution in bits. Following this SAR completion, the data bits are latched (and outputted) and the SAR is put to sleep until the next cycle.

2.2.3 Historical SAR Varieties and SAR Prior Art

To best understand both the operation and current state of the SAR ADC, it's important to take a look at both the historical and recent prior SAR ADC art that has influenced the trajectory of innovation. In this section, the SAR operation will be explained and the limitations of past and current structures will be highlighted.

1.2.3.1 Current Mode SAR

The electrical ADC itself traces its roots back to the 1930's with the expansion of communications. Pulse code modulation (PCM) would require that analog voice inputs be quantized for digital transmission that could be multiplexed, however many of these ADCs were made with the only known structures at the time, flash or counting based ADCs [10]. It wasn't until 1947 that W. M. Goodall of Bell Labs introduced a "feedback subtraction coder" that replaced the counting ADC with a primitive SAR structure [11]. The motivation (inferred from the original paper) was to speed up the coding process in such a way that PCM channels could be multiplexed digitally. To make digital communications possible, analog speech signals needed to be sampled at 8000 times per second, with 5 bits of accuracy (6 bits allowed for "high quality" voice signals, however 3 was sufficient for understanding syllables and the paper

reports that even 1 bit was enough to allow for some discernible words). Thus one channel needed to transmit 40,000 bits per second. By using a SAR ADC over the counting, the multiple PCM channels could be now be multiplexed into a single wire, thus the SAR ADC effectively killed the analog telephone.

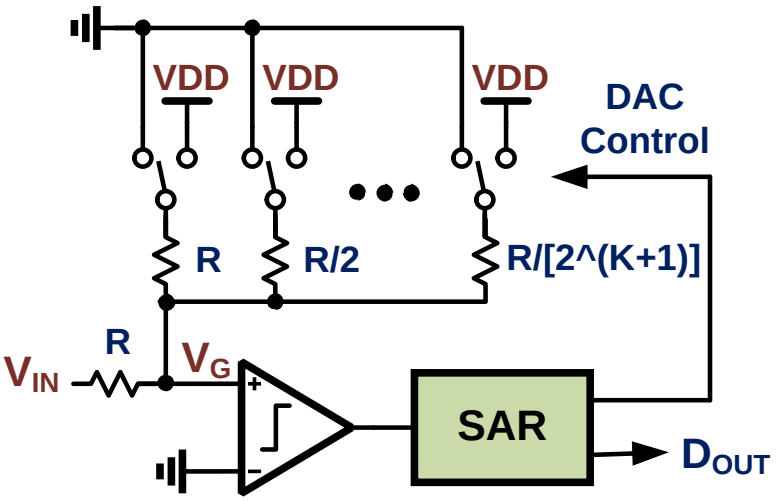

Figure 2.6: Early current mode SAR ADC

While the communications world continued the improvement of electronic telephony, the SAR ADC (or "coder" as it was known) did not gain significant attention until a breakthrough 1953 paper by B. Smith describing the resistor based SAR ADC that would essentially be the ADC of choice for the next 20 years [12]. This SAR divides the input based on the voltage division of the input resistor and the resistor DAC to create a virtual ground voltage VG. This voltage is then compared with a reference to give the 1b quantization in each stage. The feedback subtraction is performed with the binary weighted resistor array that will change the effective Norton equivalent voltage seen by the input. In each phase, the voltage subtraction that occurs will reduce the given full-scale stage range by a factor of two, performing the classical feedback subtraction algorithm.

1.2.3.2 The McCleary Charge-Redistribution SAR

As complementary metal oxide semiconductor (CMOS) technology began to take hold in the 1970s, a major shift in circuit performance took place. Now, logic circuits could burn practically no static power (only dynamic) and having a SAR ADC with a current mode feedback DAC would burn significantly more power than the neighboring logic. Thus, in 1975, the charge-

redistribution SAR was born by replacing the resistive DAC with a capacitive one (since capacitor technology had improved too). The capacitor based SAR is what is currently used today (in modified forms) and is the foundation for the rest of this thesis.

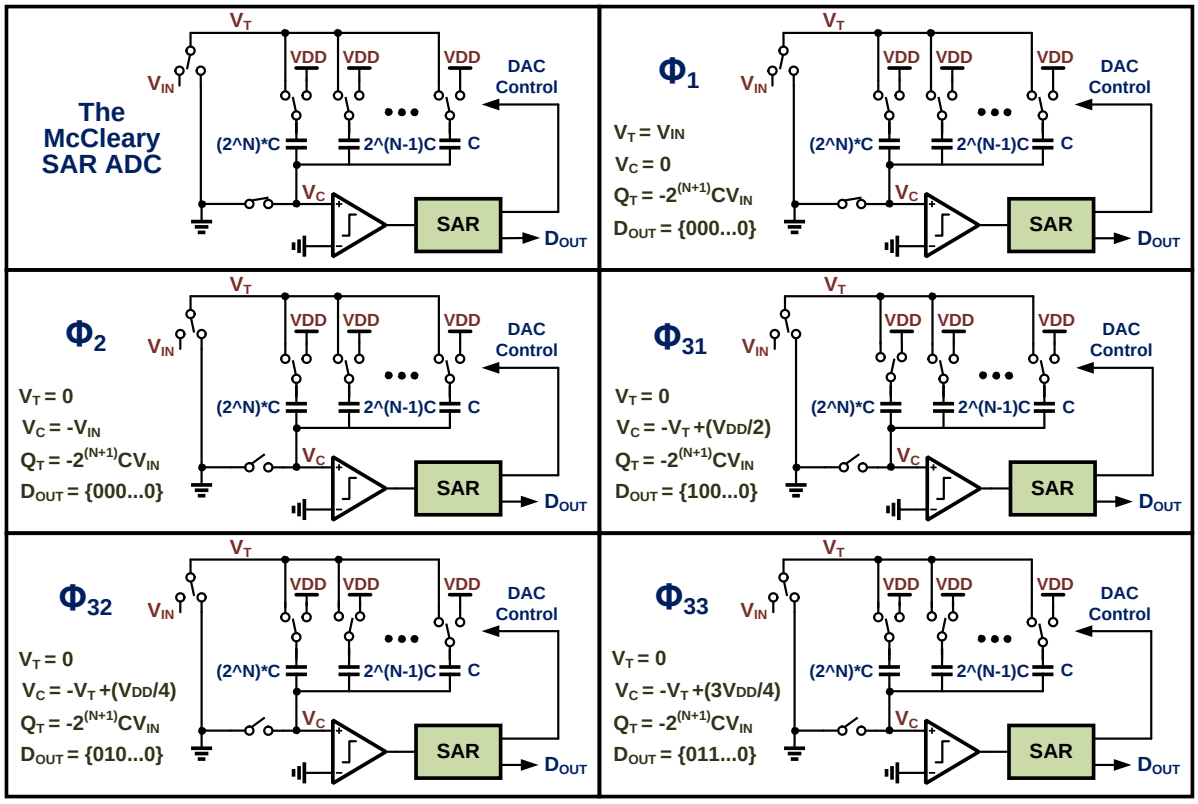

Figure 2.7: The McCleary SAR ADC operation

The paper that ushered in the charge-redistribution SAR was [13] in 1975 by McCleary in the journal of solid state circuits (JSSC) (Actually there were two papers, one with charge redistribution and one with two capacitor charge sharing). The McCleary SAR is shown in fig. 6 along with an example switching operation. This SAR is a singled ended cyclic converter with much the same structure as the previous current mode SAR, with a few important changed. The first is that the DAC operation is performed in the voltage domain. In the current mode SAR, the comparator did technically examine a voltage as well, but it was generated by current though a resistor, meaning that the input signal had to constantly be present to the SAR. Now however, the input is sampled onto a purely capacitive virtual ground node and that node is compared to a reference. The voltage on that node is then changed by adding or subtracting charge to the node though the capacitive, binary weighted DAC (since Q = CV).

Fig. 6 examines the process of this SAR. Initially in ϕ1, the input is sampled onto the bottom plates of all the DAC capacitors while the capacitor bottom plates are all tied to ground (or the same as the reference voltage). Then in ϕ2, the bottom plate of all the capacitors is left floating and the top plate is grounded. This will move the charge to the virtual ground node such that the V_C voltage is equal to –VIN. From here, the SAR is fully initialized and is ready to begin the conversion of the input in ϕ3. Here, in ϕ31, the MSB capacitor is shifted to VDD from GND resulting in the following virtual ground voltage:

$$V_C\left(\Phi_{31}\right) = -V_{IN} + V_{DD}\frac{C_{MSB}}{C_{Total}} = -V_{IN} + \frac{V_{DD}}{2} \tag{1.7}$$

This initial virtual ground voltage is compared with the comparator reference (traditionally 0V) and the comparator output of "1" or "0" due to the polarity of the input is recorded in the SAR registers. In ϕ32, the feedback DAC will subtract a voltage of either $V_{DD}/4$ or $-V_{DD}/4$ depending on the previous "1" or "0" code generated by the comparator. In the example of fig. 6, the initial V_C voltage [$V_C(\phi 31)$] was positive, thus the DAC needs to subtract $V_{DD}/4$. The subtraction is done by resetting the MSB capacitor to GND and setting the MSB-1 capacitor to V_{DD}. The addition would have been done by only setting the MSB-1 capacitor to V_{DD} and not resetting the MSB capacitor if needed. Following this DAC movement, the input polarity is again determined and the next cycle is begun.

The SAR cycles will continue, each time adding or subtracting a voltage that is half of the previous stage's subtraction voltage based on the binary weighted capacitor array and will stop when the number of bits resolved is equal to the desired resolution.

1.2.3.3 The Montonic SAR

After the McCleary SAR, a number of improvements had been made to the general SAR structure including calibration [14]-[15], bandwidth increases [16]-[17], and noise and distortion conscious designs [18]-[19]. Since about the year 2000 though, there has been a focus in the world of electronics on portability and power consumption and this has spawned the development of many novel power conscious SAR architectures [20]-[21]. One of the more famous of these structures is the monotonic SAR shown in fig. 7. The monotonic SAR attempts to solve one of the major efficiency limiting problems of the McCleary SAR which is that before every bit is determined, the DAC must first be moved in order to "test" the polarity of the input

signal. This means that when the input is initially sampled onto the DAC and comparator virtual ground nodes, it is sampled in reference to GND. Before the first conversion happens, VDD/2 must then be added to the input. In the monotonic SAR [22], the input signal is directly sampled onto the top plates of the capacitors (top plate sampling) with all of the bottom plates tied to VDD (with a common mode of VCM). In the first cycle, if the comparator output is a "1", then the top MSB capacitor is switched from VDD to GND resulting in a subtraction of VDD/2 on the differential input (and since it is differential the input can span +- VDD). This subtraction method means that there is no DAC testing phase, which saves a considerable amount of switching and driver power over the McCleary SAR. With this switching however, come the fact that the input common mode reduces with each step, greatly impacting the linearity of the SAR and making comparator design more challenging. In the next section we will show the MCS SAR which is currently the state of the art architecture that allows for even greater switching energy reduction without linearity concerns.

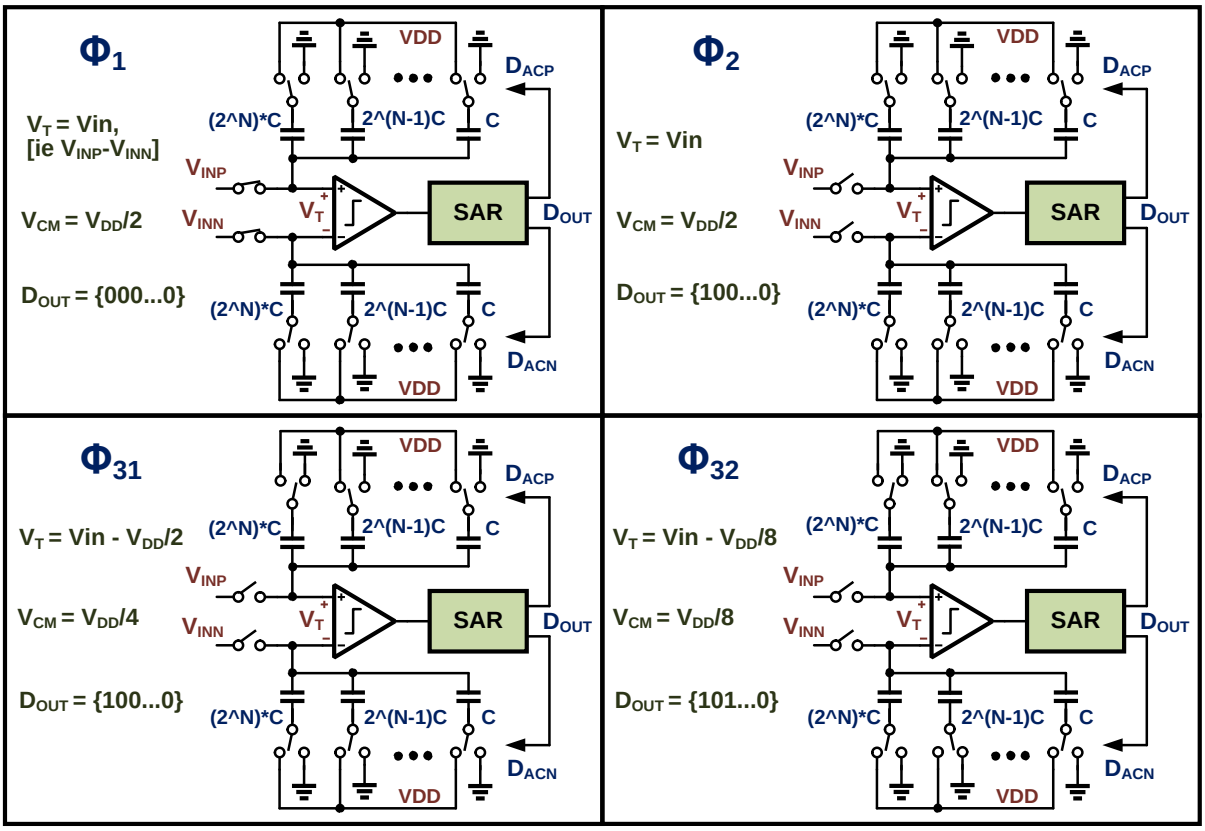

Figure 2.8: The monotonic SAR operation

2.3 The MCS SAR

While there have been many SAR varieties over the years, the current state of the art general SAR structure tends to be what is known as the merged capacitor switching (MCS) or VCM-based SAR [23]-[24]. This structure significantly lowers DAC switching energy over the other older SAR structures (McCleary, Set and Down, Monotonic) and does this with no common mode shift from the first to last cycle. The MCS SAR is the framework for this thesis, as the proposed SAR ideas are improvements to this SAR, which is today generally regarded as the most efficient structure for most applications. Because of this foundational position, the rest of this section will be devoted to describing the operation and relevant block level analysis of the MCS architecture before building on them later in the thesis.

2.3.1 MCS SAR Operation

Like previous structures, the MCS SAR consists of a comparator acting as a 1-bit quantizer, feeding into a SAR logic block with a feedback DAC minimizing the comparator input. The main structural difference is now that the feedback capacitive DAC has three reference levels instead of the traditional two (even though many two-level SARs required a third common mode anyway) and is shown in fig. 8.

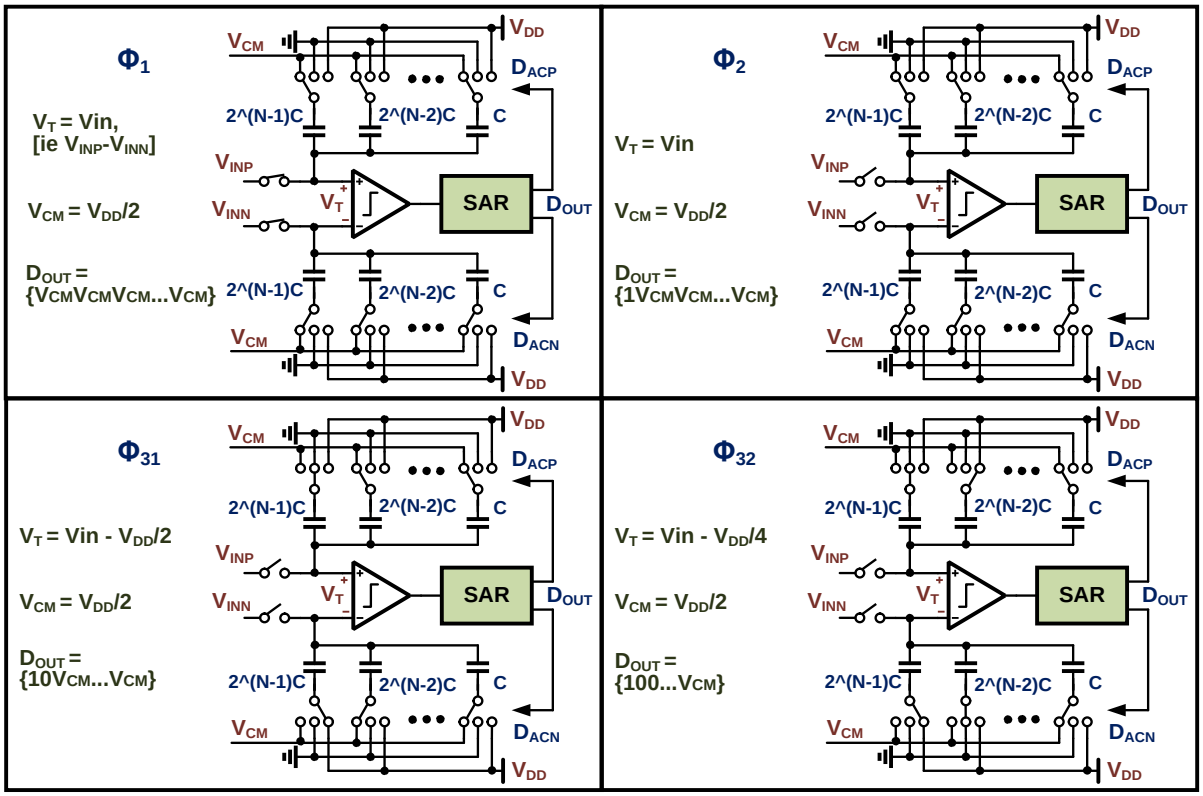

Figure 2.9: The merged capacitor switching (MCS) SAR ADC operation

The MCS operation begins by preforming a top-plate sampling much like the monotonic SAR, except the bottom plate of the capacitor DAC is now tied to the common mode reference (Note the MCS structure also allows for bottom plate sampling, but that isn't shown here). This also means that initially the bits in the MCS SAR are not a logical "1" or "0" but are halfway in between or at VCM. In the monotonic SAR, the subtraction happened when a capacitor switched from VDD to GND. Here though, that subtraction occurs when the stage capacitors switch differentially from VCM to VDD and VCM to GND. In fig. 8, phase 31 shows the switching operation when the comparator output is a "1" with the bottom plate of the positive MSB capacitor moving to GND and the bottom plate of the negative MSB capacitor moving to VDD. By differentially switching, the common mode voltage stays constant throughout the SAR conversion, allowing for high accuracy fine stage comparisons, and the switching energy is dramatically improved. Another important structural note is that there is no net current taken from the VCM node since every time VCM is switched onto a capacitor with a net charge residing on it, another capacitor is also being switched to VCM with the opposite polarity charge. The same effect holds true during the reset phase of the SAR operation.

2.3.2 MCS SAR Block Level Structure – Capacitor Array

The MCS SAR can be best understood by breaking it up into respective blocks shown in fig. 9 which include the capacitor array, cap drivers, comparator, logic, and interface circuitry. The operations, sizing, efficiency and limitations of these blocks will be summarized in the following sections and will be further explored in later chapters.

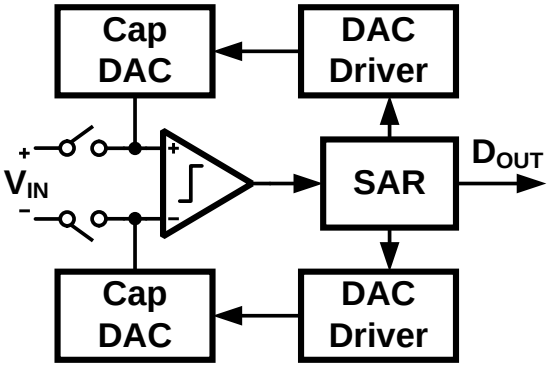

Figure 2.10: SAR block diagram showing major components

The capacitor array for the MCS SAR is used for both sampling the input onto the virtual ground node and performing the respective subtractions. The MCS array is shown in fig. 8 and care must be taken to size the array for thermal noise and mismatch specifications. To formulate the sizing, the magnitude of the quantization noise must first be known, and then the thermal noise that is added must be small in comparison. The quantization noise [1] can be formulated as the following (from integrating the digital error over an output bin):

$$\overline{V_{OUT,Q}{}^2} = \frac{Q^2}{12} = \frac{V_{DD}{}^2}{2^{2N}(12)} \tag{1.8}$$

Where N is the number of bits in the SAR ADC. The thermal noise can then be formulated as a function of the capacitance by multiplying the input thermal noise by the noise bandwidth [6]:

$$\overline{V_{OUT,T}{}^2} = \int_0^\infty 4kTR\left|\frac{1}{1+j2\pi fRC}\right|^2 df = \frac{4kTR}{4RC} = \frac{kT}{C} \tag{1.9}$$

Where k is Boltzman's constant and T is the temperature in kelvin and C is the total input capacitance. By combining the two equations, the total sampling capacitance can be determined to be the following:

$$C_T = \frac{kT\left(2^{2N}\right)(12)}{{V_{DD}}^2}\left(NF\right)\left(MF\right) \tag{1.10}$$

Where NF is the noise factor and MF is the mismatch factor. When designing a SAR ADC, it is not possible to get the full N bit resolution you are looking for because there will always be a small amount of thermal noise sitting on top of the input signal and the proximity the designer wishes to get to that ideal noise value determines the noise factor. For example, choosing an NF of 1 means that the thermal noise variance will equal the quantization noise variance, effectively causing the loss of 1 bit. Noise factors of 2 or 4 therefore are more reasonable. The mismatch factor is similarly present since in mismatch limited systems, the thermal noise requirements are not enough and the capacitors must be made some MF factor larger to match to within a given accuracy. It's also important to note that this noise condition also holds for a differential SAR since the signal to noise ratio will be maintained without changing the total capacitance.

While accurately determining the thermal noise of the SAR based on the capacitor array is important, switching energy of the array is also an often discussed topic and will be focus of the discussion in later chapters as well. To find the total DAC energy in the MCS operation, it's important to examine the switching operation one stage at a time. The energy in joules is calculated by seeing the change in voltage across the supply tied capacitor and multiplying that by the respective capacitance to get the charge, then multiplying this charge by the overall potential to get energy ($E=C(\Delta V)V_{DD}$). As an example, in the first stage, the SAR has the following switching energy:

$$\phi_1 : E_{VDD} = \left[\left(\frac{1}{2} - \frac{C_{MSB}}{2C_T}\right)V_{DD}C_{MSB}\right]V_{DD} = \frac{C_T{V_{DD}}^2}{8} \tag{1.11}$$

Where CT is the total SAR capacitance on one side of a differential SAR (CT is ½ of the total capacitance seen by the input differentially). While the first stage simply has supply charging on one capacitor, later stages must also take into account the virtual ground movement's effect of the previously supply connected capacitors. For example, the second stage switching energy for a 10 transition would be the following:

$$\phi_{2,10} : E_{VDD} = \left[\left(\frac{1}{2} - \frac{C_{MSB-1}}{2C_T}\right)V_{DD}C_{MSB-1}\right]V_{DD} + C_{MSB}\left(\frac{C_{MSB-1}}{2C_T}\right){V_{DD}}^2 = \frac{5C_T{V_{DD}}^2}{32} \tag{1.12}$$

This result shows that the energy of the MCS SAR is code dependent and is greater when the transition polarities are not constant across the DAC. To generalize this result for a given stage M looking back at the previous S stages, we have:

$$\phi_N : E_{VDD} = {V_{DD}}^2 \left[\left(\sum_{S=1}^{M-1} C_S \left(b_S \oplus b_N \right) \right) \left(0 + \frac{C_N}{2C_T} \right) + \left(\sum_{S=1}^{M-1} C_S \overline{\left(b_S \oplus b_N \right)} \right) \left(0 - \frac{C_N}{2C_T} \right) + \left(\frac{1}{2} - \frac{C_N}{2C_T} \right) \right]$$

$$= \frac{C_N {V_{DD}}^2}{2C_T} \left[\sum_{S=1}^{N-1} C_S (-1)^{\overline{(b_N \oplus b_S)}} - C_N + C_T \right] \tag{1.13}$$

Where the polarity of the final summation is determined by the XOR of the current stage bit and the Nth stage bit. From this equation, one can find the total power of a given code for the MCS SAR as follows:

$$E_{VDD}(Code) = \frac{{V_{DD}}^2}{2C_T} \left[\sum_{M=1}^{N-1} C_M \left(\left(\sum_{S=1}^{M-1} C_S (-1)^{\overline{(b_N \oplus b_S)}} \right) - C_N + C_T \right) \right] \tag{1.14}$$

This equation will be used as a baseline for other switching energy reduction schemes later in the thesis. From this formula, we can also find the max, min, and average switching energy of the MCS SAR. First the minimum energy is known to be when all of the capacitors switch to the same potential. Even though switching the whole SAR array to a given potential requires no power, because it is done in steps, the following finite power is drawn:

$$E_{VDD,MIN} = \frac{{V_{DD}}^2}{2C_T} \left[\left(\sum_{M=1}^{N-1} \left(C_N C_T - {C_N}^2 \right) \right) - \left(\sum_{M=1}^{N-1} C_N \sum_{S=1}^{M-1} C_S \right) \right]$$

$$= \frac{{V_{DD}}^2}{2C_T} \left[\left(\frac{{C_T}^2}{2} - \frac{{C_T}^2}{4} + \frac{{C_T}^2}{4} - \frac{{C_T}^2}{16} + \frac{{C_T}^2}{8} - \frac{{C_T}^2}{64} \ldots \right) - \left(\sum_{M=1}^{N-1} C_N \sum_{S=1}^{M-1} C_S \right) \right] \tag{1.15}$$

$$\approx \frac{{V_{DD}}^2}{2C_T} \left[\frac{43{C_T}^2}{64} - \left(\frac{{C_T}^2}{8} + \frac{{C_T}^2}{16} + \frac{{C_T}^2}{32} + \frac{{C_T}^2}{32} + \frac{{C_T}^2}{64} + \frac{{C_T}^2}{128} \ldots \right) \right]$$

$$\approx \frac{{V_{DD}}^2}{2C_T} \left[\frac{43{C_T}^2}{64} - \left(\frac{21{C_T}^2}{64} \right) \right] = \frac{22{V_{DD}}^2 C_T}{128}$$

One interesting note is that the thermal noise equation for determining capacitance is inversely proportional to the input magnitude and the energy is directly proportional. Combining (1.15) with (1.10) we get the following:

$$E_{VDD,MIN} = \frac{22(kT)(12)(2^{2N})}{128}(NF)(MF) \tag{1.16}$$

If we assume that the noise factor equals 2 and the mismatch factor is 1 (perhaps with calibration) we can estimate the minimum possible figure of merit for a SAR ADC based on switching efficiency alone to be the following:

$$FOM_{MCS,MIN} = \frac{(22)(kT)(12)(2^{2N})(2)}{128} \cong (2^{N})16.95x10^{-21}\ {}^{J}\!/_{CS} \tag{1.17}$$

This result shows a number of startling conclusions. First the minimum switching energy based figure of merit is independent of the input signal or supply voltage and device sizes, showing that perhaps SAR ADCs don't scale as well as previously hoped. Also, it is simply dependent on resolution and the FOM doubles with each bit increase. Thus for a 12b MCS SAR, the minimum FOM from the capacitor array alone is about 100aF (the equation gives 70aF, but the excess thermal noise will actually increase the minimum FOM by a small factor). This of course is that absolute minimum, but more reasonable lowest FOM estimates for MCS SAR ADCs will be shown later.

While the minimum switching energy is important for determining power bounds, the average and max power is also important in system design and they are the following:

$$E_{VDD,MAX} = \frac{{V_{DD}}^2}{2C_T}\left[\left(\sum_{M=1}^{N-1}\left(C_N C_T - {C_N}^2\right)\right)+\left(\sum_{M=1}^{N-1} C_N \sum_{S=1}^{M-1} C_S(-1)^{\overline{b_N \oplus b_S}}\right)\right] \quad for\ b_{OUT} = \{1,0,0,0\ldots\}$$

$$\approx \frac{{V_{DD}}^2}{2C_T}\left[\frac{43{C_T}^2}{64}+\left(\frac{{C_T}^2}{8}+\frac{{C_T}^2}{16}-\frac{{C_T}^2}{32}+\frac{{C_T}^2}{32}-\frac{{C_T}^2}{64}-\frac{{C_T}^2}{128}\ldots\right)\right]$$

$$\approx \frac{{V_{DD}}^2}{2C_T}\left[\frac{43{C_T}^2}{64}+\left(\frac{11{C_T}^2}{64}\right)\right] = \frac{54{V_{DD}}^2 C_T}{128}$$

(1.18)

$$E_{VDD,Ave} = \frac{V_{DD}{}^2}{2C_T}\left[\left(\sum_{M=1}^{N-1}\left(C_N C_T - C_N{}^2\right)\right)+\left(\sum_{M=1}^{N-1} C_N \sum_{S=1}^{M-1} C_S(-1)^{\overline{b_N \oplus b_S}}\right)\right] \quad for\ b_{OUT} = \{1,1,0,0\ldots\}$$

$$\approx \frac{V_{DD}{}^2}{2C_T}\left[\frac{43C_T{}^2}{64}+\left(-\frac{C_T{}^2}{8}+\frac{C_T{}^2}{16}+\frac{C_T{}^2}{32}+\frac{C_T{}^2}{32}+\frac{C_T{}^2}{64}-\frac{C_T{}^2}{128}\ldots\right)\right]$$

$$\approx \frac{V_{DD}{}^2}{2C_T}\left[\frac{43C_T{}^2}{64}+\left(\frac{C_T{}^2}{64}\right)\right]=\frac{44V_{DD}{}^2C_T}{128}$$

(1.19)

In the above equations, the max power is determined when only the first bit is VDD and the rest are GND resulting in the maximum charging from virtual ground. The average code is then when only the first two bits are the same and the rest are of the opposite polarity. If the average switching energy were used to determine the SAR minimum figure of merit it would be around 200aJ/CS.

2.3.3 MCS SAR Block Level Structure – DAC Drivers

The DAC of the SAR is essential for creating the feedback subtraction necessary for the input minimization and digital word generation, but it is not the only part of the feedback loop. Drivers for the DAC are needed and are designed to meet the given speed, accuracy, and power requirements. Often in moderate speed applications, the DAC drivers consist of inverter buffers, sized to allow the given DAC caps to charge to a value that meets the settling accuracy requirements set by the signal to quantization noise ratio (SQNR). Due to the resistive nature of the charging, the inverted sizes can be determined from fundamental RC charging equations (to a first order). An MCS three level DAC driver is shown for a given single capacitor in fig. 10.

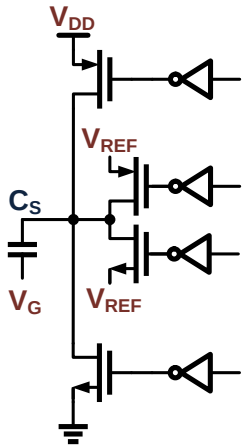

Figure 2.11: DAC inverter based drivers

To determine the switch size and diver power, the charging time of the feedback loop can first be modeled as the following RC charging:

$$\Delta V = V_S\left(1-e^{T/\tau}\right) \tag{1.20}$$

Where delta V is the voltage change on the bottom plate of the portion of the capacitor array being charged and tao is the charging time constant. Since the settling accuracy in the MCS SAR is defined by the quantization noise level of the ADC (since there is no redundancy), the charging can be modeled as the following:

$$1-\frac{1}{2^{N+1}} = 1-e^{T/RC} \tag{1.21}$$

Where N is the number of bits in the ADC, R is the inverter resistance, and C is the capacitance being charged in the given cycle. Note that since the capacitance drops in each cycle, the size of the drivers can be calculated for the MS charging cycle, and then appropriately scaled for the remaining phases. Rearranging the equation in terms of the time constant, we have:

$$\frac{1}{RC} = \frac{\ln\left(2^{N+1}\right)}{T} \tag{1.22}$$

Here, the trickier part of the driver sizing comes in determining the equivalent resistance of the inverter. Using the sub-threshold digital switching estimation made in [25], we can approximate the resistance as the following:

$$R_{Ave} = \left(\frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\right)\left(1-\frac{5}{6}\lambda V_{DD}\right) \cong \frac{3V_{DD}L}{4K'WV_{DSAT}\left[\left(V_{DD}-V_T\right)-V_{DSAT}/2\right]} \tag{1.23}$$

The equivalent capacitance is what is seen by the inverter during the MSB charging event and is often mistaken for being simply half of the overall side capacitance. This is not true however since the top plate of the MSB capacitor is tied the virtual ground node which is floating and connected to the other capacitors. The equivalent capacitance can be approximated as the following:

$$C_{Equ} = \frac{C_T}{2}\left\|\left(\frac{C_T}{2}+C_{Par}\right)+C_{PSW} \cong \frac{3}{10}C_T\right. \tag{1.24}$$

Where C_{Par} is the parasitic capacitance also tied to the virtual ground node and C_{PSW} is the parasitic capacitance of the inverter switch that shares the same node as the bottom plate of the capacitor. By substituting these time constant values into [1.22] we get the following:

$$\frac{(N+1)\ln 2}{T_{Conv}/80} = \frac{4K'W}{3V_{DD}L}\left[V_{DD}-V_T-V_{DSAT}/2\right]V_{DSAT}\left(\frac{10}{3C_T}\right) \tag{1.25}$$

Here, the total time for charging is estimated to be the total conversion time divided by 80 (divided by 20 to account for each cycle and another 4 to account for the comparator and logic time). Solving for the transistor sizes, we get the following:

$$\frac{W}{L} = \frac{27(N+1)\ln 2 V_{DD}C_T}{4T_{Conv}K'V_{DSAT}\left(V_{DD}-V_T-V_{DSAT}/2\right)} \tag{1.26}$$

Thus the sizing can be analytically derived from the ADC specification and the process parameters. With the size information, we can now estimate the Power of the DAC drivers as the following:

$$P_{Driver} = C_{Gate}V_{DD}{}^2 f_S = C_{OX}WLV_{DD}{}^2 f_S\alpha \tag{1.27}$$

Where fS is the ADC sampling frequency and COX is the process oxide capacitance. Alpha is also shown and is the activity factor since there are multiple MSB-equivalent charging events per SAR cycle. Substituting in the previously found size data, we have:

$$P_D = \frac{27(N+1)\ln 2 V_{DD}{}^3 f_S C_{OX} L^2 C_T \alpha}{4 T_{Conv} K' V_{DSAT}\left(V_{DD} - V_T - V_{DSAT}/2\right)} \tag{1.28}$$

The critical step in finding driver energy is determining the activity factor which for the MCS SAR is the following:

$$\begin{aligned}\alpha &= (\#\text{Devices / Phase})(\text{Differential Factor})(\text{Non}-\text{MSBFactor}) \\ &\quad (\text{Buffering Factor})(\text{Scaling Non}-\text{Linierity}) \\ &\cong 3*2*2*1.5*1.5 = 27\end{aligned} \tag{1.29}$$

Here, the number of devices per phase is determined to be three (one transmission gate for the reference switching and one of the two sides, either VDD or GND), the differential factor is present to account for both switching sides, the non-MSB factor accounts for the switching power of later scaled stages, the buffering factor accounts for the buffering of the large MSB switches, and the non-linearly factor accounts for the fact that the switches really don't scale by a factor of two but level out at some phase as does the buffering power. The final step in the driver analysis is to determine the respective FOM of this block. By substituting the driver power found in (1.28) into the FOM equation we get the following:

$$FOM = \frac{P}{f_S 2^N} = \frac{4.67(N+1)V_{DD}{}^3 C_{OX} L^2 \alpha}{T_{Conv} K' C_T V_{DSAT}\left(V_{DD} - V_T - V_{DSAT}/2\right)2^N} \tag{1.30}$$

Here, substituting the capacitance and of the array in for CT, we get the following final FOM equation for the drivers:

$$FOM = \frac{28(N+1)V_{DD} C_{OX} L^2 (kT) 2^N \alpha}{T_{Conv} K' V_{DSAT}\left(V_{DD} - V_T - V_{DSAT}/2\right)} \tag{1.31}$$

As an example, for a typical 0.13um process and a 12b, 50MS/s MCS SAR structure, the following FOM will be present with the example values given in table 3:

$$FOM = \frac{(13)(28)(1.2)(10fF)(.13^2)(18)(4.1e^{-21})(4096)}{(20n)(100u)(.2)(1.2-.4-.1)} \cong 120 \text{ aJ / CS} \tag{1.32}$$

Here it can be seen that the minimum energy drivers are comparable in terms of efficiency to the DAC itself. Even though circuit designers typically size the DAC to be thermal noise limited,

the drivers are often greatly over-design the drivers to account for mismatch and corner variation, thus the drivers can easily exceed the power of the DAC itself and should be carefully created. Note that the future TSAR and FITSAR will broth address the energy of driver power and will propose new improvements to significantly reduce the driver FOM limit shown in (1.31).

2.3.4 MCS SAR Block Level Structure – Quantizer

The quantizer unit is essential to all ADCs as it is the block that performs that analog and digital interfacing. In the MCS SAR, there is only one comparator and the design of this comparator is often less straightforward than the other blocks.

The MCS comparator must consist of a latch that samples the analog input and though positive feedback, then regenerates on the outputs to saturate them to a high and low voltage, representing a 1 and 0. The structure of this comparator varies significantly across different accuracy and speed specifications. Typically in low-accuracy SARs (less than 8b), a strongarm latch type structure is used. For moderate to high accuracies, often the P-latch structure shown in fig. 11 is utilized due to the greater noise immunity without the internal secondary positive feedback. Analyzing the noise requirements for these latches is important, but difficult [26]-[27] and is often determined though simulation. Some rules of thumb apply, and in creating an effective comparator, the input devices sizes are related to the input referred noise since increasing them reduces the noise with which the input current discharges the comparators output virtual nodes. The latch and tails current source then often play into the speed of the comparator (and sometimes the accuracy too). When the comparator noise optimization becomes too difficult at high accuracies or speed, often a preamplifier is placed before the latch structures to make a larger signal for the latch to regenerate.

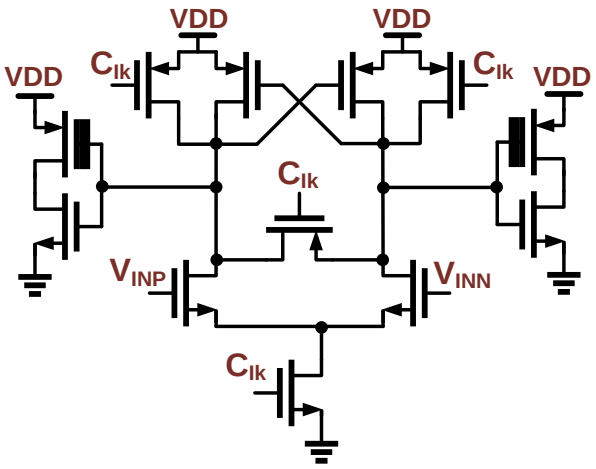

Figure 2.12: P-Latch type comparator with high-VT output buffers

A typical 12b MCS SAR comparator sized to operate in 500ps has an energy of about 42uJ, which translates to a FOM of about 2fJ/C-S for a 50MHz, 12b MCS SAR. This of course is not the absolute minimum, but just what has been found from simulation and measurement with current methods. Due to the enigma that the comparator presents, further research will be done into the structure in later chapters.

2.3.5 MCS SAR Block Level Structure – SAR Logic

The purpose of the logic unit in the SAR structure is to hold the data coming from the comparator in each phase and re-time it to the overall conversion clock as well as provide the phase internal clock for each SAR cycle from a state machine. Also included in the logic is start-up and reset circuitry and sometimes an internal clock generator. In fact, the SAR ADC gets its name because in the old days, all the SAR ADC components would be sold separately and combined on a board [10]. While comparator, DACs, SHAs, and output buffers were standard parts, the logic for internal operation was not, and thus to make the ADC, one had to purchase a special successive approximation register array or SAR and that historical name is still used today.

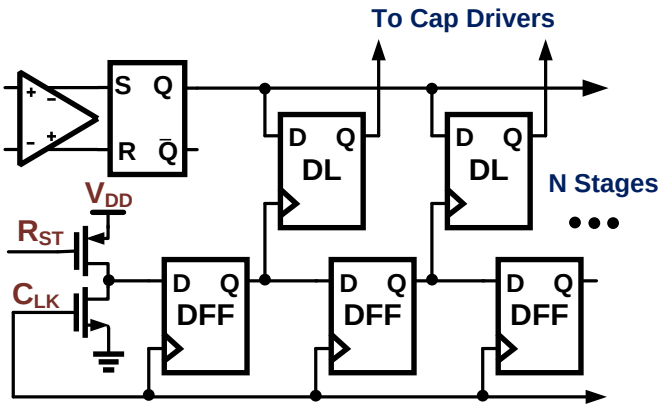

Figure 2.13: Typical SAR logic structure with one-hot ring counter state machine

The basic SAR logic often is comprised of a set of flip-flops for the state machine and latches to act as data registers as shown in fig. 12. In most designs, the logic only drives the buffers and the output load, and thus, the logic can be made to be extremely low power. This is evident in the fact that the logic takes a smaller and smaller portion of the overall ADC power as process nodes shrink since the comparator and DAC must be a fixed sized based on thermal noise requirements, but the logic only must be 1b accurate. Because the SAR is often operated in quick bursts even for small conversion frequencies, the logic can be made to be dynamic. Flip flops are typically TSPC varieties [28] as are the latches. Due to the lack of accuracy and speed requirements, the logic can theoretically take close to no power and thus ideally does not factor into the worst case SAR ADC figure of merit calculation.

2.4 SAR ADC Trends and Innovations

SAR ADCs have become popular in the past decade due to their ability to achieve high energy efficiency by leveraging device sizes and reduced supplies in sub-micron process technologies. However, the efficiency we see today wouldn't be possible without a number of innovations in the SAR architecture that have driven some aspect of SAR efficiency to a more optimal state. In the next sections we will examine the recent trends in SAR ADC design, and then look at improvements to the speed, accuracy, and energy consumption of architectures, especially the innovations that are relevant to the SAR proposals in the coming chapters.

1.3.1 SAR ADC Trends

As mentioned before, ADCs are typically classified by their figure of merit (FOM) which is a measure of efficiency, and each ADC architecture has advantages and disadvantages for achieving a low FOM. Shown in fig. 13 is a plot of the low power ADCs published in the past 15 years in major conferences (with some data taken from [4]). Here, one can see that the limit on efficiency tends to lay around 5 fJ/CS and the very high and very low accuracies tend to perform better. Generally, this effect is due to the large number of parasitic effects that must be accounted for in a high accuracy ADC in order to maintain accuracy and the number of parasitic effects that reduce speed and increase power in low accuracy converters.

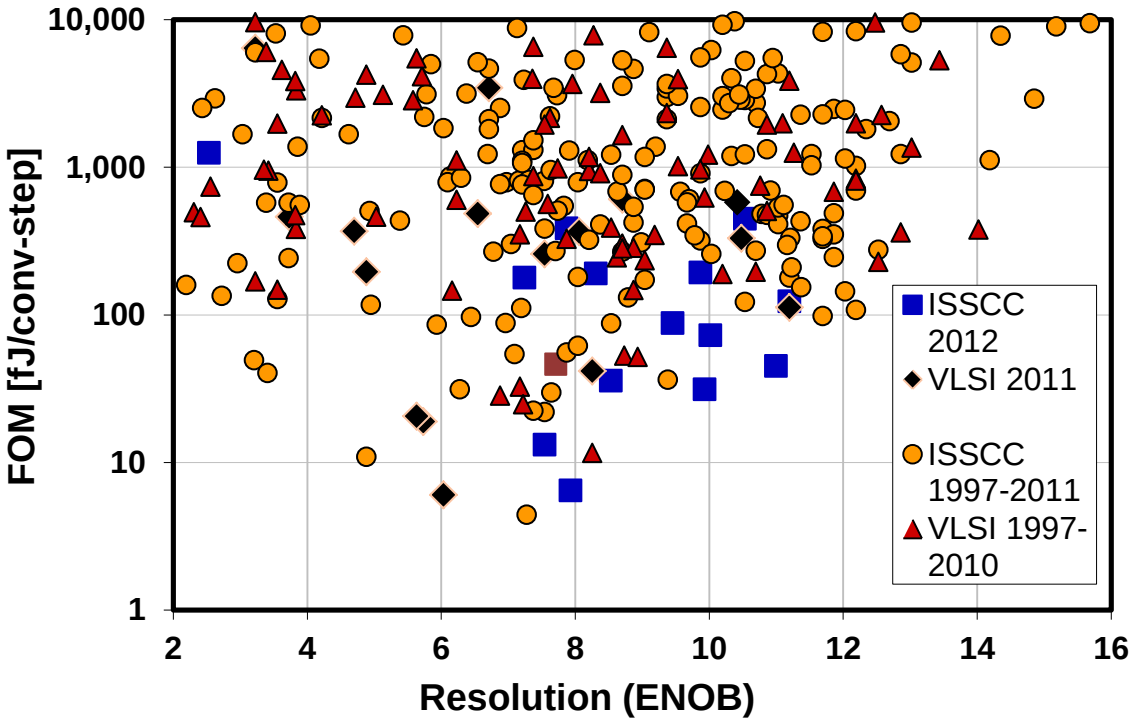

Figure 2.14: FOM vs. ENOB for many recent conference presented ADCs

In fig. 14, the FOM plot has been reduced to only show SAR ADCs (and some recent SARs were not included due to manpower constraints). Here it can be seen that all of the most efficient structures in the mid-resolution range have been SAR ADCs (even the recent low FOM ones that aren't in figure 14 are SARs). One note is that the SAR tends to have the best efficiency around the 8-10b ENOB range because above that resolution, the DAC and comparator power increases by a factor of 4 with each bit increase due to thermal noise limitations and below that

resolution, the comparator and logic energy hit a wall due to minimum device sizes being larger then thermal noise limits.

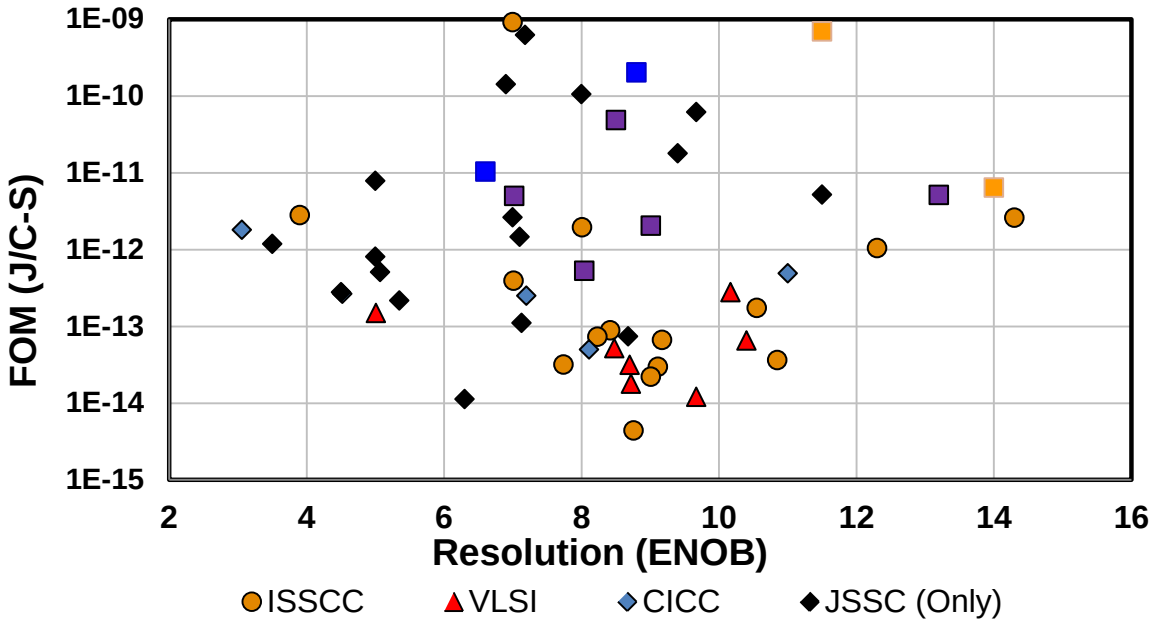

Figure 2.15: SAR ADC performance from 1980-2010

Since the SAR has been proven as a low power leader, there has been an ever increasing interest in the SAR for low power ADC research and this can be illustrated by the number of papers published per year as shown in fig. 15. Many of the SAR ADCs that have contributed to this minimized FOM will be highlighted in the next section and the improvement and further improvement in efficiency and performance will be the theme of this thesis.

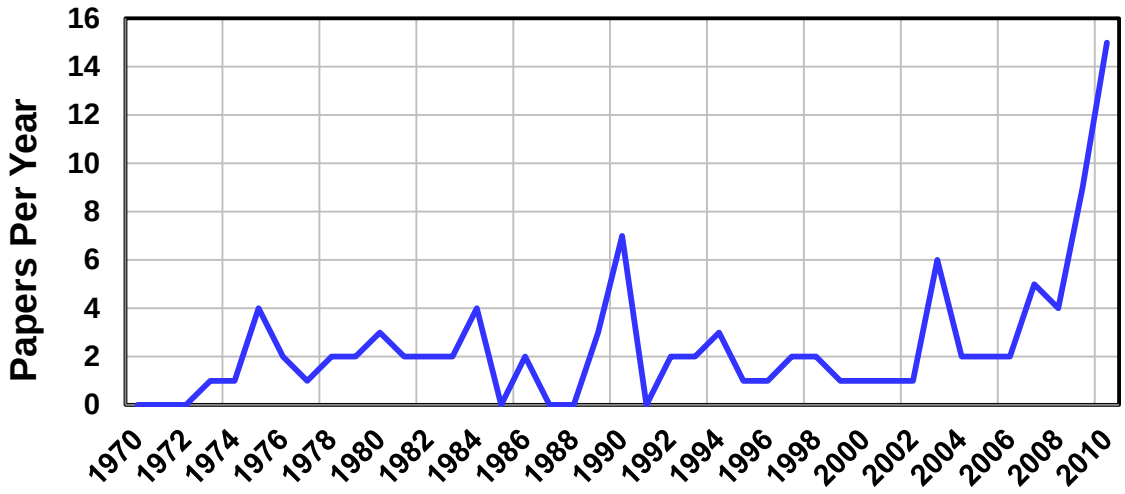

Figure 2.16: Cyclic ADC papers per year in major conferences (1970-2010)

1.3.2 Recent and Relevant SAR Innovations: The Asynchronous SAR

In a typical SAR ADC there are two types of clocks. One is the master clock that comes to every ADC and defines the rate at which the output is to become valid and the input is to be sampled. In the SAR structure, there is also an internal clock that is a sub-divided version of the master clock and determines when each phase of the SAR operates. Along with the clock, a SAR state machine holds the current phase information. This type of clocking structure works well, but is inefficient for the main reason that the delay of each SAR internal phase is dependent on the stage input magnitude. However, since the clock generator is often an isolated voltage controlled oscillator (VCO), it cannot sense how long a SAR phase will take before delivering the clock edge, thus it must be long enough to account for all possible delays up until the worst case, which is when the input is as small as the LSB/2.

The asynchronous SAR is an architecture designed to improve this timing problem by, rather than cocking the SAR with a fixed VCO clock, letting the comparator's valid output trigger the clock for the next stage, thus self-clocking [16]. In theory, this should significantly improve the overall conversion time (by about a factor of 2) since most of the conversion cycles have magnitudes much larger then LSB/2 as shown in fig. 16.

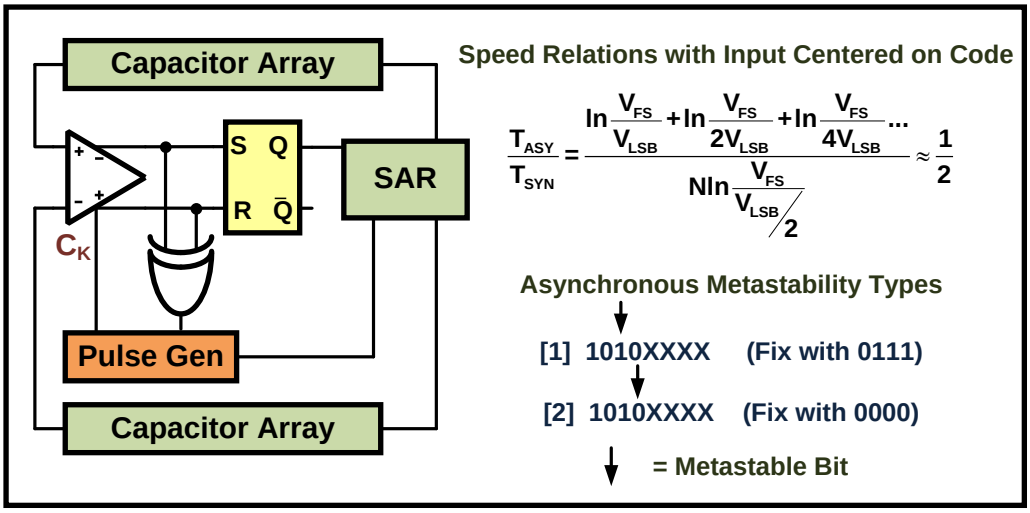

Figure 2.17: The Asynchronous SAR and metastability

However, there is one sneaky problem. This is that on some instances there is an input to a given stage of the SAR that is much smaller in magnitude then LSB/2. In a typical synchronous SAR, this is no problem since the clock of the SAR will simple cut off the comparator if it hasn't made a decision in the allocated time and arbitrarily assign it a code (typically 0). The accuracy of the SAR in this case is not affected since the input must have been small to trigger such a long comparison. In the asynchronous SAR though, because of the self-clocking, a small input can essentially lock up the SAR for an undefined amount of time, and if that time is long enough, it will result in not all of the ADC bits being determined. To fix this problem, some have come up with the solution of simply assigning the rest of the bits to 0 if they have not been determined. While simple, this doesn't fix every problem especially in that case when an internal state is a long enough time to not finish all the codes, but not long enough that the following couple of codes were not resolved as shown in fig. 16. The end result is that while the asynchronous SAR is on average faster, it results in analog metastability errors, which means there is some finite bite error rate (BER) which must be accounted for in the digital output stream.

It should also be noted that some have tried to fix the analog metastability with internal logic in the SAR critical path [17], but this typically is at the expense of additional delay because of parasitics and power due to fast path digital activity. Thus while enticing, there is no free lunch for self-clocking type speed improvements. In chapter 3, the Ternary SAR will be shown which can achieve similar speed improvements without the danger of analog metastabiliy.

1.3.3 Recent and Relevant SAR Innovations: SAR Energy Reduction

While the MCS SAR has a more energy efficient switching pattern then other structures, it is still inefficient in the fact that the three levels are not fully utilized for switching. The later chapters will try and find full solutions for this problem, but in the meantime, one solution has been proposed called a windowed SAR [29]. Here, as shown in fig. 17, the virtual ground nodes in the early stages are fed to three voltage domain comparators. The middle is the normal high accuracy comparator while the top and bottom are slightly lower accuracy and used to determine if the input is within half of the full-scale range. If the input magnitude is small, the DAC will not switch for that code, saving DAC energy. This can save up to 40% of the DAC switching energy and activity, but has a number of drawbacks, including that the voltage comparators can only be used for a couple of stages since their offset requirements and noise accuracy must grow with each stage (meaning there's no redundancy or comparator energy minimization). Also, a separate DAC is needed for the auxiliary voltage comparators if they are to be used in multiple cycles, meaning that while the DAC energy is reduced, the quantizer energy is increased. Thus, DAC energy reductions are achieved, but at the cost of quantizer and logic energy.

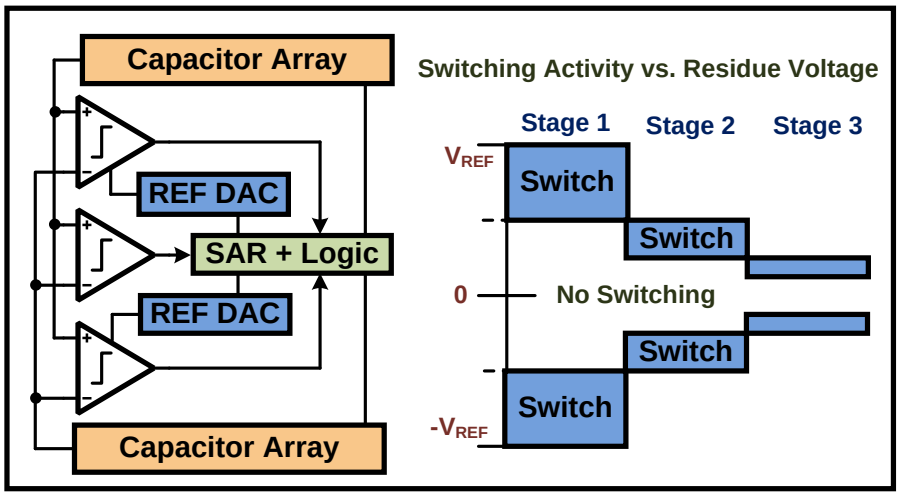

Figure 2.18: The windowed SAR with no switching region

Another popular energy reduction innovation is multi-step charging which is illustrated in fig. 18 [30]. This work relies on the principle that the first cycle is the most power inefficient due to the charging of the large MSB capacitor. Thus, rather than charging that capacitor by connecting it straight to the positive supply, it can be connected to a few large intermediate capacitors with

ever increasing voltages across them and charge share, meaning that the supply only must provide the last little amount of charge. Then, on the discharging cycle, the MSB capacitor is again connected to the intermediate capacitors in a reverse order such that the charge taken is replaced in each cycle. This is a form of charge recycling and can reduce the MSB capacitor charging power by a factor equal to the number of steps taken. While this is an effective energy reduction method (used to achieve the ADC with the best FOM), it does significantly slow down the SAR loop due to the extra cycles (the prototype had a bandwidth in the 100s of kHz) and increases the area by requiring many extra, large capacitors. Also, there is a limit to the energy efficiency as the addition of each capacitor increases the complexity of the SAR logic and drivers as well as the parasitic capacitance on the DAC bottom plates.

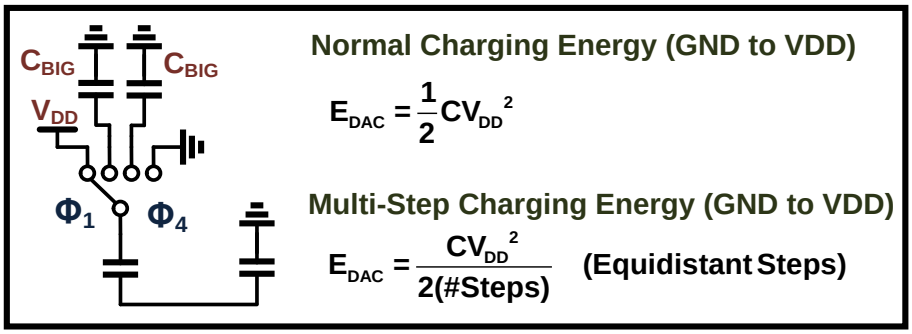

Figure 2.19: The multi-step DAC charging method

1.3.3 Recent and Relevant SAR Innovations: SAR Redundancy

Redundancy is one of the most important features of most high-accuracy nyquist ADCs. The term was first coined for pipelined ADCs, where redundancy essentially enabled the structure to work in the presence of comparator offsets [31]. In the pipelined ADC, each stage has separate comparators, and since comparators have notoriously large offsets, this meant that the pipeline structure was only as accurate as the comparator offsets themselves. While comparator design improved, the real structural benefit came with the idea of increasing the number of comparators per stage, in order to limit the full-scale range of the residue of a sub-ADC. This meant that as long as the comparators didn't have too large of offsets (typically ¼ the stage full-scale range), their offsets wouldn't affect the overall resolution since an error would be eaten up by the next stage's extra comparators. Thus redundancy was formed to prevent sub-ADC errors in multi-stage ADCs by increasing the resolution of a given sub-ADC stage.

The SAR ADC, while multi-stage like the pipelined ADC, has the distinct advantage of not having to have different comparators in each cycle, but only one accurate comparator. Here the offset problem is solved since there should be no offset relative to adjacent stages, but there could be stage dependent errors due to settling time limitations and large transients from the input. Also, redundancy allows for the injection of calibration signals in any multi-stage ADC structure. Thus, adding redundancy to the SAR has been sought after.

Since the pipelined method of achieving redundancy doesn't apply to this structure due to the lack of separate comparators, a number of innovative methods have been devised with the simplest being adding extra stages to the SAR as shown in fig. 19 [32]. This will fix over-range errors due to the lack of redundancy in previous stages. As an example, if settling noise causes a stage's residue to exceed the full-scale limit, adding an extra stage will essentially re-run that stage's comparison and pull-in any errors that are not bigger than the redundant stage's full-scale range. The main drawback of this method is that to achieve redundancy, extra cycles must be added, slowing down the SAR and adding comparator and logic energy. Also, the magnitude of the redundancy is now directly related to the number of cycles added.

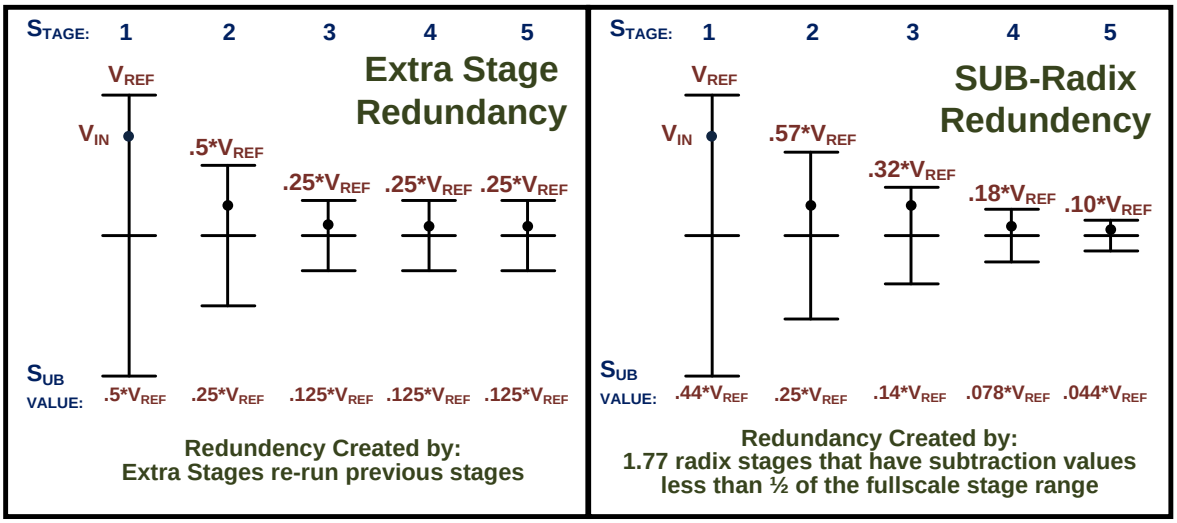

Figure 2.20: Extra stage and sub-radix redundancy illustrated with 5 stage SAR examples

Another solution that adds front-end redundancy is the sub-radix method in fig. 19 [33]. This method increases each stages full-scale range over what it would normally be in a binary search by changing the values of the DAC. This means that even though the comparator still outputs only a 1 and 0, since the magnitude of the cycle's range doesn't decrease by a factor of 2 in each

cycle, the binary quantization is larger than needed, providing redundancy. While this redundancy is achieved without explicitly copying a stage, it does add cycles due to the shrinking of the digital gain in each stage. While it may not add as much time as the extra stage redundancy, it has other drawbacks including requiring a non-binary DAC (making matching a pain, or requiring calibration) and needing a fast adder and multiplier to produce a valid binary output. Both these methods add energy and delay to the SAR operation.

The SAR ADC has been shown to be the most energy efficient ADC structure for medium speed and accuracy specifications, and numerous innovations have been proposed for the structure. The next few chapters will look at ways to not only achieve many of these innovative benefits without some of the associated problems, but also look for solutions that will push the SAR beyond the current efficiency bounds in place today.

3. THE TERNARY SAR

The main structure for building a SAR ADC has remained relatively constant for generations of previous architectures. A 2-level quanitzer (comparator), a 2 level DAC, drivers and logic were all that was needed. The design of the MCS SAR changed everything when for the first time a 3 level DAC was heavily utilized, however interfacing that DAC with the same 2-level quantizer didn't fully optimize the structural energy efficiency. This section will explore time domain innovations to create that third quantizer level without degrading the inherent SAR benefits.

3.1 Modern SAR Limitations

The ternary SAR is meant to be a direct improvement to the state of the art merged capacitor switching (MCS) SAR, however, it also solves many of the problems that other structures have tried to fix. In this section the limitations of the MCS SAR will be examined along with the limitations of numerous other ingenious SAR architectures designed to address more specific design requirements.

3.1.1 The MCS SAR

The MCS SAR is an efficient structure that has been shown in chapter 2 to maximally reduce switching energy when compared to other techniques; nevertheless, there are a number of inefficiencies with the structure. The first is that while there are three levels in the DAC {GND, VCM, and VDD} only two of them are being utilized as switchable states in the final SAR output {GND, VDD} while VCM is only used for the input sampling. Higher efficiency switching could be possible if all three of these stages could be better utilized.

The other major MCS limitation is the lack of redundancy. This means that if an error larger then LSB/2 occurs due to noise or settling time problems in an early stage of the SAR, there is no way to correct the final digital code. This also means that the accuracy of every block in every stage of the SAR must be at the accuracy of the full ADC, whereas with redundancy, the accuracy only has to be great enough to not cause an error larger than the redundancy bounds.

3.1.2 SAR Innovations

Over the past decade a number of innovative architectures have been proposed to solve specific problems associated with SAR ADCs in general, but with each of these solutions come

additional limitations in other areas. One of the most popular of these circuit architectures is the asynchronous SAR [1]. This structure can increase the overall speed of the SAR conversion by letting each stage self-clock based on the valid output of the comparator. In the early stages, there is a high probability that the comparator will resolve much fasterer than the worst case and coupled with the fact that the worst case SAR comparison will only happen twice per conversion, the average delay based on comparison should reduce by a factor of 2. The problem with this idea is that by self-clocking there is a possibility of analog metastability happening when the input is so small in a given cycle that the sum of all the cycle times is greater than the sampling rate. This either leads to a greater bit error rate (BER) of the ADC or increased critical path logic [2] to provide a time-out feature.

The variable window function SAR [3] is another innovation that reduces the switching energy of a SAR by not switching when the stage input is within $\pm V_{FS}/2$ where V_{FS} is the stage full-scale range. This creates an effective no-switching range and can reduce the total switching energy by at the most ½ (however this maximum power reduction is not physically achievable, a more reasonable value is 1/4). The problem with this scheme is in the implementation which requires extra voltage comparators whose references change in each stage adding significant power consumption to the total SAR operation, especially in thermal noise limited SARs where the comparison takes up a larger percentage of the total power consumption. Additionally, the accuracy of these auxiliary comparator increases by a factor of 2 with each stage meaning that the scheme can only be used in the first few stage of the SAR before the offset of the comparators exceeds the “no switching region” range.

The addition of redundancy through either sub-radix arrays [4]-[5] or additional stages [6]-[7] in the SAR has also been shown to be useful for the prevention of early stage and sampling transient error, settling time reduction, and the injection of test signals for background radix calibration [8]-[9]. However, in both of the redundancy adding configurations, extra stages and thus extra delay and power are required. The sub-radix array produces even more challenges as the output bits are not binary and require a special digital processing unit to recode them to binary and the actual radix values must often be individually calculated through either foreground or background calibration.

The rest of this chapter will introduce a new SAR structure that has the ability to improve speed without the analog metastability of the asynchronous SAR, reduce switching power and

provide a no switching region without the extra voltage comparators of the windowed SAR, and provide redundancy without any extra stage or sub-radix capacitors. Finally, the comparator and DAC limitations of the MCS SAR will be mitigated while improving the overall SAR accuracy, speed and energy efficiency.

3.2 The Ternary SAR Structure

A traditional binary capacitive SAR works by first sampling the analog input signal and then performing many cycles of 1-bit comparisons as illustrated in Fig. 1 and described in chapter 2. After each 1-bit decision, a DAC subtracts or adds a binary weighted voltage to the quantizer input, minimizing the voltage difference and allowing the quantizer outputs to digitally represent the input signal through a binary search algorithm. Chapter 2 also mentioned the energy efficient MCS SAR architecture. Here the input is sampled onto the top plate virtual ground nodes of the capacitive DAC with respect to the common mode voltage, V_{CM}, in the sampling phase and these nodes float during the conversion. The conversion starts by strobing the 1-bit voltage comparator which sends either a "1" or "0" quantized representation of the virtual ground inputs to the SAR logic. This logic will then trigger the bottom plate of the MSB capacitor in the DAC to switch to either V_{DD} or GND in order to minimize the differential voltage on the virtual ground nodes. One can see from this switching operation that in every phase, the bottom plate of each capacitor is switched from V_{CM} to either V_{DD} or GND starting with the MSB capacitor and progressing to the LSB with one capacitor per phase. Once the final digital word has been determined, the bottom plates of the whole capacitor DAC are reset to V_{CM}.

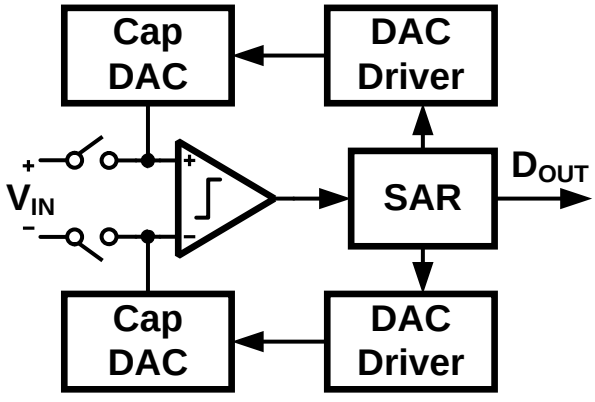

Figure 3.21: Top-Plate sampled SAR block diagram

In the previous section the MCS limitations of the three level DAC and redundancy were described as the presence of three switchable levels signifies that multiple switching trajectories could be taken to reach a given virtual ground minimization, however with only a two-level quantizer, these trajectories are limited. In order to optimize the DAC level utilization and allow for ancillary accuracy and speed benefits, an additional source of information must be found to dictate an optimized switching operation.

3.2.1 SAR Comparator Delay

One information source that can provide the information needed for three-level switching can be found by looking at the transient response of the dynamic voltage comparator. Assuming the comparator has a typical single pole response, the transfer function can be modeled as the following [10]:

$$V_{OUT} = \left(V_{IN}\right)\exp\left[\left(A-1\right)t/\tau\right] \tag{3.33}$$

Where A is the linier regenerative gain of the comparator and tao is the latch time constant. From this we can derive the minimum delay of a given SAR stage comparison as the following:

$$T_{S,Min} = \ln\left(2^{N-1}\right)\frac{\tau}{A-1} \tag{3.34}$$

Where S is the stage under analysis. While the input/output function was naturally exponential, the delay difference between consecutive stages varies linearly due to the factor of two scaling in each stage as shown:

$$T_{S,Min[M]} - T_{S,Min[M-1]} = \ln\left(2\right)\frac{\tau}{A-1} = \ln\left(2\right)C_{NT} \tag{3.35}$$

Where C_{NT} is simply a constant term. This stage by stage delay variation is plotted in fig. 2 from a dynamic comparator transistor level p-latch comparator. Since the delay response is independent of the polarity of the virtual round nodes, measuring the time delay of the comparator gives information about the absolute value of the input. Also, if the delay information were to be used to determine the magnitude of the input with respect to a percentage of a stage's full scale range, the accuracy of that time measurement would not increase from one SAR stage to the next due to the linear comparator delay verses stage.

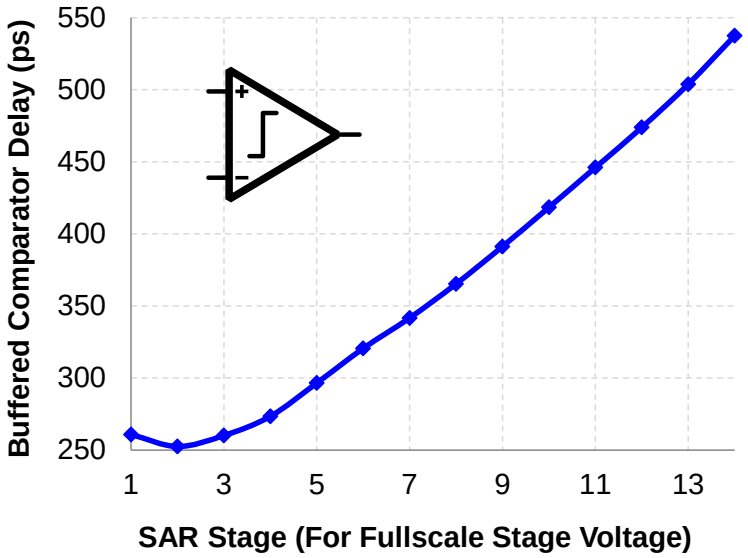

Figure 3.22: Comparator buffered output delay for an input equal to the given stage full-scale range

3.2.2 Ternary Structure

The proposed Ternary SAR (TSAR) structure that utilizes comparator delay information is shown in Fig. 3 [11]-[12]. Here, a time comparator and delay unit are introduced into the critical path of the SAR loop in a differential fashion. The purpose of the time quantizer structure is to determine if the input magnitude is smaller or larger than a given reference, with respect to the full-scale range of the given SAR stage, by examining the delay of the main voltage comparator. This time quantization is coarse and will feed to the SAR logic unit with the time quantization thresholds set by a delayed voltage comparator clock. Other standalone time comparison structures have been proposed [13]-[14], but this differs in that the time comparison does not set the SAR sub-ADC quantized output alone, but rather shifts the fine voltage comparator outputs to generate three levels per stage. This structure maintains the accuracy and global offset provided by the single traditional voltage comparator and enhances the MCS SAR operation, rather than attempting to just replace the voltage comparator with a time based structure. Finally a time comparator structure with voltage comparator was mentioned in [15], for the purpose of comparator metastability and last stage flash. However, that circuit does not take advantage of the power savings, accuracy improvements, and speed increases described in the rest of this chapter.

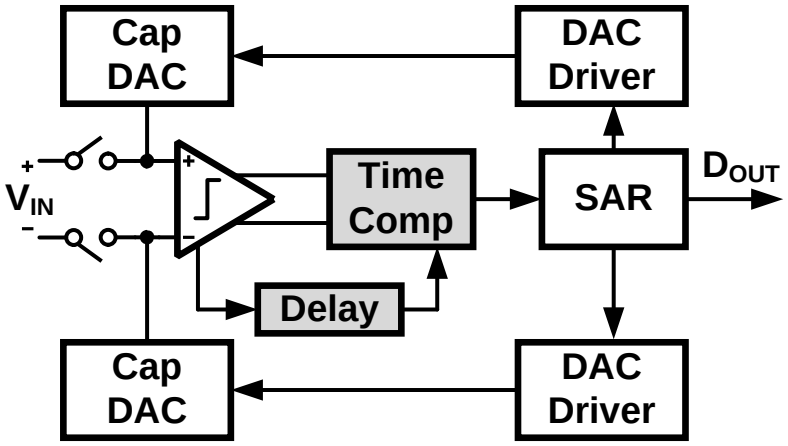

Figure 3.23: The Proposed Ternary SAR (TSAR) structure

The operation of the TSAR core for a given sample begins with the master clock sampling the input onto the DAC virtual ground nodes and starting an internal core clock. This core clock generates a clock edge for the voltage comparator and delay unit. A delayed internal clock edge is then sent to the time quantizer. If the buffered output of the voltage comparator resolves to either a high or low code before the delayed clock latches the data on the time quantizers, then the output digital code for the stage is the standard "10" or "00". However, if the input does not flip the buffer inverters to either a high or low state before the delayed clock arrives to the time quantizer, the stage digital code sent to the SAR logic will be the mid code or "01" as illustrated in Fig. 4. The benefits of this ternary coding will be explored in the next sections.

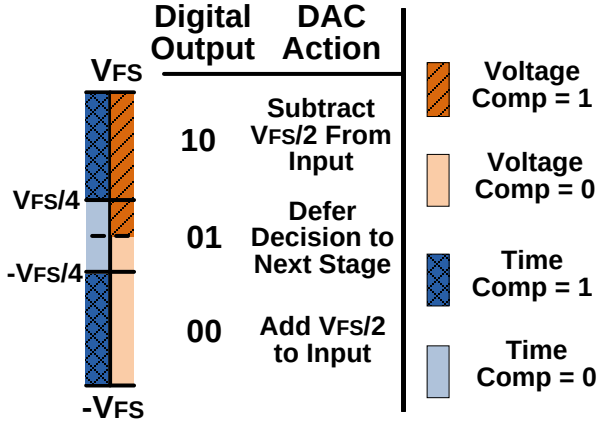

Figure 3.24: TSAR stage output diagram for a given virtual ground input

3.3 TSAR Inherent Benefits

The TSAR structure has a number of inherent benefits that come from the generation of third coarse quantizer level in the middle of the full-scale input range. These will be examined in this section and then structural enhancements that come from changing the way the ternary quantization is formed will be shown in the next section.

3.3.1 TSAR Redundancy

The first major inherent benefit of the TSAR is the presence of a redundancy that looks like the 1.5b/stage type seen in pipelined converters [16]-[17]. This redundancy is useful for tolerating small settling errors or preventing over-range errors from sampling transients. Also, as in a pipelined converter, sub-ADC reference levels can vary from $V_{FS}/2$ to 0 without causing over-range errors in later stages. This voltage domain requirement becomes more relaxed in the time domain for the TSAR since there is a set time value that corresponds to the upper redundancy limiting $\pm V_{FS}/2$ level (where V_{FS} refers to the full-scale voltage of a given TSAR stage), but not the 0 level, which would require an infinite time delay. Explained another way, as the time given for comparator regeneration is increased, the size of the mid-code redundancy region will exponentially approach zero in the limit, but the respective threshold levels will never cross. This implies that in chips with large dynamic supply and temperature variation, redundancy over-range problems can be mitigated by simply designing for a smaller initial redundancy range. Additionally, the fine comparator still decides the final polarity of a signal, so that the offset of that fine voltage comparator is still the global offset of the SAR (because in the end, the accuracy is determined by the last stage polarity decision which is related only to the voltage comparator, not time). Finally since the voltage comparator delay varies linearly with the TSAR stage scaling, as shown in Fig. 2, there is no increased time comparator accuracy requirements in later stages as would be the case if the redundancy were implemented in the voltage domain.

This time based redundancy has a great advantage over the other traditional SAR redundancy schemes of sub-radix [4]-[5]or extra stage [6]-[7] in that no additional cycles are needed and the capacitor DAC array can still be binary weighted for simplified matching and digital logic. Furthermore, the digital error correction addition of 1.5 bit/stage pipelined structures [16] can still be employed here without any analog shifting or complex digital conditioning.

3.3.2 Speed Improvements

The TSAR time comparator also has built in speed benefits. Like the asynchronous SAR, the TSAR does not wait for the worst case input dependent delay of the voltage comparator to resolve the rest of the bits in the SAR conversion. Rather, after the delayed clock strobes the time comparators, the TSAR loop clocks the critical path logic and DAC whether or not the voltage comparator has resolved. This timing structure is still synchronous, however, since every cycle is deterministically ended with the delayed internal clock edge, even in the case of voltage comparator analog metastability (note the analog comparator metastability is eliminated, but no ADC can remove digital metastability from the latching of the comparator output bits; it can only be mitigated with timing and digital gain). When compared to a traditional synchronous SAR, the TSAR structure allows for the largest time savings in early stages. In the traditional synchronous structure, the SAR must wait for the worst case delay from an input of $\pm V_{LSB}/2$ in each stage while the TSAR must only wait for an input larger than the redundancy region, often $\pm V_{FS}/4$ as illustrated in Fig. 5. In all, the worst case SAR conversion delay is significantly reduced similarly to the asynchronous SAR, but without the analog metastability that will deterministically reduce the ADC bit error rate.

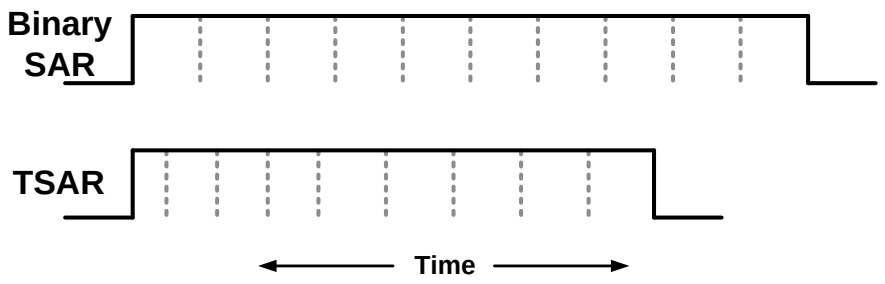

Figure 3.25: Binary SAR and TSAR cycle time spacings

3.3.3 DAC Activity Reduction

The TSAR structure also increases the efficiency of the DAC switching and drivers by eliminating switching operations when the input is differentially small. When the input is within both time comparator thresholds, no switching operation is performed meaning that no capacitor switching power or DAC driver power is used in that phase as illustrated in Fig. 6. This power saving switching method is similar to the windowed SAR of [3], however there, voltage comparators were used to create the windowing function and here that operation is pushed to

the time domain. In the voltage domain the accuracy of the extra voltage comparators has to increase by a factor of two in each stage for effective power savings, thus their useful operation is only in the first few stages. The accuracy of the comparator in the time domain does not increase from one stage to the next though due to the exponential nature of the comparator delay, allowing the windowing to be effectively applied to the whole SAR. While the energy savings of the DAC drivers and capacitor array windowing reduces by a factor of two in each stage, it will be shown that by adjusting this window properly, one can achieve greater later stage power saving though reference grouping.

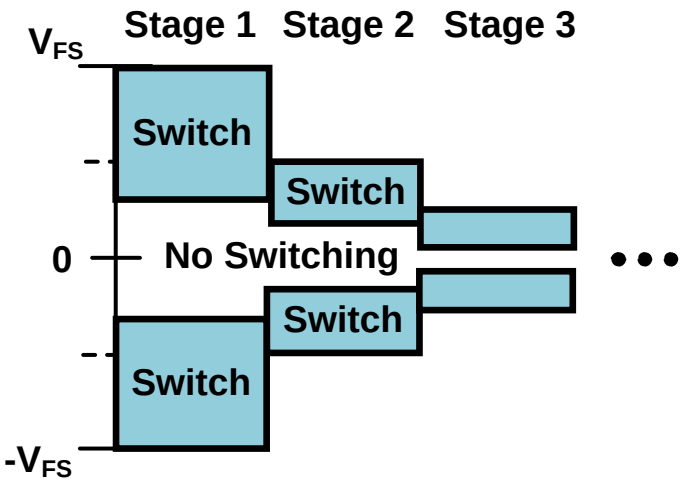

Figure 3.26: SAR DAC windowing showing "switching" and "no switching" regions of operation

3.3.4 Residue Shaping

The TSAR structure also allows for resolution improvements though residue shaping due to the three level redundancy in a multi-stage ADC [18]-[19]. Unlike in a binary or sub-radix SAR, the residue voltage after each stage of the TSAR will have a higher probability of being within the center half of the given stage's full scale range. In other words, if the SAR has a uniform input probability density function (PDF), the width of the majority of the residue in each stage should decrease by a factor of 2 in comparison to the PDF of a binary SAR and the PDF magnitude should increase by a factor of 2 as shown in Fig. 7. Note that residue shaping works just as well with a non-uniformly distributed input PDF, but the uniform is described here for conceptual understanding. Also, the reference levels in Fig. 7 are an example configuration for illustration purposes and are not the only possible setting as will be described later. Mathematically this is due to the stage transfer function of the TSAR which is the following:

$$V_{OUT,STAGE} = \begin{cases} V_{IN} - \frac{V_{FS}}{2} & \text{for} \quad V_{IN} > \frac{V_{FS}}{4} \\ V_{IN} & \text{for} \quad -\frac{V_{FS}}{4} < V_{IN} < \frac{V_{FS}}{4} \\ V_{IN} + \frac{V_{FS}}{2} & \text{for} \quad V_{IN} < -\frac{V_{FS}}{4} \end{cases} \tag{3.36}$$

Where V_{IN} and $\pm V_{FS}$ are the input and fullscale ranges of a given TSAR stage.

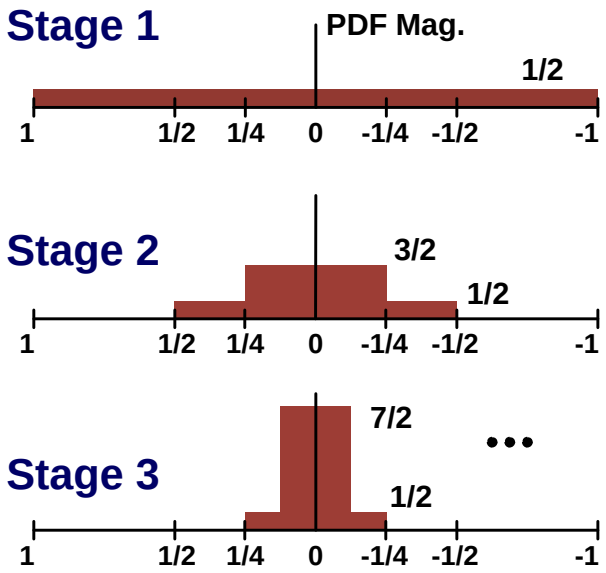

Figure 3.27: TSAR residue shaping illustration for an example uniform input PDF

This transfer function results in an input stage PDF magnitude of:

$$\text{PDF}(\text{Stage}) = \begin{cases} \frac{1}{2} & \text{for} \quad V > \frac{V_{FS}}{2} \\ 2^{(ST-1)} - \frac{1}{2} & \text{for} \quad -\frac{V_{FS}}{2} < V < \frac{V_{FS}}{2} \\ \frac{1}{2} & \text{for} \quad V < -\frac{V_{FS}}{2} \end{cases} \tag{3.37}$$

Here ST is used to denote the current stage. Since the magnitude of the PDF in the next stage's redundant region increases by a factor of 2, for each TSAR stage with redundancy, the probability of getting a mid-code is increased further, saving additional driver and switching energy over a binary SAR. Also, since this residue shaping can occur across the entire TSAR, it is shown in Fig. 8 that the last stage residue can be squeezed into half the range of a normal binary SAR last stage. A mathematical analysis will be fully derived in the next chapter, but the final result shows that the SQNR improvement possible due to full SAR residue shaping is the following:

$$\begin{aligned}\Delta\mathrm{SQNR}_{\mathrm{R-Shaped}} &= \mathrm{SQNR}_{\mathrm{R-Shaped}} - \mathrm{SQNR}_{\mathrm{Traditional}} \\ &= 20\log_{10}\left[2\left(1-2^{-\mathrm{ST}}\right)\right]\end{aligned} \tag{3.38}$$

This results in an effective extra 6dB of signal to quantization noise ratio (SQNR) or an extra bit. In a mismatch limited SAR, this can reduce the total capacitance by a factor of two since the capacitor spread decreases by one bit, resulting in large energy savings. In a thermal noise limited SAR, an extra stage can be eliminated resulting in saved comparator, driver, switching, and logic energy. The next chapter will discuss the phenomena in greater detail and show that benefits are still present even in the presence of large comparator offsets.

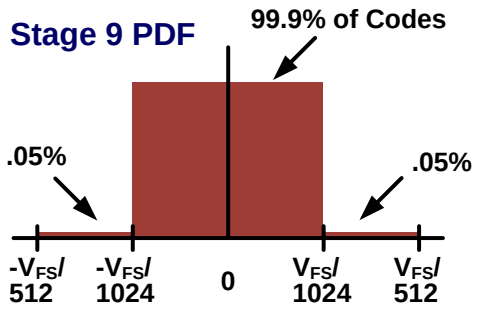

Figure 3.28: TSAR last stage residue plot

3.4 TSAR Structural Enhancements

Until this point, the assumption has been made that each stage has a separate time reference level, setting a unique redundancy threshold, however, this is not optimal for a number of reasons. The first is that we want to minimize the number of references that have to be generated for the tine comparison (even if they are coarse) and the second is that we can actually save TSAR energy by grouping reference levels together. This section will also show that only the last of the references (or last 2 if using the time comparator as a backend flash) need to be accurate and a low complexity calibration scheme will be shown for the reference generation.

3.4.1 Reference Grouping

In a pipelined 1.5b/stage ADC, the redundancy levels are dictated by the ADC wide references (typically at $\pm V_{FS}/4$), meaning that the input referred redundancy thresholds decrease by a factor of two with each stage. In the TSAR however, since there is no interstage gain, the redundancy levels must be uniquely set in each cycle (a global reference would increase by a factor of two in terms of the full-scale range of each stage as the cycles progress). While it is possible to reset them in each phase such that they decrease by a factor of two, they can also be kept the same across multiple cycles as long as the condition that the redundancy level does not exceed the next stage's full scale range ($V_{FS}/2$ of the current stage) is met, which is not possible in pipeline or algorithmic structures. Grouping reference levels turns out to be beneficial for the TSAR operation in that when two stages share a common redundancy range, there is the potential to skip stages as is illustrated in Fig. 9. Here, in the first two cycles, the input is large and positive and is outside the redundant zone. This means the output is a typical "10" code and the DAC must be switched to minimize the virtual ground voltage. In the third cycle however, the input is in the redundant or "01" region, thus the DAC and drivers do not have to operate. In the fourth stage, since the redundancy range exactly matches that of the third stage, we deterministically know the output code will be again "01." This means there is no need to do any comparison operation or switch the DAC and drivers since the code is copied from stage three and no virtual ground movement is required. Thus, the fourth cycle can be skipped, eliminating that stage's comparator, DAC, driver, and logic power. By grouping more stages, there is the potential for additional stages to be skipped, however, the initial redundancy range decreases in the first stages of the grouping. This means that adding another stage to a

large group will result in minimal energy improvement since the full-scale range of the first stage in the group will be large with comparison to the grouped redundancy range.

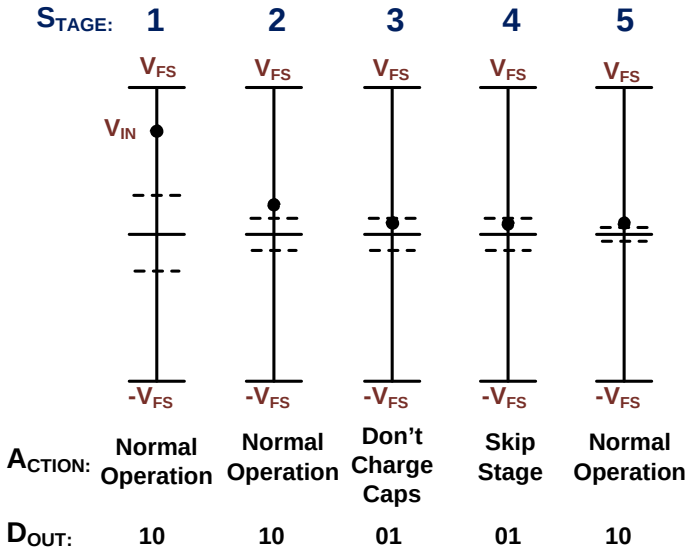

Figure 3.29: Grouped TSAR reference levels with TSAR skipping example

Since the TSAR conversion delay is still determined by the worst case delay, i.e. when no skipping occurs, the stage grouping will only improve power consumption and not ADC bandwidth. In order to maximize energy saving due to grouping, it is important to see that grouping will reduce the DAC windowed switching energy savings in early stages of the group. Thus, often having small or individual reference groups for the MSB stages is important while larger groups are better for later stages where comparator energy dominates. The grouping used in the TSAR prototype is shown in Fig. 10 and was determined by running exhaustive energy simulations with block level power data generated from simulation. Here only three separate references are used with the first two being coarse since its accuracy has no direct impact on the resolution of the TSAR as long as they do not exceed the over-range bounds of the redundancy. The third can also be coarse, but its accuracy will determine the quantization error bound for the last bit, thus to get a full final bit, the reference level will need to be slightly more accurate than the first two as is described in the next chapter. To get 2 extra bits, the time comparator can also be used as a back end flash where the full-scale range of the flash is ¼ that of the last TSAR stage. This is due to the residue shaping effect and is also described in the next chapter.

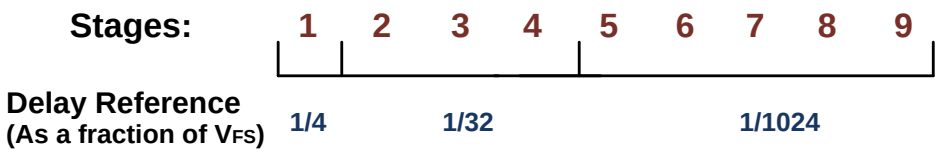

Figure 3.30: TSAR prototype reference grouping (10b chip)

3.4.2 Time Reference Calibration

Since the last reference level controls the final bit resolution, its accuracy can only degrade the final SQNR by at most 6dB assuming it does not cause an over-range error. Fig. 11 shows the SNDR degradation of the TSAR structure in the presence of time reference offsets distributed in the voltage domain from 0 to $V_{FS}/2$. Also shown is when the final time reference distribution is ideal (at $V_{FS}/4$). Even if the threshold is bounded to within $3V_{FS}/8$ to $3V_{FS}/16$ (1/2 typical allowed redundancy range) in the voltage domain, the 10b resolution can be maintained with less than 1dB of degradation as will be shown in chapter on residue shaping.

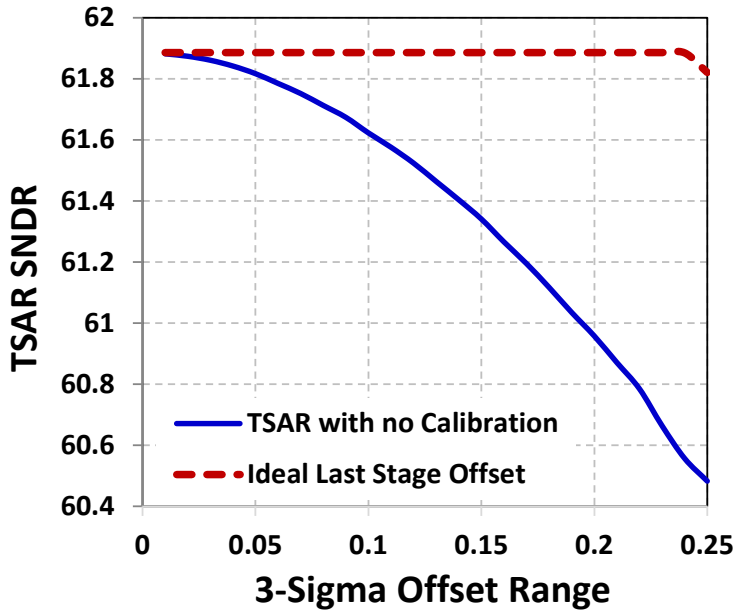

Figure 3.31: TSAR SNDR degradation in the presence of non-deal last stage time references

These are broad reference bounds when translated to the time domain and can be reasonably set by the statistical background calibration loop shown in Fig. 12. Since the ideal final stage reference level sets 50% of the second to last stage digital outputs to be redundant (due to residue shaping), the calibration unit accumulates the number of redundant (“01” code)

events for this stage with a weight of 1 and non-redundant ("00" and "10" code) events with a weight of -1. When an accumulation rollover event occurs due to an unbalanced code output, a dynamic charge pump can increment or decrement the reference value held on a capacitor feeding a current starved timing voltage controlled oscillator (VCO) to adjust the time reference. This allows the final SQNR degradation due to time reference mismatch to be controlled well under 1dB. This calibration operates in the background and counts at 1/64 the master clock rate with rollovers occurring no faster than 1/4096 the clock rate, making power consumption negligible. This calibration could also be extended to the TSAR back-end flash since the accuracy of the time reference there determines that accuracy of the final 2 output bits.

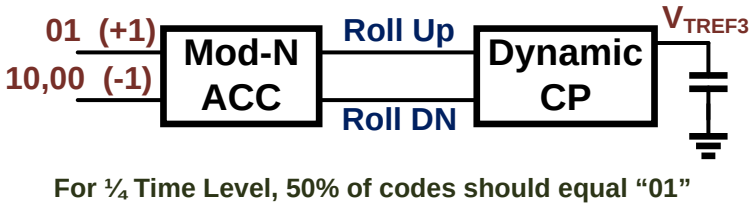

Figure 3.32: Background calibration loop for statistically setting the last time references

3.4.3 TSAR Overall Power Savings

The implementation of the TSAR structure allows for power savings from a number of sources. The resulting power reduction can be seen by examining the total DAC switching, driver, and comparator power reduction. Switching and driver power reductions are shown per code in Figs. 13(a) and 13(b) vs. the traditional MCS SAR. Here, the combined power savings come from the TSAR window function DAC activity reduction and stage skipping. In the mismatch limited case, DAC switching and driver energy is reduced by 63.9% and 61.3% respectively over the MCS structure and 27.2% and 29.6% respectively in the thermal noise limited case. Fig. 14 shows comparator activity reduction due to stage skipping and residue shaping. Due to the TSAR structure, on average, 8.03 operating cycles and 6.53 DAC switching events are required for a 10 bit output word with only three distinct time references. This translates to a comparator activity and power reduction of about 19.5%. Note that this is in stark contrast to other redundancy schemes, which often require up to 1.5x more stages and can have side effects such as non-binary arrays, digital complexity, and extra analog domain shifting [4]-[7].

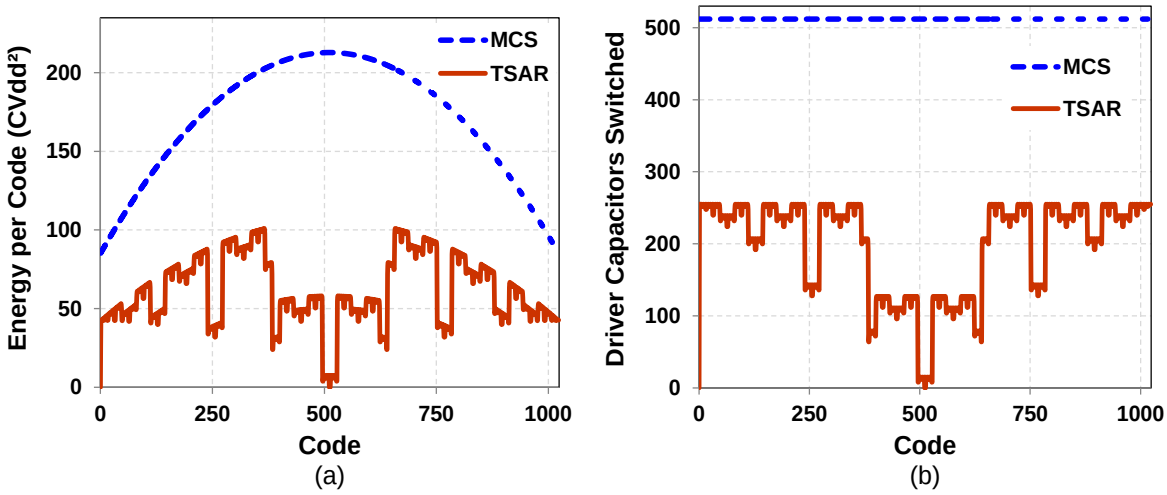

Figure 3.33: TSAR DAC energy and driver activity reductions (compared to the MCS SAR ADC)

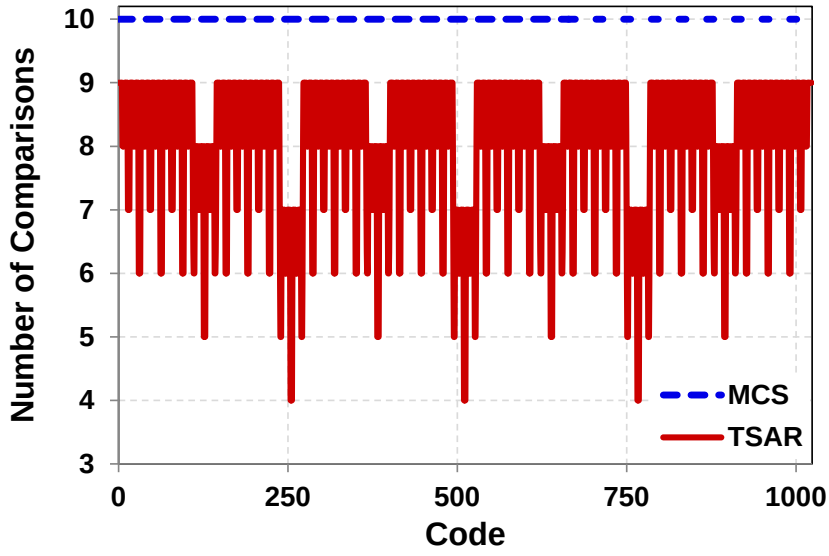

Figure 3.34: TSAR compartor activity reduction compared to the MCS SAR ADC

3.5 CMOS Circuit Implementation

The TSAR structure shares much of the same foundation as the MCS SAR [20], however to generate the ternary structure and efficient SAR core in submicron CMOS, a number of changes were made from the traditional SAR. These will be described in this section along with a rational for any major change.

The implementation block diagram showing a more detailed picture of how the TSAR functions is shown in fig. 15. Here the blocks are also color coded by analog (contunous in

voltage and time domains), discrete (continuous in voltage domain but not time), asnchronous (continous in time domain but not voltage), and digital (neither continous in voltage or time domains) charicteristics.

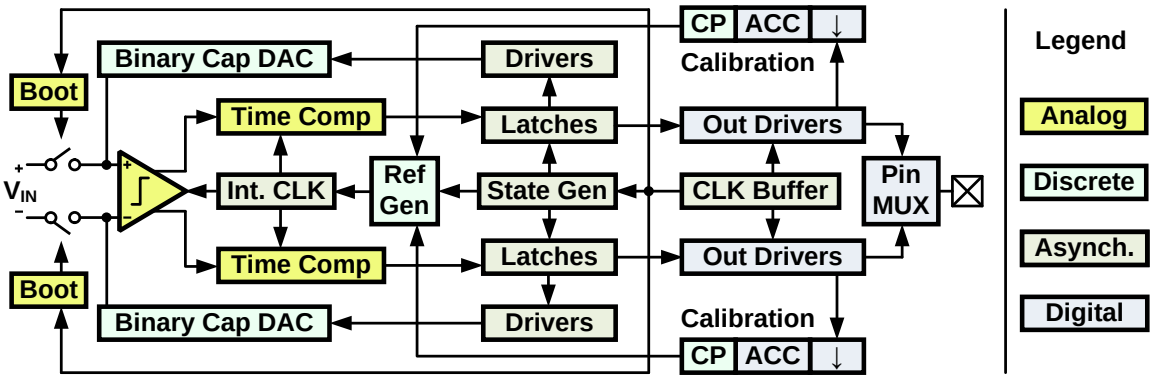

Figure 3.35: TSAR detailed implementation level block diagram

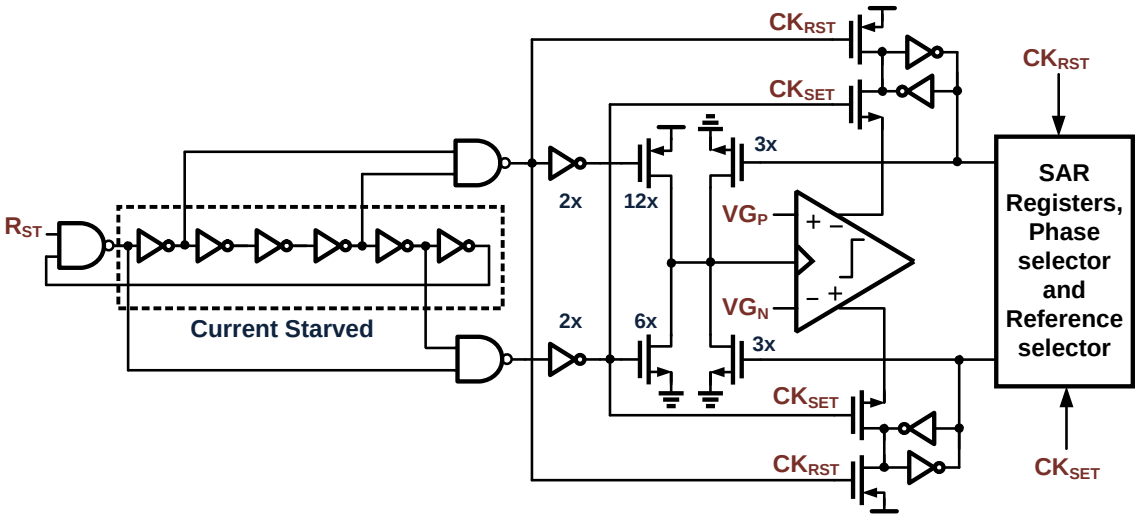

Figure 3.36: TSAR analog core implementation including quantizer, internal clocking, and SAR

3.5.1 Quantizer Implementation

The quantizer of the TSAR consists of a high accuracy dynamic voltage comparator that feeds into a time comparison structure as shown in fig. 16. The internal clocking unit of the quantizer consists of a current starved voltage controlled oscillator (VCO) started by the master system clock. The voltage comparator is shown in Fig. 17 and consists of a PMOS only latch [21] and properly sized input and clock devices for noise considerations [22]-[23], tested with transient noise simulations. The PMOS only latch allowed the input devices to sized much smaller than

the traditional stongarm latch to meet the given noise specifications, resulting in a reduced virtual ground loading and kickback transient. The output buffers contain a high VTH inverter pair to prevent comparator glitching that can occur when both latch nodes fall with small input signals. Following the output buffer are two matching time latches that perform the time quantization and they are separate since the digital outputs of the comparator are independent at this point. These latches consist of a gated and buffered back to back inverter pair that are enabled and reset by the high and low states of the quantizer clock as shown in Fig. 18. Many other time latches were explored including flip-flops, SR latches, and time arbiters, but this latch provided the best tradeoff between delay, power, and latching strength.

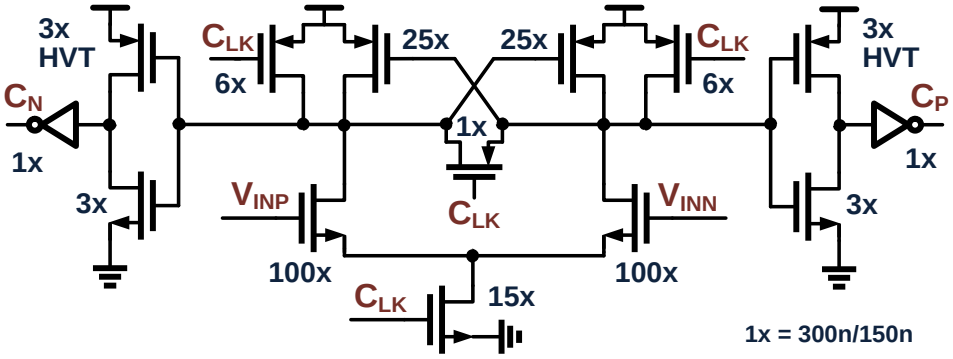

Figure 3.37: P-Latch buffered dynamic comparator used in the TSAR quantizer

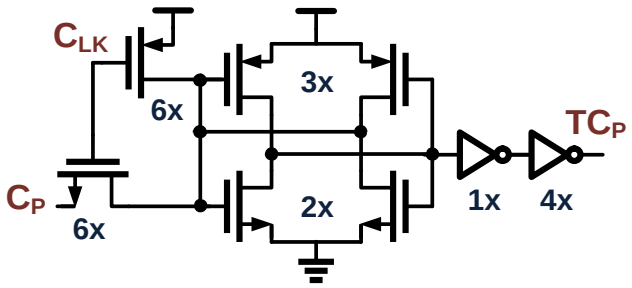

Figure 3.38: Time comparator structure half

When the clock to the quantizer rises, the voltage comparator begins regenerating, driving one output low. At the same time, the time latch becomes transparent allowing the output of the voltage comparator to pass to the SAR logic. On the falling edge of the clock the time latch opens and the voltage comparator is reset. If the voltage comparator output resolves to a logical “1” or “0” before the falling edge of the clock, then that data is passed thought the time latches and to the SAR, which drives the DAC during the reset phase. However, if the voltage

comparator does not resolve before the falling edge of the clock, the time latch outputs no data and the SAR assigns the midcode (“01”) for that stage. Thus, the TSAR time quantizer reference is based on the pulse width of the clock which is modulated by the reference voltage applied to the internal clocking VCO. Once the quantizer clock falling edge arrives and the time comparator data is latched, the DAC will operate if needed and the next SAR phase will be triggered as shown in Fig. 19. The SAR phase change will trigger a reference change if there is a reference grouping switch. This reference change will in turn control the pulse width of the next quantizer clock. One note is that in the actual implementation shown in fig. 16, the rising and falling edges of the quantizer clock are not explicitly used, rather a two non-overlapping clocks are generated that preform the same function but eliminate the possibility of crowbar current through the time comparator is for some reason both the PMOS and NMOS are both on together.

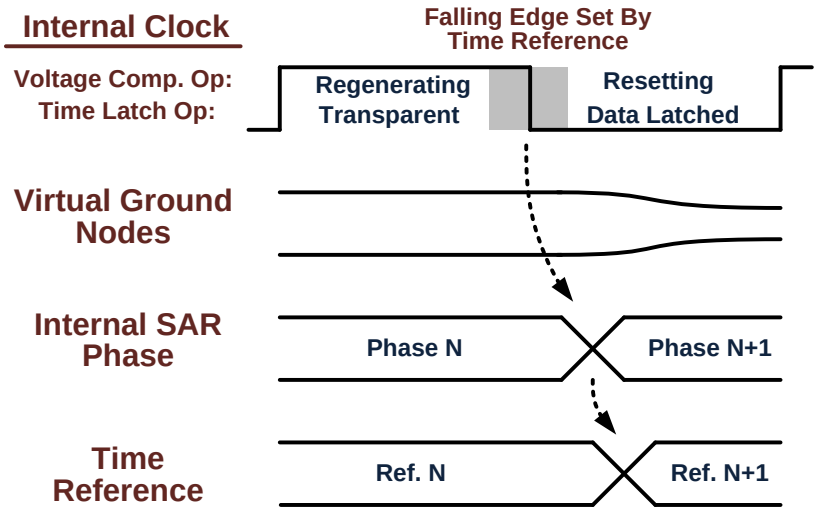

Figure 3.39: Critical path timing diagram for a large input signal

One final quantizer addition is that the comparator clock is partially gated as shown in figure 16. While the P-Latch comparator has a much better input device size to noise ratio than the strong-arm, it has the drawback of burring continuous static current is the input is small (since neither input NMOS device is fully turned off to stop the flow of current on the “1” side). To prevent excess energy dissipation, the comparator is turned on by the quantizer clock, but can be turned off in three ways. The first is by the inverted quantizer clock, signifying the end of the quantization phase and the start of DAC settling, or from the asynchronous latching of either

time comparator. Since the state clock from the VCO is present, this is not a fully asynchronous system which means there is no additional analog metastability, meaning that the power savings based on this input signal is achieved without an increased bit error rate (BER).

3.5.2 Logic Implementation

The TSAR critical path logic is similar to that of the traditional SAR structure, however contains some modifications. Typically, the SAR contains a ring counter made of flip flops to synchronize the SAR operation and another set of latches or flip flops to grab the digital data [21]. In the TSAR implementation, skipping logic blocks are added in order to either enable or skip the next phase from being generated as shown in fig. 20. These logic blocks shown in fig. 21, examine the current cycle and digital outputs in order to enable either the next state or the first state of the next time reference grouping. The logic to perform this skipping algorithm is shown in fig. 22. Here you can see that flip-flops coordinating states within each of the groupings are linked though a feedforward path to the first stage in the next grouping. If the current stage outputs don't change before the next clock cycle, the current state flip flop will be gated by the NOR input logic and the first stage of the next grouping will be enabled, allowing states to be skipped over which performs the desired SAR cycle reduction. Also, fig. 22 shows that the state machine is implemented as a one-hot ring counter with the initialization being provided by a dynamic logic based latch. The one-hot counting scheme allows the data storage function of the SAR to be implanted with latches and not flip flops, mitigated a large amount of logic power consumption.

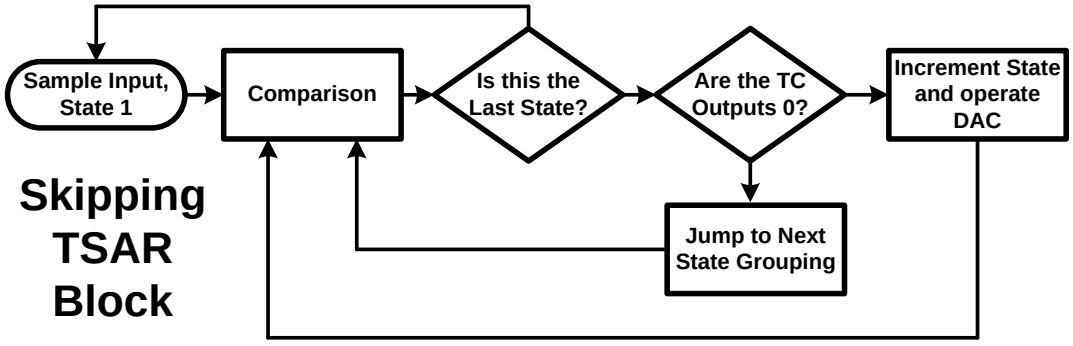

Figure 3.40: Skipping implementation algorithm using grouped redundancy levels

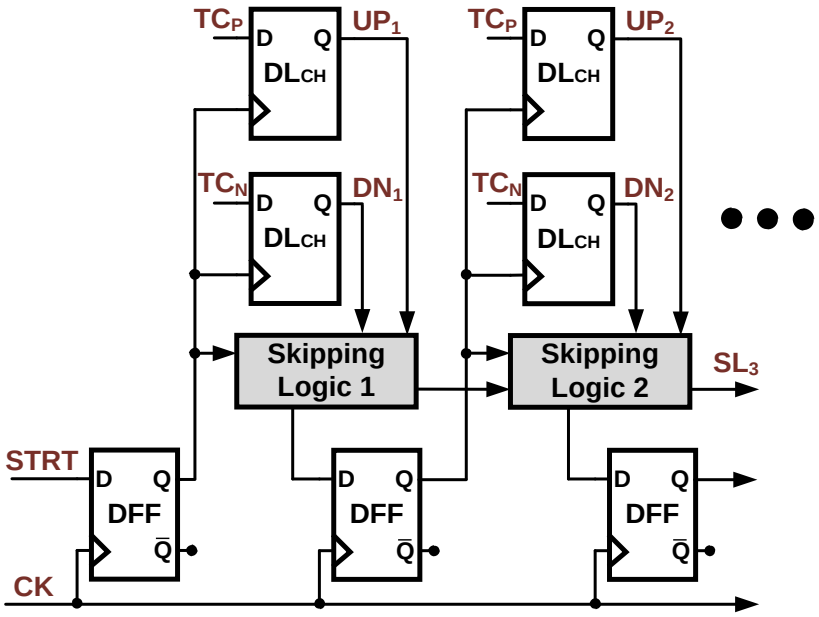

Figure 3.41: TSAR logic block showing location of skipping logic based on data and state

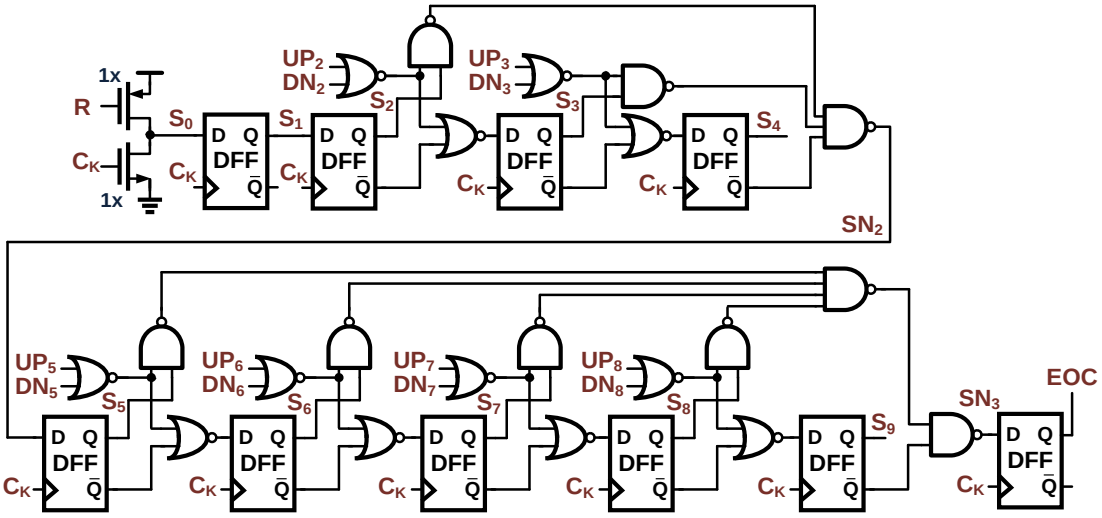

Figure 3.42: TSAR state machine with feedforward skipping paths

Another modification that was made is to the actual flip flops used in the state synchronization. In order to reduce power and provide an easy reset capability, the traditional dynamic TSPC flip-flop was utilized [24]-[25]. The dynamic nature of the flip-flop is not an issue since it is not in the critical timing path and setup and hold requirements were not violated. One downside of using this structure however, is that when the input is a logical zero and the clock is applied, a large amount of energy is used due to internal switching, as shown in table 1. This can be mitigated by clock gating [26], however that requires a large overhead for such a

small ring. Another solution is shown in Fig. 23. Here an extra PMOS transistor is added as an internal gate when the input is low, which is the majority of the time in a SAR one-hot ring counter. With this simple modification, the dynamic power of the ring counter can be reduced by nearly 70% resulting in a significant logic power savings. The one downside of this modification is that the setup time is now increased by nearly 50%, but in this application, the ring counter clock will not induce a setup time violation.

Bit (N-1)	Bit (N)	Energy TSPC	Energy Proposed
0	0	7.93 fJ	0.10 fJ
0	1	3.73 fJ	3.67 fJ
1	0	9.10 fJ	6.69 fJ
1	1	0.02 fJ	0.02 fJ

Table 3.2: Flip-flop energy per clocking event based on input and past state

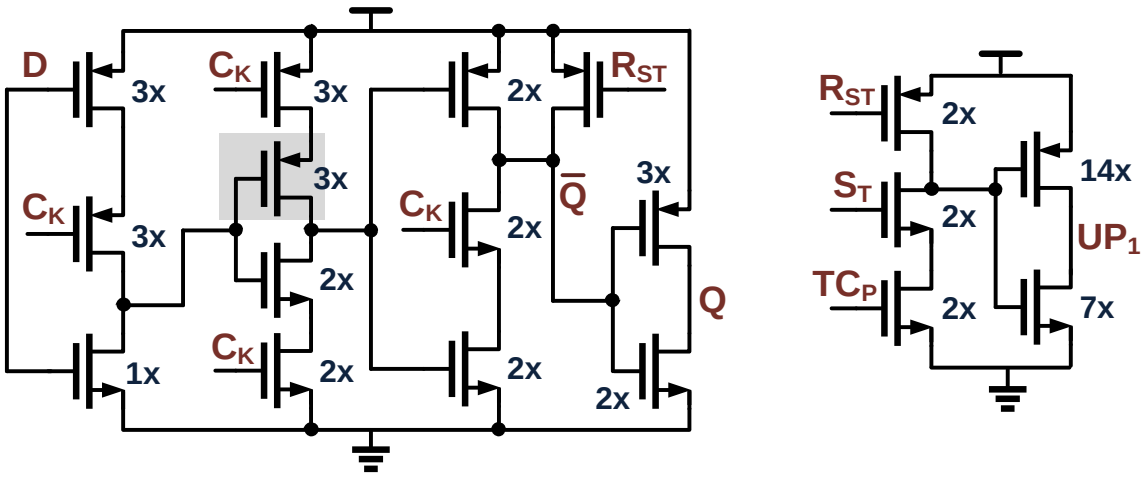

Figure 3.43: TSAR state flip-flop (left) and data latch (right)

To grab and hold the data coming from the modifed quantizer a dynamic latch was used over a flip-flop based design, both for energy reduction and because the output of the comparator is not garenteed to be synchornous with a fixed state clock. The timing of the latch is such that it is transparent when the time comparator is enable and shuts off just after the time comparator is opened with a delayed clock edge. The dynamic latch was used over a static

vesion for power conusmption, but this also means the latch must always close after the time comparator to prevent metastability. This is not difficult though as an inverter based delay can provide enough quantizer and latch clock spacing to prevent glitches. The latch structure is shown in fig. 23 and is optimized for both speed and energy.

The final piece of the logic puzzle is the analog mux used to switch between time reference levels which are implemented as voltages sent to the internal clocking VCO. This muxing mechanism is shown in fig. 24 and is slightly more complex then a typical analog mux due simply to the psudo-asynchronous nature of the single phase logic opration. As shown, the intial reference R1 is connected to the VCO at the start of the conversion with a dynamic latch. Then, on the rising edge of the first comparator clock, the state ST1 is entered, which enables the data latches for the first bit. This ST1 is also the signal for the reference to switch to R2 which is used for the second time grouping, however some timing caution must be used because in the rare event that the logic delay is so small and the comparator delay is so large that the reference switches before the end of the first compartor regeration, there could be some reference overlap leading to potential glitches. To be safe and prevent errors, the state information is gated by a slightly delayed internal clock edge before triggering the next reference switching. R2 in this case is then disconnected when the next reference R3 is connected. The connections of R3 and R4 are not dependent on a single state, but depend on the enableing of the first stage of the thrid and fourth group which is determined by the skipping logic (SN2 and SN3). Finally it should be noted that resitive and capacitive delays are critical on the main mux line as a large time constant effects both the time reference during the next stage clock pulse and the line transient noise due to crosstalk and coupling. The output line capacitance should be large enough to settle transient spikes, but small enough to allow for quick switching.

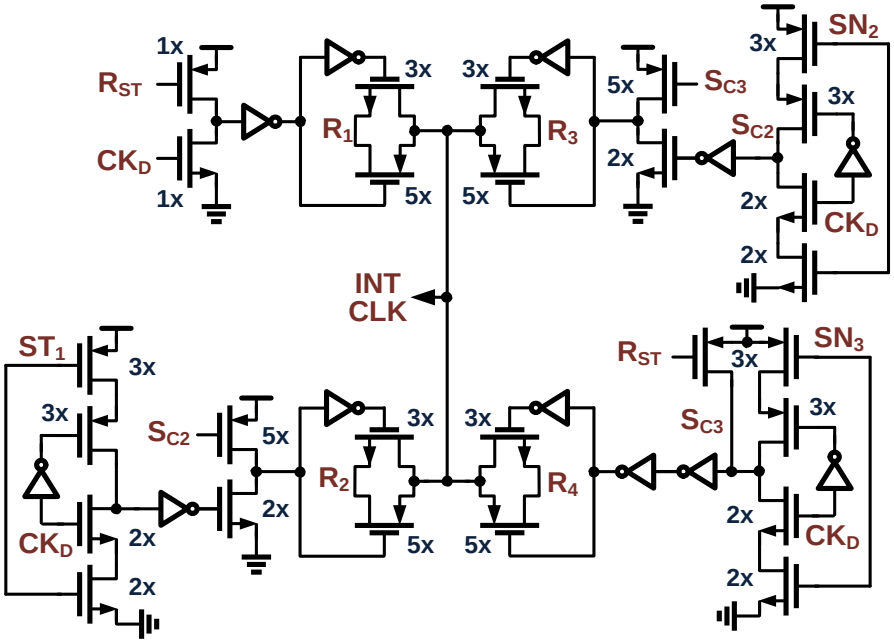

Figure 3.44: Time reference mux based on state output

3.5.3 DAC and Driver Implementation

The DAC of the TSAR is responsible for updating the SAR virtual ground nodes after each cycle with the correct subtraction value to minimize the full-scale range of the next stage. The DAC here is a capacitive charge distribution type that is binary weighted with no attenuation capacitor for linearity benefits as described in [27] and is shown in fig. 25. The capacitor array consists of unit elements of about 15fF arranged in a common centroid approach for improved matching [28]. The distribution of capacitors in terms of relative distance from the common centroid origin is also taken into account to improve matching and reduce radix errors due to non-linier gradient terms in the array itself as shown in fig. 26. In this figure, the bold horizontal lines represent were bottom-plate data lines were routed and the other horizontal lines are where the top-plate virtual ground node is located.

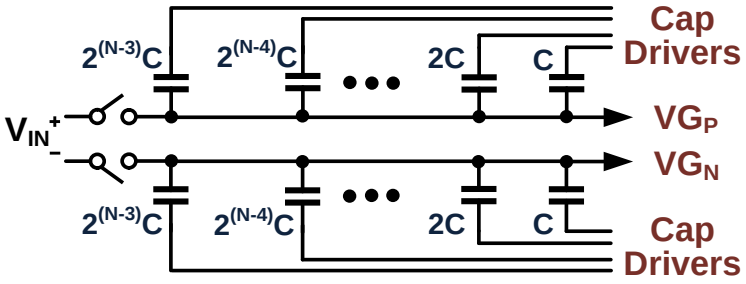

Figure 3.45: TSAR binary weighted capacitor array

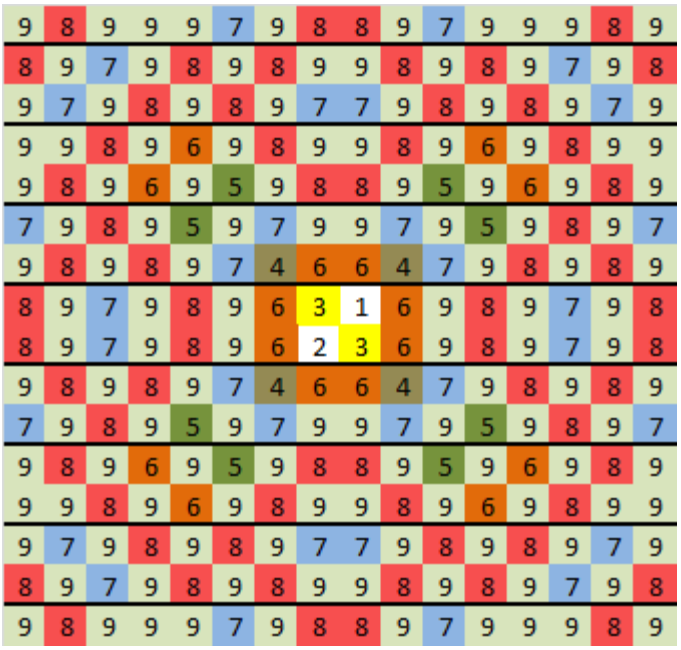

Figure 3.46: Capacitor array layout for distributed common centroid matching

For the DAC to operate, properly sized drivers are needed to switch the DAC to the appropriate bottom-plate voltages. Since the DAC has three levels, a three way analog mux is utilized with inverter based drivers sized for maximum power efficiency with the given speed requirement. One note is that the FOM is largely based on the driver efficiency, and this could be minimized further is a lower SAR bandwidth was required. A lower bandwidth means even more aggressively scaled drivers can be used, burning less energy per conversion, thus lower the FOM. Here the drivers were sized for 50MHz sampling functionality and the MSB driver unit is shown in fig. 27.

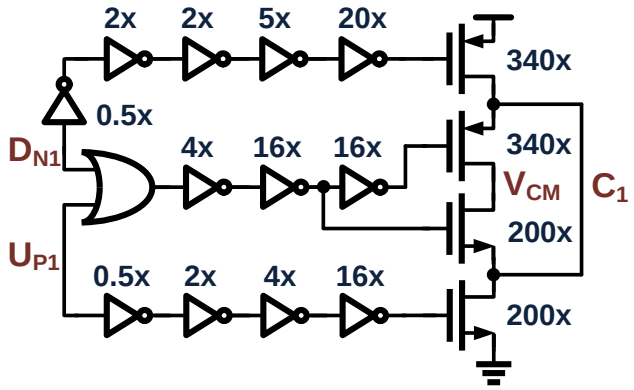

Figure 3.47: MSB capacitor three-level bottom plate driver

3.5.4 Interface Circuitry

While the TSAR core circuitry has been described, the interaction between that core and the outside world has a large impact on the overall efficiency of the structure. Perhaps the most important interface element for meeting accuracy requirements is the input switch. While only 13 bit accuracy is desired, this was still too high of a target to meet with simple transmission gates in 1.2V 0.13u CMOS technology (let alone with 0.8V). To meet the requirements, a Dessouky bootstrap switch was employed as shown in fig. 28 [29]. Here the bootstrapping capacitor was chosen as a balance of accuracy and timing requirements and the non-overlapping clock generator was generated locally and separately for either side to avoid digital coupling and crosstalk with the analog signals. Since the non-overlapping clock generator is only used for the input switch, the delays were timed to maximize the accuracy of the switch.

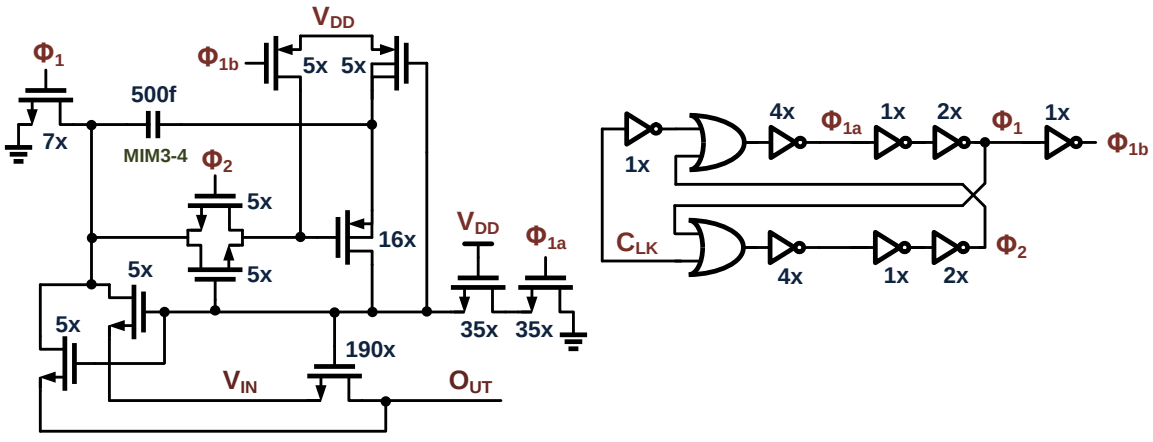

Figure 3.48: Input bootstrapped switch and non-overlapping clock generator

The other major analog signal that must get to the ADC core is the clock. The clock generator is shown in fig. 29. Here the master clock (CKM) is responsible for generating the digital clock (CKD) and the analog core clock (R) or reset clock. The main reset clock turns on to enable the SAR conversion (and internal clocking unit) based directly on the rising edge of the input clock and turns off based on the completion of the synchronous SAR algorithm through the end of conversion signal (EOC). To give some reset timing control, the delay of the EOC signal can be tuned though a current starved inverter chain. Also, since this is just a prototype chip and not a product, startup circuitry was not introduced, however a hard reset for latchup event was provided by the LCH signal. The digital clock feeds the output buffers and calibration and is the square wave equivalent of the input sine wave clock. When a given conversion has finished, the TSAR chip is in standby mode, which means the input is transparent to the capacitor array and no circuit activity occurs (however there is some leakage power) similar to [30]. One important note is that in some IC implementations, a resistive feedback is placed around the first input inverter to set the common mode, however in this case, the common mode is externally tuned for reduced on die power consumption.

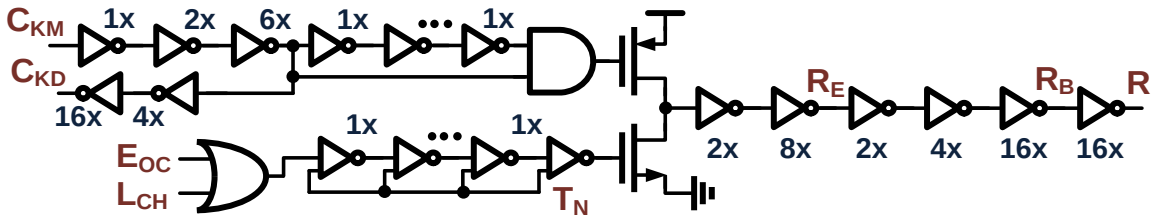

Figure 3.49: Input clock buffer and reset generator

To deliver the ADC digital data off the chip, the 20 raw bits (2 bits per binary bit) were sent out with 2 bits multiplexed onto one pin as shown in fig. 30. The output driver structure first sampled the data from the SAR latches though a low threshold inverter buffer for glitch prevention. The data was then latched by the reset conversion clock to ensure that all the data is re-timed together after the SAR is finished and is then sent across the chip to the output side. The data is then re-timed and 2 to 1 muxed onto pins with the re-timing insuring that each bit appears on the pin for exactly 50% of the master clock cycle (10ns at 50MHz). The muxed data is then driven to each pin with enough strength to allow for guaranteed valid data, but not too much so as to reduce substrate digital to analog coupling.

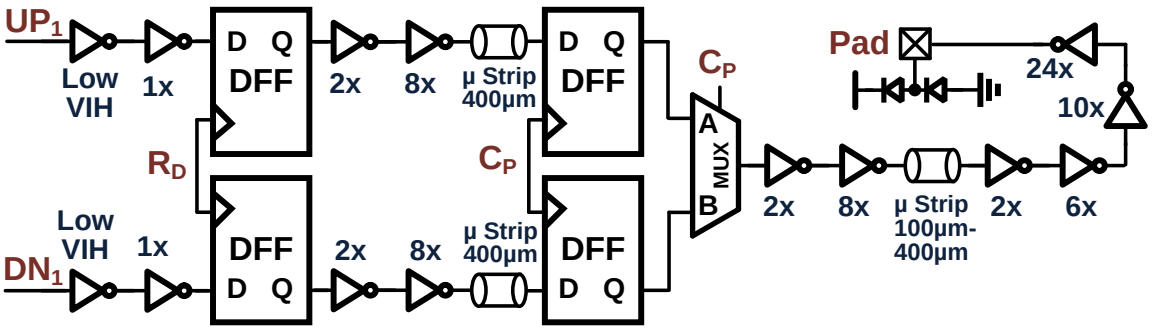

Figure 3.50: Data latching and digital output buffers for one slice

Another reason for the retiming of the data is to allow for the option of undersampling the output for noise considerations. Here, C_P can be digitally chosen though a clock muxing operation as shown in fig. 31. Even though the data is always latched at R, the outputs will only switch every C_P.

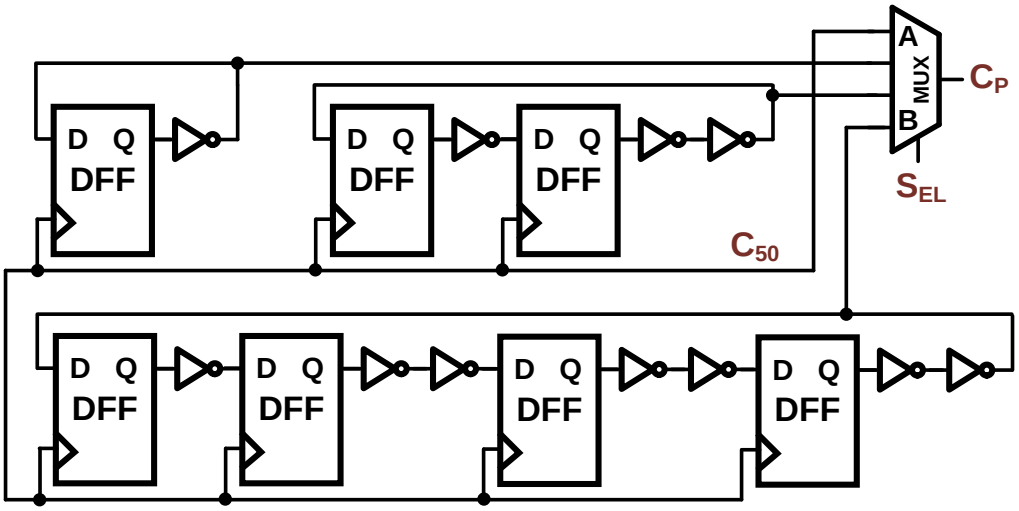

Figure 3.51: Pin driver clock selection mux for undersampling options

3.5.5 Calibration Implementation

As previously explained, in order to get the full final bit of resolution, the last reference (or two in the ternary flash case) needs to be slightly more accuracy, with the example of double accuracy for a 1dB SQNR loss. To calibrate the time reference, we can look at the statistical information of the last bit and determine whether to increment or decrement the reference. Ideally, a perfect time reference for residue shaping would mean that 50% of the last stage codes were in the redundant zone and another 50% were not (since the max extent of the

residue should be 10 $V_{FS}/2$ and the time references land the optimal redundancy voltage at $V_{FS}/4$). This algorithm can be easily implemented as shown in fig. 32. Here the up and down bit information for a stage are ORed and sent to a flip-flop operating at some fraction of the conversion frequency (in the chip, 1/64). Then, in the next cycle that redundancy data is accumulated and periodically, a pulse is formed incrementing or decrementing a dynamic charge pump based on the accumulator state (and the accumulator is then reset). One note is that there is perhaps a more optimal way of implementing this by looking at the rollovers of the accumulator, but this was not implemented in time.

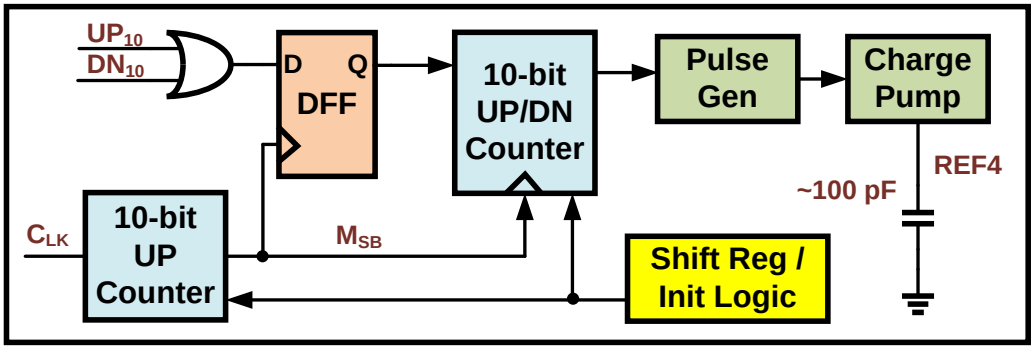

Figure 3.52: Time reference statistical calibration loop

The dynamic charge pump unit is shown in fig. 33. Here, the output of the accumulator acts as a gate to allow the clock pulse to travel to a dynamic charge pump only for the desired polarity. The charge pump transistors are sized to be approximately equal with large resistances in place both for minimizing the step size and ensuring equal up and down charging. By reducing the step size to be large enough to fight leakage plus a little extra, the bandwidth of the calibration is low, but the accuracy of the charge pump becomes negligible. Thus a very inaccurate pump can be used when compared with the active varieties often seen in structures like phase locked loops [31]. The voltage output is stored on a 100pF capacitor (can be made smaller is area is a concern) and feeds into the analog core reference mux.

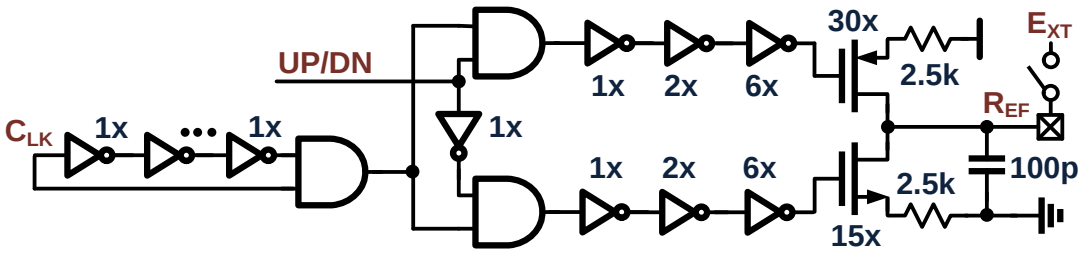

Figure 3.53: Calibration dynamic charge pump for setting voltage domain time reference

The accumulator structure is constructed as an up/down counter with reset JK flip-flops as shown in fig. 34. The JK flip-flops can be replaced with T flip-flops as well, but the JK variety was used here as it was readily available. On any strobing of the charge pump, the accumulator is reset and the accumulator operates at the divided clock frequency for a negligible overall power consumption.

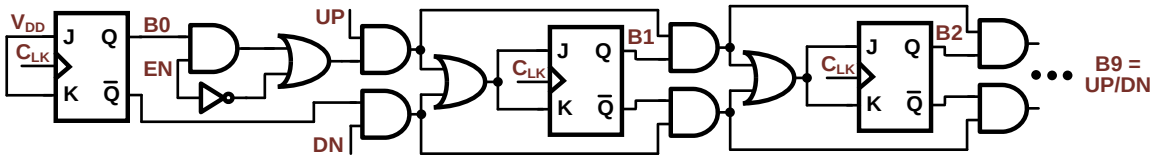

Figure 3.54: Digital accumulator used in generating the charge pump direction

3.6 Physical Design

While implementing a chip, there can be a number of issues that arise beyond the actual transistor circuit configuration and relate to the placement of components and the routing of signals. Here the layout will be described and critical block will be shown with an emphasis on the highest possible accuracy and speed with the lowest power design.

3.6.1 Top level Floorplan and Chip

The TSAR chip for the most part is a passively differential (pseudo-differential) structure, thus symmetrical layout structure was critical. The main chip floorplan is shown in fig. 35 and in this layout, the analog core circuitry is placed in-between the large capacitive DACs in order to reduce delays between the core components. The input signal is directly routed to the input switches and comparators with generous input shielding and clock generator and reference generator are placed as close as possible to the quantizer unit. The SAR data is placed at the end of the analog core to allow for easy routing to the output buffers and to reduce coupling to

the DAC units are this is the one circuit that is not possible to layout or operate differentially. Separate DAC drivers then drive each individual DAC unit and the other interface circuitry is separated from the analog TSAR.

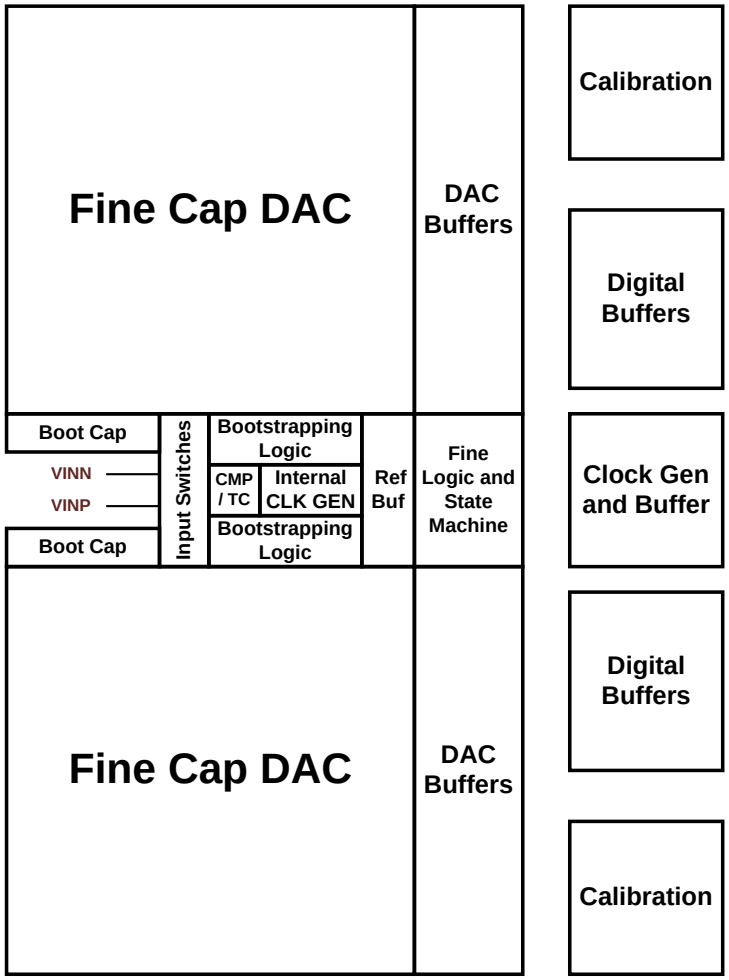

Figure 3.55: TSAR layout floorplan and input routing

The main die photo is shown in fig. 36 along with the calibration unit and the overall chip with pads. Here one can see that care was taken to insure that even the top level power routing was symmetrical to reduce distortion.

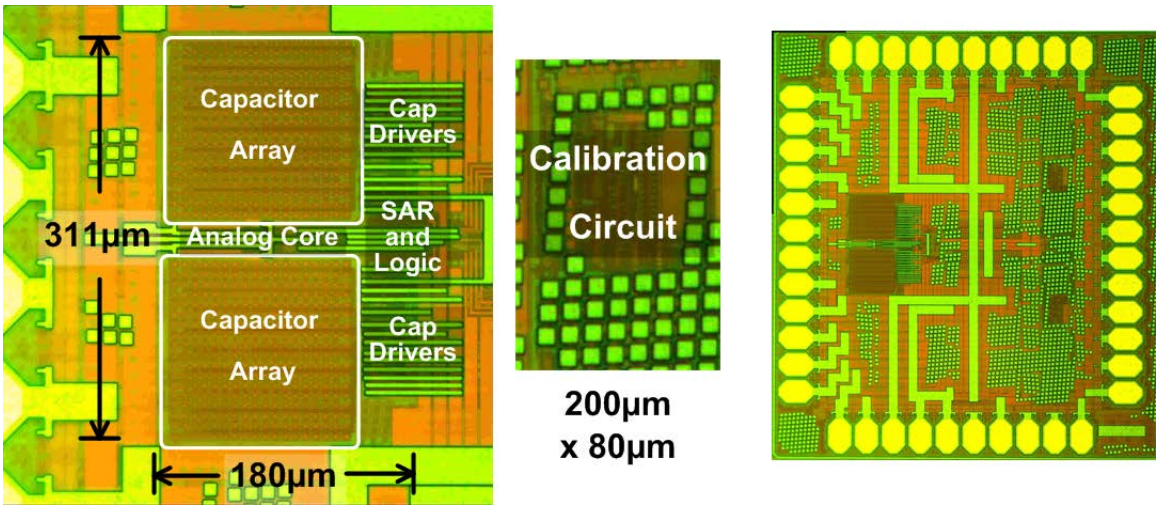

Figure 3.56: TSAR die photo along with calibration and full-chip views

The TSAR core is shown in the layout view in fig. 37, as placed in the Virtuoso tool by Cadence. Here, the relative DAC size is clear along with the input routing guarding. The whole TSAR chip is surrounded by decoupling capacitors to reduce chip noise and substrate coupling. The power routing is shown here on the top metal (metal 6 in yellow) across the whole analog core horizontally.

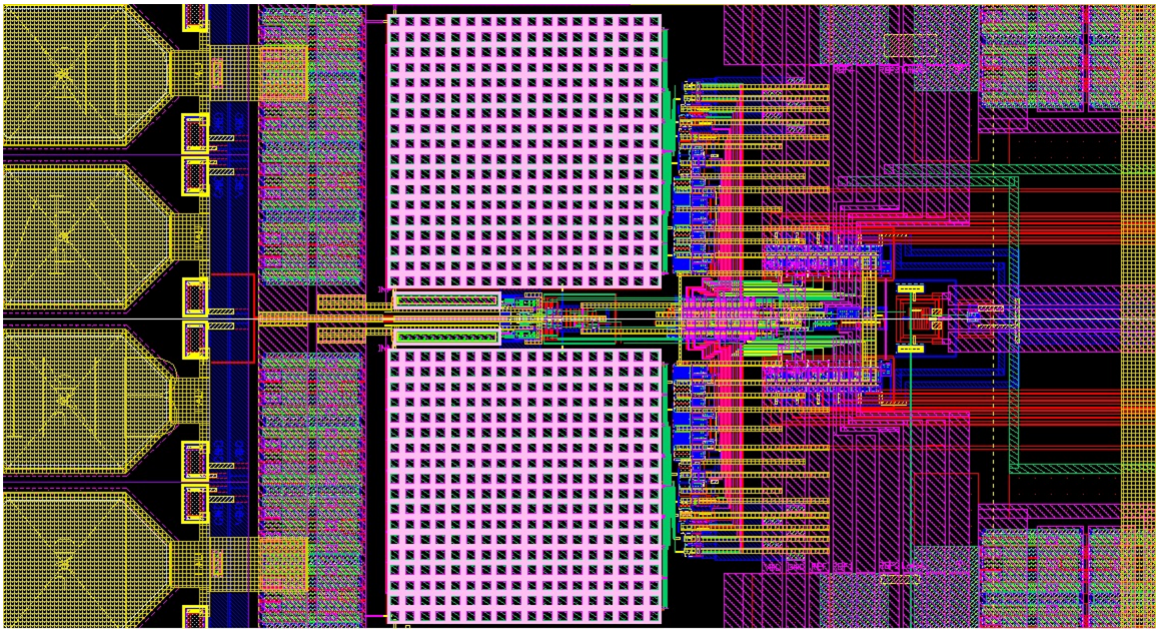

Figure 3.57: Layout tool view of the TSAR core circuitry and input path

3.6.2 Quantizer Layout

The quantizer layout is fully differential and is placed directly after the input switching in the analog core to minimize coupling and crosstalk. In most amplifier designs, the transistors are stacked, meaning that if the input came into the left side, the NMOS devices stack to the right followed by the PMOS devices after them. Here, the NMOS and PMOS device can be in parallel since there are effectively only 2 layers and no cascode transistors as shown in fig. 38. The tail source device and output buffers are then placed on the opposite side of the input to further reduce input coupling. It's also important to note that the center reset switch shown in fig. 17 is also split into 2 parts with halves on either side of the input device.

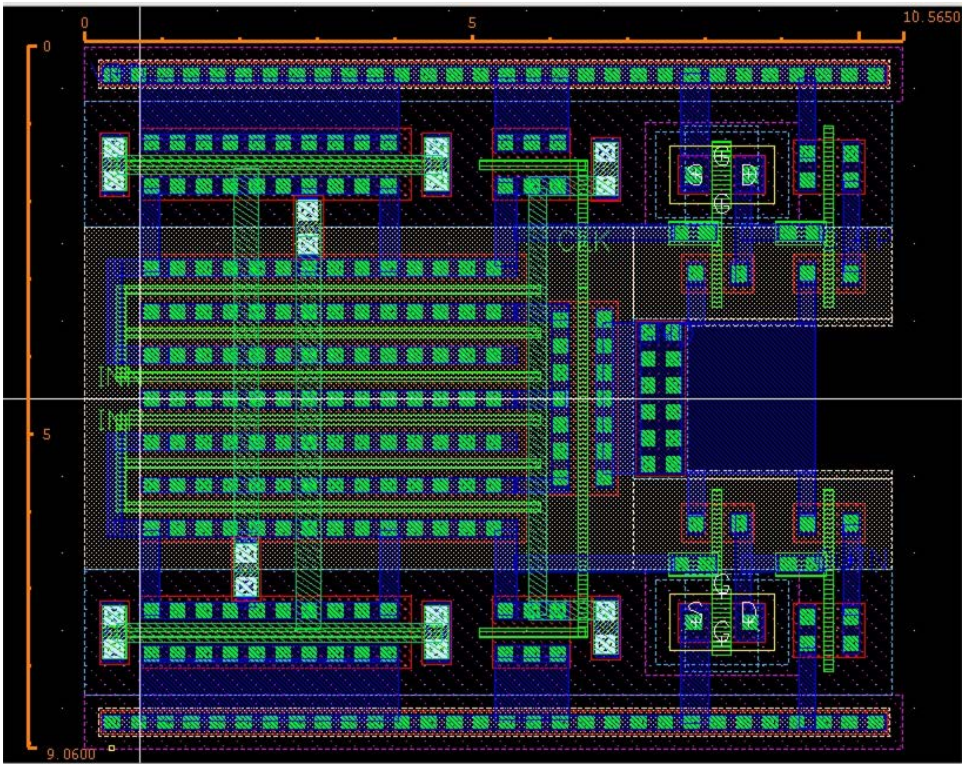

Figure 3.58: TSAR comparator and buffering layout

The time comparator structure is placed directly after the voltage comparator and before the internal clock generator to accurately grab the comparator output data. The structure has the input, reset and latch devices on the same layer as the voltage comparator with buffering rising above the quantizer level to reduce inference with the internal clock and directly feed the SAR registers as shown in fig. 39. Also, it is clear from the layout that the routing of the time comparator latch is critical for delay concerns due to the small latch area.

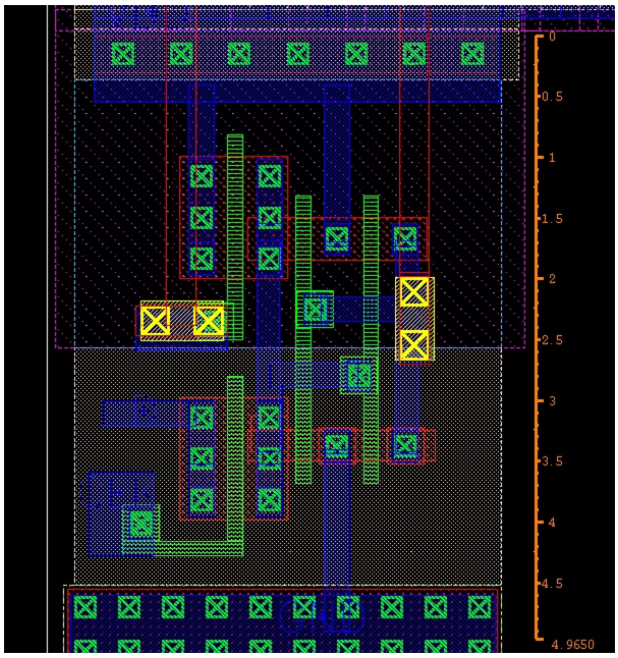

Figure 3.59: Time comparator layout side

3.6.3 DAC and Logic Layout

The DAC and logic form the majority of the area of the TSAR core and are both heavily shielded from the analog input and quantizer circuitry. The DAC is laid out in the configuration shown in fig. 26 with unit cells of 15fF. The unit cells were fabricated in both metal-insulator-metal (mim) and finger or flux capacitors as simulation options for device matching were not robust. The flux capacitors that were custom made turned out to have the better matching (perhaps due to improved process accuracies) and are shown in fig. 40. These are similar in to the capacitors of [32], just larger and in unit elements for common centroid layout.

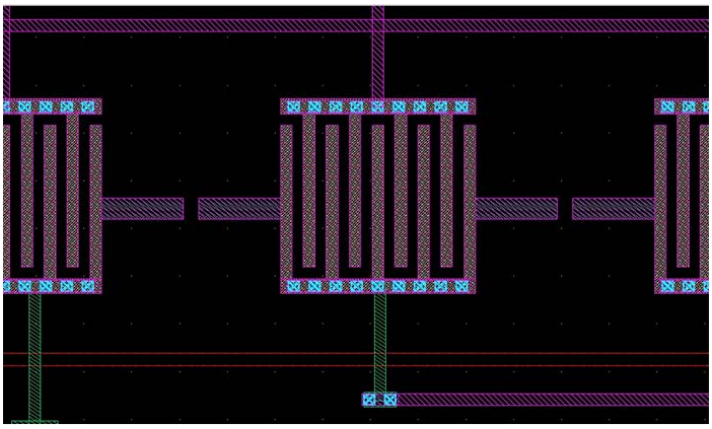

Figure 3.60: Unit finger capacitor layout for DAC

The SAR logic is placed on the edge of the analog core and is made as symmetrical as possible as shown in fig. 41. Here, the outputs to the drivers and output buffers are shown with separate wires on different layers (red and pink are layers 3 and 5 going to the drivers, green and yellow are layers 2 and 4 going to the output buffers). Directly to the right of the logic unit is the clock generator feeding into the TSAR state machine. The logic block is laid out to have the symmetrical latches on the outside with the non-symmetrical state machine on the inside so that parasitic loading seen by either half of the TSAR is the essentially the same.

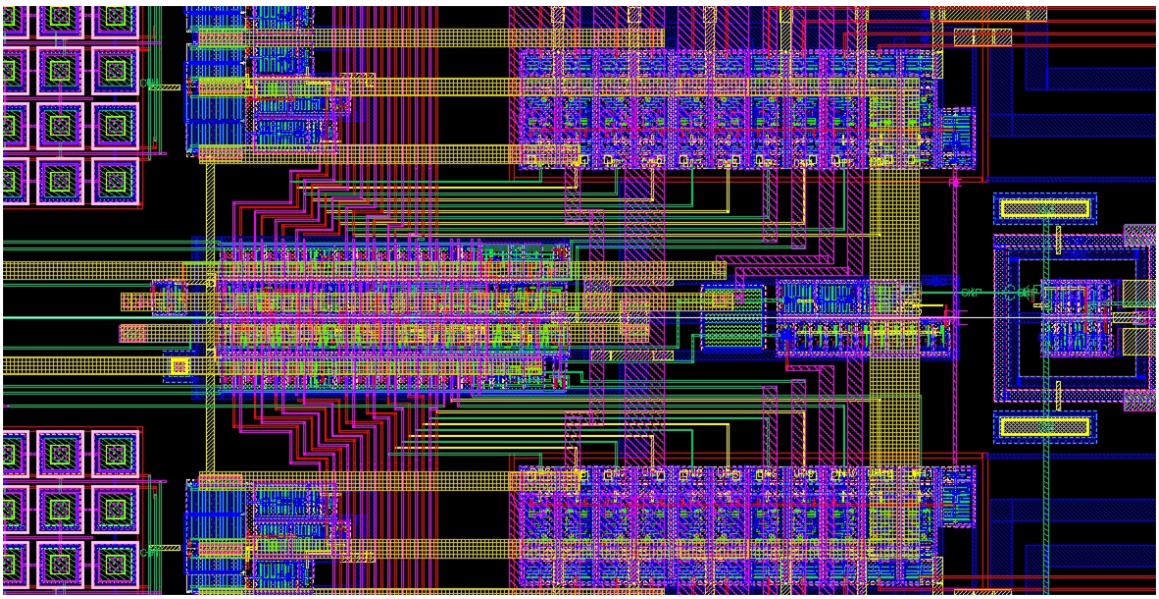

Figure 3.61: TSAR logic block and digital routing layout

Much of the TSAR logic is comprised of standard cell digital components, with the main exception of the custom TSPC dynamic flip-flop. Here, the layout, shown in fig. 42, was completed to reduce area as much as possible while leaving pad locations that are convenient for block wide routing lanes. The custom dynamic latch has similar physical design properties.

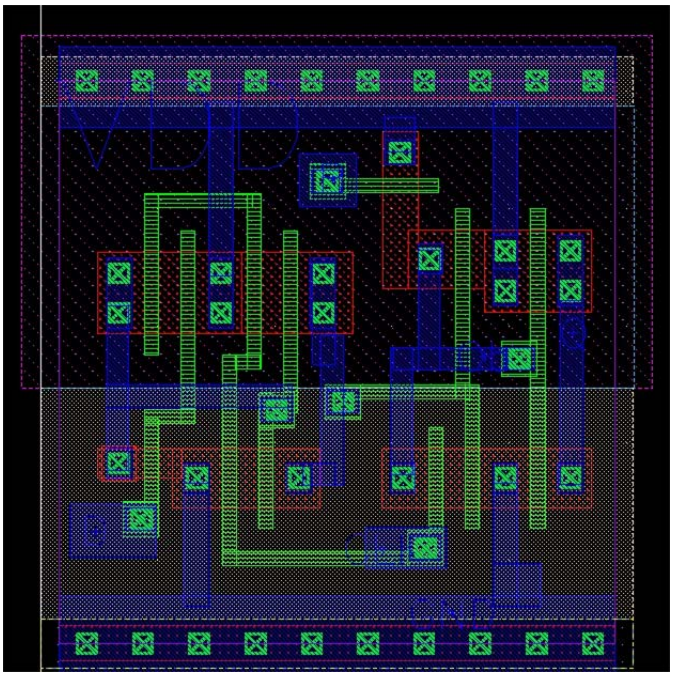

Figure 3.62: Layout for the custom low energy TSPC dynamic flip-flop

3.6.4 Interface Circuitry Layout and Placement

The interface circuitry also required careful layout and included the input switch, clock generator, and output drivers. The clock buffer was positioned such that the input master clock entered the core of the circuit and then the analog clocking path radiated out to the left of the core (strait to the SAR logic) with the digital path radiating to the right. The input of the master clock was positioned in the center of the chip with shielding surrounding the whole path to the generator circuit and only decoupling structures around the shield.

The input switch was placed within the pair of DAC units with the bootstrapping circuit elevated above the main switch to allow the shortest path possible to the voltage comparator as shown in fig. 43. Also, one can see that the bootstrapping circuit is larger than would be expected due to the spacing needed for the separate well for the high voltage PMOS gate drivers.

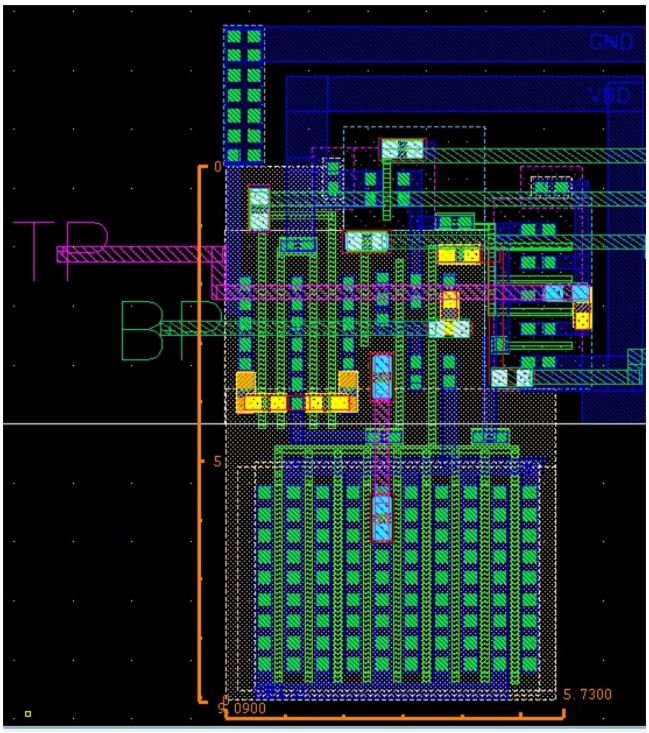

Figure 3.63: Input bootstrapped switch layout

3.7 Test Setup and Measured Results

To properly understand the idea of the ternary SAR ADC, the test prototype was characterized both to verify the ideas functionality and see how the structure interacts with non-ideal environmental conditions. The test structure and chip was setup in order to understand the accuracy, power and bandwidth limitations of the TSAR, measuring SNDR, linearity, input dependent power, and figure of merit (FOM).

3.7.1 Test and Measurement Setup

The measurement setup for the TSAR prototype is shown in fig. 44. Here the input is sent to the chip from a single-ended RF signal generator, split though a balun unit, and then passively filtered. The clock similarly comes from a RF signal generator as a sine wave and is then capacitivly coupled into the chip to be sliced by the input inverters. The supplies are all generated by low dropout regulators (LDOs) and the reference from active voltage dividers with a clean reference (and copious amount of decoupling). Finally, the digital outputs are buffered again on board before going to the logic analyzer and the digital inputs are generated from an Atmel microcontroller unit.

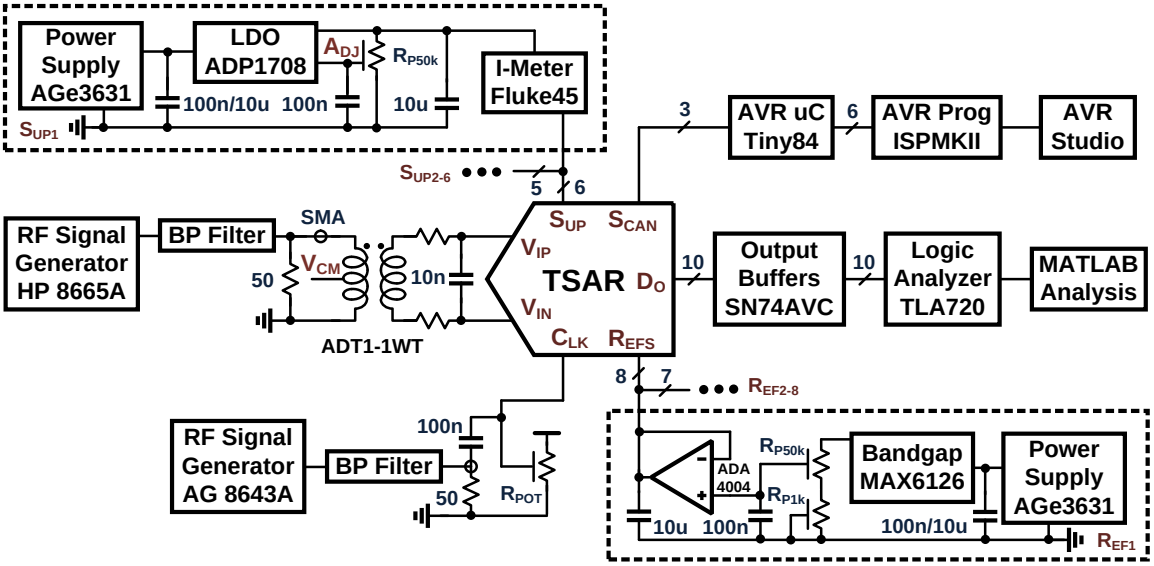

Figure 3.64: TSAR protoype measurement setup

To create the reference, supply, and digital control inputs, a testboard was created. The chip itself was placed on a separate daughter board (with input filters and output buffers) while a separate mother board was used for the other devices as shown in fig. 45. This allowed for numerous cheaper daughter boards to be used and for the chips to be soldered down permanently on a board.

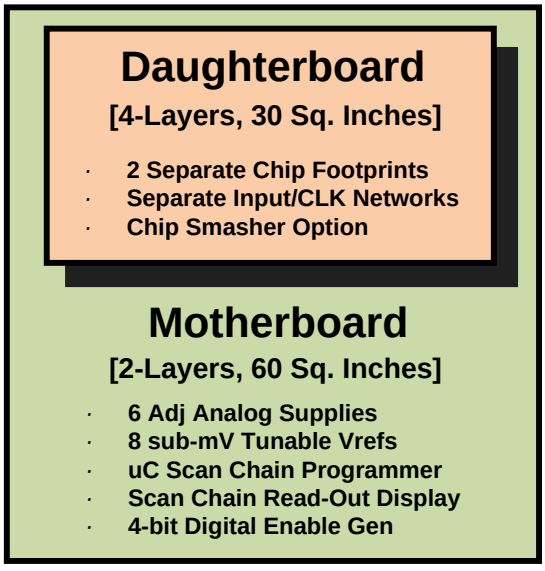

Figure 3.65: Test board mother and daughterboard configuration

3.7.2 Measurement Results: Accuracy

To characterize the test chip, a number of different accuracy measurements were taken both with the 10b and 12b prototypes operating up to 40MHz. The signal to noise and distortion ratio (SNDR) verses input frequency is shown in fig. 46 with the input signal always being at the nyquist frequency. Here the max resolution is shown to be at about 9.7b at 1.2V and 9.3b at 0.8V (for the 10b prototype). The resolution degrades some with frequency due to clock and input signal paths, but is not due to any core limitations since the core is clocked at the same frequency regardless of the overall conversion rate. For sampling bandwidths lower then 50MHz, the TSAR is powered down and placed in the sampling state for an extended period.

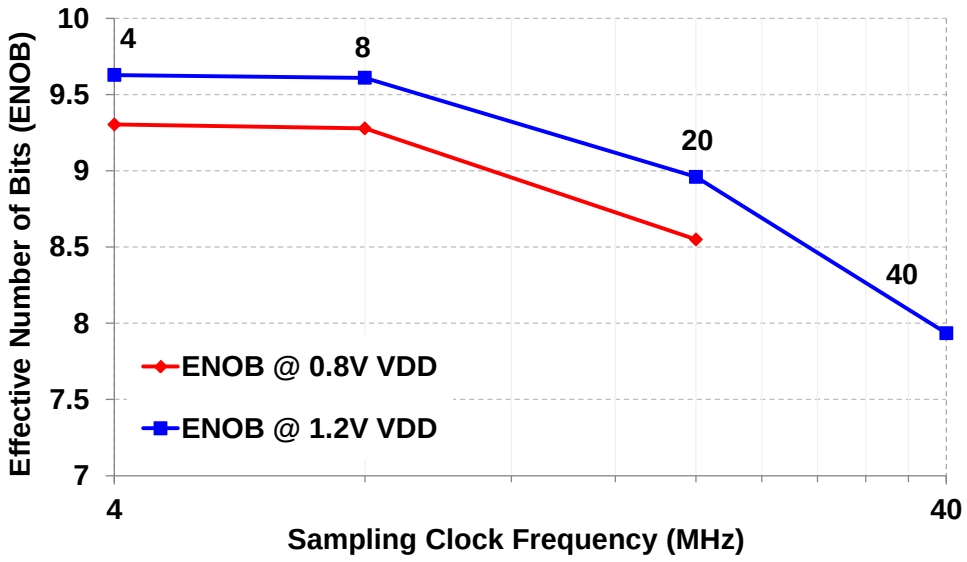

Figure 3.66: SNDR vs. sampling frequency for the TSAR 10b prototype

At 8MHz and a supply of 0.8V, the power was 83.8µW, which, with an ENOB of 9.28, results in a figure of merit (FOM) [33] of 16.9fJ/C-S. The frequency response at this point is shown in Fig. 47 and it can be seen that the resolution is not distortion limited, (note this is with foreground calibration to remove small radix errors from the capacitor array). A 12b TSAR structure was also measured where an extra two bits were gained by allowing the time comparator to act as a 2b backend flash. Here the power was not increased from the 10b prototype since this backend resolution increased was present, but not used in the original TSAR test chip. Here at 8MHz and a supply of 0.8V, the power was 75.2µW, which, with an ENOB of 9.87 results in a FOM of 10.02 fJ/CS.

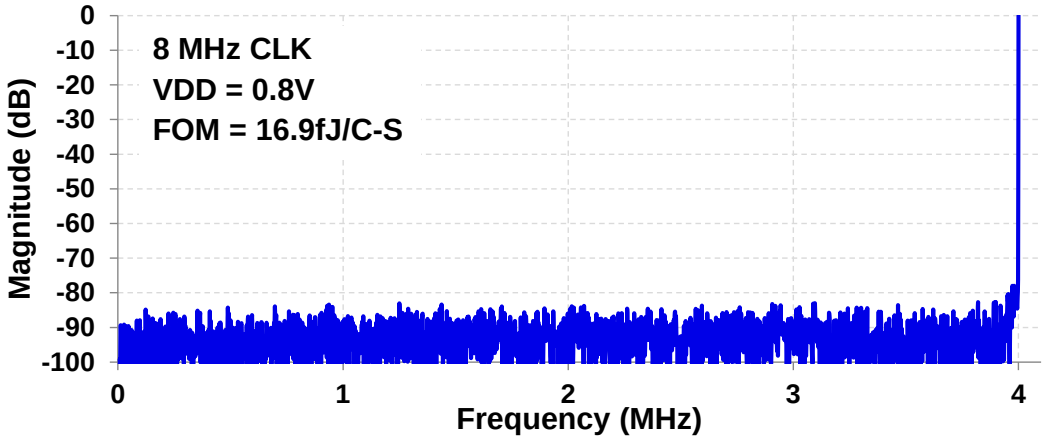

Figure 3.67: TSAR output FFT at 8 MHz sampling with a 4 MHz input

The INL and DNL plots are shown in fig. 48 for the 12b prototype. There is some large non-linearity at the 12b level due to the radix errors and last stage reference inaccuracy, but this is also reflected in the ENOB figure of 9.87. These plots are before the foreground calibration and with calibration, the INL variation become significantly reduced.

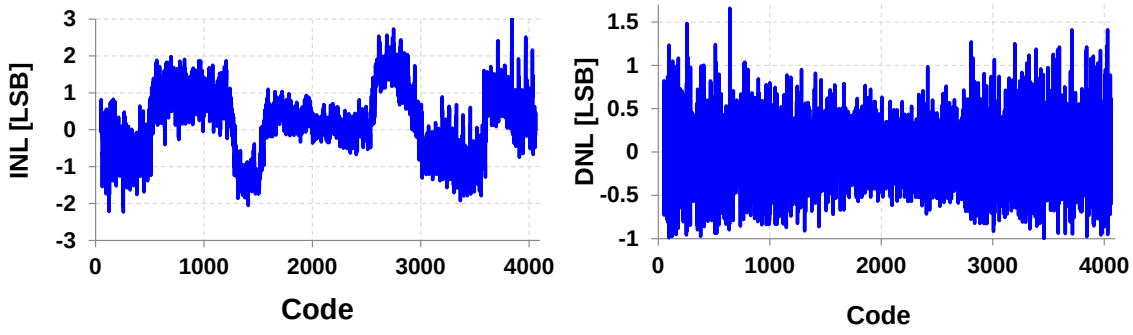

Figure 3.68: INL and DNL of the TSAR prototype with no radix calibration

3.7.3 Measurement Results: Power

The power consumption was a main concern of the TSAR structure and at 8MHz, the chip burns 75.2uW at 0.8V and for the 12b prototype and 83.8uW for the 10b prototype. The improvement stems mainly from some leaking flip-flops that were fixed in the second version. Since the power is nearly all dynamic, the power scales linearly with sampling frequency, with exception of very slow operation, where leakage plays a larger factor. The overall power consumption of the prototype TSAR was reduced by 26% in testing by enabling the time quantization at 8MHz when compared to no time comparison. Also, due to the windowing

effect, especially in the early TSAR stages, the power of a small input is much lower than that of a large input as shown in fig. 49. This is much different from most other structures where the power is uncorrelated to the input determination trajectory and this structure shows about a 30% power reduction for small inputs. This makes the architecture a good choice for signals that are normally quiet but have sparse transient inputs. Furthermore, the time threshold levels can be modified for even lower power in the presence of small inputs.

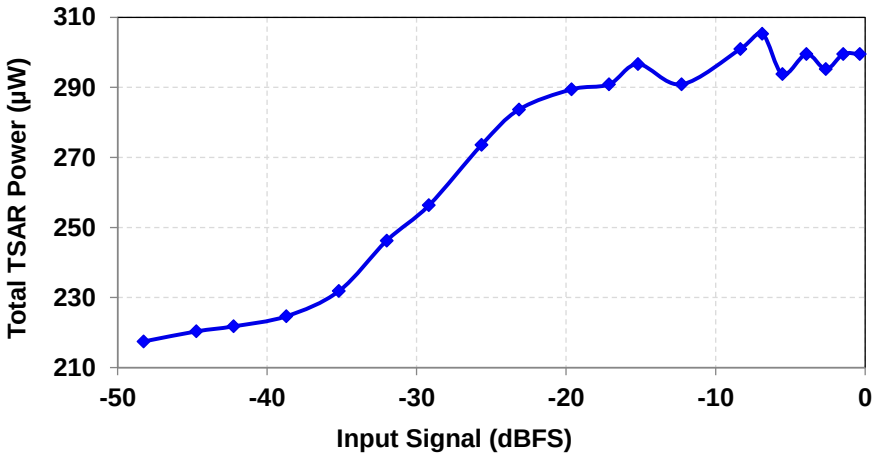

Figure 3.69: TSAR power consumption vs. input magnitude

The power consumption of the SAR is dominated by the DAC and comparator blocks. From simulation, the DAC (capacitors and drivers) consume 40% of the total power with the fine voltage comparator taking 38%. Since the time comparator structure is simple and sized for lower accuracy, it only consumes 6% of the total overall power. The remaining 16% of the power is consumed by the digital logic and clocking circuitry. Also, the power could have been further reduced if the DAC were sized for thermal noise limitations, not mismatch, if the voltage comparator were better analyzed, and if a smaller process nod could be used for the logic implementation. The power breakdown is shown in fig. 50.

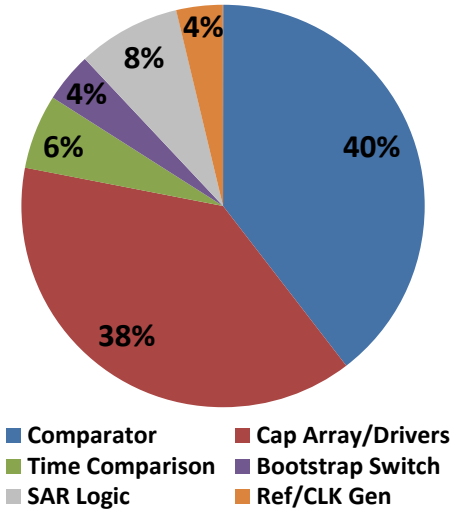

Figure 3.70: TSAR power breakdown from simulation

3.7.4 Results Comparison

Compared to other ADCs, this structure has a god efficiency rating (FOM) although not the best. However many of the much better ADCs were running at lower bandwidths and accuracy requirements. Table 2 shows a comparison table with various other ADC varieties that are in a similar accuracy and bandwidth range. Here the TSAR is very comparable and has a competitive FOM number. It's important to remember though that test chip numbers often depend on the experience of the circuit designer more than the idea merit, so read with caution.

Specification	TSAR	TSAR	TSAR + BE	JSSC 2010 [34]	VLSI 2010 [3]	JSCC 2011 [7]	JSSC 2010 [35]
Architecture	SAR	SAR	SAR	SAR	SAR	SAR	SAR
Technology	0.13µ	0.13µ	0.13µ	90n	0.18µ	0.13µ	0.13µ
Sampling Rate (MS/s)	8	20	8	100	10	40	50
Supply (V)	0.8	1.2	0.8	1.2	1.0	1.2	1.2
ENOB	9.27	8.96	9.87	8.6	9.83	8.11	9.18
SFDR (dB)	76	78	79	71	69	58	62
Power (uW)	83.8	526	75.2	3000	98	550	826
Area (mm^2)	0.056	0.056	0.056	0.18	0.086	0.32	0.052
FOM (fJ/CS)	16.9	52.8	10.0	77	11	50	29

Table 3.3: TSAR performance summary and comparison

3.8 TSAR Conclusions

This chapter has proposed a Ternary SAR (TSAR) ADC with sub-ADC decision time quantization. The TSAR structure examines the transient information of the voltage comparator regeneration in a traditional SAR loop to provide increased performance. Improvements include enhanced accuracy through redundancy, residue shaping, and statistical calibration, increased speed though reduced comparator delays and capacitor settling time, and reduced power consumption though stage skipping, DAC activity reduction, and logic modifications. Switching and driver energy were both reduced by about 60% and comparator activity was reduced by about 20%. This idea was demonstrated though a prototype implementation in 0.13μm CMOS with a FOM of 16.9fJ/C-S for the 10b TSAR and 10.0fJ/C-S for the 12b structure. Later chapters will explore ideas from this chip (residue shaping) and propose modifications to mitigate many of the limitations of the circuit and further improve efficiency (FITSAR).

3.9 Acknowledgements

The author would like to thank Tower JAZZ semiconductor for fabrication. This work was funded in part by the Center for Design of Analog-Digital Integrated Circuits (CDADIC) and Texas Instruments. The author also thanks Manideep Gande, Hari Venkatram, Allen Waters, Taehwan Oh, Amr ElShazly, Shannon Guerber and Ren Shackmann for validation and editing assistance as well as the anonymous reviewers who imparted valuable feedback for the journal version of this chapter.

4. RESIDUE SHAPING

In the past two chapters, we have described the need for high performance ADCs and seen how the TSAR structure can achieve high efficiency. In this chapter, we will take a closer look at the concept of residue shaping and how it applies to a variety of architectures. We'll start by taking an in-depth review and look at the concept of redundancy, and then mathematically and conceptually describe how residue shaping appears for multi-stage ADC structures. Following the derivations, the chapter will examine how to design for greater residue shaping benefits both ideally and in the face of comparator offsets.

4.1 Multi-Stage ADC Redundancy

For medium to high resolution and bandwidth specifications, multi-stage ADCs such as pipeline, algorithmic, and SAR structures are often used to obtain the needed resolution with increased sample rate (pipeline), power (SAR), or area (algorithmic) benefits. These inherent structural advantages can be enhanced with the use of redundancy, which has been briefly described in the previous chapter. Redundancy is the act of performing extra quantization on the input to an ADC stage, while maintaining the same overall ADC resolution, in order to achieve a greater tolerance to non-ideal effects that cause over-range errors. This allows for the ability to compensate for settling errors [1]-[3], reduce the impact of comparator offsets [4]-[5], allow for PN injectable background calibration [6]-[10], permit advanced correlated double sampling techniques to reduce amplifier gain requirements [11], and enhance the radiation hardening of critical high stress ADCs [12]-[13]. Generally, the resulting benefits of redundancy include increased speed, reduced circuit power and complexity, and the ability to compensate for device and environmental mismatches.

The impetus for the use of redundancy is to tolerate small over-range errors caused by non-ideal circuit behavior, and different types of redundancy implementations have been utilized over the past decades. It will be shown that the type of implementation can have varying effects on the statistics of the residue of each stage of a multi-stage ADC. This chapter will analyze the statistical nature of the residue after each stage and demonstrate that for some quantization noise limited multi-level redundancy configurations, an extra 6dB of resolution can be achieved. First however, this section will classify the various forms of redundancy based on

statistical and implementation differences before introducing residue shaping later in the chapter.

While the various types of redundancy in multi-stage ADCs play the similar role of correcting over-range errors due to circuit and environmental non-idealities, they can be generally classified based on implementation and statistical behavior. In this paper, redundancy will be grouped into the four general categories of half-bit, conventional restoring with Z added levels (CRZ), sub-radix, and extra stage. There is of course categorical overlap in some modern redundancy schemes, but for simplicity only these four sets will be described. Also, only multi-stage ADC redundancy is considered here, not redundancy provided by system processing such as in some communication protocols [14].

4.1.1 Half-bit Redundancy

Half-bit redundancy is commonly found in pipeline and algorithmic ADCs but can also be present in SAR structures [15]. Historically, this redundancy was created to mitigate sub-ADC non-linearity in pipeline stages [5] illustrated in Fig. 1a. This was separately discovered for algorithmic ADCs in [16]-[17] and is sometimes referred to as redundant signed digit (RSD) redundancy. The implementation of this redundancy conceptually consists of taking a given full-bit sub-ADC stage and replacing each given comparator level with two new comparison levels that closely surround the old comparison level. Ideally, these comparison levels should be located within 0 and VLSB/2 of the original threshold, when referenced to the sub-ADC resolution. By doing this, the ideal residue of each stage is now half of what it previously was and over-range errors between $\pm V_{FS}$ and $\pm 3V_{FS}/2$ of each stage are shifted back into the full-scale residue range after each cycle. Alternatively, half-bit redundancy can be understood as a shifting of the sub-ADC stage comparison thresholds, that is one bit higher resolution than is needed, by VLSB/2 and removing the top level [7]. The requirement that the sub-ADC levels now be accurate to within VLSB/2 ($V_{FS}/4$ for a 1.5b/stage ADC) of the current stage is a stark improvement to the traditional full-bit ADC structure which needs comparison levels that are accurate to within VLSB/2 of the entire ADC. For maximum offset tolerance of sub-ADC comparator offsets, the redundant comparison thresholds are often nominally placed at ±VLSB/4 (of the current stage) away from the full-bit comparison thresholds.

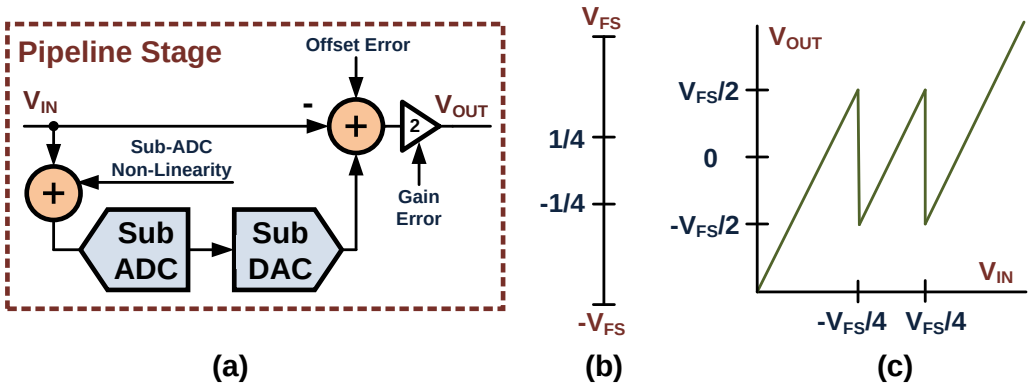

Figure 4.71: Pipeline ADC a) Stage architecture, b) Sub-ADC 1.5b levels, and c) Reside plot

Since these redundant sub-ADCs are not an integer number of bits, but can be added with 2 binary digits (three levels), they are often referred to as M.5 b/stage ADCs (1.5, 2.5, 3.5 etc.). Every M.5 b/stage redundant ADC contains (2(M+1) – 1) levels and (2(M+1) – 2) comparison thresholds. As an example, a 1b stage in a pipeline, algorithmic, or SAR ADC can be transformed to a 1.5b stage by replacing the comparator at {0} with comparator at {-VFS/4 and VFS/4}, assuming a stage full-scale range of ±VFS as shown for a pipeline in Fig. 1b. The input/output plot of the residue (also called Robertson plot) of a 1.5b pipeline ADC stage is shown in Fig. 1c.

4.1.2 CRZ Redundancy

In half-bit redundancy, the additional comparison thresholds always surround the location of the integer (or conventional restoring) ADC levels, resulting in $(2^{(M+1)} - 2)$ comparison thresholds. In conventional restoring redundancy with Z added levels (CRZ), fewer levels are used than in the half-bit redundant case, but more than in the integer ADC [18]-[19]. This, like half-bit redundancy, will allow for correction of over-range errors due to sub-ADC offsets and settling errors, but will have a smaller redundancy magnitude than half-bit redundancy. Also, in half-bit redundancy, the digital codes going to the sub-DAC are either integers or half-integers, resulting in low complexity digital recombination of stage digital outputs. However, digital outputs of a CRZ stage are more arbitrary, requiring additional digital processing at the conversion rate. Thus, there is a clear tradeoff with the CRZ scheme between the number of comparators and the loss in redundancy with greater digital complexity. One note is that [19] does achieve reduced digital complexity over [18] by changing the inter-stage gain of a pipeline stage, making the CRZ error correction logic look much more like that of a half-bit ADC. Example low-resolution full bit, half bit, and CRZ redundant stages are displayed in Fig. 2.

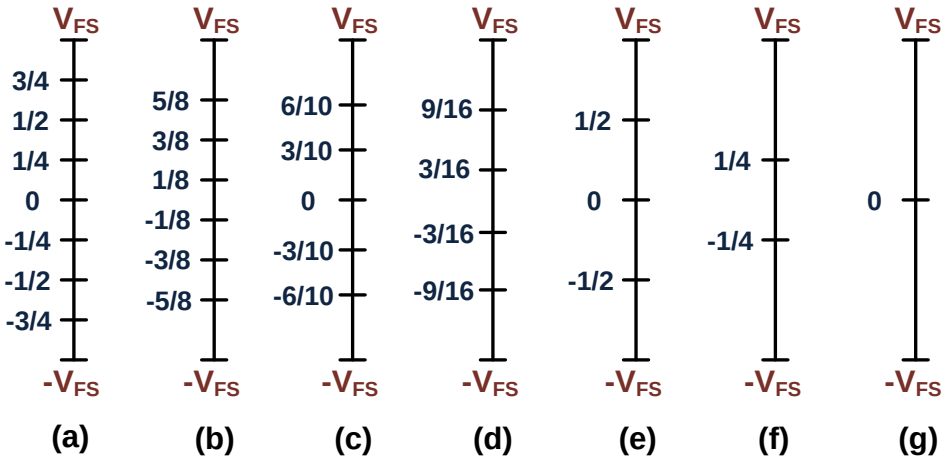

Figure 4.72: Example low-resolution sub-ADC threshold levels (a) 3b, (b) 2.5b, (c) $CRZ_{Z=2}$, (d) $CRZ_{Z=1}$, (e) 2b, (f) 1.5b, (g) 1b

4.1.3 Sub-Radix Redundancy

Sub-radix redundancy predates multi-level [3], [20] and is created not by adding comparison thresholds to a given stage, but rather by reducing the nominal ratio of a given stage full-scale range to that of the previous. As an example, a 1b per stage ADC would typically see the input referred full-scale range of each stage decrease by a factor of 2 with each cycle, effectively range scaling by 2(-ST) where ST is the current stage and 2 is the given radix. In a sub-radix ADC, this radix of 2 would be replaced by something smaller like 1.7. A 1.7 radix makes the full-scale range of every stage slightly larger than the ideal full-scale range of the residue from the previous stage as demonstrated in Fig. 3. This allows over-range errors due to settling or sub-ADC non-linearity to be captured and re-shifted into the valid residue region of future stages.

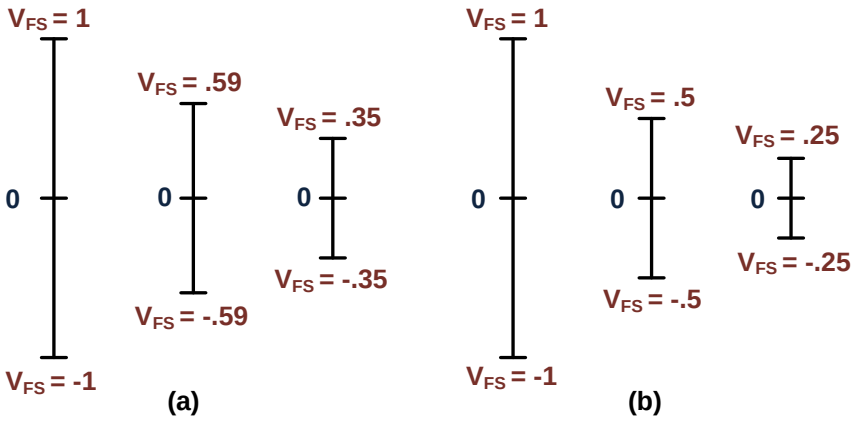

Figure 4.73: 1b SAR stage full-scale ranges for (a) sub-radix of 1.7 and (b) non-redundant binary stages

Choosing the appropriate radix in sub-radix stages is often based on the tradeoff between the error tolerance that comes with a smaller radix and the reduced cycle count of a larger radix. It is also important to note that while this method can allow for a fixed single comparison device (important in SAR ADCs), it has the drawback of increasing DAC complexity due to the non-binary nature of the stage subtraction [2] and/or a large digital engine [1], [21]. Almost always, this method is used in conjunction with DAC calibration.

4.1.4 Extra Stage Redundancy

Adding an extra cycle in a multi-stage ADC with a full-scale range that mirrors the full-scale range of the previous stage is a common redundancy method that allows for over-range errors to be shifted back into the ideal residue region. For a 1b/stage ADC, at the redundant stage, residue larger than the 0 comparator level is subtracted by the V_{FS} of the stage and the residue smaller than 0 has V_{FS} added to it. This effectively swaps the ideal residue output of a stage across the 0 threshold level. Due to this swapping, any over-range error from $\pm V_{FS}$ to $\pm 2V_{FS}$ is now brought into the appropriate residue range ensuring that the final quantization error is now within VLSB/2 of the current stage.

In its simplest form, extra stage redundancy can be implemented by replicating one or more stages in a multi-stage ADC and appropriately adjusting the digital summation block [22],[23]. Recently, more advanced techniques for SAR ADCs have been explored that pre-shift the input signal to allow for digital recombination that looks much like half-bit redundancy [24].

The following sections of this paper will demonstrate that multi-level redundancy not only compensates for over-range errors but also changes the statistics of the residue in each stage such that achieving extra resolution is possible. CRZ, sub-radix and extra cycle redundancy also affects stage residue statistics, but unlike multi-level, they either do not result in inherently improved resolution or give only partial shaping.

4.2 Ideal Residue Shaping

Half-bit redundant multi-stage ADCs have the ability to shape the PDF of the residue at the output of every distinct stage. This will be shown and analyzed first with a basic 1.5b/stage pipeline and will be extended to higher order half-bit redundancies. For a full pipeline to be designed with PDF residue shaping effects, architectural modifications should be made to the back-end ADC and will be described.

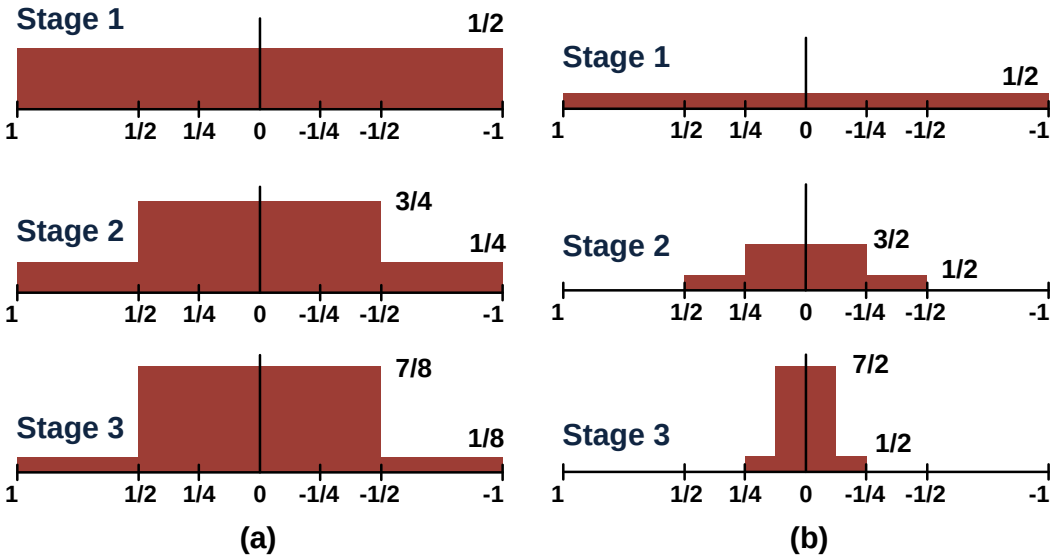

Figure 4.74: Probability distribution function of the residue output of the first three stages for 1.5b/stage redundancy in an (a) pipeline ADC and (b) SAR ADC

4.2.1 Residue Shaping in a 1.5b/stage Pipeline ADC

For a generic 1.5b/stage pipeline ADC, let us assume that the input signal probability is uniformly distributed for simplicity, and comparator thresholds are at their optimal locations of ±VFS/4 in each stage. The pipeline ADC multiplying digital to analog converter (MDAC) will quantize, subtract, and amplify the previous stage residue resulting in the following stage transfer function:

$$V_{OUT,STAGE} = \begin{cases} 2\left(V_{IN} - V_{FS}/2\right) & \text{for} \quad V_{IN} > V_{FS}/4 \\ 2V_{IN} & \text{for} \quad -V_{FS}/4 < V_{IN} < V_{FS}/4 \\ 2\left(V_{IN} + V_{FS}/2\right) & \text{for} \quad V_{IN} < -V_{FS}/4 \end{cases} \tag{1.39}$$

Where the full-scale range of the sub-ADC is ±VFS.

After each stage, the residue of the codes that were within ±VFS/4 will remain in the center half of the next stage full-scale range since there was no subtraction performed. Codes above and below this central region experience a subtraction of ±VFS/2, which shifts them towards the center of the next stage full-scale range. The result is that after each stage, the PDF of the residue becomes more concentrated in the center half of the stage full-scale range. This

phenomena is what we call PDF residue shaping and is illustrated in Fig. 4. It is important to note that a traditional 1b/stage pipeline with a uniform input distribution will ideally maintain that uniform distribution at the input of each stage. The expansion of (4.1) can then be used to derive the magnitude of the residue PDF change per stage:

$$\Delta H_{PDF,STAGE} = \begin{cases} -\dfrac{H_{PDF,ST-1}}{2} & \text{for} \quad V_{IN} > V_{FS}/4 \\ \dfrac{1-H_{PDF,ST-1}}{2} & \text{for} \quad -V_{FS}/4 < V_{IN} < V_{FS}/4 \\ -\dfrac{H_{PDF,ST-1}}{2} & \text{for} \quad V_{IN} < -V_{FS}/4 \end{cases} \tag{1.40}$$

Where ST is the stage being analyzed and H is the magnitude of the PDF. The resulting integrated PDF of the residue after each MDAC stage can then be given by:

$$PDF(\text{Stage}) = \begin{cases} \dfrac{1}{2^{ST+1}} & \text{for} \quad V > V_{FS}/2 \\ 1-\dfrac{1}{2^{ST}} & \text{for} \quad -V_{FS}/2 < V < V_{FS}/2 \\ \dfrac{1}{2^{ST+1}} & \text{for} \quad V < -V_{FS}/2 \end{cases} \tag{1.41}$$

From Fig. 4 and (4.3), one can see that with the PDF residue shaping trend continuing for many stages, the residue in the final stage of a pipeline ADC will be squeezed into nearly ½ the full-scale range of that stage as shown in Fig. 5. By discarding the codes outside the center region, almost 6dB of extra resolution can be gained due to the minimization of the quantization error. A similar result was briefly mentioned in [25] in the context of pipeline residual distribution propagation analysis. The exact resolution increase can be determined by calculating the final number of codes shifted into the center half of the full-scale range and number of total pipeline stages.

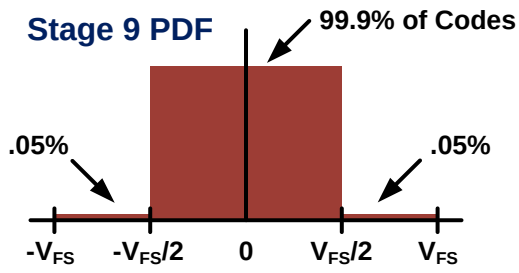

Figure 4.75: Probability distribution function of the residue output of the 9th stage in a pipeline ADC

From (4.3), assuming the total number of bits in the pipeline should ideally equal the number of 1.5b stages plus 1, then the total number of levels in the center half of the last MDAC output is given by the following:

$$\mathrm{Nlev} = \left(1 - \frac{1}{2^{\mathrm{ST}}}\right) 2^{\mathrm{ST}+1} = 2^{\mathrm{ST}+1} - 2 \tag{1.42}$$

This equation shows that there are always two effective levels missing from the center half of the final MDAC output. By tracing the shaping pattern of (4.1) across many stages, these two discarded levels are shown to be the top and bottom levels in the initial input and discarding them is synonymous to reducing the dynamic range of the pipeline input. This also means that PDF residue shaping occurs regardless of the input distribution, such as sine or gaussian. The impact on the signal to quantization noise ratio (SQNR) of the ADC from this discarding can be calculated by first defining SQNR based on the number of quantization levels in an ADC. From [26], for a uniform quantization error:

$$\mathrm{SQNR} = 20\log_{10}\left(\frac{\mathrm{V_{FS}}}{2\sqrt{2}} \cdot \frac{\sqrt{12}\left(\mathrm{NLev}\right)}{\mathrm{V_{FS}}}\right) = 20\log_{10}\left(\mathrm{NLev}\right) + 1.76 \tag{1.43}$$

By inserting (4.4) into (4.5), the total SQNR due to ideal residue shaping is given as:

$$\mathrm{SQNR}_{\mathrm{ResidueShaped}} = 20\log_{10}\left(2^{\mathrm{ST}+1} - 2\right) + 1.76 \tag{1.44}$$

The improvement over a typical pipeline configuration where residue shaping is not considered is then given by:

$$\begin{aligned} \Delta\mathrm{SQNR}_{\mathrm{R-Shaped}} &= \mathrm{SQNR}_{\mathrm{R-Shaped}} - \mathrm{SQNR}_{\mathrm{Traditional}} \\ &= 20\log_{10}\left(2^{\mathrm{ST}+1} - 2\right) - 20\log_{10}\left(2^{\mathrm{ST}}\right) \\ &= 20\log_{10}\left[2\left(1 - 2^{-\mathrm{ST}}\right)\right] \end{aligned} \tag{1.45}$$

From (4.7) one can see that given a reasonable number of pipeline 1.5b pipeline stages, the change in resolution is very close to 6dB and can be treated as an extra bit of resolution in most quantization noise limited applications. This same analysis and resolution result is also directly applicable to SAR ADCs with 1.5b/stage redundancy.

4.2.2 Higher Order Half-Bit Redundant Residue Shaping

Half-bit redundancy structures higher than 1.5b/stage will also shape the input residue across the stages of the pipeline resulting in an extra bit of resolution. For a 2.5b/stage pipeline, the MDAC transfer function of (4.1) can be modified as follows:

$$V_{OUT,STAGE} = \begin{cases} 4\left(V_{IN} - 3V_{FS}/4\right) & \text{for} \quad V_{IN} > 5V_{FS}/8 \\ 4\left(V_{IN} - 2V_{FS}/4\right) & \text{for} \quad 3V_{FS}/8 < V_{IN} < 5V_{FS}/8 \\ 4\left(V_{IN} - V_{FS}/4\right) & \text{for} \quad V_{FS}/8 < V_{IN} < 3V_{FS}/8 \\ 4V_{IN} & \text{for} \quad -V_{FS}/8 < V_{IN} < V_{FS}/8 \\ 4\left(V_{IN} + V_{FS}/4\right) & \text{for} \quad -3V_{FS}/8 < V_{IN} < -V_{FS}/8 \\ 4\left(V_{IN} + 2V_{FS}/4\right) & \text{for} \quad -5V_{FS}/8 < V_{IN} < -3V_{FS}/8 \\ 4\left(V_{IN} + 3V_{FS}/4\right) & \text{for} \quad V_{IN} < -5V_{FS}/8 \end{cases} \tag{1.46}$$

This results in an integrated residue PDF after each MDAC stage of:

$$\mathrm{PDF}(\mathrm{Stage}) = \begin{cases} \dfrac{1}{2^{2(ST)+1}} & \text{for} \quad V > V_{FS}/2 \\ 1 - \dfrac{1}{2^{2(ST)}} & \text{for} \quad -V_{FS}/2 < V < V_{FS}/2 \\ \dfrac{1}{2^{2(ST)+1}} & \text{for} \quad V < -V_{FS}/2 \end{cases} \tag{1.47}$$

Generalizing this result to all multi-level stages we get:

$$\mathrm{PDF}(\mathrm{Stage}) = \begin{cases} \dfrac{1}{2^{M(ST)+1}} & \text{for} \quad V > V_{FS}/2 \\ 1 - \dfrac{1}{2^{M(ST)}} & \text{for} \quad -V_{FS}/2 < V < V_{FS}/2 \\ \dfrac{1}{2^{M(ST)+1}} & \text{for} \quad V < -V_{FS}/2 \end{cases} \tag{1.48}$$

Where M is the number of full bits resolved from a given sub-ADC stage (i.e. M = 2 for a 2.5b stage). From (4.10) the number of levels within the center half of the final MDAC stage can then be shown to be:

$$\mathrm{Nlev} = \left(1 - \frac{1}{2^{\mathrm{M(ST)}}}\right) 2^{\mathrm{M(ST)}+1} = 2^{\mathrm{M(ST)}+1} - 2 \tag{1.49}$$

This shows that for an M.5b/stage ADC, residue shaping will still allow for all but 2 of the levels to be shaped into the center half of the final MDAC stage. By following the derivation of (4.5)-(4.7), the total generalized half-bit SQNR improvement is given by:

$$\Delta\mathrm{SQNR}_{\mathrm{R-Shaped}} = 20\log_{10}\left[2\left(1 - 2^{-\mathrm{M(ST)}}\right)\right] \tag{1.50}$$

Thus, while the higher number of comparison levels per stage presents a tradeoff between sub-ADC power and the number of overall pipeline stages, it does not affect the resolution improvements due to PDF residue shaping.

4.2.3 Ideal Back-End ADC Design

Typically, the final stage of a multi-stage ADC is a basic flash converter since there is no further subtraction or residue amplification after the final quantization stage. While exotic back-end ADCs exist [27], Fig. 6 shows some traditional 2b back-end flash stages that would be suitable for a pipeline or algorithmic structure. Since residue shaping has reduced the effective quantization error by a factor of 2, these 2b back end stages will only provide 1 bit of extra resolution. As an example, a 9-stage pipeline with a 2b traditional back-end flash ADC can have 11 total bits of resolution. However, by reducing the comparator threshold levels and back-end digital gain (radix value) by a factor of 2 (Fig. 6c), the full-scale range of the back-end flash matches that of the output reside and a full 2 bits of resolution can be gained. Thus, a 9-stage pipeline ADC with scaled 2b back-end can achieve 12 total bits of resolution.

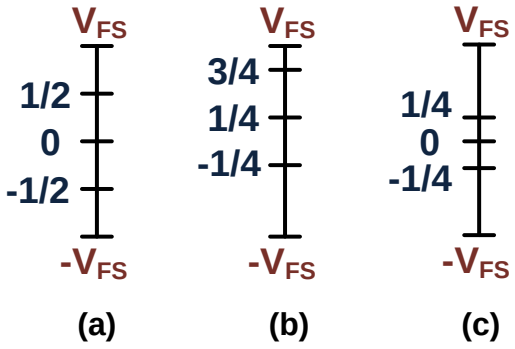

Figure 4.76: 2b back-end flash stages for a (a) traditional symmetrical back-end stage, (b) shifted back-end stage, and (c) compressed symmetrical back-end

The choice of optimal backend stage thresholds is illustrated in Fig. 7. Here the symmetrical threshold levels are swept from 0 to ±VFS with digital gains of 1 (traditional) and ½. One can see that due to PDF residue shaping, the 2b back-end ADC achieves an optimal resolution with comparison thresholds at ±VFS/4 and a back-end gain of 1/2x. Also, the achievable resolution flattens when the output comparison levels extend beyond ±VFS/2 since the residue is only located in the center half of the last stage full scale range and thresholds beyond this region do not provide any accuracy benefit. Finally, Fig. 7 illustrates that scaling the comparison thresholds to ±VFS/4 but not scaling the digital gain will result in a loss of 6dB due to the misalignment of the back-end ADC levels and corresponding digital codes.

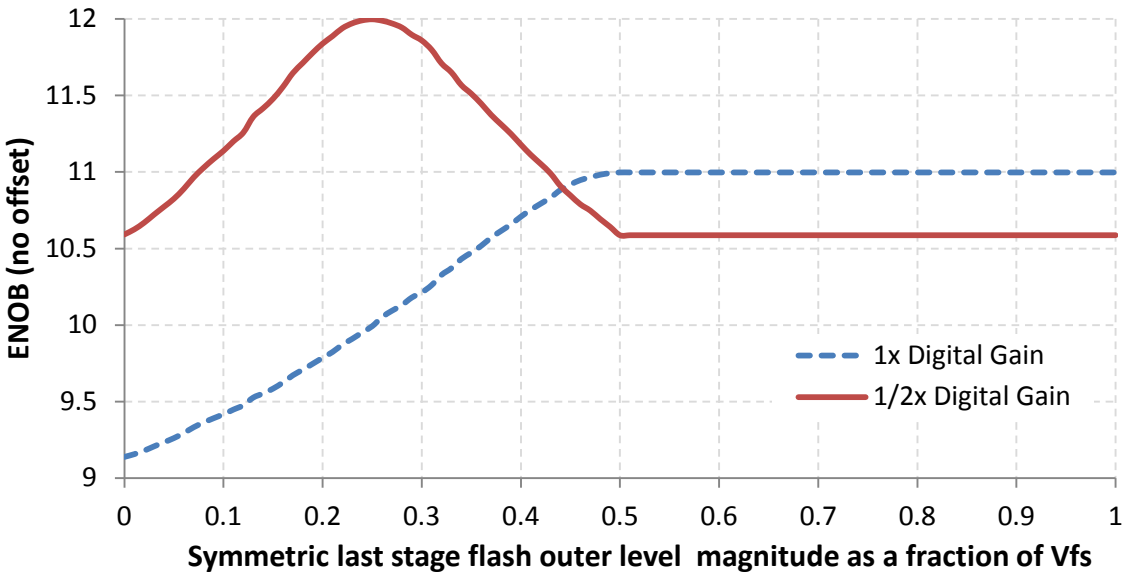

Figure 4.77: 9 x 1.5b/stage pipeline ADC with 2b back-end stage symmetric outer levels swept from 0 to ±VFS and digital gains of 1 and ½.

It should be noted that using this scaled back-end in a pipeline ADC will also reduce the number of unique reference levels that must be generated since {-VFS/4, 0, VFS/4} are all used in either the sub-ADCs or MDAC subtraction. Furthermore, the number of bits in the back-end ADC will not affect the overall resolution improvement from PDF residue shaping since (4.4) will turn into:

$$\mathrm{Nlev} = \left(2^{\mathrm{ST}+1} - 2\right)2^{\mathrm{F}} \tag{1.51}$$

Where F is the number of flash ADC bits. This equation yields the same SQNR improvement as (4.12) including the impact of the 2 lost levels in (4.11).

4.2.4 Shifted Back-End ADCs

Traditionally, the ADC of Fig. 6a has been used as a back-end 2b flash stage for a 1.5b/stage pipeline ADC, and it has been shown that Fig. 6c would be a more optimal choice. However the back-end of figure 6b has also been popular in literature [5],[28] due to the use of similar reference levels to the other sub-ADC stages and the assumption that if codes are shifted, then 3 levels are needed in the last stage to absorb the shifted residue range. This ADC is used to achieve the traditional 2b of extra resolution, however if one falsely assumes that the residue in the last stage is uniformly distributed between ±V_{FS}, then this 2b of resolution is clearly not achievable due to the large quantization error on one end of the residue curve. The actual reason this back-end stage give 2 bits is also not due to a shifting of the last stage residue, but is because of the residue shaping effects previously described. Because of PDF residue shaping, the full-scale range of the residue is captured between the bottom two reference levels (±V_{FS}/4) of Fig. 6b, and this gives two bits due to the digital coding. The top comparison level (3/4V_{FS}) ideally does not affect the resolution with the exception of adding one extra code to the full-scale range. This is demonstrated in Fig. 8 where only 2 thresholds (3 levels) are swept from 0 to ±V_{FS} with digital output codes of 00, 01, and 10 at a gain of 1. The plot shows that even with the top level removed, two levels equally spaced at ±V_{FS}/4, with nominal digital code gain, will produce 2 bits similar to the back-end ADCs of Fig. 6a and 6b.

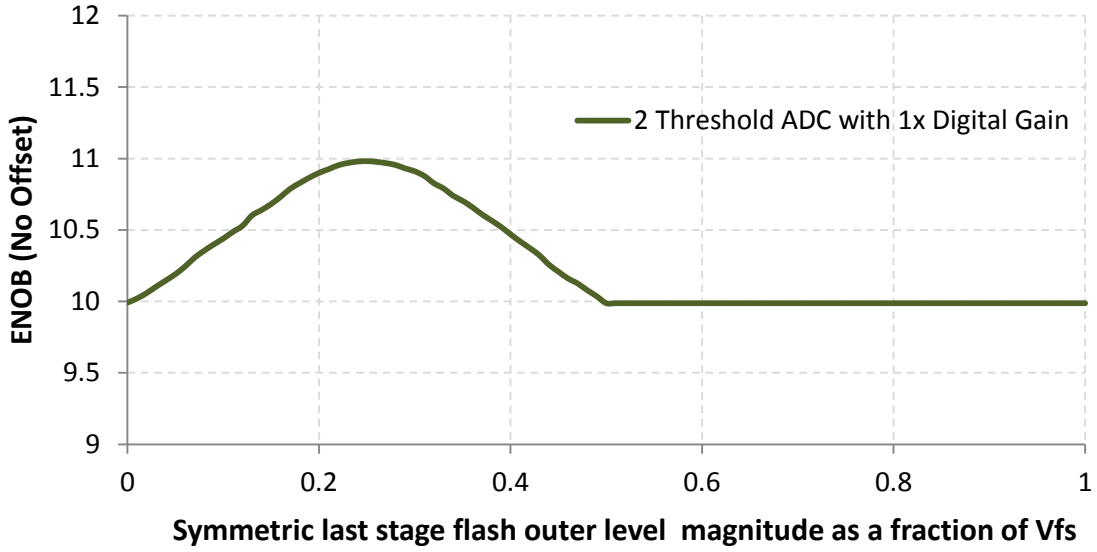

Figure 4.78: 9 x 1.5b/stage pipeline ADC with 3-level (2 threshold) back-end stage symmetric levels swept from 0 to ±V_{FS} and digital gain of 1

4.2.5 Extra Cycle, Sub-Radix, and CRZ Stage Shaping

While multi-level techniques are not the only way to implement redundancy to prevent settling and sub-ADC non-linearity errors, it is the only variety that residue shapes to give a full bit of extra resolution. This is due to the fact that some residue is held without subtraction for the following stage, resulting in a residue transfer curve that grows in the center in each successive stage.

In extra cycle redundancy, an integer bit per stage operation is performed for numerous cycles followed by a redundant stage that mirrors the previous in terms of subtraction and/or inter-stage gain. Fig. 9 illustrates that because of the integer stage quantization, no stage residue shaping occurs. Furthermore, in the redundant cycle, the positive and negative PDF regions simply swap locations across the center comparison threshold. While allowing for the correction of over-range signals, this swapping behavior does not result in increased inherent resolution. Additionally, even though the summation technique of [24] looks similar to that of half-bit redundancy, the single bit per cycle operation is still used, thus does not allow for shaping to occur.

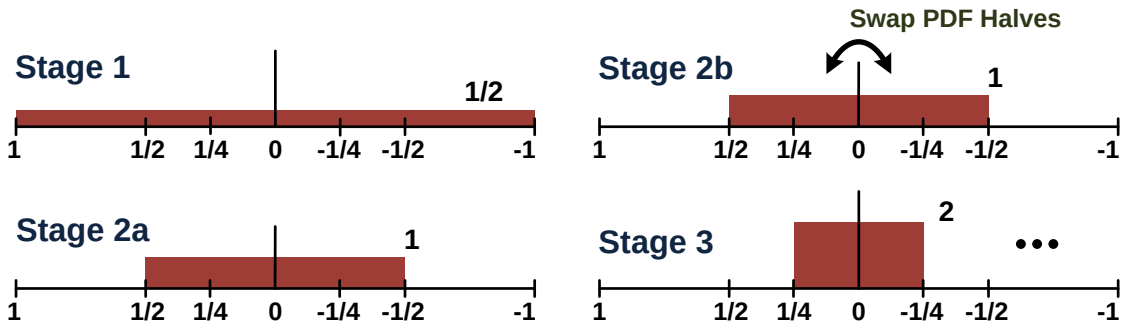

Figure 4.79: Extra cycle redundancy stage PDF shaping diagram for a SAR ADC showing no PDF residue shaping in the redundant stage

In sub-radix redundancy, an integer bit per stage operation is again performed, but with the full-scale range of each successive stage being larger than the full-scale range of the residue in the previous stage. Fig. 10 demonstrates that while this initially makes the residue look like it is being shaped, the integer quantization per stage makes codes near a comparison threshold always be pushed to the outside of the permissible residue range after a few stages, where this number of stages is related to the chosen radix. While sub-radix redundancy will cause unusual

inter-stage PDF residue transfer curves, it also does not provide the opportunity for additional resolution.

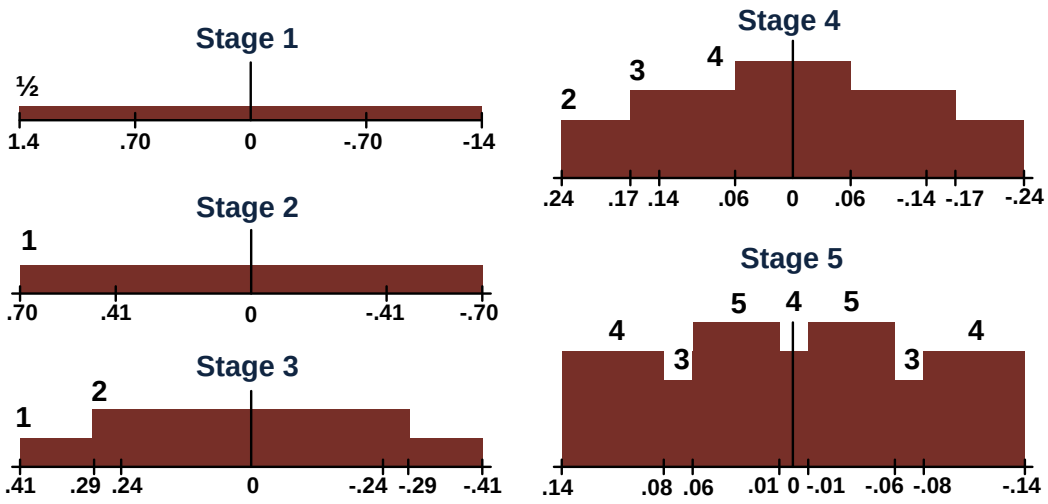

Figure 4.80: Sub-radix redundancy stage PDF shaping diagram showing no PDF residue shaping for a SAR ADC with radix of 1.7

CRZ redundancy will shape the residue across many stages. However, the ideal output residue range of each stage is more than $\pm V_{FS}/2$ because the spacing of the fewer comparison thresholds are larger. This means that the final shaped output will be between half the full-scale range and the full-scale range. This will result in a small amount of resolution improvement if the correctly scaled back-end ADC is chosen and digital codes are scaled, but not a full bit. Redesigning a given CRZ redundant ADC for full residue shaping will be described later in the chapter.

4.3 Residue Shaping Response to Non-Idealities

Reside shaping has been shown to give a 6dB resolution improvement for multi-stage ADCs with multi-level redundancy when the comparison position is set at the optimal threshold. However, physically, perfect thresholds are not possible due to inherent offsets resulting from device sizing and power consumption limits [29]. Furthermore, the variability of sub-ADC comparison levels and settling non-idealities is the main reason for using redundancy in the first place.

4.3.1 Analysis of Offsets in Residue Shaping

Offsets or settling errors in multi-level redundant ADC stages will affect the residue shaping differently in each stage and under specific conditions. These effects can be understood by analyzing the result of a sub-ADC threshold offset on the overall PDF residue shaping in a 1.5b/stage SAR ADC. A SAR is chosen as an example due to the simplicity of examining subtraction across many stages. With an offset, the residue operation of (4.1) changes to:

$$V_{OUT,STAGE} = \begin{cases} \left(V_{IN} - V_{FS}/2\right) & \text{for} \quad V_{IN} > V_{FS}/4 + \Delta \\ V_{IN} & \text{for} \quad -V_{FS}/4 < V_{IN} < V_{FS}/4 + \Delta \\ \left(V_{IN} + V_{FS}/2\right) & \text{for} \quad V_{IN} < -V_{FS}/4 \end{cases} \tag{1.52}$$

Where in the SAR case, V_{FS} corresponds to a given stage full-scale range, which in a binary weighted SAR will decrease by a factor of two in each cycle.

A stage with comparator offsets will move some residue close to the ideal $\pm V_{FS}/4$ thresholds to outside the center half of the next stage full-scale range ($\pm V_{FS}/2$ of [stage + 1]) before being quantized by that next stage. If this offset is small, the next SAR stages will re-shift the error back into the center half of the following full-scale ranges. However if the offset is so large that it cannot be shifted back into the center half of the final full-scale range ($\pm V_{FS}/2$ of the final stage), then the PDF of the final stage output will show quantization leakage beyond $\pm V_{FS}/2$, degrading the resolution improvement.

In the cases where quantization leakage occurs due to large random comparator offsets, the error does not cause distortion but rather raises the SQNR noise floor since the error mostly is uncorrelated with the input and the stage input becomes increasingly white with each progressing stage [25]. This is graphically shown in Fig. 11 where the FFT of a 12b quantization limited, PDF residue shaped ADC noise floor rises with increasing comparator offset. Additionally, since excessive comparator offset creates a slightly larger than normal code bin followed by a slightly smaller one, this comparator offset will show up as periodic DNL as plotted in Fig. 12. The DNL periodicity and the fact that this offset will occur mostly for latter stages, means that the INL does not show any global curvature.

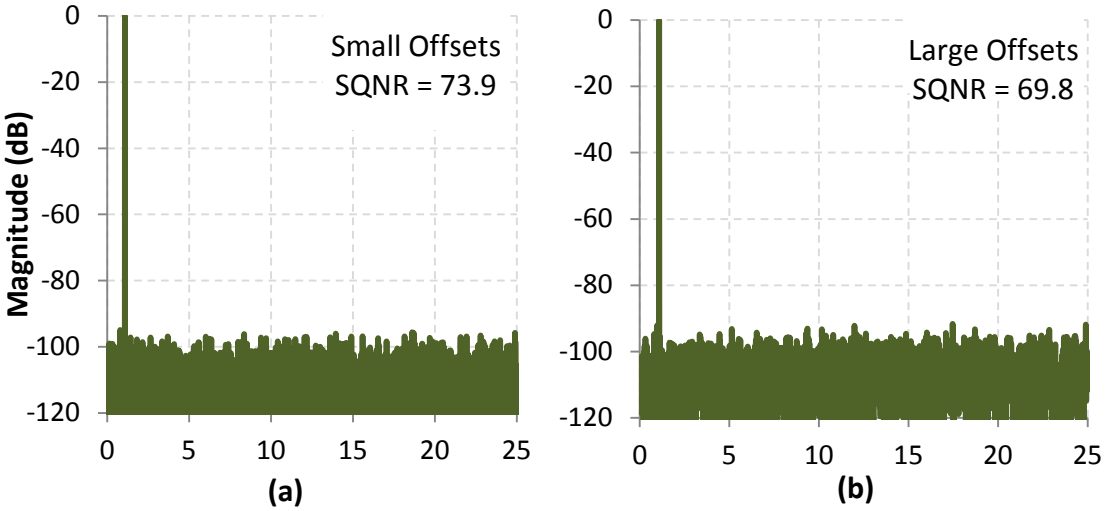

Figure 4.81: FFT plots of a 12b quantization limited, PDF residue shaped 1.5b/stage pipeline ADC with normally distributed sub-ADC offsets of (a) 0.024*VFS and (b) 0.24*VFS.

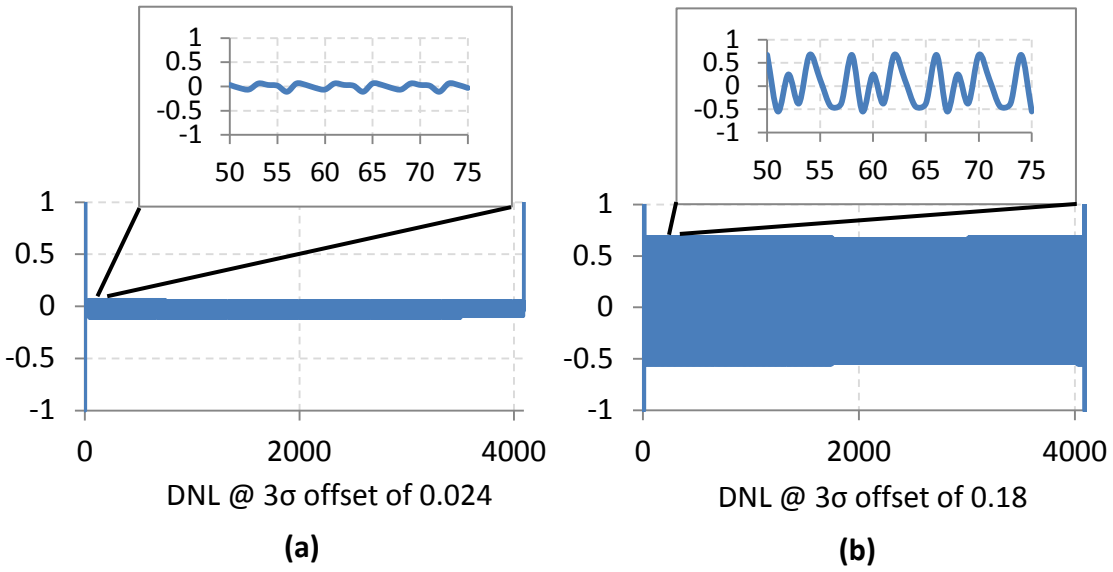

Figure 4.82: DNL plots of a 12b PDF residue shaped pipeline ADC showing periodic DNL curves for a normal distributed offset of (a) 0.024*VFS and (b) 0.18*VFS.

Since redundancy helps to fix small comparator offsets before they cause quantization leakage, it is possible to derive bounds for the comparator offset in each stage showing the tolerable offset that will cause no SQNR degradation. The allowable comparator offset for optimal residue shaping is equal to the maximum subtraction available from the stages following the offset stage that can bring an offset code that is outside the current stage

redundant center half, back into the center half of the last stage full-scale range. Continuing with the 1.5b/stage SAR, the total DAC subtraction from a given stage that is available, assuming a normalized input full-scale range of 1, is:

$$\mathrm{DACSubtraction}_{\mathrm{Total}} = \sum_{k=ST-1}^{N-1}\left(\frac{1}{2^{k}}\right) = \frac{1}{2^{ST}} - \frac{1}{2^{N-1}} \tag{1.53}$$

Where N is the total SAR resolution in bits including residue shaping with no back-end flash. Any codes outside of the region where the following stage subtraction cannot pull that code into $\pm V_{FS}/2$ of the last stage residue output, will then cause quantization leakage. This results in the following tolerable offset regions for error-free residue shaping in the 1.5b/stage SAR with an input full-scale range of ±1:

$$\mathrm{R\ Bounds}_{\mathrm{SAR}} = \begin{cases} \mathrm{Upper\ Bound} = \dfrac{1}{2^{ST}} - \dfrac{1}{2^{N}} \\ \mathrm{Lower\ Bound} = \dfrac{1}{2^{N}} \end{cases} \tag{1.54}$$

It is important to note that the ideal comparator threshold is ¼ of the full-scale stage voltage or $(1/2^{ST+1})$. The bounds in the above equation do not represent offset deviations (as zero offset from the ideal threshold would be perfect) but rather the minimum and maximum absolute threshold locations to prevent resolution degradation.

Conceptually, the result of (16) can be understood by noting that the full-scale range of a SAR stage is in this case $(1/2^{ST+1})$. Thus $(1/2^{ST})$-$(1/2^{N-1})$ is the maximum amount of subtraction available if the current stage code is in the redundant zone. However, since the final full-scale residue range after the last SAR stage is $(1/2^{N-1})$ and the final residue should be bounded between $\pm(1/2^{N})$ for residue shaping, a code exactly at the stage comparison threshold of $(1/2^{ST})$ will not fall into the bounded region due to the max allowable subtraction. Thus the maximum redundancy is bounded to $(1/2^{ST})$-$(1/2^{N})$ and $(1/2^{N})$ as opposed to the traditional boundings of $(1/2^{ST})$ and 0 to prevent residue shaped quantization leakage errors. Note that in the SAR ADC, the last stage bounds show that comparator offsets in the final stages will slightly degrade the overall 6dB resolution improvement from residue shaping, but will not cause the loss of overall net SQNR improvement.

The result of (4.16) is again similar in the 1.5b/stage pipeline or algorithmic ADC with the addition of inter-stage gain:

$$\text{R Bounds}_{\text{Pipe}} = \begin{cases} \text{Upper Bound} = \dfrac{V_{FS}}{2} - \dfrac{V_{FS}}{2^{N-ST+1}} \\ \text{Lower Bound} = \dfrac{V_{FS}}{2^{N-ST+1}} \end{cases} \tag{1.55}$$

Where N is again the total pipeline resolution in bits including the bit from residue shaping. This result is similar, but slightly more stringent than the traditional pipeline comparison threshold over-range criteria of ($V_{FS}/2$) and 0.

These pipeline and SAR 1.5b/stage results are shown graphically in Fig. 13. Similar analysis performed for higher order multi-level redundancy yields the following bounds for M.5 bit pipeline ADCs:

$$\text{R Bounds}_{\text{Pipe\_Mulit-bit}} = \begin{cases} \text{Upper Bound} = \dfrac{V_{FS}}{2^{M}} - \dfrac{V_{FS}}{2^{N-M(ST)+1}} \\ \text{Lower Bound} = \dfrac{V_{FS}}{2^{N-M(ST)+1}} \end{cases} \tag{1.56}$$

These bounds are defined as the maximum and minimum allowable spacing of the two M.5b redundant thresholds surrounding an M-bit sub-ADC comparison threshold for ideal residue shaping.

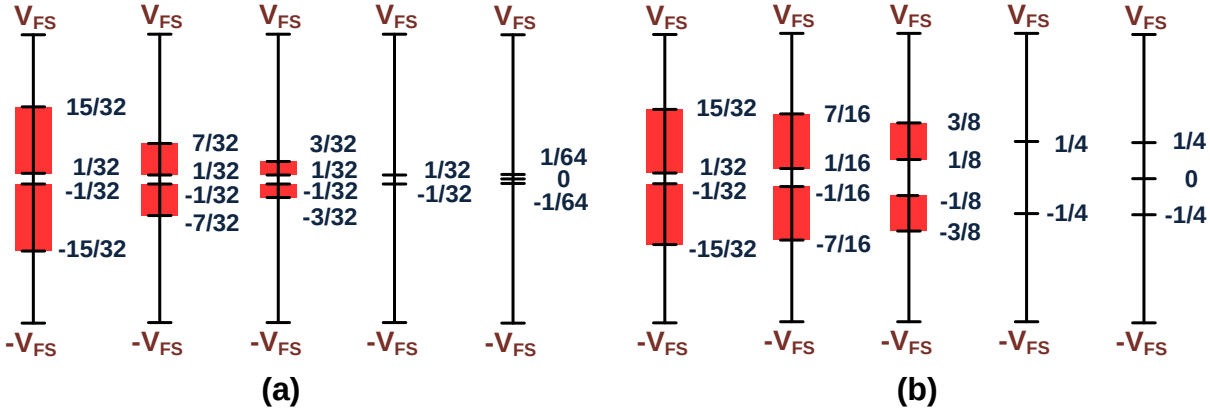

Figure 4.83: Threshold offset range to maintain ideal residue shaping in (a) a 4 x 1.5b/stage SAR ADC and (b) a 4 x 1.5b/stage Pipeline or Algorithmic ADC

4.3.2 ADC Design for Optimized PDF Residue Shaping

Comparing the allowable offset range in a traditional structure to that of the residue shaped structure, one can see that the early and back-end stages are nearly identical in terms of allowable offset or redundancy magnitude. In the PDF residue shaped structure, only the last

couple of stages before the back-end ADC have offset bound requirements that are noticeably stricter than in the traditional ADC. However, this typically does not greatly degrade the 6dB SQNR improvement since large redundancy is still available in the early stages for SAR settling error reduction and the SQNR degradation from to quantization leakage due to comparator thresholds exceeding offset bounds in pipeline ADCs is reduced in the latter stages due to the prior inter-stage gain. Also if slightly greater effort is placed on reducing the offsets in only the last couple stages of a multi-stage ADC, there can be large gains in offset tolerance.

Fig. 14 illustrates the 100 run average final resolution vs. normally distributed comparator offsets for a 9-stage pipeline ADC with 2b back-end flash for a sinusoidal input. The traditional 2b flash of Fig. 6a is compared with the proposed scaled 2b flash of Fig. 6c. Since the scaled flash full scale range matches the actual full-scale range of the ideal quantization error, the extra bit of resolution described in (4.7) is achieved. The scaled version however does lose resolution, as the nominal comparator offset is increased, at a slightly faster rate than the traditional structure due to the large offsets exceeding the redundancy bounds placed on MDAC sub-ADC stages in (4.17) causing quantization leakage. However, even with this degradation, the resolution is still better for all offset conditions before the maximum 3-sigma offset of $\pm V_{FS}/4$ is reached and for a typical design where the 6-sigma offset is $0.25*V_{FS}$ there is still greater than 4dB of average resolution gain. Also shown in Fig. 14 is a 9-stage ADC with scaled back-end ADC that has an ideal 9th stage sub-ADC. By making the last shaping stage offsets smaller through slight comparator size increases, there can be significant resolution improvements in the presence of large variation over just scaling the back-end. Finally, a 9-stage pipeline with the bounded comparison offset threshold limits of (4.17) and Fig. 13 are shown. This results in a nearly ideal 1b of resolution improvement until over-range errors degrade the performance near offset levels of $V_{FS}/4$.

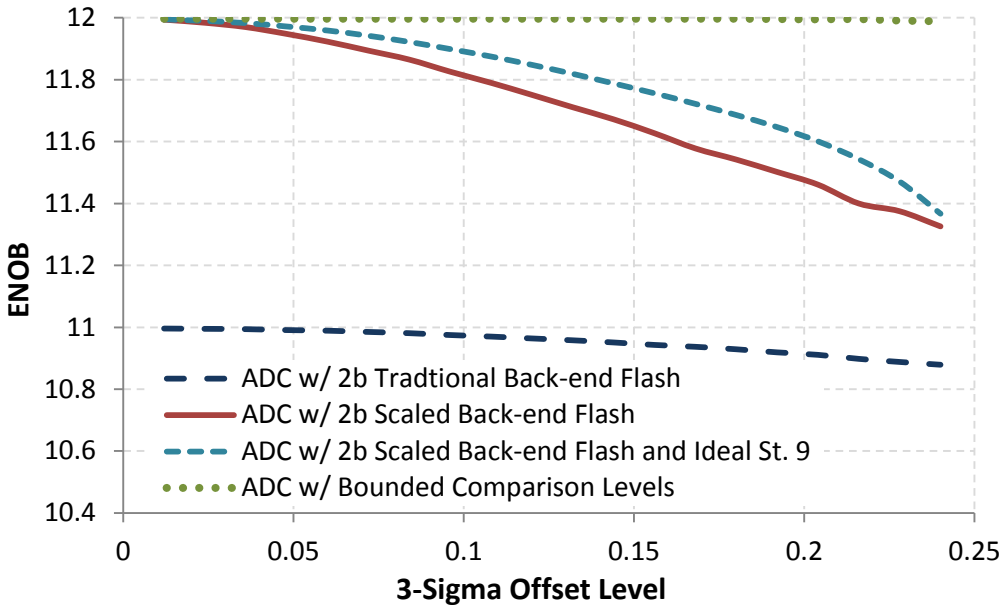

Figure 4.84: 9-stage ADC resolution comparison with a traditional symmetric back-end, proposed scaled back-end, ideal back-end, and bounded comparison levels

In order to understand the spread of the resolution at large comparator offsets, Fig. 15 shows a histogram of the 9-stage ADC ENOB values for the traditional symmetric, proposed symmetric, and proposed bounded back-end structures. Here we can see that for normally distributed offsets, the final ENOB spread of the PDF residue shaped ADC is only slightly larger than that of the traditional structure, which is important for ADC yield analysis.

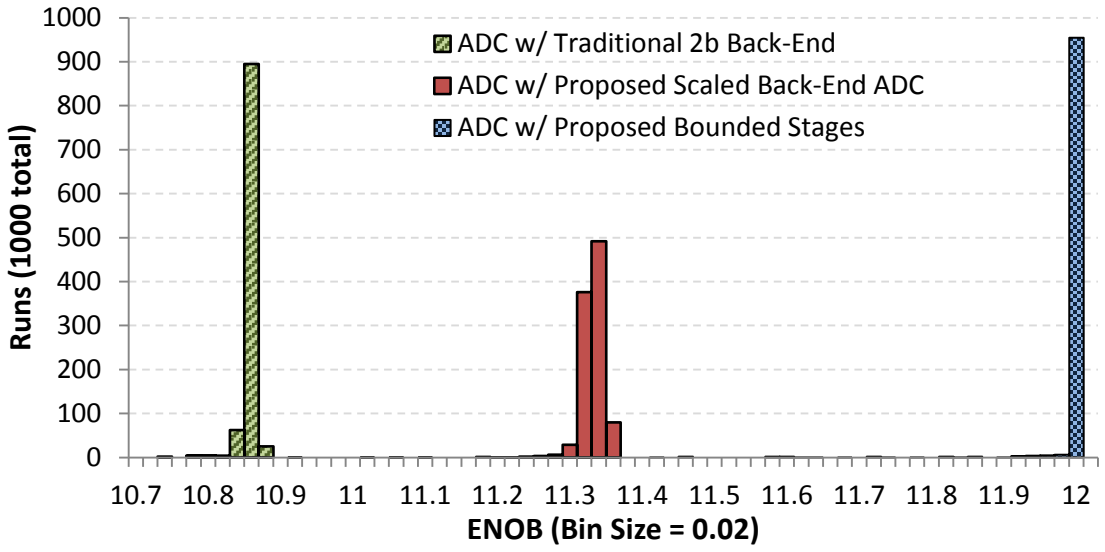

Figure 4.85: Histogram showing the ENOB distribution of 1000 runs of 9-stage pipeline ADCs with and without residue shaping, all at a 3-sigma offset level of 0.2.

When designing a multi-stage ADC it has been shown above that residue shaping can give extra resolution in a quantization noise limited system with very simple changes to the back-end ADC and digital error correction logic. In thermal noise limited designs, extra resolution may not be possible, however a pipeline stage or SAR cycle can be eliminated and the corresponding quantization made up from the PDF residue shaping property. In a pipeline this results in somewhat lowered power consumption, reduced area, reduced operational amplifier count, and lower latency. In the SAR ADC, residue shaping can eliminate an operation cycle saving both switching power, conversion delay, and comparison power. Also, the SAR DAC needs one less value in conventional binary-weighted capacitor arrays reducing cap spread and, in mismatch limited cases, reducing total cap area and power.

4.3.3 Modification to CRZ ADCs for PDF Residue Shaping

CRZ ADCs will ideally reduce the maximum magnitude of the center residue after each stage. The ideal bound of the residue within the outer thresholds after each CRZ stage can be given by the following from [18]:

$$\text{R Bound}_{\text{CRZ}} = \frac{2^{\text{M}} - 1}{2^{\text{M}} - 1 + \text{Z}} \tag{1.57}$$

Where Z is the number of additional threshold levels added from a typical M-bit stage. It is clear that this architecture will only give partial residue shaping due to the increased threshold

level sizes. However, from (4.17) it has been shown that only the final stage in a multi-stage pipeline needs to have the full and ideal half-bit redundancy to achieve 6dB residue shaping. Thus the increased residue magnitude of the CRZ stages can be acceptable in earlier stages of the pipeline if the reduced comparator non-linearity tolerance described in [18] is acceptable. Using the generalized redundancy bounds of (4.18) and the maximum residue for a CRZ converter (4.19), the following shows conditions for full-bit residue shaping with a full-scale range of 1:

$$\mathrm{R\,Bound}_{\mathrm{CRZ}} < \mathrm{R\,Bound}_{\mathrm{Pipe\_Multi-bit\_Output}}$$

$$\frac{2^{\mathrm{M}}-1}{2^{\mathrm{M}}-1+\mathrm{Z}} < 2^{\mathrm{M}}\left(\frac{1}{2^{\mathrm{M}}}-\frac{1}{2^{\mathrm{N-M(ST)+1}}}\right) \tag{1.58}$$

The required Z additional levels for a given Sub-ADC stage to achieve ideal residue shaping (assuming no comparator non-linearity) is then given as:

$$\begin{aligned} \mathrm{Z} &> \frac{2^{\mathrm{M}}-1}{2^{\mathrm{M}}\left(\frac{1}{2^{\mathrm{M}}}-\frac{1}{2^{\mathrm{N-M(ST)+1}}}\right)}-2^{\mathrm{M}}+1 \\ &> \frac{2^{\mathrm{M}}-1}{2^{-\mathrm{M(ST+1)+N+1}}-1} \end{aligned} \tag{1.59}$$

Fig. 16 shows an example 4 stage CRZ pipeline with 2b back-end sized from (4.20). The scaled pipeline consists of 2x 5-level CRZ stages followed by a 6-level CRZ stage for slightly increased stage redundancy, an ideal 2.5b stage and an ideal 2b backend flash. Fig. 17 shows the resulting scaled ENOB verses comparator offsets with a full $\mathrm{CRZ}_{\mathrm{Z=1}}$, $\mathrm{CRZ}_{\mathrm{Z=2}}$, and 2.5b/stage pipelines with ideal back-end and final pipeline stage comparison thresholds. By scaling the CRZ stages, the residue of each pipeline stage is ideally still within the PDF residue shaping range of the pipeline. However, since the number of early stage comparators have been reduced, the offset tolerance also reduces. Fig. 17 demonstrates these results by showing a pipeline of $\mathrm{CRZ}_{\mathrm{Z=1}}$ and $\mathrm{CRZ}_{\mathrm{Z=2}}$ stages which achieve less than 1b of added resolution due to PDF residue shaping. The scaled CRZ of Fig. 14 is also plotted in Fig. 17 which achieves the full 1b of resolution, but has a much lower offset tolerance when compared with the bounded pipeline structure of (4.18). Thus, scaled PDF residue shaped CRZ structures can make a lower power and complexity pipeline only if a smaller early stage redundancy range is not problematic, digital logic is cheap

and reference generation is not expensive. Otherwise, half-bit redundant architectures with PDF residue shaping are typically the better choice.

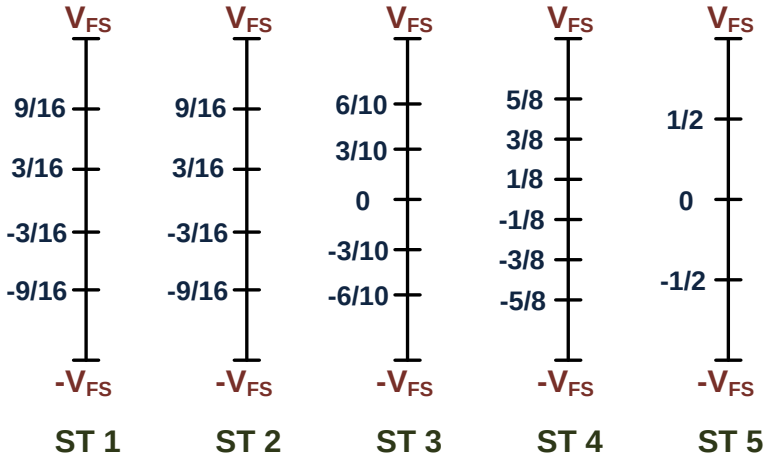

Figure 4.86: Scaled 4-stage CRZ pipeline ADC with 2b backend flash for optimal residue shaping

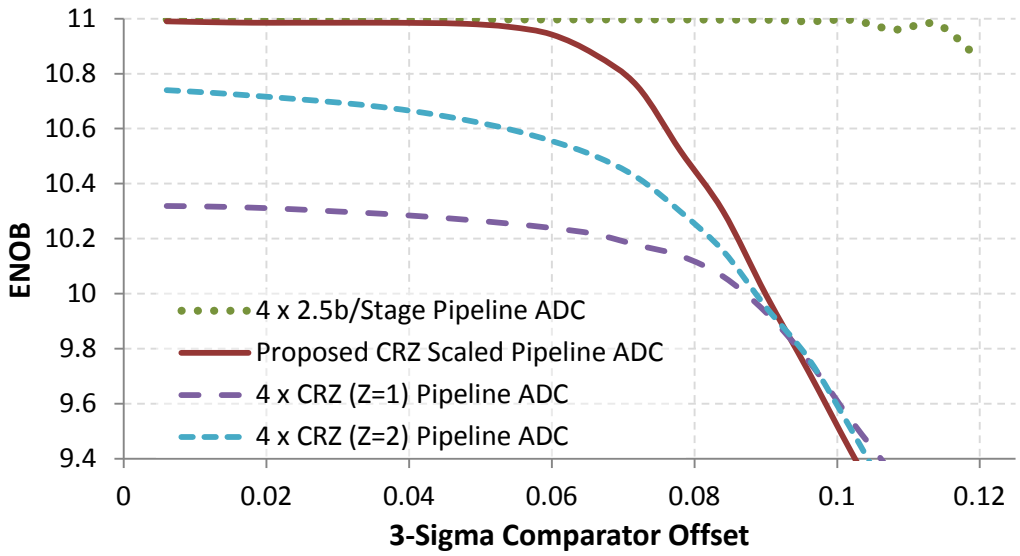

Figure 4.87: Resolution vs. 3-sigma comparator offset for normal CRZ stages, scaled CRZ, and 2.5b/stage ADCs with ideal back-end and last stage comparison thresholds

Finally, it can be shown that the pipeline of [19] also uses non-half-bit multi-level redundant stages but can achieve full bit PDF residue shaping due to the manipulation of the inter-stage gain. The analysis follows that of (4.4)-(4.7) and has offset bounds similar to that of (4.18).

4.4 Residue Shaping Conclusion

In this chapter, an analysis of PDF residue shaping was performed for multi-stage ADCs. PDF residue shaping results in nearly 6dB of extra resolution for half-bit redundancy varieties due to the PDF of the residue being centered in the middle half of the final full-scale output range of the last ADC stage. This shaping was shown to not be present in extra-cycle and sub-radix redundancy with a partial presence in CRZ redundancy. An analysis of offset errors was also performed and a modified offset tolerant threshold region was derived. Finally, design suggestions were made to maximize the resolution of a given multi-stage ADC with residue shaping by identifying critical sub-ADC stages, describing the ideal back-end ADC gain, showing optimal 2b back-end ADC threshold levels, and describing optimized CRZ redundant ADCs.

4.5 Residue Shaping Acknowledgements

This work was completed and published along with Manideep Gande and he deserves much of the credit in the development of the residue shaping idea and ADC design choices. I would like to also thank Ho-Young Lee, Ben Hershburg, Hariprasath Venkatram, and Shannon Guerber for insightful discussions on paper and chapter content and the anonymous journal reviewers for their helpful comments along the way.

5. THE EMCS SAR

In the previous chapters, the SAR ADC has been explore and enhanced by employing time and statistical innovations in the quantizer unit. In this chapter, we will move from the quantizer to the other major power consuming block in the SAR ADC, the feedback DAC. Here we will use statistical information to help optimize the DAC switching algorithm, for further power reductions and linearity improvements.

For the traditional binary capacitor based SAR without calibration, the capacitor array can often consume a large fraction of the total power consumption. Careful study has shown that the switching algorithms employed by SAR converters can have dramatic effects on the losses through this capacitor bank. It has been demonstrated in [1] that by splitting the MSB capacitor into sub-capacitors the switching power can be reduced by 37% over the traditional approach [2], while the "monotonic" method demonstrated an 81% improvement by switching only one side of a differential capacitor array per bit [3]. The merged capacitor switching (MCS) algorithm of [4]-[5] improves this savings to 87.5% by utilizing the common mode reference already present in a differential SAR. This chapter will show that the MCS switching efficiency and static linearity are further improved by intelligently selecting the time that individual binary capacitors are reset with the early reset MCS (EMCS) algorithm. Section II of this chapter will review the MCS algorithm and Section III will identify MCS in-efficiencies and propose the optimized EMCS methodology. Section IV will describe the implementation and effect on other SAR circuit components with conclusions discussed in section V.

5.1 Review of the MCS SAR DAC Switching

While many SAR switching algorithms exist for un-calibrated binary weighted capacitive structures, the merged capacitor switching algorithm [4] (also known as common mode based charge recovery [5]) has been shown in chapter 2 to be the most energy efficient to date. To review, the operation of the MCS SAR begins by sampling the differential input signal onto the virtual ground nodes of the SAR with the back end of the capacitor bank tied to V_{CM} as shown in Fig. 1. With the input voltage sampled, the polarity of the input is first determined with the single comparator. This information is stored in the SAR registers and the DAC will subtract or add a differential voltage from the virtual ground nodes based on this polarity. If the

comparator output is a 1, VDD and GND will switch to the bottom plate of the positive and negative MSB capacitors respectively, subtracting VDD/4 from the differential input. If the comparator code is 0, the VDD and GND will switch to the bottom plate of the negative and positive MSB capacitor respectively, differentially adding VDD/4. Further cycles will add or subtract in the same manner with the DAC weight decreasing by a factor of 2 in each cycle. This switching method achieves a low power consumption given that there is only one switching event per bit, the back side capacitor voltage is centered at the common mode, and the first bit is determined before any DAC operations. Furthermore, this switching still allows the virtual ground common mode of the SAR to be constant with no net power drawn from VCM, even during the reset phase.

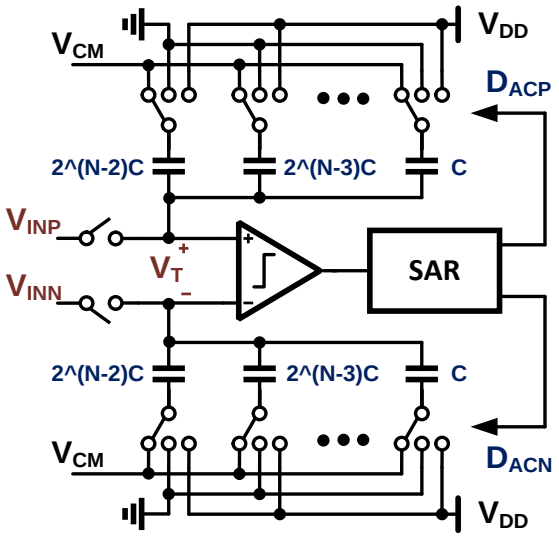

Figure 5.88: Merged capacitor switching (MCS) SAR architecture

The energy per code of the MCS switching scheme can be quantified by first examining the DAC power required in an example 3-bit MCS SAR. Fig. 2 shows this example 4C total capacitance MCS SAR and the energy required for each operation based on the current and previous codes. Here, in the first cycle, switching charge derived from VDD can be determined by calculating the differential voltage on the MSB capacitor (shown in equation 1 as the bottom plate voltage increase minus the top plate voltage increase) and multiplying by the switched capacitance. The cycle energy can then be found by multiplying the switching charge with the supply as shown:

$$\phi_1:\ E_{VDD}=\left[\left(\frac{1}{2}-\frac{C_{MSB}}{2C_T}\right)V_{DD}C_{MSB}\right]V_{DD}=\frac{C_{Unit}{V_{DD}}^2}{2} \tag{1.60}$$

Where CUNIT is defined as the LSB capacitor and the larger capacitors are composed of multiples of CUNIT. The energy from VDD of the second transition can be found in the same way for the second capacitor; however since the virtual ground voltage is moving with respect to the MSB capacitor, another term will need to be included. When the virtual ground voltages moves with respect to a VDD referenced capacitor, additional charge will be added or subtracted from the supply as shown:

$$\phi_2:E_{VDD}=\left[\left(\frac{1}{2}-\frac{C_{MSB-1}}{2C_T}\right)V_{DD}C_{MSB-1}\right]V_{DD}+C_{VDD}\left(\frac{C_{MSB-1}}{2C_T}\right)\ =\ \frac{5C_{Unit}{V_{DD}}^2}{8} \tag{1.61}$$

One can observe from (5.2) that there is an energy efficient switching step if the stage digital bit is the same as the previous bit and the step is less efficient if the bits are of the opposite polarity because of the previously switched capacitors connected to VDD. The total power of a given cycle (other than the MSB) can be generalized as the following:

$$\begin{aligned}\phi_N:\ E_{VDD}&=\left[\sum_{S=1}^{N-1}C_S\left(b_N\oplus b_S\right)\right]\left(0+\frac{C_N}{2C_T}\right){V_{DD}}^2+\left[\sum_{S=1}^{N-1}C_S\overline{\left(b_N\oplus b_S\right)}\right]\left(0-\frac{C_N}{2C_T}\right){V_{DD}}^2\\&\qquad+\left(\frac{1}{2}-\frac{C_N}{2C_T}\right){V_{DD}}^2C_N\\&=\frac{C_N{V_{DD}}^2}{2C_T}\left[\sum_{S=1}^{N-1}C_S\left(-1\right)^{\overline{(b_N\oplus b_S)}}-C_N+C_T\right]\end{aligned} \tag{1.62}$$

Where N is the given stage and (bN ⊕ bs) is the XOR of the current bit (bN) and the previous stage bit (bS). The total energy of a given MCS SAR conversion is then given by:

$$E_{VDD}\left(Code\right)=\frac{{V_{DD}}^2}{2C_T}\left[\sum_{N=1}^{M-1}C_N\left(\left(\sum_{S=1}^{N-1}C_S\left(-1\right)^{\overline{(b_N\oplus b_S)}}\right)-C_N+C_T\right)\right] \tag{1.63}$$

Where M is the SAR ADC resolution in bits and {b1, … bN} is the digital representation of the given code. This result is the same as was shown in chapter 2, just with a different example configuration.

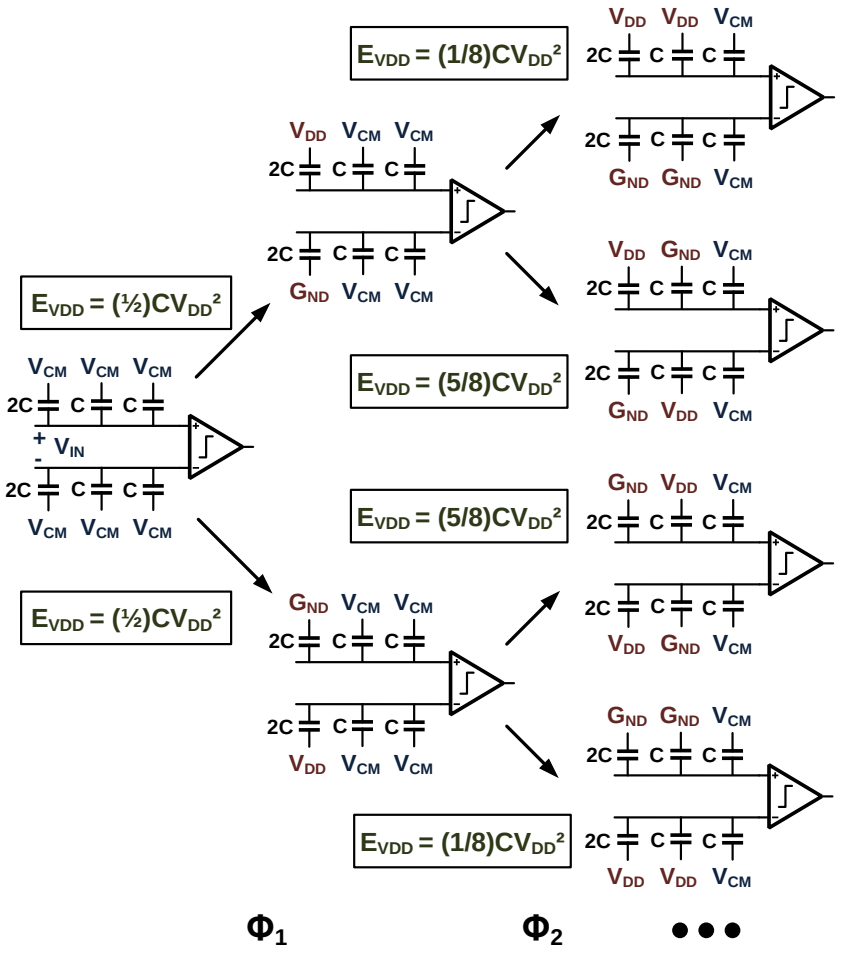

Figure 5.89: MCS SAR switching diagram and supply energy for a 3b example

5.2 The Early Reset MCS SAR

Looking at the MCS SAR described in section 5.1, one can see that in the second cycle, switching in the same direction as the previous cycle results in significantly less energy than switching in the opposite direction. However, switching in the opposite direction to correct a previous virtual ground overshoot is not always the only available option to generate the needed virtual ground voltage. Another solution is to reset the previous capacitor to V_{CM} and switch the current capacitor to the opposite polarity as shown in Fig. 3. By doing this, the energy for the capacitance connected to V_{DD} is reduced since the total supply referenced capacitance is decreased before the virtual ground node voltage changes and extra charge is added from the supply. This energy in the second phase, assuming the previous capacitor is fully reset before the next capacitor is switched, for this {1,0} transition is given as the following:

$$\phi_2 : E_{VDD} = \left[\left(\frac{1}{2} - \frac{C_{MSB-1}}{2C_T}\right)V_{DD}C_{MSB-1}\right]V_{DD} = \frac{3C_{Unit}V_{DD}^{\ 2}}{8} \tag{1.64}$$

Switching the previous capacitor to VCM requires no additional energy since it would be switched during the reset phase anyway and any prior charge on the capacitors is differential and canceled across the shared VCM node. Furthermore, reducing the supply referenced capacitance in early stages will also continue to reduce energy due to virtual ground movement in later stages. The function of the early reset MCS (EMCS) SAR algorithm is thus to reset the previous capacitor and charge the current capacitor in a given DAC operation to the opposite charge if the current bit is the opposite polarity of the previous bit. This results in the maximum energy efficiency for a 3-level DAC SAR.

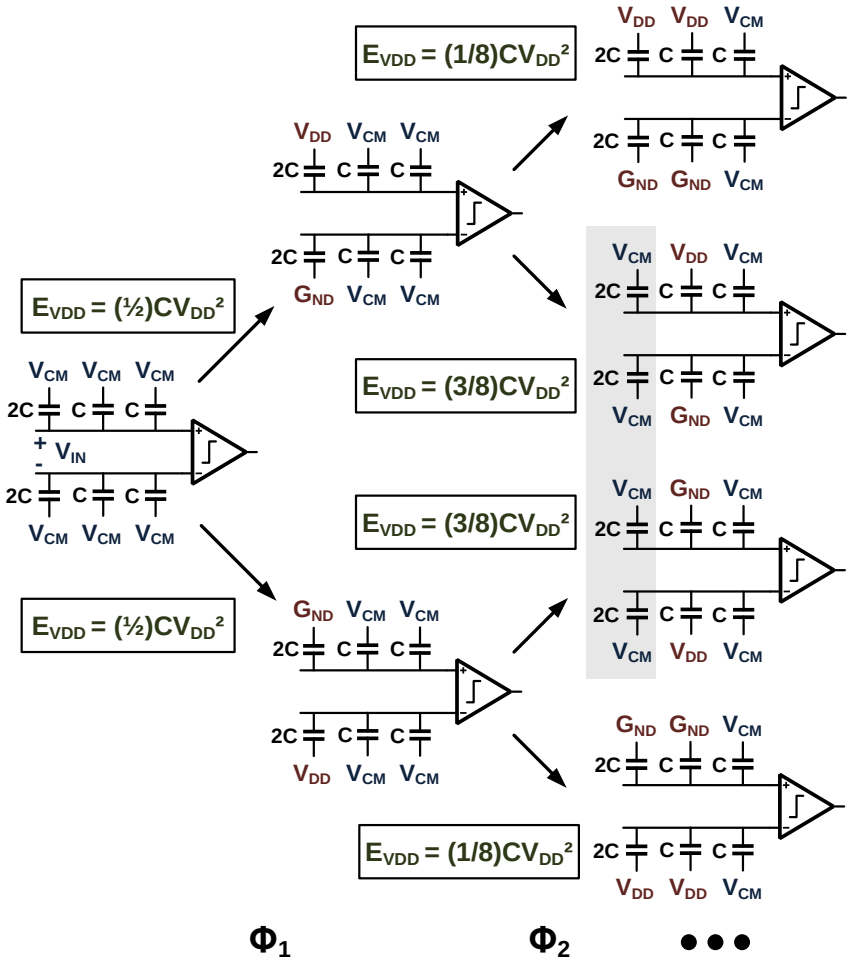

Figure 5.90: EMCS SAR switching diagram and supply energy for a 3b example

When comparing the energy of the MCS and EMCS techniques, the main difference of the EMCS algorithm is that capacitors for a given bit are only held at VDD and GND if, in the corresponding MCS digital code, the previous and next bits are the same. As an example, if the MCS digital code was {1,1,0} we know that in the second cycle the MSB-1 capacitor is charged to a "1' state. However since the next bit is a zero, the MSB-1 capacitor is reset in the next phase to VCM while the MSB-2 capacitor is charged to a "1" state. In the {1,0,0} code the MSB-1 capacitor is charged to a "1" in the second stage and reset to VCM in the third stage since the new {VCM, 1, 0} has an alternating second and third bit. Therefore, for any binary digital code representation, the supply connected capacitance corresponding to a given bit is dependent only on the previous and next bits being different. We can quantify the energy per stage of the non-MSB EMCS SAR cycles with codes corresponding to a typical binary representation as shown with the following:

$$\phi_N : E_{VDD} = \frac{C_N {V_{DD}}^2}{2C_T}\left[\sum_{S=2}^{N-1}\left(C_S\overline{\left(b_{S-1}\oplus b_{S+1}\right)}\left(-1\right)^{\overline{\left(b_N\oplus b_{S+1}\right)}}\right)+ C_1\overline{\left(b_1\oplus b_2\right)}\left(-1\right)^{\overline{\left(b_N\oplus b_1\right)}} - C_N + C_T\right] \quad (1.65)$$

The EMCS energy per binary digital code is then given by:

$$\begin{aligned} E_{VDD}\left(Code\right) = \frac{{V_{DD}}^2}{2C_T}\Bigg(\sum_{N=1}^{M-1} C_N\Bigg[\sum_{S=2}^{N-1}\left(C_S\overline{\left(b_{S-1}\oplus b_{S+1}\right)}\left(-1\right)^{\overline{\left(b_N\oplus b_{S+1}\right)}}\right) \\ + C_1\overline{\left(b_1\oplus b_2\right)}\left(-1\right)^{\overline{\left(b_N\oplus b_1\right)}} - C_N + C_T\Bigg]\Bigg) \end{aligned} \quad (1.66)$$

By comparing the power dissipation of the MCS and EMCS SARs, we can see that for every possible code, the EMCS SAR has equal or lower energy:

$$\begin{aligned} & E_{VDD,MCS}\left(Code\right) \geq E_{VDD,EMCS}\left(Code\right) \\ & \sum_{S=1}^{N-1} C_S\left(-1\right)^{\overline{\left(b_N\oplus b_S\right)}} \geq \left[\begin{array}{c}\sum_{S=2}^{N-1}\left(C_S\overline{\left(b_{S-1}\oplus b_{S+1}\right)}\left(-1\right)^{\overline{\left(b_N\oplus b_{S+1}\right)}}\right) \\ + C_1\overline{\left(b_1\oplus b_2\right)}\left(-1\right)^{\overline{\left(b_N\oplus b_1\right)}}\end{array}\right] \end{aligned} \quad (1.67)$$

The energy per code is also plotted in Fig. 4 for a 12b SAR operation normalized to (C_{UNIT}*V_{DD}^2) and energy reduction can be seen for each code. For a uniform input probability density function (PDF), the EMCS structure results in 12.5% lower average switching energy and an even lower 18.4% when the input has a Gaussian distribution (since the Gaussian PDF has more codes in the EMCS reduced energy region). The switching energy is lower for central

codes since the EMCS greatly reduces the power of alternating codes that would be seen in an MCS configuration. Compared to the set and down technique [3], the EMCS technique provides a 41.5% average switching energy reduction.

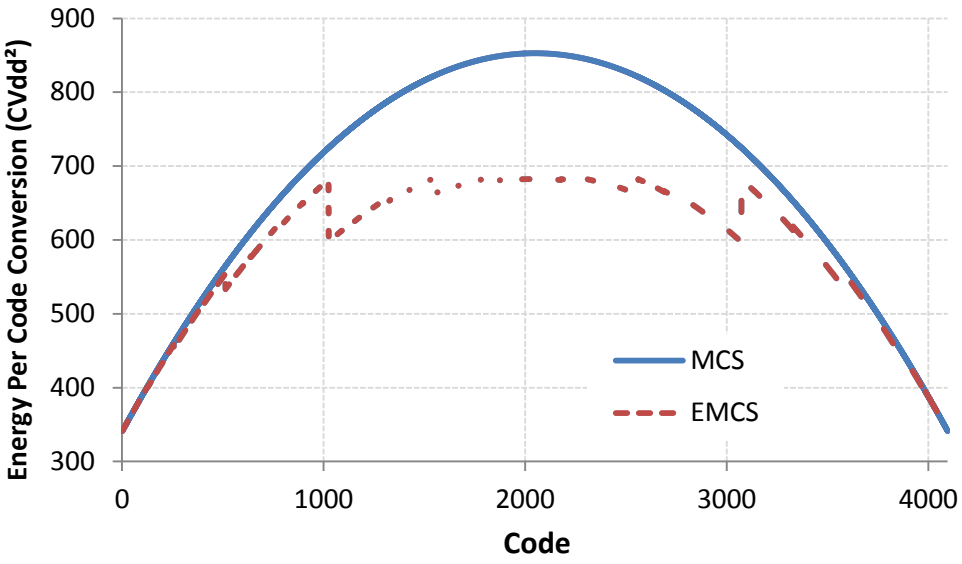

Figure 5.91: SAR switching energy per code for the MCS and EMCS structures in a 12b ADC

In addition to the power savings, the worst case code for the ADC differential non-linearity (DNL) is now no longer {1,0,0,0…} to {0,1,1,1…} since this code has an alternating set of bits. Rather the worst case transitions are now from {1,VCM, VCM, VCM…} to {VCM, 1, 1, 1…} and {0,VCM, VCM, VCM…} to {VCM, 0, 0, 0…} as shown in Fig. 5. Here, the effective variance of the virtual ground charge due to the worst case code capacitor matching requirement is reduced by a factor of 2 over the MCS SAR variance meaning the DNL is reduced by a factor of two on average. The per code DNL is shown for both the MCS and EMCS SARs in Fig. 6 with the middle transition spike not present in the EMCS case.

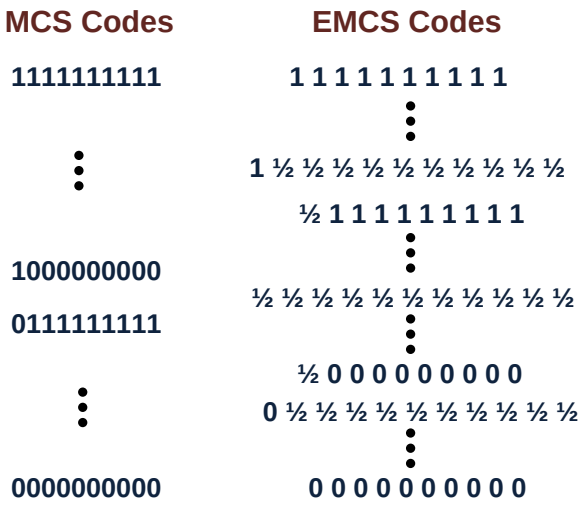

Figure 5.92: The range of MCS and EMCS codes with the major transition points highlighted

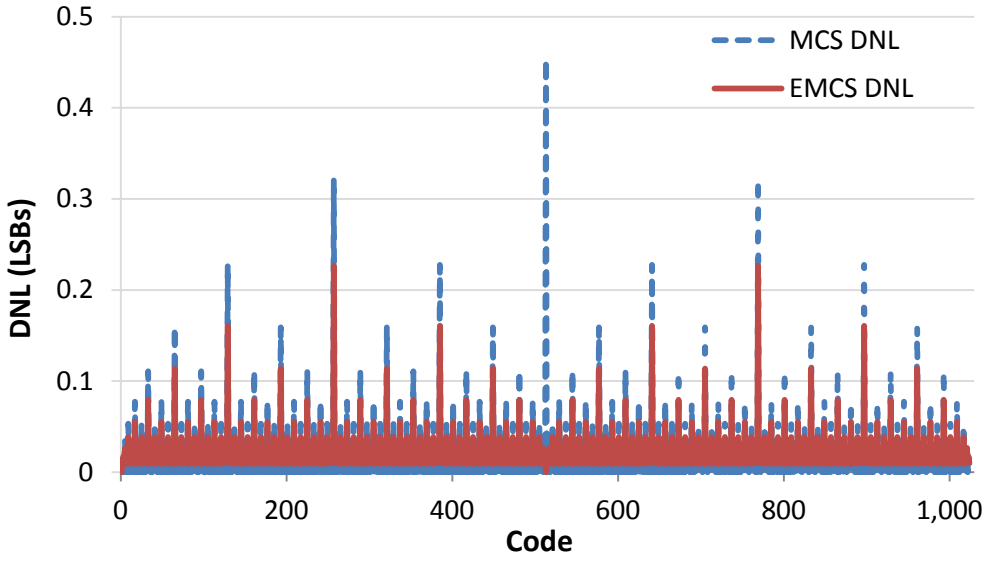

Figure 5.93: Example DNL for the MCS and EMCS SAR Architectures

The integral non-linearity (INL) is also reduced by a factor of two as shown in Fig. 7, and exhibits a dual lobe behavior due to the presence of the all "VCM" code which codes all capacitors with one value just like an all "1" or "0" code. The implication of this are that if the SAR being designed is limited by DAC matching requirements set by the process, this structure will ease those requirements, allowing for a smaller sized DAC.

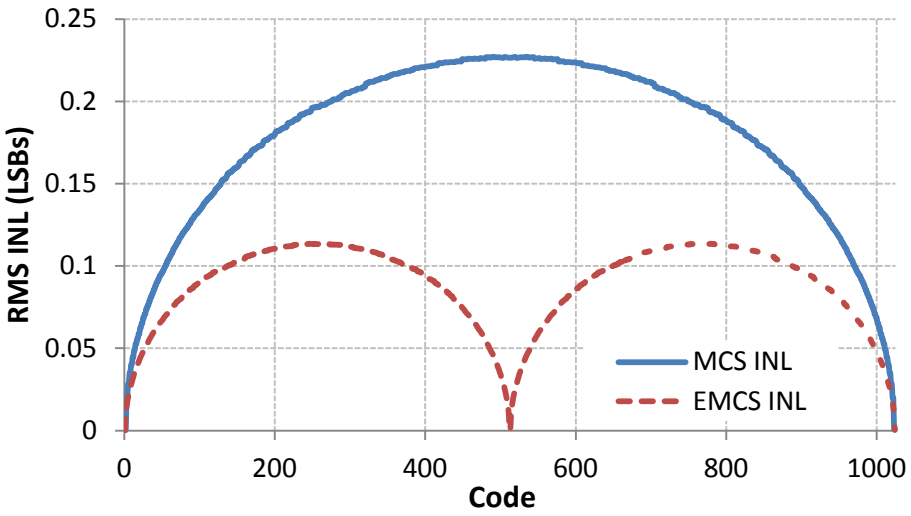

Figure 5.94: RMS INL in LSBs for the MCS and EMCS 10b SAR ADC structures with a unit capacitor sigma of 0.02 LSB (10,000 simulations) [7]

5.3 EMCS Implementation

The EMCS structure achieves a greater switching power efficiency and static linearity by identifying whether a current bit is the same as the initial first comparison output. If it is the same, the first comparator decision is kept and sent to the DAC. If the bit is complementary to the initial, the previous DAC value is reset to V_{CM}. The full switching algorithm is given in Fig. 8.

Typically in a SAR register block, the output of the comparator is captured onto a flip flop which is clocked by the appropriate SAR phase generated by a state machine. Due to the EMCS algorithm however, one can see that the current bit is always the same as the first bit regardless of the comparator output. At the circuit level, the comparator will only give information as to whether or not the previous bit should be reset to V_{CM}. Because of this operation, the EMCS structure is the same as in Fig. 1, with the only change being the SAR logic, which can be modified as shown in Fig. 9 with the addition of only a few extra gates. Here, the MCS configuration consisting of positive and negative flip flop registers are employed and when neither flip flop is holding a 1, the corresponding DAC capacitor is tied to V_{CM}. In the EMCS structure however, if the comparator output is different than the first bit, that previous stage's flip flops are synchronously reset and the current flip flop output is a copy of the previous. The final data output is then valid and has a modified three-level coding (G_{ND}, V_{CM}, V_{DD}) which can be easily added to return to a binary representation. This switching method does not add any

extra activity or loading to the DAC capacitor drivers since all capacitors would need to be reset anyway before sampling the next analog input.

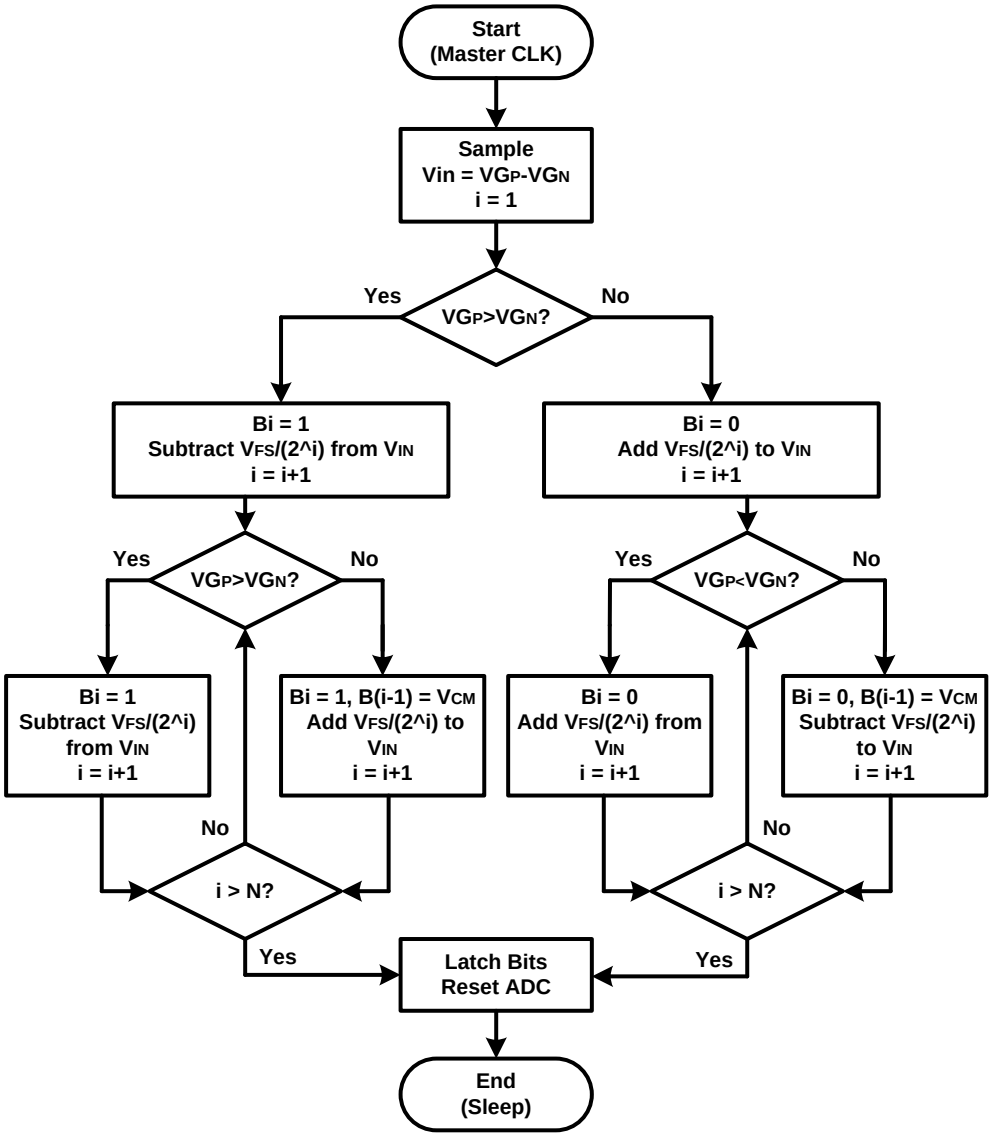

Figure 5.95: Switching Algorithm Flowchart for the EMCS SAR Implementation

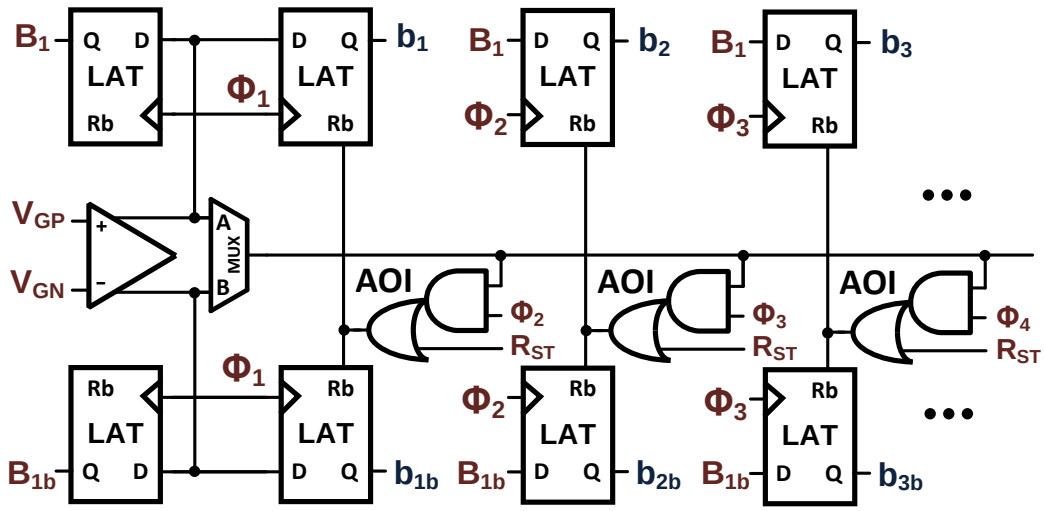

Figure 5.96: Sample logic implementation for the EMCS SAR ADC

It should also be noted that most SAR architectural variations building upon the MCS switching structure, such as the ternary SAR [6], can still reap greater energy savings with an EMCS switching algorithm and since the EMCS SAR outputs a ternary coded word, it can be used in conjunction with the TSAR structure. This second idea will be further explored in the FITSAR ADC. Also, EMCS transistor level simulations in 0.13µm CMOS have been performed and show about a 10% switching power reduction (lowered from behavior models due to capacitive parasitics) for a 10b SAR over the MCS structure.

5.4 EMCS Conclusions

This chapter has analyzed the merged capacitor switching algorithm and proposed the early reset MCS switching technique to further reduce switching power consumption by over 12% and improve static linearity by a factor of 2 over the MCS SAR ADC. This method better utilizes the available common mode reference in the MCS DAC and is shown to improve or match energy efficiency for every code as well as allow for better ADC static linearity. The implementation can be made with little logic overhead and does not increase DAC driver power.

5.5 EMCS Acknowledgements

This work was aided by the insights of Hari Venkatram and Taehwan Oh (co-authors on original paper) and Manideep Gande. Also, thanks to Dr. Moon and other reviewers who gave great feedback.

6. THE FEEDBACK INITIALIZED TERNARY SAR

The quest for ever higher efficiency ADCs that don't sacrifice performance led to the development of the ternary SAR (TSAR) in chapter 3. That structure provided windowed switching for reduced DAC activity, scalable redundancy for improved accuracy, and comparators speed optimization for improved bandwidths [1]. While the TSAR pushed the efficiency bounds of the traditional SAR, it was limited due to the framework of the historical single stage SAR ADC. This chapter will look employing TSAR ADC techniques into a split stage SAR and see how to re-analyze time domain and statistical information for an even lower power and higher bandwidth structure. This feedback initialized ternary SAR (FITSAR) will also incorporate the residue shaping of chapter 4 and the EMCS switching of chapter 5 to make one improved structure [2]-[3].

6.1 Ternary SAR Limitations

The ternary SAR, shown again in fig. 1, is meant to be a direct improvement to the state of the art merged capacitor switching (MCS) SAR, improving the power efficiency, speed, and accuracy though windowing, 1.5b/stage redundancy, residue shaping and stage skipping. In this section the TSAR will be shown once again and some of the fundamental limits of the structure will be examined. These limits will then provide the motivation for the next prototype.

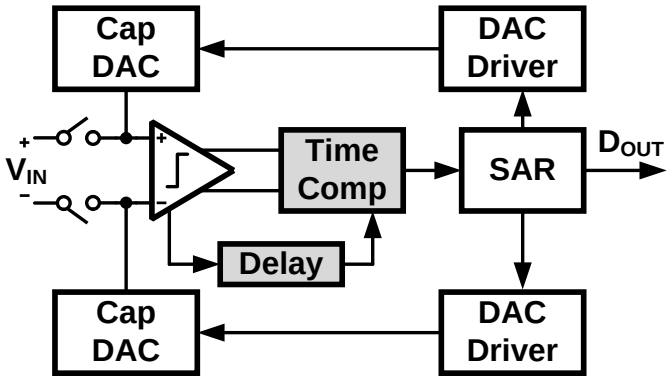

Figure 6.97: The Ternary SAR Block Diagram

6.1.1 TSAR Windowing

One of the energy saving features of the TSAR structure was DAC windowing, which reduced the activity of the DAC when the input was small. This occurred because when the input was within both time comparator thresholds, no switching operation was performed, meaning that no capacitor switching power or DAC driver power was used. Since the time comparator thresholds scaled with the full-scale range, the no switching region was a fixed percentage of each stage. However, due to the scaling of DAC capacitors, the amount of energy savings decreased by about a factor two per stage.

In order to maximally reduce DAC activity, the no switching region should be as large as possible in magnitude and the largest possible range for a three-level DAC is to have the no switching window extend to exactly half of each stage's full-scale range, as shown in fig. 2. The other factor that comes into play with this optimization though is redundancy. Redundancy is created in the TSAR (and any 1.5b/stage SAR) by keeping the largest stage bin (region between two thresholds) smaller than if there were no added levels. In the TSAR, having the two time comparator thresholds be extremely small means that the top and bottom codes are almost the same as with no time comparisons, thus there is effectively no redundancy. Also, if the time comparison thresholds are placed at ±VFS/2, then the middle code is equal in size to either the original top or bottom code and there is once again no redundancy. The maximum redundancy (in order to allow for the maximum threshold offset and settling error) is to place the two time comparator thresholds halfway between these two extremes at ± VFS/4. Thus there is a conflict between the optimal redundancy and the optimal DAC activity.

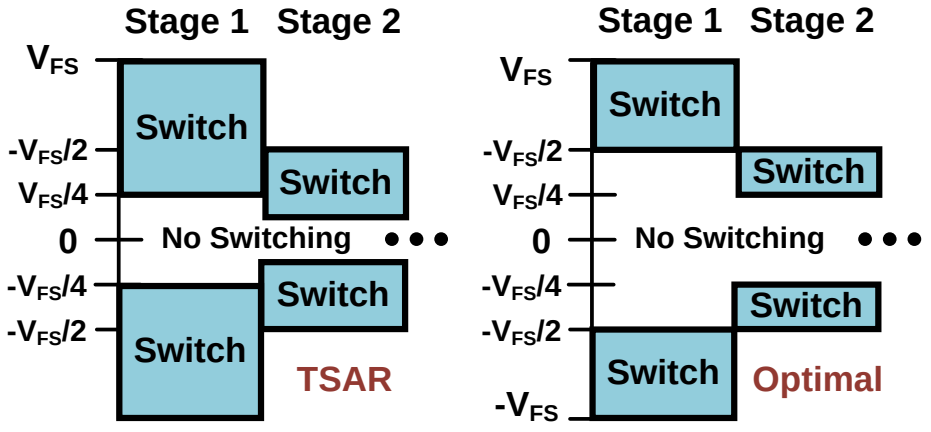

Figure 6.98: Early Stage DAC windowing in the TSAR and optimal structures

In the TSAR, redundancy was required in each stage due to the limited accuracy of the time comparison structure. Since the accuracy of the time comparison thresholds didn't change from one stage to the next (since it was implemented in the time domain), their offset was a fixed percentage of each stages full-scale range. To compound the issue, in the first stage, there was some comparator time nonlinearity due to large signal effects. Thus, in the conflict between redundancy and DAC activity, redundancy was implemented for error prevention. However, if another method were to be found to solve the question of time domain errors, the no switching region could be increased, significantly improving the structural efficiency.

6.1.2 Cyclical Switching

In most SAR structures, the DAC must be switched one capacitor at a time (hence the name successive approximation). This requires energy to not only charge the given stage capacitor, but due to the interconnection across the virtual ground nodes, extra energy may be required from the charge sharing effects of early supply connected devices. In chapter 5, this charge sharing energy was minimized by minimizing the earlier stage supply connected capacitance, but it could not be eliminated. Ideally, if multiple capacitors could be charged in one phase to one potential, the charge sharing energy could be reduced and in the best case, entirely eliminated as shown in fig. 3.

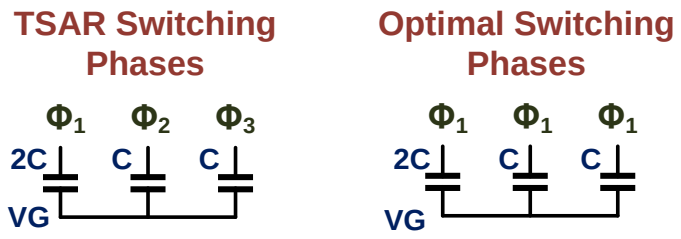

Figure 6.99: DAC switching phases in the TSAR and optimal SAR ADCs

6.1.3 Comparator Accuracy Requirements

In ADCs with redundancy, the accuracy of the sub-quantizer (like the sub-flash of a pipeline) is decoupled from the overall accuracy of the converter. Often the accuracy of the sub-ADC must only be 1 or 2 bits more accurate than the resolution of the given stage. In pipeline converters, the comparators can then be scaled, significantly reducing power consumption (and improving overall accuracy beyond what matching would normally allow).

In the SAR structure with redundancy, lower accuracy quantizers can be used in the earlier stages, however this is often not feasible since there is only one fixed comparator to prevent inter-stage offsets. The TSAR took partial advantage of the redundancy even though there was still one fixed comparator, by changing the amount of time each stage resolved for. While this improves the bandwidth of the converter, this is still much less power efficient then if the comparator was physically scaled as shown in fig. 4.

TSAR Comparator Sizes

Stage	Sized Comparator Accuracy
1	13b
2	13b
3	13b
•••	

Optimal Comparator Sizes

Stage	Sized Comparator Accuracy
1	3b
2	4b
3	5b
•••	

Figure 6.100: Comparator sizing in the TSAR and optimal SAR ADCs

6.2 The Feedback Initialized Ternary SAR

The ternary SAR provided a number of important benefits, but to account for the problems mentioned in the previous section, a new overall SAR structure has been proposed. The feedback initialized ternary SAR is shown in fig. 5 and is much like the normal TSAR with the exception of the coarse ADC path around the TSAR quantizer. This coarse path will operate only in the first few cycles and provide ternary coarse bits to the main SAR logic unit that are initialized in a single phase to allow for the optimal charging of the TSAR DAC unit.

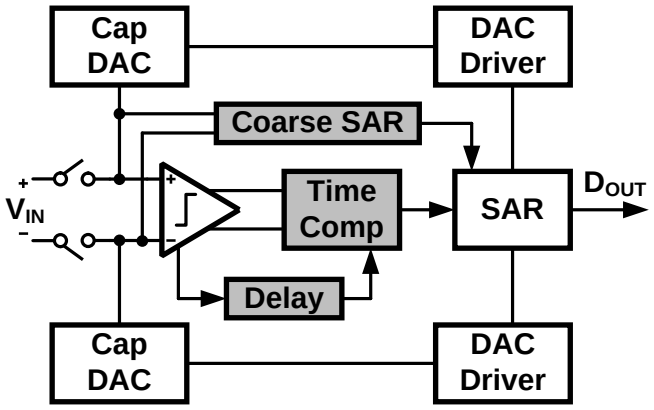

Figure 6.101: The Feedback Initialized SAR (FITSAR) block diagram

6.2.1 FITSAR Nesting

Adding an additional early stage coarse SAR path to the TSAR structure is much like adding a sub-ADC to the main fine SAR. Typically this is not done in SAR structures (unlike pipelined ADCs) due to the fact that requirements on the offsets of the stages become too large for accurate ADCs. In this structure however, the coarse ADC only extends to the point where the offsets become too much to handle with typical design (and basic calibration) methods. Also, the coarse ADC offset does not have to be smaller than the offset of the entire SAR since there is redundancy present (which will be described later) and the output is acting upon the final fine ADC, not transferring residue directly. It should be noted that this is different than a typical SAR multi-stage ADC [4]-[5] since here, the residue of the coarse stage is not being transferred to the fine stage, rather simply the digital word is sent as shown in the more detailed block diagram of fig. 6. This means that as long as no overrange errors exist, the static linearity of the ADC is only a function of the fine DAC.

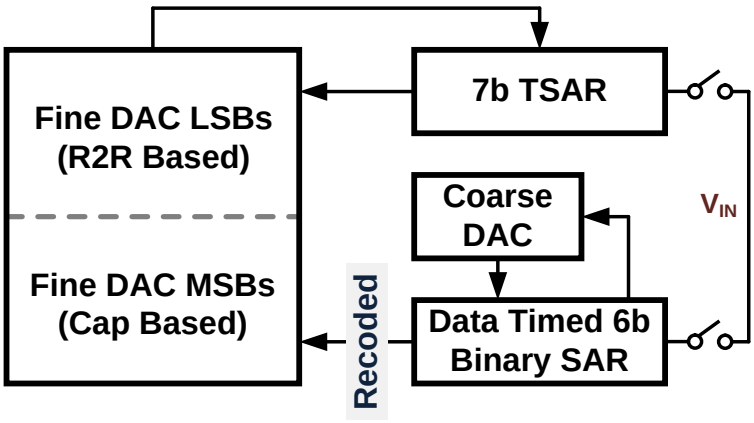

Figure 6.102: FITSAR top-level block diagram illustrating nesting

By nesting the coarse and fine stages in this manner, both the quantizer and DAC can be sized independently based on noise and matching restrictions. Additionally, there is no requirement on the algorithm of the two stages to be the same either, so a cheap binary SAR could be used for the coarse stage and a ternary SAR for the fine.

There have been some similar ideas to the coarse and fine stage, with perhaps the most famous being [6]. In this work, the authors have a single SAR circuit and split the comparator into a coarse and fine stage for the early and late cycles, but the coarse comparator is not is a sub-ADC, thus there is no DAC power savings, just comparator. Also, the redundancy must be

added into the overall loop, to correct for comparator offset errors, not just in the low power coarse. Later in the chapter, the choice of each stage's comparators and SAR algorithm will be selected to optimize each stage for efficiency.

6.2.2 Coarse/Fine Digital Recoding

While the nested SAR structure has a number of comparator energy reduction benefits, it also allows for the opportunity to optimally switch the initial coarse bits onto the fine DAC. Since the coarse and fine SAR structures are decoupled in terms of their DACs and quantizers, the coarse SAR is often not a ternary quantizer based structure, but rather a binary one, since the ternary structure has a limited impact (and could increase the energy) on very low resolution SARs. This decoupling also allows for the binary output of the coarse phase to be re-arranged in such a way that the optimal windowing of fig. 2 is achieved.

To achieve an optimal 3-level windowing from a 2-level output code, it's important to know that the 3-level DAC must only switch when the input is greater than $\pm V_{FS}/2$ of the current stage, as mentioned earlier. The truth table of such a recoding is shown in fig. 7. Here, one can see that is a karnaugh map is used to simplify the recoding implementation logic, each ternary trit should only become a "1" or a "0" if both the first bit and the stage+1 bit are the same. Otherwise, the ternary fine trit should stay at V_{CM}. The other way to think of this operation is that the first binary bit divides the input full scale range into a positive and negative half where on the positive side, only "1" and V_{CM} codes are used and on the negative, only "0" and V_{CM} are used. Then each following binary bit controls the previous stages ternary trit, reducing the magnitude of the input only when the current stage bit matches the first bit. This logic operation means that the recoding algorithm can be implemented with a simple array of AND gates, with one gate controlling each fine ternary trit.

Figure 6.103: DAC Recoding Implementation showing truth table, k-maps, and logic

6.2.3 Feedback Initialization

Recoding and nesting offers significant efficiency enhancements, but the decoupling of the coarse and fine stages also allows us to adjust the timing of the inter-stage switching operations. In a typical single DAC SAR, each DAC switching event must be made in the phase of the quantizer decision, since the DAC movement determines the next stage input voltage (residue). This is the same in the FITSAR, only now there are 2 DACs. Thus while the coarse DAC need to operate in each phase for the accurate quantization, the fine DAC does not and it turns out waiting until all the digital output codes are valid and then switching in one phase is the most optimal.

To see why this is, the three bit example of figure 8 is shown. Here, assuming the bits are all switching from GND to VDD, the energy decreases significantly when the first two capacitors are grouped, and goes to zero when they all are switched together. The reason behind this is that in the third case, the capacitive array looks like a single floating capacitor and assuming there are no parasitics, this operation should burn no energy. In the other cases, when a capacitor switches to VDD with other caps still connected to GND, the potential rise on the virtual ground node pushes some charge into GND and once that charge enterers, it is lost. One thing to note is that the last switching event in each case, where the last cap goes to the same potential as the previous caps, burns no energy because the charge from the last capacitor's supply is cancel by the charge entering the other capacitor supplies due to virtual ground voltage movement. Since the fine DAC capacitors are all initialized to the coarse codes in one, phase, the term feedback initialization is used to describe the switching (hence the FITSAR).

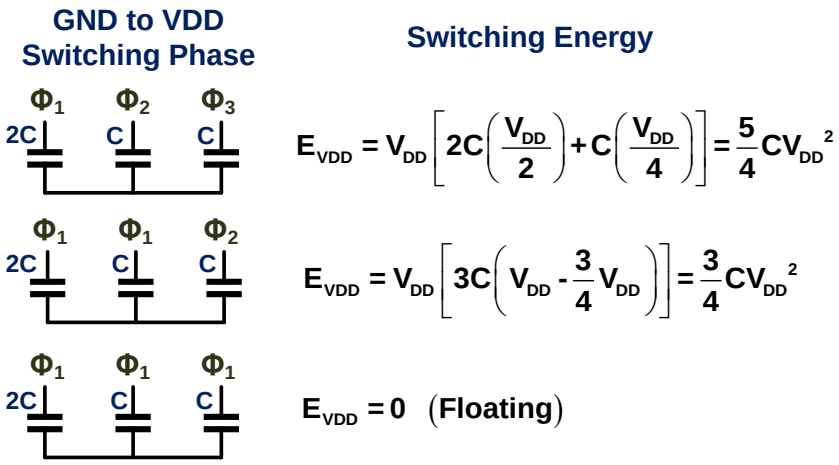

Figure 6.104: Energy reduction due to capacitive feedback initialization

Together the energy saving from the recoding and feedback initialization save 61% of the DAC switching energy and 34% of the DAC driver activity as compared to the TSAR (where the TSAR has comparator thresholds at the prototype boundaries) as shown in fig. 9 and 10. When compared to the MCS SAR, the FITSAR saves 86% of the switching energy and 74% of the driver energy. If the coarse ADC were to be extended for more stages, the efficiency might increase, but only very slightly since the DAC energy impact decreases as the stages increase. One note is that while the DAC switching energy comes from both the recoding and initialization, the driver energy reduction is nearly only from recoding, since it is based on the number of until caps charged. Because of this, the driver energy in the FITSAR forms an envelope function around the TSAR data since the TSAR has varying periods of optimized and non-optimized switching while the FITSAR maintains the DAC windowing constantly across all codes.

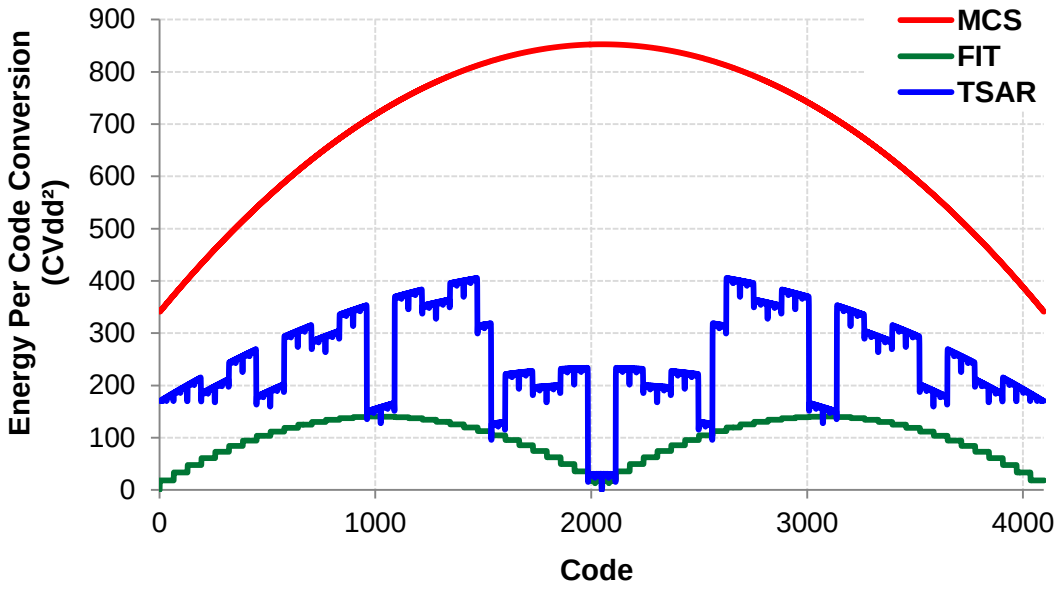

Figure 6.105: SAR DAC switching energy comparison vs. code

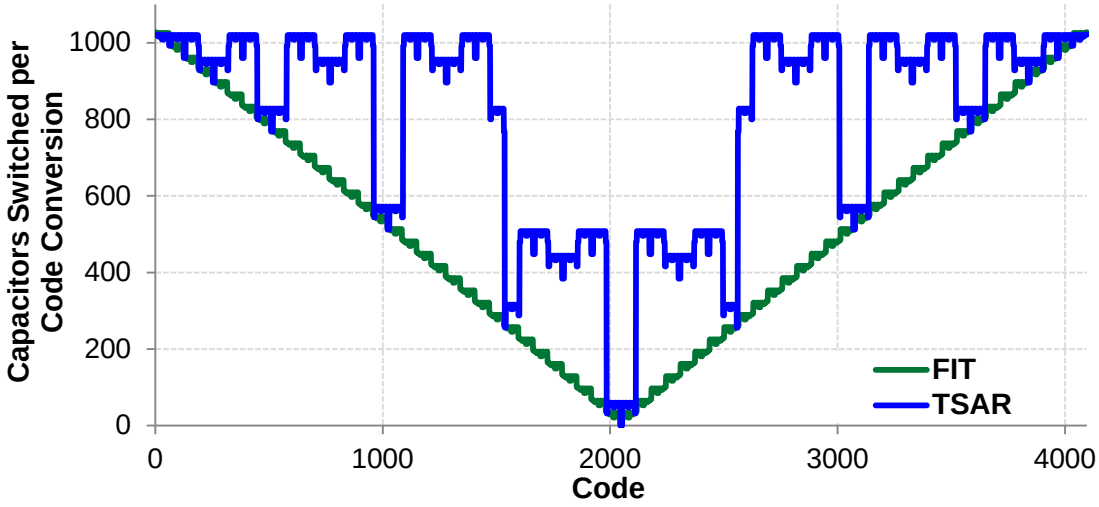

Figure 6.106: TSAR and FITSAR Driver Activity vs. code

The comparator energy will also see reductions in the FITSAR primarily with the reduced activity on the fine comparator due to nesting (coupled with the existing TSAR improvements) as shown in fig. 11. In the FITSAR comparison plot, the coarse comparisons are included and are multiplied by the energy reduction factor due to the accuracy reductions.

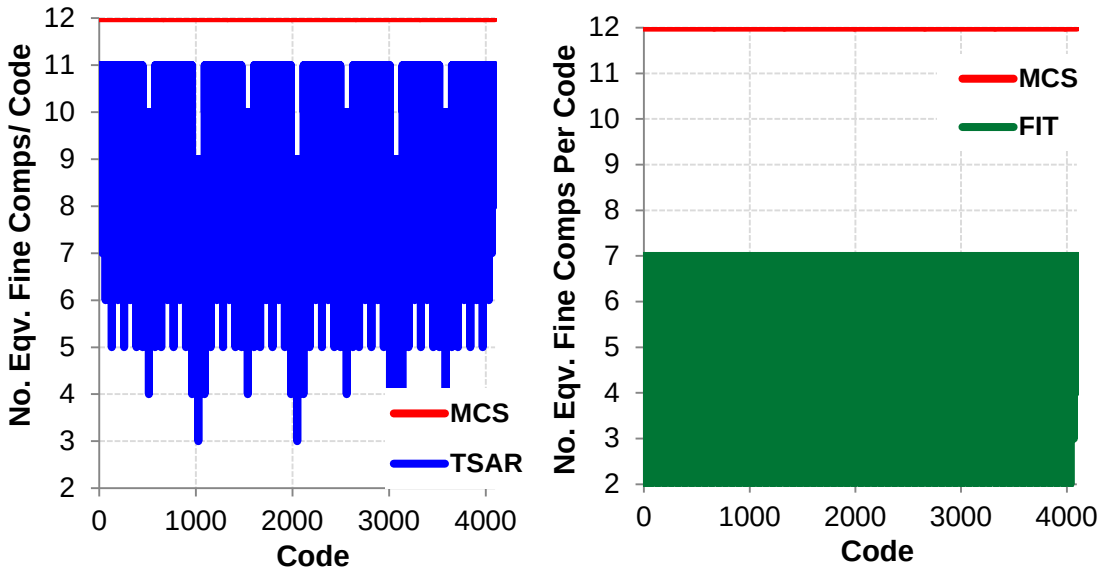

Figure 6.107: Number of equivalent fine comparisons per ADC output code

6.3 FITSAR Structural Enhancements

While the FITSAR has a number of inherent benefits due to the algorithm, the design of the structure can also lead to efficiency and performance enhancements. Here, the design of the FITSAR structure will be described to maintain the redundancy, grouping, and residue shaping effects of the TSAR, as well as optimize the coarse ADC for energy reduction and change the traditional binary capacitive DAC to allow for better matching and easy calibration.

6.3.1 Redundancy, Grouping, and Residue Shaping

The TSAR structure that forms the foundation for this work provides redundancy based on the three levels of the quantizer. This redundancy is maintained in the FITSAR fine stage, but since the coarse stage is typically not ternary, the redundancy here is added by simply making an extra stage. While this was not optimal in the ternary SAR due to the large power consumption of the DAC and comparator, here the redundancy can be added to the coarse SAR, adding a minimal amount of power and delay.

Since the redundancy is not implemented in the time domain for the coarse stage, there isn't a need for separate internal VCO time grouping for the first 5 phases (plus one for redundancy). The time grouping used in the FITSAR is shown in fig. 12. Here, the rest of the time groupings are divided between the 6-8th, 9th, and 10th phases. The separation for the last phase is for the

residue shaping extra bit to be obtained and the 9th phase grouping is to allow for some redundancy in the 8th phase (since the second to last stage does not have redundancy in residue shaping multi-stage ADCs).

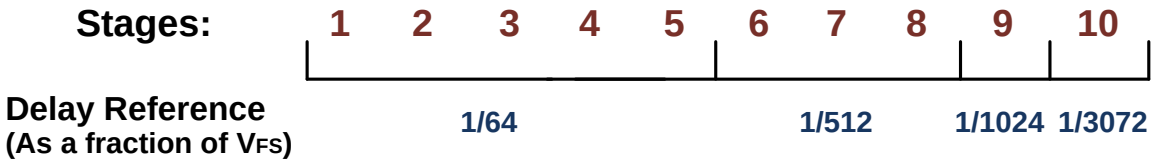

Figure 6.108: Delay reference grouping per stage for the FITSAR structure

Another modification that needs to be made to the FITSAR coding for residue shaping and redundancy to be present is a shift in the coarse codes. In fig. 7, one can see that the 2 middle codes out of the coarse ADC will both be mapped to the same code in the fine ADC. This means that there is effectively an LSB/2 offset error between a positive and negative input (LSB of the coarse stage). To solve this problem, the residue of the coarse phase can be shifted by +LSB/2 in magnitude in order to allow the final PDF of the fine DAC to be initialized to the correct region as shown in fig. 13. The shift is done in the coarse ADC to minimize power and is completed by simply adding a half sized capacitor to the coarse array with the input being bit 1b as shown in fig. 14.

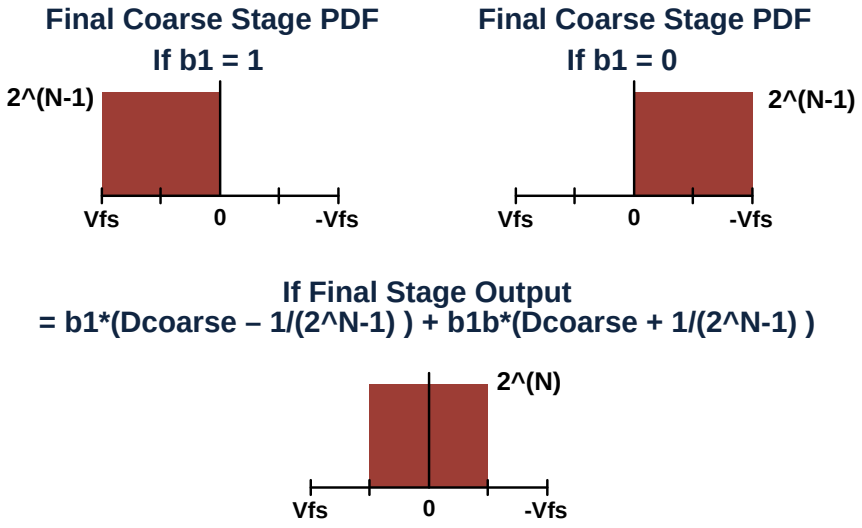

Figure 6.109: Fine DAC PDFs from the feedback initialization of the shifted and un-shifted codes

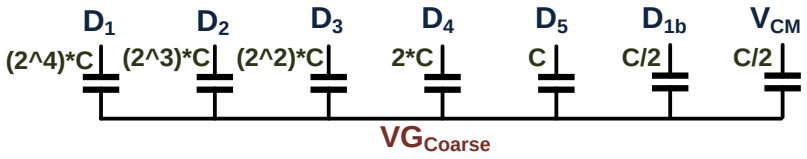

Figure 6.110: FITSAR Coarse ADC DAC with shifting to allow for redundancy in feedback idealization

While the offset of magnitude of the codes is one way of preventing the middle coarse codes from being mapped to the same point in the fine DAC, simply shifting all the fine codes by LSB/2 could also work. However as shown in fig. 15, the encoding algorithm would become more complex and the PDF would shift and be unbalanced.

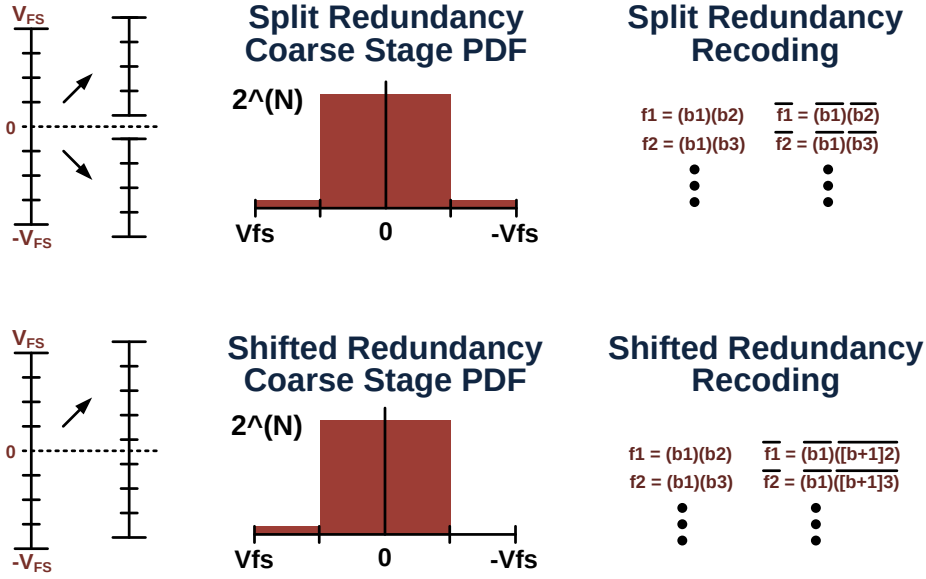

Figure 6.111: Comparisons of split redundancy and shifted redundancy

6.3.2 Coarse ADC Optimization

When describing the FITSAR structure, one of the benefits of nesting was the ability to fully decouple the coarse and fine ADCs. This means that a cheap binary SAR could be used for the first 6 bits and the TSAR structure could be implemented for the higher accuracy remaining bits. The main reason for using the binary SAR is that the three-level quantizer would have a minimal impact in the power reduction and might actually lead to a net power and bandwidth increase.

One alternative to the traditional binary SAR however, is the EMCS SAR described in chapter 5. Here a binary quantizer is still used but the MCS three-level DAC is optimized by resetting early switching events to reduce later stage charge sharing as shown in fig. 16. This turns out to be a great option, not only because of the power and linearity improvements, but also because of the fact that the output codes are automatically in three levels and are recoded based on the recoding fig. 7. This reduces the total logic needed and also reduces the number of logic stages in the coarse SAR by 1 due to the three levels per stage.

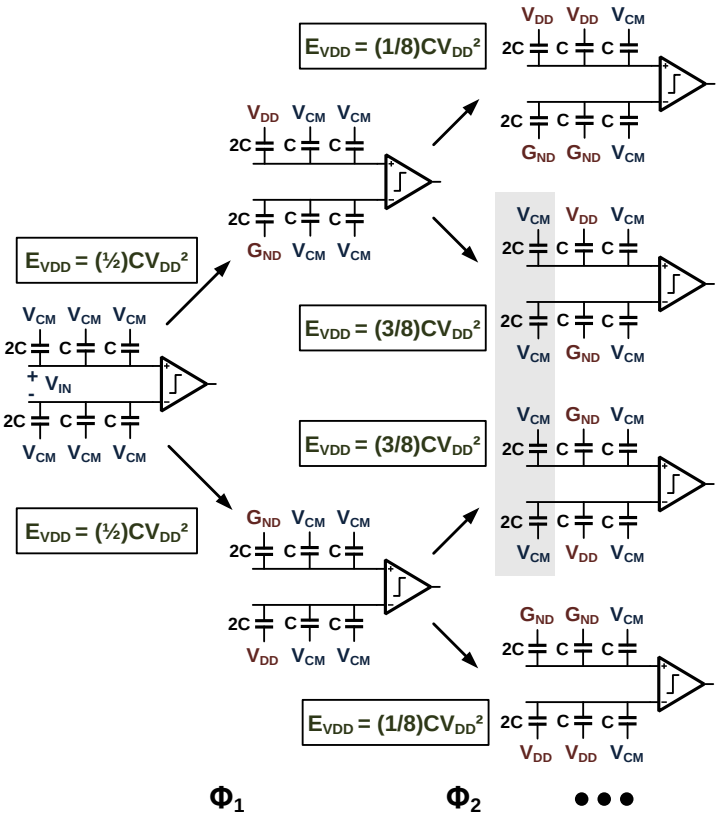

Figure 6.112: The EMCS SAR used as the coarse ADC in the FITSAR prototype

6.3.3 C-R2R DAC Optimization

In many SAR ADC (the TSAR included) the DAC is implemented as a binary weighted capacitive array. This is great for power consumption and requires the total array to be sized in order to minimize the sampled thermal noise, but is often large due to matching problems encountered because of the large device spread. To minimize this, many SARs will implement split DACs [7] which have a small binary weighted array, a coupling capacitor, and then another small capacitive array. While this can reduced the mismatch requirements of the DAC, it does

slightly increase the cap sized based on thermal noise limits and require calibration and complex adders for the non-integer coupling capacitor. This coupling capacitor problem is a result of the charge sharing of the backend DAC and the capacitance of the interstage device not creating a full-scale voltage on the input of the coupling capacitor as would be expected if it were driven be a voltage source.

To solve the mismatch problem without adding coupling capacitor complexities, the C-R2R DAC is used for the fine TSAR as shown in fig. 17. Here the back-end DAC is a ternary R2R structure which has a full-scale range that is not impacted by the coupling cap. Since the FITSAR is implemented differentially, there should be no net power though VCM and most of the transients should cancel out. A C-R DAC was shown in [8], however, the resistive part was implemented as a thermometer coded output which shifts the reference of the whole capacitive DAC, which isn't a power efficient solution. Also, a C-R2R DAC was shown in the context of a two-stage pipelined SAR [9], however that design was slit across pipelined stages, and this improves on that design by taking advantage of the ternary reference levels.

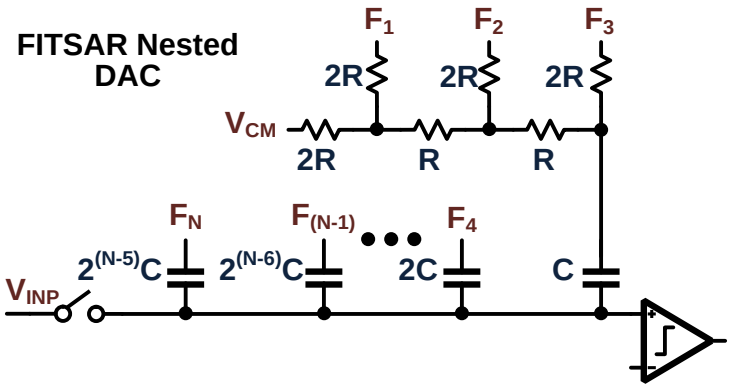

Figure 6.113: C-R2R DAC used in the FITSAR fine ADC for mismatch improvement

The three-level structure greatly reduces power consumption as compared to other 2-level R2R SAR DACs shown in fig. 18. This resistive DAC initially has all of its inputs tied to VCM as well meaning that it only burns power when the last few stages of the SAR arrive. The difference between the power curves of the 3-level and 2-level R2R DACs in the SAR configuration differ by a fixed offset because the switching events are actually the same. The only differences are that the 2-level R2R must have a test phase (like set-and-down) and will have a larger differential voltage when switching.

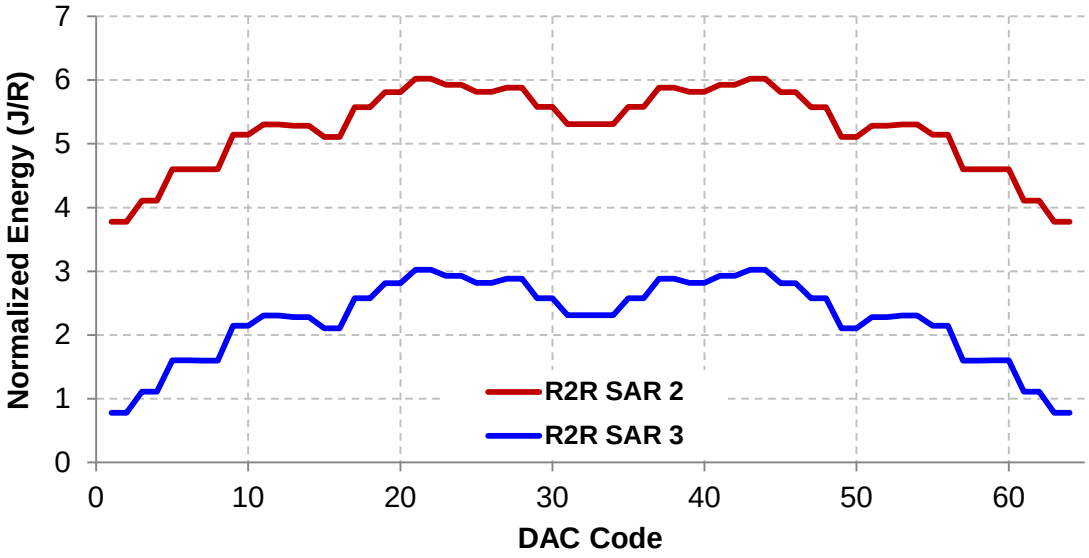

Figure 6.114: Normalized 2-level and 3-level R2R DAC energy vs. code in a SAR configuration

6.4 CMOS Circuit Implementation

The circuit implementation of the FITSAR has some similarities to the TSAR structure, but also some modifications based on the functional differences. The detailed implementation block diagram is shown in fig. 19. Here, the coarse and fine stages are separated, and while some of their respective functional blocks look similar, the block level implementation is different due to accuracy needs.

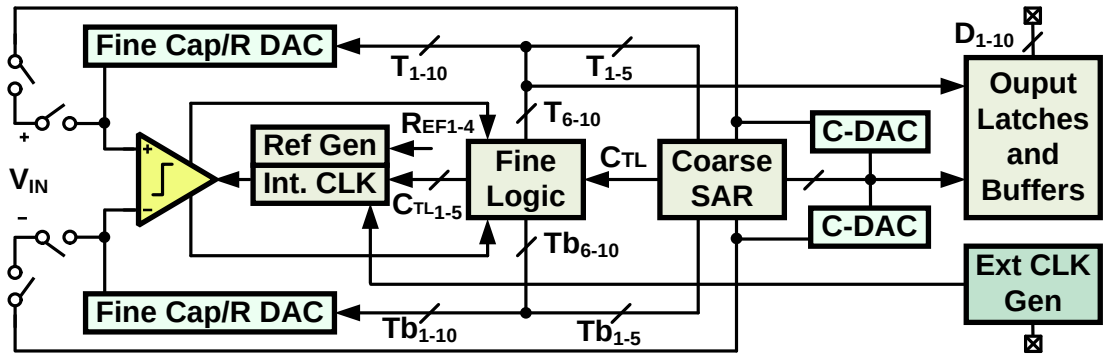

Figure 6.115: Detailed FITSAR implementation level block diagram

This section will describe in detail the quantizer, logic, and clocking changes needed to create a FITSAR prototype and the next chapter will detail many of the physical and layout changes required.

6.4.1 Quantizer Design

As mentioned before, the nesting operation of the FITSAR allows for decoupling between the quantizer units of the coarse and fine SAR stages. Because of this the fine comparator looks similar to that of the TSAR (due to the similar requirements), but the coarse comparator is a different architecture as shown in fig. 20. Here, one can see that the fine comparator is still a p-latch structure, but is scaled slightly smaller based on better transient simulations (less overdesign). This latch structure was once again chosen due to the high accuracy for relatively small input devices, at the cost of power consumption.

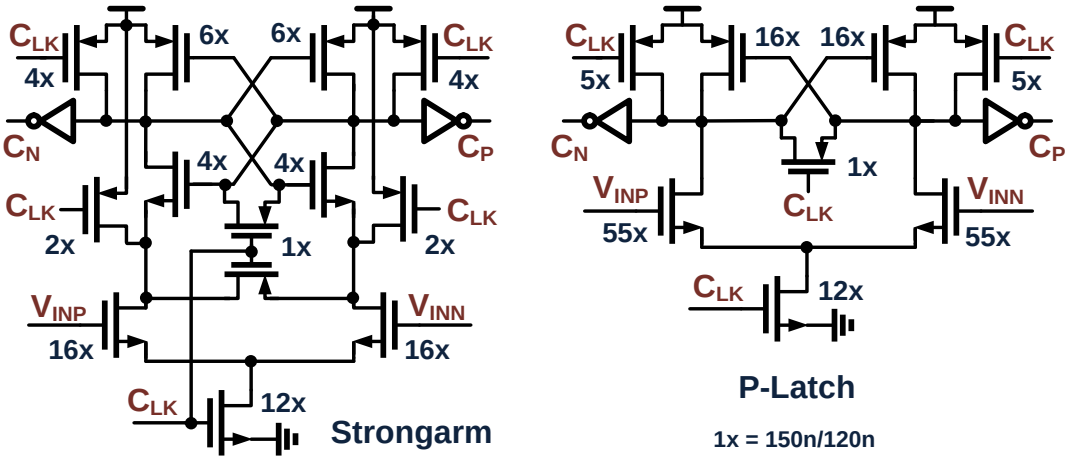

Figure 6.116: Coarse (strongarm, left) and fine (P-latch, right) comparators in the FITSAR quantizers

The other popular dynamic latch structure that is used in the coarse ADC is the strongarm comparator [10] shown in fig. 20. This structure has a worse noise performance, but has an extra NMOS internal latch, meaning that the latch and the input devices become more decoupled as the gain of the comparator increases over time. The net result of this is that the latch burns no static power, only dynamic, and operates faster because of the internal inverter-like gain. To see how the resolution, input device size, and power vary over the two structures, the input device size vs. resolution is plotted in fig. 21 and the energy vs. resolution is plotted in fig. 22.

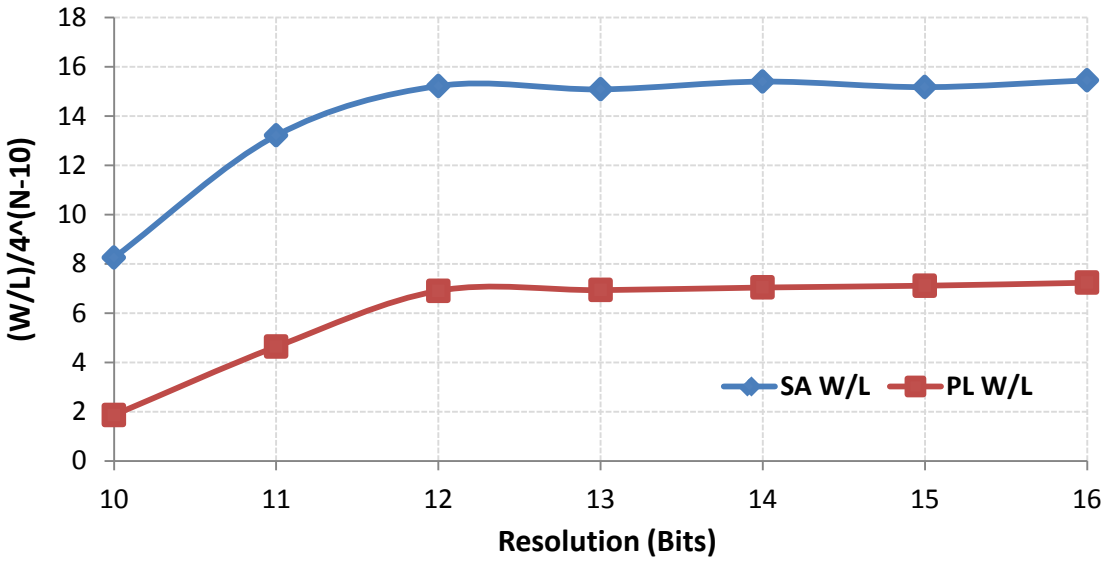

Figure 6.117: Normalized input device size vs. Resolution of the Strongarm and P-Latch comparators

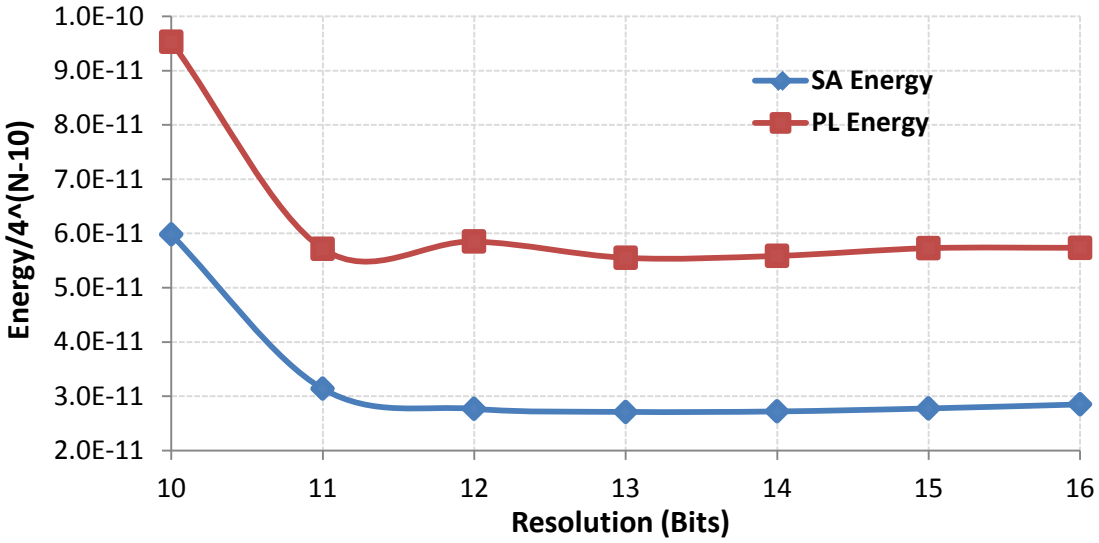

Figure 6.118: Normalized energy vs. Resolution for the Strongarm and P-Latch comparators

Here, the P-Latch and strongarm comparators have direct noise/energy tradeoffs above the 11b resolution mark, however below that things are not constant. It turns out that the 11b level is about where the devices sizes cannot scale further in the 0.13um CMOS process. This means that resolution is not an issue for either structure (both have larger devices then needed), but energy is still different. For that reason, the strongarm was chosen in the 6b case. The other interesting note is that the strongarm could also have been chosen for the fine case with about the same amount of power consumed, but the input devices would have been larger. This

implemented wasn't used because the input capacitance was already small from the DAC and on the edge of the thermal noise requirements, thus minimizing kickback though smaller comparator parasitic capacitors was important.

6.4.2 Coarse and Fine Logic (Handoff from coarse and fine, ref buffer)

Since both the fine and coarse SAR have structures that are more advanced than the basic SAR architecture, the logic needs to be changes slightly. Both logic units still have the same basic structure of a state machine, latches, and clocking control signals, however the architecture for the coarse EMCS and fine gated TSAR logic have some additional overhead.

Shown in fig. 23 is the coarse sub-ADC logic in the FITSAR. Here, the coarse comparator gets the inputs from the same source as the fine TSAR and those inputs {VGP and VGN} also feed to coarse binary weighted capacitive DACs. The comparator output feeds to a latch in the first cycle of the ADC, but in later cycles the latches all see the first determined bit, which represents the polarity of the input. The comparator output then acts to reset the previous latch if the output polarity is different than the first bit, indicating that the stage input is smaller than the optimal switching window value, or when the reset phase comes, as was shown in chapter 5 and is also muxed based on the initial polarity. The clock to the comparator comes from the clock generator but is gated by the reset phase and phase 7, which is the end of the coarse cycles. It was found though simulation, that is it somewhat helpful to send the data from the coarse ADC to the fine DAC 1 stage early. While this will slightly reduce feedback initialization benefits, it will allow more settling time on the fine stage DAC for reduced errors. This was implemented by having a separate latch set by phase 5 enable the coarse to fine transfer AND gates.

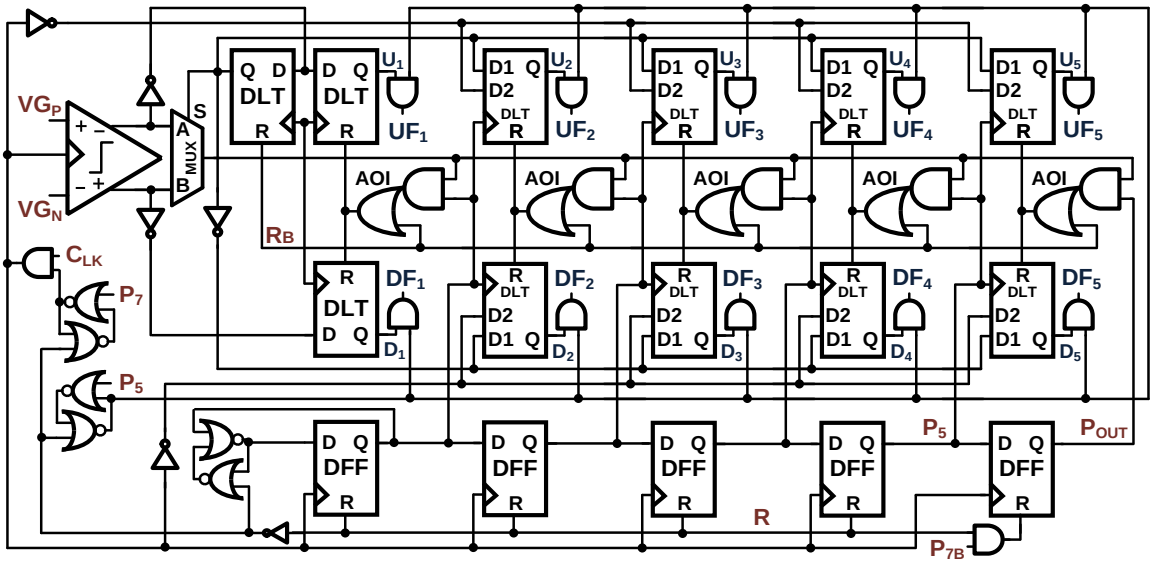

Figure 6.119: FITSAR Coarse ADC logic implementing a feedback initialized EMCS algorithm

Some of the logic design for the coarse ADC is shown in fig. 24. Here, the mux is fully digital to improve speed and digital gain (metastabilty reduction). The AND-OR-Invert (AOI) gate used to implement the resetting function is used to save logic in the ADC core and adds very little overhead to the EMCS structure. Finally, the latch structure here is different than in the ternary SAR in that there is a weak feedback gain to prevent latching errors and increase the effective BER of the system (which was seen occasionally to be a problem in simulation).

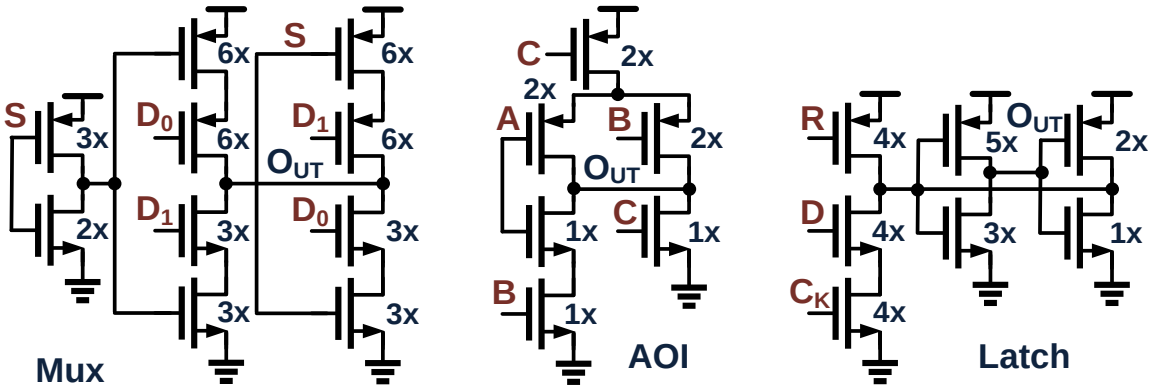

Figure 6.120: Logic cells transistor level design used in the FITSAR coarse ADC

The fine logic for the FITSAR is shown in fig. 25. Here, a similar state machine and latch combination was used as the TSAR with a few major changes. First, the stage skipping is not implemented with logic around the state machine but rather by simply gating the comparator

clock based on the latch outputs in the previous phase. This gating is generated by looking to see if an output code was generated (either a 1 or -1) in a given phase and using the phase clock, a gating signal is sent to the internal clock generator. The gating operation only takes places when there is not a reference level transition, and the gating circuit is also used to shut off the fine comparator when the coarse SAR is operating. The second major change is that the latches themselves act as the time comparator, with the falling edge of the main logic clock cutting off the comparator output. This is another reason some weak feedback was added to the latch shown in fig. 24 as more metastability reduction gain was desirable.

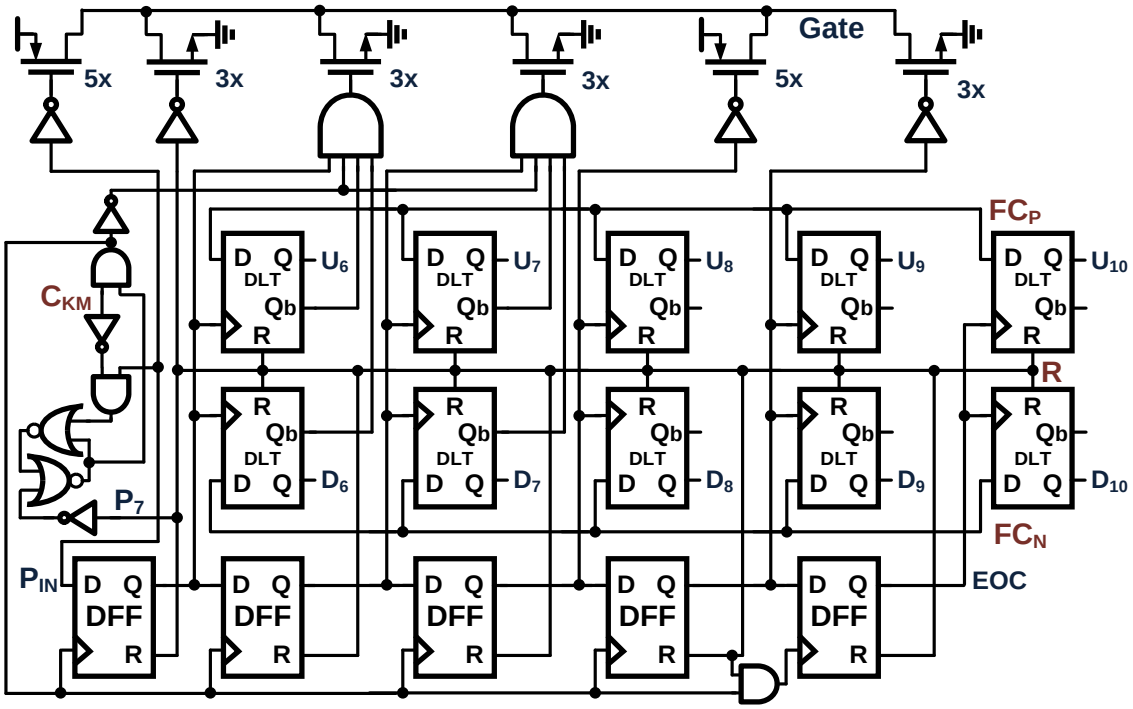

Figure 6.121: FITSAR Fine SAR logic unit with comparator gating

Since the fine logic operates only after the coarse logic has finished, the fine state machine is timed from PIN which is the last phase of the coarse state machine. The end of the state machine generates the end of conversion (EOC) signal which is sent to the external clock generator to switch into reset mode and to the internal clock generator to shut off the VCO.

6.4.3 Internal and External Clock Buffer Design

Clocking is a vital part of the FITSAR and like the TSAR, a system level clock generator is implemented to generate clock phases for the input switch, output drivers and enable the SAR, while an internal clock generator develops the phases for the SAR stage operation. The external

clock generator has the same structure as the TSAR and will not be discussed in detail. The only major change in the FITSAR to that structure is to use a static latch to hold the reset state rather than a dynamic latch, enabling wider clocking bandwidth.

The internal clock generator, shown in fig. 26, has some changes as only one phase is now needed for the fine logic due to the gating scheme (rather then skipping) and the modified reference generation. Here, the clock that outputs to all the logic units is generated by ANDing two of the internal VCO phases with enough spacing to allow the internal clock to be have nominally a 50% duty cycle. This duty cycle can then be modulated by the input time reference voltage (Ref) which lengthens or shortens the falling edge arrival time by starving every other inverter in the VCO loop. This means that as the duty cycle changes, the overall period also changes, but the reset time of each stage remains constant. To change the reset time, the starving of the other inverters can be controlled with TD. The clock for the comparator is generated from this logic clock, but is ANDed with the gating signal from the fine logic stage to save the needed comparator power. Also, the EOC and reset signals determine when the internal clock is to be shut off during the sampling phase of the SAR.

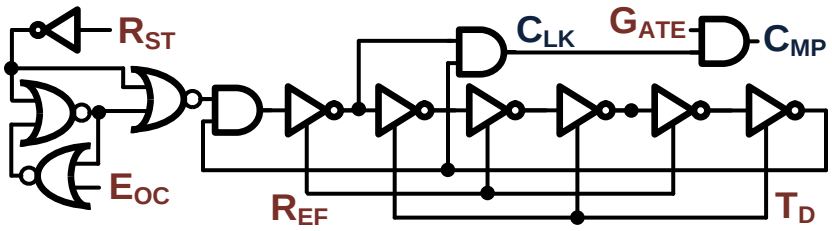

Figure 6.122: Internal clock generator with reset circuit

The modified reference buffer is shown in fig. 27. Here the reference switch controls are implemented with simple static logic which changes during the early part of the internal path reset cycles. This also prevents some of the glitching seen in the TSAR dynamic reference buffers. Some MOSCAP decoupling is added to the buffer inputs to reduce transient reference noise.

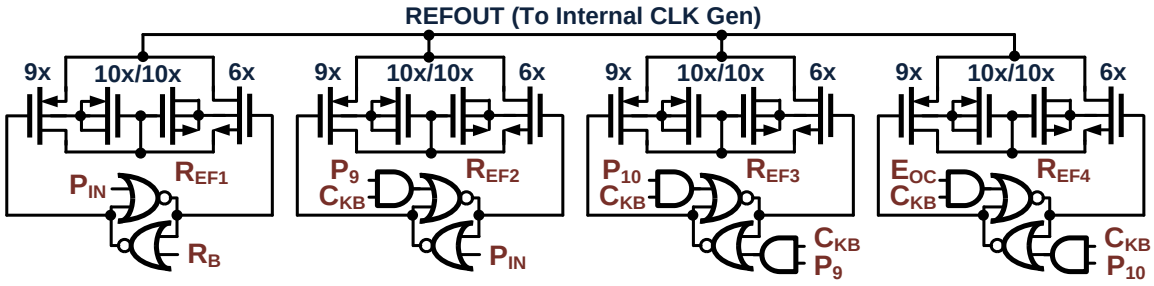

Figure 6.123: Reference mux for the internal clock generator

6.5 Physical Design

To prove the FITSAR concept and show a reference design, a prototype was created in 0.13u CMOS technology though National Semiconductor. The circuit features all the blocks shown in fig. 19 as well as ESD, decoupling, and a scan chain for testing different states. In this section the demonstrated layout will be shown for some critical blocks that have notable design tradeoffs.

6.5.1 Top Level Floorplan

The overall active die photo for the FITSAR is shown in fig. 28. Here, the active area is 0.06mm^2 and is mostly dominated by the fine capacitive and resistive DACs. The vertical lines to the left and right of the active area are for reference and supply routing while the horizontal lines across the chip are local supplies. Surrounding the chip are dummy patterns and filler/decoupling. Even though chip has added complexity in terms of logic and sub-ADC splitting, the total area is about the same as the TSAR due to the splitting of the DAC into capacitive and resistive components.

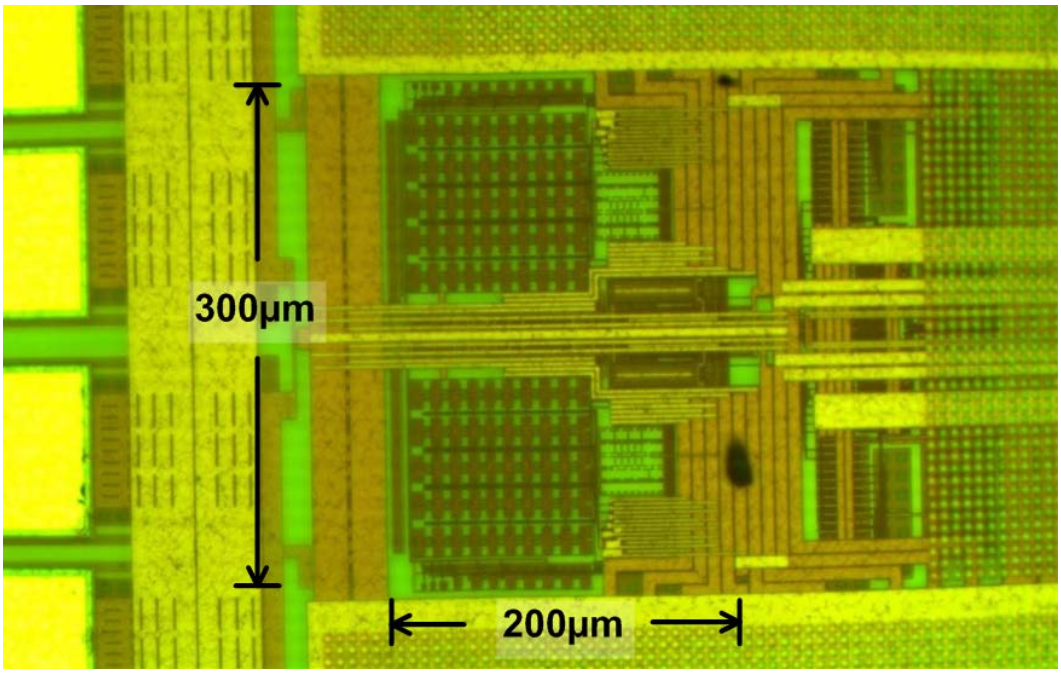

Figure 6.124: FITSAR die photo in 0.13u CMOS from National Semiconductor

A handy floorplan of where everything is located is shown in fig. 29 and care was taken to ensure the differential layout for matching. In the floorplan, one can see that the analog circuitry was again placed in between the larger DAC units to ensure the best possible analog matching, and the fine analog structures were placed closer to the input. The coarse SAR acts as a buffer between the digital and analog sides of the chip as its accuracy requirements are smaller than the fine SAR. Since the coarse ADC outputs tend to feed into the capacitive section of the fine DAC and the bandwidth requirements of that fine charging is not as stringent (since an extra cycle is given for the feedback initialization), thus, the fine DAC buffers are placed at the top and bottom of the chip. Finally, the left side of the chip has the on-chip output buffers, test scan chain, and trim logic.

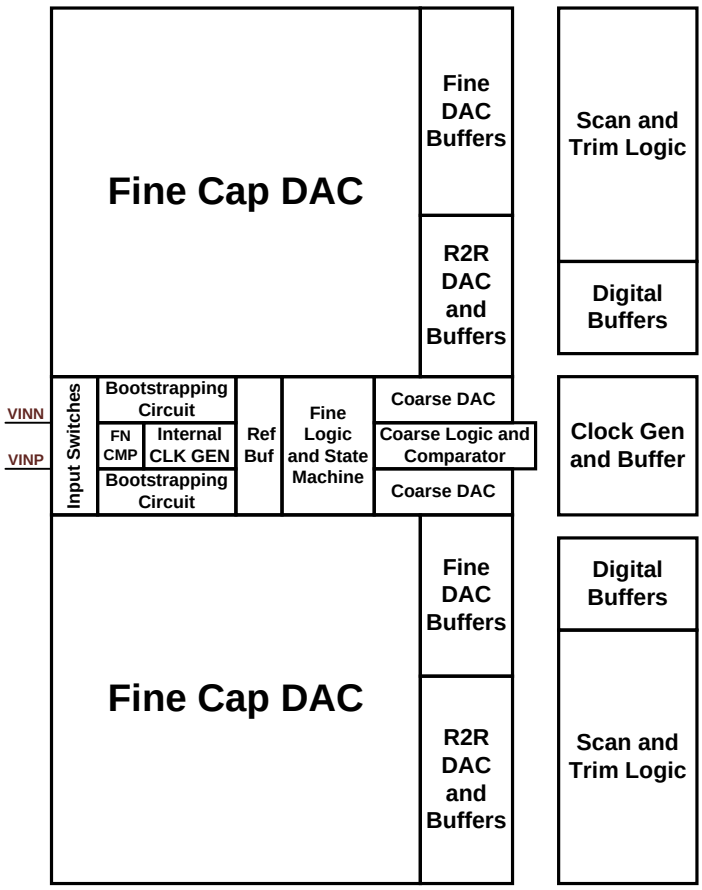

Figure 6.125: FITSAR full layout floorplan

6.5.2 Quantizer Layout

One of the critical blocks in the FITSAR is the comparator and the fine layout structure is shown in fig. 30 (green is poly, blue is metal 1, red is metal 2, purple is Nwell, and brown is composite). Here the large device on the left of the picture is the input switch and the larger input devices connect directly to that in one block of diffusion. The PMOS latch devices are outside (top and bottom) of the input devices, which works in this configuration due to the lack of cascode transistors. The bias device is then to the right of the input switch, allowing the comparator current to come from a low impedance supply rail.

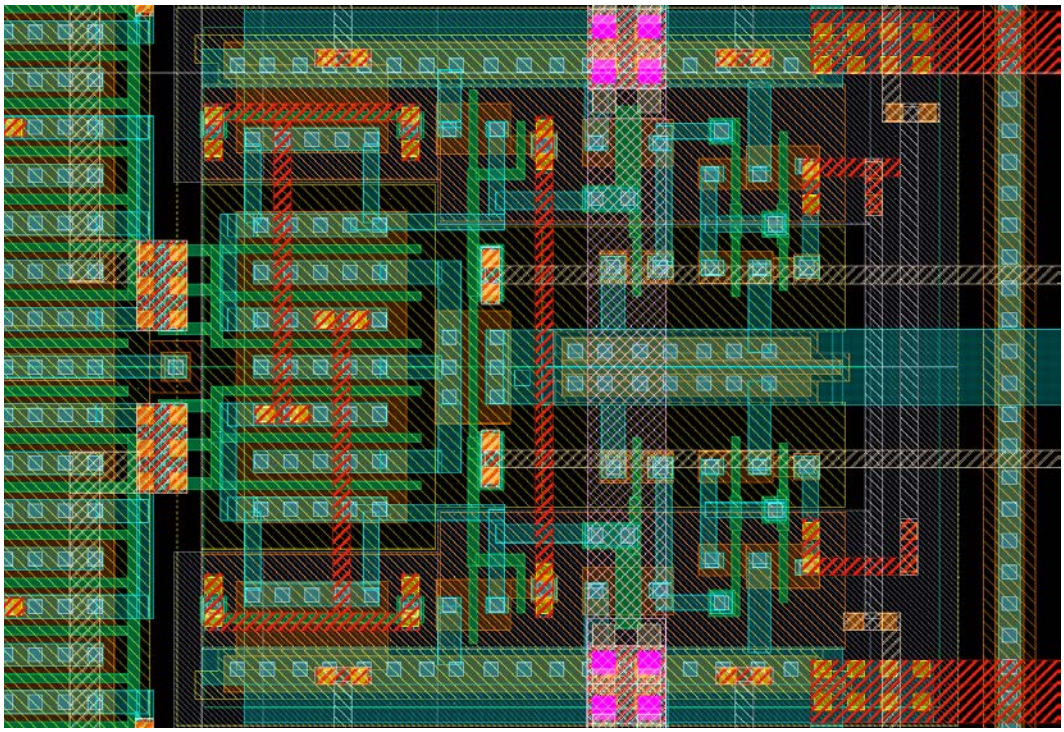

Figure 6.126: Fine quantizer layout diagram (top metal removed)

The full fine input path is shown in fig. 31 and the proximity of the fine comparator and input switch is seen. The input switch is placed as close as possible to the fine comparator to reduce parasitics on the fine virtual ground node and isolate the comparator from the rest of the digital circuitry. The bootstrapping for the switch is placed above and below the fine comparator while the bootstrap clock generator is in the logic block to the right of the comparator (along with the internal clock generator). Also, the input switch is divided into 4 sections. The center two pieces are large devices for the fine virtual ground node and on the outside are small devices feeding the coarse virtual ground and comparator, not shown in the picture.

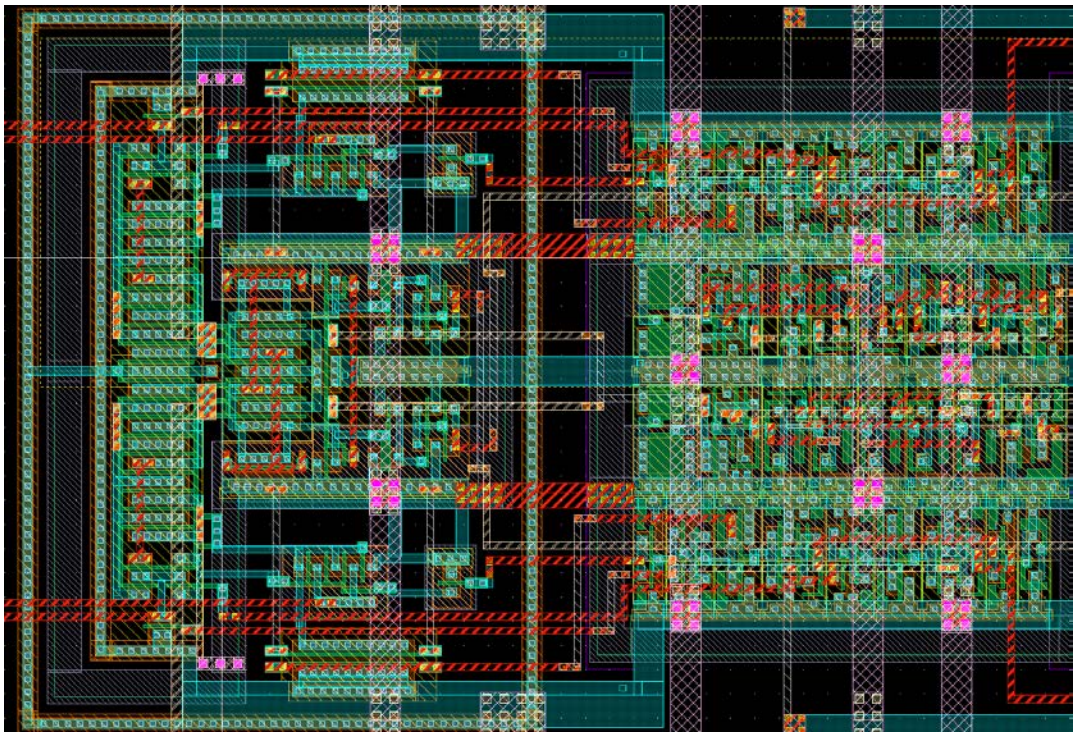

Figure 6.127: Analog input path layout (input switch, fine comparator, and internal clock generator)

6.5.3 Coarse and Fine DAC

The other major layout change from the TSAR to the FITSAR is in the feedback DACs used for the coarse and fine stages. In the coarse stage the feedback DAC was localized around the coarse ADC since there was no sharing of drivers between it and the fine structure as shown in fig. 32. A zoomed in version of the coarse DAC is shown in fig. 33. Here, unit single-finger flux caps of 4.15fF are used in a dual array form. The actually size is much larger than what is dictated by noise requirements and is more sized for matching and design rule needs. On the left of the DAC is a 2b calibration unit that can add or subtract some small extra capacitance to match the gain of the coarse and fine stage. More control is located on the fine capacitive DAC as well.

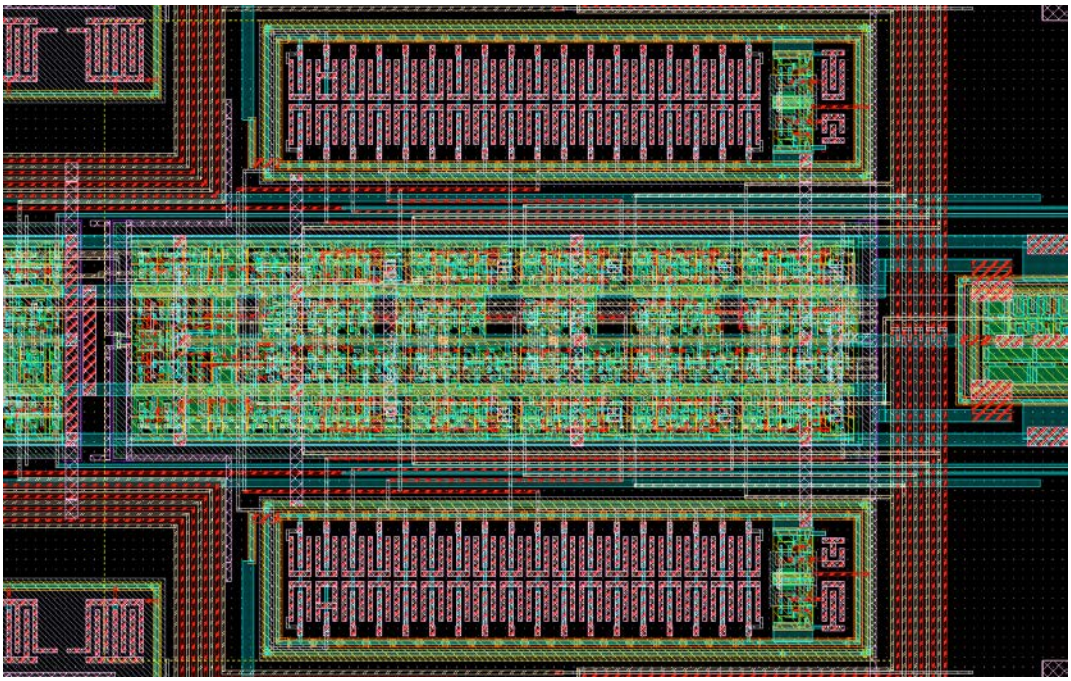

Figure 6.128: Coarse ADC with DACs on the outside

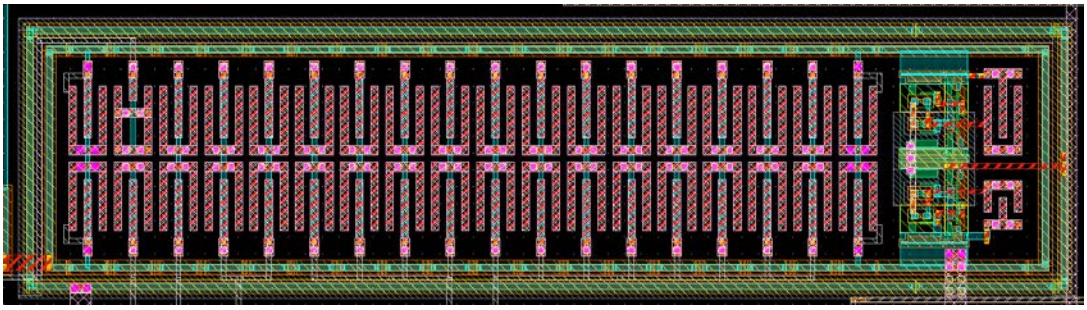

Figure 6.129: Enlarged Coarse ADC DAC and calibration

The fine DAC can be seen in fig. 28 and the capacitive part is similar to the TSAR with unit finger caps of 11.4fF. Here, the devices are slightly smaller due to the matching improvement from the split DAC and are sized for thermal noise requirements. The resistive half of the fine DAC is shown in fig. 34. Here, the elements are split into unit Nwell resistors of 2.5kΩ (R here is 5kΩ) with the first bit on the left and last on the right of the picture. A ring of dummy resistors surrounds the array for better matching along with a Ptap guard ring.

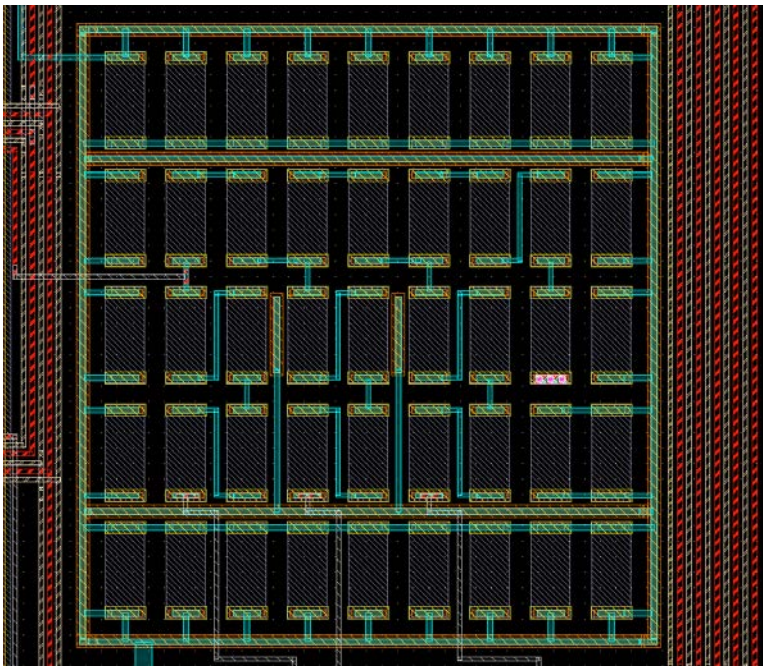

Figure 6.130: Fine resistive DAC half with unit Nwell elements

6.6 Test Setup and Measured Results

The FITSAR test setup for measuring results is virtually the same as in the TSAR with only small changes in the scan interface and reference generation. While at the time of press, measured results from the full chip were not available, transistor levels sims show an improvement in efficiency when compared to the TSAR. Fig. 35 has the transistor level FFT for a 50MHz master clock and 7MHz input while fig. 36 shows a transistor level comparison of the TSAR and FITSAR in with the FITSAR having an efficiency increase of about 2.5x (at 0.8V). Also, the TSAR simulations were slightly optimistic as they didn't include the parasitic capacitances that limited the fabricated energy efficiency in the end (the final TSAR device measured at an FOM of about 10 fJ/CS).

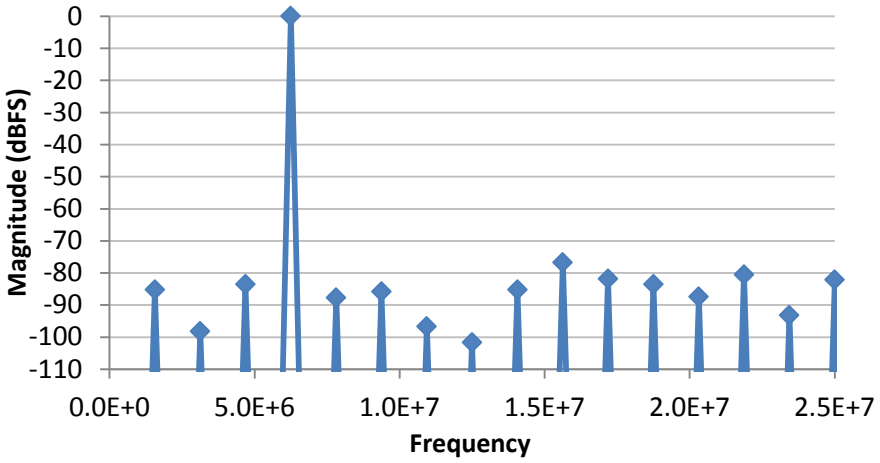

Figure 6.131: FITSAR FFT, 50MHz clock, 7MHz input, 11.65 ENOB

Spec/Date	April 15, 2010 TSAR	August 25, 2010 TSAR	April 3, 2012 FITSAR	April 3, 2012 FITSAR
ENOB	11.69	11.67	11.76	11.18
Frequency	62.5 MHz	62.5 MHz	50 MHz	10 MHz
Power	1.015 mW	778 uW	362 uW	32.8 uW
Process (VDD)	CMOS9T (1.8)	Jazz13 (1.2)	Optimos2 (1.2)	Optimos2 (0.8)
FOM	4.92 fJ/CS	3.82 fJ/CS	2.08 fJ/CS	1.41 fJ/CS

Figure 6.132: Transistor level comparison of FITSAR and TSAR efficiency

6.7 FITSAR Conclusions

The Feedback Initialized Ternary SAR was shown in the chapter to be a structure that improves the overall SAR ADC efficiency by using the TSAR structure where it is most effective (mid-resolution steps) and creating a sub-ADC made of the more efficient low-resolution EMCS SAR. By optimizing each stage for noise considerations, recoding the data from the coarse to the fine stages, and initializing the feedback operation in one single phase, a 61% percent DAC energy reduction was made and a 34% driver activity reduction was produced. A prototype demonstrated the performance with a FOM of 1.41fJ/CS in simulation and architectural

improvements that include a 3-level C-R2R split DAC, comparator gating, and distributed latch based time comparison.

6.8 Acknowledgements

Many people contributed to this work in terms of ideas, prototype assistance and critical feedback. Some of these include Manideep Gande, Hari Venkatram, Taehwan Oh, and Allen Waters.

7. THE TERNARY R2R DAC

In the previous sections, the quest for higher efficiency in the translation of analog signals into the digital domain was examined, however another major problem in interfacing with the real world is translating digital data back into analog waveforms. While this problem is not the central focus of this thesis, many of the ides used in the previous sections for ADCs can be applied to DACs, especially the ideas relating to the sub-DACs within ADC structures.

7.1 Digital to Analog Conversion

Digital to analog converters (DACs) are ubiquitous in our modern devices in order to translate digital data into real world signals. Often they consist of a few blocks as shown in fig. 1. Here a digital input (either externally delivered or from an SOC) is encoded for the DAC and latched. Then that data passes through a DAC unit to generate an analog voltage and then is buffered (and sometimes filtered) before being sent to the load. In some structures, such as delta-sigma DACs, the pre-encoding and post filtering are very important steps while less emphasis is placed on the DAC itself. On the other end of the spectrum, current source DACs often require no special encoding and little buffering or filtering. This work will focus on the R2R DAC which is a common low power DAC architecture based on element matching.

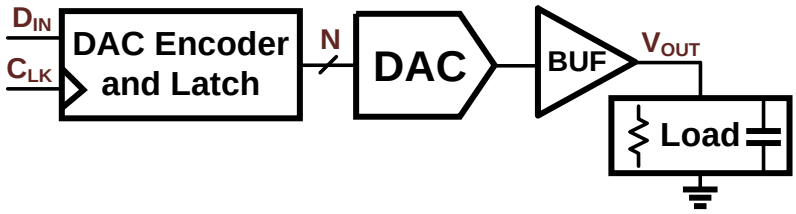

Figure 7.133: Typical DAC signal path structure

7.2 Traditional R2R DACS

Resistive DACs are common in many stand-alone DAC architectures, and can either be implemented in resistor string or R2R structures. The resistor string is essentially one large voltage divider with many elements, but the structure becomes difficult to use for high resolutions due to the thermometer nature which requires a large decoder and the sheer number of matched devices. The R2R DAC is more popular and has wide use in applications

ranging from sensors [1], digital waveform generation [2], and general purpose mid-speed and high accuracy DACs [3]. R2R circuits can also be used along with thermometer DACs to make segmented structures or inverted for current mode operation.

Typically, an R2R DAC is designed as shown in fig. 2, with a series of R and 2R segments and 2-level digital codes on the segment inputs. As the segments move away from the virtual ground node, the impact of the digital code on the output voltage decreases by a factor of 2 in each stage. The energy consumed in this DAC is then determined not by the magnitude of the output, but by the number of unit segments that are switched in opposite directions and their proximity to each other. For example the digital code 111000 would burn more static power than the 110000 code, but much less static DAC power then the code 101010 due to the interleaving of the supply and ground connected resistive segments. Also, connecting this DAC differentially will burn on average, double the power.

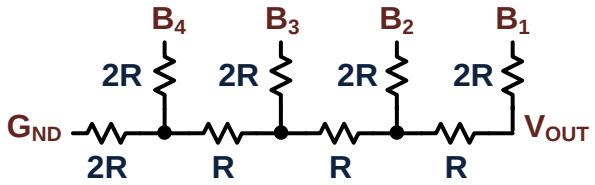

Figure 7.134: Traditional 4b binary R2R DAC

7.3 Ternary R2R DACs

One alternative to the traditional binary R2R structure for improved power consumption in differential operation is the ternary R2R DAC shown in fig. 3, which has a similar three level reference selection to [4] and [5]. Here, each digital input to the DAC can take a level of the set {0, V_{CM}, V_{DD}} whereas the binary DAC could only take the levels {0, V_{DD}}. The implication is then that by appropriately selecting when to use the V_{CM} level in the DAC, the energy of the overall structure can be reduced.

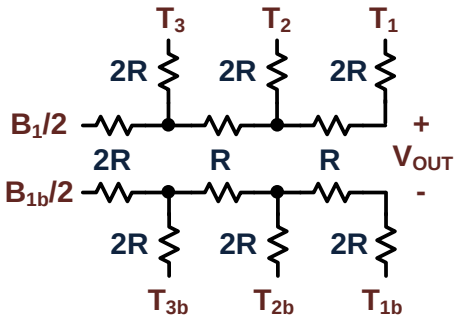

Figure 7.135: Proposed 4b Ternary R2R DAC Structure

To determine the optimal three-level switching operation of this structure, we should make a couple observations. First, the lowest power DAC coding is when the inputs are all the same code, either all VDD, GND, or VCM. Secondly, when current flows into VCM on one side of the DAC, it is also flowing out on the other differential side. Thus, the optimal coding should maximize the time that VCM is connected to a segment of the DAC (minimizing the number of supply connections). To do this we need a binary to ternary coding shown in fig. 4. This coding operation is implementing the following logical function:

$$T_N = B_1 \square B_{N+1} \tag{3.68}$$

The function is ANDing the first and current digital binary code to determine the optimal ternary DAC level. Notice that this operation does not change the output voltage of the final conversion except for adding an LSB/2 offset to the positive and negative codes. This can be corrected for by adding that offset back (B1/2) to the R2R as shown in fig. 3. Also, this coding scheme reduces one of the total number of stages in the R2R by replacing the information from the first binary bit by the direction of charging.

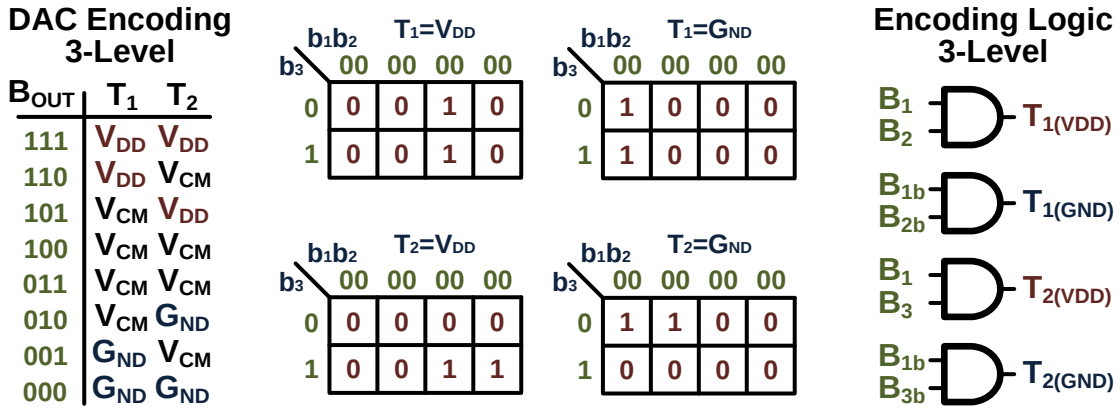

Figure 7.136: Encoding truth table (left), Karnaugh maps (center), and logic for the ternary 3b DAC

7.4 Modified 2-level DAC

In the previous section, the power consumption of the traditional R2R DAC was reduced by adding a middle code to reduce the effect of alternating supply referenced codes on the binary DAC inputs. This same effect can be emulated with only 2 levels differentially as shown in fig. 5. Here, assuming the DAC is fully balanced around the middle of the supply, the VCM switching events can be replaced by simply shorting the two sides of the respective R2R stages together. To ensure the balancing and maintain only 2 reference levels, the binary first bit and its inverse should be used on the ends of the DAC. This results in a 2 LSB jump when the input transitions from a code with "1" as the first binary bit to a code with "0" as the first bit. To account for the missing middle code, a middle code can be generated by shorting the two outputs when the binary input is a "1" followed by all zeros (1000).

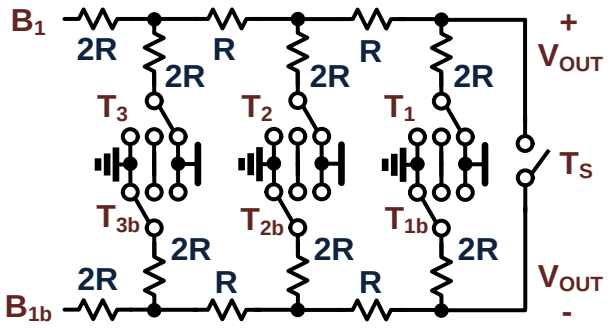

Figure 7.137: Modified 4b 2-level R2R DAC

The coding for the option of this DAC is also shown in fig. 6 where "SH" stands for short and "OP" stands for open. The coding is slightly more complicated to maintain the balanced nature, but can still be implemented with a simple adder and logic. Due to the coding and shorting, the

DAC can also reach one level more than the 3-level structure and operates as a mid-rise converter. Also, while this DAC outputs the same codes as the previous 3-level DAC (with LSB/2 offset), the settling time can be worse due to sampling transients on the input nodes for sharing events, but this could be minimized by connecting all the shoring nodes together (since they should only ideally be at a potential of V_{CM}).

DAC Encoding Mod 2-Level

B_{OUT}	T_1	T_2	T_S
111	V_{DD}	S_H	O_P
110	S_H	V_{DD}	O_P
101	S_H	S_H	O_P
100	S_H	S_H	S_H
011	S_H	S_H	O_P
010	S_H	G_{ND}	O_P
001	G_{ND}	S_H	O_P
000	G_{ND}	G_{ND}	O_P

Figure 7.138: Modified 2-level DAC encoding

7.5 DAC energy and Linearity Comparison

To understand the energy difference between the 2-level and 3-level R2R structures (here the modified 2 level has the same energy profile as the 3-level), the normalized static power per code is shown in fig. 7 for a 6b R2R differential example (ignoring switch resistance). The power of the ternary R2R is improved by nearly 79% for a uniform input and the power for each individual code is reduced. The peaks and troughs in both the plots correspond to the high power codes when there are many interleaved digital codes on the DAC inputs and the low power events when there is string of the same code across some portion of the DAC. The power in both cases does not go to zero when the inputs are all the same potential due to the current through the last R2R stage in the differential configuration.

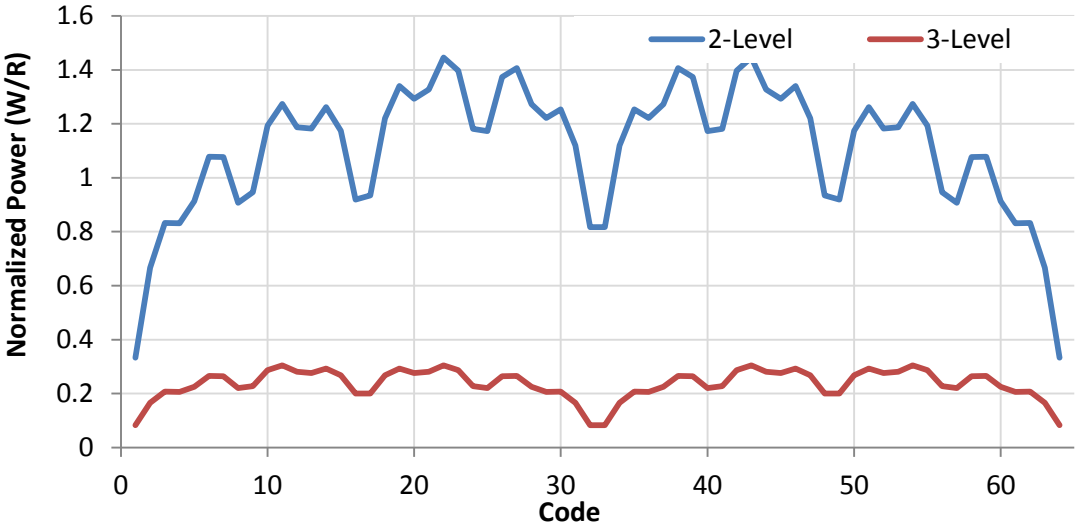

Figure 7.139: Normalized Power per Code for a 6b example differential 2-level and 3-level R2R DACs

Also the static linearity, measured by the DAC's INL, improves by a factor of 2 based on the addition of an extra reference level to the output. This is because in the binary R2R DAC, there could be a large DNL event (code jump) between the 1000… and 0111… middle codes since all of the resistors are changing their supply references between the 2 events. In the 3-level case though, the middle transition is when all the DAC inputs are V_{CM}, except the switching last stage, meaning the code jump due to mismatch in the resistive elements is small. This result is similar to that of 3-level capacitive DACs as in [6].

When implementing the 3-level structure, it should be mentioned that the net current from V_{CM} is always 0 due to the differential nature, thus much more relaxed regulators could be used for this reference (even the transient switching events should be complimentary). Additionally, the R2R structure could be implanted in a single end fashion with significant power savings, but the V_{CM} reference would then source and sink current.

7.6 R2R Conclusions

An R2R DAC using 3 digital input levels rather than 2 has been shown. The power of this proposed DAC is reduced by nearly 79% and the worst case static linearity due to device mismatches is improved by a factor of 2. The additional reference used in the design sources no net current differentially and logic for coding that DAC has been shown. Also, a modified 2-level

structure has been proposed that can emulate the energy reduction benefits of the 3-level R2R structure.

7.7 Acknowledgements

This work was funded in part by the Semiconductor Research Corporation (SRC, GRC Task ID #1836.097) and Texas Instruments.

8. CONCLUSIONS

The research work shown in this thesis focused on high efficiency ADC structures and examined ways to improve their performance. This section will have a summary of the work shown, outline some future ideas, and have some general concluding remarks.

8.1 SAR ADC and DAC Modification Summary

While there were a number of ideas presented in this thesis, they were linked together by their improvement of the overall efficiency and performance of the traditional SAR and DAC structures in terms of accuracy, speed, and power efficiency. The thesis ideas are summarized in table 1 showing the top-level contributions of the TSAR, EMCS, residue shaping, FITSAR, and 3-level R2R DAC.

Idea	Improvement	Accuracy	Speed	Energy
TSAR	**Time based extra quantizer level**	**Redundancy and calibration**	**Comparator time reduction**	**Skipping / Windowing**
EMCS	**Early Reset Algorithm**	**Linearity from 3 references**	**DAC size reduction (settling)**	**Improved Switching Algorithm**
Residue Shaping	**Optimization based on residue statistics**	**Extra bit of resolution**	**Reduced number of stages in SAR**	**Improved probability of later stage windowing**
FITSAR	**Split-recoded TSAR**	**Multi-stage redundancy and C-R2R DAC**	**Coarse speed enhancements**	**Feedback init., recoding, gating, comp. optimization**
3-Level R2R	**Three level R2R encoding**	**Improved linearity**	**NA**	**3-level encoding and modified 2-level**

Table 8.4: SAR ADC and DAC improvements outlined in this thesis

Over the course of the thesis, a few themes have emerged. The overarching theme of this work was to look for ways to utilize signals in the ADC that had previously been discarded and apply them to the improvement of the overall structure. This includes looking at the time in the TSAR and statistics in residue shaping. Another theme has been improving algorithms for the operation of multi-stage SARs both with and without this extra parasitic information utilization. A summary of some of the major switching algorithm improvements is shown in fig. 1 for a generic medium magnitude positive input. The EMCS SAR starts by not changing the algorithm

of the initial switching, but by introducing an early reset phase, saving energy. The TSAR then eliminates some of the DAC driver activity though the windowing provided by the time information. Finally recoding allows for all the fine DAC movements to be in a single direction and feedback initialization makes all these events happen in one phase. For a generic input, the energy is only about 1/3 of what it initially would have been in the MCS configuration.

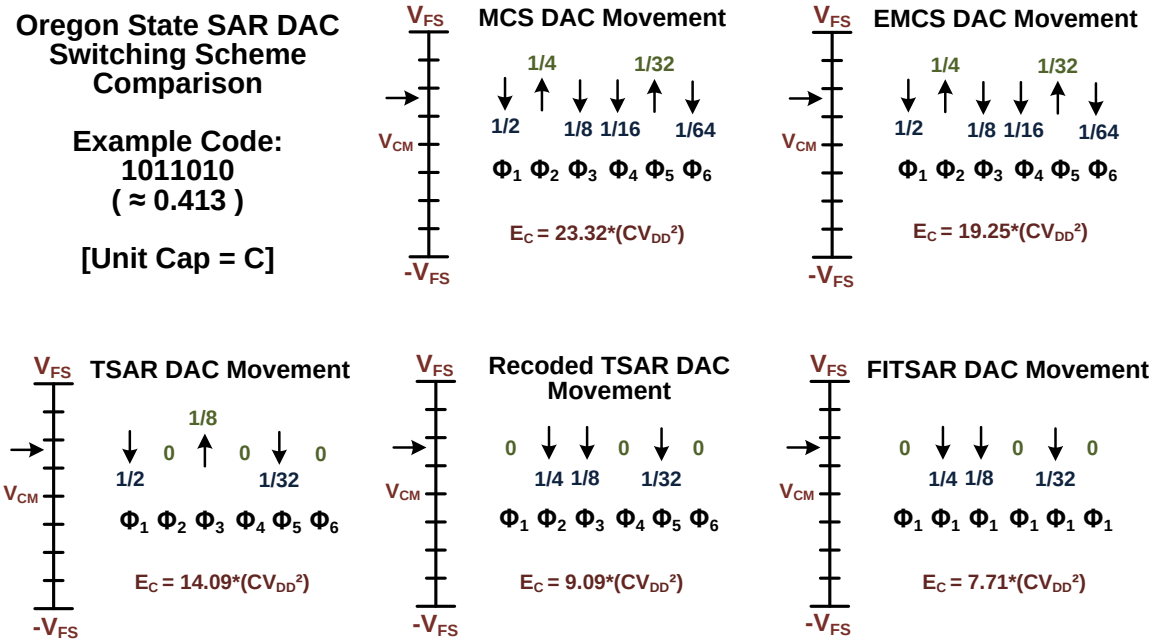

Figure 8.140: Proposed SAR DAC algorithm comparison and energy consumption

8.2 Future Work

While this thesis shown a number of interesting structural changes to the traditional SAR ADC, it has also sprouted a number of ideas that could be fruitful research projects later.

One class of ideas is to use the ternary quantizer structure in applications other than SARs. A potential application might be in a serial link receiver where the slicer is a set of dynamic comparators. When the channel disrupts the signal, the output code could be in error, but this will probably happen when the input to the receiver is small. By using the time comparator, the delay of the comparator could be used as a coarse detector of the channel code magnitude and could flag a bit as potentially wrong.

Another application of the ideas shown here would be in the creation of optimized multi-stage ADCs. While a number of papers have demonstrated multi-stage amplifier free

subranging ADCs, none has shown them with DAC recoding for improved stage to stage energy. One incarnation of this is shown in fig. 2 for a 1b per stage 12b structure. Here, recoding greatly reduces the overhead of having multiple DAC paths and the noise scaling of each stage allows for much better optimized comparators. Also, since here each 1b stage is fully decoupled, on the fly reconfigurability can be achieved, allowing an optimal FOM for logarithmic or split-resolution applications.

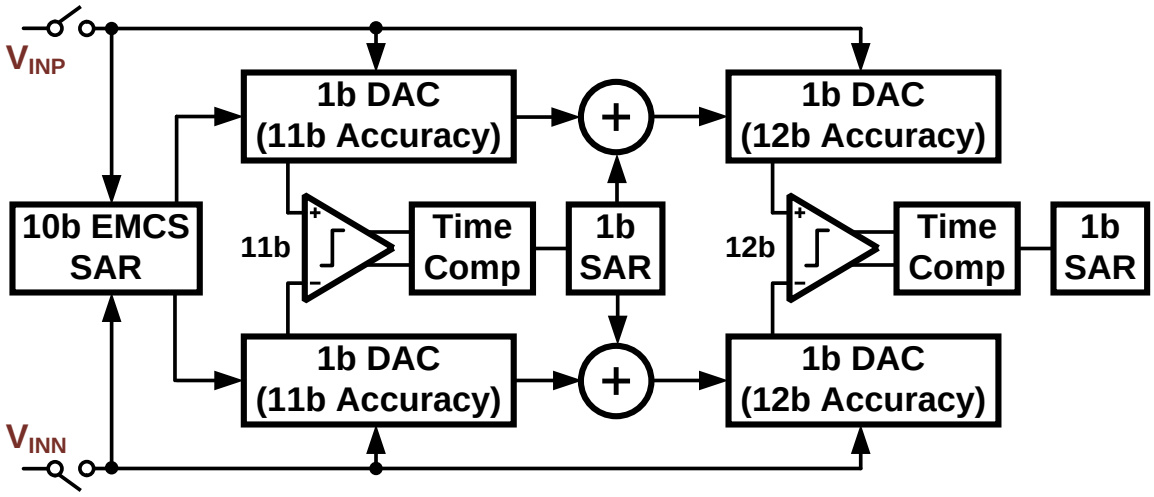

Figure 8.141: Multi-stage recoded and reconfigurable SAR ADC

A different path of work resulting from the ideas in this thesis is to improve the structure of the implemented SARs shown in this document. One possible improvement is in the noise and power tradeoffs in the SAR quantizer. Previously, the P-Latch and strongarm comparators were compared and it was found that for a given noise specification, the P-latch had smaller input devices (lower kickback) but the strongarm had lower energy. The main reason for the input device reduction is that in the P-latch, the input devices have some control over the output throughout the regeneration (even though it decreases with time) while the strongarm shuts off. However this shutting off and purely latching is what saves the strongarm energy. One potential improvement is to delay the shutting off of the inputs devices to the output until the latch has resolved to a point that the input devices can't impact the decision further. This is shown in fig. 3 with a delayed latch clock path for a strongarm structure. The normalized energy and input sized are shown form simulation for the three structures (the new device is labeled PLLP) in fig. 4.

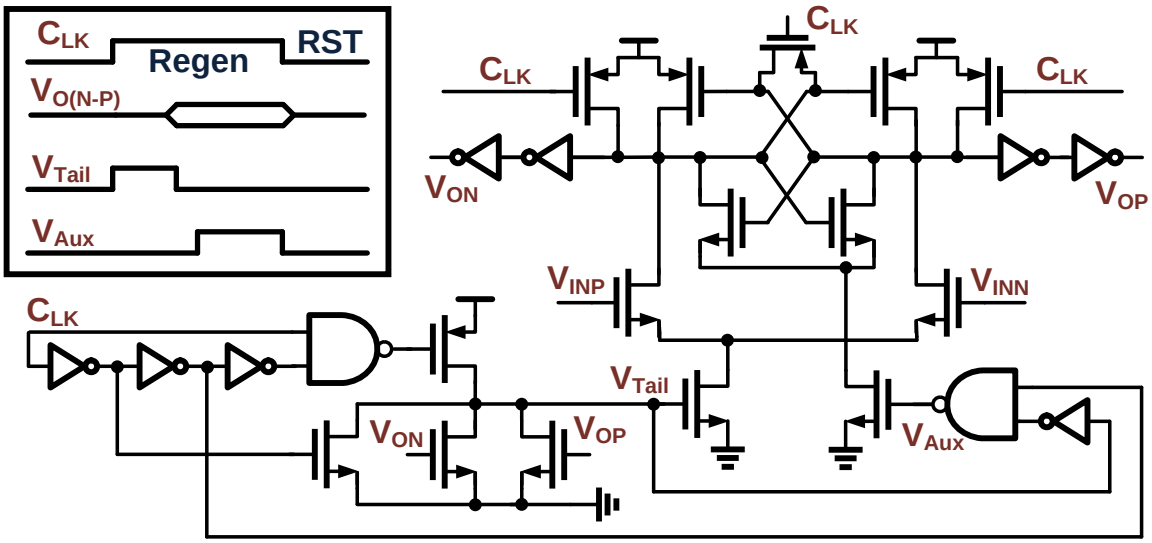

Figure 8.142: Proposed modified P-Latch low power structure with delayed input disabling

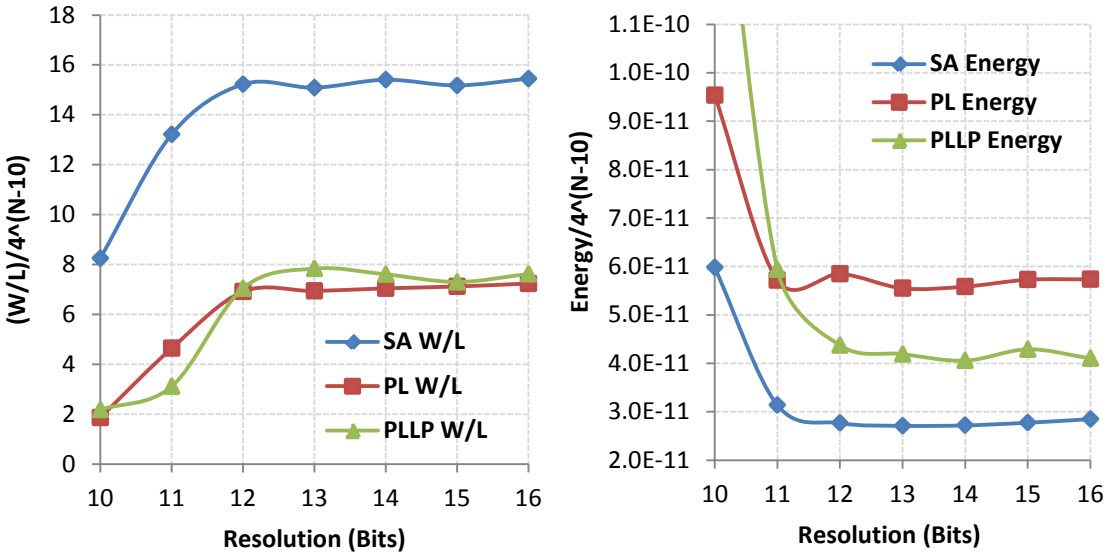

Figure 8.143: Normalized input size and energy for stongarm, p-latch, and low power structures

Other potential ideas exist as well such as combining these ideas with other SAR switching schemes, using the TSAR outputs as direct multi-valued logic, and perhaps even the data converters them to synthesized applications, but for now these will be left as exercises for the reader.

8.3 Conclusions

This thesis has demonstrated a number of innovations for nyquist ADCs and DACs, as well as demonstrated their effectiveness in prototype designs. Future work could also build upon these developments and as processes continue to improve, these ideas can be further adapted to the specific issues those devices present.

8.4 Acknowledgements

This thesis work was funded in part by the Semiconductor Research Corporation (SRC, GRC Task ID #1836.097), Texas Instruments, and CDADIC. Also, thanks for the help of all those in the grad group of Dr. Moon for their proofreading and idea assistance as well as Shannon Guerber.

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