AN ABSTRACT OF THE DISSERTATION OF

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Pavan Kumar Hanumolu

Desire for low-power, high performance computing has been at core of the symbiotic union between digital circuits and CMOS scaling. While digital circuit performance improves with device scaling, analog circuits have not gained these benefits. As a result, it has become necessary to leverage increased digital circuit performance to mitigate analog circuit deficiencies in nanometer scale CMOS in order to realize world class analog solutions.

In this thesis, both circuit and system enhancement techniques to improve performance of clock generators are discussed. The following techniques were developed: (1) A digital PLL that employs an adaptive and highly efficient way to cancel the effect of supply noise, (2) a supply regulated DPLL that uses low power regulator and improves supply noise rejection, (3) a digital multiplying DLL that obviates the need for high-resolution TDC while achieving sub-picosecond jitter and excellent supply noise immunity, and (4) a high resolution TDC based on a switched ring oscillator, are presented. Measured results obtained from the prototype chips are presented to illustrate the proposed design techniques.

Performance Enhancement Techniques for Low Power Digital Phase Locked Loops

by

Amr Elshazly

A DISSERTATION

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June 18, 2012

APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Director of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Amr Elshazly, Author

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PERFORMANCE ENHANCEMENT TECHNIQUES FOR LOW POWER DIGITAL PHASE LOCKED LOOPS

CHAPTER 1. INTRODUCTION

Recent developments in the integrated circuit (IC) fabrication technology joined with circuit and system design techniques have paved the way to implement high performance digital systems. With CMOS processes scaling, transistor sizes decrease and the supply voltage reduces. While digital circuit performance improves with device scaling: their level of performance (speed) increases while cost (power consumption and die area) decreases. On the other hand, analog circuits have not gained these benefits. As a result, it has become necessary to leverage increased digital circuit performance to mitigate analog circuit deficiencies in nanometer scale CMOS in order to realize world class analog solutions. This led to an increased demand of highly digital integrated circuits, where analog circuits can be replaced with digital alternative. This allows implementing high performance circuits with minimal power and area.

Complex systems-on-chip (SOC) is formed by integrating several ICs into the same chip. It contains analog, digital, mixed-signal, and radio-frequency (RF) building blocks, consisting of millions of transistors. Since there are many transistors switching at wide-spectrum of frequencies, the supply voltage suffers from dynamic variations. Depending on system components, the variations on the supply voltage can have frequencies ranging from DC to multi-gigahertz. These supply variations degrade the overall system performance. Moreover, the variations in the

process, voltage, and temperature (PVT) also affect the performance. For example, a state-of-the-art microprocessor runs at several gigahertz clock frequency, and should be able to operate in a wide range of operating conditions: process corners, different temperature (-40 to 125°C), and supply voltage variations (±10%). Due to these reasons, there is a great research interest to mitigate the effect of supply noise on the system performance.

The focus of our work is on performance enhancement techniques to implement frequency synthesizers for such large systems, with low jitter in the presence of supply noise, while being able to operate in different PVT conditions [1–4].

1.1 Frequency Synthesizers Applications

Highly digital clock generator architectures, most commonly implemented using digital phase-locked loops (DPLLs), are evolving as the preferred means for synthesizing on-chip clocks, allowing high levels of stability, accuracy, and integration [5–12]. They are widely employed in various applications such as cellular phones, wireless products, personal computers, laptops, televisions, gaming systems, and wireless transceivers, as displayed in Fig. 1.1.

The DPLL's digital loop filter can be reconfigured dynamically, therefore offering flexibility in setting their loop response and optimizing the locking behavior [10, 13]. These features becomes handy when they are integrated in large digital systems such as microprocessors. A generic block diagram of a leading edge cell-phone SOC is shown Fig. 1.2(a), and a state-of-the-art microprocessor SOC is depicted in Fig. 1.2(b). Clock generators (also known as: frequency synthesizers, and clock multipliers) are key building blocks in determining the overall system performance. They generate an on-chip high frequency clock from a low

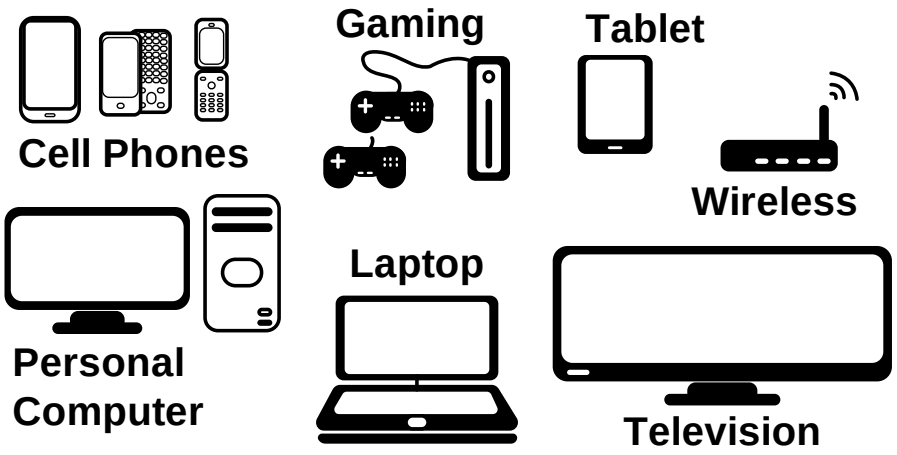

Figure 1.1: Applications of clock generator circuits.

frequency clock, typically provided by a crystal oscillator. These clock generators must generate clocks with low jitter while consuming minimum power. Because they operate in a noisy environments, they must be immune to supply noise. While there are many challenges in designing a clock generator, the focus of this research is to investigate system- and circuit-techniques that enable low jitter highly digital clock generator which mitigates supply noise.

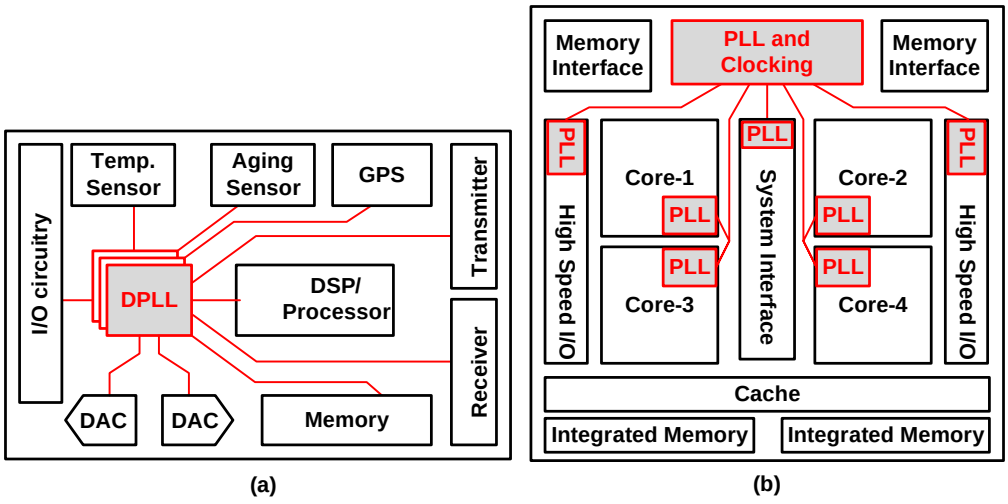

Figure 1.2: Block diagram of SOC chips employing PLLs.

1.2 Thesis Organization

Since the focus of this dissertation is on techniques to realize low-jitter digital clocking schemes, Chapter 2 illustrates the main issues of clock multipliers. The effect of clock jitter on system performance is introduced. The trade-offs and metrics of evaluating the performance of a clock multiplier are then discussed.

Chapter 3 explores the use of supply noise cancellation as an alternative to conventional suppression techniques implemented using supply-regulated architectures. A digital phase-locked loop (DPLL) that employs noise cancellation to mitigate performance degradation due to noise on the ring oscillator supply voltage is presented. A deterministic test signal based digital background calibration is used to accurately set the cancellation gain and thus achieve accurate cancellation under different process, voltage, temperature, and frequency conditions.

Chapter 4 discusses the design of a low power digital PLL that achieves a wide operating range. The proposed DPLL decouples the regulator bandwidth tradeoffs exist in conventional DPLLs, and employs a low power regulator to achieve wide range of supply noise rejection. After a brief review of the drawbacks of conventional DPLLs, a new architecture that achieves low power and high noise rejection is presented.

A highly-digital calibration-free digital multiplying delay-locked loop (DMDLL) that obviates the need for a high-resolution TDC is presented in Chapter 5. This architecture also achieves sub-picoseconds of jitter and a wide tracking range making it suitable for systems high performance applications.

Chapter 6 discusses a high resolution time-to-digital converter based on a switched ring oscillator (SRO-TDC). The proposed TDC shows improvement in power and performance with state-of-the-art designs.

CHAPTER 2. BACKGROUND

Highly digital clock generator architectures are evolving as the preferred means for synthesizing on-chip clocks [5–10, 12]. They are widely employed in various applications, and allow high levels of stability, accuracy, and integration. Digital clock multipliers are now commonly emerging as CMOS technology scales to lower process nodes. The digital loop filter of these multiplier can be reconfigured dynamically, therefore offering flexibility in setting their loop response and optimizing the locking behavior [10, 13]. Nowadays digital clock multipliers have demonstrated the ability of achieving a high performance clock multipliers that exceeds the existing analog implementations. Because they are integrated in a larger systems, the overall system performance is therefore determined by the performance of a clock multiplier. For high performance applications, such as high-speed serial links and high performance ADCs, the rms timing jitter is an essential issue. It is important to analyze the effects of clock jitter on the overall performance of such systems.

2.1 Clock Jitter

Jitter is the timing error/uncertainty of a clock source measured by its time-domain zero-crossings deviation from an ideal edge. The clock jitter is pictorially depicted in Fig. 2.1. It is typically represented as a peak-to-peak (pk-pk) or root mean square (rms) value, and can be evaluated by different types of jitter: long-term absolute jitter, period jitter, and cycle-to-cycle jitter. Absolute jitter, also

referred to as long-term jitter, is the difference in the clock edge compared to an ideal clock. Period jitter represents the deviation in the clock periods from the ideal period. Cycle-to-cycle jitter represents the difference between two consecutive periods of the output clock. These jitter sources are related, and can be derived from each other. Long-term absolute jitter represents the worst-case jitter and once measured the other jitter metrics can be evaluated. Therefore, in many applications, long-term jitter is the metric that mostly used and will be focused on here.

2.2 Clock Jitter and System Performance

Jitter contains two fundamental components: deterministic jitter (DJ) and random jitter (RJ). Random jitter represents timing noise with no evident pattern. Thus, RJ has a Gaussian probability distribution and usually characterized by its standard deviation value, expressed as a root-mean square (rms) quantity. Deterministic jitter is caused by events in the system and appears as timing noise with recognizable patterns. DJ is usually repeatable, persistent, and predictable. In addition, DJ is usually the result of dithering sources, data dependence patterns, layout mismatches, leakage, and power supply noise. DJ can be further classified into: periodic jitter, data-dependent jitter that is also known as inter-symbol interference(ISI), duty-cycle-distortion jitter, voltage supply noise, and any other timing jitter that is uncorrelated to the data.

The total jitter (TJ) is composed of both components described earlier, random and deterministic components. There are several techniques for estimating the total jitter. TJ can be found by measuring the long term jitter histogram of time error measurements compared with an ideal clock. It is usually a root-mean

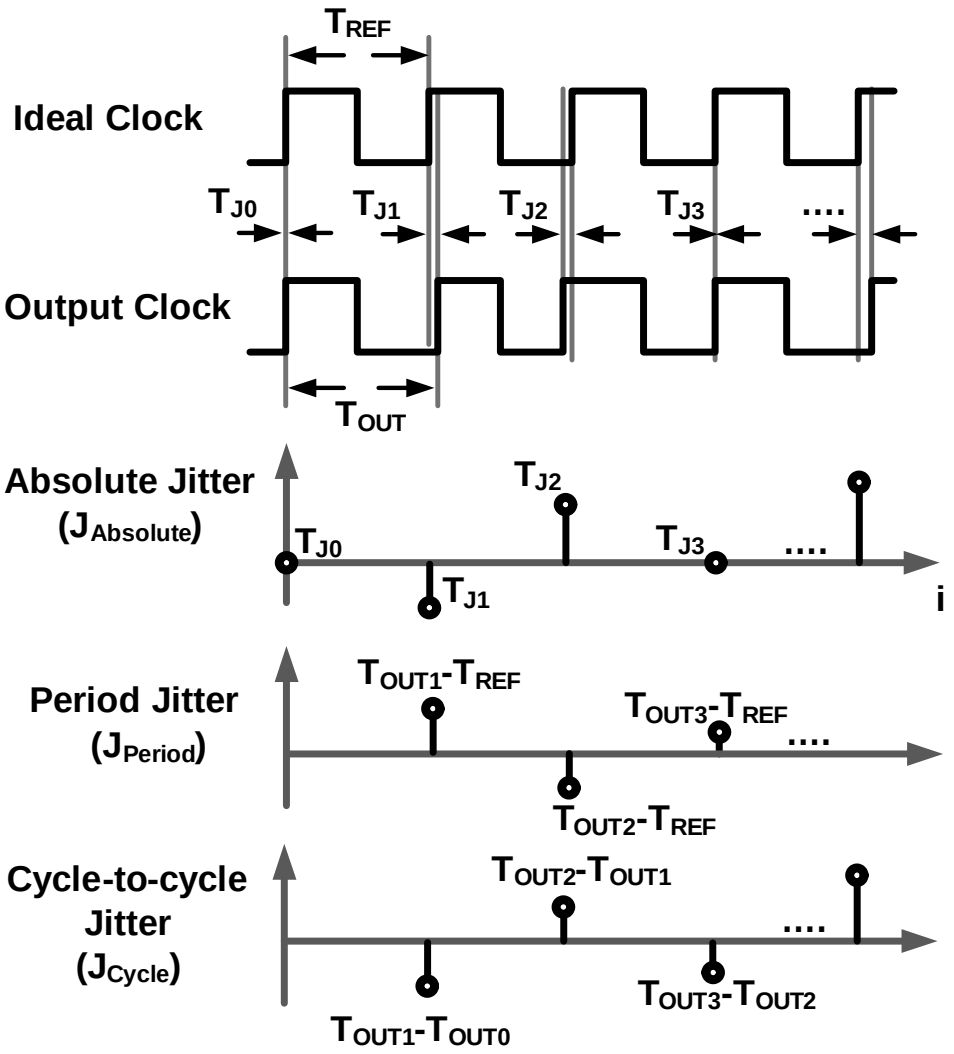

Figure 2.1: Timing diagram defining: long-term, period, and cycle-to-cycle jitter.

square (rms) and peak-to-peak (pp) value expressed in seconds (and sometimes in picoseconds) or fractions of a unit interval (UI). For example, 0.2 UI means that jitter is 20% of the sampling clock. Some other ways of finding the TJ is by resolving it into RJ and DJ components, then adding them together. To predict the overall performance of a system it is important to understand the types of jitter and their effects, and be to characterize and qualify all jitter components in

a system and determine the sources of jitter. To evaluate the impact on system performance, two examples illustrating the impact of clock jitter are presented in this section for: high-speed serial links, and high performance data converters.

2.2.1 Impact of Clock Jitter on High Speed Serial Links

A representative block diagram of a typical serial link is shown in Fig. 2.2. It consists of a transmitter, channel, and receiver. Clocking circuits designed for high-speed and high performance are used in the transmitter and receiver to transmit and receive data, respectively. Clock jitter distorts both the transmitted data and recovered data and severely affects the bit error rate (BER) of the link. Reducing the BER is the primary goal to design low-jitter clocks.

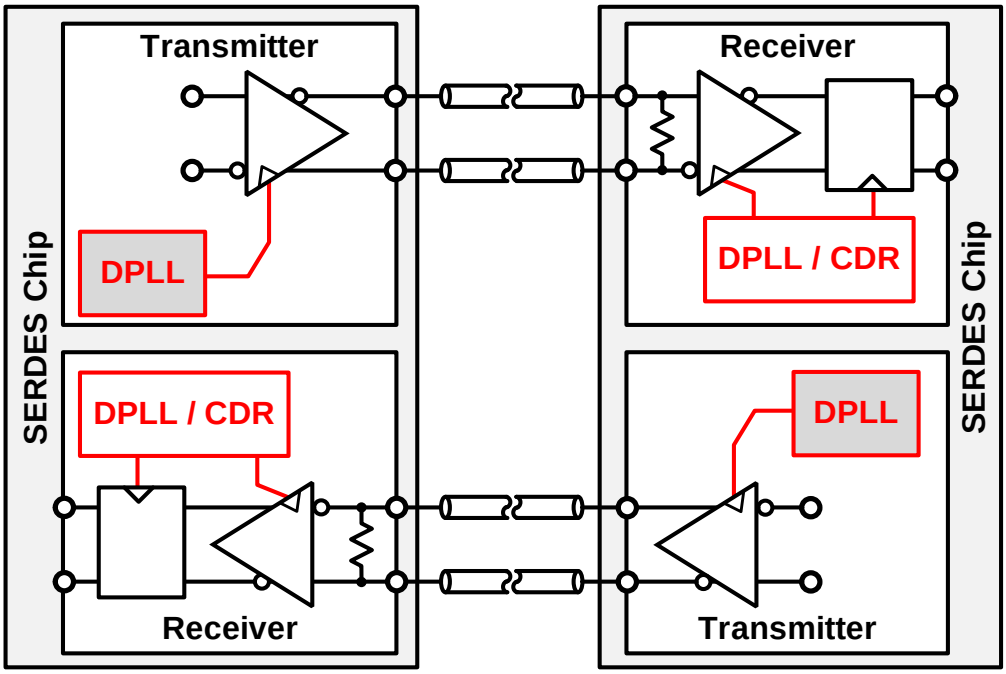

Figure 2.2: Block diagram of serial link.

The effect of clock jitter in serial links can be understood by looking at the

eye-diagram, as depicted in Fig. 2.3. The eye diagram is generated by plotting the time-domain signal and overlapping the traces for a certain number of clock periods. The clock jitter directly modulates the transmitted data, while jitter on the recovered clock results in sub-optimal sampling of the incoming data, both of which result in degraded BER. For example, the eye-diagram opening in time domain defines the resultant BER as shown in Fig. 2.3.

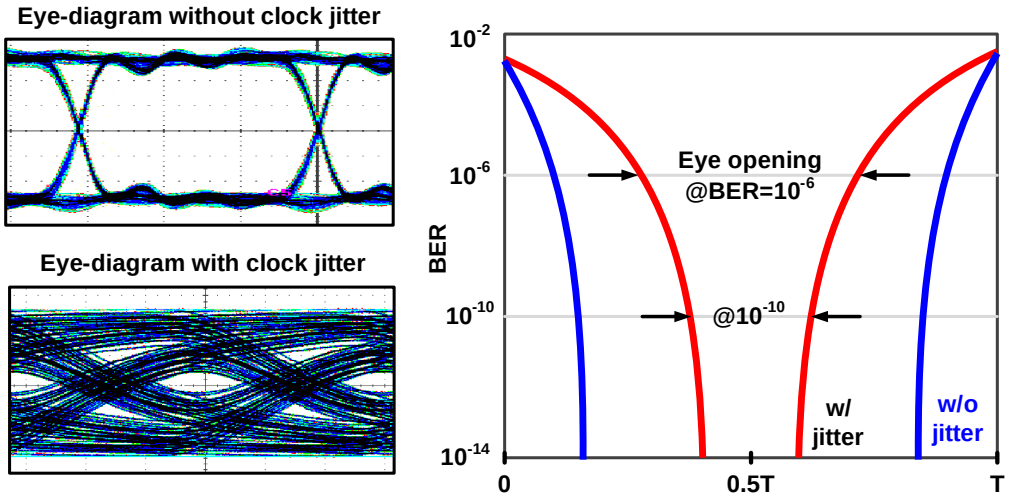

Figure 2.3: Impact of clock jitter on the link signals. Eye-diagram without and with jitter and the effect of jitter on BER.

2.2.2 Impact of Clock Jitter on High Performance Data Converters

Another example is high performance data converters, either high speeds (higher than 100MHz) or high resolution (better than 10 bits). For high performance data converters, the sampling clock jitter is critical to achieve high performance. A block diagram of a data converter module is illustrated in Fig. 2.4. It consists of a digital-to-analog converter (DAC), analog-to-digital converter (ADC), and DPLL clocking circuit.

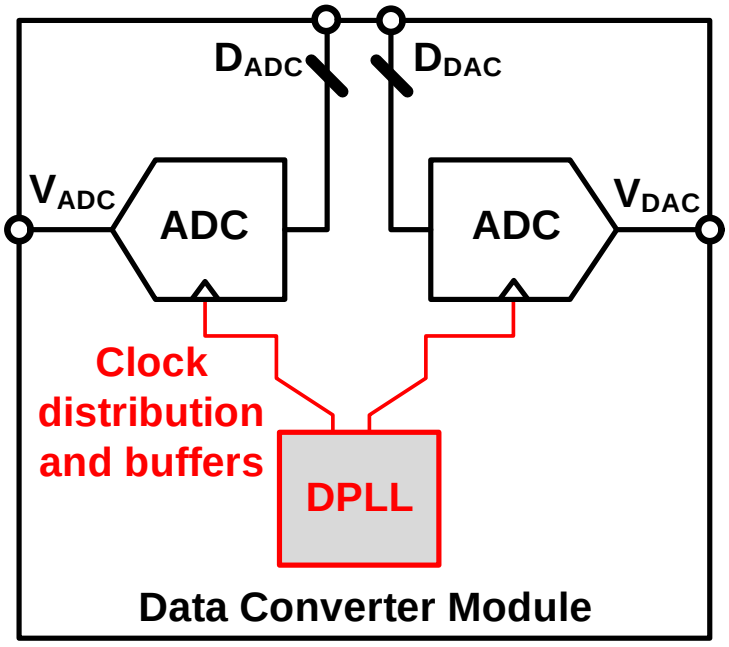

Figure 2.4: Block diagram of a data converter module.

Figure 2.5(a) shows the clock jitter relation with voltage error in a sampled ADC. For an ADC input with a time-varying signal V_{ADC}, the sampling time error of Δt results in a change in sampled voltage of ΔV, see Fig. 2.5(b). If we assume an input sinusoidal signal with amplitude of A and frequency of F_{IN}, and a long-term clock jitter with Gaussian noise source with a standard deviation of σ_J, one can derive the resulting signal-to-noise ratio (SNR) of the ADC for a full-scale sinusoidal input solely considering the long-term jitter of the sampling clock to be

$$SNR(dB) = 10log_{10}\left[\frac{\frac{A^2}{2}}{\frac{1}{2}\left(\frac{2\pi A}{T_{IN}}\right)^2}\right] = 20log_{10}\left(\frac{1}{2\pi F_{IN}\sigma_J}\right). \tag{2.1}$$

Similarly the effective number of bits can be calculated as

$$ENOB(bits) = \frac{SNR(dB) - 1.76}{6.02}. \tag{2.2}$$

Figure 2.5(b) displays the relationship between the rms long-term clock jitter, input frequency, and ENOB. For fixed clock jitter, as the input frequency increases, the ADC SNR/ENOB decreases. For high performance ADCs, sub-picosecond clock jitters are often required for high performance. For example, to achieve an SNR of 74dB with a 60MHz, full-scale input frequency requires long-term clock jitter of $0.5ps_{rms}$. When other sources exist, such as thermal and flicker noise, the jitter requirement is more stringent, so that the jitter due to the clock source does not degrade SNR significantly.

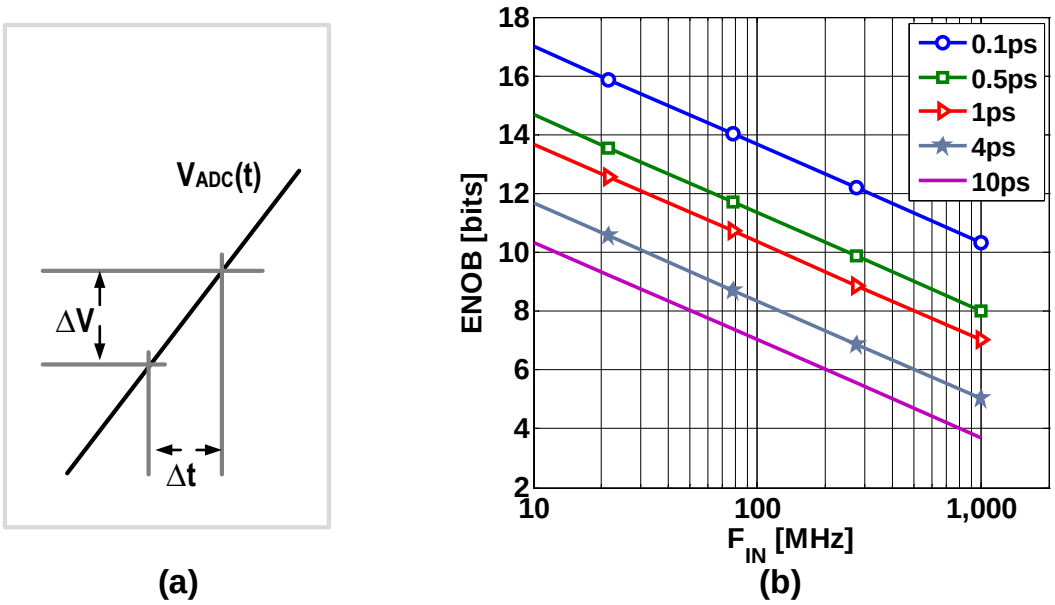

Figure 2.5: (a) Relation between sampling clock jitter and voltage error, and (b) maximum ENOB versus input frequency of an ideal ADC, for different values of rms long-term clock jitter.

In practice, clock sources can have deterministic jitter and spurs. Spurs in the data converter clock source can result in harmonic distortion at the output of the converter, thus degrading performance and reducing the data converter spurious free dynamic range (SFDR). Another source of error in ADC clocking is non-ideal clock skew between channels in time-interleaved ADCs.

2.3 System Clock Design

The clock system is usually classified into two distinct categories: clock generation and clock distribution. Depending on the system requirements, different clocking schemes can be chosen based the power consumption, jitter specification, area requirements, and number of clock phases needed in the system. In high-performance systems various phases of the clock can be overlapped in order to increase total system performance, such as clock and data recovery circuits, or non-overlapping phases in the case of data converters.

Clock generation begins on a system board, where the system reference clock is generated from a crystal oscillator. System clock is set to directly correspond to the speed of data busses on the system board, that is, from 100MHz, 250MHz, and higher in printed circuit boards (PCBs), to a few hundred MHz in specialized systems. However, the on-chip clocks operate at frequencies that are in the GHz range. In some cases, even when the on-board clock signal of the same frequency as the on-chip clock could be generated, the low-frequency system clock is first brought on-chip and then frequency multiplication is performed to achieve the desired on-chip clock rate. The main task of the clock generator is to generate the on-chip internal clock from the lower frequency external reference clock. There are two main categories of clock multiplication techniques: phase locked loops (PLLs) and delay locked loops (DLLs).

A block diagram of a classical charge pump phase locked loop (PLL) is shown in Fig. 2.6. It consists of a phase frequency detector (PFD), charge pump (CP),loop filter (LF), voltage-controlled oscillator (VCO) and feedback divider. The PD detects the phase difference between reference clock and feedback clock and generate an output that is proportional to the phase error. The CP output current is propor-

tional to the phase error based on the PFD up and down signals. The charge-pump combined with the loop filter generates the control voltage which derives the VCO towards phase and frequency lock.

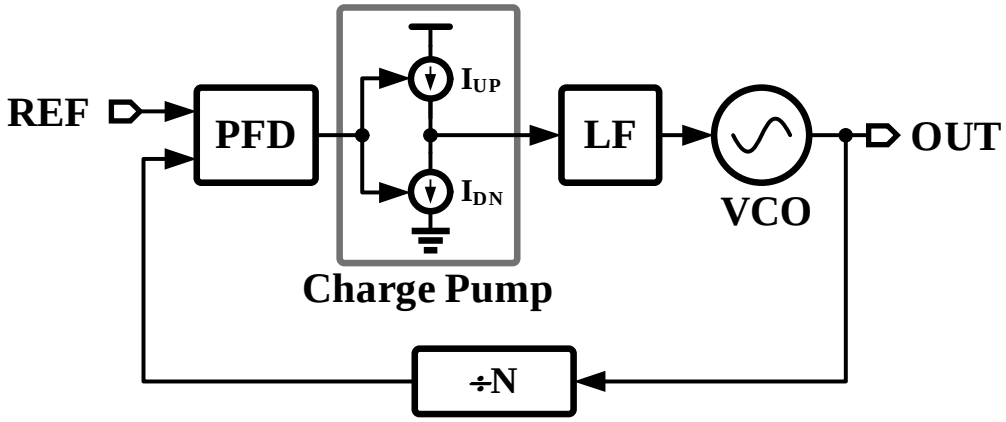

Figure 2.6: Phase locked loop (PLL) block diagram.

The other type of clock generation is delay-line based or delay-locked loop (DLL), as shown in Fig. 2.7. The VCO in a PLL is replaced by the voltage-controlled delay line (VCDL), which delays the external clock until the recovered clock becomes aligned with the reference clock, at which point the control voltage of the VCDL become steady and the loop stays in lock. Because the input and output clocks has the same frequency, only a phase detector (PD) is required for the case of DLL.

PLLs can perform frequency multiplication in easier ways than DLLs. Figure 2.8 shows a block diagram of DLL as clock multiplier, where the delay line output phases are combined to generate the multiplied frequency [14]. Typically, to guarantee an output clock with low jitter: (1) the reference clock is required to provide a 50% duty cycle, and (2) a minimal delay mismatch in the delay cells of the VCDL is needed. Such requirements are not necessarily required for a typical PLL. From noise performance standpoint, the VCO is the most critical compo-

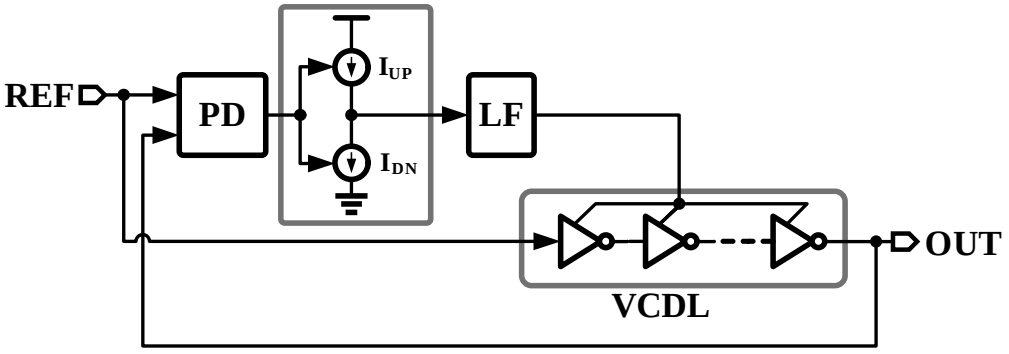

Figure 2.7: Delay locked loop (DLL) block diagram.

nents of the PLL, unless the system is poorly designed. The oscillator is built either as a ring oscillator topology, or an inductance-capacitance (LC) tank oscillator. Ring-oscillator-based VCOs require less area than LC tank oscillators, but the noise performance is worse than that of an LC-VCO.

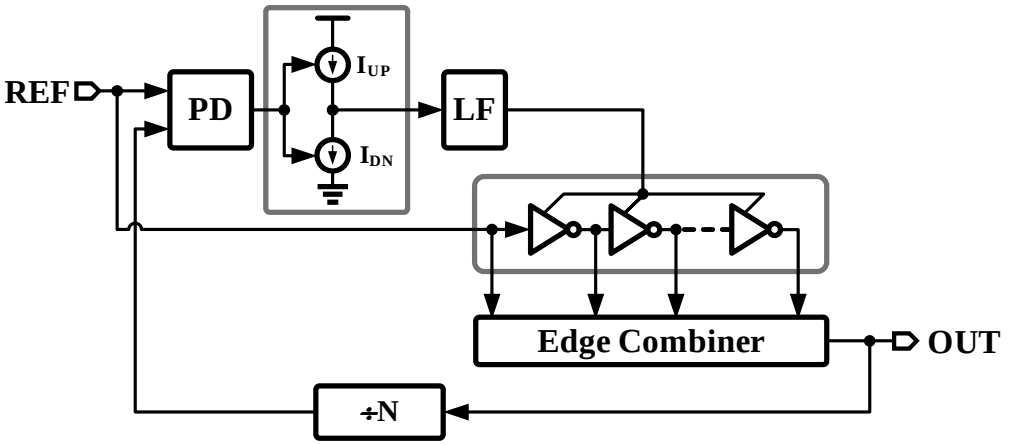

Figure 2.8: Block diagram of a DLL clock multiplier.

Multiplying delay-locked loops (MDLL) have been recently proposed for clock multiplication to overcome jitter accumulation in PLLs [15, 16]. It combines PLLs with MDLLs in a special configuration to reduce jitter accumulation. The block diagram of an MDLL, also are referred to as a recirculating DLL or realigned

PLL (RPLL), is shown in Fig. 2.9. It consists of a phase detector, loop filter, multiplexed ring oscillator, and selection logic.

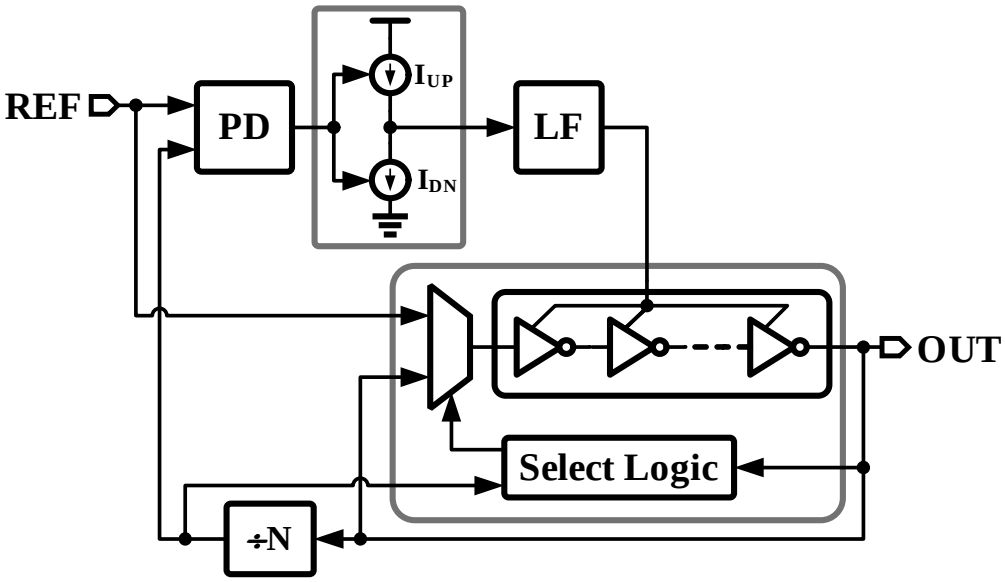

Figure 2.9: Block diagram of a multiplying DLL (MDLL).

Unlike in a PLL, the reference clock edge is periodically injected into the oscillator based on selection logic. The reference edge replaces the VCO edge every N cycles, where N is chosen to determine the multiplication ratio. The select logic generates a pulse during which the positive edge of the VCO is replaced by the positive edge of the reference clock (illustrated by timing diagrams in Fig. 2.10). Therefore, any jitter accumulation present at the VCO output will be reset accordingly. This resetting action makes the MDLL behave as a 1st order feedback system, thus making it unconditionally stable and also leads to superior noise suppression.

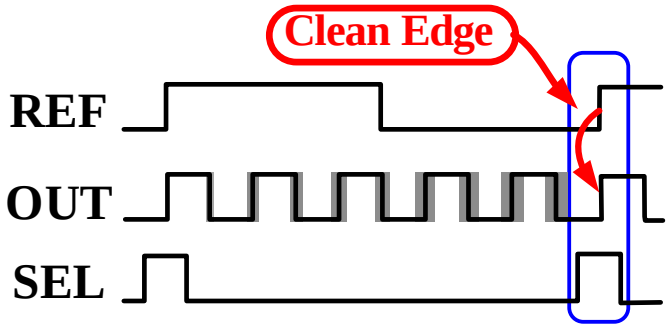

Figure 2.10: Timing diagram of an MDLL.

2.4 Supply Noise in Clock Multipliers

Clock multipliers are integrated into a large digital system. They must be immune to supply variations due to the switching of different building blocks. Additionally, the ring oscillator is susceptible to supply noise, which especially limits the jitter performance of a clock multiplier. The focus of our work is on mitigating supply noise in ring oscillator based DPLLs. Further, the ring oscillator is the most sensitive block, and the focus will be on system and circuit design techniques that desensitize the DCO to supply noise. The two commonly used techniques to mitigate supply noise are based on either suppression or cancellation.

Supply regulation techniques primarily focusing on suppressing the supply noise in the ring oscillator have been employed [17–20]. A general representation of a classical supply-regulated charge-pump PLL is depicted in Fig. 2.11. It consists of a 3-state phase-frequency detector (PFD), charge-pump (CP), low-pass loop filter, VCO, and feedback divider. The VCO control voltage is applied to its supply through a low-dropout regulator, depicted as a buffer in Fig. 2.11. The low-dropout regulator shields the VCO from supply noise and prevents it from

reaching the internal VCO supply at the expense of additional area and power, and reduced voltage headroom [21].

In practice, the regulator function is to completely isolate supply noise from the output. However, due to various circuit non-idealities such as the finite transistor output impedance and insufficient regulator bandwidth, it might fail to completely isolate the oscillator from supply noise, and some of these noise leak to the output of the clock multiplier as output jitter. While commonly used, the supply regulation approach has its drawbacks.

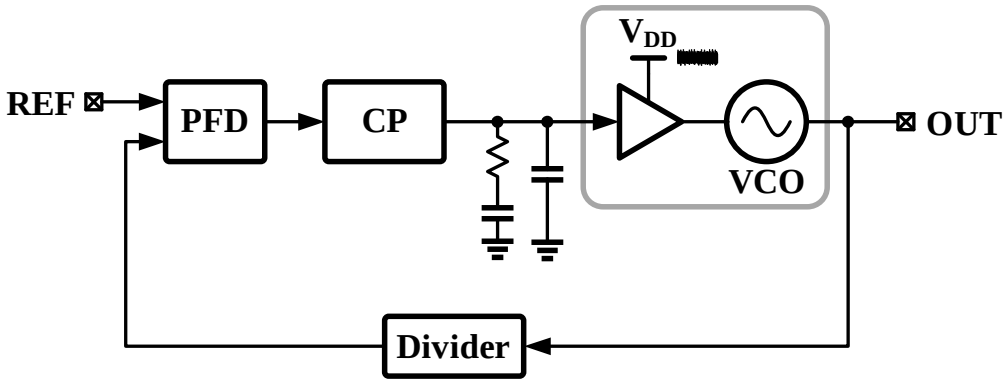

Figure 2.11: Supply regulated PLL block diagram.

The power supply noise rejection of the regulated-PLL greatly depends on the regulator to PLL bandwidth ratio (BWR). For reasonable suppression, the regulator bandwidth must be made much larger than the PLL bandwidth. For instance, for a modest 8dB of worst-case power supply noise rejection (PSNR), the regulator bandwidth must be fifty times the PLL bandwidth [17]. Designing the regulator for such a wide bandwidth increases power dissipation. On the other hand, because VCO phase noise is high-pass filtered by the feedback loop, increasing BWR by reducing the PLL bandwidth exacerbates jitter due to oscillator phase noise. Second, the dropout voltage of the regulator limits the maximum control voltage of the VCO and reduces its tuning range. A lower dropout voltage

increases the operating range of the VCO but compromises its PSNR. Finally, a large decoupling capacitor is needed in the design of all regulators [17, 18].

In view of these drawbacks, supply noise cancellation techniques were proposed as an alternative approach that eliminates the regulator while mitigating supply noise. This is pictorially depicted in Fig. 2.12 In contrast to supply regulation, supply noise cancellation techniques can operate at a lower supply voltage and have the potential to accomplish excellent supply noise immunity without using a large decoupling capacitor. However, in a practical implementation, the effectiveness of this approach is greatly reduced by process, voltage, and temperature variations. Several attempts have been already made to cancel the effect of supply noise in the VCO [22, 23]. In [22], the additional current induced by supply noise is cancelled at the output of the voltage-to-current (V-to-I) converter. The noise cancellation gain required, that best matches the V-to-I sensitivity was determined from transistor-level simulations. Ideally, with complete cancellation, the current-controlled oscillator frequency becomes independent of supply noise. However, in practice, process and temperature variations severely impact the VCO supply noise sensitivity[1]. Thus, using a fixed cancellation gain as in [22] is grossly sub-optimal. Therefore, it is necessary to calibrate the cancellation gain.

An analog foreground calibration was proposed in [23] to determine the optimal cancellation gain. While this technique successfully mitigates process dependence, it is susceptible to variations in operating conditions, because of its foreground nature. As illustrated later, the supply sensitivity greatly depends

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[1]The supply noise sensitivity is defined as the percentage change in the VCO oscillating frequency to the percentage change in the supply voltage, i.e., $\frac{\partial f_{VCO}(\%)}{\partial V_{DD}(\%)}$

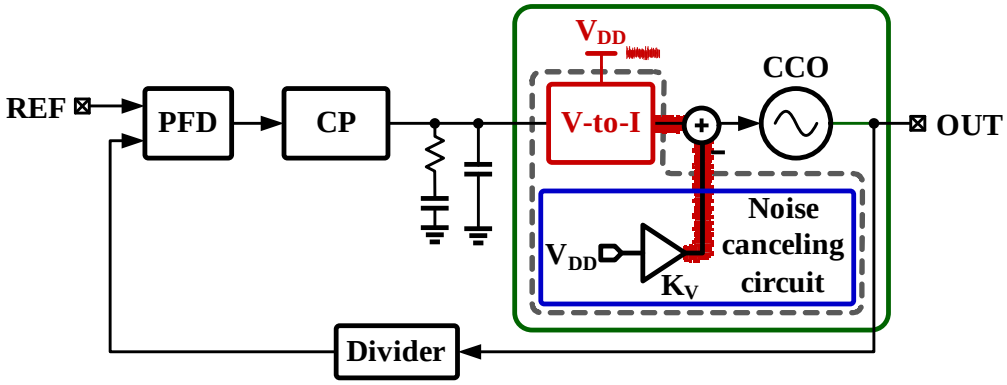


Figure 2.12: PLL block diagram with supply noise cancellation technique.

on the oscillation frequency and the supply voltage DC value. This dependence makes any foreground approach ineffective in a practical setting. Furthermore, this technique relies on accurately probing the analog control voltage, and hence it is susceptible to analog circuit imperfections. To overcome these drawbacks, we present a digital background calibration scheme that seeks to determine the optimal cancellation gain in the presence of process, voltage, temperature, and oscillation frequency variations.

2.5 Digital PLLs

Traditionally, analog charge-pump based PLLs (CP-PLLs) have been used for clock multiplication. However, the performance of CP-PLLs is severely limited by technology imposed constraints. First, transistor leakage in deep-submicron processes mandates the use of metal capacitors in place of high-density MOS capacitors, causing significant increase in the loop filter area. Second, current mismatch in the charge pump, exacerbated by the degraded transistor output impedance, causes large deterministic jitter. Third, the sensitivity of analog circuits to PVT

variations compromise the robustness of the PLL. Finally, short channel effects make it difficult to port the PLL from one process to another.

To overcome these drawbacks, digital PLLs (DPLLs) have recently emerged as an alternative to analog PLLs [5–10, 12]. The block diagram of a digital PLL (DPLL) is shown in Fig. 2.13.

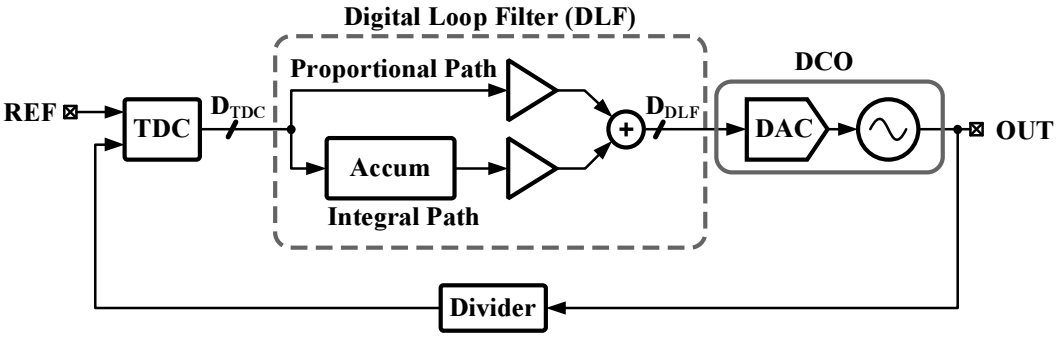


Figure 2.13: Block diagram of a digital PLL (DPLL).

It consists of a time-to-digital converter (TDC), digital loop filter (DLF), digitally-controlled oscillator (DCO), and feedback divider. The TDC generates a digital word proportional to the phase error between the reference clock (REF), and the feedback divider output. The DLF is a proportional-integral filter realizing the Type-II PLL response. A digital-to-analog converter (DAC) interfaces the DLF to the voltage controlled oscillator (VCO).

The DPLL offers several system- and circuit-level advantages. By obviating the need for a large loop filter capacitor and high performance charge-pump, DPLLs offer area savings; wide range of operating conditions; immunity to process, voltage, and temperature (PVT) variations; and easier scalability to newer processes. The ability to reconfigure the digital loop filter dynamically offers flexibility in setting the loop response and helps to optimize the locking behavior of the DPLL [10]. While these features are attractive, DPLLs suffer from unique band-

width, operating range, and noise tradeoffs that have limited its usage in high performance applications. Conflicting bandwidth requirements to simultaneously suppress TDC quantization error and oscillator phase noise mandate low DPLL bandwidth and a low phase noise oscillator to minimize jitter [12].

Conventional TDCs quantize the phase error in steps of an inverter delay, and consequently its resolution is limited to the minimum achievable inverter delay in a given process. For example, in a 90nm CMOS processes, the TDC step size is about 20ps. This rather poor resolution manifests itself as phase-quantization error which, if left unfiltered, appears as jitter at the DPLL output. Further, this TDC also leads to a bang-bang behavior of the loop, thus making it susceptible to dithering jitter due to excess loop delay. Also required in a high performance DPLL is a high resolution DCO. The finite resolution of the embedded DAC inside the DCO adds quantization noise that appears as DCO frequency error. Also due to the bang-bang behavior of the TDC at zero phase error, the steady state of the DPLL is a bounded limit cycle wherein the oscillator is dithered between two discrete frequencies. As a consequence, jitter accumulates at a rate proportional to the DCO frequency resolution.

The tradeoff between DCO resolution and tuning range is a classical limitation in a DPLL. Smaller DCO frequency step size is necessary for minimizing output jitter, while a larger step size widens the DCO tuning range and extends the DPLL operating range. For instance, with a given DAC resolution of L+1 bits and a required frequency resolution of ΔF, the DCO tuning range is limited to $\pm 2^{L} \times \Delta F$. A wider tuning range comes only at the expense of large frequency quantization error. The resolution versus tuning range tradeoff can be alleviated by using a higher resolution DAC. However, the design of such a DAC introduces many other design complexities.

Reducing the detrimental impact of TDC quantization error and DCO phase noise imposes conflicting bandwidth requirements. Wide bandwidth is needed to suppress the DCO phase noise, while low bandwidth is needed to mitigate TDC quantization error. Specifically, in a ring oscillator based DPLL this tradeoff deteriorates the jitter performance. Because of these difficulties, designing a low jitter wide tuning range digital PLL is a challenging design task.

Several attempts have already been made to address some of the aforementioned DPLL issues. For example, an LC-based DCO with excellent phase noise is combined with a very low PLL bandwidth to suppress the TDC quantization error [5]. Very high DCO resolution is achieved by simply limiting the DCO tuning range. On the other hand, a reasonably wide tuning range is obtained at the expense of a large output clock jitter caused by the large frequency step size [6, 7].

In this work, we focus on using a ring-based oscillator-based implementations to minimize the area requirements, while the goal is to design high performance digital clock multiplier.

2.6 Summary

Clock multiplier specifications and limitations, specifically based on jitter specifications, is presented in this chapter. Impact of clock jitter on the overall system performance is discussed. This indicates that the jitter of a DPLLs determines the highest performance that a system can achieve. The discussions also illustrate the different on-chip clock multiplication techniques. The effect of supply noise on clock multipliers, and different supply noise mitigation techniques have been discussed. The following chapters will target solving some of the issues in typical digital PLLs with circuit design examples.

CHAPTER 3. DIGITAL PLL WITH PVT INSENSITIVE SUPPLY NOISE CANCELLATION

Digital phase-locked loops (DPLLs) have recently emerged as a viable alternative to classical charge-pump analog PLLs [5–10,12]. A conventional DPLL block diagram is shown in Fig. 3.1. It consists of a time-to-digital converter (TDC), digital loop filter (DLF), digitally-controlled oscillator (DCO), and feedback divider. The TDC generates a digital word proportional to the phase error between the reference clock (REF), and the feedback divider output. The DLF is a proportional-integral filter realizing the Type-II PLL response. A digital-to-analog converter (DAC) interfaces the DLF to the voltage controlled oscillator (VCO). By obviating the need for a large loop filter capacitor and high performance charge-pump, DPLLs offer area savings; wide range of operating conditions; immunity to process, voltage, and temperature (PVT) variations; and easier scalability to newer processes. The ability to reconfigure the digital loop filter dynamically offers flexibility in setting the loop response and helps to optimize the locking behavior of the DPLL [10]. While these features are attractive, DPLLs suffer from unique bandwidth, operating range, and noise tradeoffs.

Conflicting bandwidth requirements to simultaneously suppress TDC quantization error and oscillator phase noise mandate low DPLL bandwidth and a low phase noise oscillator to minimize jitter [12]. In view of this, an LC-based DCO with excellent phase noise is combined with a very low DPLL bandwidth to suppress the TDC quantization error [5]. The DCO frequency quantization error imposes a DPLL operating range-resolution tradeoff. For a given hardware

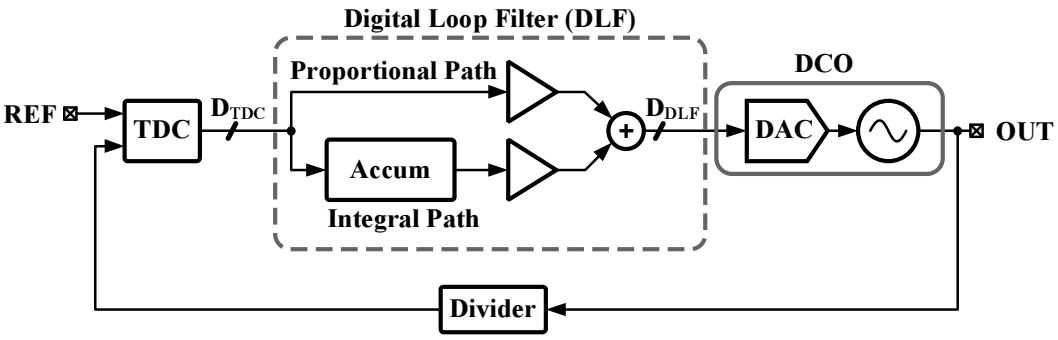


Figure 3.1: Block diagram of a conventional DPLL.

complexity, DCO resolution can be improved only by limiting its tuning range. A reasonably wide tuning range is achieved using a ring-DCO at the expense of larger output clock jitter [6, 7], while a high resolution DCO with narrow tuning range has been used to achieve good jitter performance [5]. Because of these difficulties, designing a low jitter wide tuning range digital PLL requires optimization of conflicting design parameters. Further, much like analog PLLs, when integrated into a large digital system, the ring oscillator is susceptible to supply noise, which especially limits the jitter performance of a DPLL. The focus of our work is on mitigating supply noise in ring oscillator based DPLLs. Further, the ring oscillator is the most sensitive block, we will focus on system and circuit design techniques that desensitize the DCO to supply noise.

Supply regulation techniques primarily focusing on suppressing the supply noise in the ring oscillator have been employed [17–20]. A general representation of a classical supply-regulated charge-pump PLL is depicted in Fig. 3.2. It consists of a 3-state phase-frequency detector (PFD), charge-pump, low-pass loop filter, VCO, and feedback divider. The VCO control voltage is applied to its supply through a low-dropout regulator, depicted as a buffer in Fig. 3.2. The low-dropout

regulator shields the VCO from supply noise and prevents it from reaching the internal VCO supply at the expense of additional area and power, and reduced voltage headroom [21].

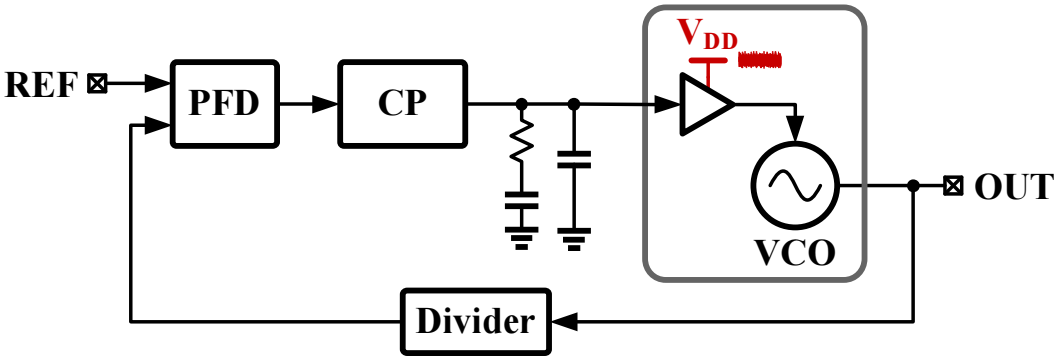


Figure 3.2: Supply-regulated PLL block diagram.

In practice, the regulator fails to completely isolate supply noise from the output due to various circuit non-idealities such as the finite transistor output impedance and insufficient regulator bandwidth. While commonly used, the supply regulation approach has several drawbacks. First, the power supply noise rejection of the regulated-PLL greatly depends on the regulator to PLL bandwidth ratio (BWR). For reasonable suppression, the regulator bandwidth must be made much larger than the PLL bandwidth. For instance, for a modest 8dB of worst-case power supply noise rejection (PSNR), the regulator bandwidth must be fifty times the PLL bandwidth [17]. Designing the regulator for such a wide bandwidth increases power dissipation. On the other hand, because VCO phase noise is high-pass filtered by the feedback loop, increasing BWR by reducing the PLL bandwidth exacerbates jitter due to oscillator phase noise. Second, the dropout voltage of the regulator limits the maximum control voltage of the VCO and reduces its tuning range. A lower dropout voltage increases the operating range of the VCO but compromises its PSNR. Finally, a large decoupling capacitor is needed in the

design of all regulators [17, 18].

In view of these drawbacks, our work focuses on supply noise *cancellation* techniques to mitigate supply noise. In contrast to supply *regulation*, supply noise *cancellation* techniques can operate at a lower supply voltage and have the potential to achieve excellent supply noise immunity without using a large decoupling capacitor. However, in a practical implementation, the effectiveness of this approach is greatly reduced by process, voltage, and temperature variations [22, 23].

In this work, we present a deterministic test signal based continuous background calibration scheme that leverages the highly digital nature of the DPLL to adaptively cancel the supply noise in the DCO. The proposed DPLL seeks to achieve low jitter, low power, and wide tuning range over a wide range of operating conditions and supply noise. The prototype DPLL fabricated in 0.13μm CMOS process achieves accurate supply noise cancellation over an output frequency range of 0.4GHz-to-3GHz. The cancellation circuitry reduces peak-to-peak jitter from 330ps to 50ps in the presence of 30mV_{pp} supply noise. At 1.5GHz, the DPLL consumes 2.65mW from a 1.0V supply.

The rest of the chapter is organized as follows. The concept of noise cancellation along with a brief review of conventional supply noise cancellation techniques are presented in Section 3.1. The proposed DPLL architecture is described in Section 3.2, and the circuit design details of important building blocks are presented in Section 3.3. Section 3.4 shows the experimental results obtained from the prototype integrated circuit. Finally, key contributions of this prototype are summarized in Section 3.5.

3.1 Supply Noise Cancellation

The general concept of noise cancellation is pictorially depicted in Fig. 3.3. It is based on the fact that a sensitive circuit can be desensitized to noise by cancelling the noise before it appears at the output. Conceptually, this can be achieved by subtracting the appropriately scaled noise from the output of the sensitive circuit. While its simplicity is appealing, the effectiveness of this approach greatly depends on the accuracy of the cancellation gain, K_V.

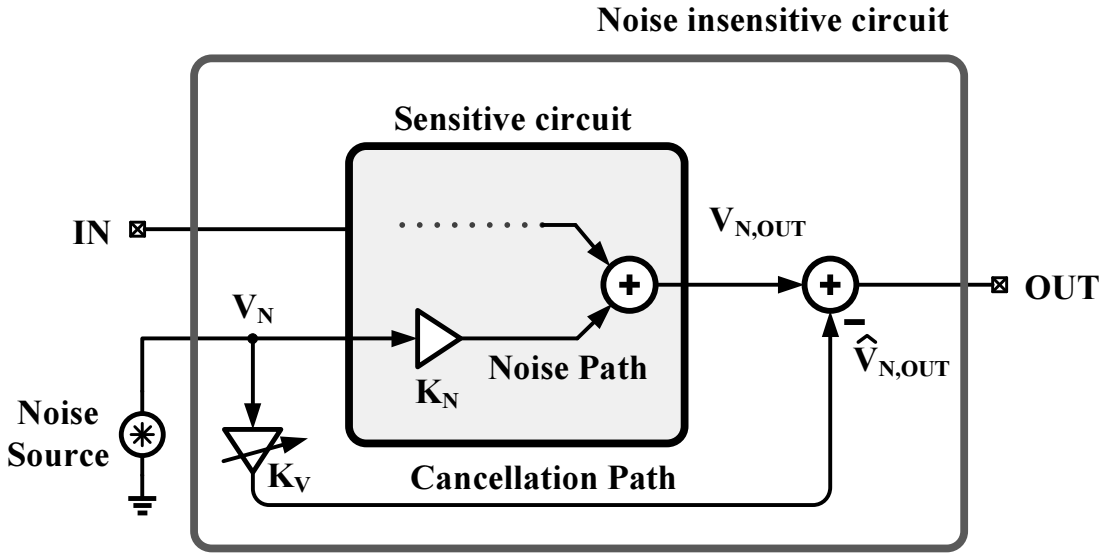


Figure 3.3: Illustration of noise cancellation concept.

Ideally, K_V must be equal to the intrinsic noise sensitivity of the circuit, K_N. Under this condition, the estimated output noise, $\hat{V}_{N,OUT}$, completely cancels the output induced noise, $V_{N,OUT}$. In practice, the sensitivity of K_N to PVT variations poses a challenge in setting K_V appropriately. While the concept of noise cancellation can be applied in many applications, the focus of our work is in the context of cancelling supply noise in a VCO. To this end, we present a digital background calibration algorithm that determines optimal K_V under all operating

conditions and helps achieve robust cancellation of supply noise in the VCO.

Several attempts have been already made to cancel the effect of supply noise in the VCO [22,23]. In [22], as shown in Fig. 3.4, the additional current induced by supply noise is cancelled at the output of the voltage-to-current (V-to-I) converter. The noise cancellation gain, G_m, that best matches the V-to-I sensitivity was determined from transistor-level simulations.

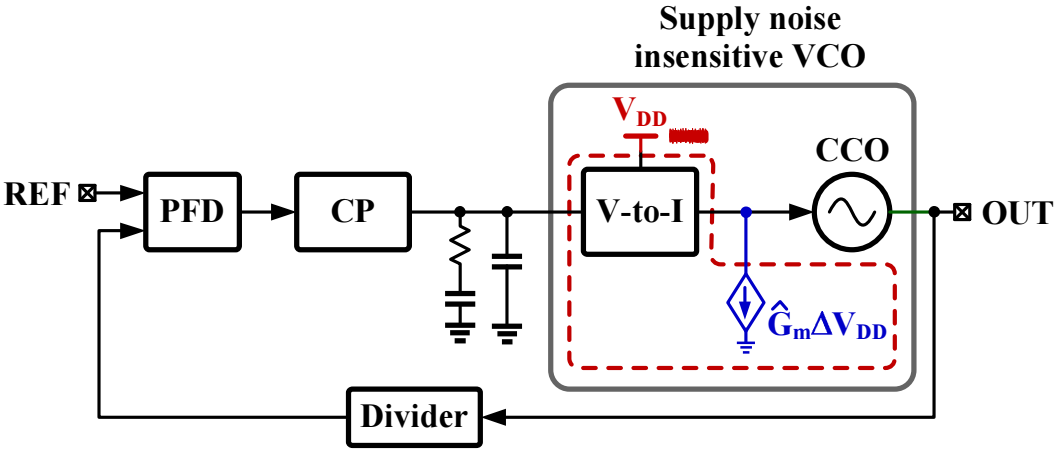


Figure 3.4: PLL architecture employing open loop supply noise cancellation with a fixed cancellation gain $\hat{G}_m$.

Ideally, with complete cancellation, the current-controlled oscillator frequency becomes independent of supply noise. However, in practice, process and temperature variations severely impact the VCO supply noise sensitivity[2] as shown in Fig. 3.5 and Fig. 3.6. This illustrates that the supply sensitivity varies with process corners, DC level of supply voltage, and operating temperature. Thus, using a fixed cancellation gain as in [22] is grossly sub-optimal. Therefore, it is necessary

[2]The supply noise sensitivity is defined as the percentage change in the VCO oscillating frequency to the percentage change in the supply voltage, i.e., $\frac{\partial f_{VCO}(\%)}{\partial V_{DD}(\%)}$.

to calibrate the cancellation gain.

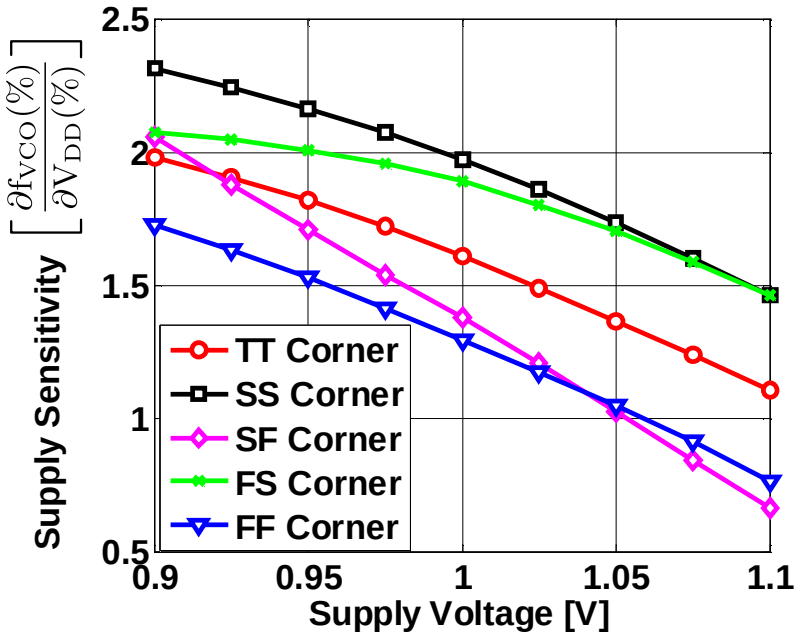


Figure 3.5: Simulated VCO supply sensitivity for different process corners at 27°C temperature.

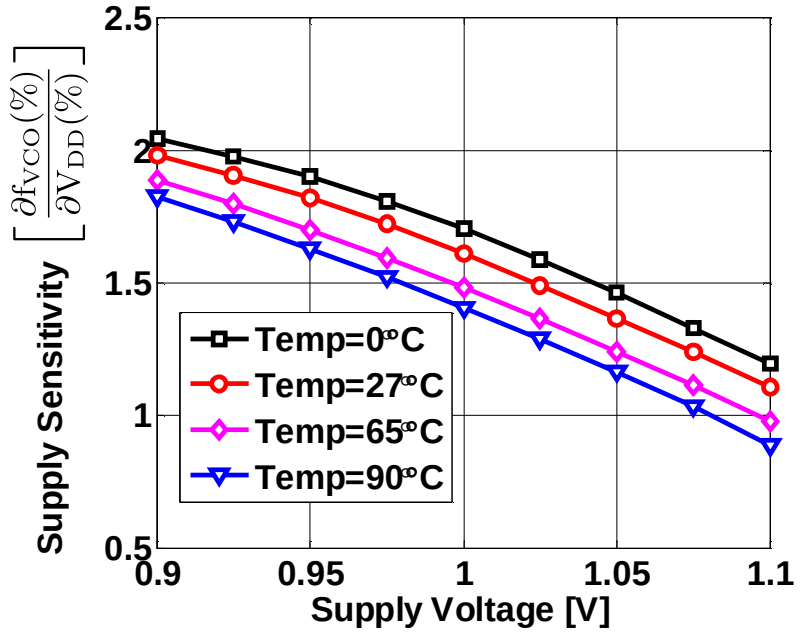


Figure 3.6: Simulated VCO supply sensitivity at different temperatures.

An analog foreground calibration was proposed in [23] to determine the optimal cancellation gain. On power up, once the PLL is locked, a known step voltage is applied to the VCO supply, as illustrated in Fig. 3.7(a). Using the loop's response to this known perturbation, the foreground calibration circuitry estimates VCO supply noise sensitivity and determines the desired cancellation gain.

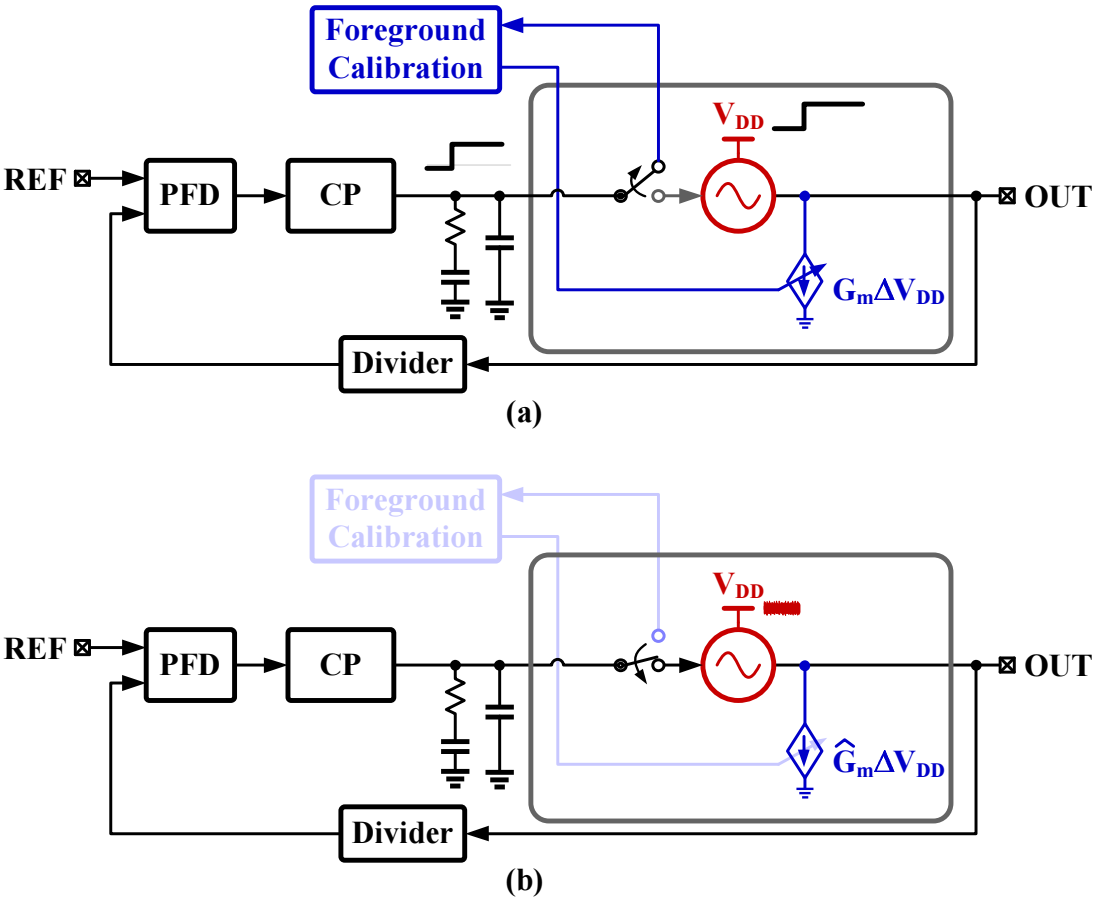


Figure 3.7: Analog foreground calibration scheme (a) calibration mode, and (b) normal PLL mode.

Once the foreground calibration algorithm converges to the desired cancellation gain, $\hat{G}_m$, the PLL is switched back to operate in its normal mode of operation as shown in Fig. 3.7(b), and the cancellation gain remains fixed at $\hat{G}_m$. While this technique successfully mitigates process dependence, it is susceptible to variations

in operating conditions, because of its foreground nature. As illustrated by the simulated results in Fig. 3.8 and validated by measured results in Section 3.4, the supply sensitivity greatly depends on the oscillation frequency and the supply voltage DC value. This dependence makes any foreground approach ineffective in a practical setting. Furthermore, this technique relies on accurately probing the analog control voltage, and hence it is susceptible to analog circuit imperfections. To overcome these drawbacks, we present a digital background calibration scheme that seeks to determine the optimal cancellation gain in the presence of process, voltage, temperature, and oscillation frequency variations.

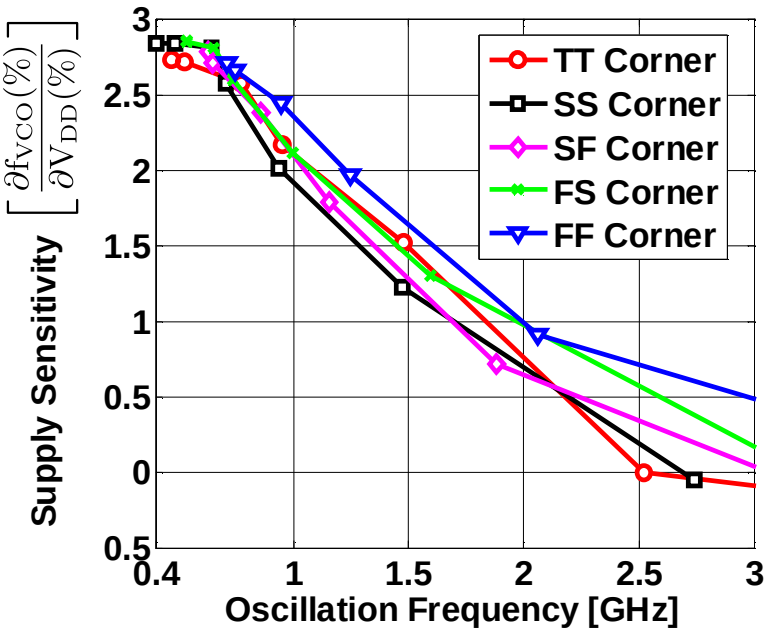


Figure 3.8: Simulated VCO supply sensitivity for operating frequencies from 400MHz-to-3GHz at different process corners.

3.2 Proposed DPLL Architecture

The detailed block diagram of the proposed DPLL is shown in Fig. 3.9 [1]. It consists of separate proportional and digital integral paths, feedback divider, supply noise cancellation gain calibration logic, and supply noise insensitive DCO. The proportional control is implemented using a 3-state PFD that directly drives the oscillator through a 3-level current-mode DAC, thus eliminating TDC quantization error in the proportional path. A flip flop (FF) acts as an early/late detector on PFD outputs and drives the digital accumulator with the sign of the phase error. A low bandwidth digital integral path suppresses the phase quantization error of the FF.

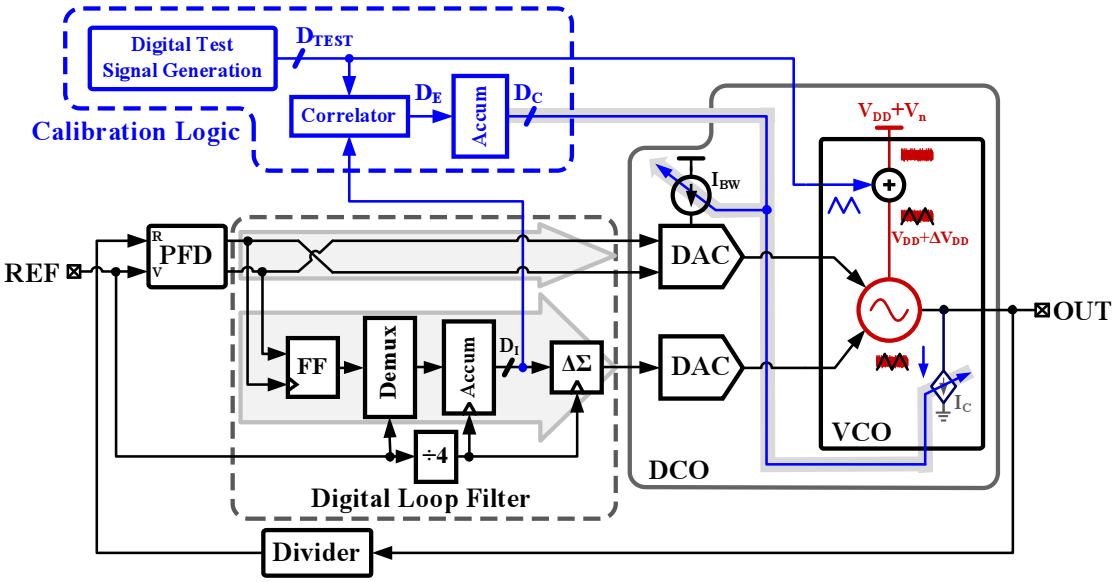


Figure 3.9: Block diagram of the proposed DPLL using deterministic background calibration of the supply noise cancellation gain.

Separating the proportional and integral path helps in extending the DPLL operating range without degrading either the quantization error induced deterministic jitter or the thermal noise induced random jitter [24, 25]. A 1-to-4 demulti-

plexer is used to ease the speed requirements of the fully-synthesized digital control logic. The digital delta-sigma modulator truncates the 14-bit accumulator output, D_I, to 15-levels and drives a current-mode DAC. A second-order passive low-pass filter suppresses the out-of-band quantization error and drives the integral control voltage input of the oscillator.

The DCO supply noise immunity is improved greatly, as discussed earlier, by intentionally injecting at the oscillator output an appropriate magnitude cancellation current, I_C, in proportion to the supply noise. Because the optimal value of I_C depends on PVT variations and oscillator frequency, a test signal based digital background calibration scheme is employed to determine the compensation gain accurately and achieve excellent broadband supply noise immunity under all operating conditions. By injecting a test signal into the oscillator supply and correlating it with the digital integral path output, the digital background calibration engine estimates the cancellation gain, G_m, and desensitizes the oscillator to supply noise. As with foreground calibration, the effectiveness of this background calibration method greatly depends on the accuracy with which G_m can be estimated. Before examining the process of G_m estimation, it is instructive to evaluate the dynamics of the DPLL loop.

3.2.1 DPLL Loop Dynamics

The proposed DPLL was designed to have a heavily over-damped Type-II response, wherein the digital integral path has a minimal effect on the loop dynamics. The s-domain closed-loop transfer function of the DPLL is given by,

$$\frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{N(1 + sK_P/K_I)}{1 + sK_P/K_I + s^2N/K_I} \tag{3.1}$$

where N is the feedback divide ratio; K_P and K_I denote the cumulative gain through the proportional and the integral path, respectively; and K_{VDD} is the VCO gain from the supply node. The proportional and integral path gains are

$$K_P = K_{PDAC} \cdot K_{P,DCO} \tag{3.2}$$

$$K_I = K_{IDAC} \cdot K_{I,DCO} \ . \tag{3.3}$$

Comparing Eq. (3.1) to the standard second order transfer function represented in control theory notation leads to,

$$\frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{N(1 + s2\zeta/\omega_n)}{1 + s2\zeta/\omega_n + s^2/\omega_n^2} \ , \tag{3.4}$$

where the damping factor can be calculated to be

$$\zeta = \frac{K_P}{2\sqrt{NK_I}} \ . \tag{3.5}$$

In the proposed DPLL, K_I was chosen to be much smaller than K_P in order to minimize dithering jitter caused by bang-bang phase detector non-linearity and DCO quantization error. As a consequence, the DPLL exhibits an over-damped response, wherein its two poles, zero, and 3dB bandwidth are

$$\omega_{P1} \approx \omega_Z = \frac{K_I}{K_P} \tag{3.6}$$

$$\omega_{P2} \approx \frac{K_P}{N}, \ \omega_{P2} \gg \omega_{P1} \tag{3.7}$$

$$\omega_{BW} \approx \frac{K_P}{N} = \frac{K_{PDAC} \cdot K_{P,DCO}}{N}, \ \zeta \gg 1 \ . \tag{3.8}$$

Because $\zeta \gg 1$ remains valid over the entire operating frequency range, DPLL remains over-damped K_{IDAC} variation has negligible impact on loop stability.

3.2.2 Estimating the Cancellation Gain

As has been discussed, accurate calibration of the cancellation gain is vital to the performance of any supply noise cancellation technique, which can be viewed as an application of adaptive control as described in the Appendix [26]. In the proposed background calibration approach, we hypothesize that by adding a low frequency test signal to the supply of the oscillator, as illustrated in Fig. 3.9, and adjusting G_m until the test signal completely disappears at the accumulator output leads to convergence of G_m to the optimum value. Intuitively, if the noise cancelling circuit accurately cancels the injected test signal, then the accumulator output should not change in steady-state. A low frequency, deterministic digital test signal, D_{TEST}, is converted to an analog voltage and added to the DCO supply voltage. Because the supply noise cancellation circuit is indiscriminate of the noise source, adjusting the cancellation gain to cancel D_{TEST} also suppresses supply noise.

To understand the process of G_m calibration, it is instructive to first consider the transfer functions associated with the DCO supply node. The magnitude response of the DCO supply to the PLL phase output transfer function is given by,

$$\frac{\Phi_{out}(s)}{V_{DD}(s)} = \frac{(NK_{VDD}/K_I)\,s}{1 + sK_P/K_I + s^2N/K_I}\ , \tag{3.9}$$

and its magnitude response exhibits the well known band-pass transfer characteristic, shown in Fig. 3.10(a). In other words that both the low- and high-frequency supply perturbations are suppressed at the PLL output.

On the other hand, the low-pass shape of the DCO supply to the accumulator

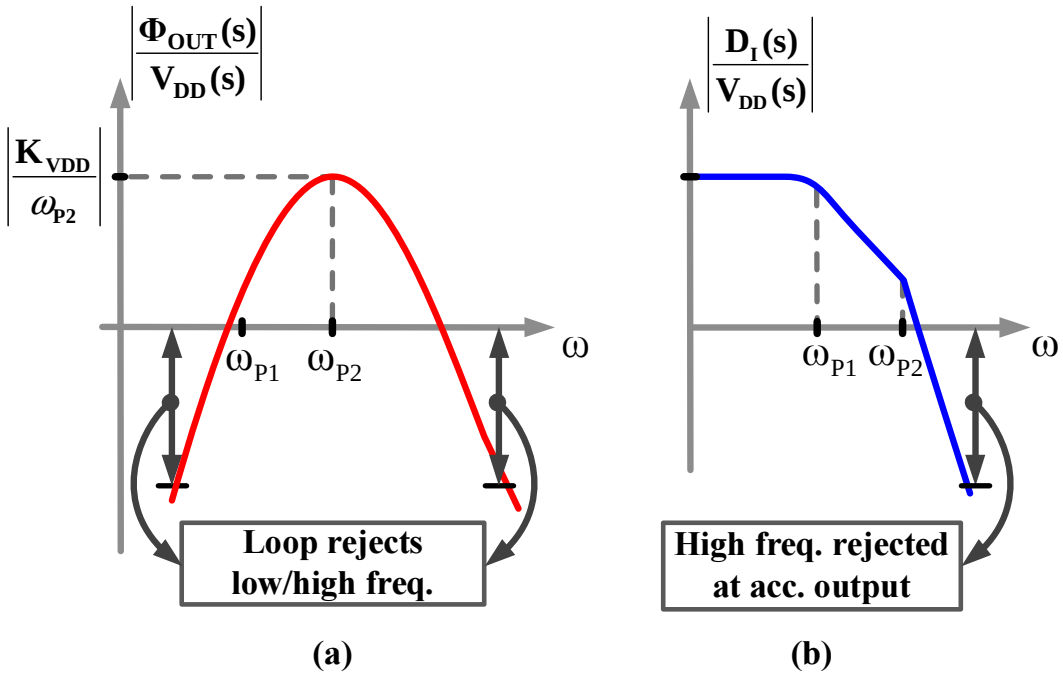


Figure 3.10: DCO supply node transfer functions to: (a) DPLL output, and (b) accumulator output, D_I.

output transfer function, given by,

$$\frac{D_I(s)}{V_{DD}(s)} = \frac{K_{VDD}}{1 + sK_P/K_I + s^2N/K_I}\ , \tag{3.10}$$

illustrates that low frequency disturbances on the supply voltage appear at the accumulator output while high frequency disturbances are attenuated by the loop, shown in Fig. 3.10(b). Based on these observations, a low frequency test signal was chosen to calibrate the cancellation gain (see Fig. 3.11) under the assumption that the cancellation gain is independent of the supply noise frequency. This assumption is validated by the measurement results in Section 3.4.

Note that in an over-damped DPLL, the bandwidth and the center frequency of the transfer functions $\frac{D_I(s)}{V_{DD}(s)}$ and $\frac{\Phi_{OUT}(s)}{V_{DD}(s)}$ are equal to the lower (ω_{P1}) and the higher (ω_{P2}) of the two closed-loop poles, respectively. Consequently, a test signal

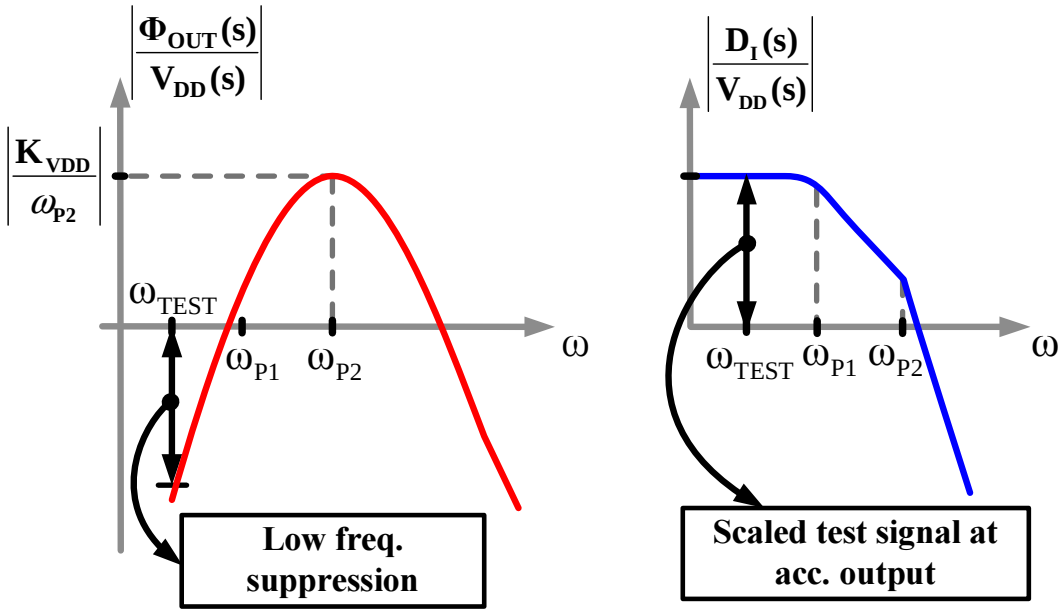


Figure 3.11: Illustration in the design criterion in the choice of test signal frequency.

(whose frequency is lower than ω_{P1}) appears at the accumulator output with little attenuation, while it is heavily suppressed at the DPLL output. In other words, a low frequency test signal injected into DCO supply does not degrade the output jitter and presence of the test signal in the accumulator output provides a measure of VCO supply noise sensitivity. Therefore, the accumulator output is used to continuously calibrate the cancellation gain.

Shown in Fig. 3.12 is the time domain waveform of the calibration code (D_C), the test signal (D_{TEST}), and the accumulator output (D_I). In the absence of supply noise cancellation ($I_C = 0$) and owing to the low-pass characteristic of $\frac{D_I(s)}{V_{DD}(s)}$, a scaled version of the test signal appears at the accumulator output, as shown in Fig. 3.12(a). When the calibration is enabled, the cancellation gain is adjusted until the test signal completely disappears at the accumulator output, as shown in Fig. 3.12(b). Under this condition, both the test signal and the supply noise

are accurately cancelled at the DCO output, and the DPLL becomes insensitive to noise on the ring oscillator supply. Because the DPLL output phase is not disturbed by supply noise and assuming the absence of any other noise sources, the accumulator output remains fixed.

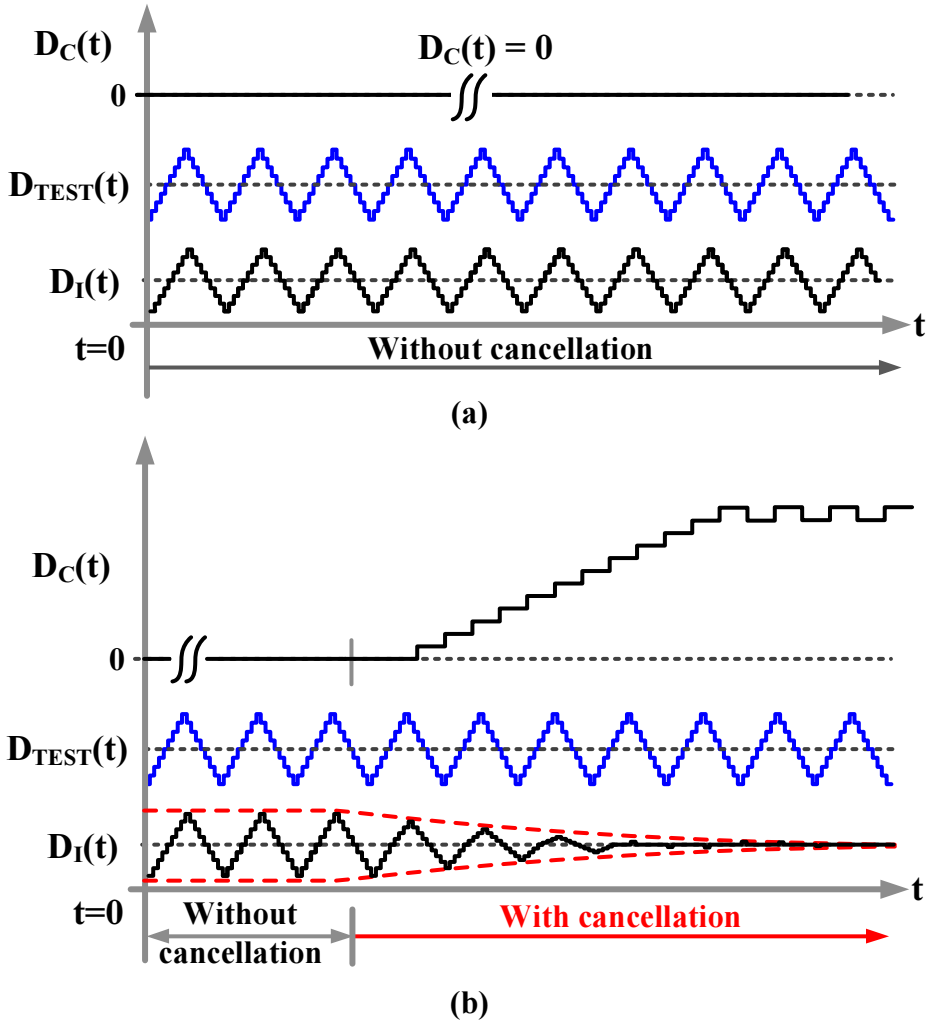


Figure 3.12: Time domain waveforms illustrating the evolution of the accumulator output, D_I, (a) without cancellation, and (b) with cancellation.

3.2.3 Noise Cancellation and System Stability

The proposed deterministic test signal based digital background calibration can be viewed as an application of adaptive control [26]. The background calibration estimates the *supply noise gain*, $K_N(s)$, and sets the *cancellation gain*, $K_V(s)$ accurately to track $K_N(s)$. In the proposed implementation,

$$K_N(s) = K_{N,VDD} H_N(s) \tag{3.11}$$

$$K_V(s) = K_{V,VDD} H_V(s) \tag{3.12}$$

where, $K_{N,VDD}$ and $K_{V,VDD}$ are the DC gains of $K_N(s)$ and $K_V(s)$, and $H_N(s)$ and $H_V(s)$ are the normalized transfer functions, of the noise gain and the cancellation gain, respectively. The adaptive system will be stable if these transfer functions, $H_N(s)$ and $H_V(s)$, are *strictly positive real* (SPR) [26]. In the proposed implementation, the transfer functions can be approximated as,

$$K_N(s) = K_{N,VDD} H_N(s) \approx K_{N,VDD} \tag{3.13}$$

$$K_V(s) = K_{V,VDD} H_V(s) \approx K_{V,VDD} \quad ; \; K_{V,VDD} = \theta_{cal} K_0 \tag{3.14}$$

where, K_0 is the nominal cancellation gain and θ_{cal} is the correction factor to achieve optimal cancellation gain. By virtue of our circuit implementation, $H_V(s)$ and $H_N(s)$ exhibit nominally identical single pole low-pass transfer characteristics with a bandwidth much greater than the PLL bandwidth. Consequently, they satisfy the SPR conditions, thus guaranteeing system stability. In steady-state, the correction factor θ_{cal} converges to K_N/K_0, resulting in $K_V = K_N$, as desired. Large mismatch between the transfer functions, $H_N(s)$ and $H_V(s)$, manifests as un-modeled dynamics and could lead to convergence failure or sub-optimal cancellation gain [26]. The test signal (sometimes referred to as training signal) was

chosen to not affect the loop dynamics and to simplify the hardware requirements. A sinusoidal test signal is easier to analyze, but it is more complicated to generate digitally. A *pseudo-random binary sequence* (PRBS), can also be used as a test signal. However, this will degrade the phase noise performance and also increases the hardware complexity of the correlator. In view of these tradeoffs, a low frequency triangular test signal was employed in the prototype chip. The choice of test signal frequency will determine the calibration convergence time. Since the test signal needs to be at a lower frequency than PLL loop bandwidth, its frequency was chosen to be 100kHz. At 1.5GHz output frequency, the calibration converges in four calibration cycles, approximately 40μs. Due to the use of 5-bit calibration code, the start-up time can be up to 31 cycles, or 310μs. Note that, once steady-state is reached, the calibration loop continuously tracks slow variations in process, temperature, and DC supply voltage.

3.3 Building Blocks

In this section, the transistor-level implementation of key building blocks is discussed. The PFD is implemented using the well-known three-state architecture and is implemented using the pass transistor structure [27]. A sense-amplifier flip-flop is used as the bang-bang phase detector in the digital integral path [28], and all digital building blocks are synthesized using standard cells. The design details of the supply noise insensitive DCO and the proportional and integral path DACs are discussed in the following.

3.3.1 Supply Noise Insensitive DCO

The schematic of the ring oscillator, including test signal injection and supply noise cancellation circuitry, is shown in Fig. 3.13. Because the test signal and supply noise must have the same transfer function, the test signal is directly injected into the VCO supply using a digitally controlled resistor, R_{DTEST}. A fixed resistor, R_0, provides the nominal VCO supply current, while D_{TEST} controls the supply resistance and varies the internal VCO supply, V_{DD_VCO} [29]. To minimize the headroom penalty, voltage drop across the variable resistor is designed to be less than 20mV at 1.5GHz output frequency, and less than 30mV under all operating conditions.

The three-stage ring oscillator is composed of pseudo-differential delay cells, as shown in Fig. 3.13. The cross-coupled PMOS transistors guarantee differential operation of the delay cells without using a tail-current bias [30]. The integral and proportional controls are implemented by tuning the strength of the latch load and the output time constant, respectively. To minimize supply noise coupling, integral control voltage (V_I) is coupled to V_{DD_VCO} instead of ground. However, the V_{DS} of the latch-load PMOS transistors varies with the supply voltage, causing the current in the delay cell to change. An increase in the supply voltage leads to an increase in the current, and therefore an increase in the oscillation frequency. Since the supply noise injects additional current into the VCO, adding cancellation circuitry to sink the same amount of current eliminates the noise appearing at the output. In other words, this oscillator and the cancellation circuitry exhibit positive and negative supply noise sensitivities, respectively. After calibration, these sensitivities cancel, and the VCO has ideally zero supply voltage sensitivity. The injected test signal along with supply noise is cancelled by using transistors, M_{n1}-M_{n6}, at delay cell

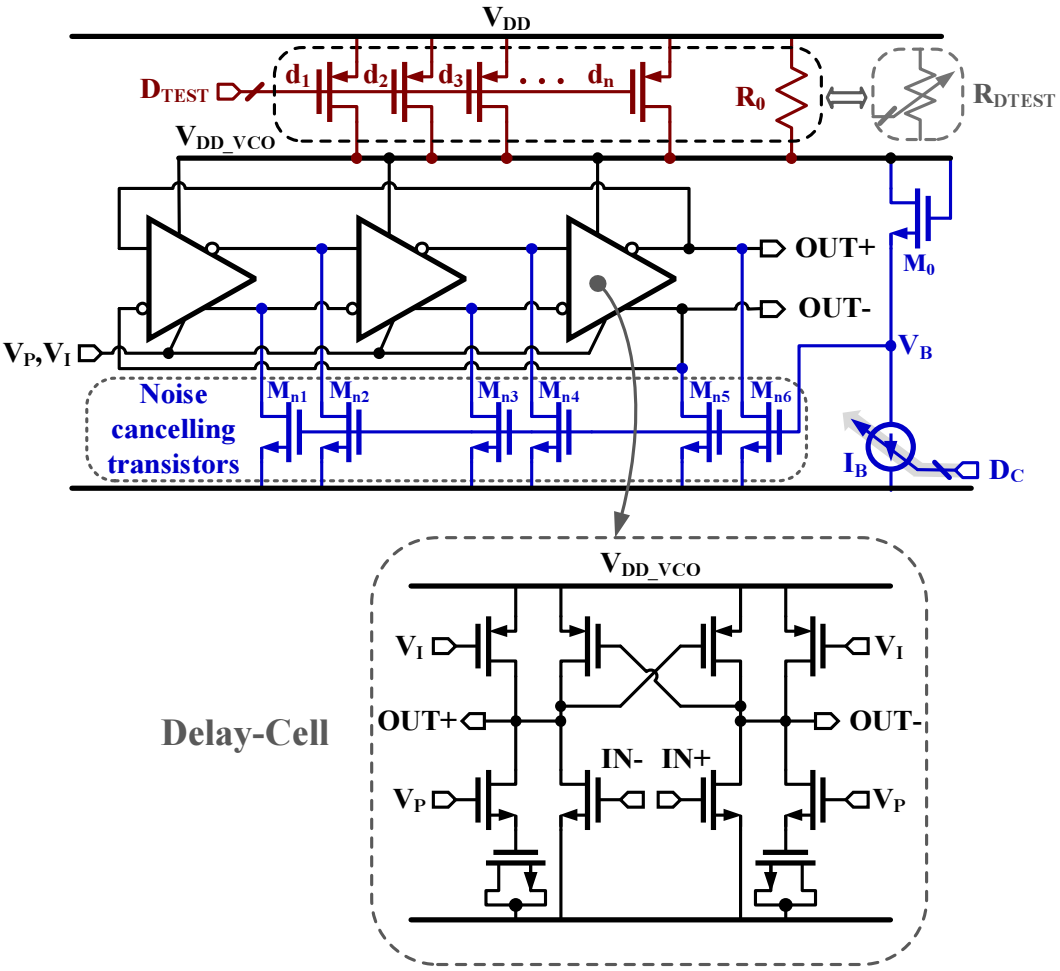


Figure 3.13: Schematic of the proposed ring oscillator with supply noise cancellation.

outputs in the VCO, as shown in Fig. 3.13. Transistor M_0 couples supply noise to the gates of the cancelling transistors with a digitally calibrated gain that is set by current I_B. Intuitively, when the supply voltage increases, the current in the oscillator increases leading to an increase in the oscillation frequency. At the same time, voltage V_B also increases due to transistor M_0, causing the cancelling transistors to sink more current to ground. This reduces the oscillator frequency thus compensating for the increase in the oscillation frequency due to increased

supply voltage. The circuit schematic of the complete supply noise insensitive DCO is shown in Fig. 3.14.

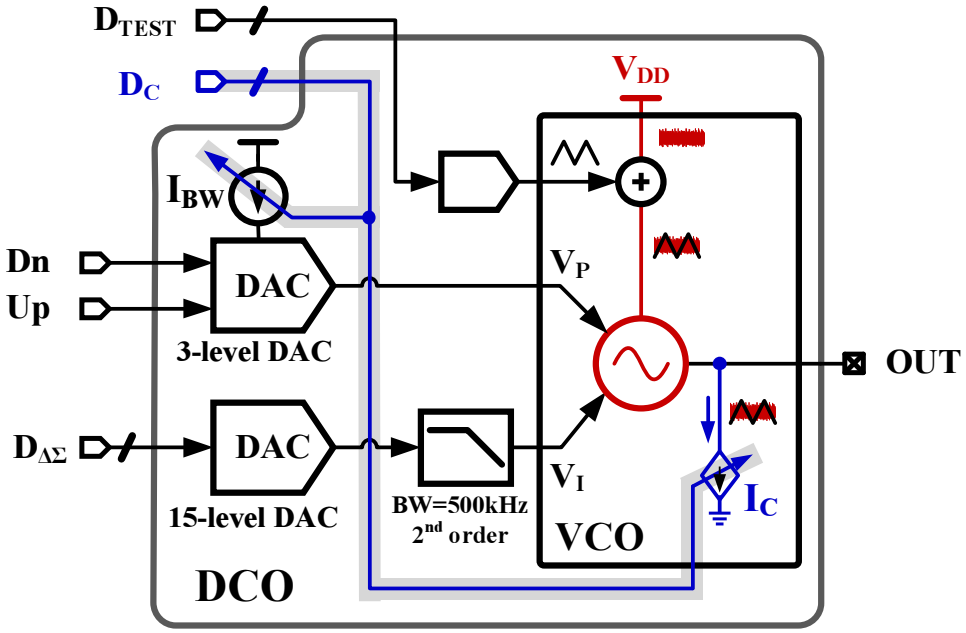


Figure 3.14: Block diagram of the complete supply noise insensitive DCO.

It consists of a 3-level DAC and a 15-level DAC to implement the proportional and integral control, respectively; variable resistor to inject the supply noise; and noise cancelling transistors that sinks the noise cancellation current (I_C) from the output of the oscillator. Simulations indicate that the noise cancelling transistors, M_{n1}-M_{n6}, degrade phase noise by about 3dB at 1MHz offset. Because the phase noise contribution from M_{n1}-M_{n6} scales inversely with the calibration code (D_C), varying the proportional path bias current accordingly increases the PLL bandwidth and mitigates jitter degradation.

3.3.2 Proportional Path DAC

The circuit schematic of the DAC employed in the proportional path is shown in Fig. 3.15. Its inputs are driven by pulse-width modulated PFD output signals, Dn and Up, and is implemented with a 3-level current source. As illustrated by the truth table in Fig. 3.15, the three PFD states, Up, Reset, and Dn are mapped to 0, I_1, and $2I_1$ currents, respectively, where I_1 is the bias current. This uni-polar implementation of the proportional control minimizes current mismatch compared to a conventional bi-polar charge-pump [31]. A diode connected transistor converts the DAC output current to a voltage. It's important to note that the cancellation of noise on the PDAC supply node is only effective to the extent that the noise is correlated to the VCO supply.

To alleviate the phase noise degradation due to noise canceling transistors, the PLL loop bandwidth is scaled, without changing the center frequency of the oscillator, by varying the digitally controlled current (I_{BW}). Decreasing the calibration code (D_C) increases I_{BW}, which increases the proportional gain, thus increasing PLL bandwidth. This mechanism is illustrated in Fig. 3.16. A biasing circuit is used to generate the required voltages, V_{B1} and V_{B2} (see Fig. 3.15).

Under phase lock condition, both Up and Dn signals are identical and the current DAC output $I_0 = I_1$. The current I_2 in addition to I_1 sets the nominal current I_P, such that $I_{P0} = I_1 + I_2$. The current I_P through the I-to-V converter determines the nominal proportional control voltage, $V_P = V_{P0}$. The biasing circuit ensures that $I_1 + I_2$ is constant, thus keeping the center frequency fixed while varying the bandwidth.

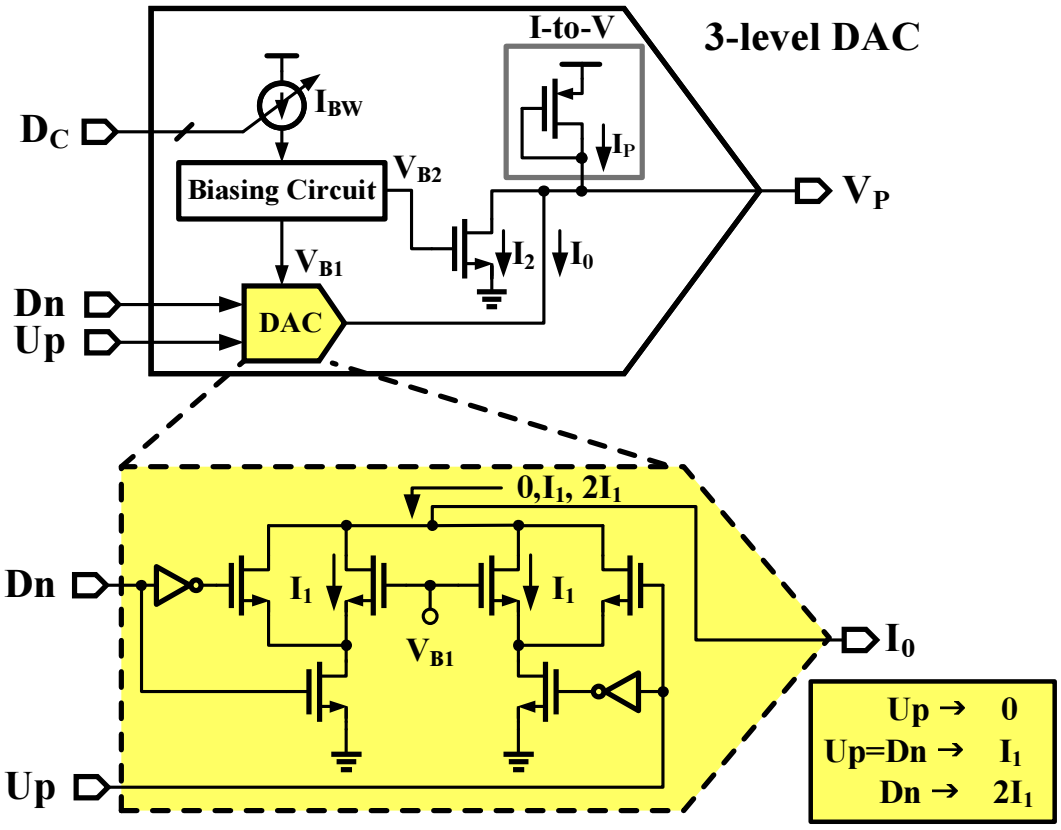


Figure 3.15: Circuit implementation of the proportional path DAC.

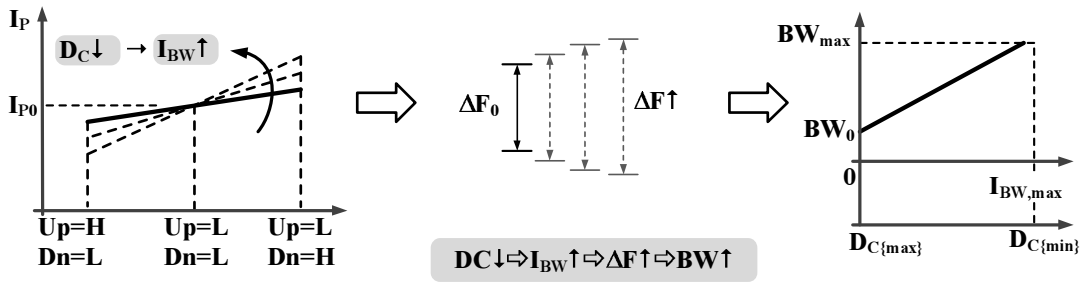


Figure 3.16: Concept of bandwidth variation in the proportional path.

3.3.3 Integral Path DAC

The block diagram of the digital-to-analog converter used in the integral path is shown in Fig. 3.17. A 14-bit second order digital delta-sigma modulator

(DSM) truncates the accumulator 14-bit digital word, D_I, to 15-levels and drives a 15-element current mode DAC.

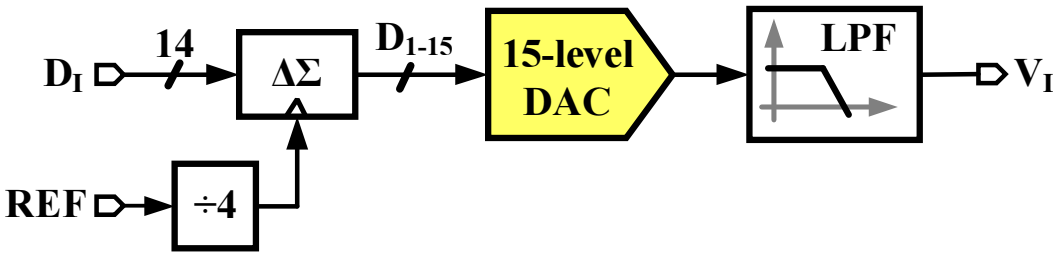


Figure 3.17: Block diagram of the delta-sigma DAC used in the integral path.

A current-mode DAC, consisting of 15 nominally matched current sources, converts the digital input to an equivalent output current, as shown in Fig. 3.18. Resistor R converts the DAC output current to voltage. A second order passive low-pass filter (LPF), with a 500kHz bandwidth, suppresses out-of-band quantization error and generates the integral control voltage of the oscillator, V_I. The delta-sigma DAC architecture eases hardware requirements, but the phase shift introduced by LPF increases loop latency and degrades the jitter performance. In the proposed DPLL, dithering jitter is suppressed by ignoring the lower 4 least significant bits of the accumulator output and passing only the 14 most significant bits to the DAC.

3.4 Experimental Results

The proposed DPLL was fabricated in a 0.13μm CMOS process, and the die photograph of the prototype chip is shown in Fig. 3.19. It occupies an active area of 0.08mm^2 (200μm×400μm). The analog portion occupies 50% (4% for the VCO and 46% for the remaining analog circuits); the digital portion occupies 37.5%; while

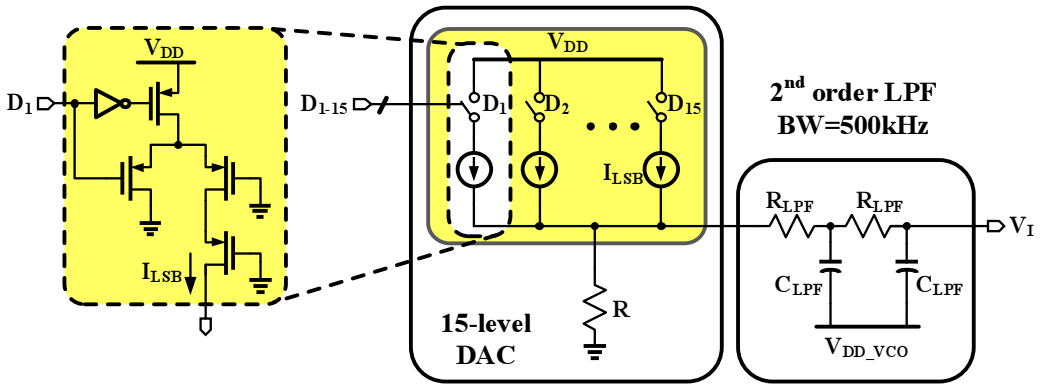


Figure 3.18: Circuit schematic of the 15-level current mode DAC and post filter.

the test signal generation, calibration logic, and cancellation circuitry occupy only 12.5% of the overall DPLL area.

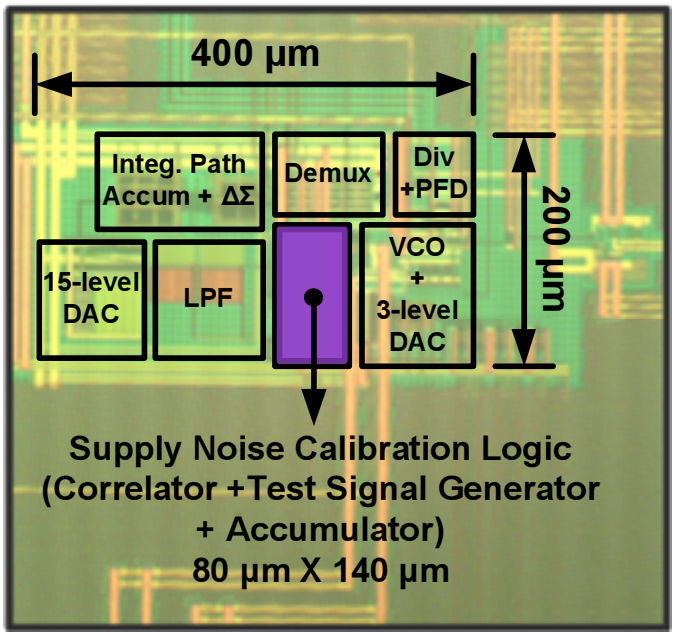


Figure 3.19: Prototype DPLL die photograph.

The measurement setup used to characterize the prototype IC is shown in Fig. 3.20. The supply noise measurements were performed by modulating the VCO supply with either a white gaussian noise or a sinusoidal tone. An arbitrary

waveform generator (Tektronix AWG7122B) was used to inject white noise, while an RF signal generator (Fluke 6062A) was used to introduce sinusoidal noise tones on the VCO supply. An integrated supply noise monitor (implemented using a wide bandwidth voltage follower) was used to measure the amount of on-chip VCO supply noise and guarantee the fidelity of all supply noise measurements. The input reference clock was generated using the same arbitrary waveform generator. Since the prototype chip's feedback divide ratio is fixed at four, the desired output frequency was obtained by varying the reference frequency. A communication signal analyzer (Tektronix CSA8200) was used for the time domain long term absolute jitter measurements.

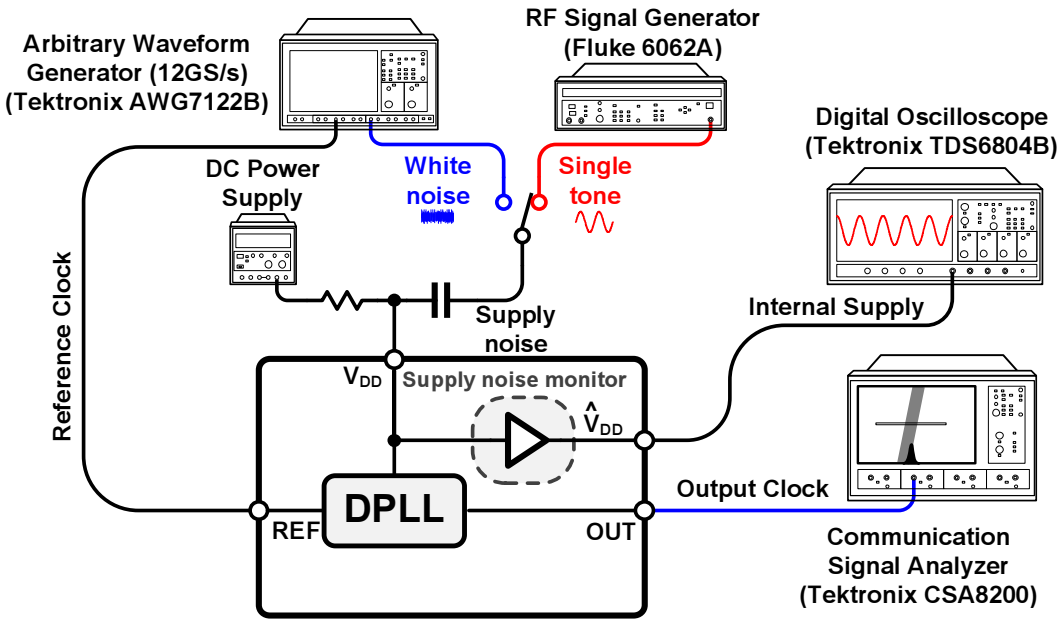


Figure 3.20: DPLL measurement setup.

A wide range of measurements were performed to evaluate the performance of the prototype chip and validate the proposed deterministic background supply noise calibration technique. All measurements were performed at an output frequency of 1.5GHz unless otherwise specified. Figure 3.21 shows the measured jitter

histograms of four different test signal and supply noise conditions. In the absence of both the supply noise and test signal, the measured absolute peak-to-peak jitter with 50k hits is 47ps.

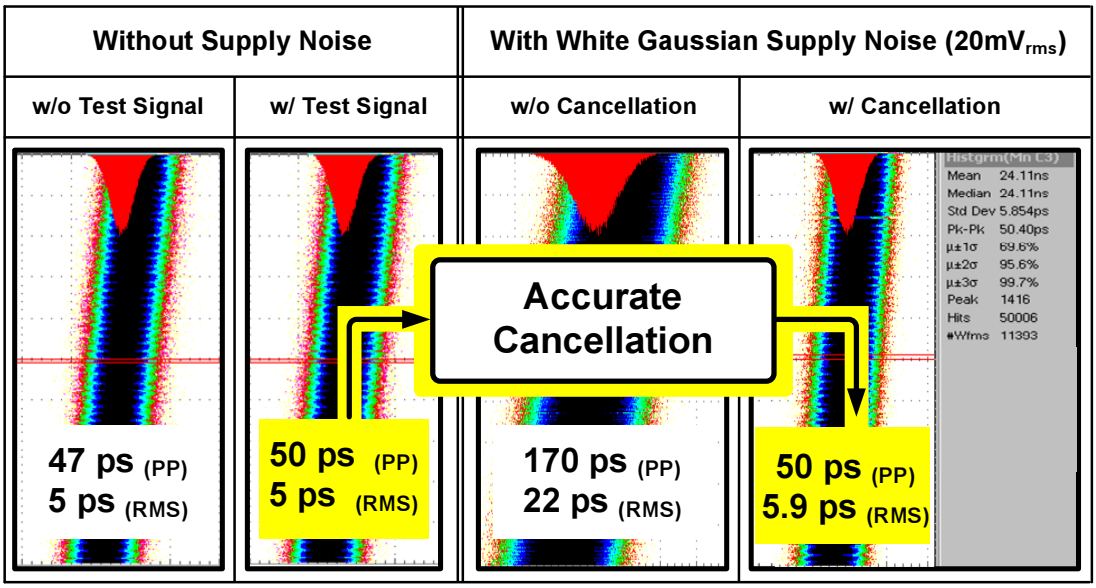


Figure 3.21: Measured long term jitter histograms (50k hits) at 1.5GHz output frequency for 20mV$_{rms}$ white gaussian supply noise.

When a 10mV$_{pp}$ test signal is added, minimal jitter degradation is observed with the peak-to-peak jitter increasing by only 3ps. When a 20mV$_{rms}$ white Gaussian supply noise is additionally superimposed on the supply voltage, the peak-to-peak jitter increases to 170ps, indicating the high supply noise sensitivity of the oscillator. When cancellation is enabled, the calibration loop converges to the digital code 4, and the output jitter is reduced from 170ps to 50ps, thus illustrating the effective cancellation achieved by the proposed architecture. Because the VCO is most sensitive to supply noise tones in the vicinity of the DPLL bandwidth (see Fig. 3.10), jitter degradation is at its worst under this condition. To characterize the jitter performance under this worse-case condition, a 30mV$_{pp}$, 10MHz noise tone is injected on the VCO supply, and the peak-to-peak jitter without and with

cancellation was measured to be 330ps and 50ps, respectively (see Fig. 3.22).

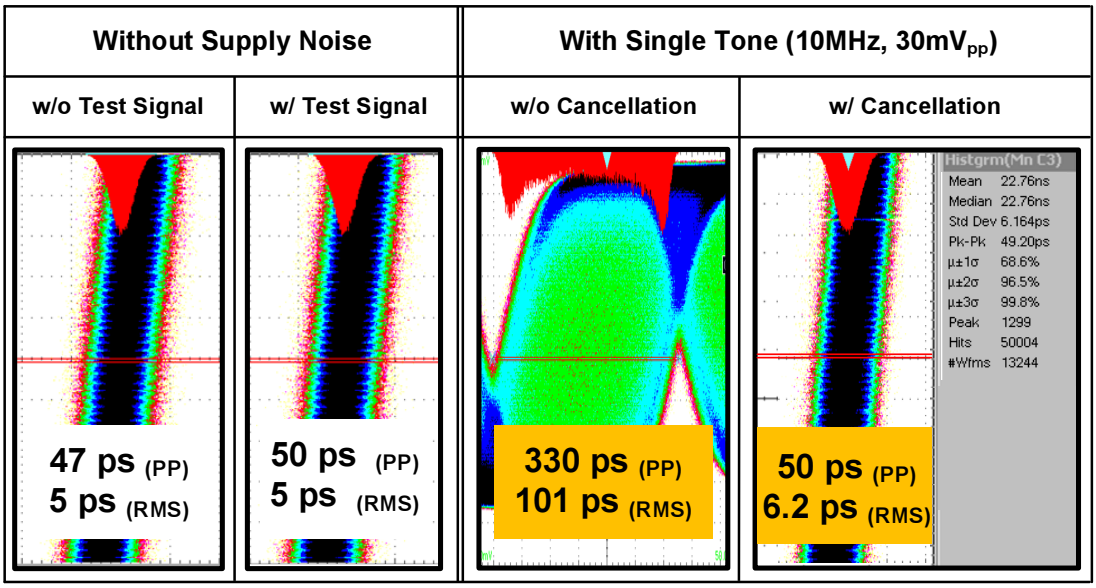


Figure 3.22: Measured long term jitter histograms (50k hits) at 1.5GHz output frequency for $30mV_{pp}$, 10MHz single tone supply noise.

To evaluate the effective cancellation bandwidth of the proposed scheme, the supply noise frequency is swept from 0.1MHz-to-2GHz, and the measured peak-to-peak jitter is plotted in Fig. 3.23. Since the noise on the DCO supply is band-pass filtered by the PLL, the supply noise sensitivity is highest around the PLL bandwidth (approximately 10MHz). When cancellation is enabled, the jitter degradation is mitigated over a wide range of supply noise frequencies, thus illustrating the very wide cancellation bandwidth of the proposed scheme.

To ensure that the on-chip digital self-calibration algorithm converged to the optimal cancellation gain, the calibration code was set externally and the measured rms jitter is plotted in Fig. 3.24 under different supply noise conditions. The optimal calibration code is equal to 4 and is independent of supply noise frequency. The calibration loop always converged to the same calibration code of 4 under the same set of conditions. Thus it can be concluded that the supply noise

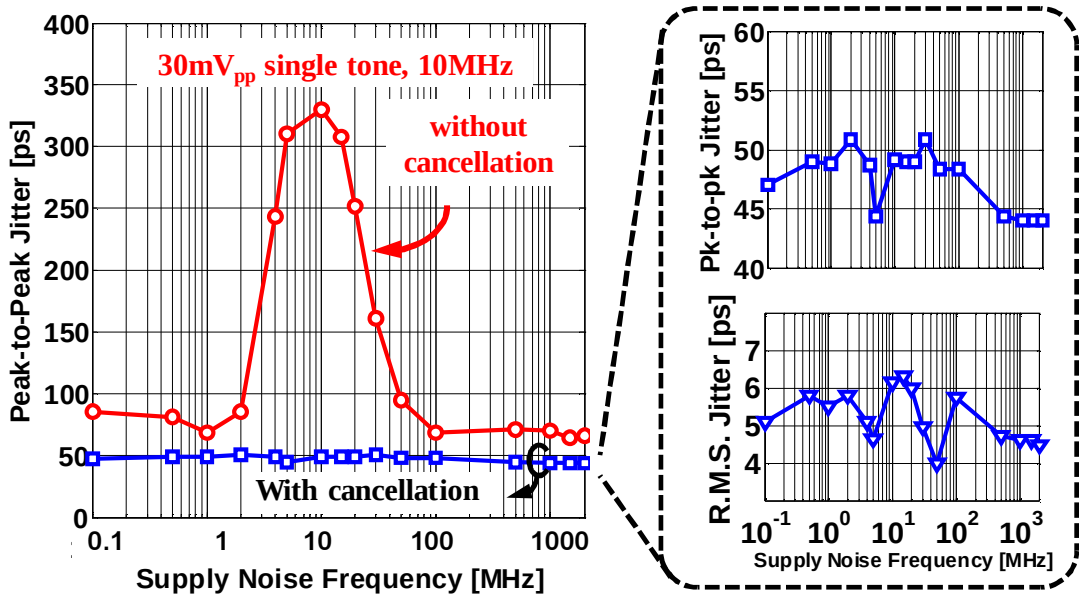


Figure 3.23: Measured peak-to-peak jitter as a function of supply noise frequency at 1.5GHz output frequency.

sensitivity is independent of the supply noise frequency, which validates our earlier assumption that the cancellation gain calibrated at a single test signal frequency is optimal at all supply noise frequencies.

The measured rms jitter, plotted as a function of the 5-bit calibration code at 1.5GHz and 2GHz output frequencies in Fig. 3.25, illustrates that the supply noise sensitivity is a function of DCO frequency. In both cases, the on-chip calibration loops converged to the optimum codes of 4 and 16, respectively.

The effect of DC level variation of the supply voltage is obtained by varying the supply voltage by ±5%. The rms jitter with three different supply voltages is plotted as a function of the calibration code in Fig. 3.26. The results show that the supply noise sensitivity is also a function of the DC level of the supply voltage. As with different supply noise frequencies, and different operating frequencies, the calibration loop converged to the optimum code for these different supply voltages.

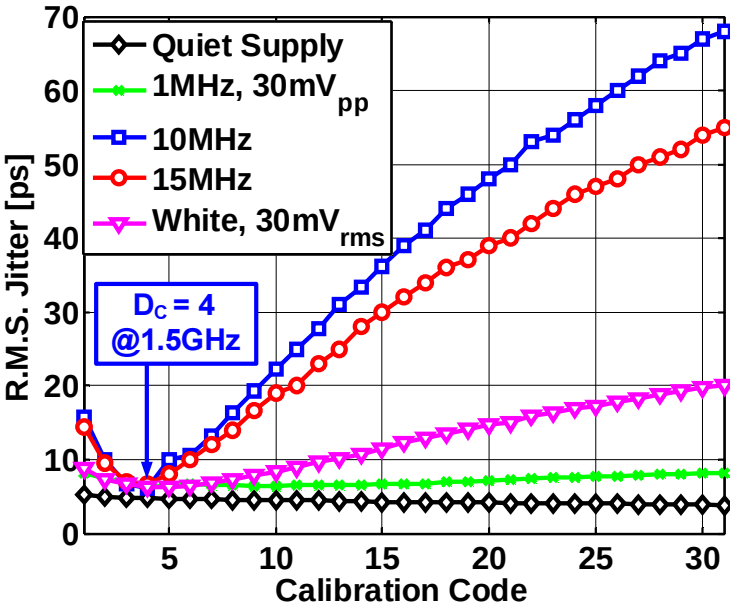


Figure 3.24: Measured rms jitter for different supply noise conditions.

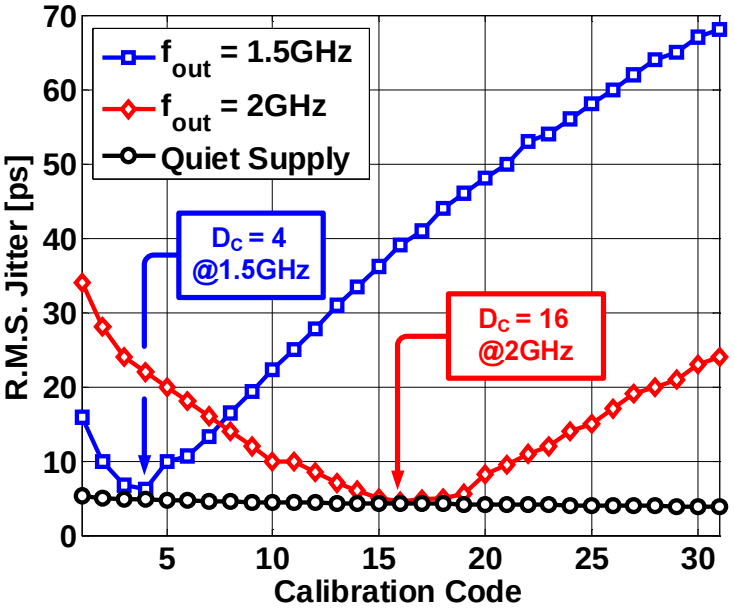


Figure 3.25: Measured rms jitter as a function of the 5-bit calibration code at 1.5GHz and 2GHz output frequencies.

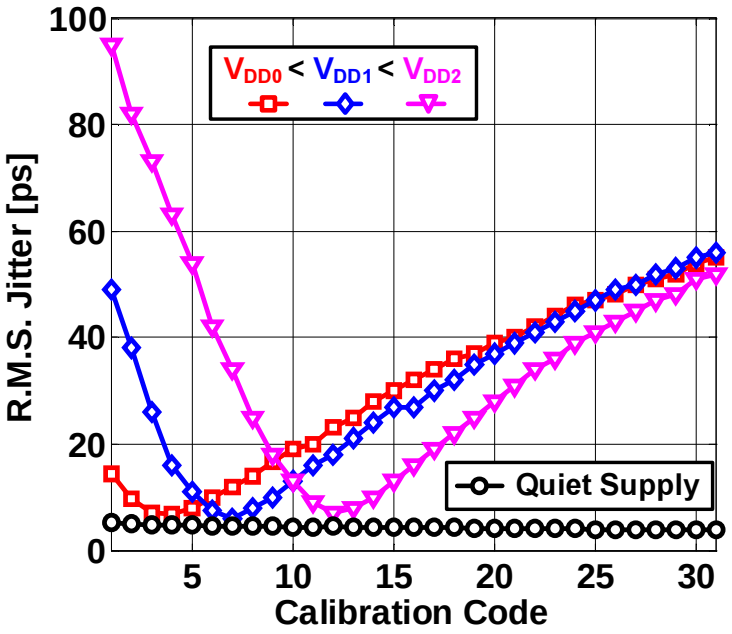


Figure 3.26: Measured rms jitter at three different supply voltages.

The range of the proposed background cancellation scheme is evaluated by plotting the measured worst-case peak-to-peak jitter over the entire range of DPLL output frequencies as shown in Fig. 3.27. With a $30mV_{pp}$, 10MHz sinusoidal supply noise tone, accurate cancellation is achieved over 800MHz-to-2.5GHz output frequencies, while only partial cancellation is achieved outside this range. This is due to the dynamic range limitation of the cancellation circuitry. The optimum calibration code saturates outside the cancellation range, resulting in only partial cancellation of supply noise (see Fig. 3.28).

The cancellation range can be further extended either by increasing the dynamic range of the calibration current I_B or increasing the size of noise cancelling transistors M_{n1}-to-M_{n6} or both. It is worth mentioning that in the presence of $20mV_{rms}$ white gaussian noise ($\approx 130mV_{pp}$), the peak-to-peak jitter did not degrade over the entire range of operating frequencies, 400MHz-to-3GHz. The rela-

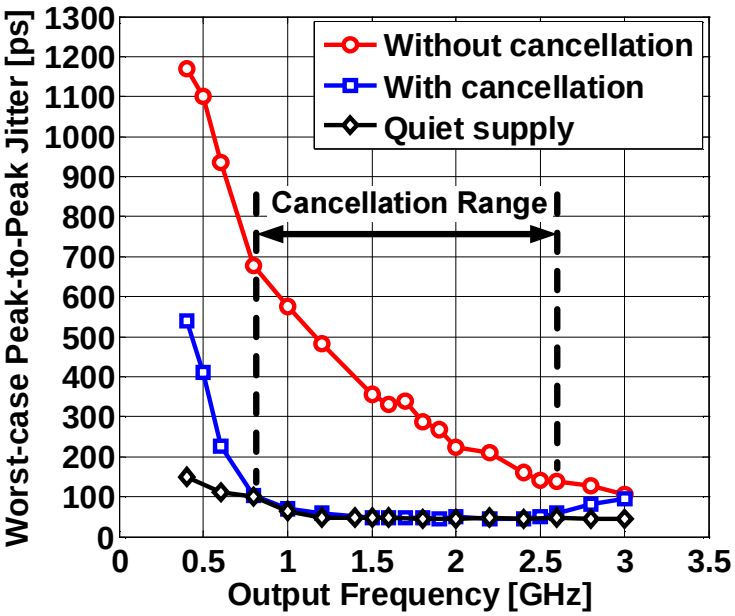


Figure 3.27: The worst-case peak-to-peak jitter versus DPLL output frequency for a 30mV$_{pp}$, 10MHz supply noise tone.

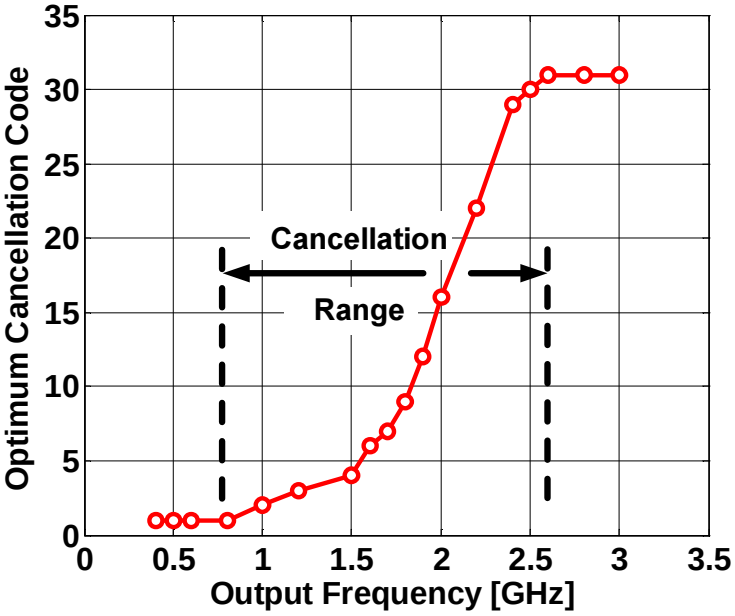


Figure 3.28: Optimum calibration code versus output frequency, illustrating the cancellation range as 0.8GHz-to-2.5GHz.

tively high jitter floor limits the ability to measure the actual effectiveness of the cancellation scheme, therefore, frequency domain measurements using a test setup similar to that outlined in [17] were performed. The power supply noise rejection (PSNR) curve obtained with supply noise amplitude of 30mV$_{pp}$ is plotted in Fig. 3.29. The worst-case PSNR of -10dB with cancellation enabled represents an improvement of 32dB over the PSNR without cancellation.

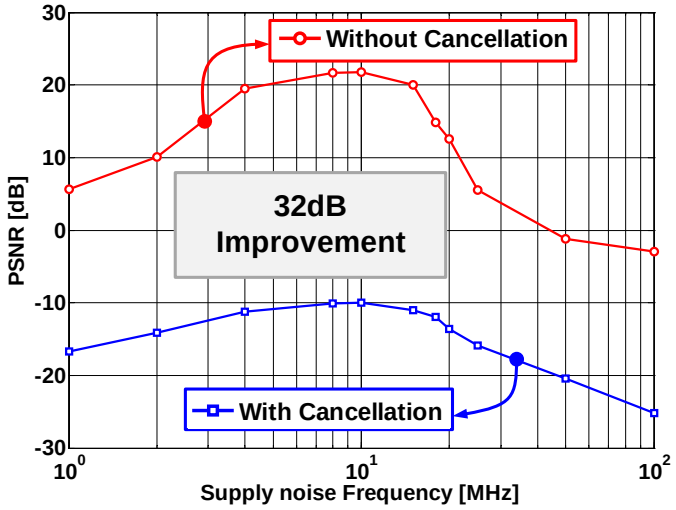


Figure 3.29: The measured power supply noise rejection (PSNR) performance.

The measured power consumption of the proposed DPLL over the entire range of output frequencies is plotted in Fig. 3.30. The cancellation circuitry (including noise cancelling transistors, on-chip test signal generation, and background calibration logic) consumes less than 340μW which amounts to only 9.5% of total DPLL power dissipation at 1.5GHz output frequency.

The performance of the prototype DPLL is summarized in Table 6.1 and compared with the state-of-the-art PLLs in Table 3.2. Compared to PLLs with supply noise cancellation, the normalized power of the proposed DPLL is 6 times lower. The worst-case supply noise rejection is better than -10dB without using any decoupling capacitor.

Table 3.1: DPLL Performance Summary

Technology			0.13μm		
Frequency Range			0.4-to-3GHz		
Supply Voltage			1.0V		
Worst-Case Jitter [ps] R.M.S./Peak-to-Peak	Operating Frequency		800MHz	1.5GHz	2.5GHz
	Quiet Supply		11/100	5/47	4.6/47
	30mV$_{pp}$ single tone	w/o cancellation	208/630	101/330	32/131
		w/ cancellation	17/104	6.2/50	6.1/50
	20mV$_{rms}$ white noise	w/o cancellation	48/340	22/170	8/76
		w/ cancellation	12/101	5/50	4.8/50
Power Consumption		Total	2.1mW	2.65mW	3.1mW
		Analog (VCO)	41%	52%	54%
		Analog (Other)	41%	35%	35%
		Digital	2%	3.5%	4%
		Cancellation	16%	9.5%	7%
Area			0.08mm^2		

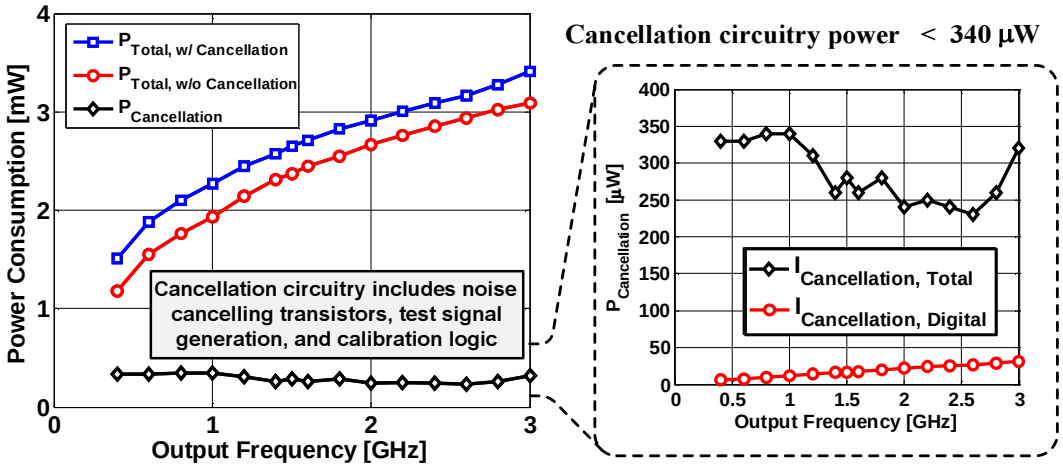


Figure 3.30: Measured power consumption versus output frequency (400M-3GHz).

3.5 Summary

Supply noise *cancellation* is proposed as an attractive alternative to conventional *suppression* techniques implemented using supply-regulated architectures. A digital phase-locked loop (DPLL) that employs noise *cancellation* to mitigate performance degradation due to noise on the ring oscillator supply voltage is presented. A deterministic test signal based digital background calibration is used to accurately set the cancellation gain and thus achieve accurate cancellation under different process, voltage, temperature, and frequency conditions. A hybrid, linear proportional control and bang-bang digital integral control, is used to obviate the need for a high resolution time-to-digital converter and reduce jitter due to frequency quantization error.

Table 3.2: DPLL Performance Comparison with State-of-the-Art Designs

	This Work	JSSC07 [23]	JSSC03 [22]	JSSC11 [24]	JSSC09 [17]
Technology	0.13μm	0.13μm	0.25μm	90nm	0.18μm
Area [mm^2]	0.08	0.064	0.028	0.36	0.093
Supply [V]	1.0	1.0	2.5	1.0	1.8
Freq. Range [GHz]	0.4-3.0	0.5-2.0	0.13-1.6	0.7-3.5	0.5-2.5
Output Freq. [GHz]	3	1.4	1	2.5	1.5
Power [mW/GHz]	1.13	6.9	10	0.64	2.6
Jitter RMS/PP [ps] w/o Supply Noise	4.6/44	3.9/30	3.3/28.9	1.6/11.6	1.9/15
Jitter RMS/PP [ps] w/ Supply Noise @ Noise freq.	5/46 20mV$_{pp}$ @10MHz	3.97/33.2 10mV$_{pp}$ @10MHz	N/A N/A	N/A N/A	4.9/25 200mV$_{pp}$ @8.85MHz
Worst-case Supply Noise Freq.	10MHz	10MHz	N/A	N/A	8.85MHz
Supply Noise Mitigation	Yes Cancellation (Background)	Yes Cancellation (Foreground)	Yes Cancellation (No-calib.)	No N/A	Yes Regulation
PSNR [dB]	-10	N/A	N/A	N/A	-28
Implementation	Digital	Analog	Analog	Digital	Analog

CHAPTER 4. LOW POWER DIGITAL PLL WITH SUPPLY-NOISE IMMUNITY

There are many challenges in designing a clock multiplier that is robust to supply noise while consuming low power. In the previous chapter, supply noise cancellation approach was proposed to mitigate performance degradation due to noise on the ring oscillator supply voltage.

In this chapter, we focus on the most common approach to mitigate supply noise, which is supply noise suppression (regulation). The issues associated with the design of a conventional digital PLLs with supply noise regulation, such as the effect of loop dynamics and regulator bandwidth on supply noise rejection, are addressed. The regulator bandwidth requirements are first discussed in conventional digital PLL architectures. Then a DPLL architecture is presented to overcome these drawbacks. The proposed supply regulated DPLL allows using a low power regulator, by decoupling the regulator bandwidth from the PLL bandwidth, and improves supply noise rejection.

4.1 Supply Regulated DPLLs

The block diagram of a supply regulated digital PLL is shown in Fig. 4.1. It consists of a time-to-digital converter (TDC), a digital loop filter (DLF), a supply regulated digitally controlled oscillator (DCO), and a feedback divider. The TDC generates a digital word proportional to the difference between the reference and feedback clock.

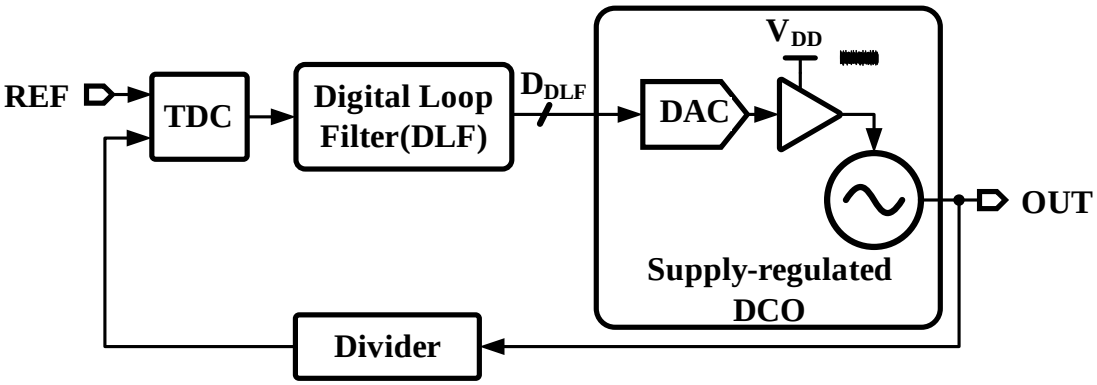


Figure 4.1: Supply regulated digital PLL block diagram.

The sign of the phase error is then fed to the DLF, which consists of a proportional and integral paths (denoted as K_{BB} and K_I in Fig. 4.1, respectively). The proportional-integral filter realizes the Type-II PLL response and a digital-to-analog converter (DAC) interfaces the DLF to the voltage controlled oscillator (VCO). The regulator shields the VCO from supply noise. Then, the output of the DCO is divided by the feedback divider and fed to the TDC input.

At steady state, DPLL exhibits a bang-bang behavior, and the TDC switches between two values corresponding to the sign of the phase error. This results in a nonlinear dynamics of the digital PLL which manifests as limit cycle behavior caused by the loop delay (D_{DPLL}), which is the number of z^{-1} delay elements operation in the loop. Loop delay increases the period of the limit-cycles and affects the output clock phase-noise spectrum frequency distribution of the DPLL, and results in undesirable peaking. This worsens the output jitter, both rms and peak-to-peak in a linear way. For instance, for $D_{DPLL} = 0$ the output jitter toggles between two values and the DPLL output will show a strong fundamental tone peaking at half the reference frequency $1/(2T_{REF})$.

Higher values of D_{DPLL} move the peaking toward lower frequencies. In gen-

eral, the peaking of a DPLL will occur at frequency $1/(2(1+2D_{DPLL})T_{REF})$.

In [32], it was proven that jitter minimization can be achieved by minimizing K_{BB}, loop delay, and K_I/K_{BB}. For a fixed K_{BB} and loop delay, increasing K_I always worsens jitter. In general, K_I and the ratio K_I/K_{BB} are determined by the transient behavior of the DPLL, while loop delay is fixed by implementation. Therefore, the minimum jitter can be achieved for very small values of K_{BB}. A very small value of K_{BB} will cause the DPLL to be close to instability and the jitter increases dramatically. Reasonably big-enough values of K_{BB} will stabilize the DPLL, however increasing it further will cause jitter to grow, due to the increase in quantization error in the proportional path (see Fig. 4.2).

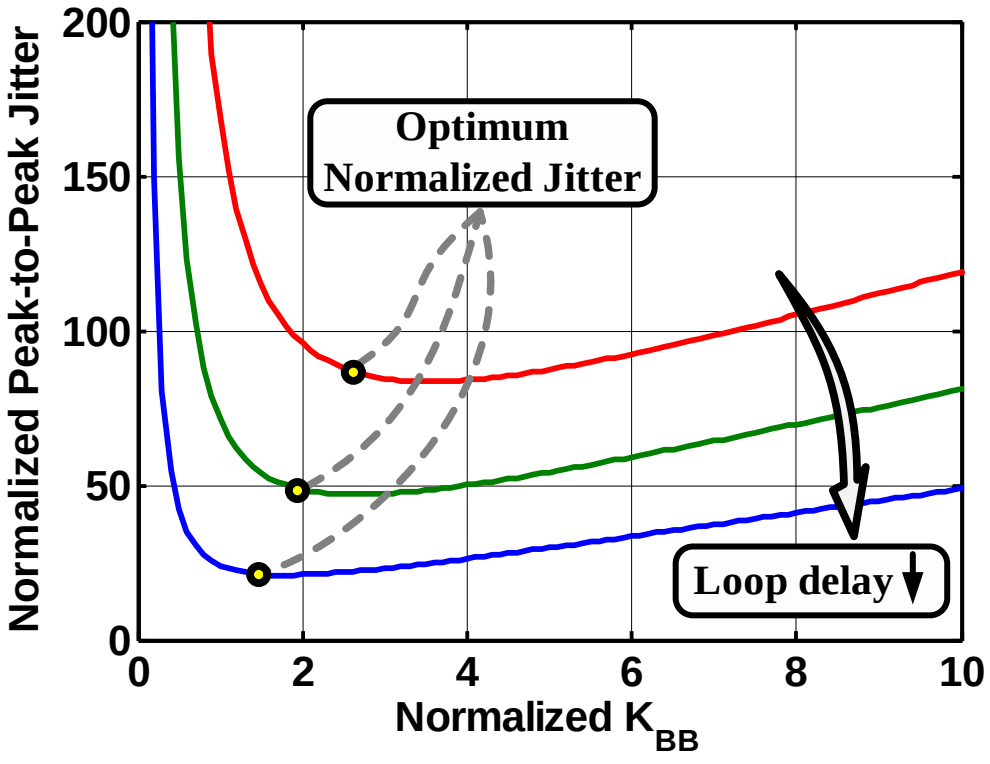


Figure 4.2: Peak-to-peak jitter plotted as a function of the normalized proportional path gain, K_{BB}.

For values of the K_{BB} approaching zero, the peak-to-peak jitter increases as $1/K_{BB}^2$ due to being close to the DPLL instability region, which is further degraded by the oscillator phase-noise. For large values of K_{BB}, the jitter increases linearly.

The minimum jitter can be observed at an optimum value of proportional path gain, $K_{BB,Opt} \approx (1.38 + 1.88D_{DPLL})K_I$, and the corresponding normalized peak-to-peak jitter can be found to be about $5.22(1 + D_{DPLL})^2$. Therefore, even when for an optimized K_{BB} value, the optimum jitter still depends on D_{DPLL}, thus increasing D_{DPLL} increases the output jitter.

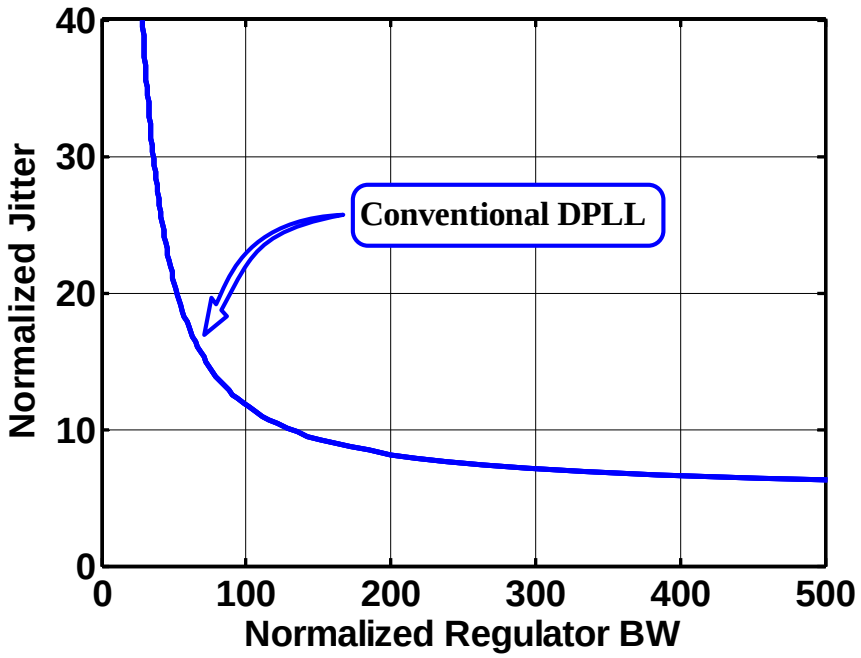


Figure 4.3: Peak-to-peak jitter versus regulator bandwidth in conventional PLLs.

The highly non-linear nature of digital PLLs makes the supply-noise sensitivity depends on several parameters such as loop delay, proportional path gain, and jitter. As a result, it is difficult to predict supply-noise to output jitter transfer characteristics. A low bandwidth regulator in the proportional path increases the loop delay dramatically and makes the peaking exist in the output phase-noise

spectrum worse, thus necessitating the use of a very power hungry wide-bandwidth regulator. The peak-to-peak optimum jitter, obtained at $K_{BB,Opt}$, is plotted as a function of the normalized regulator bandwidth in Fig. 4.3.

We propose a supply-regulated DPLL that seeks to improve supply-noise immunity without increasing loop delay, as illustrated in Fig. 4.3. This can be achieved by employing the regulator in the proportional path only. Consequently, loop delay does not increase if regulator bandwidth is lowered, and output jitter is not degraded.

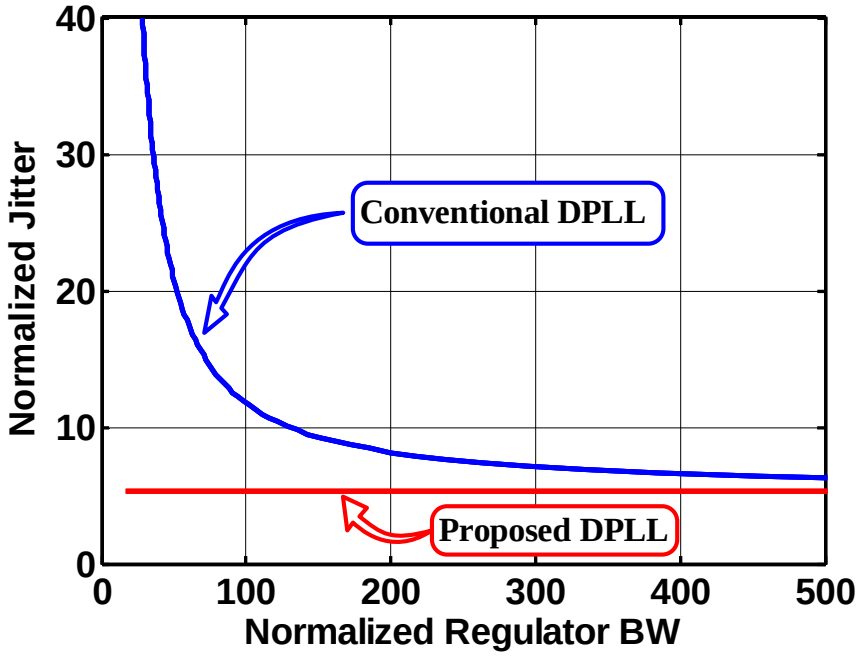


Figure 4.4: Peak-to-peak jitter versus regulator bandwidth for the proposed DPLL.

4.2 Proposed DPLL Architecture

The block diagram of the proposed supply-noise regulated Type-II Digital PLL (DPLL) is shown in Fig. 4.5. It consists of separate bang-bang proportional and digital integral paths, a digitally controlled oscillator, a replica regulator, and a feedback divider. A flip-flop (FF) acts as an early/late detector on classical 3-state PFD outputs and drives the oscillator and the digital accumulator to implement the proportional and integral controls, respectively. Because the low bandwidth digital integral path suppresses phase quantization error of the FF, the dithering jitter is mainly caused by the proportional path. A 1-to-4 de-multiplexer eases the speed requirements of fully synthesized digital control logic.

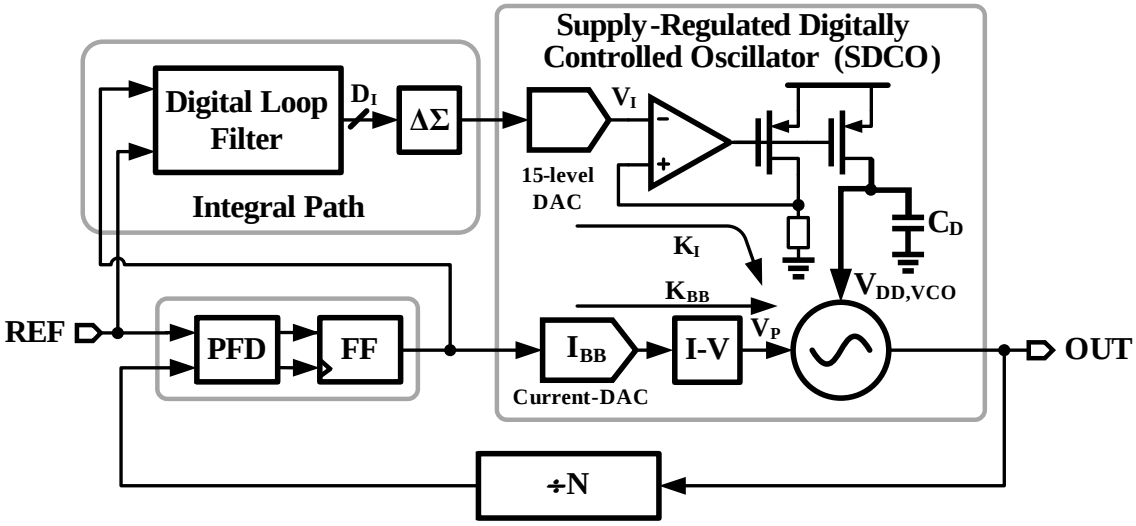


Figure 4.5: Block diagram of the proposed DPLL.

The digital modulator truncates the 14-bit accumulator output, D_I, to 15-levels and drives a current-mode DAC. A 2^{nd} order passive low-pass filter suppresses the out-of-band quantization error and drives the integral control voltage input of the oscillator. Because the regulator is placed in the low-bandwidth integral

path, high frequency supply noise rejection can be achieved by introducing a low-frequency pole in the regulator's supply noise transfer function [17].

All digital building blocks are synthesized using standard cells. For the proposed DPLL, the TDC is implemented using a phase-frequency detector (PFD) whose output is sampled using a flip-flop which provides the bang-bang phase detector output (see Fig. 4.5). The PFD is implemented using the well-known three-state architecture and is implemented using the pass transistor structure [27].

The block diagram of the digital loop filter is shown in Fig. 4.6. The digital loop filter is a simple digital accumulator which is driven by the sign of the phase error. A 1-to-4 de-multiplexer is used to ease the speed requirements of the fully-synthesized 18b accumulator.

The impact of quantization error on output jitter is minimized by lowering the time constant of the digital accumulator. Lowering the bandwidth does not exacerbate oscillator phase noise, and the dithering jitter caused by excessive loop delay is reduced by ignoring the accumulators lower 4 LSBs. In other words, only the 14MSBs are fed to the high resolution $\Delta\Sigma$ DAC whose details are discussed next.

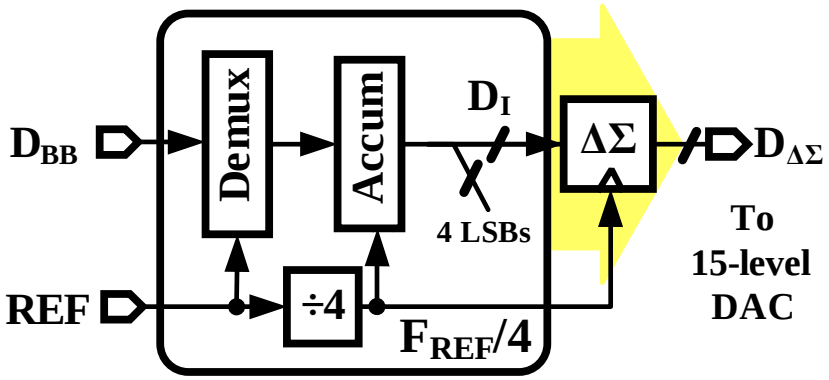


Figure 4.6: Block diagram of the digital loop filter (DLF).

The block diagram of the digital-to-analog converter used in the integral

path is shown in Fig. 4.7. A 14-bit second order synthesized digital delta-sigma modulator (DSM) truncates the accumulator 14-bit digital word, D_I, to 15-levels and drives a 15-element current mode DAC.

A current-mode DAC, consisting of 15 nominally matched current sources, converts the digital input to an equivalent output current (see Fig. 4.7). Resistor R converts the DAC output current to voltage. A second order passive low-pass filter (LPF), with a 500kHz bandwidth, suppresses out-of-band quantization error and generates control voltage of the oscillator.

The delta-sigma DAC architecture eases hardware requirements, however increased loop latency introduced by the LPF phase shift degrades the jitter performance. Ignoring the lower 4 LSBs of the accumulator output and passing only the 14 most significant bits to the DAC suppresses the dithering jitter.

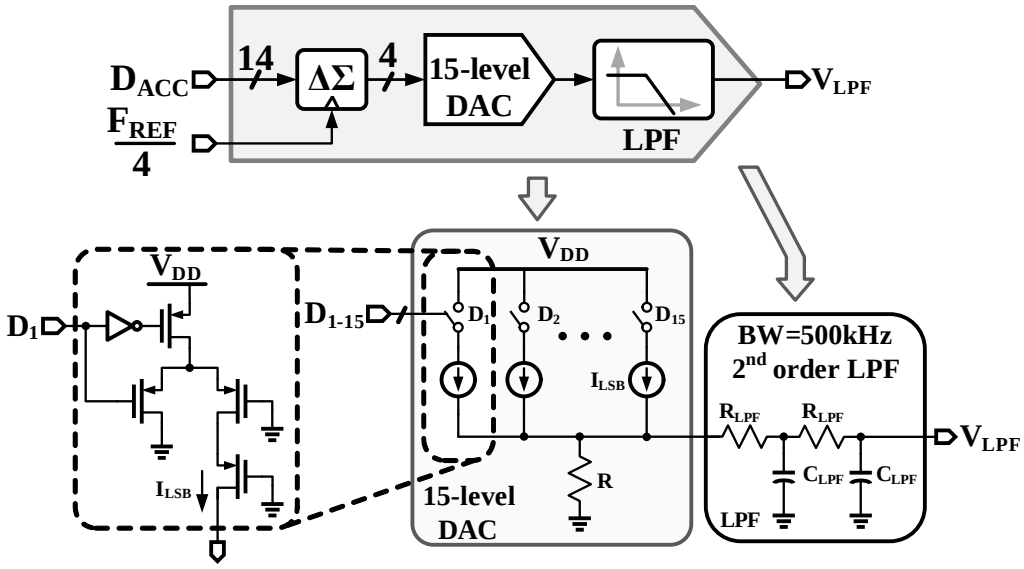


Figure 4.7: Block diagram of the delta-sigma DAC, and circuit schematic of the 15-level current mode DAC and post filter.

The schematic of the replica-biased regulator, optimized to achieve high supply-noise rejection is shown in Fig. 4.8. It buffers the DLF control voltage,

and generates the virtual supply voltage of the oscillator denoted as $\mathrm{VDD_{VCO}}$. Because the regulator is placed in the low-bandwidth, wide-band supply noise rejection is achieved by introducing a low-frequency pole ω_D at the VCOs supply node [17, 20].

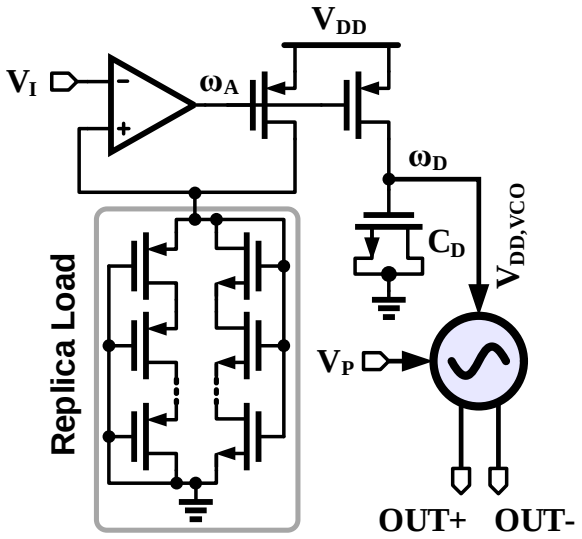


Figure 4.8: Schematic of the high PSRR replica-biased regulator.

By making ω_D to be lower than the pole at the amplifier output, ω_A, the peaking in the power supply rejection present in conventional regulators can be eliminated. By closing the feedback around the replica of the VCO, a replica-biased regulator facilitates an area efficient means to improve PSRR by introducing a low frequency pole ω_D. The simulated PSRR curves for various values of the bypass capacitance $\mathrm{C_D}$ are shown in Fig. 4.9 illustrate this improvement. As expected, increasing $\mathrm{C_D}$ lowers ω_D and improves PSRR beyond ω_A. The replica load is implemented with stacked diode-connected devices to achieve good matching between the VCO and the replica load.

The schematic of the ring oscillator is shown in Fig. 4.10 . It is composed of a cascade of 3 pseudo-differential delay cells that are tuned by the integral path

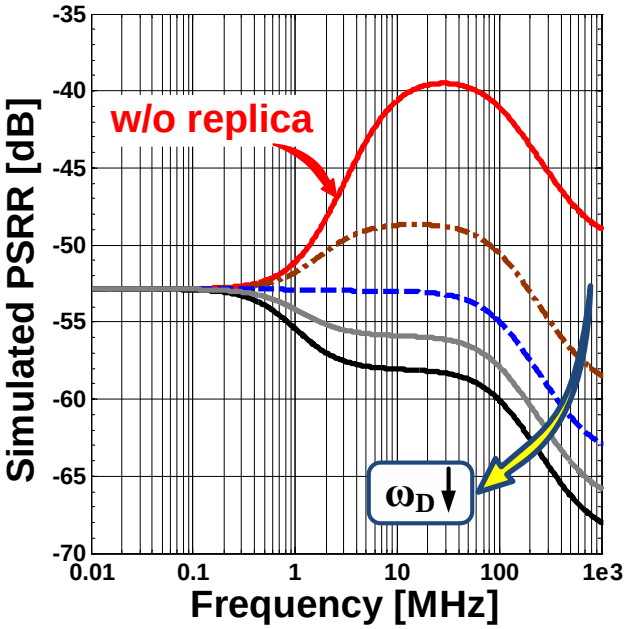


Figure 4.9: Simulated regulator PSRR for different bypass capacitor (C_D) values.

and proportional path by varying the supply voltage and the output time constant, respectively. The delay cells are implemented using CMOS inverters coupled in a feed-forward manner to ensure differential operation.

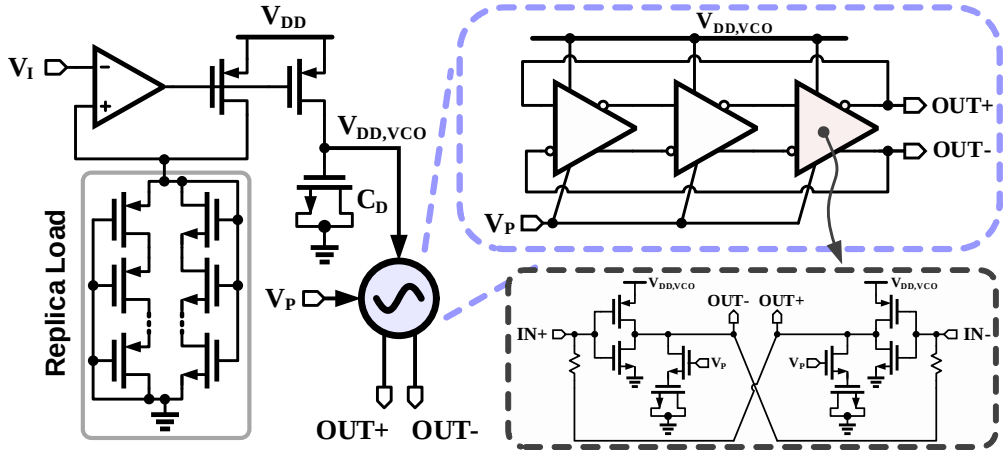


Figure 4.10: Schematic of the regulated digitally controlled ring oscillator.

4.3 Experimental Results

The DPLL clock multiplier is fabricated in a 0.13μm CMOS process and occupies 0.2mm^2 active area. The die photograph of the prototype chip is shown in Fig. 4.11. A fully-synthesized digital logic is used to reduce design time and ease portability to newer processes. The measurement setup used to characterize the prototype ICs is shown in Fig. 4.12. Supply noise measurements are performed by modulating the VCO supply with sinusoidal tone. An arbitrary waveform generator (Tektronix AWG7122B) is used to provide the input reference clock, while an RF signal generator (Fluke 6062A) is used to introduce sinusoidal noise tones on the VCO supply. Since the prototype chip's feedback divide ratio is fixed, the desired output frequency was obtained by varying the reference frequency. A communication signal analyzer (Tektronix CSA8200) was used for the time domain long-term absolute jitter measurements. The spectrum Analyzer (Tektronix RSA3308B) is used to measure the reference and noise spurs. To guarantee the fidelity of all supply noise measurements, an integrated supply noise monitor, implemented using a wide bandwidth voltage follower, is used to measure the amount of on-chip VCO supply noise.

The prototype chip consumes 1.35mW at 1.5GHz output frequency, with a nominal supply voltage of 1.1V. It operates over a wide range of output frequencies of 0.8-to-1.8GHz. Fig. 4.13 shows the measured phase noise spectrum at 1.5GHz output frequency. The measured phase noise at 1MHz offset is -112dBc/Hz. The rms jitter obtained by integrating the phase noise from 10kHz-to-100MHz is 3.2ps. Limit cycle induced peaking at around 40MHz increases the rms jitter. This peaking also exacerbate supply noise sensitivity as illustrated later.

The jitter accumulation is investigated by measuring the long-term jitter.

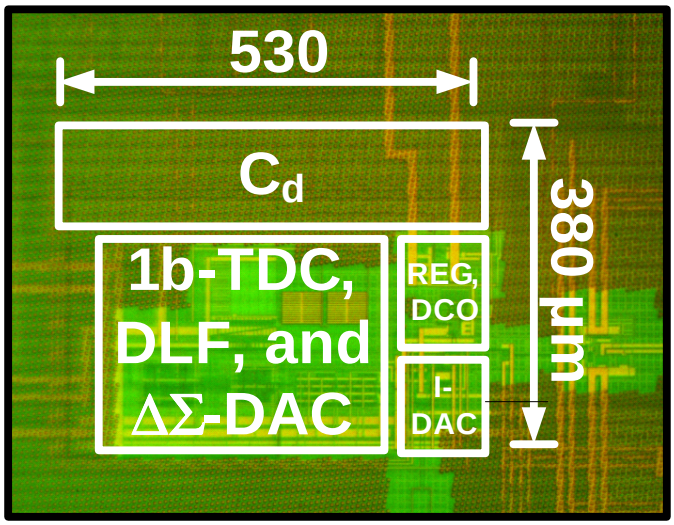


Figure 4.11: DPLL die photograph.

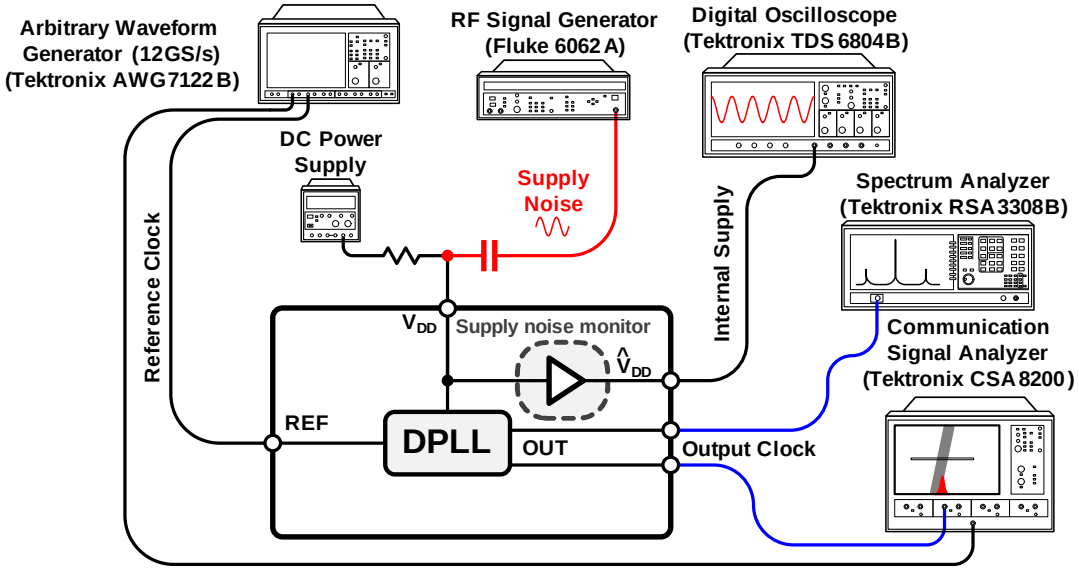


Figure 4.12: Measurement setup.

Figure 4.14 shows the measured jitter histograms at 1.5GHz output frequency, in the case of a quite supply voltage. The long-term absolute jitter measured over 1M hits is about 4.2ps$_{\text{rms}}$ and 30ps peak-to-peak.

To evaluate the effectiveness of the proposed supply noise rejection, a large

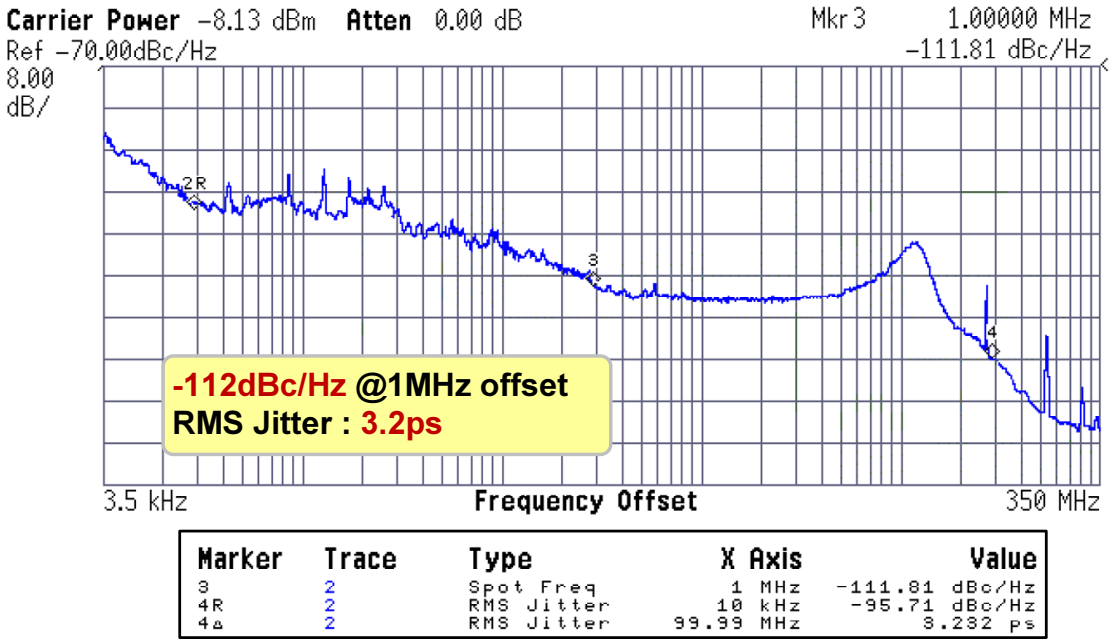


Figure 4.13: Measured phase noise at 1.5GHz output frequency.

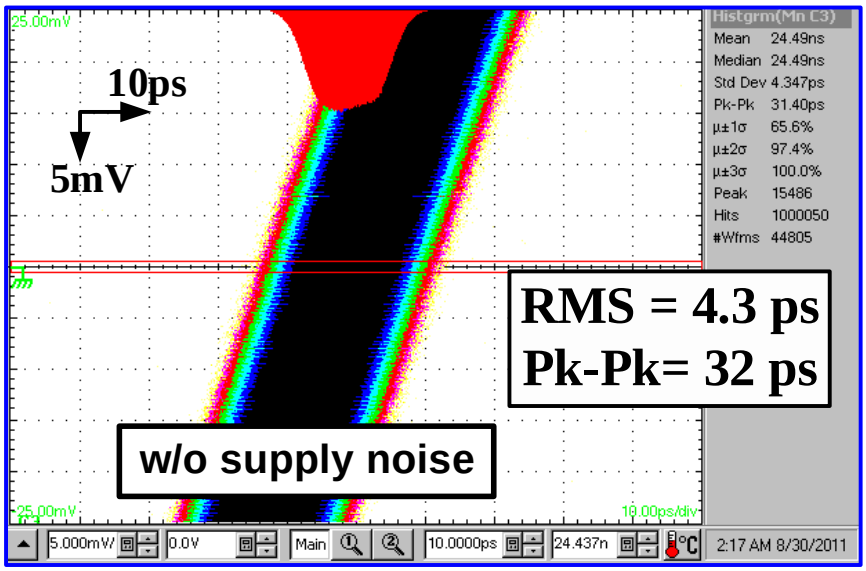


Figure 4.14: Measured long term jitter histograms (5 M hits).

200mV peak-to-peak sinusoidal tone is additionally superimposed on the supply voltage and the supply noise frequency is swept from 1MHz-to-1.4GHz. The mea-

sured peak-to-peak jitter degradation (calculated by subtracting the jitter in the absence of the supply noise) is plotted in Fig. 4.15. This plot quantifies the measured dynamic supply noise sensitivity by plotting peak-to-peak jitter degradation. In the worst case, long-term peak to peak jitter degraded by only 10ps peak-to-peak, as shown in Figure 4.16. The supply noise sensitivity of the proposed clock multiplier is $50fs_{pp}/mV_{pp}$. This plot shows that the supply noise sensitivity is highest around 40MHz, which is the peaking frequency identified earlier in the phase noise plot. This peaking is attributed to the limit cycles present in the steady-state of the DPLL as illustrated earlier.

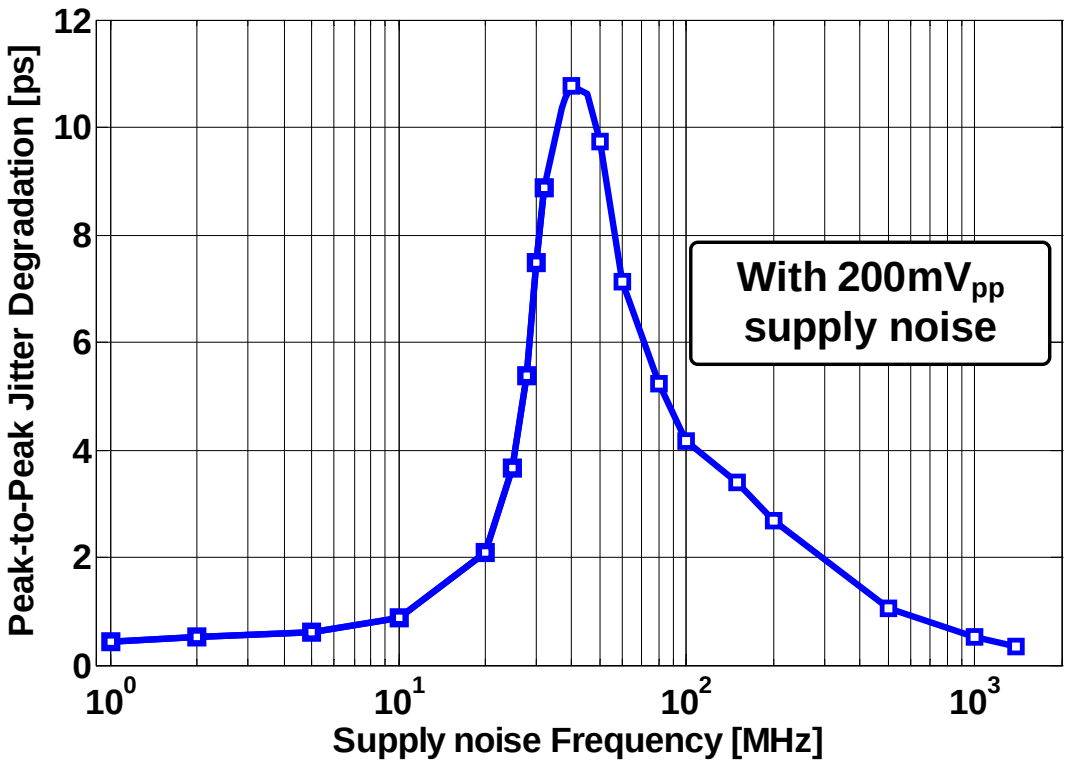


Figure 4.15: Measured peak-to-peak jitter degradation as a function of supply noise frequency at 1.5GHz output frequency.

Figure 4.17 demonstrates the impact of K_{BB} on the jitter performance of the DPLL. This is done by measuring the jitter for different values of bang-bang

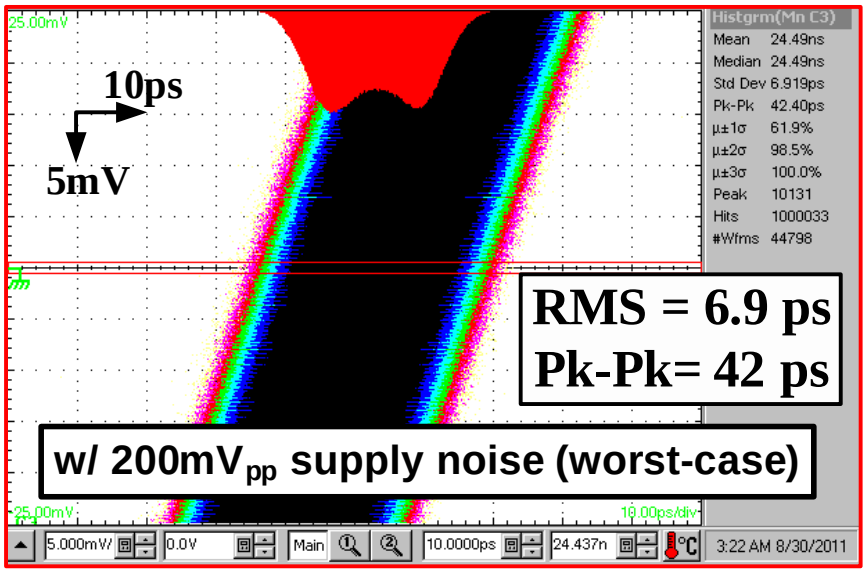


Figure 4.16: Measured worst case jitter histograms in the presence of $200mV_{pp}$ supply noise at the worst case noise frequency of 40 MHz.

proportional path gain, K_{BB} (implemented by varying I_{BB} in Fig. 4.5). In the absence of supply noise, at lower values of K_{BB} the DPLL loop is close to instability and the oscillator phase noise dominates the output jitter. As K_{BB} increases, dithering jitter caused by the increase in the step size of the proportional path starts to dominate, and the jitter increases linearly. In the presence of supply noise, the worst-case peak-to-peak jitter degradation for a 25X increase in K_{BB} remains nearly constant 9-to-12ps $_{pp}$. Thus, the supply noise rejection offered by the proposed supply regulation scheme is independent of K_{BB}, thereby allowing independent optimization of raw jitter and supply noise rejection performance.

The measured overall jitter, provided by the long-term time domain jitter histograms, includes both random and deterministic jitter components. The random jitter component is measured directly by integrating the phase noise spectrum (see Fig. 4.13). By looking at a frequency domain rather components than the time-

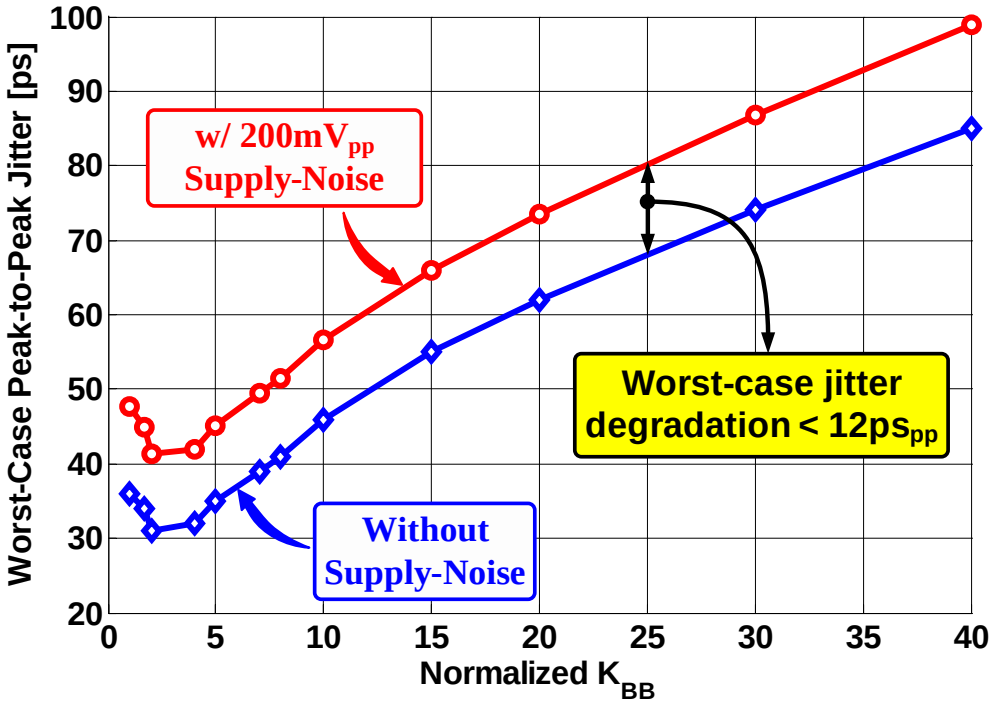


Figure 4.17: Measured worst-case peak-to-peak jitter for different K_{BB} values.

domain histograms, deterministic jitter can be estimated. Figure 4.18 shows the measured output spectrum of the DPLL in the case of quiet supply voltage. The measured reference spur is -46dBc which translates to only 2ps_{pp} deterministic jitter estimated using the following equation

$$\text{DJ}_{\text{OUT}} = \frac{2}{\pi}\text{T}_{\text{OUT}} \times 10^{\frac{\text{Spurs(dBc)}}{20}} \tag{4.1}$$

When 200mV_{pp} supply noise is introduced at the worst case noise frequency of 40MHz, the reference spurs are not degraded, and the spurs due to supply noise are found to be at about -31dBc level (see Fig. 4.19). The deterministic jitter degradation due to supply noise is found to be only 11ps peak-to-peak.

The performance of the prototype clock multiplier is summarized and com-

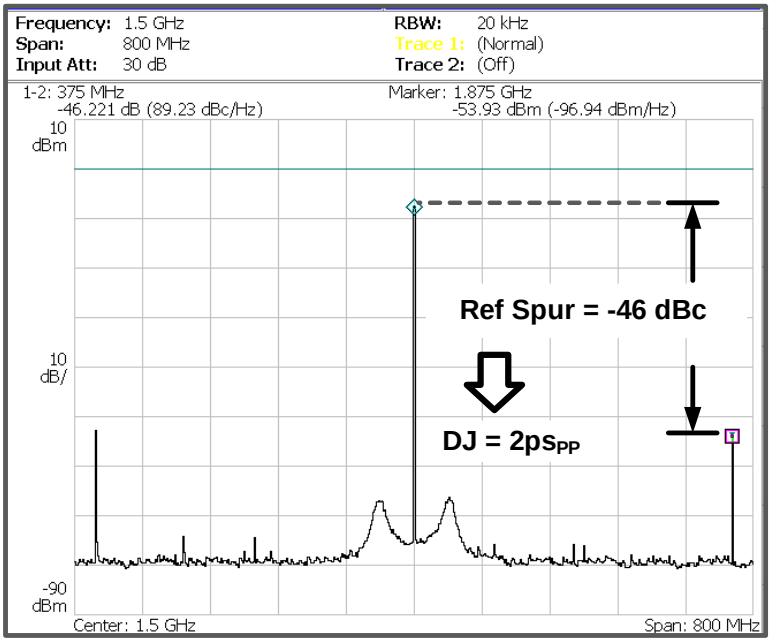


Figure 4.18: DPLL reference spurs.

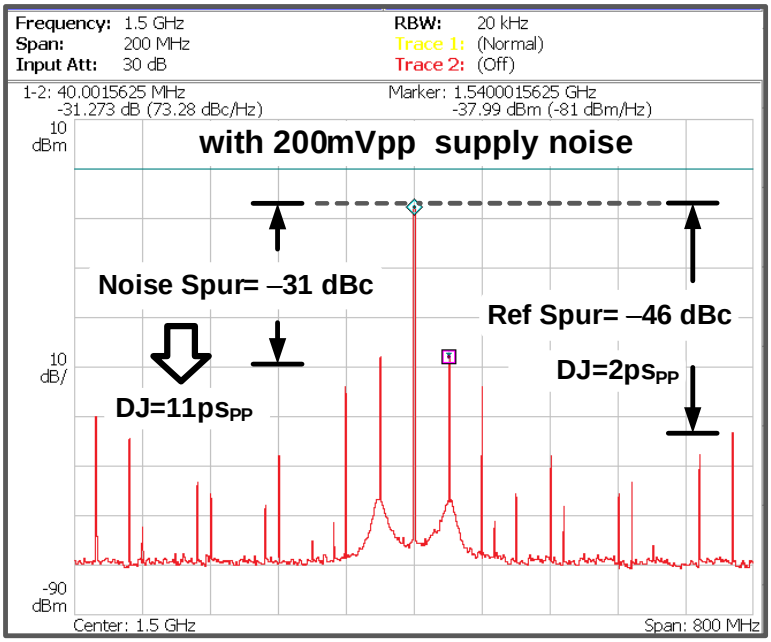


Figure 4.19: DPLL noise and reference spurs, for 200mV$_{pp}$ supply noise at the worst case supply noise frequency (40 MHz).

pared with the state-of-the-art DPLLs and supply regulated PLLs in Table 4.1. Compared to state-of-the-art DPLLs and supply regulated PLLs, the proposed DPLL archives the lowest power consumption and supply noise sensitivity.

Table 4.1: DPLL Performance Comparison with State-of-the-Art Designs.

	This Work	CICC10 [33]	JSSC09 [17]
Technology	0.13μm	65nm	0.18μm
Area [mm^2]	0.2	0.026	0.093
Supply [V]	1.1	1.0	1.8
Frequency Range [GHz]	0.8-1.8	0.2-3.8	0.5-2.5
Output Frequency [GHz]	1.5	3.0	1.5
Power [mW]	1.35	2.0	3.9
Jitter RMS/PP [ps] w/o Supply Noise	4.3/32	2.1/21.9	1.9/15
Jitter RMS/PP [ps] w/ Supply Noise	6.9/43 $200\text{mV}_{\text{pp}}, 40\text{MHz}$	3.93/34.4 $14.7\text{mV}_{\text{rms}}$	4.9/25 200mV_{pp}, 8.85MHz
Worst-case Supply Noise Frequency	40MHz	N/A	8.85MHz
Implementation	DPLL	DPLL	PLL

4.4 Summary

A supply-regulated DPLL that seeks to improve supply-noise immunity without increasing loop delay is presented. The proposed DPLL uses a low power regulator only in the integral path, and achieves low jitter, low power consumption, and immunity to supply noise. The supply noise rejection offered by the proposed supply regulation scheme is independent of K_{BB}. This allows independent optimization of raw jitter and supply noise rejection performance.

CHAPTER 5. DIGITAL CLOCK MULTIPLICATION TECHNIQUES USING MULTIPLYING DELAY-LOCKED LOOPS

In the previous chapters, the two commonly used supply noise mitigation techniques are addressed. However, a DPLLs supply noise rejection is limited by the DPLL architecture. In this chapter, an attractive multiplying DLL (MDLL) alternative for clock multiplication is investigated to improve supply noise rejection.

DPLLs suffer from a unique TDC/DCO coupled noise bandwidth tradeoff, which is illustrated in Fig. 5.1. The TDC noise is low pass filtered, while oscillators phase noise is high pass filtered. This conflicting bandwidth requirements to simultaneously suppress TDC quantization error and oscillator phase noise poses several design challenges. For instance, a lower bandwidth suppresses TDC quantization error but cannot adequately suppress oscillator phase noise and vice versa. Consequently, either a high resolution TDC or a low noise oscillator is needed to achieve low jitter at the expense of large power dissipation and area [12]. For example, an excellent phase noise LC-DCO is combined with a very low DPLL bandwidth to suppress the TDC quantization error in [5].

The quantization error in the DCO frequency imposes a DPLL operating range-resolution tradeoff. The DCO resolution can be improved only by limiting its tuning range, for a given hardware complexity. A reasonably wide tuning range is achieved using a ring-DCO at the expense of larger output clock jitter [6, 7], while a high resolution DCO with narrow tuning range has been used to achieve good jitter performance [5]. Because of these difficulties, designing a low jitter wide

tuning range digital PLL requires optimization of conflicting design parameters.

To overcome jitter accumulation and the coupled noise bandwidth tradeoff, a new digital MDLL (DMDLL) architecture that overcomes conventional MDLLs and DPLLs drawbacks is presented. The DMDLL achieves low jitter without either using a high resolution TDC or low phase noise DCO while being able to operate over a wide range of frequencies. Because supply noise always degrade the clock multiplier performance, the DMDLL employs a low power regulator to achieve excellent supply noise rejection.

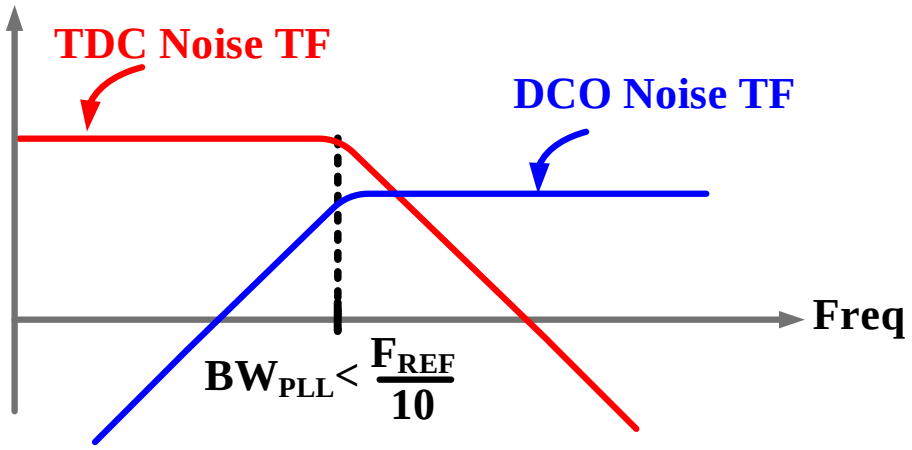


Figure 5.1: Coupled TDC/DCO bandwidth tradeoff for DPLLs.

The rest of the chapter is organized as follows. Section 5.1 describes non-conventional MDLLs. In Section 5.2 a new highly digital MDLL architecture that overcomes the drawbacks of conventional MDLLs is presented to achieves superior jitter performance and supply noise rejection. The circuit implementation details of key building blocks are illustrated in Section 5.3. Section 5.4 shows the experimental results obtained from the prototype IC. Finally, key contributions of this work is summarized in Section 5.5.

5.1 Conventional MDLLs

Multiplying delay-locked loops (MDLL) have been recently proposed for clock multiplication to overcome jitter accumulation in PLLs [15, 16]. It combines PLLs with MDLLs in a special configuration to reduce jitter accumulation. The block diagram of a conventional MDLL is shown in Fig. 5.2. It consists of a phase detector, loop filter, multiplexed ring oscillator, and selection logic. Unlike in a PLL, the reference clock edge is periodically injected into the oscillator based on selection logic. The reference edge replaces the VCO edge every N cycles, where N is chosen to determine the multiplication ratio. The select logic generates a pulse during which the positive edge of the VCO is replaced by the positive edge of the reference clock (illustrated by timing diagrams in Fig. 5.3) . Therefore, any jitter accumulation present at the VCO output will be reset accordingly. This resetting action makes the MDLL behave as a 1st order feedback system, thus making it unconditionally stable, and also leads to superior noise suppression [16].

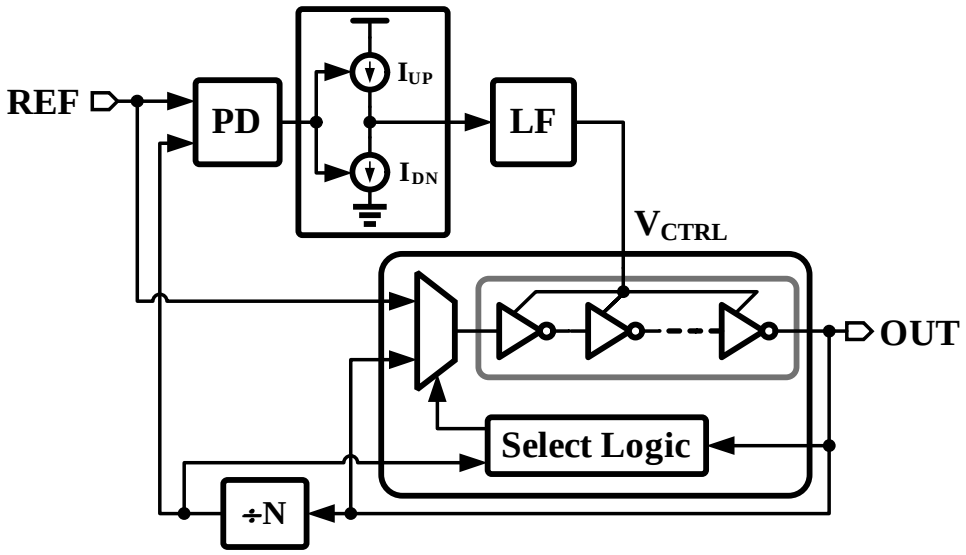


Figure 5.2: Conventional MDLL block diagram.

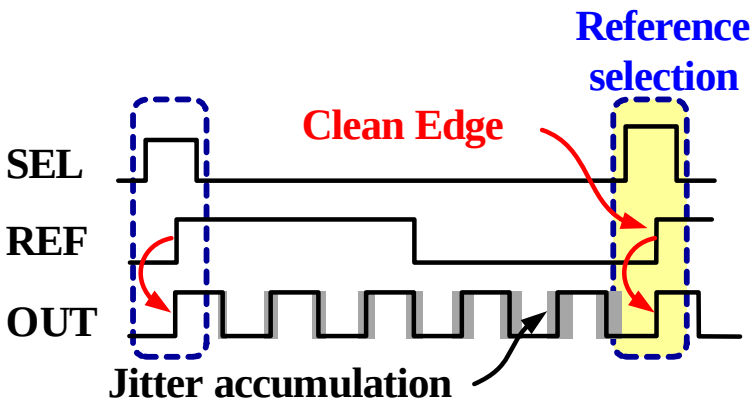


Figure 5.3: MDLL timing diagram illustrating the periodic reference injection.

While analog MDLL clock generators have been shown to have superior random jitter performance compared with PLLs [15, 16, 34, 35], their performance is limited by the static phase offset (SPO) induced deterministic jitter degradation. In the presence of phase detector and charge pump current mismatches, the MDLL locks with static phase offset denoted here by ΔT. In practice, ΔT can be as high as 20-to-30ps, which severely limits the deterministic jitter performance of the MDLL. By obviating the need for a charge pump, a digital MDLL implementation can eliminate the biggest source of deterministic jitter. In [36], a digital MDLL was proposed using a high resolution TDC to eliminates SPO and achieves low jitter. The TDC compares cycle periods of the MDLL output, and deterministic jitter is directly seen as the difference between the periods of MDLL output. While this digital MDLL implementation reduces static phase offset and achieves low jitter, it still requires a high resolution power hungry TDC and is also susceptible to supply noise. To overcome the drawbacks of conventional MDLLs, we present a highly digital MDLL architecture that uses only a 1b TDC and low power supply regulator to achieve excellent jitter performance and supply noise immunity.

5.2 Proposed DMDLL Architecture

A simplified block diagram of the proposed digital MDLL is shown in Fig. 5.4. Leveraging the decoupled TDC and oscillator noise bandwidth tradeoff, the MDLL uses a 1b TDC to detect the sign of the phase error. The TDC output is then fed to the digital loop filter which drives the digitally-controlled multiplexed oscillator toward phase lock. The divider in combination with the selection logic resets jitter accumulation in the oscillator. To achieve a wide operating range, a fully synthesized frequency-locking loop (FLL) is used to drive the digitally multiplexed ring oscillator (DXRO) toward frequency lock. Using separate DACs in the FLL and MDLL relaxes the stringent quantization error requirements otherwise present in a shared DAC architecture. A low drop-out replica-biased regulator is used to shield the oscillator supply, which makes the proposed DMDLL immune to supply noise. Since the regulator is embedded in very low bandwidth FLL, the regulator bandwidth can also be chosen to be low. This allows to improve regulators PSRR with minimal power penalty, as will be discussed later. Before presenting the details of the regulator design, It is instructive to look at the supply noise rejection properties of an MDLL.

The process of jitter accumulation in VCOs is depicted in Fig. 5.5, and accumulated jitter in a VCO is plotted as a function of measurement interval ΔT. This reveals that jitter accumulates indefinitely in an open loop VCO. When the VCO is embedded in a PLL, the feedback prevents indefinite jitter accumulation [37], and the PLL loop suppresses VCO noise within its bandwidth. Because this bandwidth is at most one tenth the reference frequency, the jitter suppression is limited as well. However, when the same VCO is embedded in an MDLL loop its jitter accumulation is reset periodically due to the injection of reference clock into

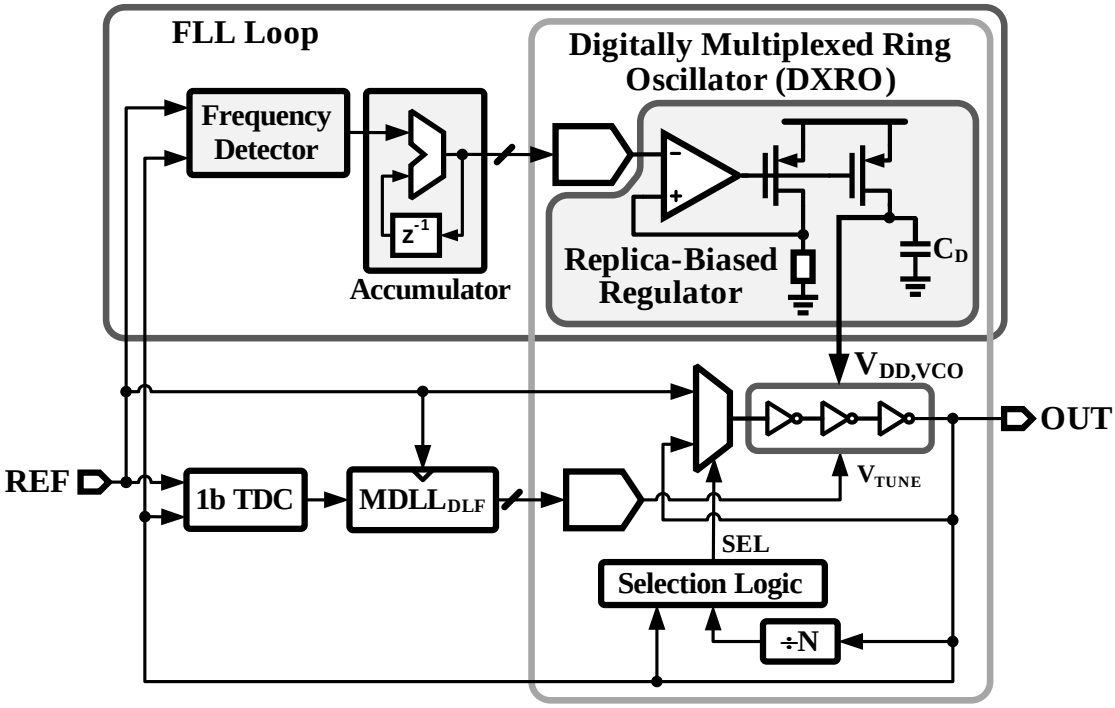


Figure 5.4: Proposed digital MDLL block diagram.

the VCO. As a result, MDLL suppresses VCO noise within a bandwidth which is approximately one fourth of the reference frequency, and this is at least twice the PLL bandwidth.

The jitter suppression in an MDLL can also be seen clearly in the frequency domain phase noise plot shown in Fig. 5.6. In both the PLL and MDLL, the VCO phase noise is high-pass shaped by the loop bandwidth. Because MDLL bandwidth can be at least 2.5× higher than that of a PLL, the in-band phase noise in an MDLL is at least 8dB lower than that of a PLL. Interestingly, the reference injection that reduces jitter accumulation in MDLLs also makes them more immune to supply noise compared to PLLs. Because supply noise also causes jitter to accumulate in a VCO, realignment of the VCO edge with the reference edge reduces supply-noise induced jitter as well. This can be more clearly seen by studying the supply

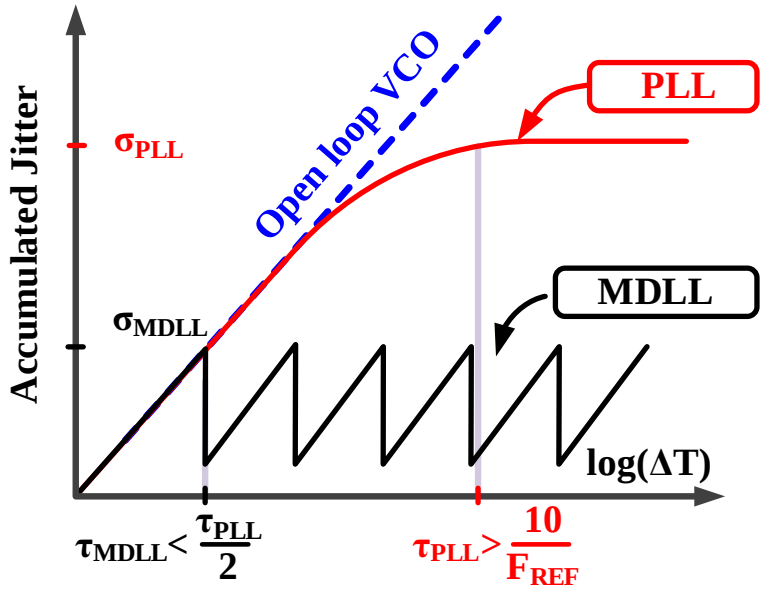


Figure 5.5: Jitter accumulation in VCOs.

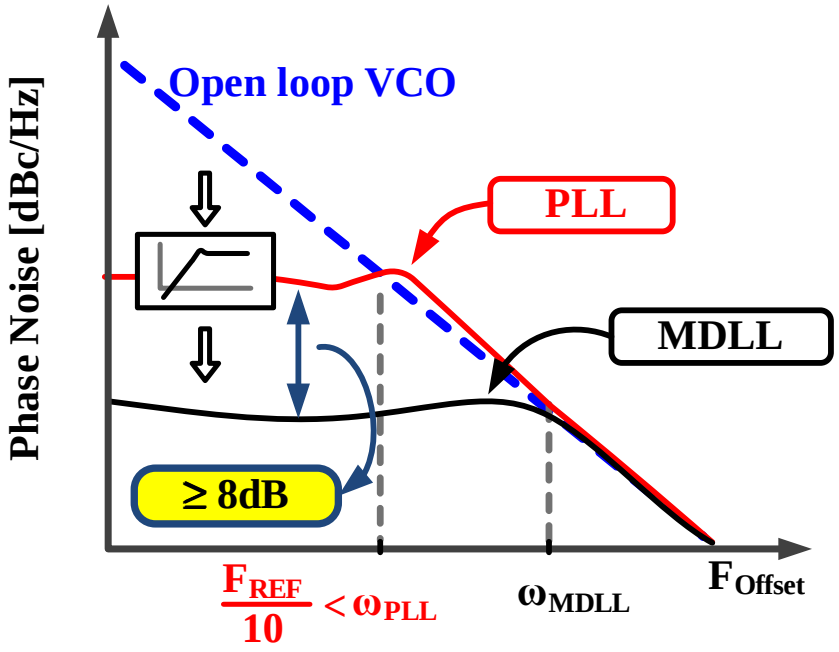


Figure 5.6: VCO phase noise suppression for PLLs and MDLLs.

noise transfer function. The magnitude response of the VCO supply to the PLL phase output transfer function is illustrated in Fig. 5.7. It exhibits a well-known band-pass transfer characteristic indicating that the PLL is most sensitive around its bandwidth. However, in the MDLL due to the jitter reset mechanism provided by the reference clock injection, the output phase noise due to supply noise is inherently suppressed by at least 8dB more, just like oscillator phase noise as discussed earlier. In spite of this phase noise improvement, the use of MDLLs has been relatively limited due to difficulties in implementing them as illustrated earlier. In our design this property is combined with a high PSRR regulator to achieve excellent supply noise immunity.

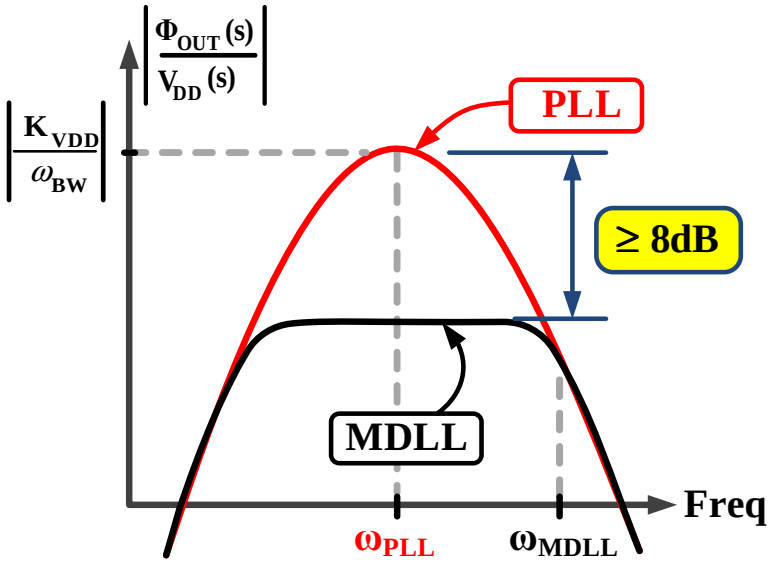


Figure 5.7: Supply noise transfer functions.

5.3 Implementation Details

In this section, the transistor-level implementation of key building blocks is discussed. All the digital building blocks are synthesized using standard cells. Because oscillator noise is suppressed by reference injection, the MDLL bandwidth can be lowered to aggressively suppress TDC quantization error without any oscillator phase noise penalty. This is illustrated by the decoupled TDC/DCO noise bandwidth tradeoff of an MDLL in Fig. 5.8. We exploit this decoupled tradeoff and use only a 1b TDC. The design details of the TDC, replica-biased regulator, digitally multiplexed ring oscillator (DXRO), frequency detector employed in FLL, and the delta-sigma DACs are discussed in the following.

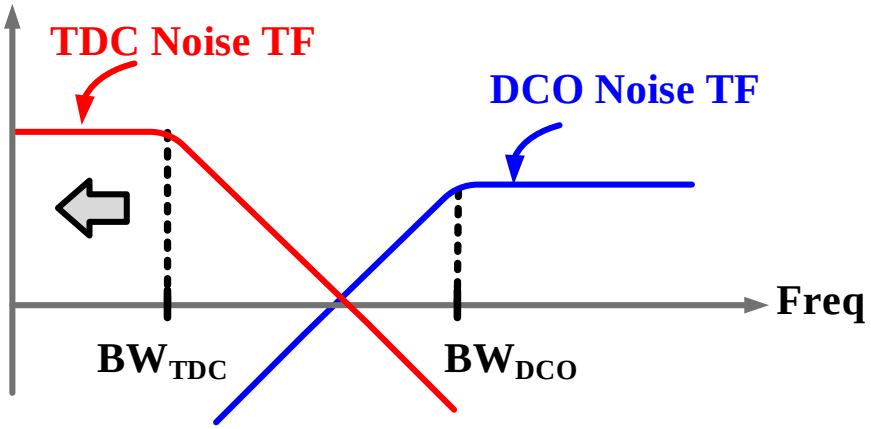


Figure 5.8: Decoupled TDC/DCO bandwidth tradeoff in an MDLL.

5.3.1 Low Power 1-bit TDC

The schematic of the 1b TDC is shown in Fig. 5.9, and the flip-flops are realized using sense-amplifier flip-flops [28]. The 1b TDC sub-samples the output clock with the input reference clock using a flip-flop. It detects the sign of the phase

error in the form of early/late decisions. The first flip-flop output is re-sampled by an identical flip-flop, FF2, to reduce hysteresis caused by output state-dependent loading. Because there are only two flip flops clocked at relatively low reference frequency, this TDC is very power efficient. However, as with the analog MDLLs, the input referred voltage offset of the FF1 appears as static phase offset and causes deterministic jitter. This causes the VCO period to be longer by ΔT whenever the reference clock is injected. This is can illustrated by the timing signals in Fig. 5.10.

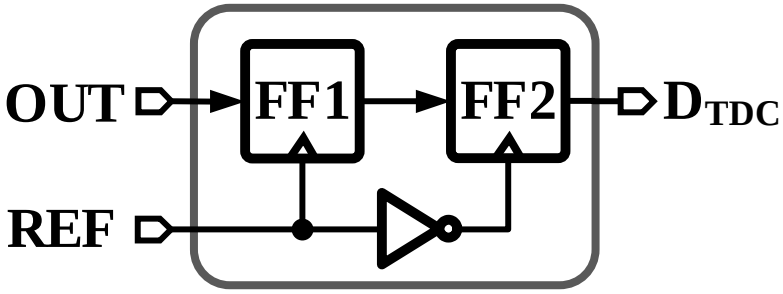


Figure 5.9: Schematic of the 1b TDC.

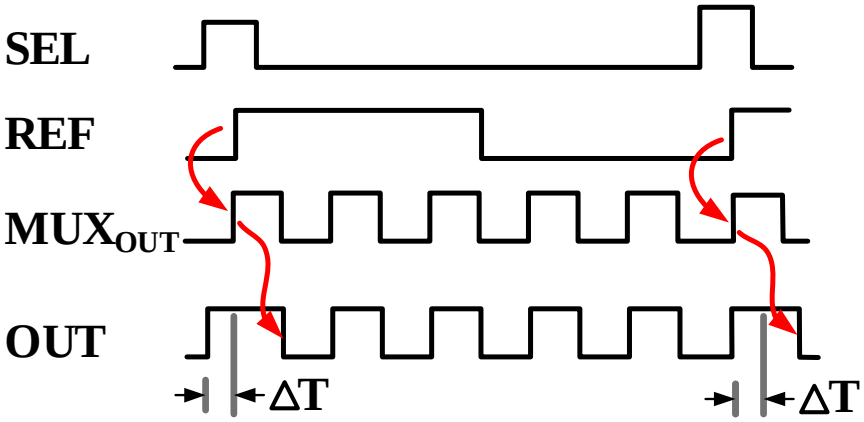


Figure 5.10: Impact of static phase offset on MDLL deterministic jitter.

In our design, the voltage offset is minimized by increasing the device dimensions, and the impact of voltage offset on phase offset is reduced by utilizing fast rise/fall times for both reference and feedback clocks. The 1 bit TDC offset was

simulated using Monte-Carlo analysis and the output histogram is shown Fig. 5.11. The standard deviation of the voltage offset is about 7.5mV With a rise/fall time of 30ps. This voltage offset translates to a 3σ phase offset of less than 0.7ps .

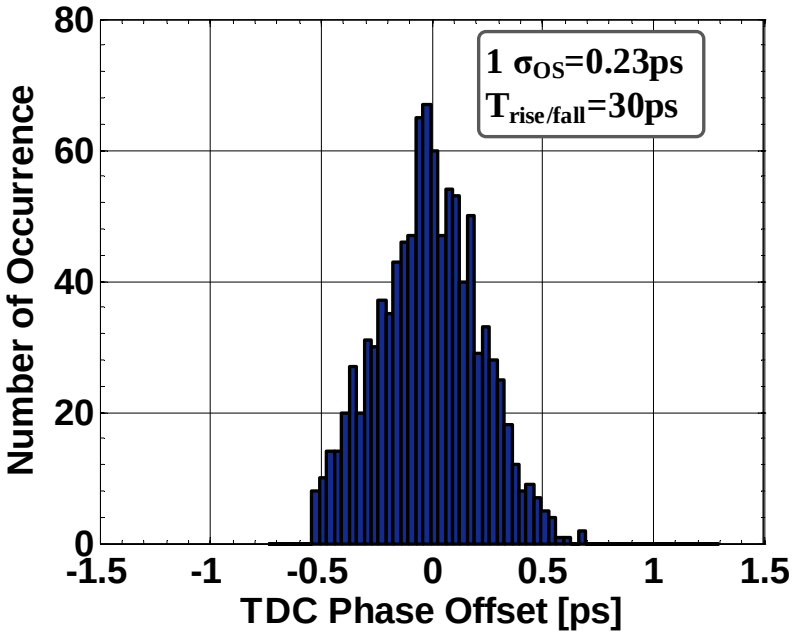


Figure 5.11: Simulated TDC phase offset using .

5.3.2 Digital Loop Filter

The block diagram of the MDLL tuning loop digital loop filter $\mathrm{DLF_{MDLL}}$ is shown in Fig. 5.12. The digital loop filter is a simple digital accumulator which is driven by the sign of the phase error. A 1-to-4 de-multiplexer is used to ease the speed requirements of the fully-synthesized 18b accumulator. The impact of TDC quantization error on output jitter is minimized by lowering the time constant of the digital accumulator. Lowering the DMDLL bandwidth does not exacerbate oscillator phase noise as in a DPLL, and the dithering jitter caused by excessive

loop delay is reduced by ignoring the accumulators lower 4 LSBs. In other words, only the 14MSBs are fed to the high resolution $\Delta\Sigma$ DAC whose details are discussed next.

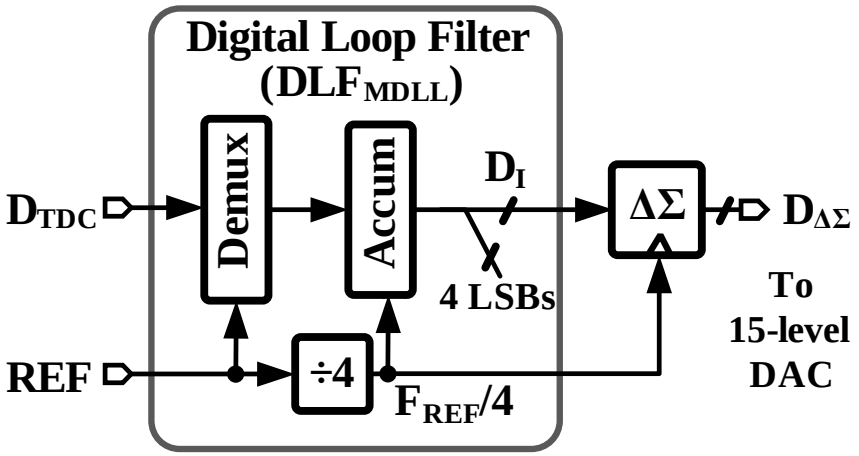


Figure 5.12: Block diagram of the digital loop filter $\mathrm{DLF_{MDLL}}$.

5.3.3 $\Delta\Sigma$ DAC

The block diagram of the digital-to-analog converter used in the MDLL tuning loop and the FLL loop is shown in Fig. 5.13. A 14-bit second order synthesized digital delta-sigma modulator (DSM) truncates the accumulator 14-bit digital word, $\mathrm{D_I}$, to 15-levels and drives a 15-element current mode DAC. A current-mode DAC, consisting of 15 nominally matched current sources, converts the digital input to an equivalent output current (see Fig. 5.13). Resistor R converts the DAC output current to voltage. A second order passive low-pass filter (LPF), with a 500kHz bandwidth, suppresses out-of-band quantization error and generates control voltage of the oscillator,($\mathrm{V_{FLL}}$ or $\mathrm{V_{TUNE}}$). The delta-sigma DAC architecture eases hardware requirements, however increased loop latency introduced by the

LPF phase shift degrades the jitter performance. In the proposed DMDLL, ignoring the lower 4 LSBs of the accumulator output and passing only the 14 most significant bits to the DAC suppresses the dithering jitter.

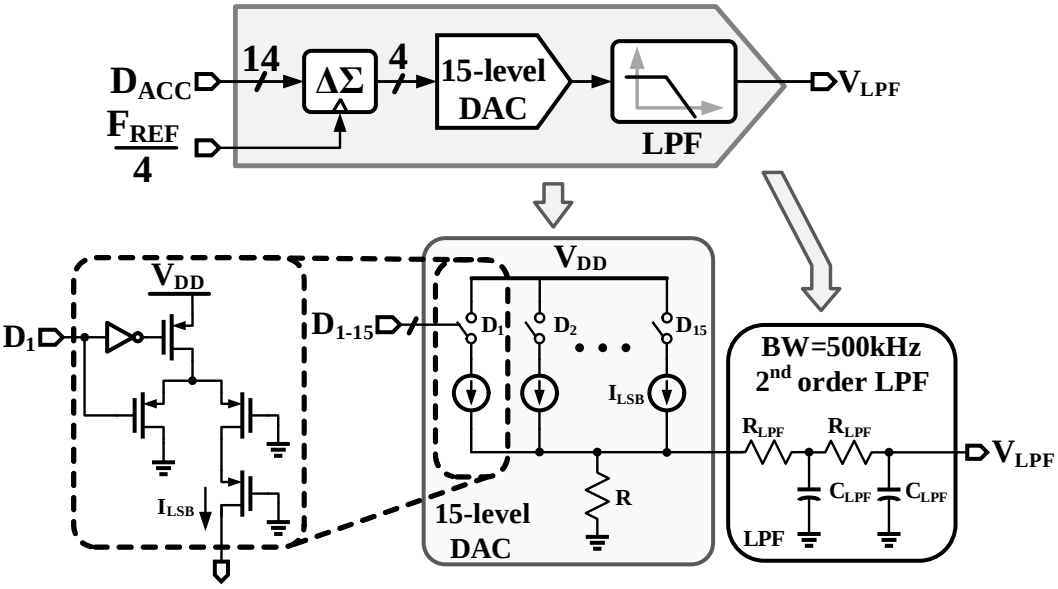


Figure 5.13: Block diagram of the delta-sigma DAC, and circuit schematic of the 15-level current mode DAC and post filter.

5.3.4 Digitally Multiplexed Ring Oscillator (DXRO)

The schematic of the replica-biased regulator, optimized for high supply-noise rejection is shown in Fig. 5.14. It buffers the FLL control voltage, and generates the virtual supply voltage of the oscillator denoted as $\mathrm{VDD_{VCO}}$. Because the regulator is placed in the low-bandwidth FLL, wide-band supply noise rejection is achieved by introducing a low-frequency pole ω_D at the VCOs supply node [17, 20]. By making ω_D to be lower than the pole at the amplifier output, ω_A, the peaking in the power supply rejection present in conventional regulators can be eliminated. By closing the feedback around the replica of the VCO, a replica-biased regulator

facilitates an area efficient means to improve PSRR by introducing a low frequency pole ω_D. The simulated PSRR curves for various values of the bypass capacitance C_D are shown in Fig. 5.15 illustrate this improvement. As expected, increasing C_D lowers ω_D and improves PSRR beyond ω_A. The replica load is implemented with stacked diode-connected devices to achieve good matching between the VCO and the replica load.

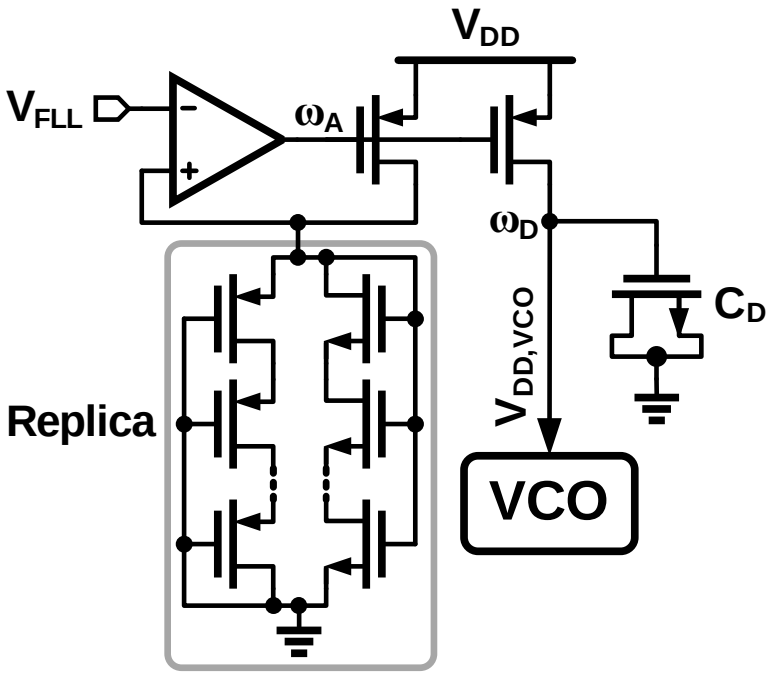


Figure 5.14: Schematic of the high PSRR replica-biased regulator.

The schematic of the multiplexed ring oscillator is shown here. It is composed of a cascade of a mux and 3 pseudo-differential delay cells that are tuned by the FLL and MDLL by varying the supply voltage and the output time constant, respectively. The delay cells are implemented using CMOS inverters coupled in a feed-forward manner to ensure differential operation. The transmission gate multiplexer is carefully designed to ensure clean reference injection.

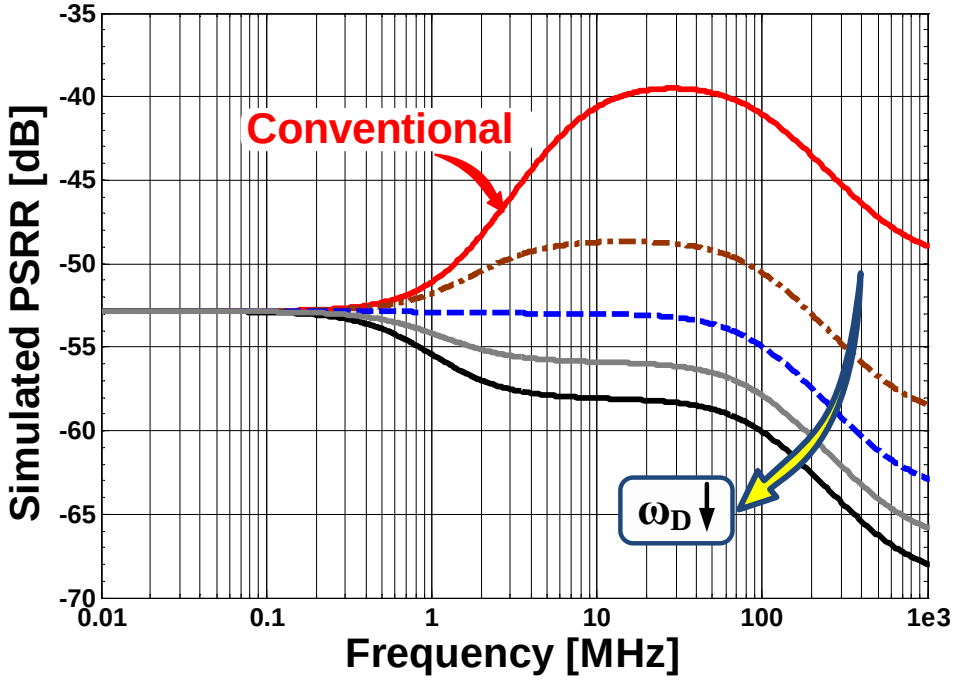


Figure 5.15: Simulated regulator PSRR for different bypass capacitor (C_D) values.

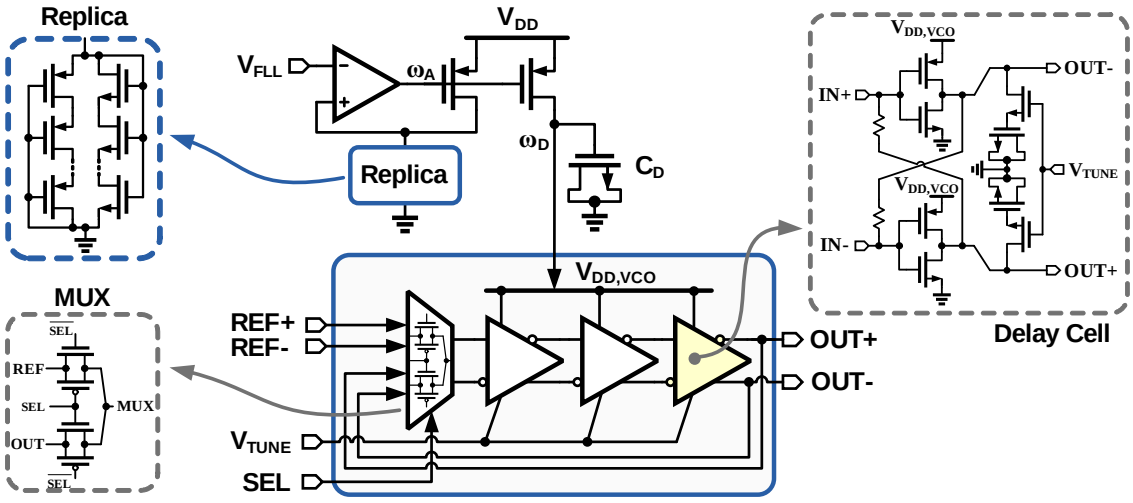


Figure 5.16: Schematic of the proposed regulated multiplexed ring oscillator.

5.3.5 Frequency Locking Loop (FLL)

To achieve a wide operating range, a fully synthesized frequency-locking loop (FLL) is used to drive the DXRO toward frequency lock (see Fig. 5.4). A counting

type frequency detector is used in this implementation, and its schematic is shown in Fig. 5.17. Frequency error is found by measuring the difference between the number of oscillator periods in adjacent reference periods. The DXRO clock is first divided by 64 before it is fed to a 14-bit counter to relax counter speed requirements. Deviation of the counter output from 128, between the two divided clocks, is the measure of frequency error. A cascade of two registers is used to perform digital differentiation $1 - z^{-1}$ and the resulting frequency error is fed to the digital loop filter. The digital loop filter is composed of a digital accumulator whose output drives the DXRO using a $\Delta\Sigma$ DAC, whose implementation details are similar to the one used for the MDLL tuning loop.

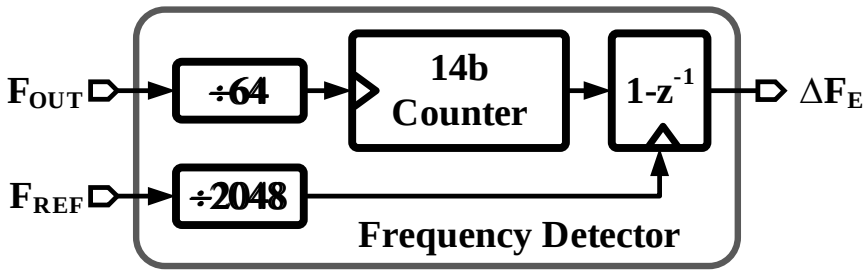


Figure 5.17: Block diagram of the frequency detector used in the FLL.

5.4 Experimental Results

the detailed block diagram of the proposed DMDLL is shown in Fig. 5.18 [3]. The DMDLL is fabricated in a 0.13μm CMOS process and occupies an active area of 0.25mm^2. Die photographs of the prototype chips is shown in Fig. 5.19, where a fully-synthesized digital logic is used to reduce design complexity and ease portability to newer processes.

The measurement setup used to characterize the prototype IC is shown in

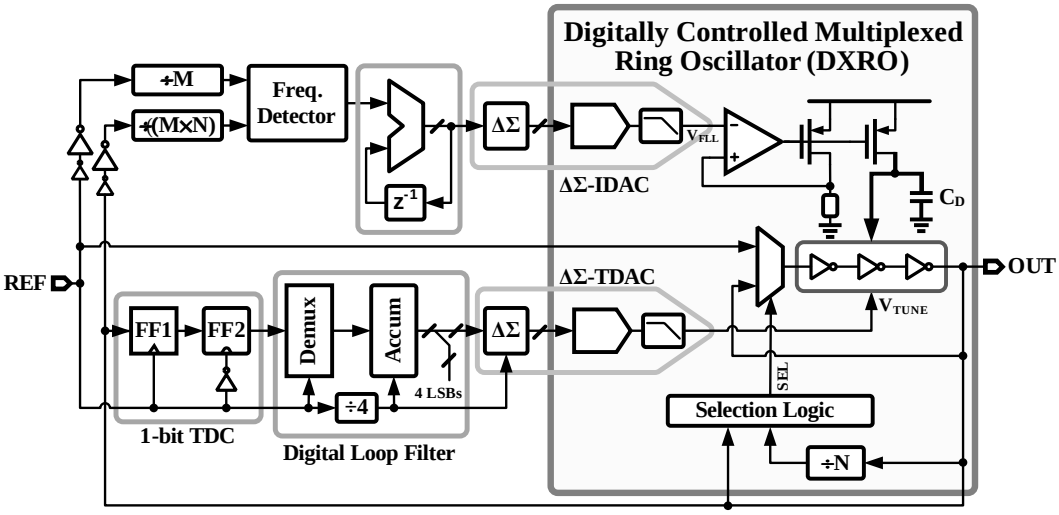


Figure 5.18: Proposed DMLL detailed block diagram.

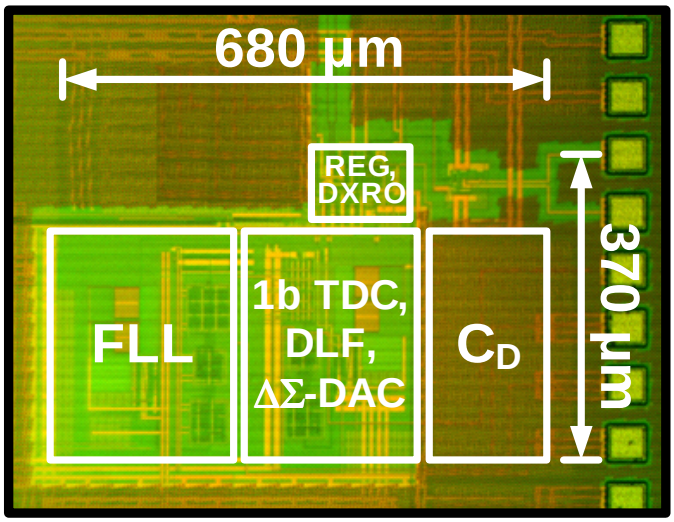


Figure 5.19: DMDLL die photograph.

Fig. 5.20. Supply noise measurements are performed by modulating the VCO supply with sinusoidal tone. An arbitrary waveform generator (Tektronix AWG7122B) is used to provide the input reference clock, while an RF signal generator (Fluke 6062A) is used to introduce sinusoidal noise tones on the VCO supply. Since the prototype chip feedback divide ratio is fixed, the desired output frequency was

obtained by varying the reference frequency. A communication signal analyzer (Tektronix CSA8200) was used for the time domain long-term absolute jitter measurements. The spectrum Analyzer (Tektronix RSA3308B) is used to measure the reference and noise spurs. To guarantee the fidelity of all supply noise measurements, an integrated supply noise monitor, implemented using a wide bandwidth voltage follower, is used to measure the amount of on-chip VCO supply noise.

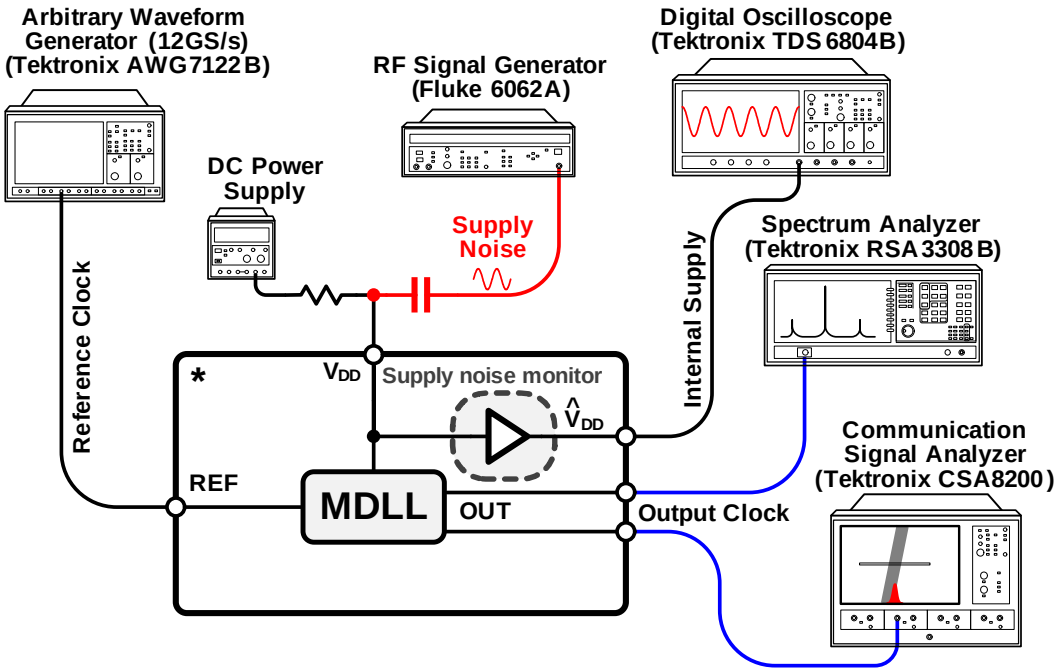


Figure 5.20: Measurement setup.

The prototype DMDLL has a power consumption of 890μW at 1.5GHz output frequency with a nominal supply voltage of 1.1V. The proposed DMDLL operates over a wide range of output frequencies of 0.8-to-1.8GHz. Fig. 5.21 shows the measured phase noise spectrum at 1.5GHz output frequency. For comparison, the proposed DMDLL is compared with the DPLL in Chapter 4. The DPLL is separately optimized for low jitter and high supply noise rejection and is implemented with identical blocks to the DMDLL. The measured phase noise at 1MHz

offset are nearly -129dBc/Hz and -112dBc/Hz for the DMDLL and DPLL designs, respectively. The rms jitter obtained by integrating the phase noise from 10kHz-to-100MHz is only 400fs for DMDLL and it is 3.2ps for DPLL, illustrating the lower jitter in the MDLL due to the reference injection mechanism. In the case of the DPLL, limit cycle induced peaking at around 40MHz increases the rms jitter. This peaking also exacerbate supply noise sensitivity as illustrated later, and as expected, no such peaking is observed for the DMDLL.

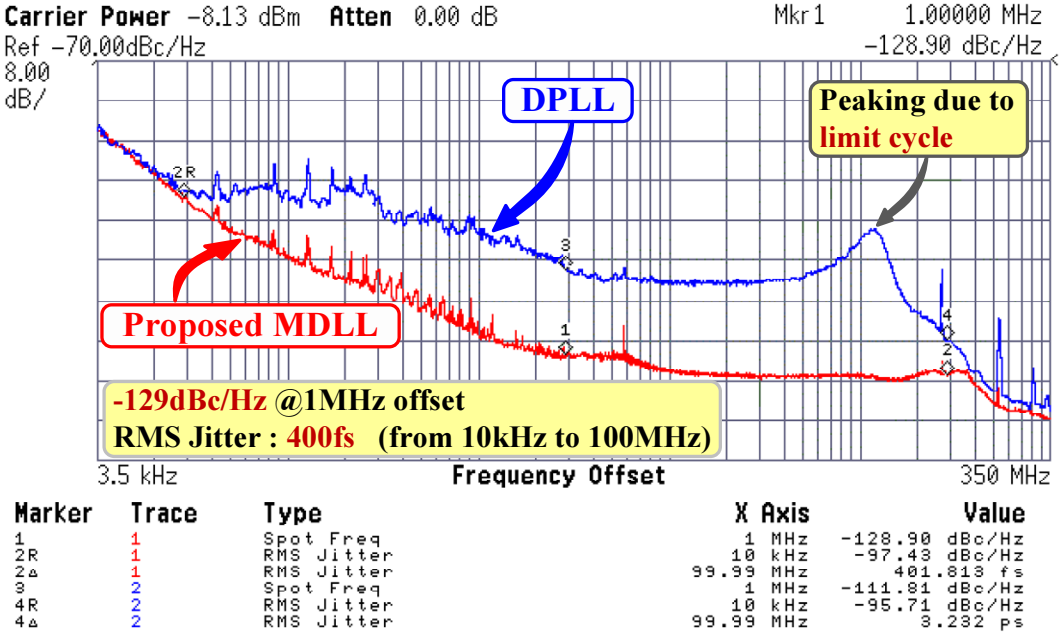


Figure 5.21: Measured phase noise at 1.5GHz output frequency.

The jitter accumulation is investigated by measuring the long-term jitter. Figure 5.22 shows the measured jitter histograms at 1.5GHz output frequency, in the case of a quite supply voltage. The long-term absolute jitter measured over 5M hits is only 920fs$_{rms}$ and 9.2ps peak-to-peak for the DMDLL, which is about 4× lower than that of the DPLL. The DPLL jitter is about 4.2ps$_{rms}$ and 30ps peak-to-peak.

To evaluate the effectiveness of the proposed supply noise rejection, a large

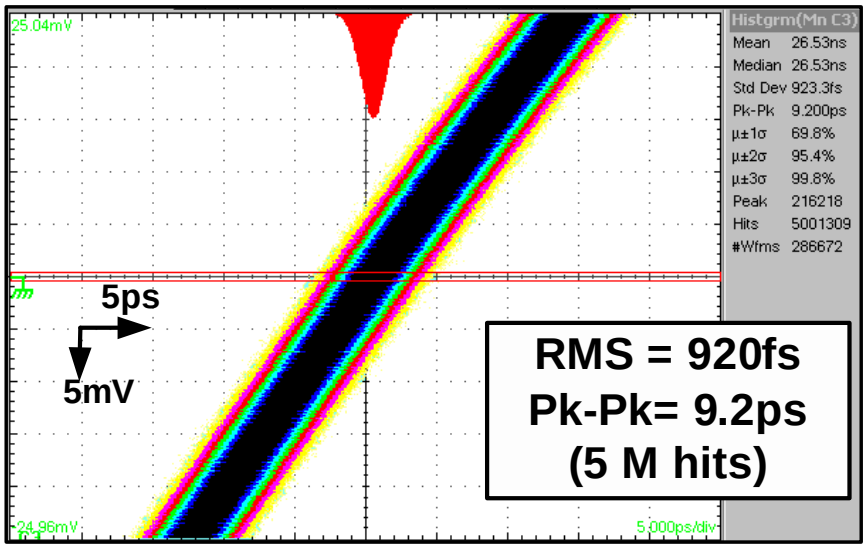


Figure 5.22: Measured long term jitter histograms (5 M hits).

200mV peak-to-peak sinusoidal tone is additionally superimposed on the supply voltage and the supply noise frequency is swept from 1MHz-to-1.4GHz. The the measured peak-to-peak jitter degradation (calculated by subtracting the jitter in the absence of the supply noise) is plotted in Fig. 5.23.

This plot quantifies the measured dynamic supply noise sensitivity by plotting peak-to-peak jitter degradation. In the worst case, long-term peak to peak jitter degraded by only 3.8ps peak-to-peak for the MDLL which is 3× lower than the DPLL. The worst case peak to peak jitter histogram for the DMDLL case is shown in Figure 5.24.

The supply noise sensitivity of the proposed DMDLL is only $18\text{fs}_{\text{pp}}/\text{mV}_{\text{pp}}$. The plot corresponding to the DPLL (Fig. 5.23) shows that the supply noise sensitivity is highest around 40MHz, which is the peaking frequency identified earlier in the phase noise plot. This peaking is attributed to the limit cycles present in the steady-state of the DPLL as illustrated earlier in.

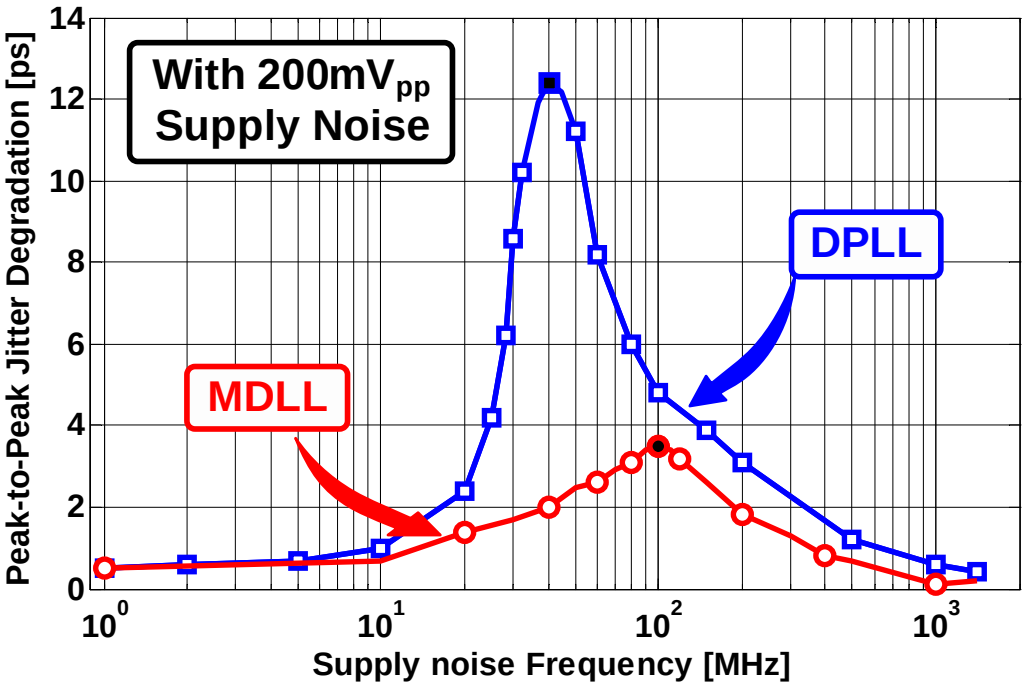


Figure 5.23: Measured peak-to-peak jitter degradation as a function of supply noise frequency at 1.5GHz output frequency.

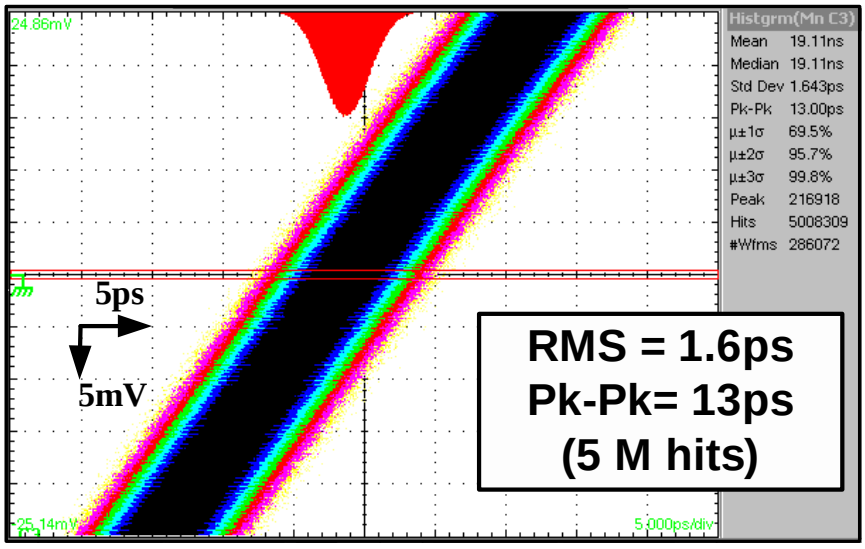


Figure 5.24: Measured worst case long term jitter histograms in the presence of 200mV_{pp} supply noise.

The measured overall jitter, provided by the measured long-term time domain jitter histograms, includes both random and deterministic jitter components. Since the focus of this work is to achieve both low deterministic and random jitter, it is of importance to be able to measure each of these components separately. The random jitter component is measured directly by integrating the phase noise spectrum (see Fig. 5.21). By looking at a frequency domain rather components

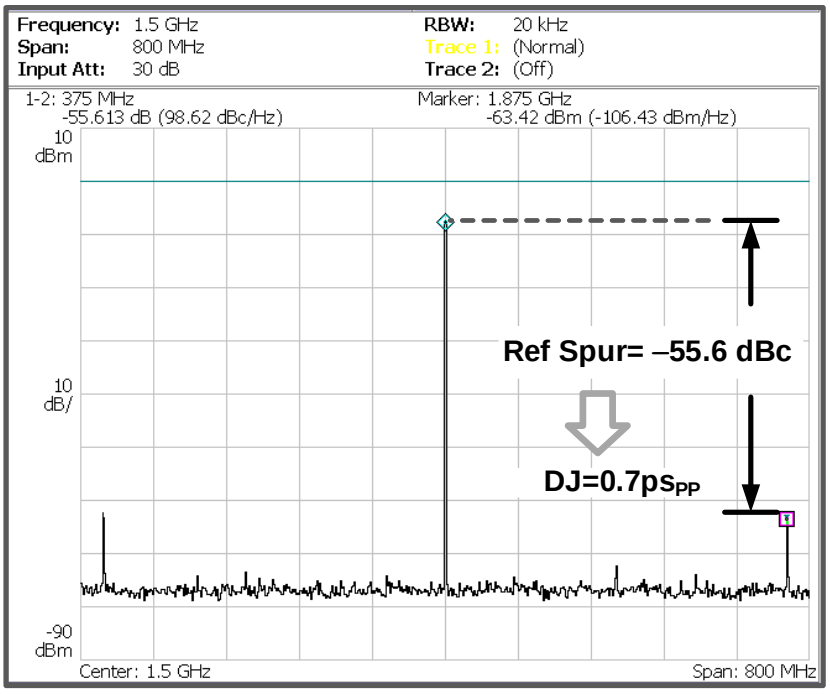


Figure 5.25: MDLL reference spurs.

than the time-domain histograms, deterministic jitter can be estimated. Because deterministic jitter occurs periodically at a reference clock rate, it will appear in the frequency domain as a spurious tones with a fundamental frequency offset corresponding to the reference frequency. Based on Fourier analysis, estimate of the deterministic jitter from reference spurs in the measured output clock spectrum can be given by

$$DJ_{OUT} = \frac{2}{\pi} T_{OUT} \times 10^{\frac{Spurs(dBc)}{20}} \tag{5.1}$$

where T_{OUT} is the output clock period, Spurs(dBc) level difference between the spurious reference tone and that of the carrier.

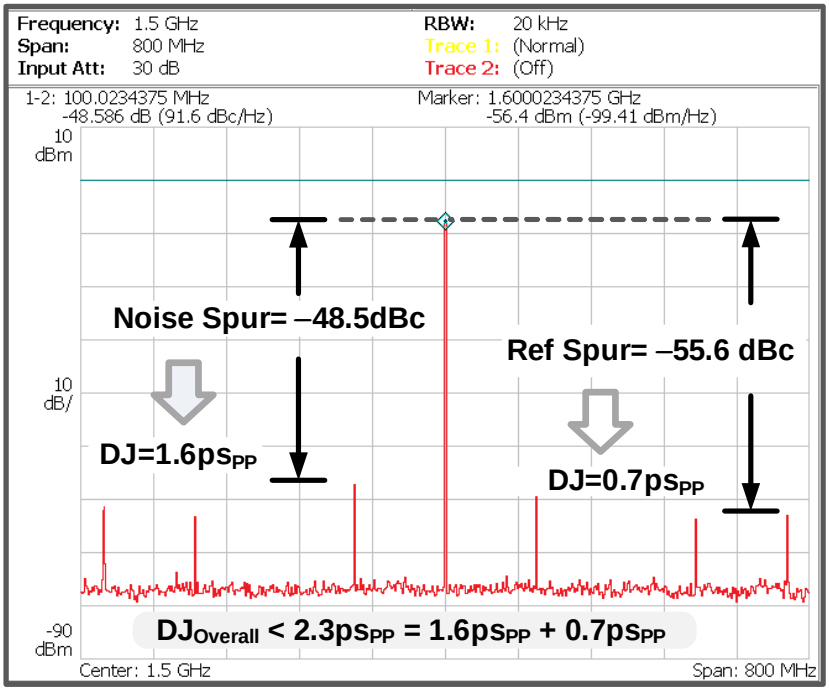


Figure 5.26: MDLL noise and reference spurs, for 200mV$_{pp}$ supply noise at the worst case supply noise frequency (100 MHz).

Figure 5.25 shows the measured output spectrum of the DMDLL in the case of quiet supply voltage. The measured reference spur is −55.6dBc which translates to only 0.7ps$_{pp}$ deterministic jitter estimated using the Eq. 5.1. When 200mV$_{pp}$ supply noise is introduced at the worst case noise frequency of 100MHz, the reference spurs are not degraded, and the spurs due to supply noise are found to be at about −48dBc level (see Fig. 5.26). The deterministic jitter degradation due to supply noise is found to be only 1.6ps peak-to-peak.

The performance of the prototype digital MDLL is summarized and com-

pared with the state-of-the-art designs in Table 5.1. Compared to state-of-the-art MDLLs and supply regulated PLLs, the proposed MDLL archives the lowest power consumption and the lowest supply noise sensitivity.

Table 5.1: MDLL Performance Comparison with State-of-the-Art Designs.

	This Work	ISSC11 [35]	JSSC11 [36]	JSSC09 [17]
Technology	0.13μm	65 nm	90nm	0.18μm
Area [mm^2]	0.25	0.025	0.76*	0.093
Supply [V]	1.1	1.2/1.0	1.2	1.8
Freq. Range [GHz]	0.8-2.0	N/A	N/A	0.5-2.5
Output Freq. [GHz]	1.5	4.6	1.5	1.5
Power [mW]	0.89	6.8	9.2*	3.9
Jitter RMS/PP [ps] w/o Supply Noise	0.9/9.2	2.0/17.8	0.93/11.1	1.9/15
Jitter RMS/PP [ps] w/ 200mV$_{pp}$ Supply Noise	1.6/13 @100MHz	N/A	N/A	4.9/25 @8.85MHz
Worst-case Supply Noise Freq.	100MHz	N/A	N/A	8.85MHz
Implementation	DMDLL	MDLL	DMDLL	PLL

* Off-chip components: added area of 0.7 mm^2, and power of 4.1 mW [36]

5.5 Summary

Digital MDLLs are an attractive alternative to PLLs for clock multiplication. A highly-digital calibration-free digital multiplying delay-locked loop that obviates the need for a high-resolution TDC has been presented.

The proposed DMDLL combines 1b-TDC with a replica regulator to achieve excellent jitter performance and supply noise immunity. This architecture also achieves sub-picoseconds of jitter and a wide tracking range making it suitable for systems high performance applications. Compared to state of the art digital PLLs, the prototype MDLL has lower jitter, better supply noise immunity, while consuming lower power consumption.

CHAPTER 6. A HIGHLY DIGITAL TIME-TO-DIGITAL CONVERTER USING SWITCHED RING OSCILLATORS

Time-to-digital converters (TDCs) are widely employed in various applications such as automatic test equipment and timing jitter measurements. Recent developments in the area of high-resolution TDCs have opened up new opportunities in the design of mostly digital phase-locked loops (PLLs) and energy efficient analog-to-digital converters (ADCs) [5, 8, 38, 39]. Digital PLLs (DPLLs) has emerged as the preferred means to synthesis on-chip clock, as shown in Fig. 6.1(a). It consists of a time-to-digital converter (TDC), digital loop filter (DLF), digitally-controlled oscillator (DCO), and feedback divider. The TDC generates a digital word proportional to the phase error between the reference clock (REF), and the feedback divider output. The DLF interfaces the TDC with the DCO to control the output frequency and phase.

Time-based ADCs such as the one shown in Fig. 6.1(b) have been recently developed to be used in low power, and portable applications. A voltage-to-time converter (V-to-T) converts the input voltage into time, and the time-to-digital converter (TDC) evaluates the equivalent digital output code. Because the V-to-T and TDC can be implemented with small power, this approach offers an area saving and power reduction if the V-to-T linearity is maintained.

Different types of TDCs have been proposed to overcome area limitations or improve resolution. The flash is the simplest to implement, however its resolution is technology-limited by the minimum gate delay and increasing the measurement

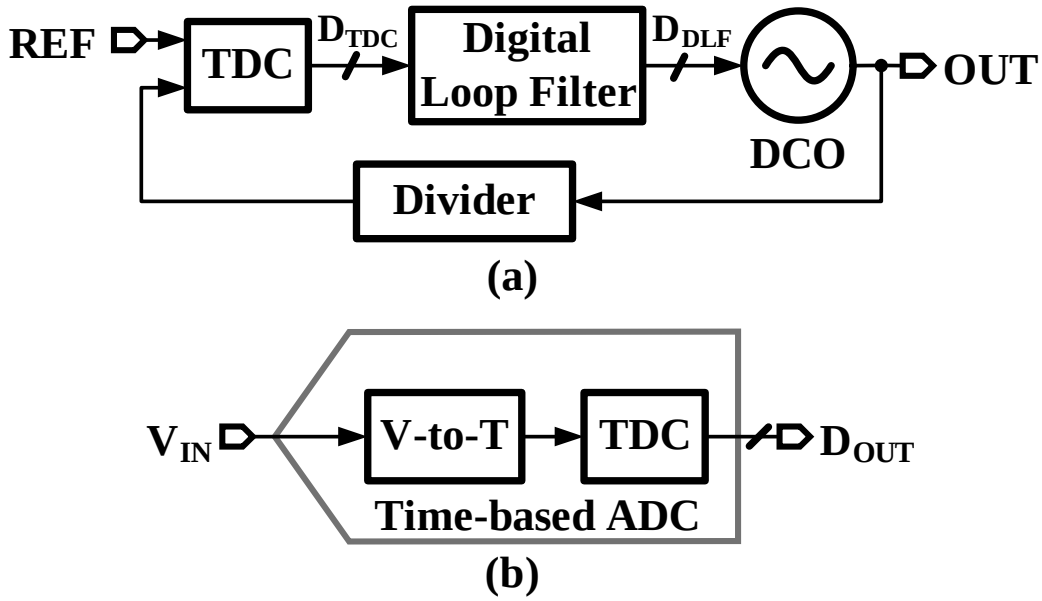


Figure 6.1: Basic block diagram of a digital PLL and an energy efficient ADC.

range requires larger chain of delay buffers thus increasing both power and area. The Vernier TDC was proposed to overcome the technology-limited resolution of a flash TDC [40, 41]. While the Vernier technique may appear to considerably improve the TDC resolution, the mismatch between the delay lines severely limits the resolution in practice. A two-step pipelined TDC was proposed to overcome the technology limitation, but it still requires calibration techniques to even achieve moderate resolution [42]. To achieve high resolution, noise-shaping TDCs with feedback topologies such as delta-sigma modulators can be used for time to digital conversion [43, 44], however it is very sensitive to analog circuit imperfections.

To overcome these drawbacks, a highly digital switched ring oscillator based TDC (SRO-TDC) that achieves noise shaping and leverage oversampling to improve TDC resolution, is presented. The OSR is also decoupled from the carrier frequency and it is therefore capable of operating at high OSRs. In this chapter,

we propose time-to-digital conversion techniques using switched ring oscillators (SRO) [4]. The SRO-TDC implemented using simple CMOS logic gates achieves high resolution by noise shaping the quantization error.

This chapter is organized as follows. In Section 6.1 a brief study of prior-art TDC designs is viewed. Section 6.2 illustrates the proposed switched ring oscillator(SRO) structure and its operational details, and the SRO usage in a TDC. The SRO-TDC is compared to the GRO-TDC in Section 6.3. Implementation details of critical building blocks of the SRO-TDC are illustrated in Section 6.4. Section 6.5 shows the experimental results obtained from the prototype IC. Finally, key contributions of this work is summarized in Section 6.6.

6.1 Evolution of TDC Architectures

The evolution of TDCs has followed that of the ADCs from several decades ago. For example, one of the earliest TDCs is implemented using a flash architecture in which digital output is generated by quantizing the time input in units of delay, T_{delay}, as illustrated in Fig. 6.2(a). Although a flash TDC is the simplest, its resolution is technology-limited by the minimum gate delay which is about 30ps in a 90nm CMOS process. Furthermore, increasing the measurement range requires larger chain of delay buffers thus increasing both power and area. For instance, an N-bit flash TDC will require 2^N delay elements.

A Vernier TDC, shown in Fig. 6.2(b), overcomes the technology-limited resolution of a flash TDC [40,41]. By delaying both the input and the reference edges using slightly mismatched delay elements, a Vernier TDC achieves a resolution equal to the difference between two delays of the delay chains ($T_{Delay1} - T_{Delay2}$). While the Vernier technique may appear to considerably improve the TDC resolu-

tion, the mismatch between the delay lines severely limits the resolution in practice. Also a wide measurement range requires a lot more delay cells compared to a flash TDC making it impractical in high resolution wide range applications. Therefore, unless a small range is allowed, Vernier TDC must be combined with other circuit techniques to improve resolution without significantly increasing power and area.

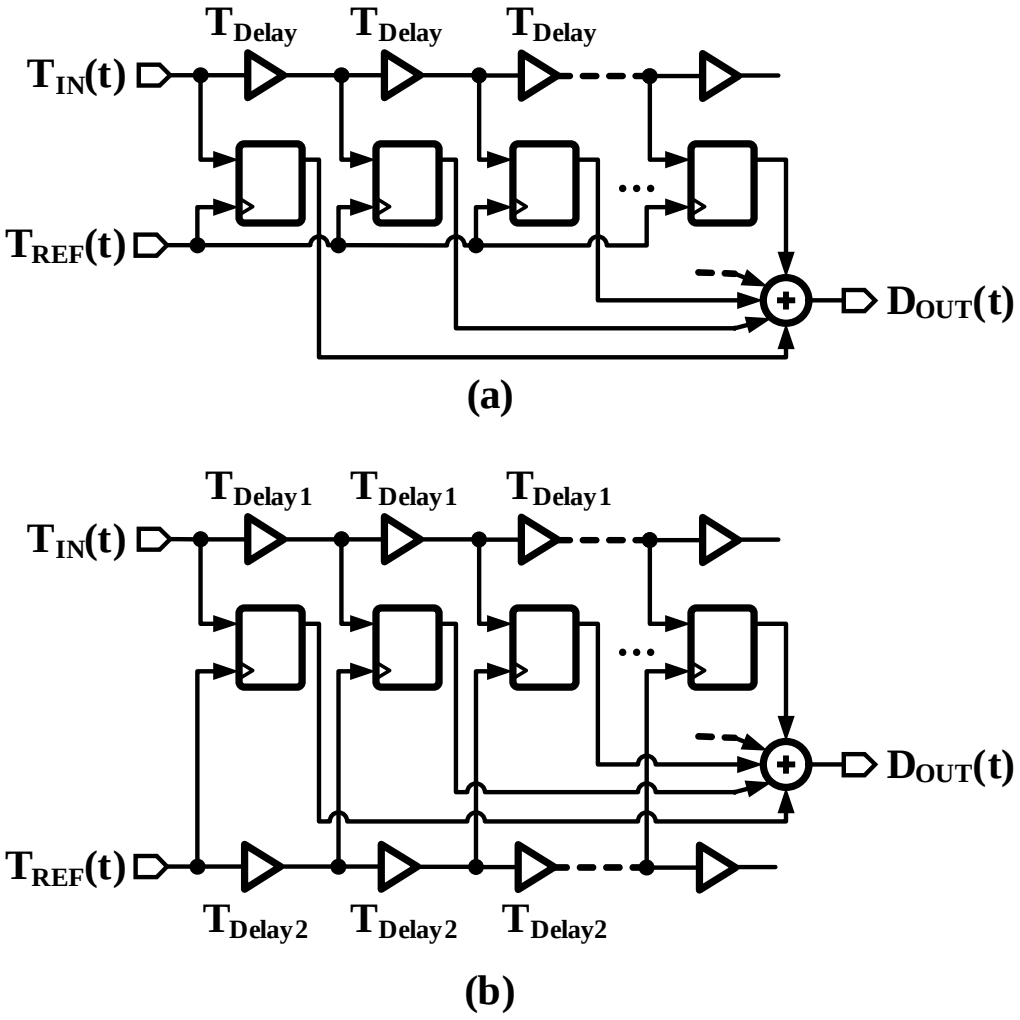


Figure 6.2: Time-to-digital converters: (a) Flash TDC and (b) Vernier TDC.

A two-step pipelined TDC was proposed to overcome the technology limitation without greatly increasing the number of delay cells [42]. As shown in Fig. 6.3,

the pipeline TDC employs a coarse stage followed by a fine stage. The coarse flash TDC acts as the first stage and generates an output code, D_{OUT1}. An inter-stage time difference amplifier generates residual quantization error which is then quantized by the second flash TDC to produce the fine output code, D_{OUT2}. The sum of properly scaled D_{OUT1} and D_{OUT2} yields the final TDC output. This approach reduces both the number of unit delay elements and their resolution requirements. However, unlike a voltage amplifier, the characteristics of the inter-stage time-residue amplifier are inherently nonlinear and are sensitive to PVT variations. Therefore, extensive calibration techniques are required to even achieve 8-to-9bit resolution [42].

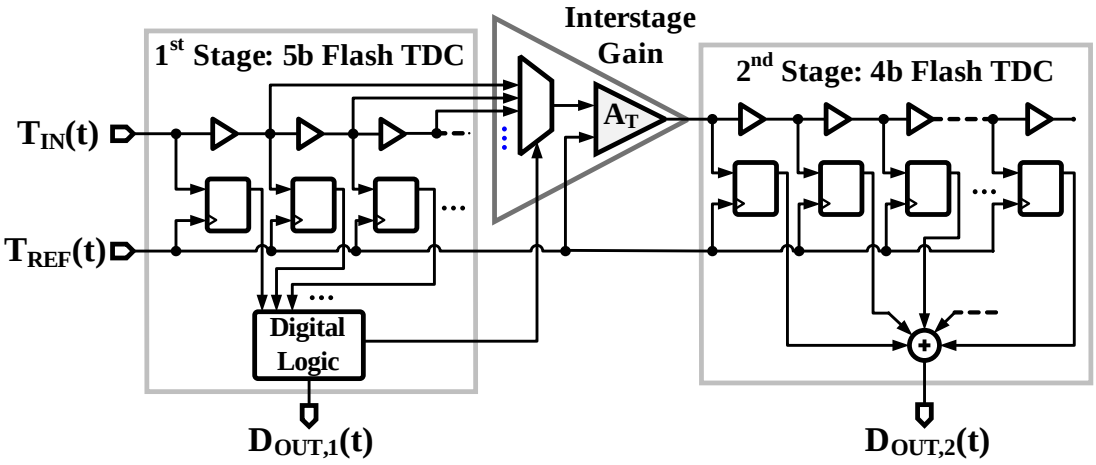


Figure 6.3: Two-step pipeline TDC with coarse and fine flash-based TDC stages.

As opposed to the feed-forward architectures discussed thus far, feedback topologies such as delta-sigma modulators can also be used for time to digital conversion. A conventional first order CT $\Delta\Sigma$ modulator can convert the time input into a noise-shaped digital output [43, 44]. However, amplifiers needed to implement active integrators are power hungry and the need for feedback DACs increases hardware complexity [43].

oversampled noise shaping TDC using 1-1-1 MASH $\Delta\Sigma$ architecture that doesn't require amplifiers is displayed in Fig. 6.4 [44]. It is composed of a cascade of three stages, each stage is implemented as a first order time-based $\Delta\Sigma$ modulator. The MASH structure performs high-order noise shaping by feeding the quantization error of the preceding stage to the next. This allows cancellation of quantization noise of the first and second stages, and the last stage quantization error is third order noise shaped. While the MASH TDC can improve the resolution, the process of extracting the quantization error in the time domain poses many challenges and is very sensitive to analog circuit imperfections [44].

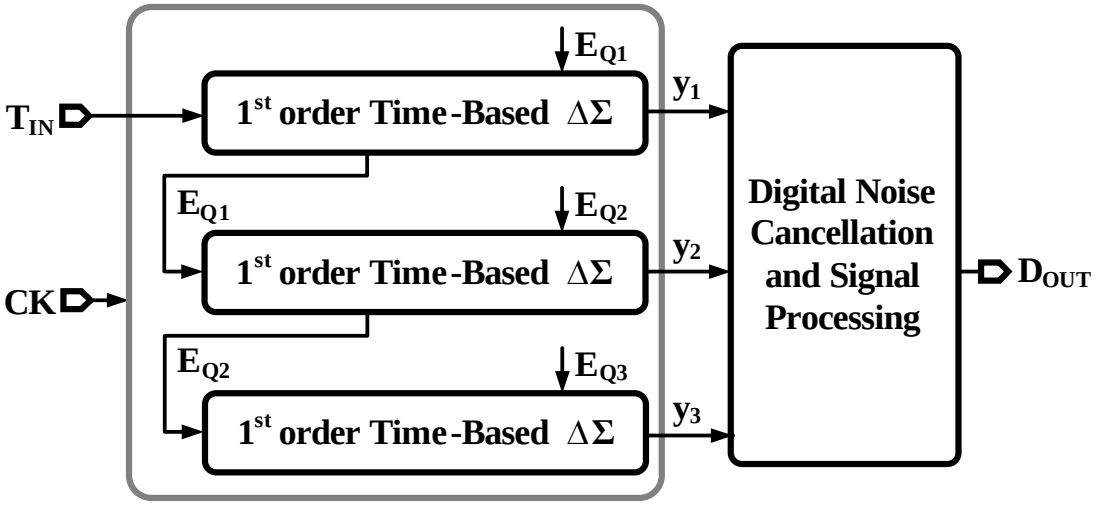


Figure 6.4: Block diagram of the 1-1-1 MASH TDC.

In addition to the limitations pointed out so far, all the TDCs require the sampling clock frequency, F_S, to be equal to the input carrier frequency, F_C. For instance, in the flash TDC (Fig. 6.2), because the phase error can be measured only once during each input clock period, oversampling does not provide any benefit. In other words sampling frequency F_S must be equal to carrier frequency F_C and the oversampling ratio (OSR) is equal to $F_C/(2\times\text{Bandwidth})$. If one can decouple F_C from F_S, then oversampling can be leveraged to improve TDC resolution. To

overcome these drawbacks, we present a highly digital switched ring oscillator based TDC (SRO-TDC) that achieves noise shaping in an open loop manner. The OSR is also decoupled from the carrier frequency and it is therefore capable of operating at high OSRs.

6.2 Proposed SRO TDC

The genesis of the proposed SRO-TDC can be best understood by first looking at the operation of a conventional first order CT $\Delta\Sigma$ modulator shown in Fig. 6.5. It consists of an integrator, quantizer and a feedback DAC. When it is fed with a pulse width-modulated input signal whose duty cycle is D_{IN}, the modulator converts the input duty cycle into noise-shaped digital output, D_{OUT}. In other words, the average value of the output digital bit stream (D_{OUT}) equals input duty cycle (D_{IN}) and quantization error (E_Q) is $1^{st}-$order noise-shaped.

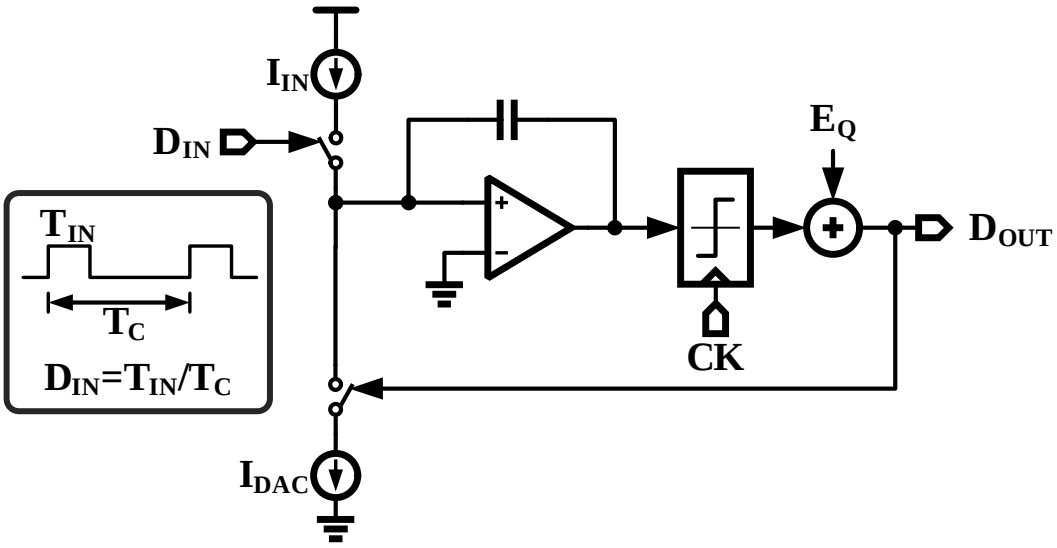


Figure 6.5: Conventional first order CT $\Delta\Sigma$ modulator.

Conceptually, assuming that the integrator never saturates, noise shaping

can be achieved in an open-loop manner by using an integrator and a digital differentiator block as illustrated in Fig. 6.6. Because E_Q is added before the digital differentiator, it is $1^{st}-$order noise-shaped. While this is impractical in the voltage domain, implementing it in the phase domain leads to the proposed switched ring oscillator TDC depicted in Fig. 6.7.

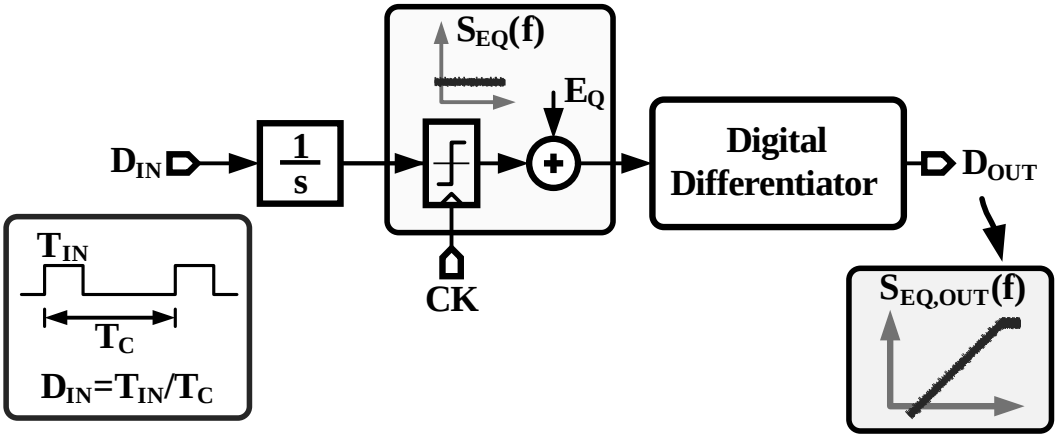


Figure 6.6: Open-loop implementation of a first order CT $\Delta\Sigma$ modulator.

Considering phase as the output variable, the VCO integrates the input voltage and generates an output phase. Since output phase exhibits modulo-2π instead of hard saturation, using VCOs as open loop integrators is feasible. The VCO output is quantized using a phase quantizer and its output is differentiated to produce the output of the modulator. Mathematically, the digital output, D_{OUT}, is given by

$$D_{OUT} = D_{IN}T_S + (1 - z^{-1})E_Q \tag{6.1}$$

where T_S is the time period of the sampling clock. Substituting the input duty cycle D_{IN} with $\frac{T_{IN}}{T_C}$ leads to

$$D_{OUT} = T_{IN}\left(\frac{T_S}{T_C}\right) + (1 - z^{-1})E_Q \tag{6.2}$$

where T_C is the time period of the input carrier clock ($1/F_C$). This reveals an interesting property of the proposed TDC: doubling the sampling frequency (F_S) doubles OSR and reduces in-band quantization noise power by 9dB. However, it also reduces the output signal power by 6dB resulting in a net signal-to-quantization noise ratio (SQNR) improvement of 3dB. This benefit is unique to the proposed TDC [4]. Because D_{IN} switches the oscillator between two frequencies we refer to the oscillator as switched ring oscillator (SRO).

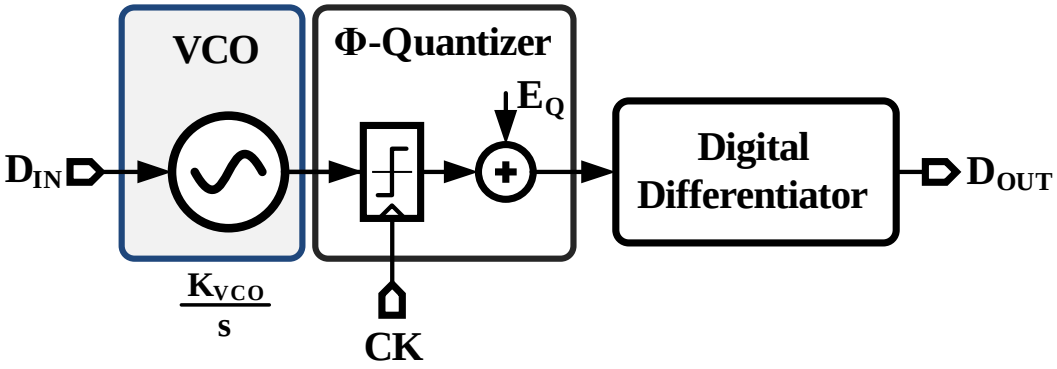


Figure 6.7: Feedforward TDC implementation using VCO as an integrator.

The block diagram of the proposed SRO-TDC is illustrated in Fig. 6.8. A time-difference generator (TDG) detects the time difference between the input signal (T_{IN}) and reference signal (T_{REF}). The generated time difference pulse (V_{TD}) is fed to a switched ring oscillator (SRO). The SRO switches between two reference voltages, V_H and V_L, based on the TDG output. As a result, the oscillator switches between only two frequencies denoted as F_H and F_L, corresponding to the high and the low values of the control voltage, respectively. Because F_H is higher than F_L, the SRO phase accumulates at a faster rate during F_H and at a slower rate during F_L. In both cases, the output phase rolls over to zero when it reaches to 2π, rendering SRO to behave as a modulo 2π integrator. The SRO output phase is then quantized to produce Φ_{SRO}, and fed to a ROM encoder. The ROM encoder

derives the digital differentiator to generate the final TDC output, D_{OUT}. Because of the highly digital nature of its building blocks, the SRO-TDC is immune to analog circuit imperfections.

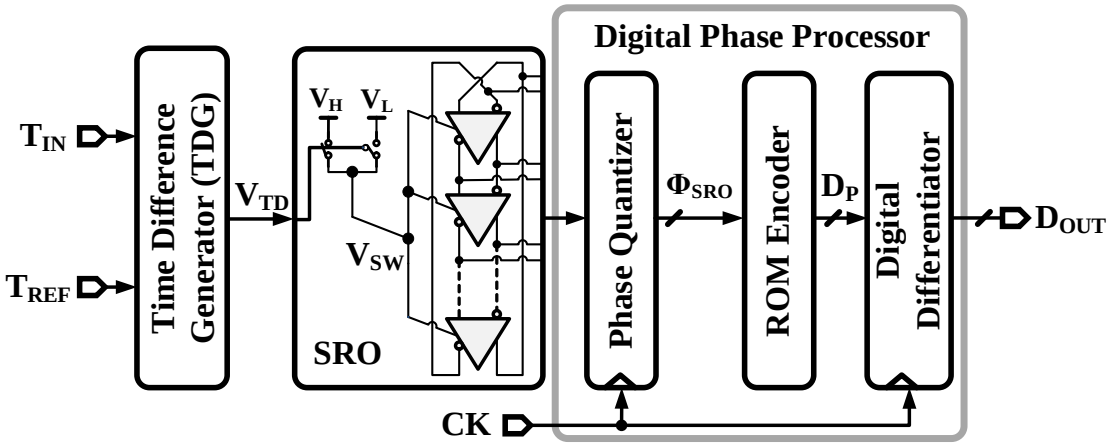


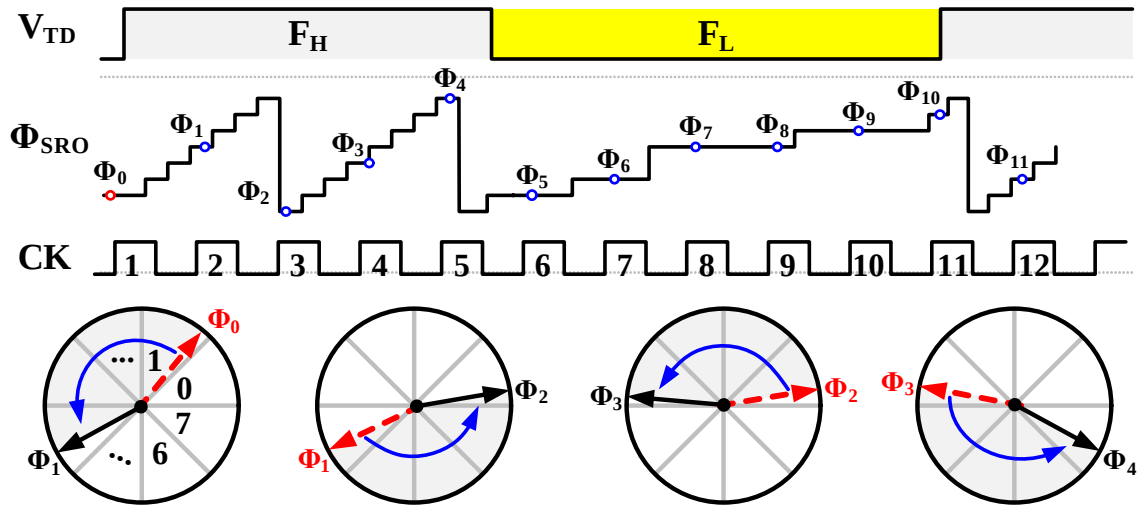
Figure 6.8: Simplified block diagram of the proposed SRO-TDC.

To understand more the operation details of the proposed architecture, it's instructive to take a closer look at the phase processing of the SRO-TDC. The operation principle of the SRO-TDC is elucidated using the phase diagrams depicted in Fig. 6.9. When the SRO oscillates at its highest frequency F_H, the phase accumulates at a faster rate, and while operating at F_L, it accumulates at a much slower rate.

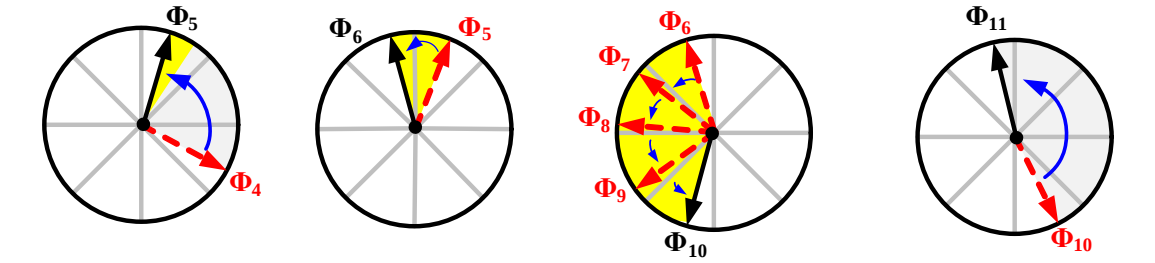
For simplicity, a 4-stage differential oscillator is used and the carrier frequency is assumed to be 10 times lower than the sampling frequency. For the first five sampling clock cycles, the oscillator phase accumulates approximately π radians per clock cycle equaling the time delay of 4 oscillator stages. The sampled phase is quantized by mapping it to the corresponding phase segment number ranging from 0-to-7.

The TDC output is calculated by sample-by-sample differentiation of the quantized phase. The phase wrapping around 2π is accounted for by a simple

modulo-8 operation performed in the digital differentiator. For sampling clock cycles 5-to-10, the phase accumulates at a very low pace resulting in only infrequent changes in the quantized phase value (see Fig. 6.9). To prevent phase roll-over due to accumulation of more than 2π in one clock period, the sampling clock frequency, F_S, must be higher than F_H.



Cycle	1	2	3	4
Φ_{OUT}	$\Phi_1 = 4$	$\Phi_2 = 0$	$\Phi_3 = 3$	$\Phi_4 = 7$
D_{OUT}	$D_{OUT,1} = 3$	$D_{OUT,2} = 4$	$D_{OUT,3} = 3$	$D_{OUT,4} = 4$



Cycle	5	6	7, 8, 9, and 10	11
Φ_{OUT}	$\Phi_5 = 1$	$\Phi_6 = 2$	$\Phi_{7,8,9,10} = 3,4,4$, and 5	$\Phi_{11} = 2$
D_{OUT}	$D_{OUT,5} = 2$	$D_{OUT,6} = 1$	$D_{OUT,7,8,9,10} = 0,1,0$, and 1	$D_{OUT,11} = 4$

Figure 6.9: Phase quantization and the frequency readout process of the SRO-TDC.

6.3 SRO-TDC versus GRO-TDC

To maximize dynamic range of the TDC, F_L must be much smaller than F_H. When F_L is set to zero, the oscillator is fully stopped (gated) and the SRO-TDC simplifies to the recently proposed gated ring oscillator based TDC (GRO-TDC) [45]. In a GRO, the ring oscillator operates in two states. In one state, the GRO oscillates at F_H much like an SRO. However, when F_L=0, the GRO is stopped and the phase of the oscillator must be preserved. This requirement to hold the oscillator phase makes the GRO-TDC susceptible to analog circuit imperfections (see Fig. 6.10).

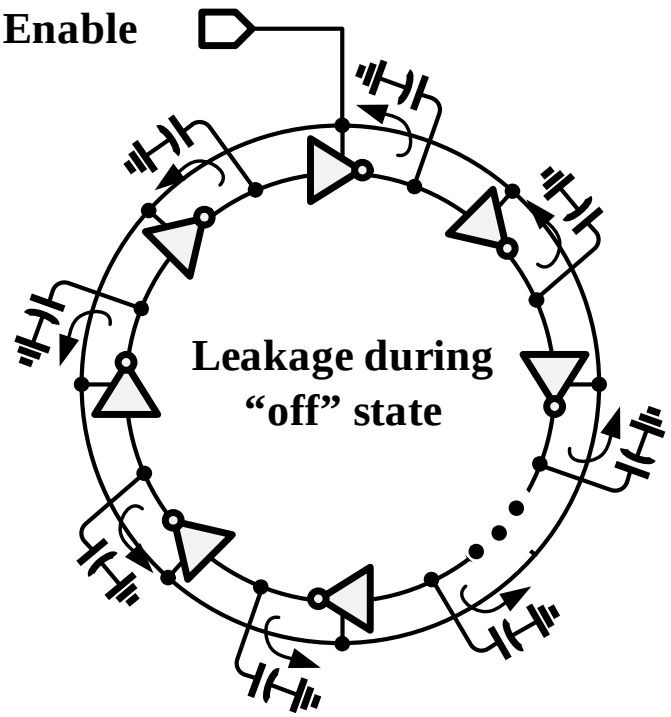


Figure 6.10: GRO-TDC illustrating leakage during the off-state.

Consider the waveforms in Fig. 6.11, during the off state, leakage and charge redistribution will cause the output phase to change resulting in a phase error,

$\Delta\Phi$ [46]. We refer to this as skew error. This skew error can be measured using the time quantity T_{Skew} as illustrated by the phase trajectories in Fig. 6.12. The phase trajectory of a GRO is illustrated for ideal and actual phase trajectories of the oscillator when disabled at the time $t_{disable}$. T_{Skew} can be measured as the difference between these two phase trajectories. Two sources of error cause T_{Skew}, first since it is not physically possible to gate an oscillator off and on instantaneously, therefore we can expect a small amount of delay time, that happens in both cases, when the GRO is disabled and again when oscillation resumes. The second source of error comes from the off state leakage and charge redistribution.

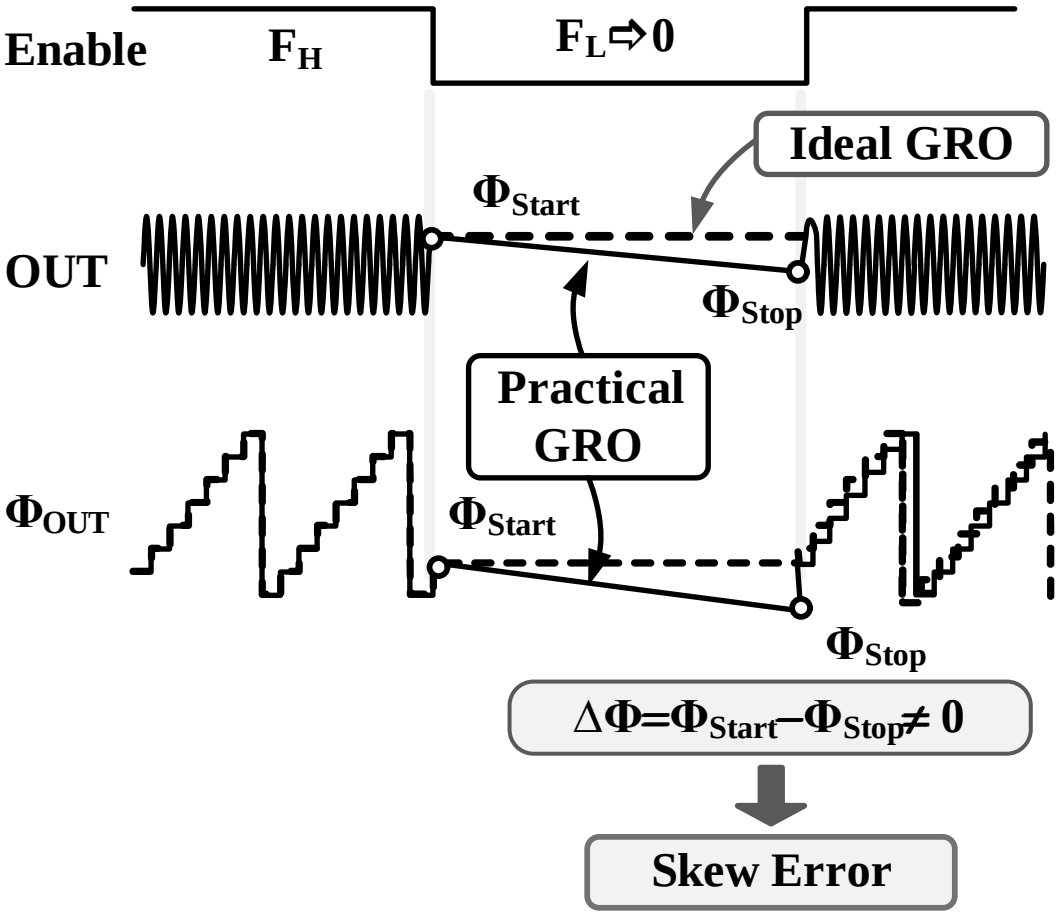


Figure 6.11: Skew error in GRO-TDC.

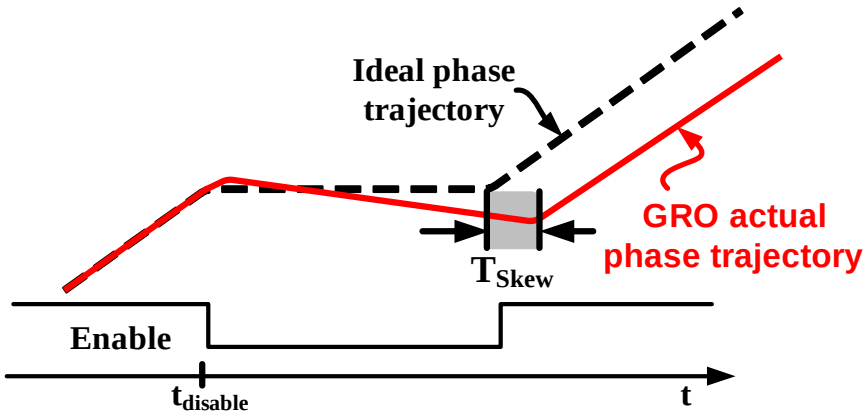


Figure 6.12: Phase trajectory skew error due to the non-idealities of oscillator gating.

Because SRO is not stopped, it has minimal skew error. To quantify these errors, both SRO and GRO circuits were simulated. The normalized skew error for both SRO and GRO is plotted in Fig. 6.13.

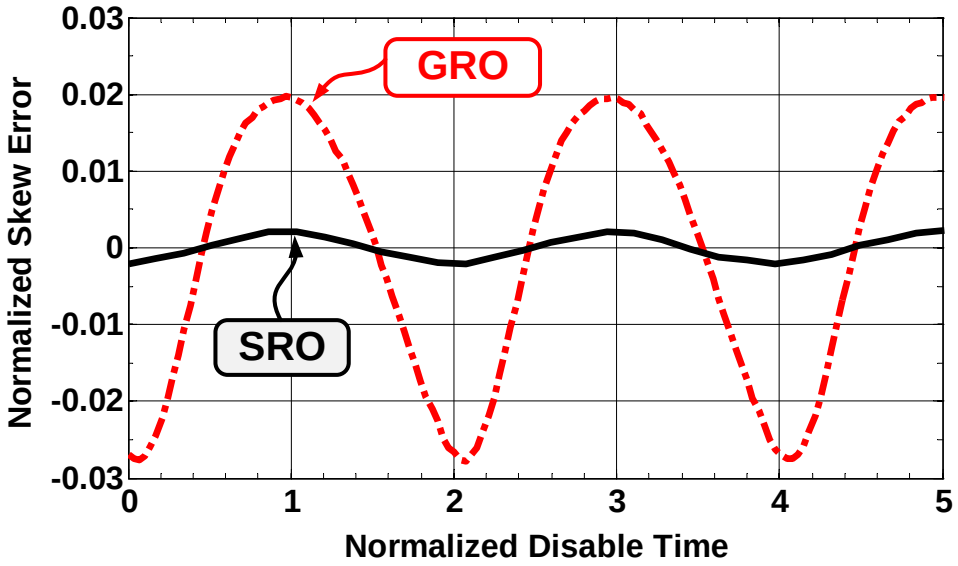


Figure 6.13: Simulated skew error for SRO and GRO.

This shows that skew error in a GRO is much larger than that of the SRO. Detailed simulations also indicate that skew error increases with lowering F_L and

the worst case skew error is observed when the oscillator is fully gated, i.e. F_L=0). An important effect of skew errors is it can cause dead-zone in the TDC's transfer characteristics.

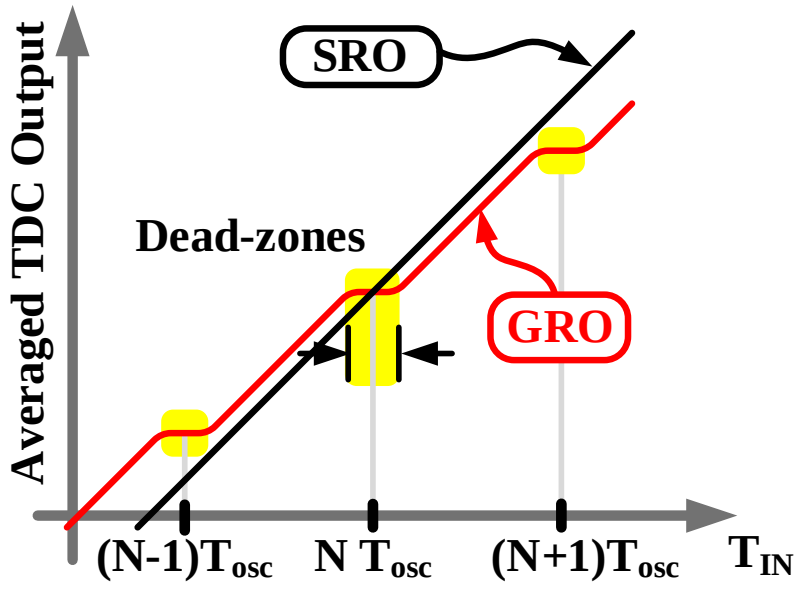


Figure 6.14: Deadzone behavior in SRO and GRO TDCs.

The dead zone behavior in SRO and GRO TDCs is illustrated in Fig. 6.14. Simply, when T_{IN} is in the vicinity of an integer multiple of the oscillation period, the skew error causes the final oscillator state to be equal to the initial state during both F_H and F_L durations. In other words, as can be seen in Fig. 6.15. $\Phi_1 = \Phi_2 = \Phi_3$, even if the input time difference is not exactly equal to an integer multiple of oscillation period.

This effect manifests as dead-zone in the TDC transfer characteristics. Note that, dead-zones occur only if F_H and F_L are synchronous with each other. Because in GRO, the low frequency F_L=0 will always be synchronous with F_H, GRO TDC will always suffer from dead-zone. By making F_H and F_L asynchronous with each other, SRO-TDC can be completely immune to dead-zone.

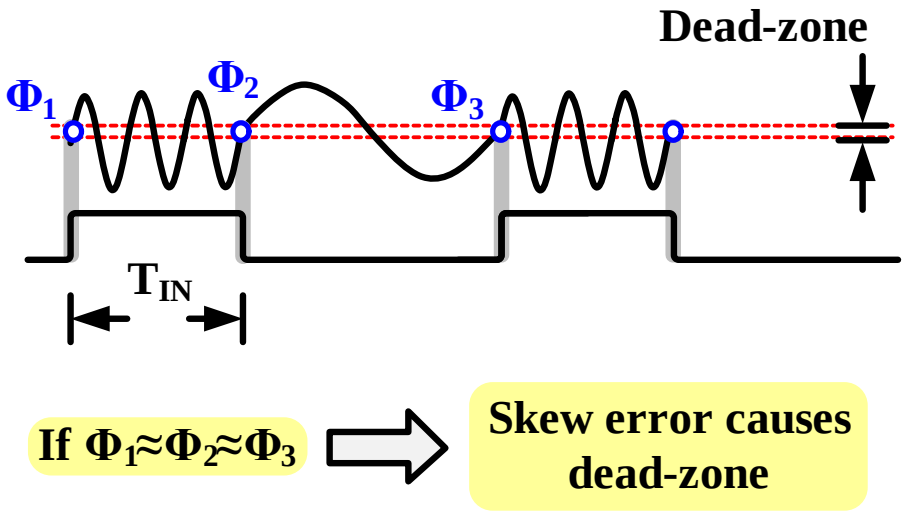


Figure 6.15: Illustration of the oscillator phase around deadzone.

Having discussed the basic operation of the SRO, and it's special cases, details of the proposed SRO-TDC, and its key building blocks will be discussed next.

6.4 Prototype SRO-TDC Implementation

The prototype SRO-TDC is depicted in Fig. 6.16. A pseudo-differential architecture is used to reduce the quantization error by 3dB compared to a single-ended TDC. Each half-circuit consists of an SRO that switches between two frequencies, F_H and F_L, based on the TDG output. The differentiated positive half circuit output is subtracted from the other complimentary half-circuit output ($D_{OUT,N}$) to generate the final TDC output, D_{OUT}. I will now present the circuit implementation details of each of the building blocks.

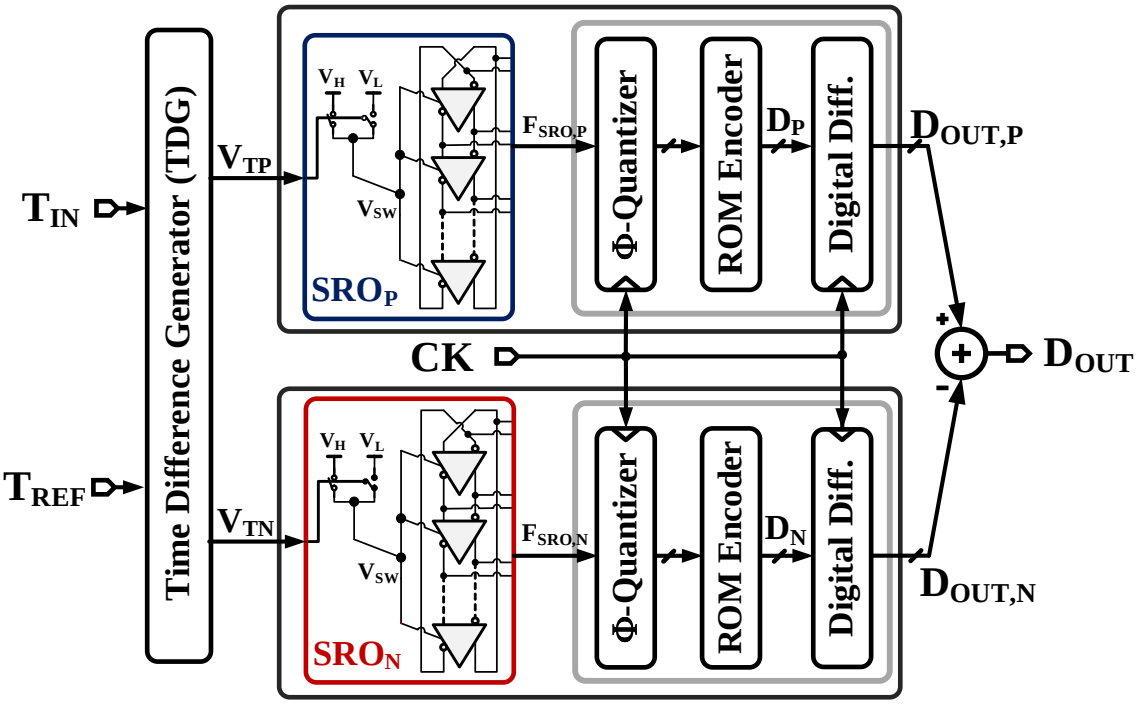


Figure 6.16: Complete block diagram of the proposed SRO-TDC.

6.4.1 Time Difference Generator (TDG)

The schematic of the time difference generator is shown in Fig. 6.17. It is implemented using a classical NAND gate based 3-state phase frequency detector [47] and an XOR gate. The TDG circuitry detects the time difference between the positive edges of its two inputs and generates an output digital pulse whose width is equal to the input time difference. The XOR gate is implemented using a fully symmetric static CMOS logic (see Fig. 6.17). Simulations indicate that static logic, compared to dynamic logic greatly minimizes nonlinearity caused by the dynamic charging/discharging transients of the internal nodes.

The simulated integral non-linearity (INL) obtained using a linear fit of the TDG's DC transfer curve is plotted in Fig. 6.18. This indicates that better than

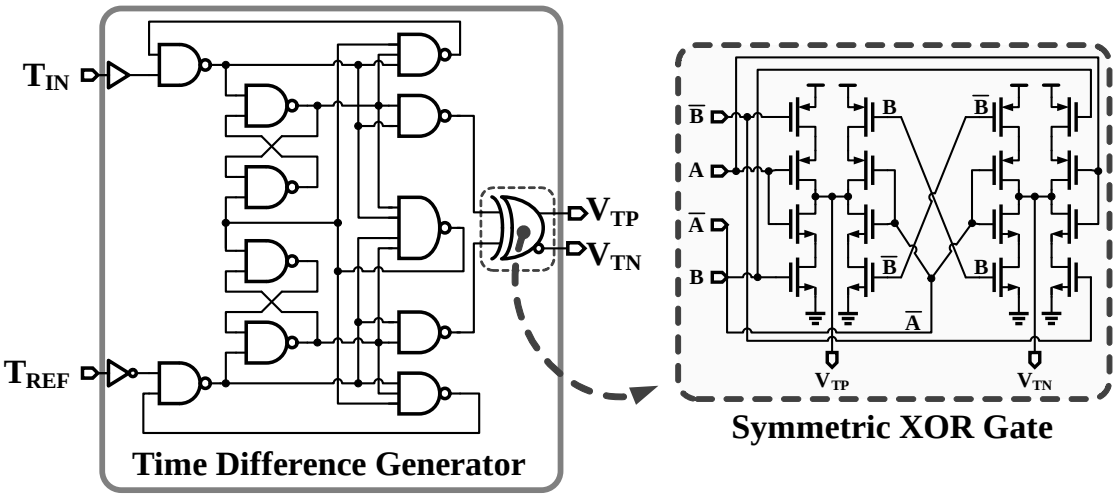


Figure 6.17: Schematic of the time difference generator (TDG), and the fully symmetric XOR gate.

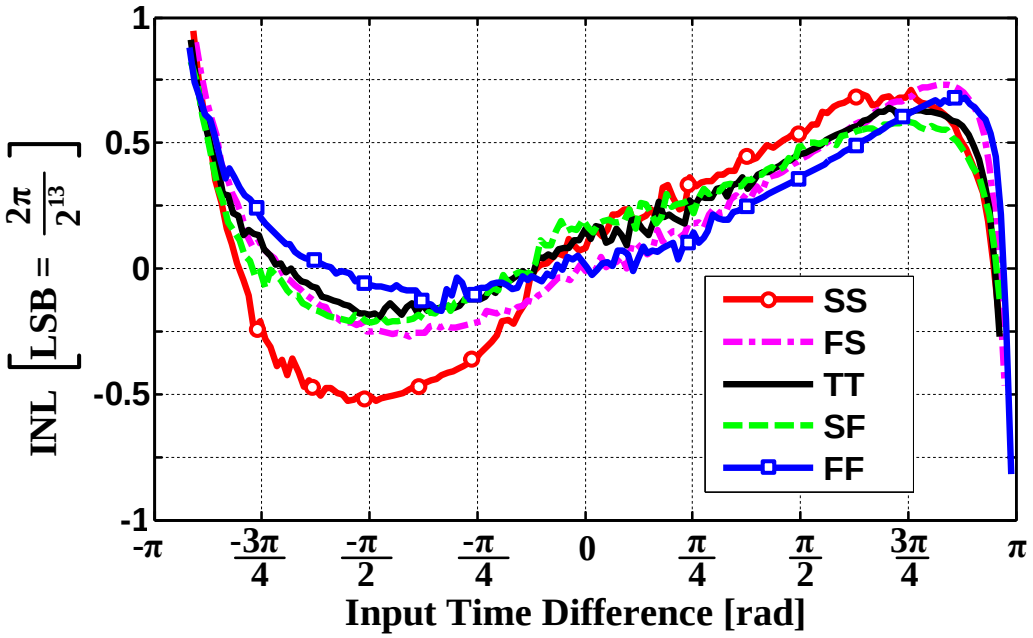


Figure 6.18: Simulated TDG integral non-linearity (INL).

13b static linearity is achieved with -0.5dB full scale input, under different process corner conditions.

6.4.2 SRO Implementation

The schematic of the SRO is shown in Fig. 6.19. It is implemented using a ground-switched 16-stage pseudo-differential ring oscillator. The delay cells are realized using CMOS inverters coupled in a feed-forward manner using a resistor to ensure pseudo-differential operation. The sources of all the NMOS transistors are connected together and switched between two voltages V_L and V_H. This voltage switching ensures fast switching between the high (F_H) and low (F_L) frequencies, respectively.

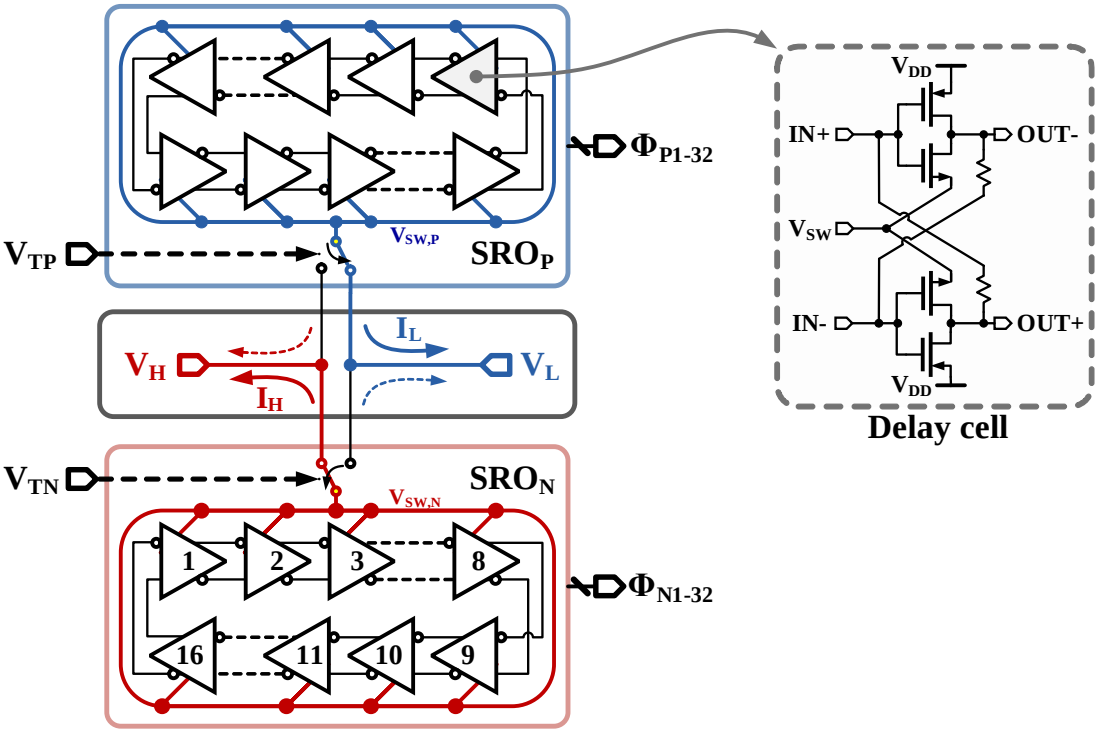


Figure 6.19: Complete schematic of the complementary SRO.

The power dissipation of the pseudo differential SRO-TDC is independent of the input time difference and input clock frequency. In SRO-TDC the two oscillators switch in a complementary manner between F_H and F_L such that the

combined current drawn from the supply is constant and equals to the sum of current for two oscillators running at F_H and F_H, respectively. In other words, the combined power of the two SROs is constant and is approximately equal to the power dissipated in one oscillator running at the highest frequency, F_H. This reduces the ripple on the supply and minimizes non-linearity due to the self-induced supply noise.

6.4.3 Phase Processor

The block diagram of the digital phase processor is shown in Fig. 6.20. It consists of a phase quantizer, ROM encoder, and a digital differentiator. Sense-amp flip-flops [28] are used to sample the SRO phase, and a transition detector compares adjacent sampled phases to detect phase transitions.

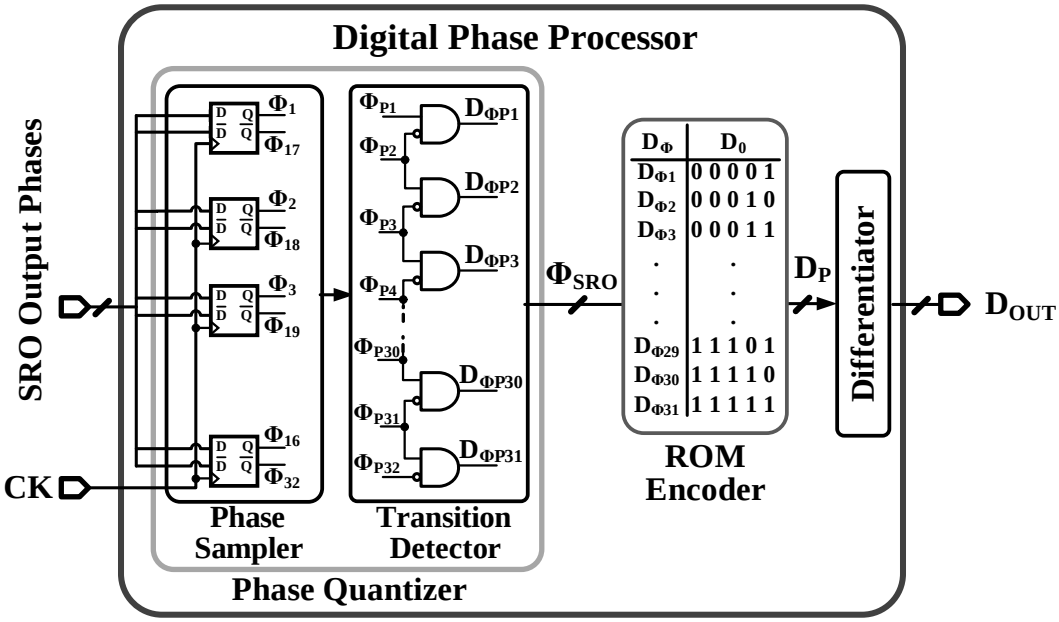


Figure 6.20: Block diagram of the digital phase processor.

It outputs a thermometer coded value of the quantized SRO phase. The

phase quantizer is then followed by a ROM encoder, which is used to map the 31-level phase quantizer output into a 5b binary code. The ROM encoder output is digitally differentiated to generate the final TDC output, D_{OUT}.

6.5 Experimental Results

The proposed SRO-TDC was fabricated in a 90nm CMOS process and occupies an active area of $0.02mm^2$ while operating from a 1.0V supply. The die photograph of the prototype chip is shown in Fig. 6.21, and a variable delay line is also integrated for testing purposes.

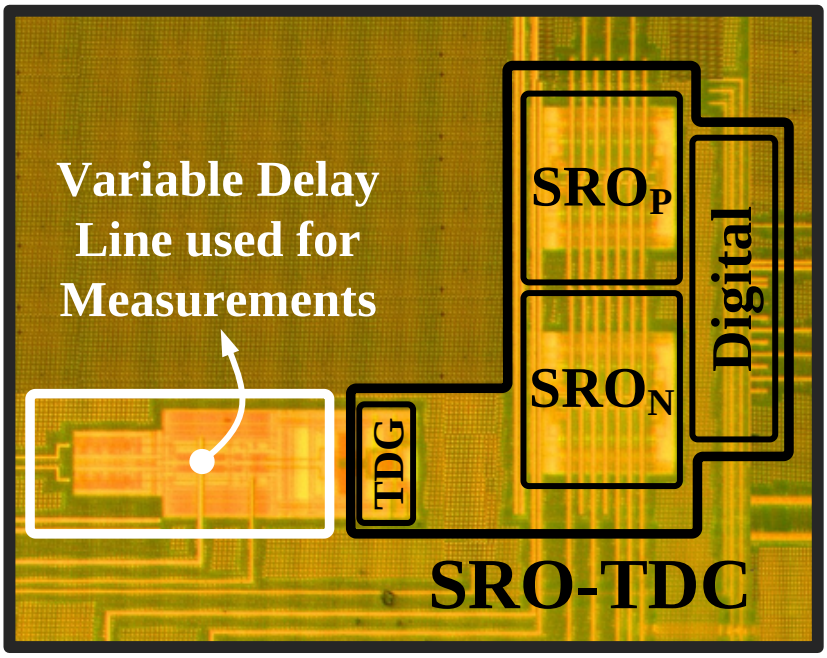


Figure 6.21: Prototype SRO-TDC die photograph.

6.5.1 Measurement Setup

The measurement setup used to characterize the prototype IC is illustrated in Fig. 6.22. Testing the linearity of a TDC is a challenging task due to the difficulty in generating a linear phase modulated input carrier. Two different methods to characterize the SRO-TDC were used. In the first method, an on-chip variable delay line is used as a phase modulator. The main limitation of this approach is the non-linearity of the delay line at large modulation amplitudes. In the second method, a phase modulated sinusoidal signal is generated using an arbitrary waveform generator. A first-order passive low-pass filter is used to suppress quantization error caused by the limited resolution of the AWG. A low noise PLL is used to suppress higher-order signal harmonics generated by the non-linearity of the arbitrary waveform generator.

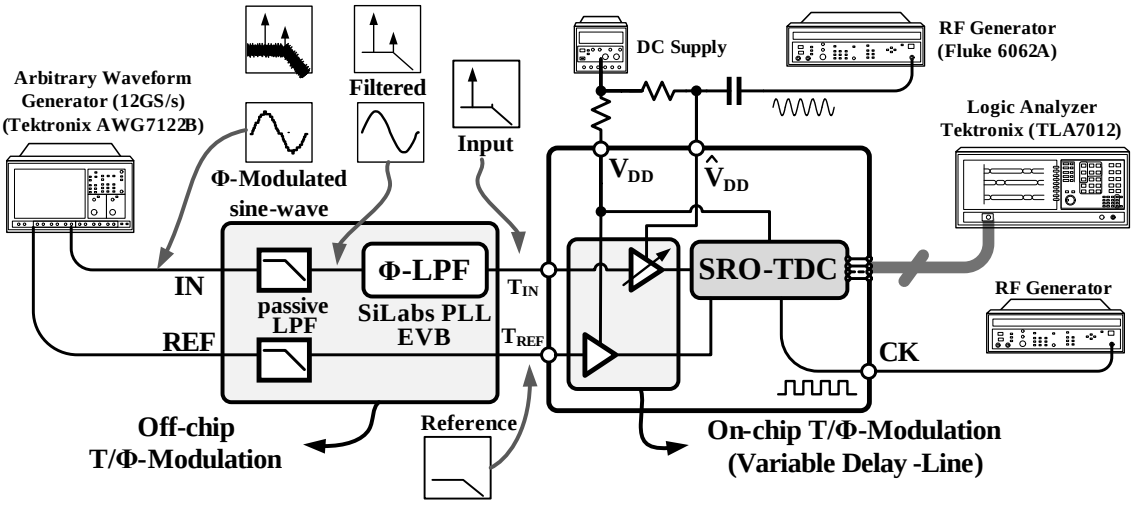


Figure 6.22: TDC measurement setup.

6.5.2 Measurement Results

The measured DC transfer curve is shown in Fig. 6.23. Averaged TDC output is plotted on the y-axis against the input time difference on the x-axis. It is obtained by offsetting the carrier frequency from the reference frequency and filtering the output with a 1MHz digital low-pass filter. The TDC achieves a measurement range of pi radians. No dead zones were observed in the DC transfer characteristic. The INL obtained from a linear fit of the transfer curve is shown at the bottom of Fig. 6.23. The worst case INL is equal to ±1.26ps.

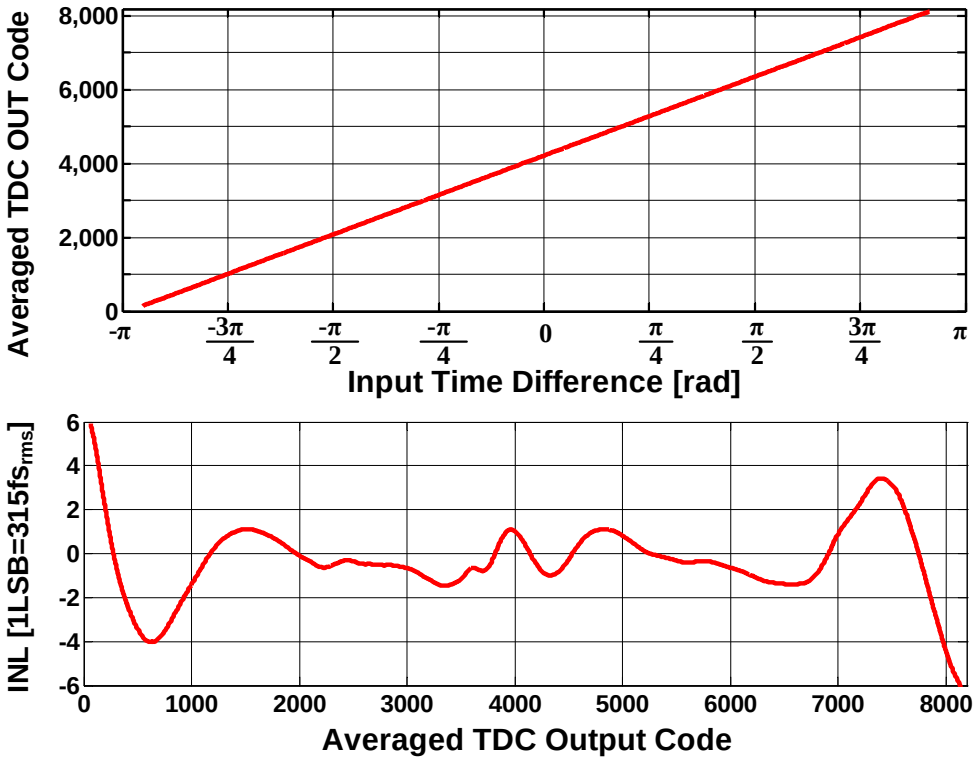


Figure 6.23: Measured DC transfer characteristics of the SRO-TDC.

The measured output power spectral density with a 60kHz 125ps peak-to-peak sinusoidal input is shown in Fig. 6.24. The sampling frequency is 500MHz and the carrier frequency is 80MHz. The measured results show good agreement

with the ideal first-order noise-shaping. The filtered time domain waveform after a 1MHz digital low pass filter is also shown in Fig. 6.25. The integrated noise in 1MHz bandwidth is 315fs$_{rms}$, and it increases to 1ps when the bandwidth is increased to 5MHz.

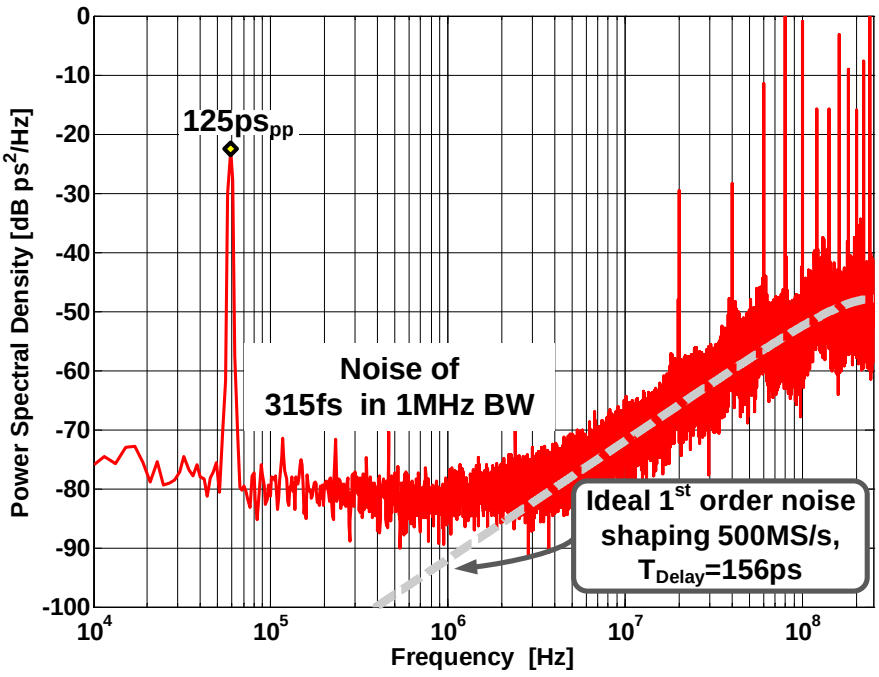


Figure 6.24: Measured output spectrum for a 125ps$_{pp}$.

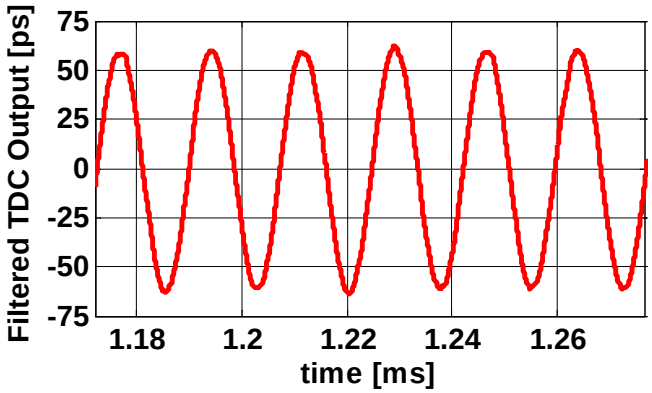


Figure 6.25: TDC output filtered with 1MHz digital LPF, for a 125ps$_{pp}$ input.

The output spectrum when the TDC is fed with a 8ps peak-to-peak sinusoidal input is shown in Fig. 6.26. The TDC is able to resolve this small input and similarly the filtered time domain waveform with a 1MHz digital LPF is shown in Fig. 6.27.

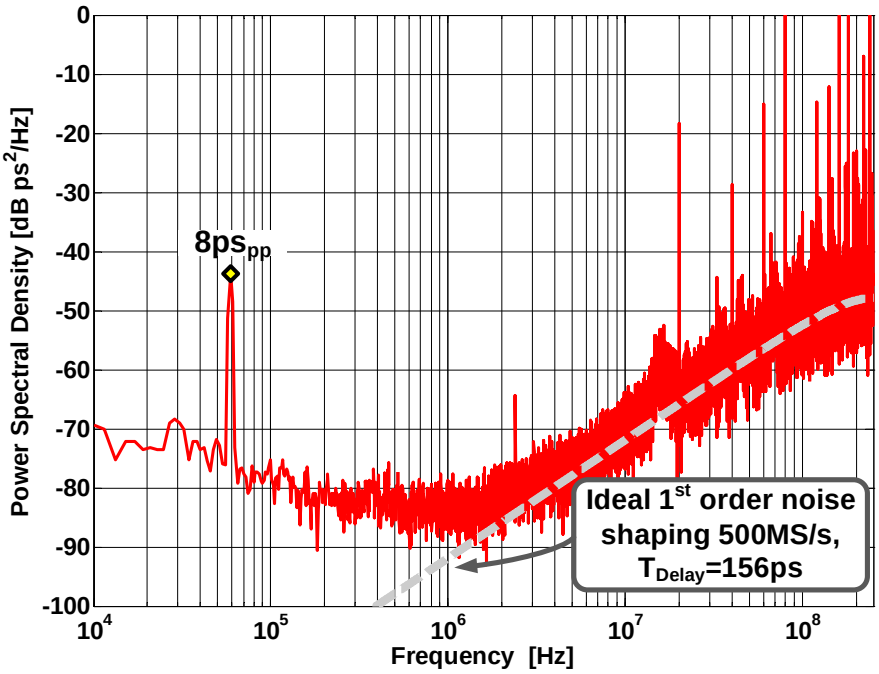


Figure 6.26: Measured output spectrum for a $8ps_{pp}$.

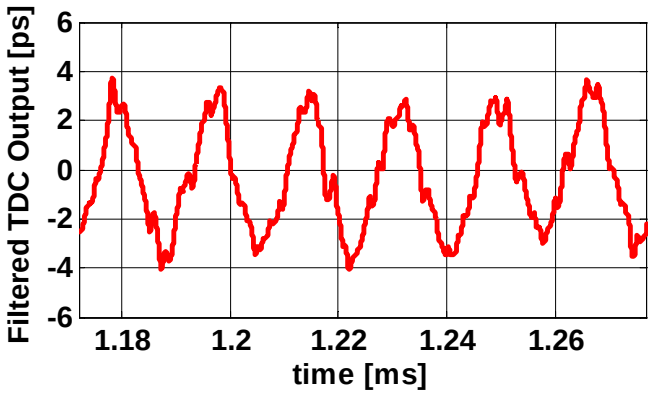


Figure 6.27: TDC output filtered for a small input of $8ps_{pp}$.

The integrated noise plotted as a function of OSR (varied by changing signal bandwidth) is shown in Fig. 6.28 illustrating two distinct regions. At lower OSRs, the TDC resolution is quantization-error limited, while at higher OSRs it is thermal/flicker-noise limited. As a result, with each doubling of the OSR, the total noise power reduces approximately by 9dB in the quantization error limited regime and by only 3dB in thermal noise limited regime.

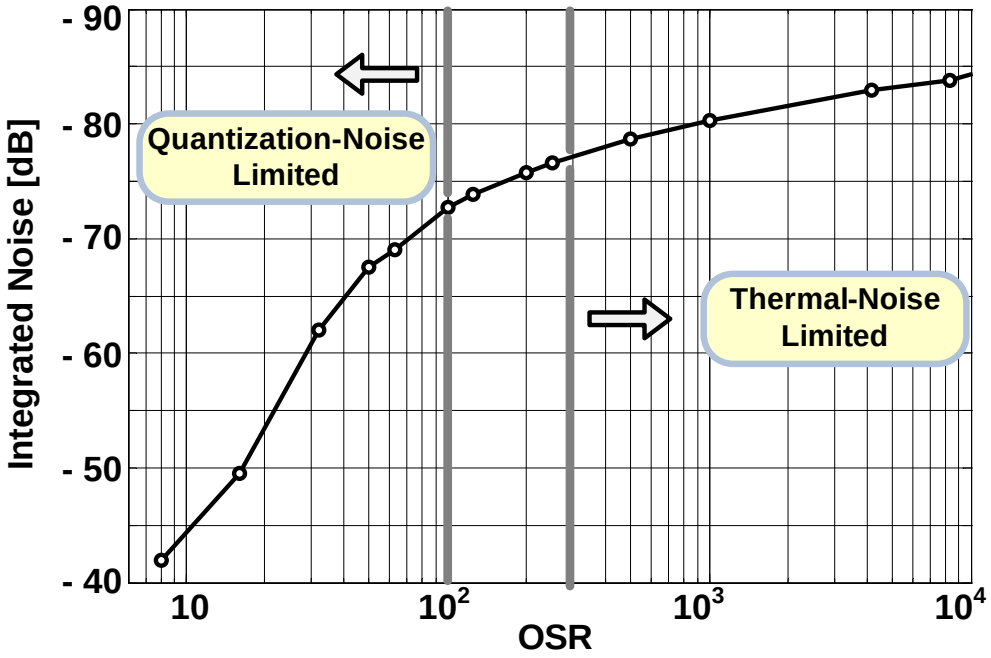


Figure 6.28: Integrated noise plotted as a function of OSR.

The measured output spectrum of the SRO-TDC for sampling frequencies of 250MS/s and 500MS/s is shown in Fig. 6.29. As discussed earlier, doubling F_S reduces the in-band quantization noise power by 9dB but also reduces the output signal power by 6dB, resulting in a net 3dB SNR improvement. This improvement is unique to our proposed TDC as illustrated by Fig. 6.29.

The integrated Noise in a 1MHz and 5MHz bandwidth are plotted versus the carrier frequency in Fig. 6.30. In a 1MHz bandwidth, the integrated rms noise

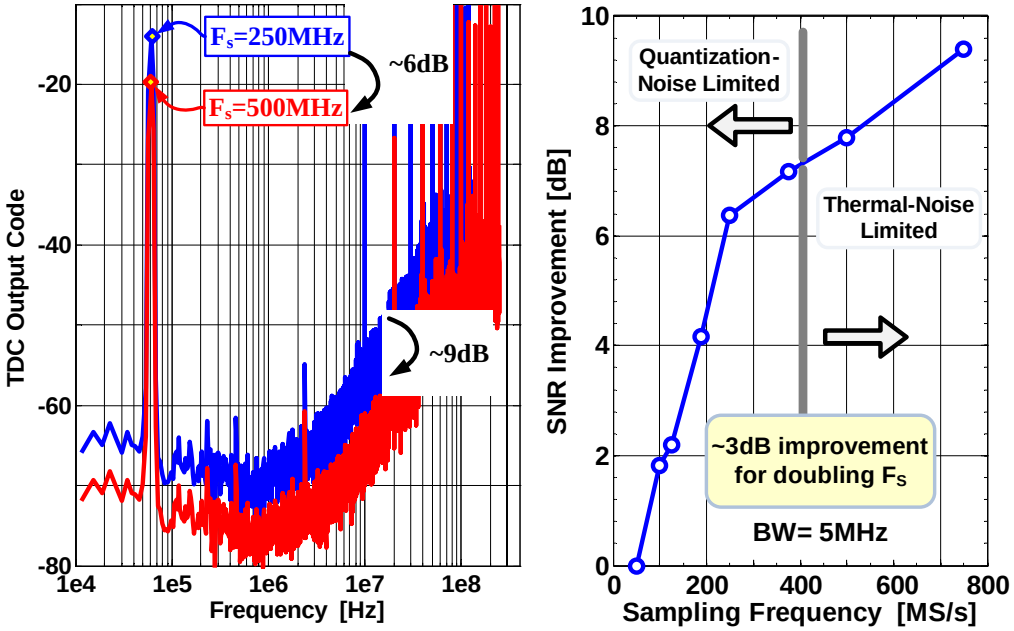


Figure 6.29: Measured spectrum for different sampling frequencies.

is less than $2ps_{rms}$ over carrier frequencies ranging from 10MHz-to-700MHz. The integrated jitter is less than $1ps_{rms}$ for any bandwidth lower than 5MHz for carrier frequencies higher than 50MHz. The performance summary for the SRO-TDC is summarized in Table 6.1.

6.6 Summary

A highly digital TDC using switched ring oscillator that decouples the carrier and sampling frequencies was presented. It operates over a wide range of both carrier and sampling frequencies. The use of switched ring oscillator reduces the skew error and provide immunity to deadzone. This facilitates the design of an area and power efficient TDC. As a result, this architecture achieves high resolution with immunity to analog circuit imperfections.

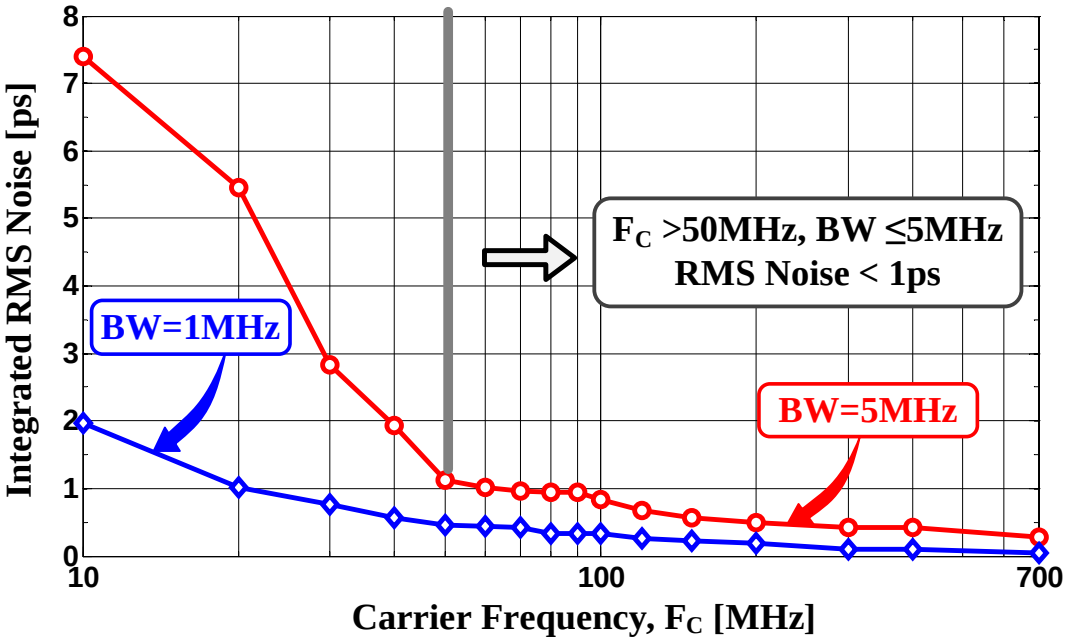


Figure 6.30: Integrated RMS noise plotted as a function of F_C.

Table 6.1: SRO-TDC Performance Summary

Technology	90nm CMOS
Supply voltage	1.0V
Input Carrier Range,F_C	0.6-to-750MHz
Sampling Frequency,F_S	50-to-750MS/s
Bandwidth	1MHz
Raw Delay/Stage	156ps
Integrated RMS Noise in 1MHz	315fs@F_C=80MHz
Range	±840ns@F_C =0.6MHz ±10ns@F_C =50MHz ±2ns@F_C =250MHz
Power Consumption	2mW
Area	0.02mm^2

CHAPTER 7. CONCLUSION

In this thesis, we have introduced, analyzed, and demonstrated a set of performance enhancement techniques that utilize digital circuits to improve the performance of clock multipliers in a variety of ways. Circuit and system design techniques that seek reducing clock jitter and mitigate the effect of supply noise on timing circuits have been explored.

The effect of clock jitter on system performance was first studied in Chapter 2, where we have discussed clock multiplication and supply noise mitigation techniques.

Several design enhancement techniques were applied to four distinct highly digital state-of-the-art designs. Within the scope of clock multipliers, the two common methods used to mitigate power supply noise have been investigated in the three designs in Chapters 3-5. On the other hand, Chapter 6 focused on time-to-digital conversion techniques to improve performance of digital clock multipliers.

We explored supply noise cancellation techniques in Chapter 3. It has been shown that the use of noise cancellation to mitigate the effect of supply noise provides an attractive alternative to the conventional suppression techniques implemented using regulated architectures. This allows significant area improvement over conventional approach, and enables area efficient designs. The DPLL prototype chip that employs digital background calibration to accurately cancel supply noise was presented, and measurement results validated the proposed scheme.

In Chapter 4, a digital PLL which improves supply noise rejection without the need for a high bandwidth regulator was presented and discussed. The proposed

DPLL decouples the regulator bandwidth tradeoffs exist in conventional DPLLs, and employs a low power regulator to achieve wide range of supply noise rejection. Because there is no requirements on the regulator bandwidth, a low power high performance clock multiplier was possible.

To further improve the performance beyond conventional PLL architectures, Chapter 5 examined the use of multiplying delay locked loops (MDLLs) for providing means of efficient clock multiplication. It was demonstrated that MDLL clock multiplication techniques, when combined with supply regulation, can achieve low jitter and excellent supply noise immunity. A calibration-free digital multiplying delay-locked loop (DMDLL) that obviates the need for a high-resolution TDC was presented. The MDLL prototype demonstrated the realization of sub-picoseconds of jitter, both random and deterministic, with sub-mW power consumption and femtoseconds/mV supply noise sensitivity.

Finally, in Chapter 6 highly digital time-to-digital conversion techniques were presented and discussed. A high resolution time-to-digital converter based on a switched ring oscillator (SRO-TDC) that achieves a first-order noise shaping was demonstrated and presented. This highly digital SRO-TDC with overcomes the leakage issues associated with conventional GRO-TDCs.

In all prototypes, highly digital circuitry was leveraged to efficiently achieve high-performance designs in advanced CMOS technologies. Measured results obtained from the prototype chips were presented to demonstrate the proposed design techniques.

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