AN ABSTRACT OF THE THESIS OF

Jyi-Ren Wang for the degree of Master of Science in Mechanical Engineering presented on December 20, 1994. Title: A Numerical Study of the Thermal Performance for Surface Mounted and Through-Hole Mounted Integrated Circuits

Abstract approved: _____
Dwight J. Bushnell

A numerical method for the analysis of temperature distributions and the prediction of maximum operating temperatures for both surface mounted and through-hole mounted IC packages is presented. Equations representing a two-dimensional model, coupled with convection boundary conditions and uniform package die heat generation, as based upon the finite-element method were solved.

The COSMOS/M finite-element software code was used to perform the analysis. The package model was generated using a computer-aided-design system, then exported for use with COSMOS/M code. After the geometrical configurations were meshed, the material properties of the components were input and thermal boundary conditions were described for each configuration. COSMOS/M was then used to automatically perform thermal network calculations as well as to generate a complete input file for the thermal network analyzer, which can then be used to perform thermal stress or other forms of thermal analysis.

Once the calculations were completed, the results were presented for convenient evaluation. The postprocessing capabilities of the COSMOS/M finite-element code include graphic and text displays of results. Package thermal network models can be stored in a database to allow for repeated use in the case of changes in either boundary conditions or material properties.

Since the predominant mode of heat transfer is based upon conduction, the thermal conductivity of package component materials has the greatest impact upon package thermal performance. Accordingly, the thermal conductivity of the various package components was analyzed to determine different effects upon package junction-to-ambient thermal resistance (θ_{ja}), which in turn provides a standardized judgement of the performance reliability of IC packages. These materials included dies, adhesives, lead and die attach pads, molding compounds, and printed circuit boards. In addition, the effect of power dissipation upon θ_{ja} was also addressed.

Based upon statistical regression analysis, a correlation equation for each surface mounted and through-hole mounted package was developed for package maximum operating temperatures, convective heat transfer coefficients, and the levels of power being dissipated. These equations were used to predict package maximum operating temperatures at given power dissipation levels for specified cooling strategies.

A Numerical Study of the Thermal Performance for Surface Mounted and Through-Hole Mounted Integrated Circuits

by

Jyi-Ren Wang

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Completed December 20, 1994
Commencement June 1995

Master of Science thesis of Jyi-Ren Wang presented on December 20, 1994

APPROVED:

Major Professor, representing Mechanical Engineering

Chair of Department of Mechanical Engineering

Dean of Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

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Jyi-Ren Wang, Author

ACKNOWLEDGEMENT

I wish to express my heartfelt gratitude to my major advisor, Dr. Dwight J. Bushnell, for his kindly guidance and encouragement. This thesis could not have been completed without his assistance.

I would like to thank the Department of Mechanical Engineering at Oregon State University for providing me with a teaching assistantship during my graduate program.

Without the devotion of my parents, my goals could not have been accomplished. Finally, I would like to express my sincere thanks to my fiancee, Yueh-Chou, for her love and consistent encouragement throughout this period of study.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF TABLES

NOMENCLATURE

k	Thermal conductivity (Watt/m °C)
T_{max}	Maximum operating temperature (°C)
P	Power dissipation at the die (Watt)
h	Convective heat transfer coefficient (Watt/m^2 °C)
G	Heat generation per unit volume (Watt/m^3)
t	Time (second)
T	Temperature (°C)
α	Thermal diffusivity (m^2/sec)
θ_{ja}	Junction-to-ambient thermal resistance (°C/Watt)
θ_{jc}	Junction-to-case thermal resistance (°C/Watt)
θ_{ca}	Case-to-ambient thermal resistance (°C/Watt)
Q	Heat generation per unit time and volume (Watt/m sec)
$\mathbf{q}_n$	Heat flux vector
$\mathbf{n}$	Outward normal unit vector
N	Shape function matrix
A	Area
$\mathbf{a}^e$	Vector of the nodal temperature
$\mathbf{K}^e$	Element stiffness matrices
$\mathbf{f}^e$	Element nodal force vectors

A NUMERICAL STUDY OF THE THERMAL PERFORMANCE FOR SURFACE MOUNTED AND THROUGH-HOLE MOUNTED INTEGRATED CIRCUITS

CHAPTER 1
INTRODUCTION

1.1 Background and Research Motivation

Packaging of electronic circuits is the science and the art of establishing interconnections and a suitable operating environment in which predominantly electrical circuits can process or store information [1]. As the present decade has opened, the quest for smaller sized and higher performance systems has led to an increase in power dissipation per circuit and an increased number of circuits per package. As microelectronic power densities increase, the need for accurate prediction of operating junction temperatures is becoming crucial. Engineers designing reliable packages have the responsibility to ensure that the steady-state package temperatures remain within the operating temperature ranges of integrated circuit (IC) packages.

In the packaging hierarchy, several levels of packaging have been used, depending on the degree of integration and the totality of packaging needs. For example, quad flat pack (QFP) and pin-grid array (PGA) are referred to as first-level packaging, whereas multilayer cards or boards are identified as second-level packaging. Between the first- and second-levels there are two basic types of connections: those with pins requiring plated-through-holes (PTH) or those with surface mounted pins (i.e., SMD, surface mounted devices using SMT, or surface

mounted technology) or pads. In Figure 1.1, all the available packages are classified in one of these two categories.

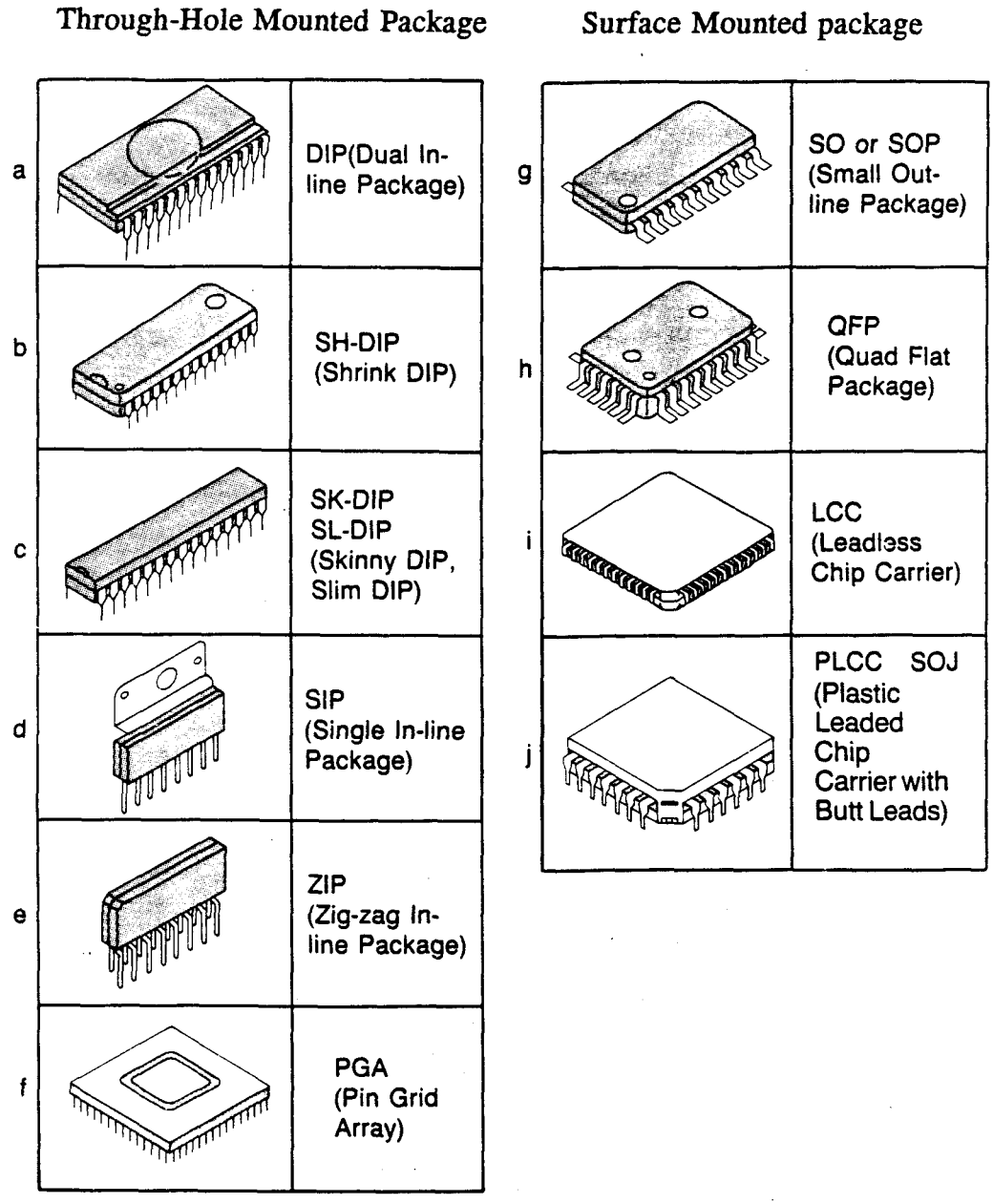

Figure 1.1 Typical plate-through-hole and surface mounted packages.

In many cases, chemical corrosion processes responsible for many of the failures found in IC packaging are temperature-dependent. Higher temperatures in IC packages accelerate reactions and shorten the time to failure, and also have a significant effect on the operation and lifetime of the component junctions. Increasing junction temperatures results in an increase in reverse voltage, which contributes to a further increase in power dissipation. This cycle continues until the temperature difference between the package component junctions of components and their environment reaches a level where the heat transfer rate matches the rate of heat production. Consequently, where there is poor heat transfer the equilibrium temperature can be high, and can result in severe damage to the IC package.

As depicted in the listing of acceleration factors for hybrid circuit elements shown in Table 1.1, higher operating temperatures increase the failure rates of essentially all components within an IC package [2,3,4]. Overall, the failure rate of a typical IC increases exponentially with temperature, as illustrated in Figure 1.2 [4,5]. Other IC types show the same overall pattern of behavior. These data indicate that it is important to maintain low operating temperatures to promote extended device and system lifetimes, and that the acceleration factor can be highly nonlinear for such devices features as intermetallic bonds.

Clearly, it is necessary to conduct thermal analysis prior to the manufacture process to ensure that the operating temperatures within the package do not exceed the extended lifetime limits for particular device elements. Hence, the present

Table 1.1 Thermal acceleration factors for various hybrid circuit elements.

Circuit Element	25°C	50°C	75°C	100°C	125°C
Au-Al ball bond	1	4	20	100	1200
Au-Au wedge bond	1	1	1	1	1
Al-Al wedge bond	1	1	1	1	1
Thick - film resistor	1	2	3	4	5
Chip capacitor	1	1.5	2.5	6	25
Low-power trans. chip	1	3	9	27	70
High-power trans. chip	1	2	6	18	54
SSI circuit (25 gates)	1	1.8	9	41	--
LSI circuit (100 gates)	1	1.8	9	--	--

-- indicates no data available

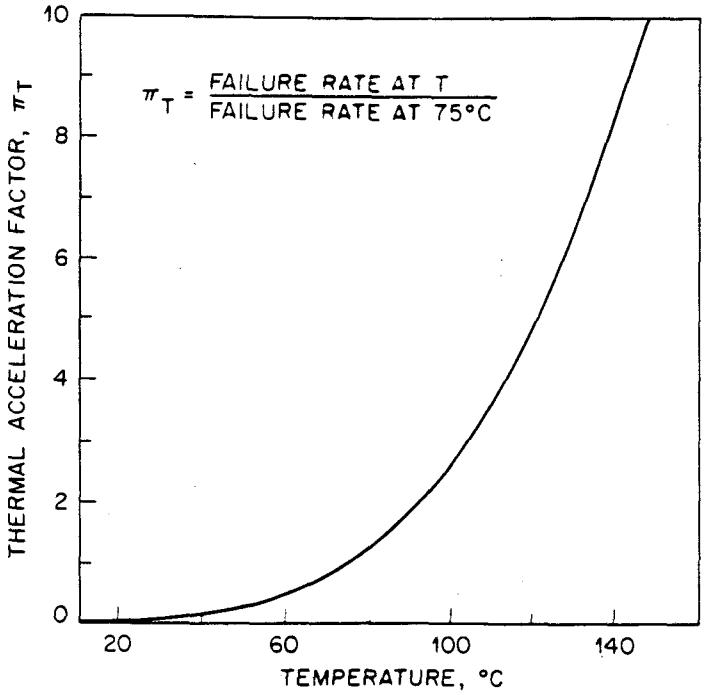

Figure 1.2 Thermal acceleration factor for failure of bipolar digital devices.

study consists of a numerical analysis using different boundary conditions of thermal performance for both surface mounted and through-hole mounted IC packages.

1.2 Research Description

With reference to the geometrical configurations given in Figure 1.3 - 1.5, and based on a varied choice of materials for package and PCB components, as described following , the objectives of the present numerical analysis are as follows:

1) Measure the effect of different materials on the thermal resistance of a molded package for both surface mounted and through-hole mounted packages.
2) Obtain steady-state temperature distributions and maximum operating temperatures within the packages for each situation when one and only one element of the package composites is changed, while other elements remain unchanged.
3) Derive a favorable numerical correlation in the form

$$T_{max} = f(P, h)$$

where P is the power dissipation at the die and h is the convective heat transfer coefficient.

4) Demonstrate the most effective means to improve package thermal performance.

A number of analytical and numerical tools exist for the performance of the thermal analysis of microelectronic equipment, varying in accuracy, flexibility, and modeling realism. They range from analytical models (e.g., TASIC, TAMS) and thermal network analyzers (e.g., TNETFA, CINDA) to finite element codes (e.g., ANSYS, NASTRAN, COSMOS/M). Analytical methods have the advantage of providing exact solutions, but these solutions cannot be applied to most realistic package geometries. Therefore, most microelectronic heat transfer problems require numerical analysis. Moreover, numerical solutions are usually preferable where several separate materials and interfaces are present. However, different types of IC packages have been studied using various forms of thermal analysis.

A finite-element method (FEM) code (COSMOS/M) has been employed to analyze temperature distributions within some packages. Since the computing time and the memory space required by three-dimensional cases are an order of magnitude greater than those for two-dimensional cases using numerical computation, a two-dimensional model is considered for the present study. Figure 1.3 shows the cut -away view of an IC package; Figure 1.4 illustrates a cross-section view of a surface mounted package on a printed circuit board (PCB); Figure 1.5 shows the cross-section view of a PCB-mounted through-hole package; and the basic sizes, referred to in Figures 1.2 - 1.4, are given in Table 1.2.

The materials used for packaging electronic devices play key roles in the proper function and useful life of the package assembly. The most obvious function is the conduction of the signals through the circuit, contributed by metals

in the form of wires, contacts, foils, plating, and solders. The electrical insulation function, which prevents the loss of signal currents and confines them to desired paths is of equal and often greater importance. The insulation systems exist in a variety of forms, including liquids, solids and gases, and they determine the life of the devices. Other materials perform structural roles and support the circuit physically.

Symbol	Size unit:cm
OL_w	1.56
M_w	1.26
L_w	0.9
D_w	0.78
A_w	0.88
BS_w	1.32
M_t	0.5
P_t	0.22
S_t	0.12
t_a	0.09
s	0.10

Symbol	Size unit:cm
d_t	0.21
t_d	0.09
$t_{D/A}$	0.02
$t_{L/F}$	0.05
d_b	0.13
t_l	0.05
L/F Down set	0.04
S_w	0.19

Table 1.2 Dimensional values used for numerical computations.

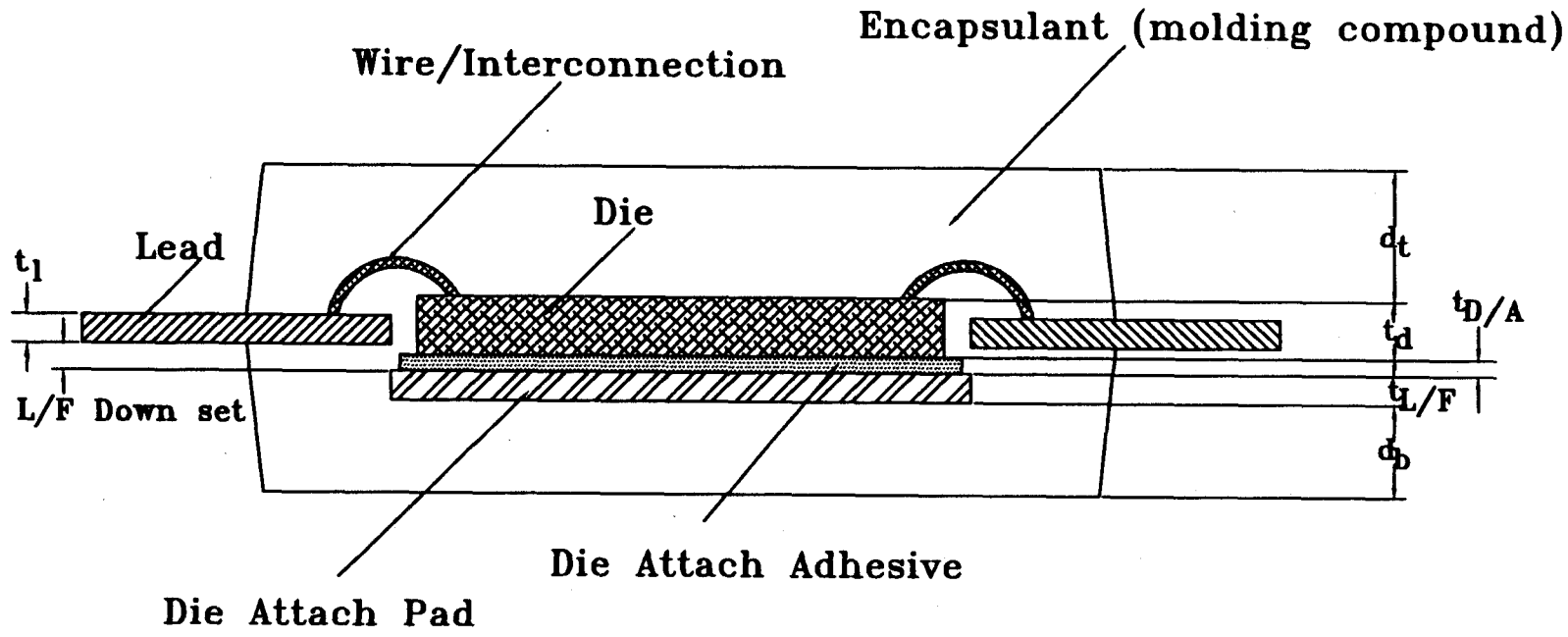

Figure 1.3 Cut-away view of an IC package, provided by National Semiconductor, INC.

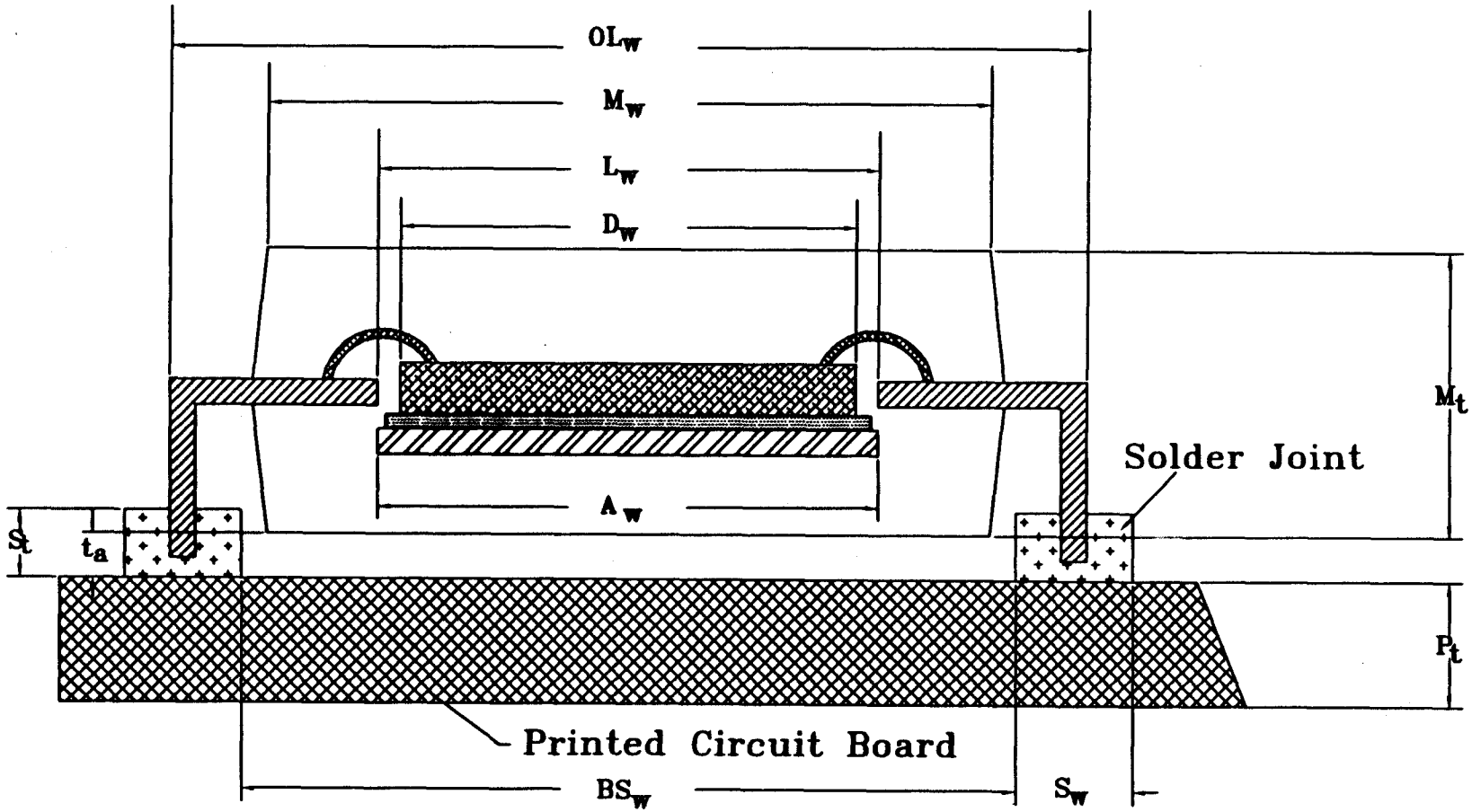

Figure 1.4 Cross-section view of a surface mounted IC package.

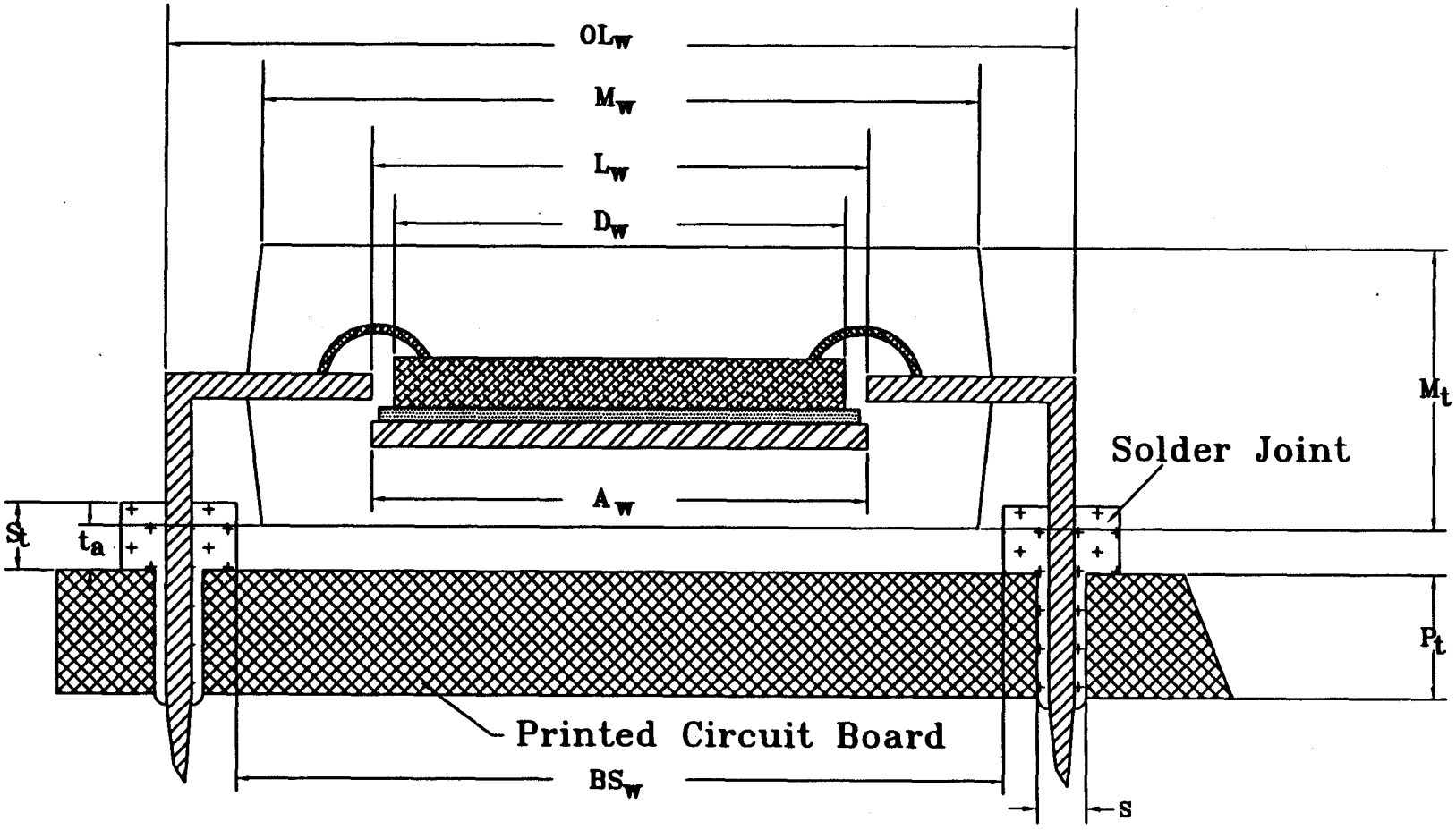

Figure 1.5 Cross-section view of a through-hole mounted IC package.

For the present study, a molded IC package was assumed to be a composite system made up of the following parts:

- die (or chip),
- die attachment material,
- molding compound,
- die attach pad,
- lead, and
- wire/interconnection.

With respect to the physical properties of the materials commonly used a molded IC packages, the three most important semiconductor types are composed of germanium (Ge), silicon (Si), and gallium arsenide (GaAs), principally used as dies. Germanium and silicon have been used extensively, whereas gallium arsenide presents different properties than the other two materials. In particular, GaAs provides a different bandgap for photonic applications, a different interval-carrier transport, and a higher mobility for the generation of microwaves than silicon. Compared to bipolar silicon, GaAs also requires up to 50% less power. In addition, GaAs devices can operate over wide temperature ranges (-200 °C to +200 °C), making them ideal for applications such as automotive uses that involve higher operating temperatures. Table 1.3 indicates the thermal properties of Ge, Si, and GaAs.

The most widely used method for attaching dies to interconnect substrates is the epoxy adhesive bonding method. An estimated 90 percent of all hybrid

Table 1.3 Thermal properties of semiconductor material: Ge, Si, and GaAs.

Thermal properties	Germanium Ge	Silicon Si	Gallium arsenide GaAs
Specific heat unit: Joule/g °C	0.31	0.7	0.35
Thermal conductivity unit: Watt/m °C	60	150	46
Thermal diffusivity unit:cm^2/sec	0.36	0.9	0.44

microcircuits produced employ epoxy adhesives because of their low cost, low processing temperatures (125 °C to 165 °C), and ease of rework. Attachment materials serve three functions: mechanical, electrical, and thermal. The foremost consideration is that the attachment material provides sufficient bonding strength to assure that components remain in place, not only for the life of the circuit, but also during accelerated mechanical, thermal, and chemical stresses that may be imposed during processing and screen testing. To ensure the highest levels of performance and reliability, the choice of die attachment materials may have to meet the requirements of specific applications and be compatible with specific packaging technologies. Table 1.4 summarizes the thermal conductivity of the most commonly used die attachment materials.

The molding compound is the most important polymer material used in plastic packaging for IC devices. It provides both mechanical and chemical

Table 1.4 Thermal conductivities of adhesive materials used for die and substrate attachment.

Die attachment materials	Type	Thermal conductivity unit: Watt/m °C
Silver filled epoxy	Electrically conductive Solvent-free paste	1.56~2.6
Gold filled epoxy	Electrically conductive Solvent-free paste	2.08
Alumina filled epoxy	Electrically insulative Solvent-free paste	0.66~1.44
Epoxy film	Electrically insulative	0.173

protection for the device at costs that are significantly below those for metals, ceramics or glass packaging, as well as below those for premolded plastic packaging. The principal requirements of molding compound are to offer very high yields, high productivity, and good reliability. Several different types of molding plastics can be used for IC packaging, but the epoxy molding compounds are by far the most commercially important materials. Alternative materials have filled some specialty niches, and their use could grow significantly in the future as the rapid increase in device size and lead count extends epoxy molding materials to their limit. Table 1.5 lists the thermal properties of the typical molding compounds commonly used in the electronics industry.

The die attach pad is the central supporting structure of the package to which every other element is attached. Etched or stamped from a thin sheet-metal

Table 1.5 Thermal properties of typical molding compound materials [19].

Thermal properties	Alumina	Kovar	Epoxy molding compound	Sealing glass
Thermal conductivity unit: Watt/m °C	18~19.6	17.5	0.58~0.67	0.6
Coefficient of thermal expansion unit: 10^{-6}/°C	7.0~7.2	5.3	$\alpha_1 \leq 23$ $\alpha_2 \leq 80$	6.3~7.0

strip into a filigree or narrow beams that radiate from a central platform, the pad carries the die throughout the assembly process and is imbedded in plastic after molding. The material selection for the die attach pad depends on factors such as cost, ease of fabrication, and specific functional requirements. A number of alloys formulated for plastic IC packages are indicated in Table 1.6.

Table 1.6 Thermal properties of lead and die attach pad materials.

Thermal properties	Copper alloy MF 202	Alloy 42	CDA 155	TAMAC 5	OLIN 194	Alloy 151
Thermal conductivity unit:W/m°C	160	15.7	347.27	190	263	359.8
Coefficient of thermal expansion 10^{-6}/°C	17.0	4.5	17.7	16.7	16.3	17.7

The lead is electrically connected to the die with fine-diameter gold wires ($k = 300$ W/m°C). In many practical applications, the materials of the lead can be the same as the materials of the die attach pad, but have different functions and cost considerations. Heat conduction along the lead is an important heat dissipation mechanism in molded plastic packages, and the superior thermal conductivity of the alloys makes them a good choice for high-power devices. When choosing lead materials, consideration must be given to the degree of adhesion of the molding compound to the lead, thermal-mechanical shrinkage stresses, the trim and form characteristics of the materials, and the buckling resistance of the lead after molding. All of these characteristics have direct implications for packaging yield and reliability.

From Table 1.6, Alloy 42 provide the lowest coefficient of thermal expansion. For this reason, it is a very popular material in common use for leads or die attach pads. Alloy 42 contains iron and nickel with just trace amounts of other materials. Compared to other copper-rich alloys, its significantly lower coefficient of thermal expansion allows Alloy 42 to provide lower thermal shrinkage stress and better adhesion to epoxy molding compounds. Its greater rigidity confers better resistance to damage during assembly and molding operations, and assures less buckling under the compressive loads applied by the molded body. But the principal drawback of Alloy 42 is its low thermal conductivity. IC packages using Alloy 42 as lead and die attach pad materials have less power dissipation capacity. When higher power dissipation capacity is a

serious consideration, Alloy 42 is often replaced by the copper alloys. In fine-pitch applications, thinner leads and die attach pads are used, particularly where the applied materials require higher strength properties. Specifically, through-hole mounted packages require high-strength lead and die attach pad materials to resist damage when they are inserted through the PCB.

Printed circuit boards, or PCBs, are often referred to as the baseline in electronic packaging. PCBs serve a wide variety of functions. Foremost, they contain the wiring required to interconnect the package electrically and act as the primary packages support structure. In some instances the PCB is also used to conduct and disperse IC-generated heat. The PCB is thus the interconnection medium upon which electronic components are formed into electrical systems, and is a laminate composed of four materials that usually constitute its base fabric: e-glass, s-glass, quartz, and aramid (aromatic polyamide polymer) fiber. The thermal properties of each are given in Table 1.7.

Table 1.7 Thermal properties of printed circuit board materials

Thermal properties	e-glass	s-glass	Quartz	Aramid
Specific heat unit: cal/ g°C	0.197	0.175	0.230	0.260
Thermal conductivity unit:W/m°C	0.89	0.9	1.1	0.5

After the leads have been formed, several solder coatings are often required to facilitate high-yield attachment to the circuit board for both surface mounted and through-hole packaging. This thin coat of solder, typically less than 0.0005 inch, is applied using either a solder-dipping or solder-plating operation. The elements commonly used in solder alloys are tin (Sn), lead (Pb), silver (Ag), bismuth (Bi), indium (In), antimony (Sb), and cadmium (Cd). Hereafter, the solder joint is specified as Pb-In ($k = 22$ Watt/m°C). The effect of solder joint materials will not be investigated, because it is not obvious compared to other package components.

CHAPTER 2
LITERATURE REVIEW

Advances in the state of the art for thermal packaging of electronic equipment are leading to unforeseen and continuous improvements. The field of thermal management in electronic equipment has thus become both broader and more diverse. Several texts, including those by Scott [6] and Kraus and Bar-Cohen [7], may be recommended for reviewing the fundamentals of this field. The scope of this chapter is to highlight some of the more important methods and discoveries, as well as to describe some details of past studies related to the present investigation.

Simons [8] pioneered the thermal management study of electronics packages, deriving two primary objectives for thermal management of electronics packages. The first objective was to ensure that the temperatures of all components were maintained within their specified functional limits. Failure to satisfy this objective could have adverse consequences, ranging from logic failures to actual physical destruction of the component package. The second objective was to ensure that the distribution of component operating temperatures satisfied reliability objectives. Simons also described nonconventional package cooling applications and discussed environmental considerations and constraints related to thermal management. The results of this research indicated that to meet future trends toward higher circuit densities, higher circuit power, and the demand for increased reliability in overall package thermal design, both internal and external

package thermal resistance had to be reduced rigorously. It was suggested that this reduction could be achieved by appropriate selection of materials and development of potential methods of package cooling enhancement.

Ellison [9] introduced two programs, TAMS and TNETFA, which could be used for IC package thermal analysis and design. Both of these digital computer programs are based on solutions to the partial differential equation for heat conduction. TAMS is capable of analytically determining temperatures at the center of rectangular multilayered substrates. The bottoms of substrates may be cooled by convection or held at an isothermal temperature, while the sides of rectangular substrate are assumed to be insulated. The geometries not within the restrictions of the three-dimensional slab requirements of TAMS may be represented by a thermal network model. Such models may be used to describe adequately nearly all thermal packaging problems and may have the advantage of being able to accommodate nonlinearities, including temperature-dependent quantities such as thermal conductivity, natural convection heat transfer coefficients, and the rather complex multiple surface radiation exchange phenomena. The program TNETFA includes these phenomena as well as others, and can be used for both steady-state and transient thermal problems to predict temperatures, pressures, and air flows.

Funk et al. [10] developed a quick, easy-to-use, semi-analytical method for the prediction of steady-state temperatures on PCBs subject to heating by a single or multiple heat sources. The method included separate analytical solutions for the

circuit board and for the packages to be mounted on the board. The board solution was developed using Green's function method for solving the heat diffusion equation. For the IC package, the solution of the heat diffusion equation was obtained by using the method of separation of variables. The temperature solution for the package was determined by using an iterative procedure between the package model and the board model. The accuracy of the method was verified by comparison with detailed FEM techniques. Findings indicated that the use of this method could help to reduce design costs since repetitive finite element model generation to change package configuration was eliminated, and the number of expensive prototypes required was decreased. This method also offered significant advantages in reduced CPU time and could be feasibly used on a 386-PC, eliminating the need for mainframe access.

Nigen and Amon [11] conducted numerical investigation of the thermal and fluid behavior of five different grooved-channel geometries, three of which differed in groove width, two in groove depth, and one consisting of a suspended electronic package. In this study, the local heat transfer coefficients were determined within the groove and used to calculate the temperature distributions within surface mounted packages. The importance of using locally-defined instead of spatially-averaged heat transfer coefficients for thermal design and the analysis of electronics packages was also discussed. Through comparison of maximum junction temperatures, the effectiveness of self-sustained oscillatory flows in enhancing the convective cooling of surface mounted packages was demonstrated.

Furthermore, for a typical electronic package, they found that the use of spatially-averaged heat transfer coefficients led to significantly different temperature distributions. The accuracy of the spatially-averaged heat transfer coefficient was related to the proportion of the total surface area corresponding to the top of the package. In this case, the use of the average value led to underestimates of maximum temperatures and internal temperature gradients. However, this might not always have been the case, and it was suggested that thermal designers must be careful when using spatially-averaged heat transfer coefficients.

Hadium and Nagurny [12] developed a numerical analysis of the effects of several important thermal design parameters on the thermal performance of surface mounted LCC (leadless chip carrier) packages, including the following: chip and carrier size, cavity floor thickness, air gap thickness, die and carrier materials, and solder material. INSTAN, an interfacing software package for thermal analysis, was used to generate thermal network representations of the models in conjunction with a thermal network analyzer. It was found that both the die size and carrier size had a significant effect on thermal resistance and that effect was more pronounced in smaller dies and chip carriers. When the base floor thickness was increased, thermal resistance decreased rapidly and reached an asymptotic value when the base floor thickness was greater than 30 mils (0.762 mm). An increase in air gap thickness from 1 mil (0.0254 mm) to 5 mils (0.127 mm) resulted in a larger increase in thermal resistance than when the air gap thickness was increased from 5 mils (0.127 mm) to 10 mils (0.254 mm). When a thermal adhesive was

used in the air gap, the thermal resistance was drastically reduced, whereas it remained virtually constant with changes in carrier size. The change in thermal resistance with carrier size was more significant when the carrier material had low thermal conductivity. In addition, these results demonstrated the use of INSTAN software for efficient thermal design optimization in electronics packaging.

Cooley and Razani [13] proposed a method for the thermal analysis of complex geometries for a wide range of applications. Their method was based on homogenization or simplification of a complex region by the introduction of an effective homogeneous material. Using this method, different models of heat transfer could be lumped together and various available computer codes could be utilized for the rapid thermal design analysis of microelectronic devices. Results indicated that the single parameter θ_{jc} (i.e., thermal resistance between junctions and the case) was limited in its applicability. The analysis indicated that single parameters were no longer feasible for the thermal analysis of complex microelectronic systems requiring three-dimensional system modeling. Finite element modeling provided an accurate method for temperature prediction in microelectronics and was particularly attractive when model simplifications were necessary to save either or both time and costs. It was concluded, both theoretically and experimentally, that junction to case temperatures were not convenient parameters for thermal characterization of the heat transfer processes in the complex geometry under consideration.

Rajala and Renksizbulut [14] conducted a thermal analysis of a ceramic microelectronic package with six configurations, under prescribed free- and forced-convection conditions. The results of their numerical study compared favorably with the available experiment data for both free- and forced-convection cases, and demonstrated that thermal radiation accounted for about 21 percent of the total heat transfer from the package in natural convection. But in forced convection, both for cavity-down and cavity-up configurations, the thermal radiation effects were found to be negligible, accounting for less than 5 percent of the total energy removed.

Aghazadeh and Mallik [15] presented a study at the 1990 IEEE 6th Annual Semiconductor Thermal and Temperature Measurement Conference which focused attention upon the thermal performance of single- and multi-layer PQFP packages. Using experimental and computational techniques, it was shown that significant reduction in package thermal resistance could be achieved by using a multi-layer lead frame structure for medium- and high-lead count PQFP packages. They also demonstrated that the contribution to overall thermal resistance of low thermal conductivity insulating adhesive tape was about 1 (°C/Watt). In addition, it was observed that increasing the power and ground plane thickness from 6 to 10 mils (0.1524 to 0.254 mm) resulted in only about 1.5 (°C/Watt) improvement in the junction to ambient thermal resistance (θ_{ja}).

Liu, Hunter, and Kozarek [16] developed an emerging analysis tool called the boundary element method (BEM) for the thermal evaluation of electronic

packaging systems. The BEM, discretizing only the problem boundary, provided a potentially faster method of problem modeling. Particularly for three-dimensional models, parametric variations of particular designs could be evaluated more rapidly. It was suggested that this decreasing turnaround-time could become a priority in the future analyses of more sophisticated VLSI (very large-scale integration) or PGA (pin-grid array) packages which required design optimization on size and space arrangements to achieve higher power capacity. The BEM results were compared to FEM models, using FIDAP™, and demonstrated no apparent differences in accuracy between models. The BEM models could also serve as a tool for linear elastic thermal stress calculations during initial package design stages.

Ozmat [17] compared the thermal performance of multichip modules (MCM) based upon interconnection technology. The comparisons were made for hermetic- and conduction-cooled environments. Thermal performance for high density interconnect (HDI) technology, the flipped-chip (FCP) technology, and the flipped-tape automated bond (FTAB) technology were analyzed and compared for MCM applications. The COSMOS/M finite element software package was employed to analyze the thermal performance of each interconnect technology and to suggest the most effective ways to improve MCM performance.

Bar-Cohen, Elperin, and Eliasi [18] examined the θ_{jc} (junction-to-case thermal resistance) characterization of IC packages. To fully characterize thermal behavior, it was proposed that there was a numerical correlation among package

temperature, the temperature of each distinct segment of the package, and power dissipation. It was suggested that thermal steady-state package temperature could be expressed by

$$T_j = \sum_{k=1}^{n} A_k T_k + A_{m+1} Q \qquad (2\text{-}1)$$

where Q was internal heat dissipation within the package. The quality and utility of the analytical chip junction temperature relation was evaluated with a numerical analysis of a plastic-leaded chip carrier (PLCC) package, 2.9 cm wide and 0.335 cm high. A PLCC T_j relation, of the form (2-1), was extracted from the results obtained via a 360-element, two-dimensional generic, finite element ANSYS model. The numerical results neglected contact resistances within the package and assumed uniform heat generation within the package. Using plastic, silicon, and aluminum thermal conductivities of 1.5, 175, and 190 Watt/m °C, this operation yielded the T_j relation

$$T_j = 0.366\,T_\tau + 0.00031\,T_{lead} + 0.617\,T_{bot} + 0.0159\,T_{side} + 8.37\,Q$$

for the narrow heat spreader, and a significantly lower thermal resistance expression for the wide heat spreader:

$$T_j = 0.339\,T_\tau + 0.001\,T_{lead} + 0.588\,T_{bot} + 0.071\,T_{side} + 5.61\,Q$$

This proposed approach was not only capable of accurately describing the package temperature for a variety of thermal management strategies, but it also highlighted the impact of specific thermal design features.

CHAPTER 3
THEORETICAL ANALYSIS

In a typical IC package the heat dissipated at the die as a result of the conversion of electrical energy to heat is transferred to the package external surface by a conduction mechanism. The die attach pad, bonding wires, lead, and molding compound are all conduction paths that the heat follows to leave the die. Heat pulled through the bond wires and into the lead is generally conducted into the PCB itself, spreading through the ground planes. Heat that goes through the molding compound is conducted to the surface of the IC package and radiated to other surrounding surfaces or convected into the IC ambience. Figure 3.1 illustrates a typical heat flow mechanism from the package to the IC ambience.

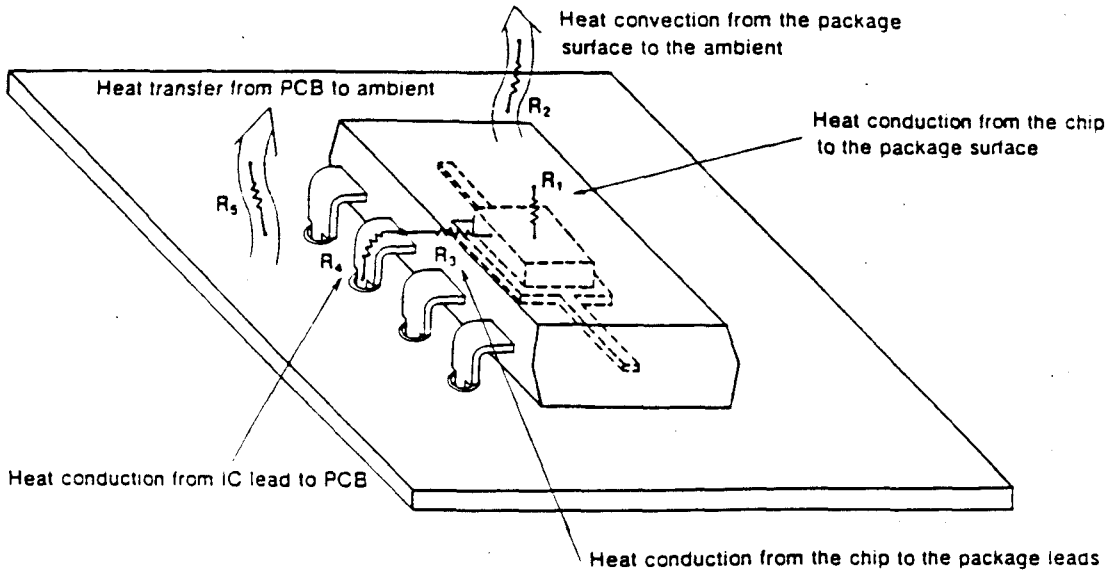

Figure 3.1 Heat flow mechanism from the package to the IC ambience [25].

Heat transfer from the solid surfaces (i.e., the IC package and PCB) to the cooling ambient media (air, water, or other coolants) is governed by a combination of conduction, convection, and radiation mechanisms. Since the temperature differences between the solid surfaces inside system channels are relatively small, the radiation effect is typically less than 10% of the convection effect. Hence, the radiation effect will be neglected in numerical computations. A major objective in a conduction analysis is to determine the temperature field in a medium resulting from conditions imposed upon its boundaries. Throughout the analysis, the temperature distributions within the medium, which represent how temperatures vary with position in the medium, can be obtained.

3.1 Governing Equations and Principal Assumptions

In general, heat transfer can be characterized by a three-dimensional heat-transfer conduction equation. Thermal conduction is governed by

$$\frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(k_z \frac{\partial T}{\partial z}\right) + G = \rho C_p \left(\frac{\partial T}{\partial t}\right) \tag{3-1}$$

where G is heat generation per unit volume. If thermal conductivity is constant in global x, y and z directions (isotropic), the heat equation can be simplified to

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \frac{G}{k} = \frac{1}{\alpha} \frac{\partial T}{\partial t} \tag{3-2}$$

where $\alpha = k/\rho C_p$ is defined as the thermal diffusivity.

Additional simplifications of the general form of the heat equation are often possible. When considering the steady-state condition, there can be no change in the amount of energy storage. The heat equation hence reduces to

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \frac{G}{k} = 0 \tag{3-3}$$

Moreover, if the heat transfer model is specified as two-dimensional (e.g., in only the x and y directions), equation (3-3) reduces to

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{G}{k} = 0 \tag{3-4}$$

In Cartesian coordinates, the general form of the heat equation provides the basic tool for heat conduction analysis, based upon assumptions of a steady-state and a two-dimensional model. From its solution, the temperature distribution T(x,y) within the package can be obtained. The apparent complexity of this expression should not obscure the fact that it describes an important physical condition; that is, the conservation of energy.

The boundary conditions for solving this heat equation have been specified as convection heat transfer. The convection heat flux is expressed as

$$q = h\,(T_s - T_\infty) \tag{3-5}$$

If the heat is transferred from the surface, ($T_s > T_\infty$), the convection heat flux is assumed to be positive; if the heat is transferred to the surface, ($T_\infty > T_s$), the convection heat flux is assumed to be negative. For solution of the numerical computation, the heat transfer coefficients (h) are presumed to be known, with typical values as listed in Table 3.1, and the ambient temperature is assumed to be 25 °C.

Table 3.1 Range of heat transfer coefficients for various cooling techniques.

Fluid	Mode	Range of heat transfer coefficient unit: Watt/m^2 °C	Typical value of heat transfer coefficient unit: Watt/m^2 °C
Air	Free convection	3 to 12	5
Air	Forced convection	10 to 100	50
FC* liquid	Free convection	100 to 300	200
FC* liquid	Forced convection	200 to 2000	1000
FC* liquid	Boiling	2000 to 6000	4500
Water	Forced convection	3000 to 7000	4500

* Fluorocarbon

3.2 Thermal Resistance

In a systems environment, the junction temperatures of a semiconductor device are dependent upon the thermal resistance between the die and the system thermal sink (typically, ambient air), as well as upon the device power dissipation. The junction-to-ambient thermal resistance (θ_{ja}), junction-to-case thermal resistance

(θ_{jc}), and case-to-ambient thermal resistance (θ_{ca}) are used as measures of IC packaging thermal performance and are thus recognized as important tools for package characterization and specific package selection. They are used to design thermally efficient systems and to determine suitable thermal management at the component and system levels. Since package thermal resistance, for either θ_{ja}, θ_{jc} and/or θ_{ca}, is not a constant entity, there are several packaging and environmental parameters as well as mounting configurations that will impact package thermal resistance values; those factors are investigated in the present study.

The evaluation of θ_{ja}, θ_{jc} and θ_{ca} in essence involve the determination of temperature differences for given input powers. The basic equations used for these calculations are given as:

$$\theta_{ja} = \frac{T_j - T_a}{P} \tag{3-6}$$

$$\theta_{jc} = \frac{T_j - T_c}{P} \tag{3-7}$$

$$\theta_{ca} = \frac{T_c - T_a}{P} \tag{3-8}$$

$$\theta_{ja} = \theta_{jc} + \theta_{ca} \tag{3-9}$$

where T_j is the junction temperature, defined as the highest temperature on the die; T_c is the case temperature, defined as the surface temperature of the package; T_a is the assumed average ambient temperature; and P is the power dissipation at the die.

There are specified definitions and characterizations for each thermal resistance. For example, θ_{jc} is a measure of package internal thermal resistance from the die to the package exterior. This value is strongly dependent upon package geometry and the thermal conductivity of the packaging materials. It can vary significantly with package attachments, the thermal characteristics of the second-level packaging technique, and the external convective heat transfer coefficients. On the other hand, θ_{ja} values include not only package internal thermal resistance, but also convective and conductive thermal resistances from the package exterior to its ambience. Material conductivities and package geometry, as well as such ambient conditions as flow rates and coolant physical properties, can also impact the values of θ_{ja}. Thermal resistance from the package case to the ambience, θ_{ca}, is dependent upon package geometry, air flow characteristics, the geometrical effects of the surrounding components, and the temperature at the package surface. To meet the requirements of system applications, the thermal resistances, θ_{jc}, θ_{ca} and θ_{ja}, may have to be maintained within specified values by adjusting the factors that impact the values of thermal resistance. A number of alternative standard techniques for measurement of package thermal resistance exist, but these experimental techniques are not examined in the present investigation.

CHAPTER 4
NUMERICAL PROCEDURES

A thermal analysis interfacing software package (COSMOS/M,Unix Version 1.65) was used to generate the thermal network models. This software consists of several modules which interface with a AutoCAD (computer-aided design software) system and a thermal network analyzer to facilitate model generation and thermal network calculations. The geometrical configurations of the package components were specified using AutoCAD, and then imported to the COSMOS/M software package. After the geometrical configurations were meshed, the material properties of the components were input and the thermal boundary conditions were described for each configuration. COSMOS/M was then used to automatically perform thermal network calculations as well as to generate a complete input file for the thermal network analyzer, which in turn could be used to perform thermal stress or other forms of thermal analysis. Once the calculations were completed, the results are presented for convenient evaluation. The postprocessing capabilities of the COSMOS/M finite element code include graphic and text displays of the results. Package thermal network models can be stored in a database to allow for repeated use in the case of either boundary condition or material property changes. Verification calculations were conducted using Ozisik's model, and the results obtained were in good agreement with the model analytical solutions.

4.1 Fundamentals of Finite Element Analysis

The finite element method (FEM) presents important features each with a dual nature. First, a geometrically complex problem domain is represented as a collection of geometrically simple subdomains, or finite elements, which may be triangles or quadrilaterals in two dimensions or tetrahedrons or pentahedrons in three dimensions. Different element types can be mixed within the same solution as long as they reflect the same dimensions and the whole of the domain is covered without any gaps. Second, approximation functions are derived over each finite element, based upon the concept that any continuous function may be represented by a linear combination of algebraic polynomials. The approximation functions are derived using concepts from interpolation theory, and are therefore referred to as the interpolation functions. In close analogy to piecewise FEM application, the basic steps necessary to solve the heat conduction equation are presented using the Galerkin method.

Note that the two-dimensional region is shown as a relatively thin plate of variable thickness. As in the simple model shown in Figure 4.1, a volumetric heat source is also included. Both lateral and boundary heat transfer effects, including convection and insulation, are included in the model.

The governing differential equation for temperature, T, is easily derived if an energy balance is completed for an elemental volume, tdxdy, where t is the thickness of the plate. Under the assumption of steady-state, two-dimensional, and isotropic material properties, it may be demonstrated that the governing equation

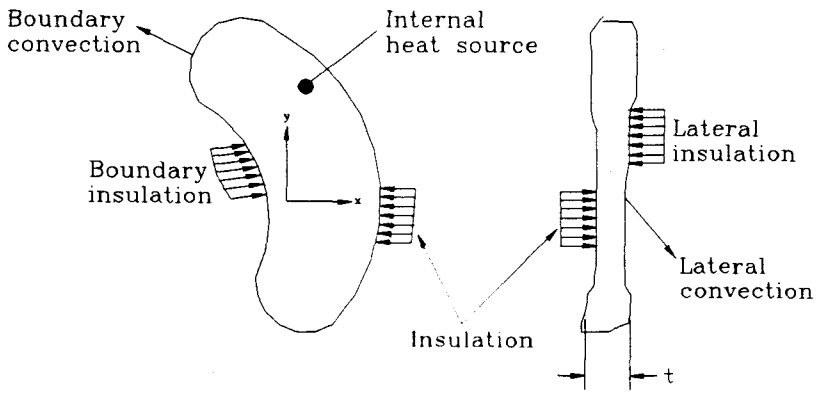

Figure 4.1 Schematic of a general two-dimensional heat conduction problem.

(3-4) can be written as

$$\frac{\partial}{\partial x}\left(kt\frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(kt\frac{\partial T}{\partial y}\right) + Qt = 0 \qquad (4\text{-}1)$$

where Q is heat generation per unit time and volume.

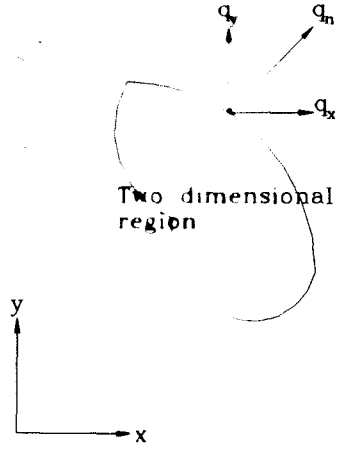

Figure 4.2 Boundary of two-dimensional region showing net (normal) heat flux q_n and components in the x and y directions.

A heat flux is generally a vector and represents the heat-transfer rate per unit area. In isotropic materials, the heat flux is always normal to surfaces. For the present study, the net (normal) heat flux vector is denoted as $\mathbf{q}_n$, the magnitude of which is simply q_n, as illustrated in Figure 4.2.

In terms of the outward normal unit vector $\mathbf{n}$, $\mathbf{q}_n$ and q_n can be written

$$\boldsymbol{q} = q_n \boldsymbol{n} \tag{4-2}$$

$$q_n = -k\frac{\partial T}{\partial x}n_x - k\frac{\partial T}{\partial y}n_y \tag{4-3}$$

Since it clearly emphasizes that q_n represents the net (normal) heat flux from conduction leaving a surface, equation (4-3) is of great importance. The expressions for the finite element characteristics may be derived by specifying the three-node triangular element. First, the shape-function matrix N is defined by

$$\mathbf{N} = [\, N_i, N_j, N_k] \tag{4-4}$$

where it can be shown for each N_i, N_j, and N_k that

$$\begin{aligned} N_i(x,y) &= m_{11} + m_{21}x + m_{31}y \\ N_j(x,y) &= m_{12} + m_{22}x + m_{32}y \\ N_k(x,y) &= m_{13} + m_{23}x + m_{33}y \end{aligned} \tag{4-5}$$

and in turn

$$
\begin{aligned}
m_{11} &= (x_j y_k - x_k y_j)/2A \\
m_{12} &= (x_k y_i - x_i y_k)/2A \\
m_{13} &= (x_i y_j - x_j y_i)/2A \\
m_{21} &= (y_j - y_k)/2A \\
m_{22} &= (y_k - y_i)/2A \\
m_{23} &= (y_i - y_j)/2A \\
m_{31} &= (x_k - x_j)/2A \\
m_{32} &= (x_i - x_k)/2A \\
m_{33} &= (x_j - x_i)/2A
\end{aligned}
\tag{4-6}
$$

and

$$
A = \frac{1}{2} \times \det \begin{pmatrix} 1 & x_i & y_i \\ 1 & x_j & y_j \\ 1 & x_k & y_k \end{pmatrix} = \text{area of triangle } ijk \tag{4-7}
$$

It should be noted that the m_{ij} are strictly a function of the nodal coordinates. Since the area A of the triangular element is never zero, the inverse indicated in equation (4-7) will always exist.

A typical element e has nodes i, j, and k, specified in a counterclockwise order with, respectively, temperatures T_i, T_j, and T_k. On an element basis, the Galerkin method requires

$$
\int_{A^e} \mathbf{N}^T \left[\frac{\partial}{\partial x} \left(k t \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left(k t \frac{\partial T}{\partial y} \right) + Q t \right] dx dy = 0 \tag{4-8}
$$

It is emphasized that this integral applies to a typical element e and the integrations are to be performed over the area A^e of the element. Note that each term in equation (4-8) has units of energy per unit time. If the Green-Gauss theorem is

applied to the two terms containing second-order derivatives, we get

$$\begin{aligned} &\int_{C_e} \mathbf{N}^T k\, t \frac{\partial T}{\partial x} n_x dC - \int_{A_e} \frac{\partial \mathbf{N}^T}{\partial x} k\, t \frac{\partial T}{\partial x} dx dy \\ &+ \int_{C_e} \mathbf{N}^T k\, t \frac{\partial T}{\partial y} n_y dC - \int_{A_e} \frac{\partial \mathbf{N}^T}{\partial x} k\, t \frac{\partial T}{\partial x} dx dy \\ &+ \int_{A_e} \mathbf{N}^T Q\, t\, dx dy = 0 \end{aligned} \tag{4-9}$$

However, the two integrals around the element boundary may be combined with the help of equation (4-3) to give

$$\int_{C_e} \mathbf{N}^T \left(k \frac{\partial T}{\partial x} n_x + k \frac{\partial T}{\partial y} n_y \right) t\, dC = \int_{C_e} \mathbf{N}^T (-q_n)\, t\, dC \tag{4-10}$$

At this point it is convenient to consider the nongeometric boundary conditions. As noted above, convection is to be included and perfect insulation is a special case of zero heat flux. We can perform an energy balance (i.e., on an area basis) for the global boundary shown in Figure 4.3, such that it may be written,

$$q_n = q_{cvB} = h_B (T - T_{aB}) \tag{4-11}$$

where h_B is the convective heat transfer coefficient at the element boundary and T_{aB} is the ambient fluid temperature. Strictly speaking, the T in equation (4-11) should be the temperature at the element boundary, but as will be subsequently demonstrated, the shape-function matrix in equation (4-10) will automatically take care of this.

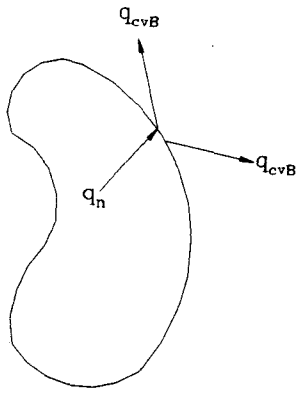

Figure 4.3 Typical convection boundary in a two-dimensional heat conduction problem showing the heat fluxes considered in the finite element.

Hence, equation (4-10) can be written as

$$\int_{C^e} \mathbf{N}^T (-q_n)\, t\, dC = \int_{C^e} \mathbf{N}^T h_B\, t\, T_{aB}\, dC - \int_{C^e} \mathbf{N}^T h_B\, t\, T\, dC \qquad (4\text{-}12)$$

The parameter function for the temperature T may be written in terms of the nodal temperature as

$$\mathbf{T} = \mathbf{N}\,\mathbf{a}^e \qquad (4\text{-}13)$$

where **N** is the shape-function matrix and $\mathbf{a}^e$ is the vector of the nodal temperatures for element e. It follows that equation (4-9) may be written as

$$\mathbf{K}^e\,\mathbf{a}^e = \mathbf{f}^e \qquad (4\text{-}14)$$

where

$$\mathbf{K}^e = \mathbf{K}^e_{xx} + \mathbf{K}^e_{yy} + \mathbf{K}^e_{cvB} \qquad (4\text{-}15)$$

and

$$f^e = f^e_Q + f^e_{cvB} \tag{4-16}$$

The element stiffness matrices are in turn given by

$$\mathbf{K}^e_{xx} = \int_{A^e} \frac{\partial \mathbf{N}^T}{\partial x} k\, t \frac{\partial \mathbf{N}}{\partial x}\, dx\, dy \tag{4-17}$$

$$\mathbf{K}^e_{yy} = \int_{A^e} \frac{\partial \mathbf{N}^T}{\partial y} k\, t \frac{\partial \mathbf{N}}{\partial y}\, dx\, dy \tag{4-18}$$

$$\mathbf{K}^e_{cvB} = \int_{C^e} \mathbf{N}^T h_B\, t\, \mathbf{N}\, dC \tag{4-19}$$

and the element nodal force vectors by

$$f^e_Q = \int_{A^e} \mathbf{N}^T Q\, t\, dx\, dy \tag{4-20}$$

$$f^e_{cvB} = \int_{C^e} \mathbf{N}^T h_B\, t\, T_{aB}\, dC \tag{4-21}$$

For the three-node triangular element, the stiffness matrices and nodal force vectors are each of sizes 3 x 3 and 3 x 1, respectively. It may be seen, nearly by inspection, that each of these stiffness matrices is symmetric. Note the use of the subscript B for those terms that arise from the boundary conditions. In these cases, the integrations are to be performed around the boundaries of each element. However, if all legs of the element are internal (i.e., within the body) and not on the global boundary, then the corresponding stiffness matrices and the nodal force vectors are simply taken to be null matrices and vectors.

Consequently, an FEA solution then consists of assembling the K_e and $\mathbf{f}_e$

values in a large system of algebraic equations, known as the system equations, then solving this system of equations for the $\mathbf{a}^e$ coefficients, using a direct iteration method. The nodal temperatures can be solved by substituting $\mathbf{a}^e$ into equation (4-13) after the shape functions are solved. Throughout these calculations, the temperature for each node of each element can be obtained. Typically, a two-dimensional model of an IC package can generate approximately 3,000 system equations composed of 9,000,000 terms. To achieve greater problem resolution, the use of smaller elements is preferred, but this approach can increase computation time and costs. Accordingly, it is necessary to carefully construct the mesh using large elements in regions of little interest and low temperature gradients, while providing sufficient refinement in areas prone to high temperature gradients, such as the vicinity of the die and pad.

The most obvious benefit from using the FEM is that it can provide solutions to a number of complicated problems that would otherwise prove intractable using other techniques. All finite element applications use basically the same types of mathematical techniques. Hence, once a finite element computer program is developed it can be used to solve not just one specific problem, but an entire class of problems that differ substantially in geometry, boundary conditions, and other properties. This advantage greatly assists the development of commercial finite element analysis packages, which in turn provide a diverse set of geometric modeling capabilities, particularly when combined with flexible meshing options to create complex models with relative ease. The COSMOS/M finite

element software package was employed for the present numerical study. The procedure for solving heat conduction problems is discussed in the following section.

4.2 Modeling Procedure

The success of the finite element method for the modeling and the analysis of engineering systems is based largely upon the basic procedures used. Numerical simulation using COSMOS/M FEM software requires complete information on the domain under consideration. The basic procedure for a COSMOS/M finite element analysis, as schematically shown in Figure 4.4, consist of the following steps:

- Create the problem geometry (as imported from the CAD system);
- Mesh the defined geometry with appropriate type of elements;
- Apply boundary conditions (constraints) to the FEM model;
- Define the loads for the model;
- Submit the completed finite element model for analysis; and
- Interpret and analyze the results.

All of the operations performed prior to submitting the generated model to analysis are referred to as preprocessing. The following discussion is organized principally to illustrate the preprocessing concepts and the supplement of boundary conditions used for the analysis.

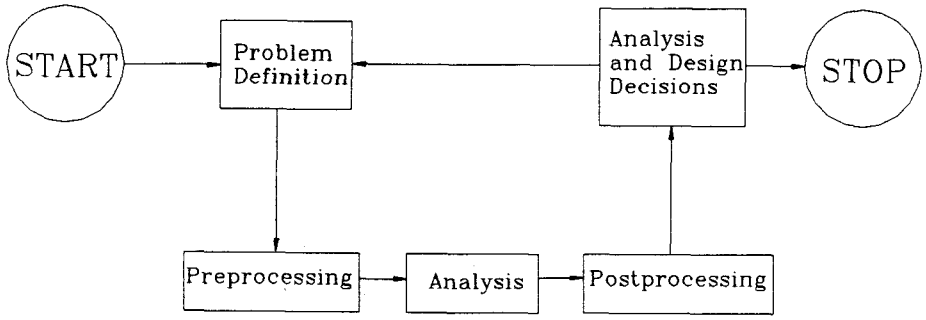

Figure 4.4 COSMOS/M general finite element analysis steps.

Since, as shown in Figures 1.4 and 1.5, the problem package models are symmetric, only one-half of the package with a PCB was analyzed. Heat dissipation (0.2, 0.5, 0.8, 1.0 and 1.5 Watt/die) was loaded and assumed to be uniformly generated in the 1 cm thick active volume associated with the entire surface of the die. The values of the volumetric heat generation input were 2.849, 7.1225, 11.396, 14.245 and 21.3675 Watt/cm^3, respectively, correlated to each of the die heat dissipations.

The shape of elements was triangular and a total of 1,395 elements was used for all cases to model this half of the array for thermal analysis. Figure 4.5 and 4.6 illustrate the meshed models with boundary conditions and heat generation inputs. The connection of finite elements meshed between any two component bonding interfaces should match and be compatible. The boundary conditions consisted of convection around the package and the PCB and, based upon the assumption that the PCB lengths were infinite compared to the package dimensions,

insulation on the left side of the PCBs. Adiabatic boundary conditions were imposed at the planes of symmetry locations. Moreover, between the molding compound and the PCB existed a 0.09 cm air gap assumed to be stagnant with conductivity k = 0.0263 Watt/m °C. Throughout these preprocessing inputs, results were presented with respect to the temperature at each node of each element. A typical input file for the COSMOS/M FEM software package is included as Appendix A.

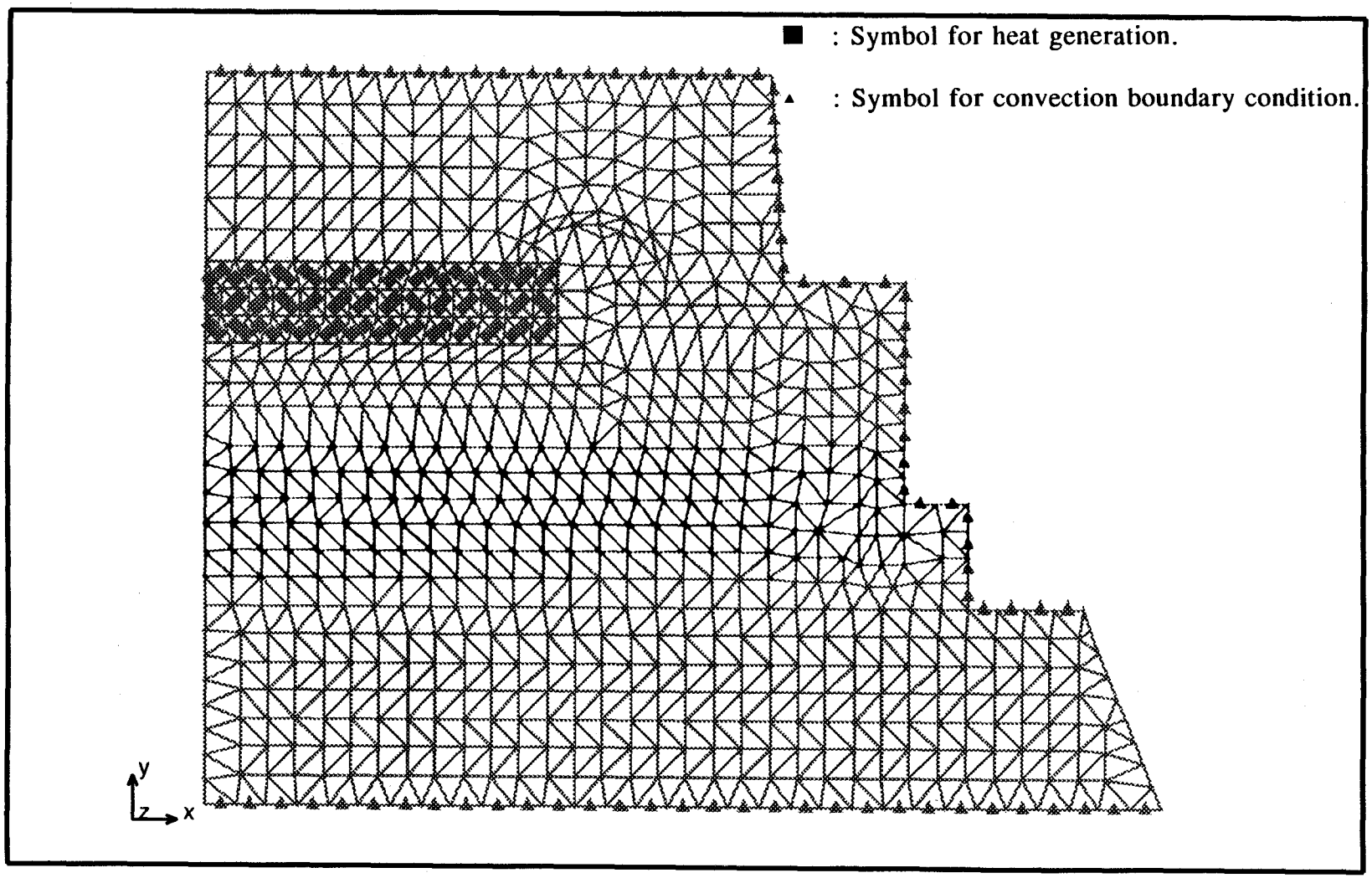

Figure 4.5 Heat generation and convection boundary condition input in the COSMOS/M finite-element analysis for a surface mounted package.

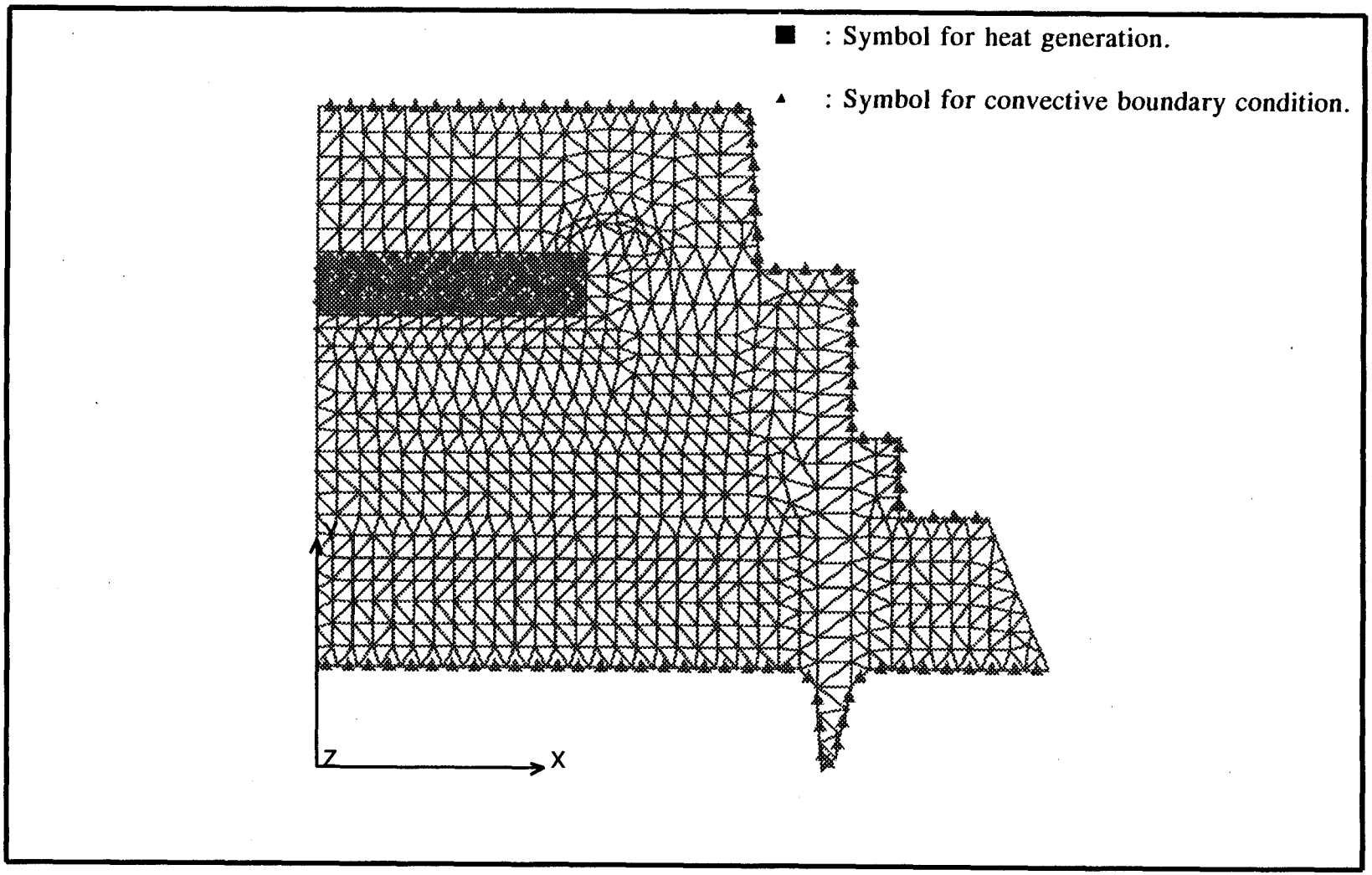

Figure 4.6 Heat generation and convection boundary condition input in the COSMOS/M finite-element analysis for a through-hole mounted package.

CHAPTER 5
RESULTS AND DISCUSSION

Temperature profiles were derived from the two-dimensional finite element analysis and identified as complex heat flow patterns. For each package, the maximum operating temperature is indicated in the temperature distribution plots provided in Figures 5.1 - 5.8. From these plots, whether or not the operating temperatures within the IC package for each constituent component and PCB were in excess of extended lifetime limits was determined.

A standardized method of characterizing thermal performance was employed, based upon junction-to-ambient thermal resistance (θ_{ja}) as computed from the results of thermal analysis. The factors which impact thermal resistance were also considered. Since small values for θ_{ja} are preferred for the package design process, package thermal performance improvement can be achieved through analysis of these impacting factors. Specific numerical correlation equations between package maximum operating temperature and power dissipation (Watt/die), as well as for the convective heat transfer coefficient (Watt/m^2 °C) were proposed from the following functional form:

$$T_{max} = f(P , h)$$

Though the present investigation was limited to two specific packages, it is believed that the results obtained may serve as a valuable database for the future verification of analytical models that may be more widely applied.

5.1 Temperature Distribution within Packages

The contour plots of steady-state temperature distributions within packages are demonstrated in Figures 5.1 - 5.6 for different die materials, including silicon (Si), germanium (Ge), and gallium arsenide (GaAs). Other package constituent components are specified as follows:

- gold wire (k = 300 Watt/m °C),
- adhesive of silver-filled epoxy (k = 2.6 Watt/m °C),
- alloy 42 lead and die attach pad (k = 15.7 Watt/m °C),
- Pb-In solder joint (k = 22 Watt/m °C),
- e-glass PCB (k = 0.89 Watt/m °C), and
- epoxy molding compound (k = 0.67 Watt/m °C).

The uniform power dissipated by the die was set for 0.5 Watt/die. The cooling method was air-forced convection with a convective heat transfer coefficient of $h = 50$ Watt/m^2 °C. The ambient temperature was specified as 25 °C for all cases, as shown in Figures 5.1 - 5.6.

The die or so-called chip is the heart of the entire package. From Figures 5.1 - 5.6, since heat is generated uniformly at the die, it may be observed that the maximum temperature region is always around the chip. From the analytical results, it can be concluded that the higher thermal conductivity of the die could have served to reduce maximum operating temperature within the packages. From comparisons based upon thermal analysis, since the through-hole mounted packages have a greater heat transfer area at the lead than the surface mounted packages, the

through-hole mounted packages reflected lower maximum operating temperatures than the surface mounted packages with identical constituent components and the same boundary conditions. However, based upon design considerations for the entire system design as well as the trend toward increased use of high-density packaging in the electronics industry, surface mounted packages have been more extensively used. Surface mounted packages present a number of advantages. Typically, they can be mounted on both sides of the PCBs, resulting in higher density packaging requiring less board area, a factor which lowers the cost of packaging for the total system.

When the air gap between the molding compound and the PCB was not assumed to be the stagnant, boundary conditions could possibly be applied. Figures 5.7 - 5.8 show temperature distributions for these situations using silicon material for the die. As expected, due to increased package heat transfer area, maximum operating temperatures within packages were reduced significantly. To provide more realistic comparisons, because of the small sizes of the air gap, the air within the gap was specified to act as a conductive medium for all air-cooling strategies, with the exception of those cases for which liquid cooling was used.

The results of the calculated temperature distributions within packages, in conjunction with the predicted maximum operating temperature for each component, can be used to determine whether or not acceptable levels of reliability have been achieved with the direct air, forced convective or liquid cooling strategies. Should an unacceptable level of reliability be determined for any of the

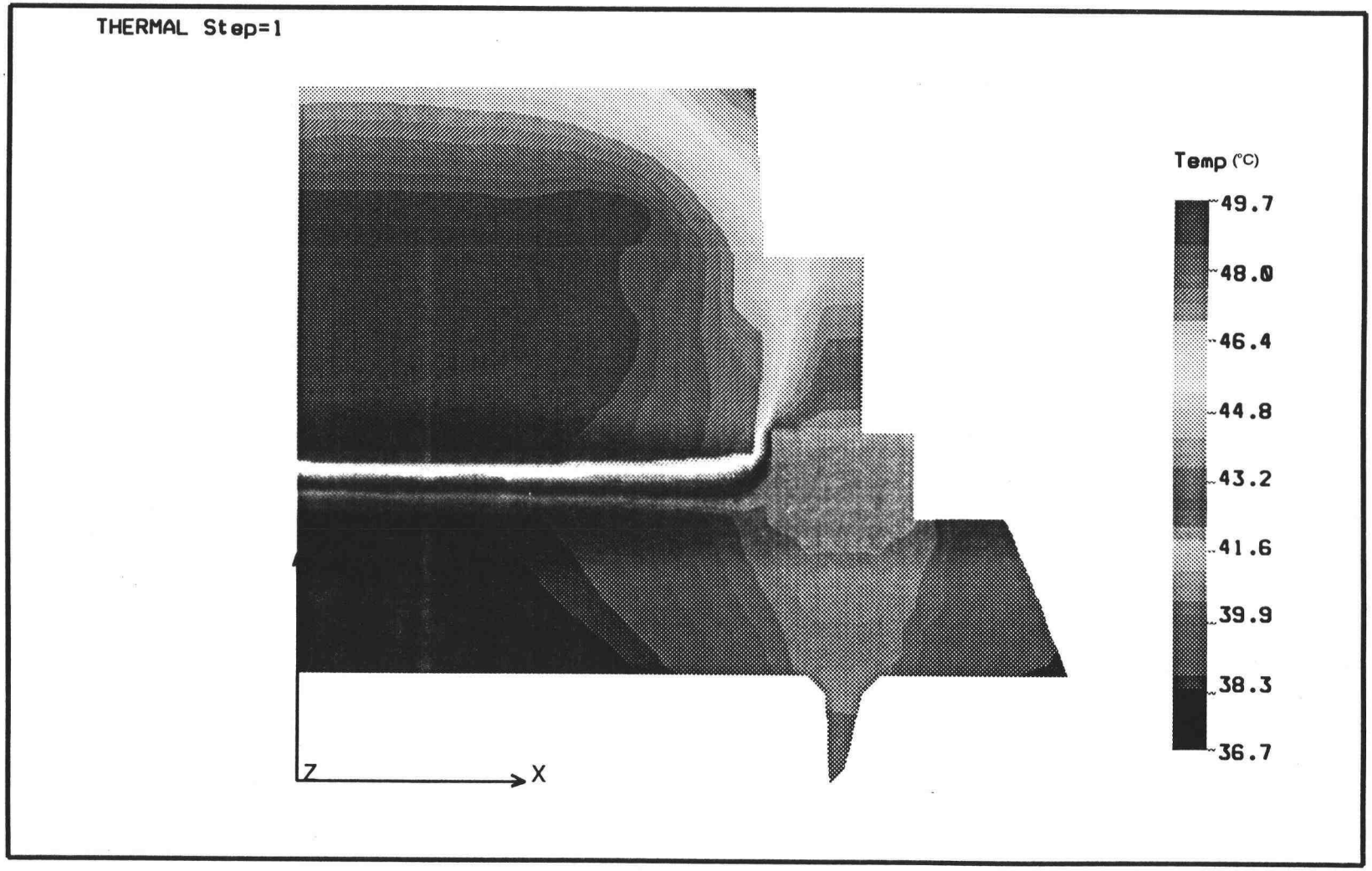

Figure 5.1 Temperature distribution along the board and the package with Si die material for through-hole mounted package (P=0.5 Watt/die, h=50 Watt/m^2 °C).

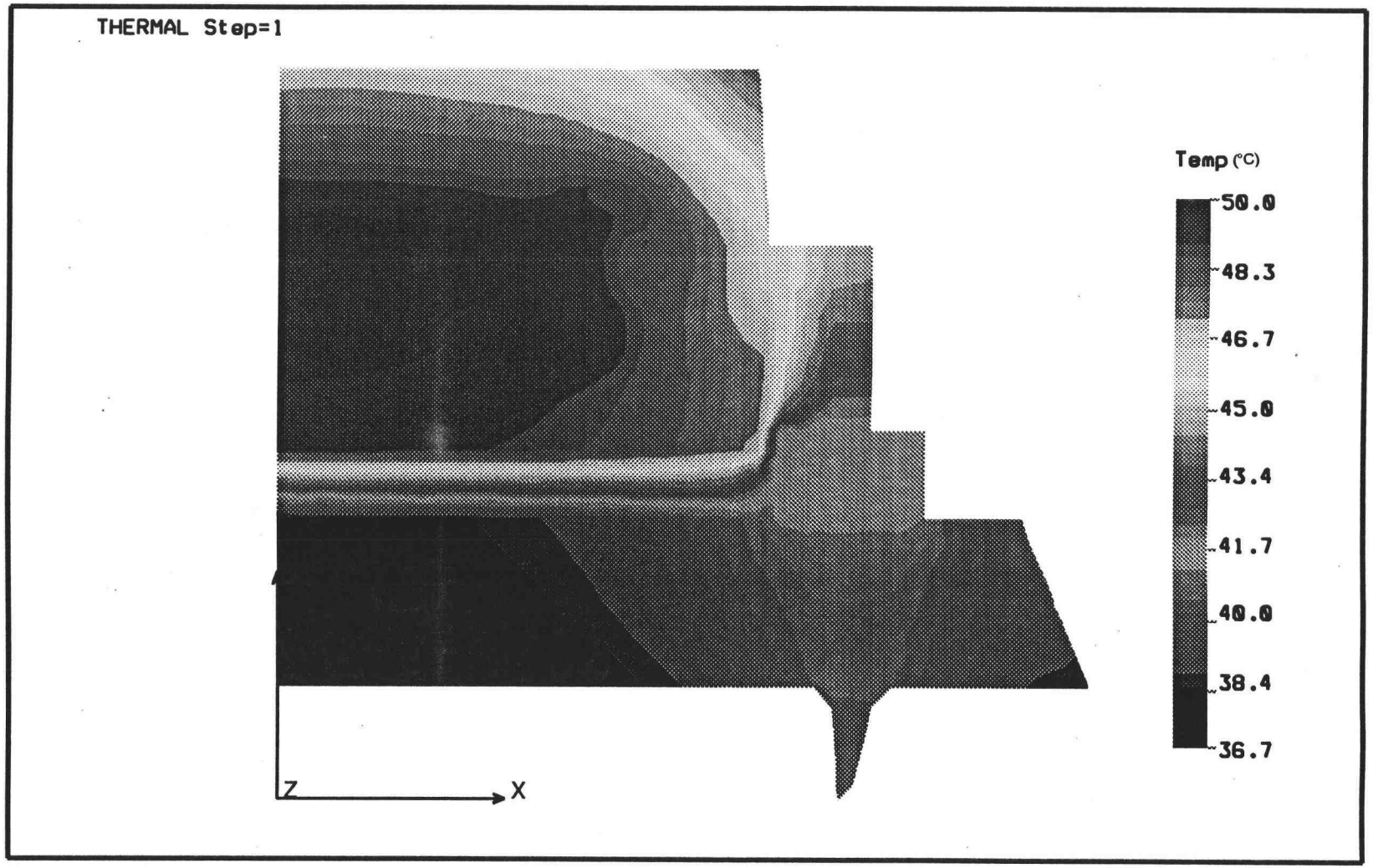

Figure 5.2 Temperature distribution along the board and the package with Ge die material for through-hole mounted package (P=0.5 Watt/die, h=50 Watt/m^2 °C).

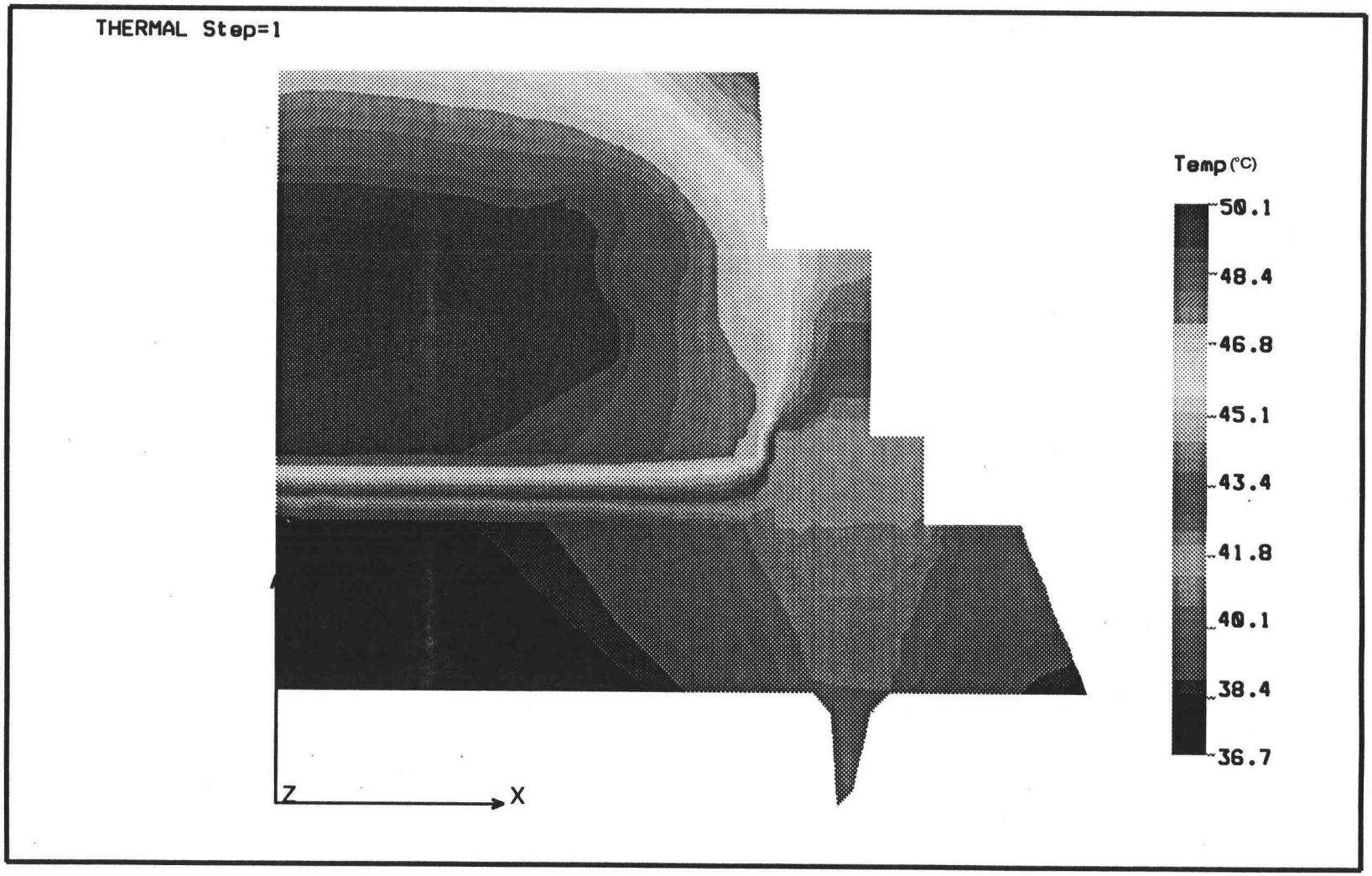

Figure 5.3 Temperature distribution along the board and the package with GaAs die material for through-hole mounted package (P=0.5 Watt/die, h=50 Watt/m^2 °C).

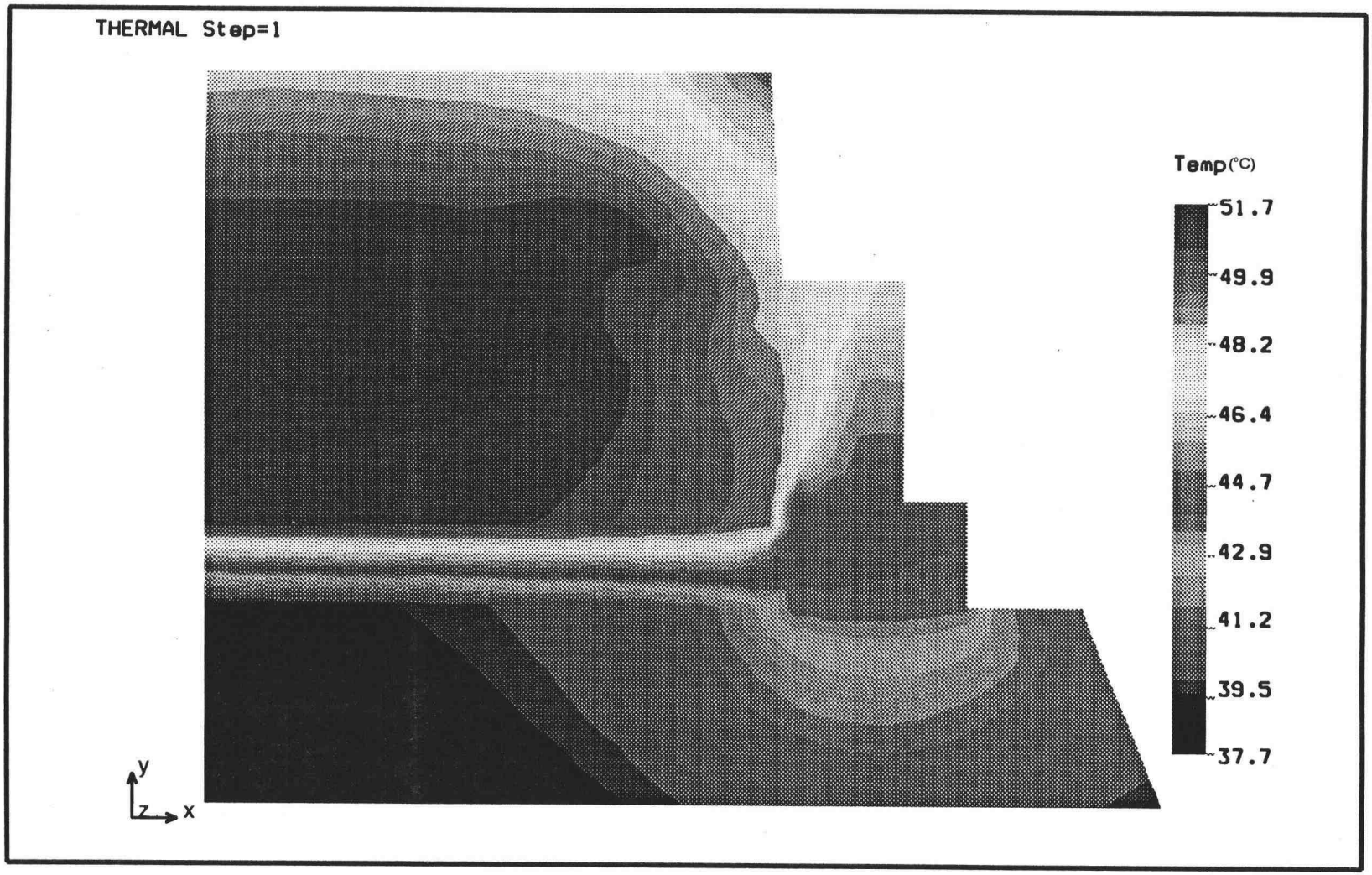

Figure 5.4 Temperature distribution along the board and the package with Si die material for surface mounted package (P=0.5 Watt/die, h=50 Watt/m^2 °C).

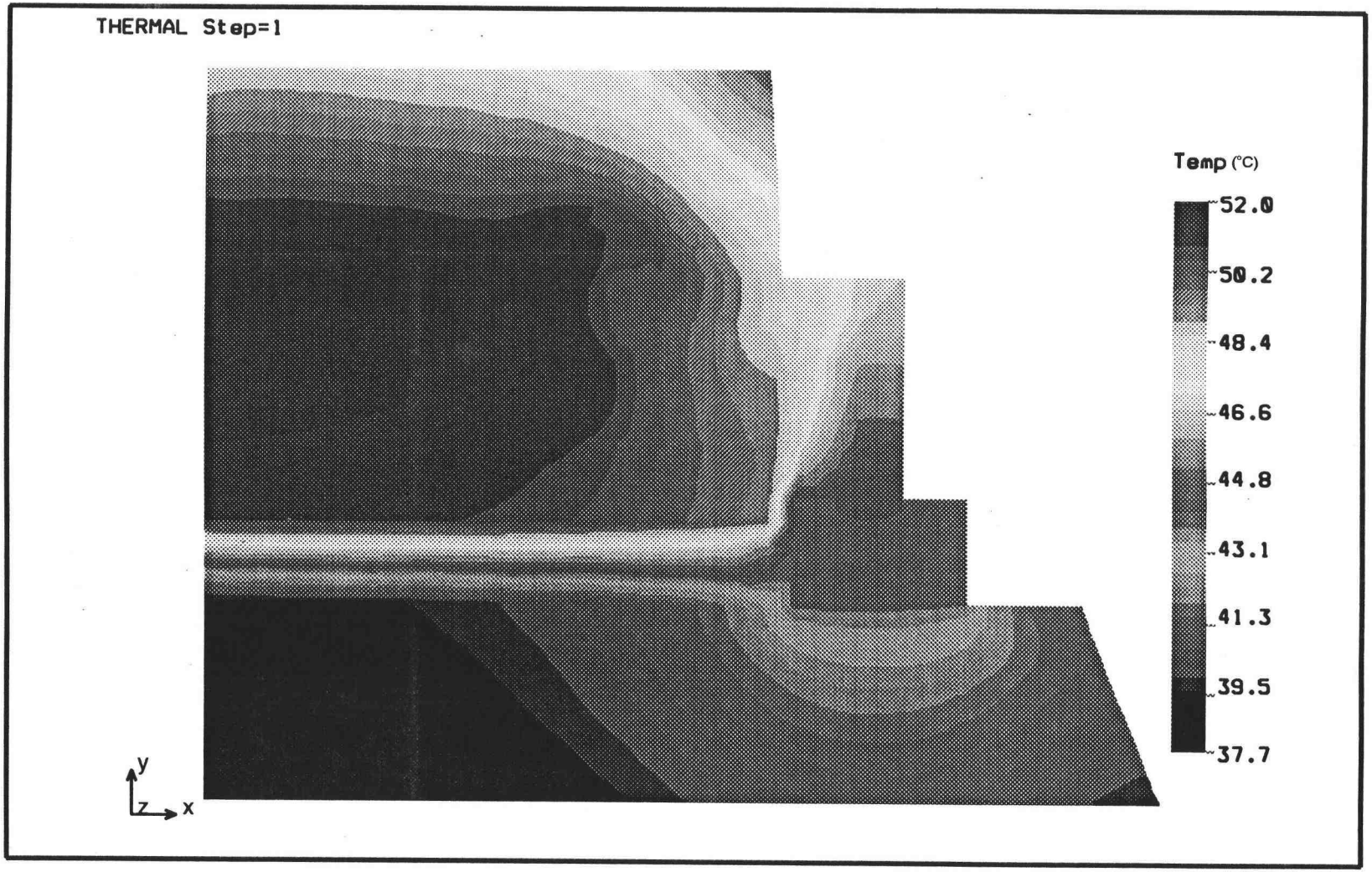

Figure 5.5 Temperature distribution along the board and the package with Ge die material for surface mounted package (P=0.5 Watt/die, h=50 Watt/m^2 °C).

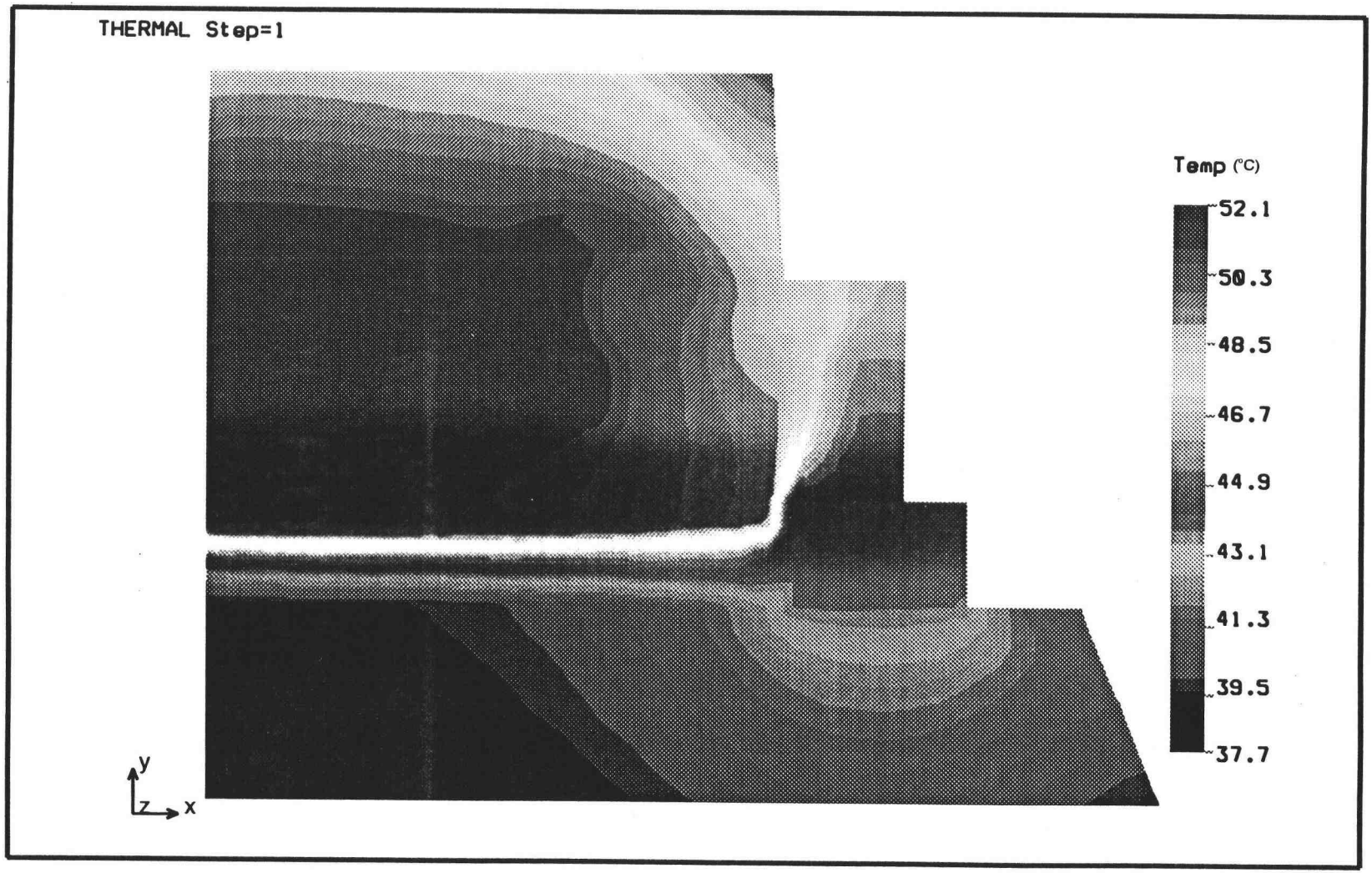

Figure 5.6 Temperature distribution along the board and the package with GaAs die material for surface mounted package (P=0.5 Watt/die, h=50 Watt/m^2 °C).

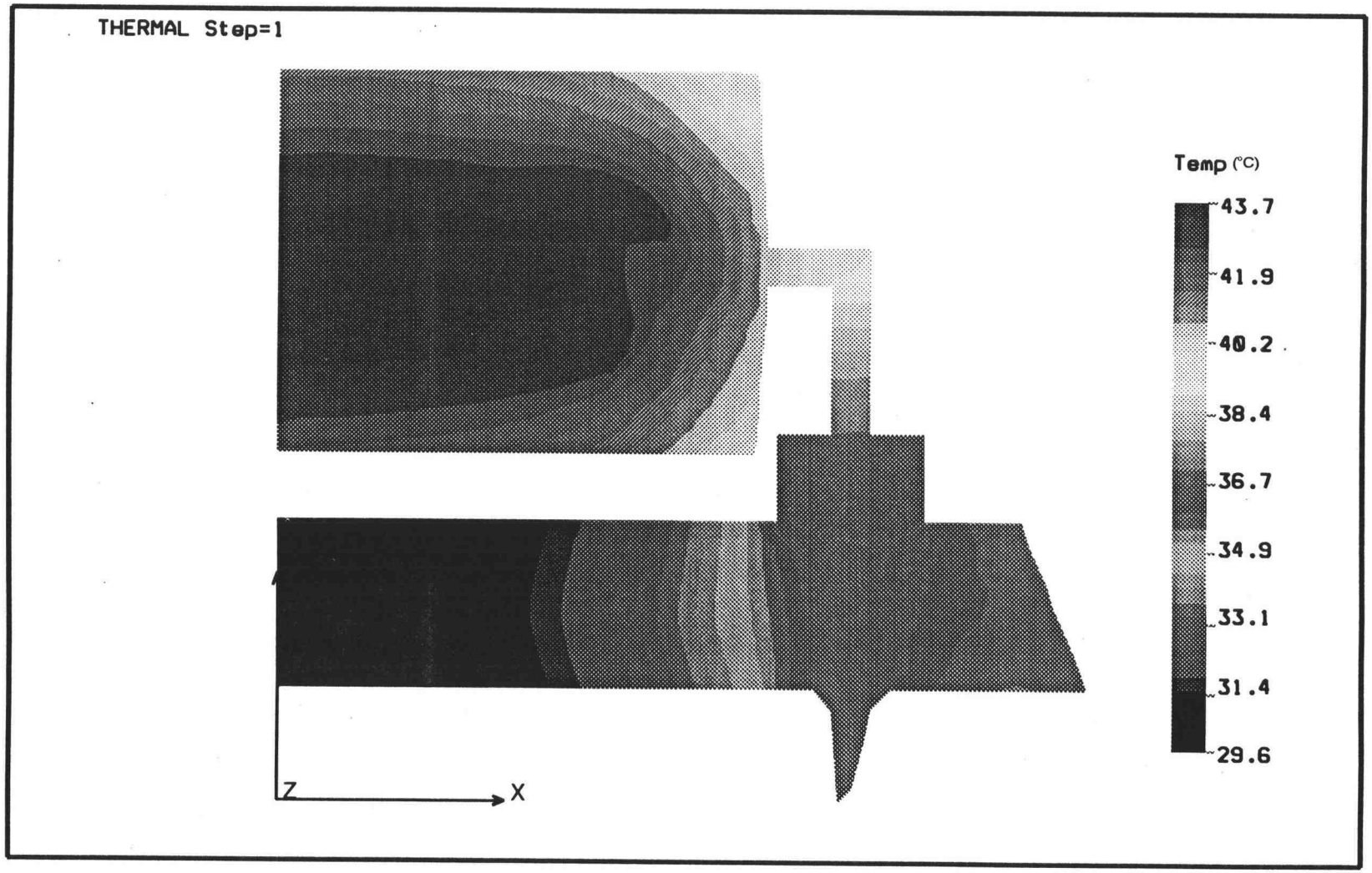

Figure 5.7 Temperature distribution along the board and the package with Si die material for through-hole mounted package (P=0.5 Watt/die, h=50 Watt/m^2 °C), with convective boundary applied around the air gap.

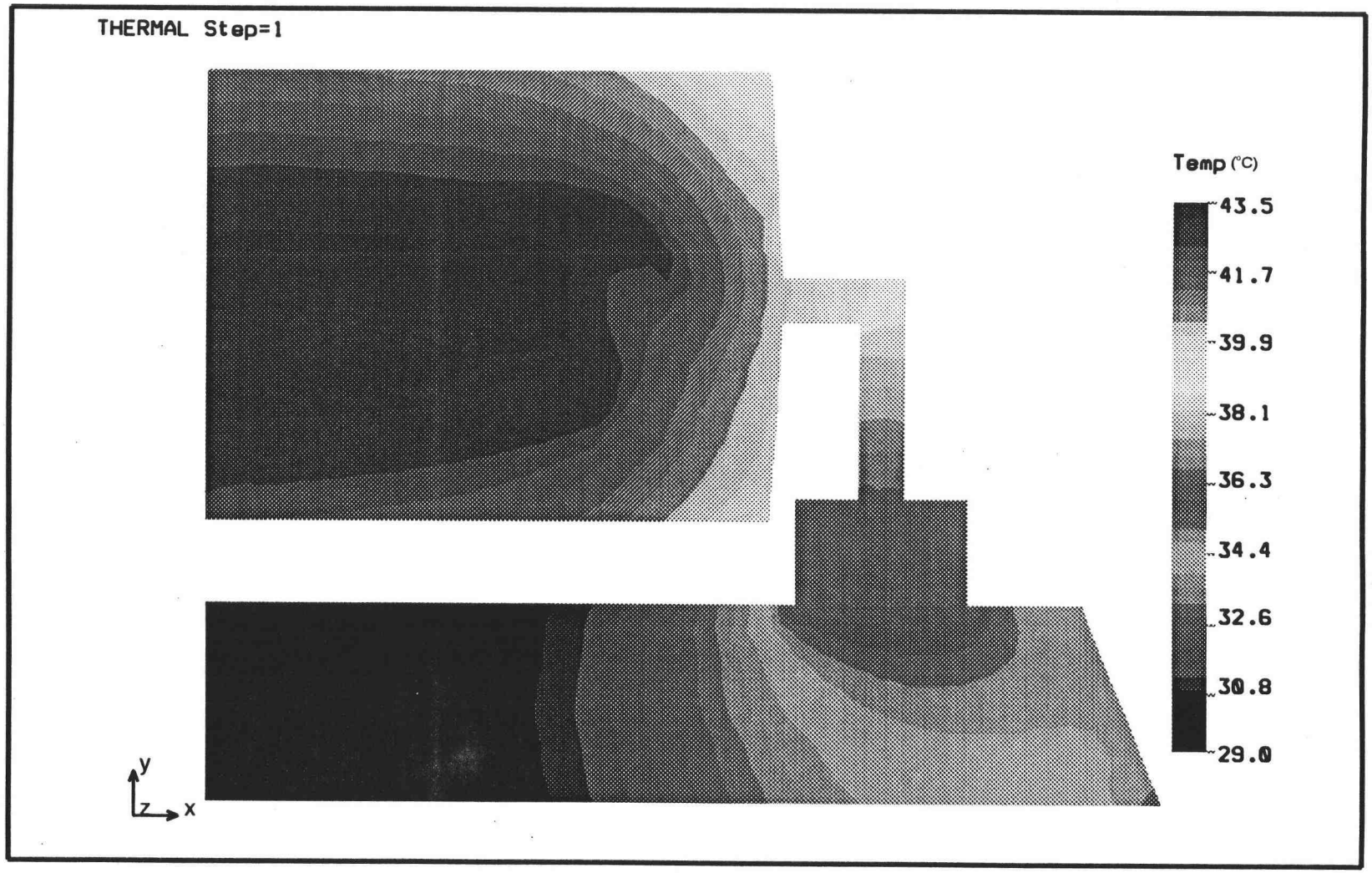

Figure 5.8 Temperature distribution along the board and the package with Si die material for surface mounted package (P=0.5 Watt/die, h=50 Watt/m^2 °C), with convective boundary applied around the air gap.

system components, then such corrective measures as the replacement of the initially specified molding compound materials, change of cooling method, or placement of fins on the top of packages could be initiated.

5.2 Factors Impacting Package Thermal Resistance

Since the predominant mode of heat transfer within packages is based upon conduction, the thermal conductivity of package component materials has the greatest impact upon package thermal performance. Accordingly, the thermal conductivity of the various package components was analyzed to determine different effects upon package junction-to-ambient thermal resistance (θ_{ja}), which provides a standardized judgement of the performance reliability of IC packages. These materials included dies, adhesives, lead and die attach pads, molding compounds and PCBs, and are discussed below. In addition, the effect of power dissipation on θ_{ja} was also addressed.

5.2.1 Die Material

Comparison of the thermal performance of packages containing silicon (Si) dies to similar packages containing gallium arsenide (GaAs) and germanium (Ge) dies is shown in Figure 5.9. Although both GaAs and Ge dies have significantly lower thermal conductivity than silicon, thermal resistance (θ_{ja}) using GaAs and Ge packaging increased by relatively small and uniform amounts for both surface

mounted and through-hole mounted packages. Due to its lower thermal resistance (θ_{ja}), silicon has gained wide acceptance as the die material for IC package. However, GaAs is sometimes used for the high-performance packaging required by some military applications. The major advantages for the use of GaAs die material are: (1) lower power requirements than Si die material, (2) wide temperature operation ranges, (3) higher operating frequencies, and (4) greater radiation withstanding levels. These advantages allow for a wide variety of uses in special applications.

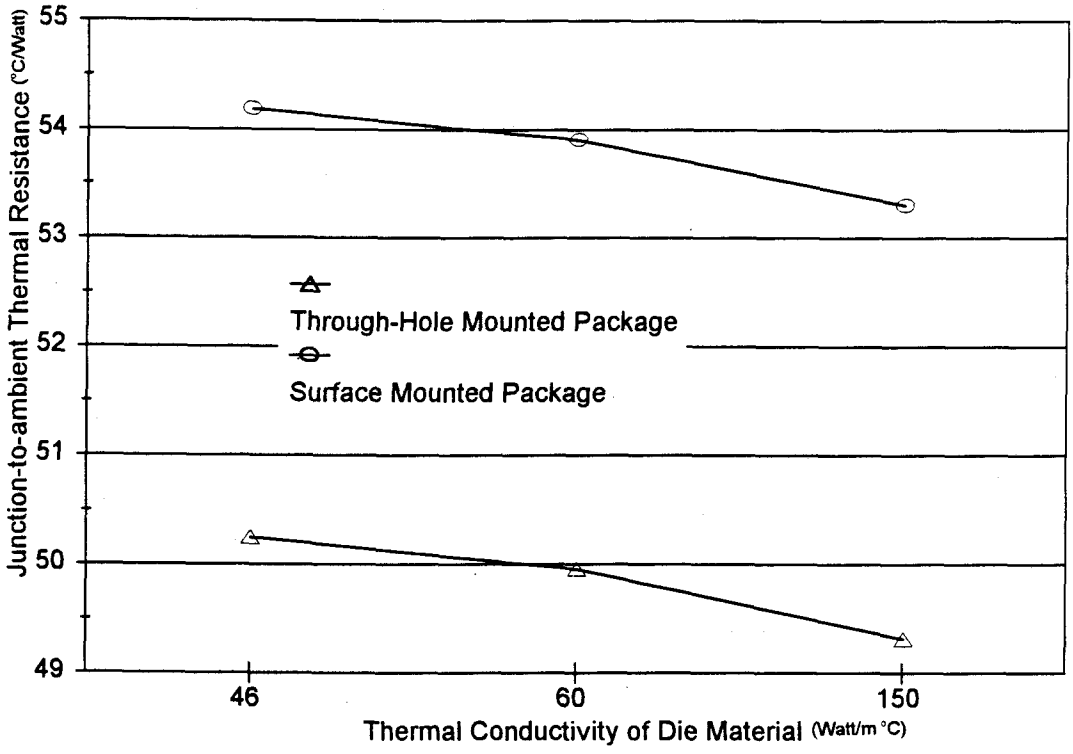

Figure 5.9 Effect of die material on package thermal resistance.

5.2.2 Adhesive Material

One of the functions of adhesive materials is to act as an efficient thermal transfer medium, conducting heat generated by the die to the die attach pad and from the pad to the plastic or ceramic package. From Figure 5.10, thermal resistance (θ_{ja}) is inversely proportional to the thermal conductivity of the adhesive materials. Changes in thermal resistance are also more acute at lower thermal conductivity levels for adhesive materials.

Since the thermal conductivity of the four most widely used epoxy-adhesive bonding agents (i.e., silver-filled, gold-filled and alumina-filled epoxy and epoxy film) is very low, the effect of the adhesive materials upon the thermal resistance of the entire package is less than obvious. However, in the highly competitive electronics industry, any improvements which serve to enhance package thermal performance must be considered. To provide heat conductivity, epoxies which are heavily filled with thermally conductive but electrically insulative materials, such as alumina, can provide this functional requirement as well as the advantages of easy rework and lower processing temperatures.

5.2.3 Lead and Die Attach Pad Material

The major functional requirements of lead and die attach pads are to serve as a support matrix for packages and to serve as electrical and thermal conductors from the die to the board. Thus, their ability to channel heat from the die to the

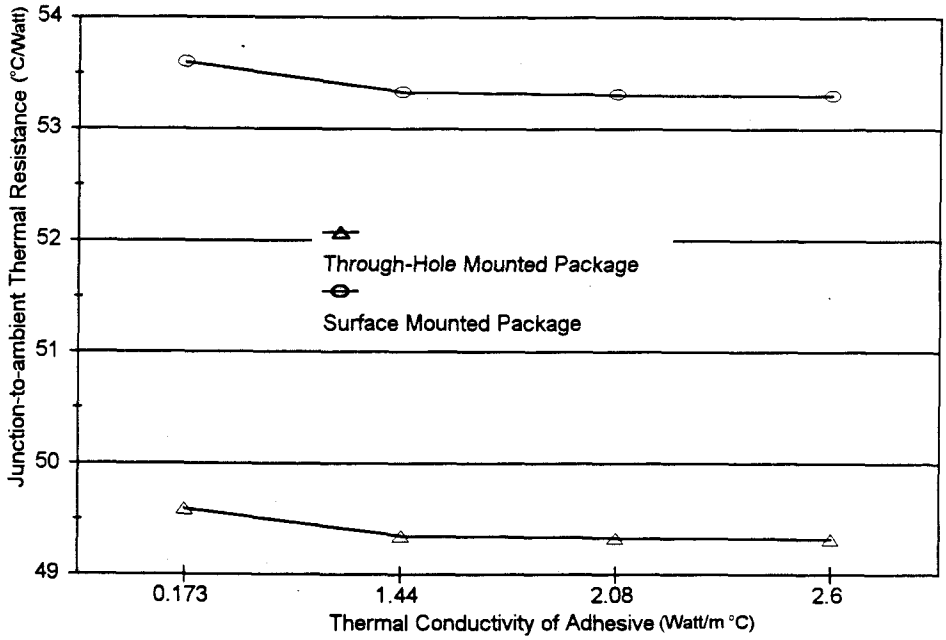

Figure 5.10 Effect of adhesive material on package thermal resistance.

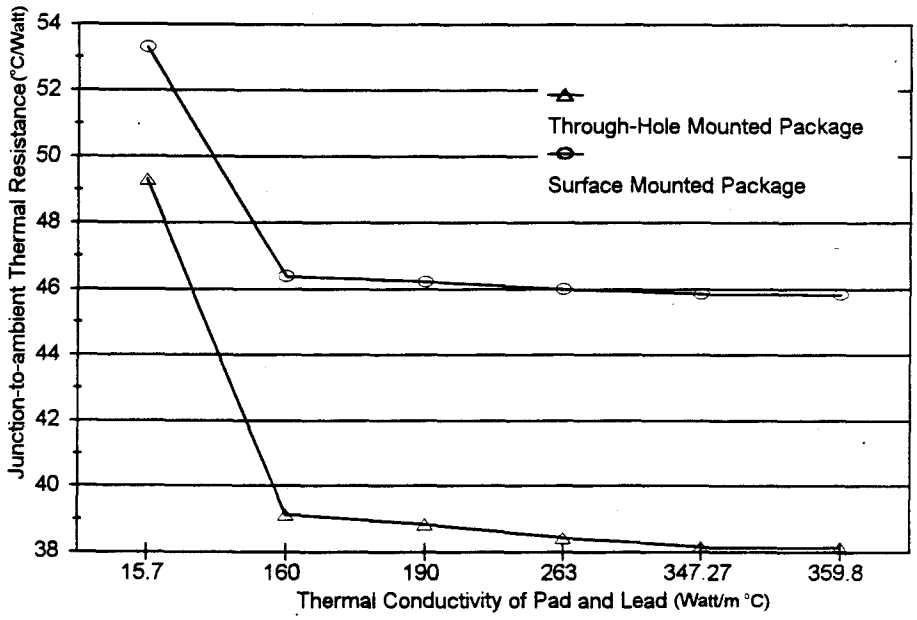

Figure 5.11 Effect of lead and die attach pad material on package thermal resistance.

board is related to the thermal conductivity of the lead and die attach pad materials. The analytical results for the thermal conductivity of the lead and die attach pad materials as well as their effect upon the thermal resistance (θ_{ja}) of the packages is shown in Figure 5.11. Where the effect was an increase in the thermal conductivity of the lead and die attach pad materials, a significant reduction in package thermal resistance was achieved, an effect which was particularly obvious for through-hole mounted packages.

5.2.4 Molding Compound Material

As shown in Figure 5.12, the molding compound material had a considerable effect upon package thermal resistance (θ_{ja}). For given power dissipation from the silicon die, increased thermal conductivity values for the molding compound reduced the package maximum operating temperatures and resulted in significantly improved and lower package thermal resistance. However, such an increase in thermal conductivity may sometimes require a sacrifice with respect to other material properties. For example, higher thermally conductivity molding compounds may have lower fracture toughness, providing less resistance to damage due to thermal-mechanical stresses. Nonetheless, by incorporating these mechanical factors into design considerations during package development, problems that were not previously realized may be diagnosed, resulting in the development of more reliable electronic systems.

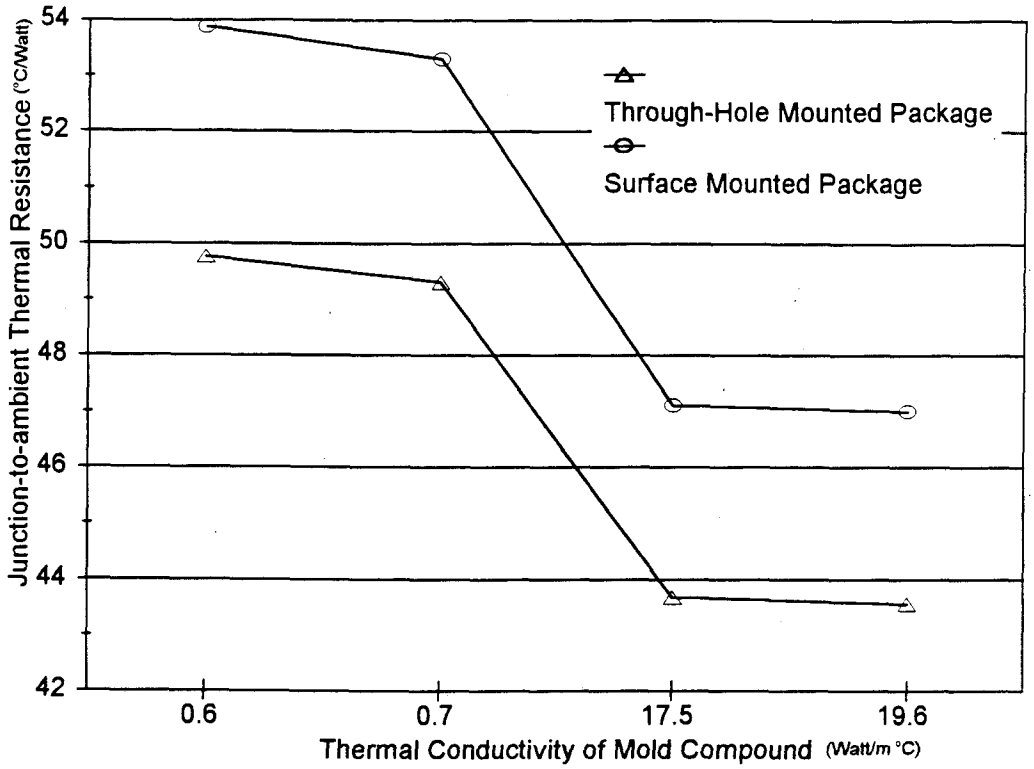

Figure 5.12 Effect of molding compound material on package thermal resistance.

5.2.5 PCB Material

A PCB acts as a heat fin and can provide additional package heat transfer area, resulting in lower junction-to-ambient thermal resistance (θ_{ja}). From Figure 5.13, as PCB thermal conductivity was increased, the spread of resistance through the board was reduced. Similar to heat fins, PCB effectiveness in package thermal enhancement is dependent upon the thermal impedance between the IC package, the PCB, and board area, as well as upon PCB thermal conductivity and the convective heat transfer coefficient between the board and its ambient conditions.

That is, the higher the PCB thermal conductivity, the greater the heat spread on the PCB, resulting in significant reductions in package thermal resistance. In addition, package thermal resistance is also strongly dependent upon the area of the board. With increased board area, there will be a concomitant reductions in thermal resistance values. This is because both the internal and external thermal resistances are inversely proportional to the heat transfer area.

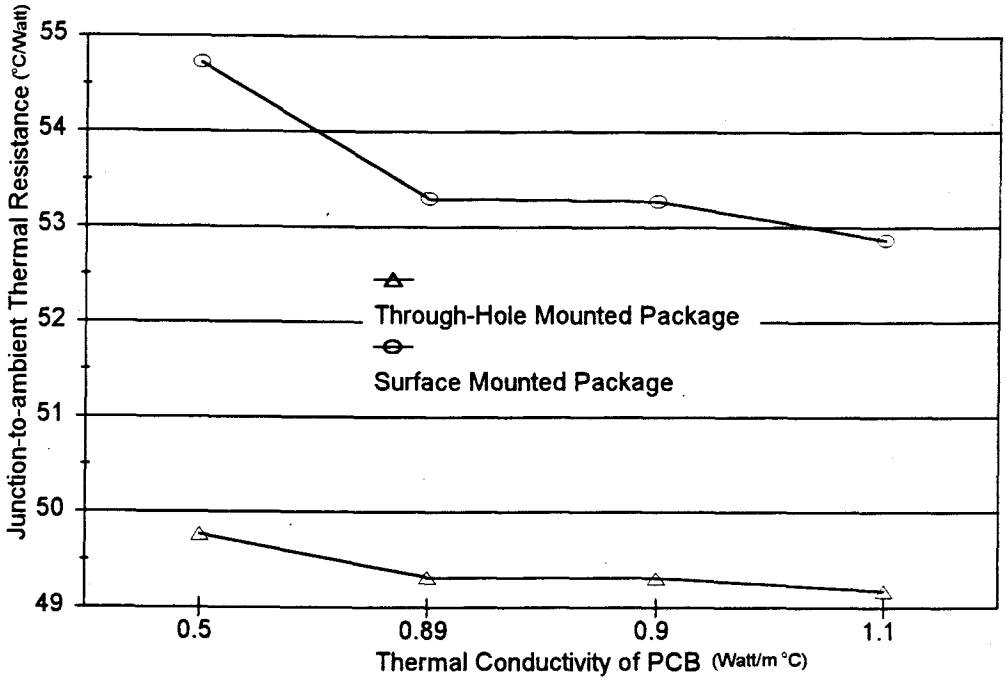

Figure 5.13 Effect of PCB material on package thermal resistance.

5.2.6 Power Dissipation

As could have been anticipated, increased package power dissipation, raising package operating temperatures, resulted in significantly lower junction-to-

ambient thermal resistance (θ_{ja}) values. As shown in Figure 5.14, at lower levels of power dissipation θ_{ja} was strongly dependent upon power dissipation, but as power dissipation was increased, the θ_{ja} values became less sensitive to changes in power dissipation. It should also be noted that at lower power levels the θ_{ja} values for the surface mounted packages were lower than for the through-hole mounted package, but as power dissipation was increased, the thermal resistance values for the surface mounted package became larger than for the through-hole mounted package.

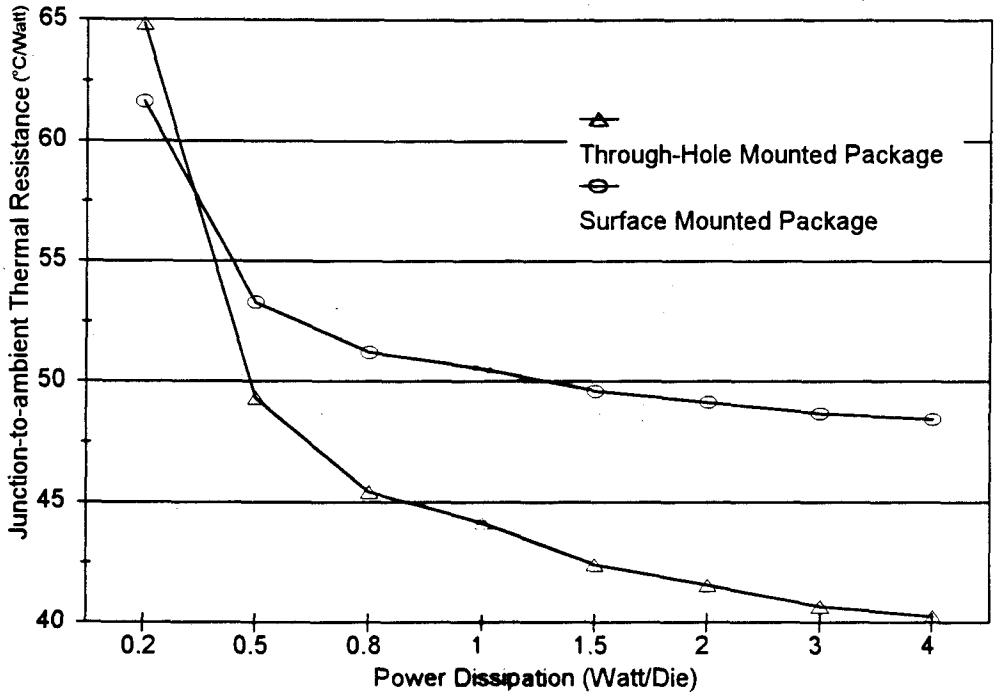

Figure 5.14 Effect of power dissipation on package thermal resistance.

The thermal resistance of electronic packages can be adversely altered by such defects as voids, cracks or the delamination of interfaces within packages. If these types of defects occur in critical heat-flow paths, junction temperatures can rise significantly beyond values forecast for defect-free packages, thereby resulting in increased θ_{ja} values. However, the concept of package thermal resistance is used to quantify package thermal performance as well as to provide a means to determine IC package cooling requirements within a systems environment. With reference to Figures 5.9 - 5.16, the most important results may be summarized as follows. The materials of both the lead and die attach pads and the molding compounds had significant effects upon package thermal resistance and package maximum operating temperature. These effects were greatest for those materials with the highest thermal conductivity. When the package power dissipation was increased, package thermal resistance decreased rapidly, especially at the lower levels of power dissipation. In actuality, the selection of the best method to assure good package thermal performance is dependent upon the high thermal conductivity values of component materials, at least to the extent that other material properties of package components are not sacrificed. The ability to measure package component material thermal characteristics and then select appropriate materials for the package design is the key to optimizing package thermal performance.

5.3 Numerical Correlation Equations for Package Maximum Operating Temperature

Once packages specifications are known, power generation as well as dimensional and material data and acceptable ranges of package operating temperatures become available knowledge. It is then possible to approximate the heat transfer coefficients required for adequate cooling. The choices of coolant and mode of heat transfer determine the magnitude of the heat transfer coefficient which may be achieved. That is of particular importance in that the heat transfer coefficient characterizes the effectiveness with which heat can be removed from an electronic package. The heat transfer coefficient value can be determined either from empirical heat transfer correlations for electronic equipment and systems or from experimental results. If the specified could not be adequately cooled, then the operating temperatures of all package components could not be maintained within their respective functional limits and the result would be a shortened package lifetime. To achieve substantial heat removal from the package while maintaining component operating temperatures within functional limits, direct-immersion liquid cooling using forced convection or boiling can sometimes be applied. The boiling mode of heat transfer offers the highest heat transfer coefficients, and water is the most effective nonmetallic coolant. However, because of their chemical compatibility and their positive heat transfer characteristics, fluorocarbon (FC) liquids have generally been considered the most suitable coolants for direct-immersion cooling applications.

As indicated in Figure 5.15, for a case with power dissipation of 0.5 Watt/die, the package maximum operating temperatures are inversely proportional to the heat transfer coefficients. That is, the higher the heat transfer coefficient, the greater the ability to remove the heat generated by the die from the package. However, from same example case, when the heat transfer coefficient values are large enough (i.e., in excess of 200 Watt/m^2 °C), the maximum package operating temperatures remain almost constant for both the surface mounted and through-hole mounted packages. This phenomenon reveals that for a limited package power dissipation, excessive cooling would be inadequate and wasteful. Therefore, the proper selection of cooling strategy may save the package costs and have a far-reaching effect upon other aspects of total system design.

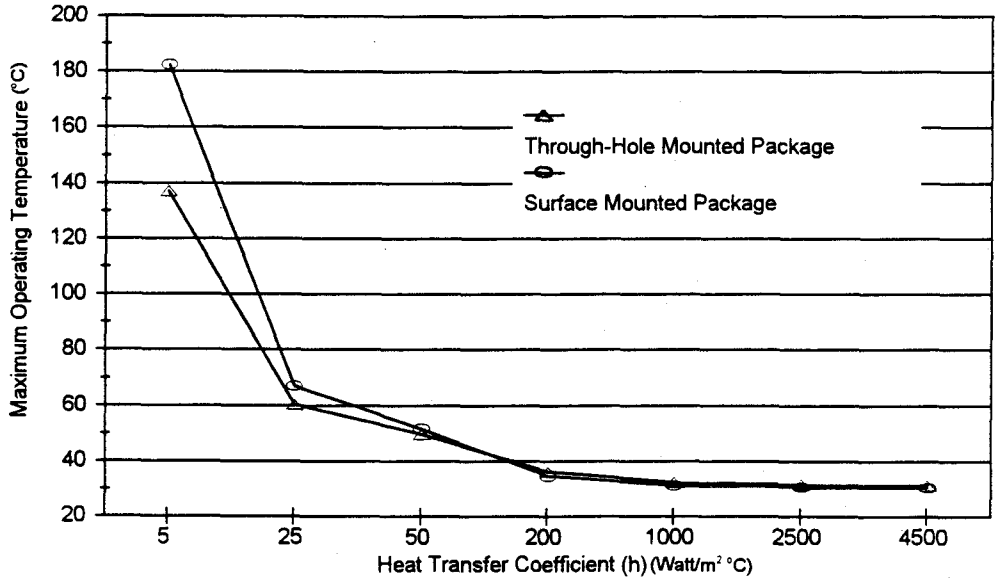

Figure 5.15 Package maximum operating temperature versus convective heat transfer coefficient with constant power dissipation (0.5 Watt/die) at the die.

The effect of the package power dissipation on package maximum operating temperature for various heat transfer coefficients is shown in Figures 5.16 and 5.17 for, respectively, through-hole mounted and surface mounted packages. These effects revealed that conventional forced convection with higher convective heat transfer coefficient values sharply reduced package maximum operating temperatures.

If a cooling alternative, package dimension and component materials are specified, then the maximum operating temperatures within the package are principally associated with power dissipation at the package die. To comprehensively characterize package thermal behaviors, an analytical relation between the maximum operating temperatures and package power dissipation for various heat transfer coefficients is proposed for both surface mounted and through-hole mounted packages, based upon statistical analysis of the FEA results as shown in Figures 5.16 and 5.17. A logarithmic expression, as indicated in equation 5-1, was obtained to predict package maximum operating temperatures for the through-hole mounted package:

$$\ln(T_{max}) = 3.9521 - (0.0078 * h) + (0.7731 * P) - (0.0869 * P^2) \quad (5\text{-}1)$$

The analytical relation for the surface mounted package was:

$$\ln(T_{max}) = 4.0511 - (0.01 * h) + (0.8910 * P) - (0.1056 * P^2) \quad (5\text{-}2)$$

For equations (5-1) and (5-2), P is the uniform power dissipation (Watt/Die) at the die and h is the approximately convective heat transfer coefficient around the packages. The applied heat transfer coefficient range was from 25 Watt/m^2 °C to 75 Watt/m^2 °C, a range in the category of air-forced convection, the most widely used technique for cooling computer systems in present-day use.

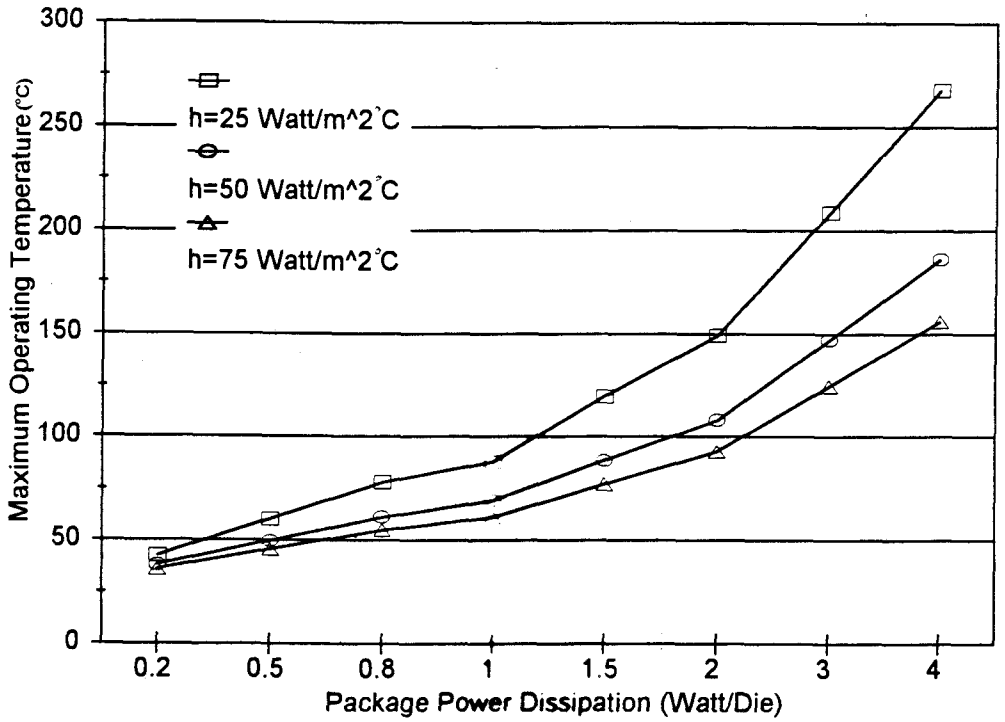

Figure 5.16 Package maximum operating temperature versus package power dissipation at various heat transfer coefficients for through-hole mounted package.

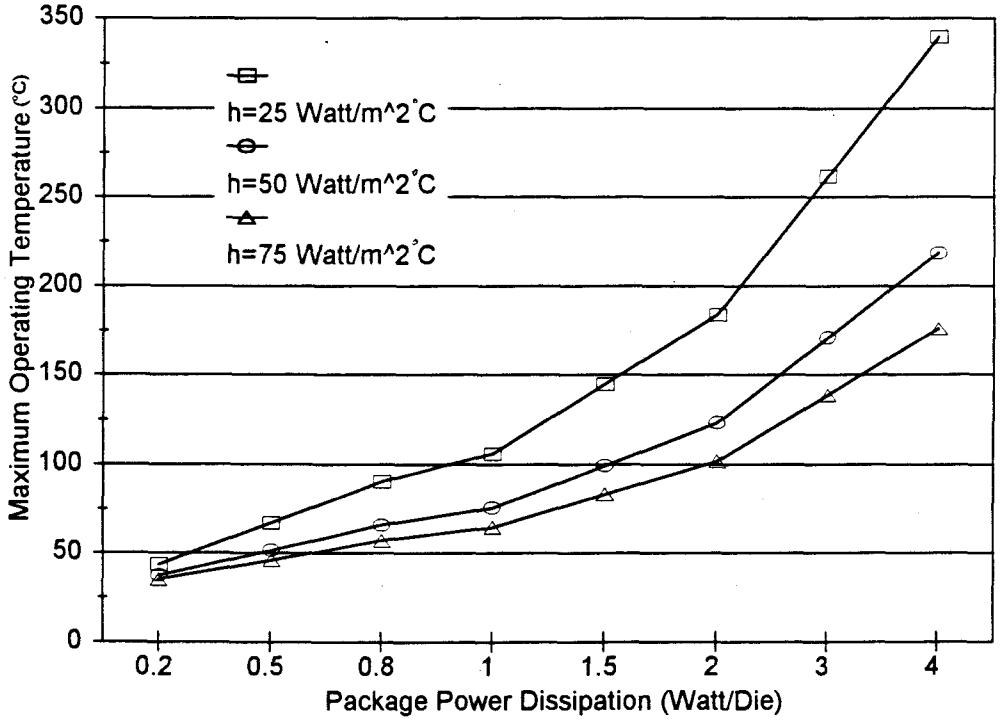

Figure 5.17 Package maximum operating temperature versus package power dissipation at various heat transfer coefficients for surface mounted package.

CHAPTER 6
CONCLUSIONS AND RECOMMENDATIONS

6.1 Conclusions

The results of a numerical study based upon two-dimensional finite element analysis (COSMOS/M) of surface mounted and through-hole mounted IC packages for printed circuit boards, as applied to an investigation of the effects of materials and cooling mechanisms upon IC package thermal performance, has been presented. From the discussions provided in previous chapters, the following conclusions are provided.

The maximum operating temperatures of the IC package are principally dependent upon package power dissipation, the thermal characteristics of the package materials, heat removal capabilities between the package and the heat sink ambience, and ambient temperatures. As might have been expected, the lower temperature environments promoted lower operating temperatures, which in addition were proportional to the thermal conductivity of the package components. In particular, the high thermal conductivity of the package molding compounds served to significantly promote lower operating temperatures for a given thermal loads. This finding underscores the need to develop high thermal conductivity molding compounds that can accommodate dies with higher heat outputs.

In addition, maximum package operating temperatures were also inversely proportional to the heat transfer coefficient for the outer surfaces of molded

packages. The ability of the system to channel the heat outward from the package is largely related to the magnitude of the heat transfer coefficient. Lower heat transfer coefficients serve to dramatically increase package operating temperatures, resulting in significant increases in the package failure rate. Hence, these results suggest that by increasing the area of heat transfer, it will be possible to directly compensate for lower heat transfer coefficients. In many applicable cases, this may be accomplished by attaching a high surface area radiator to the package.

Junction-to-ambient thermal resistance (θ_{ja}) was associated with the transfer of heat from the package directly to the cooling liquid, or indirectly through a so-called heat sink. Although package thermal resistance (θ_{ja}) is an oversimplification of a typically complex heat-flow field both within or outside the package, it can be used as a thermal performance figure of merit. The values of θ_{ja} are dependent upon several parameters, including packaging material thermal conductivity, package size and geometry, PCB thermal characteristics and the cooling mechanisms. Basically, the enhancement of package thermal performances can be achieved by the choice of higher thermally conductive materials, including the die, the lead and die attach pad, and the molding compound. At the same time, however, a number of other factors require simultaneous consideration to achieve optimum or near-optimum results. For example, higher thermal conductivity of the molding compound can be achieved by the use of such fillers as aluminum nitride, which has a higher thermal conductivity than fused silica. However, some of the fillers will interact with the curing agent or catalyst in the molding compound and

thus retard chemical reactions. In addition, the costs for these higher thermally conductive fillers are greater than for silica. Therefore, even if the need is particularly urgent, significant technical hurdles may remain before higher thermally conductive molding compounds can be developed.

Correlations have been developed among package maximum operating temperatures, heat transfer coefficients, and the power dissipation used to predict the maximum operating temperature at given power dissipation level for specified cooling strategies. Close examination of these relations demonstrated that the regression analyses proposed for use can be utilized to evaluate package thermal performances during the early stages of package and system-level design, as well as for determining design strategies and providing descriptions of IC package operating temperatures for a variety of thermal management strategies.

It is anticipated that the successful application of the results of these numerical analyses will help to achieve the objective of reducing thermally caused failures, shortening design cycle times and time-to-market in the modern highly competitive marketplace of commercial electronics.

6.2 Recommendations

The FEM are useful for acquiring qualitative knowledge of the features of heat transfer for convectively-cooled packages. The major deficiency of the present model is that it analyzes only the heat transfer processes for a simulated two-dimensional IC package. In reality, the geometries and heat transfer

capabilities of electronic packages are three-dimensional. From an ideal perspective, it is recommended that the detailed package thermal model should be coupled directly to a fluid-flow code for simultaneous solution. However, the model considered can presently be used to identify the effects of some design changes and material selections. The following recommendations are provided for the future research necessary to extend the findings of the present study relative to the field of heat transfer in electronic packages.

1) To establish a sound basis for comparison of thermal resistance, the conduct of experiments based upon realistic applications is recommended.
2) Obtain heat transfer coefficient values corresponding to air-flow rates and ambient temperatures prior to the calculation of temperature distributions within IC packages.
3) Extend the factors which impact package thermal resistance to involve die sizes, air-flow rates outside the package, the number of lead counts, and the area of PCBs, including the effects of neighboring components.
4) Based upon the model considered in the present investigation, analyze the distribution of thermal-mechanical stress within IC packages, thereby providing an additional deciding factor in the selection of IC package materials.

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APPENDIX

Appendix A: File Input for Finite Element Analysis

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C* COSMOS/M Geostar V 1.65
C* Problem :Thermal analysis for a through-hole mounted package
     with silicon die material.
C*

CRLCORD 1 0 0.0 0.001472 0.0 0.0 0.003672 0.0
CRLCORD 2 0 0.0 0.003672 0.0 0.0 0.004572 0.0
CRLCORD 3 0 0.0 0.004572 0.0 0.0 0.005872 0.0
CRLCORD 4 0 0.0 0.005872 0.0 0.0 0.006372 0.0
CRLCORD 5 0 0.0 0.006372 0.0 0.0 0.006572 0.0
CRLCORD 6 0 0.0 0.006572 0.0 0.0 0.007472 0.0
CRLCORD 7 0 0.0 0.007472 0.0 0.0 0.009572 0.0
CRLCORD 8 0 0.0 0.009572 0.0 0.00625 0.009572 0.0
CRLCORD 9 0 0.0 0.001472 0.0 0.007 0.001472 0.0
CRLCORD 10 0 0.007 0.001472 0.0 0.007 0.003672 0.0
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CRLCORD 14 0 0.0 0.006572 0.0 0.0039 0.006572 0.0
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CRLCORD 36 0 0.00775 0.007272 0.0 0.00775 0.004822 0.0
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CRLCORD 41 0 0.00845 0.003672 0.0 0.008 0.003672 0.0
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CRLCORD 44 0 0.00725 0.001222 0.0 0.00732 0.000011 0.0
CRLCORD 45 0 0.00732 0.000011 0.0 0.007513 0.000183 0.0
CRLCORD 46 0 0.007513 0.000183 0.0 0.00775 0.001222 0.0
CRLCORD 47 0 0.00346 0.007472 0.0 0.0039 0.007472 0.0
CRACSE 48 0 0.0 0.004236 0.007012 0.005256 0.007271 0.003290 0.007471 &
CRACSE 50 0 0.0 0.004236 0.007012 0.005100 0.007271 0.003460 0.007471 &
CRLCORD 52 0 0.005256 0.007272 0.0 0.006397 0.007272 0.0
CRLCORD 53 0 0.005101 0.007272 0.0 0.005256 0.007272 0.0
CRLCORD 54 0 0.004203 0.006372 0.0 0.0044 0.006372 0.0
CRLCORD 55 0 0.003289 0.007472 0.0 0.00346 0.007472 0.0
ACTSET CS 0
SCALE 0.000000
VIEW 0.000000 0.000000 1.000000 0
CLS 1

PLANE Z 0.000000 1
EGROUP 1 PLANE2D 0 1 0 0 0 0 0
RCONST 1 1 1 2 0.01 0.000000

MPROP 1 KX 150
CTNU 1 6 13 10 55 1 47 2 15 3 14 13 6 3
RG 1 1 1 0
MA_RG 1 1 1 0
QERG 1 7122507.1225 1 1

MPROP 2 KX 300
CTNU 2 6 49 4 48 4 53 1 50 4 51 4 55 1
RG 2 1 2 0
MA_RG 2 2 1 0
NMERGE 1 76 1 0.000100 0 1 0

MPROP 3 KX 2.6
CTNU 3 5 14 13 19 1 20 1 17 14 5 1
RG 3 1 3 0
MA_RG 3 3 1 0
CLS 1
NMERGE 1 105 1 0.000100 0 1 0
```

```
NCOMPRESS 1 105 1

MPROP 4 KX 15.7
CTNU 4 5 17 14 54 1 18 2 16 15 4 2
RG 4 1 4 0
MA_RG 4 4 1 0
NMERGE 1 139 1 0.000100 0 1 0

MPROP 5 KX 0.7
CTNU 5 7 8 20 24 7 52 3 48 4 49 4 13 10 7 6
RG 5 1 5 0
MA_RG 5 5 1 0
NMERGE 1 282 1 0.000100 0 1 0
CTNU 6 15 51 4 50 4 22 2 23 2 21 6 25 7 12 20 3 4 16 15 18 2 54 1 20 1&
 19 1 15 3 47 2
RG 6 1 6 0
MA_RG 6 6 1 0
NMERGE 1 441 1 0.000100 0 1 0
NCOMPRESS 1 441 1

MPROP 6 KX 0.0263
CTNU 7 8 32 3 35 6 34 2 38 4 11 21 2 3 12 20 25 7
RG 7 1 7 0
MA_RG 7 7 1 0
NMERGE 1 489 1 0.000100 0 1 0
NCOMPRESS 1 489 1

MPROP 7 KX 15.7
CTNU 8 14 22 2 53 1 52 3 33 3 36 8 27 10 46 3 45 1 44 3 26 10 35 6 32 &
3 21 6 23 2
RG 8 1 8 0
MA_RG 8 8 1 0
NMERGE 1 525 1 0.000100 0 1 0
NCOMPRESS 1 525 1

MPROP 8 KX 22
CTNU 9 6 37 2 39 4 41 2 28 8 43 1 27 10
RG 9 1 9 0
MA_RG 9 9 1 0
NMERGE 1 531 1 0.000100 0 1 0
NCOMPRESS 1 531 1
CTNU 10 6 34 2 26 10 42 1 10 8 40 2 38 4
RG 10 1 10 0
MA_RG 10 10 1 0
```

```
NMERGE 1 551 1 0.000100 0 1 0
NCOMPRESS 1 551 1

MPROP 9 KX 0.89
CTNU 11 5 11 21 40 2 10 8 9 23 1 8
RG 11 1 11 0
MA_RG 11 11 1 0
NMERGE 1 734 1 0.000100 0 1 0
NCOMPRESS 1 734 1
CTNU 12 5 41 2 29 4 31 8 30 8 28 8
RG 12 1 12 0
MA_RG 12 12 1 0
NMERGE 1 771 1 0.000100 0 1 0
NCOMPRESS 1 771 1

CECR 8 50 25 8 1 0
CECR 24 50 25 24 1 0
CECR 33 50 25 33 1 0
CECR 36 50 25 37 1 0
CECR 39 50 25 39 1 0
CECR 29 50 25 29 1 0
CECR 9 50 25 9 1 0
CECR 42 50 25 46 1 0
CECR 30 50 25 30 1 0

SCALE 0.95
PAPER_SETUP A 0 0 0.12 0.88 0.2 0.82 1
PAPER_SETUP A 0 0 0.12 0.88 0.2 0.82 0

C*
C*
```