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In this dissertation, two important current mode circuit design subjects have been explored. In the first part, the switched-current circuit technique has been investigated. The fundamental performance and limitations of this technique are explored. One of the major limitations, the signal distortion caused by clock feedthrough has been substantially reduced by a newly developed clock feedthrough cancellation technique. In addition, a filter synthesis technique has been developed by directly simulating the structure of digital filter. Several experimental CMOS prototypes have been designed and fabricated. The measured frequency and phase responses demonstrated the feasibility of this synthesis technique. In the second part, a new logic family called current-steering logic has been developed. The fundamental performance and characteristics of this technique have been discussed including the basic inverter and NOR gate with DC analysis, transient analysis and power-delay product. It has been shown that the current-steering logic has a much smaller current spike than conventional CMOS logic circuits, which is especially desirable in mixed-mode applications. Several experimental prototypes have verified the functionality and performance of this new technique.

# Current Mode Analog and Digital Circuit Design

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## INTRODUCTION

The Integrated Circuit (IC) is the most important and commonly used component in today's electronic systems. It was invented by Jack Kilby of Texas Instruments in 1958 [1]. Since then, many different IC technologies have been developed. A majority of today's IC's are made of the silicon metal-oxide-semiconductor field effect transistors (MOSFET). The MOS technology was first developed to implement digital ICs in the early 1960's. Since then, the evolution of scaled MOS digital processes has pushed the level of integration to more than a million transistors on a single chip. With such capability, a complex digital system can now be easily integrated on a single silicon chip. To interface with the external world, it is usually required to perform various analog operations such as amplification, modulation, filtering, etc. Therefore, in order to increase system functionality as well as performance, and to reduce the total manufacturing cost, it is often necessary to integrate analog and digital circuits together on a single mixed-mode chip [30].

The first analog MOS IC was developed in 1969 by Chalfan and Looney at Oregon State University [2]. With the further development of the MOS operational amplifier in the early 1970's, and the switched-capacitor (SC) technique in the late 1970's [3][4][7][8][9], analog MOS technology provided efficient and accurate analog signal processing techniques. It used nearly ideal MOS switches, accurate voltage operational amplifiers and excellent capacitor matching properties to achieve the first high-performance CMOS analog signal processing technique. Currently,

switched-capacitor circuits play a major role in analog and mixed-mode integrated circuits and systems.

For economic reasons, the analog part of a mixed-mode IC has to be fully compatible with a semiconductor process technology tailored for digital circuits. This means that in mixed-mode applications, the analog circuits must operate at high speeds and lower power supply voltages. For example, in the newly developed submicron processes, the power supply voltage has been reduced from 5.0 volts to 3.3 volts. Moreover, in mixed-mode applications, the analog circuits are required to reject the interference of high-frequency power supply noise generated by CMOS digital circuits. In this high-frequency mixed-mode environment, the performance of commonly-used operational amplifiers is unsatisfactory resulting in switched-capacitor circuits that have reduced accuracy.

To resolve this dilemma, current instead of voltage, can be used to represent the signal [5][6][14][15][16][28][29]. By using current, the required voltage swing can be reduced for a given signal swing due to the inherent nonlinear I-V relationship of most active devices. For example, the drain current of a saturated MOS device is proportional to the square of its gate voltage. Therefore, if drain current is used to represent the signal, a four times change of signal current causes only a doubling of the excess gate voltage. Current-mode processing also increases the bandwidth and reduces the requirement for high power supply voltage analog circuits.

Based upon the same consideration, especially in the submicron processes, the reduced power supply voltage also reduces the voltage swing of a digital circuit, and results in a lower noise margin. In addition, the higher operating speeds will cause higher power supply noise due to the switching current spike of static CMOS

logic circuits. To improve the performance of mixed analog/digital integrated circuits, current can also be used to represent the digital "1" and "0" logic levels. A technique called current-steering logic is developed here [16]. Our analysis shows that compared to static CMOS logic, the current-steering circuit reduce power supply and ground current spikes by nearly two orders of magnitude, operate under lower power supply voltages, and achieve similar switching speeds.

This dissertation is divided into two parts. In the first part, it focuses on one of the most important current-mode analog signal processing techniques, switched-current circuits. The basic operating principle and building blocks of switched-current circuits are presented. Then, most of the important circuit performance parameters are analyzed. Following that, it discusses the major limitation on the accuracy of switched-current circuits--the clock feedthrough problem. A clock feedthrough cancellation technique is developed to substantially reduce the harmonic distortion and linear gain error caused by clock feedthrough. Finally, based on the switched-current circuit building blocks, a direct sampled-data filter synthesis approach is discussed. Rather than simulating an active-RC or switched-capacitor filter prototype [5][6], the switched-current filter is synthesized by mapping the digital filter structure directly. A switched-current Finite Impulse Response (FIR) filter is given as an example, and the deviations in its frequency response due to nonideal circuit effects are discussed.

In the second part, the current-steering logic technique is developed and analyzed. First, the digital "1" and "0" logic levels are defined in the current domain. Then the current-steering inverter is introduced as well as the current-steering NOR gate; some common digital applications using current-steering logic circuits such as flip-flop and Programmable Logic Array (PLA) are presented. In

addition, the dc transfer and transient delay characteristics of current-steering circuits are discussed. It is shown that the current-steering logic circuits have a much smaller switching current spike and comparable operating speed to static CMOS logic circuits. Its operation and performance are independent of power supply voltages over a wide range.

# PART I

# SWITCHED-CURRENT FILTER DESIGN

## CHAPTER 1. OVERVIEW

Monolithic precision integrated filters are widely used in many different types of electronic systems. Due to the rapid advancement of VLSI technology, it is often desirable to integrate various precision filters together with other analog or digital circuits on a single silicon chip usually using complementary metal on silicon (CMOS) technology. In addition, it is also required that the integrated filters occupy a small silicon area, are insensitive to processing and operating parameter variations, and operate at high speeds with high accuracy.

In the early 1970's, Charge-Transfer Devices (CTD) were introduced and used to implement analog sampled-data transversal filters; this approach has two major disadvantages. First, the transversal filter was the only type of filter that CTD devices could implement accurately and efficiently. Although the transversal filter has the advantage of a linear phase response, it requires a very high order filter when a large stopband attenuation is needed. Moreover, the requirements for high-performance CTD transversal filter, in terms of high charge-transfer efficiency and low insertion loss usually mandate the use of a non-standard MOS technology. Furthermore, the low doping levels required for high-performance CTD's are contrary to the trend to higher doping levels as MOS technology is scaled to smaller feature sizes. Hence, the technology required to implement high-performance CTD transversal filters is not compatible with scaled VLSI analog and digital integrated circuits which are essential for modern system applications.

Since the late 1970's, Switched-Capacitor (SC) circuits have dominated the analog sampled-data signal processing area. They are reliable, precise and (with the inclusion of linear capacitors) compatible with other analog and digital MOS circuits, and have been applied to a wide range of analog signal processing applications. Switched-capacitor circuits do not fit the standard digital VLSI processing technology as extra options such as two layers of polysilicon are needed for precision capacitors. In addition, as the VLSI feature size shrinks, the size of operational amplifiers cannot be reduced proportionally. So in mixed-mode integrated systems, the cost of switched-capacitor filters rises, and the required low power supply voltage limits circuit performance.

Since the explosion of VLSI technology, in the mid-1980's, many low frequency signal processing applications have been implemented using purely digital signal processing techniques. Although it is less silicon-area-efficient and dissipates more power than analog techniques such as switched-capacitor circuits, the digital approach offers the flexibility and high accuracy of digital signal processing, easier application of computer aided design tools, and simpler test procedures. These advantages are usually realized only in low frequency applications. The complexity and cost of high-speed A/D and D/A converters and high-speed digital multipliers usually prohibit most applications in the middle to high-frequency regions.

The Switched-Current (SI) filtering technique was first proposed in 1989 [5]. Since then, different types of switched-current filters have been developed, and it has been shown that the SI technique has several advantages over the other filtering techniques discussed above. It is entirely compatible with standard CMOS digital processing technology, and achieves reasonable accuracy using low power

supply voltages. The high bandwidth capability of the MOS current mirrors used to implement SI circuits provides the potential to operate at higher frequencies than switched-capacitor circuits.

Chapter 2 explains the configurations and operation of the basic building blocks of SI circuits. In Chapter 3, the practical design aspects of SI circuits are discussed including the finite output resistance effects, nonideal MOS switch effects, MOSFET threshold mismatch effects, and noise and dynamic range considerations. In Chapter 4, the clock feedthrough mechanism is presented, and a cancellation technique is proposed to reduce its effects of linear current gain error and harmonic distortion. In Chapter 5, one method to implement SI filters is reviewed based on the first-generation SI integrator. Synthesis procedures starting from various digital filter structures are presented. Finally, some experimental results of CMOS SI FIR filters are presented, and a summary of this research project is presented in Chapter 6.

# CHAPTER 2. BASIC BUILDING BLOCKS

This chapter begins by introducing the basic definition of current-domain signal processing. Followed by the switched-current circuit implementations of several essential analog signal processing functions are presented. Finally, in order to interface with the existing voltage-domain circuits, the voltage-to-current and current-to-voltage converters are discussed.

## 2.1. Definitions

A switched-current (SI) circuit is defined as an analog sampled-data circuit which uses currents instead of voltages to represent analog signals; thus all analog signal processing tasks are performed in the current domain. Although there are always voltages existing within the SI circuit, these voltages are an indirect consequence of current signals, and are only used as intermediate media for signal processing.

Because the signal current flows in either direction, the positive direction of a current signal must be defined. For convenience, the signal flowing into the input node and out of the output node are defined as positive as shown in Fig. 1.

## 2.2. Building Blocks

A circuit which performs the summation operation in the current domain is easily constructed as shown in Fig. 2. By applying Kirchoff's Current Law (KCL), it is clear that

$$i_o(t) = i_1(t) + i_2(t) + i_3(t). \tag{1}$$

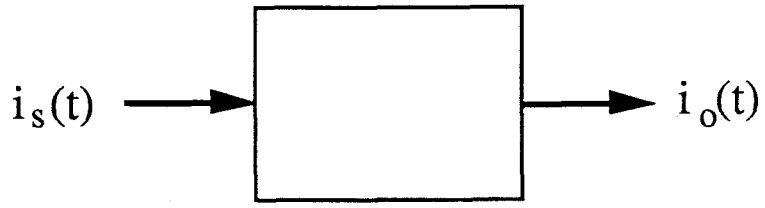



Fig. 1 Definition of positive current signal direction.

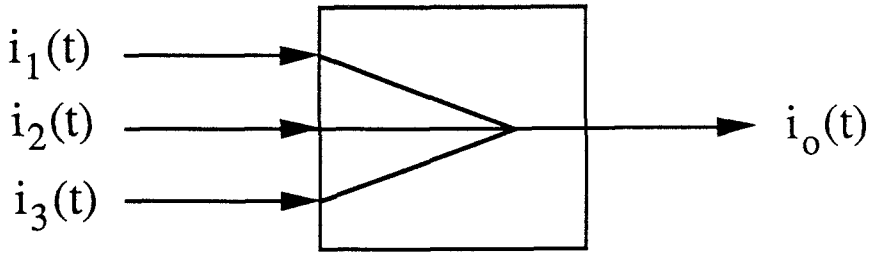



Fig. 2 Current signal summation circuit.

Unlike voltage signal processing, an important advantage in current domain is that signal summation is easily implemented by simply connecting all signals together as shown.

Next, consider the simple biased current mirror amplifier shown in Fig. 3, and assume both MOSFETs are saturated:

$$I_{ds1} = \frac{1}{2} K'_n(W/L)_1(V_{gs1}-V_{t1})^2 \tag{2a}$$

$$I_{ds2} = \frac{1}{2} K'_n(W/L)_2(V_{gs2}-V_{t2})^2 \tag{2b}$$

With $V_{gs1} = V_{gs2}$ under ideal matching between $M_1$ and $M_2$, and ignoring channel length modulation effects, $I_{ds2} = I_{ds1}$. Apply KCL to Fig. 3 we see that

$$I_{ds1} = I + i_s \tag{3a}$$

$$I_{ds2} = I - i_o \tag{3b}$$

and therefore

$$i_o = - i_s. \tag{4}$$

Hence, the simple biased current mirror amplifier performs the signal inversion operation in the current domain.

By using a similar circuit as shown in Fig. 4 with $(W/L)_2 = K(W/L)_1$ and KI as biased current in the output branch, we see from (2a) and (2b) that

$$V_{gs1} = \sqrt{\frac{2I_{ds1}}{K'_n(W/L)_1}} + V_{t1} \tag{5a}$$

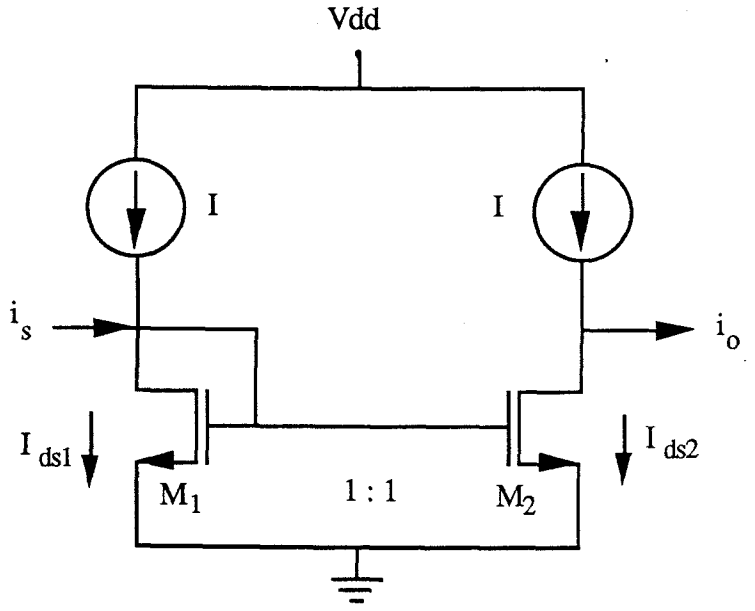
$$V_{gs2} = \sqrt{\frac{2I_{ds2}}{K'_n(W/L)_2}} + V_{t2} \tag{5b}$$

Again, with $V_{gs1} = V_{gs2}$, and also assuming matched process parameters, then

$$I_{ds2} = \frac{(W/L)_2}{(W/L)_1} I_{ds1} \tag{6}$$

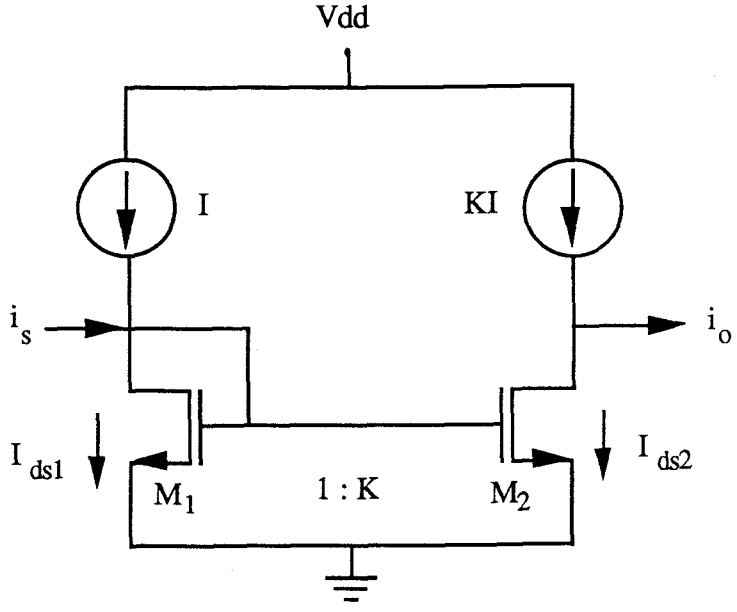
Using (3a) with $I_{ds2} = KI - i_o$, from KCL where $K = \frac{(W/L)_2}{(W/L)_1}$, then

$$i_o = - \frac{(W/L)_2}{(W/L)_1} i_s \tag{7}$$




$$(W/L)_2 = (W/L)_1$$

Fig. 3 Current signal inversion circuit.




$$(W/L)_2 = K(W/L)_1$$

Fig. 4 Current signal scaling circuit.

Hence a simple biased current mirror with ratioed output device and output bias current performs the scaling operation in the current domain. With CMOS VLSI technology, relatively accurate MOSFET pair matching is achieved, which means the accuracy of all the current signal processing circuits discussed above is also relatively high.

By adding a switch between the two gates of the MOSFETs in the biased current mirror amplifier as shown in Fig. 5, the current track-and-hold (T/H) circuit is configured. When Clock is HIGH and the switch $M_s$ is turned ON, $V_{gs1} = V_{gs2}$, and the circuit is equivalent to the simple biased inverter shown in Fig. 6(a); since $i_o(t) = - i_s(t)$, the output current simply tracks the input current with inversion. When at time $T_1$ Clock goes LOW and the switch $M_s$ is turned OFF, the instantaneous gate voltage of $M_2$ is held on the gate capacitance $C_{gs2}$, so that $V_{gs2}(t) = V_{gs1}(T_1)$ for $t > T_1$. In the current domain, $i_o(t) = - i_s(T_1)$. If the switch is implemented using an n-channel MOSFET with its gate controlled by a clock signal of pulse width $T_1$ and period $T_2$, then the output of this circuit is

$$i_o(t) = - i_s(t) \qquad 0 \le t < T_1 \tag{8a}$$

$$i_o(t) = - i_s(T_1) \qquad T_1 \le t < T_2. \tag{8b}$$

One interpretation of Eq. (8) is that the switched-current track-and-hold circuit delays the input current signal by a half clock period to the output, so that this circuit is useful as an analog sampled-data delay circuit.

### 2.3. Voltage-Current Converters

For historical reasons, almost all of the existing signal-processing circuits and systems are designed and operated in the voltage domain. In order to implement the emerging current signal processing techniques together with other existing circuits and systems, it is essential to convert between the voltage and current

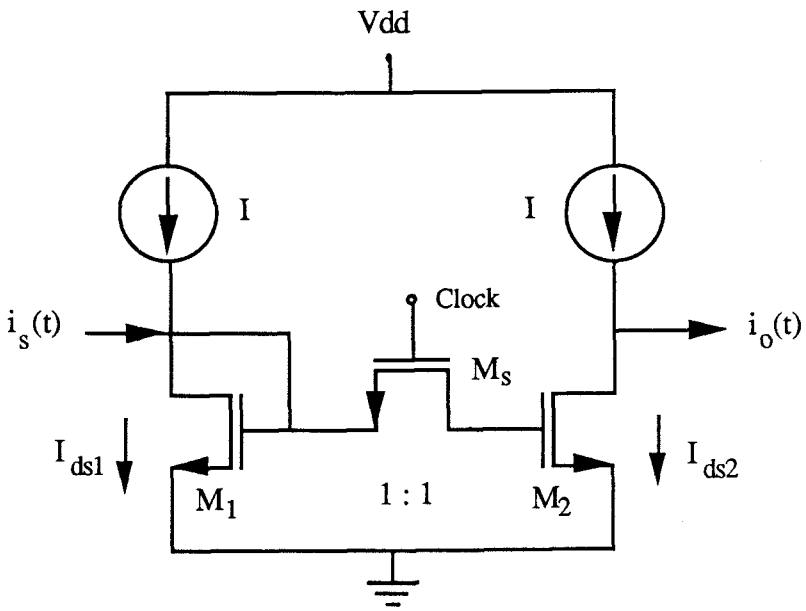
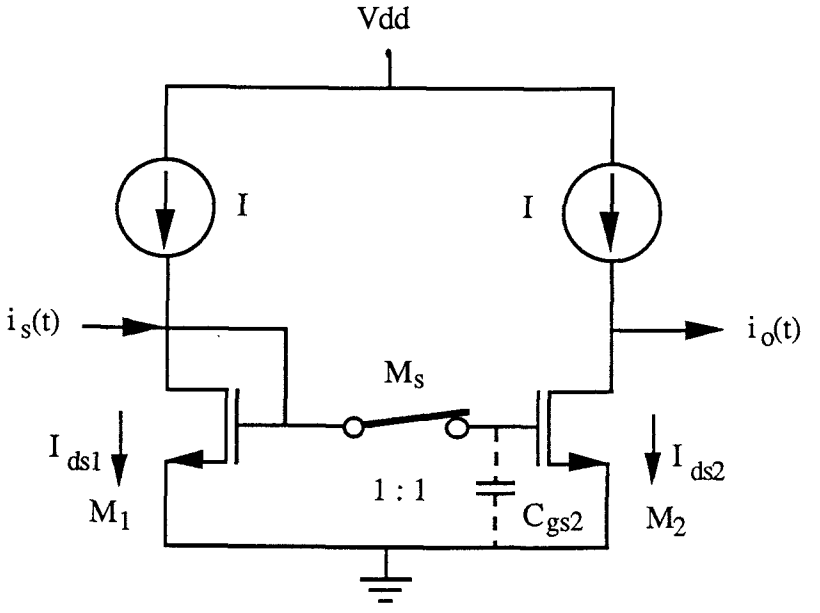
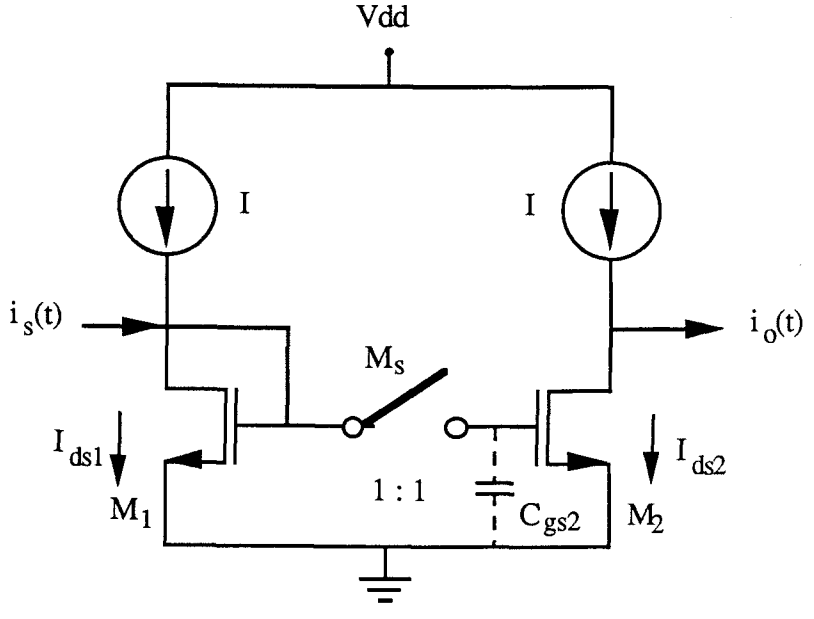



Fig. 5 Current signal track-and-hold circuit.




(a)




(b)

Fig. 6 Current signal track-and-hold circuit.

(The switch symbol represents an ideal NMOS switch)

domains. The ideal voltage/current (V-I) converter is defined as a circuit which has a linear transfer characteristics between input voltage and output current; ideally then, no harmonic distortion is introduced during the V/I conversion.

Two circuits which perform the voltage-to-current conversion are shown in Fig. 7. In Fig. 7(a), assuming an ideal operational amplifier, $v+ = v- = v_{in}$, Hence $V_R = v_{in}$, and $I_R = V_R/R$ due to the infinite input impedance of opamp. Hence

$$i_{out} = I_R = \frac{v_{in}}{R} \tag{9}$$

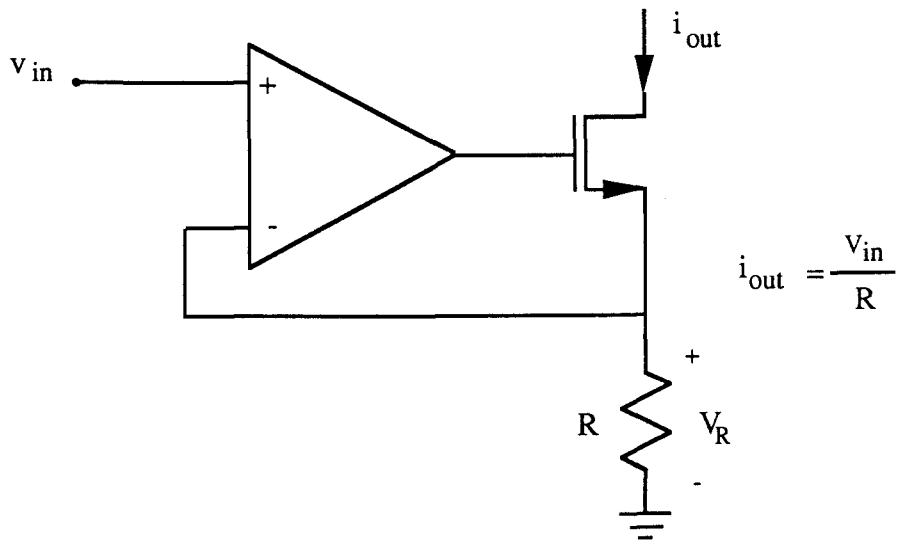
To the degree that R is linear, a linear V/I conversion is achieved.

A second voltage-to-current converter is shown in Fig. 7(b). The basic principle is that the input current $I_R = v_{in}/R$ flows into the drain of $M_1$ due to the negative feedback action around the opeartional amplifer. If any current error is produced in $M_1$, the voltage on v+ changes, and is amplified by the open-loop gain of opamp, so that the gate voltage of $M_1$ is adjusted to reduce its current error. The V/I relation is the same as in Eq. (9).

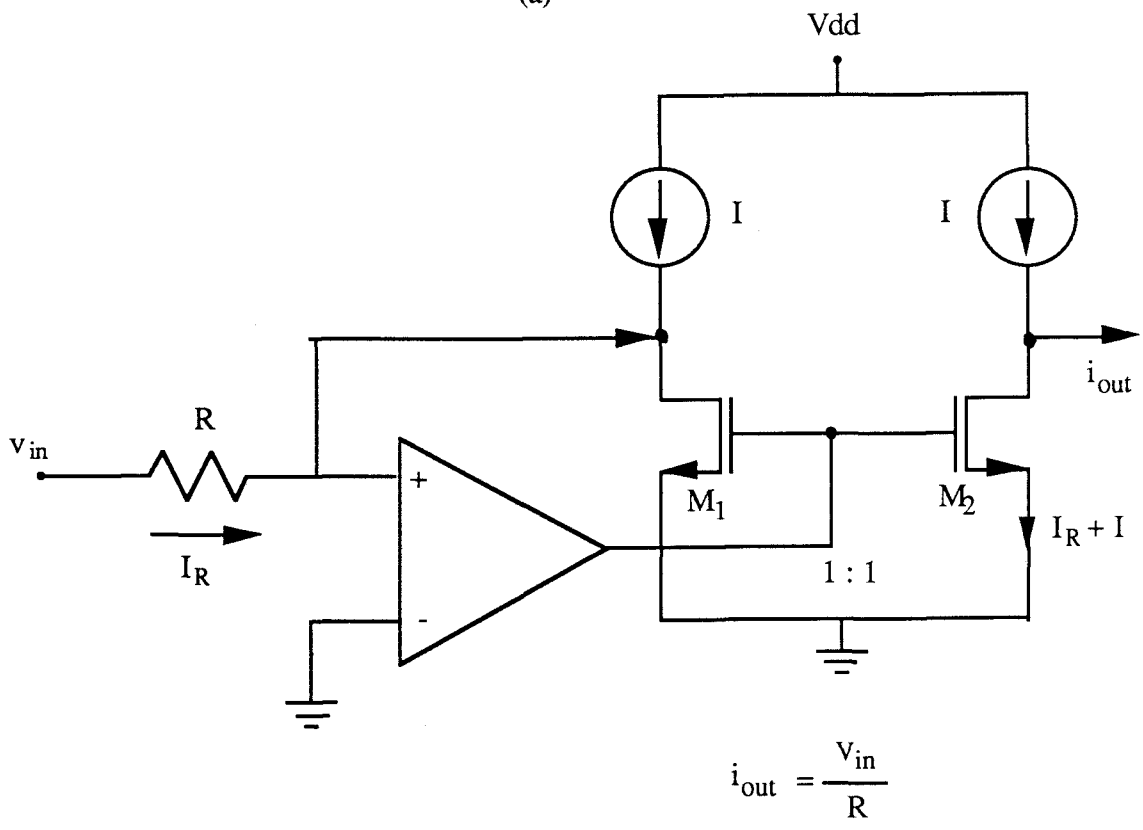
The output current-to-voltage (I-V) conversion is implemented using the simple circuit as shown in Fig. 8. Assuming an ideal opamp, it is obvious that

$$v_{out} = i_{in} R. \tag{10}$$

In this section we have shown various switched-current circuit building blocks which are used to implement the basic analog signal processing functions such as summation, inversion, scaling, and delay. We also showed some simple circuits which are used to implement voltage/current and current/voltage conversions.




(a)




(b)

Fig. 7 Voltage-to-current converters using ideal operational amplifiers.

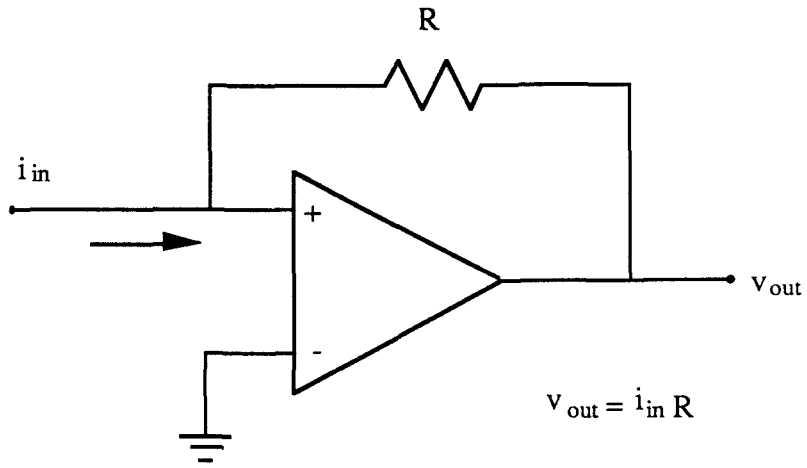



Fig. 8 Current-to-voltage converter using ideal operational amplifier.

# CHAPTER 3. PERFORMANCE ANALYSIS OF SWITCHED-CURRENT CIRCUITS

The CMOS switched-current circuits discussed in the previous chapter can be used to implement various analog sampled-data signal processing systems including SI filters [5][6][14][15]. In order to achieve high accuracy and performance similar to switched-capacitor filters, many nonideal factors must be considered, including finite output resistance effects, MOSFET threshold and size mismatch effects, nonidealities associated with the MOS switches, clock feedthrough effects, etc. These practical design issues and performance limitations of switched-current circuits are discussed in this chapter.

## 3.1. Finite Output Resistance Effects

From the previous discussion, the basic building block of switched-current circuits is the simple biased current mirror amplifier shown in Fig. 9(a) where the input source is represented as a Norton equivalent and the output loading resistance is $R_L$. Its small-signal ac model is shown in Fig. 9(b). At low frequencies ignoring all capacitances, its current-domain transfer function is given by

$$\frac{i_o}{i_s} = \frac{-g_{m2}g_L}{(g_{ds2}+g_{ds4}+g_L)(g_{m1}+g_{ds1}+g_{ds3}+g_s)} \tag{11}$$

It is evident from Eq. (11) that even if the two MOSFETs match with $g_{m1} = g_{m2}$, the nonideal input and output conductances, $g_{ds1}$, $g_{ds2}$, $g_{ds3}$, $g_{ds4}$, $g_s$, result in a lossy current mirror, which means the output current signal is always less than the input current signal. With this gain error, the basic circuit blocks such as the inverting, scaling and delay stages also exhibit gain errors. These gain errors usually cause a frequency response error for the entire filter. For example, if the channel length modulation constant is $\lambda = 0.05$, the bias current I = 100 μA, and

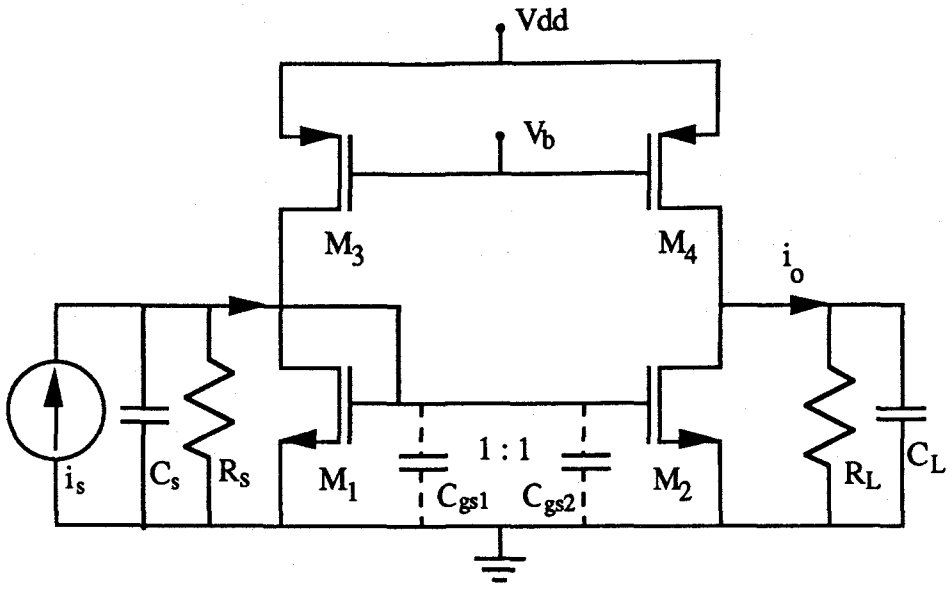
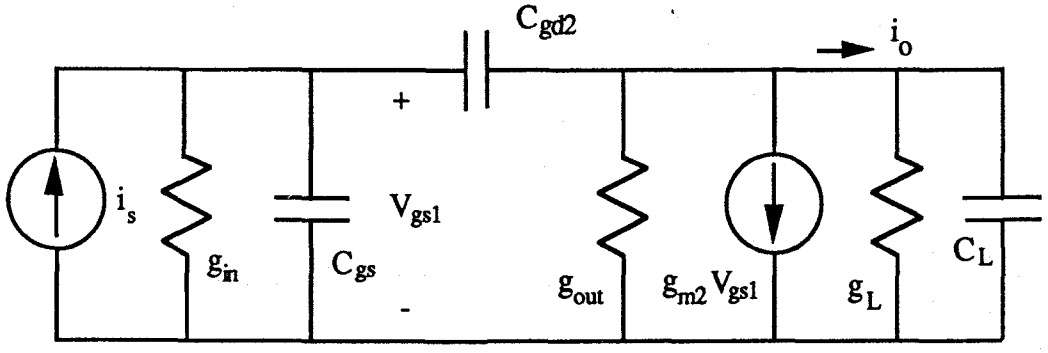



Fig. 9(a) Simple current mirror amplifer with source and loading.




$$g_{in} = g_s+g_{m1}+g_{ds1}+g_{ds3}$$

$$g_{out} = g_{ds2}+g_{ds4}$$

$$C_{gs} = C_{gs1}+C_{gs2}+C_s$$

Fig. 9(b) Small-signal equivalent circuit of simple current mirror amplifier.

W/L = 100μm/10μm for $M_1$ and $M_2$, then $g_{ds} = \lambda I = 5\mu S$, $g_m = 300\mu S$, and the gain error is about eight percent. Figure 10 shows the simulation results of a simple current mirror where the output signal amplitude is reduced by about seven percent relative to the inputs.

In high-frequency applications, short-channel lengths must be used to increase transconductances and reduce gate capacitances. Unfortunately, the stronger channel-length modulation effects increase the output conductance of each MOSFET proportionally and result in a higher gain error for each stage. To improve the performance in these applications, a cascode current mirror (Fig. 11) should be adopted as the basic building block. Two cascoded MOSFETs are used to replace each MOSFET of previous circuit. The output conductance of each cascoded MOSFET pair can be easily calculated. For example, the equivalent output conductances of MOSFET pair $M_3$, $M_7$ is

$$g_{out3,7} = \frac{g_{ds3}\, g_{ds7}}{g_{ds3}+g_{ds7}+g_{m7}} \approx \frac{g_{ds3}\, g_{ds7}}{g_{m7}} \tag{12a}$$

The equivalent output conductance is substantially reduced without affecting the high-frequency performance. Hence, the transfer function of this cascode current mirror is

$$\frac{i_o}{i_s} = \frac{-g_{m2}g_L}{(g_{out2,6}+g_{out4,8}+g_L)(g_{m1}+g_{out1,5}+g_{out3,7}+g_s)} \tag{12b}$$

Using the same parameters as above, from Eq. (12a), the equivalent output conductances $g_{out1,5}$, $g_{out2,6}$, $g_{out3,7}$ $g_{out4,8}$, are about 0.08μS, then the gain error of this cascode current mirror is about 0.15 percent, which is adequate for most applications.

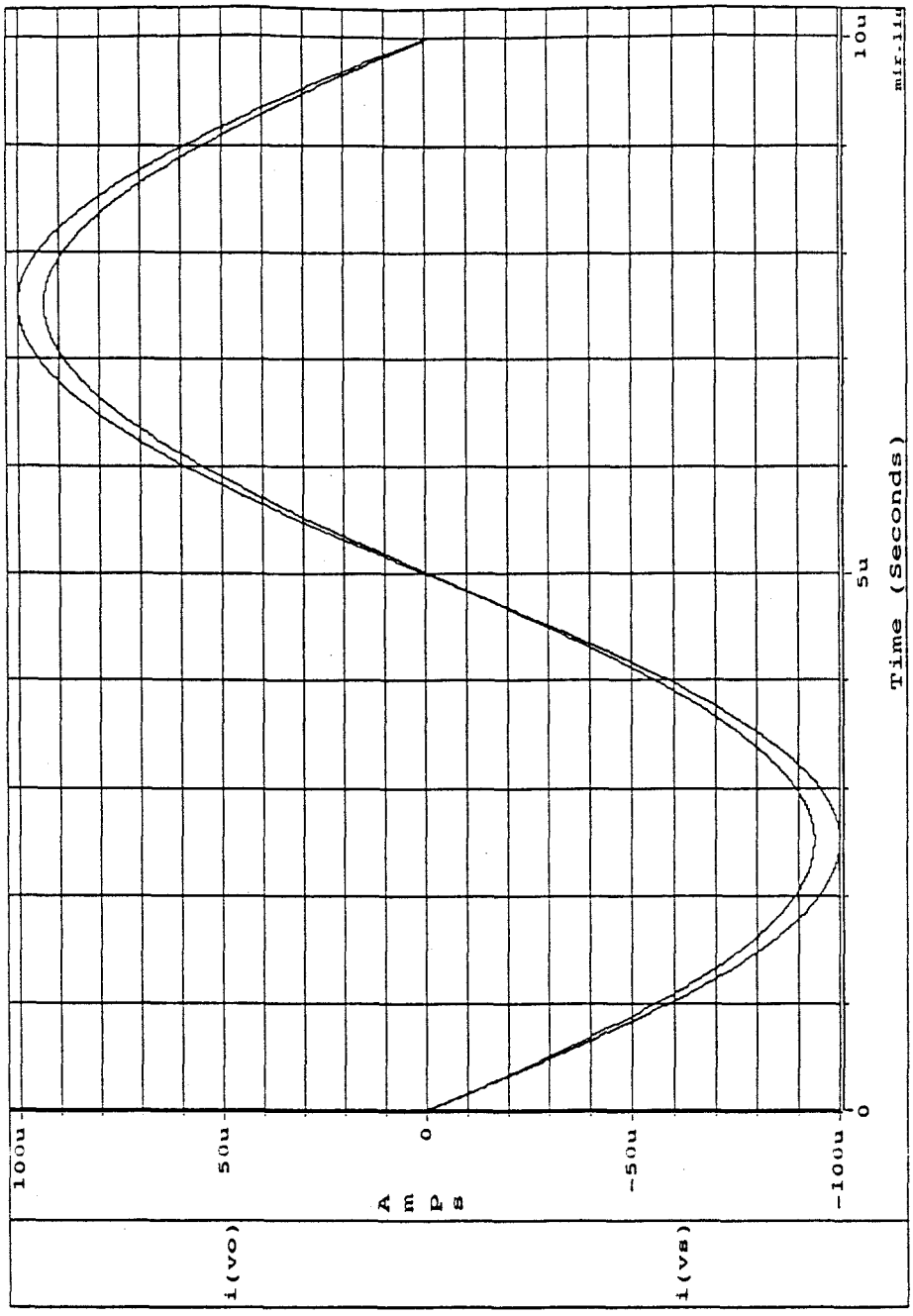



Fig. 10 SPICE simulation of finite output resistance effects for circuit of Fig. 9(a), with $(W/L)_1 = (W/L)_2 = (W/L)_3 = (W/L)_4 = 100\mu m/10\mu m$, $R_s = R_L = 0$, and bias current $I = 100\mu A$.

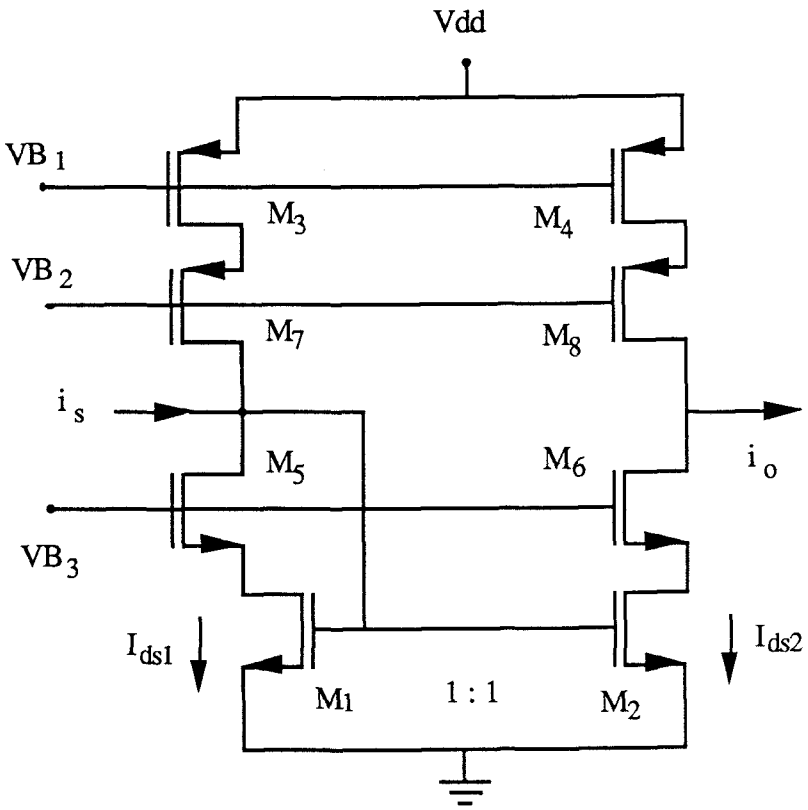



Fig. 11 Low-voltage cascode current mirror.

### 3.2 Nonideal MOS Switch Effects

Since MOSFETs are used as switches in switched-current delay circuits, the channel resistance of MOSFETs limits the rate that charge is transfered to the holding capacitor, and thus limits the maximum operating speed.

During the sampling period, the channel resistance of the switch can be represented as a simple linear resistor as shown in Fig. 12. Assume the maximum channel resistance of the switch is $R_c$, and the holding capacitance is $C_{gs2}$. If the input current signal is small relative to the bias current, then the signal voltage on the gate of $M_1$ is

$$v_{g1} = \frac{i_s}{g_{m1}} \tag{13}$$

and the hold voltage after time period $t = T_S$ is

$$v_{g2} = v_{gs1}\,(1 - \exp(-\frac{T_s}{R_c C_{gs2}})) \tag{14}$$

Then the output signal current is

$$i_o = g_{m2}\, v_{g2} = \frac{g_{m2} i_s}{g_{m1}} (1-\exp(\frac{-T_s}{R_c C_{gs2}})) \tag{15}$$

where $T_S$ is the ON time of the clock period. So a certain amount of error will be generated due to the channel resistance of the switch, and the error is

$$i_{error} = \exp(-\frac{-T_s}{R_c C_{gs2}}) i_s. \tag{16}$$

Hence incomplete charge transfer during the clock sampling results in an additional current gain error for each delay stage. To reduce this error, a longer sampling period is required. For example, a raio of $\frac{T_s}{R_c C_{gs2}} = 6.9$ results in a 0.1 percent current gain error.

### 3.3. MOSFET Mismatch Effects

From the previous discussion, it is also evident that unlike switched-capacitor circuits where the filter response is determined by capacitor ratios, the

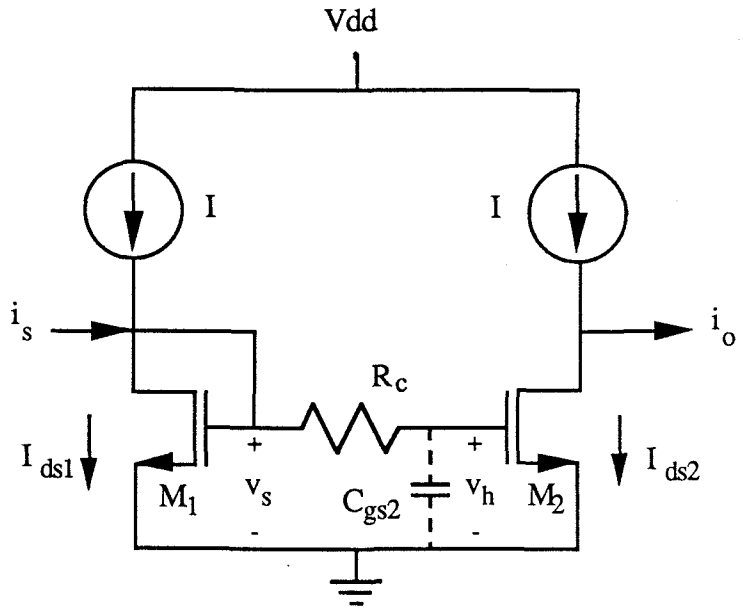



Fig. 12 Models of the SI T/H circuit with the sampling switch ON and modelled as a linear resistor, $R_c$.

accuracy of switched-current circuits depends entirely on the matching accuracy of the transistor aspect ratios.

There are several factors affecting the accuracy of the biased current mirror amplifier. Consider a MOSFET that has a size of WxL $\mu m^2$. In a square-law saturation condition, the MOSFET is approximately modeled as

$$I_d = \frac{\mu C_{ox}}{2}(\frac{W}{L})(V_{gs}-V_t)^2 = ß(V_{gs}-V_t)^2 \tag{17}$$

where $I_d$ is the drain current, $\mu$ is the effective electron mobility, $C_{ox}$ is the gate capacitance per unit area, $V_t$ is the threshold voltage, W and L are the effective width and length of the channel, ß is the conductance constant.

It has been shown that the mismatching of the conductance constants between two nominally identical MOSFETs is mainly caused by following factors [19][20][31]:

a. Mismatch due to the edge variations of the channel which is proportional to $(\frac{1}{L^2}+\frac{1}{W^2})^{1/2}$;

b. The gate oxide capacitance variation;

c. The carrier mobility variation. Due to the damage in the substrate caused by the threshold adjust implant.

In Fig. 3, assuming two MOSFETs of different conductance constant $ß_1$ and $ß_2$, but same threshold voltage $V_{t1} = V_{t2} = V_t$, their drain currents are

$$I_{d1} = ß_1(V_{gs1} - V_t)^2 \tag{18a}$$

$$I_{d2} = ß_2(V_{gs2} - V_t)^2. \tag{18b}$$

With $V_{gs1} = V_{gs2} = V_{gs}$, $ß = ß_1+ß_2$, and $\Delta ß = ß_1-ß_2$, then the difference of two drain current is

$$\Delta I = I_{d1} - I_{d2} = \Delta ß(V_{gs} - V_t)^2 = \frac{\Delta ß}{ß} I_a, \tag{19}$$

where $I_a = ß(V_{gs} - V_t)^2 = \frac{I_{d1}+I_{d2}}{2}$. From Eq. 3, we have

$$i_o = -i_s + \frac{\Delta ß}{ß} I_a = - i_s + \frac{2\Delta ß}{2ß+\Delta ß} i_s + \frac{2\Delta ß}{2ß+\Delta ß} I, \tag{20}$$

where I is the bias current. Hence, any deviation of the conductance constant ß will generate a current gain error of

$$i_{error} = \frac{2\Delta ß}{2ß+\Delta ß} i_s, \tag{21a}$$

and a current offset of

$$I_{offset} = \frac{2\Delta ß}{2ß+\Delta ß} I. \tag{21b}$$

On other hand, it had also been shown that the deviation of the threshold voltage in the MOSFET is mainly caused by:

a. The nonuniform distribution of fixed oxide charge;

b. The nonuniform distribution of depletion charge;

c. The nonuniform distribution of implanted ions; and

d. The variation of gate oxide capacitance.

It has been observed for an n-channel device with a 6μm/3μm size that the standard deviation of the threshold mismatch is about 4 to 5 mV. The threshold mismatch for p-channel devices is about 6 to 10 mv due to the additional threshold adjust implantation [31].

Assuming two MOSFETs have the same conductance constant ß, but different threshold voltages $V_{t1}$, $V_{t2}$, with $\Delta V_t = V_{t1} - V_{t2}$ and $V_{gs1} = V_{gs2} = V_{gs}$, then the drain current of $M_2$ is

$$\begin{aligned} I_{d2} &= ß(V_{gs} - V_{t2})^2 \\ &= ß(V_{gs} - V_{t1} + \Delta V_t)^2 \\ &= I_{d1} + ß\Delta V_t^2 + 2ß\Delta V_t\sqrt{\frac{I_{d1}}{ß}} \\ &= I + i_s + ß\Delta V_t^2 + 2\Delta V_t(\frac{I}{(V_{GS1}-V_{t1})})(1 + \frac{i_s}{I})^{1/2}, \end{aligned} \tag{22}$$

where $(V_{GS1}-V_{t1}) = \sqrt{\frac{I}{ß}}$ is the bias excess voltage of the current mirror. By applying the binomial expansion to the above equation, the output current is [15]

$$i_o = i_s + \beta\Delta V_t^2 + \left(\frac{2\Delta V_t I}{V_{GS}-V_{t1}}\right)\left[1+\frac{1}{2}\left(\frac{i_s}{I}\right) - \frac{1}{8}\left(\frac{i_s}{I}\right)^2 + \frac{1}{16}\left(\frac{i_s}{I}\right)^3 + \ldots\right]. \quad (23)$$

Equation (23) shows that threshold voltage mismatch generates a dc current offset of

$$I_{offset} = \beta\Delta V_t^2 + \left(\frac{2\Delta V_t I}{V_{GS}-V_{t1}}\right), \quad (24a)$$

a linear gain error of

$$i_{error} = \left(\frac{\Delta V_t}{V_{GS}-V_{t1}}\right) i_s, \quad (24b)$$

and harmonic distortion. The second and third harmonic distortion terms are

$$HD_2 \approx \frac{1}{8}\frac{\Delta V_t}{V_{GS}-V_t}\left(\frac{i_s}{I}\right) \quad (25a)$$

$$HD_3 \approx \frac{1}{16}\frac{\Delta V_t}{V_{GS}-V_t}\left(\frac{i_s}{I}\right)^2 \quad (25b)$$

and the total harmonic distortion is

$$THD = \left(HD_2^2 + HD_3^2 + \ldots\right)^{1/2} \quad (25c)$$

Fig. 13 shows the total harmonic distortion under different bias currents, and threshold voltage mismatches.

### 3.4. Frequency Response

The small-signal equivalent circuit of a simple biased current mirror amplifer with identical stages as its source and load was shown in Fig. 9. Using the small-signal model of Fig. 9(b), it can be shown that the frequency response is

$$H(s) = \frac{(g_L + sC_L)(sC_{gd2} - g_{m2})}{(g_L + sC_L + sC_{gd2})(g_{in} + sC_{gs} + sC_{gd2}) - sC_{gd2}(sC_{gd2} - g_{m2})} \quad (26)$$

where $g_{in} = g_s + g_{m1} + g_{ds1} + g_{ds3} \approx g_{m1}$, and $C_{gs} = C_{gs1} + C_{gs2} + C_s$.

After ignoring the small gate-to-drain capacitance of $M_2$, the dominant pole can be approximated as

$$\omega_c \approx \frac{g_{m2}}{C_{gs}} \quad (27)$$

Hence, the small-signal bandwidth of the current amplifier is determined by the transconductance of $M_2$ and total capacitance of input node. In the previous

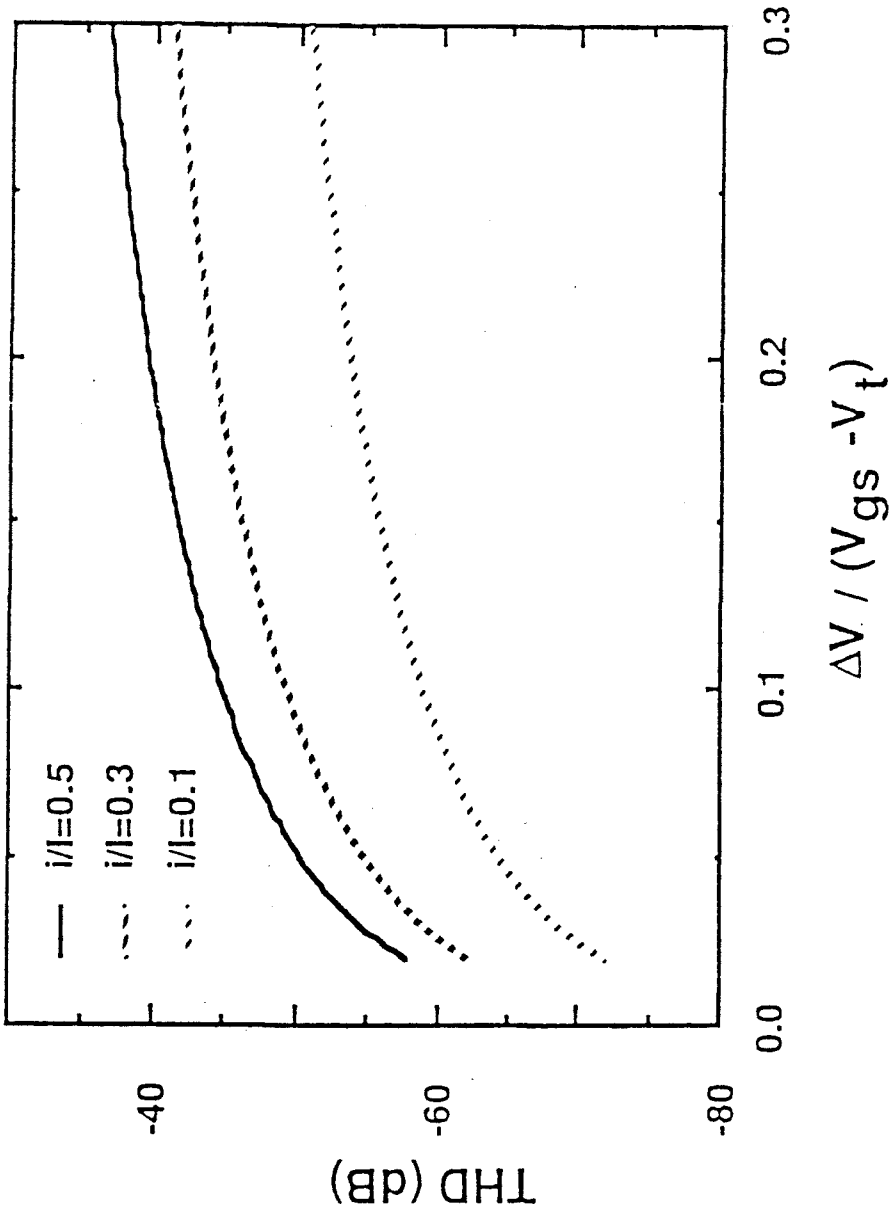



Fig. 13 Calculated total harmonic distortion of Eq. 25 under different signal current to bias current ratio.

analysis, it was stated that the matching error is inversely proportional to the device feature size. Therefore, the bandwidth of the current mirror is increased by reducing the gate capacitance, but with a decrease in accuracy. Fig. 14 shows the simulated frequency responses of two different current mirrors. Under the same bias current of 200μA, when the feature size changes from 20/2 μm to 100/10 μm, the current mirror bandwidth is reduced from about 650MHz to about 40MHz.

### 3.5. Noise and Dynamic Range

It has been shown that the two dominant noise sources in the MOSFET are the flicker noise and thermal noise [13]. Both are modeled by a single noise current generator from drain to source in the small-signal equivalent circuit as shown in Fig. 15 with a value of .

$$\bar{i}_d^2 = 4kT(\frac{2}{3}\frac{1}{g_m})\Delta f + K_f\frac{I_d^{\alpha}}{f}\Delta f, \tag{28}$$

where constants $K_f$ and $\alpha$ are process dependent, $i_d$ is the RMS noise drain current, and $g_m$ is the small-signal transconductance at the dc operating point. The flicker noise is inversely proportional to frequency and has its greatest impact at low frequencies. It can be ignored for high-frequency applications of switched-current circuits.

Based on the equivalent circuit of Fig. 15, the total output noise current of a simple current mirror can be calculated as

$$\bar{i}_{no}^2 = (\bar{i}_{d1}^2 + \bar{i}_{d3}^2)(\frac{g_{m2}}{g_{m1}})^2 + \bar{i}_{d2}^2 + \bar{i}_{d4}^2 \tag{29}$$

where $i_{d1}$, $i_{d2}$, $i_{d3}$, $i_{d4}$ are the equivalent RMS noise generators of the four MOSFETs. Assuming unity current gain for the current mirror, then $g_{m1}=g_{m2}$, and the input-referred equivalent current noise is

$$\bar{i}_{ni}^2 = \bar{i}_{no}^2 = 4kT(\frac{2}{3})\Delta f(\sum_{i=1}^{4}\frac{1}{g_{mi}}) \tag{30a}$$

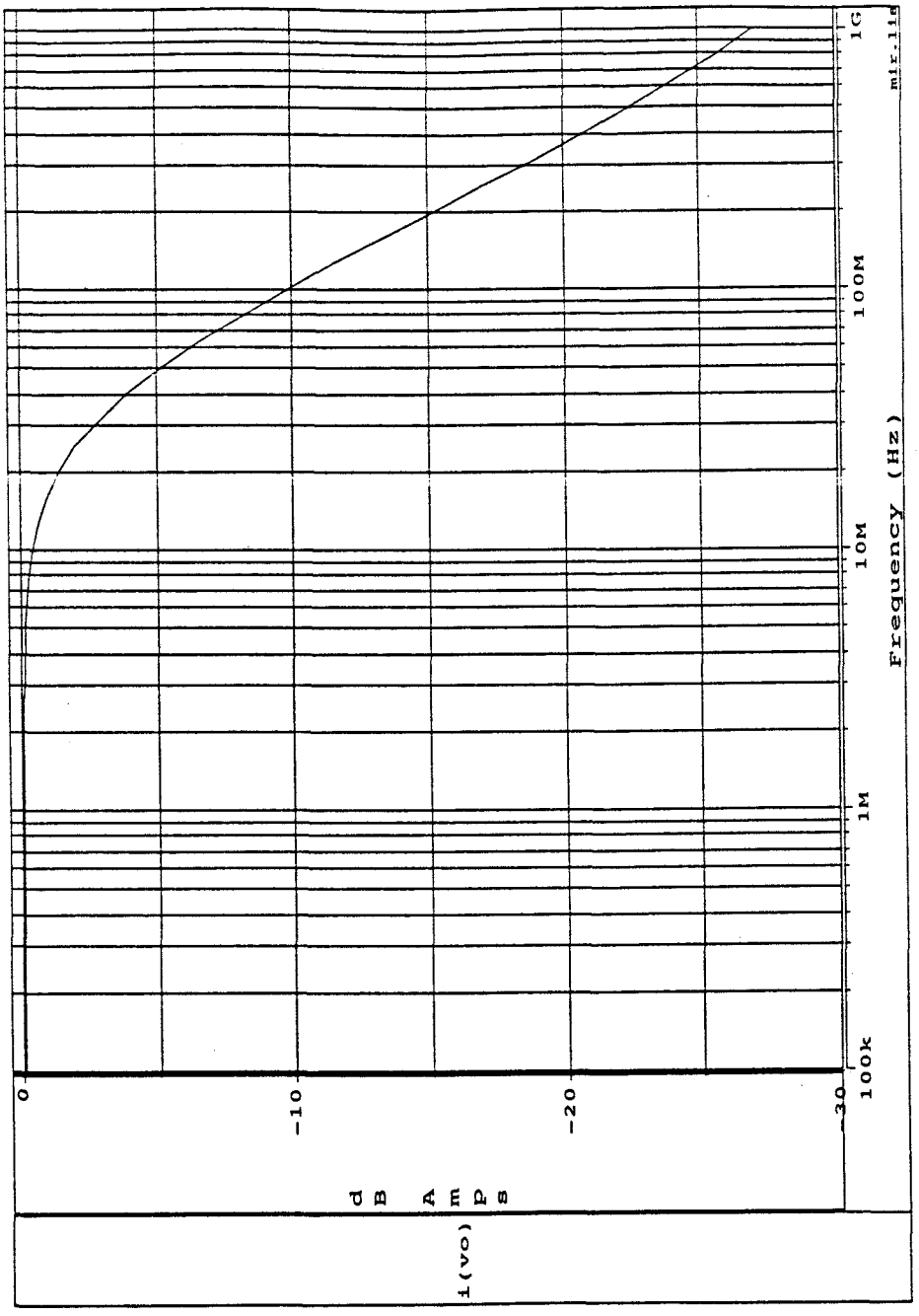



Fig. 14(a) Frequency response of simple current mirror with $(W/L)_1 = (W/L)_2 = (W/L)_3 = (W/L)_4 = 100\mu m/10\mu m$, $R_s = R_L = 0$, and bias current $I = 200\mu A$.

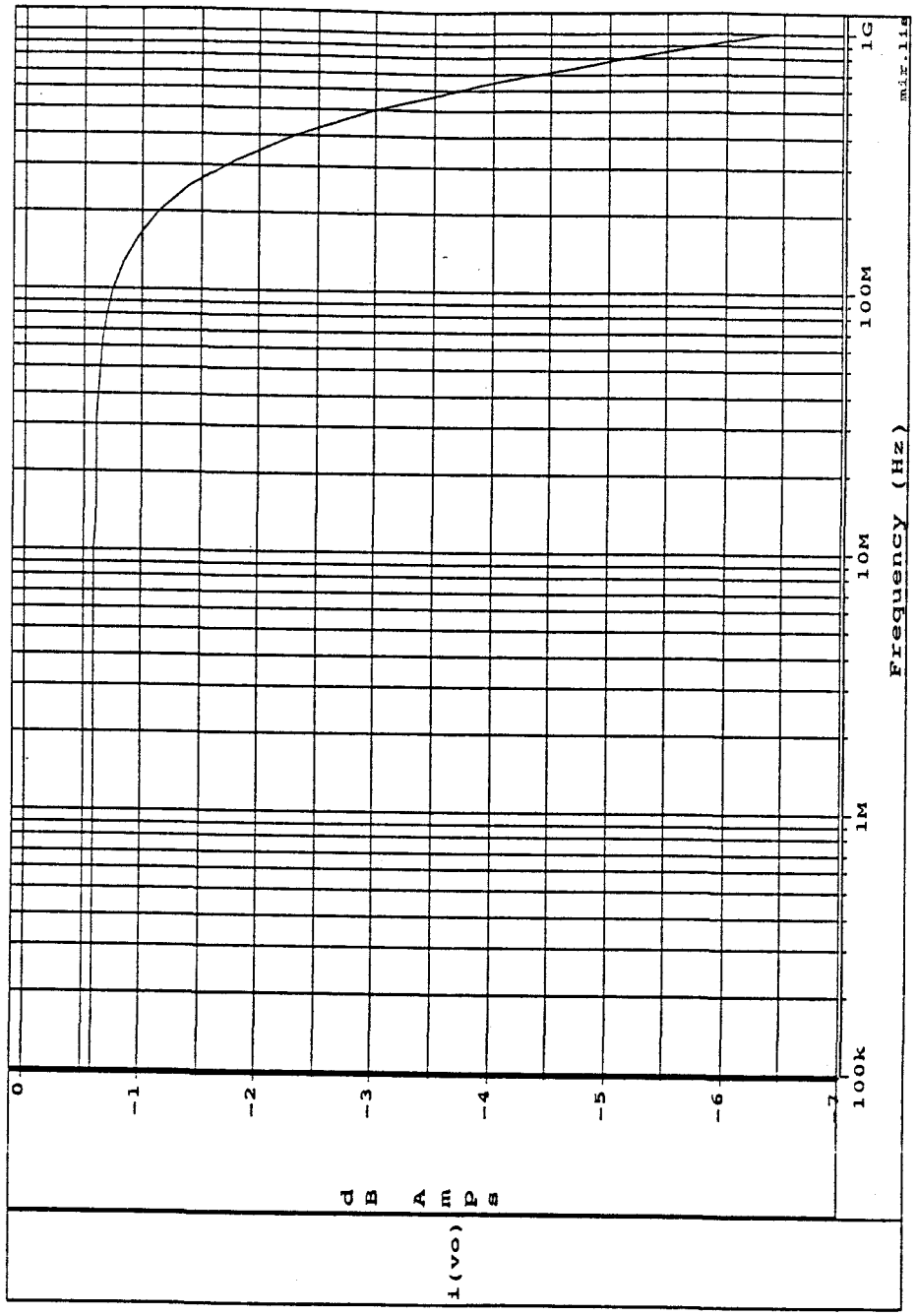



Fig. 14(b) Frequency response of simple current mirror with $(W/L)_1 = (W/L)_2 = (W/L)_3 = (W/L)_4 = 20\mu m/2\mu m$, $R_s = R_L = 0$, and bias current $I = 200\mu A$.

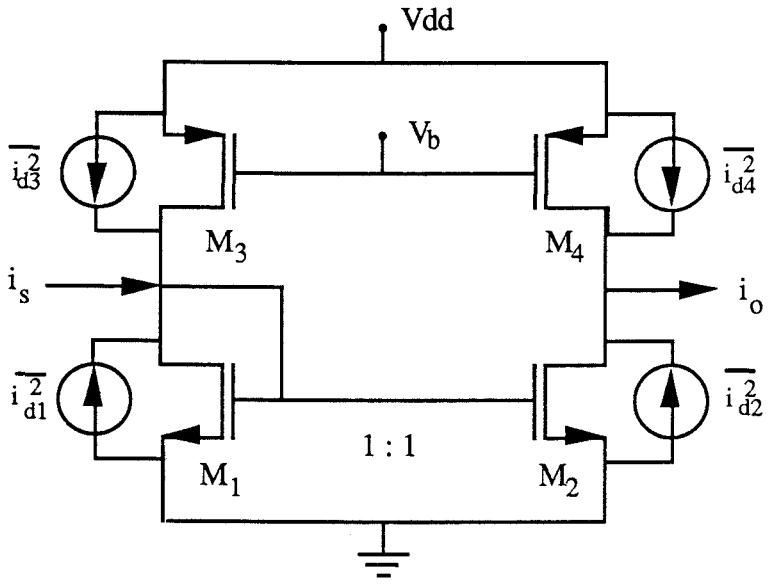



Fig. 15 Noise equivalent circuit of a simple current mirror.

For example, with the feature size W/L = 100μm/10μm, and bias current I = 200μA, then the input refereed noise spectral density is about $1.48\times10^{-16}A/\sqrt{Hz}$.

For the cascode current mirror, two MOSFETs are used in each branch. The input referred equivalent current noise is

$$\bar{i}_{ni}^2 = \bar{i}_{no}^2 = 4kT(\frac{2}{3})\Delta f(\sum_{i=1}^{8}\frac{1}{g_{mi}}) \tag{30b}$$

For the delay stage of Fig. 16(a), MOS switch $M_S$ introduces an extra noise source. Assuming the switch channel resistance is $R_{on}$, then the thermal noise power is

$$v_{ns}^2 = 4kTR_{on}\Delta f, \tag{31a}$$

which generates an output noise current of

$$\bar{i}_{nos}^2 = 4kTR_{on}g_{m2}^2\Delta f. \tag{31b}$$

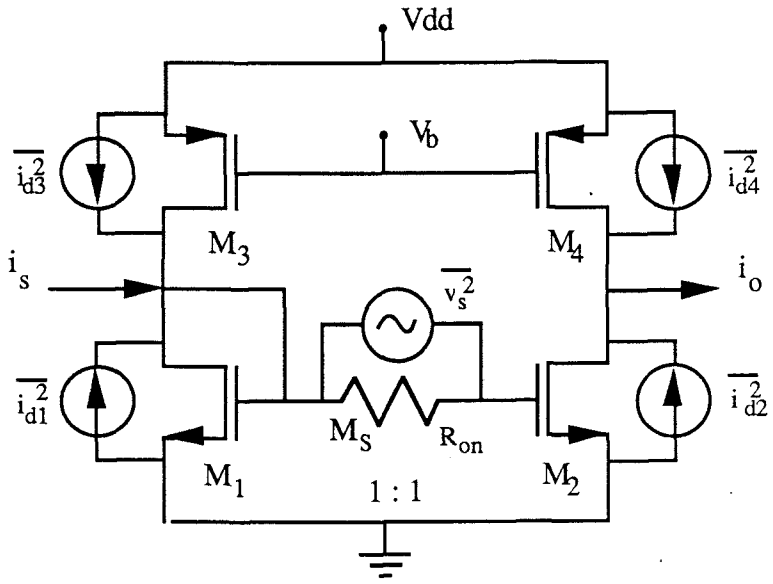
Hence, the total input-referred current noise of a simple delay stage is

$$\bar{i}_{ni}^2 = 4kT(\frac{2}{3})\Delta f(\sum_{i=1}^{4}\frac{1}{g_{mi}}) + 4kTR_{on}g_{m2}^2\Delta f, \tag{32}$$

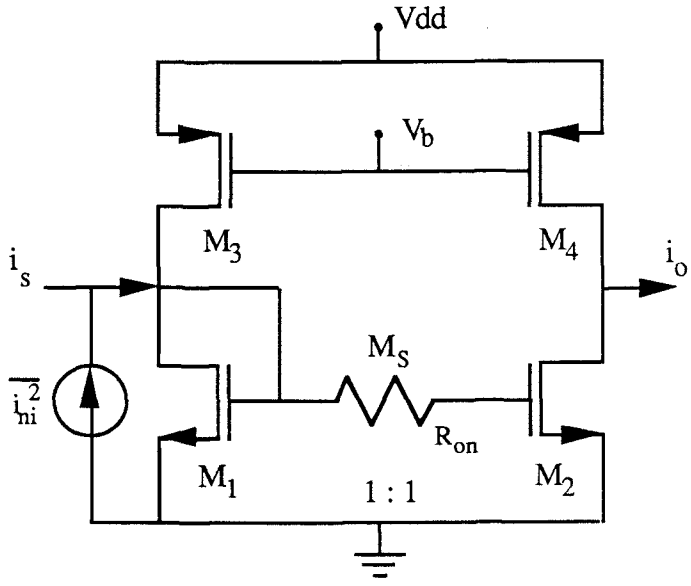
as shown in Fig. 16(b). In general, the sampling frequency must be much less than the noise bandwidth in order to avoid current gain errors caused by the finit circuit bandwidth and switch channel resistance. Because the noise generated by $M_1$ and $M_3$ is sampled by the analog switch $M_S$. After considering noise aliasing effects, the total input-referred noise spectral density is [32]

$$S_i \approx 4kT\left[(\frac{BW_n}{f_s})(\frac{4}{3})(\frac{1}{g_{m1}}+\frac{1}{g_{m3}}) + (\frac{2}{3})(\frac{1}{g_{m2}}+\frac{1}{g_{m4}})+R_{on}g_{m2}^2\right] \tag{33}$$

where $BW_n$ is the equivalent noise bandwidth, and $f_s$ is the sampling frequency. For example, at room temperature if the noise bandwidth is five times higher than the sampling frequency $f_s$, and the MOSFETs of the current mirror have W/L = 100μm/10μm, bias current I = 200μA, and the maximum channel resistance of the switch is 10KΩ, then $S_i \approx 1.48 \times 10^{-15}\ A/\sqrt{Hz}$. If the circuit equivalent noise




(a) Simple SI delay circuit with equivalent current noise sources.




(b) Simple SI delay circuit with input-referred current noise source.

Fig. 16 Noise equivalent circuit of a SI delay stage.

bandwidth is 1MHz, then the input-referred RMS noise level is approximately 1.48nA. If the maximum signal level is 100μA, then the dynamic range will be about 96dB.

## 3.6. Conclusions

In this chapter, we analyzed the basic performance of a switched-current circuit. It was shown that the nonideal input/output resistances, and MOSFET mismatches affect the accuracy of SI circuits. Although the resistance loading effects can be reduced using a cascode current mirror, the MOSFET mismatches, especially the threshold mismatch, will degrade the accuracy and cause gain errors and signal harmonic distortion. The switched-current circuits do have the advantages of high operating speed, low power supply voltages, and simpler circuitry.

# CHAPTER 4. CLOCK FEEDTHROUGH AND CANCELLATION

In the last chapter, it was shown that the difference in excess gate voltages caused by threshold mismatches is one of the major causes of harmonic distortion in switched-current circuits. Unfortunately, there is another large error source which also contributes to this excess gate voltage difference; namely, the clock feedthrough effect. In this chapter, the clock feedthrough effect is analyzed, and a newly developed clock feedthrough cancellation technique is discussed.

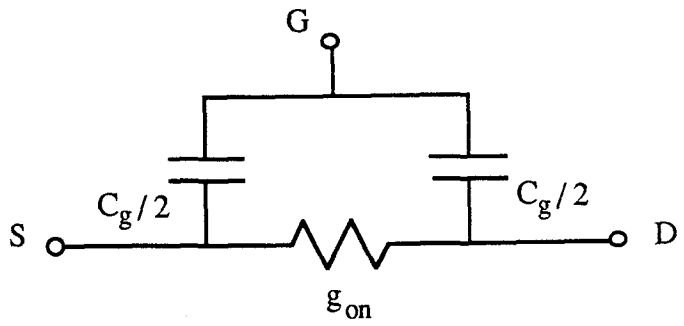
## 4.1. Clock Feedthrough Analysis

Clock feedthrough or charge injection is a common problem for all sample-and-hold circuits, and has therefore been investigated by many researchers. Vittoz and Sheu developed the lumped RC-model [30][41]. Kuo and Van Peteghem introduced distributed RC circuits to model the fast turnoff mode of the switch [38], and Kuo also included the charge pumping effects occuring when the gate voltage falls very quickly [17][18].

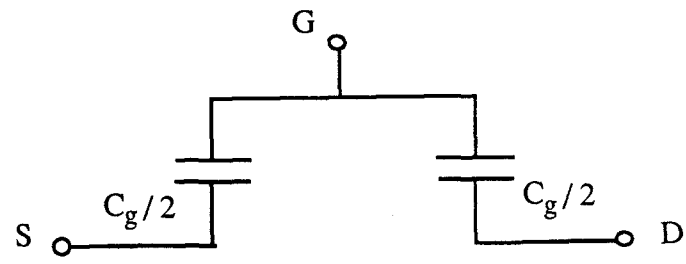
Due to the limitations of circuit bandwidth in switched-current circuit applications, the gate voltage of the analog switch changes much slower than the intrinsic carrier transit time in the transistor. According to the previous work, the analog switch of the sample-and-hold circuit can be described by the lumped RC model as shown in Fig. 17(a) for the ON state and Fig. 17(b) for the OFF state.

For the simple S/H configuration shown in Fig. 18, the gate voltage is assumed to change linearly with time and is expressed as

$$V_g(t) = \begin{cases} V_H & \text{for } t < 0 \\ V_H - \alpha t & \text{for } 0 \le t \le t_f \\ V_L & \text{for } t > t_f \end{cases} \qquad (34)$$




(a) ON state with $g_{on}$ as channel conductance, $C_g$ as gate capacitance and $C_g = 2C_{ovl} + C_{ox}W_{eff}L_{eff}$.




(b) OFF state with $C_g$ as gate capacitance and $C_g = 2C_{ovl}$.

Fig. 17 Lumped RC-model of clock feedthrough

where $t_f$ is the fall time from the high level $V_H$ to the low level $V_L$ of the gate voltage, and $\alpha$ is the slope of the sampling pulse of period T.

When $V_g(t) - V_s > V_T$, the analog switch has a conductive channel with

$$g(t) = ß(V_g(t) - V_s - V_T) \tag{35}$$

where $ß = \mu_n C_{ox} \frac{W_{eff}}{L_{eff}}$ .is the conductance constant of MOSFET. During the decrease of the gate voltage, the transistor model of the analog switch is changed from the conductive phase of Fig. 17(a) to the nonconductive phase of Fig. 17(b). For the simple track-and-hold circuit shown in Fig. 18, assume that the error voltages $v_d$ and $v_s$ introduced by the clock feedthrough remain small compared to the swing of the gate voltage $V_H - V_L$. Then the charge injection can be expressed by two current sources injecting into the drain and source nodes, each of value

$$i_{inj} = C_g \frac{dV_g}{dt} = - \alpha C_g. \tag{36}$$

During the conductive phase,

$$C_g = 2C_{ovl} + C_{ox} W_{eff} L_{eff} \tag{37}$$

And during the nonconductive phase,

$$C_g = 2C_{ovl} \tag{38}$$

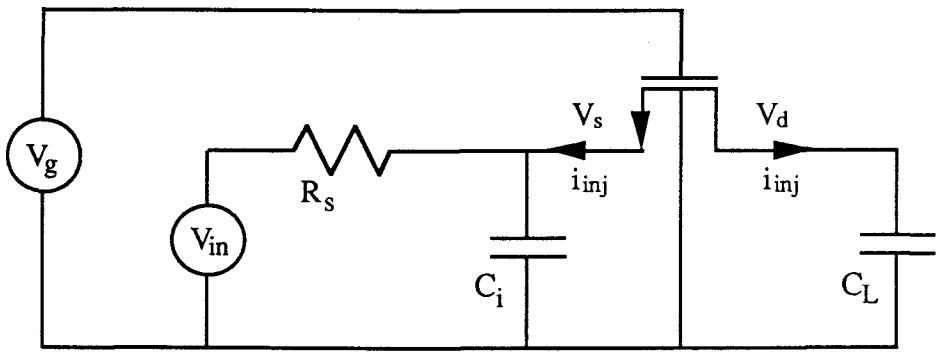
Where $C_{ovl}$ is the overlap capacitance between gate and drain or source of the analog switch.

Based on above assumptions, the error voltage of clock feedthrough can be described by the following differential equations:

$$\frac{\partial v_s}{\partial t} C_i = g(t)(v_d - v_s) - \frac{v_s}{R_s} + i_{inj} \tag{39a}$$

$$\frac{\partial v_d}{\partial t} C_L = g(t)(v_s - v_d) + i_{inj} \tag{39b}$$

By solving two equations above, the clock feedthrough voltage on the hold capacitance can be determined. It has been shown that the clock feedthrough error




$i_{inj} = C_g \frac{dV_g}{dt}$ is the injection current of clock feedthrough,

$V_d$ and $V_s$ are clock feedthrough error voltages.

Fig. 18 Simple model of SI track-and-hold circuit.

voltage has a typical magnitude of 1 to 20mV, depending on the value of loading capacitance. Fig. 19 shows the effect of clock feedthrough on the output current signal of a delay stage. Combining the clock feedthrough and threshold voltage mismatch term together, the total gate voltage error during the holding period in a switched-current delay stage is

$$\Delta V_e = \Delta V_t + V_{cf} \tag{40}$$

where $\Delta V_t$ is contributed by the threshold mismatch, and $V_{cf} = v_d(t_f)$ is contributed by the clock feedthrough. Equation (23) can now be rewritten as

$$i_o = i_s + \beta \Delta V_e^2 + \left(\frac{2\Delta V_e I}{V_{GS}-V_{t1}}\right)\left[1 + \frac{1}{2}\left(\frac{i_s}{I}\right) - \frac{1}{8}\left(\frac{i_s}{I}\right)^2 + \frac{1}{16}\left(\frac{i_s}{I}\right)^3 + \ldots\right] \tag{41}$$

From (41), the constant current offset is

$$I_{offset} = \beta \Delta V_e^2 + \left(\frac{2\Delta V_e I}{V_{GS}-V_{t1}}\right) \tag{42a}$$

and the gain error is

$$i_{error} = \frac{\Delta V_e}{V_{GS}-V_{t1}}\, i_s. \tag{42b}$$

So the current offset, gain error and harmonic distortion are all increased proportionally due to the gate voltage error introduced by clock feedthrough. For example, assuming bias current I = 100 μA, (W/L) = 10, $V_{GS}-V_{t1}$ = 1 Volt, an error voltage $\Delta V_e$ = 10 mV, will generate offset current of 2 μA, and gain error of one percent.

## 4.2. Clock Feedthrough Cancellation

From the previous analysis, it is obvious that the clock feedthrough voltage depends on many different factors such as the source impedance, load impedance, transconductance of the switch, gate voltage slope, source voltage, etc, and most of them are very difficult to precisely control. In conventional voltage-mode circuits, previous cancellation techniques were developed by trying to separate the clock

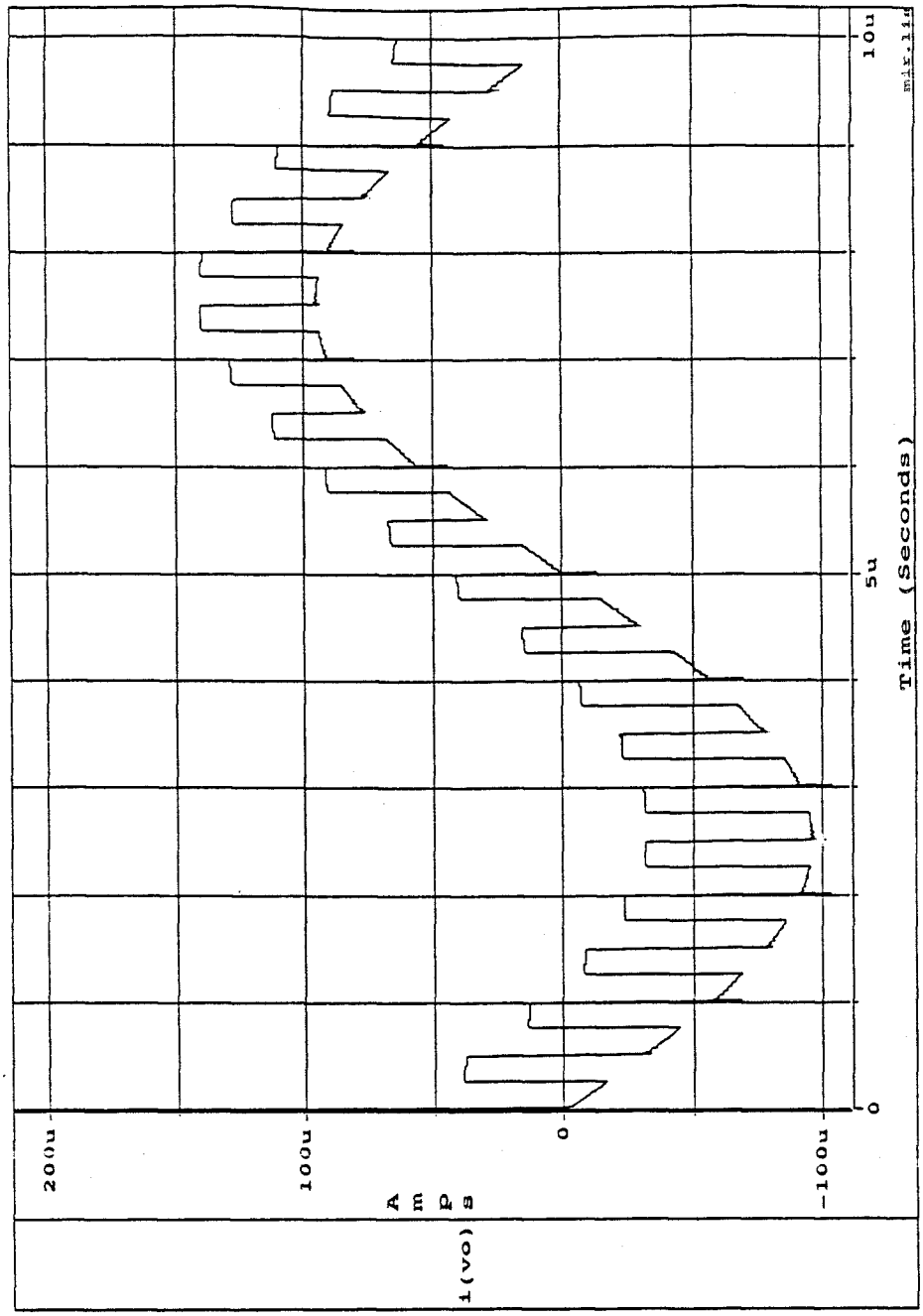



Fig. 19 Clock feedthrough effect on the output current signal of a SI delay stage with $(W/L)_1 = (W/L)_2 = (W/L)_3 = (W/L)_4 = 100\mu m/10\mu m$, and MOS switch $(W/L)_s = 6\mu m/2\mu m$, $R_s = R_L = 0$, and bias current $I = 100\mu A$.

feedthrough voltage from the signal voltage. For example, in the dummy switch technique [18], an extra switch is added which is controlled by an opposite polarity clock. The dummy switch turns on while the analog switch is turning off. This technique requires two critically-timed clock phases, and its accuracy depends strongly on interactions between the two clock phase edges which are very difficult to control. In switched-current circuits, it has been shown that by using identical circuit cells, the signal-independent current offset caused by clock feedthrough can be cancelled [11]. In this section, a new circuit is presented to cancel the signal-dependent components in the output current signal.

The newly-developed clock feedthrough cancelation circuit is shown in Fig. 20. The sources of two identical MOS switches $M_{s1}$ and $M_{s2}$ are connected to the same input node, and their gates are controlled by the same clock signal. Two switches have identical gate and source voltages and identical gate capacitances but different loading capacitance by connecting to MOSFETs of different size. Because the clock feedthrough voltage depends on the loading capacitance, two different clock feedthrough voltage will be generated on the gates of $M_2$ and $M_3$ which will cause different error components in the output current signals. By subtracting two different output current signals, the clock-feedthrough error components are canceled.

Assuming $M_2$, $M_3$ have the same channel length but different width so that

$$\frac{(W/L)_3}{(W/L)_2} = r \tag{44}$$

where r is a constant. Then the transconductance constants $M_2$ and $M_3$ are similarly related

$$ß_3 = r\, ß_2, \tag{45}$$

and the gate capacitances of $M_2$ and $M_3$ are related as

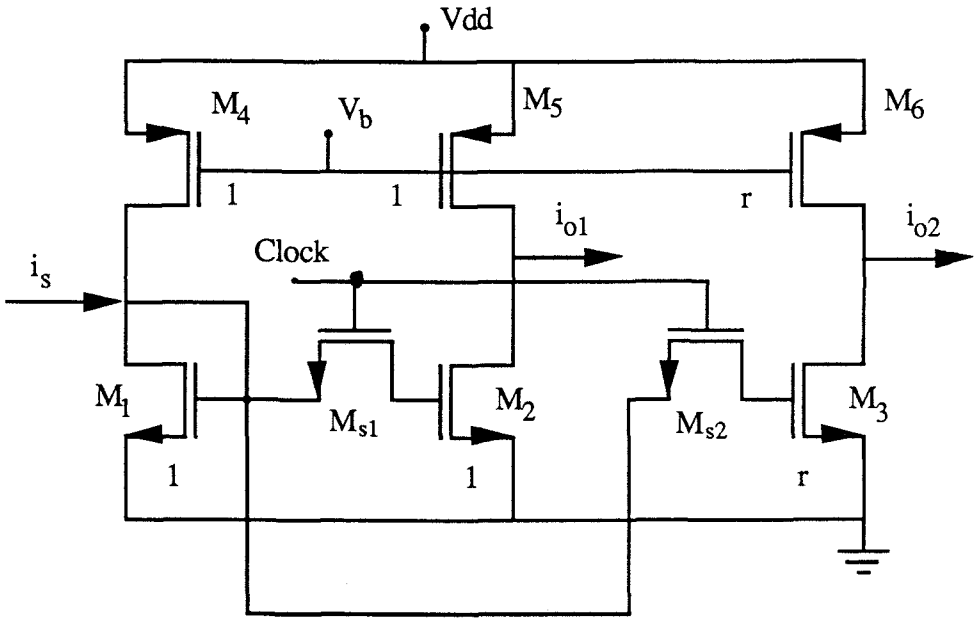



Fig. 20 Simple SI track-and-hold circuit incorporating new clock feedthrough cancellation technique.

$$C_{g3} \approx rC_{g2}. \tag{46}$$

Furthermore, assuming $V_{cf2}$ and $V_{cf2}$ are the clock feedthrough voltages on the gates of $M_2$ and $M_3$ respectively, because of the different loading capacitance, it can be approximated that

$$V_{cf2} = rV_{cf3} \tag{47}$$

The drain current of $M_2$ is

$$I_{ds2} = ß_2(V_{gs2} - V_{t2} - V_{cf2})^2. \tag{48}$$

Assuming $M_1$ and $M_2$ match, $ß_2 = ß_1$, and $V_{t1} = V_{t2} = V_{t3}$, then

$$I_{ds2} = I_{ds1} - 2ß_2(V_{gs1} - V_{t1})V_{cf2} + ß_2V_{cf2}^2 \tag{49}$$

and output current signal is

$$i_{o1} = i_s - 2ß_2(V_{gs1} - V_{t1})V_{cf2} + ß_2V_{cf2}^2. \tag{50}$$

Similarly since $V_{gs1} = V_{gs3}$, the drain current of $M_3$ is given by

$$I_{ds3} = ß_3(V_{gs1} - V_{t3} - V_{cf3})^2. \tag{51}$$

From (46), $ß_3 = rß_1$

$$I_{ds3} = rI_{ds1} - 2rß_2(V_{gs1} - V_{t1})V_{cf3} + rß_2V_{cf3}^2 \tag{52}$$

and output current signal is

$$\begin{aligned} i_{o2} &= ri_s - 2rß_2(V_{gs1} - V_{t1})V_{cf3} + rß_2V_{cf3}^2. \\ &= ri_s - 2rß(V_{gs1} - V_T)\frac{V_{cf2}}{r} + rß(\frac{V_{cf2}}{r})^2. \end{aligned} \tag{53}$$

Subtract equations (49) and (53), the final output current is

$$\begin{aligned} i_{out} &= i_{o1} - i_{o2} \\ &= (1 - r)\, i_s - \left(1 - \frac{1}{r}\right) ß_2V_{cf2}^2 \end{aligned} \tag{54}$$

For example, if r = 2, then

$$i_{out} = - i_s - \frac{1}{2} KV_{cf2}^2. \tag{55}$$

Hence, the harmonic distortion and gain error components of the output current signal are cancelled. The clock feedthrough only generates a current offset

$$I_{offset} = -\left(1 - \frac{1}{r}\right) \beta V_{cf2}^{2}. \quad (56)$$

And if the clock feedthrough voltage $V_{cf2}$ is constant, this constant current offset will not affect circuit performance.

But when input current signal levels varies, MOSFET $M_1$ has varying gate voltages. Therefore for a constant sampling clock voltage, the gate-to-source voltage of the analog switches is signal dependent. From Eq. (39), the clock feedthrough voltage $V_{cf2}$ is dependent on the transconductance of the switch. Hence last term of Eq. (55) is signal dependent. To avoid the signal-dependent current offset, an adaptive clock technique is developed as shown in Fig. 21. Two additional source followers are used to track the gate voltage of $M_1$. But the PMOS source follower shifts signal voltage up about two volts, and the NMOS source follower shifts the signal voltage down about one volt. And these two signals are used as clock high and low levels respectively to control two analog switches $M_{s1}$ and $M_{s2}$ as shown in Fig. 22. Because both high and low levels of the clock signal are tracking the gate voltage of $M_1$, the transconductances of both switches are kept constant with respect to input signal variations. Therefore the clock feedthrough is independent of input signal, and only a constant current offset is generated after above cancellation circuit. Simulation results have shown that by using the adaptive clock feedthrough

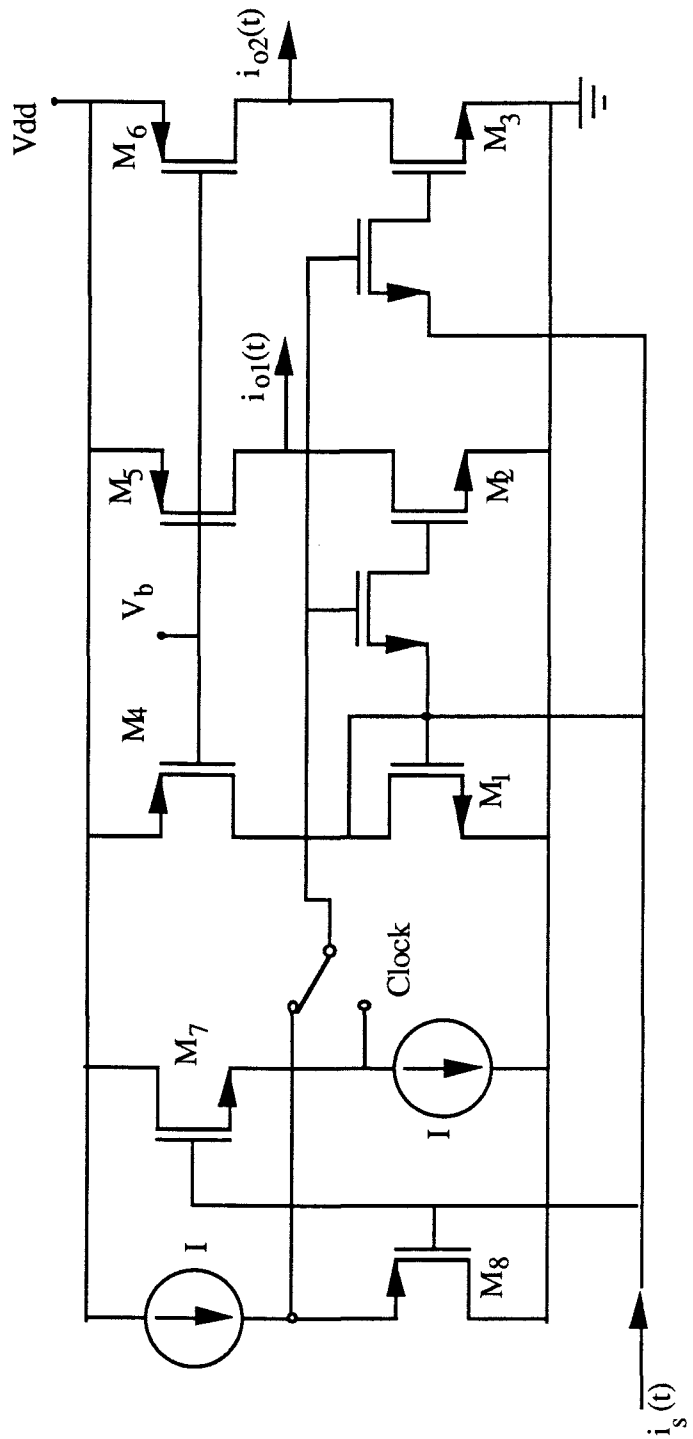



Fig. 21 Simple SI track-and-hold circuit incorporating adaptive clock feedthrough cancellation circuit

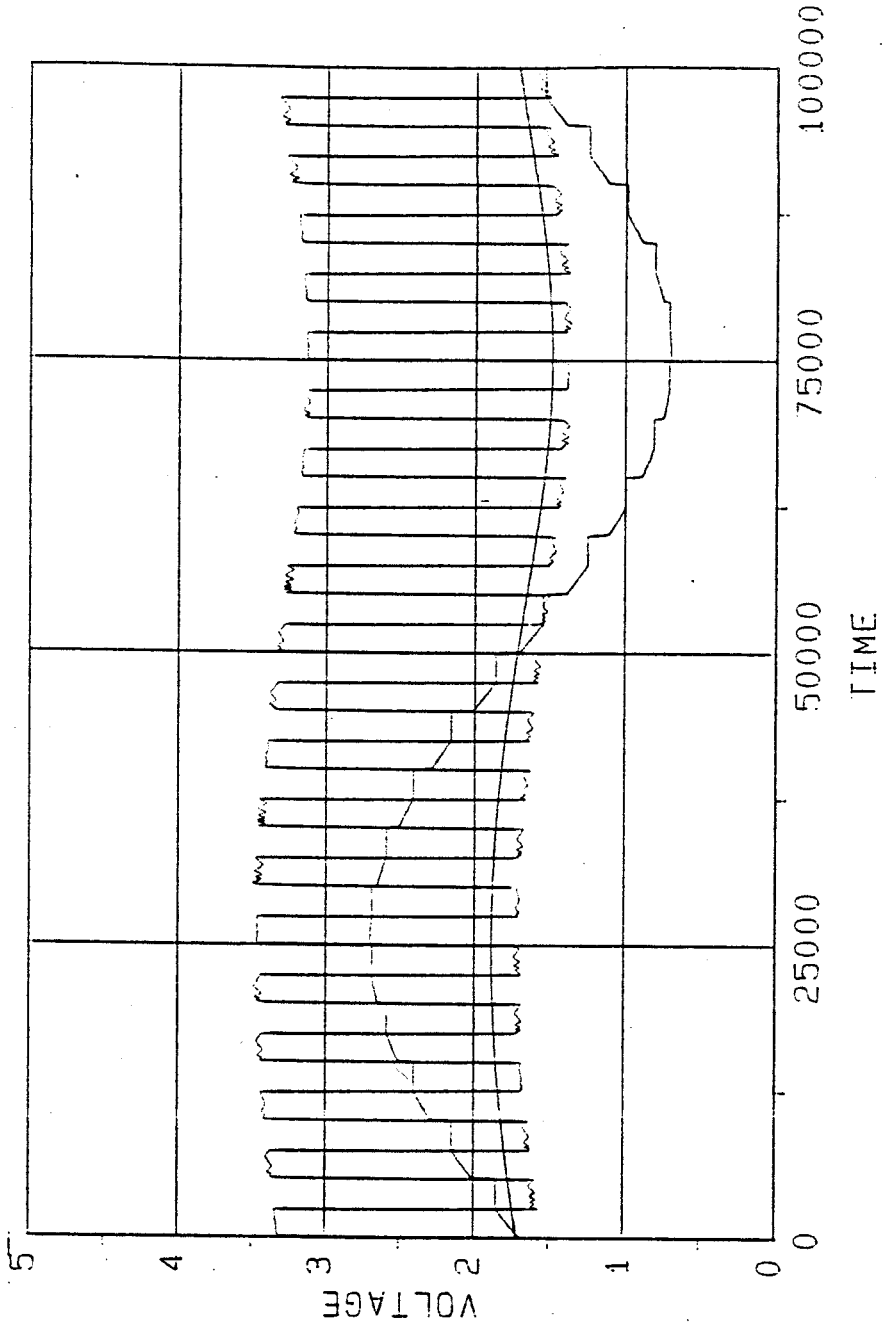



Fig. 22 Signal waveforms of adaptive clock feedthrough cancellation circuit.

cancelation circuit with a delay stage of size of W/L = 20μm/2μm, the total harmonic distortion is reduced from over 10 percent to less than 0.5 percent. Fig. 22 also shows the output current signal waveforms after adaptive clock feedthrough cancellation.

# CHAPTER 5. SWITCHED-CURRENT FILTER DESIGN AND SOME EXPERIMENTAL RESULTS

The conventional approach to switched-current filter synthesis is directly leveraged from switched-capacitor synthesis techniques. It is based on a classic double-terminated LC filter prototype and signal flowgraph techniques. It has the advantage of being directly analogous to existing switched-capacitor circuits. But it has been shown that the unique properties of conventional switched-current circuits limit filter performance [15]. On the other hand, from the previous section it is evident that switched-current circuits have similar functional blocks to that of digital filters. Thus, the synthesis of switched-current filters can also be directly analogous to digital filters, and, many design techniques developed for digital filters can be directly applied to switched-current filter design. In this section, the synthesis of different switched-current digital filters is presented, and the effects of linear gain errors on the filter frequency response are discussed.

## 5.1. Switched-Current Doubly-Terminated Ladder Filter

It has been shown that a passive doubly-terminated LC ladder filter can achieve very low sensitivity to component variations in the passband response [8][9][40]. Many switched-capacitor filters are constructed based on LC ladder filter prototypes. The basic building block is the switched-capacitor differential integrator shown in Fig. 23. Assuming an ideal operational amplifier, its output (sampled on CLK 1) can be expressed as

$$v_{out}(z) = \left(\frac{C_u}{C_I}\right)\frac{(v_1 z^{-1} - v_2 z^{-1/2})}{(1 - z^{-1})}. \qquad (57)$$

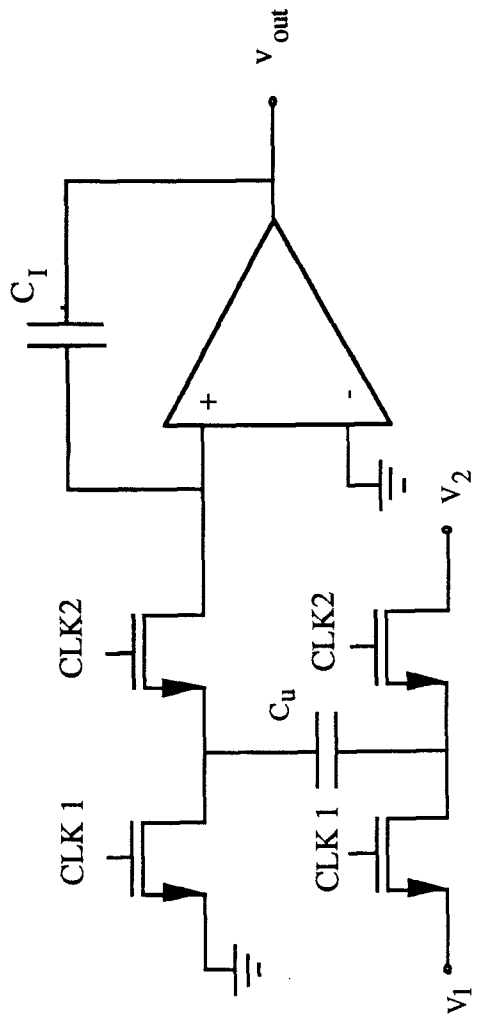



Fig. 23 Switched-capacitor differential integrator.

By using the building blocks discussed previously, an analagous switched-current integrator can also be constructed as shown in Fig. 24. Its output signal sampled on CLK 1 is

$$i_{out}(z) = A\frac{(i_1 z^{-1} - i_2 z^{-1/2})}{(1 - z^{-1})} \tag{58}$$

It is evident that two circuits above have one-to-one correspondence with

$$A = \frac{C_u}{C_I} \tag{59}$$

Therefore by selecting the proper scaling factor A, a switched-capacitor filter can be transformed directly to a switched-current filter. One major difference is that in switched-capacitor circuits only one output node is required, while each input requires a sampling/summing capacitor. In switched-current circuits, the signal summation function is performed by a direct connection of all input current signals to the input node, but each output requires a unique output stage because only one current signal can flow to one destination.

The above switched-current integrator can be used directly to synthesize ladder filters using a modified signal flowgraph method [6]. But it has been shown that due to the limited matching accuracy and more importantly, the clock feedthrough effects of the MOSFET T/H switches, the switched-current technique is unlikely equal the impressive accuracy of switched-capacitor circuits at low frequencies [15].

## 5.2. Switched-Current Digital Filter

It is well known that inversion, addition, multiplication and delay are the basic operations required in digital signal processing techniques. From the previous discussion, we see that switched-current circuits can perform similar operations for analog sampled-data signals. Thus, many existing digital signal processing

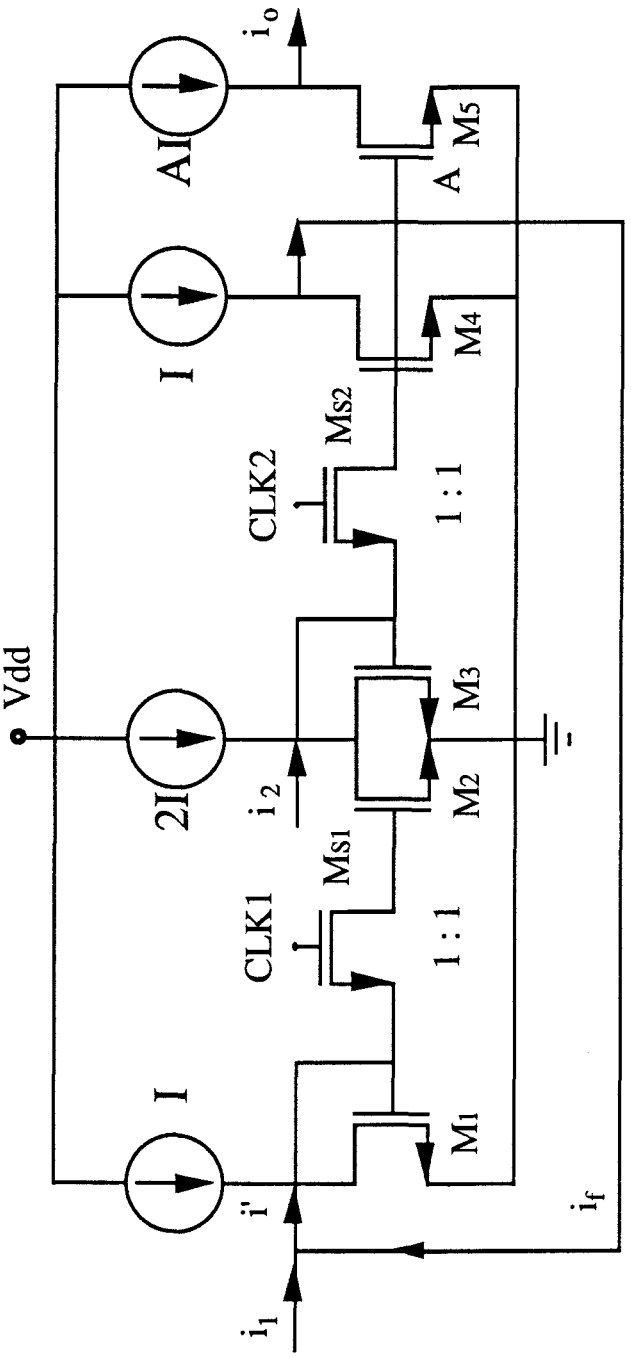



Fig. 24 First-generation switched-current integrator.

techniques can be directly applied to switched-current circuit design. In this section, different types of switched-current filters are designed based on the same techniques developed for digital filter design.

The simplest digital filter is the Finite-Impuse-Response (FIR) filter. It consists of a number of delay stages determined by the order of the filter. The output of each delay stage is appropriately weighted, and all weighted signals are summed together to produce the final output of the FIR filter.

Based on the same structure as the digital filter, the direct-form switched-current FIR filter can be configured as shown in Fig. 25. The input current signal passes through a chain of delay stages. Two identical copies of the current signal are generated by each delay stage. One copy is fed to next delay stage, and the other is forwarded to its scaling stage where it is multiplied by an appropriate weighting coefficient, $h_k$ (k=0,1,2,... N). Finally, all weighted current signals are then summed in a simple wired-OR fashion to yield the overall output. The frequency response of the FIR filter is given by

$$H(f) = \sum_{k=0}^{N} h_k e^{-j2\pi kf/N}. \tag{60}$$

In the above FIR filter, the two output delay stage can be implemented using the circuit shown in Fig. 26. It consists of a cascade of two simple half delay stages driven by two non-overlapping clocks. For the entire filter, all delay stages sample the input current signal during CLK 1 are store a corresponding voltage on the gate capacitance of $M_2$. During CLK 2, all delay stages produce output currents which are multiplied by the appropriate coefficients in scaling stages, and finally summed together to generate the output of the filter. Usually, a relatively high scaling ratio is required to implement the different weighting coefficients, but the ratio that is

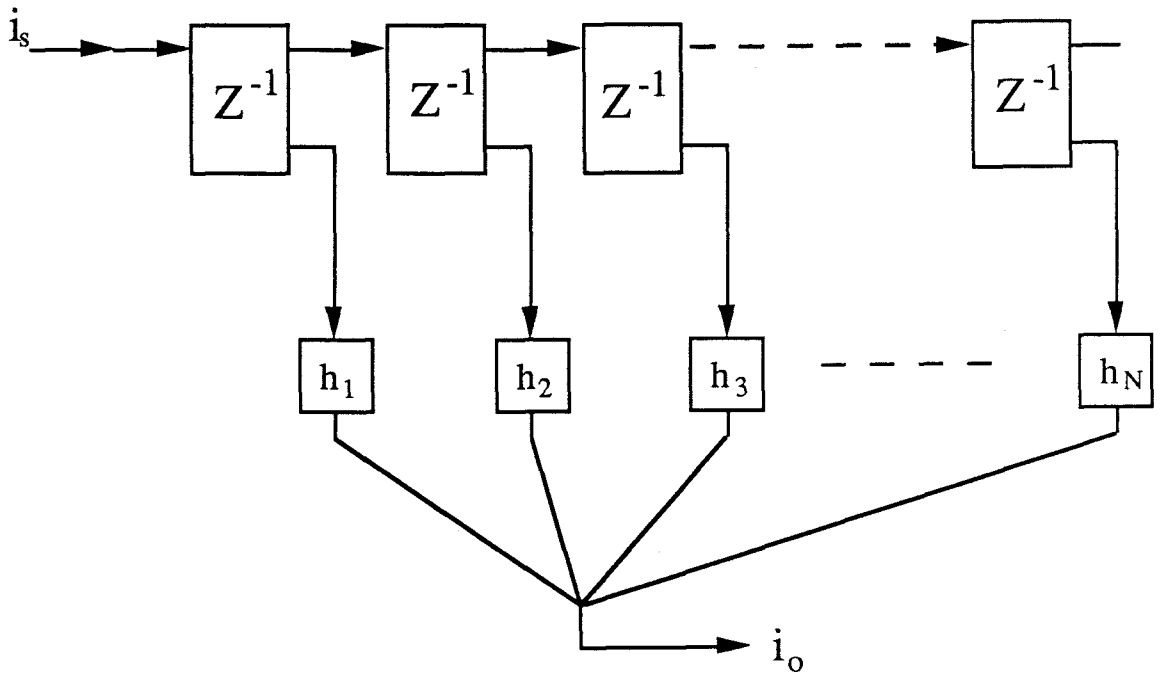



Fig. 25 Block diagram of an Nth order switched-current FIR filter.

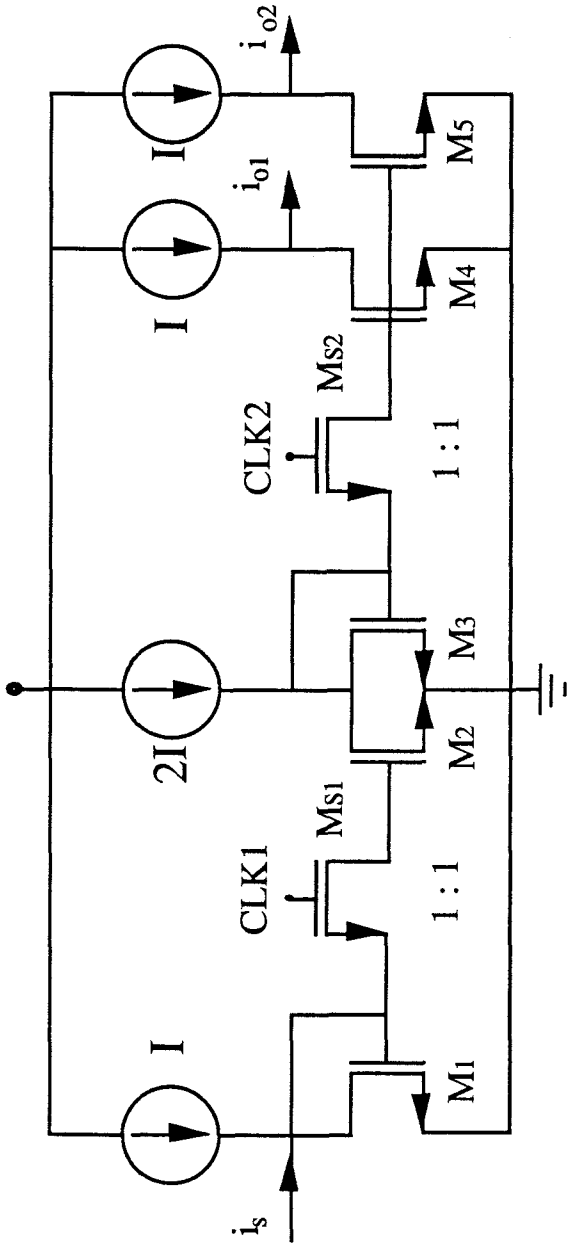



Fig. 26. The full delay stage of switched-current filter with two unity-gain outputs.

accurately achieved by a single scaling stage is limited by the resolution of the layout and the size of MOSFETs. To implement a high scaling ratio, several scaling stages can be cascaded together as shown in Fig. 27. For a cascade of N stages, the total scaling ratio is

$$K = (-1)^n K_1 K_2 ... K_n \tag{61}$$

In the special case where the scaling circuitry is binary-weighted, then the scaling ratio can be digitally programmed as shown in Fig. 28. In this example, there are 8 possible scaling ratios that can be selected by controlling the switches $a_0$, $a_1$ and $a_2$. The total scaling ratio is

$$K = - (2^{-1}a_2 + 2^{-2}a_1 + 2^{-3}a_0) \tag{62}$$

where $a_i$ =1 when the switch is on, and $a_i$ = 0 when the switch is off. A programmable switched-current filter can be easily implemented using the programmable scaling stage [42].

By using similar techniques, other types of digital filters can also be implemented with switched-current circuits. Fig. 29 shows a direct-form realization of a switched-current Infinite Impulse Response (IIR) filter. An extra input stage is required because the feedback and the input must be added to generate the output signal. This input stage can be implemented by either a current inverter or a delay stage. The frequency response of the IIR filter is

$$H(f) = \frac{1}{\sum_{k=0}^{N} a_k e^{-j2\pi kf/N}}. \tag{63}$$

Fig. 30 shows a direct-form implementation of a switched-current Auto-Recurssive and Moving Average (ARMA) filter. Hence, each delay stage requires three identical outputs for the feedforward and feedback signal paths, and the input to the next delay stage. Its frequency response is given by

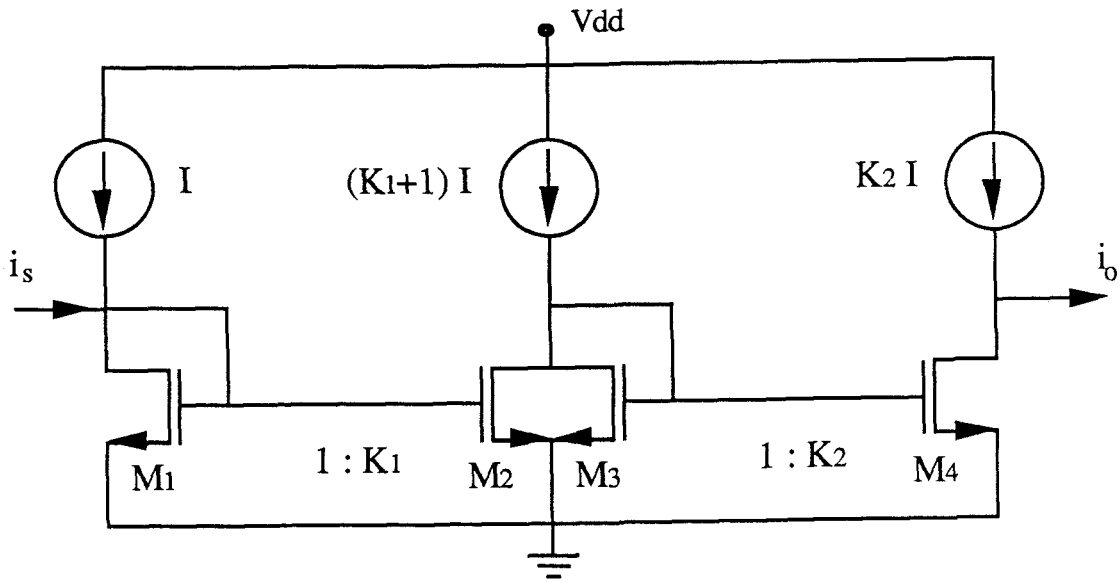



Fig. 27 Cascaded current signal scaling stage with overall current gain of $K_1K_2$.

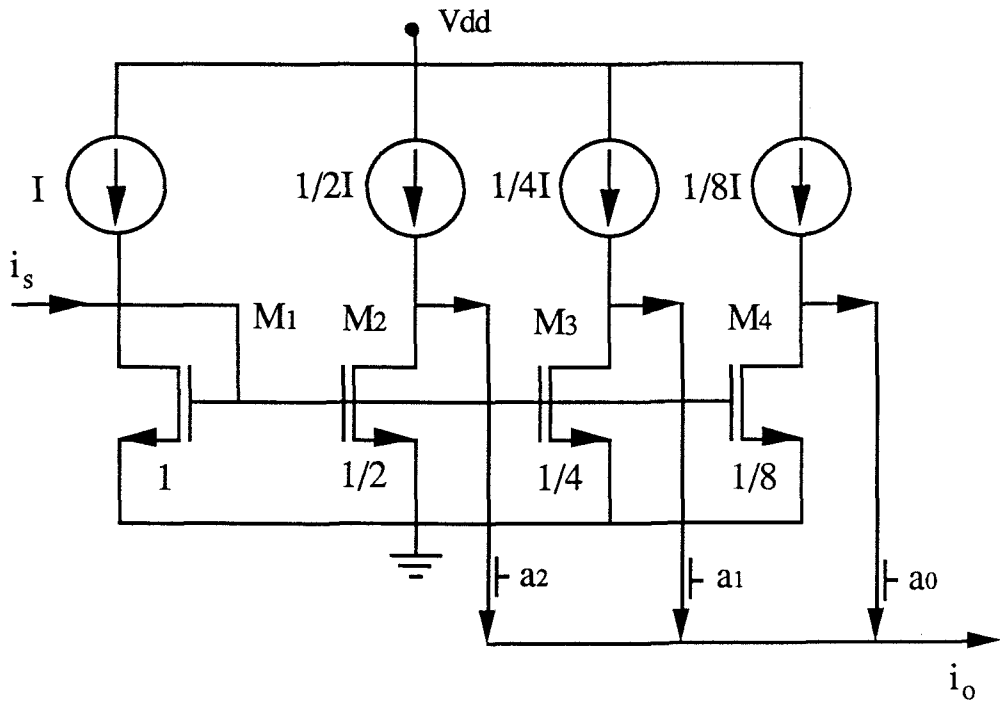



Fig. 28 Digitally-programmable binary-weighted scaling stage with symbols of $a_0$ - $a_2$ represent ideal MOS switches.

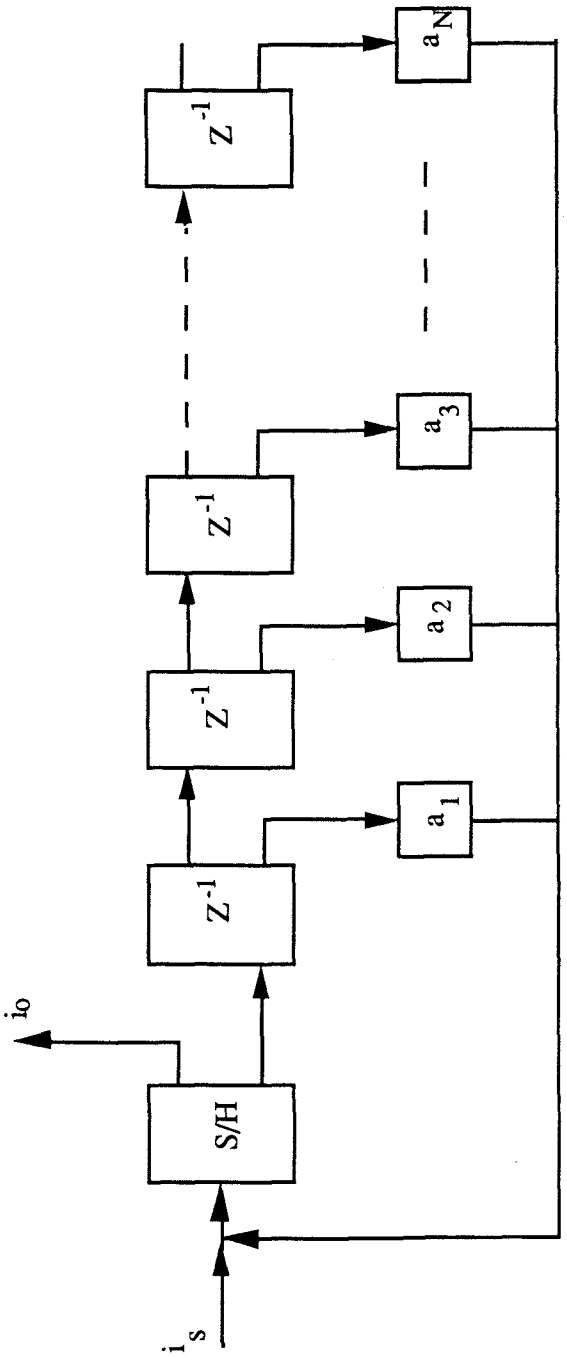



Fig. 29 Switched-current implementation of a direct form IIR filter.

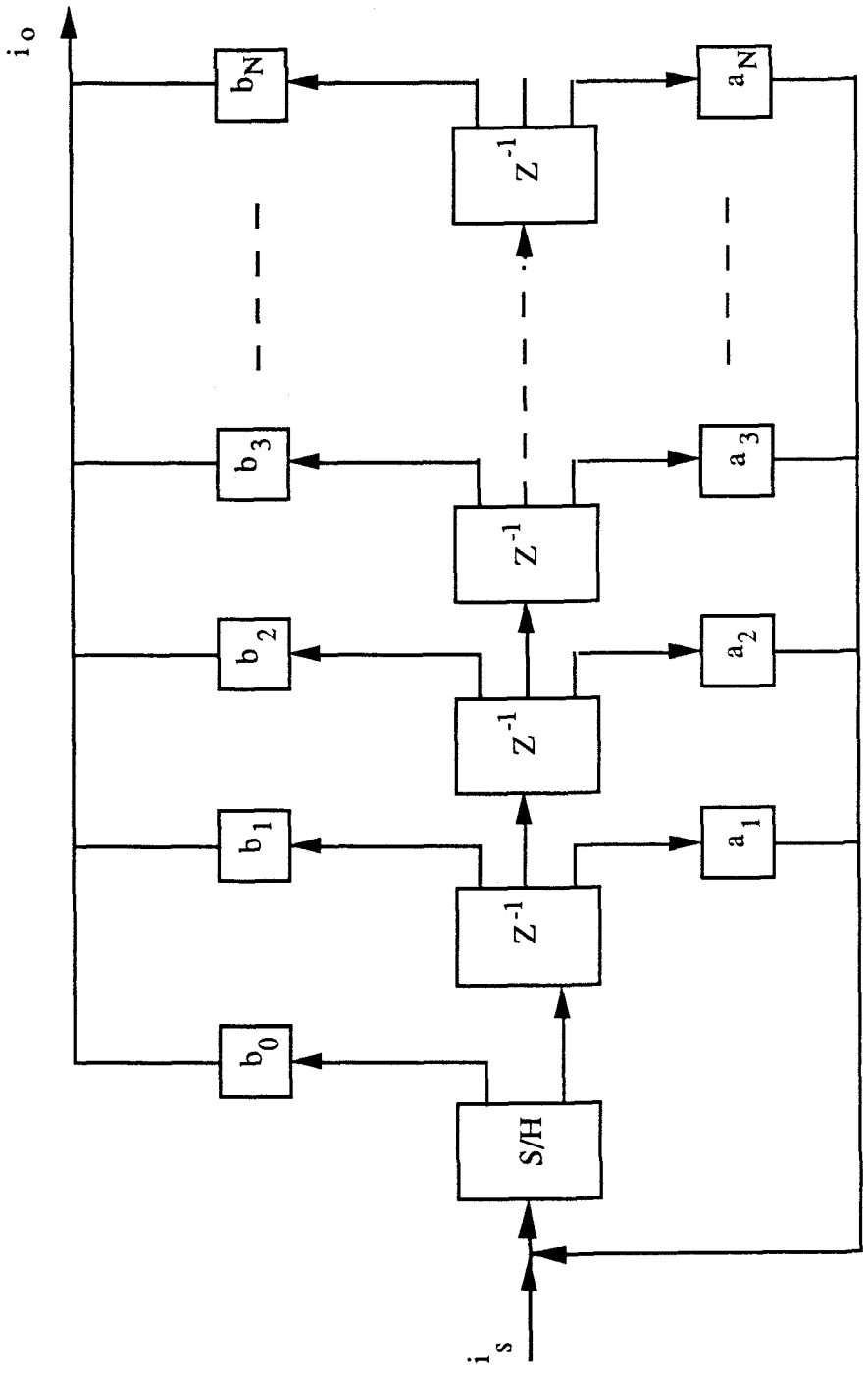



Fig. 30 Switched-current implementation of an ARMA filter.

$$H(f) = \frac{\sum_{k=0}^{N} b_k e^{-j2\pi kf/N}}{\sum_{k=0}^{N} a_k e^{-j2\pi kf/N}}. \tag{64}$$

## 5.3. Nonideal Factors and Experimental Results

The frequency response accuracy of a switched-current filter is mostly affected by the gain errors associated with the delay and scaling stages. Eq. (19) shows that any gate voltage mismatch causes a linear gain error. Two major sources of gate voltage mismatch are the threshold mismatch and the clock feedthrough error voltage. Because the threshold mismatches are randomly distributed[19] and clock feedthrough errors are relatively constant, the total gain error can be expressed by a random variable v which has the expected value r.

Assume the gain errors of all delay stages have the same distribution and are independent of each other. For a direct-form FIR filter after considering the gain error of each delay stage, its frequency response can be expressed as

$$H(f) = \sum_{k=1}^{N} h_k v^k e^{-j2\pi kf/N} \tag{65}$$

where $v^k$ is the gain error products of previous k stages. The expected value of the filter frequency response is

$$E\{H(f)\} = \sum_{k=1}^{N} h_k E\{v^k\} e^{-j2\pi kf/N}. \tag{66}$$

If E(v) = r, then

$$E\{H(f)\} = \sum_{k=1}^{N} h_k r^k e^{-j2\pi kf/N}. \tag{67}$$

So from Eq. (67) the effective filter coefficient $h_k'$ is equal to the ideal coefficient $h_k$ multiplied by an error factor $r^k$. If no gain errors are introduced, r = 1, and the ideal

frequency response is achieved. Fig. 32 shows the simulated effects of gain errors on the magnitude response of an eleventh order FIR filter.

Two switched-current FIR filters have been designed and implemented using the MOSIS 2 μm digital CMOS technology. Table 1 shows the circuit design parameters. Low-voltage cascode current mirrors were used as the basic building block for all delay and scaling stages. Fig. 33 shows the measured magnitude and phase responses of an integrated FIR filter (Lowpass FIR 1) of order 11, Fig. 34 shows the measured magnitude and phase responses of an integrated FIR filter (Lowpass FIR2) of order eight. Finally, Fig. 35 shows the die photo of the 11th-order FIR filter prototype.

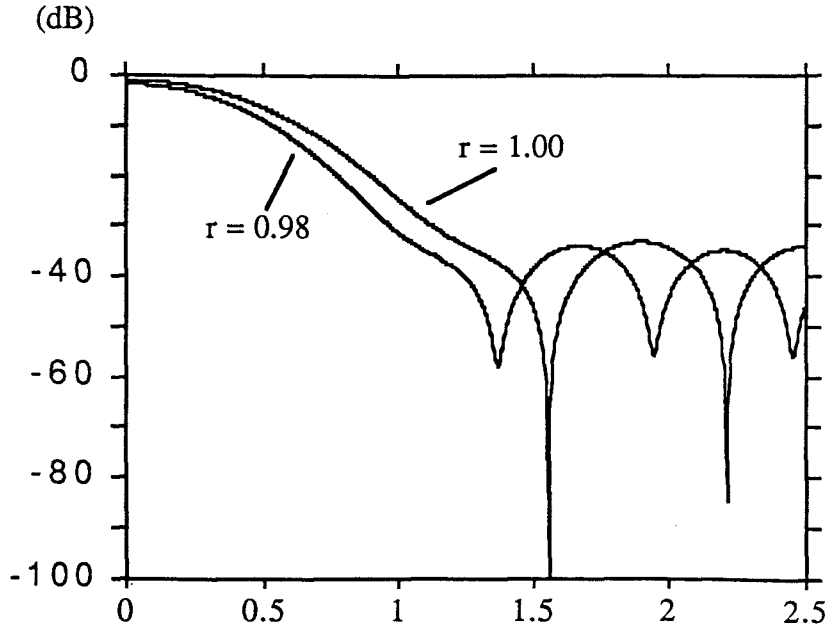



Fig. 31 The simulated effects of gain errors on the magnitude response of an eleventh-order FIR filter.

Table 1. The parameters of the switched-current FIR filter prototypes with sampling rate of $F_s$.

| Filter Type | Lowpass FIR1 | Lowpass FIR2 |
|---|---|---|
| Order | 11 | 8 |
| Cutoff Frequency | $0.1F_s$ | $0.125F_s$ |
| NMOSFET W/L | 20μm/2μm | 20μm/2μm |
| PMOSFET W/L | 20μm/2μm | 20μm/2μm |
| NMOS Switch W/L | 4μm/2μm | 4μm/2μm |
| Bias Current | 200μA | 200μA |
| Power Supply Vdd | 5V | 5V |
| Power Dissipation | 24mW | 20mW |
| Active Die Size | 550x800 $\mu m^2$ | 550x600 $\mu m^2$ |
| Maximum Fs Tested | 10MHz | 10MHz |

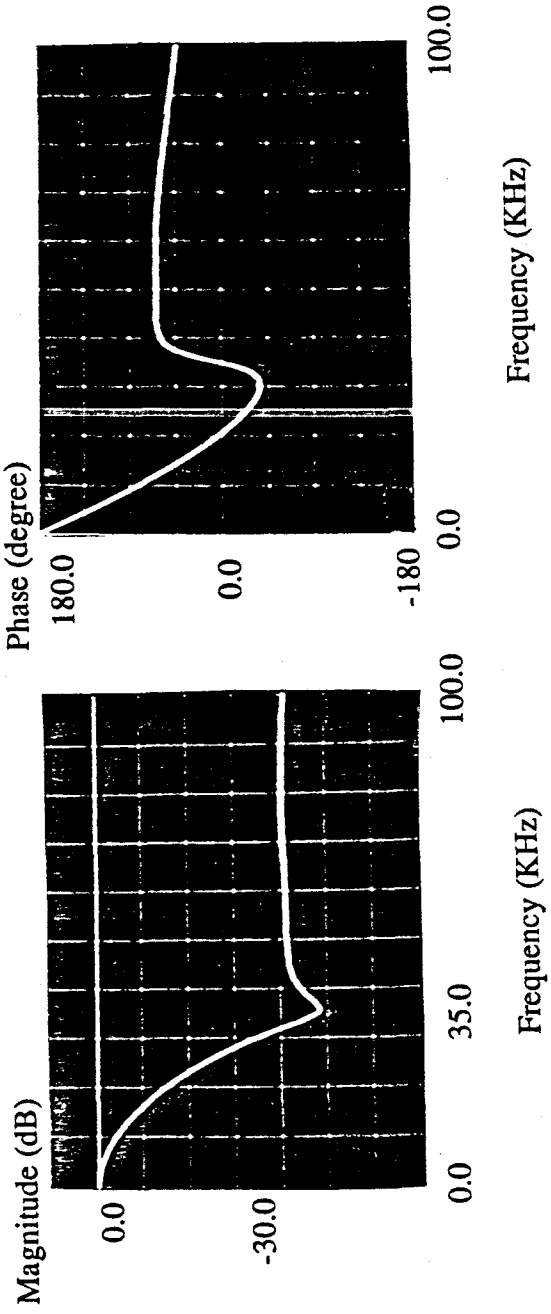



Fig. 32 Measured magnitude and phase responses of the 11th-order FIR filter implemented in the 2 μm P-well MOSIS CMOS technology.

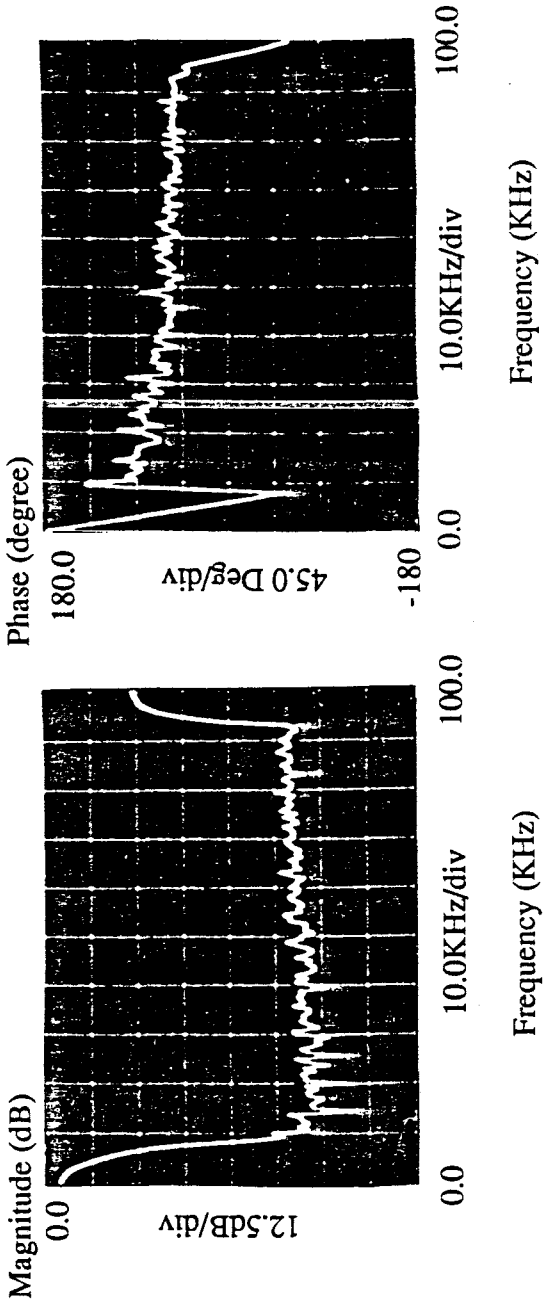



Fig. 33 Measured magnitude and phase responses of the 8th-order FIR filter implemented in the 2 μm P-well MOSIS CMOS technology.

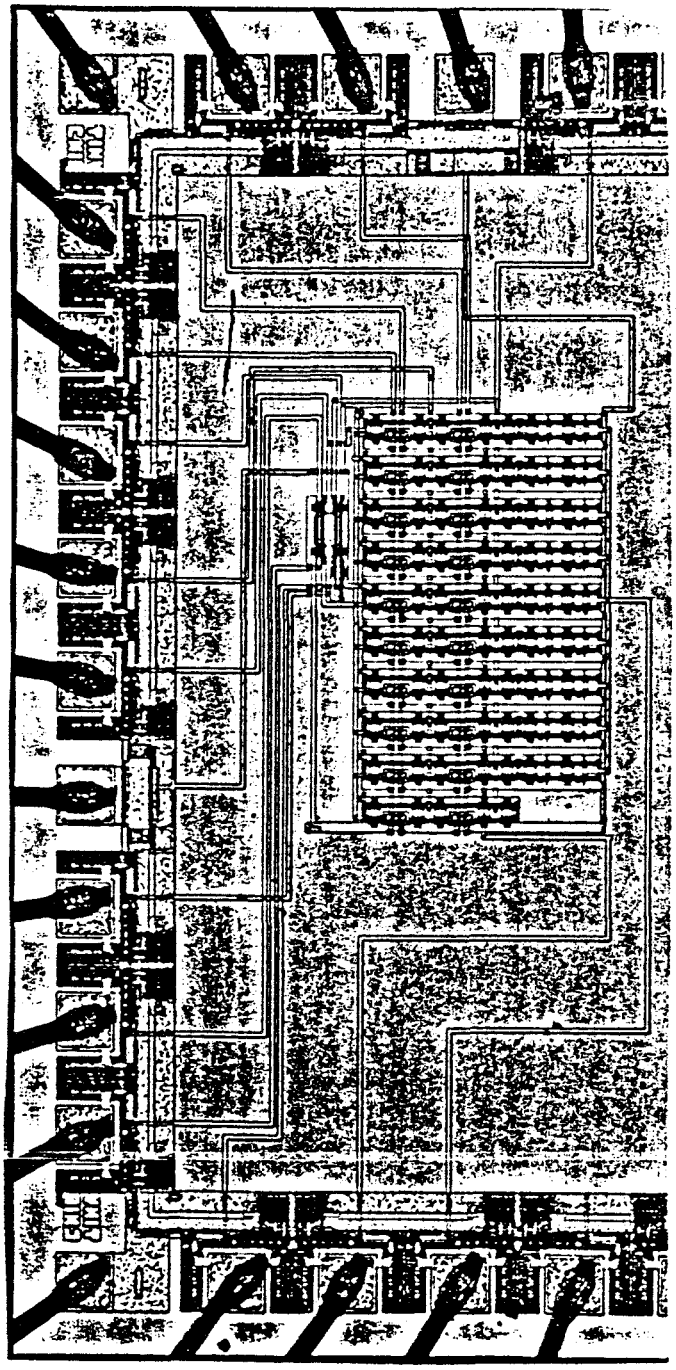


Fig. 34 Die photo of the 11th order FIR filter implemented in the 2 μm MOSIS P-well CMOS technology.

# CHAPTER 6. CONCLUSIONS

A new approach for the synthesis of switched-current filters has been developed which uses switched-current building blocks to directly simulate digital filters. This switched-current filter design method has several important advantages over other approaches: (1) By simulating the conventional digital filter, many existing digital filter design techniques can be directly applied to switched-current filter applications. For example, the unique linear phase property of digital FIR filters can now be achieved using analog switched-current FIR filters. (2) The digital switched-current filter has a very simple structure and high modularity since only two basic blocks are required--the delay stage and scaling stage. (3) A digitally-programmable switched-current filter can be easily implemented by using a programmable scaling stage. By changing the coefficients and the filter structure, any filter type can be realized. (4) Since the switched-current filter response depends only on the ratio of MOSFETs as precision components, reasonably accurate frequency responses can be obtained which are insensitive to temperature and processing variations.

The fundamental performance limitations of switched-current filter have been analyzed including the nonideal input/output resistance effects, nonideal switch effects, MOSFET mismatch effects, the limitations of circuit bandwidth, and the performance of noise and dynamic range. Moreover, the relationships among the clock feedthrough voltages, linear gain errors, and harmonic distortion have been investigated. It has been shown that the clock feedthrough and threshold mismatches are the major sources of linear gain errors and harmonic distortion. A clock feedthrough cancellation circuit has been developed to reduce the total linear gain errors and harmonic distortion of switched-current filters.

Several experimental CMOS prototype switched-current filters have been designed and fabricated. These filters demonstrated the advantages of simple structure, easy design procedures, high operating frequency, etc. Several circuit cells were also designed and fabricated to verify the new clock feedthrough cancellation technique which can be used to improve the performance of switched-current filters.

# PART II

# CURRENT-STEERING LOGIC CIRCUIT DESIGN

## CHAPTER 1. OVERVIEW

With the advancement of CMOS analog and digital technology, CMOS analog/digital mixed-mode integrated circuits are a topic of growing interest. Due to the application of sub-micron technology, mixed-mode circuits have a trend of higher frequency and higher accuracy analog circuitry combined with increasingly complex digital circuitry, e.g., 16-20 bit self-correcting and sigma-delta analog-to-digital converters. To date, the achievable accuracy of such systems has been limited by the adverse effects of power supply noise associated with the switching of conventional CMOS logic circuits integrated on the same chip. In the future, this problem will become proportionately worse with the reduction of the power supply to 3.3 volts, and the reduction of the power supply rejection ratio of the analog circuitry at higher operating frequencies.

CMOS static logic is widely used because of its high packing densities, noise margins, and operating frequencies. Although it dissipates zero static power, a large overlap current spike (~1mA/gate) flows from Vdd to GND during a logic state transition. Large current pulses from many logic gates flow through the inductances and resistances associated with the substrate, power supply lines, bonding wires and package pins of the chip, and cause about 1 volt of switching noise on the chip power supply lines. This switching noise interferes with the analog circuitry and limits the achievable accuracy and dynamic range of the entire mixed-mode integrated system.

One way to increase the accuracy of mixed-mode IC's in the presence of digital switching noise is to increase the power supply noise rejection capabilities of the analog circuitry. With fully-differential analog architectures, power supply noise appears as a common-mode signal that is rejected by an amount equal to the common-mode-rejection-ratio (CMRR). However, CMRR usually decreases in direct proportion to increases in frequency. The transmission and coupling of digital switching noise between the digital and analog subsystems can also be reduced by using different guardbanding and/or power supply separation techniques. The separation of analog and digital power supply lines is usually used to minimize the common power supply impedance. Unfortunately, the success of the above techniques is determined by the nature of the power supply connections to the substrate. When laying out digital cells using a p-well CMOS technology, it is common practice to incorporate within each cell several ohmic contacts from the digital Vdd supply line to the substrate to deter catastrophic latch-up. Hence, switching noise associated with digital Vdd is coupled directly into the analog circuitry via the common substrate.

Significant reduction of power supply noise may also be achieved by reducing the magnitude of the switching current spike generated by the digital circuits. In conventional CMOS logic circuits, the current spike originates with the overlap current pulses generated during logic state transitions. More precisely, the current spike occurs because the power supply current is not constant. One way to implement logic circuits with a constant current is to use MOS differential pairs to steer a constant current source similar to bipolar Emitter-Coupled Logic (ECL) techniques. This technique requires several additional transistors per gate, and the

MOSFET's are usually required to have large W/L ratios at high operating frequencies [35].

In this part of the dissertation, the newly developed current-steering logic is presented as an alternative to static CMOS logic for high-frequency, high-accuracy mixed-mode applications. Since the first MOS logic circuit was developed in the early 1960's[37], it has been customary to use voltages to represent the logic states. All exiting commercially-available digital circuits are based upon this assumption. It will be shown that by using currents instead of voltages to represent the logic states, a totally different logic family can be developed. It can be implemented using a standard scaled digial CMOS technology. By steering a constant current to either a current sink or to the next stage, ideally no current spike is generated during the transition time. Due to the nonlinear V/I characteristics of MOSFET, only a small voltage swing is required for a full current swing. Thus, CMOS current-steering logic has the advantages of high speed and is independance to power supply voltages.

In Chapter 2 of this section, the principle of current-steering logic circuits is introduced. It starts with the definitions of the current logic levels, and then the operation of the current steering logic inverter is presented. Following that, the basic logic NOR gate is developed. Applications of current-steering logic are also discussed such as, filp-flops, Programmable Logic Arrays (PLA), etc. Chapter 3 analyzes the basic performance of current-steering logic circuits including the static transfer characteristic, noise margins, switching speeds, gate-delays, power-delay products, fanout effects and power supply voltage effects. In Chapter 4, the current spike of current-steering logic is discussed together with some experimental results from integrated prototypes. Finally, the conclusions are given in Chapter 5.

# CHAPTER 2. CURRENT-STEERING LOGIC CIRCUITS

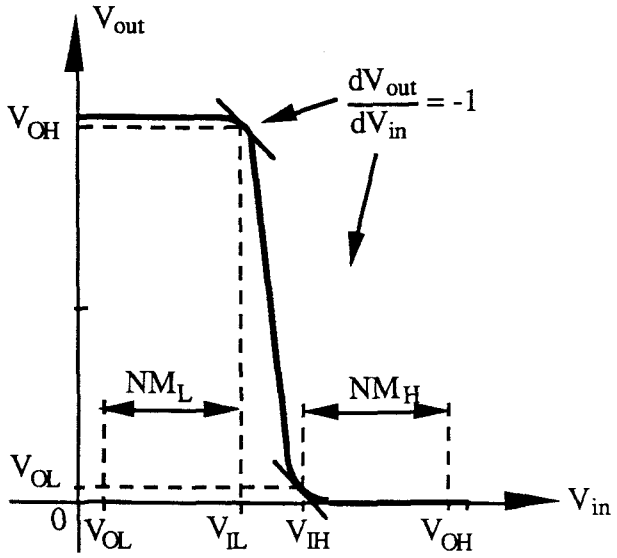
This chapter begins with the basic logic level definitions of a current-steering circuit by using the example of an inverter. It is shown that in the current-steering circuits, the logic levels no longer depend on the power supply voltage, but only on the bias current supplied to the circuit. Following that, the basic logic NOR gate is constructed and analyzed. Finally, some application circuits such as flip-flops and PLAs are presented.

## 2.1. Basic Inverter

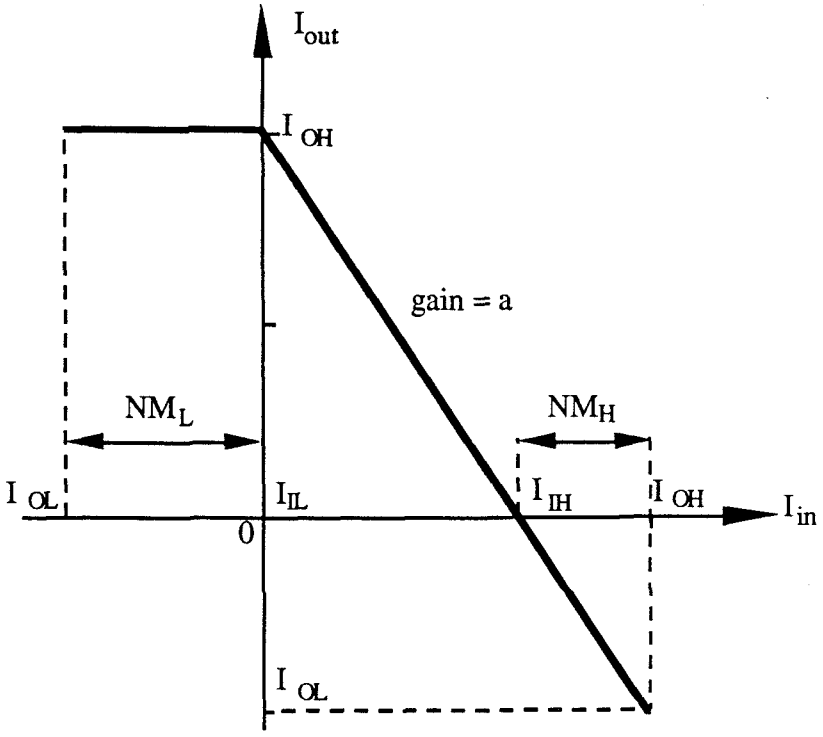
The conventional CMOS logic inverter has the transfer function shown in Fig. 35a. Two output logic states are determined by two input threshold voltages, $V_{IH}$ and $V_{IL}$. For input voltage $V_{in} > V_{IH}$, logic state "1" is assumed. For input voltage $V_{in} < V_{IL}$, logic state "0" is assumed. If $V_{IH} > V_{in} > V_{IL}$, then logic state is not determined.

By following a similar principle with current instead of voltage used to represent the logic states, the transfer function of current-steering inverter is shown in Fig. 35b. Two threshold currents, $I_{IH}$ and $I_{IL}$ can be used to determine the output logic states. For any input current $I_{in} > I_{IH}$, logic state "1" is assumed, and for any input current $I_{in} < I_{IL}$, logic state "0" is assumed. If $I_{IH} > I_{in} > I_{IL}$, the logic state is not determined.

Based upon the above definitions and the positive current definitions, the ideal current-steering inverter is implemented in Fig. 36. Assume the current-steering circuit drives an identical stage, and MOSFETs $M_1$ and $M_2$ are matched with $(W/L)_1 = (W/L)_2$. When $I_{in} = 0$, $M_1$ and $M_2$ are off, are $I_{out} = I$. When $I_{in} = I$, $I_{ds1} = I_{ds2} = I$, and $I_{out} = 0$. Note that the total current drawn from the




(a) Transfer function of conventional CMOS logic inverter.




(b) Transfer function of a current-steering logic inverter.

Fig. 35 Transfer functions of voltage and current mode logic inverter.

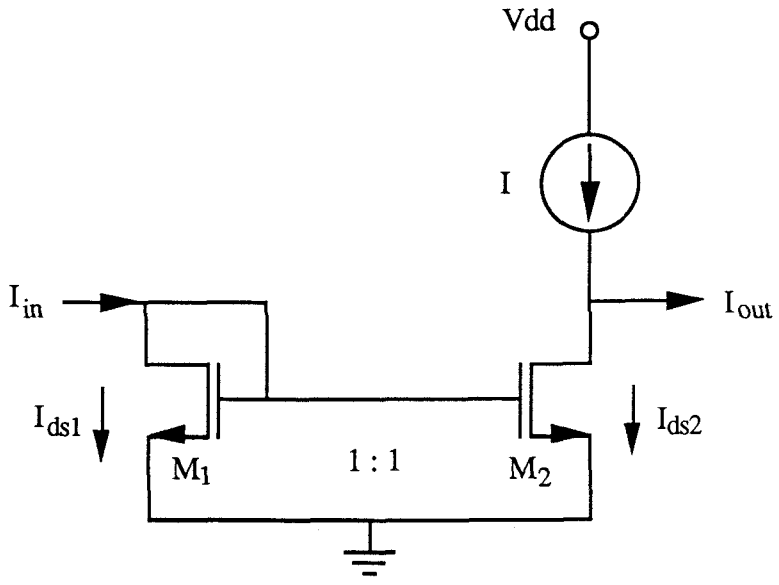



Fig. 36 Simplified schematic of a CMOS current-steering inverter with a current gain of one.

power supply is constant at I, so ideally no current spike is generated during logic state transitions.

Due to the nonlinear V/I characteristics of MOSFETs, the voltage swing of the current-steering logic circuits is smaller than the conventional CMOS logic circuits. In saturation condition, the drain current of $M_1$ is

$$I_{ds1} = \beta_1(V_{gs1} - V_{t1})^2. \tag{68}$$

At logic "1" state, the gate voltage of $M_1$ is

$$V_H = \sqrt{\frac{I}{\beta_1}} + V_{t1}. \tag{69}$$

At logic "0" state, $I_{ds1} = 0$, and the gate voltage is $V_L = V_{t1}$. Hence the voltage swing is

$$\Delta V = V_H - V_L = \sqrt{\frac{I}{\beta_1}}. \tag{70}$$

For a bias current I = 100 μA, and $(W/L)_1 = 2$, the voltage swing is $\Delta V = 1.4$ V.

In a practical application, the constant current source of Fig. 36 is realized using a PMOSFET biased by a constant voltage as shown in Fig. 37. Furthermore, similar to the switched-current analog circuits, because each output current signal can have only one destination, current-steering logic circuits requires an identical output branch for each fanout. Fig. 38 shows a current-steering inverter of fanout of 2.

## 2.2. Current-Steering NOR Gate and Some Applications

The two input current-steering logic NOR function (with fanout of one) is realized by connecting the outputs of two inverters as shown in Fig. 39. When either or both input currents $I_{in1}$ and $I_{in2}$ equal I, the output current is $I_{out} = 0$. When both of the input currents are zero, the output current is $I_{out} = I$. Hence a two-input current-steering logic NOR gate with fanout of one is realized with its

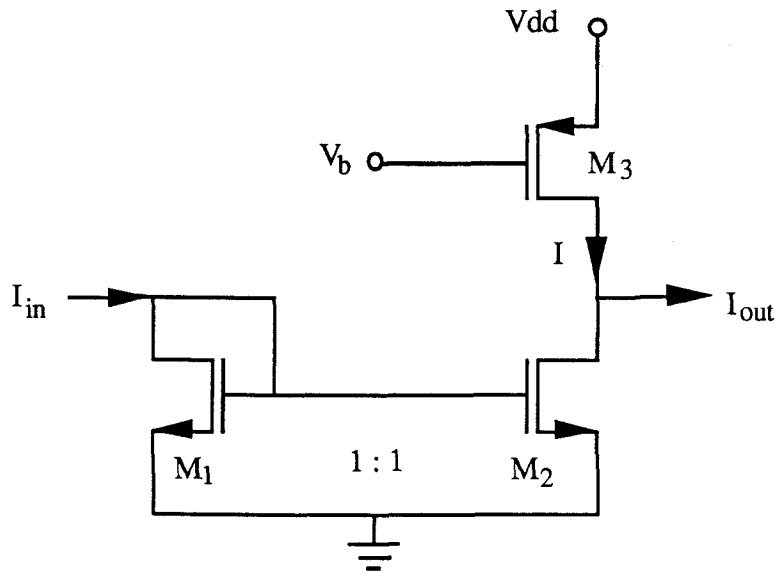



Fig. 37 Complete schematic of a CMOS current-steering inverter with a current gain of one. PMOS $M_3$ provides a nearly constant bias current I.

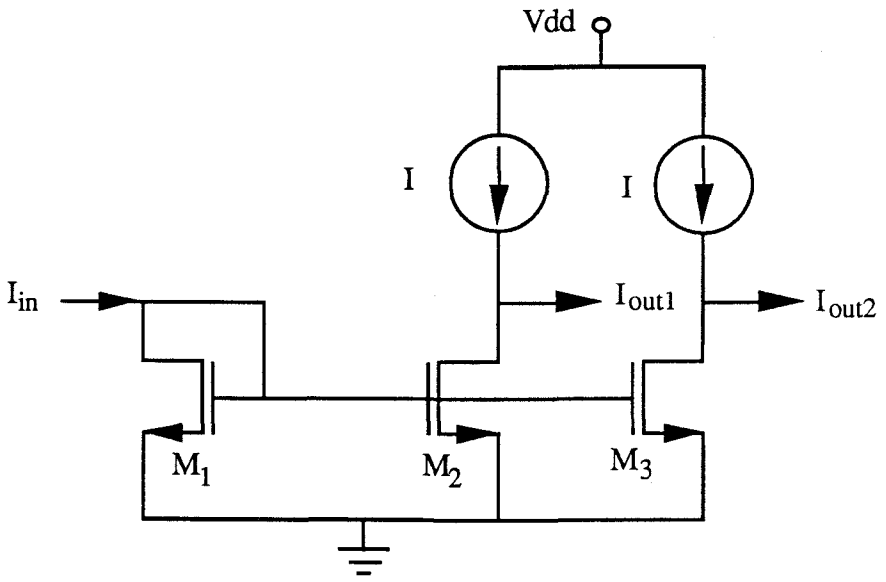



Fig. 38 Simplified schematic of a current-steering inverter with a fanout of two.

(One additional output branch is required for each additional fanout.)

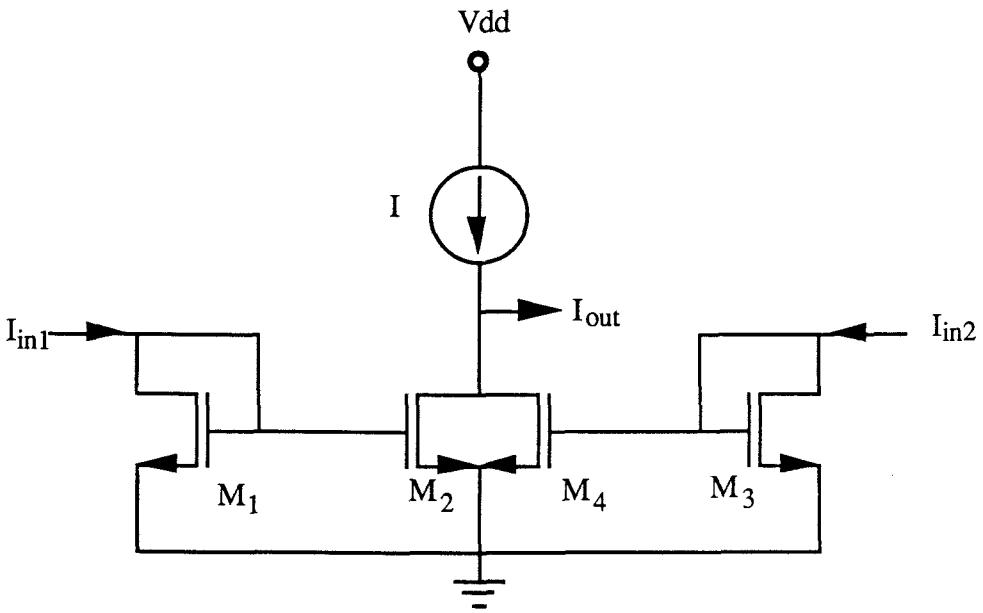



Fig. 39 Simplified schematic of a CMOS current-steering two-input NOR gate with a fanout of one.

truth table shown in Table 2. Similarly, by connecting the outputs of three current-steering inverters together, a three-input NOR gate is realized, etc. It is well known that all logic functions can be realized using logic NOR gates, i.e., the NOR gate is a logically complete set.

Table 2. Truth table of the two-input current-mode NOR gate.

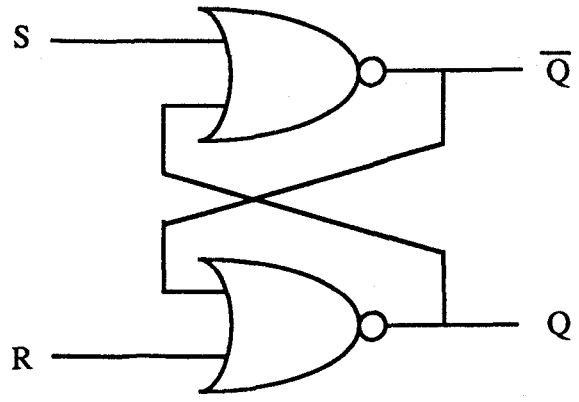
| $I_{in1}$ | $I_{in2}$ | $I_{out}$ |
|---|---|---|
| 0 | 0 | I |
| 0 | I | 0 |
| I | 0 | 0 |
| I | I | 0 |

Because of its unique fanout structure, current-steering logic cannot directly replace conventional CMOS logic circuits. For example, Fig. 40(a) shows a standard RS flip-flop. If current-steering logic NOR gates are used, the RS flip-flop is realized as shown in Fig. 40(b). Other CMOS logic circuits are implemented by applying similar modifications.

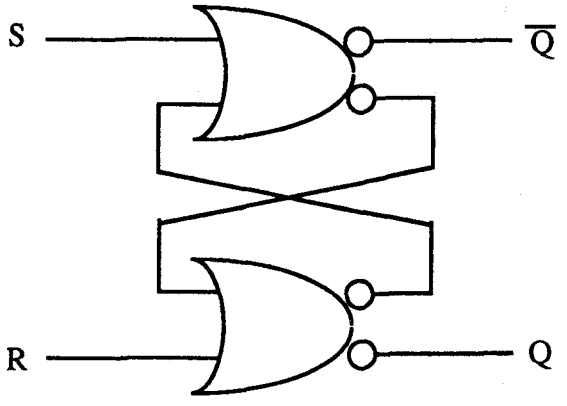
Although all existing logic circuits can be replaced by current-steering circuits, the resulting circuits may not be optimized for performance in terms of packing density, speed, or power consumption. Most commonly-used logic circuits and systems can be customized based on the unique properties of current-steering logic circuits to achieve optimum overall performance. For example, the Programmable Logic Array (PLA) is one of the most commonly-used blocks in combinational logic circuits. Fig. 41 shows a logic circuit of a conventional pseudo-static CMOS PLA[37]. It is evident that in the first NOR plane, the number of fanouts of every NOR gate is determined by the product number. A PLA with a large product number requires those gates having a large fanout. But in current-

steeringcircuits, every fanout requires an additional output branch, so a direct implementation of a current-steering PLA results in a complicated circuit that occupies a large silicon area.

In order to simplify the circuit for implementation as a current-steering PLA, a different approach is taken as shown in Fig. 42. Inside the PLA, intermediate voltages are used as variables to represent the logic states. After the operation through the two NOR planes, the intermediate voltages are converted back to currents. The logic voltage levels and logic voltage swing of the intermediate variables are determined by the bias current. The equivalent voltage-mode current-steering inverter is shown in Fig. 43. A prototype current-steering PLA was designed and fabricated using the MOSIS 2 μm CMOS technology. It has eight possible inputs, four outputs and 15 possible product terms. It is configured as a thermometer code to a binary code converter with an overflow output. Fig. 44 shows the measured transition waveform of first output when the input binary code changes from 00111111 to 01111111.




(a) Conventional CMOS implementation of an RS flip-flop.




(b) Current Steering implementation with fanout of two for each NOR gate.

Fig. 40 Implementation of voltage and current mode RS flip-flops.

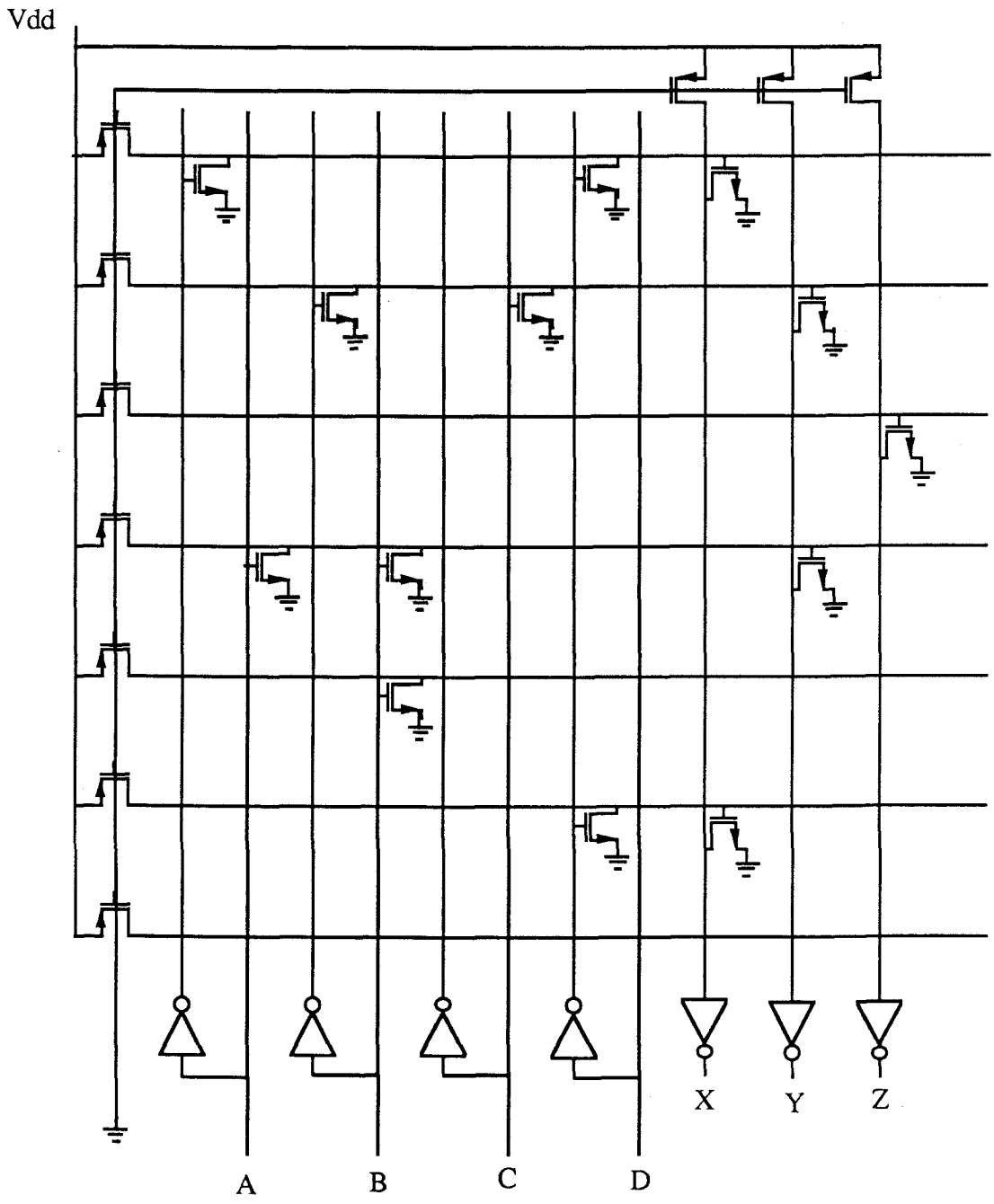



Fig. 41 Conventional pseudo-static CMOS PLA with five product terms and three sum terms actually implemented.

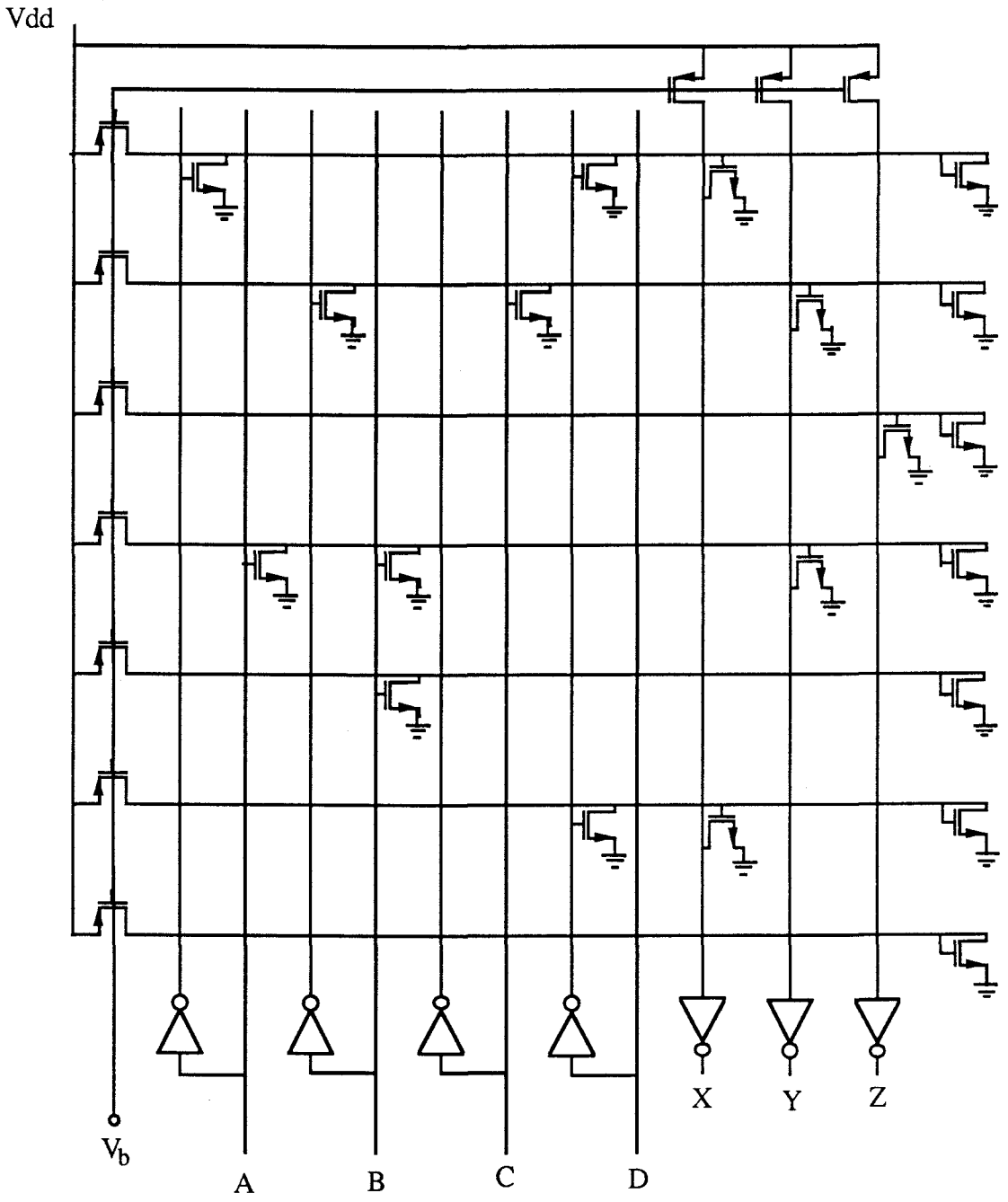



Fig. 42 Current-steering implementation of the NOR PLA with five product terms and three sum terms. Voltages are used to represent logic levels within the PLA.

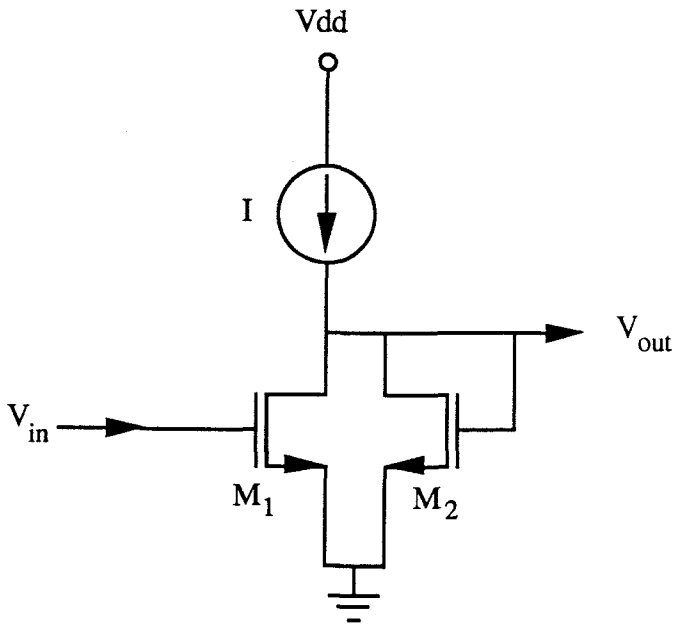



Fig. 43 Equivalent voltage mode current-steering inverter.

(The voltage swing is designed to be about 1.4 volt for PLA.)

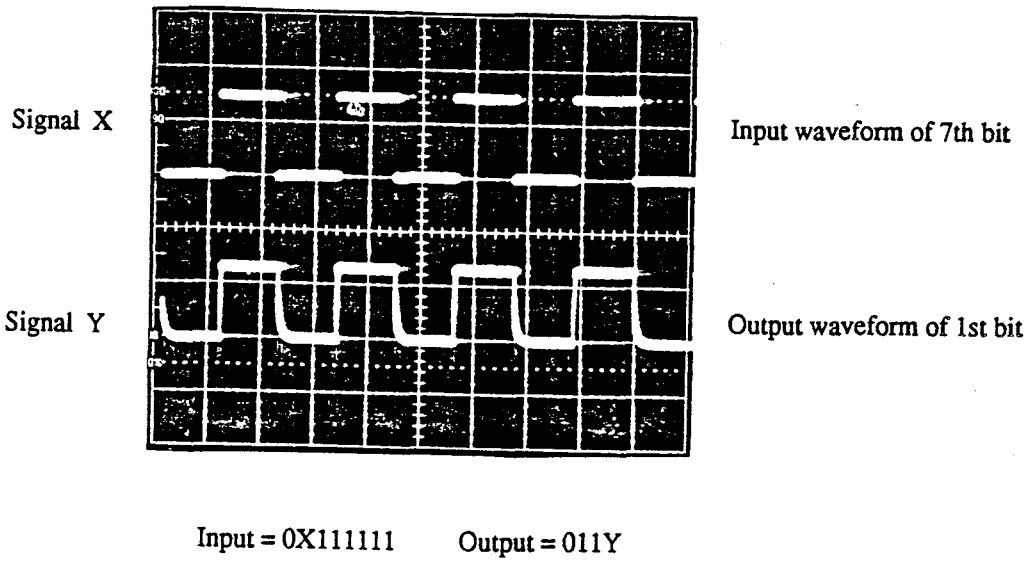



Fig. 44 Measured transition waveform of one output of a current-steering PLA implemented in a 2 μm MOSIS CMOS technology.

# CHAPTER 3. TRANSIENT ANALYSIS

In this chapter, the current-steering logic circuit is characterized. At first, the transfer characteristic and noise margins of the current-steering inverter are investigated, and the switching characteristics are discussed. Finally, the relationships between the bias current and propagation delays are analyzed.

## 3.1. Transfer Characteristics and Noise Margins

The transfer characteristics of the ideal current-steering inverter are shown in Fig. 45. It can be divided into three regions: the logic low region where $I_{in} \leq I_{IL}$, the logic high region where $I_{in} \geq I_{IH}$, and the transition region where $I_{IL} < I_{in} < I_{IH}$.

Noise margins are a measure of a logic circuit's tolerance to noise in either of the two logic states. A noise margin is determined by how much the input can change without significantly disturbing the present logic output state. In current-steering logic circuits, the logic levels are represented by currents, so the noise margins must also be defined using currents. By analogy to conventional CMOS voltage-mode static logic, the current noise margins are defined as

$$\text{High level} \qquad NM_H = I_{OH} - I_{IH} \tag{71a}$$

and

$$\text{Low level} \qquad NM_L = I_{OL} - I_{IL} \tag{71b}$$

where $I_{IH}$ and $I_{OH}$ are the input and output nominal logic high levels, and $I_{IL}$ and $I_{OL}$ are the input and output nominal logic low levels. Fig. 45 shows the transfer function of a unity-gain current-steering inverter and its four threshold voltages.

In Fig. 45, both the input and output of the unity-gain current-steering inverter have the same logic low level, and the same logic high level $I_{IH} = I_{OH} = I$, and $I_{IL} = I_{OL} = 0$. Based on the definitions of noise margins, both high and low

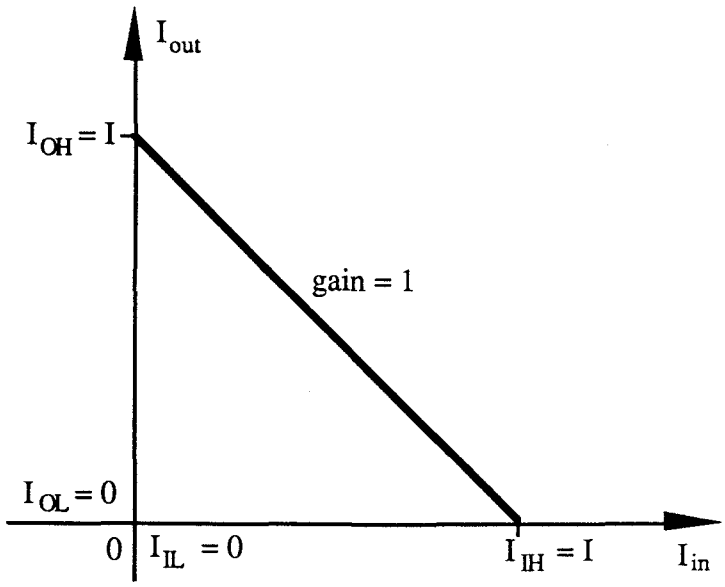



Fig. 45 Transfer characteristic of unit-gain current-steering inverter with $I_{OH}(I_{IH})$ and $I_{OL}(I_{IL})$ define the output (input) logic high and low levels respectively.

level noise margins are therefore equal to zero. Hence, the unity-gain current-steering logic circuits are not suitable for practical applications.

Similar to the switched-current scaling stage, in Fig. 46 a current gain of A is introduced into the current-steering inverter, by ratioing the size of $M_2$ relative to $M_1$ so that $A = \frac{(W/L)_2}{(W/L)_1} > 1$. The transfer characteristics are shown in Fig. 47. For example, if A=1.5, when $I_{in}$=I , $I_{ds2}$=1.5I, so $I_{out}$ can be as small as I - $I_{ds2}$=-0.5I. This means the next stage must supply 0.5I current to this stage or $M_2$ will go to nonsaturation. In this example, the actual logic high level is I and the logic low level is 0. From the definitions, it is found that $I_{OH}$ = I, $I_{OL}$ = -0.5I, $I_{IH}$ = 0.67I, and $I_{IL}$ = 0. Therefore, the noise margins are

$$\text{High level} \qquad NM_H = I_{OH} - I_{IH} = 0.33I, \tag{72a}$$

$$\text{Low level} \qquad NM_L = I_{IL} - I_{OL} = 0.5I. \tag{72b}$$

For example, if two identical inverters are cascaded, with a logic low input level, if input current is corrupted by noise with a value between -0.5I are 0, the output of the first inverter still has the correct value I, and the second inverter has the output value zero. Similarly, for the logic high input level, if the input current is from 0.67I to I, the output value of first inverter will be less than 0, and next inverter stage will have the output value of I. In both cases, any perturbation of the input logic level within the noise margin is recovered by the logic circuit. Hence, current-steering logic circuits are a restoring logic family. If the value of input current falls within the transition range, any small perturbation is amplified until a valid output signal is reached.

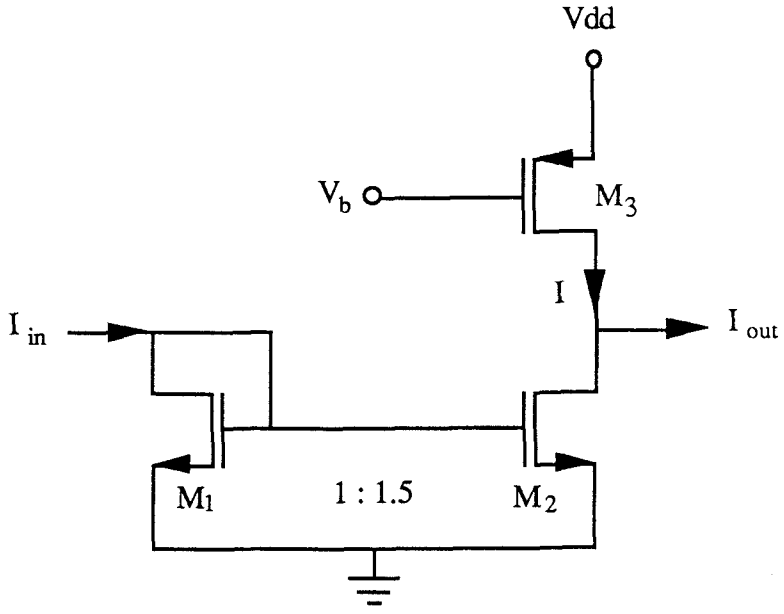



Fig. 46 Practical implementation of a current-steering inverter with a current gain of 1.5.

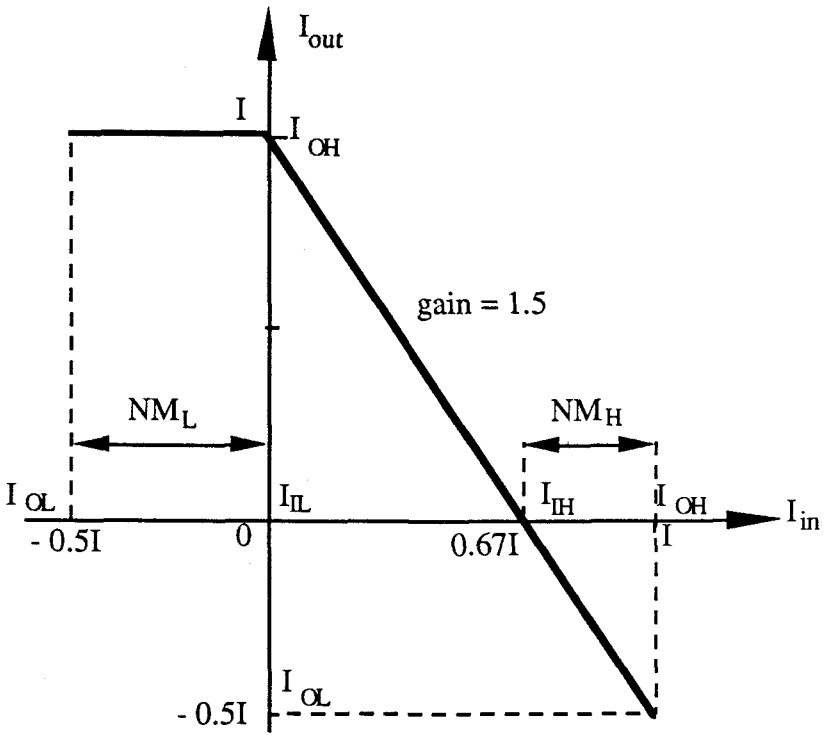



Fig. 47 Transfer characteristics of a practical CS inverter with a current gain of 1.5.

### 3.2. Transient Analysis and Power Delay Product

Assuming the output of a previous stage is an ideal current pulse as shown in Fig. 48, its logic high level is $I_{OH} = I$, and logic low level is $I_{OL} = 0$. Because there is no active source connected to the input node during the logic low state, the previous stage is forced into nonsaturation, which means that at the logic low state, the input voltage is less than $V_t$. For example, if the current gain is equal to two, then $\beta_2 = 2\beta_1$. From $I_{ds1} = I_{ds2}$ we have

$$\beta_1(V_{gs}-V_t)^2 = \beta_2[(V_{gs}-V_t)V_{ds2} - \frac{1}{2}V_{ds2}^2], \tag{73}$$

and the output voltage at logic low state is

$$V_{OL} = V_{ds2} = V_{gs}-V_t. \tag{74}$$

For $(W/L)_1 = 2$ and $I = 50\ \mu A$, $V_{ds2} = 0.8$ V. Hence, during the rise time, there are two different regions. First $M_1$ and $M_2$ shut off and the equivalent circuit is simply a constant current source charging the capacitor $C_{in}$ of the input node, where $C_{in} \approx C_{gs1} + C_{gs2}$ as shown in Fig. 49a. Assuming this period starts when $V_{gs1} \approx V_{OL}$, and ends when $V_{gs1} = V_T$,

$$C_{in}\frac{dV_{gs1}}{dt} = I_{OH} \tag{75}$$

and the time of this period is

$$T_{r1} = \frac{V_t-V_{OL}}{I}C_{in} \tag{76}$$

After $M_1$ turns on, the equivalent circuit is a constant current source connected to a capacitor $C_{in}$ and a diode $M_1$ as shown in Fig. 49b. This region starts when $I_{ds1} = I_{ds2} = 0$, $I_{out} = I$, and ends when $I_{out} = 0$, or $I_{ds2} = I$. Because part of input current flows through $M_1$, the capacitor is charged by the current

$$I_c = I_H - \beta_1 (V_{gs1} - V_t)^2 = C_{in}\frac{dV_{gs1}}{dt} \tag{77}$$

By solving the differential equation, the time of this period can be expressed as

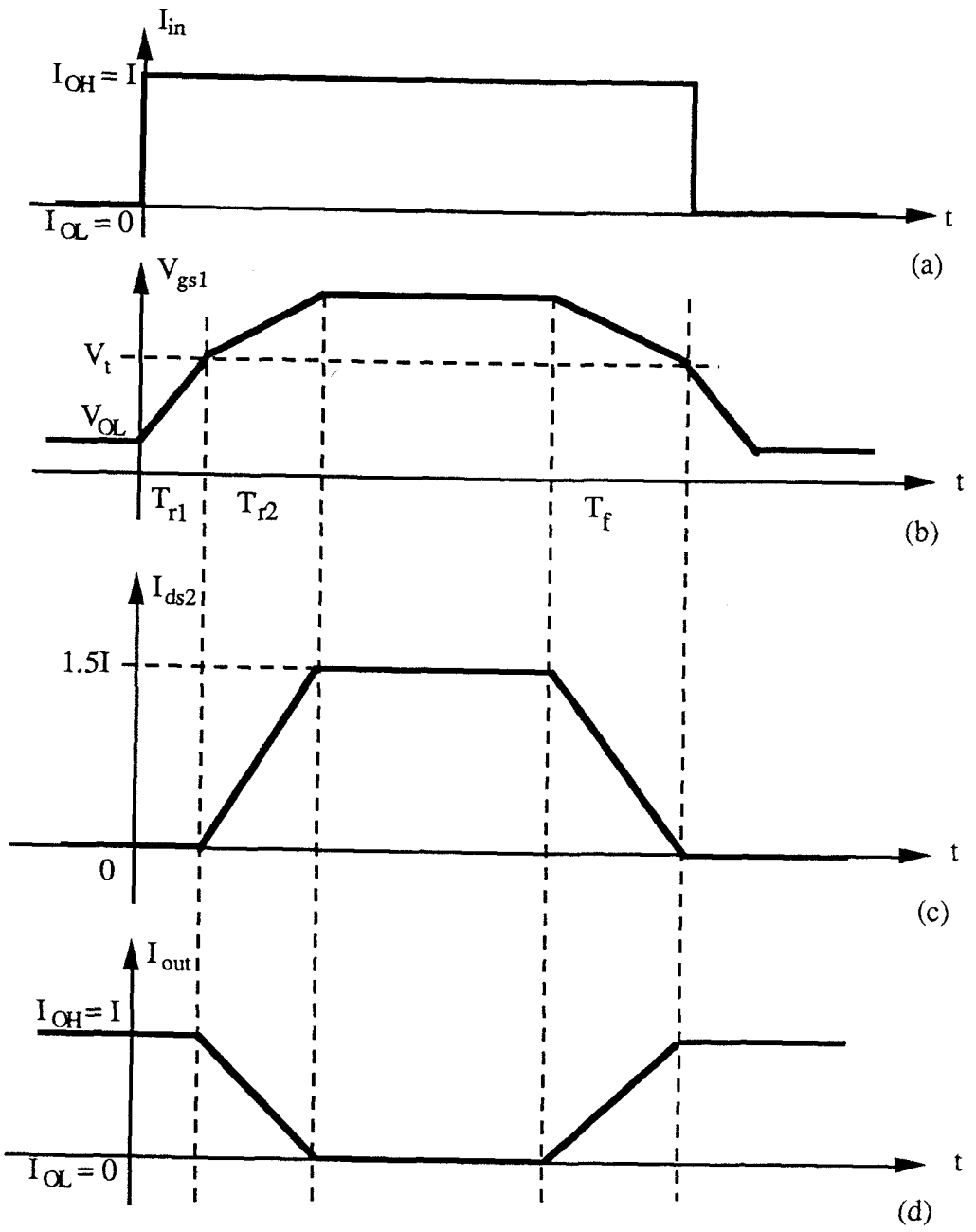
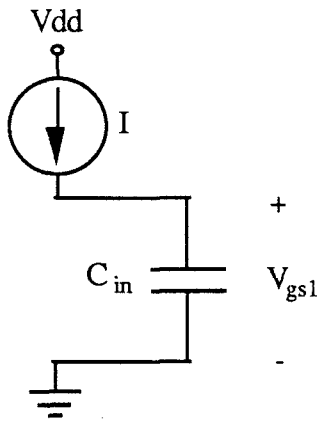
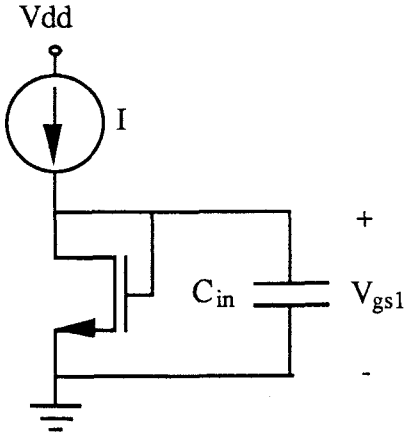


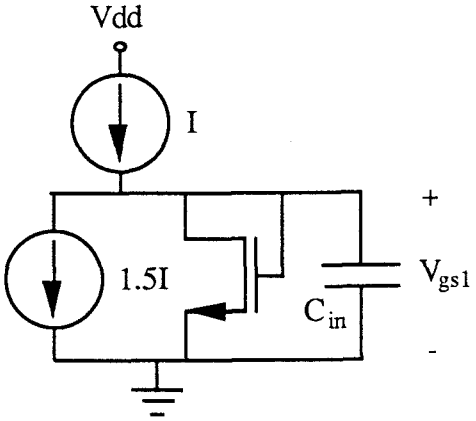

Fig. 48 Simplified transition waveform of the current-steering logic inverter.




(a) At rising edge, before $M_1$ turns ON.




(b) At rising edge, after $M_1$ turns ON.




(c) At falling edge, before $M_1$ turns OFF with current gain = 1.5.

Fig. 49 Equivalent circuits of current-steering inverter

at different transition period.

$$T_{r2} = \frac{C_{in}}{2}\sqrt{\frac{1}{\beta_1 I}}\ln\left(\frac{\sqrt{1/\beta_1}+\sqrt{1/\beta_2}}{\sqrt{1/\beta_1}-\sqrt{1/\beta_2}}\right) \quad (78)$$

where $\beta_1$ and $\beta_2$ are the transconductance constant of $M_1$ and $M_2$. The total rise time is therefore

$$T_r = T_{r1} + T_{r2} = \frac{(V_t - V_{OL})C_{in}}{I} + \frac{C_{in}}{2}\sqrt{\frac{1}{\beta_1 I}}\ln\left(\frac{\sqrt{1/\beta_1}+\sqrt{1/\beta_2}}{\sqrt{1/\beta_1}-\sqrt{1/\beta_2}}\right) \quad (79)$$

During the fall time before $M_1$ turns off, the capacitance of the input node is discharged through the diode and the input current $I_{OL}$ as shown in Fig. 49c. This period starts when $I_{out} = 0$ and ends when $I_{out} = I$, or $V_{gs1} = V_{t1}$. The discharging current of capacitor $C_{in}$ is

$$I_c = I_L + \beta_1(V_{gs1} - V_{t1})^2 = -C_{in}\frac{dV_{gs1}}{dt} \quad (80)$$

and the total fall time is found as

$$T_f = C_{in}\sqrt{\frac{1}{(\beta_2-\beta_1)I}}\arctan\left(\sqrt{\frac{\beta_1}{\beta_2-\beta_1}}\right). \quad (81)$$

From the above results, the average propagation gate delay is found as

$$\begin{aligned} T_p &= (T_r + T_f)/2 \\ &= \frac{(V_t - V_{OL})C_{in}}{2I} + \frac{C_{in}}{4}\sqrt{\frac{1}{\beta_1 I}}\ln\left(\frac{\sqrt{1/\beta_1}+\sqrt{1/\beta_2}}{\sqrt{1/\beta_1}-\sqrt{1/\beta_2}}\right) \\ &\quad + \frac{C_{in}}{2}\sqrt{\frac{1}{(\beta_2-\beta_1)I}}\arctan\left(\sqrt{\frac{\beta_1}{\beta_2-\beta_1}}\right) \end{aligned} \quad (82)$$

This equation shows that the gate delay of current steering logic is reduced by either increasing the bias current I and/or decreasing the node capacitance $C_{in}$ which can be achieved through the use of smaller feature size. Moreover, because the bias current is constant, the power-delay product is easily found from equation (82) as

$$\begin{aligned} PDP &= V_{dd} I T_p \\ &= \frac{V_{dd}C_{in}(V_t - V_{OL})}{2} + \frac{V_{dd}C_{in}}{4}\sqrt{\frac{I}{\beta_1}}\ln\left(\frac{\sqrt{1/\beta_1}+\sqrt{1/\beta_2}}{\sqrt{1/\beta_1}-\sqrt{1/\beta_2}}\right) \\ &\quad + \frac{V_{dd}C_{in}}{2}\sqrt{\frac{I}{(\beta_2-\beta_1)}}\arctan\left(\sqrt{\frac{\beta_1}{\beta_2-\beta_1}}\right). \end{aligned} \quad (83)$$

Fig. 50 shows the measured propagation delay of a current-steering inverter at different bias currents. The data is measured from a 2μm CMOS ring oscillator prototype. For example, when bias current I = 100 μA, $T_p \approx 0.7$ nS, and $V_{dd} = 5V$, the power-delay product is PDP = 0.35 pJ, and the power dissipation is 0.5 mW. Although static logic dissipate zero static power, it dissipate dynamic power given by $CV^2f$. So the current-steering logic consumes more power at low frequencies, but it actually dissipates less power than static logic circuit for high frequency operation. For example, if the total loading capacitance of static CMOS inverter is 0.2 pf, the bias current of current-steering inverter is 100 μA, for the same power supply voltage $V_{dd} = 5V$. The static CMOS inverter will dissipate more power when the operating frequency is higher than 100MHZ.

### 3.3. Scaling of Current Steering Logic

With the continuing advancement of integrated circuit fabrication technology, the internal dimensions of MOS devices will be reduced steadily until fundamental physical limitations are reached. From the previous discussion, the power-delay product and the average delay time of current-steering logic circuits are related to the capacitance, threshold voltage, and conductance constant of the MOSFETs. In this section, we discuss the first-order changes to the current-steering logic characteristics as the internal device dimensions are reduced.

There are three major scaling laws. The first is called constant electric field (CE) scaling, wherein all vertical and horizontal device dimensions and all voltages, including threshold voltages, are reduced by a scaling factor of S. Since the oxide thickness is reduced by S, oxide capacitance per unit area is increased by S. However, because the device area is reduced by $S^2$, the total oxide capacitance is reduced by a factor of S. Moreover, if the carrier mobility does not change in the

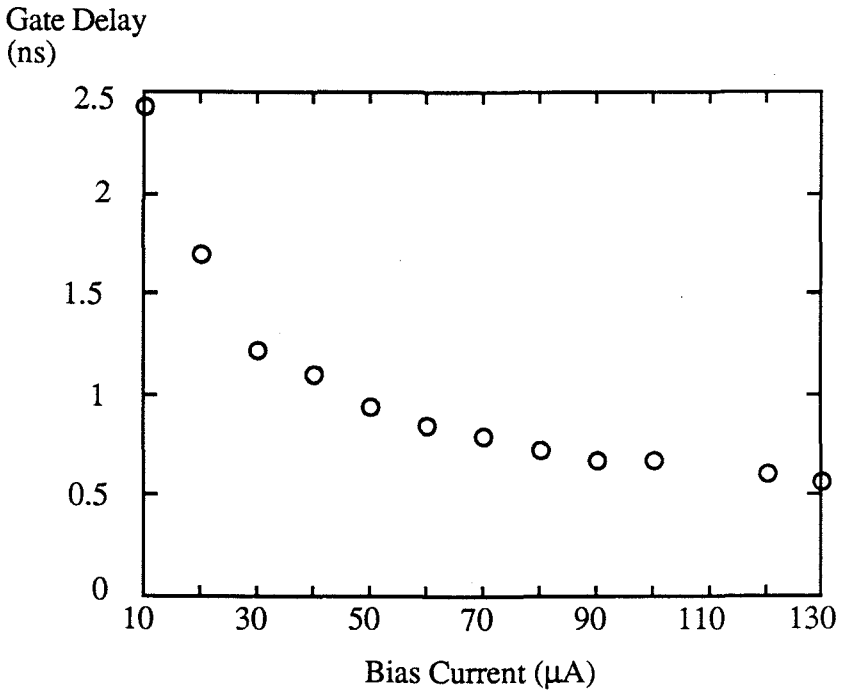



Fig. 50 Measured average gate delay of a prototype current-steering ring osillator at different bias currents with $(W/L)_1$ = 3μm/2μm, $(W/L)_2$=4μm/2μm, $(W/L)_3$=6μm/2μm and $V_{dd}$ = 5V.

scaling process, the conductance constant ß is increased by S due to the reduced oxide thickness. So from Eq. (82), assuming the same amount of bias current I, the average delay time is

$$T_p' = \frac{(V_t - V_{OL})C_{in}}{2IS^2} + \frac{C_{in}}{4S}\sqrt{\frac{1}{ß_1 IS}}\ln\left(\frac{\sqrt{1/ß_1} + \sqrt{1/ß_2}}{\sqrt{1/ß_1} - \sqrt{1/ß_2}}\right) + \frac{C_{in}}{2S}\sqrt{\frac{1}{(ß_2 - ß_1)IS}}\arctan\left(\sqrt{\frac{ß_1}{ß_2 - ß_1}}\right) \quad (84)$$

and is reduced by a factor of $S^{3/2}$ for a scaling of S.

The second possible scaling law is called constant voltage (CV) scaling. It reduces all lateral device dimensions by S, the oxide thickness by $\sqrt{S}$, but keeps all voltages constant. The third scaling law is called quasi constant voltage scaling, and it reduces all lateral and vertical device dimensions by S, and all voltages by $\sqrt{S}$. Through a similar analysis, the relations between scaling laws and the performance of the current-steering logic circuits are shown in Table 3. From Table 3 it is clear that all three scaling laws can by used to improve the performance of current-steering logic circuits. But the constant field law can achieve the maximum power-delay product improvement.

Table 3 The scaling relation of current-steering logic

| Parameters | Constant Field | Quasi Constant V | Constant Voltage |
|---|---|---|---|
| W, L | 1/S | 1/S | 1/S |
| $t_{ox}$ | 1/S | 1/S | $1/\sqrt{S}$ |
| $V_{dd}$, $V_t$ | 1/S | $1/\sqrt{S}$ | 1 |
| Capacitances | 1/S | 1/S | $1/S^{3/2}$ |
| ß | S | S | $\sqrt{S}$ |
| Average delay $t_p$ | $1/S^{3/2}$ | $1/S^{3/2}$ | 1/S |
| Power-delay Product | $1/S^{5/2}$ | $1/S^2$ | 1/S |
| Bias Current I | 1 | 1 | 1 |
| Power Consumption | 1/S | $1/\sqrt{S}$ | 1 |

# CHAPTER 4. POWER SUPPLY NOISE

In conventional static logic circuits, the large overlap current pulse (~1mA) of every gate during the logic state transition, shown in Fig. 51, flows through the inductances and resistances associated with the substrate, power supply lines, bonding wires, package pins, etc., and causes as much as 1 volt of power supply voltage noise.

In current-steering logic, the constant current source draws current from a power supply, and ideally no current spike is generated. In practical applications, the PMOSFET is used to implement the current source. Due to the parasitic capacitances and channel-length modulation effects, a small current spike is generated, and can be analyzed by dividing the overall current spike into two separate components.

First, assume two inverters are cascaded together and the current sources are realized as simple PMOSFETs biased by a constant voltage as shown in Fig. 52. At two different logic states, the different input currents cause the input node X of the second stage to have different voltages, which means that the drain-to- source voltage of $M_3$ is different at the two logic states. Because of the channel- length-modulation effect, the bias current supplied by $M_3$ is different. If

$$I_{ds3} = \beta_3(V_{gs3} - V_{t3})^2(1+\lambda V_{ds3}), \tag{85}$$

then the current difference between the two logic states is

$$\Delta I = \lambda I_0 \Delta V_{ds3} \tag{86}$$

where $I_O = \beta_3(V_{gs3}-V_{t3})^2$ is the ideal bias current. On the ground line, the bias current flows either through $M_2$ or through $M_4$, and so the total ground current always equals the bias current I. Due to the channel-length modulation effect, the difference in the ground current is the same as the difference in the power supply

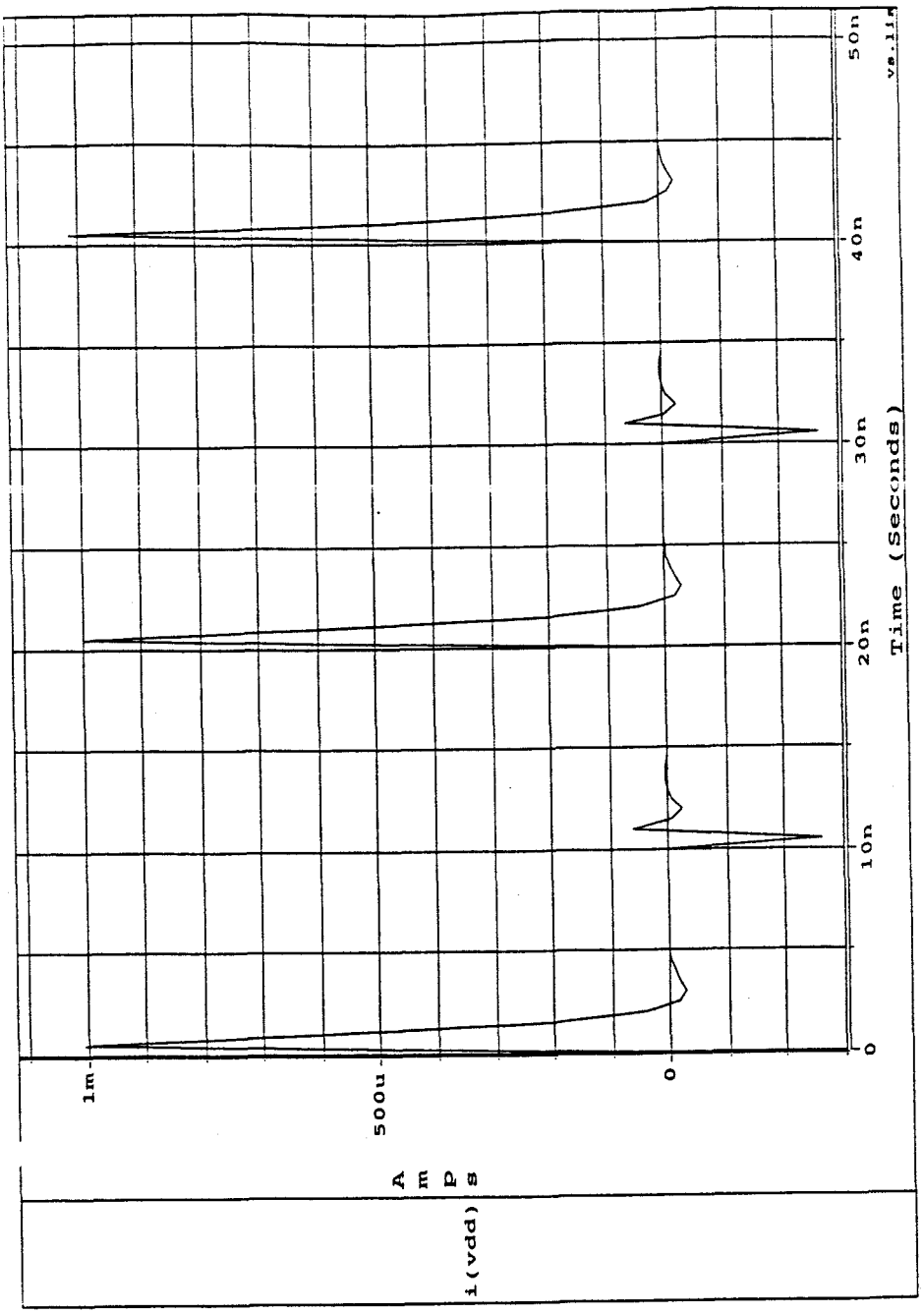



Fig. 51 Simulated $V_{dd}$ current spike of static CMOS inverter with Vdd = 5V, $(W/L)_n$ = 10μm/2μm, $(W/L)_p$ = 6μm/2μm, and $C_L$ = 0.1pf.

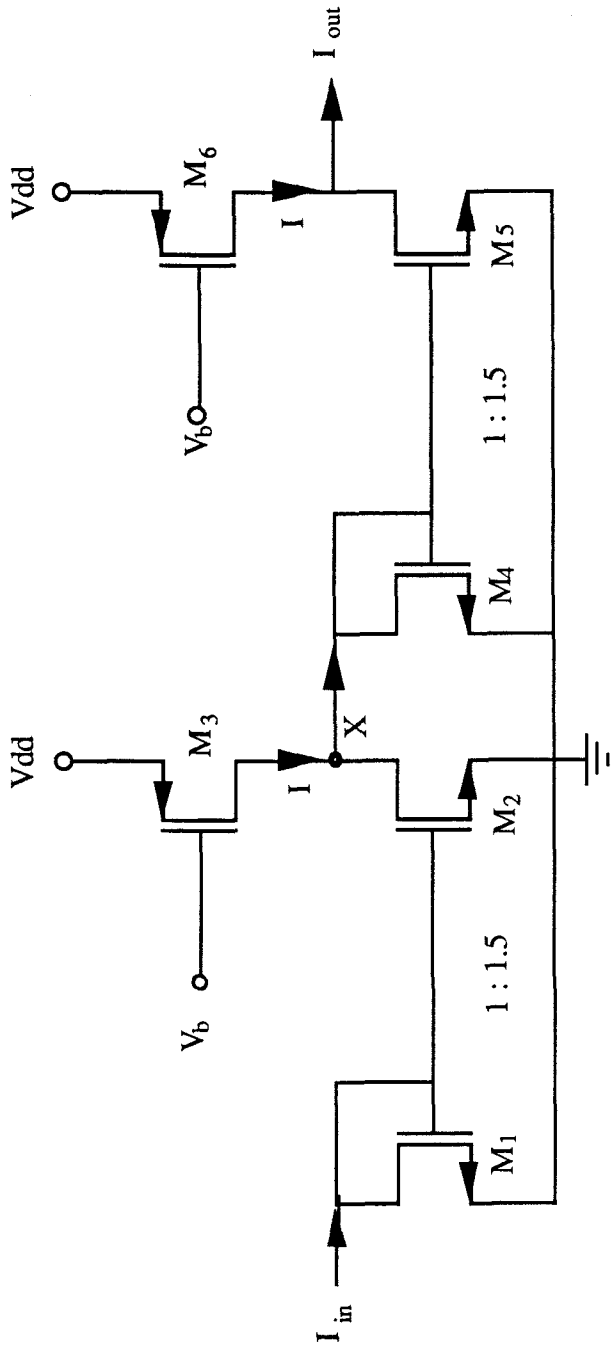



Fig. 52 Cascaded current-steering inverters with fanout of one, $(W/L)_1=(W/L)_4=4\mu m/2\mu m$, $(W/L)_2=(W/L)_3=(W/L)_5=(W/L)_6=6\mu m/2\mu m$, Vdd = 5V, and bias current I=135μA.

current, ΔI. For example, if the ideal bias current = 100 μA, and the difference of drain voltage $\Delta V_{ds3}$ at two logic states is 1 volt, and the channel-length modulation coefficient of a 2 μm PMOSFET is 0.056 $V^{-1}$, then the power supply and ground current differences are both ΔI = 5.6 μA.

The second source of Vdd current spikes is due to the charging or discharging of the drain to substrate capacitor of $M_3$, $C_{db3}$. Due to the different drain voltage level of $M_3$ at different logic states, whenever the circuit switches to a new logic state, $C_{db3}$ has to be charged or discharged to the new voltage, which causes a displacement current spike on the power supply. It can be expressed as

$$i_{sp} = C_{db3} \frac{dV_{ds3}}{dt} \tag{87}$$

Its peak amplitude is proportional to the highest slew rate of the drain voltage $V_{ds3}$, and the maximum value is reached when a constant current source charges the capacitance of input node. For example at node A, the current spike can be expressed as

$$i_{spmax} = \frac{C_{db3} I}{C_L} \tag{88}$$

where $C_L \approx C_{db2} + C_{gd2} + C_{gs4} + C_{gs5} + C_{gb4} + C_{gb5} + C_{db4} + C_{db3} + C_{gd3}$. Because $C_{db3} \ll C_L$, then $i_p \ll I$. On the ground line, because of the high capacitance $C_L$, between the output node and ground the current spike should have the same value as the bias current. But in above analysis, it was assumed that the previous stage turned off instantaneously, and all bias current is used to charge the capacitance. In practice, the previous stage is turned off gradually and only a portion of the bias current is used to charge the capacitance. So the ground current spike is still less than the bias current. Fig. 53 shows the simulation result of power supply and ground current spike generated by current-steering inverter, and Fig. 54 shows the measured total current spike at the power supply and ground of a 2 μm

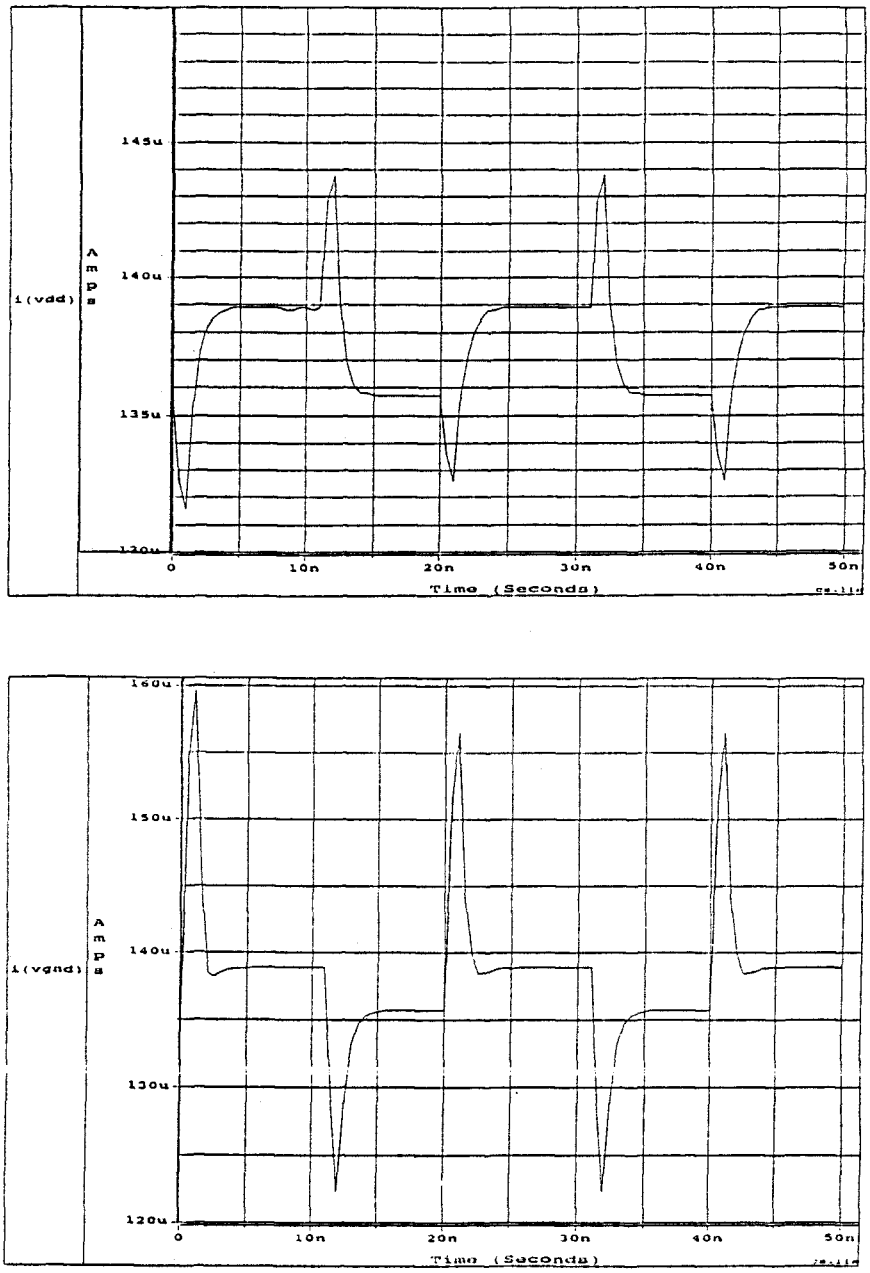



Fig. 53 Simulation results of current-spike for circuit of Fig. 52.

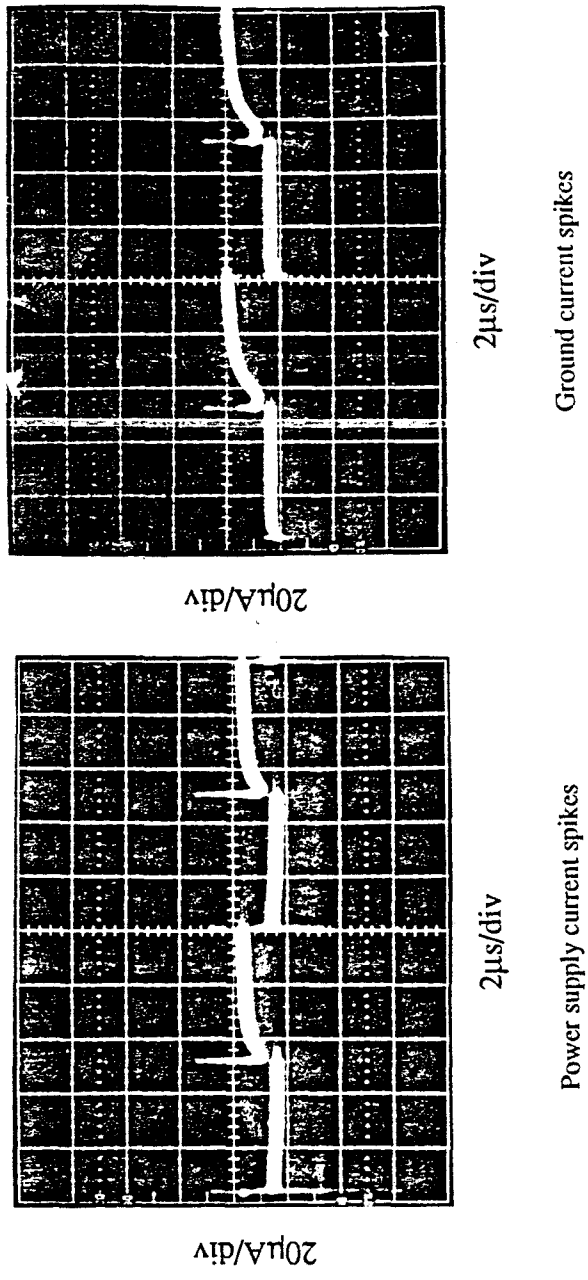



Fig. 54 Measured current spike of a current-steering inverter, with $(W/L)_1 = (W/L)_4 = 4\mu m/2\mu m$, $(W/L)_2 = (W/L)_3 = (W/L)_5 = (W/L)_6 = 6\mu m/2\mu m$, Vdd = 5V, and bias current I=125μA.

CMOS current-steering inverter. When the bias current I = 125μA, the power supply has less than 20 μA current spikes, compared to the 1mA spike of conventional CMOS logic. If cascode current source is used to replace the simple PMOS current source, the first component of current spike can be further reduced.

# CHAPTER 5. CONCLUSIONS

A new CMOS logic family called current-steering logic has been developed which uses current instead of voltage to represent the logic states. The current-steering logic circuits have several important advantages over conventional CMOS voltage logic circuits. First, its operation and performance are independent of power supply voltage. As long as the bias current is constant, it can interface with other logic circuits of different power supply. Second, although the nonideal current spike of current-steering circuits dissipate some dynamic power, it is much less than the constant power dissipated by the bias current. Compared to the conventional CMOS, at high frequency, it actually dissipates less power because of its smaller voltage swing. Third, under the same bias current, the operating speed is inversely proportional to the device size, and high speed can achieved by using a smaller channel length process. And finally, the current spike generated during the logic state transition is two order of magnitude smaller than that of conventional CMOS circuits, which substantially reduces the digital circuit interference in mixed-mode applications.

## SUMMARY

In this dissertation, two important current-mode circuit design and signal processing subjects have been explored. First, the emerging switched-current analog circuit technique has been investigated. The fundamental performance and limitations of this technique have been explored, and one of the major limitations, the linear gain error and signal distortion caused by clock feedthrough have been substantially reduced by a new clock feedthrough cancellation technique. In addition, a filter synthesis technique has been developed by directly simulating the structure of digital filters. This technique enables analog sampled-date filters to implement various types of digital filters including the linear phase FIR filter. Several experimental CMOS switched-current FIR filter prototypes have been designed and fabricated. The measured frequency and phase responses demonstrated the feasibility of this synthesis technique. Possible future research areas include the further exploration of the applications of digital signal processing techniques in analog sampled-data circuit design, such as the implementation of N-path filters, FFT bandpass filters, and high-order filter implementations.

In the second part of this thesis, a new logic family called current-steering logic has been developed. The fundamental performance and characteristics of this technique have been discussed including the basic inverter, NOR gate, the DC analysis, transient analysis, power supply noise analysis, etc. It has been shown that current-steering logic has a small power-delay product, and its current spike is about two orders of magnitude smaller than conventional CMOS static logic circuits. Experimental prototypes have verified the functionality and performance of this new technique. Possible areas for future research include optimum circuit

design for multiple fanout requirements, further reduction of ground current spikes, and implementation of other basic logic cells.

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