AN ABSTRACT OF THE THESIS OF

Giri NK Rangan for the degree of Master of Science in Electrical & Computer Engineering presented on June 22, 1993.

Title : High Speed Buffers for Op-amp Characterization

Abstract approved:_ Redacted for Privacy

John G. Kenney

The feasibility of developing test circuits to perform in-circuit testing of analog circuits is investigated in this thesis. A modular approach to analog testing has been adopted. Accordingly, the testing of an operational amplifier, which is a basic building block in analog circuits, is addressed. One convenient technique for measuring the frequency response of an op-amp requires a unity gain buffer to be inserted into its feedback loop. This buffer has to be simple in construction, small and accurate. Two buffer circuits that satisfy these requirements are described in this thesis. Enhanced slewing techniques are devised to achieve increased levels of performance. The buffers were integrated with an op-amp into a test chip. Digital logic is used to provide controllability and accessibility to each of the buffers and the op-amp so that they can characterized separately.

The performance of the enhanced slewing buffers was verified with measurements performed on the test chip. The performance of the buffers conformed well with the simulated values. The buffers exhibited excellent settling times even while driving large capacitive loads. Their output swing and distortion performance were good for inputs as large as 2 V peak-to-peak values.

High Speed Buffers for Op-amp Characterization

by

Giri NK Rangan

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Completed June 22, 1993.

Commencement June 1994.

APPROVED :

Redacted for Privacy

Professor of Electrical and Computer Engineering in charge of major

Redacted for Privacy

Head, Department of Electrical and Computer Engineering

Redacted for Privacy

Dean of Graduate School

Date Thesis is presented June 22, 1993

Thesis typed by Giri NK Rangan

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (continued)

LIST OF TABLES

Chapter 1. Introduction

Testing is an important stage in the design cycle of an integrated circuit. It is also the most time consuming stage. Large amounts of research has gone into simplifying the task of the test engineer. This research has been varied ranging from development of test generation tools in software to defining new design concepts with testing in perspective. Two important developments in this direction are the *Design for Testability* (*DFT*) and the *Built-in Self Test* (*BIST*) [6] techniques. The underlying principle in these methods is to integrate test principles into the design phase so that test-time is greatly reduced. Both of the above techniques are intended to provide greater controllability and observability of the critical nodes in an IC. Many of the performance parameters can be measured easily if voltage, current or logic values can be controlled or accessed easily.

In the digital world, *DFT* and *BIST* have become standard. Some of the notable test methods using *DFT* and *BIST* techniques are the *Level Sensitive Scan Design* and the *Boundary Scan Design* [6]. The reason for such quick developments in test designs and their standardization is that digital design in itself has become standardized and modular. Also, much research has gone into developing fault models for digital circuits. The fault models predict the observable anomalies in a design due to the occurence of some faults in the circuit. Fault modeling is simpler for digital circuits as only logic values are involved. Using these fault models, the error in a circuit can be accurately predicted even before the final silicon is obtained. The observed results are then compared with the predicted results to locate a fault in the circuit.

Such fault models, unfortunately, have not yet been developed for analog circuits. Some amount of research has been done in this direction, but the inherent complexity and

the varied functions performed by analog circuits make the development of fault models difficult. A large number of parameters are found in even the simplest of the analog blocks such as op-amps which are impossible to fully model. Moreover, analog functions are closely controlled by the circuit parameters like device sizes, bias currents and voltages, parasitic capacitances, values of the supply voltages etc. This dependency makes the development of fault models very difficult.

The motivation behind this work is to investigate the prospects of adapting or developing *DFT* techniques for analog integrated circuits. As mixed mode ICs incorporating both analog and digital functions on the same chip become more prevalent, the demand for inexpensive analog testing techniques, preferably using digital testers, becomes even more significant from the standpoint of production costs. In the work described in this thesis, circuits have been designed to be integrated with an operational amplifier so that the frequency response of the op-amp can be accurately characterized. The main requirements of a test circuit are: the size of the test circuit must be much smaller in comparison to the block it is meant to test — inclusion of test means increasing the die size which increases the cost of the IC; the test circuit should not degrade any of the characteristics of the block under test – any change thus introduced could alter the functionality of the block as well as the overall system which defeats the whole purpose of testing; the accuracy of the test outputs depends upon the accuracy of the test circuit added to a design. For example, in order to test an op-amp with a particular bandwidth, the test circuit added should have bandwidths larger than that of the op-amp to avoid erroneous measurements.

Several test and measurement techniques have been devised to characterize the parameters of an operational amplifier. In one of the techniques, which can be used to measure the DC gain, the Frequency Response and the Common Mode Rejection Ratio (CMRR), the important test circuit needed is a unity gain buffer. Many unity gain buffer designs have been reported for various applications before [4]. Described in detail in this

thesis are two buffers which show excellent performance and provide the necessary bandwidth to test op-amps with large bandwidths. These circuits are extremely simple and satisfy the three conditions mentioned previously. The succeeding chapters describe the design, analysis and the performance of each of these circuits.

This thesis is organized as follows. Chapter 2 describes the issues involved in testing an operational amplifier. Some of the frequency response measurement techniques are described. Also, the reason for including the buffer in the feedback loop of the op-amp test system is explained. Some of the salient requirements of the buffer are highlighted. Chapter 3 describes the design and analysis of the buffer circuits. Chapter four presents the simulation results obtained for each of the buffers. The thesis ends with a conclusion that summarizes the results of this work and also presents a note on future work in the area of analog testing.

Chapter 2. Op-Amp Testability Issues

This chapter reviews some of the important issues involved in testing an operational amplifier. Normally, two kinds of tests are performed on integrated circuits. One is the functional test and the other, the characterization test. Verification of the functional integrity of a circuit constitutes functional testing. Characterization testing involves measuring the performance parameters of the circuit and verifying that they conform to the designed values. Characterization tests are more complex, time consuming and expensive. In this chapter, some of the techniques to characterize the frequency response of an op-amp are discussed. One of the methods addresses the effect of non-idealities of the op-amp at high frequencies when measuring its frequency response. It also proposes a solution which requires a unity gain buffer whose specifications are also discussed in this chapter.

2.1 Op-amp parameter measurements.

As more analog functions are integrated in a single integrated circuit, a cell based test approach to such analog systems gains significance. Cell based testing is a bottom-up approach to test a system in which the different functional modules that constitute the system are tested individually. The operational amplifier is a fundamental building block in almost all analog systems. Hence, simple strategies for measuring the performance parameters of an op-amp are important.

The op-amp has a large number of parameters. Some of the important ones are its frequency response, slew rate, settling time, input offset voltage and the common mode range. The application for which an op-amp is used decides which of these parameters are critical. For op-amps used in switched capacitor circuits, the important parameters are its offset voltage, dc gain and the unity gain bandwidth. Design techniques like offset cancellation have been implemented that try to make the functionality of a circuit as little dependent on the op-amp parameters as possible. However, the op-amp's parameters closely control a circuit's operation and the measurement of these parameters is crucial in estimating the performance of the circuit.

2.2 Frequency response measurement techniques.

In most designs, the performance of the op-amp is assumed to be ideal. For instance, the differential-mode open-loop gain of the op-amp is assumed to be very high. This assumption, however, is reasonable only at low frequencies. At high frequencies, the gain of the op-amp is reduced to ensure stability.

Since the op-amp gain is so high, measurement of the gain response cannot be done when the op-amp is in open-loop. Even very small voltages at the inputs of the op-amp will cause the output to saturate at the supply voltages. Hence, in the conventional gain response measurement techniques, the op-amp is connected in a closed loop. Some of the frequently used methods are described in [2].

In one method, the op-amp is connected in an inverting amplifier configuration. The circuit connection along with the small signal equivalent circuit of the op-amp is shown in figure 2.1. In this figure, Z is the output impedance of the op-amp. Neglecting the effects of the offset voltage of the op-amp, a relation for the ratio (V_{out}/V_{neg}) can be obtained. Considering just the controlled voltage source along with Z and R_1 and recognizing that the value of the controlled voltage source is ($-A_v V_{neg}$),

$$-A_v V_{neg} = V_{out} + iZ$$

where $i = \dfrac{V_{out} - V_{neg}}{R_1}$.

Substituting for i and solving for the ratio (V_{out}/V_{neg}), we get

$$G(\omega) \cong \frac{V_{out}(\omega)}{V_{neg}(\omega)} = -\frac{A_v(\omega) - \dfrac{Z}{R_1}}{1 + \dfrac{Z}{R_1}} .$$

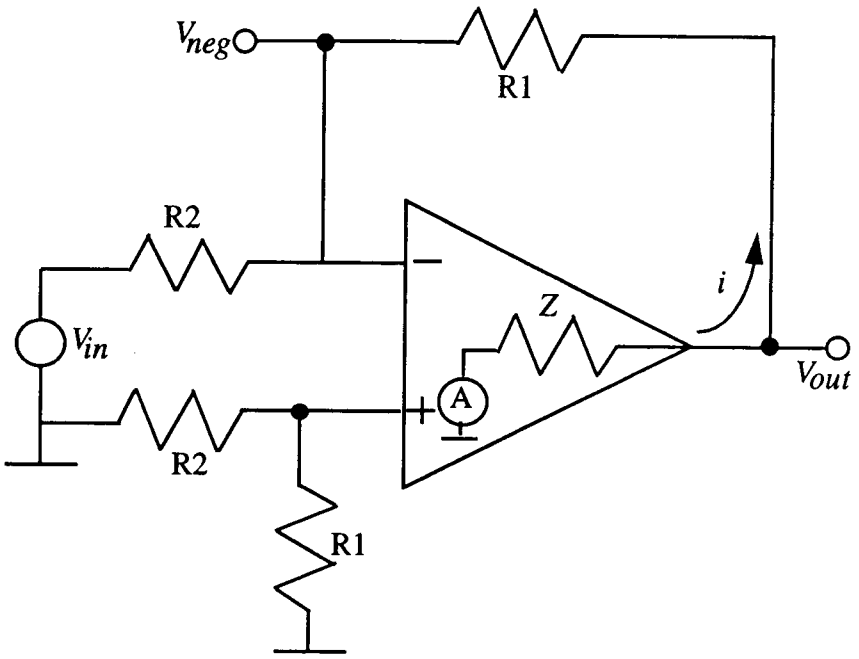


Fig 2.1. Conventional test circuit to measure open-loop gain response of an op-amp.

The above equation shows that the signal produced by the op-amp at high frequencies, where the value of $A_v(\omega)$ is very low, can be smaller than the feedthrough of the input signal through R_1. Consequently, a parasitic feed-forward path is established from the inverting input to the output of the op-amp. In an experimental measurement described in [2], the effect of the output impedance was demonstrated using an LM741 op-amp. An increase in the gain response was detected just above 1MHz (which is the unity gain frequency of LM741) indicating the presence of a parasitic zero in the frequency response. Secondly, for single stage op-amps that do not use an output stage (eg., a folded cascode op-amp), the value of Z is large even at lower frequencies and in such cases, the gain measured by the above method is clearly different from the actual value.

2.3 Frequency response characterization using unity gain buffer.

The errors caused by the non-ideal behaviour of the op-amp can be eliminated if the parasitic feed-forward path is removed from the op-amp in closed loop. The solution is

to include a unity gain buffer in the feedback loop of the test circuit as shown in figure 2.2. The buffer, while maintaining the voltage feedback path between V_{out} and V_{neg}, eliminates the feed-forward path.

The buffer is modelled as having a gain very close to 1, with a large input impedance Z_{ib} and a small output impedance Z_{ob}. Some of the conditions that need to be satisfied in order to use this test setup are: $R_1 >> Z_{ob}$ and $Z_{ib} >> Z$. Under these conditions, the differential gain A_v is just the ratio (V_{out}/V_{neg}).

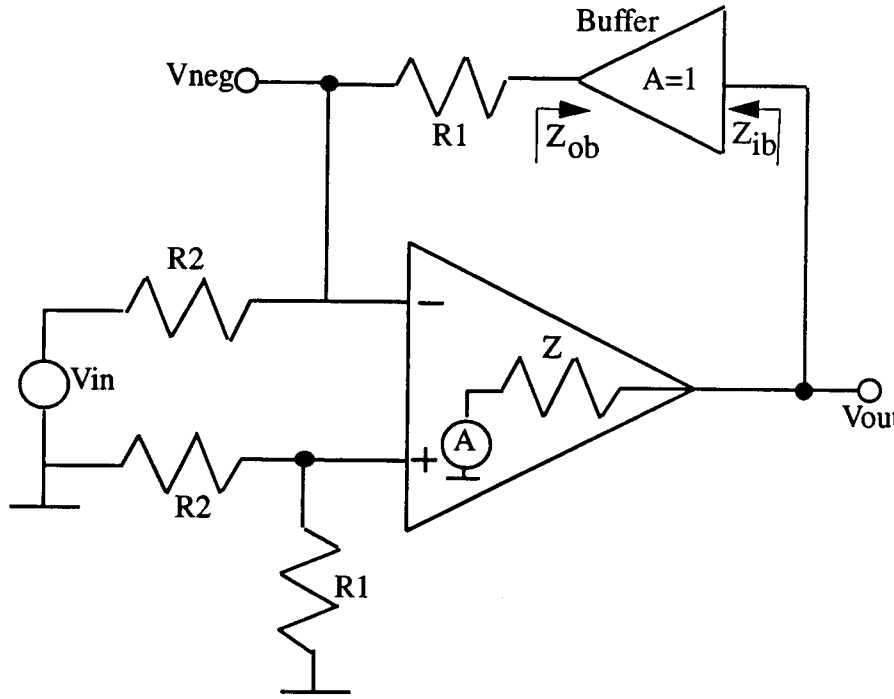


Fig 2.2. Op-amp test circuit with buffer in the feedback loop

All of the above requirements are easily satisfied in CMOS circuits. The input impedance of a MOS transistor is extremely large as only a small capacitance is seen at the gate of the MOSFET. Hence, even if the op-amp does not contain an output stage, Z_{ib} will be much larger than Z. In order to satisfy condition 1 and also ensure a reasonably small value of R_1, Z_{ob} must be as small as possible. The buffers described in chapter 3 exhibit output impedances on the order of 600 Ω. Accordingly, the value of R_1 is 50 kΩ.

As the buffer is needed at high frequencies, the bandwidth requirements of the buffer are important. Obviously, the 3-db frequency of the buffer can not be less than the unity gain frequency of the op-amp. Two serious problems arise if such a case were to occur. For starters, at frequencies close to op-amp's unity gain frequency, the gain of the buffer will be significantly less than 1 and the output of the buffer will no longer be same as V_{out}. Secondly, at frequencies close to its 3-dB point, the buffer introduces appreciable phase shift which poses stability problems in the circuit. Hence, the bandwidth of the buffer must be much larger than the unity gain bandwidth of the op-amp. For CMOS op-amps used in present IC processes, the bandwidths are of the order of 10-50 MHz making the bandwidth requirement of the buffer about 200 MHz.

The output of the op-amp will often swing between large amplitudes even at reasonably high frequencies. This requires that the buffer have a large output swing, high linearity, large bandwidth and a large slew rate. Any non-linearity will introduce excessive harmonic distortion which is undesirable. Moreover, as the op-amp output swings over a large voltage range, the output of the buffer should be able to dynamically follow the op-amp's output as closely as possible, which requires the buffer to have a large slew rate.

The subsequent chapters focus on two unity gain buffer designs. Since these buffers are intended for op-amp characterization, issues related to the kind of passive circuitry required to make the op-amp measurements will be formulated. Simulated and measured results will also be presented.

Chapter 3. The High Speed Buffer Circuits

This chapter describes the theory and implementation of enhanced slewing buffer circuits. The simplest unity gain buffer in MOS technology, the source follower, is presented first and analyzed to bring out its drawbacks. Two buffer circuits are proposed as a alternative to the source follower.

3.1 The source follower.

The circuit diagram for a basic source follower is shown in figure 3.1. The n-channel MOSFET $M1$ is the input transistor and the n-channel MOSFET $M2$ acts as a constant current source. Figure 3.2 shows the small signal dc equivalent circuit of the source follower. In this circuit, the body effect on $M1$ has been neglected as its substrate is connected to its source. In a p-well process, this is achieved by placing $M1$ in a separate p-well. Applying KCL at the output node yields,

$$-g_{m1}(v_{in} - v_{out}) + v_{out}g_{d1} + v_{out}g_{d2} = 0 \quad (1)$$

$$v_{out}(g_{m1} + g_{d1} + g_{d2}) = g_{m1}v_{in} \quad (2)$$

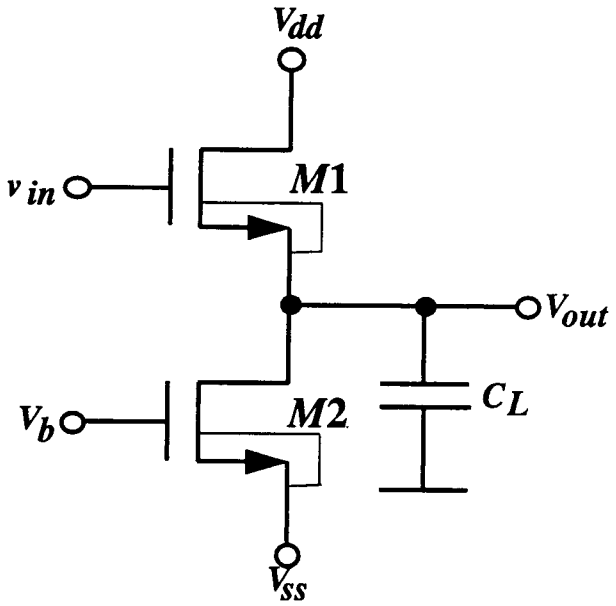


Fig 3.1. The source follower buffer.

From the above equation, we get for v_{out}/v_{in},

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{d1} + g_{d2}} . \tag{3}$$

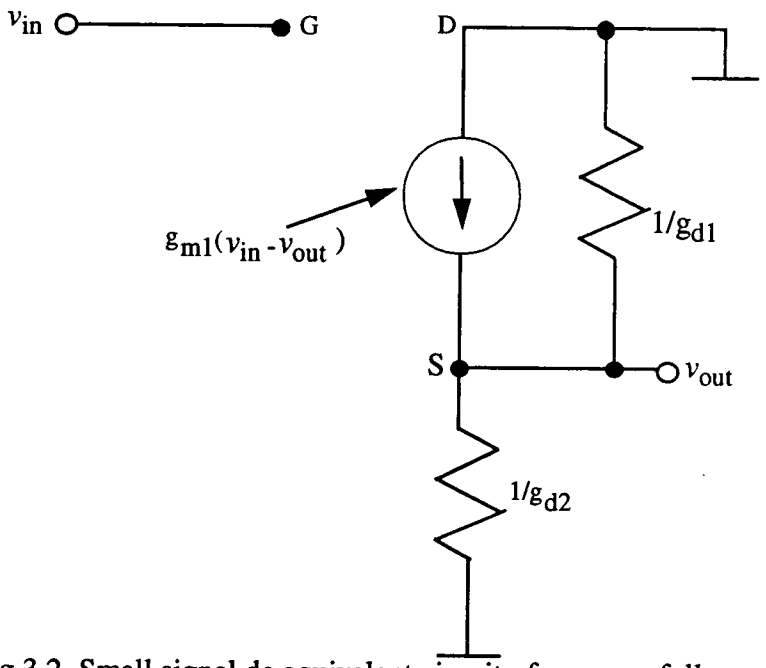


Fig 3.2. Small signal dc equivalent circuit of a source follower

Normally, $g_{m1} >> g_{d1}, g_{d2}$. Under such conditions, the gain of the circuit can be made very close to unity. One way to achieve this is to increase the width of the transistor $M1$. By increasing the width of $M1$ the overlap and the junction capacitances at the source and the drain nodes are increased as well. This increases the total capacitance at the output node thereby reducing the bandwidth of the circuit. The output resistance of this circuit can be determined by applying a test voltage at the output and connecting its input to ground [1]. A simple nodal analysis at the output shows that the output resistance is given by,

$$\frac{v_o}{i_o} = \frac{1}{g_{m1}} \tag{4}$$

where the g_d's of the two transistors are neglected. Normally, the g_m of a MOSFET will be of the order of few tenths of mmhos which makes the output resistance for the source follower to be around a few kΩ.

The frequency response of the source follower can be determined by adding the parasitic capacitances and the load capacitance to the circuit. The resulting ac equivalent circuit is indicated in figure 3.3. In this figure, the gate-to-drain capacitance C_{gd1} of $M1$ appears between the input node and ground so it can be neglected if the output impedance of the previous stage is small. The gate-to-drain capacitance and the drain-to-substrate capacitance of the transistor $M2$ are much smaller than C_L and are hence neglected. Applying KCL at the output node, we obtain

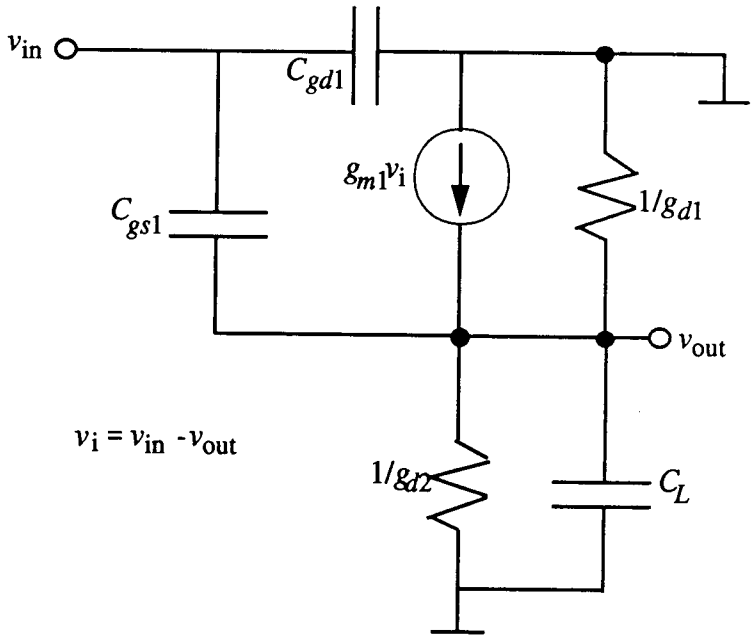


Fig 3.3. AC small signal equivalent circuit of a source follower

$$sC_{gs1}(v_{in} - v_{out}) + g_{m1}(v_{in} - v_{out}) - v_{out}(g_{d1} + g_{d2}) - sC_L v_{out} = 0 \qquad (5)$$

from which we can obtain the s-domain transfer function for the circuit to be,

$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{g_{m1} + sC_{gs1}}{(g_{m1} + g_{d1} + g_{d2}) + s(C_L + C_{gs1})} \qquad (6)$$

Normally, $C_L >> C_{gs1}$ and hence C_{gs1} can be neglected in the denominator of (6). From the above equation, the pole frequency occurs at $f_p = \frac{g_{m1} + g_{d1} + g_{d2}}{2\pi C_L} Hz$ and the zero occurs at a frequency $(g_{m1}/2\pi C_{gs1})$. Since C_{gs1} is very small, the zero frequency is much

higher than the pole frequency. For $g_{m1} \approx 0.7mmho$, $C_{gs1} = 60$ fF and $C_L = 5$ pF, we get $f_p = 21$ MHz and $f_z = 1.8$ GHz. Thus $f_z >> f_p$ and does not affect the bandwidth of the circuit.

The ability of the source follower to respond to inputs with large amplitudes is explored now. The large signal behavior of the source follower depends upon the current that the circuit can source and sink to charge and discharge the output node. A serious drawback is noticed during this time. The transistor $M2$ operates as a constant current source. When a large negative-going input step is applied, the output tries to track the input, but is limited by this constant current source. For example, suppose that the output falls from 3 V to 0 V within 20 ns at a load capacitance of 5 pF. Assuming that the output slews for half the time and settles exponentially in the other half, the slewing current given by the formula $i = C\frac{dV}{dt}$ will be 750 μA. This amount of current cannot be sunk by $M2$ unless it is made extremely wide or the bias voltage is increased. Increasing the bias voltage reduces the output swing which is not desirable. Hence, the constant current source poses a limitation on the large signal behaviour of the source follower. Simulation results showed fall times of about 60 ns. This speed and the corresponding bandwidth do not match the requirements of the buffer presented in the previous chapter.

These drawbacks of the source follower have prompted the design of different buffer circuits for this application. The underlying principle in these designs is to dynamically control the slewing current to boost the discharge current supplied by $M2$ [3]. The following sections describe these circuits.

3.2 The current feedback buffer.

The circuit diagram of the first buffer is shown in figure 3.4. Transistors $M1$-$M6$ form the signal path while transistors $M7$-$M11$ establish a bias voltage at the gate of $M6$ thereby setting the operating current of the circuit.

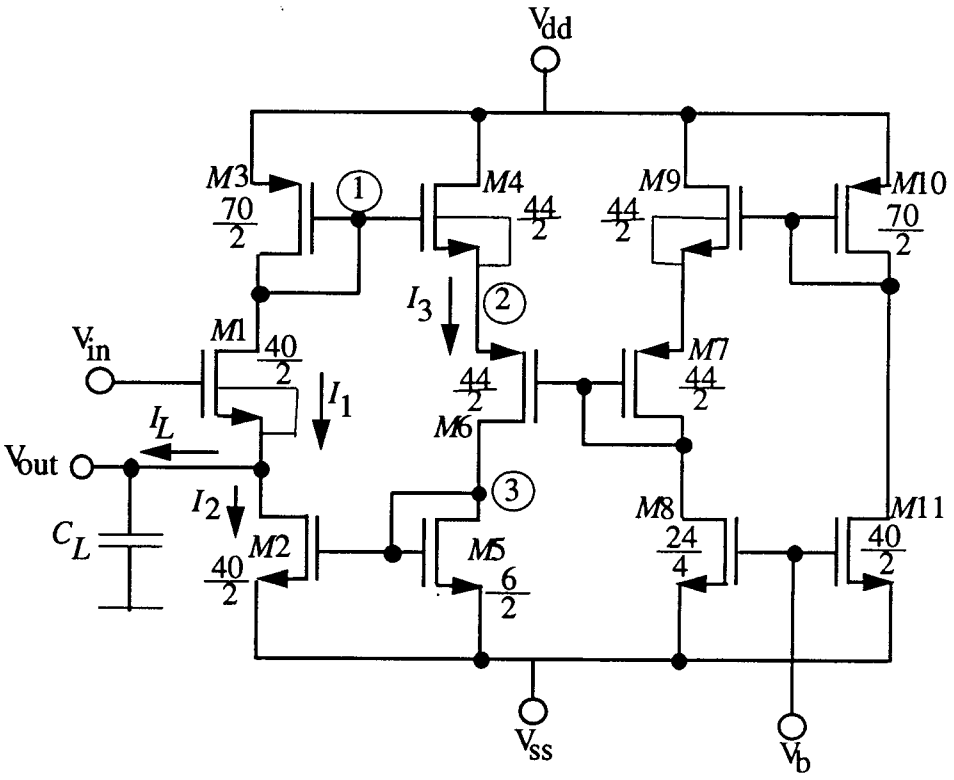


Fig 3.4. Circuit diagram of the current feedback buffer

3.2.1 Circuit Operation.

The large signal transient behavior of the circuit is explained here to bring out the way in which the boost in the slewing current is achieved. When V_{in} is suddenly increased, the response time at the output node is determined by the ability of the circuit to charge and discharge C_L quickly. Since a voltage V_{gs1} is required between the gate-source nodes of $M1$ to assure a quiescent current of $I1$, a voltage difference in which V_{in} - V_{out} > V_{gs1} will cause a current greater than $I1$ to flow through $M1$. This additional current charges the load capacitance, C_L. In addition, the increase in $I1$ results in a decrease in V_1. This decreases the V_{gs} of transistor $M4$ which in turn decreases $I3$. Since $M5$ and $M2$ form a current mirror, the decrease in $I3$ results in a proportional decrease in $I2$. Thus, more charging current can be driven into the load capacitance thereby decreasing the rise time of the circuit [3].

A negative going step input voltage presents a slightly different scenario. When V_{in} is decreased suddenly, the transistor $M1$ shuts off. This causes $v1$ to tend toward V_{dd}. As a result, the gate-source voltage of $M4$ increases because the voltage at node 2 is fixed by the bias at the gate of $M6$. The resulting increase in $I3$ is reflected as a large increase in $I2$ because of the ratioing of $M2$ and $M5$. Thus, a large discharge current is available and the load capacitance is discharged quickly [3].

3.2.2 DC analysis.

It is of interest to know how a current injected at the source of $M1$ would be related to the resultant current in $M2$. In order to do that, consider the simplified equivalent circuit shown in figure 3.5. In this figure, i_L is the load current injected at the output node of the buffer. The input of the circuit is grounded. Application of KCL at the output node yields,

$$i_L + i_1 - i_2 = 0. \tag{7}$$

KCL at node 1 gives,

$$-g_{m3}v_1 = i_1 \text{ or } v_1 = -\frac{i_1}{g_{m3}}.$$

Similarly, applying KCL at node 2, we get

$$g_{m4}(v_1 - v_2) = g_{m6}v_2.$$

Rearranging the above equation, we get,

$$v_1 = v_2\left(\frac{g_{m4} + g_{m6}}{g_{m4}}\right).$$

Application of KCL at node 3 gives,

$$g_{m5}v_3 = g_{m6}v_2$$

and from fig. 3.5, we also have $v_3 = \frac{i_2}{g_{m2}}$.

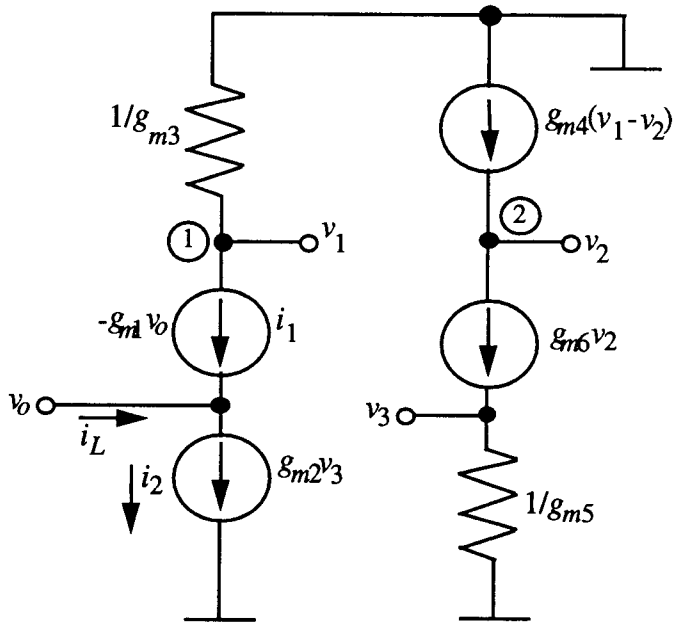


Fig 3.5. Small signal equivalent circuit of the buffer driven by a current source

Substituting for v_3 in the KCL equation at node 3 and substituting for v_1 and v_2 in the KCL equation at node 2, we arrive at the following relation between i_1 and i_2:

$$i_1 = -i_2 \frac{g_{m3}(g_{m4}+g_{m6})}{7g_{m4}g_{m6}}. \tag{8}$$

Substituting for i_1 in (7) and rearranging we get,

$$i_2 = i_L \frac{7g_{m4}g_{m6}}{7g_{m4}g_{m6}+g_{m3}(g_{m4}+g_{m6})}. \tag{9}$$

The above equation shows that as the device ratio between transistors $M2$ and $M5$ is made larger and larger, the gain from i_L to i_2 approaches unity. An adaptation of this circuit that makes use of the properties of the above equation is explained in chapter 5.

The low-frequency small signal equivalent circuit for the buffer is shown in figure 3.6. The body effect on $M6$ is neglected in this circuit. The other transistors have their bulks connected to the respective sources and hence do not have any body effect on them. The diode connected transistors $M3$ and $M5$ are modelled as resistances ($1/g_m$). Applying

KCL at the output node,

$$g_{m1}(v_{in} - v_{out}) + g_{d1}(v_1 - v_{out}) - g_{m2}(v_3) - g_{d2}(v_{out}) = 0, \tag{10}$$

that is,

$$g_{m1}v_{in} - v_{out}(g_{m1} + g_{d1} + g_{d2}) = g_{m2}v_3 - g_{d1}v_1. \tag{11}$$

Application of KCL at node 1 yields

$$-g_{m3}v_1 + g_{m1}(v_{out} - v_{in}) + g_{d1}(v_{out} - v_1) = 0 \tag{12}$$

In the above equation, solving for v_1 we get,

$$v_1 = \frac{(g_{m1} + g_{d1})\, v_{out} - g_{m1}v_{in}}{g_{m3} + g_{d1}}. \tag{13}$$

A similar expression for v_3 has to be found so that equation (11) can then be used to determine the overall transfer function. Applying KCL at node 2, we get,

$$g_{m4}(v_1 - v_2) - g_{d4}v_2 - g_{m6}v_2 + g_{d6}(v_3 - v_2) = 0 \tag{14}$$

Now applying KCL at node 3,

$$-g_{m5}v_3 + g_{m6}v_2 - g_{d6}(v_3 - v_2) = 0 \tag{15}$$

or,

$$v_2 = v_3 \frac{g_{m5} + g_{d6}}{g_{m6} + g_{d6}}. \tag{16}$$

Substituting for v_2 in (14) and solving,

$$g_{m4}v_1 - v_3\left(\frac{(g_{m5} + g_{d6})\,(g_{m4} + g_{m6} + g_{d4} + g_{d6})}{g_{m6} + g_{d6}} - g_{d6}\right) = 0. \tag{17}$$

The product $g_{m6}g_{d6} \gg g_{d6}^2$ and hence the square term can be neglected. Rearranging the equation after neglecting the square term, we have

$$v_3 = v_1 \frac{g_{m4}g_{m6}}{g_{m5}(g_{m4} + g_{m6}) + g_{m4}g_{d}}. \tag{18}$$

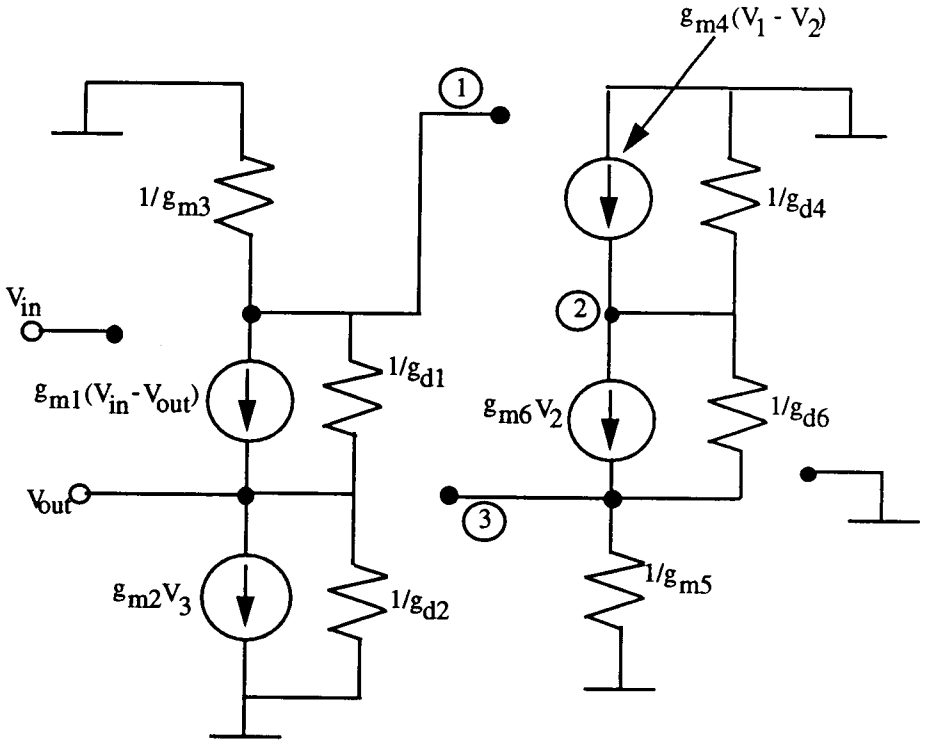


Fig 3.6. Low frequency, small signal equivalent circuit of the buffer

Let, $K = \dfrac{g_{m4}g_{m6}}{g_{m5}(g_{m4}+g_{m6})+g_{m4}g_{d6}}$. In equation (13), if the drain conductance g_{d1} is neglected in comparison to g_{m1} and g_{m6}, we get $v_1 = \dfrac{g_{m1}}{g_{m3}}(v_{out}-v_{in})$. Substituting for v_1 given in (13) into (18), we get v_3 as a function of v_{in} and v_{out}. Then substituting for v_3 and v_1 into (11) and rearranging, we get the following expression in terms of v_{in} and v_{out}:

$$v_{out}\left(K\frac{g_{m1}g_{m2}}{g_{m3}}-\frac{g_{m1}g_{d1}}{g_{m3}}+(g_{m1}+g_{d1}+g_{d2})\right)=v_{in}\left(K\frac{g_{m1}g_{m2}}{g_{m3}}-\frac{g_{m1}g_{d1}}{g_{m3}}+g_{m1}\right.$$

At this stage, we can make some approximations and get a simplified expression for the low frequency gain of the circuit. In the expression for K, we can safely neglect the product $g_{m4}g_{d6}$ owing to the fact that g_{d6} is very small. In addition, we have $g_{m2} >> g_{d1}$ and since $K > 1$, we can safely neglect g_{d1}. Incorporating these approximations, we get,

$$K = \frac{g_{m4}g_{m6}}{g_{m5}(g_{m4}+g_{m6})} \quad .$$

We can substitute for K and also note that the ratio g_{m2}/g_{m5} for this particular choice of device sizes is approximately 7. Then solving for the ratio (v_{out}/ v_{in}) we arrive at the following expression:

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}\left(1+\frac{7g_{m4}g_{m6}}{g_{m3}(g_{m4}+g_{m6})}\right)}{g_{m1}\left(1+\frac{7g_{m4}g_{m6}}{g_{m3}(g_{m4}+g_{m6})}\right)+g_{d1}+g_{d2}} \qquad (19)$$

In the above equation, if the output conductances of transistors $M1$ and $M2$ are made much smaller than the transconductance of $M1$, the dc gain of the circuit can be made close to 1.

A simple hand calculation can be done to get a value for the dc gain of the circuit. Appendix A contains the spice deck for the simulation of the buffer and also parts of the operating point simulations. From this, we have g_{m1} = 0.7 mmho, g_{m3} = 0.56 mmho, g_{m4} = 0.24 mmho, g_{m6} = 0.12 mmho, g_{d1} = 38 µmho and g_{d2} = 42 µmho. Then, $\frac{v_{out}}{v_{in}}$ = 0.95.

Output Resistance, R_o:

The next important parameter of the circuit, the output resistance, is now derived. The equivalent circuit necessary to derive the expression for R_o is shown in figure 3.7. Here, the input is grounded and the output is driven by a test voltage source. R_o is the ratio of the test voltage v_o to the test current i_o.As before, the diode connected transistors $M3$ and $M5$ are modelled as resistances ($1/g_m$). Applying KCL at the output node,

$$-g_{m1}v_o + g_{d1}(v_1 - v_o) + i_o - g_{m2}v_3 - g_{d2}v_o = 0 \quad .$$

Rearranging, we obtain

$$-v_o(g_{m1}+g_{d1}+g_{d2}) + i_o = g_{m2}v_3 - g_{d1}v_1 \; . \qquad (20)$$

An expression for v1 as a function of v_o is obtained by setting $v_{out} = v_o$ and $v_{in} = 0$ in equation (13). Accordingly we get,

$$v_1 = v_o \frac{g_{m1} + g_{d1}}{g_{m3} + g_{d1}} .$$

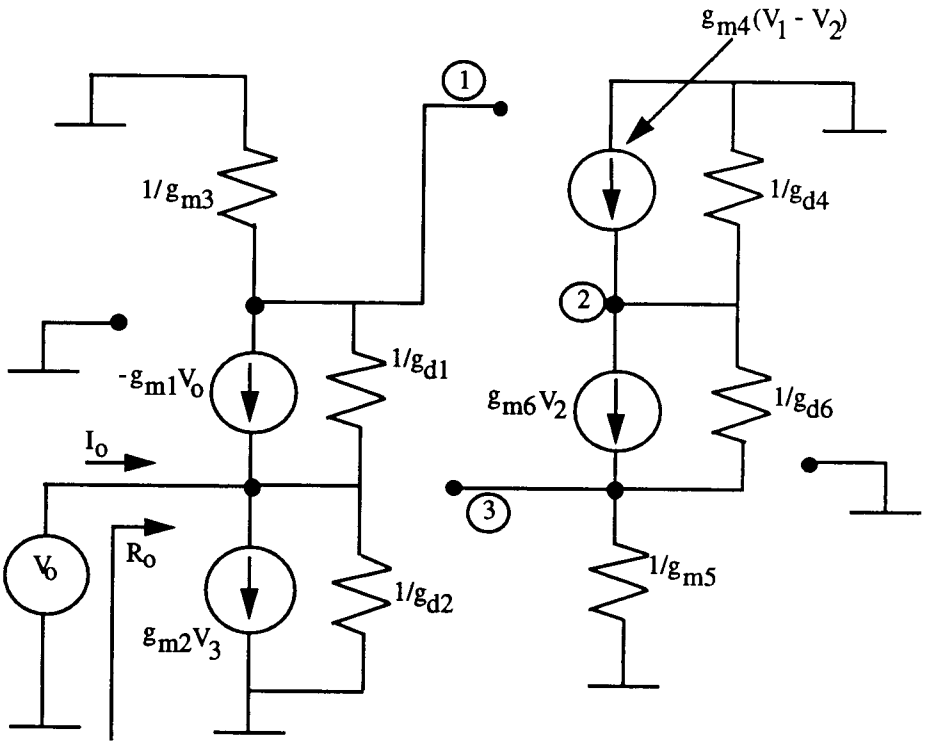


Fig 3.7. Equivalent circuit to find the output impedance of the buffer

Applying KCL again at node 2, we get

$$g_{m4}v_1 - (g_{m4} + g_{m6} + g_{d4} + g_{d6})\, v_2 + g_{d6}v_3 = 0 \qquad (21)$$

We notice that v_2 as a function of v_3 is obtained by applying KCL at node 3 and is given by the equation (16). Also, after substituting for v_2 in (21) and rearraning, we get v_3 in terms of v_1 as given by (18). If $g_{m4} >> g_{d4}$ and $g_{m6} >> g_{d6}$, (18) can be simplified to be,

$$v_3 = v_1 \frac{g_{m4}g_{m6}}{g_{m5}(g_{m4} + g_{m6})},$$

where the product $g_{m4}g_{d6}$ has been neglected in the denominator in comparison to the first term. Substituting for v_3 in (20), we get

$$-v_0(g_{m1}+g_{d1}+g_{d2})+i_o = v_1\left(\frac{g_{m2}g_{m4}g_{m6}}{g_{m5}(g_{m4}+g_{m6})}-g_{d1}\right)$$

and substituting for v_1 in terms of v_o and rearranging, we have

$$i_o = v_o\left(\left(\frac{g_{m2}g_{m4}g_{m6}}{g_{m5}(g_{m4}+g_{m6})}-g_{d1}\right)\left(\frac{g_{m1}+g_{d1}}{g_{m3}+g_{d1}}\right)+(g_{m1}+g_{d1}+g_{d2}),\right.$$

so that $R_o = (v_o/i_o)$ is given by,

$$R_o = \frac{1}{\left(\left(\frac{g_{m2}g_{m4}g_{m6}}{g_{m5}(g_{m4}+g_{m6})}-g_{d1}\right)\left(\frac{g_{m1}+g_{d1}}{g_{m3}+g_{d1}}\right)+(g_{m1}+g_{d1}+g_{d2})\right.}. \qquad (22)$$

In the above expression, g_{m2}/g_{m5} is approximately 7 and hence we can neglect g_{d1} in comparison with $g_{m4}g_{m6}/(g_{m4}+g_{m6})$ and also in comparison with g_{m1} and g_{m3}. The expression for R_o then reduces to

$$R_o = \frac{1}{g_{m1}\left(1+\frac{7g_{m4}g_{m6}}{g_{m3}(g_{m4}+g_{m6})}\right)}. \qquad (23)$$

If this expression is compared with (4), we notice that the ratio of R_o of a simple source follower to that of the current feedback buffer is $\left(1+\frac{7g_{m4}g_{m6}}{g_{m3}(g_{m4}+g_{m6})}\right)$. Using the values given previously, this ratio works out to be 2.2. Hence, a reduction in the output resistance has been achieved. Using the g_m values, we get $R_o \cong 649\Omega$.

The focus now shifts to determining the output swing of the buffer. A large output swing is desirable so that bigger signals can be applied with little distortion. The negative swing of the buffer is essentially controlled by the saturation voltage of *M2*. In order for *M2* to be in saturation, a drain to source voltage of atleast V_{dsat} is required. Hence we have, $(V_{out})_{\min} = V_{ss} + V_{dsatn}$. In order to find the maximum positive output swing, we recognize that the drain-to-source voltage of the transistor *M3* is at V_{dsatp}, which is also the gate-to-source voltage for *M3*. And from the gate of *M3* to the source of *M3*, we see a V_{tp}. For transistor *M1* to be in saturation, a voltage V_{dsat} is required between node 1 and the output node. Hence, we have for the output voltage,

$$(V_{out})_{\max} = V_{dd} - V_{dsatp} - V_{tp} - V_{dsatn} \tag{24}$$

3.2.3 AC analysis.

The high frequency, small signal equivalent circuit of the buffer can be written by adding the gate-source and the load capacitances to the dc equivalent circuit. Such an equivalent circuit is shown in figure 3.8. In this figure, the capacitance $C' = C_{gs2} + C_{gs5}$. Also, for simplicity, The output conductances of all the transistors have been neglected because they are substantially smaller than the transconductances.

Starting the analysis at the output node,

$$v_{in}(g_{m1} + sC_{gs1}) - v_{out}(g_{m1} + sC_L) = g_{m2}v_3, \tag{25}$$

where the condition $C_L >> C_{gs1}$ has been used. Applying KCL at node 1,

$$-v_1(g_{m3} + sC_{gs3}) - sC_{gs4}(v_1 - v_2) - g_{m1}(v_{in} - v_{out}) = 0,$$

from which we get,

$$-v_1(g_{m3} + sC'') + sC_{gs4}v_2 = g_{m1}(v_{in} - v_{out}), \tag{26}$$

where $C'' = C_{gs3} + C_{gs4}$.

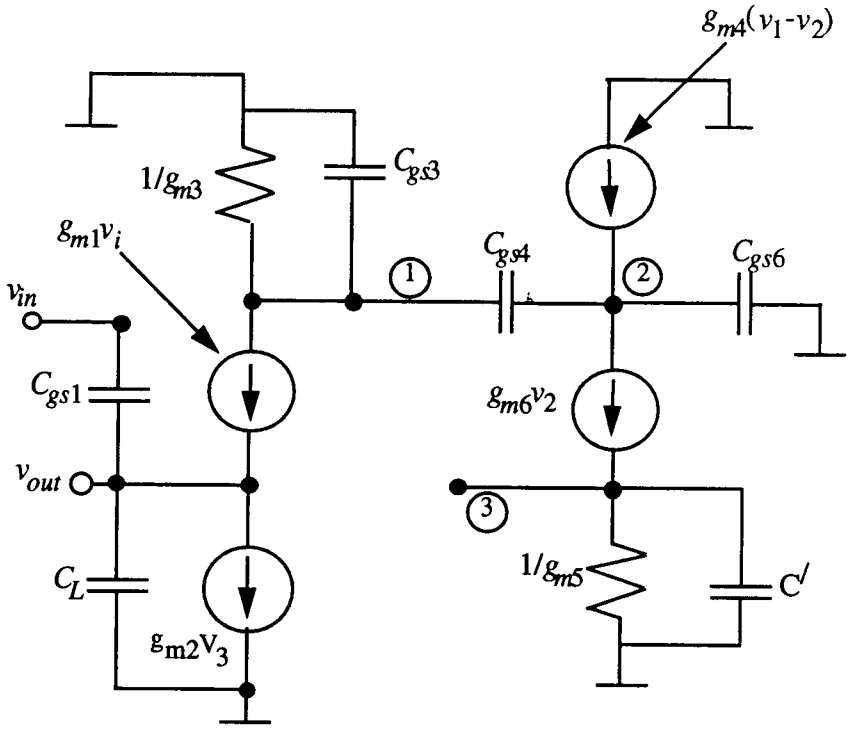


Fig 3.8. Small signal, ac equivalent circuit of the buffer

Now applying KCL at node 2,

$$g_{m4}(v_1 - v_2) + sC_{gs4}(v_1 - v_2) - v_2(g_{m6} + sC_{gs6}) = 0.$$

Rearranging the above equation and letting $C_{gs4} + C_{gs6} = C'''$, we get

$$v_2 = v_1 \frac{g_{m4} + sC_{gs4}}{g_{m4} + g_{m6} + sC'''}. \qquad (27)$$

Finally, applying KCL at node 3, we get

$$g_{m6}v_2 - v_3(g_{m5} + sC') = 0,$$

from which $v_3 = v_2 \frac{g_{m6}}{g_{m5} + sC'}$. Substituting for v_2 from (27) we get,

$$v_3 = v_1 \frac{g_{m6}(g_{m4} + sC_{gs4})}{(g_{m5} + sC')\ (g_{m4} + g_{m6} + sC'')}. \tag{28}$$

We now have expressions for v_2 and v_3 in terms of v_1. We can substitute for v_2 in (27) and for v_3 in (26) so that we get two expressions for v_1 in terms of v_{in} and v_{out}. We can then solve for the transfer function. Complex algebraic manipulations are involved in the process and a fourth order transfer function is obtained which is symbolically represented as:

$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{K + sa_1 + s^2a_2 + s^3a_3 + s^4a_4}{K + sb_1 + s^2b_2 + s^3b_3 + s^4b_4}. \tag{29}$$

The coefficients in the above equation are given below. It can be seen from the transfer function that the DC gain is 1 (note, however, that the g_d's have been neglected).

$$K = g_{m1}g_{m2}(g_{m4}g_{m6} + \frac{g_{m3}}{7}(g_{m4}+g_{m6})),$$

$$a_1 = g_{m1}g_{m3}(g_{m4}+g_{m6})C' + g_{m3}g_{m5}(g_{m4}+g_{m6})C_{gs1} + g_{m1}g_{m3}g_{m5}C''' + g_{m1}g_{m5}(g_{m4}+g_{m6})C'' + g_{m1}g_{m2}g_{m6}C_{gs4} - g_{m1}g_{m4}g_{m5}C_{gs4},$$

$$a_2 = g_{m3}(g_{m4}+g_{m6})C'C_{gs1} + g_{m1}g_{m5}(C''C''' - C^2_{gs4}) + (g_{m1}C'+g_{m5}C_{gs1})(g_{m3}C'''+(g_{m4}+g_{m6})C''-g_{m4}C_{gs4}),$$

$$a_3 = (g_{m1}C'+g_{m5}C_{gs1})(C''C''' - C^2_{gs4}) + C'C_{gs1}(g_{m3}C'''+(g_{m4}+g_{m6})C''-g_{m4}C_{gs4}),$$

$$a_4 = C'C_{gs1}(C''C''' - C^2_{gs4})$$

and

$$b_1 = g_{m1}g_{m3}(g_{m4}+g_{m6})C' + g_{m3}g_{m5}(g_{m4}+g_{m6})C_L + g_{m1}g_{m3}g_{m5}C''' + g_{m1}g_{m5}(g_{m4}+g_{m6})C'' + g_{m1}g_{m2}g_{m6}C_{gs4} - g_{m1}g_{m4}g_{m5}C_{gs4},$$

$$b_2 = g_{m3}(g_{m4}+g_{m6})C'C_L + g_{m1}g_{m5}(C''C''' - C^2_{gs4}) + (g_{m1}C'+g_{m5}C_L)(g_{m3}C'''+(g_{m4}+g_{m6})C''-g_{m4}C_{gs4}),$$

$$b_3 = (g_{m1}C'+g_{m5}C_L)(C''C''' - C^2_{gs4}) + C'C_L(g_{m3}C'''+(g_{m4}+g_{m6})C''-g_{m4}C_{gs4}),$$

$$b_4 = C'C_L(C''C''' - C^2_{gs4}).$$

The various values of the g_m's and the capacitances can be obtained from the spice output file included in Appendix A. The roots of the numerator, which are the zeros of the circuit were found to be (-1.7e10), (-3.5e9+j5.4e9), (-3.5e9-j5.4e9) and (-6.2e9). From these roots, the lowest zero frequency is found to be 900 MHz.

From the values obtained from Appendix A, the roots of the denominator, which are the poles of the circuit were found to be at (-6.4e9+j4.7e9), (-6.4e9-j4.7e9), (-1.6e9) and (-5.3e8). Accordingly, the frequency of the first pole is calculated to be about 85 MHz. Thus, the current feedback buffer exhibits a larger bandwidth than a simple source follower buffer. For the same values of g_{m1} and C_L, we notice that the bandwidth of the current feedback buffer is more than four times as large as that of a source follower.

From the above discussions, we can conclude that the buffer exhibits all of the characteristics required: high gain, high bandwidth, a large slew rate and a large output swing.

3.3 The Folded Cascode Buffer.

The circuit and the operation of the next buffer is based roughly on the principle of a folded cascode op-amp. Figure 3.9 shows the schematic of the folded cascode buffer. Transistors $M1$-$M5$ form the signal path while transistors $M6$-$M10$ set up the necessary bias voltages and currents.

3.3.1 Circuit operation.

The p-channel MOSFET $M5$ establishes a current I_b which is divided between the two signal paths formed by $M1$, $M2$ and $M3$, $M4$. The ratio in which the bias current is split between the two branches is decided by the relative sizes of $M2$ and $M3$.

A fast positive going step input to the circuit causes a dynamic increase in the current $I1$ and since I_b remains constant, there will be a corresponding decrease in the current $I2$. Hence, a greater fraction of I_b flows through $M1$ into C_L. For very large step inputs, $I2$

decreases substantially and since this current is mirrored into $M2$, $M2$ will turn off. In the limiting case, all of I_b flows through $M1$ into C_L thereby charging the output node quickly.

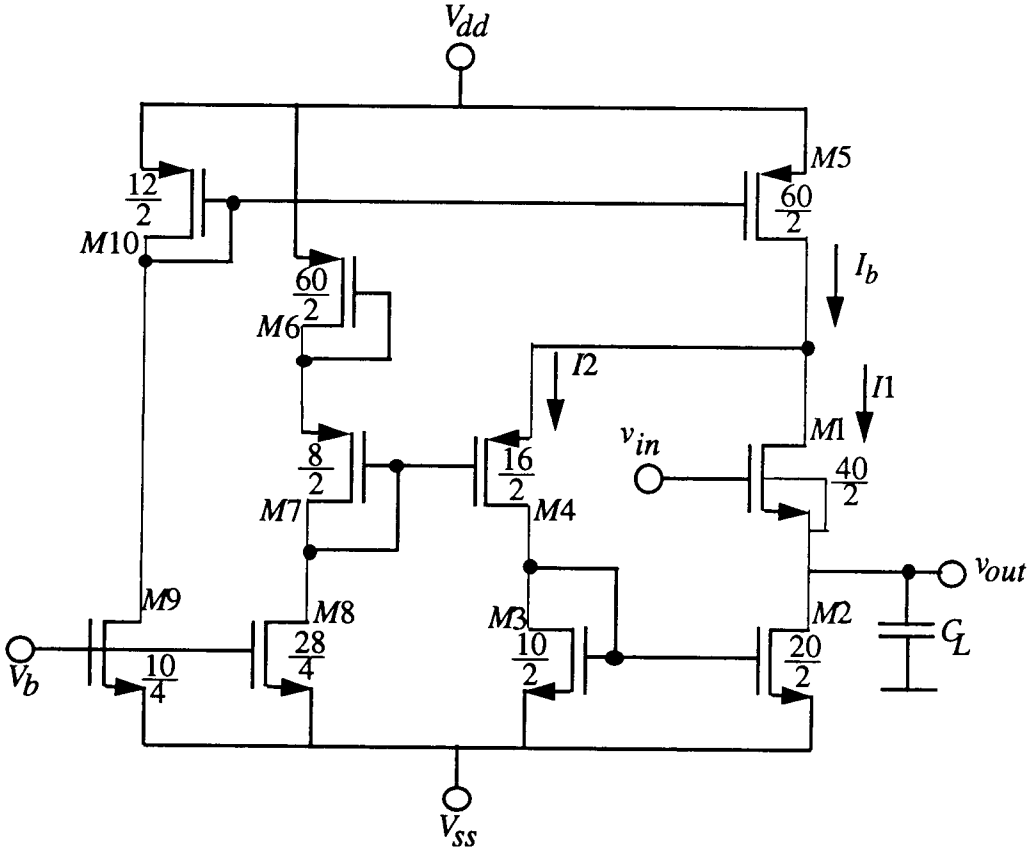


Fig 3.9. Circuit diagram of the folded cascode buffer

When a fast negative-going step is applied at the input, it causes transistor $M1$ to turn off. This causes a larger fraction of I_b to flow through $M3$ and $M4$. This additional current is mirrored by $M3$ into $M2$. Hence, a large current will flow through $M2$ and this results in the output node being discharged in a very small duration of time.

Ideally, the increase in slew rate in the negative direction can be obtained for equal sizes of $M2$ and $M3$. However, due to channel length modulation effects between $M2$ and $M3$, the increase in current in $M3$ will not be fully reflected in $M2$. Thus, a device ratio of greater than 1 should be allowed between $M2$ and $M3$ in order to achieve the predicted increase in the slewing current. In this particular implementation, a ratio of 2 was used. The independence of the drain current of the drain-to-source voltage of a MOSFET is only

approximate. A first order approximation of the drain current as a function o fthe drain-to-source voltage is given by:

$$I_D = \frac{K_n W}{2L}(V_{gs} - V_T)^2(1 + \lambda V_{ds}),$$

where λ is the channel length modulation factor. Due to this dependence of I_D on V_{ds}, the currents in two transistors of a simple current mirror like $M2$ and $M3$ will not be same even though their sizes and the V_{gs}'s are the same. In applications where it is necessary to have perfect current matching, current mirrors with higher output impedance like the Wilson's current mirror or the Cascode current mirror should be used. In our application, though, the importance is to have as much increase in the slewing current as possible through $M2$ and a ratio greater than 1 between the $M2$ and $M3$ serves this purpose well. Larger ratios betwen $M2$ and $M3$ will be impractical as it would make I_2 very small causing transistors to turn off or come out of saturation.

3.3.2 DC analysis.

The low-frequency, small signal equivalent circuit for the buffer circuit is shown in figure 3.10. Here, the transistor $M5$ has been modelled as a high resistance $1/g_d$ and the diode connected transistor $M3$ is modelled as a low resistance $1/g_m$. Application of KCL at the output node gives,

$$g_{m1}(v_{in} - v_{out}) + g_{d1}(v_1 - v_{out}) - g_{m2}v_2 - g_{d2}v_{out} = 0$$

$$g_{m1}v_{in} - v_{out}(g_{m1} + g_{d1} + g_{d2}) = g_{m2}v_2 - g_{d1}v_1 \qquad (30)$$

Applying KCL at node 1,

$$v_1(g_{m4} + g_{d1} + g_{d4} + g_{d5}) - v_2 g_{d4} - v_{out}(g_{m1} + g_{d1}) + g_{m1}v_{in} = 0. \qquad (31)$$

Finally, application of the current law at node 2 gives,

$$g_{m4}v_1 + g_{d4}(v_1 - v_2) - g_{m3}v_2 = 0.$$

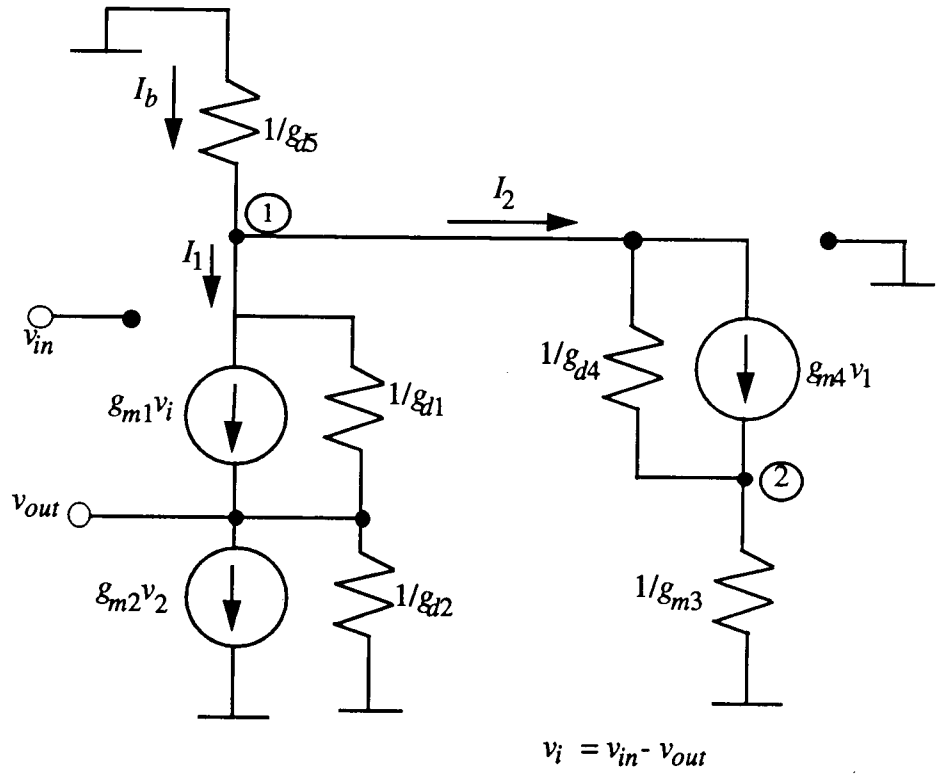


Fig 3.10. Low frequency, small signal equivalent circuit of the buffer

Rearranging the above equation, we get an expression for v_2 as a function of v_1 to be,

$$v_2 = v_1 \frac{g_{m4} + g_{d4}}{g_{m3} + g_{d4}}. \tag{32}$$

In the above equation, the drain or the output conductance g_{d4} may be neglected in comparison to g_{m3} and g_{m4}. Neglecting g_{d4} and substituting for v_2 in equation (31), we get

$$v_1 (g_{m4} + g_{d1} + g_{d4} + g_{d5}) - v_1 \frac{g_{m4}}{g_{m3}} g_{d4} = v_{out} (g_{m1} + g_{d1}) - g_{m1} v_i,$$

from which we get the following expression for v_1 in terms of v_{out} and v_{in}:

$$v_1 = \frac{g_{m1}}{g_{m4} + g_{d1} + g_{d4} + g_{d5}} (v_{out} - v_{in}) \quad . \tag{33}$$

In the above equation, the following approximations have been made : $g_{m1} >> g_{d1}$ and $g_{m3}(g_{m4}+g_{d1}) >> g_{m4}g_{d4}$. Equation (34) can be substituted into (33) so that an expression for v_2 in terms of v_{out} and v_{in} is obtained. We can then use that result along with (34) and (31) to come up with the low frequency transfer function for the circuit. Accordingly,

$g_{m1}v_{in} - (g_{m1} + g_{d1} + g_{d2})\, v_{out} =$

$$\frac{g_{m1}g_{m2}g_{m4}}{g_{m3}(g_{m4} + g_{d1} + g_{d4} + g_{d5})}(v_{out} - v_{in}) - \frac{g_{m1}g_{d1}}{g_{m4} + g_{d1} + g_{d4} + g_{d5}}(v_{out} - v_{in}) \ .$$

Let, $g' = g_{m4}+g_{d1}+g_{d4}+g_{d5}$. Also, recognize that $\frac{g_{m2}}{g_{m3}} \equiv 2$. Making these two substitutions into the above equation and rearranging in terms of v_{in} and v_{out}, we get

$$v_{in}(g_{m1} + \frac{g_{m1}}{g'}(2g_{m4} - g_{d1})) \ = v_{out}(g_{m1} + g_{d1} + g_{d2} + \frac{g_{m1}}{g'}(2g_{m4} - g_{d1})).$$

We can now make the approximation $2g_{m4} >> g_{d1}$ and drop the g_{d1} term from the above equation to get,

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1} + \frac{2g_{m1}g_{m4}}{g'}}{g_{m1} + g_{d1} + g_{d2} + \frac{2g_{m1}g_{m4}}{g'}}. \qquad (34)$$

In the above equation, if $g_{m1} >> g_{d1}$ and g_{d2}, we notice that the low-frequency gain can be made close to 1. This condition is similar to that for a source follower. If the value of g_{m4} can be made much larger than g_{d1}, g_{d4} and g_{d5}, equation (34) reduces to

$$\frac{v_{out}}{v_{in}} = \frac{3g_{m1}}{3g_{m1} + g_{d1} + g_{d2}},$$

which gives a dc gain much closer to unity than a source follower. However, the condition of g_{m4} being greater than the output conductances is hard to achieve because transistors $M1$ and $M5$ carry large currents and their output conductances will be substantial. (From simulations, g_{m1}=0.8 mmho, g_{m4}=0.17 mmho, g_{d1}=0.04 mmho, g_{d4}=0.02 mmho and g_{d5}=0.05 mmho). Using these values, we get a dc gain of 0.95.

Output resistance, R_o:

In order to find the output resistance of the buffer, the input is connected to ground and a test voltage source is applied at the output. Figure 3.11 shows a small signal equivalent circuit with the test voltage source. Applying KCL at the output node,

$$-g_{m1}v_o + g_{d1}(v_1 - v_o) + i_o - g_{m2}v_2 - g_{d2}v_o = 0.$$

Rearranging the above equation we get,

$$-v_o(g_{m1} + g_{d1} + g_{d2}) + i_o = g_{m2}v_2 - g_{d1}v_1. \qquad (35)$$

Similarly, application of KCL at node 1 gives,

$$v_1(g_{m4}+g_{d1}+g_{d4}+g_{d5}) - g_{d4}v_2 = v_o(g_{m1}+g_{d1}). \qquad (36)$$

Applying KCL at node 2 gives us an expression for v_2 in terms of v_1. This expression is already given by (33). In (33), the output conductance g_{d4} can be neglected so that $v_2 = v_1\frac{g_{m4}}{g_{m3}}$. The expresson for v_1 as a function of v_o is obtained by setting $v_{in} = 0$ and $v_{out} = v_o$ in (34). Accordingly, we get

$$v_1 = v_o\frac{g_{m1}}{g_{m4} + g_{d1} + g_{d4} + g_{d5}},$$

and $v_2 = v_o\frac{g_{m1}g_{m4}}{g_{m3}(g_{m4} + g_{d1} + g_{d4} + g_{d5}}$.

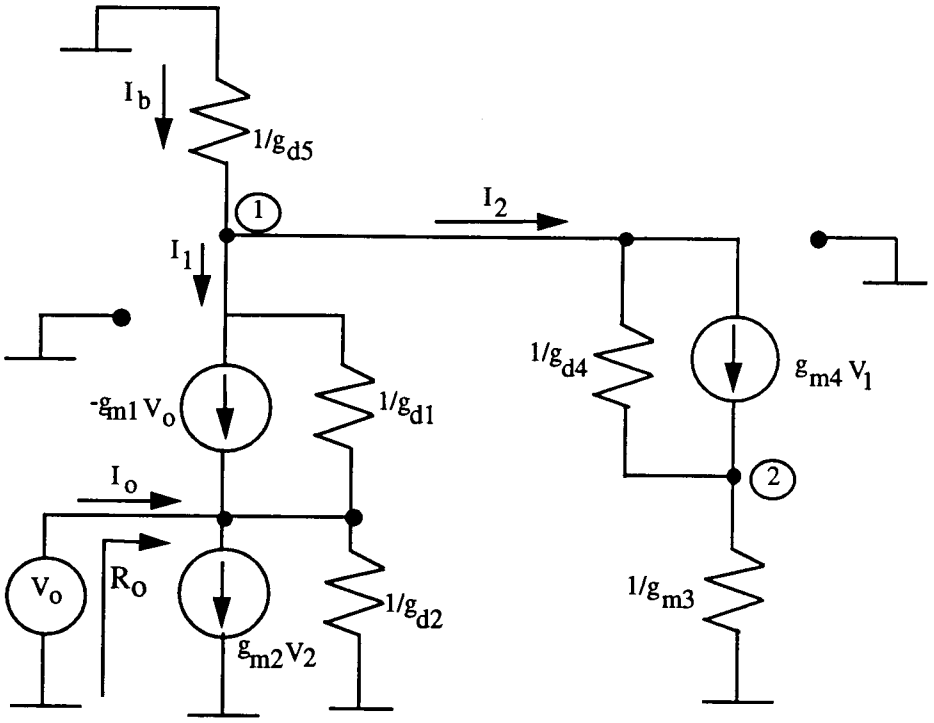


Fig 3.11. Small signal equivalent circuit to find the output resistance

Substituting for v_1 and v_2 in (35), we get

$$-v_o(g_{m1}+g_{d1}+g_{d2})+i_o=\frac{g_{m1}g_{m2}g_{m4}}{g_{m3}g'}v_o-\frac{g_{m1}g_{d1}}{g'}v_o\ ,$$

where $g' = g_{m4}+g_{d1}+g_{d4}+g_{d5}$. In above equation, the ratio g_{m2}/g_{m3} is approximately 2. Making this substitution, we find that $2g_{m4} >> g_{d1}$ and g_{d1} can be dropped. With this approximation, the above equation can be rearranged to get,

$$R_o=\frac{v_o}{i_o}=\frac{1}{g_{m1}+g_{d1}+g_{d2}+\dfrac{2g_{m1}g_{m4}}{g'}}.$$

Following conclusions can be drawn from the above equation. First, the output resistance will be less than that of an ordinary source follower buffer. The reduction in R_o is depen-

dent upon the values of g_{m4}, g_{d1}, g_{d2} and g_{d5}. If all the output conductances can be neglected, we get $R_o = \frac{1}{3g_{m1}}$. This value is 3 times lesser than that of an ordinary source follower. If the above assumptions are not satisfied, we will still have an additive term in g_{m1} which will reduce the output resistance. Using the values given previously, the value of R_o comes out to be 538 Ω.

Another important large signal parameter of the buffer circuit is its output swing. The negative going output swing is controlled by the saturation voltage of $M2$. Hence, we have $(V_{out})_{\min} = V_{dsatn}$. On the positive side, the output swing is controlled by the saturation voltages of $M1$ and the constant current source, $M5$. Hence, the maximum output swing is $(V_{out})_{\max} = V_{dsatn} + V_{dsatp}$.

3.3.3 AC analysis.

The small signal ac analysis can be performed on the circuit by including the load and the parasitic capacitances into the circuit. The high frequency small signal equivalent circuit for the buffer is accordingly shown in figure 3.12. In this figure, $C' = C_{gs2}+C_{gs3}$ as these two capacitances appear in parallel. Application of KCL at the output node yields,

$$(g_{m1}+sC_{gs1})(v_{in}-v_{out}) + g_{d1}(v_1-v_{out}) - g_{m2}v_2-(g_{d2}+sC_L)v_o = 0.$$

$$v_{in}(g_{m1}+sC_{gs1}) - v_{out}(g_{m1}+g_{d1}+g_{d2}+sC_L) = g_{m2}v_2 - g_{d1}v_1, \qquad (37)$$

where the condition $C_L >> C_{gs1}$ is made use of. Similarly, applying KCL at node 1,

$$v_1(g_{m4}+g_{d1}+g_{d4}+g_{d5}+sC_{gs4}) - g_{d4}v_2 = v_{out}(g_{m1}+g_{d1}) - v_{in}g_{m1}.$$

In the above equation, $g_{m1} >> g_{d1}$. And let $g' = g_{m4}+g_{d1}+g_{d4}+g_{d5}$. Also, since g_{d4} is very small , we can safely neglect $g_{d4}v_2$ in comparison with the first term. Then the above equation reduces to the following form,

$$v_1(g'+sC_{gs4}) = g_{m1}(v_{out} - v_{in}). \qquad (38)$$

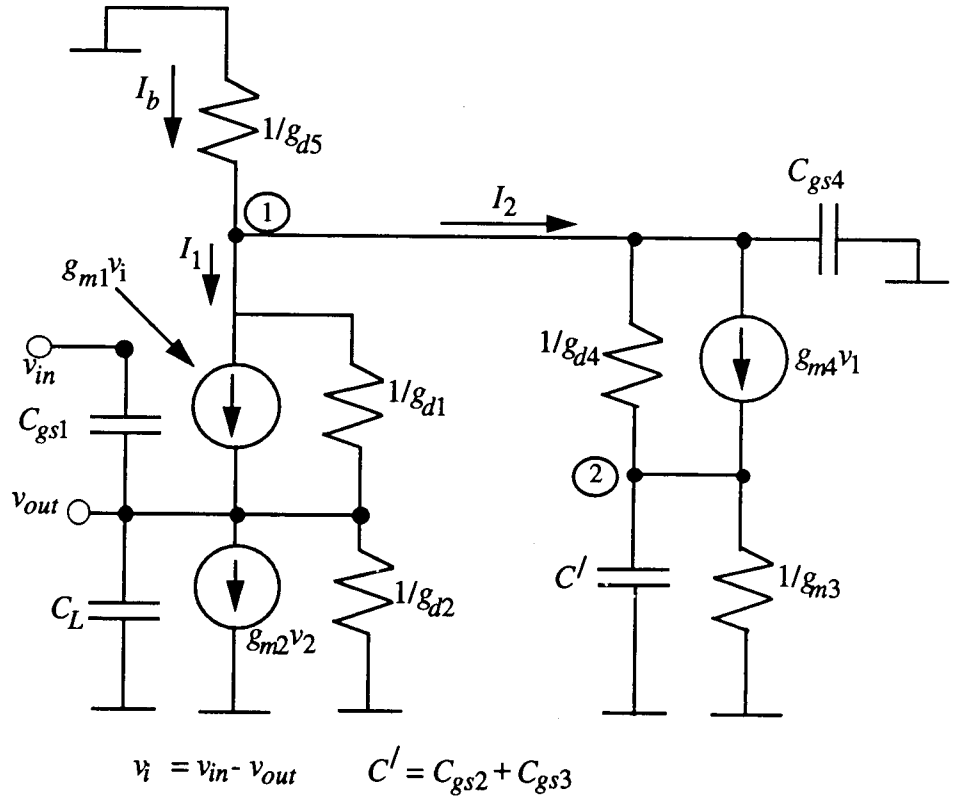


Fig 3.12. High-frequency, ac equivalent circuit of the buffer.

The s-domain relation between v2 and v1 is obtained by adding sC' at the denominator of equation (32) and neglecting g_{d4} as it is small. Accordingly, v_2 is given by,

$$v_2 = \frac{g_{m4}}{g_{m3} + sC'} v_1 \ .$$

Substituting for v1 from (38) we get,

$$v_2 = \frac{g_{m1} g_{m4}}{(g_{m3} + sC')\ (g' + sC_{gs4})} (v_{out} - v_{in}) . \qquad (39)$$

Substituting for v_1 and v_2 in equation (37), we get

$$(g_{m1} + sC_{gs1})\, v_{in} - (g'' + sC_L)\, v_{out} =$$

$$\frac{g_{m1}g_{m2}g_{m4}}{(g_{m3} + sC')\,(g' + sC_{gs4})}\,(v_{out} - v_{in}) - \frac{g_{m1}g_{d1}}{(g' + sC_{gs4})}\,(v_{out} - v_{in}) \qquad (40)$$

where $g'' = g_{m1} + g_{d1} + g_{d2}$. In order to solve for the zeros of the circuit, consider only the terms associated with the input voltage v_{in}. From (40), we get these terms to be,

$$(g_{m1} + sC_{gs1}) + \frac{g_{m1}g_{m2}g_{m4}}{(g_{m3} + sC')\,(g' + sC_{gs4})} - \frac{g_{m1}g_{d1}}{(g' + sC_{gs4})}.$$

Expanding the above equation and neglecting the denominator as it gets cancelled with that of the terms associated with v_{out}, we get a third order equation in "s" as shown below:

$$(g'g_{m1}g_{m3}+g_{m1}g_{m2}g_{m4}-g_{m1}g_{d1}g_{m3})+s(g_{m3}g'C_{gs1}+g_{m1}g_{m3}C_{gs4}+g'g_{m1}C'-g_{m1}g_{d1}C')+s^2(g_{m3}C_{gs1}C_{gs4}+g'C'C_{gs1}+g_{m1}C'C_{gs4})+s^3C'C_{gs1}C_{gs4}. \qquad (41)$$

The three roots of the above equation were found to be:

-1.4589e+10, (-0.6986e+10 + j0.9257e+10) and (-0.6986e+10 - j0.9257e+10). Notice that the zeros occur at very high frequencies. The capacitance values were found from Appendix A and a hand calculation gave the lowest frequency zero was found to be 1.1 GHz.

Instead of going through the rigorous algebraic manipulations of the terms associated with v_{out} in equation (40), we can substitute C_L in place C_{gs1} in equation (41) to obtain the same expression. The resulting third order equation is given below:

$$(g'g_{m1}g_{m3}+g_{m1}g_{m2}g_{m4}-g_{m1}g_{d1}g_{m3})+s(g_{m3}g'C_L+g_{m1}g_{m3}C_{gs4}+g_{m1}g'C'-g_{m1}g_{d1}C')+s^2(g_{m3}C_{gs1}C_{gs4}+g'C'C_L+g_{m1}C'C_{gs4})+s^3C'C_LC_{gs4}. \qquad (42)$$

As before, $g_{m3} = 0.5g_{m2}$ and $g' = g_{m4}+g_{d1}+g_{d4}+g_{d5}$. The three roots of the above equation were found to be at -1.4589e+10, -0.6350e+10 and -0.0352e+10. This puts the dominant pole frequency to be at 56 MHz. Thus, the bandwidth of the folded cascode buffer is almost three times larger than a simple source follower.

We can now conclude that both the current feedback buffer and the folded cascode buffer have achieved significant improvements over that of a simple source follower. The compromise done in the output swing to achieve a bigger bandwidth and slew rate is minimal. As these buffers are capable of driving large load capacitances, the buffers can also be used as output stages for high bandwidth op-amps.

Alternative buffer topologies also exist. These topologies predominantly use an operational amplifier in the unity gain configuration. The unity gain frequency of the op-amp will decide the 3-db bandwidth of such buffers. The advantage that the current feedback buffer and the folded cascode buffer have over that of the op-amp based buffers is simplicity. Moreover, as these circuits are intended to be used as test circuits, the smaller silicon area these circuits occupy, the better.

Chapter 4. Results

4.1 The testable op-amp system.

The test structure shown in fig 2.2 was implemented in silicon in a 2 micron p-well process. The two high speed buffer circuits along with another enhanced slew rate buffer circuit described in [3] were integrated in a testable operational amplifier. The testable op-amp is shown in figure 4.1. Digital logic is provided to switch any of the buffer circuits into the feedback loop of the op-amp for testing. The logic also provides access and control of the outputs and the inputs of the buffer circuits. The inputs and the output of the op-amp are brought out to pins and using the TMS signal, the op-amp can be isolated fully and characterized.

By keeping the switches C2 and C3 open, the respective outputs of the two buffers are gated to the IC pins. Since the inputs of these buffers are also available at IC pins, we get full access to each of the buffers. The reason for gating the outputs of the buffers is to avoid the capacitive loading of the buffer outputs as a result of the pad and the probe capacitances, when the buffer is in the op-amp's feedback path. The input/output pads are loaded by capacitances of approximately 4-5pF and this will reduce the bandwidth of the buffer. When the buffer is in the feedback path, this extra capacitive loading on the buffer output is avoided by using a transmission gate. However, the capacitive loading on the order of 4-5 pF at the inputs of the buffers will load the output of the op-amp whenever the buffers are switched into the op-amp's feedback path.

The operational amplifier used in the circuit was of a folded cascode type. A folded cascode amplifier was chosen as it does not need internal compensation. The resistors were implemented in polysilicon. For easier testing purposes, separate *Vss* lines were given to each of the buffer circuits and the op-amp.

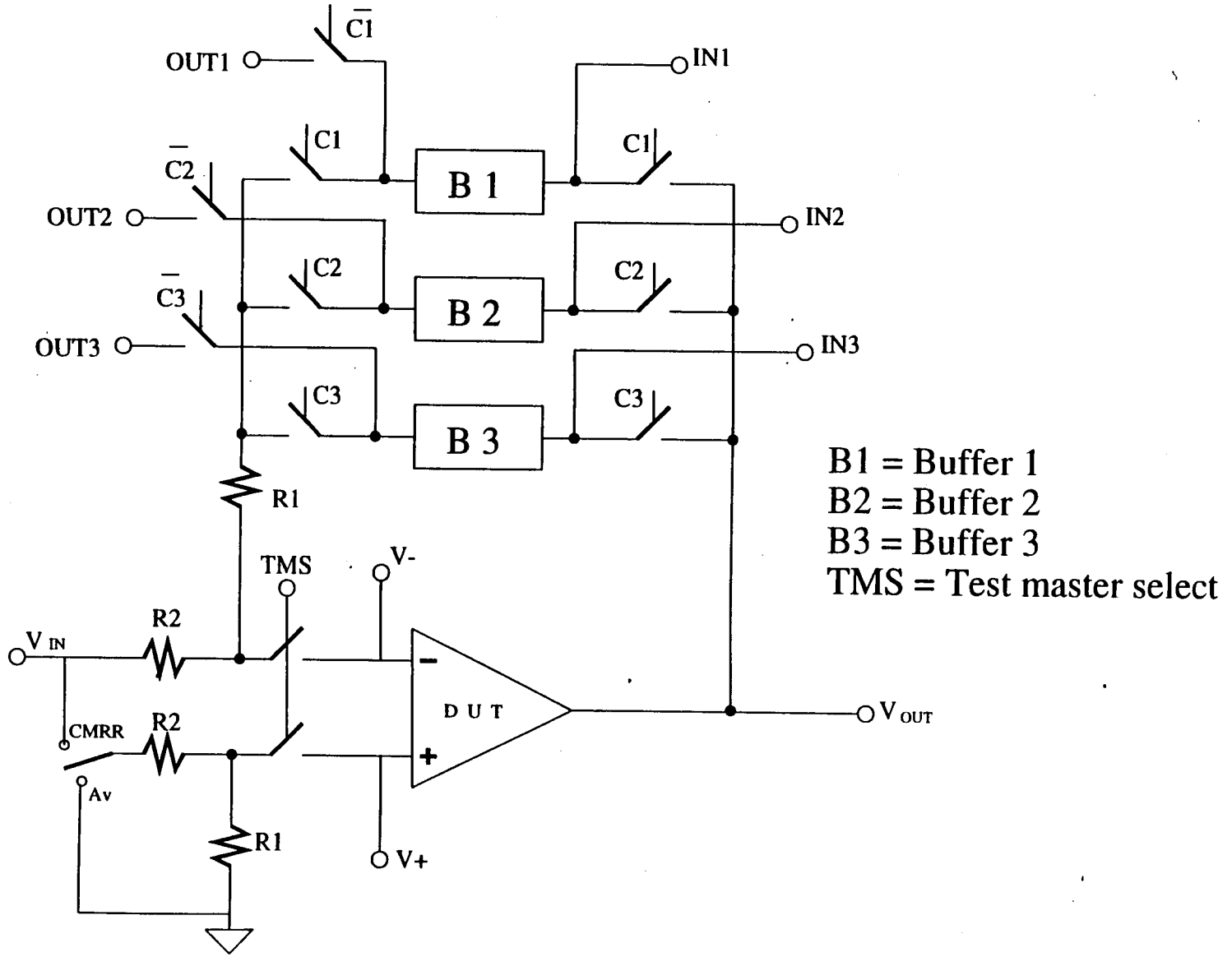


Fig 4.1. Testable Op-amp system architecture.

4.2 The current feedback buffer.

4.2.1 Simulation results.

The circuit was simulated using the Hspice circuit simulator. Figure 4.2 shows the schematic of the buffer circuit. Appendix A contains the spice deck along with the Mosis level-2 and the Bsim model parameters. The simulated DC parameters were:

1. DC gain 0.92

2. Output resistance,Ro 641 Ohms

3. Static power dissipation, Pd 2.14 mW

Figure 4.3 shows the dc transfer characteristic of the buffer. It should be noted that the buffer saturates at about 0.6 Volts on the positive swing. This swing is smaller than that of a simple source follower. The reason for the loss of headroom in the positive side is the diode connected PMOSFET, *M*3.

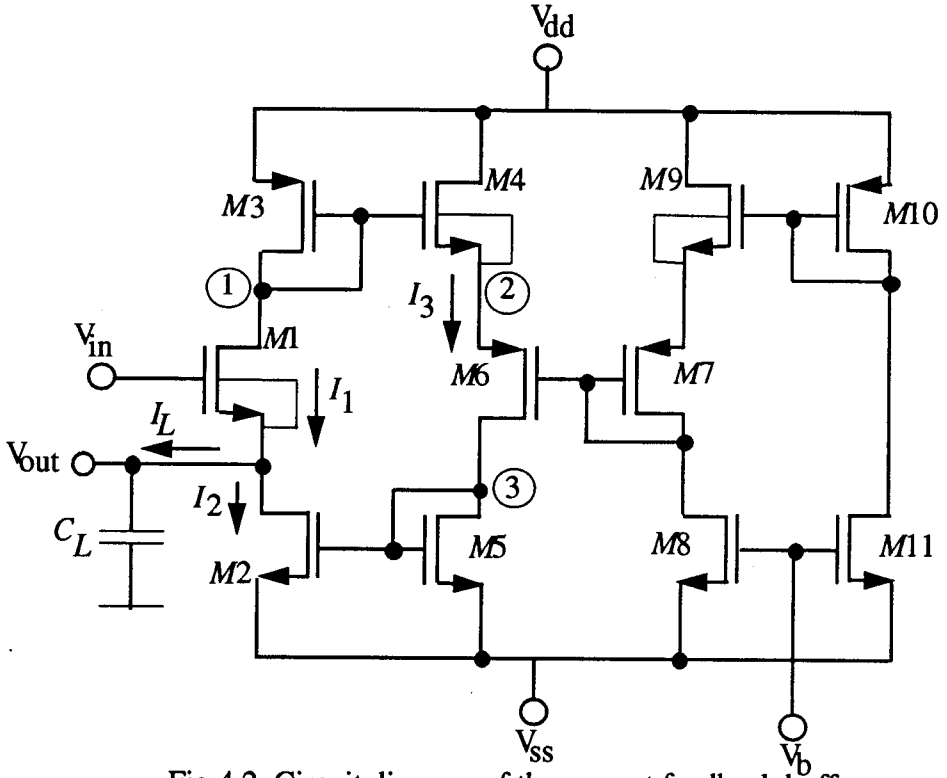


Fig 4.2. Circuit diagram of the current feedback buffer

Figure 4.4 shows the frquency response of the current feedback buffer. The 3-db frequency occurs at 63 MHz. This bandwidth is a 3x improvement over that of a simple source follower. This value is different from the predicted value of 85 MHz in chapter 3 but approximations were done for simplicity in arriving at the predicted value.

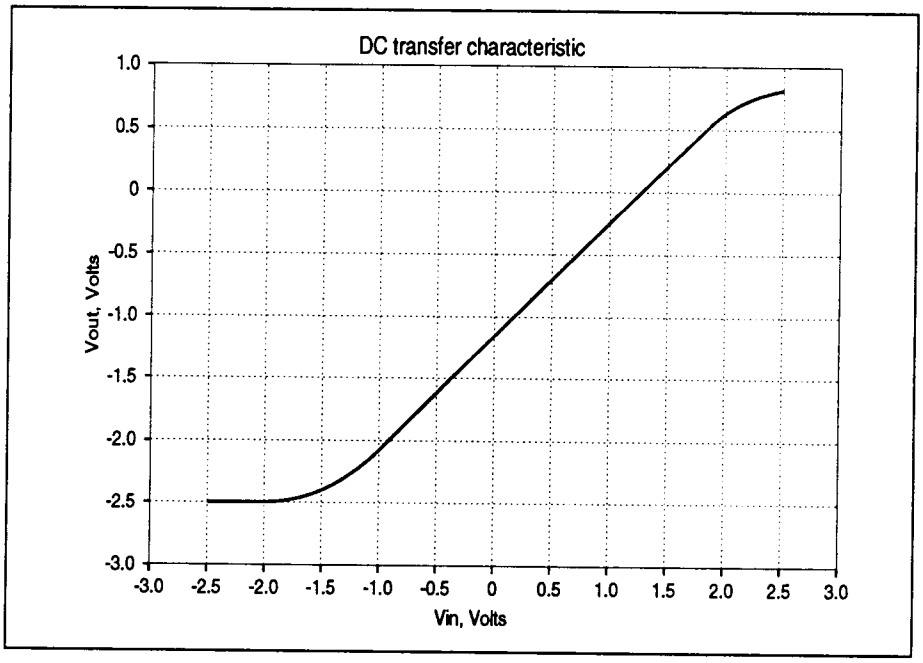


Fig 4.3 DC transfer characteristics of the buffer.

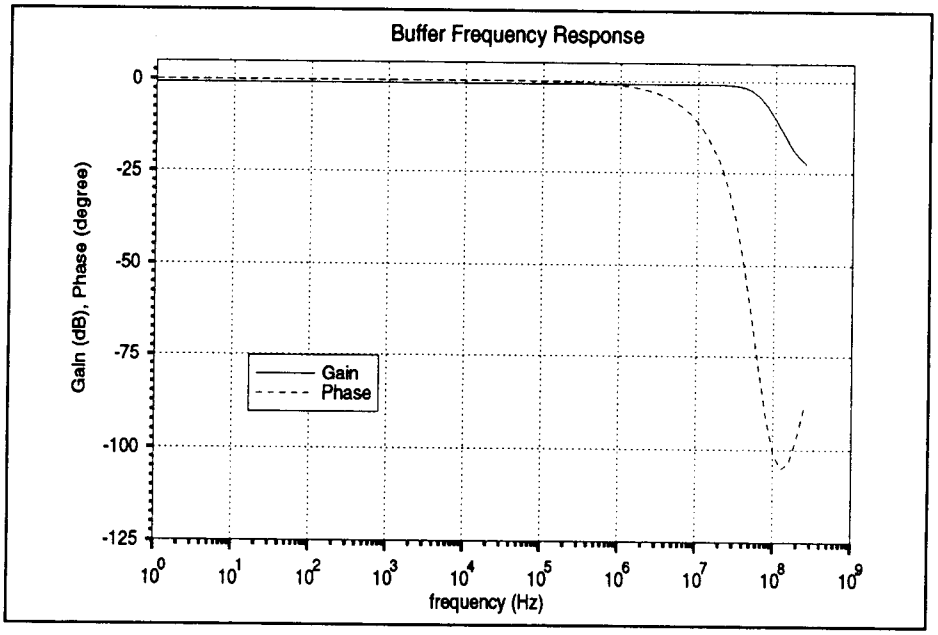


Fig 4.4. Simulated frequency response of the buffer

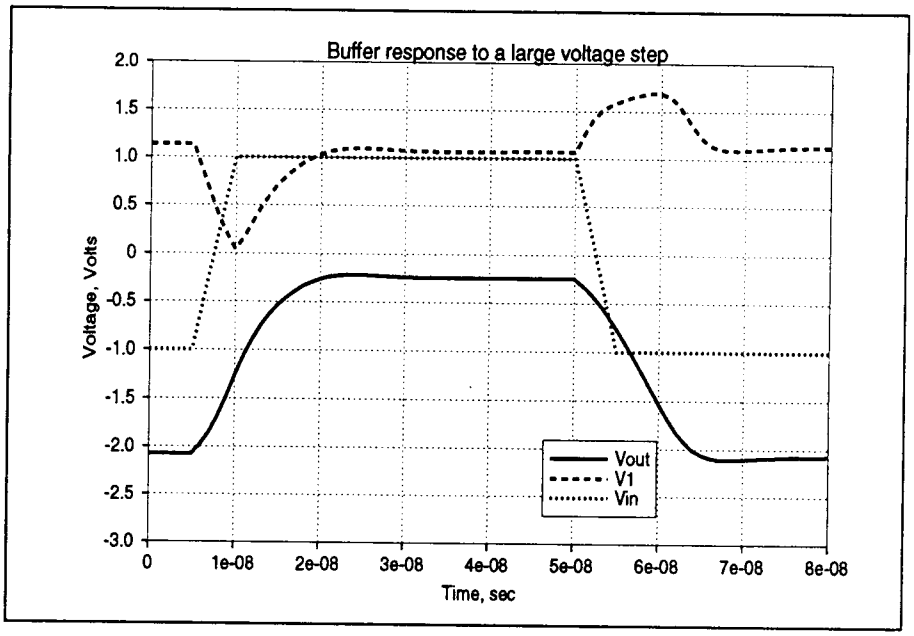


Fig. 4.5. Large signal transient response of the buffer

One of the important criterion is the realization of the buffer is its ability to respond to large signal step inputs. In figure 4.5, the input step is a 2 V peak to peak square wave with rise and fall times of 5ns. The buffer exhibits a DC level shift of about 1.1 Volts. The voltage at node 1 is also shown in the figure. As expected, the voltage at 1 reduces steeply during the time when the output rises and the transistor $M1$ conducts heavily. During the negative edge, v_1 rises toward *Vdd* thereby increasing the gate-to-source voltage of $M4$. The rise and fall times, measured for the output to settle to within 1% of its final values, are 18 ns and 17 ns respectively. These times can be improved by increasing the bias voltage V_b at the expense of output swing. We also notice that the buffer exhibits a small amount of ringing before reaching a steady state. The overshoot is extremely small and indicates the existence of complex conjugate poles. The existence of complex conjugate poles was predicted by the AC analysis done in the previous chapter.

Figure 4.6 shows the various transient current waveforms. The effect of the current mirror gain between $M2$ and $M5$ can be clearly observed in the figure. When the input voltage is rising fast, the transistor $M1$ will have a dynamic increase in v_{gs} and this results

in its conducting a large amount of current as signified by the current spike in $i(M1)$ in fig 4.6. During the falling edge of the input voltage, $M1$ has shut off and $i(M1)$ has reduced almost zero. But there is an increase in $i(M4)$ due to a dynamic increase in its v_{gs} and this increase has been amplified by the current mirror gain as shown by $i(M2)$. This large current has helped discharge the output node very fast.

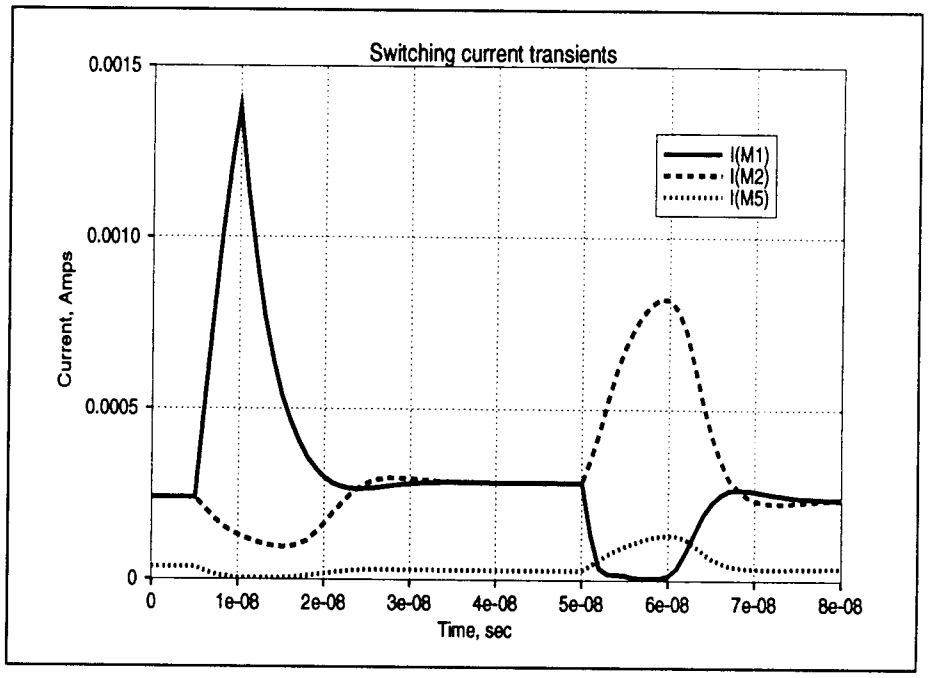


Fig 4.6. Transient current waveforms for a large step input

In figure 2.2 in chapter 2, the output of the buffer is connected to a 50 kOhms resistor. Large resistors values fabricated in MOS processes occupy a large area [1]. In a typical Mosis process, the 50 kOhm polysilicon resistor occupied an area of 2.5×10^5 sq microns. If this resistor is replaced by a switched capacitor clocked at 1 MHz and a double poly process is used to realize the capacitor, it was found that the area occupied by the capacitor was 40,000 sq microns. Hence, these resistors can be replaced with their switched capacitor equivalents, as highly accurate capacitors can be realized in double-poly MOS processes. The buffer was designed and simulated for capacitive loads as indicated in the schematics. However, the buffer's performance was also evaluated for resistive loads. The reduction in the dc gain because of a resistive load was not significant as the

value of the resistance was big. The dc gain, however, reduced from 0.92 to 0.915. Figure 4.7 shows the frequency response of the buffer for a resistive load. The bandwidth of the buffer increased as the capacitance at the output node now was small. .

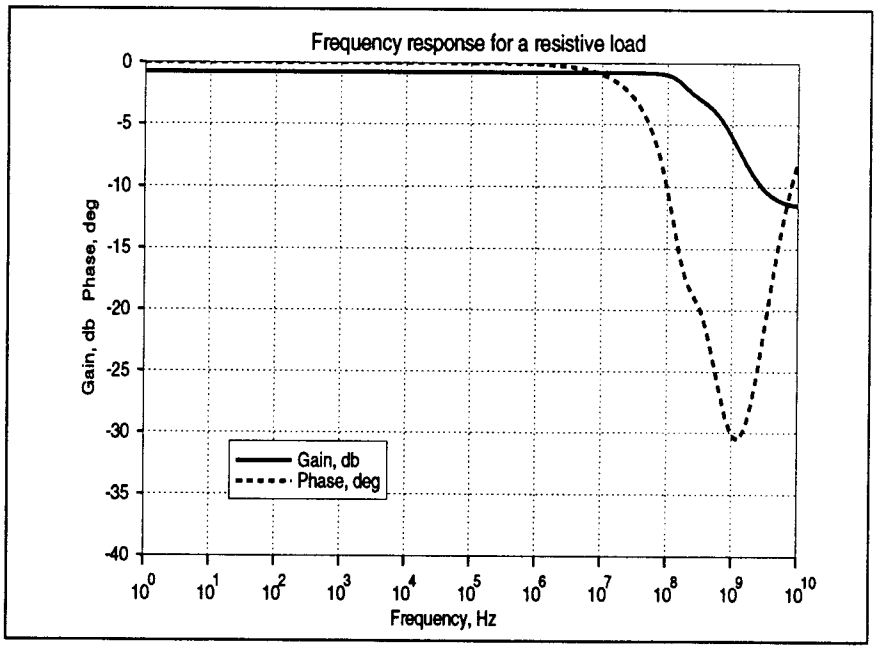


Fig 4.7. Frequency response of the buffer for a resistive load

The total harmonic distortion of the buffer circuit was simulated for input frequencies ranging from 100 kHz to 60 MHz. Table 1 shows the simulated THD values. All of these values were measured for a sinusoidal input of 2 Volts peak-to-peak value. The harmonic distortion increased significantly for input frequencies above 10 MHz. A spectrum analysis showed significant presence of the second harmonic for input frequencies greater than 10 MHz indicating that the buffer was experiencing slew rate limiting.

Table 1: Simulated harmonic distorion for the current feedback buffer

Frequency, Hz	THD, %
100 k	0.2
1 M	0.2
10 M	0.2
60 M	5

4.2.2 Experimental results.

The current feedback buffer in the test chip was tested and its performance was evaluated. The buffer exhibited excellent performance and conformed to the simulated values well. Figure 4.8 shows an oscilloscope picture of the DC transfer characteristic of the buffer. The linear swing of the buffer is about 2.3 volts.

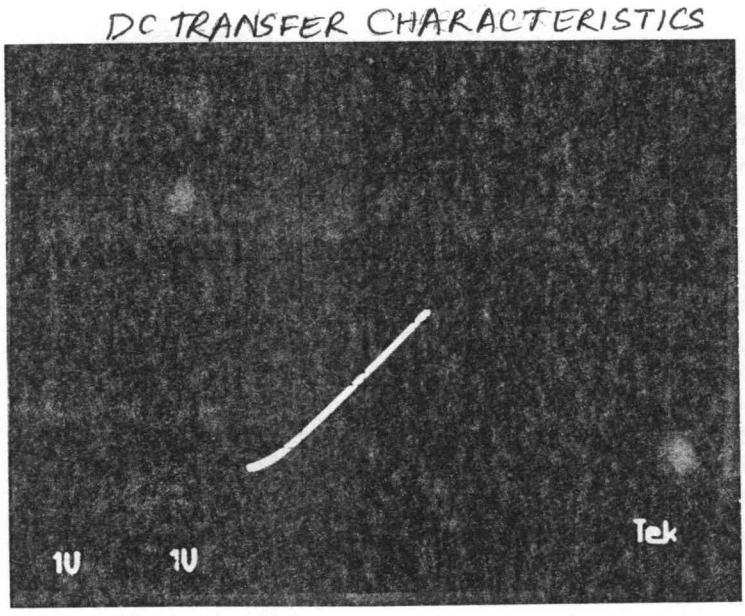


Fig 4.8. Measured DC transfer characteristic

Figure 4.9 shows the response of the buffer for a large input step. A 2 V peak-to-peak square wave of 2 MHz frequency was applied to the buffer. The output of the buffer settled to within 1% of the final value in 50 ns on the rising edge and 70 ns on the falling edge. These values show significant speed in the large signal behaviour of the buffer because the capacitive load on the output of the buffer is on the order of 20 pF owing to the pad and the probe capacitances. It should be noted that the DC level shift of the buffer is about -1.3 Volts. This value conformed to the simulation values.

Figure 4.10 shows the measured spectrum of the output signal. Notice that the second harmonic is very low compared to the first indicating that the buffer is not experiencing any slewing. The third harmonic appears to be significant, the reason being the poor

quality of the input signal itself. A spectrum of the input signal showed significant presence of the third harmonic in the input.

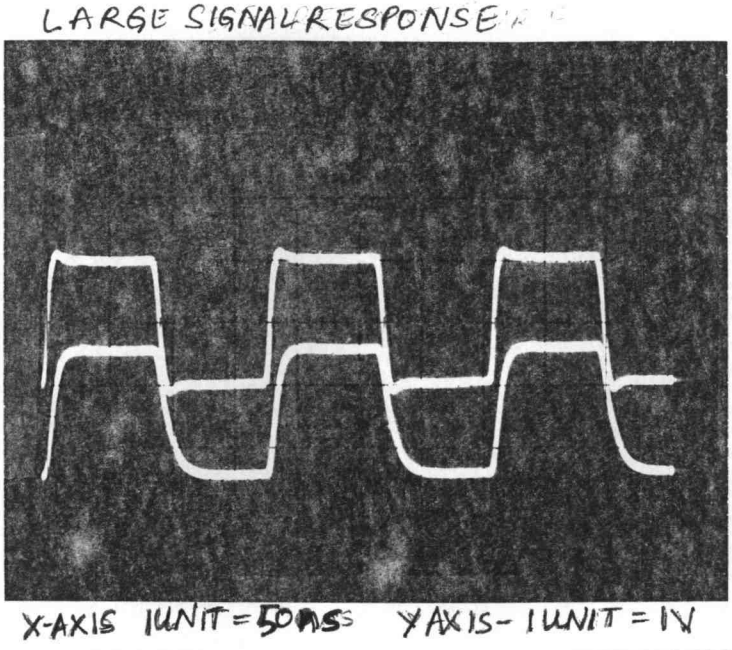


Fig 4.9. Measured large signal response of the buffer

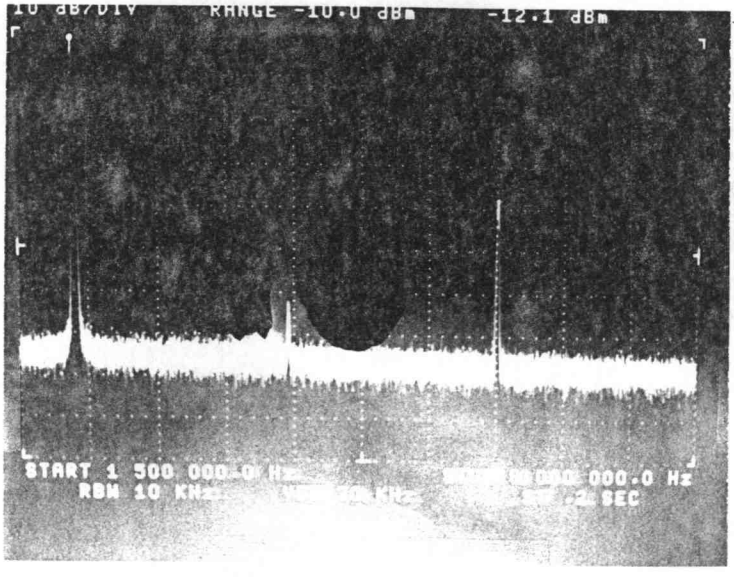


Fig 4.10. Measured output spectrum of the buffer

Figure 4.11 shows the response of the current feedback buffer to a large input sinusoidal. The input had a peak-to-peak value of 2 Volts. The measured phase shift between the input and the output at 2 MHz was only -9 degrees. Also notice that the gain of the buffer is still close to one. The measured low frequency gain of the buffer was 0.94 which is slightly higher than the simulated value.

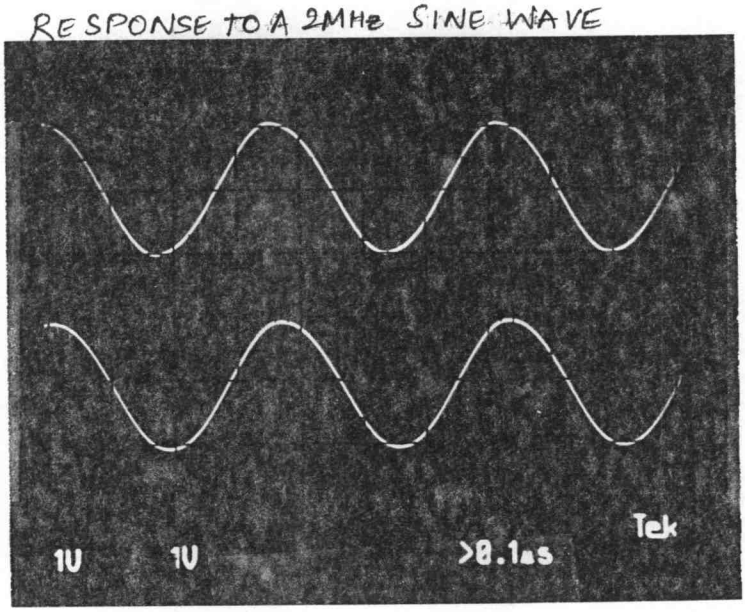


Fig 4.11. Measured response of the buffer to a sine wave

The 3-dB bandwidth of the buffer could not be measured because the maximum frequency of the signal generator was only 2 MHz. The simulated 3-dB bandwidth of the buffer for a load of 20 pF was about 16 MHz.

4.3 The folded cascode buffer.

4.3.1 Simulation results.

The simulation of the circuit was done using Hspice. The spice deck along with the level-2 and the Bsim models are included in Appendix A. The following data was obtained from the operating point analysis.

1. DC gain. (Vout/Vin) 0.93

2. Output resistance, Ro 548 Ohms

3. Static power dissipation, Pd 2.5 mW

Figure 4.12 reproduces the circuit schematic of the folded cascode buffer. The DC transfer characteristic of the circuit is shown in figure 4.13. We notice that in the simulation, the output saturates at an earlier value than predicted.

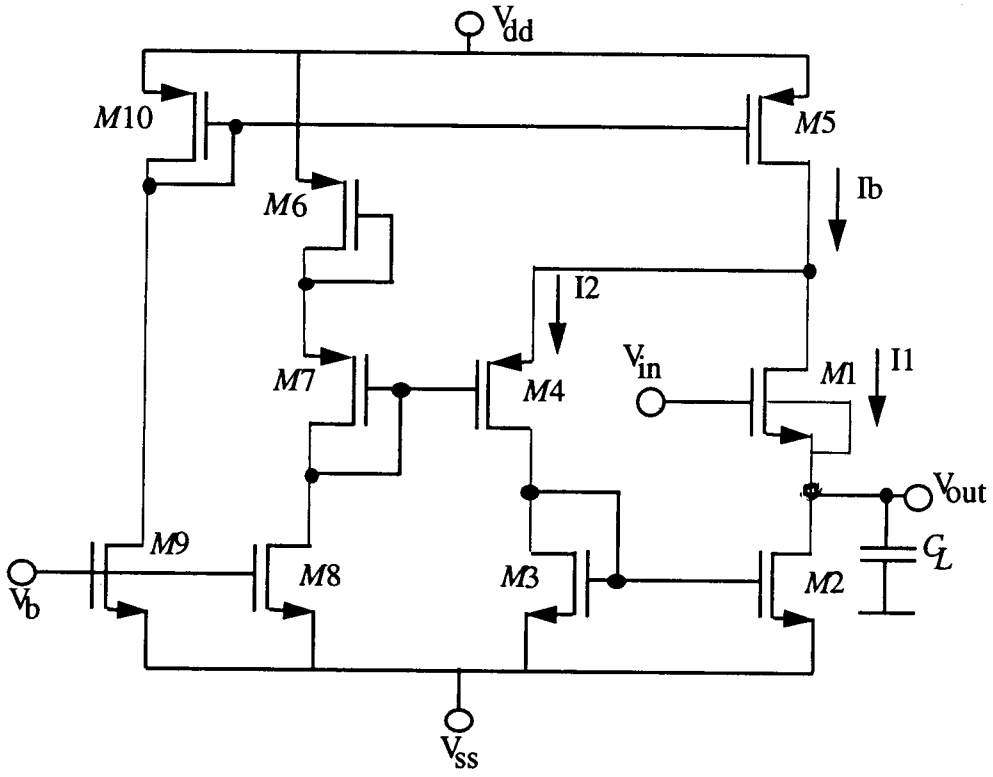


Fig 4.12. Circuit diagram of the folded cascode buffer

Figure 4.14 shows the frequency response of the buffer. The 3-dB frequency occurs at 54 MHz and this value conforms well with the predicted value of 55.7 MHz. A pole-zero analysis performed on the circuit using Hspice confirmed these two values.

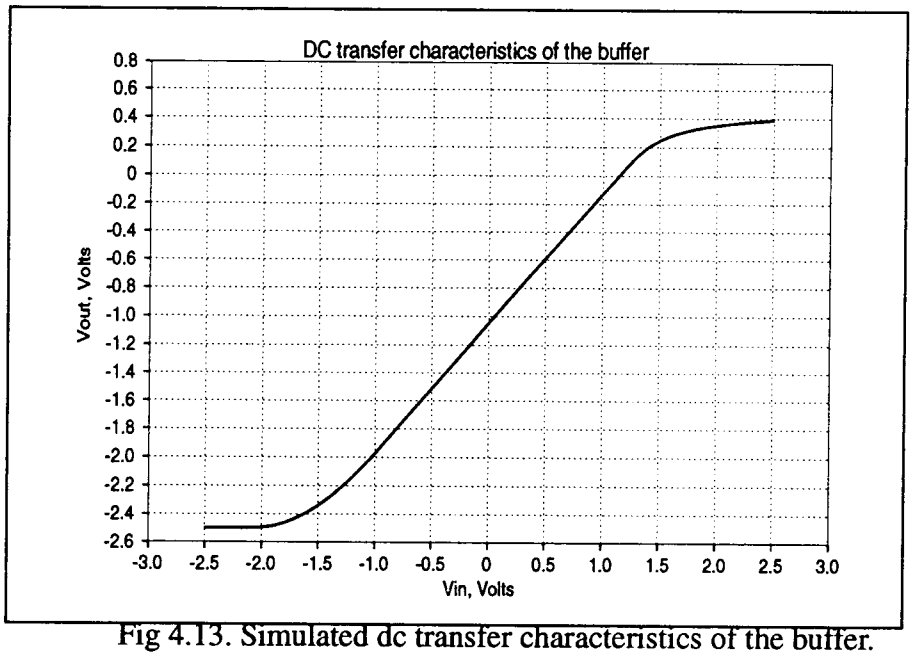


Fig 4.13. Simulated dc transfer characteristics of the buffer.

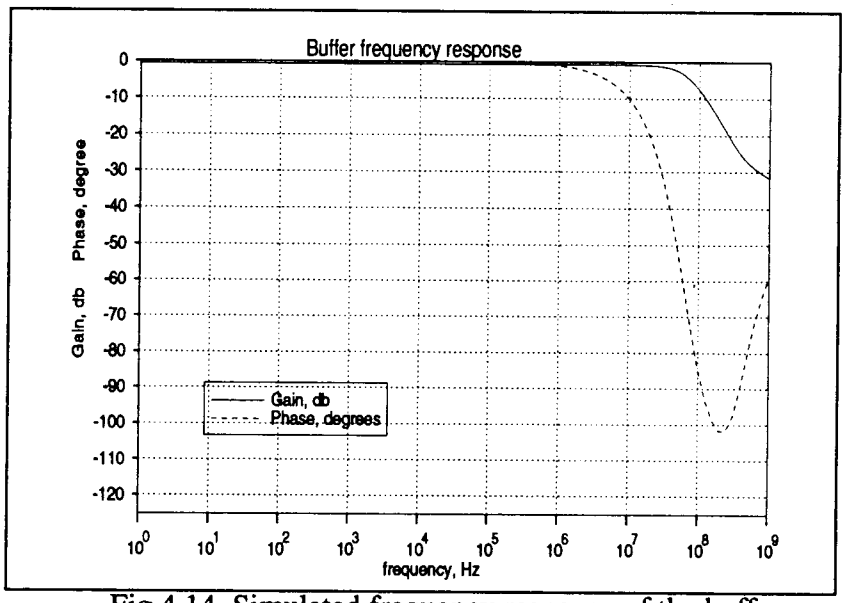


Fig 4.14. Simulated frequency response of the buffer.

Figure 4.15 shows the large signal transient response of the circuit. A pulse input with a peak-to-peak value of 2 V with rise and fall times of 5ns was applied to the circuit. We notice that the output settles to within 1% of the final value in about 23 ns on the rising edge and in about 19 ns on the falling edge.

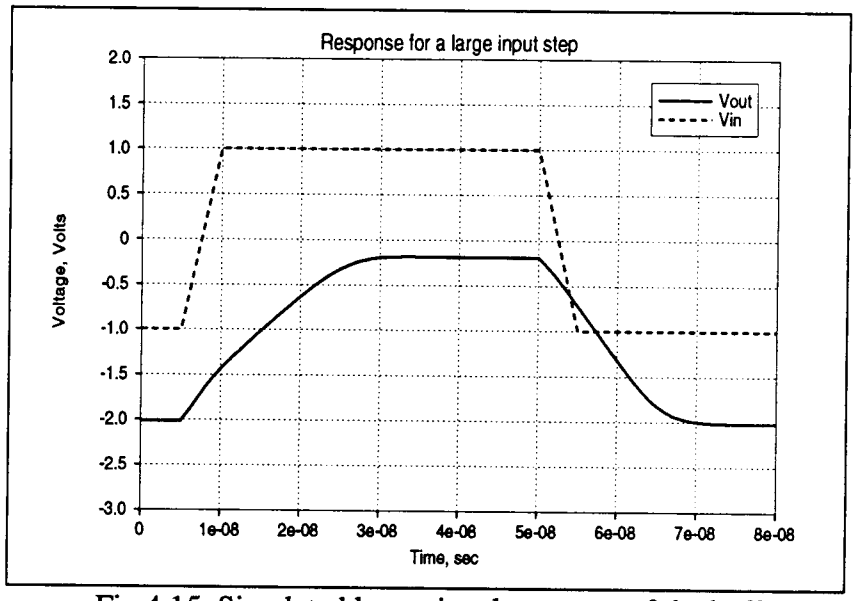


Fig 4.15. Simulated large signal response of the buffer

We notice that the output voltage suffers noticeable slew rate limiting during its rise time and to a lesser extent during its fall time. The slew rate of the buffer is limited by the constant current source *M*5. The point worth noting is that the circuit achieves reduction in rise and fall times by redistributing a constant current.

Figure 4.16 shows the transient current waveforms in the two branches of the circuit. Notice the effect of the current gain between *M*2 and *M*3. When the input falls rapidly, the current through *M*1 decreases while the current through *M*3 increases. And the current mirror gain has resulted in an amplified discharging current through *M*2. Notice that after the initial spike, *i*(*M*1) reduces slowly causing the output to slew unlike the current spike witnessed in the current feedback buffer. The circuit, though achieves significant improvement in rise and fall times over that of a simple source follower running at the same bias currents.

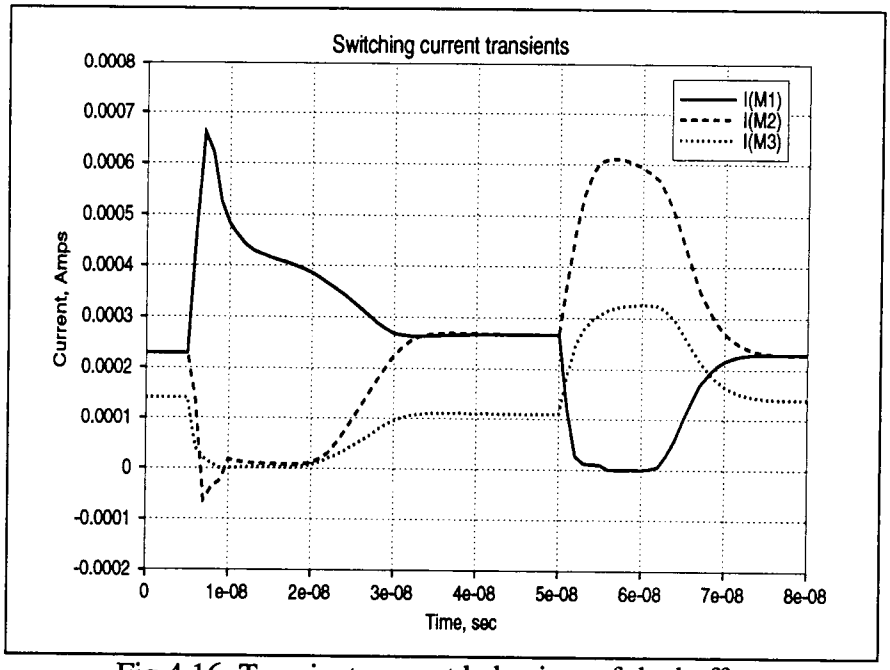


Fig 4.16. Transient current behaviors of the buffer.

Table 2: Simulated harmonic distortion for the folded cascode buffer

Frequency, Hz	THD, %
100 k	0.2
1 M	0.2
10 M	0.4
60 M	9

The harmonic distortion of the buffer was simulated at different frequencies for a 2V peak-to-peak sine wave. Table 2 shows the distortion values obtained for various frequencies.This circuit's distortion at very high frequencies was poor. The circuit exhibited considerable slewing during rise time as can be noticed from fig. 4.11. And this caused excessive distortion to occur at 60 MHz. A spectrum analysis was performed on the output of the buffer for input frequencies in excess of 10 MHz. The second harmonic was of considerable value indicating that the output was slewing.

4.3.2 Experimental Results.

The performance of the folded cascode buffer in the test chip was also measured. The measured DC gain was 0.92 which conformed well with the simulated value. Figure 4.17 shows the measured DC transfer characteristic of the folded cascode buffer. Notice that the linear output swing of the buffer is about 2 volts. The dc shift of the buffer was about -1.0 volt.

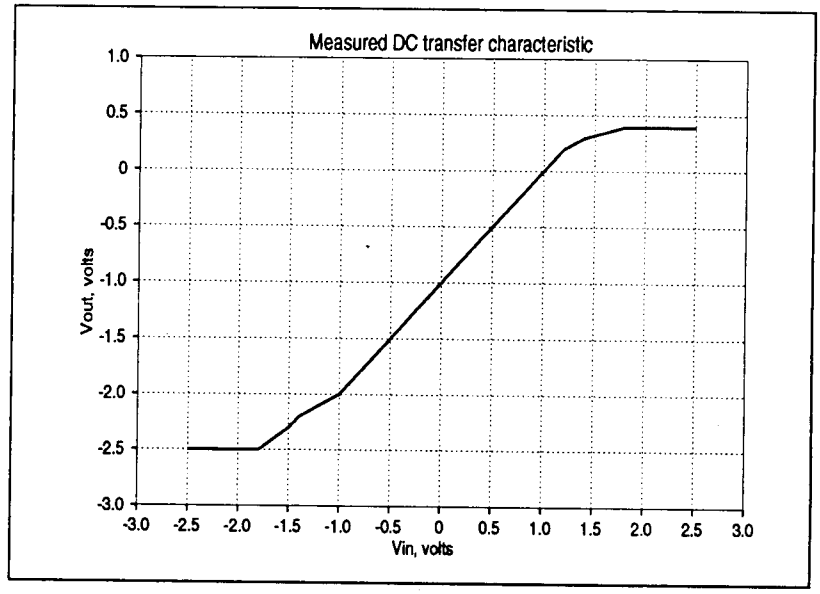


Fig 4.17. Measured dc transfer characteristic of the buffer

Figure 4.18 shows the large signal response of the buffer. The input applied is a square wave (the waveform at the top in the figure) of 2 V peak-to-peak value. The output of the buffer settled to within 1% of its final value in about 80 ns on the rising edge and 40 ns on the falling edge. The smaller fall time is due to the current mirror gain between transistors *M*2 and *M*3.

Figure 4.19 shows the spectrum analysis of the output. The input applied was a 2 volts peak-to-peak sine wave. Notice that the buffer is experiencing second order distortion, indicating that it is slew rate limited. The slew rate limitation of the buffer can be alleviated by replacing the constant current source *M*5 in figure 4.12 by a diode connected transistor.

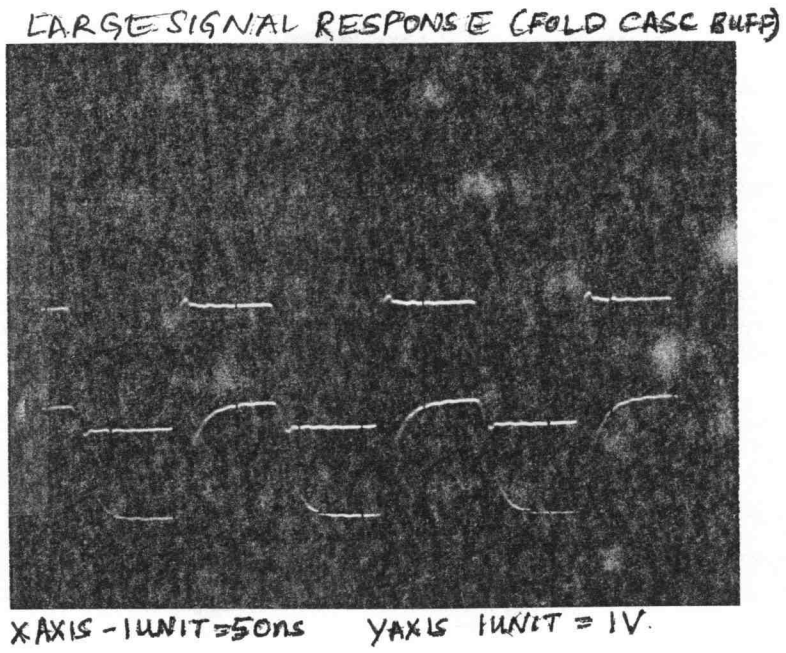


Fig 4.18. Measured large signal response of the buffer

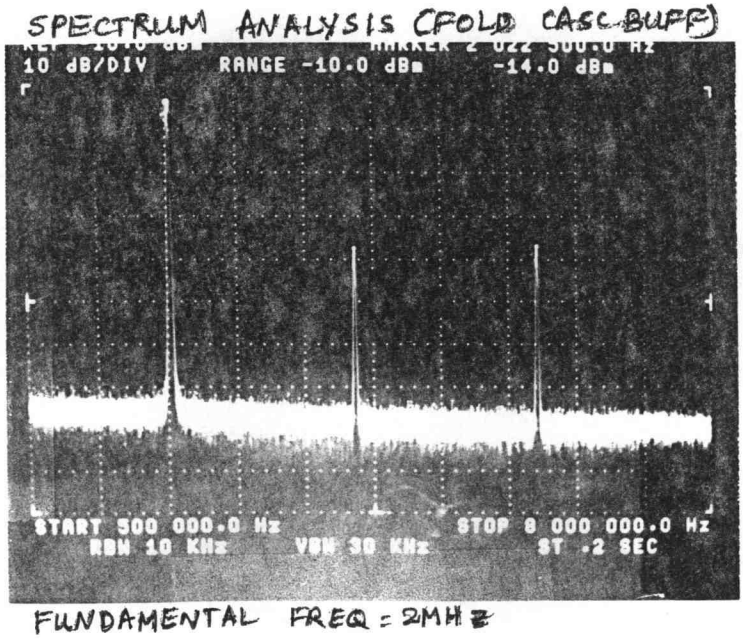


Fig 4.19. Measured output spectrum of the buffer

Note that the gain of the buffer is close to its dc value even at frequencies as high as 2 MHz. The signal generator could source only up to 2 MHz and hence the 3-dB bandwidth of the buffer could not be measured. However, a simulation run with a load of 20 pF showed that the buffer had a bandwidth of 13 MHz.

In order to evaluate the effect of the buffer in the test circuits, the op-amp's frequency response was simulated without the buffer. Since, the op-amp under test was a folded cascode op-amp without an output stage, the measured low-frequency gain was 52 dB while the actual gain of the op-amp was 56 dB. This discrepency was removed by the inclusion of the buffer. A simulation of the test circuit with the buffer gave the low-frequency gain to be 55.7 dB which is close to the actual value.

Chapter 5. Conclusions

5.1 Summary

This thesis described two enhanced slew rate buffers to be integrated with an op-amp. These circuits facilitate accurate measurement of an op-amp's frequency response.

Chapter 2 examined a frequency response measurement technique and its drawbacks. At frequencies approaching the unity gain frequency of the op-amp, the relative magnitudes of its output impedance and its gain response are such that a forward signal path exists through the feedback resistor. This path introduces a zero into the closed loop frequency response of the op-amp thereby altering its gain. The solution to this problem is to include a unity gain buffer in the feedback path of the test circuit. The chapter also listed the specifications of the buffer.

In chapter 3, two high speed buffers were described. The most basic unity gain buffer in CMOS technology, the source follower, was explained. The limitations of the source follower in terms of speed and output swing trade-offs were delineated. Of the two buffers, the first one used a current feedback mechanism to achieve increase in speed while the second circuit used folded cascode techniques along with current mirror gains to achieve the increase in speed. DC and AC analyses were performed to predict the gain, the output resistance, the output swing and the bandwidth of the circuit.

The fourth chapter presented the simulation and the experimental results obtained. The simulations were done using the circuits extracted from the layout that was sent to Mosis for fabrication.

The current feedback buffer showed excellent conformity between the simulated and the measured values. It exhibited very good settling behavior. At parasitic capacitive loads as high as 20 pF, the output of the buffer was able to settle to within 1 % of its final

value in 50 ns on both rising and falling edges. This indicated an extremely fast settling of the buffer at lower loads. At frequencies as high as 2 MHz, the buffer experienced negligible slew rate limiting. This was noticed by analyzing the spectrum of the output of the buffer. The second harmonic was almost 60 dB below that of the first harmonic giving low distortion levels. The measured output swing of the buffer was 2.3 volts which was slightly smaller than the simulated value.

The folded cascode buffer matched the performance of the current feedback buffer. It had good linearity and output swing. Simulations on the buffer showed a 3-dB bandwidth of about 54 MHz. The buffer had an output resistance of about 550 Ohms which again satisfied the requirements. The measured results on the folded cascode buffer agreed well with the simulated values. The measured dc gain was 0.92. The folded cascode buffer experienced some amount of slew rate limiting as shown by the spectrum analysis of the output of the buffer.

The fourth chapter also discussed the testable op-amp integrated circuit that has been fabricated. Digital control scheme was used to provide controllability and accessibility for each of the buffer circuits as well as the op-amp under test. This allows each of the circuits to be characterized separately. Using control signals, any one of the buffers can be integrated with the op-amp and its gain response can be measured.

5.2 Future Work.

Resistors in the MOS technology are usually realized using polysilicon or diffusion layers. The area of the resistor is calculated depending upon the sheet resistance values of these layers. These values vary from process to process. Hence, it is difficult to achieve high accuracy while fabricating MOS resistors. Secondly, for large resistances, the area of the resistor will be large. The problems posed by the resistors can be alleviated by replacing the resistors with switched capacitors. Accurate capacitor ratios can be realized in MOS technology. A resistor R may be replaced by an equivalent switched capacitor ($T/$

C) where T is the clock period. Some of the practical issues involved are the stray capacitance effects, clock feedthrough, charge injection and the op-amp characteristics. Different circuit techniques have been devised to take care of stray capacitance effects. Clock feedthrough and charge injection occur due to the parasitic capacitances and the channel charges in the transistors which are switched on and off periodically. The op-amp characteristics decide the clock frequency. The clock frequency depends upon the settling time and the bandwidth of the op-amp. The buffer circuits have been designed and simulated with capacitive loads as high as 5 pF. They have shown very good performance making them useful for switched capacitors also.

In an analog system containing several op-amps, the same test circuit may be used to characterize the gain response of all the op-amps. The test circuit may be switched from one op-amp to the other using digital control and transmission gates. This involves very minimal circuit overhead but allows us to use the same test circuitry to test many modules. Two simple, accurate tests to measure the gain bandwidth and the slew rate of the op-amp are described in [5]. These tests do not require any test inputs and are particularly suited for testing analog circuits using digital testers. Using these tests and the frequency response measurement incorporating the buffers, the op-amp can be completely characterized.

In equation (9) in chapter 3, we derived a relationship between i_2 and i_L for the current feedback buffer. The equation is reproduced here again:

$$i_2 = i_L \frac{7 g_{m4} g_{m6}}{7 g_{m4} g_{m6} + g_{m3} (g_{m4} + g_{m6})} .$$

Suppose that we need to make the gain from i_L to i_2 to be 1. We can achieve this either by increasing the current gain between transistors $M2$ and $M5$ (ref fig. 3.4) or by decreasing the value of g_{m3}. In the circuit of the current feedback buffer, we can see that the nodes 1 and 3 are low impedance nodes. By making node 1 a high impedance node, we can reduce

g_{m3} or by making node 3 a high impedance node, the current mirror gain can be increased. Node 3 may be made a high impedance node by replacing $M5$ with a current source. Then if the current through $M1$ is held constant (ref fig. 3.5), we see that $i_2 = i_L + C$, where C is a constant. Since, the current i_L is injected at a very low impedance node, transistor $M1$ can be biased such that current i_1 remains constant. Under these conditons, the circuit can be said to perform the function of a current conveyor. The input current may be injected either from a voltage source with a source resistance or a current source. Initial simulations showed that the circuit exhibited good linearity. The voltage at the source of $M1$ varied by only 0.1 V and as a result i_1 was constant. Further work can be done to realize a high linearity current conveyor. A current conveyor is a versatile and useful building block in current mode circuits [8], [9].

Bibliography

1. R. Gregorian and G. Temes, *Analog MOS Integrated Circuits for Signal Processing*, John Wiley and Sons, 1986.

2. W.M.C. Sansen, M. Steyaert and P.J. Vandeloo, "Measurement of Operational Amplifier Characteristics in the Frequency Domain", *IEEE Transactions on Instrumentation and Measurement,* vol. IM-34, pp 59-64, March 1985.

3. G. Rangan, J. Kenney, K. Ramamurthy and G. Temes, "High speed buffers for Op-amp characterization", *IEEE International Symposium on Circuits and Systems,* May 1993.

4. P.K. Wu, "Unit-Gain buffer Switched-Capacitor Filters - Design Techniques and Circuit Analysis", PhD Thesis, UCLA 1986.

5. K. Ramamurthy, J. Kenney and G. Rangan, "On-chip tests for gain bandwidth and slew rate", *IEEE International Symposium on Circuits and Systems,* May 1993.

6. M. A. Breuer, "Design for testability and Built-in-self-test", *IEEE VLSI Design conference,* New Delhi, India, 1991.

7. Proceedings, *the fifth IEEE P1149.4 Mixed-Signal Test Bus Standards working group meeting,* January 1993.

8. A.S.Sedra, "The current conveyor: History and Progress", *IEEE International Symposium on Circuits and Systems,* 1989.

9. C. Toumazou, F.J. Lidgey and D.G. Haigh, *Analogue IC design: the current-mode approach,* Peter Peregrinus Ltd., 1990.

Appendix A. Hspice listings.

```
**********************************************************************
                    CURRENT FEEDBACK BUFFER

 The Hspice operating point output file. Contains the input spice
deck, operating point node voltages, nodal capacitances, static
power dissipation, operating point information for each of the
transistors and small-signal transfer characteristics.
**********************************************************************
******  input listing
 .subckt posbuff in_buff out_buff bias vdd vss
 * ( input output bias vdd vss )
 * devices:

 m1 1 in_buff out_buff out_buff mosis1_n l=2u w=40u ad=200p
+as=200p pd=90u ps=90u
 m2 out_buff 5 vss vss mosis1_n l=2u w=40u ad=200p as=200p pd=90u
 +ps=90u
 m3 1 1 vdd vdd mosis1_p l=2u w=72u ad=360p as=360p pd=154u
+ps=154u
 m4 vdd 1 6 6 mosis1_n l=2u w=44u ad=220p as=220p pd=98u ps=98u
 m5 5 5 vss vss mosis1_n l=2u w=6u ad=30p as=30p pd=22u ps=22u
 m6 6 7 5 vdd mosis1_p l=2u w=44u ad=220p as=220p pd=98u ps=98u
 m7 7 7 8 vdd mosis1_p l=2u w=44u ad=220p as=220p pd=98u ps=98u
 m8 7 bias vss vss mosis1_n l=4u w=24u ad=120p as=120p pd=58u
+ps=58u
 m9 vdd 9 8 8 mosis1_n l=2u w=44u ad=220p as=220p pd=98u ps=98u
 m10 9 9 vdd vdd mosis1_p l=2u w=72u ad=360p as=360p pd=154u
+ps=154u
 m11 9 bias vss vss mosis1_n l=2u w=40u ad=200p as=200p pd=90u
+ps=90u

 * lumped capacitances:
 c1 1 0 89.1f
 c2 vdd 0 199f
 c3 vdd 1 1.2f
 c4 out_buff 0 46.2f
 c5 out_buff 1 2.03f
 c6 vss 0 89.2f
 c7 vss 1 7.21f
 c8 vss out_buff 0.958f
 c9 5 0 35f
 c10 5 1 0.272f
 c11 5 vdd 0.355f
 c12 5 out_buff 1.73f
 c13 5 vss 0.125f
 c14 6 0 55.1f
 c15 6 1 0.0125f
 c16 6 vdd 1.87f
 c17 6 5 2.33f
 c18 7 0 47.5f
 c19 7 1 0.544f
 c20 7 vdd 0.947f
 c21 7 vss 0.29f
 c22 7 5 0.438f
 c23 7 6 3.81f
 c24 8 0 50.4f
```

```
c25 8 vdd 1.92f
c26 8 6 0.85f
c27 8 7 1.51f
c28 9 0 58.7f
c29 9 1 0.544f
c30 9 vdd 2.04f
c31 9 vss 0.5f
c32 9 6 1.16f
c33 9 7 0.0667f
c34 9 8 3.88f
c64 in_buff 0 9.26f
c65 in_buff 1 1.3f
c66 bias 0 16.2f
c67 bias 1 0.544f
c68 bias 7 0.296f
c69 bias 9 0.296f
.ends posbuff

x1 in out1 bias vdd vss1 posbuff

*vi in 0 dc 0 ac 1
vi in 0 dc 0
*vi in 0 pulse(-1.0 1.0 5ns 5ns 5ns 40ns 80ns)
*vc ctrl 0 0
*vi in 0 sin(0 1 1e7 0 0 0)
vb bias 0 dc -1.5
vd vdd 0 2.5
*vs vss 0 -5
vs1 vss1 0 -2.5
.op
.tf v(out1) vi
.include '//bifur/users/gnk/mosis/models/hdr'
*.dc vi -2.5 2.5 0.1
*.tran 1ns 300ns
*.four 1e7 v(out1)
*.ac dec 10 1 200meg
*.pz v(out1) Vi
cl out1 0 5pf
.end
**********************************************************************
 maximum nodal capacitance=  5.319E-12      on node    0:out1
**********************************************************************
 total voltage source power dissipation=  2.14097e-03      watts
**********************************************************************
 **** mosfets
 element     1:m1          1:m2          1:m3          1:m4
 model       0:mosis1_n    0:mosis1_n    0:mosis1_p    0:mosis1_n
  id       1.91349e-04   1.91349e-04  -1.91349e-04   2.12228e-05
  ibs         0.            0.            0.            0.
  ibd     -4.5397e-14   -2.88402e-14   5.15256e-14  -3.97764e-14
  vgs        1.057992      1.107115     -1.288140      0.700683
  vds        2.269851      1.442008     -1.288140      1.988823
  vbs         0.            0.            0.            0.
  vth        0.563739      0.590054     -0.663985      0.570615
  vdsat      0.359356      0.376789     -0.510222     9.89443e-02
  gm       6.93846e-04   6.63872e-04   5.48936e-04   2.35872e-04
  gds      3.7893e-05    4.27824e-05   4.14672e-05   9.05346e-06
  gmb      1.96292e-04   1.91809e-04   1.32708e-04   6.97536e-05
```

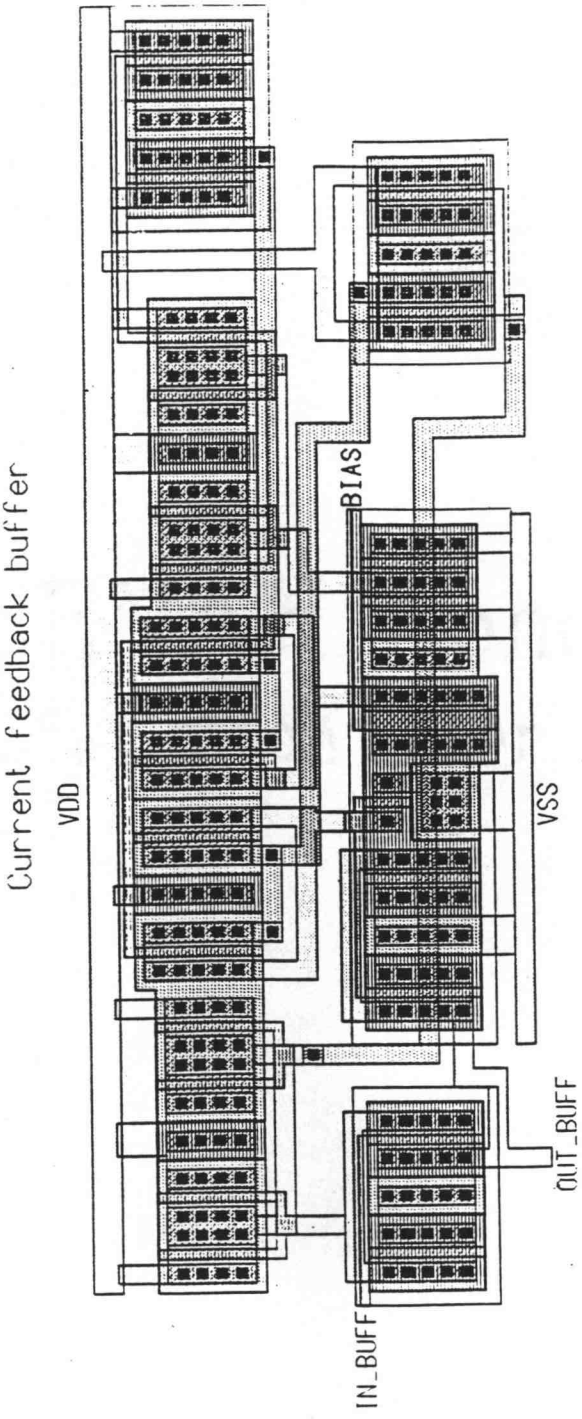
```
 cgs      4.50914e-14    4.51592e-14  8.189e-1414    2.09512e-14

element     1:m5           1:m6          1:m7           1:m8
model       0:mosis1_n     0:mosis1_p    0:mosis1_p     0:mosis1_n
 id       2.12228e-05   -2.12228e-05   -1.66544e-05   1.66544e-05
 ibs        0.          7.78578e-14     3.96204e-14     0.
 ibd     -1.10711e-14   3.97764e-14     6.3346e-144  -1.83270e-14
 vgs        1.107115     -0.725581       -1.186286      1.000000
 vds        1.107115     -1.904062       -1.186286      1.832696
 vbs        0.            1.988823        1.981019      0.
 vth        0.648676     -0.943481       -0.975403      0.695798
 vdsat      0.331056     -0.207654       -0.186554      0.228212
 gm       8.36355e-05   1.56791e-04     1.33297e-04   1.00018e-04
 gds      5.30369e-06   8.53472e-06      7.65924e-06   1.62473e-06
 gmb      2.83713e-05   1.68807e-05      1.45657e-05   3.90550e-05
 cgs      6.51703e-15   2.09638e-14      4.20080e-14   5.13635e-14

element      1:m9          1:m10          1:m18
model        0:mosis1_n     0:mosis1_p    0:mosis1_n
 id        1.66544e-05  -1.98968e-04    1.98968e-04
 ibs         0.             0.            0.
 ibd      -3.96204e-14 - 5.20372e-14    7.39814e-14
 vgs         0.680085     -1.300933     1.000000
 vds         1.981019     -1.300933     3.699067
 vbs         0.             0.          0.
 vth         0.570861     -0.663452     0.523363
 vdsat     8.33094e-02     -0.520651    0.344593
 gm        2.0149e-4      5.58248e-04   7.45742e-04
 gds       7.50992e-06    4.25384e-05   3.12464e-05
 gmb       5.97462e-05    1.34806e-04   2.01678e-04
 cgs       2.09512e-14    8.19076e-14   4.495e-14
**********************************************************************
**
 ****     small-signal transfer characteristics

      v(out1)/vi                                =    0.9222
      input resistance at         vi            =  1.000e+20
      output resistance at v(out1)              =  641.2416
**********************************************************************
```

```
**********************************************************************
 FOLDED CASCODE BUFFER

 The Hspice operating point output file. Contains the input spice
deck,operating point node voltages, nodal capacitances, static
power dissipation, operating point information for each of the
transistors and small-signal transfer characteristics.
**********************************************************************
 ******  input listing

 * devices:
 m1 1 in out out mosis1_n l=2u w=50u
 + as=150p ad=150p ps=110u pd=110u
 m2 out 6 vss vss mosis1_n l=2u w=20u
 + ad=100p as=100p pd=50u ps=50u
 m3 6 6 vss vss mosis1_n l=2u w=10u
 + ad=30p as=30p pd=22u ps=22u
 m4 6 7 1  vdd mosis1_p l=2u w=16u
 + ad=80p as=80p pd=42u ps=42u
 m5 1 4 vdd vdd mosis1_p l=2u w=60u
 + ad=300p as=300p ps=130u pd=130u
 m6 8 8 vdd vdd mosis1_p l=2u w=60u
 + as=300p ad=300p ps=130u pd=130u
 m7 7 7 8   vdd mosis1_p l=2u w=8u
 + ad=40p as=40p pd=26u ps=26u
 m8 7 bias vss vss mosis1_n l=4u w=28u
 + ad=140p as=140p pd=66u ps=66u
 m9 4 bias vss vss mosis1_n l=4u w=10u
 + ad=50p as=50p pd=30u ps=30u
 m10 4 4 vdd vdd mosis1_p l=2u w=12u
 + ad=60p as=60p pd=34u ps=34u

 * lumped capacitances:
 c1 1 0 54.6f
 c2 vdd 0 124f
 c3 vdd 1 0.75f
 *c4 out 0 48f
 c5 out 1 1.23f
 c6 4 0 30.9f
 c7 4 1 6.08f
 c8 4 vdd 0.15f
 c9 vss 0 61.7f
 c10 vss out 0.25f
 c11 6 0 19.8f
 c12 6 1 0.313f
 c13 6 vdd 0.24f
 c14 6 4 0.897f
 c15 6 vss 0.075f
 c16 7 0 31f
 c17 7 vdd 0.2f
 c18 7 4 0.0222f
 c19 7 vss 0.275f
 c20 7 6 0.471f
 c21 8 0 37.4f
 c22 8 vdd 1.33f
 c23 8 7 0.645f
 c41 in 0 11.5f
 c42 in out 1.33f
```

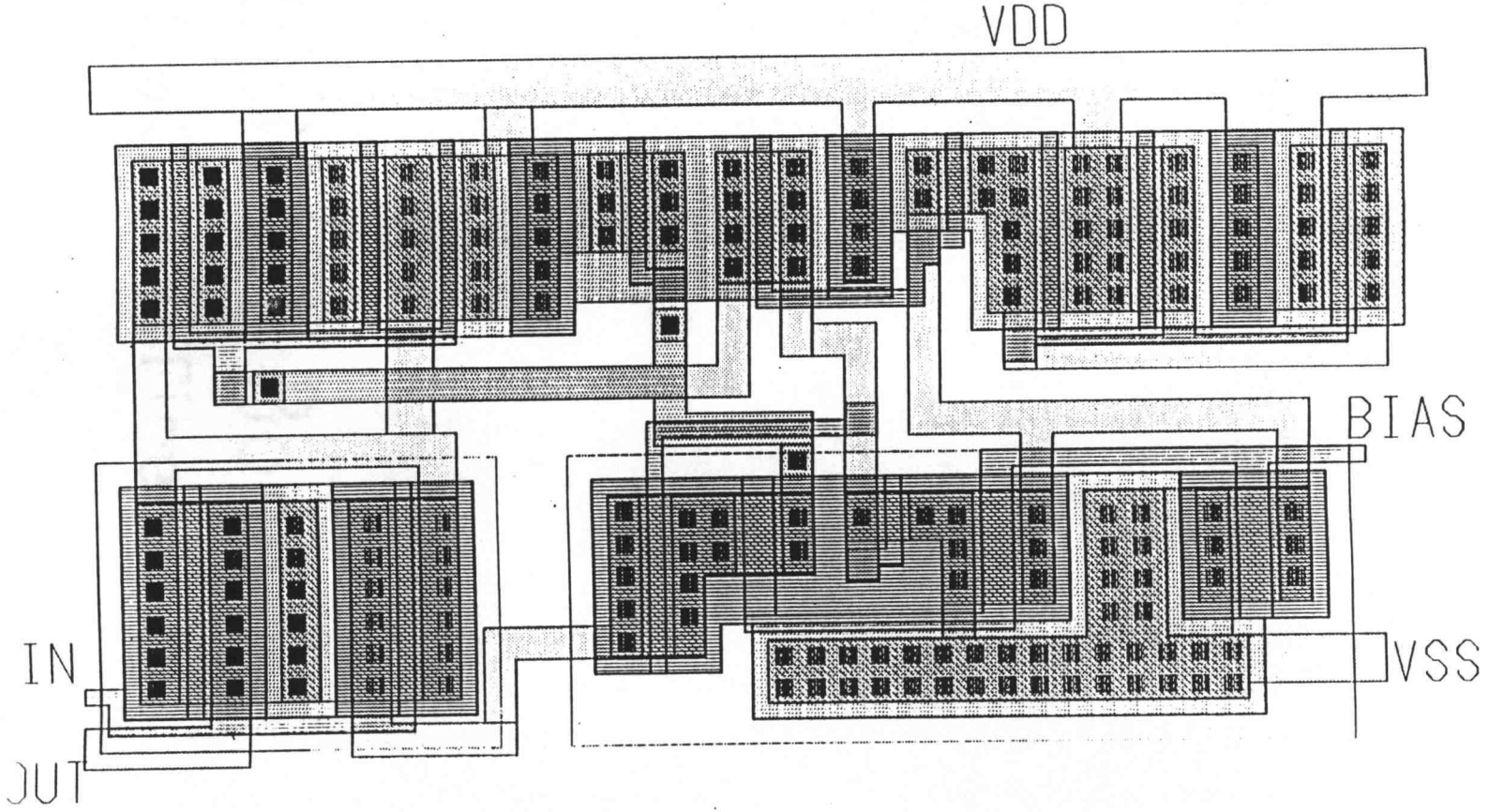
```
c43 bias 0 20.4f
c44 bias vss 0.296f
c45 bias 6 0.287f
c46 bias 7 0.592f

vi in 0 dc 0
*vi in 0 pulse (-1 1 5ns 5ns 5ns 40ns 80ns)
*vi in 0 sin(0.2 1 1e7 0 0 0)
*vi in 0 dc 0 ac=1
vb bias 0 dc -0.9
vd vdd 0 dc 2.5
vs vss 0 dc -2.5

cl out 0 5pf

.op
.tf v(out) vi
.dc vi -2.5 2.5 0.1
*.tran 1ns 80ns
*.ac dec 10 1 1000meg
*.plot ac vdb(out) vp(out)
*.pz v(out) vi
.include '//bifur/users/gnk/mosis/models/hdr'
.end

**********************************************************************
 maximum nodal capacitance=  5.104E-12      on node    0:out
**********************************************************************
 total voltage source power dissipation=  2.54123e-03     watts
**********************************************************************
 **** mosfets
 element     0:m1          0:m2          0:m3          0:m4
 model       0:mosis1_n    0:mosis1_n    0:mosis1_n    0:mosis1_p
  id        2.11435e-04   2.11435e-04   9.84301e-05  -9.84301e-05
  ibs         0.            0.            0.          1.94834e-14
  ibd      -1.59978e-14  -1.45188e-14  -1.39746e-14   3.60254e-14
  vgs         1.048117      1.397461      1.397461     -1.947804
  vds         1.599777      1.451883      1.397461     -1.654200
  vbs         0.            0.            0.           1.948339
  vth         0.573109      0.589728      0.611511     -0.955321
  vdsat       0.348838      0.571621      0.554148     -0.830468
  gm        7.98543e-04   4.57813e-04   2.20384e-04   1.71599e-04
  gds       4.84769e-05   3.73456e-05   1.76904e-05   1.67482e-05
  gmb       2.21941e-04   1.27505e-04   6.58267e-05   2.01737e-05
  cgs       5.68984e-14   2.27311e-14   1.11843e-14   1.84275e-14

 element    0:m5          0:m6          0:m7          0:m8
 model      0:mosis1_p    0:mosis1_p    0:mosis1_p    0:mosis1_n
  id       -3.09865e-04  -1.43408e-04  -1.43408e-04   1.43408e-04
  ibs         0.            0.          1.24526e-14     0.
  ibd       1.94834e-14   1.24526e-14- 3.89614e-14  -1.10386e-14
  vgs        -1.502655     -1.245264     -2.650880      1.600000
  vds        -1.948339     -1.245264     -2.650880      1.103856
  vbs         0.            0.            1.245264      0.
  vth        -0.632035     -0.661139     -0.846757      0.698572
  vdsat      -0.703532     -0.480421     -1.426485      0.669324
  gm        6.21586e-04   4.40201e-04   1.26918e-04   3.00305e-04
  gds       5.07917e-05   3.25219e-05   1.59790e-05   1.21965e-05
```

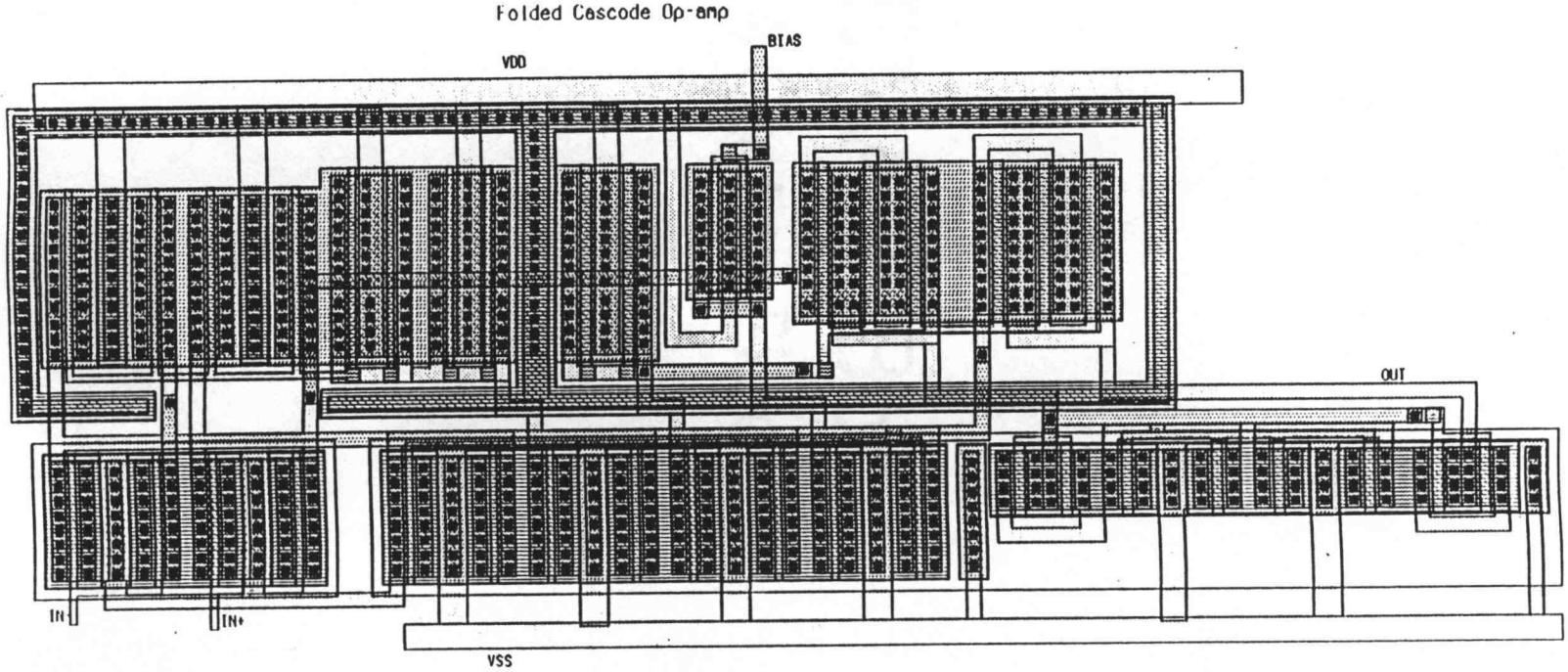
```
  gmb      1.43030e-04  1.04304e-04  1.86240e-05  1.09325e-04
  cgs      6.98497e-14  6.95523e-14  8.93340e-15  6.17597e-14

 element      0:m9           0:m10
 model        0:mosis1_n     0:mosis1_p
  id         5.49727e-05   -5.49727e-05
  ibs          0.             0.
  ibd        3.49734e-14    1.50266e-14
  vgs          1.600000      -1.502655
  vds          3.497345      -1.502655
  vbs          0.             0.
  vth          0.711879      -0.658671
  vdsat        0.650258      -0.678520
  gm         1.16853e-04    1.14362e-04
  gds        2.43034e-06    9.84473e-06
  gmb        4.43753e-05    2.75901e-05
  cgs        2.15935e-14    1.35036e-14
**********************************************************************
 ****     small-signal transfer characteristics

      v(out)/vi                                 =    0.9235
      input resistance at         vi            =  1.000e+20
      output resistance at v(out)               =  548.3234
**********************************************************************
```

Appendix B. Buffer and Op-amp layouts



Folded Cascode Buffer




Folded Cascode Op-amp
BIAS
VDD
OUT
IN-
IN+
VSS