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A new approach to oversampled delta-sigma A/D converters ($\Delta\Sigma$ modulators) is introduced, where a differential pseudo-*N*-path filter stage is used as a basic cell. In this band-pass application, the z to $-z^N$ transformation is employed to realize a RAM-type pseudo-2-path lossless integrator. The bandpass second-order and 4th-order delta-sigma A/D converters are implemented by switched-capacitor (SC) circuits using this kind of integrator. The effects of components inaccuracy, finite op-amp gain, as well as clock feed-through noise are studied in simulations. The results verify that such A/D converters possess a remarkable insensitivity to imperfect components and a high signal-to-noise ratio (SNR). A 6th-order dual-quantizer delta-sigma A/D converter with a digital canceller is then designed, which achieves 86 dB (>14 bit) conversion accuracy and 95 dB (>15 bit) dynamic range for a low oversampling ratio (OSR=32) even with low-accuracy analog components (4-bit internal D/A with 6-bit linearity).

Analysis and Design of Bandpass Delta-Sigma A/D Converters

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Head of Electrical and Computer Engineering Department

Dean of Graduate School

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Introduction

Today's fine-line VLSI technology offers high speed and high density, but a reduced signal range due to the reduced bias voltage. On the other hand, the accuracy of analog components is low, unless laser trimming is used. Self-calibration techniques consume more than 200% area of the original circuit [1] , and only achieve 12-bit conversion accuracy in many A/D converter cases [2]. So the reduction of dynamic range and analog resolution in data conversion is unavoidable.

Hence, an exchange of digital complexity and speed for analog resolution in a mixed-mode (digital and analog, voltage and current) environment is needed. A possible answer is to use oversampling data converters, discussed in chapter 2. Classified by basic operation, there are predictive converters, noise-shaping converters, and combined predictive/noise-shaping converters [3]. In oversampling data converters, the dynamic range or converter resolution is primarily determined by the system's structural parameters: the oversampling ratio and the order of the converter.

An efficient oversampling data converter structure, which possesses noise-shaping performance, is the delta-sigma modulator. It offers the benefits of inherent linearity, reduced anti-aliasing filter complexity, and high tolerance to component imperfection [4]. The insensitivity to component imperfection is the main advantage of a delta-sigma modulator in comparison with a predictive converter [5].

A traditional delta-sigma modulator is a lowpass converter (LΔΣ modulator). It places all the noise transfer-function zeros at $\omega=0$, in order to suppress the quantization noise in a narrow band around DC. As described in chapter 3, this noise-shaping concept can be extended to the bandpass case [6]. There, the noise transfer-function zeros are placed at $\omega=\omega_0>0$, and the quantization noise is drastically reduced in a narrow band around ω_0. For a narrow band signal away from DC, a bandpass delta-sigma modulator can achieve a high signal to quantization noise ratio at a lower sampling rate than required for a lowpass delta-sigma modulator. Also, the in-phase and quadrature components of a bandpass delta-sigma modulator can be separated easily [7].

A lowpass filter can be transferred to a bandpass filter through the z to z^N or z to $-z^N$ mapping [8]. The same transformation can be employed to obtain a bandpass delta-sigma converter (BΔΣ modulator). In this research, a RAM type pseudo-N-path filter stage is used in a differential lossless integrator to construct some novel configurations. In chapter 4, a second-order and a 4th-order BΔΣ are examined carefully. There, simulations are concentrated on the most common problems of integrated

realizations , i.e., the component imperfections. The results exhibit the theoretically predicted insensitivity. In chapter 5, a 6th-order dual-quantizer BΔΣ is described, along with a digital canceller. It can maintain a high performance at low OSR, even with low analog component linearity.

Chapter 1

General Procedure

1.1 Research Outline

First, we need study the special requirements in different applications. Only in a specified subregion can we set some criteria to compare any advantage or limitation of the different configurations. The subregion of interest here is the application in spectrum analyzers, voice processor, digital radios, televisions, etc. In these applications an A/D converter is used as a waveform coder in a relatively low-speed environment. The fidelity of reconstruction of the input waveform from an A/D output is measured by the signal-to-noise ratio (SNR). Otherwise, for a data acquisition A/D, the peak instantaneous error is commonly used as the performance measure of the conversion .

Second, we can simulate some reported circuits to obtain a comparison, while designing and simulating our novel schemes. The nonideal effects introduced by any capacitor, op-amp, and internal converter must be analyzed. Sometimes, a new scheme may be impractical due to excessive sensitivity.

In the last stage, an integrated chip may be laid out and fabricated . If necessary, the first realization may be built only in a

breadboard using commercial IC's for testing and trouble-shooting. But in this thesis research, this last stage is not included.

1.2 Simulation Procedure

The detailed steps to deal with the second stage of the research tasks mentioned above can be described as follows:

1. The feasibility analysis is performed by simulations in the time domain on the functional level (system level). Some of these are illustrated in the block diagrams Fig.4 (b), Fig.5 (a) and Fig.21. At this level, the simulations are performed by solving difference equations. For any new idea or novel structure, the basic performances will be examined on this level. The simulation programs required are written in the C or FORTRAN languages. The frequency of an input signal is increased step by step, so that the frequency region of interest can be scanned fast and automatically.

2. If the results of Step 1 are acceptable, then the switched-capacitor circuits are implemented in the schemes shown in Fig.5 (b), Fig.12, and Fig.16.

However, for further simulations, several components need to be modified to fit the special requirements of the simulation software-package described in Step 3. For example, a differential internal A/D converter may be constructed by using an subtractor, a single-end A/D converter, and an inverter.

3. Schemes on the component level (circuit level) are simulated by using the software package GCK [9], SWITCAP [10] or SWITCAP/2 [11]. At this level, the simulations are performed by solving charge-redistribution equations.

SWITCAP and SWITCAP/2 are more powerful to simulate larger circuits. They possess the capability of frequency analysis and spectrum analysis. But the spectrum analysis is bounded by a fixed windowing function. Moreover, there allow no resistors, no quantizers, and no delay elements. Some subcircuits can be developed as shown in Fig.8 and Fig.9.

4. The signal-to-quantization-noise ratio can be determined by analyzing the time-domain data obtained from Step 1 or Step 3, using Fast Fourier Transformation (FFT) [12]. The program is written in FORTRAN, which is convenient for operation in complex variables.

Since a different window function gives a quite different frequency-domain result [13], a Hanning window is used throughout this research, to pre-weigh the input data of the FFT.

The output spectrum is a convolution of output signal spectrum with the spectrum of the window function. Since a deconvolution is too complex to use as a general mathematic operation following the FFT, to renormalize the spectrum peak is not practical. If we want to compare the frequency domain results between different schemes or implementations under same scale, all we need is the same relative peak height from the noise floor, no matter whether the peak is above or below 0 dB.

5. The simulation results on the component level are compared with those on the functional level. Both of them are under ideal conditions. If they coincide with each other, then the nonideal effects can be investigated one by one.

The parameters of some selected components will then be changed from their ideal values, and the names of these components will be shown. The other components remain anonymous. If the nonideal component changes not only its parameter value, but also its configuration from the ideal model, then a subcircuit must be called up to replace the component in the scheme, and in the simulation program as well. An example is a nonideal MOS transistor switch used in the clock feedthrough simulation, which includes *Cgs, Cgd, Cbs, Cbd,* and a *Ron* shown in Fig.15.

6. After the schemes or scaling factors have been improved, sometimes the amplitude or the frequency of the input signal is changed, and the simulation on both functional and component levels is run again. Finally, the input signal level versus signal-to-noise ratio is plotted to obtain a global view. The highest peak of SNR and the intersection points with the 0 dB axis are found to determine the conversion accuracy and dynamic range.

Chapter 2

Oversampled A/D Converter

2.1 The Oversampling Method

Oversampling means using artificially high sampling rates, which may be several orders higher than the Nyquist rate. Suppose that a signal is in frequency band $0 \leq f < f_b$, then the Nyquist rate is $2f_b$, and the oversampling ratio is defined as the ratio of sampling rate to Nyquist rate:

$$OSR = f_S / 2f_b \qquad (1)$$

Fig.1 shows the output waveform difference between a conventional multibit flash A/D converter (a), and a single-bit oversampling delta-sigma A/D converter (b). Both are sinusoidal responses. Fig.1 (c) is the response of a multibit oversampling delta-sigma A/D converter. The input is a ramp signal.

The output signal of any oversampling converter oscillates between internal quantizer levels. It does not necessarily have a one-to-one correspondence to the input signal, but its local average equals the average of the input signal [5]. Like the radio FM band may present higher quality than AM band, the oversampling method trades resolution in time for resolution in amplitude. The resolution of a PCM system can be improved by increasing the frequency (increasing the OSR) at a given component accuracy; but

the fine dividing of a PCM signal amplitude is directly limited by the device accuracy.

There are several different structures of the oversampling converter, as shown in the block diagrams of Fig.2. Any version of an oversampling converter has an internal A/D in its forward path and an internal D/A in its feedback path. At least one feedback loop is closed at the comparison point where an input signal, say X, enters. While the feedback signal approaches the input signal X at this point, the output signal, say Y, is forced to trace X. But most conventional converters are open loop systems. In general, a feedback system can use lower accuracy in-loop components, while maintaining the same performance quality. Further discussion will be continued in section 2.4.1.

However, an oversampling converter is slower than a conventional converter by the factor OSR. Bounded by the speed limitation, the oversampling converter is now used mainly in the audio frequency region. Also, as a feedback system, stability is always one of the design considerations.

2.2 Predictive Converters

2.2.1 Predictive converters

In the family of the oversampling converters, most early work was concerned with the predictive converter. Its basic structure is shown in the block diagram of Fig.2 (a), where X is an input signal, Y is an output signal. In the system analysis,

assuming that the internal A/D and D/A converters are ideal, we can model the A/D converter as a linear device adding the quantization error; and the D/A converter as a unit gain device. The input-to-output z-transfer function is

$$Y(z)=Hp(z)[X(z)+E(z)] \quad (2)$$

$$Hp(z)=1/[1+H_d(z)] \quad (3)$$

where $E(z)$ is the z-transfer of the quantization error. The loop filter function $Hp(z)$ is a predictive characteristic factor, which creates a linear distortion of input signal $X(z)$. The distortion can be removed by a matched demodulator as illustrated on the right part of Fig.3 (a), provided that the decoding transfer function is chosen as $Hp^{-1}(z)$. The restored signal will then be

$$X^*(z)=X(z)+E(z) \quad (4)$$

For reducing the prediction error, an approach to cancel the first N terms of the mean square prediction error $<E_N^2>$ was recommended [14]. The resulting optimum predictive filter of a Nth-order predictor is

$$Hp(z)=(1-z^{-1})^N \quad (5)$$

For $N=1$, this leads to the delta modulator, shown in Fig.3 (b), which is the most popular predictive converter. But in its transfer function (2), $X(z)$ and $E(z)$ are also bonded together. So, the output of a predictive converter is always contaminated with the quantization noise directly. However, larger values of X are possible, and hence the signal-to-noise ratio can be increased.

2.2.2 Noise-shaping converters

A noise-shaping converter reduces the quantization noise power inside of the signal band. In contrast to a predictive converter, it changes the spectrum of the noise but leaves the input signal unchanged, except for some delay. As illustrated in Fig.2 (b), its output transfer function is:

$$Y(z)=z^{-N}X(z)+H_{NS}(z)E(z) \quad (6)$$

$$H_{NS}(z)=1/[1+H_a(z)] \quad (7)$$

where $H_{NS}(z)$ is noise-shaping characteristic factor.

2.2.3 Predictive/noise-shaping converters

A predictive and a noise-shaping converter can be combined with each other to obtain a structure shown in Fig.2 (c). In this case,

$$Y(z)=Hp(z)\,[X(z)+H_{NS}(z)E(z)] \quad (8)$$

In a predictive converter, the digital filter $H_d(z)$ can be designed to make the feedback signal approaching the input signal X. After subtracting, a small deviation is sent to the input terminal of the internal A/D. This allows X to swing without internal A/D clipping in a range larger than that of a noise-shaping converter. On the other hand, the noise-shaping converter shifts the quantization noise spectrum out of the signal band, and leaves a small in-band noise. Thus, the combined predictive/noise-shaping converter has some of the advantages of both oversampled converters.

2.3 Error-Feedback Structure

2.3.1 Ideal noise-shaping performance

In Fig.4 (a), the block diagram of a first-order system is used to illustrate the general concept of an error-feedback converter. It was first described in the 1950's [15]. The main idea is to measure the quantization error by subtracting the input and output signal of the internal A/D, then to compensate this error by feeding back the measured quantity and subtracting it from the next input sample. This represents a form of prediction. The output transfer function of this error-feedback converter presents a typical noise-shaping form:

$$Y(z)=X(z)+(1-z^{-1})E(z) \tag{9}$$

The quantization noise is highpass filtered by the differentiating factor $(1-z^{-1})$. Replacing z by $exp(j\omega\tau)$:

$$|1-exp(-j\omega\tau)|=sqrt\{[1-cos(\omega\tau)]^2+sin^2(\omega\tau)\}$$

$$=2sin(\pi f/2f_s) \tag{10}$$

While the input signal band is limited to $0 \leq f < f_s/2$ by the anti-aliasing filter, the $(1-z^{-1})$ factor shapes the quantization noise spectral density in the frequency range of $0 \sim f_s/2$, resulting a curvature like the sine waveform in the first quarter period. This is true provided that the input signal is busy, and the quantization noise is nearly white.

2.3.2 Sensitivity problems

Unfortunately, in practical implementation, the inaccuracy of the analog subtractor degrades the noise shaping. An example is

given in the following component level simulation. The block diagram of a modified error feedback converter is shown in Fig.5 (a), and its switched-capacitor circuit realization is shown in Fig.5 (b). This circuit achieves a third-order noise-shaping performance. The ideal sinusoidal response is plotted in Fig.6 (a). However, when a capacitor in one of the subtractor branches has a 0.5% inaccuracy, the RMS noise increases drastically, and hence the signal-to-noise ratio drops sharply. The result is plotted in Fig.6 (b). Further investigation reveals that any inaccurate capacitor or an op-amp with finite DC gain in the feedback path will distort the desired feedback function Fi and spoil the performance [16]. Therefore, the error feedback structure cannot be used as an independent A/D converter, but it can be used as a demodulator or a D/A converter in a digital environment.

2.4 Delta-Sigma Converter

A delta-sigma converter is algebraically equivalent to an error feedback converter. The first-order delta-sigma converter in the block diagram of Fig.4 (b) employs an accumulator with a transfer function

$$H_a(z)=z^{-1}/(1-z^{-1}) \qquad (11)$$

The resulting output is similar to (9), given by:

$$Y(z)=z^{-1}X(z)+(1-z^{-1})E(z) \qquad (12)$$

2.4.1 Loop gain and in-loop components

According to equation (11), the gain of the accumulator is given by

$$|H_a(f)| = |z^{-1}/(1-z^{-1})|_{z=e^{j\omega\tau}}$$

$$= [2\sin(\pi f/2f_S)]^{-1} \approx f_S/2\pi f \qquad (13)$$

In this lowpass converter case, the passband is centered at $f=0$. At the band center the ideal gain of the accumulator is infinite; away form the band center the gain decreases as a $1/\sin(f)$ waveform. This is true for the bandpass case as well. Fig.7 shows the accumulator output waveform corresponding to a input sine wave signal. These are open loop output waveforms without clipping. The frequency of the input signal is exactly at the band center in Fig.7(a), in contrast with being away from the band center in Fig.7(b). We can see from Fig.7 (a) that the infinite accumulator gain drives the output to a increasing amplitude until saturation limits it. Both functional and component level simulation provide the same curves.

In a narrow signal band, the accumulator gain approximates OSR/π. By increasing OSR, the gain $|H_a(f)|$ can be raised high enough to eliminate the inaccuracy effects introduced by some in-loop components. The frequency domain transfer function of the delta-sigma converter in Fig.4 (b) is

$$Y(f)/X(f) = H_a(f)H_{A/D}(f) / [1 + H_a(f)H_{A/D}(f)H_{D/A}(f)]$$

$$\approx [H_{D/A}(f)]^{-1} \qquad (14)$$

where $H_{A/D}(f)$ is the transfer function of the internal A/D. It includes the nonlinear distortion other than the quantization noise. In comparison with the gain of $H_a(f)$ defined by (11) and (13), $H_{A/D}(f)$ can be neglected. $H_{D/A}(f)$ is the transfer function of the internal D/A; it also includes the nonlinear distortion.

According to (14), the misplaced A/D threshold causes little trouble on baseband properties of a delta-sigma converter. [17] However, the quality of the internal D/A will determine the conversion resolution and system stability of a delta-sigma converter. In Chapter 5, a special strategy will be developed to compensate the nonlinearity of an internal D/A.

2.4.2 Number of the quantizer levels

Although, a single-bit internal A/D or D/A is inherently linear, a multibit delta-sigma converter has a higher signal-to-noise ratio. This ratio in the passband is calculated from

$$SNR=10Log\ [X(\omega_S)^*X(\omega_S)/\int_0^{f_b} E(\omega)^*E(\omega)d\omega] \qquad (15)$$

The asterisk * means the conjugate complex quantity. Because the quantization noise is treated as a white noise, the mean square value of the quantization noise is given by:

$$e^2_{rms}=1/\Delta\left(\int_{-\Delta/2}^{+\Delta/2} e^2 de\right)= \Delta^2/12 \qquad (16)$$

The quantization step size Δ is proportional to 2^{-M}, where M is the number of the quantizer bits. As the quantization noise

decreases exponentially with M, the SNR increases. Also, the system stability increases, for the feedback loop more closely approaches a linear system.

The internal A/D converter must be a flash type converter, because stability of the loop requires low-delay conversion.

For SWITCAP/2 simulation, a multibit internal A/D converter was designed. It is a 4-bit flash A/D, shown in Fig.8. The resistors can be made of polysilicon, but here each one is assumed to be a switched-capacitor subcircuit as shown in Fig.9 (a). These SC resistors share a internal clock signal *ckf* with the latched comparator shown in Fig.9 (b). This clock is 5~10 times faster than the actual sampling frequency. It works well in a intermediate frequency region. The sinusoidal response of this all-SC flash converter has been shown in Fig.1 (a).

Chapter 3

N-path Delta-Sigma Converters

3.1 Bandpass Converters

3.1.1 Bandpass modulation

A bandpass delta-sigma converter (BΔΣ) has a higher center frequency in comparison with a LΔΣ, and this advantage may offer the potential capability for future video frequency applications.

The present tendency for A/D converters is to reduce the requirements for pre-filtering and moving the converter toward the analog signal source [1]. Bandpass delta-sigma converter are well suited for use in the front-end of radio receivers, allowing direct conversion to digital form at the intermediate frequency (IF). An early conversion to digital signal results in a more robust system with improved IF-strip testability [18].

Fig.10 illustrates a bandpass delta-sigma modulator and its demodulator. In communications, the single-sideband modulation system faces three key tasks [19]:

<1> Intermediate frequency filtering.

<2> In-phase and quadrature-phase components separation.

<3> High accuracy analog-to-digital conversion.

All of these tasks can be easily accomplished by using a bandpass delta-sigma modulator.

3.1.2 The z to $-z^N$ transformation

A bandpass delta-sigma converter can be easily transformed from a LΔΣ. Comparing the structure of the BΔΣ in Fig.10 with the LΔΣ in Fig.4 (b), the difference is that a BΔΣ uses a bandpass filter to replace an accumulator in a LΔΣ. Such a replacement in the z-domain is the frequency transformation of z to z^N, mapping an nth-order lowpass filter $H(z)=(1-z^{-1})^{-n}$ into an nN_Lth-order bandpass filter given by

$$H_{a_L}(z)=(1-z^{-N_L})^{-n} \qquad (17)$$

Another way to obtain a BΔΣ is from a highpass delta-sigma converter (HΔΣ), through the transformation of z to $-z^N$, resulting in an nN_Hth-order bandpass filter given by

$$H_{a_H}(z)=(1+z^{-N_H})^{-n} \qquad (18)$$

A detailed analysis [20] of (17) and (18) indicated that in both functions unit-circle noise transmission zeros are realized. For $H_{a_L}(z)$ the zeros are at $exp[-j(2k+1)\pi/N_L]$, $k=0,1,2,\ldots, N_L-1$; for $H_{a_H}(z)$ the zeros are at $exp[-j2(k+1)\pi/N_H]$, $k=0,1,\ldots, N_H-1$. Usually we select a band center at $f_S/4$ for easy separation of I and Q, and then the noise transmission zeros should be at $z_{1,2}=\pm j$. This can be achieved with the minimum order $N_L=4$, for $H_{a_L}(z)$. But for $H_{a_H}(z)$, only $N_H=2$ is needed.

If we just want to minimize the order of the bandpass filter, but do not specify the band center frequency at $f_S/4$ [21], then the passband of $H_{a_L}(z)$ can be centered at half of the sampling frequency. To avoid the upper half of the passband aliasing with that of lower half, the minimum N_L must be 3. However, the

passband of $H_{a_H}(z)$ can be centered at $f_S/(2N_H)=f_S/4$, free from the aliasing problem, if $N_H=2$ is chosen as before. Because in the z to $-z^N$ transformation, the loss response of the resulting filter is the same as z to z^N transformation, but shifts $\pi/NT_S/_{N=N_H}$ along the frequency axis:

$$-z^{N_H}=e^{j(\omega N_H T_S+\pi)}=e^{jN_H T_S(\omega+\pi/N_H T_S)} \qquad (19)$$

3.1.3 Transient requirement

The settling requirements of a BΔΣ, whether it comes from the z to z^{N_L} or z to $-z^{N_H}$ transformation, are no more stringent than those of a LΔΣ , because sufficient settling depends on the op-amp design, the bias currents, and the capacitor sizes. Assuming that the integrator outputs are not saturated, the settling constant is based on the sampling rate, not on the input signal frequency [18]. Furthermore, incomplete settling of transient in a SC converter affects its SNR in a manner similar to the degradation due to finite op-amp DC gain [22]. Therefore the op-amp bandwidth and slew-rate requirements are not discussed in this thesis.

3.2 Pseudo-N-Path Filter with RAM Type Operation

3.2.1 Pseudo-N-path approach

The realization of transforming a HΔΣ to a BΔΣ is illustrated in the block diagram of Fig.11 (a), which was originally introduced for continuous-time system [8]. The center frequency of an N-path filter is f_S/N, independent of circuit parameter variations. If a perfect match exists between the N paths, the phasors of the unwanted mirror frequencies form a polygon with zero resultant. Otherwise they appear at the output, including a component at the center of the passband. To overcome the sensitivity to signal path mismatch, the pseudo-N-path approach can be used, where only one physical path exists, though the entire circuit acts as a different path for different time periods. Each memory-possessing element in the path is connected to a delay line which discharges and recharges these elements circularly or as a random access memory.

Since the op-amp is shared by every path, the source of path mismatch will come from the capacitors and switches. The values of the capacitors $C1$ or $C2$ in Fig.11, which form the storage-elements of the delay line and circulate charge in and out of feedback capacitor CF, do not affect the transfer function. This statement is valid only when the op-amp gain is high enough to provide a virtual ground [23].

3.2.2 RAM type operation

The charge packet in the circulating-delay-type operation is transferred 3 times during a path period T, via C_1-C_2-C_F-C_1 , while in the RAM-type operation it is transferred twice, via C_1-C_F-C_1 (phase b), or C_2-C_F-C_2 (phase a). Moreover, one of these two transfers, C_i-C_F , is lossless, since the charge is later returned from C_F to C_i, reunited with the charge which remained in C_i due to the first incomplete transfer [8]. So the RAM-type operation is faster than circulating-delay-type operation and is less affected by finite op-amp gain.

It is well known that the circulating-delay-type operations can get rid of the band-center clock feedthrough noise. A hybrid-type circuit [24] and some modified circulating-delay-type operations [25] also achieve clock feedthrough immunity. The RAM-type operation, if used in a lowpass-based bandpass filter, will suffer from clock feedthrough noise [8]. However, if it is used in a highpass-based bandpass filter, the problem can be eliminated completely, for its passband has been shifted by $\pi/N_H T_S$ [26] .

Chapter 4

Fully Differential Mode Operation

4.1 Basic N-path Integrator

To make the circuit stray-insensitive, the RAM-type pseudo-2-path integrator can be implemented in a fully differential mode [27] [28]. In the differential circuits the dynamic range is doubled, the power supply noise and clock feedthrough noise are attenuated, and the even harmonics are suppressed [29].

The operation can use the scheme of a multibit second-order bandpass A/D converter as shown in Fig.12. When phases "a" and "1" are high, capacitor C_F receives charge from the two input capacitors C_i (one connects the input signal, the other connects the output feedback signal) and the storage capacitor C_1'. C_1' is symmetric with C_1, but is in the opposite path. This operation gives the sign inversion. During phases "a" and "2", the updated charge in C_F is transferred back to C_1 which is in the same side of C_F. The operation is repeated during phase "b". The resulting z-domain transfer function of the differential pseudo-2-path integrator is

$$H(z)=(V_{out}^{+}-V_{out}^{-})/(V_{in}^{+}-V_{in}^{-})=-C_i/[C_F(1+z^{-2})] \qquad (20)$$

Fig.13 (a) shows the frequency response of this basic bandpass integrator. The band center is located at $f_S/(2N_H)$ as

discussed in the previous chapter. This guarantees a good frequency stability, for the band center frequency is automatically locked to a specified value determined only by the sampling rate and the path number.

4.2 Second-Order BΔΣ

4.2.1 Ideal performance with different quantizer resolutions

Using the integrator of section 4.1, the 4-bit second-order bandpass A/D converter of Fig.12 achieves a good noise-shaping performance. The simulation result is plotted in Fig.13 (b). The output signal spectrum of the same kind of BΔΣ, but using single-bit internal A/D and D/A converters, is plotted in Fig.14 (a). As a comparison, the noise-shaping curves of a second-order LΔΣ are plotted in Fig.14.(b), with 4-bit and 1-bit quantization.

4.2.2 Immunity to clock feedthrough noise

The symmetry of a differential configuration suppresses the switch-coupled noise as a common mode noise, and the RAM type operation shifts the unsymmetrical clock feedthrough noise out of signal band. When imperfect switches modeled in Fig.15(b) or (c) are introduced, the simulation results of both multibit and single-bit second-order BΔΣ are exactly the same as that for ideal switches, which are already plotted in Fig.13 (b) and Fig.14 (a). Hence it is

not necessary to plot the resulting spectra of the simulations with nonideal switches.

4.3 4th-Order BΔΣ

4.3.1 Stability

When the order of a delta-sigma converter is higher than 3, the converter can only be conditionally stable. Here, the definition of stability is changed from BIBO to "unclipped signal levels occurring throughout the system" [30].

To investigate the stability property, a 4th-order BΔΣ was implemented as shown in Fig.16. As for any nonlinear system, the stability of a delta-sigma converter depends on both the amplitude and the frequency of its input signal [31]. It is difficult to apply limit cycle or phase plane analysis to these circuits when implemented at the component level. This leaves us the choice of using a stable-input test. It is a necessary, but may not be a sufficient condition [32]. The detailed form of the frequency response for various input amplitude levels is plotted in Fig.17 (a). It shows that the quantization noise increases drastically when the amplitude of input signal rises to 0 dB, i.e., the same value as the internal converter reference voltage, since clipping entails a loss of state information, and hence a performance degradation.

Given a fixed oversampling ratio of 32, the passband center and bandwidth are given by

$$F_C=F_S/(2N_H)=4096/(2x2)=1024 \quad (21)$$

$$Bw=F_S/(2\ OSR)=4096/(2x32)=64 \quad (22)$$

The signal-to-noise ratio in the passband can be calculated from equation (15). But, now the summation accumulates from F_C-$Bw/2$ to F_C+$Bw/2$. The relationship between the signal-to-noise ratio and the input signal amplitude is plotted in Fig.17 (b). The simulation results on a functional level and on a component level agree well.

4.3.2 Sensitivity to capacitor inaccuracy and to finite op-amp DC gain

The immunity to nonideal effects is the most attractive advantage of the differential pseudo-2-path delta-sigma converter. Its frequency response, obtained using a 4096-points FFT analysis, demonstrates this property. If the nonideal effects introduced are capacitor mismatches $\pm$0.5%, or a finite op-amp gain 1E3 (60 dB), no significant degradation can be observed.

If the mismatch of some important capacitors increases to $\pm$2%, the degradation is still negligible, as shown in Fig.18 (a) where the input amplitude is -9dB, to avoid clipping. Moreover, as mismatch is introduced to different capacitors, the increased RMS noise levels are almost identical. So, the effects of C49 mismatch, shown in Fig.18 (b), can be used as a general example of all capacitor mismatch effects.

If all the op-amp gains drop to 100 (40dB), the resulting degradation is still be acceptable, as shown in Fig.19 (a). This nonideal condition is more serious than that described in most

papers, where the value of a finite op-amp gain ranges from 1E3 (60 dB) to 1E4 (80 dB).

The comparison in terms of signal-to-noise ratio is plotted in Fig.19 (b). The largest difference between the results for ideal conditions and for finite op-amp gain (40 dB) is 5.1 dB. This inaccuracy is less than one bit. The largest difference between the ideal results and that for capacitor C49 mismatch (+2%) is 1.8 dB. This performance is truly remarkable.

Chapter 5

Digital Correction

5.1 Dual Quantizer Configuration

Fig.20 (a) shows the output spectrum of a multibit 4th-order BΔΣ, in comparison with the spectrum of a single-bit one. Both are implemented in a differential RAM-type 2-path configuration. Obviously, the conversion accuracy is improved by increasing the number of internal A/D and D/A levels, as discussed in section 2.4.2 . The required linearity of a multibit internal D/A is very difficult to achieve if we do not use off-chip elements and/or trimming [33], or on-chip calibration. A way to cancel the nonlinear D/A error by using a programmable memory (EPROM) was suggested in [34]. Another approach is to employ a single-bit feedback loop in addition to a multibit feedback loop, and then reduce the multibit D/A's error by filtering [35].

Fig.21 shows a dual-quantizer configuration of a multibit 6th-order 2-path BΔΣ. A 4-bit internal A/D and D/A is used to feed back signal to the last stage, in order to achieve multibit resolution and stability. A comparator with a threshold reference set at 0 is used as a ideal single-bit A/D-D/A, feeding back signal to the other stages for linearity. Three feedback loops are formed. The system noise includes the quantization errors e_4 and e_1, generated by the

multibit and single-bit A/D converters respectively, and the nonlinear error d_4 introduced by the 4-bit D/A. From (16), e_1 has greater mean square value than e_4 has. Hence, e_1 must be canceled completely. So a high order digital canceller is employed. Also, e_4 can be noise-shaped. Thus to attenuate d_4 by the first two bandpass filters together with the digital canceller is the reason of raising the order of this configuration to six. To ensure that the system is stable for a given clipping level, the equivalent scaling method is introduced [36]. Two scale factors of 0.5 are placed in the forward path to prevent integrator overload [37]. This allows the single-bit quantizer to have a full scale output swing $\pm Vref$, same as that of the multibit one.

After the digital correction, the overall output signal is given by:

$$Y(z)=z^{-2}X(z)/4+(1+z^{-2})^3E_4+z^{-2}(1+z^{-2})D_4 \qquad (23)$$

The quantization noise of the multibit A/D is thus 6th-order filtered, and the nonlinear error of the multibit D/A is second-order corrected.

5.2 Performance for Inaccurate Internal D/A

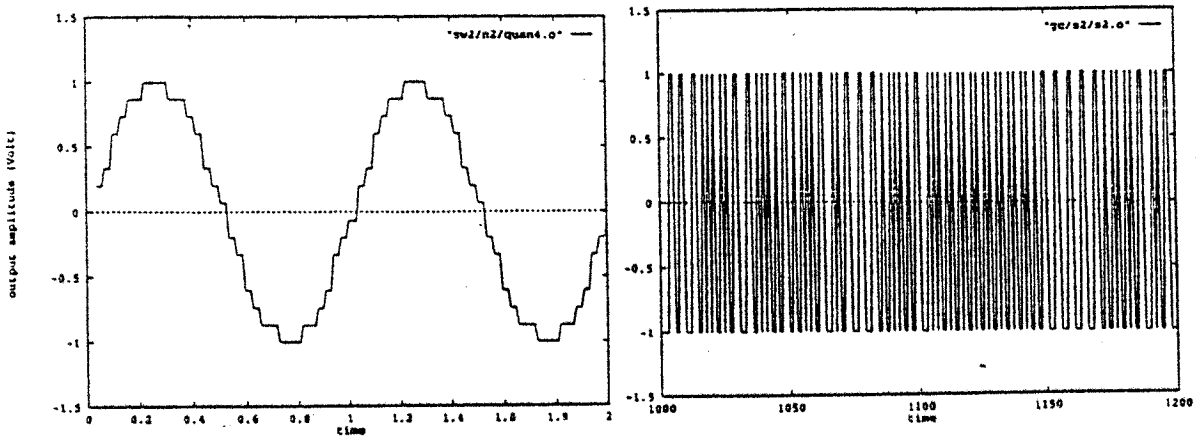
Given an oversampling ratio as low as 32, and using a 8192-points FFT, the output spectrum with linear D/A is plotted in Fig.20 (b) as a standard for comparison purpose. This configuration achieves a 86 dB signal-to-noise ratio (>14 bit conversion

accuracy). If we define the dynamic range as the region between the input amplitudes corresponding to the highest conversion accuracy and to a 0 dB SNR, this BΔΣ achieves a 95 dB (>15 bit) dynamic range. When the nonlinearity of the 4-bit D/A is introduced, from the characteristics of the SNR versus input signal level plotted in Fig.22, it can be seen that the 4-bit D/A with 8-bit or 6-bit linearity does not degrade the performance appreciably. This result is in agreement with [35]. Even for a 4-bit D/A with only 4-bit linearity, the resulting curve is still acceptable. Its conversion accuracy reaches 84 dB , dynamic range is 86 dB. Also, the even worse cases of D/A converters with 3-bit or 2-bit linearity are plotted there.

Thanks to the precision of the digital circuit, the cancellations are exact and independent of the frequency of input signal. The three analog blocks are implemented using the differential 2-path integrators discussed before. The whole circuit is highly insensitive to capacitor mismatch, finite op-amp DC gain, and clock feedthrough noise.

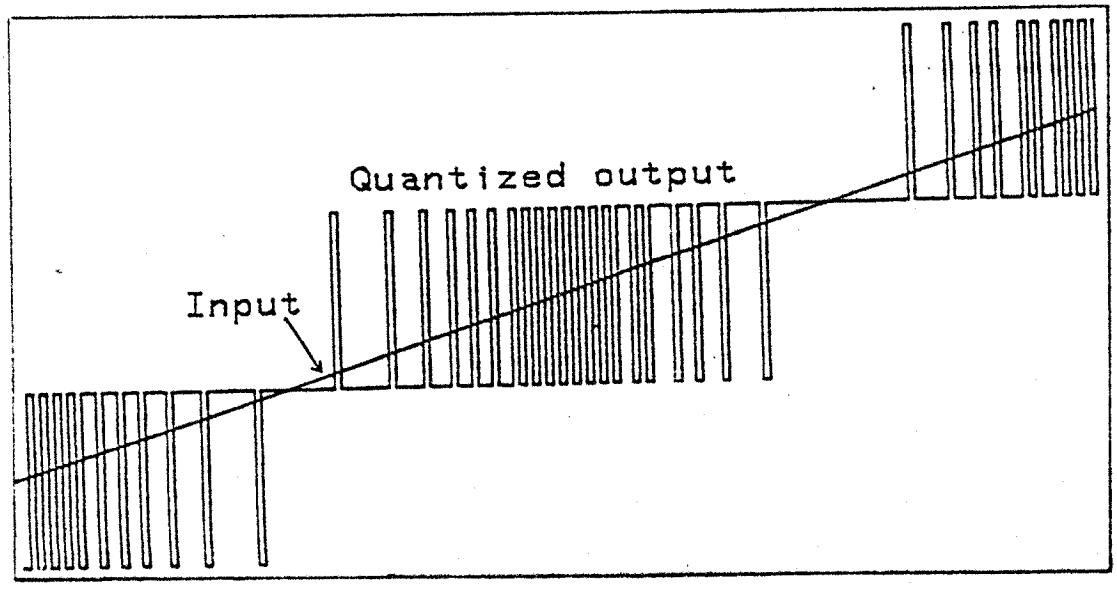
Conclusion

It is a promising design technique to use a differential pseudo-*N*-path RAM type filter stage in a basic bandpass integrator. A second-order and a 4th-order delta-sigma A/D converters were designed, taking advantage of all the techniques mentioned in previous Sections 3.1.2, 3.2.2, 4.1, and 4.2.2. The resulting converters have a high signal-to-noise ratio and insensitivity to stray capacitor effects or element inaccuracy, finite op-amp DC gain, and signal band clock feedthrough noise. As an attractive application, the 6th-order dual-quantizer BΔΣ exhibits the above immunities, in addition to the improvements contributed by a digital canceller. A good performance with 86 dB (>14 bit) conversion accuracy, 95 dB (>15 bit) dynamic range for a low oversampling ratio (OSR=32) and low-accuracy analog components (4-bit internal D/A converter with 6-bit linearity) is achievable.



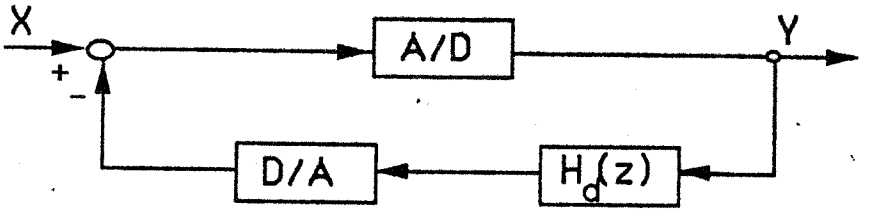
(a) sinusoidal response of a 4-bit flash A/D converter

(b) sinusoidal response of a 1-bit $\Delta\Sigma$ A/D converter

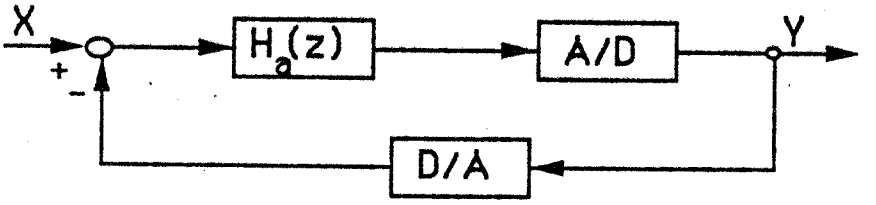


(c) ramp response of a multibit $\Delta\Sigma$ A/D converter

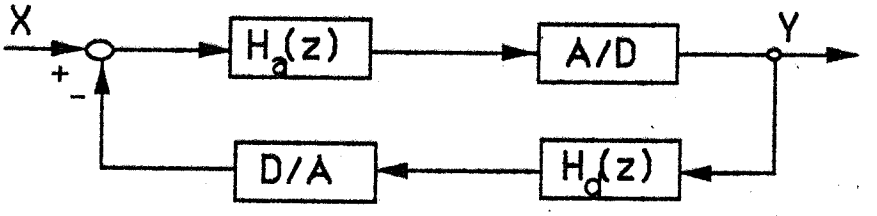
Fig.1 Different output waveform of A/D converters
(a) conventional A/D converter
(b) (c) oversampling A/D converters



(a) predictive type converter
*general linear feedback encoder
*delta modulator

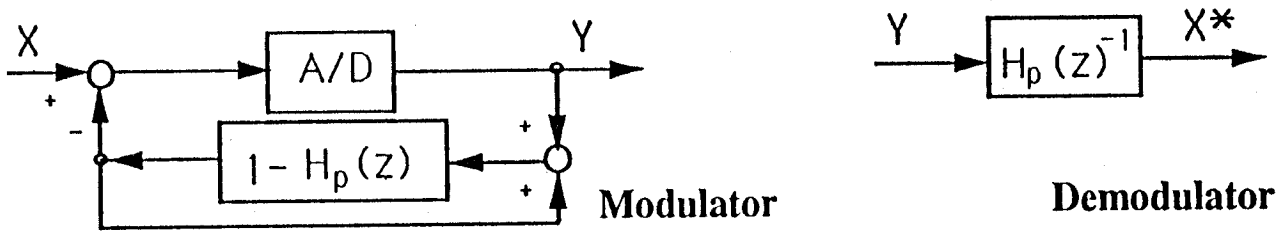


(b) noise-shaping converter
*quantizer error feedback converter
*delta-sigma converter
*noise-shaping converter using N-path filter stage

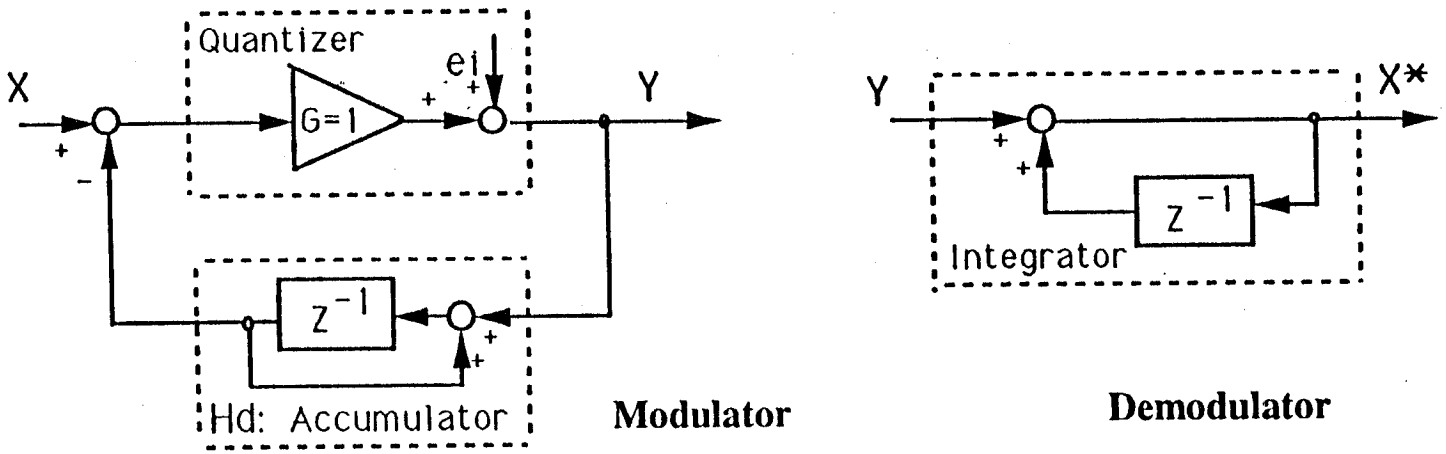


(c) predictive/noise-shaping converter

Fig.2 Block diagram of different kinds of oversampling converters

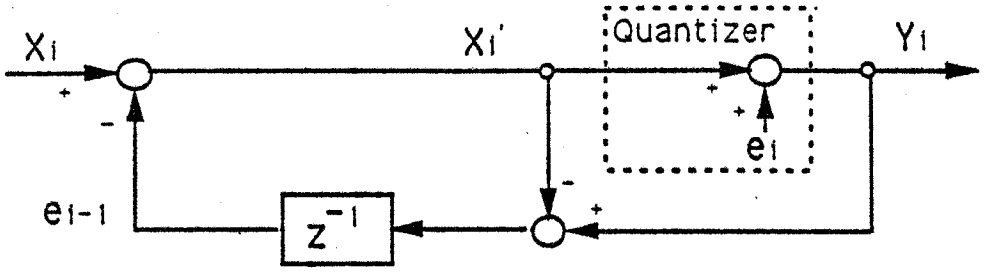


(a) general linear feedback predictive coder

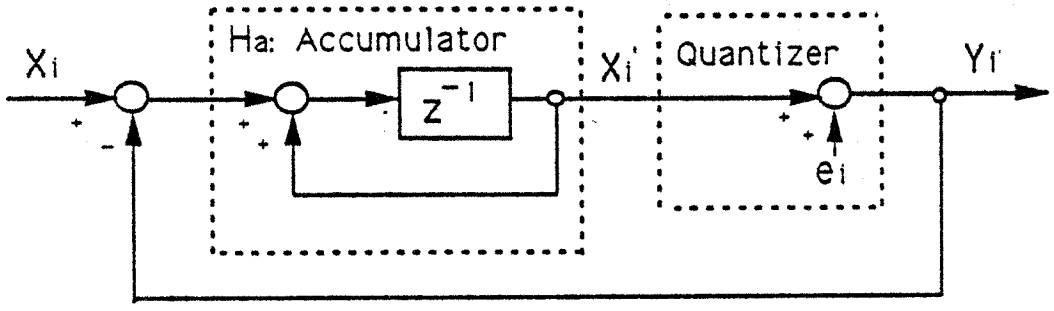


(b) Delta modulator and its demodulator

Fig.3 Predictive converters

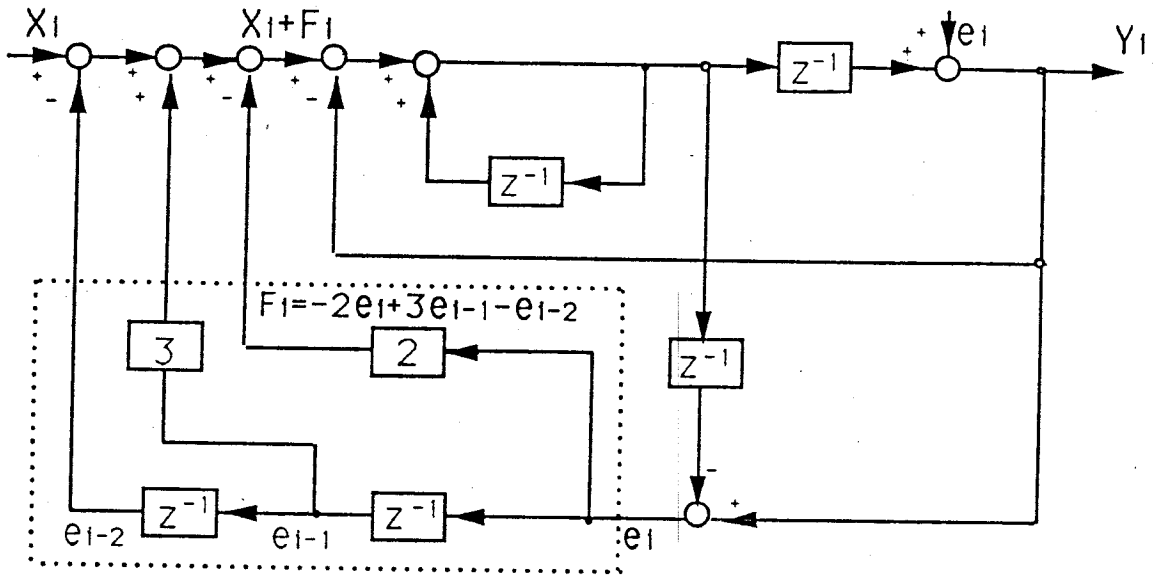


(a) First-order error feedback converter

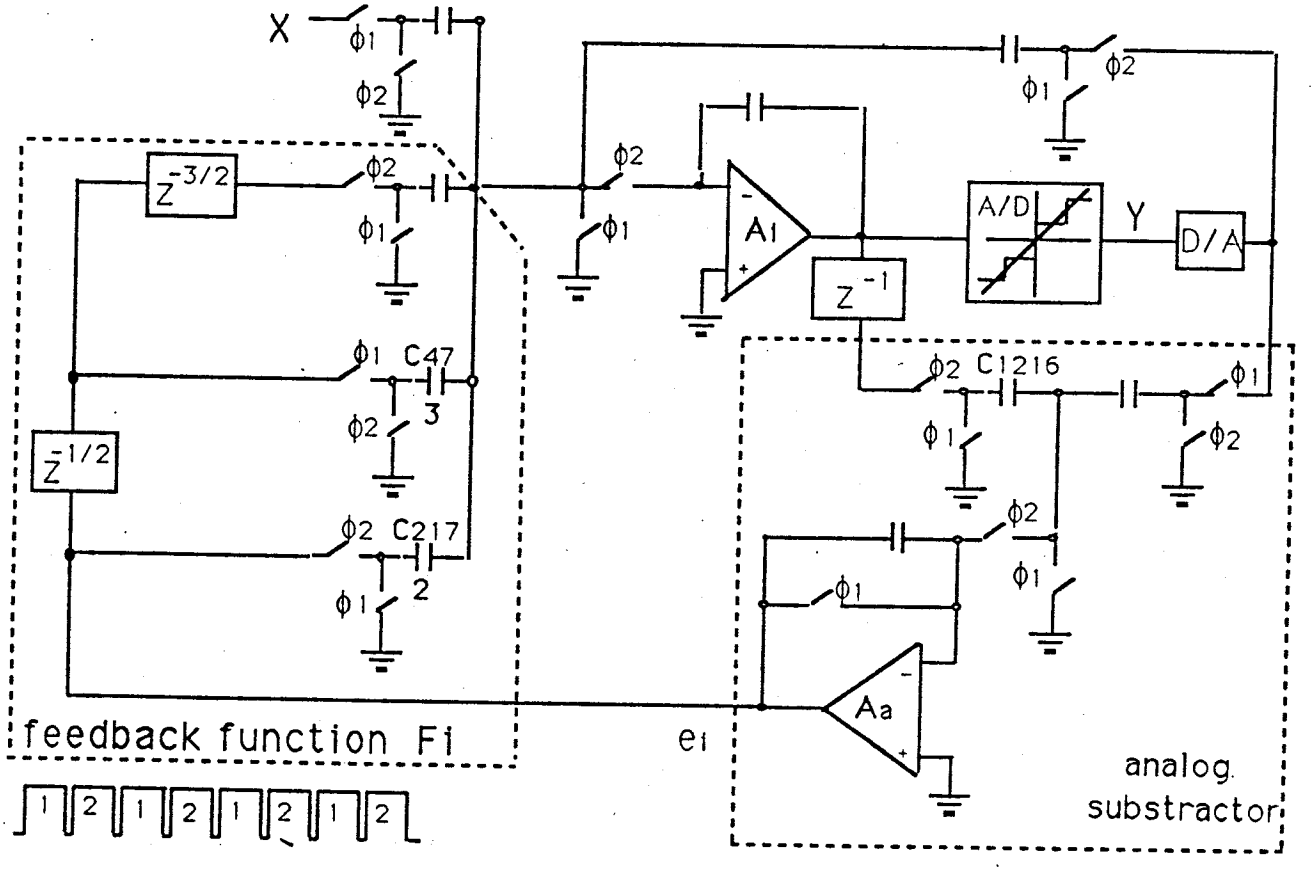


(b) First-order delta-sigma converter

Fig. 4 Noise-shaping A/D converters

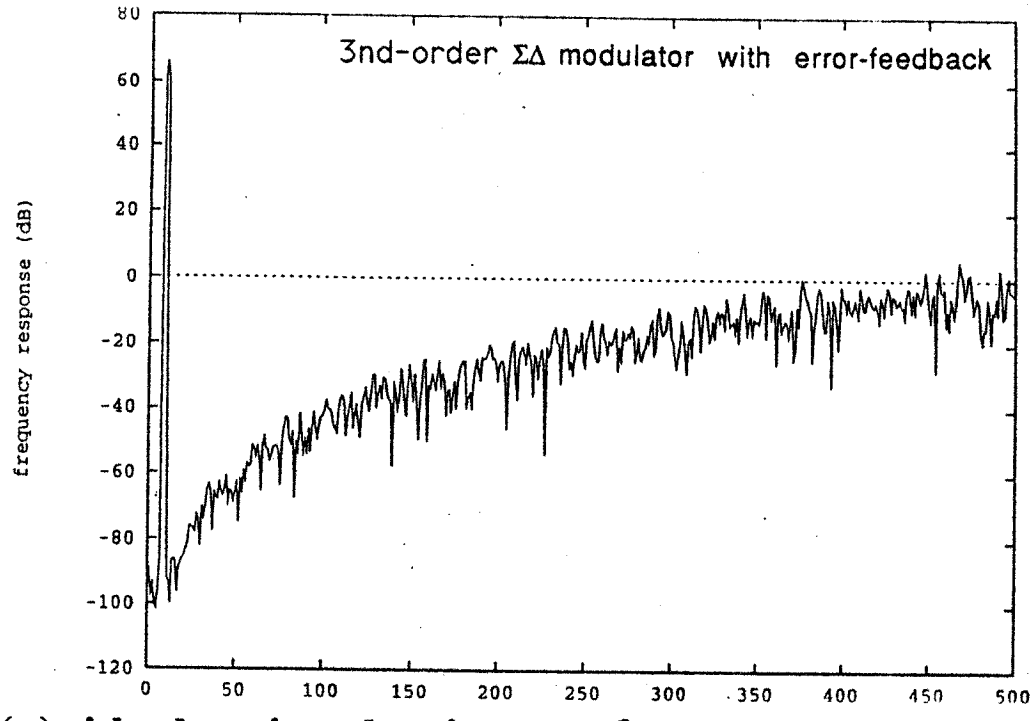


(a) A modified error feedback converter

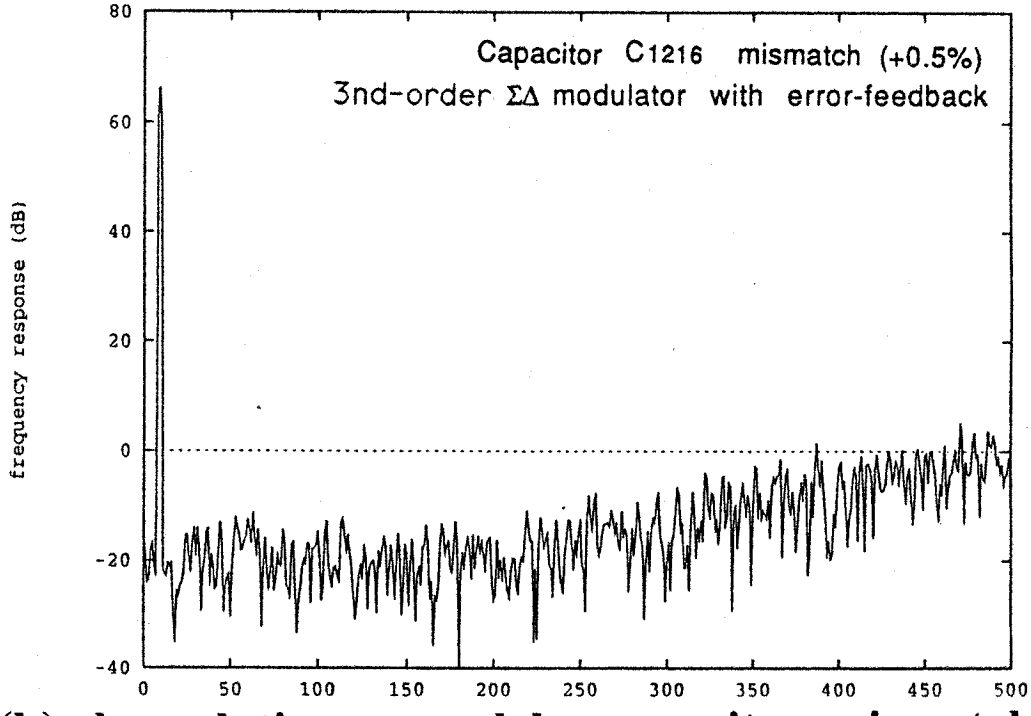


(b) Implemented switched-capacitor circuit of a modified error feedback converter

Fig. 5 Error feedback converters

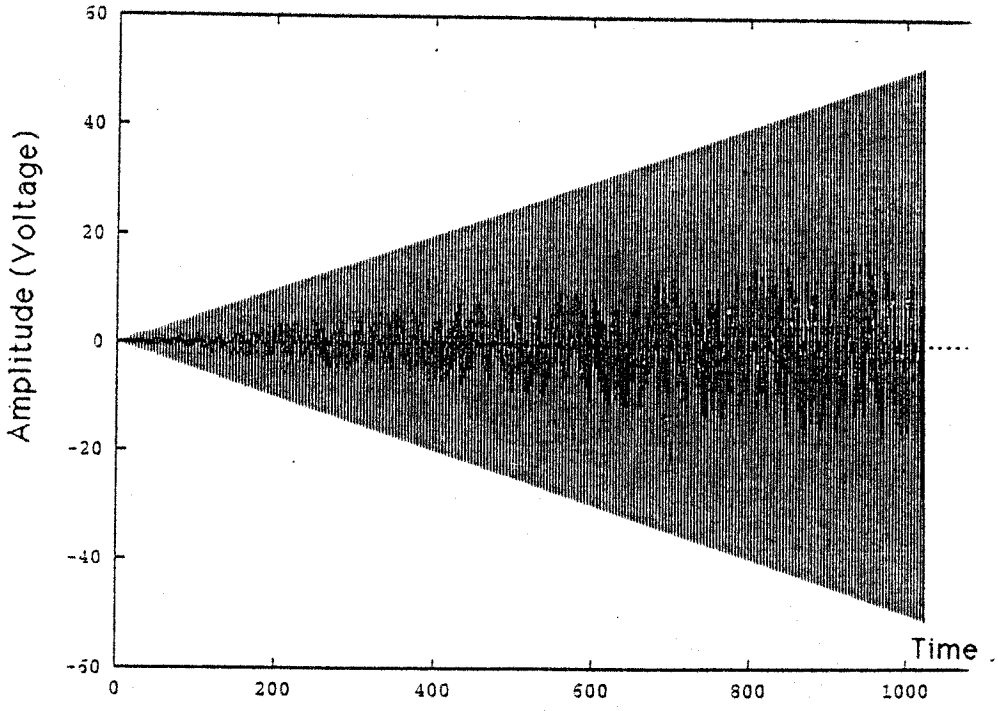


(a) ideal noise-shaping performance

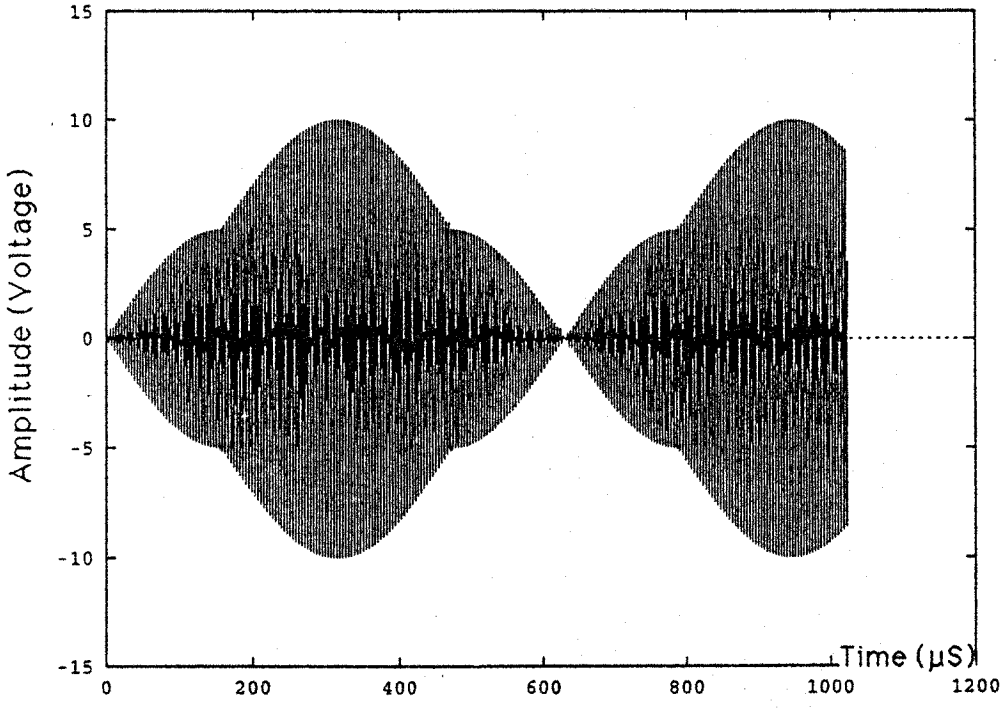


(b) degradation caused by capacitor mismatch

Fig.6 Sensitivity problem of error feedback converter SC circuit is shown in Fig.5 (b).



(a) input signal frequency at band center



(b) input signal frequency away from band center

Fig.7 Accumulator output waveform with sine input

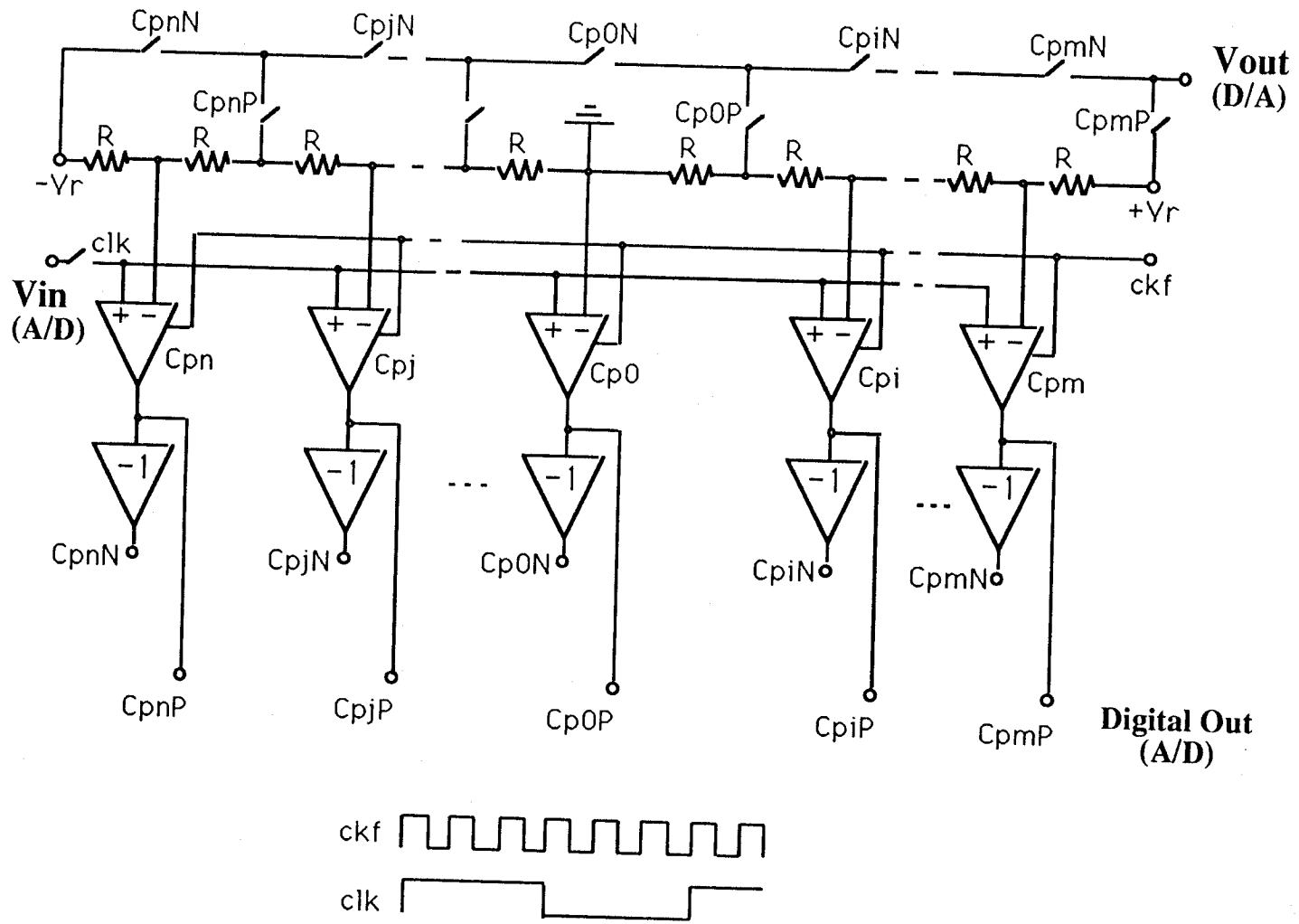
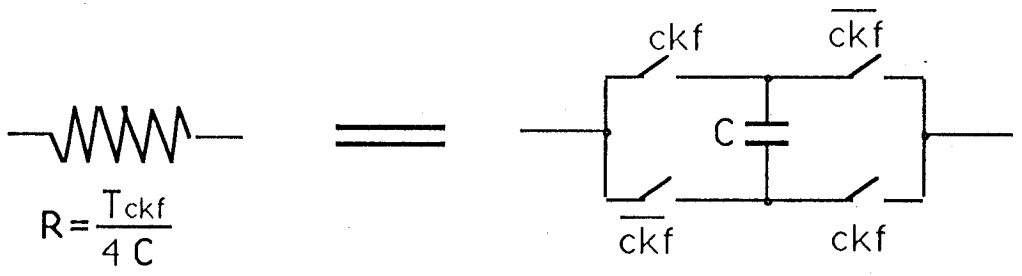
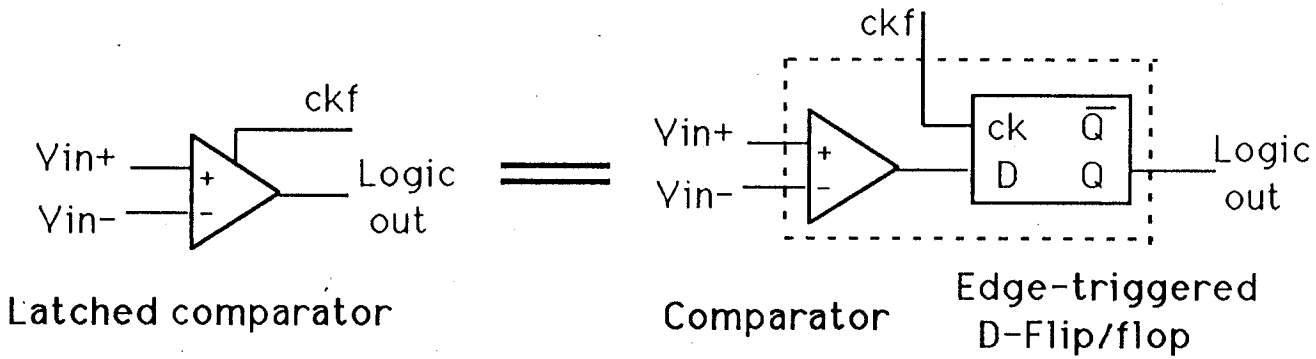


Fig.8 Multibit internal flash A/D converter (with internal D/A converter)



(a) Finite resistance



(b) Equivalent model of a latched comparator

Fig. 9 Some subcircuits used in simulation

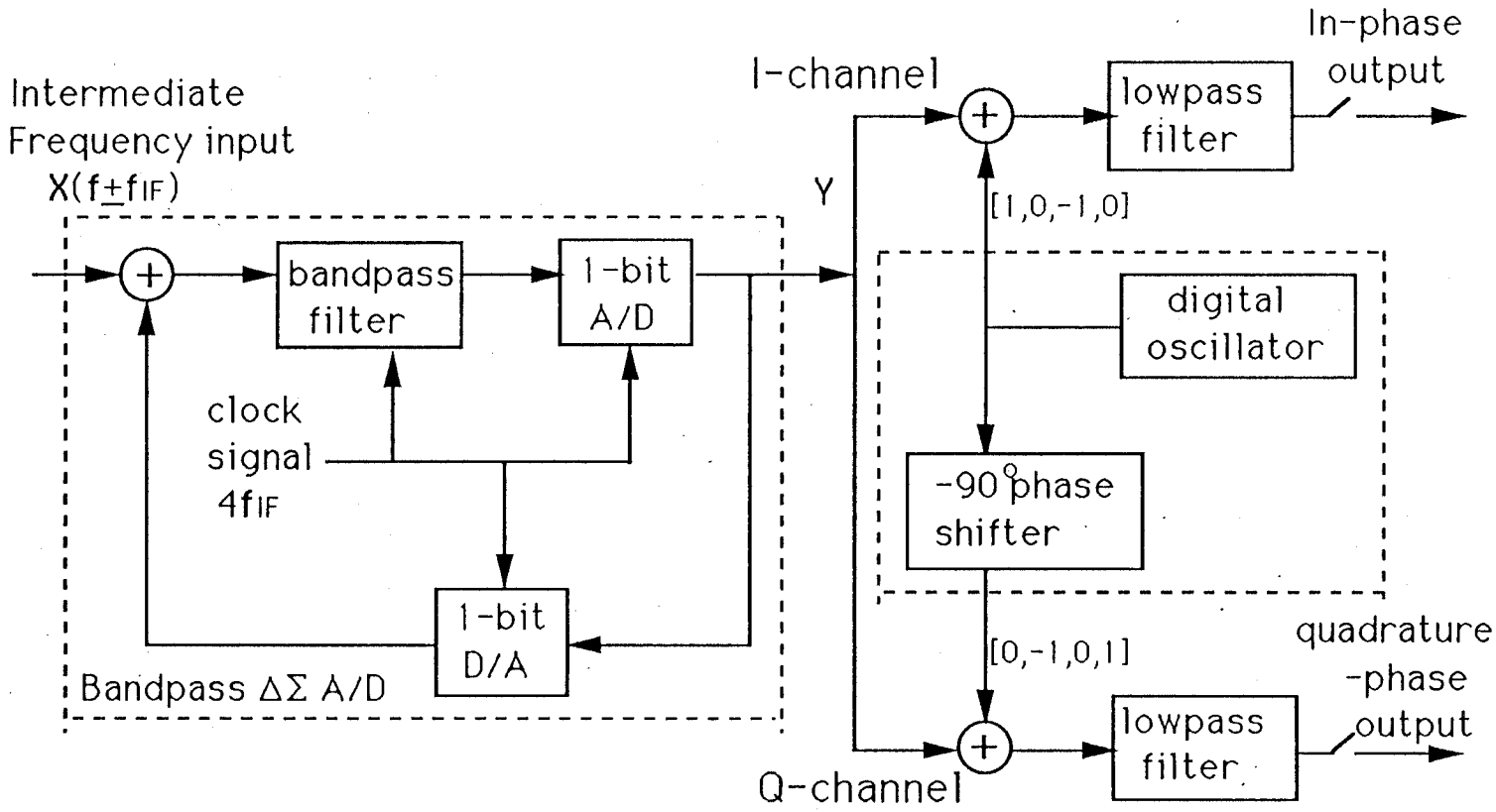
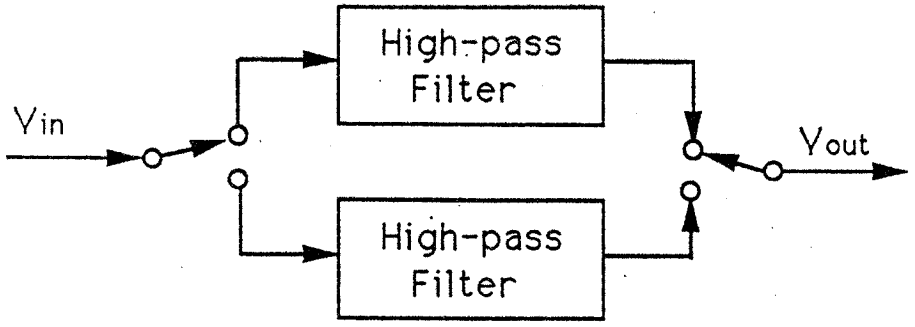
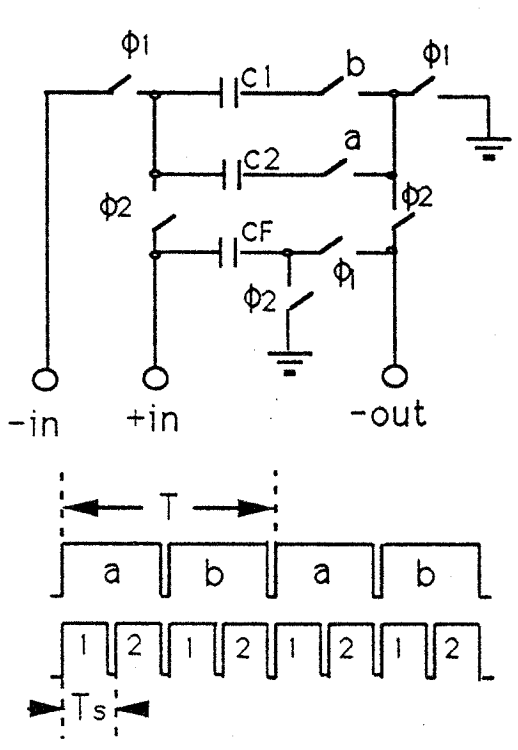


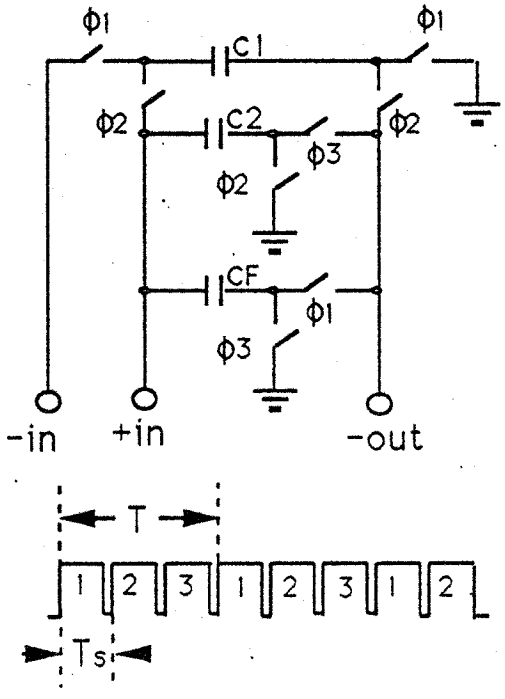
Fig.10 Bandpass delta-sigma A/D system



(a) 2-path filter, the path filters are high-pass filters



(b) RAM-type pseudo-2-path cell



(c) Circulating-delay type pseudo-2-path cell

Fig.11 Pseudo-2-path bandpass cell used in differential SC lossless integrator

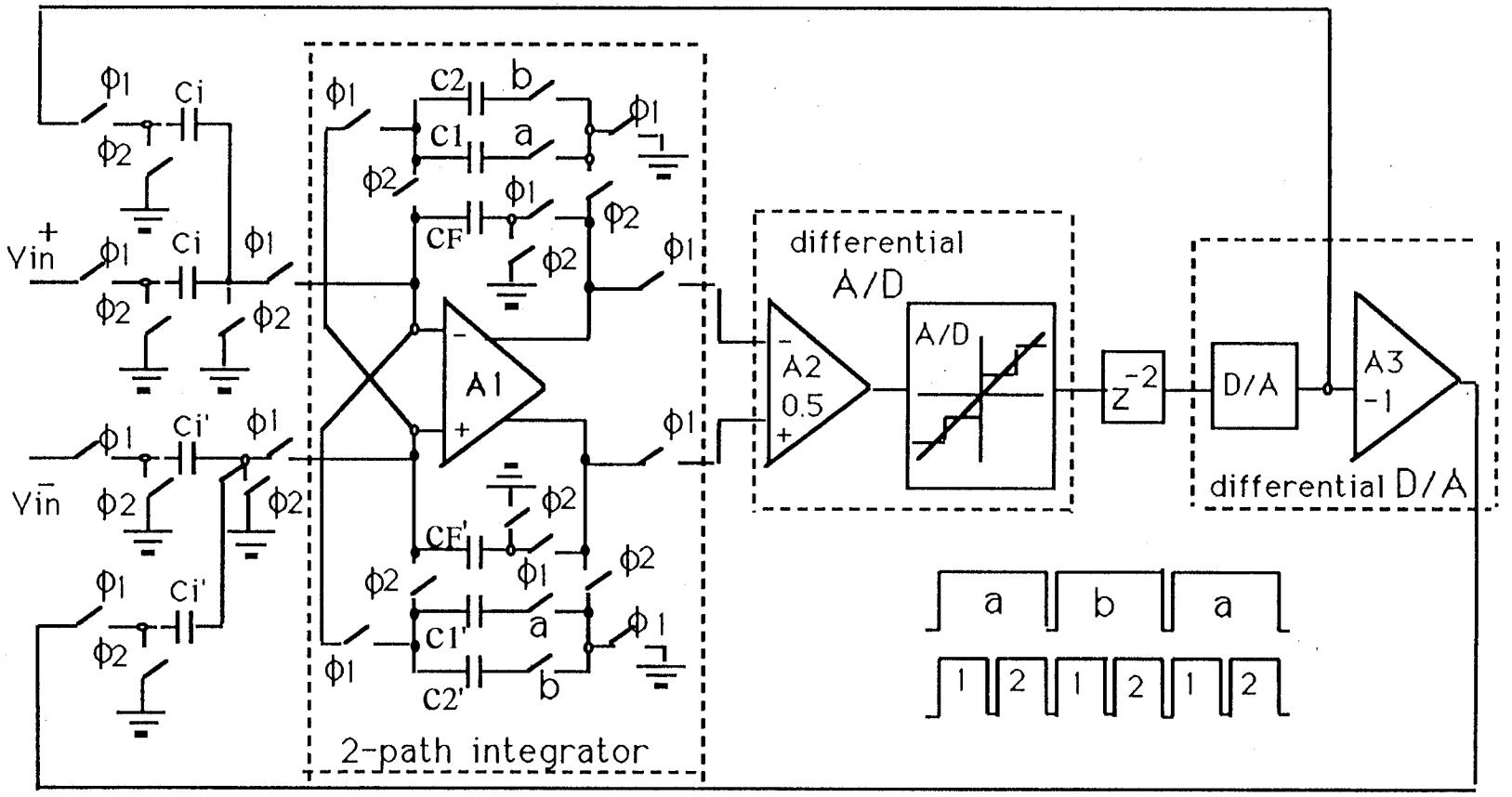
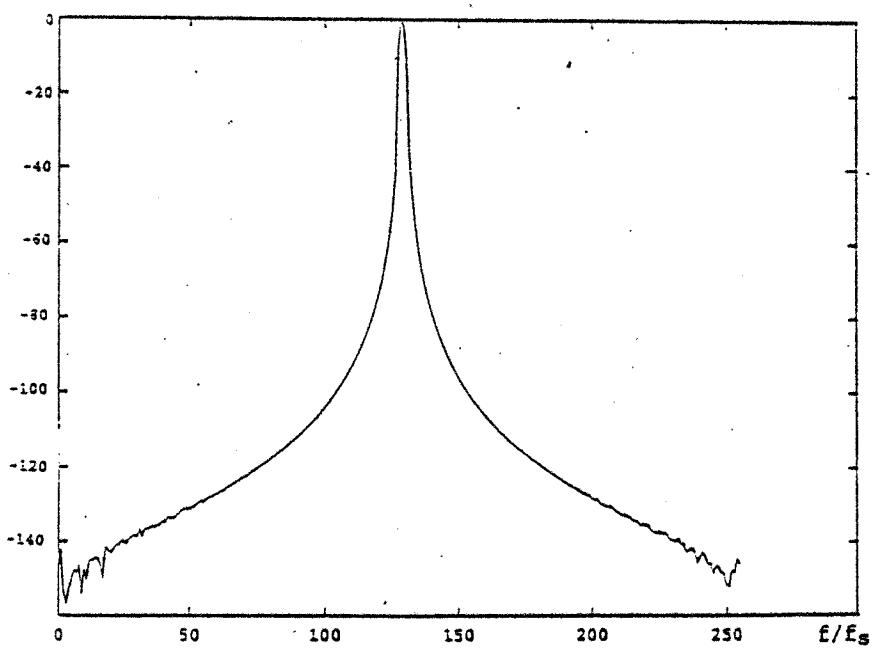
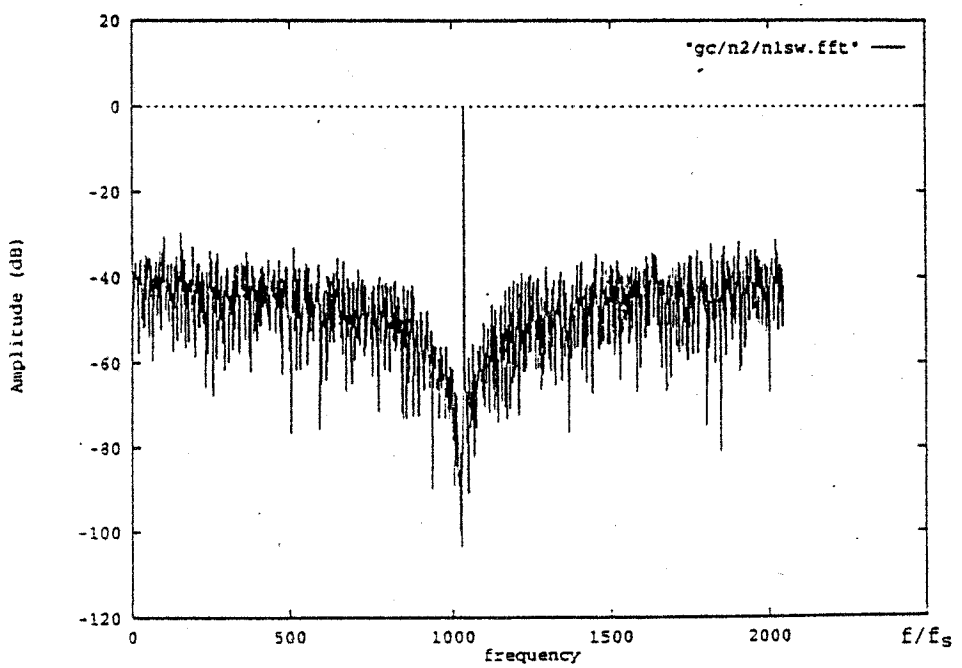


Fig.12 A differential second-order pseudo-2-path bandpass delta sigma converter

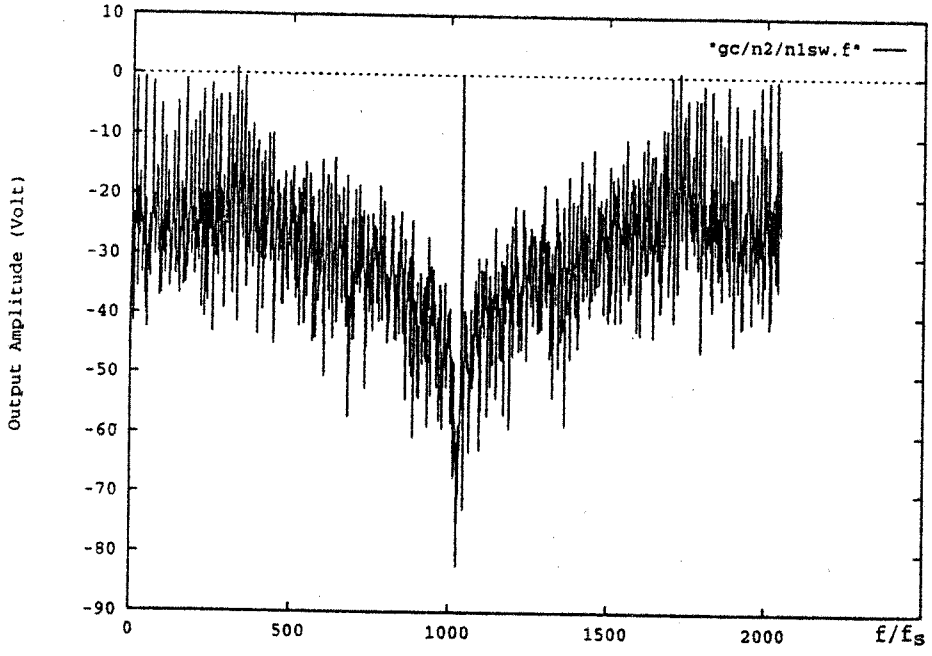


(a) frequency response of the differential 2-path integrator

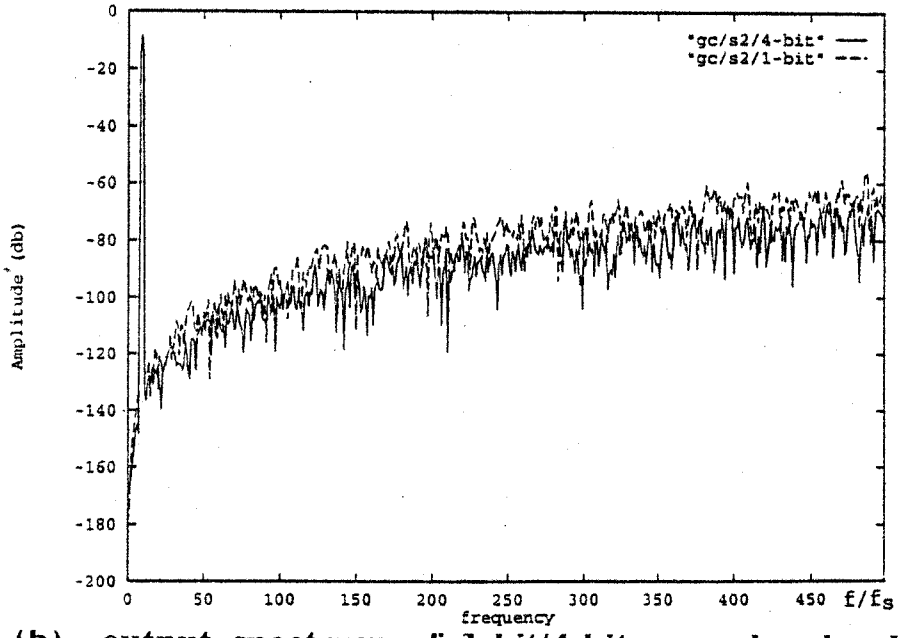


(b) noise-shaping curve of a 4-bit second-order BΣΔ constructed by using the above integrator

Fig. 13 Frequency characteristic of the differential 2-path integrator and the its resulting circuit

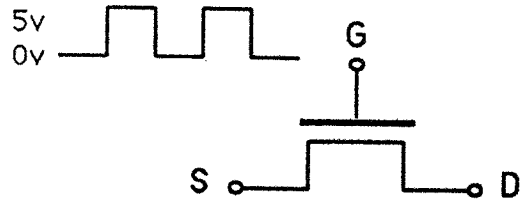


(a) output spectrum of 1-bit second-order BΣΔ constructed by using the integrator of Fig.13 (a)

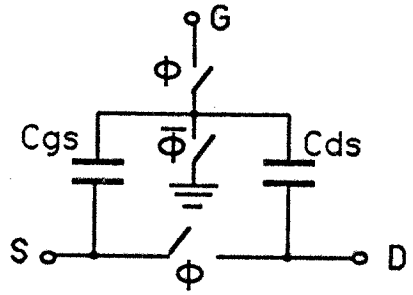


(b) output spectrum of 1-bit/4-bit second-order LΣΔ

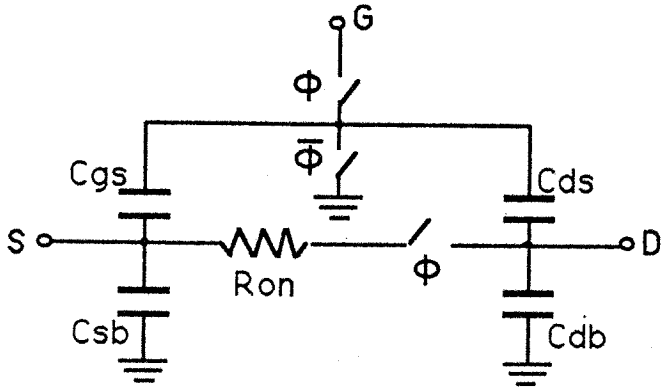
Fig. 14 Multi/Single-bit effects on second-order BΣΔ and LΣΔ



(a) a MOS switch



(b) simplified nonideal switch



(c) complete model of nonideal switch

Fig.15 Model of nonideal switch

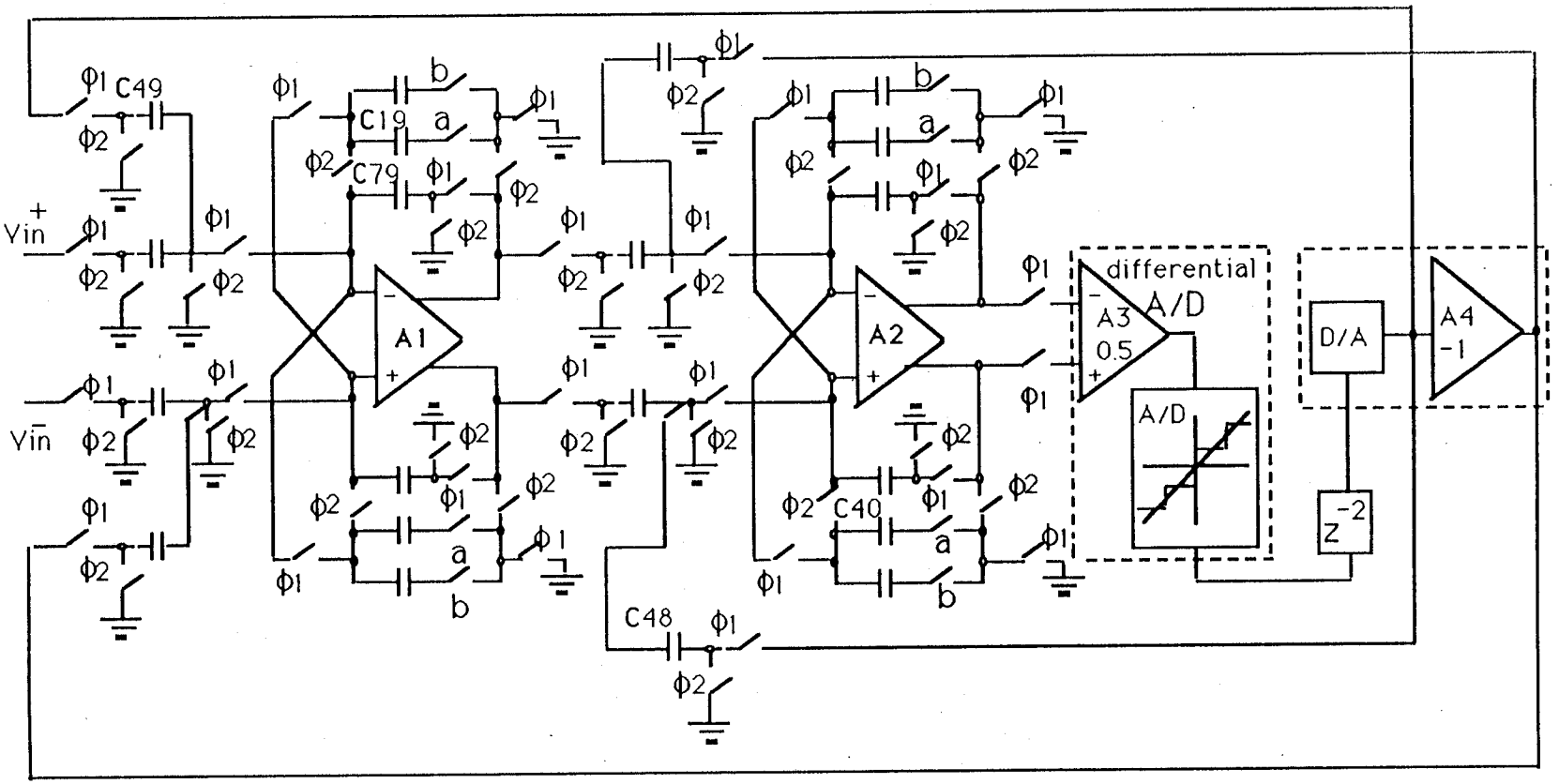
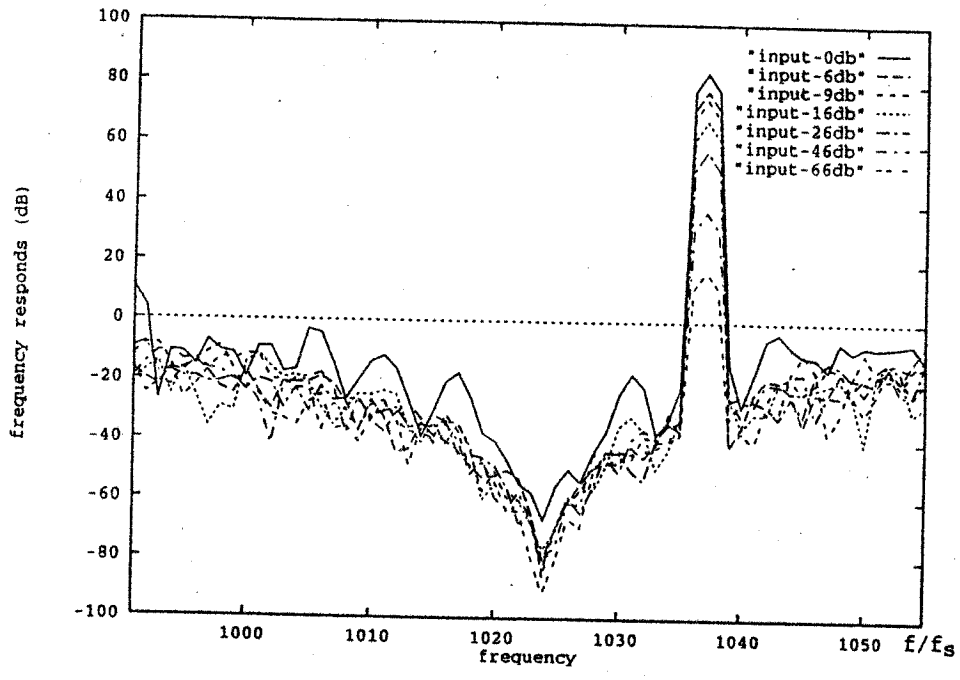
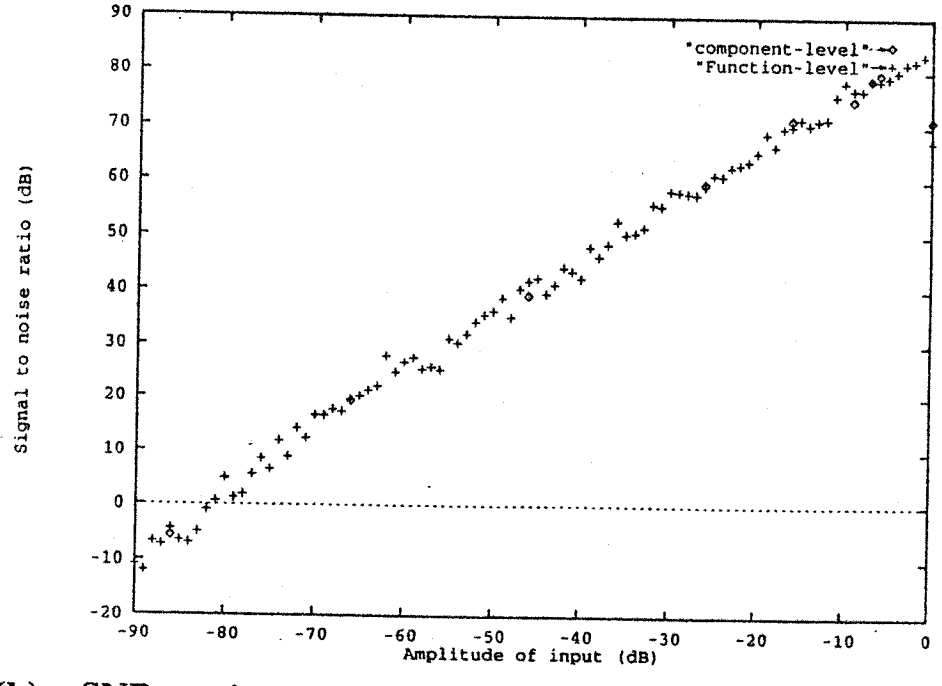


Fig.16 A differential 4th-order pseudo-2-path delta-sigma converter

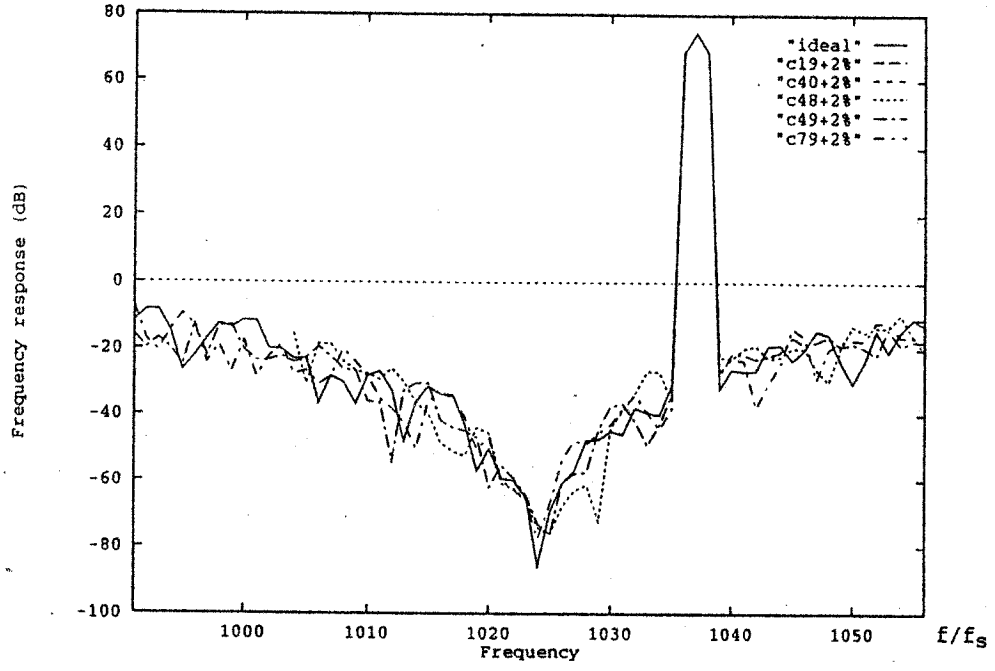


(a) frequency response of 4th-order BΣΔ with different inputs

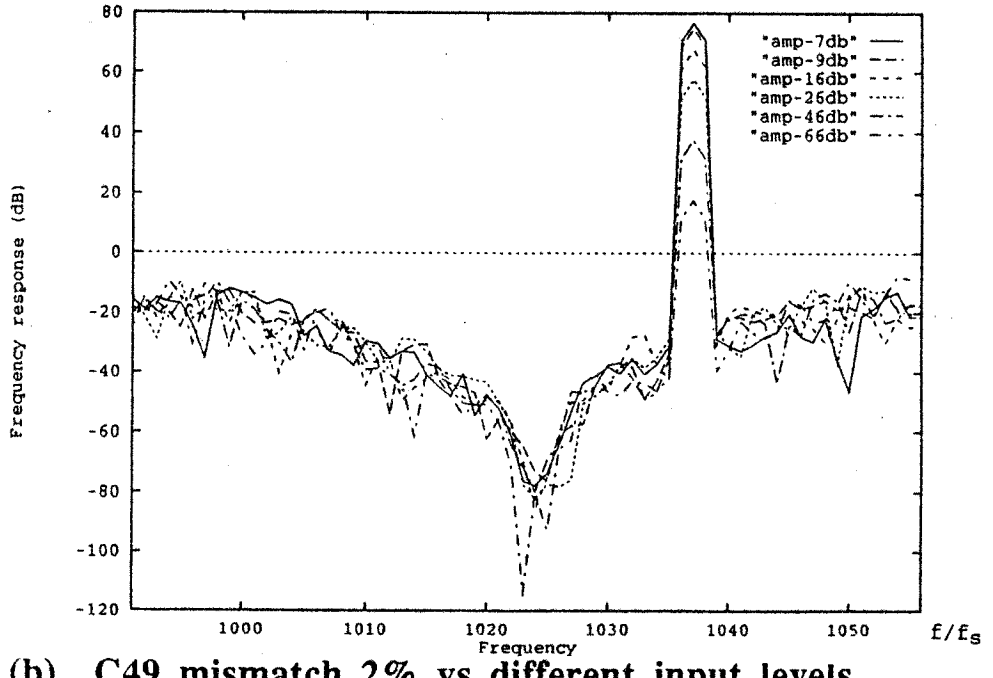


(b) SNR vs input levels (functional and component simulation)

Fig. 17 Effect of input level (ideal circuit)

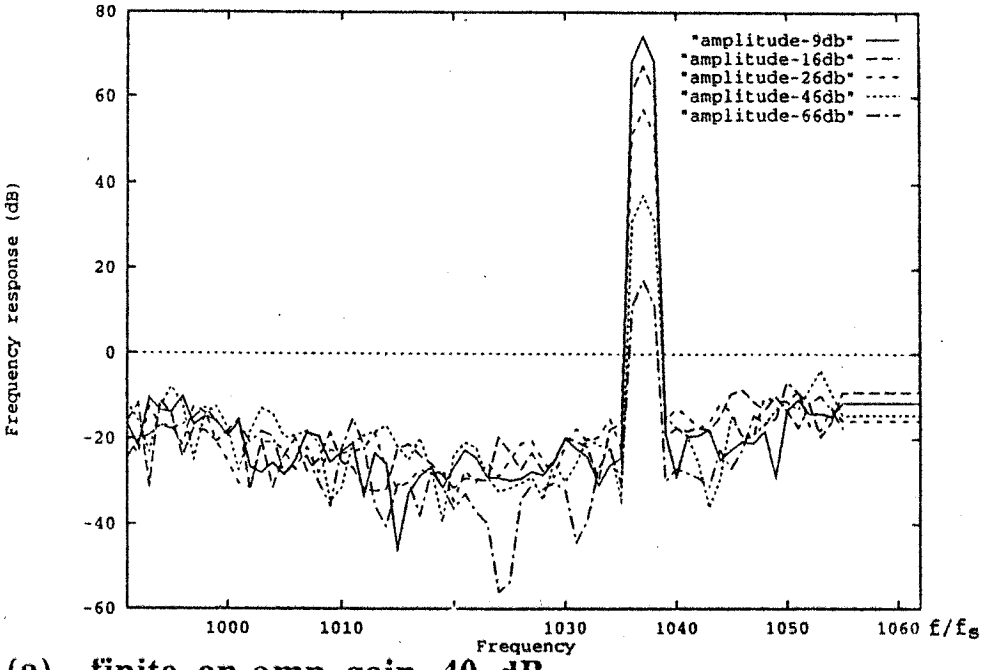


(a) some important capacitors mismatch 2%

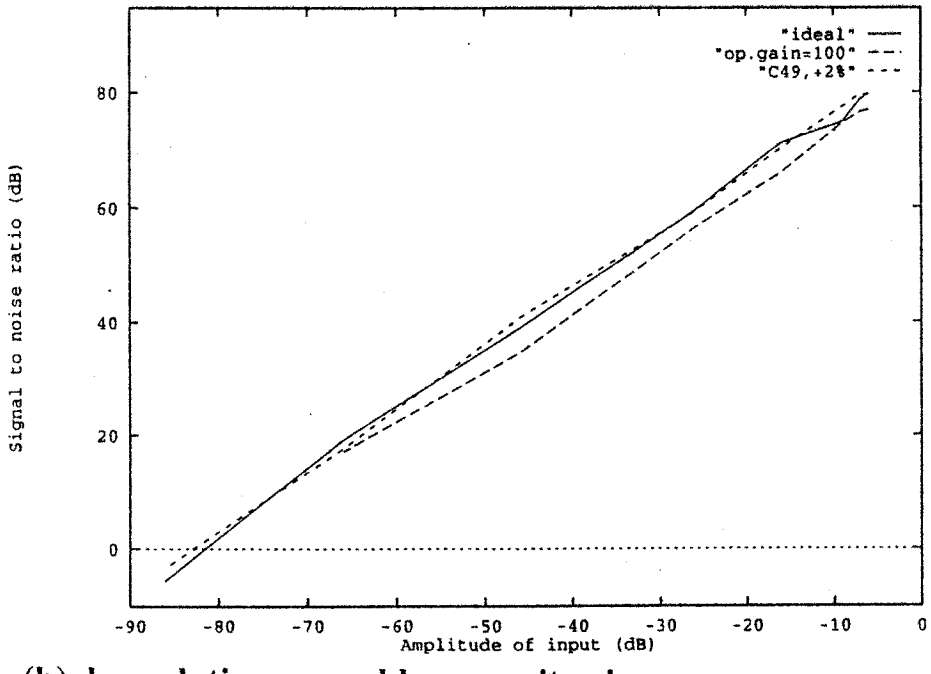


(b) C49 mismatch 2% vs different input levels

Fig.18 Sensitivity of the 4th-order 2-path B$\Delta\Sigma$ to capacitor inaccuracy

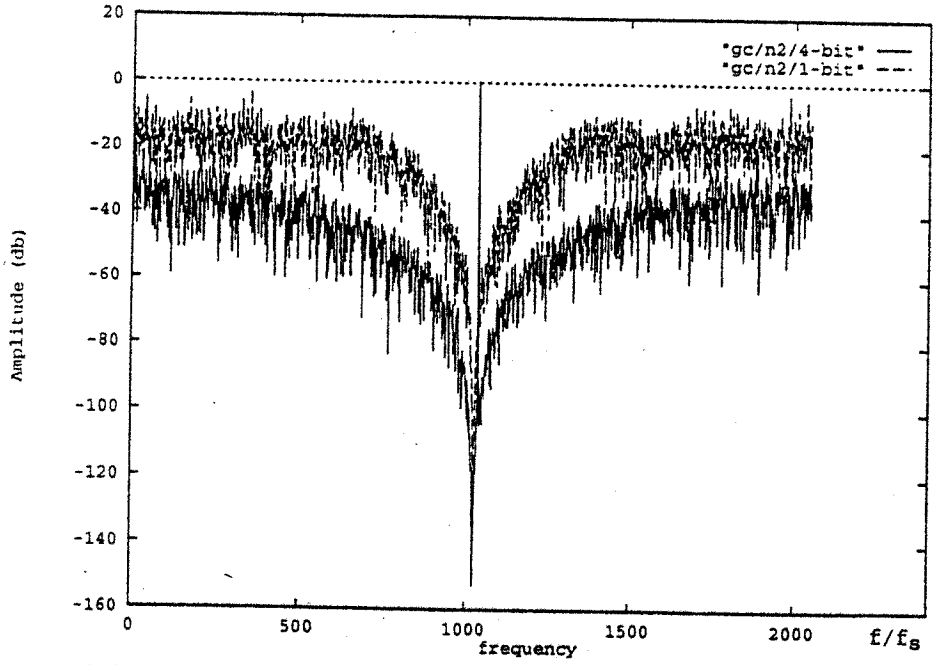


(a) finite op-amp gain=40 dB

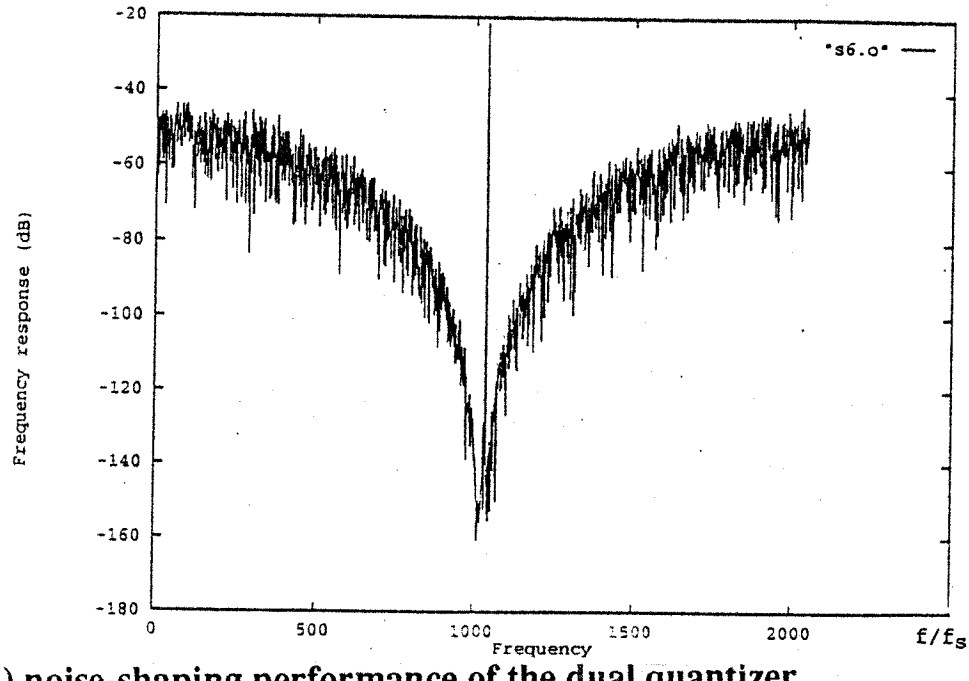


(b) degradation caused by capacitor inaccuracy or finite op-amp DC gain

Fig. 19 4th-order 2-path BΣΔ insensitive to op-amp finite gain



(a) 4-bit/1-bit 4th-order 2-path BΣΔ output spectrum



(b) noise-shaping performance of the dual quantizer 6th-order 2-path BΔΣ

Fig. 20 High order 2-path BΣΔ performance

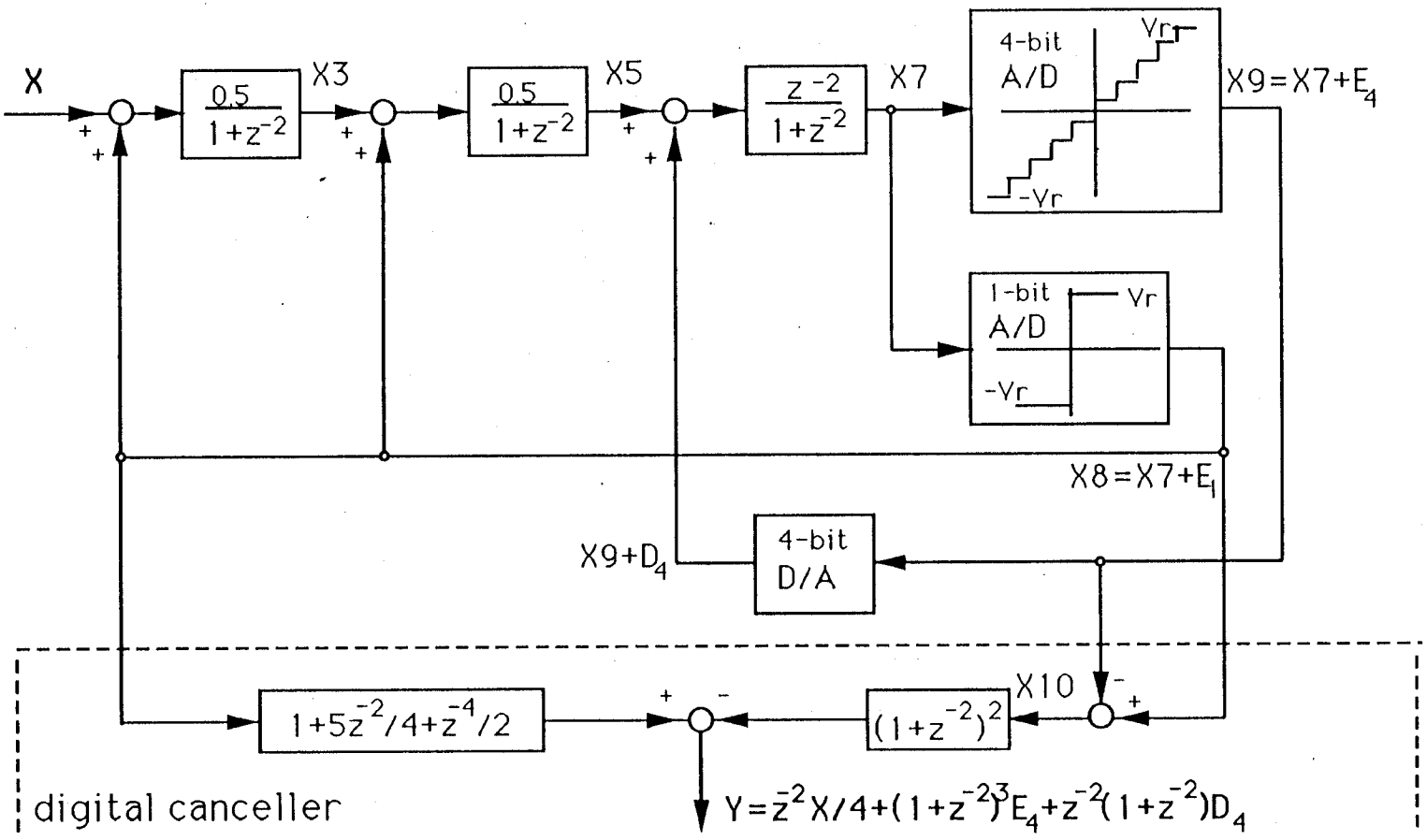


Fig. 21 The block diagram of a dual-quantizer 6th-order 2-path BΔΣ with digital correction

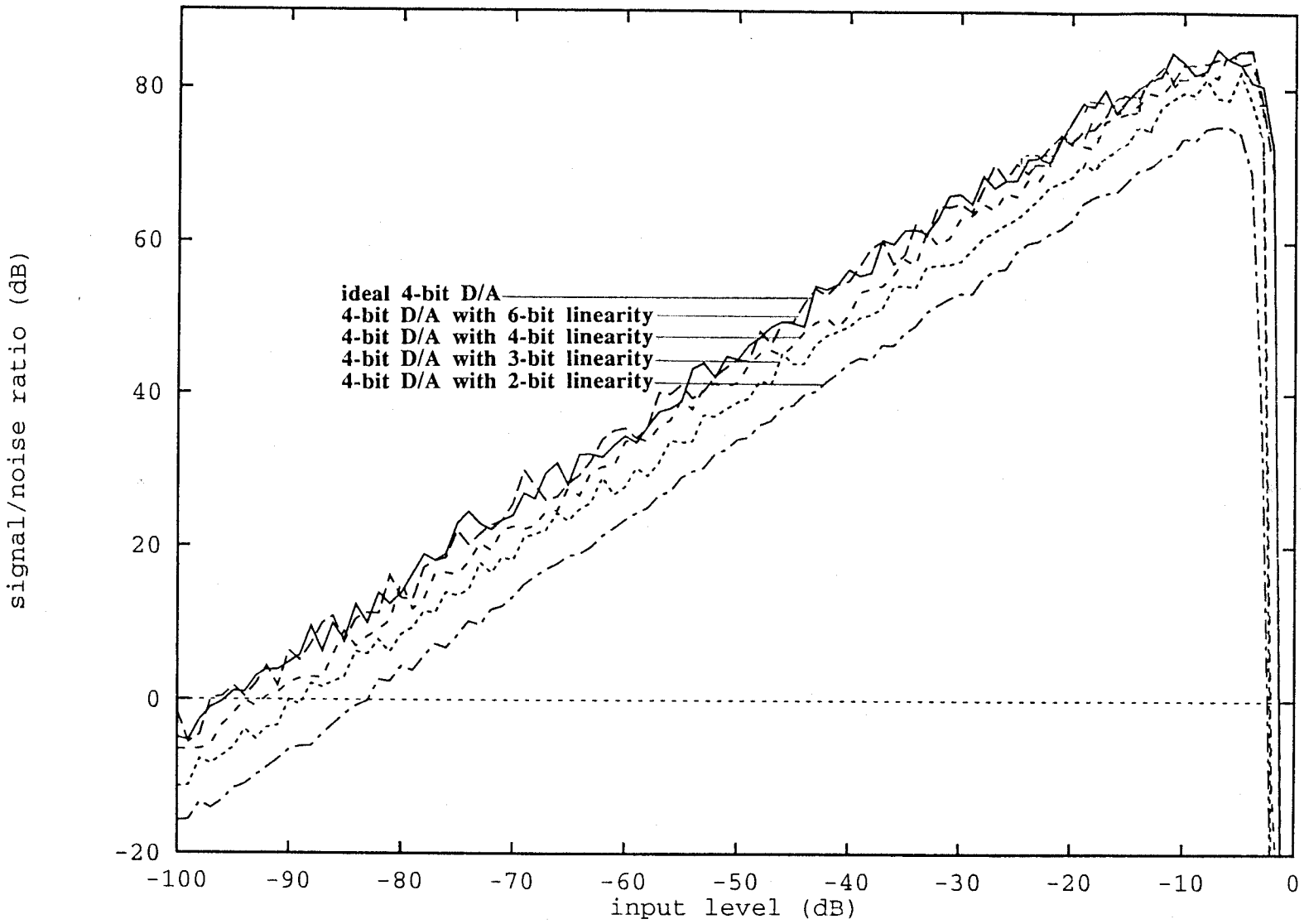


Fig.22 SNR degradation of the dual quantizer 6th-order 2-path BΔΣ with internal D/A nonlinearity

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