AN ABSTRACT OF THE THESIS OF

Charles Grant Myers for the degree of Master of Science in Electrical and Computer Engineering presented on February 4, 2005.

Title:

Design of High-Performance Pipeline Analog-to-Digital Converters in Low–Voltage Processes .

Abstract approved: _____

Un-Ku Moon

Pipeline analog-to-digital converters (ADCs) have long been used in high-speed systems for power-efficient data conversion. Broadband communication and video processing systems are placing high demands on converter accuracy and speed (above 14 bits and in the multiple-MHz range). The increasing converter requirements coupled with lower supply voltages in modern processes makes designing pipeline ADCs to meet these requirements exceedingly difficult.

This thesis addresses the issues associated with designing a pipeline ADC for high accuracy under modern low-voltage process limitations. Fundamental barriers to an economical solution at this accuracy level, such as kT/C thermal noise, are addressed through system and circuit level design. These include such concepts as rail-to-rail inputs for improved signal power and sample-and-hold (S/H) removal for noise and power savings.

The presented concepts are combined in a prototype design implementation using a 0.18μm, 1.8V process. This serves as a platform for addressing issues with integrating the ideas simultaneously. Simulations and modeling presented illustrate the feasibility of such a design.

Design of High-Performance Pipeline Analog-to-Digital Converters in Low–Voltage Processes

by

Charles Grant Myers

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Presented February 4, 2005
Commencement June 2005

Master of Science thesis of Charles Grant Myers presented on February 4, 2005.

APPROVED:

Major Professor, representing Electrical and Computer Engineering

---

Associate Director, School of Electrical Engineering and Computer Science

---

Dean of Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Charles Grant Myers, Author

ACKNOWLEDGMENTS

I owe thanks to many people for my success in completing this thesis. My fellow researchers in the mixed signal research lab have been an invaluable resource for discussion and insight. This is especially true for my good friends Pavan Kumar Hanumolu, Gil-Cho Ahn, and Jose Silva. Thank you for all you input and for bringing me up-to-speed in the convoluted world of data converters. I may have been able to do this on my own, but I have a much greater understanding of this field than I ever could have achieved on my own.

My major professor, Dr. Un-Ku Moon, has been a source of great insight to the world of analog circuit design over the years I have spent at Oregon State University. It has been a pleasure studying under him and I hope to maintain a solid relationship with him as I continue into my work life. Thank you Professor Moon for giving me the opportunity to push myself and for helping me push myself from time to time. :-)

Thanks to my committee for coming together in such a short time. I am honored to have such superior professionals and great people participate in the formal steps of my graduate education. Special thanks goes to Ferne Simendinger in the EECS office who performed heroic deeds on the day of my defense so that I could actually defend.

I would also like to mention the support of couples that have given myself and my wife a great deal of stability and joy through their friendship with us. These are Todd and Jen, Jose and Marcella, and Merrick and Hannah. We hope to remain good friends with you for many years to come.

It has been an enjoyable experience sharing this time in my life with so many people from such diverse backgrounds. I like to think of all of you as my friends, and I wish you good fortune in all that you endeavor.

I would like to thank my family for all their support. My wife Meredith, who has lived the life of a graduate student every bit as much as me. I love you and appreciate all your patience and encouragement. My parents, who are always asking how my research

is going and are always willing to offer up a bit of encouragement. You have enabled me to do many things in my life through your constant assertion that I can do anything. I hope to pass the same encouragement on to my children some day. My wife's parents, who by the way are great in-laws. Thanks for your kindness and for your genuine care you have shown me over this relatively short time we have known each other.

Lastly, I would like to thank God for giving me strength to continue when I was unsure of myself, and giving me peace when I was most unsettled. Thank you for placing me in the midst of such wonderful people. I feel truly blessed.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

Page

TABLE OF CONTENTS (Continued)

Page

LIST OF FIGURES

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF TABLES

DESIGN OF HIGH-PERFORMANCE PIPELINE ANALOG-TO-DIGITAL CONVERTERS IN LOW–VOLTAGE PROCESSES

CHAPTER 1. INTRODUCTION

High-performance applications such as broadband communication systems require high-performance analog-to-digital converters (ADCs) with high-resolution and bandwidth (over 14 bits and several MHz). Such applications are often the domain of pipeline ADCs, due to their highly efficient and conversion-speed-centric architecture. The increasing focus on low-voltage digital processes places great strains on the design of such systems and makes them very costly to implement using current pipeline ADC design techniques. This thesis explores these issues in detail and presents alternative design techniques for economically achieving these performance goals in modern low-voltage processes.

1.1. Motivation

Analog-to-digital converters are important components in applications requiring the interface between analog and digital domains. These are varied and numerous and range from digital radio systems to military and medical sensors to wire-line and wireless communications.

There are a number of different ADC architectures available to accomplish the data conversion task; however, no single architecture is independently suited for all applications. As illustrated in Fig. 1.1, these architectures span a range of intended

resolutions and conversion speeds. Some also have differences in power-consumption and conversion latency and must be chosen to fit the given application.

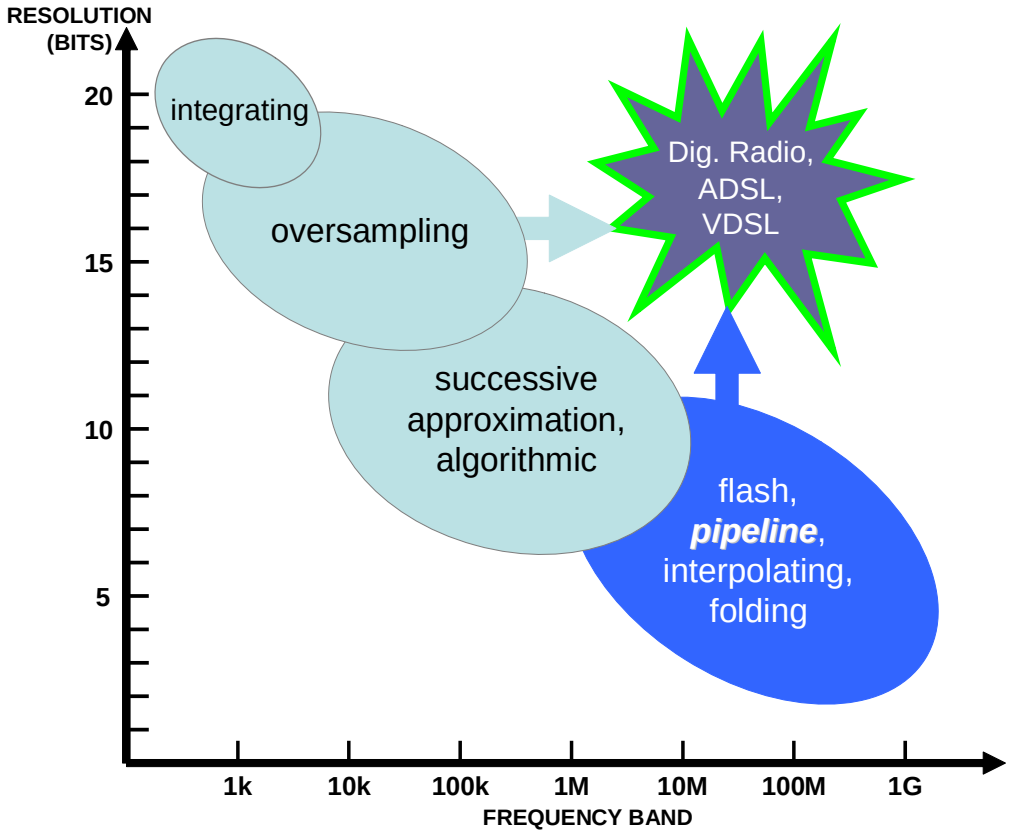

Figure 1.1: Types of analog-to-digital converters

Consumer acceptance and use of digital communication technology coupled with advancements in the technology of wired and wireless communications have increased the demand for high-performance ADCs that must be incorporated in these systems. One example of this trend is the rising speed requirements for DSL systems.

Digital subscriber lines (DSL) target unused bandwidth in current twisted-pair telephone infrastructure. These lines were originally used to carry only low-bandwidth voice data and therefore leave a large portion of the overall bandwidth unused. This unused bandwidth is utilized by DSL for high-speed digital communications. Current

standards for Asymmetric DSL (ADSL) and Very high-speed DSL (VDSL) require ADCs used in these systems to meet conversion requirements of 2.5 MS/s and 24 MS/s respectively with resolutions on the order of 13 to 14 bits [1]. These requirements will only increase as the technology matures and as consumers demand more bandwidth for applications such as video streaming.

The requirements imposed by this application (and many others) have spawned research in two major areas, represented by the arrows in Fig. 1.1.

- One research direction concerns itself with the improvement of Nyquist-rate ADCs. Pipeline ADCs are currently the most researched of these type of ADCs. Their architecture is most suited for medium resolution and high speed, and therefore requires accuracy improvements to meet the stringent digital communication system requirements. Recent work in current analog processes has shown *effective* resolutions of 12 bits [2, 3, 4, 5], while previous designs in older analog processes have shown effective resolutions of 13 bits [6, 7].

- The other research direction concerns itself with the improvement of oversampling $\Delta\Sigma$ ADCs. These ADCs are often utilized for high to very-high resolution and low to medium speed. The high resolution is achieved by oversampling, which trades bandwidth for resolution by averaging multiple samples. Further improvement can be attained by use of z-domain functions aimed at shaping the noise of the $\Delta\Sigma$ ADC. Recent work done in this area focuses on improving the speed of these ADCs [8, 9, 10].

This thesis covers the first research direction listed and includes other important considerations for designing in today's modern semiconductor processes.

At the same time as communications applications are seeing increased system performance requirements, digital CMOS processes are following a trend of reduced supply voltages. This is motivated by speed improvements and area savings achievable with smaller device dimensions [11]. For many analog applications, a lower supply voltage

is a crippling design limitation – this is especially true for ADC designs whose accuracy directly depends on the power of the input signal. Many new processes are developed with processing options that allow the use of high-voltage analog devices, but these make the cost of manufacturing mixed-signal and SOC (System on Chip) microchips much more expensive.

The challenge from this design perspective is to achieve high accuracy in an ADC using modern low-voltage digital transistors. This thesis focuses on improving the accuracy of pipeline ADCs while mitigating manufacturing costs as much as possible.

1.2. Contributions

There are two main design concepts presented in this thesis. The first is based on published work by Ian Mehr [12] and work by Dong-Young Chang [13]. The second is based on low-voltage ADC design concepts developed by Jipeng Li while he was a Ph.D. student at Oregon State University. The design concepts are:

- Removal of sample-and-hold (S/H): The removal of this key block provides significant noise and power savings for pipeline ADCs; however, it places extra strain on the first stage of a pipeline ADC. This stage now must take care of the sampling function and must do so on two independent signal paths.

- Rail-to-rail input: Signal power is greatly increased by allowing a rail-to-rail input. The active pipeline stages cannot drive this level at their outputs and therefore the inter-pipeline stage residue signal amplitude must be reduced. This is compensated for with system design changes that may introduce a gain error in the pipeline ADC. A calibration scheme is developed to combat this error source.

Other contributions of this work include discussion on multi-bit stage optimization, stage scaling, and high-gain, wide-swing opamp design. The overall contributions culmi-

nate in the presentation of a design strategy for achieving high performance in pipeline ADCs suitable for today's and tomorrow's high-bandwidth communication technologies.

1.3. Thesis Organization

Following this introduction, Chapter 2 presents necessary background in the field of pipeline ADCs. Items discussed are basic pipeline ADC operation, the widely used X.5 digital correction architecture, error sources, calibration techniques, and other commonly used techniques for improvement of pipeline ADCs.

System design concepts for reaching the high-bandwidth communications goals are presented in Chapter 3. The two major thesis contributions are first presented here. Also included in this chapter is a discussion on power optimization in pipeline ADCs.

Chapter 4 covers circuit implementation of the system described in the previous chapter. This includes opamp design, system linearity and analog path matching considerations, comparator design, digital MUX design (for calibration scheme), and layout issues.

The thesis is concluded in Chapter 5 with a summary of this work's contributions and discussion on future research directions in this area.

CHAPTER 2. LITERATURE REVIEW

Pipeline analog-to-digital converters have been extensively used in high-speed medium-accuracy systems due to their partitioned nature. The accuracy partitioning of pipeline ADCs significantly reduces the power and area requirements of a given ADC design, thus allowing designers to push pipeline ADCs to very high speeds.

This chapter will cover pipeline ADCs in their most common implementations, as well as established circuit and system design practices for improving the performance of a pipeline ADC. There will also be some discussion on pipeline ADC error sources.

2.1. Basic A/D Concepts

The basics of the analog-to-digital conversion should be covered before any attempts are made to discuss Pipeline ADCs in detail. The major function of any ADC is to convert a continuous-time, continuous-value signal into a discrete-time, discrete-value signal. This implies quantization in both the time and signal-level (or "value") domains, where value is most often voltage. These two quantization steps are functionally independent, but in some cases they are combined into a single step.

The first step is time-quantization, also known as *sampling*. A simple example of this function in circuit form is shown in Fig. 2.1. In this example, while the switch is closed, the voltage on the sampling capacitor closely matches the input voltage. When the switch is opened at $t = t_0$, the value of the input signal at the switching instant t_0 is held on the sampling capacitor.

The next step in A/D conversion is signal-level-quantization, and is often given the general name *quantization*. There are many different methods of accomplishing this task, but they can all be reduced to two basic implementations: serial and parallel.

Serial quantization requires some kind of feedback system to identify what the previously resolved bit was, but parallel converts the signal all at once and does not need any information feedback. The parallel implementation is the basis of the *Flash ADC*.

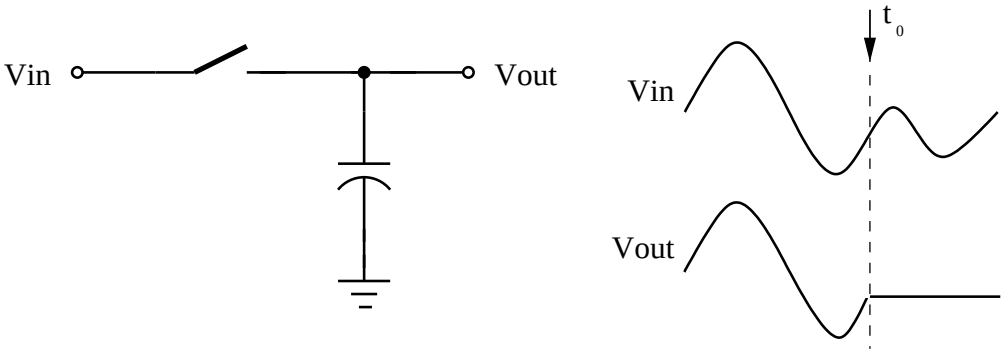

Figure 2.1: Sampling in A/D Systems

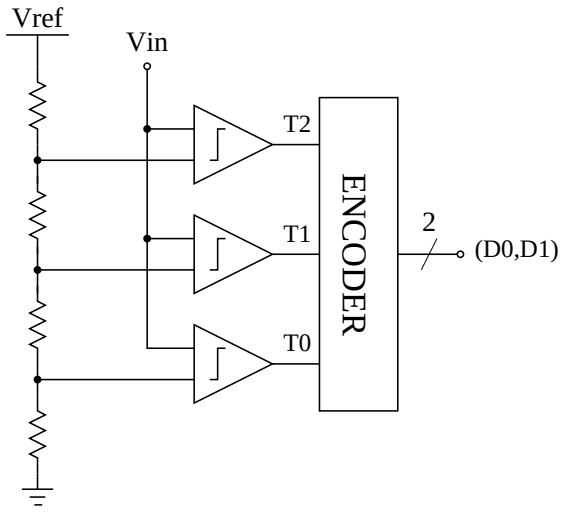

Figure 2.2: Simple Flash ADC Example

The Flash ADC compares the input with the analog equivalents of all possible digital levels in parallel. In other words all level comparisons occur at the same time. A simple example of a flash comparator (without the sampling function) is shown in Fig. 2.2. The output of this converter is a digital word that *approximates* the input signal

with respect to an analog reference voltage (V_{REF}). An early example of the use of this concept can be found in [14].

Note that there is an intermediate digital signal (T0, T1, T2) that appears in Fig. 2.2, this signal is a *Thermometer Code* signal. Thermometer Code is defined as a grouping of bits (like binary code) where the total number of ones increases for each increase of one in value. The ones "fill up" like a thermometer where the value is determined by the location of the boundary between the ones and zeros. For example the value '3' represented in an 8-bit thermometer code is '00000111'.

A common measurement reference in data-converter design is known as *LSB (or Least-Significant Bit)*. This is defined as converter full-scale divided by the total number of levels converted. For example, if a flash A/D converter is designed for a 0V-1V input range and converts 4 bits, 1 LSB is equal to (1/16)V. Many specifications in data-converter designs are given in LSBs.

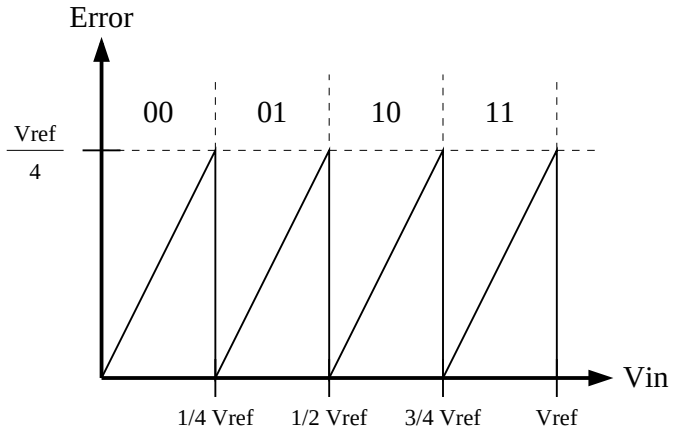

Figure 2.3: Flash ADC Quantization Error

The quantization step introduces an error in the final value of the signal known as *quantization error* and can be shown to have an input/output relationship as is shown in Fig. 2.3. It is easy to show that the quantization error can be reduced by increasing the accuracy of the data conversion; however, for a Flash ADC this can be quite costly.

For each one-bit increase in ADC resolution, the number of comparisons required goes up by a factor of two.

A closer look at the quantization error reveals that the signal is still present in the error. If the quantization error of the conversion can be extracted and amplified, it would be possible to repeat the conversion step to resolve more bits. This structure is known as a Two-Step ADC [15] and is often used to increase the resolution of high-speed Flash ADC designs.

The quantization error can be generated by subtracting the analog-equivalent of the resolved digital bits from the original input signal. This signal is known as the *residue* of the first conversion. An amplification block is then used to make the maximum possible residue value equal to the analog reference voltage (Fig. 2.4). The digital-to-analog conversion, subtraction and multiplication are often combined into one functional circuit block known as the MDAC (Multiplying-Digital-to-Analog Converter).

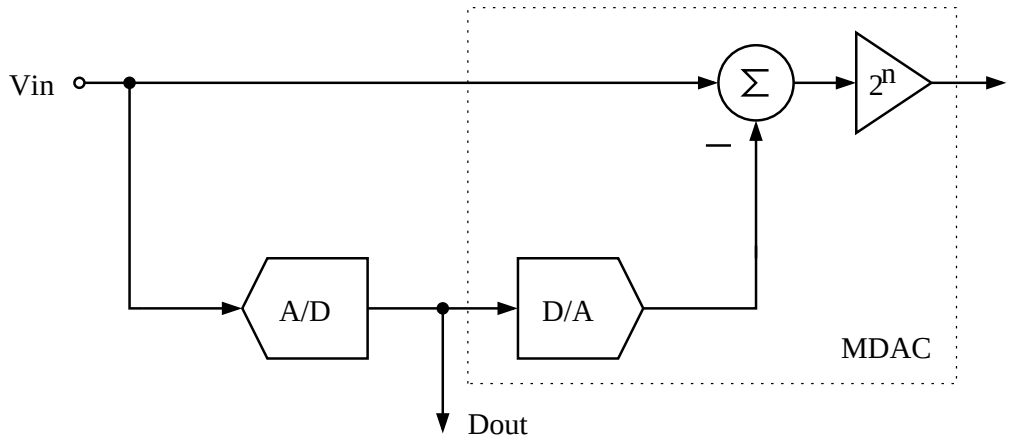

Figure 2.4: Flash Residue Generation

The MDAC is most commonly implemented in the charge domain with a switched-capacitor topology. One example of this is shown in Fig. 2.5. During the *sampling phase*, the input charges the input capacitor (parallel combination of ΣC_{DAC} and C_F) and is sampled at the end of the sampling phase. Next, during the *amplification phase*

the DAC capacitors are individually connected to reference voltages and a capacitive feedback system forces charge onto the feedback capacitor (C_F).

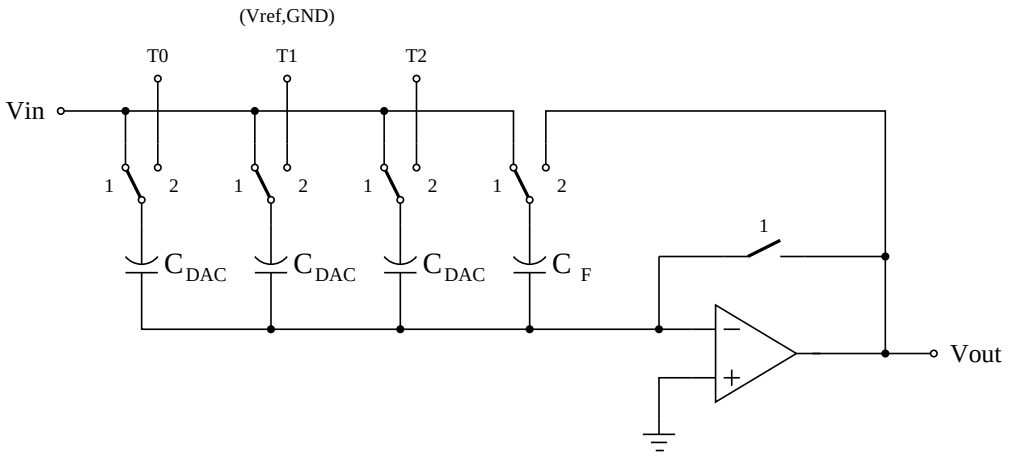

Figure 2.5: MDAC Circuit Implementation

The number of C_{DAC} capacitors connected to the high reference voltage depends on the digital value converted by the quantization in the current stage – this is the subtraction function shown in Fig. 2.4. The gain portion of the MDAC block is achieved with the feedback system. While the total charge moved onto C_F is equal to the difference between the the input and the analog value of the digitally-converted input, the voltage gain is equal to $(\Sigma C_{DAC} + C_F)/C_F$. This can easily be calculated via the capacitor charge equation $Q = CV$.

2.2. Pipeline ADC

The Two-Step ADC can be further extended by adding additional MDAC and comparator stages – this creates the basis for the *pipelined* ADC. In fact, the system shown in Fig. 2.4 is a simple representation of a Pipeline ADC stage. This stage is repeated until the number of bits required can be resolved from the pipeline (Fig. 2.6). Most text books covering data converters discuss the pipelined ADC including [16]. Note

that a S/H stage is required at the front-end to make the first stage's conversion task simpler.

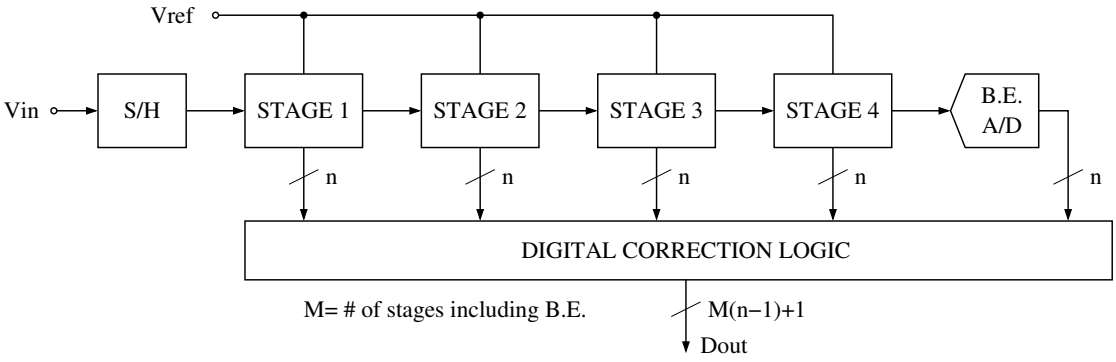

Figure 2.6: Pipeline ADC

2.2.1. Per-Stage Resolution

The pipelined ADC architecture allows a designer flexibility in the choice of quantizer (or *subADC*) resolutions for each stage. As such, the most common implementation of the Pipeline ADC is a 1.5 bits-per-stage structure. (The partial-bit resolution nomenclature will be explained shortly.) The reduction in stage resolution allows for very fast conversion times and small power consumptions. This is due to the relaxed requirements on the subADC portion of the pipeline stage, and is most effective in designs for low-to-medium resolutions.

Most other Pipeline ADCs fall into a class of pipelines known as *Multi-Bit* Pipeline ADCs. These are pipelines with a greater-than 1.5 bit-per-stage subADC resolution, and are most useful in design situations requiring large overall ADC resolutions.

The advantage of a multi-bit pipeline is its large gain at the output of the first MDAC – noise power contributions of all following stages are reduced by the squared MDAC gain. High-resolution designs place stringent requirements on the ADC noise

and, with the larger gain from a multi-bit stage, the size and power consumptions of the back-end stages can be aggressively scaled. (The last stage in a Pipeline ADC is often referred to as the Back-End A/D (or B.E. A/D) and is usually a flash ADC.) The aggressive scaling leaves more budgeted power and area available for the critical initial stages of the pipeline.

2.2.2. Digital Redundancy

Another factor in the choice of subADC resolution is the achievable accuracy of the comparator block. This concern is not limited to the choice of stage resolution, but also affects the overall ADCs resolution and linearity. Without careful consideration, it is also possible for comparison errors to erroneously saturate lower bits in the ADC.

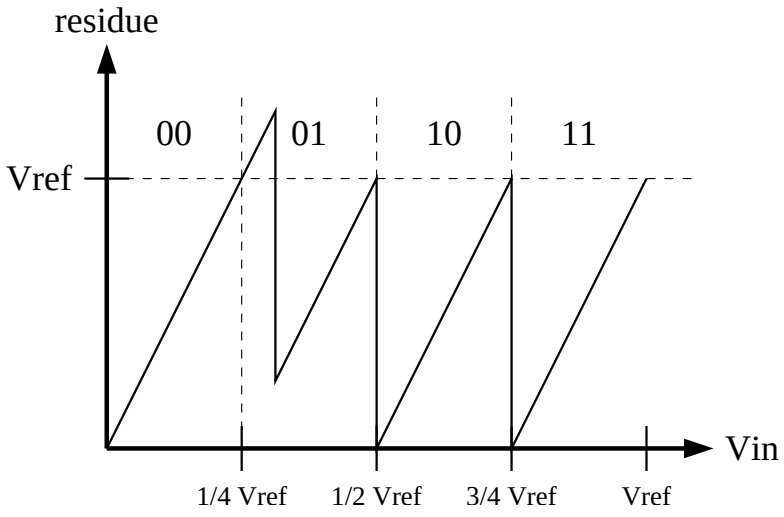

Figure 2.7: Residue Error Example

Consider the example shown in Fig. 2.7. A comparison error at the '00' to '01' transition has allowed the residue voltage to extend beyond the ADC reference voltage. For all signals greater than Vref/4, and less than the actual comparison level, the converter will produce all ones in the remaining pipeline stages and generate significant

non-linearities in the converted signal. An error in the opposite direction will have the same clipping effect, but instead all of the remaining conversions will be zero.

In addition to the saturation error, comparison errors in the first stage contribute to the overall accuracy of the entire pipelined A/D. This means that the first stage comparator function must be as accurate as the entire ADCs desired accuracy.

The fundamental problem with the comparison operation is the level of offset inherent in the comparison operation itself. This comes from inaccurate generation of reference levels and mismatch in the comparator blocks. These can be reduced by a process known as offset-storage [17], but at the cost of increased circuit complexity. Furthermore, the saturation problem still remains.

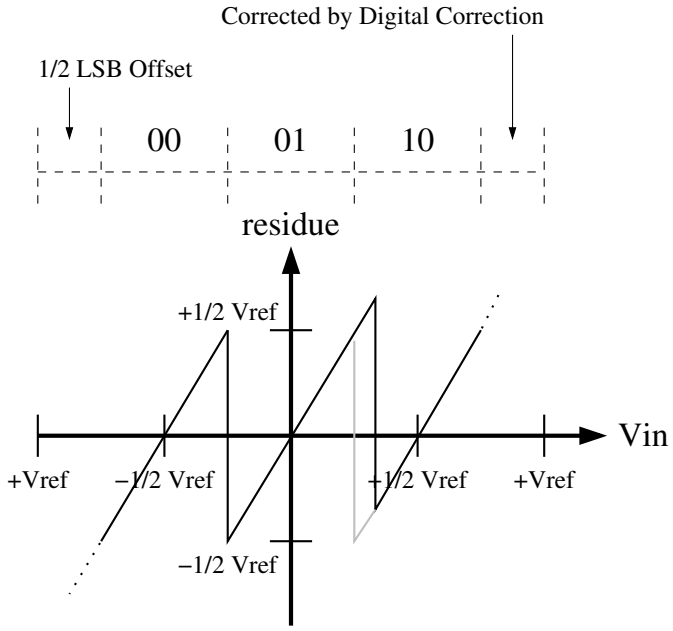

Figure 2.8: Digital Correction Residue

Another, more elegant, solution is to allow each pipeline stage's conversion to overlap with adjacent stages [18] – commonly referred to as *digital redundancy* or *digital correction*. This allows neighboring stages to weigh-in on the correctness of a given output code from neighboring stages. Not only does this correct mistakes in conversion,

but it also keeps the residue output voltage within Vref as long as the comparison error never exceeds 1/2 LSB.

The seminal work on this concept was completed by S. Lewis [19], and also introduced the 1.5 bit-per-stage architecture. In this paper, Lewis suggests the inclusion of 1/2 LSB offsets into the subADC/subDAC path in combination with digital redundancy. This effectively allows the removal of one comparison in a 2-bit subADC (making it a 1.5-bit stage) Fig. 2.8, further reducing the complexity and power requirements. An additional advantage to the 1/2 LSB offset is that there is no longer a comparison point located at the exact common mode of the system. Noise in such systems can make zero-valued signals generate larger-than-designed noise signals in the converted output.

Since Lewis's work, it has been shown that his concepts can be applied to multi-bit pipeline stages as well; an example of this is shown in [20, 21]. The concepts of digital redundancy and 1/2 LSB offset are now standard in most Pipeline ADC designs.

2.3. Data Converter Error

Non-idealities in data converters result in errors in conversion that are measured in LSBs. These errors are commonly referred to as Differential Non-Linearity (DNL) and Integral Non-Linearity (INL). The former is defined by measuring the step between adjacent codes. If the converter is ideal, the step-size should be exactly equal to 1 LSB. This corresponds to a DNL of 0 LSB. The latter is then defined as the "running" integration of all DNL values from code 0 to code $2^N - 1$.

Extreme errors in DNL can produce missing codes. These can occur when the DNL is greater the 1.0 LSB. Generally, the maximum DNL on a part should be less than 0.5 LSB if missing codes could be an issue in the system. This is because two 0.5 LSB comparison level errors can create a missing code (Fig. 2.9). Multi-stage ADCs, including Pipeline ADCs, can also introduce non-monotonicities in the conversion transfer function

that can cause big problems for systems with feedback loops incorporating the ADC. This error type generally comes from gain mismatch between the stages.

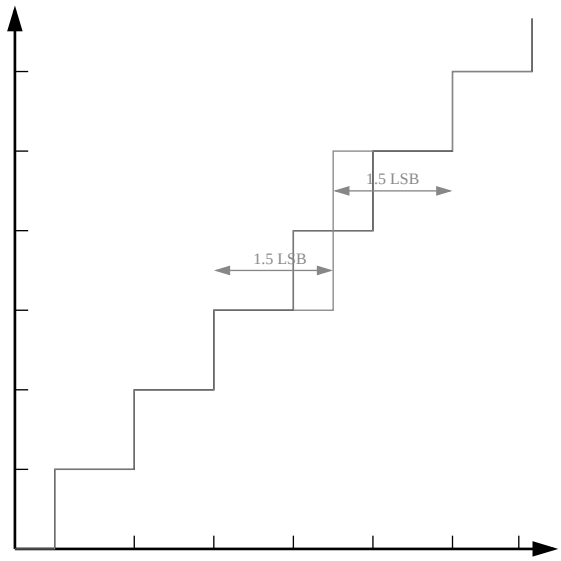

Figure 2.9: Missing Code DNL Condition

These measurements (DNL and INL) are a "static" measurement of the non-linearity. A "dynamic" linearity measurement can be accomplished by applying a single-tone sine wave to the input of the ADC and measuring the spectra to determine harmonic components. Generally, the INL is a pretty good approximation of the value generated from this type of measurement; even so, both measurements are usually taken when characterizing a new ADC design.

2.4. Pipeline Error Sources

Pipeline Analog-to-Digital data converters have many potential error sources – many of them are the same error sources found in other ADCs. There is, however, a fundamental difference in how the error sources appear in the final converted signal for pipelined ADCs.

The segmented nature of the Pipeline ADC is very helpful in addressing power and speed concerns, but complicates understanding and reduction of error propagation from stage to stage. Simple errors in Pipeline ADCs produce non-linearities that are difficult to correct. Much effort has therefore been spent on understanding these errors [22] and finding means of reducing them [17, 23, 24]. Before discussing these Pipeline ADC improvement methods, the error sources themselves should be examined.

2.4.1. Offset Error

Offset errors are simple additive errors that can be modelled as an error constant summed with the signal. Offset errors in analog-to-digital converters are generally not difficult to compensate for – especially when the offset propagates directly to the output. In such a case, a simple system-level calibration can correct this error. The situation is not that simple for Pipeline ADCs. Offsets that occur mid-pipeline can create significant non-linearities; this necessitates special design techniques and careful design to reduce the amount of signal offset present in the pipeline.

Common offset sources in Pipeline ADCs are charge injection, opamp offset and finite gain, comparator offset, and DAC offset.

- Charge injection is a general term for when circuit components that add inadvertent charge. The most common source of charge injection in switched-capacitor circuits is "orphaned" charge originating from the inversion layer when a MOSFET switch is turned off. Charge injection offset can be mitigated with careful design. There are also several "tricks" often used to reduce this offset including early-clocking, dummy switches, and complimentary switches [16].

- Opamp offset compensation and correction techniques are discussed in the following Performance Improvements section. Finite opamp gain is usually addressed by designing the open-loop gain to be "high-enough" to create no ill effects at the

accuracy level desired.

- Comparator offset is nearly a non-issue now that digital correction [19] and input-offset and output-offset storage techniques [17] are commonly used in Pipeline ADC designs. Offset storage techniques will also be discussed further in the Performance Improvements section.

- DAC offset is not present in a stage's output digital code, and therefore cannot be corrected by digital redundancy in the pipeline. There have been several capacitor averaging and self-trimming techniques developed to address this issue [25, 24, 26]. The most common approach to this issue, however, is to complete design and layout using "best practices" to achieve the maximum DAC capacitor matching possible. (These range from matching like components in the circuit design to complicated common-centroid architectures [27] for effective matching in layout.)

2.4.2. Gain Error

Gain error is a multiplicative error that acts on the input signal. It can be modelled as a gain stage where a gain of one is the optimal gain value. Like offset error, gain error on the system level is a fairly simple error to correct. Also, just like offset error within pipelined stages, gain errors can create difficult-to-remove non-linear errors. The most common gain error sources are feedback capacitor to DAC capacitor mismatch and under-settled discrete-time signals.

- Feedback capacitor mismatch is most often mitigated through the use of "best practice" design and layout strategies, as mentioned in the discussion on DAC offset error. Capacitor shuffling techniques have also been used to successfully address this issue.

- Incomplete linear settling creates a gain error on the signal being processed. Careful

design and simulation techniques are usually implemented to be sure that all signals internal to the pipeline settle to the required accuracy within the conversion time. This also limits the presence of non-linear settling components in the output.

- One other gain error source not *usually* a concern for Pipeline ADCs is reference mismatch from stage to stage. Generally the voltage reference is a very-low impedance signal that is sent to each stage of the pipeline. The reference mismatch is almost always negligible. This error source is of concern for this work and will be discussed in detail in the next chapter.

2.4.3. Non-Linear Errors

Linearity is simply defined as a property of a system whereby the input-to-output characteristic is wholly linear and can be described in the form $y_0 = mx_0 + b$. Earlier discussions in this chapter have discussed how simple error sources such as offset error and gain error can contribute to the system non-linearity. There are also some error sources in Pipeline ADCs that are inherently non-linear. These are opamp output non-linearity, signal-dependant switch resistance, and non-linear capacitance.

- Opamp non-linearity comes from the open-loop gain dependance on output level. Opamp output stages have a heavily gain dependant output impedance and therefore a signal-dependant open-loop gain. It can be further inferred that the closed-loop characteristics are also affected by this signal-dependance. The most common design approach to this problem is to provide enough open-loop gain over the expected output range to keep the non-linear effects of the signal-dependant gain in the noise of the data converter.

- Signal-dependant switch resistance is a well-known error source in switched-capacitor circuits [16]. There are two commonly accepted methods for reducing this error.

The first is by use of complimentary switches utilizing both NMOS and PMOS devices. While this is effective to resolutions as high as 10-bits at 100MHz [28], higher-performance designs require better switch linearity than is available with CMOS switches. The second method for reducing non-linear switch resistance is known as *bootstrapping*. This circuit method maintains a constant V_{GS} on the floating sampling switch during the sampling phase and can greatly improve the switch linearity [29, 30].

- Portions of parasitic capacitance within circuit devices are often non-linear. A common source of this non-linearity is depletion region width dependencies on signal voltage. This is most often present at the P-N junctions located at the source and drain nodes of MOSFET devices but can also exist in some types of capacitor devices.

2.4.4. Noise

Unlike other error sources in Pipeline ADCs, noise does not suffer from the complications of stage-to-stage propagation. Because of its random nature, noise in one stage is simply RMS-summed with noise from the preceding stage. This random nature also makes it very difficult to remove noise once it is injected into the ADC. Common sources of noise in Pipeline ADCs are kT/C thermal noise, active circuit noise, and digital switching noise.

- Thermal kT/C noise is the single-pole, bandwidth-limited thermal noise in a basic switched-capacitor sampling system (Fig. 2.10). The thermal noise spectral density at the top-plate capacitor node can be written as

$$\overline{N_O}^2(\omega) = \frac{4kTR_{SW}}{1 + (\omega R_{SW} C_S)^2} \Delta\omega. \tag{2.1}$$

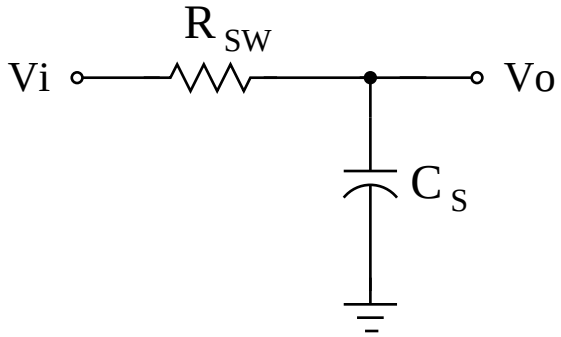

Figure 2.10: Simple Switched-Capacitor Sampling System

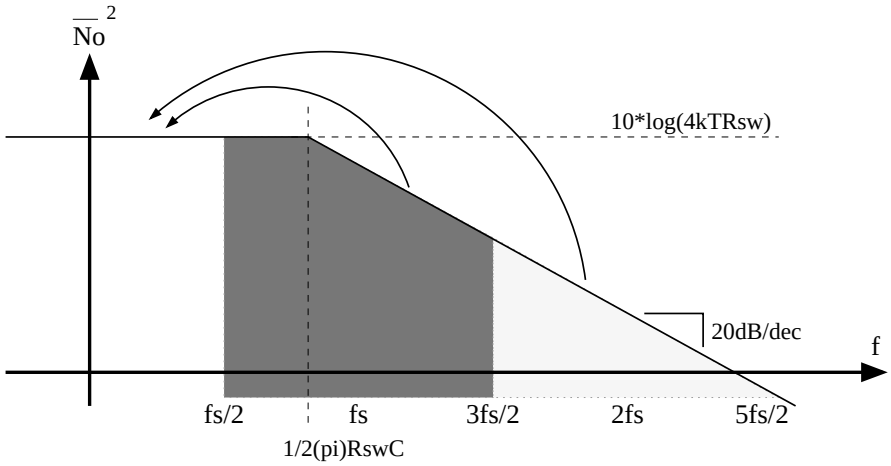

Figure 2.11: Half-Band kTC Noise Integration

When the switch is opened, the sampling action effectively folds the noise contributions from *all* frequencies into the $\pm f_s/2$ frequency band (Fig. 2.11). The thermal noise contribution of the sampling circuit can therefore be computed by integrating the noise spectral density from zero to infinity:

$$N_O^2 = \int_0^\infty \frac{4kTR_{SW}}{1+(\omega R_{SW}C_S)^2} d\omega = \frac{kT}{C_S}. \tag{2.2}$$

This result shows that the switched-capacitor circuit's thermal noise is independent of the actual noise source. The explanation of this behavior is as follows: if the

switch resistance is increased, the thermal noise contribution of the resistor also goes up. However, the bandwidth of the single-pole system goes down with the resistance increase, providing no net difference in integrated noise (Fig. 2.12).

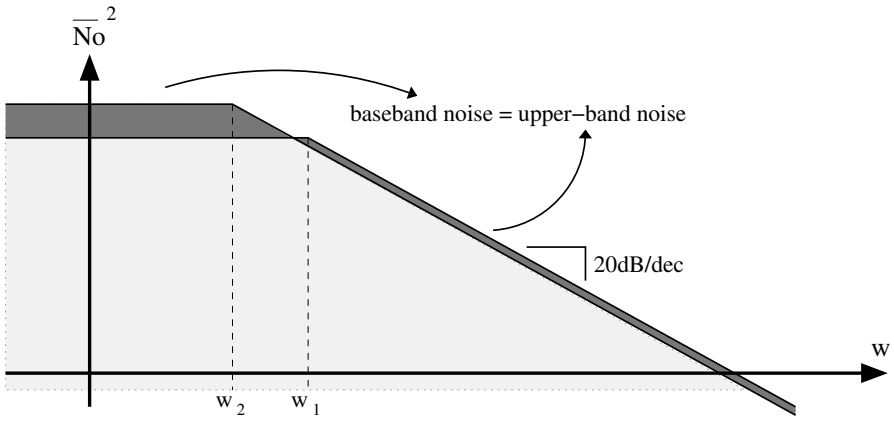

Figure 2.12: Half-Band Noise Density Variation

- Active circuit components also contribute noise to the overall system noise. Generally these noise levels can be reduced by increasing device area and increasing power consumption. Switched-capacitor systems are often limited by kT/C thermal noise, and as such may not be very sensitive to active component noise. Hand calculations and simulation should be completed to ensure that this is true.

- System-on-a-chip (SOC) trends have lead to a mixing of analog and digital circuits on a single chip. While this has definite advantages in manufacturing cost and system implementation, the digital portions of an SOC chip often inject current noise into the substrate and power supplies that have a potential of contaminating analog signals in the analog processing portions of the chip. This issue is addressed at both the system and layout level: first, effort is made to make sure that no major switching event occur during important analog signal-processing periods, and second, significant effort is made to physically isolate analog and digital portions of the chip with separated power supplies and heavy substrate contact shielding

around analog circuits.

2.5. Performance Improvements

There have been many useful circuit and system methods developed to address the issues mentioned in the previous section. These methods include offset storage [31], correlated double-sampling (CDS) [23, 32], capacitor error averaging [25, 24, 33, 26], and many others. The three mentioned are the most commonly used performance enhancement methods.

2.5.1. Offset Storage

The basic concept of offset storage can be explained as a simple two-step process. First, the offset voltage present in the circuit is sampled onto a capacitor during one clock phase. Next, during a following clock phase, this offset is incorporated with some signal processing function in such a way that subtracts the offset from the signal. This produces a net-zero offset as long as the offsets match during both phases.

Offset cancellation was first presented in a paper by R. Poujois *et al.* [31], but was standardized as a fundamental data-converter technique by Behad Razavi in his paper on high-speed, high-resolution comparators [17].

There are two major offset storage methods mentioned in Razavi's paper. These are Input Offset Storage (IOS) and Output Offset Storage (OOS). Both of these methods are intended to correct opamp offset. Simple examples of how each of these offset-storage methods work are given in Fig. 2.13.

- Input Offset Storage works by storing the pre-amplification offset on an input capacitor by means of a unity-gain feedback network around the amplifier. The offset cancellation is only as accurate as the virtual ground level, which is directly

related to the open-loop gain of the amplifier. This form of offset cancellation is often used in MDAC design for pipeline ADCs.

- Output Offset Storage corrects for offset by storing the amplified offset on a capacitor at the output of the amplification stage. This structure limits the allowable gain of the amplification stage, but allows for low-power open-loop amplifier configurations.

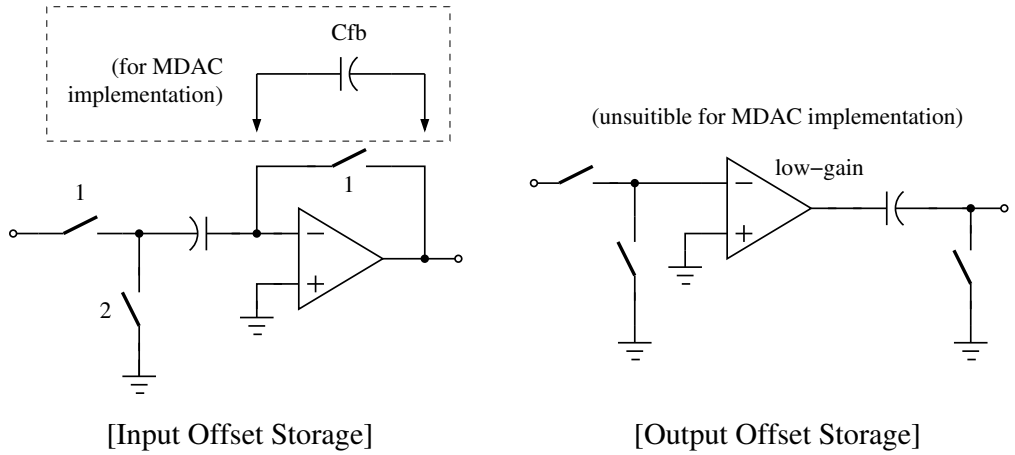

Figure 2.13: Offset Storage Methods

Combinations of these methods placed in series can improve the accuracy of the offset cancellation [17]. Offset cancellation also has the added benefit of cancelling low-frequency noise. The bandwidth of the noise cancelled depends on the time between the sampling and computation phases – when the time between samples is shorter, there is more correlation between the two samples.

2.5.2. Correlated Double-Sampling

Correlated Double-Sampling (CDS), as the name implies, uses two samples to cancel correlated signals. As was mentioned previously, offset storage also cancels noise in

this manner. What CDS provides over other offset storage methods is an improved virtual ground node, thereby greatly increasing the effectiveness of both offset cancellation and signal processing in general. The major drawback of CDS is the added time required to settle the two processed signals used in CDS.

Basic CDS operation is illustrated in Fig. 2.14 – the circuit is a charge-based amplifier. During the first phase, two sampling capacitors $C_{DAC1} + C_{FB1}$ and $C_{DAC2} + C_{FB2}$ are charged to the input voltage. Next, in the second phase, C_{DAC2} and C_{FB2} are connected to the opamp in a standard feedback system. Also, a separate capacitor C_I is connected to the virtual ground and samples the value generated at that node. This value contains the offset and information about the input signal. At this point, the error of the output signal is

$$e_{phase2} = \frac{-1}{A}\left(1 + \frac{C_{DAC1}}{C_{FB1}}\right) V_{o(ph2)}, \tag{2.3}$$

where V_o is the output voltage and A is the open-loop amplifier gain. This equation (2.3) shows an inverse dependance of the error on open-loop amplifier gain. During the final phase, C_{DAC1} and C_{FB1} are disconnected and C_{DAC1} and C_{FB1} are connected in the feedback system. The error-storage capacitor C_I is then placed in series with the virtual ground node. This creates an improved virtual ground and the final error seen out the output is approximately

$$e_{phase3} \approx \frac{-1}{A^2}\left(1 + \frac{C_{DAC1}}{C_{FB1}}\right)\left[\left(1 + \frac{C_{DAC1} + C_I}{C_{FB1}}\right) V_{o(ph2)} - \left(\frac{C_I}{C_{FB1}}\right) V_{o(ph3)}\right]. \tag{2.4}$$

This equation equation (2.4) shows that correlated double-sampling squares the effective open-loop gain of the opamp. The relaxed open-loop gain requirement makes this method very attractive for high-resolution Pipeline ADC designs.

One of the major drawbacks of this technique is the extra clock phase required for the CDS operation. Recent work in this area has produced a method for removing this

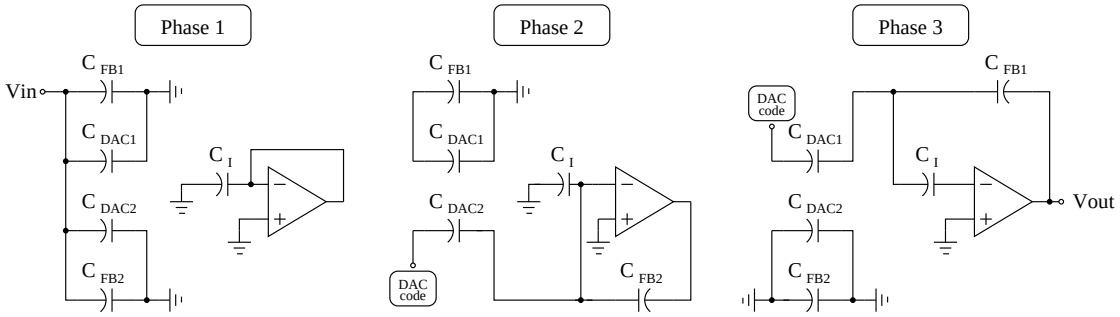

Figure 2.14: Correlated Double-Sampling

extra phase while still maintaining most of the benefit of CDS [28] – it is called *time-shifted CDS*. A special sample-and-hold circuit is required to implement this version of CDS and would be difficult to implement at the high resolutions targeted in this thesis.

2.5.3. Capacitor Error Averaging

Capacitor mismatch is a problem for both the DAC and multiplication functions in charge-based MDAC circuits. These create both offset and gain errors that translate into non-linearities in pipeline ADCs.

Early high-accuracy ADC designs employed trimming to achieve matching beyond the accuracy of the process [6]; however, this is an expensive post-processing step. There have been many circuit techniques developed to address the matching issue without the use of trimming. The most commonly used technique today was first introduced as Dynamic Element Matching (DEM) [25], but has also been referred to more generically as capacitor error averaging.

The basic concept of capacitor error averaging is to shuffle the use of individual capacitors in the MDAC so that the device-to-device mismatch over time is averaged (Fig. 2.15). This produces an improved linearity result over not shuffling.

Some error averaging techniques offer significant capacitor-matching improvement by averaging opposing polarity errors. One of these methods is known as Passive Capac-

itor Error Averaging (PCEA) [34]. The drawback of these methods is that extra clock phases are required to average multiple samples together.

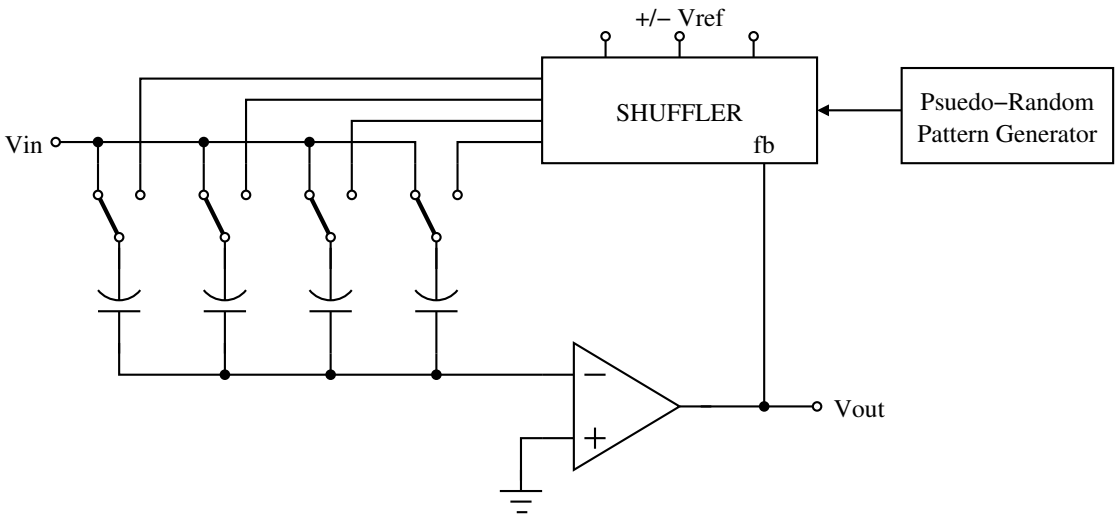

Figure 2.15: Capacitor Shuffling for DEM

2.6. Calibration Techniques

A more passive approach to correcting errors in ADCs is calibration. Generally, calibration can be categorized into two major operation modes: foreground and background.

Foreground calibration requires that the ADC stop conversion in order to process a calibration signal of some kind. Data from the conversion of this calibration signal is then used to store calibration data that will ether directly be applied to the output result or control the operation of the ADC during normal operation. Depending on the system the ADC is placed in, this type of calibration may or may not be acceptable – calibration can take up to several seconds to complete in many implementations and may need to be periodically updated.

Background calibration, on the other hand, works transparently in the background

during normal ADC operation. The calibration values are calculated while data is being converted in the ADC. In order to accomplish this, a test signal (usually a psuedo-random sequence) is injected into the real signal, then correlation techniques are used to extract the data required for calibration from the output. Some published examples of this are [35, 36]. The major disadvantage of this method of calibration is that the test signal takes up a portion of the signal swing and therefore reduces the SNR achievable by the ADC.

Most calibration concepts can be implemented as either foreground or background; however, the background version is usually more complicated. The three most common areas of calibration in Pipeline ADCs are Code-Error Calibration, Radix Calibration, and Non-linear Calibration.

2.6.1. Code-Error Calibration

Capacitor mismatches in MDACs directly generate DNL errors for remaining stages. In addition, the error levels are different for each individual code. Code-error calibration [21] generates error correction codes that, when added to the output code, correct each individual code error.

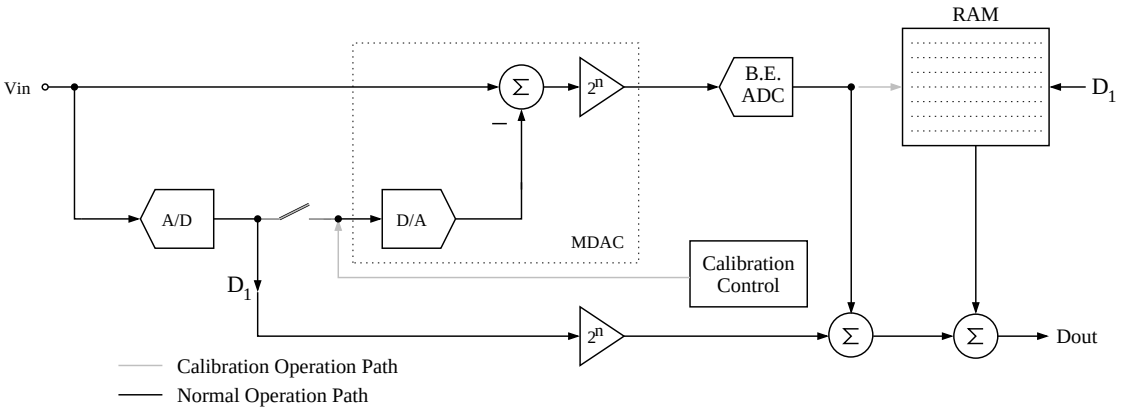

Figure 2.16: Code-Error Calibration Implementation

The first step in this calibration technique is to measure the step error from one DAC code to the next. The error is then measured with the remaining A/D stages in the pipeline. The expected value is subtracted from the result and all that remains is the error, which becomes the correction code for that particular DAC code. This process is illustrated in Fig. 2.16. The remaining stages of the Pipeline ADC must be a higher resolution than actual requirement for normal signal conversion. Multiple measurements can be averaged to make sure that thermal noise is removed from the error correction code.

The error correction codes are often stored in RAM memory on-chip and addressed by the first stage DAC codes. This correction technique is easy to implement and the required addition during data-conversion is an easy task to accomplish in parallel to normal processing.

2.6.2. Radix Calibration

Capacitor mismatch can also generate gain errors in Pipeline ADCs. Other potential sources for this type of error are finite MDAC amplifier gain and linear settling errors. All of these errors can be addressed in Pipeline ADCs through Radix Calibration [37].

Standard 1.5 bit-per-stage Pipeline ADCs have a nominal radix of two. This means that the code resolved at each stage has an expected base value of two. Gain errors directly adjust this value, but if the new radix value is known by the system using the ADC, a "perfect digital code" (radix two code) can be generated through simple calculation using the individual radix values for each code converted at each stage in the pipeline (Fig. 2.17).

$$decimal\_value = (1.9)(2.1)(2)D_1 + (2.1)(2)D_2 + (2)D_3 + D_4. \tag{2.5}$$

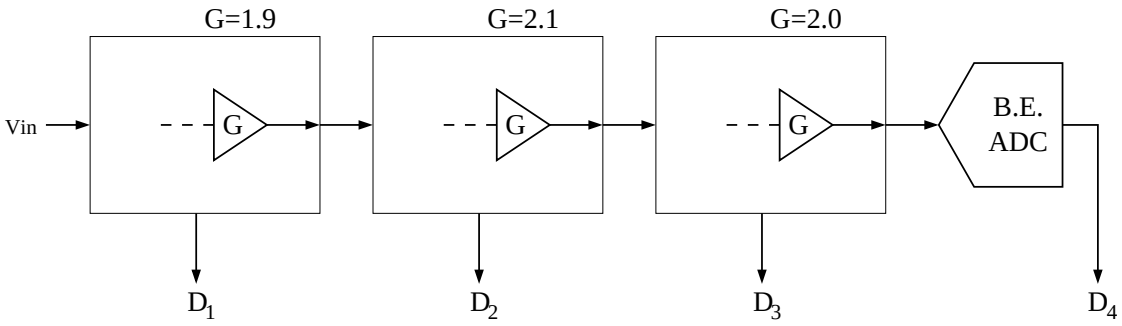

Figure 2.17: Radix Calibration

This is an elegant solution for 1.5 bit-per-stage Pipeline ADCs, but can be computationally intensive to implement. Also the conversion-time processing requirements are quite large, due to the floating-point multiplication required to correct the digital output.

2.6.3. Non-linear Calibration

This type of calibration addresses non-linear errors inserted by devices behaving in a non-linear fashion within individual pipeline stages. Common non-linearity sources are MOSFET switches and operational amplifiers. The calibration of non-linear errors allows low-power and low-complexity analog circuits to be used within the ADC at the cost of higher digital complexity for correcting the errors generated by these circuits. Recent examples of this calibration concept can be seen in [38] and [39].

CHAPTER 3. SYSTEM AND CIRCUIT ARCHITECTURE DESIGN

This chapter will cover system design considerations for high-resolution, medium-speed Pipeline ADCs. Specifically, 14-bits of ENOB at 20 MSPS (Mega-Samples Per-Second) is the desired performance of the Pipeline ADC. The high-resolution requirement places stringent requirements on the front-end of the pipeline and therefore substantial thought and consideration should be placed in choosing the system structure. A poor choice in architecture can lead to excessive waste in power and area.

Additionally, the noise contributed from kT/C sampled thermal noise dictates that for each single-bit increase in SNR, a 4x increase in sampling capacitance is required. As mentioned in the introduction, recent designs have limited their ENOB to approximately 12-bits. The 2-bit improvement desired for this work requires a 16x increase in capacitance to improve the SNR performance of similar converters to the required level. Achieving SNR improvement economically will require some extra effort in the system level design.

3.1. Bits-Per-Stage Architecture

One major architecture consideration in the design of any Pipeline ADC is the choice of bits resolved per-stage. Low resolutions per-stage are generally suited for lower resolution and higher speed Pipeline ADCs, while high resolutions per-stage (often referred to as multi-bit) are more suited to the high accuracy requirements of the applications mentioned in this thesis.

3.1.1. MDAC Tradeoffs

There are three major metrics within MDAC design that can determine the required cost (in power and area) dependant on per-stage-resolution. They are conversion speed, converter accuracy, and noise, and are assumed to be fixed design requirements. A simplified MDAC structure is shown in Figure 3.1 for reference during this discussion.

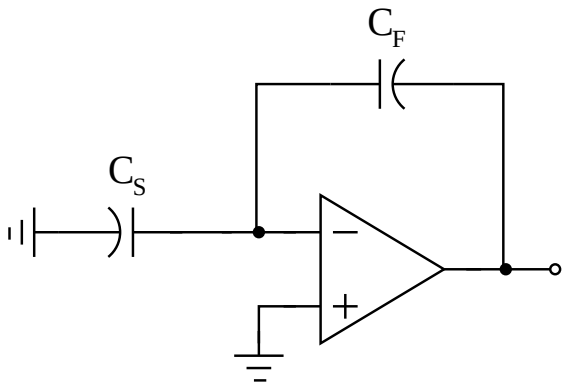

Figure 3.1: Simple MDAC Reference (Amplification Phase)

Conversion Speed

Conversion speed is directly related the per-stage-resolution by way of the loop feedback factor. The feedback factor is easily determined to be

$$\beta = \frac{C_F}{C_S + C_F}, \tag{3.1}$$

where C_S and C_F are the capacitance values as shown in Fig. 3.1. Stage gain (determined by per-stage resolution) is equal to C_S/C_F, and by substitution, the feedback factor becomes

$$\beta = \frac{1}{G+1}, \tag{3.2}$$

where G is the stage gain defined as 2^n. The variable 'n' is bits-resolved-per-stage.

A common starting design parameter is the loop unity-gain bandwidth (UGBW). This determines (in conjunction with capacitive loads and feedback factor) such design parameters as opamp power consumption and device sizes, and is stipulated by stage settling requirements. Loop UGBW relates to the feedback factor (β) in equation 3.2 by the following equation:

$$\omega_{t(open)} = \omega_{t(loop)} \frac{1}{\beta} = \omega_{t(loop)}(G+1), \tag{3.3}$$

where $\omega_{t(open)}$ is the required amplifier open-loop UGBW to meet the loop UGBW requirement.

Equation (3.3) shows that increasing the stage gain increases the bandwidth requirement, and therefore the power consumption of the MDAC stage; however there is a compensating factor. The gain increase reduces the number of stages required to meet the design goal, but at a diminishing rate in comparison to power consumed. Increasing the stage-resolution increases the power consumption needed to meet the settling requirements.

These statements ignore the common practice of load-scaling from stage-to-stage, which would improve the power consumption required for setting. The incorporation of this scaling can actually *improve* the power consumption required for settling; however, this breaks-down as the desired A/D conversion speed approaches the given technology's f_t limitations. In this condition, there is a diminishing return on open-loop UGBW for increased power consumption. This is why single-bit-per-stage Pipeline ADCs (or 1.5 bit-per-stage) are common for high-speed data conversion systems.

Converter Accuracy

Overall converter accuracy sets limitations on allowable error in the analog signal between stages in the pipeline. For instance, if an overall converter accuracy (noise and linearity) requirement is 12 bits, the sample-and-hold stage must be able to output a greater-than 12 bit accurate analog output signal for the following stage.

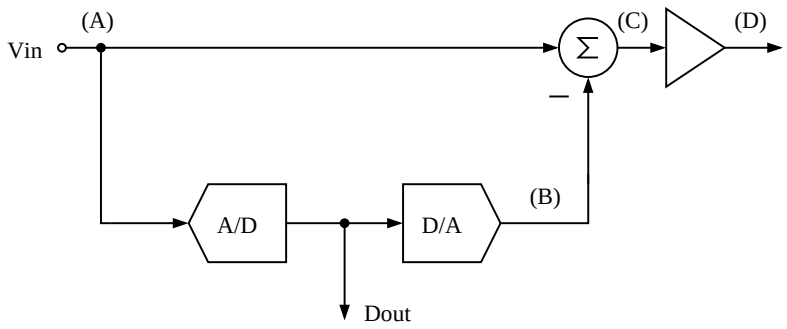

Figure 3.2: System-Level Pipeline ADC Stage

A system-level representation of a Pipeline ADC stage is shown in Fig. 3.2; it can be seen that the signal accuracy at points (B) and (C) must match the accuracy at point (A). After the gain, point (D) need only be as accurate as point (A) divided by the gain. This implies that the output accuracy requirement is lessened when more bits are resolved within a given pipeline stage.

The relationship between per-stage-resolution and power consumption due to settling accuracy requirements can expressed as a UGBW frequency:

$$\omega_t = \frac{-ln\left(2^{-(M-n)}\right)}{t_{settle}}, \tag{3.4}$$

where the numerator is the commonly used $t = x \cdot \tau$ settling time calculation [16], M is the overall desired ADC accuracy, and t_{settle} is allowable half-clock-phase settling time. It should be noted that ω_t is the *loop* unity-gain bandwidth requirement.

From (3.4) it can be seen that when the stage-resolution (n) is increased, the required closed-loop bandwidth is reduced. This partially compensates for the power increase experienced from the change in feedback factor by increasing stage gain.

Sampled Noise

High accuracy ADC designs require careful consideration of noise contributors and system architecture to realize power-efficient ADCs while still maintaining desired accuracy levels. Again, the simple MDAC example in Fig. 3.1 is used to develop an

equation illustrating the effect of stage-resolution on this design parameter.

The charge noise of each capacitor is given as $\overline{q}_n^2 = kTC$. The output referred voltage noise is then

$$\overline{v}_{n(out)}^2 = \frac{2kTC_S + 2kTC_F}{C_F^2}, \tag{3.5}$$

where it is assumed that each capacitor samples a value during each of two phases (generating the '2' in '$2kTC$'). Reduction of the equation provides

$$\overline{v}_{n(out)}^2 = \frac{2kT}{\beta C_F} = \frac{2kT}{C_F}\left(G+1\right), \tag{3.6}$$

where G is defined as in (3.2). Referring (3.6) to the input of the MDAC gives

$$\overline{v}_{n(in)}^2 = \frac{2kT}{C_F}\left(\frac{G+1}{G^2}\right). \tag{3.7}$$

A simple substitution from the MDAC gain equation, $G = \frac{C_S}{C_F}$, into (3.7) gives

$$\overline{v}_{n(in)}^2 = \frac{2kT}{C_S}\left(\frac{G\left(G+1\right)}{G^2}\right) = \frac{2kT}{C_S}\left(\frac{G+1}{G}\right). \tag{3.8}$$

Actual MDAC implementations would use the feedback capacitor C_F for sampling as well – this reduces the $G+1$ term to G. Equation (3.8) then shows that sampled, input referred noise has no dependance on per-stage resolution.

Active Circuit Noise

Active circuit noise can be considered in a similar fashion. Figure 3.3 is used to develop the equation describing active circuit dependance on per-stage resolution. There are two noise sources shown in the figure; each source will be considered independently by way of superposition.

The first noise source to be considered is $\overline{v}_{n1}$, which models the one of the input-pair noise sources. It's contribution to output noise can be calculated by the following:

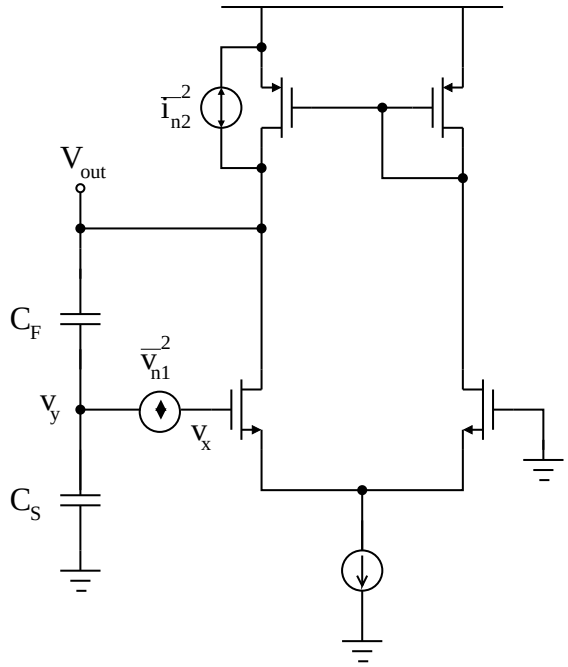

Figure 3.3: Active Circuit Noise Sources Example

Nodes v_x and v_y can be written as

$$v_x = -\frac{v_{out}}{A}; v_y = \beta v_{out}, \tag{3.9}$$

where A is the open-loop gain of the amplifier and β is the feedback-factor defined by the capacitive feedback network. The value of the noise source $\overline{v}_{n1}^2$ can be written as

$$\overline{v}_{n1}^2 = \overline{v}_y^2 - \overline{v}_x^2 = \beta^2 \overline{v}_{out}^2 + \frac{\overline{v}_{out}^2}{A^2}. \tag{3.10}$$

Rewriting (3.10) for $\overline{v}_{out}^2$ reveals the output noise contribution:

$$\overline{v}_{out}^2 = \frac{\overline{v}_{n1}^2 A^2}{1 + \beta^2 A^2} \approx \frac{\overline{v}_{n1}^2}{\beta^2}. \tag{3.11}$$

If it is assumed that $\beta \approx 1/G$, then the *input* referred noise can be written as

$$\overline{v}_{in}^2 \approx \overline{v}_{n1}^2. \tag{3.12}$$

This shows no dependance on stage resolution for input-referred noise.

Next, the current noise source ($\bar{i}_{n2}^2$) will be considered, which represents a load noise source. The output-referred noise of this noise source is

$$\bar{v}_{out}^2 = \bar{i}_{n2}^2 r_o^2, \tag{3.13}$$

where r_o is the amplifier output resistance. The same noise input-referred is shown as

$$\bar{v}_{in}^2 = \frac{\bar{i}_{n2}^2 r_o^2}{G^2}. \tag{3.14}$$

It is evident from this equation that there is a per-stage resolution dependance for this noise source. This is true for all amplifier noise sources outside the feedback loop. The implication of (3.14) is that active circuit noise can be reduced (as measured at the input) by using a higher stage resolution.

Number of Stages and Noise

Another important stage resolution dependant noise consideration is the more stages vs. less stages tradeoff. This is essentially the same as less resolution per-stage vs. more resolution per-stage, but will be considered on a more basic architectural level.

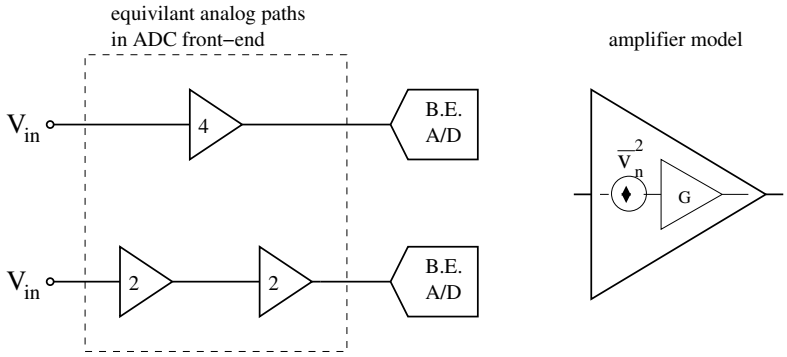

Figure 3.4: Stage Number Noise Tradeoff Comparison

A simple comparison of two stage conversion size options is shown in Fig. 3.4. Both signal paths achieve the same signal conversion before the back-end A/D and both

stages have the same overall gain from the input to the back-end A/D. If it is assumed all amplifiers have the same input referred noise, as implied by eqn. (3.12) it is easy to see that the single-amplification signal path has less noise than the other path. This makes intuitive sense because more stages means more devices and more opportunity for noise to be injected into the signal path.

3.1.2. Capacitor Matching

The ability to make a highly-accurate Pipeline ADC (without calibration) depends heavily on capacitor matching parameters of the CMOS process. The Digital-to-Analog portion of the MDAC block must be accurate to the number of bits of accuracy required at the input of that stage (node (B) in Fig. 3.2). The DAC accuracy is directly dependant on the capacitor matching, which can be 10 to 14 bits (or higher) depending on the process and capacitor unit size.

Achieving these levels of matching requires very large unit-size capacitors (on the order of a picofarad) as well as good common-centroid layout techniques [27]. Common-centroid layout is fairly straightforward for low-resolution capacitor DACs, but DACs for multi-bit Pipeline ADCs, with 3 or more bits, can make good common-centroid layout very difficult.

Even so, there is a matching/linearty benefit to be gained from using a multi-bit architecture. The Differential Non-Linearity (DNL), which is highly dependant on the capacitor matching in the DAC, can be improved by increasing the stage-resolution [40]. The relationship describing this improvement is

$$DNL = \frac{k \cdot 2^{M-n/2}}{\sqrt{C_{total}}}, \tag{3.15}$$

where M is the total converter resolution, n is stage resolution, k is a capacitor device parameter, and C_{total} is the total capacitance used in the DAC. The result of this equation

is that Differential Non-Linearity (DNL) improves by a factor of $\sqrt{2}$ for every single-bit increase in stage conversion.

The explanation for this behavior is as follows. The standard deviation of the capacitance in a unit capacitor has been derived from device models and measurements [41] and can be written as

$$\sigma_c = k \cdot \sqrt{\sigma_A^2}. \tag{3.16}$$

Stated in words, the standard deviation of a unit-sized capacitor is proportional to the square-root of the area variance. Furthermore, the area variance is directly proportional to the area of the capacitor. This is expected because the capacitance value is proportional to the area of the capacitor. This then implies that the standard deviation of a set of unit-sized capacitors is proportional to the square-root of the unit-sized capacitor area

$$\sigma_{cu} \propto \sqrt{A_{cu}}. \tag{3.17}$$

The application of this relationship to the DAC within the Pipeline ADC stage can be summarized. If the number of bits resolved in a stage is increased by one, the DAC unit-capacitor size is reduced by two. This implies a *increase* in error by a factor of $k \cdot \sqrt{2}$ relative the the unit-sized capacitor; however, the absolute error has been *reduced* by a factor of $\sqrt{2}$ (if $k = 1$). This is due to the extra bit resolved in the stage; the allowable error at the output has increased by two because there is one less bit to resolve. The reduction of absolute error in the MDAC produces net decrease in overall converter DNL.

Only Differential Non-Linearity is addressed by eqn. (3.15) and the preceding discussion, but converted signal linearity is affected by both Differential Non-Linearity and Integral Non-Linearity (INL). In order to study the effects of capacitor mismatch and per-stage resolution on INL as well as DNL, a C-program was developed that mathematically replicated the function of an MDAC and included programmable random errors

on the capacitor values. The results of this program are shown in Figures 3.5 – 3.10.

The figures are a histogram of maximum DNL and INL levels over 400 simulations of the Pipeline ADC system. This system is comprised of two stages where the first stage is scaled from 2 to 6 bits and the second stage is adjusted to generate 12 total bits. The x-axis (going into the page) defines the number of bits resolved in the first stage for each run starting with 2 bits for the front histogram and ending with 6 bits for the last histogram. The capacitor standard-deviation scaling factor k from eqn. (3.16) was chosen to be '1' for these simulations. The total available capacitance was not changed between the different stage resolution sizes. The result of these choices is that the capacitor mismatch (σ) gets worse by a factor of $\sqrt{2}$ for each bit increase in stage resolution.

As expected, the DNL improvement is approximately $\sqrt{2}$ for each bit increase in the first stage. Examination of the INL, however, shows no improvement over change in first stage resolution. An intuitive explanation for this is that the total error within C_{total} did not change with first stage resolution, it was just spread among smaller parts. DNL can be considered the part-to-part mismatch, and INL can be thought of as the overall mismatch.

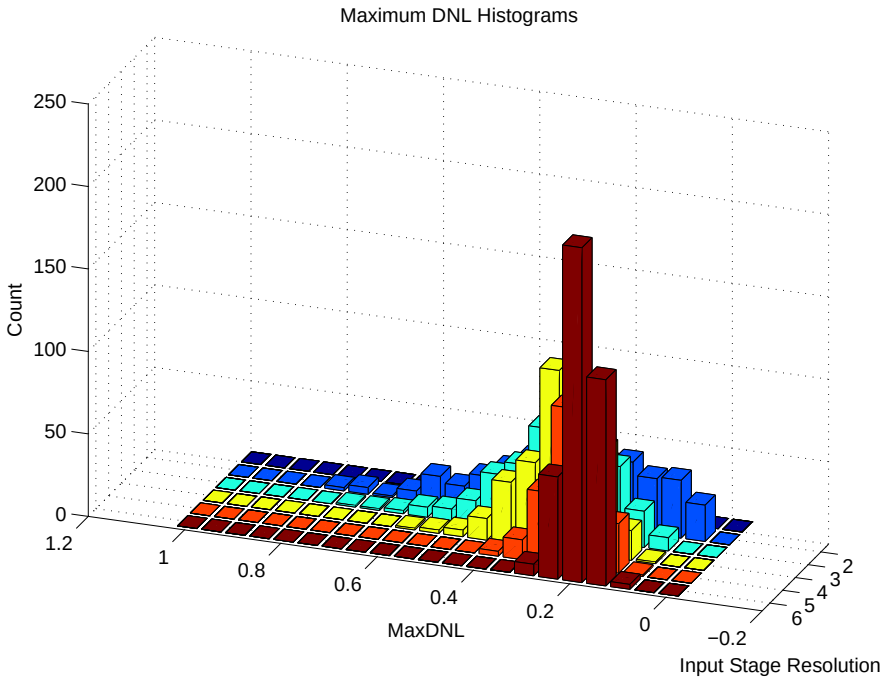

Figure 3.5: Maximum DNL Histogram Comparison

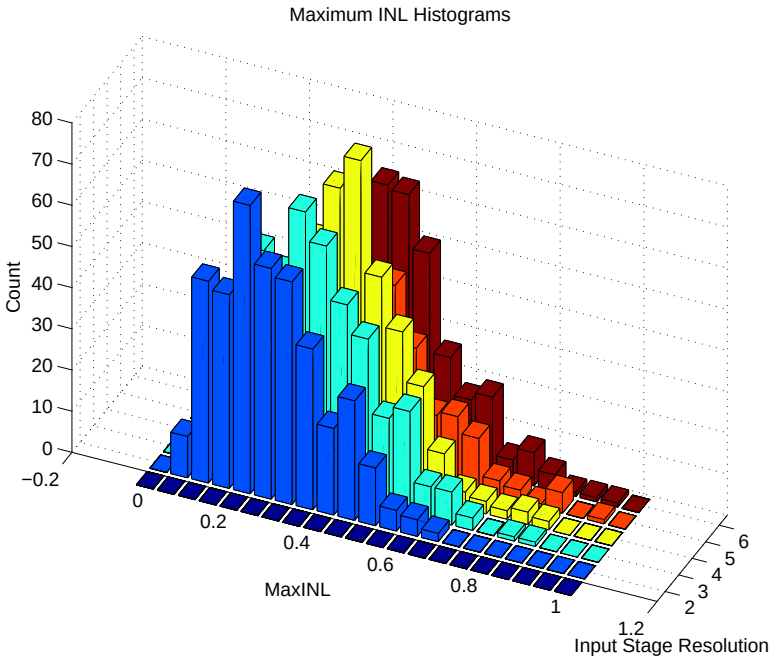

Figure 3.6: Maximum INL Histogram Comparison

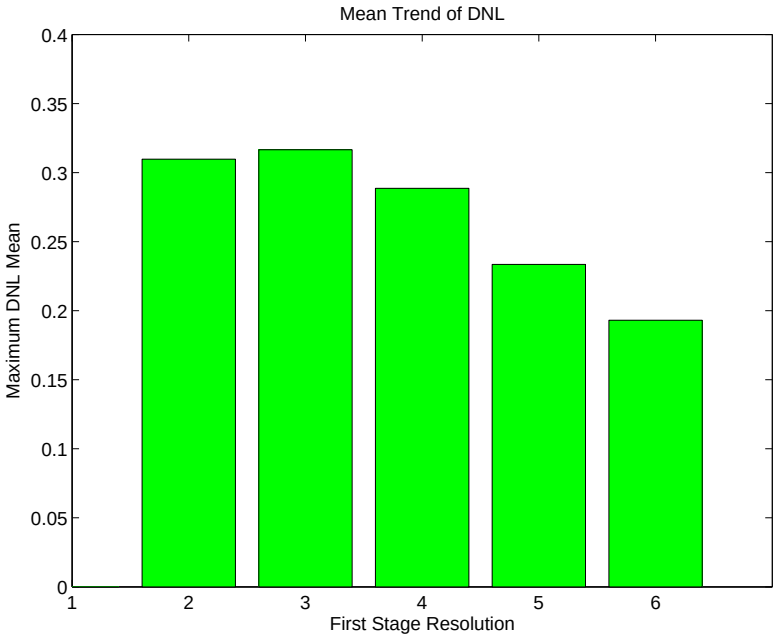

Figure 3.7: Maximum DNL Mean Over Stage Resolution

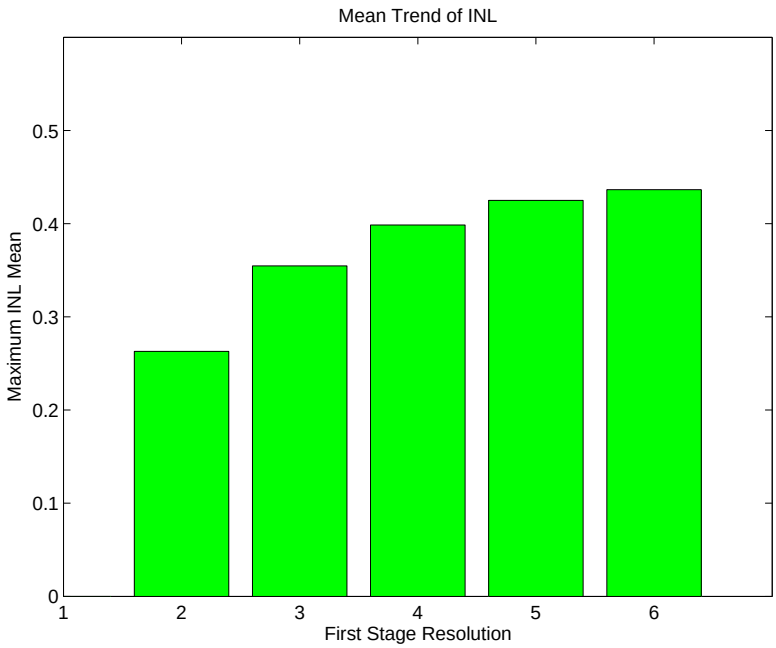

Figure 3.8: Maximum INL Mean Over Stage Resolution

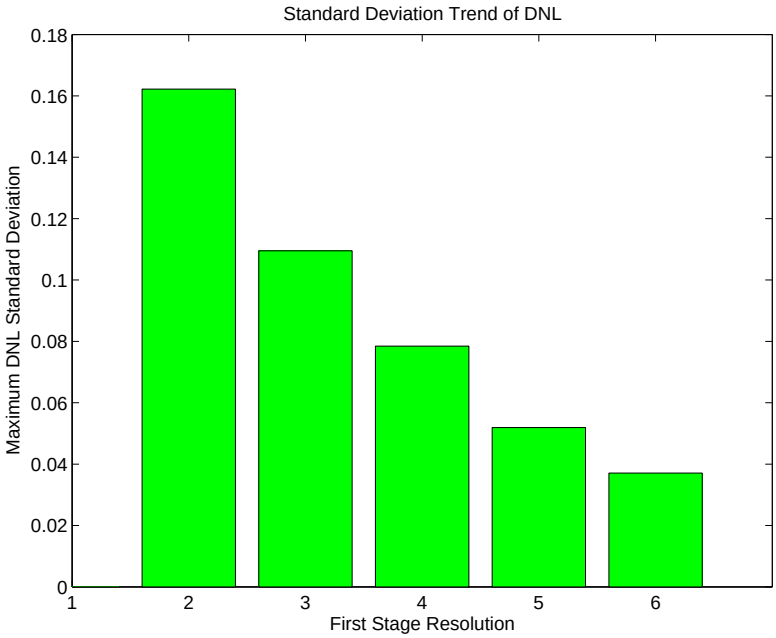

Figure 3.9: Maximum DNL Standard-Deviations Over Stage Resolution

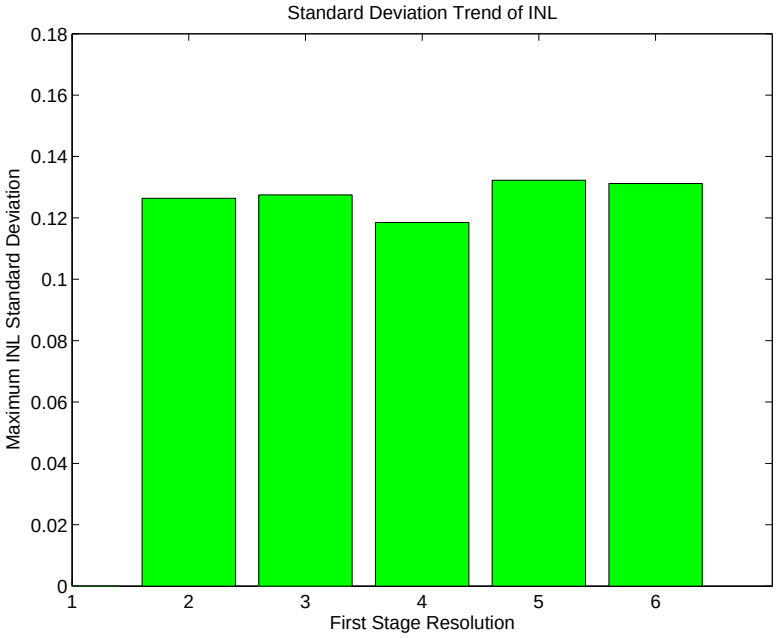

Figure 3.10: Maximum INL Standard-Deviations Over Stage Resolution

3.1.3. Comparator Tradeoff

Thus far in the comparison between single-bit per-stage and multi-bit per stage Pipeline ADC architectures we have seen several compelling reasons to choose higher-resolution pipeline stages over lower-resolution stages. One major drawback to the multi-bit architecture not mentioned thus far is the exponentially increasing power consumption in the flash-type comparator within each pipeline stage. This will obviously limit the per-stage-resolution that can be achieved efficiently.

Low-resolution stages also have the advantage of a large digital correction range. This allows comparators for these stages to be built very cheaply and to consume very little power. The per-stage resolution tradeoff will be revisited in Section 3.4, Pipeline Optimization.

3.2. Sample-and-Hold Removal

One major contributor to overall system noise and power consumption is the Sample-and-Hold (S/H) circuit. The circuit provides a sampled, unity-gain signal to the first pipeline stage, which allows some flexibility in the operation of the pipeline stage. The sampling function can, however, be incorporated into the first stage of the pipeline if the Sample-and-Hold is removed.

The removal of the S/H will effectively cut the required power consumption *and* capacitor area in half. This is because the unity-gain provided by the S/H circuit implies equal relative noise contributions between the S/H and the first Pipeline stage. For high-resolution designs, the noise contributions of these stages are usually dominated by kT/C thermal noise. If it is assumed that pipeline stages after the first stage consume a minimal amount of power and area in the overall system budget, then the power and area savings from the S/H removal is approximately half.

3.2.1. First Stage Pipeline Sampling

The removal of the S/H circuitry requires additional complexity within the first pipeline stage in the ADC. In a typical Pipeline ADC, each pipeline stage pre-resolves the sub-ADC level (Fig. 3.11) before the completion of sampling on the MDAC sample capacitors. The extra time allows the DAC subtraction levels to be determined before the MDAC switches from sampling mode to amplification mode.

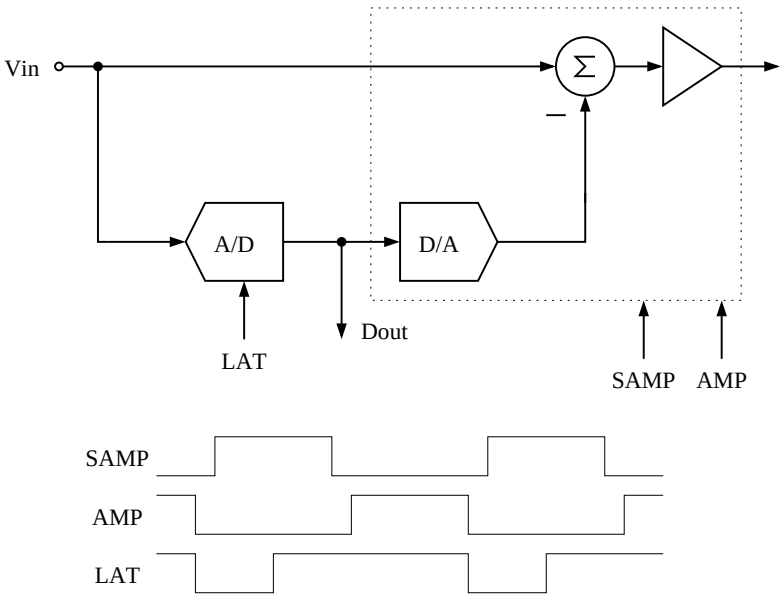

Figure 3.11: Pre-Resolution within Pipeline sub-ADC

The continuous-time input signal is directly applied to the first stage of the Pipeline ADC, and thus the comparator and MDAC must both sample the input at exactly the same time to properly resolve the correct residue voltage (Fig. 3.12). This requirement was addressed in [12], wherein a global input switching network was used to try and match the sampling paths (Fig. 3.13).

This solution, however, still suffers from independent sampling switches and diffi-

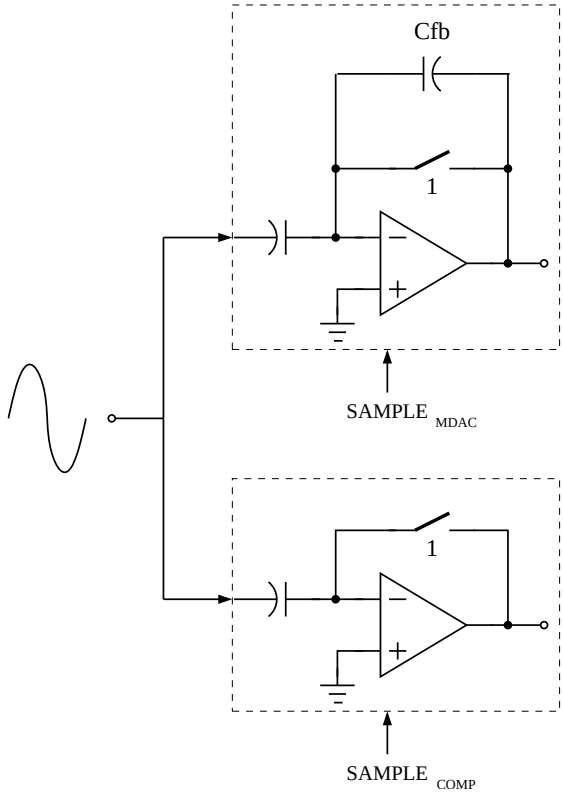

Figure 3.12: Two Sampling Paths

culty in matching the impedance as seen by both sampling paths. That is, the Gm of the comparator preamplifier and the Gm of the MDAC operational amplifier must be matched to provide the same transient response across the sampling capacitors in the comparator and MDAC respectively. Additionally, separate reference sampling capacitors are required in the MDAC, to the detriment of both the feedback factor and the kT/C noise.

An improvement to this structure was introduced in [13]. Instead of sampling the top-plate of the sampling capacitor via unity-gain feedback, both paths are sampled on MOSFET switches to a reference voltage (Fig. 3.14). This makes the matching of the sampling paths much easier to achieve. Also, because of the independent input switches, the extra reference sampling branch in the MDAC is not required and the kickback suppression provided by preamplifiers in the comparator is no longer required. It should also

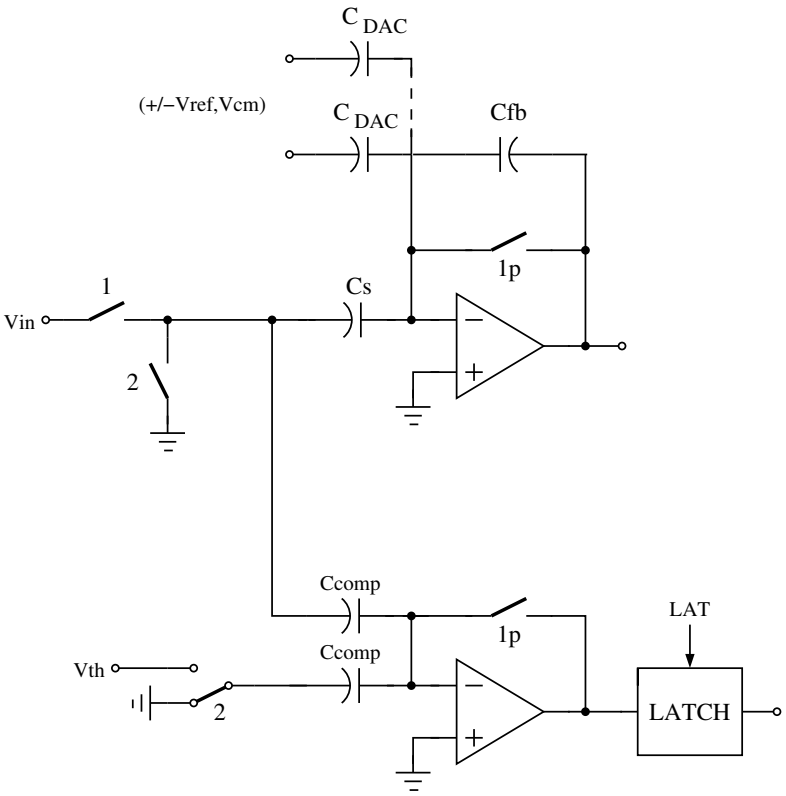

Figure 3.13: Shared Sampling Architecture without S/H

be noted that a charge summing structure is used to perform the comparison operation in the comparator. This is required because the reference cannot be pre-sampled on the input capacitor.

Latch regeneration time must also be considered for the first pipeline stage. In a Pipeline ADC with a Sample-and-Hold stage, the latches in the first stage comparators regenerated during the time between the comparator sampling instant and the MDAC sampling instant. This guarantees that the reference signals to be applied to the MDAC DAC capacitors during the amplification phase will be determined and settled before the MDAC changes modes.

With the removal of the S/H, latch regeneration time must now be scheduled in between the dual-channel (MDAC and Comparator) sampling phase and the amplification phase. This implies an extra phase, and assuming a uniform distribution of the

conversion period, results in a very undesirable speed loss.

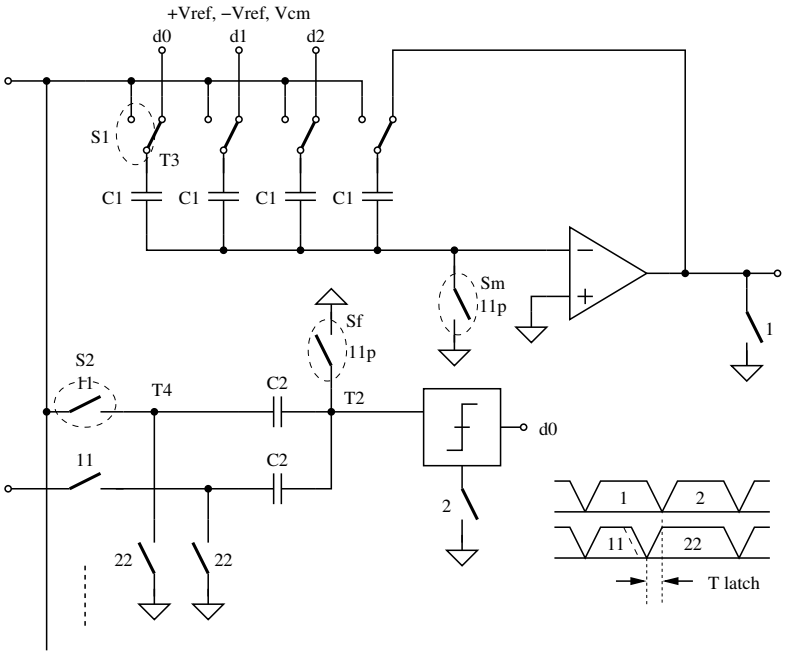

Figure 3.14: Separate Sampling Architecture without S/H

One simple solution to this is to schedule the latch regeneration time into the sampling time. Because the sampling switches must be optimized for high-linearity, they will already have relatively small time-constants and therefore provide for a fast settling time. Reduction of the sampling time is not as critical as reduction of the amplification time – especially when the required power consumption increase to the amplifier is considered.

An adaptation of the S/H removal concept in [13] is used in this work. Preamplifiers are kept in the comparators, and output offset storage (OOS) [17] is used to cancel latch and preamplifier offsets – this is especially important because the MDAC opamp offset and any sampling mismatch will eat into the digital correction range. The implementation is as shown in Figure 3.15; timing is included and shows the latch regeneration time.

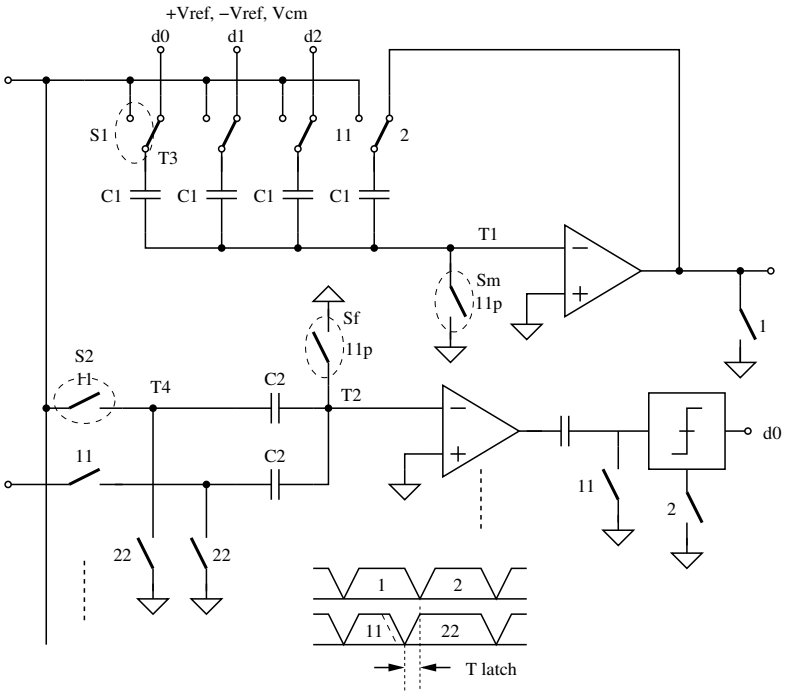

Figure 3.15: First Pipeline Stage with no S/H

3.2.2. Mismatch Tolerance

The most important requirement of the sampling first-stage is that both the comparator input sample and the MDAC input sample be accurate to within the digital correction range of the pipeline stage (1/2 LSB). There are two key components to the matching of these sampled values. The first of these is the matching of the continuous-time response of the RC circuits and the second is the matching of the sampling response (opening the sampling switches).

The first component is addressed by matching the RC networks as precisely as possible. It practice, exact matching cannot be achieved due to physical displacement of devices to be matched on the silicon die. Additionally, the comparator contains a capacitive branch not present in the MDAC that is used for charge summing during the comparison operation. Both of these problems limit the matching that the continuous-

time signals can achieve. The use of unit-sized capacitors in both the comparator and MDAC can significantly improve the capacitor matching between the MDAC and comparator sampling capacitors, but the large difference in desired capacitance size between the two different paths makes this solution highly undesirable.

An equation that quantifies the allowable RC mismatch (to a first order) is presented in [12] and is shown to be

$$V_{error} = V \cdot 2\pi f_{in} \tau \epsilon, \tag{3.18}$$

where V_{error} is the error voltage, V is the signal amplitude of a sine wave, τ is the RC time-constant of the assumed first-order system, and ϵ is the time-constant mismatch. This error voltage can be modelled as an offset and therefore can be corrected if it remains within the 1/2 LSB correction range of the stage. Note that the error voltage goes up with input frequency.

If a settling time of $10 \cdot \tau$ is assumed (for 15-bit settling), then $f_{in}\tau < 0.1$ for all input frequencies less than 40MHz (assumes 25nS settling time). Under this assumption, 3.18 can be rewritten with respect to ϵ as

$$\epsilon < \frac{0.5 \cdot LSB}{2\pi \cdot 0.1}. \tag{3.19}$$

For a 3.5 bit-per-stage system, the required ϵ matching for correction by digital redundancy is approximately 5%. This kind of matching cannot be achieved between different types of components, therefore it is necessary to use similar components in both sampling paths (i.e. matching an amplifier transconductance to MOSFET 'on'-resistance at the 5% level is not easily accomplished).

Further checking was done with SPICE simulation to verify the allowable offset in the real multi-order system. This was accomplished by measuring the difference between the continuous tracking of the sampling capacitors to an input signal.

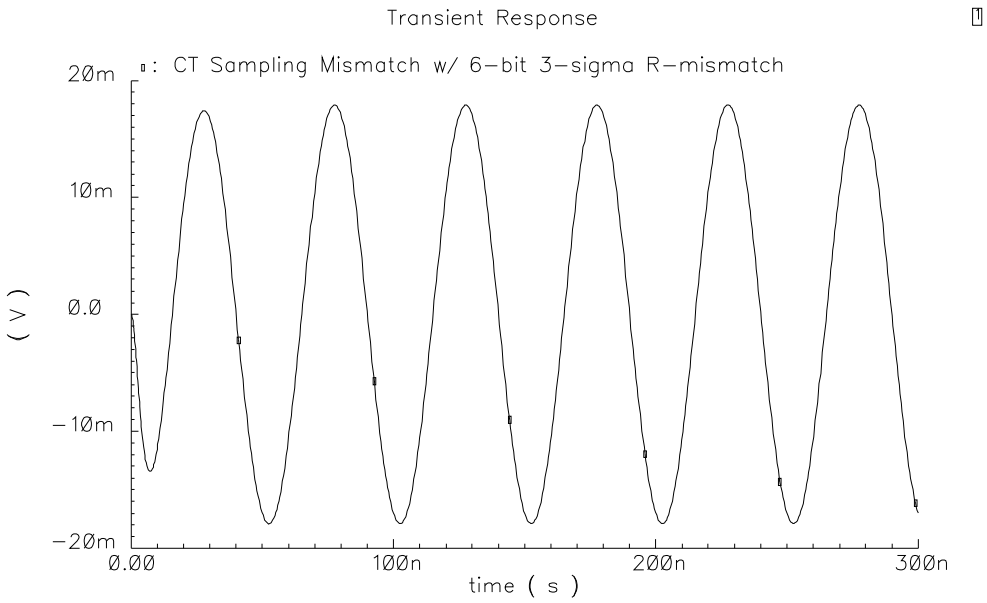

Figure 3.16: Continuous-Time Sampling Mismatch at 20MHz

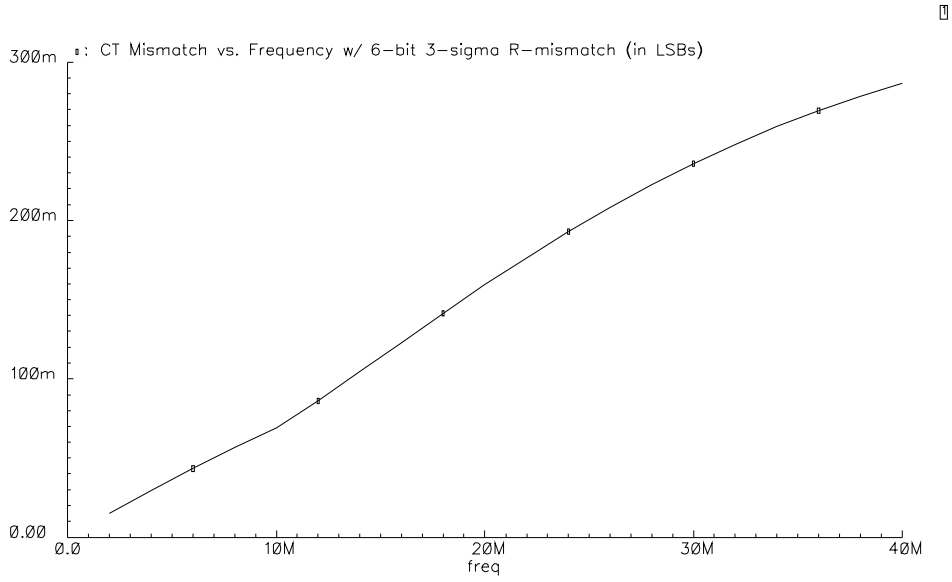

Figure 3.17: Continuous-Time Sampling Mismatch vs. Frequency

Figure 3.16 shows the continuous tracking error given a 6-bit, 3-sigma mismatch (4.69%) in τ, and an input frequency of 20MHz. The resulting continuous time sampling mismatch is 18mV – for a 1.8V input signal with 4 bits resolved on that stage,

the error is equivalent to 0.16 LSB. The simulation was repeated for multiple frequencies and the mismatch was shown to increase with frequency as shown in Figure 3.17. Input frequencies of 40MHz or higher could probably be tolerated if 6-bit τ matching is achieved.

Simulation of the charge injection of the sampling switches onto the sampling capacitors shows only a small (< 0.05 LSB) voltage change on the sampling capacitor. Mismatches between the two switches would therefore contribute less error than this amount and can be ignored for our purposes.

From calculation and simulation it can be determined that mismatch of the input circuit time-constant (τ) at the 6-bit, 3-sigma level is tolerable and can be corrected by digital correction (discussed in Chapter 2). This matching level is only achievable if similar devices are used in both the MDAC sampling path and the comparator sampling path (i.e. MOSFET - MOSFET or capacitor - capacitor).

3.3. Rail-to-Rail Input

The removal of the sample-and-hold circuit saves a lot of power and makes meeting the ENOB goal presented at the beginning of this chapter more approachable. Now that the S/H is no longer present in the signal path, the input voltage is no longer limited to the linear output range of an active stage. In fact, the only limitation on the signal is process voltage limitations – commonly the power supply voltages. The implementation of a true rail-to-rail (RTR) input is now possible.

This signal range is a great boost for economically achievable signal-to-noise ratio, and therefore will also help reach the ENOB goals presented in this thesis.

3.3.1. MDAC Redesign

This new input signal range requires a change in the first pipeline stage. The comparators must compare over the input signal range which is now the power supply, and the DAC portion of the MDAC must inject references equal to the supply rails during the amplification phase. This is equivalent to changing the stage reference voltage to be equal to the supply rails. The operation of the pipeline stage, with this change, is now the same as the classical pipeline stage.

Two-Reference Design

Classical pipeline stages require that the MDAC's active output stage drive signals to the reference voltage. For the architecture presented, this implies driving the output to the power supply rails (V_{REF2} for later reference). The amplifier responsible for creating the output level is not capable of driving to the supply rails accurately.

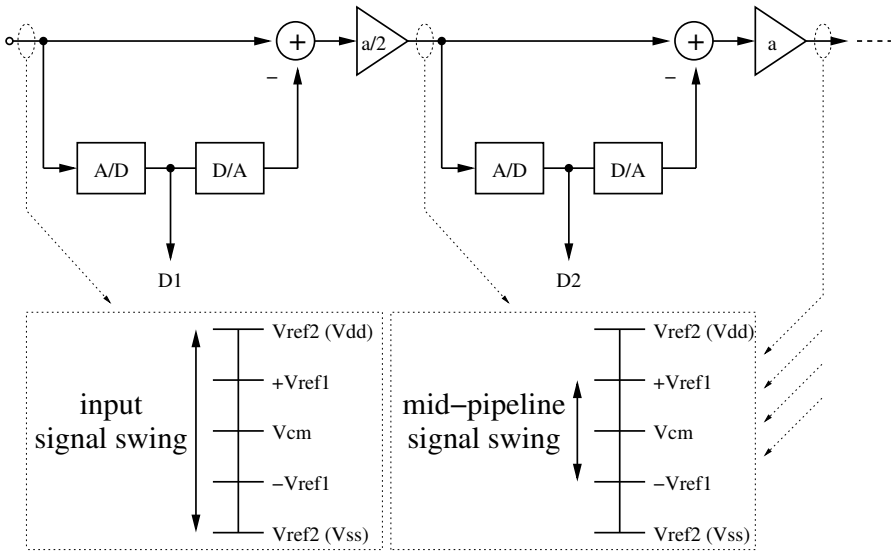

Figure 3.18: Two-Reference Pipeline Architecture

A simple solution to this problem is to reduce the MDAC gain from the standard 2^{n-1} to 2^{n-2}, where n is the number of bits resolved in the current stage. The remaining

pipeline stages would therefore have a reference voltage equal to one-half the power supply rails, or V_{REF1}. The final architecture is shown in Figure 3.18.

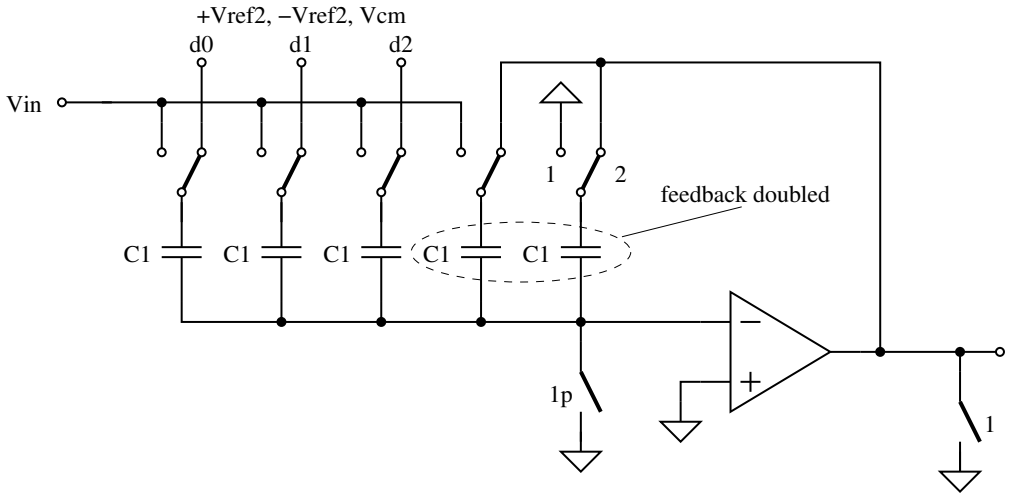

Figure 3.19: First Stage MDAC Redesign for Two-Reference Pipeline

The circuit implementation of this MDAC is very straightforward; the only change required is that the feedback capacitance must be doubled (Fig. 3.19). The reduced gain increases the contribution of noise from following stages, but as long as the stage resolution of the first stage is chosen to be large enough (more than 1.5 bits-per-stage), the first stage will still provide some help. One beneficial result of this architecture decision is that the feedback factor is increased, and therefore the required power consumption of the MDAC stage will be reduced.

An issue with this two-reference solution is the potential mismatch between the two references. If the references are not exactly 2x from each other, then there will be some gain error injected at the boundary between the two references. As discussed in Section 2.4.2, this will introduce a non-linear error in the overall conversion. A method for correcting this error will be discussed shortly.

One-Reference Design

A single-reference version of a rail-to-rail input Pipeline ADC could also be used to circumvent this problem; however, it requires some capacitor resizing to create the 2x variation in reference voltage between the first and remaining pipeline stages. This can be accomplished either with all stages operating with a V_{REF2} or a V_{REF1} reference voltage.

First, the V_{REF2} reference solution will be considered. The implementation of this solution requires no change to the standard MDAC structure of the first stage except for the half-gain. The remaining stages require some adjustment to their capacitance values to make the reference look like one-half of V_{REF2}.

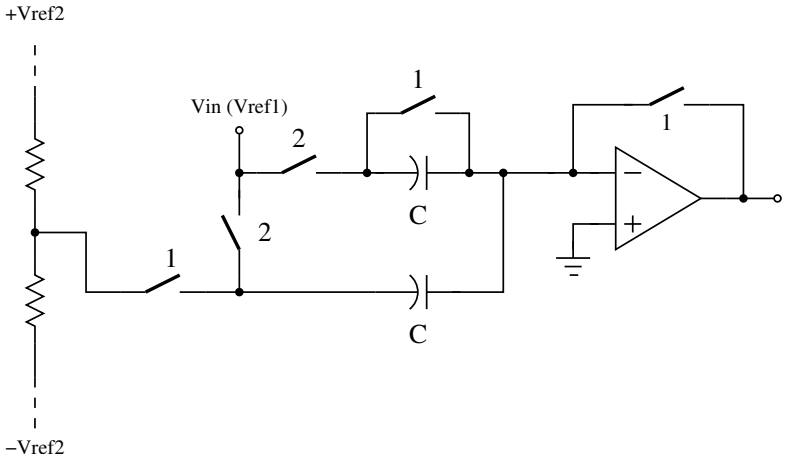

Figure 3.20: Comparator Design for Single-Reference Pipeline (V_{REF2})

The comparators for each of the remaining stages can be implemented with Input-Offset Sampling (IOS) [17]; additionally each comparator pre-samples the reference and starts comparing the input at the start of the sampling phase. This matches the most common method used for switched-capacitor comparators. The comparator for the single reference (V_{REF2}) solution does require an extra capacitor and switches to implement the charge summing accurately (Fig. 3.20). The extra capacitor connected in the sample

phase compensates for the 2x difference between the input signal swing and the resistor ladder reference voltages.

The MDAC in the remaining stages must also be changed to allow all references to be V_{REF2}. The DAC portion of the MDAC must employ 1/2 size capacitors so that the total charge subtracted from the signal remains equivalent to using V_{REF1}. A 2.5-bit implementation of this is shown in Figure 3.21.

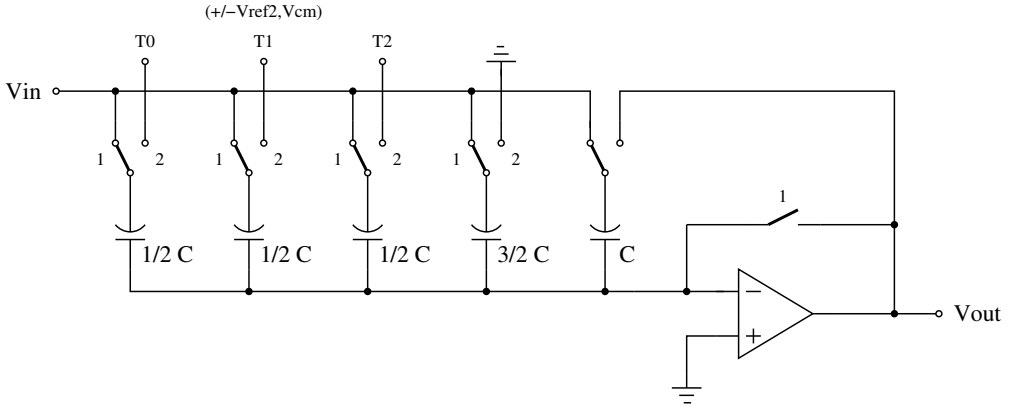

Figure 3.21: MDAC Design for Single-Reference Pipeline (V_{REF2})

The second single-reference solution is to use V_{REF1} as the only reference for the entire converter. In this solution, all of the stages after the first stage can be standard Pipeline ADC stages. The first stage must have similar adjustments made to it as was done for the remaining stages in the V_{REF2} single-reference solution.

The comparator on the first stage must have weighted capacitors similar to the other single-reference solution. Like the original S/H removal comparator block, the sampling in the comparator and MDAC must occur at the same time, necessitating a charge-summing structure. The reference ladder sampling capacitor must be 2x the signal sampling capacitor (Fig. 3.22) to account for the discrepancy between the signal range and the available reference voltage. The added capacitance will reduce the sampling accuracy between the MDAC sampling path and the comparator sampling path.

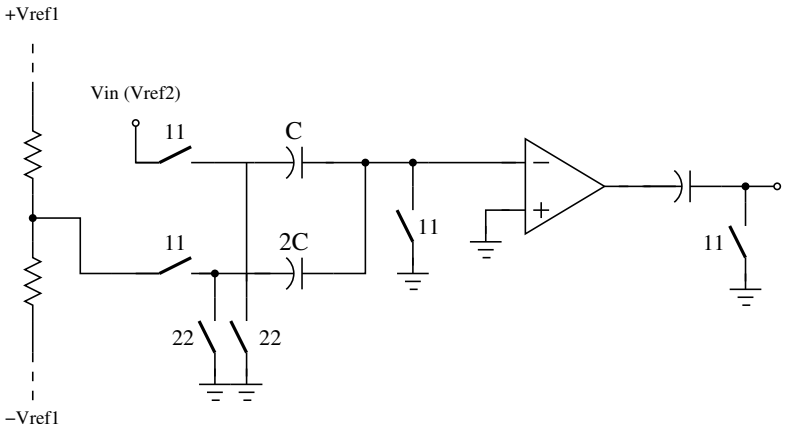

Figure 3.22: Comparator Design for Single-Reference Pipeline (V_{REF1})

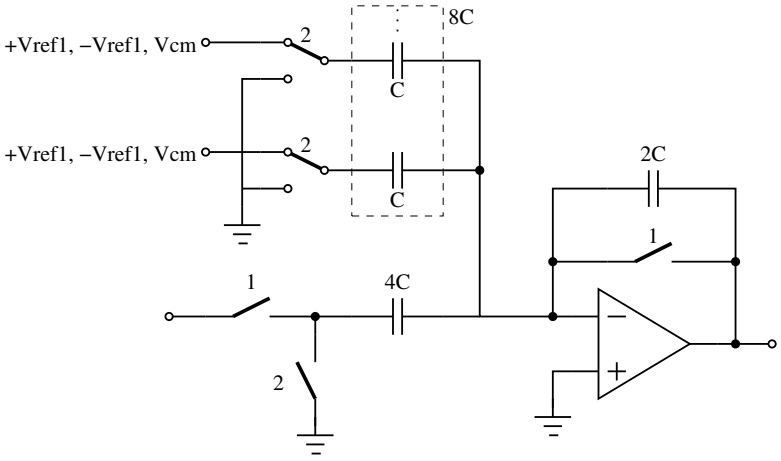

Figure 3.23: MDAC Design for Single-Reference Pipeline (V_{REF1})

The first stage MDAC must change similarly to the remaining stages for the V_{REF2} single-reference solution. The DAC capacitors in the MDAC must now be twice as large to subtract the equivalent of a signal with a V_{REF2} reference. This MDAC is shown in Figure 3.23. The added capacitance to the input of the amplifier reduces the feedback factor, requiring more power for the same speed. Furthermore, the extra capacitance also injects more charge noise into the signal than the simple two-reference version of the MDAC. An improvement to this design can be achieved if the sampling capacitors are reused in the DAC (Fig. 3.24); however, the feedback factor degradation and extra

charge-noise problems persist.

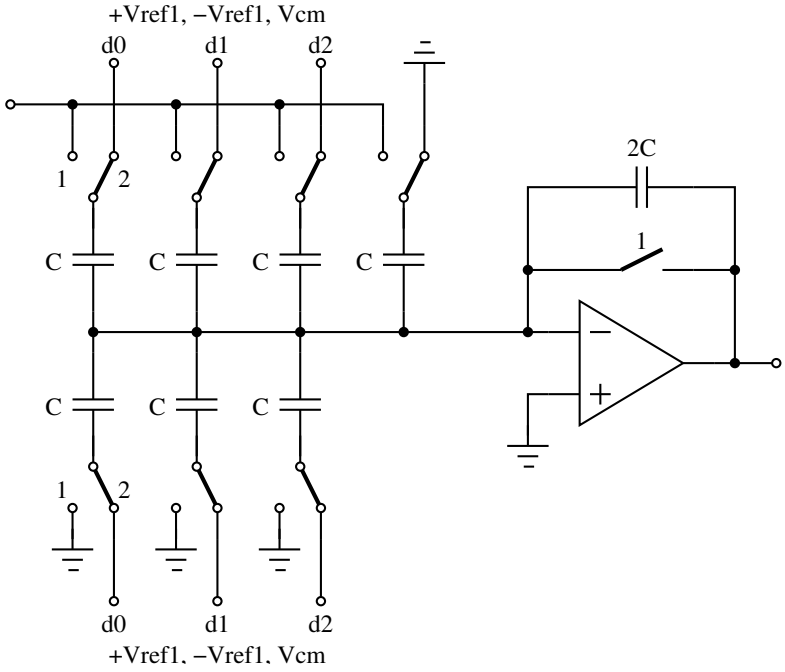

Figure 3.24: Better MDAC Design for Single-Reference Pipeline (V_{REF1})

Both single-reference solutions are possible, but only the V_{REF1} single-reference solution looks advantageous because it does not suffer from the kT/C and feedback factor penalty experienced in the V_{REF2} single-reference solution. In the end, the two-reference solution was chosen because of its simplicity and the possibility to calibrate other errors at the same time as the reference mismatch is calibrated.

3.3.2. Reference Calibration

It was previously mentioned that any mismatch between the two reference levels in the two-reference, rail-to-rail solution would cause non-linear error. Furthermore, this error is derived from a gain-type of error at the boundary between the first stage and the following stages.

As mentioned in Chapter 2, gain errors can be corrected by the use of a radix calibration scheme [37]. The correction is a two-step process: first, the actual radix must be determined, and second, the actual radix should be used to create the final value of the bits resolved. This is a computationally intensive step and often limits the use of this calibration method.

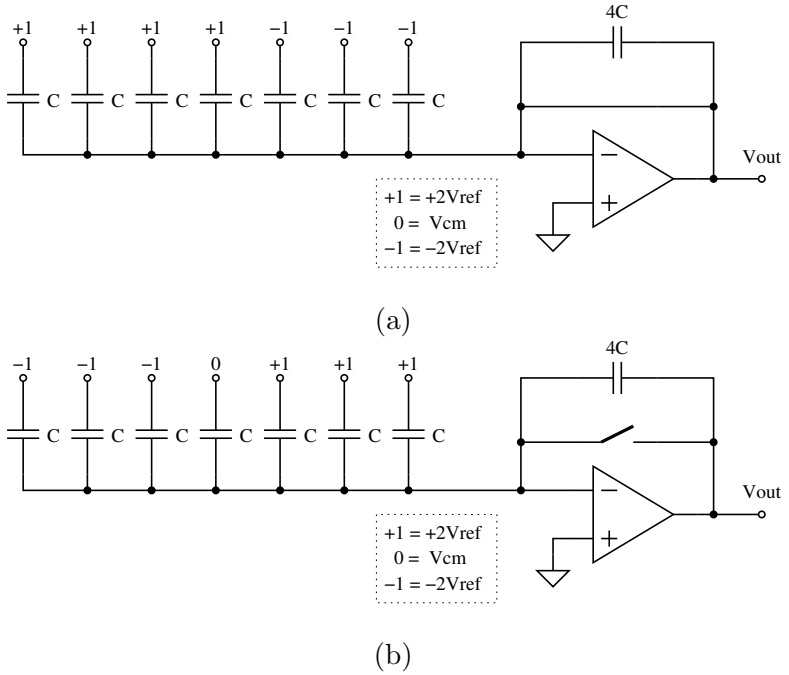

Figure 3.25: Reference Mismatch Extraction Circuit (Two Phases)

A circuit method for extracting the gain error is shown in Figure 3.25. It can be shown that any one-bit code increase from (a) to (b) will produce a voltage on the output equal to $(1/4)V_{REF2}$ (assuming an input range between +/- V_{REF2}). The equation describing the relationship between V_{REF1} and V_{REF2} is

$$V_{REF2} = \beta \cdot 2V_{REF1}, \tag{3.20}$$

where β is the gain error. Rewriting 3.20 with respect to β gives

$$\beta = \frac{V_{REF2}}{2V_{REF1}} = \frac{(1/4)\cdot V_{REF2}}{(1/2)\cdot V_{REF1}} = \frac{D_{HR}\cdot V_{REF1}}{(1/2)\cdot V_{REF1}} = 2\cdot D_{HR}, \tag{3.21}$$

where D_{HR} is the digital *half-reference* as computed by the remaining stages in the pipeline ADC. The value is computed with respect to the reference used in those stages, which is V_{REF1}.

The final value for beta (β) is extracted by averaging multiple measurements. A floating-point multiplier is then used to determine a correction code for each first stage code and is stored in a RAM memory using the first stage code as the address and the correction code as the stored value. This is a simple startup task for a system with an on-board processor that can divert resources for a startup calibration cycle.

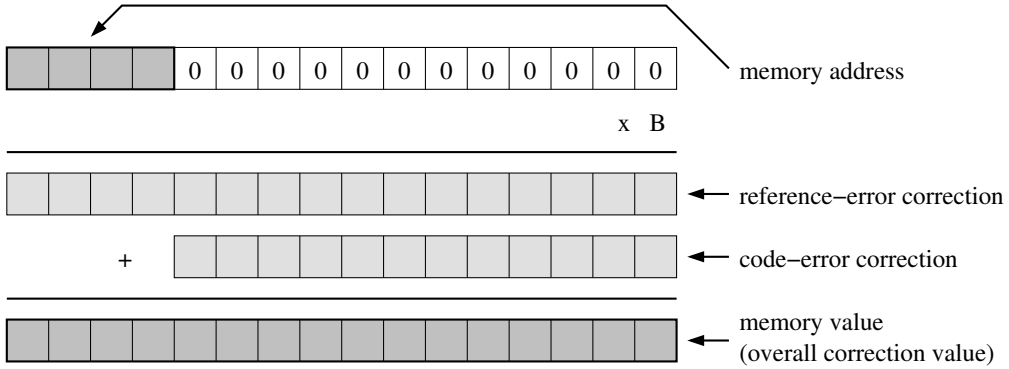

Figure 3.26: Generation of Correction Code

The reference mismatch measurement circuit is very similar to error extraction for code-error calibration [21]. This circuit could conceivably be used to perform a code-error calibration if it is required to compensate for capacitor mismatch in the first pipeline stage. Figure 3.26 shows how the error correction code could be determined and stored.

Figure 3.27 shows the simulated improvement in linearity performance of a Pipeline ADC with ∼0.7% reference mismatch and β measured with 13 bits of quantization (from the back end of the ADC).

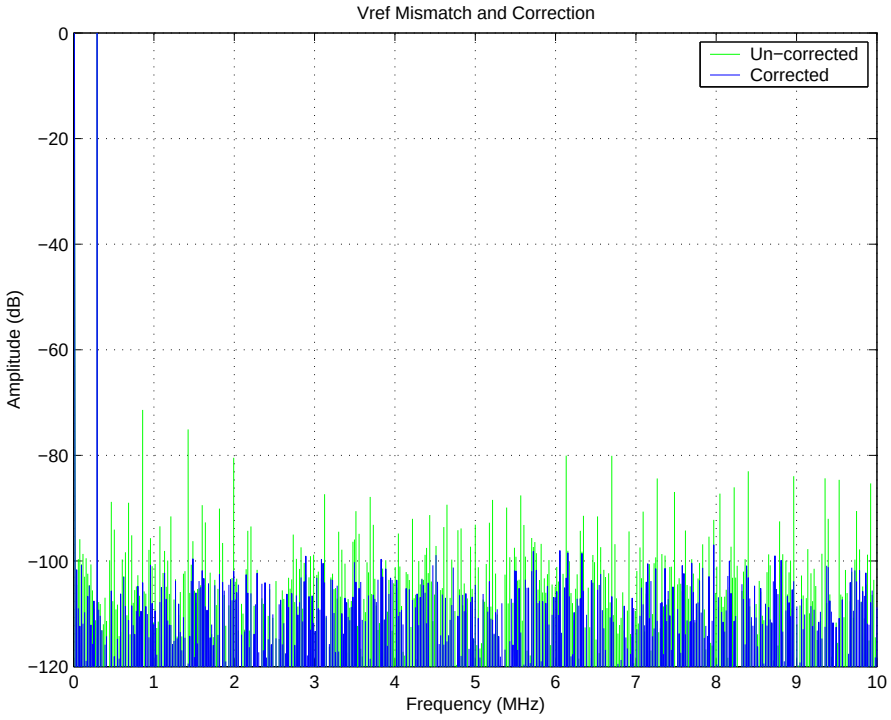

Figure 3.27: Matlab-Simulated Reference Mismatch Calibration FFTs

3.4. Pipeline Optimization

The decision of what architecture to use in a given Pipeline ADC design ultimately becomes an optimization problem. The variable quantities are per-stage resolution and inter-stage power and capacitor scaling. The constraint for this optimization is a defined noise performance, and the costs to be minimized are total area and power consumption.

3.4.1. Generalized Optimization

A basic optimization method for Pipeline ADC power was introduced by [42] wherein two different levels of optimization are discussed (zeroth order and first order). The basis of this optimization is to vary a taper factor that determines the rate at which the sampling capacitors are scaled down the pipeline in a Pipeline ADC. This was done

for several per-stage resolutions. The scaling is defined as

$$s = 2^{nx}, \tag{3.22}$$

where n is the per-stage-resolution and x is the taper factor.

The zeroth order optimization assumes that the load capacitance is dominated by the sampling capacitance of the current stage. This ignores the effect of feedback factor and loading of the following stage. The power is then assumed to be directly proportional to the the load capacitance.

The first-order optimization takes into consideration both the feedback factor and the following stage's load capacitance when computing the total load. As in the zeroth-order optimization, the power is assumed to be directly proportional to the load capacitance.

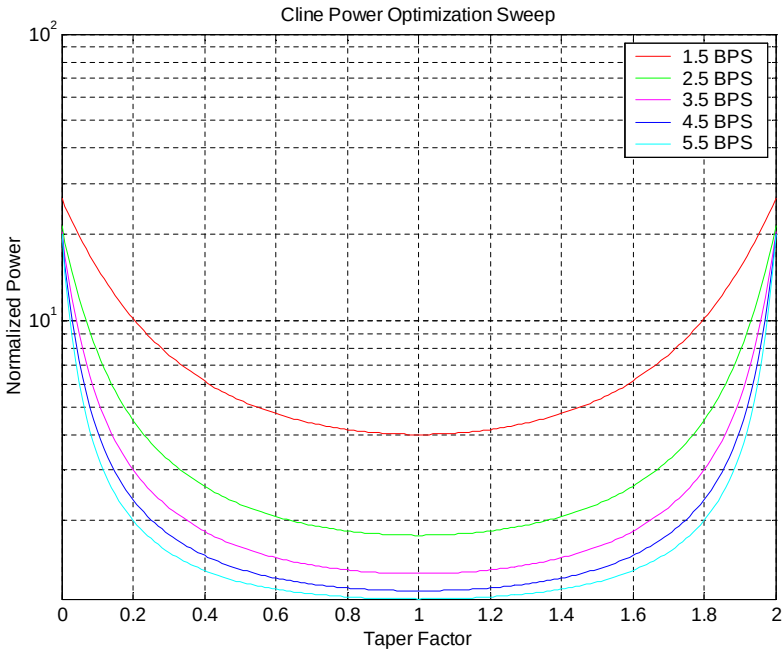

Figure 3.28: Zeroth-Order Optimization Curves

Both optimization levels were built into Matlab scripts and the optimization curves

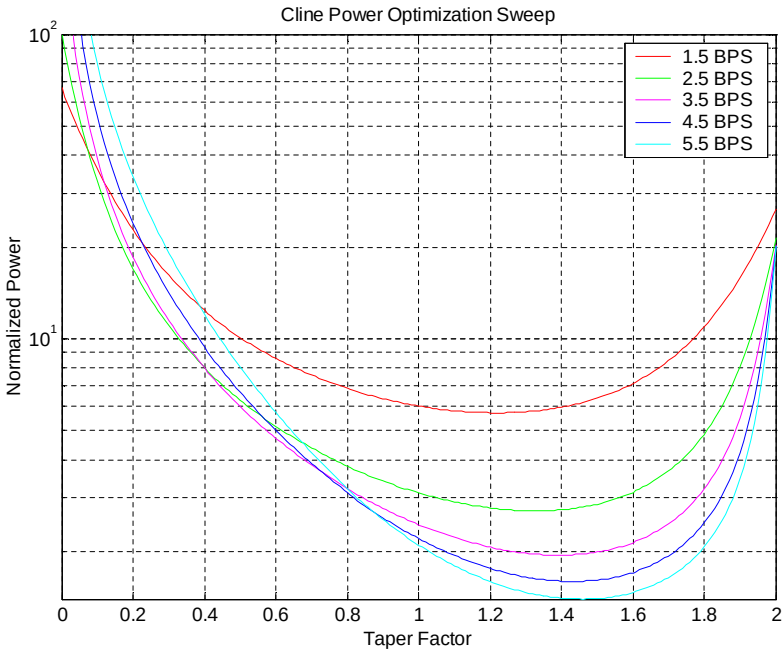

Figure 3.29: First Order Optimization Curves

for both are shown in Figures 3.28 and 3.29. These match the curves shown in [42]. It should be noted that neither optimization considers the power consumption of the comparator, which was previously noted to play a major role in how many bits-per-stage is reasonable for a given design. Additionally, these optimizations assume a large number of stages and the capacitors in the final stages are arbitrarily small, which is not possible in a real design.

3.4.2. Design-Specific Optimization

The taper-factor optimization method was applied to the design structure adopted in this work. That is, a two-reference Pipeline ADC design incorporating a half-gain MDAC in the first pipeline state with an ENOB of 14 bits at 20 MSPS and at least 15 bits converted.

Power was calculated from the required tail current of the input pair of the MDAC

opamp to reach the settling requirement on the output of each MDAC stage. Also included in the power calculation is an estimate of comparator power consumption that changes with the bits resolved per-stage.

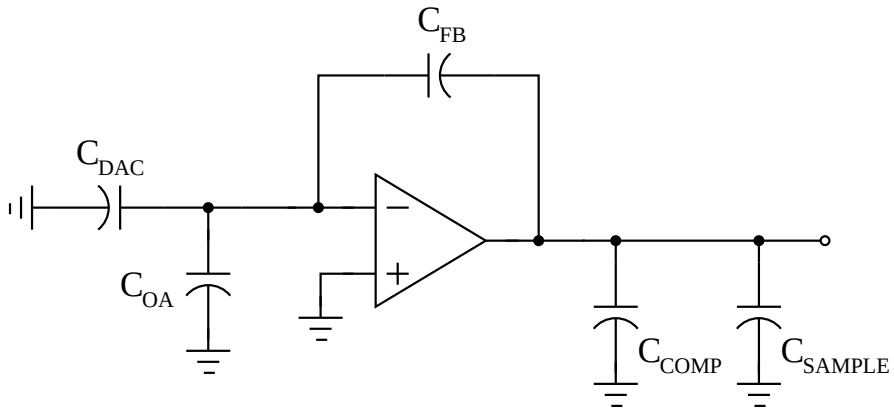

Figure 3.30: MDAC Optimization Model

Capacitance load and feedback factor for each MDAC opamp is calculated based on the model in Figure 3.30. This results in the following equations:

$$C_L = C_{COMP} + C_{SAMPLE} + C_{FB}||(C_{OA} + C_{DAC}) \tag{3.23}$$

$$\beta = \frac{C_{FB}}{C_{DAC} + C_{OA} + C_{FB}} \tag{3.24}$$

where C_{DAC} is the current stage's input sampling capacitance and DAC subtraction capacitance, C_{OA} is the opamp parasitic input capacitance, C_{FB} is the feedback capacitance that determines the gain during the amplification phase of the MDAC, C_{COMP} is the comparator input capacitance, and C_{SAMPLE} is the following stage's input sampling capacitance.

The opamp input capacitance and the comparator capacitor capacitance are estimated based on initial circuit designs. The opamp input capacitance is directly scaled with main capacitance scaling, and the comparator capacitance is scaled with stage-

resolution assuming a unit input capacitance for each comparator.

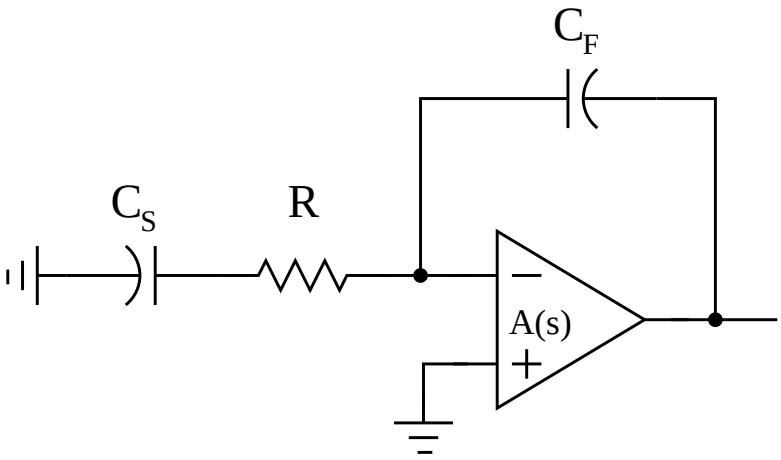

Figure 3.31: "Real" MDAC Settling System

The allowable settling time is 22nS (half-clock phases at 20 MSPS plus some non-overlap time.) The required bandwidth of an opamp is often calculated based on a single-pole system assumption where $t_{settle} = x \cdot \tau = x \cdot \omega_t \beta$. Examination of the "real" system shows a finite resistance between the sampling capacitance and the virtual ground node as shown in Figure 3.31. The transfer function becomes

$$H(s) = \frac{C_S \omega_p Ao}{s^2(RC_S C_F) + s(C_S + C_F + RC_S C_F \omega_p(1 + Ao)) + (C_F \omega_p(1 + Ao))}, \quad (3.25)$$

where $A(s) = Ao/(1 + s/\omega_p)$.

It can be seen that the inclusion of a non-negligible R adds another pole to the system. This slows down the step-response of the system. The extra pole can be simulated, and was done so for this work. It was determined that padding the required UGBW by 20% would assure good settling and allow a simple model for the purposes of the optimization.

The noise cost calculation is simple and results in the following equation for output noise:

$$\overline{v}_n^2 = \frac{4kT}{\beta C_F}, \tag{3.26}$$

where C_F is the feedback capacitance and β is the feedback factor of the MDAC amplifier system.

The number of bits resolved per-stage were swept from 1.5 to 5.5 and the taper factor was swept from 0 to 2 for each of the per-stage resolution settings. Power dissipation for each stage and total capacitance in the pipeline were logged for each of the bits-per-stage and scaling data points. The final result of the optimization is shown in Figures 3.32 and 3.33. The first figure shows the optimum taper factor for each per-stage resolution for noise performance, while the second figure shows the optimum taper factor for total capacitance at each per-stage resolution.

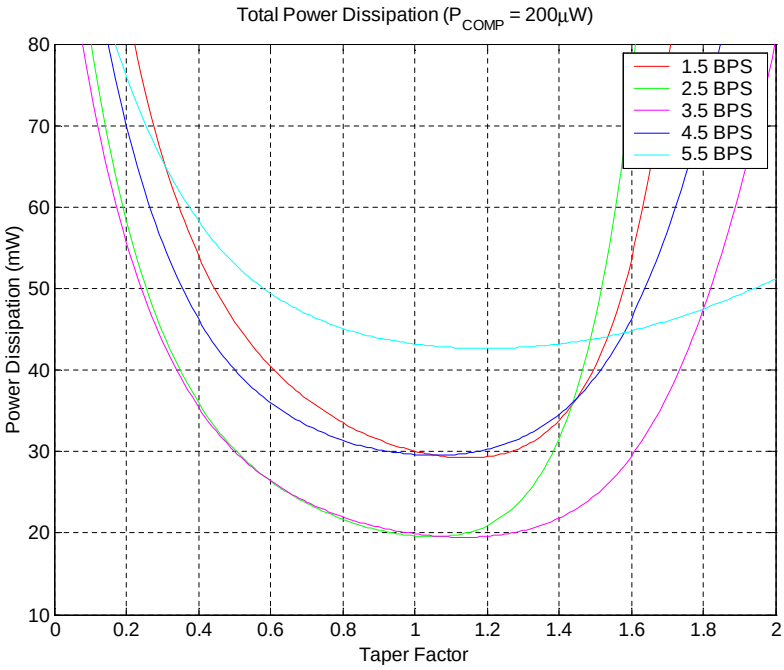

Figure 3.32: Pipeline Power Optimization Curve

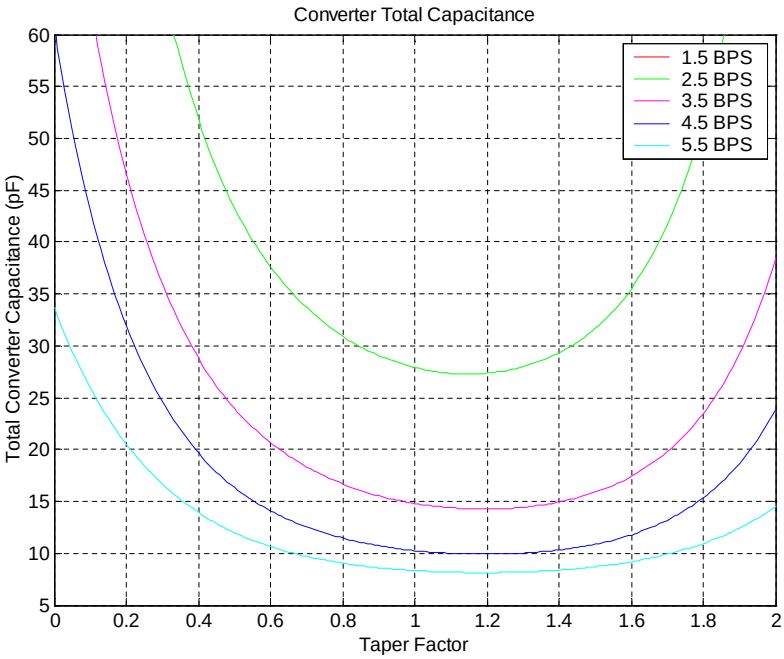

Figure 3.33: Pipeline Capacitance Area Optimization Curve

3.5. Final System Design Strategy

It has been shown that there are many things to consider in designing a high-resolution Pipeline ADC efficiently. The most fundamental of these is the distribution of bits to-be-resolved in each stage and the power and sampling-capacitor scaling. Additionally, two major design concepts to boost the efficiency of the Pipeline design were considered – both significantly improving the achievable performance of the pipeline.

3.5.1. Architecture

Based on the consideration of these concepts, a final architecture was chosen to meet the 14-bit ENOB at 20 MSPS. This architecture includes an initial conversion stage capable of handling rail-to-rail continuous-time signals. In addition, this stage incorporates a MDAC with half of the normal MDAC gain to allow two reference domains

in the pipeline. Finally there is calibration scheme for correcting reference mismatch.

The stage resolutions were chosen to be 3.5 bits-per-stage with a 1.1 taper factor. Matlab simulation is Section 3.4 shows this to be a good solution for an efficient Pipeline ADC design (in both power and area).

3.5.2. Noise Budgeting

Before actual circuit design can be started, the unit capacitors for each pipeline stage must be determined. This can be calculated based on the desired SNR (kT/C noise contribution) and taper factor. The allowable pipeline input-referred noise contribution for kT/C thermal noise must be calculated. The first step is to calculation the SNR ratio. The ratio is calculated at the output of the first stage because the output noise is a more practical noise measure to connect with the optimization scheme used for Section 3.4. The signal-to-noise ratio at this point should be three bits less than the overall pipeline SNR (these bits are already resolved in the first stage with no redundancy). This is given by

$$SNR = 6.02dB(11) = 66.22dB; \tag{3.27}$$

the value was rounded up to 67dB for convenience and converted to a "Voltage" measure

$$SNR = 67dB = 5.012 \times 10^6. \tag{3.28}$$

Next the input signal power should be calculated:

$$\sigma_u^2 = \frac{(FS/2)^2}{2} = \frac{0.9^2}{2} = 0.405 \tag{3.29}$$

where FS is the maximum differential signal swing at this point in the circuit. The combination of (3.28) and (3.29) results in the following equation for allowable noise referred to the output of the first stage:

$$\frac{\sigma_u^2}{\sigma_n^2} = SNR \Longrightarrow \sigma_n^2 = \frac{\sigma_u^2}{SNR} = \frac{0.405}{5.012 \times 10^6} = 80,800(\mu V)^2 = 284\mu V - rms. \quad (3.30)$$

The noise signal (σ_n^2) is composed of several noise sources including jitter noise, active circuit noise, and kT/C sampled thermal noise. It is expected that the kT/C thermal noise will dominate the error in this design, therefore a conservative 50% budget was chosen for the kT/C thermal noise within the allowable noise. This results in a total noise voltage allowable of $40,400$ $(\mu V)^2$ or 201μV-rms at the output of the first stage.

This value was applied to the final architecture with a taper factor of 1.1 from one stage to the stage immediately following, across all stages.

STAGE	Ceq	NOISEout	Cunit	Cfb	Cs
1	484 fF	185 μV-rms	1.1 pF	2.2 pF	8.8 pF
2	49.2 fF	580 μV-rms	0.4 pF	0.4 pF	3.2 pF
3	13.5 fF	1151 μV-rms	0.1 pF	0.1 pF	0.8 pF
4	13.5 fF	1151 μV-rms	0.1 pF	0.1 pF	0.8 pF

Table 3.1: Noise and Capacitor Stage Distribution

Table 3.1 shows the choice of sampling capacitor and noise contributed at each stages' output node, where 'Ceq' is equal to $\beta \cdot C_F$. The output noise can be calculated as

$$\overline{v}_{n(kT/C)}^2 = \frac{4kT}{Ceq}, \quad (3.31)$$

where the '4' kT multiplier is derived as 2x from the summing of noise between two phases and another 2x from the summing of the positive and negative differential path. The total first-stage output referred kT/C noise is 199.5μV-rms.

This stage structure is the starting point of the circuit design in the next chapter. The per-stage resolution and capacitor sizes serve to constrain the circuit design to a simpler set of solutions and set many circuit design specifications. These include

open-loop gain, feedback factor, and capacitive load as well as digital specifications for designing the calibration measurement control circuits and digital correction circuitry.

CHAPTER 4. DESIGN IMPLEMENTATION

In the previous chapter a system architecture was chosen. This decision was based on various power and area optimization considerations. The final result was a two-reference Pipeline ADC with 3.5 bits per-stage.

The first stage is the most important stage in the design. The remaining stages see the input after it has experienced a fair amount of gain and after some of the signal has already been resolved; therefore, the requirements on the back-end stages will be much lower than the first stage's requirements.

Some of the specifications that the first stage must meet are: low-noise ($\sim$180μV-rms at the output, from all noise sources), >15 bits linearity sampling, >12 bits linearity at the output, >14 bit settling during sampling, and >11 bit settling on the output. The sampled, thermal noise portion of the overall noise has already been accounted for with the optimization in the previous chapter. The linearity is a function of the linearity of the components and open-loop amplifier gain. Settling time is determined by the pole locations within the circuits and can be determined by RC-networks as well as opamp bandwidth and stability.

4.1. First Stage Sampling

In Chapter 3, the matching of both sampling paths is discussed in detail; however, the linearity requirements of the input sampling were not discussed. Furthermore, the impact of rail-to-rail input on the input sampling circuits was not covered.

4.1.1. Switch Linearity

The linearity requirements of the sampling circuit are determined by the the overall desired linearity. The first stage sampling linearity must therefore be better than the overall desired linearity. For a 14-bit ENOB Pipeline ADC it is desirable that the linearity be at least 15 bits. This allows the noise component of the ENOB measurement to be dominant. Additionally, if the linearity requirement is met for the entire system, then the DNL and INL should also be at least 15 bits.

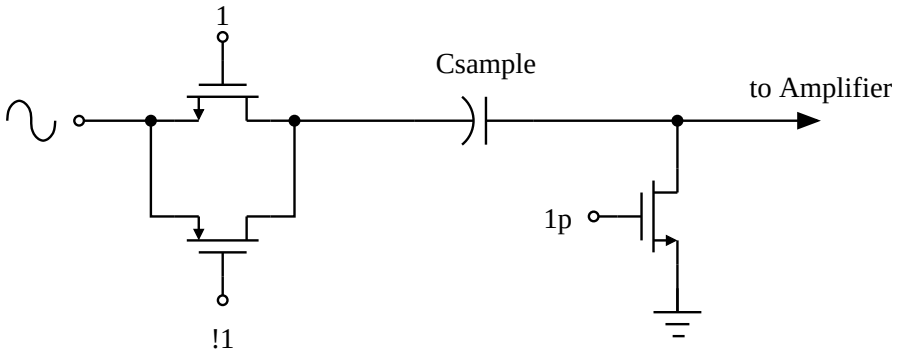

Figure 4.1: Input Sampling with CMOS Switch

A common implementation of a switched-capacitor input sampling circuit is shown in Figure 4.1. The "floating" CMOS switch (or transmission gate) passes signals anywhere in the range from the positive power supply to the negative power supply. This switch experiences a signal-dependant change in resistance from the transistor "on resistance" dependency on gate-source voltage

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}, \tag{4.1}$$

where $\mu_n C_{ox}$ is a device constant, W and L are the physical dimensions of the MOSFET channel, and $(V_{GS} - V_{TH})$ is the MOSFET overdrive voltage.

This signal-dependant resistance makes the sampled voltage on the input-sampling

capacitor non-linear. The effects of this can be greatly reduced if the resistance contributions of the PMOS and NMOS transistors are balanced. This improves the linearity because signals near the positive power supply experience similar resistance from the CMOS switch as signals near the negative power supply. To accomplish this balance, usually the PMOS device needs to be 2 to 3 times larger that the NMOS device. Linearities achievable in the available 0.18um CMOS process with CMOS switches are on the order of 10 bits (Fig. 4.2).

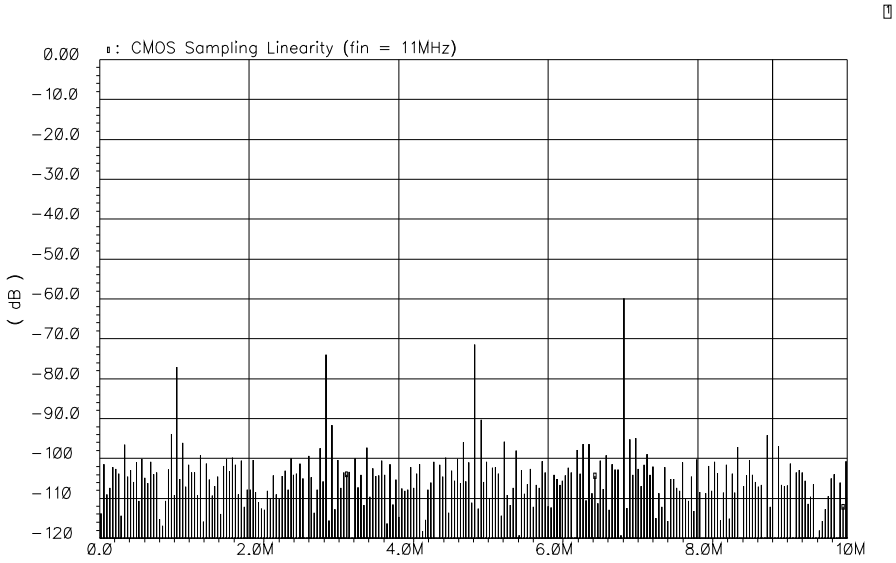

Figure 4.2: CMOS Switch Sampling Linearity

4.1.2. Bootstrapping

The sampling linearity can be greatly improved if the gate-source voltage is held constant for all input signals. A simple example of this would be to place a voltage source between the input (source) and gate of an NMOS switch. Ideal voltage sources are generally not within an IC design, therefore capacitors are often used as a replacement for the voltage source. A sampling system incorporating a simplistic version of bootstrapping

is shown in Figure 4.3.

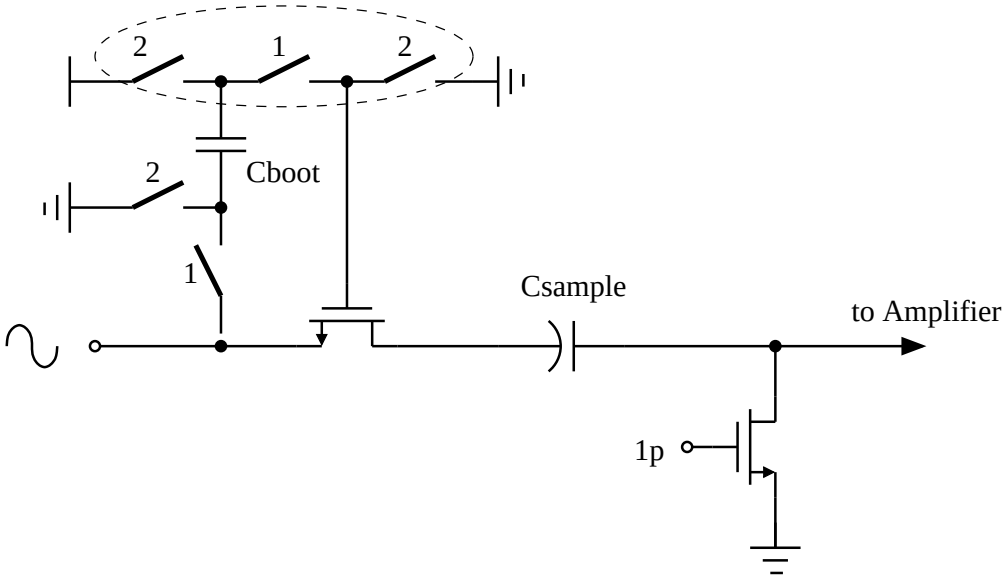

Figure 4.3: Input Sampling with Bootstrapped NMOS Switch

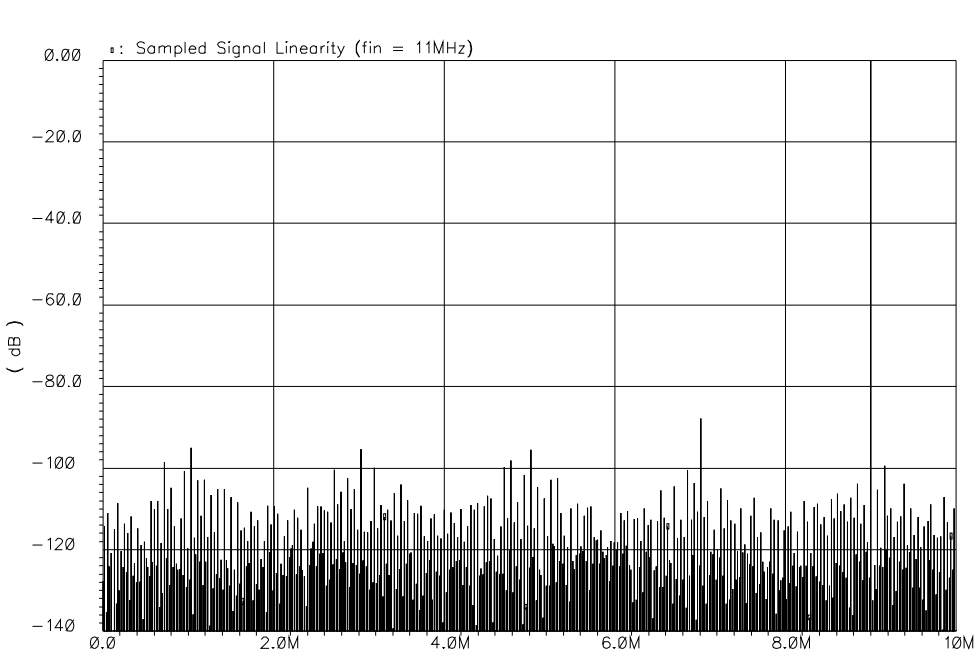

Figure 4.4: Bootstrapped NMOS Switch Sampling Linearity

One of the major difficulties with bootstrapping clock circuits is keeping all transistors from experiencing voltages greater than the power supply. For example, the switches on the gate of the NMOS switch (circled) would experience source-bulk and drain-source voltages greater than the power supply. A popular circuit used to circumvent this problem was introduced by Dessouky [29] and is used in this work as well. Linearities of about 15 bits can be achieved in the available 0.18um CMOS process with a bootstrapped NMOS switch. (Fig. 4.4).

4.2. MDAC Opamp

The first stage MDAC is the most difficult circuit block to design in this system. Not only does it need to meet stringent first-stage input and output linearity, settling, and noise requirements, but it also must deal with a rail-to-rail input, and sample a continuous-time signal.

The specifications that the opamp must meet are as follows:

- Open Loop Gain > 15 bits (90dB)
- Settling Accuracy > 12 bits
- Settling Time = ∼25nS
- Linear Output Range = 900mV single-ended

The large output range (900mV on a 1.8V supply) and high-speed requirements of the system make the folded-cascode opamp a natural choice for the MDAC operational amplifier. The folding provides maximum output range while maintaining the high-speed simplicity of a single-stage amplifier. An example of how this amplifier will be used in the MDAC is shown in Figure 4.5.

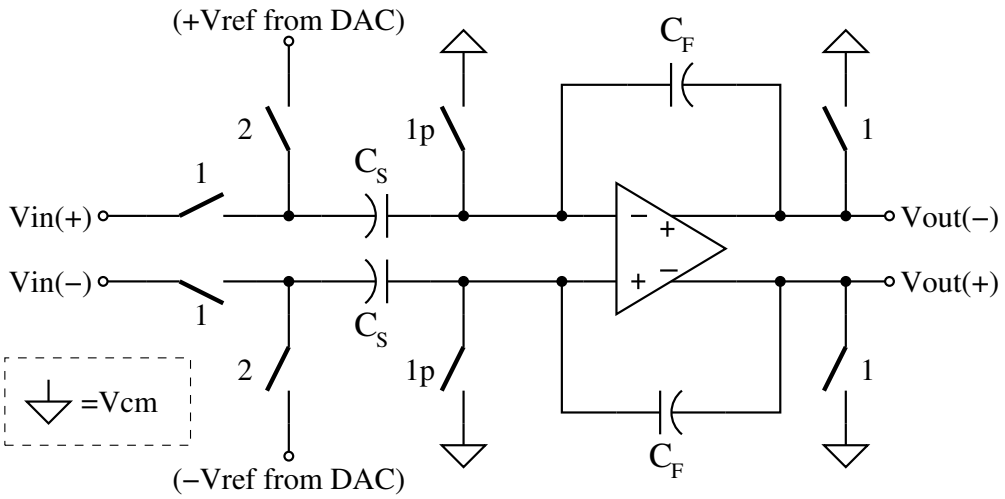

Figure 4.5: General MDAC Circuit

4.2.1. Gain Boosting

Achieving gains of greater than 80dB in a 2x "$g_m r_o$" stage (single cascode) in modern, short-channel transistor processes is often not possible. For the output range desired, multiple cascodes are not an option, and two-stage cascode or folded cascode amplifiers would still suffer from the speed penalties associated with compensating a two pole-system.

One useful technique in a situation such as this is *gain boosting* (also known as *active cascode*) [16]. The concept behind this technique is quite simple. An auxiliary amplifier is used to drive the gate of the second transistor in a cascode configuration (shown in Fig. 4.6). The amplifier forces the drain node of the first transistor to be steady with an accuracy inversely proportional to the open-loop gain of the amplifier. This is an extra effect in addition to the resistance boost that the cascode transistor provides.

The gain boosting can also be applied as a fully-differential amplifier. In this case, the output common mode control of the amplifier sets the bias voltage of the cascode transistor. The differential gain boosting technique was the approach taken in this work.

It was chosen for its ease of implementation and symmetry properties.

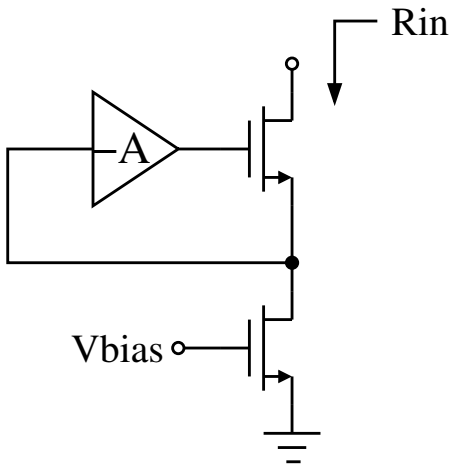

Figure 4.6: Active Cascode Example

One potential problem with the active cascode technique is the addition of a pole-zero doublet to the overall amplifier transfer function. This issue is discussed in [43]; in this work it is determined that the pole-zero doublet can be accommodated if a certain relationship between the amplifier poles is maintained. This is given as

$$\beta\omega_{ugbw-main} < \omega_{ugbw-boost} < \omega_{p2}, \tag{4.2}$$

where β is the feedback factor of the opamp system, $\omega_{ugbw-main}$ is the main amplifier unity-gain bandwidth, $\omega_{ugbw-boost}$ is the boost amplifier unity-gain bandwidth, and ω_{p2} is the main amplifier's second pole. The amplifier was designed to meet these requirements. This was verified by observing a transient step in the amplification phase configuration. The step response was stable and settled to $\sim$14 bits accuracy within the desired 25nS half-clock phase time.

4.2.2. Common-Mode Feedback

The common-mode feedback was handled in two different ways for this amplifier. First, in the main amplifier, a common switched-capacitor feedback system was employed (Fig. 4.7 [16]). This circuit uses a capacitive divider to determine the common-mode level of the amplifier and feedback is directly provided to the gate of a current source within the amplifier. Every non-amplifying phase, the capacitor charge is refreshed to keep the common-mode value from drifting.

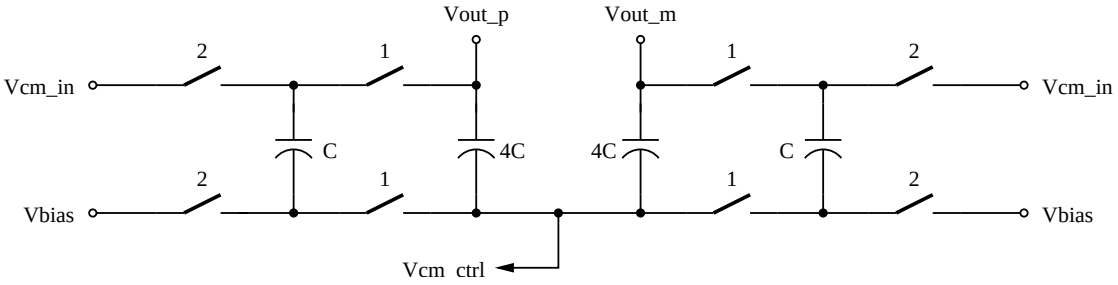

Figure 4.7: Switched-Capacitor Common-Mode Feedback Circuit

The second method of common-mode feedback employed in the amplifier is a linear-region MOSFET common-mode feedback [16]. This CMFB method is especially appropriate in systems with small output swing as the linear range of a MOSFET transistor is not very large. As such, the boost amplifiers are a perfect location for this kind of common-mode feedback. The outputs of the boost amplifiers only need to change slightly to maintain their gain-boosting operation.

4.2.3. Full Amplifier Architecture

The final architecture of the first stage MDAC amplifier is shown in Figure 4.8. Notice that gain-boosting is applied to both sets of cascode transistors. The common-

mode feedback control is applied to the NMOS current sources because changes in current through these devices only affect the output branch.

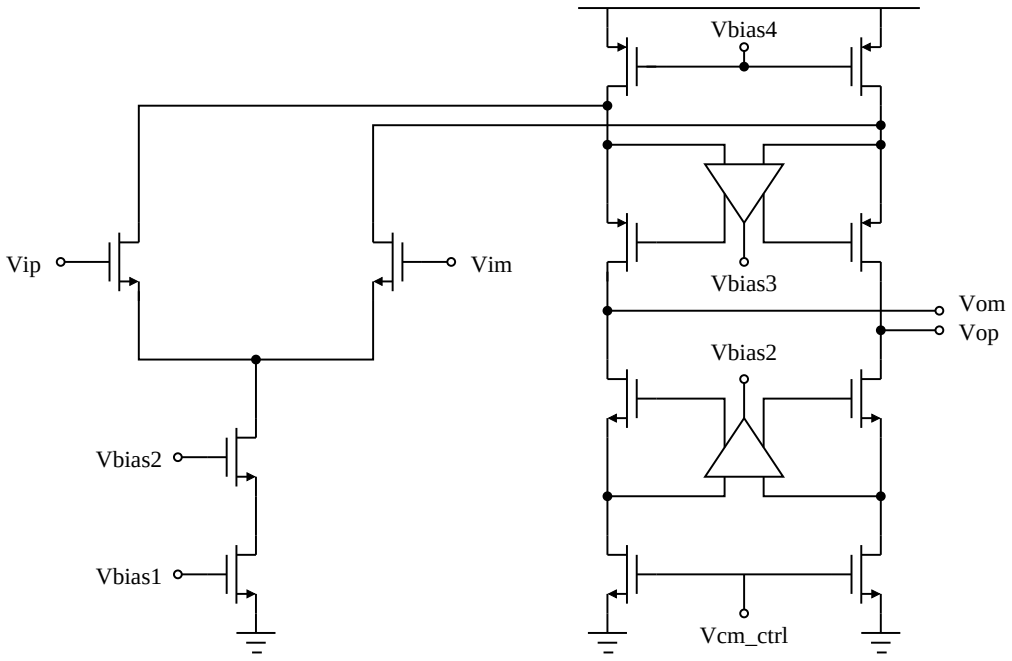

Figure 4.8: Top Level Opamp Circuit

The boost amplifiers were implemented as two opposite polarity folded-cascode, double-cascode amplifiers (NMOS input pair for the top amplifier (Fig. 4.9) and PMOS input pair for the bottom amplifier). The additional cascode is available because of the near-zero output swing required for the boost amplifiers. Additionally, minimal current was required for these amplifiers as the output load is only the gate capacitance of the main amplifier cascode devices.

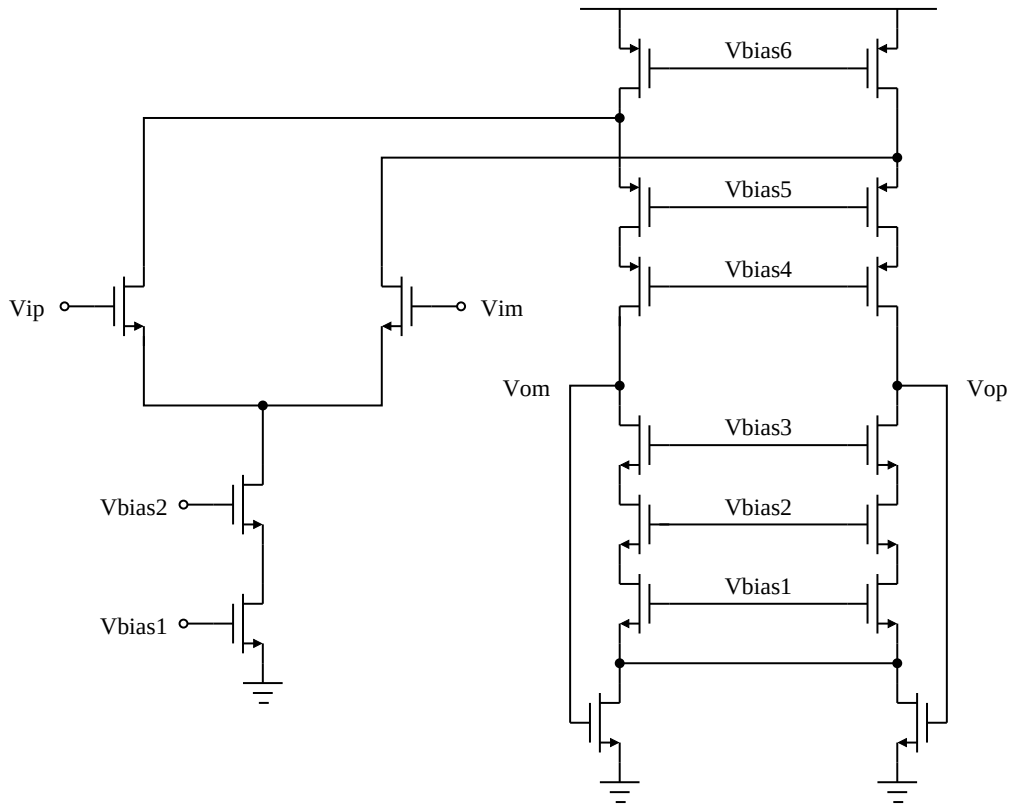

Figure 4.9: Gain-Boosting Amplifier (TOP)

4.2.4. Amplifier Linearity

The output linearity of the amplifier is an important specification that needs to be achieved. The amplifier provides linearity through its open-loop gain. The portion of the gain used in the feedback loop directly divides the non-linear components of the amplifier's gain; however, if the amplifier gain is not kept high enough over the entire expected output range, then the linearity of signals experiencing the full output range will suffer.

A common way of extrapolating the amplifier system linearity is to check the open-loop gain of the amplifier over the entire amplifier output range. If the output open loop gain stays higher than the desired input linearity over the entire output range, then the system linearity requirements should be met by the design. This was done for the

designed amplifier, and a plot of the gain over output range is shown in Figure 4.10.

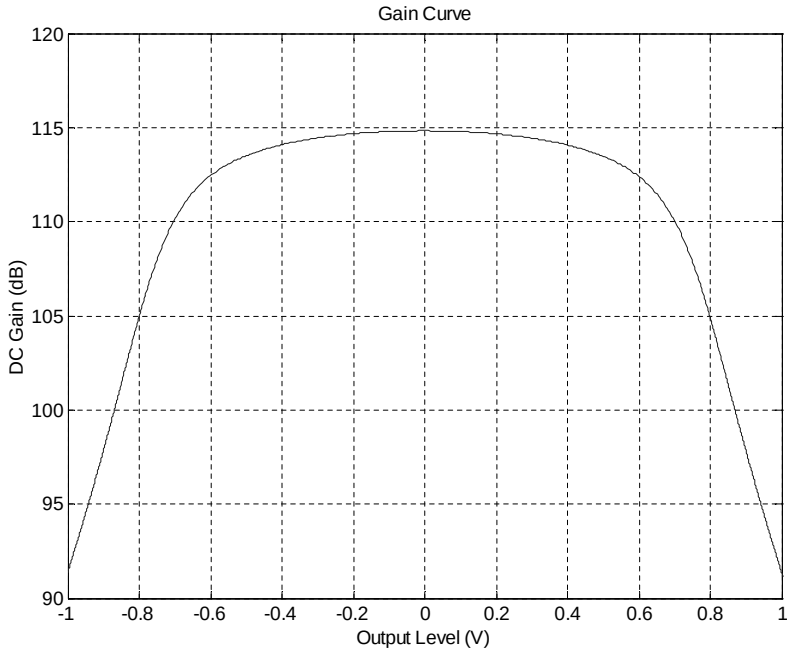

Figure 4.10: Open-Loop DC Gain Over Output Range

A more rigorous method of determining the linearity of the system incorporating the designed amplifier is to extract the transfer function of the amplifier (linear and non-linear components) and apply a sine wave to the input. The resultant waveform can be examined for non-linear components and the output linearity of the amplifier can be determined.

This process was completed for the designed amplifier. The transfer function was extrapolated over many points (Fig. 4.11), and imported into Matlab. A polynomial function fit was done on the imported curve and a sine wave was applied to the resultant equation. The non-linear components were extracted from an FFT of the result and provided a Total Harmonic Distortion (THD) value for the range of output signal amplitude. The results of this analysis are shown in Figure 4.12. This shows that the THD (when divided by the open-loop gain) is more than sufficient for the output requirement of >12 bits linearity.

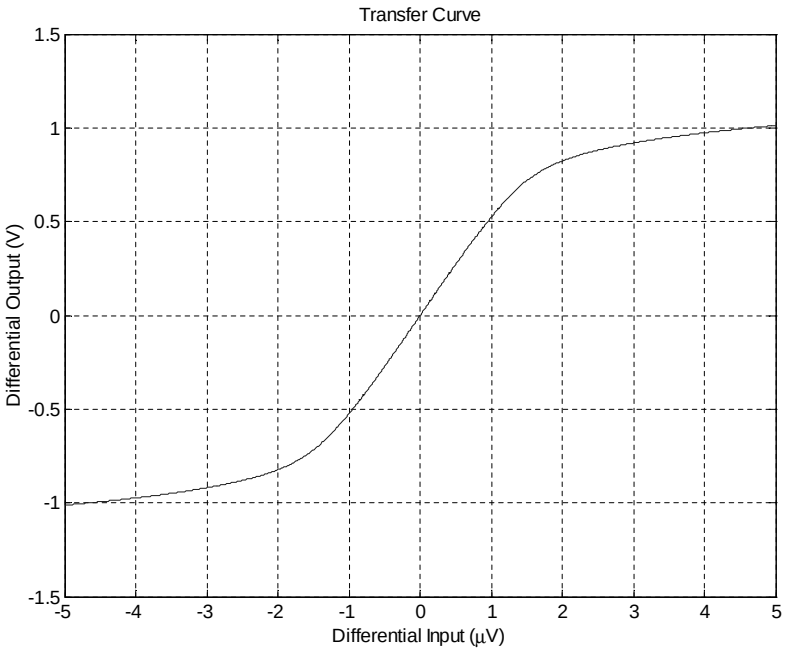

Figure 4.11: Amplifier DC Gain Curve

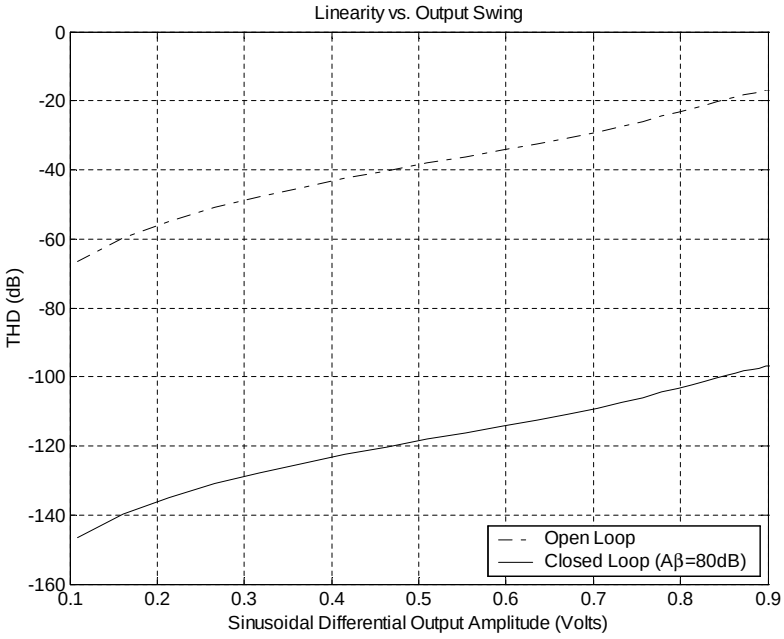

Figure 4.12: Total Harmonic Distortion (THD) vs. Output Range

A transient simulation was also completed in SPECTRE that measured the output linearity of a maximum-swing output signal with an input frequency of 11 MHz. It is important to note that the input frequency of the Matlab simulation is essentially DC, because the transfer curve is an extracted DC gain curve. The results show a better than 13-bit linearity at the output (Fig. 4.13). Examination of the transient signal with this setup also confirms the settling accuracy of ∼14 bits.

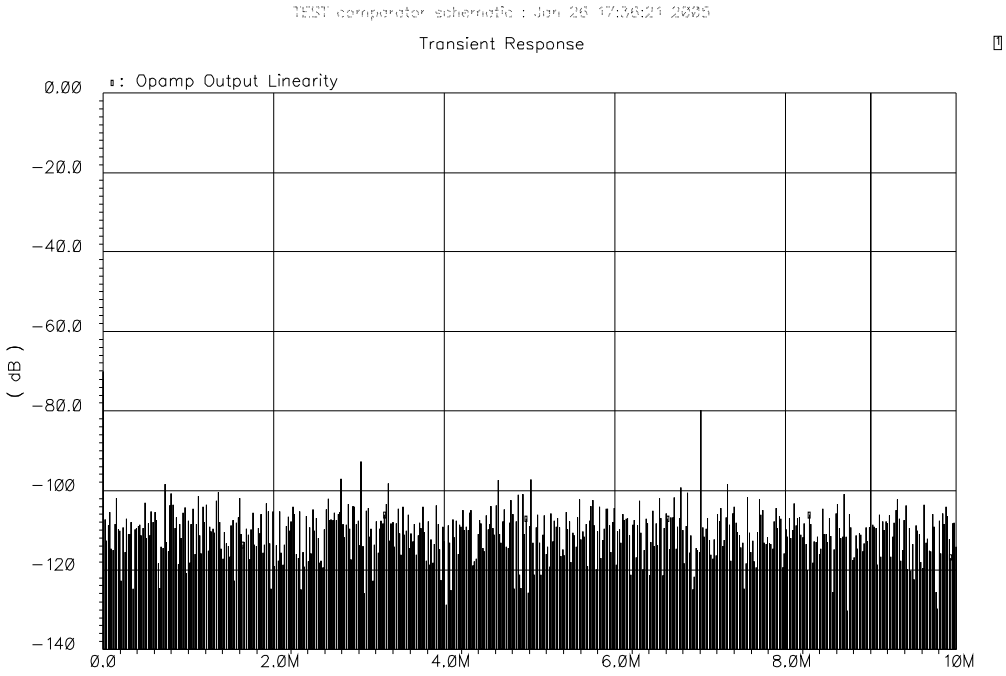

Figure 4.13: Opamp Output Linearity Simulation (SPECTRE)

4.2.5. Amplifier Noise

The noise of the amplifier should also be considered. The noise from the amplifier will add to the sampled kT/C thermal noise in the system and further degrade the system SNDR. The noise from other potential sources was included in the noise budgeting done in Section 3.5.2. The allowable budget for "other noises" at the output of the first

amplifier is $184\mu V$-rms.

Noise simulation in SPECTRE gives $151\mu V$-rms integrated noise over the whole noise band. (This wide integration bound is due to the sampling that will fold all noise frequencies into the fs/2 frequency band.)

4.3. Final MDAC System

The final MDAC implementation is shown in Figure 4.14. The input is differentially sampled on sixteen unit-sized capacitors (eight on each side) with the middle terminal held at the common mode of the input signal. There are four unit-sized capacitors on each side for feedback. Two of them are only used for the radix calibration β extraction operation.

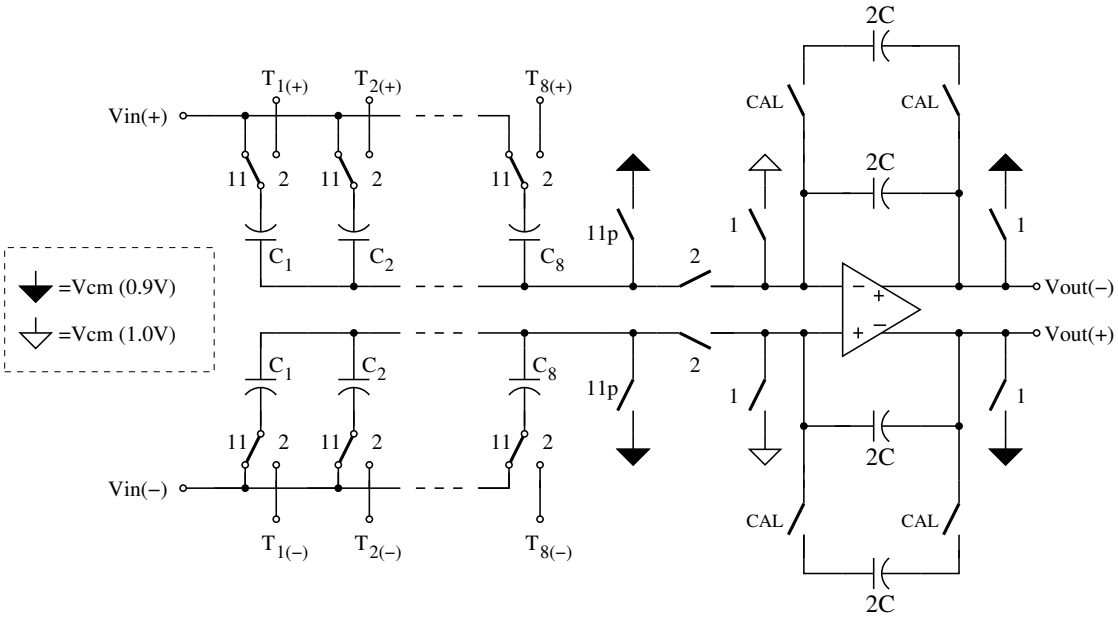

Figure 4.14: Final MDAC Implementation

The operation of the MDAC is as follows. During the first phase, the input is sampled on the sixteen input capacitors. This phase is also known as the *sampling phase*.

The opamp is isolated from the sampling operation, and has its inputs shorted together and outputs shorted together. During this phase, the switched-capacitor common-mode feedback within the main amplifier is also refreshed. The four non-calibration measurement feedback capacitors are also pre-charged to the difference between the input and output common mode of the amplifier; this keeps the input of the amplifier from experiencing a glitch when the MDAC switches to the next phase.

Before the end of the first phase, the comparator has resolved the first stage's bits and generated a reference code to be used in the next phase of the MDAC operation. During the next phase, called the *amplification phase*, the thermometer DAC codes are applied to the capacitor reference selection switches. This forces some charge to be added or subtracted from the signal, only allowing the unresolved signal to progress as charge to the feedback capacitors. The capacitor ratio determines the voltage gain experienced by the signal. The equation describing the function of the MDAC is

$$V_{out} = 4 \cdot V_{in} - d_i \cdot V_{REF2}, \tag{4.3}$$

where d_i is determined by the comparator output and can experience the values {-8/2, -7/2, -6/2, -5/2, -4/2, -3/2, -2/2, -1/2, 0, 1/2, 2/2, 3/2, 4/2, 5/2, 6/2, 7/2, 8/2}.

4.4. Comparator

The first stage comparator requires some specialized design to accommodate the special timing needed for continuous-time sampling within the first stage of the Pipeline. Additionally, an offset correction scheme is employed to allow for maximum sample mismatch correction by the digital redundancy of the pipeline architecture.

The comparator circuit is shown in Figure 4.15. During the first phase (phase 11), the input is sampled on one of the input capacitors while the appropriate reference is sampled on the the other input capacitor. The comparator sampling circuit is matched

to the MDAC sampling circuit but is 1/64 the size of the MDAC sampling circuit. Also, during this phase, the inputs of the pre-amplifier are shorted together. The pre-amplifier offset is sampled on the offset storage capacitor at the end of the first phase.

During the second phase (phase 22), the charge stored on the input sampling capacitors is averaged together. This signal is then applied differentially to the inputs of the pre-amplifier and amplified through the offset storage capacitors and applied to the inputs of the differential latch. After a short delay, the latch is allowed to regenerate, and the output value is available to the digital circuits that multiplex and buffer the signals before sending them to the MDAC DAC inputs for the start of the MDAC amplification phase.

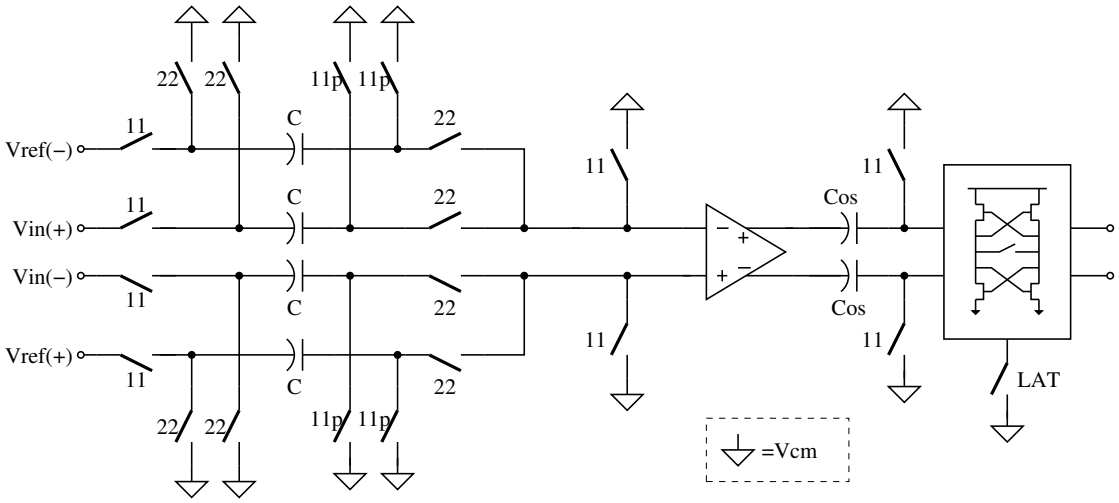

Figure 4.15: Top-Level Comparator Circuit

Simulation of the comparator verifies its operation. It can resolve 10mV (<0.1 LSB) comparison signals in 4nS (2nS for the pre-amp and 2nS for the latch regeneration).

4.4.1. Pre-Amplifier

The pre-amplifier is a simple single-stage amplifier with low current and moderate gain (Fig. 4.16). The common-mode feedback employed is the linear operation MOSFET feedback. Their operation is poor over a wide input range; however, this is of minimal importance as the most important comparator signals are the well-behaved, near-zero-differential signals.

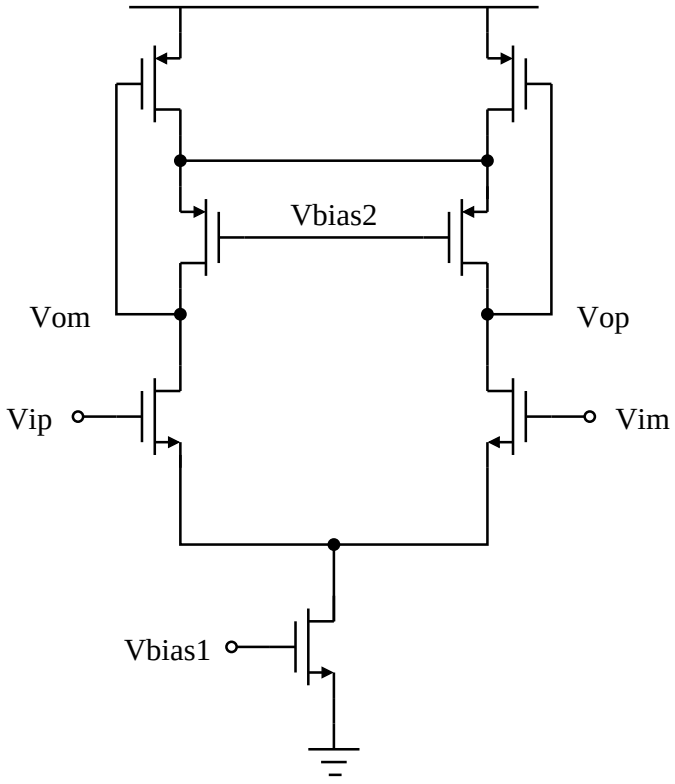

Figure 4.16: Comparator Pre-Amplifier

4.4.2. Latch

The latch is composed of two cross-coupled positive feedback transistors, current input PMOS transistors and a NMOS reset switch. The circuit is shown in Figure 4.17. The reset switch allows the inputs to start near mid-rail and not depend on a race from the supply rail to determine the latched value. This should reduce the effect of device mismatch within the comparator.

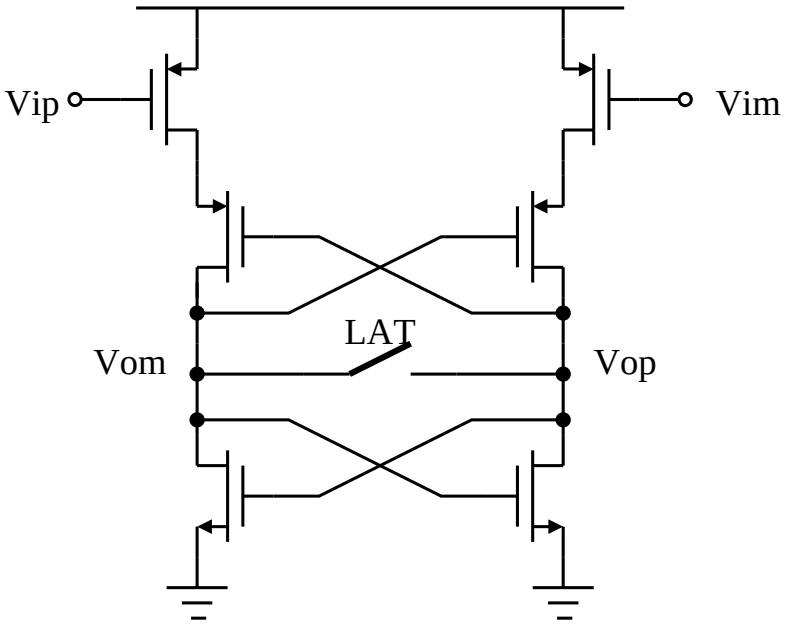

Figure 4.17: Differential Positive-Feedback Latch

The DC current within the latch before regeneration is set by the common mode input provided by the pre-amplifier. This value was chosen to be small ($\sim$50μA) so that the total power consumption of the comparator block within the Pipeline ADC would be minimal in comparison to the required bias currents in the MDAC opamp ($\sim$5mA). The pre-amplifier burns approximately 20μA. This gives a comparator array power consumption of 1.1mA.

4.5. Digital Circuits

The digital portion of the chip begins at the output of the comparator latch and ends at the switch selection circuitry that selects the references to be switched onto the MDAC DAC capacitors during the the amplification phase. There are a few digital circuit blocks needed for correct operation of the ADC. These include latches, bubble correction logic, and digital signal multiplexer.

4.5.1. S.R. Latch

The Set-Reset Latch is a simple digital circuit that stores digital information within the latch. The S.R. latch is constructed by connecting two cross-coupled NOR gates as shown in Figure 4.18. The function of this circuit is to drive the output Q to a high value whenever the *set* signal is asserted and drive Q to a low value whenever the the *reset* signal is asserted. Additionally, this signal is held until the opposite signal (set or reset) is asserted again. The operation of the circuit is summarized in Table 4.1.

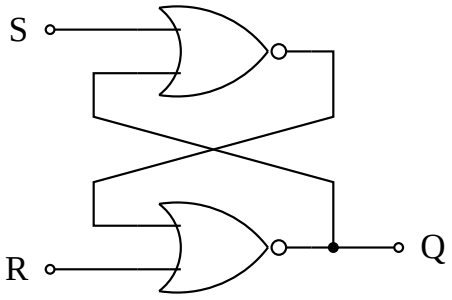

Figure 4.18: S.R. Latch Circuit

The S.R. latch is used to latch the digital data received by the differential latch at the output of each comparator. The rest stage of the differential latch circuit is such that

SR	Q
00	Q
01	0
10	1
11	0

Table 4.1: S.R. Latch Operation

it looks similar to a logical '00', which keeps the S.R. latch "latched" until the output changes to a '01' or '10'.

4.5.2. Bubble Correction

A bubble is an error artifact within thermometer code that occurs when comparison levels are not in order or when a single comparator is not operating correctly. The error is seen when the thermometer output code is not completely separated into one group of ones and one group of zeros.

A straight-forward method of detecting and fixing these errors is by comparing adjacent thermometer codes and by determining the actual code by a so-called "democratic" process. The more votes that occur for a '1' or a '0' determine the final code. An implementation of a three-input version of this type of bubble correction is shown in Figure 4.19 and Table 4.2 shows an example of the bubble correction's operation. This method can only correct for a single bubble code, but this should be enough for most cases.

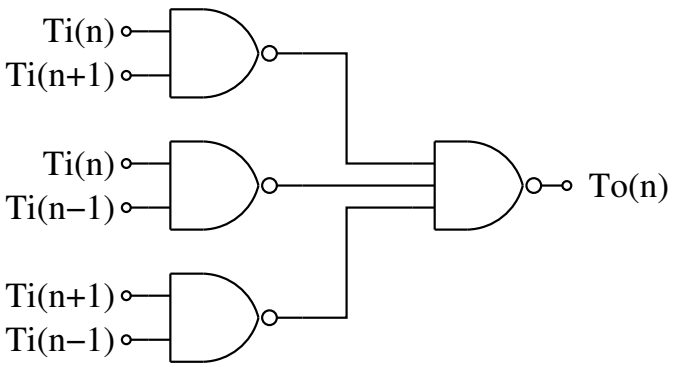

Figure 4.19: A Democratic Bubble Correction Implementation

COMP. OUT	CORRECTED
0	0
0	0
1	0
0	1
1	1
1	1

Table 4.2: Example of Bubble Correction Operation

4.5.3. Digital Signal Mux

The operation of the digital signal multiplexer (MUX) is to allow the comparator output to the DAC input channel to be overwritten with external calibration codes. The operation of this MUX is shown in Figure 4.20. The MUX switches the external inputs to the DAC during calibration mode for extraction of β in radix calibration.

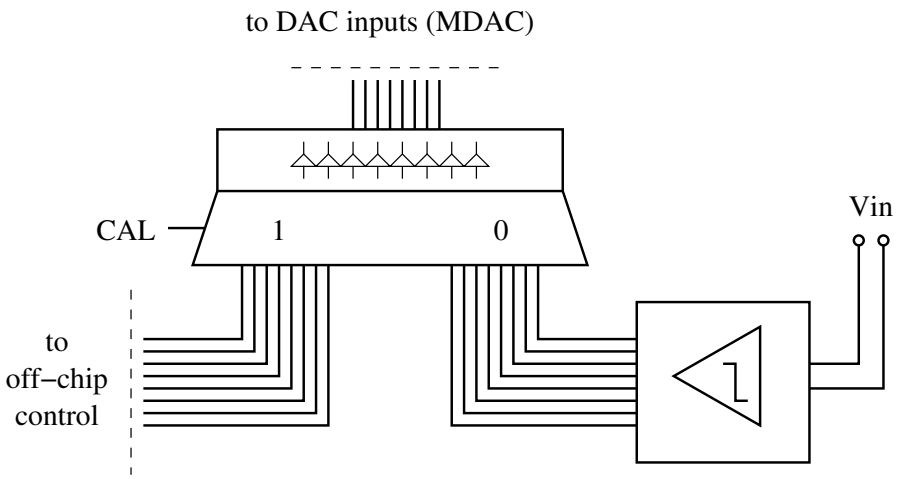

Figure 4.20: Digital Mux Operation

4.6. Layout

The layout of the first stage was completed as part of this thesis project. There are many layout issues to be considered with the design of a high-resolution ADC. These include signal and reference protection, analog circuit isolation, matching, and clock routing.

4.6.1. Floor-Planning

The first major concern in floor-planning any mixed-signal circuit is isolation of analog and digital circuits. This is best accomplished by segmenting the design into analog and digital portions and keeping sensitive analog circuits as far away from the digital circuits as possible. Additionally, analog and digital circuits should be on separate power supplies, and each circuit should have a guard ring tied to a low impedance node.

Other major concerns when determining the general layout structure are isolation signal traces themselves. The physical separation of analog and digital blocks will go a long way towards helping this issue, but sometimes it is not possible to keep these signals

apart (i.e. switches in the MDAC circuit). When sensitive analog signals must travel near to any other signal, shielding the lines with parallel ground lines (and sometimes top and/or bottom ground planes) is an effective strategy.

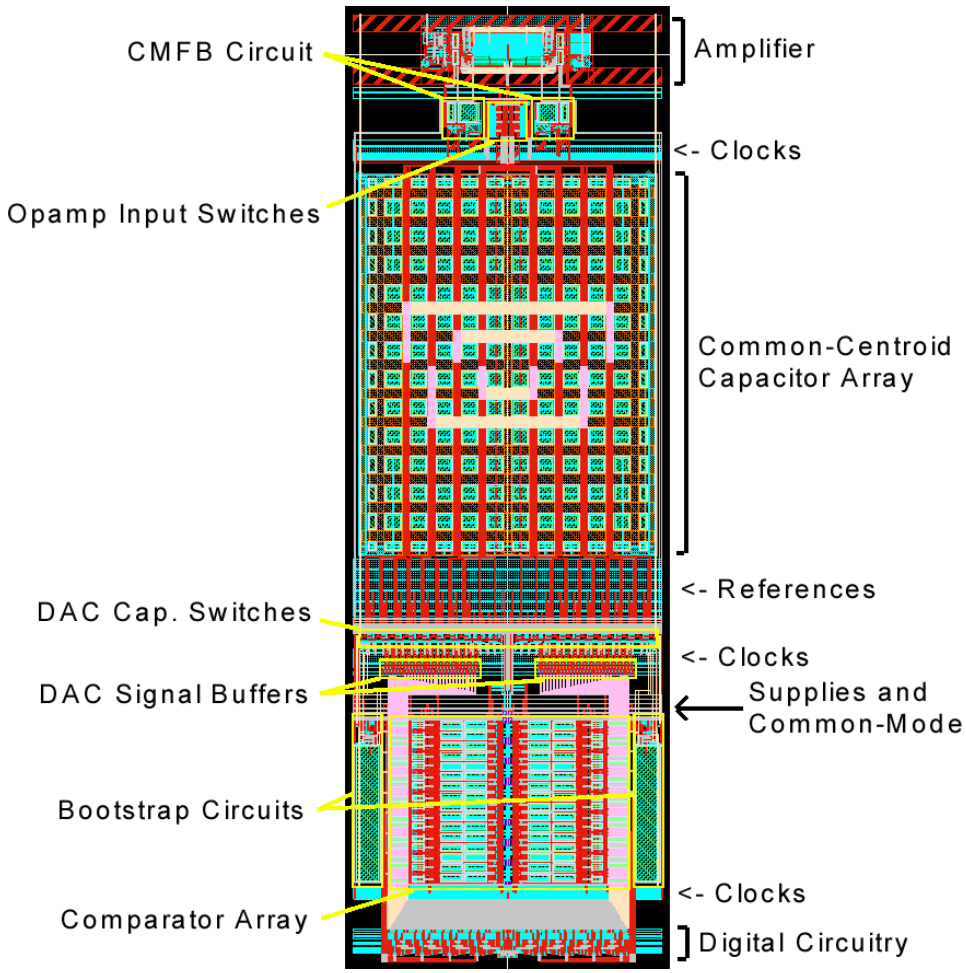

Figure 4.21: First Stage Layout

The layout for the first stage is shown in Figure 4.21. Notice that the analog amplifier circuit is on the opposite side as the digital circuitry. Additionally, clock signals only travel horizontally in dedicated clock channels – this avoids coupling of the clock signals to signals traversing the height of the stage. The references are grouped and isolated from any potential noise sources. They are also made from wide sheets of

metal to improve the response of the node to any transient glitch coupled onto the node.

4.6.2. Common-Centroid Capacitor Array

The matching requirement in a good analog layout is usually addressed by placing matched elements physically close to one another and by creating them from regular elements. The component that needs to maintain the best matching in Pipeline ADCs is generally the capacitor used as sampling and DAC capacitors within the MDAC.

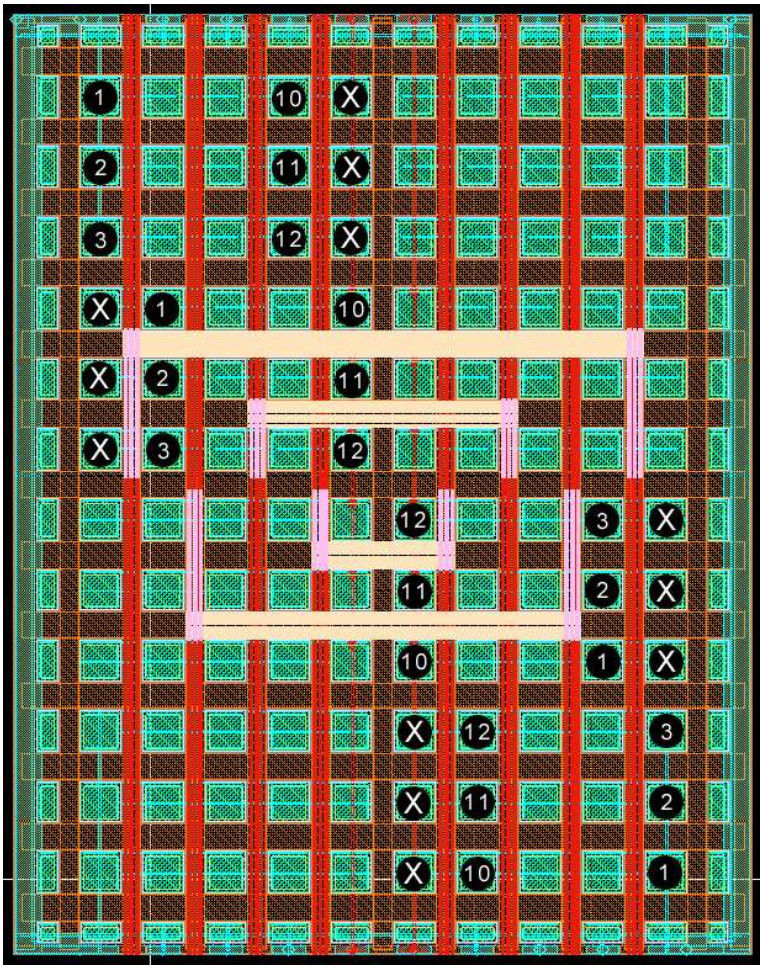

Figure 4.22: Common-Centroid Multibit Capacitor Array

These capacitors in the first stage need to have a matching equivalent to the entire ADC linearity specification. In order to reach these goals, common-centroid layout techniques should be used. This was done for the MDAC capacitor layout of the first stage. The structure of this array is represented by Figure 4.22. Multi-bit DACs make the common-centroid layout technique very difficult, but the approach taken limits the unmatched parasitic capacitance seen by each capacitor and creates a great deal of dispersal – an important property for cancelling of capacitance gradients. It is expected that this common-centroid layout would perform very well compared to other lower-resolution common-centroid arrays.

CHAPTER 5. CONCLUSION

The difficulty of implementing a high-resolution Pipeline ADC in a low-voltage process has been established and explored in detail in this thesis. Several solutions to this problem have been explored and an implementation incorporating a few of these solutions has been implemented on the modeling and simulation level.

5.1. Conclusions

The major components presented in this thesis towards the goal of a high-resolution Pipeline ADC in low-voltage processes are as follows:

- Sample-and-Hold Removal: The removal of the Sample-and-Hold circuit greatly reduces the power consumption and area use of the Pipeline ADC. This comes at the cost of a higher complexity in the first stage of the Pipeline.
- Rail-to-Rail Input: A rail-to-rail input is achievable with the sample-and-hold stage removed from the system. This increases the available signal range, thereby improving the SNR of the system. Special consideration is made for the operation of the MDAC in this situation. A final ADC structure incorporating two reference voltages was perused and a calibration scheme for correcting reference mismatch errors was developed.
- Stage Size/Scaling Optimization: The decision of how many bits to resolve in each pipeline stage was explored and an optimization method was developed and applied to the design implementation chosen for this work. The optimization greatly improved the noise and area performance in the design.
- Design Implementation: The design implementation portion of the thesis covered

many important parts in the design of a high-resolution ADC Pipeline stage. The first of these was the sampling structure which incorporated bootstrapped switches for high linearity. A high-gain amplifier meeting stringent bandwidth and noise consideration was also designed. Specialized, high-accuracy comparators were developed to handle the timing and strict matching requirements with the MDAC sampling (allowing S/H removal). Digital support circuits were created to handle such tasks as latching the comparator output data, performing bubble correction, and providing calibration control to the first stage MDAC. Finally, layout was completed on the first pipeline stage to show the feasibility of the implementation.

5.2. Future Work

Further development of this design strategy and completion of a test chip are an important next step in the continuation of this work.

Some other extensions to this work are as follows:

- One other MDAC structure for the rail-to-rail input (the single-reference V_{REF2} MDAC in Figure 3.21) showed promise and did not require the use of a calibration scheme. A rail-to-rail input Pipeline based on this structure may be a worthwhile exploration.

- Stage scaling optimization schemes allowing independent changes in stage-resolution and stage-scaling for each pipeline stage may find more optimum configurations for high-resolution Pipeline ADCs. Also better modeling of power consumption of the comparator stages would improve this optimization.

- Poor capacitor matching (even with common-centroid arrays) may require that some form of capacitor error correction [33, 34] be incorporated into the design.

Bibliography

[1] "Very-high-speed digital subscriber lines," System Requirements Document (T1E1.4/98-043R3) American National Standards Institute, 1998.

[2] E. Siragusa and I. Galton, "A digitally enhanced 1.8V 15b 40MS/s CMOS pipelined ADC," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, February 2004, vol. 1, pp. 452–453.

[3] H. Liu, Z. Lee, and J. Wu, "A 15b 20MS/s CMOS pipelined ADC with digital background calibration," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, February 2004, vol. 1, pp. 454–455.

[4] K. Nair and R. Harjani, "A 96dB SFDR 50MS/s digitally enhanced CMOS pipeline A/D converter," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, February 2004, vol. 1, pp. 456–457.

[5] Y. Chiu, P. Gray, and B. Nikolic, "A 1.8V 14b 10MS/s pipelined ADC in 0.18μm CMOS with 99dB SFDR," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, February 2004, vol. 1, pp. 458–459.

[6] D. Mercer, "A 14-b 2.5 MSPS pipelined ADC with on-chip EPROM," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 1, pp. 70–76, January 1996.

[7] O. Erdogan, P. Hurst, and S. Lewis, "A 12-b digital-background-calibrated algorithmic ADC with −90-dB THD," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 12, pp. 1812–1820, December 1999.

[8] José Silva, *High-Performance Delta-Sigma Analog-to-Digital Converters*, Ph.D. thesis, Oregon State University, School of Electrical Engineering and Computer Science, July 14, 2004.

[9] P. Balmelli and Q. Huang, "A 25 MS/s 14b 200mW $\Sigma\Delta$ modulator in 0.18μm CMOS," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, February 2004, vol. 1, pp. 74–75.

[10] B. Putter, "$\Sigma\Delta$ ADC with finite impluse response feedback DAC," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, February 2004, vol. 1, pp. 76–77.

[11] "International technology roadmap for semiconductors," Semiconductor Industry Association, available online: http://www.sia-online.org, 2001.

[12] I. Mehr and L. Singer, "A 55-mW, 10-bit, 40-Msample/s nyquist-rate CMOS ADC," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 318–325, March 2000.

[13] D. Chang, "PAPER TITLE UNKNOWN," *IEEE Transaction on Circuits and Systems–I*, to appear in 2005.

[14] J. Peterson, "A monolithic video A/D converter," *IEEE Journal of Solid-State Circuits*, vol. SC-14, no. 6, pp. 932–937, December 1979.

[15] B. Song, S. Lee, and M. Tompsett, "A 10-b 15-MHz CMOS recycling two-step A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 6, pp. 1328–1338, December 1990.

[16] D. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley and Sons, Inc., 1997.

[17] B. Razavi and B. Wooley, "Design techniques for high-speed, high-resolution comparators," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 12, pp. 1916–1926, December 1992.

[18] S. Lewis and P. Gray, "A pipelined 5-Msample/s 9-bit analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. SC-22, no. 6, pp. 954–961, December 1987.

[19] S. Lewis, H. Fetterman, G. Gross, R. Ramachandran, and T. Viswanathan, "A 10-b 20-Msample/s analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 3, pp. 351–358, March 1992.

[20] S. H. Lee and B. S. Song, "A direct code error calibration technique for two-step flash A/D converters," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 919–922, June 1989.

[21] S. Lee and B. Song, "Digital-domain calibration of multistep analog-to-digital converters," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 12, pp. 1679–1688, December 1992.

[22] Y. Lin, B. Kim, and P. Gray, "A 13-b 2.5-MHz self-calibrated pipelined A/D converter in 3μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 4, pp. 628–636, April 1991.

[23] G. Temes, Y. Huang, and P. Ferguson, "Switched-capacitor circuits with reduced sensitivity to amplifier gain," *IEEE Transactions on Circuits and Systems–II: Analog and Digital Signal Processing*, vol. 42, no. 8, pp. 559–561, August 1995.

[24] B. Song, M. Tompsett, and K. Lakshmikumar, "A 12-bit 1-Msample/s capacitor error-averaging pipelined A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 6, pp. 1324–1333, December 1988.

[25] R. Van De Plassche, "Dynamic element matching for high-accuracy monolothic D/A converters," *IEEE Journal of Solid-State Circuits*, vol. SC-11, no. 6, pp. 795–800, December 1976.

[26] H. Chen, B. Song, and K. Bacrania, "A 14-b 20-MSample/s CMOS pipelined ADC," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, pp. 997–1001, June 2001.

[27] Alan Hastings, *The Art of Analog Layout*, Prentice-Hall, Inc., 2001.

[28] J. Li and U. Moon, "A 1.8-V 67-mW 100-MS/s pipelined ADC using time-shifted CDS technique," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 9, pp. 1468–1476, September 2004.

[29] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio $\Sigma\Delta$ modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 349–355, March 2001.

[30] A. Abo and P. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[31] R. Poujois *et al.*, "Low-level MOS transistor amplifier using stroage techniques," *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, pp. 152–153, February 1973.

[32] K. Nagaraj, T. Viswanathan, K. Singhal, and J. Vlach, "Switched-capacitor circuits with reduced sensitivity to amplifier gain," *IEEE Transactions on Circuits and Systems*, vol. CAS-34, no. 5, pp. 571–574, May 1987.

[33] Y. Chiu, "Inherently linear capacitor error-averaging techniques for pipelined A/D conversion," *IEEE Transactions on Circuits and Systems–II: Analog and Digital Signal Processing*, vol. 47, no. 3, pp. 229–232, March 2000.

[34] S. Ryu, S. Ray, B. Song, G. Cho, and K. Bacrania, "A 14b-linear capacitor self-trimming pipelined ADC," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, February 2004, vol. 1, pp. 464–465.

[35] D. Fu, K. Dyer, S. Lewis, and P. Hurst, "A digital background calibration technique for time-interleaved analog-to-digital converters," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 1904–1911, December 1998.

[36] J. Ming and S. Lewis, "An 8-bit 80-Msample/s pipelined analog-to-digital converter with background calibration," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 1489–1497, October 2001.

[37] A. Karanicolas, H. Lee, and K. Bacrania, "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 12, pp. 1207–1215, December 1993.

[38] B. Murmann and B. Boser, "A 12-bit 75MS/s pipelined ADC using open-loop residue amplification," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, December 2003.

[39] C. Grace, P. Hurst, and S. Lewis, "A 12b 80MS/s pipelined ADC with bootstrapped digital calibration," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, February 2004, vol. 1, pp. 460–461.

[40] W. Yang, D. Kelly, I. Mehr, M. Sayuk, and L. Singer, "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at nyquist input," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 1931–1936, December 2001.

[41] J. Shyu, G. Temes, and K. Yao, "Random errors in MOS capacitors," *IEEE Journal of Solid-State Circuits*, vol. SC-17, no. 6, pp. 1070–1076, December 1982.

[42] D. Cline and P. Gray, "A power optimized 13-b 5Msample/s pipelined analog-to-digital converter in 1.2μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 294–303, March 1996.

[43] K. Bult and G. Geelen, "A fast-settling CMOS op amp for SC circuits with 90-dB DC gain," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 6, pp. 1379–1384, December 1990.