AN ABSTRACT OF THE DISSERTATION OF

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Adaptive, Wideband Analog-to-Digital Conversion for Convergent Communication Systems

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Terri Fiez

The exponential rate of advances in modern communication devices in the last several years have brought us higher levels of functionality and performance as well as reductions in physical size and power consumption. To continue this rate of advancement, next generation systems require wider bandwidth and higher resolution ADCs. Additionally, in order for ADCs to be used in a wide range of applications, reconfigurability and adaptability are critical features of future ADCs. Reconfigurable ADC architectures allow consolidation of receivers for multiple communication standards into one, providing size, power and functionality improvements over multiple discrete ADCs. This thesis presents a high performance track-and-hold block and reconfigurable high performance ADC for multi-functional communication applications.

In the design of analog-to-digital converters (ADCs), the front-end track-and-hold or sample-and-hold is often one of the most challenging parts of the design. Open-loop

designs with high sample rates are reaching the limits of their linearity. Presented here is a high-speed, high-resolution closed-loop track-and-hold in a 0.18um SiGe BiCMOS technology. The architecture provides both high linearity and high speed, with 98.7dB and 89.4dB SNDR at 50MS/s and 100MS/s, respectively.

As these specifications evolve to meet customer demands, new, high performance ADCs are needed. To this end, an efficient parallel $\Delta\Sigma$ ADC architecture has been designed that achieves high performance in digital processes, while also providing additional architecture flexibility. This ADC, consisting of four parallel $\Delta\Sigma$ ADCs and a single pipeline ADC provides high performance and reconfigurablity. This ADC is suited to applications requiring not only wide-bandwidth, high resolution signal conversion but an on-the-fly reconfigurable resolution and bandwidth.

Adaptive, Wideband Analog-to-Digital Conversion for Convergent Communication Systems

by

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APPROVED:

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Robert Batten, Author

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DEDICATION

To my friends and family.

To Kurt, thanks man!

Chapter 1 – Introduction

Mixed-signal circuits are an invisible but ubiquitous part of everyday life. Cell phones, computers, network systems, automobiles, television, radar, airplanes and many more systems of today have been transformed through the development of high performance mixed-signal circuits [1, 2]. As consumers become more reliant on these technologies for their everyday lives, they expect significant advances in each new generation of products. These advances include higher levels of functionality and performance, as well as reductions in physical size and power consumption [3, 4].

The evolution of cellular phones over the last decade illustrates the technological advancements that have been made. Just a short 10 years ago, cellular phones were the size of small bricks, needed frequent charging and could only send and receive calls. Contrast this with today's typical cell phone that includes digital cameras, global positioning systems (GPS), MP3 players, full internet access and email capabilities, and wireless networking [5]. These devices also serve as complete digital assistants and last for days on compact batteries. Next generation devices will enable high speed, wide bandwidth video and multimedia streaming and communication. With this capability it becomes a personal multimedia system with a form factor smaller than a wallet [1, 2]. Incorporated into the system is the ability to process different signal and carrier frequencies for the many wireless standards such as Bluetooth, Wi-Fi, WiMax, cognitive radio and GPS [6]. It is unrealistic from a cost and size perspective to include a separate

receiver for each wireless standard. Single receiver architectures are needed that can provide the functionality of multiple receivers, providing the technology so that small handheld, energy efficient multimedia devices can be realized in the future.

Much the same as in portable wireless products, this trend of combining multiple functionality and improved performance extends to many other product areas. With competition for sites to place cellular towers, the expense of a tower installation, and the limited space and power for equipment, wireless base stations must provide multi-standard communications with minimal increase in size and power consumption [7]. Other systems, such as military and commercial radar systems, have a growing need for reconfigurable front ends to provide enhanced information and an ability to better track multiple objects [8, 9, 10]. These market forces pushing products in competing directions, higher performance and increased functionality, while reducing size and power consumption, are driving the need for innovation in reconfigurable, wireless front-end systems.

1.1 Illustrative System: Radar

To illustrate the challenges in the system design, a radar system is examined with a simplified block diagram shown in Fig. 1.1 [8]. A radar system is much like other communication systems consisting of an antenna, transmit/receive (T/R) switch, transmitter, receiver and associated control and user interfaces. The transmitter transmits a signal to an antenna where it is aimed at a target. Some of the energy incident on the target is reflected from the target back in the direction of the radar system. With the radar now

in receive mode, it listens for this reflection, processing the return signal to display it in a form the operator can understand.

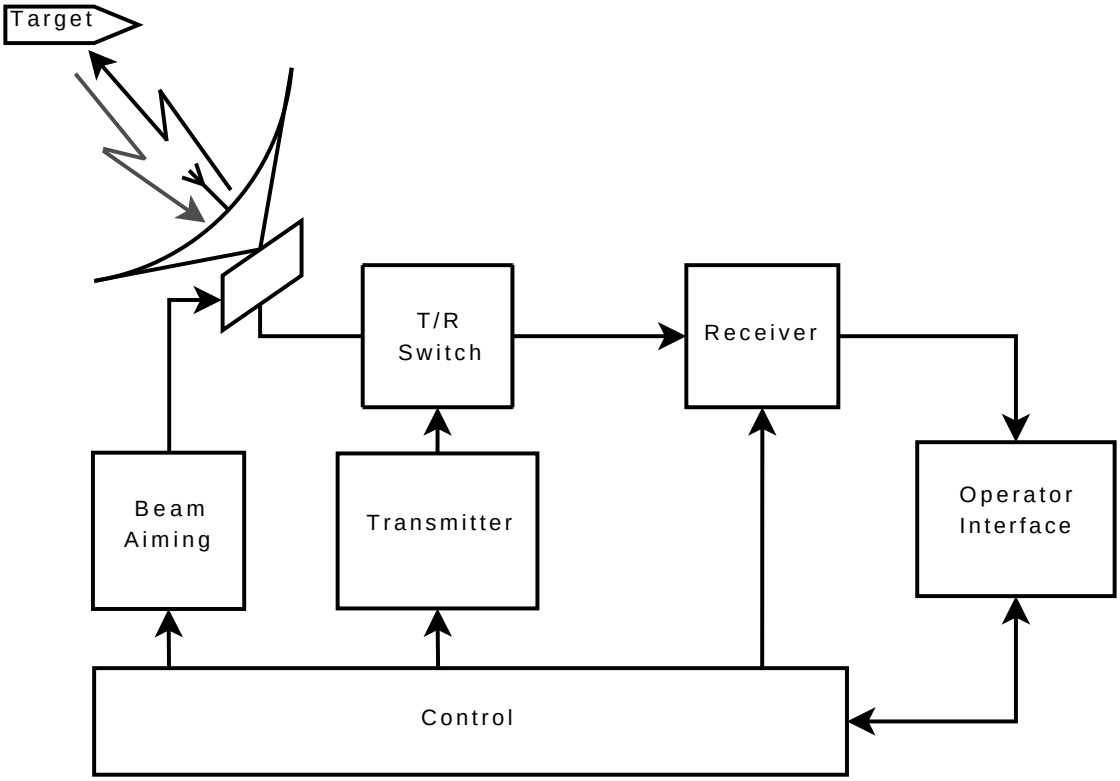


Figure 1.1: Block diagram of a radar system.

Modern radar is a complex system operating in dynamic and very complex environments such as airports, battlefields, open ocean, small harbors and a host of other places. These radar systems are embedded in moving systems such as boats, airplanes and missiles, and in fixed systems such as air traffic control, missile tracking and early warning systems. With such a complexity and broad range of radar applications, there is no single radar system that will work for all applications. Hence, the design of a radar system involves many parameters and trade-offs for each application. Parameters like

beam size and shape, beam steering method, transmit power, frequency and pulse duration, receiver sensitivity, signal-to-noise ratio and bandwidth are all important choices in the design process. Some of these parameters are shown in Table 1.1 for various military radar systems [8]. Wide area search radar needs high power, wide bandwidth and low pulse rates to find small objects at long distances. Navigation radar needs a narrower bandwidth and higher pulse rates to provide accurate information about the area around the radar. Fire control radars usually have narrower bandwidths, lower power and very high pulse rates to track targets and provide accurate position and speed information.

Radar Type	Carrier Frequency (GHz)	Peak Transmit Power (kW)	Bandwidth (MHz)	Pulse Rate (Hz)
AN/SPS-10	5.4 - 5.8	195 - 280	1 / 5	625-650
AN/SPS-55	9 - 10	130	1.2 / 12	750-1500
AN/SPS-40	0.4 - 0.45	200	0.07 / 1.7	300
AN/SPS-49	0.8 - 0.9	280	0.4	275 / 285
AN/SPS-48	2.9 - 3.1	60 - 2200	17.7	161-1366
AN/SPY-1	3.1 - 3.5	4000 - 6000	10	Variable

Table 1.1: Various radar bandwidths and pulse rates.

Of special interest is the receiver bandwidth and sensitivity. Many of today's communication systems are moving toward simplified receivers where significant portions of the analog and RF circuitry have been replaced with wide-band, high resolution analog-to-digital converters. Radar is no exception [9, 10]. Radar systems have evolved from complex multi-stage receiver systems to the modern single intermediate frequency (IF) receiver such as the receiver shown in Fig. 1.2 [8, 10]. This modern receiver system consists of an antenna followed by a mixer that converts the received RF signal to a lower IF signal. The IF signal is amplified and filtered in the IF stage, modulated to I

and Q signals, then converted to digital signals by the two complementary ADCs. The digital signals are then processed further in the digital signal processor (DSP). Two optional blocks are the pulse and moving object detection systems. Depending on the radar requirements, they may be done in either analog or digital domains.

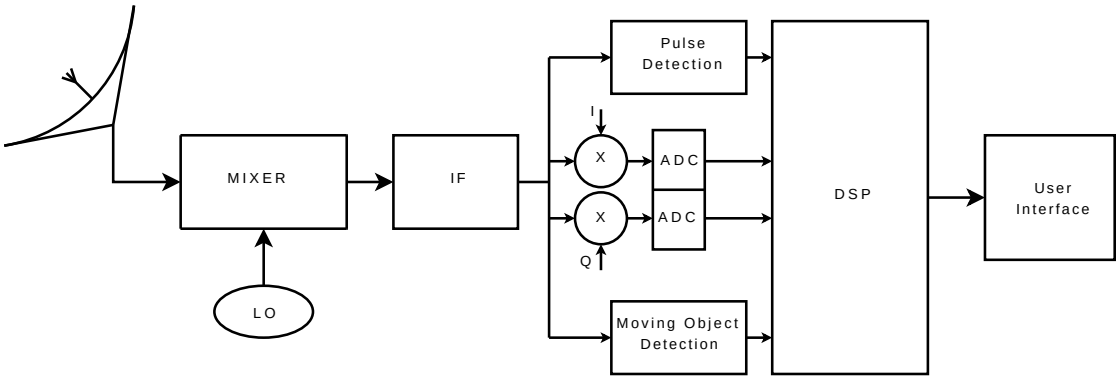


Figure 1.2: Block diagram of a single IF radar receiver.

Many of these modern single-IF systems are currently limited by the resolution and bandwidth of the system ADC. In these systems, the next closest limiting factor, the LO phase noise, ranges from 10dB better at 100MS/s to almost 25dB at 3GS/s than the ADC [11]. Accordingly, at 3GS/s, an ADC performance increase of 20dB can directly improve the overall receiver performance by as much as 20dB. The bandwidth of the receiver also affects the performance of the radar system in several ways. A wider bandwidth allows acquisition of fast moving targets and causes less pulse shape distortion, thus resulting in more accurate target information, better clutter removal, increased target resolution and allows easier implementation of complex Electronic Counter Measures (ECM) in the digital domain. But when designing a wide bandwidth system, the increase in noise is often the limiting factor. Thus, when choosing the ADC for a radar

system, two of the important specifications are resolution and bandwidth. To limit this overall noise increase, a wide-band ADC must have an effective resolution or signal-to-noise+distortion ratio (SNDR) typically above 14 bits [9, 10].

Modern radar is a complex system operating in dynamic and very complex environments. Many of these systems, especially in combat arenas, are required to be flexible enough to provide alternate functionality if another system is damaged or fails. Particularly in battle systems where size, weight and power consumption are factors, having a radar system that can perform the tasks of several systems is of large benefit [8]. Of equal concern are radar systems that are difficult to detect and difficult to jam. Radar receiver architectures that can dynamically adjust resolution, bandwidth and signal coding are an essential building block to achieving such modern, flexible radar systems. Research into extending the performance of both of these areas is important to expanding the current state of the art.

1.2 Current State of the Art

For many communications applications, the bandwidth of the signal is partially or even completely defined by other external factors. To be able to send more information over the same bandwidth, the SNDR of the channel has to be increased. In many cases, this means increasing the ADC resolution and lowering the ADC distortion. Table 1.2 shows the ADC specifications for various wireless communication systems [6, 8, 12, 13, 14]. The first two systems, GSM and CDMA, are designed for voice communication for cellular phone applications. The next three systems, WCDMA, Bluetooth and WiMax,

are designed for higher speed communications that may include both voice and data. The last type of system shown is a radar system which was discussed earlier. The table shows that each system needs an ADC with a specific input bandwidth and resolution.

Communication System	Bandwidth (MHz)	SNDR (dB)	ADC Architecture
GSM	0.2	70 - 80	$\Delta\Sigma$
CDMA	2.0	50	$\Delta\Sigma$
WCDMA	4.0	60 - 70	$\Delta\Sigma$
Bluetooth	1.5	70	$\Delta\Sigma$
WiMAX	1 - 20	50 - 70	$\Delta\Sigma$
Radar	0.07 - 20	30 - 90	Various

Table 1.2: Various communication system bandwidths and SNRs.

Summarized in Fig. 1.3 is the bandwidth versus SNDR for published data converters from 1997 to 2008 [15]. The solid line corresponds to 1ps rms jitter and represents where jitter noise becomes the performance limitation. By plotting each type of converter with a different symbol, the type of converter best for which bandwidth and SNDR combination is obvious. This insight provides the initial starting direction for this research. Analyzing the plot there are several obvious trends. Flash ADCs are centered in the high bandwidth, low SNDR region. Delta-Sigma ($\Delta\Sigma$) ADCs are centered in the low bandwidth, high SNDR region with the other types sandwiched in the middle. Pipeline and folding architects occupy the higher portion of the middle zone, while successive approximation architectures generally occupy the lower performance regions.

Re-examining Table 1.2 with this survey in mind, it becomes clear which converters are best suited to each application. With bandwidths in the one to four MHz range and SNDR requirements between 50 and 80dB, $\Delta\Sigma$, SAR, pipeline and folding architec-

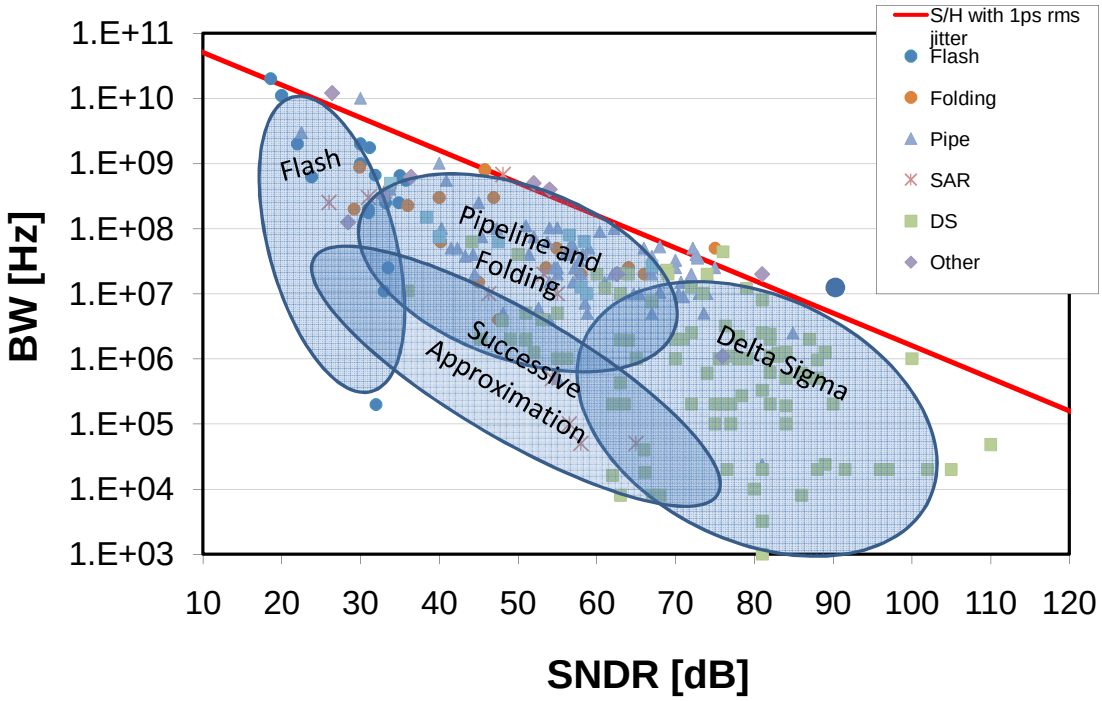


Figure 1.3: Survey of ADC performance (1997 - 2008).

tures are all possibilities for the CDMA, WCDMA, Bluetooth and WiMax applications. And in many applications $\Delta\Sigma$ ADCs are chosen because of their low power usage, high linearity and ease of integration in existing digital processes [6, 14]. For GSM, with very narrow bandwidth and high SNDR requirements, the preferred implementation is a $\Delta\Sigma$ ADC. The radar system with its high variability in both bandwidth and SNDR uses several architectures. Very wide bandwidth radar with low SNDR is usually implemented with a flash ADC while low bandwidth, high SNDR radar is usually implemented with $\Delta\Sigma$ ADCs. The mid-resolution radar systems can be implemented in either pipeline, flash, SAR, or $\Delta\Sigma$ depending on the actual requirements [10, 11, 16].

Some of the communication applications that were discussed earlier are pushing the

envelope of both bandwidth and SNDR performance. In Fig. 1.3, this is the area near the jitter performance limitation and on the upper right side of that line. To achieve convergent communication systems means not only are better clock generation circuits and track-and-hold circuits needed to help meet the jitter requirements but also significantly improved ADC designs.

For SNDRs greater than approximately 75 dB, the most common ADC architecture by far is $\Delta\Sigma$ based. This is for several reasons. First, a $\Delta\Sigma$ ADC is designed to trade-off speed for linearity, giving it inherently higher SNDR. Secondly, the structure of a $\Delta\Sigma$ ADC makes it much less sensitive to process non-idealities compared to most other ADC architectures. $\Delta\Sigma$ ADCs allow the design of very high SNDR ADCs with relatively poorly performing circuit components. While the $\Delta\Sigma$ ADC architecture can be highly linear, speed is traded off to obtain this high linearity [17]. To increase both linearity and bandwidth, one option is to use the parallel $\Delta\Sigma$ architecture [18], sacrificing silicon area for increased speed. For many applications, where cost is the driving concern, this is not the best option. However, for some applications where performance needs warrant the cost, this solution is viable. Not only is this approach well suited to fine line digital processes, but the design is easily scalable. The parallel approach also has the advantage of basic on-the-fly reconfigurable signal processing, and easily reconfigurable bandwidths and resolutions. The system, with multiple channels and reconfigurable modulation and filter banks, enables bandwidth changes from a wide bandwidth, low resolution option to a narrow bandwidth, high resolution option. This architecture can capture multiple narrow band signals at different frequencies with high accuracy by tuning sets of channels to capture different signals. There is also an added

advantage for systems where signals are encoded with orthogonal codings such as in radar or CDMA [10, 19, 20]. The reconfigurable modulation can be further utilized to help improve signal correlation before the signal enters the ADC, thus improving SNR.

The next generation of wireless communications systems will require not only wider bandwidth, high SNDR ADCs but also ADCs that are reconfigurable and adaptable, thus allowing the same ADC to be used for a range bandwidths and SNDRs. The ADC needs to be reconfigured during operation to meet the requirements of each standard.

Consolidating multiple receiver architectures into one provides size, power and functionality improvements over multiple discrete receivers. From the insight provided in Fig. 1.3, to direct the search for converter architectures for the next generation convergent wireless receiver communication systems, wide bandwidth and high SNDR $\Delta\Sigma$ ADCs are a necessity. This research provides one solution to address this need.

In this dissertation, a novel parallel $\Delta\Sigma$ ADC is presented that utilizes ideas from flash architectures, and includes flash and pipeline sections in a parallel $\Delta\Sigma$ ADC architecture to create a convergent reconfigurable ADC that outperforms other ADCs. Chapter 2 describes a novel closed-loop track-and-hold architecture that reduces previous stage loading while improving SNDR and has reduced sensitivity to clock aperture jitter. The novel parallel $\Delta\Sigma$ ADC architecture is presented in Chapter 3. Chapter 4 describes the design and measured results of the converter. Finally, Chapter 5 provides an overall summary of the work and future research directions.

Chapter 2 – A High Performance Track and Hold

2.1 Introduction

As the initial operational block of a discrete-time ADC, track-and-hold or sample-and-hold circuits are important building blocks in many analog and mixed-signal circuits. As shown in Fig. 2.1, the track-and-hold block samples the input signal based on a clock signal and then holds that value at the output until the clock signal triggers the next sample. This is necessary so that the ADC circuit that follows has a stable analog input signal to convert. The track-and-hold circuit is at the front-end of the ADC and signal errors introduced by the track-and-hold block can be very difficult, if not impossible, to correct or remove. Considering this, performance of the track-and-hold circuit can easily be the limiting factor in the design of high performance analog-to-digital converters and other circuits. Distortion, noise, and to a lesser extent gain and offset errors are indistinguishable from the input signal to the ADC. Therefore, research into the next generation of ADCs is not complete unless there are also improvements in track-and-hold circuits and architectures.

Critical to the performance of track-and-hold circuits are sampling and aperature jitter and sampling error. Sampling jitter is the time variance between when the input should be sampled and when it is actually sampled. Aperature jitter is the variation in the settling time when the switch is closed. Sampling error is the difference between

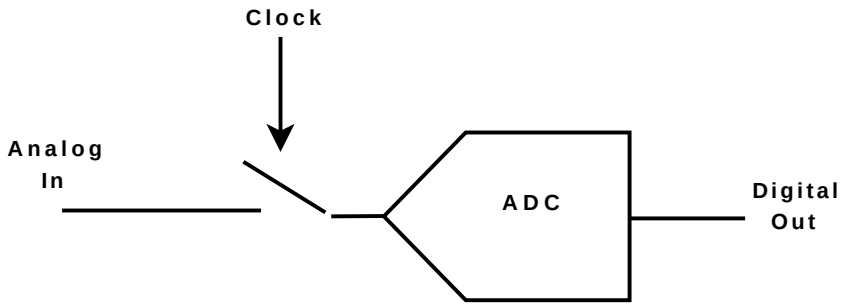


Figure 2.1: An ADC showing the track-and-hold block.

an “ideally” sampled signal and the actual signal. These inaccuracies in sampling the signal result in a reduction in the signal-to-noise ratio (SNR) of the track-and-hold.

2.2 Comparasion of Track-and-Hold Architectures

There are two classes of track-and-holds (T/H). The first class and simplest are the open-loop track-and-holds [21, 22, 23]. These architectures consist of a switch, a hold capacitor and usually an opamp as shown in Fig. 2.2. When the switch is closed, the output of the open-loop track-and-hold circuit tracks the input signal. When the switch is opened, the voltage stored on the sampling capacitor, C_s, is held at the final input value at the instant before the switch was opened. The amplifier buffers the hold capacitor and provides a stable output voltage. Unfortunately, since it is an open-loop circuit, high linearity is difficult to achieve, especially at high sample rates where switch non-idealities limit performance. Many schemes to help linearize this switch have been proposed including clock boosting, dummy switch transistors, and special switch phasing [24, 25, 26]. The final serious drawback is that the unbuffered switch at the input

can adversely effect the previous circuitry due to excessive loading and input switching transients.

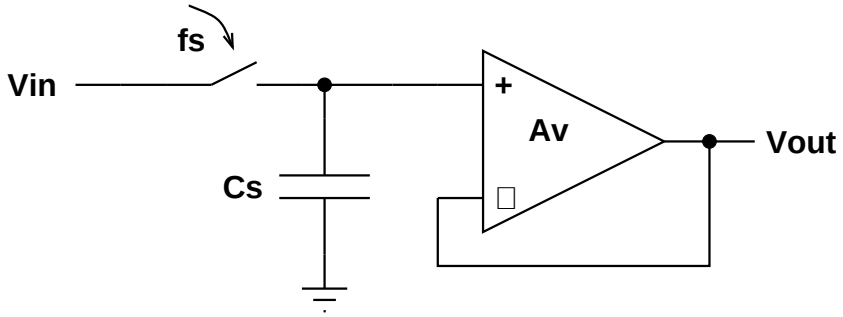


Figure 2.2: Open-loop track-and-hold architecture.

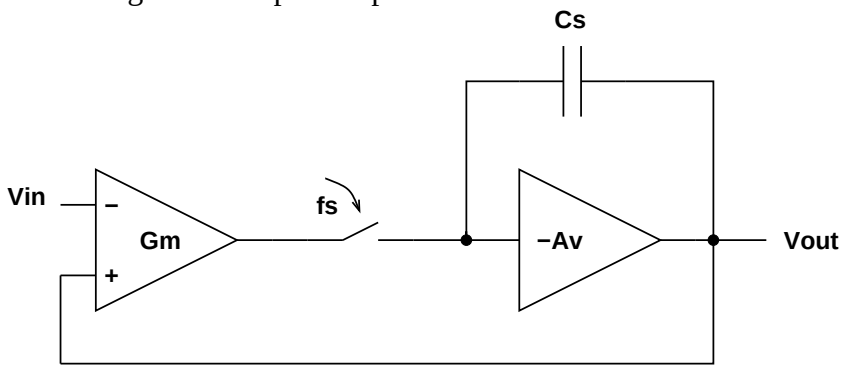


Figure 2.3: A closed-loop track-and-hold architecture.

The second class of track-and-hold circuits are the closed-loop track-and-holds [22, 23, 27] as shown in Fig. 2.3. This is a more complex architecture, where the switch is contained within a closed loop, reducing the non-ideal switch effects and providing a built-in anti-aliasing filter. In a closed loop architecture, the input signal, V_{in} is compared to the output signal, V_{out}. The difference between these two signals is converted to an error current which passes through the switch element and charges the hold capacitor, C_s. The output amplifier, $-Av$, is capable of driving the output.

The closed-loop track-and-hold has some disadvantages. There is an increase in complexity and power due to the system architecture. The bandwidth of the track-and-hold is limited by the bandwidth of the initial transconductor block. Thus it not suitable for very high speed sub-sampling applications. And, in addition to being somewhat more complicated and requiring more power to operate, it requires higher frequency (f_T) transistors to achieve the same sample rate as an open-loop design. While these disadvantages make the closed-loop track-and-hold a poor choice for some applications, it is well suited for applications where high-linearity is the key system goal and for applications where noise and loading on the previous circuit are a significant consideration. Since the switch is enclosed in a feedback loop, many of the non-idealities of the switch have little impact on the performance of the circuit. This negative feedback loop also suppresses the nonlinearities that exist in the transconductor and amplifier. This allows for high overall linearity with relaxed individual circuit linearity requirements. The switching transients are isolated from the previous circuit and do not have to supply the high current to charge the capacitor.

Clock jitter at the front-end track-and-hold can easily be the limiting factor in data converter performance [15] and its affect on open and closed loop track-and-holds is different. While clock jitter cannot be corrected in the track-and-hold, aperature jitter, or the variation of the sampling period, can be greatly reduced by using a closed-loop track-and-hold. The expression for the reduction in aperature jitter noise of a closed-loop over an open-loop track-and-hold is given below [28]:

$$SNR_{CL-OL} = 10\log\left[\left[\frac{e^{2\omega_0\tau}+1-2e^{\omega_0\tau}cos(\omega_{in}\tau)}{(1-e^{-\omega_0\sigma_\tau})^2+\omega_{in}^2\sigma_\tau^2e^{-2\omega_0\sigma_\tau}}\right]\left[\frac{sin(\pi f_{in}\tau)}{\pi f_{in}\sigma_\tau}\right]^{-2}\right] dB \quad (2.1)$$

where f_{in} is the input frequency, τ is the integration time and σ_τ is the standard deviation of the aperture jitter, and where ω_0 is the unity-gain bandwidth of the closed loop and $\omega_{in} = 2\pi f_{in}$. Solving this equation with an input frequency of 1MHz, an integration time of 5ns, a closed-loop bandwidth of 160MHz and sweeping the jitter from 0ps to 100ps rms, shows approximately 62dB of improvement in aperature jitter induced error. Thus, using a closed-loop track-and-hold significantly reduces the aperature jitter while improving the linearity.

Having compared the open-loop to the closed-loop track-and-hold architectures, the closed-loop architecture was chosen. For this design, with requirements of moderately high sample rates and high linearty, the closed-loop architecture is the best choice. Next, a novel implementation of this architecture, is presented that achieves both high linearity operation and moderate sample rates. The performance is improved by extending the sampling bandwidth and relaxing the input drive requirements.

2.3 The Closed-Loop Architecture

The closed-loop track-and-holds shown in Fig. 2.5 (a) and (b), consist of one or more transconductors, a switch, a hold capacitor, and an opamp [29, 22, 30, 28]. These closed-loop track-and-hold architectures can be classified into two major catagories based on

the location of the summing node. In Fig. 2.5(a) there are two separate G_m blocks, one for the input signal (G_{mi}) and one for the feedback signal (G_{mf}) followed by a current summing node. Since the G_{mi} block is outside the feedback path, any errors or distortion introduced will not be suppressed by the feedback loop. This is also true for the feedback transconductor, G_{mfb}. Additionally, any gain errors between the two G_m blocks will result in an overall T/H gain error since the track-and-hold gain is related to the ratio of the input and feedback G_m blocks. The second architecture shown in Fig. 2.5(b), subtracts the input signal from the feedback signal at the input of the G_m block. The error signal then passes through the rest G_m block where it is converted to a current and charges the hold capacitor. In many cases the summing is done with passive, linear resistors and only the error signal is passed through active components. This results in a very linear track and hold circuit, limited only by the ability of the circuit to keep the resistor node at a virtual ground.

Assuming that each architecture uses the same resistor-based transconductor, the linearity of each can be compared. Non-linearity can be shown to be a function of the node voltage at the virtual ground of a non-linear block in feedback [31]. In this case, the virtual ground node is v_s, connected to the resistor in Fig. 2.6. Comparing the signal magnitude at the virtual ground node for both architectures provides an easy way to compare relative linearities. The equation for transfer function from v_{in} to each v_x for the first architecture is:

$$\frac{v_{x1}}{v_{in}} = \frac{-1}{g_{mb}R_{in}A - 1}$$
$$\frac{v_{x2}}{v_{in}} = \frac{\frac{-g_{mf}R_lA}{(2A_vg_{mb}^2R_{fb}R_{in}A - g_{mb}g_{mf}R_{in}R_lA + g_{mf}R_l - 2A_vg_{mb}R_{in} - 2A_vg_{mb}R_{fb})A + 2A_v}}{1 + sC\frac{(A_v+1)(g_{mb}^2R_{fb}R_{in}R_lA^2 - g_{mb}R_{in}R_lA - g_{mb}R_{in} - g_{mb}R_{fb}R_lA + R_l)}{(2A_vg_{mb}^2R_{fb}R_{in}A - g_{mb}g_{mf}R_{in}R_lA + g_{mf}R_l - 2A_vg_{mb}R_{in} - 2A_vg_{mb}R_{fb})A + 2A_v}} \tag{2.2}$$

and for the second architecture is:

$$\frac{v_x}{v_{in}} = \frac{\frac{(A_v+1)R_{fb}R_lsC + R_{fb}}{(g_{mb}R_{fb}R_{in} - A_vg_{mf}R_{in}R_l)A - R_{in} - R_{fb}}}{1 + sC\frac{(A_v+1)R_l(g_{mb}R_{fb}R_{in}A - R_{in} + R_{fb})}{(g_{mb}R_{fb}R_{in} - A_vg_{mf}R_{in}R_l)A - R_{in} - R_{fb}}} \tag{2.3}$$

where R_{in} and R_{fb} are the input and feedback resistors, g_{mf} and g_{mb} are the feedforward and feedback transconductors, R_l is the output impedance of the g_{mf} block, A is the gain of the gain block in the modified transconductor, and OGF is the opamp gain factor $1/A_v + 1$ where A_v is the gain of the hold amplifier.

Plotting $max(v_{x1}, v_{x2})$ for the first case and v_x for the second case in Fig. 2.4, it is obvious that at low frequencies in the second architecture, v_x has significantly a lower magnitude. This result shows that for input signal frequencies below $800MHz$ the second closed-loop architecture provides significantly improved linearity.

Analyzing Equation (2.3), we see that the low frequency behavior, when $jw = 0$ and $R_{in} \approx R_{fb}$, is governed by:

$$\left.\frac{v_x}{v_{in}}\right|_{\omega=0} = \frac{R_{fb}}{Ag_{mb}R_{fb}R_{in} - AA_vg_{mf}R_{in}R_l - R_{in} - R_{fb}} \approx \frac{1}{-AA_vg_{mf}R_l} \tag{2.4}$$

showing that increasing either the feedforward transconductance, g_{mf}, the transconduc-

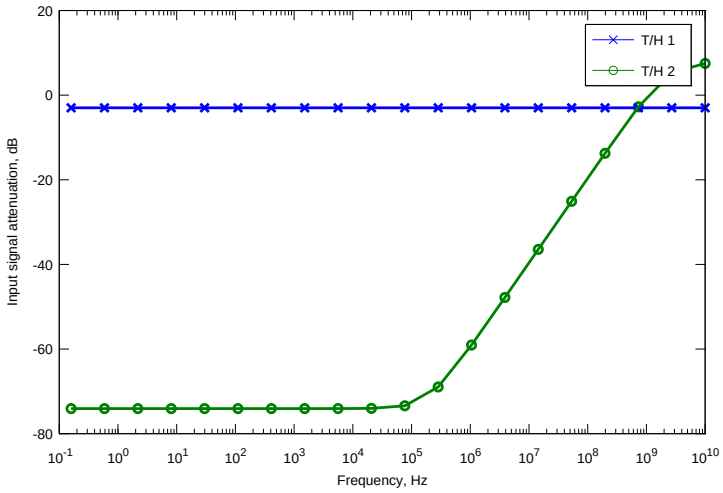


Figure 2.4: Input signal attenuation at virtual ground node for two track-and-hold architectures.

tor output impedance, R_l, or the gain of the amplifiers A and A_v, reduces the magnitude of v_x, thus improving system linearity. At higher frequencies, the magnitude of v_x begins to increase at 20 db/dec due to a system zero. The frequency of the zero is given by:

$$\omega_z \approx \frac{1}{(A_v + 1)R_l C}. \tag{2.5}$$

At some point the magnitude of v_x stops increasing with frequency due to a high fre-

Parameter	Equation
ω_{pole}	$\frac{g_{mf}}{g_{mb}}\frac{1}{AR_{fb}C}$
ω_{zero}	$\frac{1}{(A_v+1)R_lC}$
$\lvert V_x\rvert_{\omega=0}$	$\frac{1}{-AA_vg_{mf}R_l}$

Table 2.1: Pole, zero and gain equations for v_x node.

quency pole in the circuit. This pole is localed at:

$$\begin{aligned}\omega_p &\approx \frac{(g_{mb}R_{fb}R_{in} - A_v g_{mf}R_{in}R_l)A - R_{in} - R_{fb}}{(A_v+1)R_l(g_{mb}R_{fb}R_{in}A - R_{in} + R_{fb})C} \\ &\approx \frac{A_v g_{mf}R_{in}A}{(A_v+1)(g_{mb}R_{fb}R_{in}A - R_{in} + R_{fb})C} \\ &\approx \frac{g_{mf}}{g_{mb}}\frac{1}{AR_{fb}C}\end{aligned} \tag{2.6}$$

and decreasing A, R_{fb} or C will increase the pole frequency. Table 2.1 shows these simplified equations.

To optimize the linearity of this design, increasing the pole and zero frequencies and decreasing the magitude of v_x at DC are necessary. Decreasing the zero frequency, while reducing the high frequency magnitide of v_x, is not desirable since it can make the track and hold unstable. From Table 2.1, to achieve this optimization, g_{mf}, R_l, A_v could in increased within reason as R_l and A_v also control the zero frequency. Similarily, g_{mb} and R_{fb} can be decreased to help achieve the necessary performance.

Either of these track-and-hold architectures can be used for this design. But, since the goal of this work is a highly linear track-and-hold circuit, the second architecture with the best inherent linearity was choosen. Choosing this closed-loop architecture limits the available choices of transconductor types leaving only one, the resistor-based

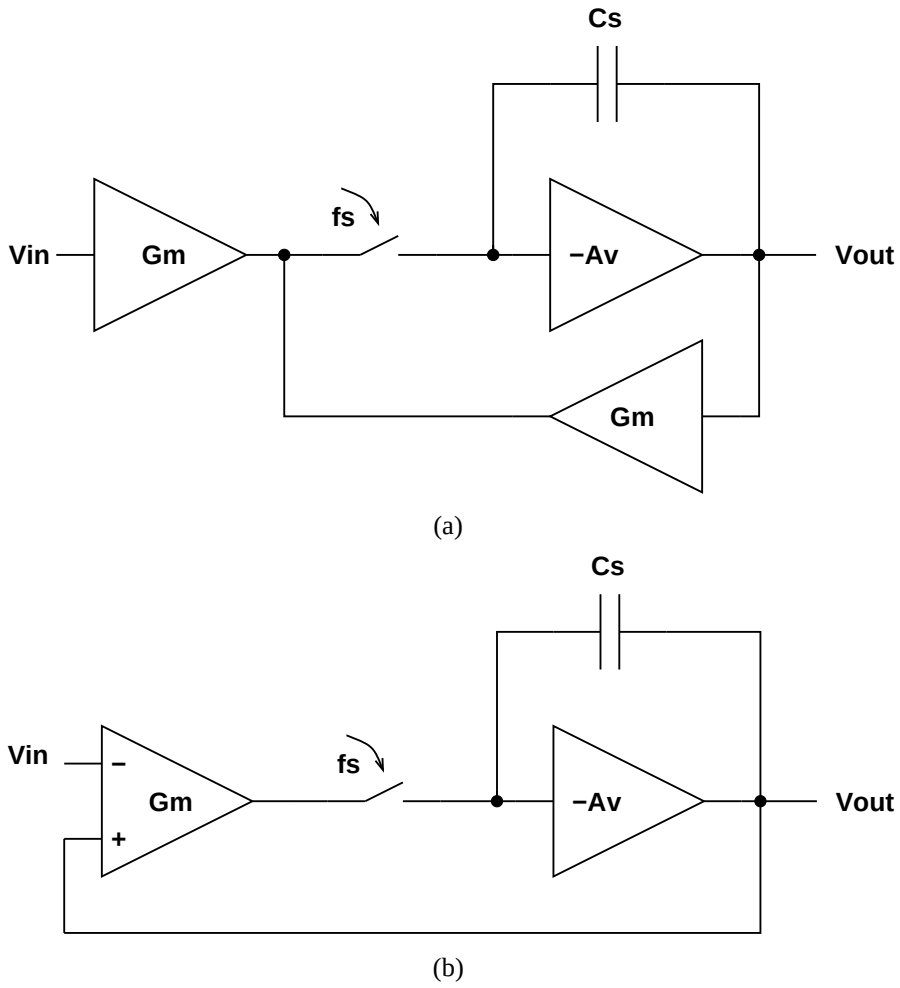


Figure 2.5: Various closed-loop architectures.

transconductor.

Assuming ideal components, the closed-loop transfer function for the track-and-hold (switch closed) is:

$$\frac{Vo}{Vi} = \frac{1}{1 + s\frac{C_s}{G_m}}, \tag{2.7}$$

where C_s is the capacitance and G_m is the transconductance. The closed-loop settling

is then governed by the closed-loop time constant which, from (2.7), is $\frac{C_s}{G_m}$. Since the capacitor size is set by the $\frac{kT}{C}$ noise requirements, the transconductance, G_m, must be selected so that the settling and distortion requirements are met.

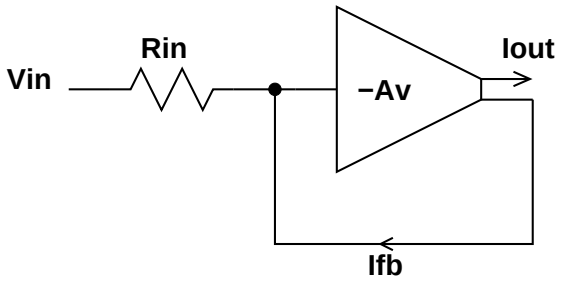


Figure 2.6: A standard resistor-based transconductor.

A standard high-linearity resistor-based transconductor [22, 30] is shown in Fig. 2.6. For this circuit, the transconductance is approximately $\frac{1}{R}$, where R is the size of the resistor.

For fast, high resolution track-and-holds, the performance is fixed by the closed-loop time constant and the $\frac{kT}{C}$ noise from the resistor capacitor combination. Assuming ideal components, the closed-loop transfer function for the track-and-hold (switch closed) can be shown to be:

$$\frac{Vo}{Vi} = \frac{1}{1 + s\frac{C_s}{G_m}}, \tag{2.8}$$

where C_s is the capacitance and G_m is the transconductance. The closed-loop settling is then governed by the closed-loop time constant which, from (2.8), is $\frac{C_s}{G_m}$. Since the capacitor size is set by the $\frac{kT}{C}$ noise requirements, the transconductance, G_m, must be selected so that the settling and distortion requirements are met.

Once the capacitor is sized to meet noise requirements, the settling rate must be

set by the resistor and, for fast settling rates, the resistance becomes too small for a completely integrated solution to be feasible. For example, for 16 bit settling accuracy at 100MS/s with a 20pF capacitor, 12 time constants (12τ) are required and the resistor size needed would be:

$$R = \frac{\tau}{C} = \frac{\frac{1}{12Fs/2}}{C} = 20\Omega. \tag{2.9}$$

A small-valued input resistor results in excessive loading of both the earlier stages and the hold amplifier driving the feedback into the transconductor block. As a result, the design consumes excessive current to drive this low impedance and greatly increases the chip area and power consumption.

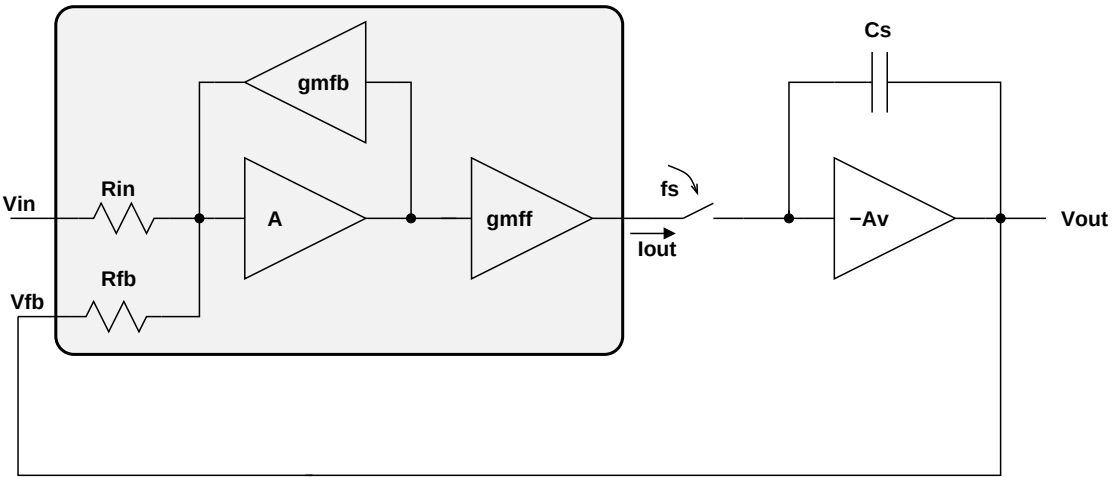


Figure 2.7: Low distortion closed-loop track-and-hold architecture.

To avoid the prohibitively small valued resistors, an extra degree of freedom needs to be introduced which decouples the choice of the resistor size from the circuit bandwidth. The novel circuit architecture that achieves this goal is shown in Fig. 2.7. Inside the shaded box is the G_m block, detailed to show the constituent parts. Resistors sub-

tract the output from the input and since these resistors are linear, passive elements, they will not introduce any significant distortion. The summing node, S, is held at virtual ground by the amplifier block, A, and the local G_m feedback block, G_{mfb}. The feedforward transconductance, G_{mff}, converts the error voltage to a current to charge the hold capacitor. The amplifier, $-Av$, drives the output.

Considering just the input transconductor block transfer function, from the input, V_{in}, to the output current, I_{out}, is:

$$\frac{i_o}{V_{in}} = \left.\frac{G_{in}g_{mff}}{g_{mfb}+\frac{G_{in}}{A}}\right|_{\frac{G_{in}}{A}<<g_{mfb}} \approx G_{in}\frac{g_{mff}}{g_{mfb}} \tag{2.10}$$

where G_{in} is $\frac{1}{R_{in}}$, A is the gain of the amplifier, g_{mff} is the conductance of the feedforward transconductor and g_{mfb} is the conductance of the feedback transconductor. By modifying the ratio of the feedforward conductance to the feedback conductance, a reasonably sized resistor can be used while maintaining the same track-and-hold bandwidth. For example, from Eq. (2.9) for 16 bit settling accuracy at 100MS/s with a 20pF capacitor, the input resistor size is 20Ω. Using Eq. (2.10) with a $\frac{g_{mff}}{g_{mfb}}$ ratio of 10, the resulting resistor size is 200Ω. This reduces both the loading on the previous circuit driving the track-and-hold and the output current of the hold amplifer at the output of the track-and-hold, resulting in easier integration and lower power consumption.

Referring back to Fig. 2.7, it is seen that V_{in} is converted from a voltage to a current by the input resistor R_{in}. This current is summed on the other side of the resistor with the feedback current through R_{fb} to create an error signal. The voltage at this node is measured with the error amplifier, A. This amplifier provides gain which reduces errors,

improves linearity and maintains the summing node at virtual ground. The G_{mfb} output is the negative of the error current which cancels the error current at the summing node. The G_{mff} block provides the current which charges the hold capacitor, C_s.

The amplifier, $-A_v$, with the hold capacitor, C_s, functions as an integrator, integrating the error current onto the hold capacitor. The voltage at the output of the integrator, V_{out}, provides both the feedback signal for R_{fb} and the final output of the track-and-hold.

The switch element in the feedforward path provides the track and hold functionality. When the switch is closed, the system tracks the input signal, keeping the voltage across hold capacitor, C_s, equal to the input voltage. When the clock changes state, the switch opens, disconnecting the error current from the integrator, preventing current from being integrated onto the hold capacitor. In this state the voltage across the hold capacitor does not change, and therefore V_{out}, the output of the track-and-hold, is held constant.

2.4 Track-and-hold Circuit Design

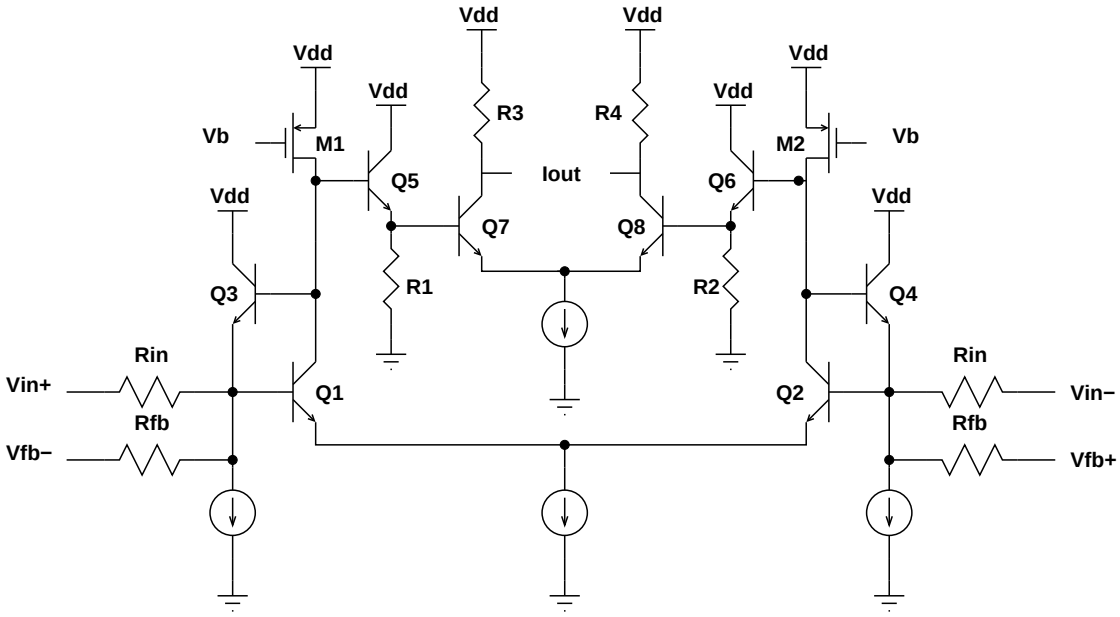
To achieve the necessary specifications of 100MS/s sample rate while maintaining the high linearity of 95dB SNDR (15 bits), a closed-loop track-and-hold must be built in a process that has high bandwidth transistors. For low current consumption, the small signal transistor transconductance, gm, must be high for a specific bias current. With this in mind, the track-and-hold was designed in IBM's 7HP SiGe BiCMOS processes, taking advantage of the 120GHz f_t NPN bipolar transistors and the 0.18μm CMOS transistors. The NPN transistors in this process are designed to work up to a 2.5V supply voltage. There are three varieties of CMOS transistors, standard 1.8V and 2.5V

ones and a thick gate oxide transistor that can operate at 3.3V.

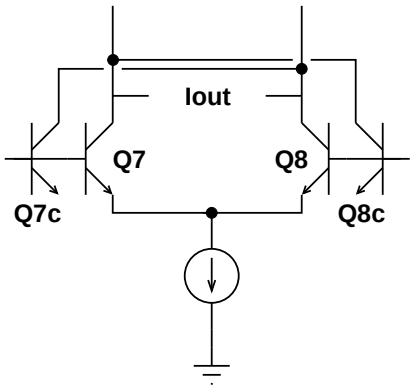
To achieve the full performance that this architecture promises, careful circuit design is critical. There are three major blocks to the modified closed-loop track-and-hold of Fig. 2.7. These blocks are the input transconductor, the switch element, and the output amplifier.

The schematic of the resistor-based transconductor is shown in Fig. 2.8. The schematic has been annotated to show the various functional blocks contained in Fig. 2.7. The shaded regions show each of the functional blocks. At the input are the input resistors, connected at the summing node, S, to the input of the amplifier, A and the G_{mfb}. In the center of the circuit is the G_{mff} circuitry. Starting with the input, the input and feedback resistors are R_{in} and R_{fb}, respectively. The A block of Fig. 2.7 is composed of $Q_{1,2}$ and associated load transistors $M_{1,2}$. The G_{mfb} block is created from the transistors $Q_{3,4}$ and the associated tail currents. The combination of amplifier, $Q_{1,2}$, and feedback, $Q_{3,4}$ can also be viewed as a voltage regulator which keeps the summing node at the base of $Q_{1,2}$ at a fixed voltage. The G_{mff} block in Fig. 2.7 is made of the differential pair $Q_{7,8}$ in association with the tail current source. The load resistors $R_{3,4}$ provide bias current for the OTA as well as setting the output common-mode at a fixed value. $Q_{5,6}$ in conjunction with $R_{1,2}$ level shift the output of the error amplifier A to maintain signal swing and allow the circuit to operate at lower supply voltages.

This circuit is designed to meet specifications as a building block for covergent communications systems, where relatively wide bandwidth and high linearity are key requirements. The track-and-hold is designed to provide 15 bits or 90dB of SNDR at a sample rate of 100MS/s. The sampling capacitor, calculated based on signal swing and



(a) Overall transconductor schematic.



(b) C_{bc} compensation.

Figure 2.8: The resistor-based transconductor.

noise ($\frac{kT}{C}$), is 20pF in size. To achieve the necessary bandwidth for complete settling, using Eq. (2.9), a G_m of $50mS$ is required. Using Eq. 2.10, a $\frac{g_{mff}}{g_{mfb}}$ ratio of 10 is chosen to give an input resistor size of 200Ω.

Transistors Q_1 and Q_2 that compose the main part of the amplifier (A) are sized

with the collector current at 2.5mA, to maximize bandwidth and provide adequate gain for the linearity and stability requirements. Transistors Q_3 and Q_4 constitute the g_{mfb} part of the circuit and are sized to compensate for the current from a 0.5V difference between the input signal across the 200Ω input resistor and the 200Ω feedback resistor. This results in a bias current of 2.5mA. The $\frac{g_{mff}}{g_{mfb}}$ ratio is set by the ratio of current between $Q_{3,4}$ and the feedforward block of $Q_{7,8}$. This dictates that the current through $Q_{7,8}$ is 25mA.

The relatively large current through $Q_{7,8}$ means that to keep the current density of the transistors within acceptable limits, the transistors must be large. As the NPN transistor increase in size, the capacitance between the base and the collector, C_{bc} also increases. This capacitance creates a zero in the transconductor transfer function, thus degrading the phase margin of the transconductor and making the overall track-and-hold difficult to stablize. To compensate for this zero, extra NPN transistors are added to the transconductor. These are shown in Fig. 2.8. By connecting $Q_{9,10}$ across the differential pair, $Q_{7,8}$, in this manner, the zero can be approximately canceled by providing a matched capacitance that is connected to the opposite side of the amplifier [32]. A similar scheme is employed to compensate for the zeros of $Q_{1,2}$.

The switch element is the next circuit block examined. The switch is inside the feedback loop and connects the sampling capacitor to transconductor output. The switch on-resistance is not critical since one side of it is connected to a relatively high impedance current source. This means that the switch can be very small, thus reducing clock coupling and charge injection. With these relaxed requirements, a simple NMOS switch can be used instead of a complex switch with compensation schemes such as clock boosting.

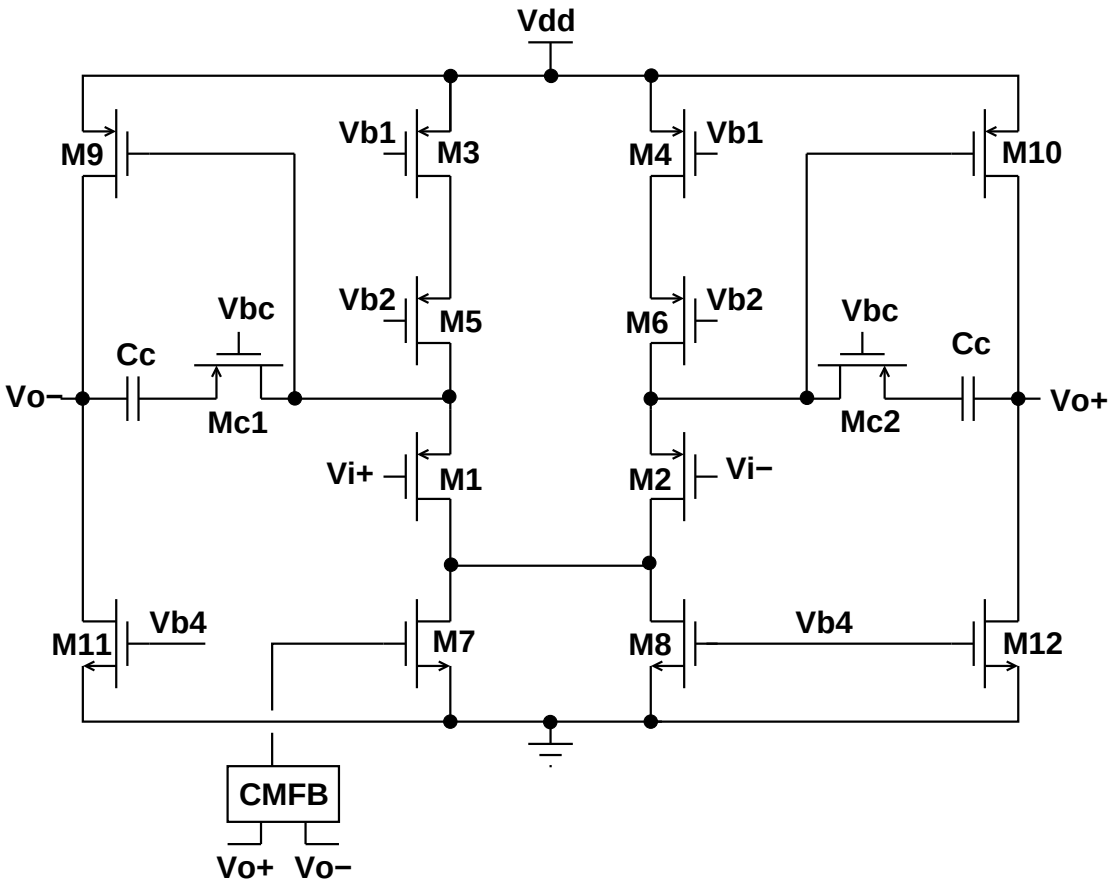


Figure 2.9: Hold capacitor amplifier.

The final circuit block in the track-and-hold is the hold amplifier. A two-stage CMOS amplifier is used in this design. The amplifier, Fig. 2.9, consists of a differential pair, $M_{1,2}$, and active load $M_{3,4}$ followed by the output stage M_{5-10}. The common mode feedback circuit consisting of M_{12-14} sets the output common mode by adjusting the differential pair tail current [33]. The major design requirement is providing the slewing currents required to charge the hold capacitor. For a hold capacitor of $20pF$, the current in the output branch must be 25mA. The amplifier is designed to have a open-loop gain

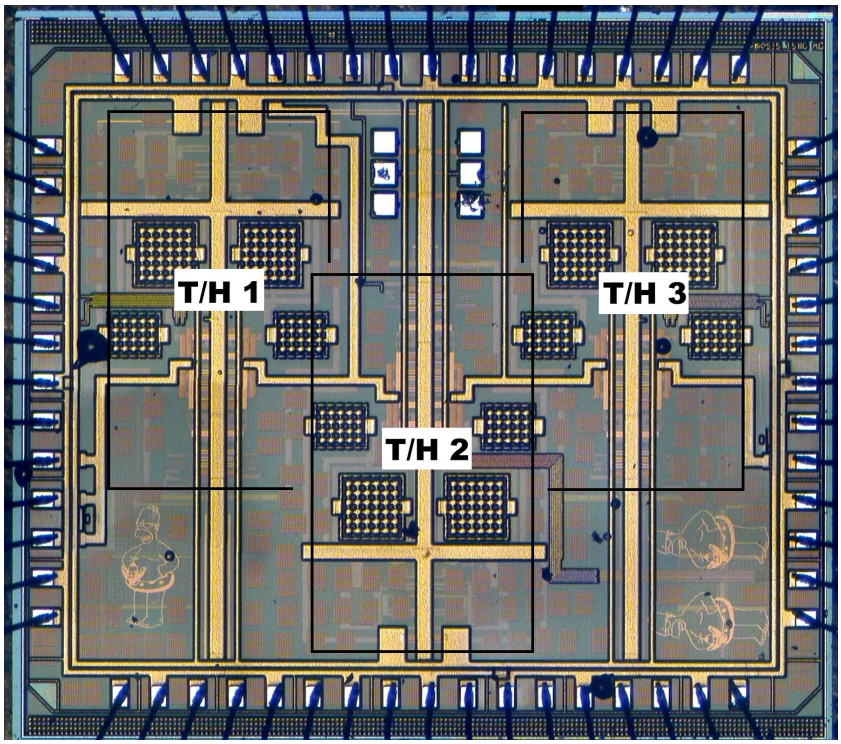
of 45 dB and a unity gain bandwidth of 800 MHz. This relatively low amplifier gain is sufficient because the track-and-hold feedback loop compensenates. However, wide bandwidth is important to preserve overall loop stability. Since the main pole of the closed-loop track-and-hold is set by the transconductor G_m and the hold capacitor, to maintain loop stability any second poles such as the hold amplifier pole must be high enough in frequency to not affect the main loop phase margin.

2.5 Simulations and Experimental Results

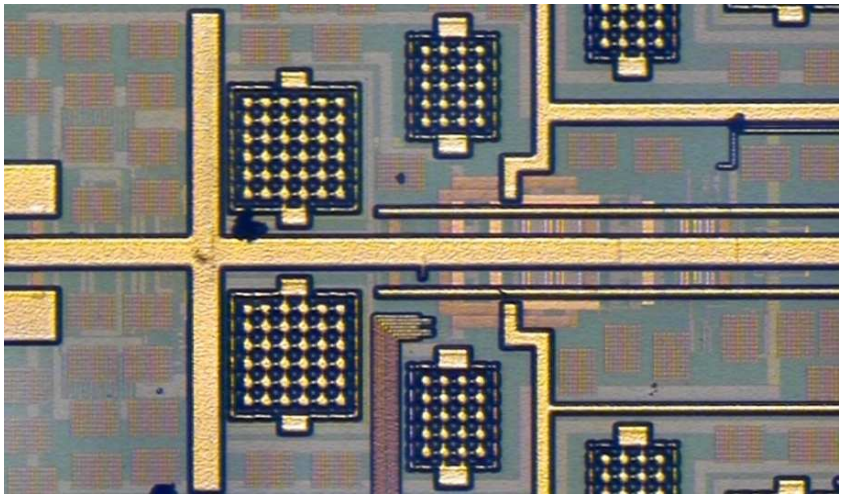
This design is integrated in IBM's 7HP BiCMOS process with 6 metal layers occuping a total active area is 3 x 4 mm^2. The die photo is shown in Fig. 2.10(a) and includes 3 separate, identical track and hold circuits. A close-up photo of a single track-and-hold is shown in Fig. 2.10(b) and occupies 1.2 x 2 mm^2. The blocks of the track-and-hold, starting at the inputs on the left are the input and feedback resistors which are interdigitated for matching. These are followed by the transconductor. The switch elements come next, followed by the hold capacitors. The final block is the hold amplifier.

The 20pF hold capacitor is implemented as a MIM capacitor on the metal layer 5 and each one occupies an area of 400um x 400um. Using a MIM capacitor reduces parasitic capacitance and because of the metal and oxide used in construction, it has a very low voltage coefficient making it very linear. Next to the capacitor is the switch and driver. The switch is made of a single NMOS transistor with a size of $\frac{200um}{0.6um}$.

The transconductor block is shown in Fig. 2.10(b). The input transconductor is a critial block in this design with a total current consumption of approximately 70mA



(a) Complete die photo.



(b) Single track-and-hold die photo.

Figure 2.10: Track-and-hold die photos.

at 2.5V. The majority of that current, 50mA, flows through the G_{mff} block. The two transistors in this block, $Q_{7,8}$, have collector currents of 25mA each. With such large currents, proper layout is critical to provide matching between the transistors and maintain constant temperature across both transistors. The final block is the hold capacitor amplifier as shown on Fig. 2.10(b). Each branch of the amplifier is biased at 25mA, resulting of a total current consumption of 100mA to meet the slewing requirements. The input transistors, sized for these currents have a $\frac{W}{L}$ of $\frac{2000\mu m}{0.38\mu m}$. The layout and routing for such large currents is an issue, making the amplifier significantly larger than just the transistor area alone. With a maximum current density of 500μA per 1μm of width, the metal routing for the amplifier has to be wide and use several layers to carry all the current. A via resistance of 10Ω means that most of the connections in the amplifier require a "sea of vias" to lower the inter-metal connection resistance. Routing large power busses on the upper, thicker copper metal layers, with their significantly increased current carrying capacity, provides stable, low impedance power supply routing to the amplifer. Careful layout and judicious interdigitation are vital to proper operation of this circuit.

Testing a high-speed, high accuracy track-and-hold (T/H) presents some unique challenges. If the track-and-hold performance is comparable or better than available ADCs, there is no easy way to measure the T/H output at full speed and at the full accuracy. To circumvent this problem, one T/H is connected to another identical T/H so that the second T/H sub-samples the output of the first T/H. This test system is shown in Fig. 2.11. The sub-sampled output of the second T/H is held for a much longer time so that it can be accurately measured by a slow, but very accurate ADC. The origonal

output signal of the first T/H circuit can then be reconstructed. This reconstruction is illustrated in Fig. 2.12. The first T/H is clocked with a clock running at F_s. The second T/H is then clocked at $\frac{F_s}{1+N}$ where N is a large number. After N samples, it is possible to reconstruct one period of the output of the first T/H circuit. To have the minimum negative effect on the performance, the parasitics between the T/Hs are minimized. This is accomplished by connecting one T/H to another on the same silicon die. This can be seen in Fig. 2.10(a) where T/H_1 and T/H_2 are connected together with separate clock inputs and T/H_3 is a single T/H to aid in debugging.

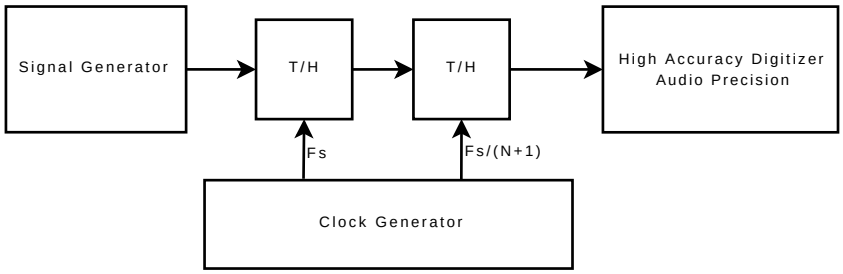


Figure 2.11: Experimental Test Setup.

A printed circuit board (PCB) was created with chip and associated support circuitry on it. The PCB is designed using chip-on-board (COB) technology to provide the lowest parasitic packaging possible. The chip is positioned in the center of the board and can be clearly seen in Fig. 2.13. The rest of the circuitry is placed around the board to provide the best connection paths while allowing room to probe the chip using RF probes if necessary.

The time domain response of the track-and-hold is shown in Fig. 2.14. Fig. 2.14 (a) shows a complete input cycle of a 3.125MHz input signal sampled at 50MS/s. Part (b) of the figure shows a single sample of the same waveform where slewing, tracking, and

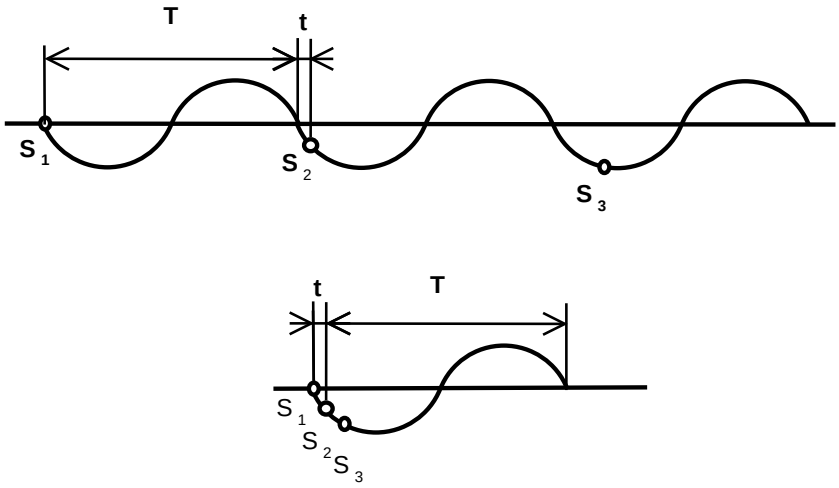


Figure 2.12: Reconstruction of T/H output.

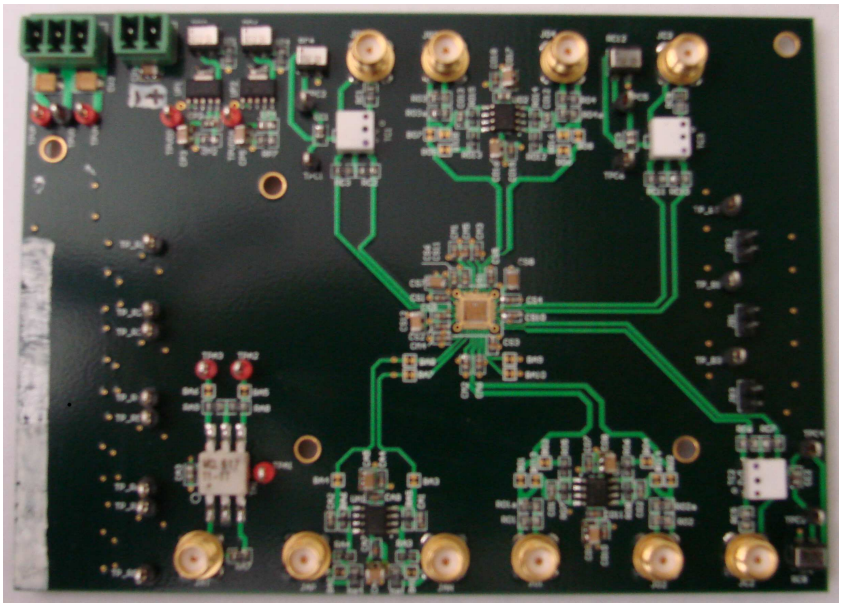


Figure 2.13: PCB photograph showing chip on board.

holding parts of the sample can be clearly seen. When the clock switches from hold mode to track mode the track-and-hold initially slews to begin tracking the input signal.

Once the sampling switch opens again, the track-and-hold goes into hold mode where it no longer tracks the input signal but keeps the output held at a constant level that is equal to the signal level the instant the switch is opened.

Fig. 2.15 shows the frequency spectrum for various sample rates and input frequencies. Fig. 2.15 (a) shows the results for a 50MS/s sample rate, with a SNDR of over 16 bits. Fig. 2.15 (b) shows the results for a 100MS/s sample rate, and an SNDR of approximately 15 bits. In both of these plots, the input tone plus the first 3 harmonics of the input signal are visible. The noise floor, dominated by flicker noise in the low frequency region, is below 100dB. The total SNDR of the system is limited by the power in the first harmonic.

The final specifications from simulation and testing are summarized in Table 2.2. The simulation results show an SNDR ranging from 98.7dB (16.4 bits) at 50MS/s down to 84.4dB (14 bits) at 400MS/s.

	Simulation
Supply Voltage	2.5V
Supply Current	220mA
SNDR @ 50MS/s	98.7dB
SNDR @ 100MS/s	89.4dB
SNDR @ 200MS/s	89.3dB
SNDR @ 400MS/s	84.4dB
Signal Feedthrough:	
0-100MHz	$<$-92dB
above 100MHz	$<$-65dB
Signal Bandwidth (-3dB)	156MHz

Table 2.2: System Specifications

The simulated performance of this track-and-hold has been compared to other pub-

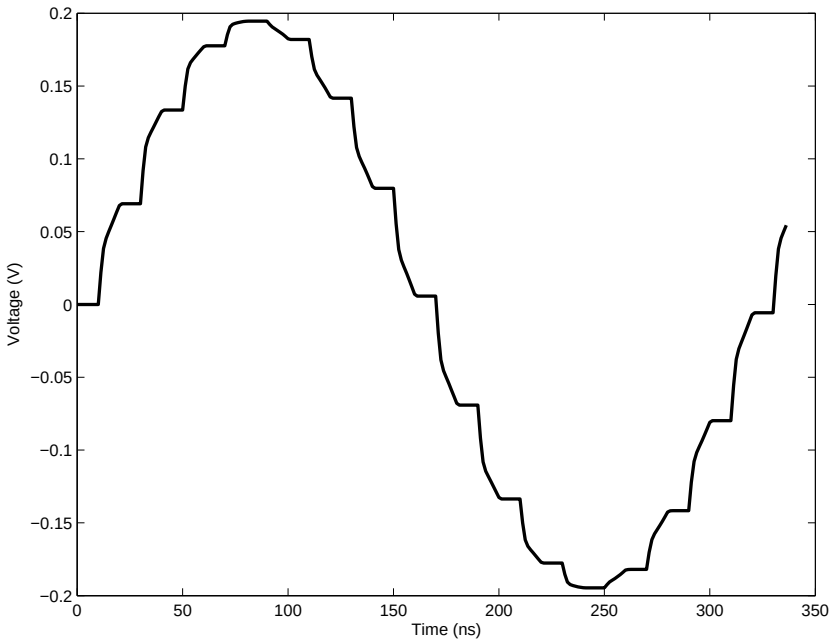
lished T/Hs in Fig. 2.17 [23, 34, 35, 36]. The first plot, Fig. 2.17(a), plots resolution as a function of power consumption. This work, shown as the circles in the upper right quandrant, achieves the highest SNDR for the power consumption. The second plot, Fig. 2.17(a), plots resolution as a function of sample rate. Again, this work is represented by circles. Operating the track-and-hold at various frequencies results in multiple circles showing different performance points. For the sample rate this track-and-hold achieves the best performance of any track-and-hold currently published.

Initial testing of the track-and-hold chip resulted in the discovery of several ESD diodes that had been connected backwards. This caused a short circuit from the power rails to ground. The chip was processed by Evans Analytical Group using Focused Ion Beam (FIB) Milling to attempt to removed the diode connections. Testing of this processed chip reveiled a second short circuit in the common-mode feedback of one of the track-and-holds. This short was discovered using infrared imaging and is shown in Fig. 2.16. The origin of this short is still unknown since it is only in one of the three identical track-and-holds. Subsequent FIB attempts we not successful in removing all shorts since FIBing the thick copper metal layers in the process is difficult.

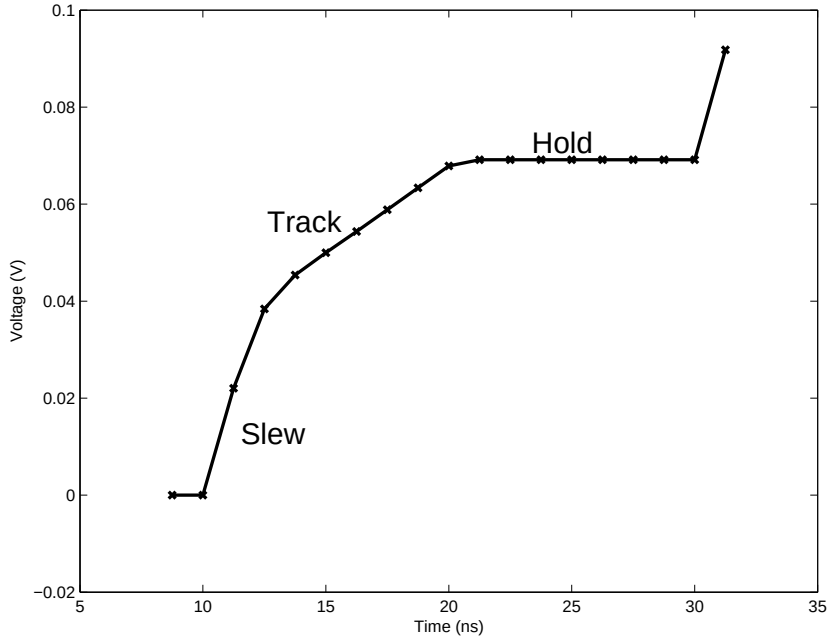
2.6 Conclusions

A 2.5V BiCMOS track-and-hold that achieves a simulated SNDR ranging from 98.7dB (16.4 bits) at 50MS/s down to 84.4dB (14 bits) at 400MS/s has been presented. The use of a modified transconductor in the closed-loop architecture and a BiCMOS process were crucial in achieving this high performance design. The circuit operates on a single

2.5V supply and consumes 220mA of current. This design is an important achievement in the design of higher and faster data converters and other mixed signal circuits.

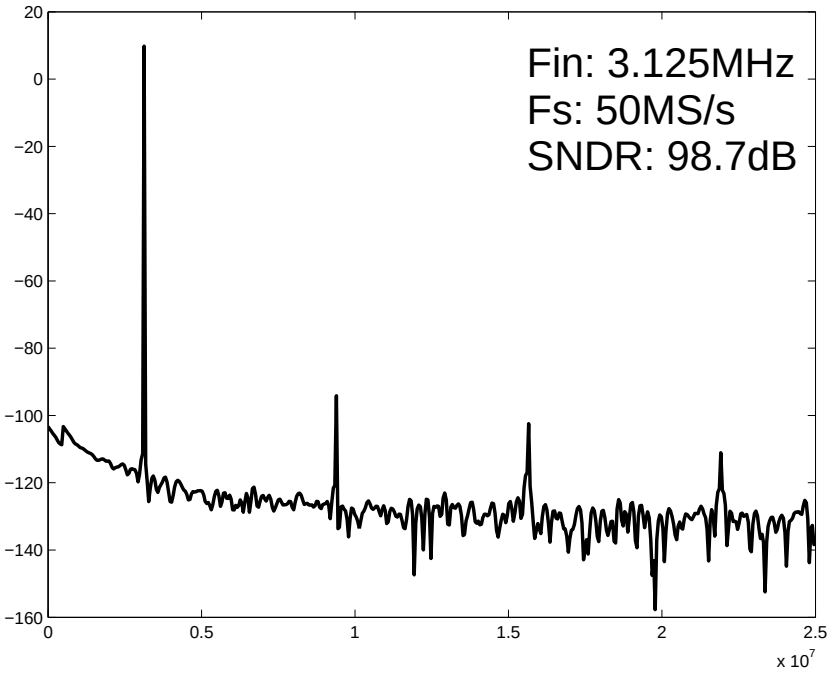


(a) Single Cycle

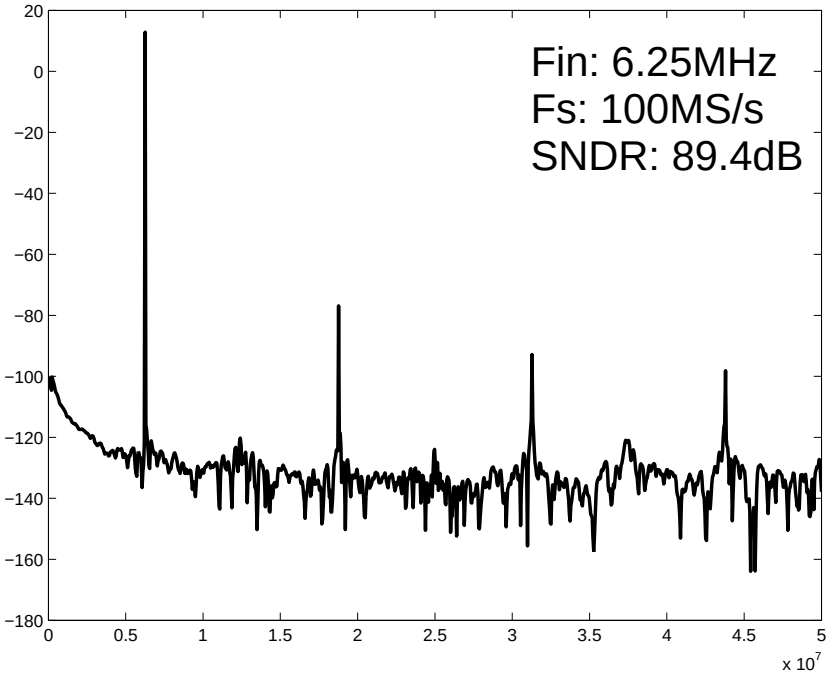


(b) Single Sample

Figure 2.14: Simulated time-domain track-and-hold output from post-layout extraction.



(a)



(b)

Figure 2.15: Simulated frequency domain track-and-hold output from post-layout extraction.

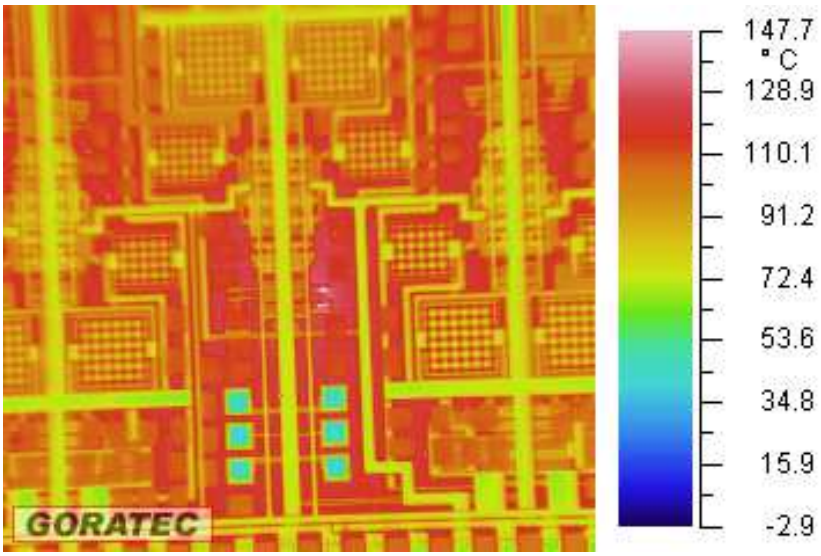
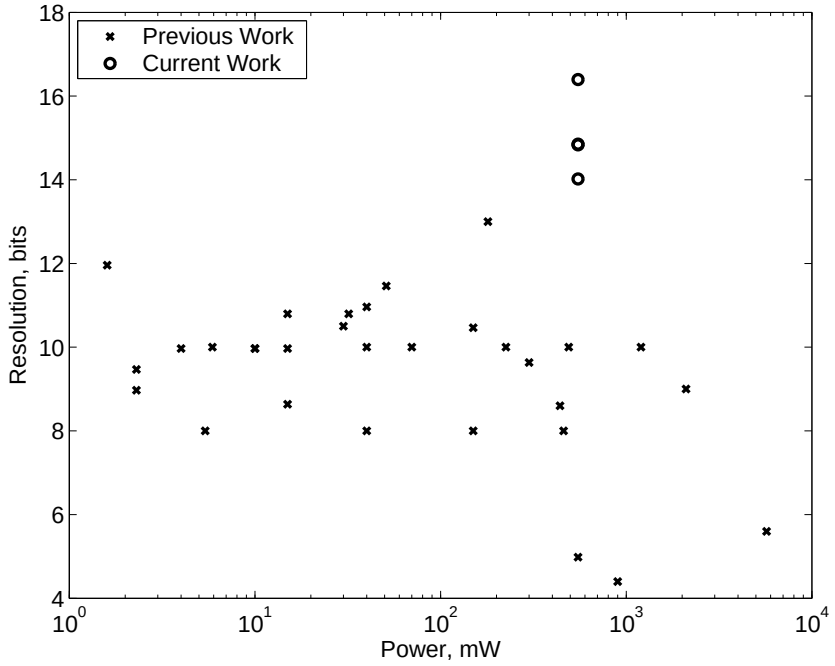
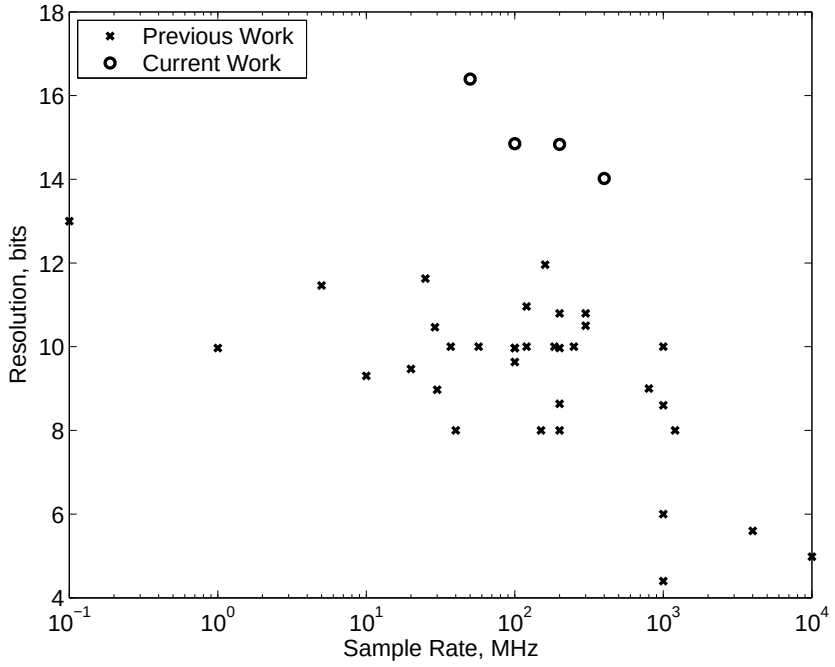


Figure 2.16: Temperature of the track-and-hold.



(a)



(b)

Figure 2.17: Comparison to previously published track-and-holds.

Chapter 3 – A Parallel $\Delta\Sigma$ ADC Architecture for Covergent Systems

3.1 Introduction

A high-speed, high-resolution $\Delta\Sigma$ architecture is introduced that combines parallelism and a shared multi-bit quantizer. This architecture provides significantly reduced power and area consumption compared to conventional parallel $\Delta\Sigma$ ADCs, while maintaining high resolution [18]. The architecture uses a reduced sample-rate Leslie-Singh channel to enable sharing of one second stage ADC between the parallel channels. This results in reduced power consumption and smaller chip area.

The design in this paper achieves 16 bits of resolution, with a 4 times oversampling ratio using a parallel system with four third-order channels and one 9-bit second stage. The paper is organized as follows. In Section 2, we review the parallel $\Delta\Sigma$ architecture and discuss the reduced sampling MASH architecture. In Section 3 the new architecture improvements are discussed. Analysis and a design example are presented in Sections 4 and 5. Section 6 contains the simulation results followed by the conclusion.

3.2 Architecture

Traditionally to increase the bandwidth of a $\Delta\Sigma$ A/D converter while maintaining the required resolution, either the order of the system is increased and the zeros of the system optimized or the sample rate of the system is increased or both. If parallelism is

used then the bandwidth can be adjusted independent of the order of the $\Delta\Sigma$ modulator and to some degree the sample rate of the system.

The parallel $\Delta\Sigma$ architecture is shown in Fig. 3.1. It consists of a front-end signal modulator, a set of standard $\Delta\Sigma$ A/D converters, digital filtering, signal demodulation and recombination to form the overall digitized output [37, 38]. The modulation sequence decouples the input signal from the quantization noise of each channel to provide a performance increase such that doubling the number of channels increases the resolution in a similar fashion to doubling the oversampling of a single $\Delta\Sigma$ modulator.

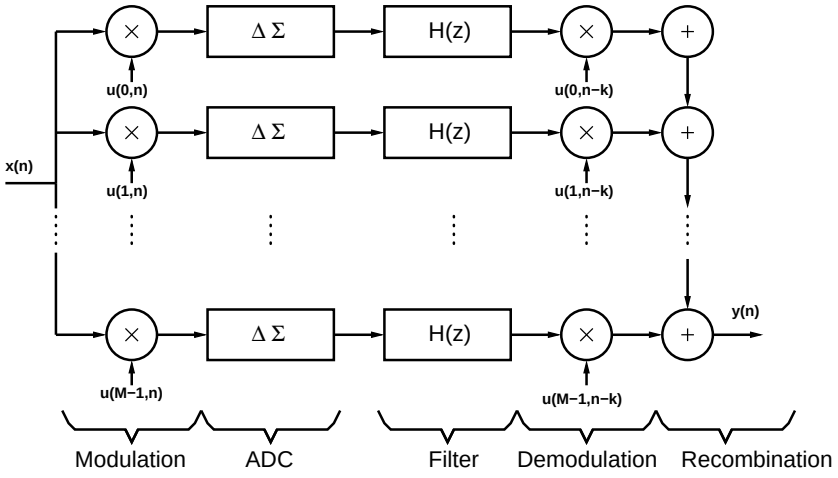


Figure 3.1: Parallel $\Delta\Sigma$ ADC architecture.

The modulation sequences can be any unitary orthogonal basis set. For ease of implementation, useful modulation schemes consist of pass, cross, or disconnection of the input signal. This corresponds to a sequence that contains +1,-1, and 0, respectively. The Hadamard sequence gives a performance increase of L bits for every doubling of number of channels [37]. However, the area requirements of the filter make practical implementation less desirable. An alternative modulation scheme uses a time-interleaved

approach [38]. With this approach, performance of $L - \frac{1}{2}$ bits for every doubling is achieved. The lower performance of the time-interleaved scheme is offset by the reduction in chip area and architecture complexity.

An example of other applications of this modulation is using the front end modulation to increase the SNR of the signal entering the ADC [19]. Assuming that the signal is coded when it is transmitted, providing the decoding at the input to the ADC helps decorrelate the signal and noise and provides extra signal gain. The result is a better overall SNR without increasing the SNR performance of the ADC. This architecture can accommodate low-pass, bandpass and high-pass $\Delta\Sigma$ modulators. Bandpass parallel structures require unique modulators, each with a different center frequency, on each channel which increases the design complexity considerably. Low-pass parallel structures are simpler since identical modulators are used on each channel. The need for high resolution and low oversampling requires high-order low-pass $\Delta\Sigma$ modulator with a multi-bit quantizer.

An attractive solution to a high-order low-pass $\Delta\Sigma$ modulator with a multi-bit quantizer is the Leslie-Singh architecture as shown in Fig. 3.2 [39]. It consists of two stages. The first stage is a standard $\Delta\Sigma$ modulator with a single bit feedback. The second stage is a multi-bit Nyquist-rate ADC which digitizes the quantization noise of the first stage. The digitized noise from the second stage is processed with a digital filter which simulates the noise transfer function of the first stage and is then subtracted from the digital output.

An improvement to the Leslie-Singh architecture is shown in Fig. 3.3 [40]. The decimation is transfered from the output to between the first and second stages. The

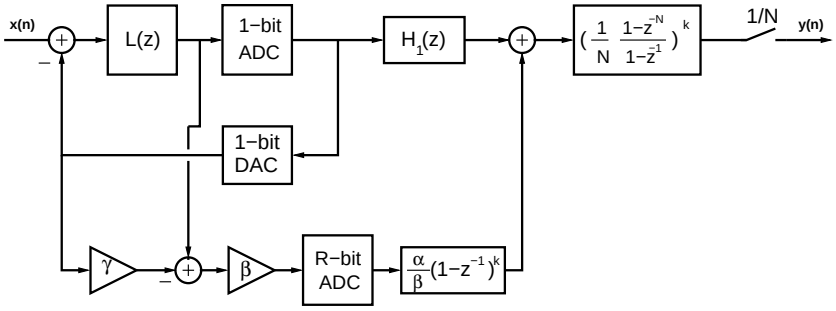


Figure 3.2: A Leslie-Singh $\Delta\Sigma$ modulator.

second stage ADC is then clocked at a rate lower than the first stage $\Delta\Sigma$ modulator. Thus, the decimation relaxes the speed requirements of the multi-bit ADC at the expense of a 3dB loss in resolution for every doubling of the decimation rate [40].

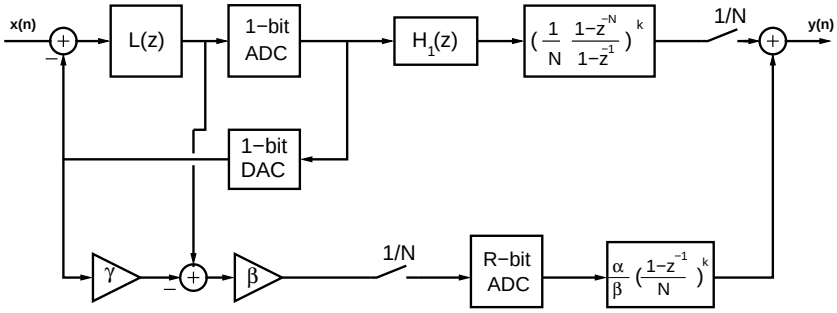
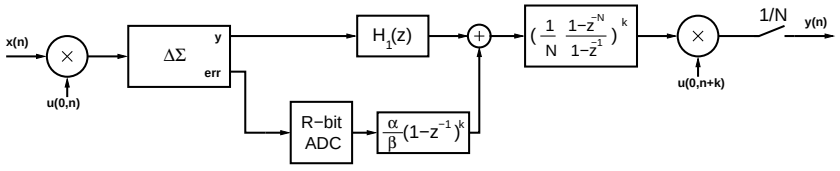


Figure 3.3: A reduced sample rate Leslie-Singh $\Delta\Sigma$ modulator.

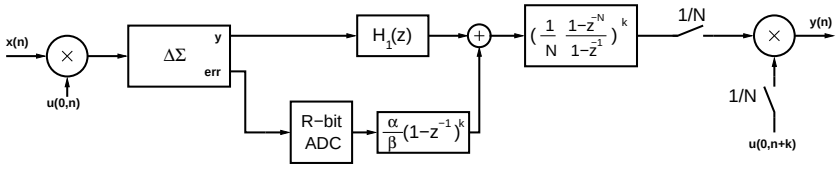
3.3 Parallel $\Delta\Sigma$ with the Shared ADC

Using the Leslie-Singh architecture in a parallel $\Delta\Sigma$ system results in the replication of the second stage ADC on each channel. This replication leads to excessive power and chip area requirements. This can be partially avoided if the reduced sample rate Leslie-Singh architecture is integrated into the parallel system as described next.

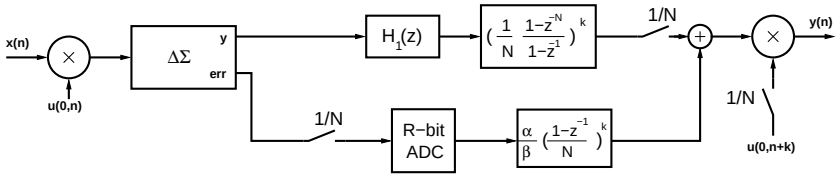
A single parallel channel with a Leslie-Singh ADC is shown in Fig. 3.4(a). This is a complete channel without the digital recombination section. The decimation is performed at the end of the channel after all the other signal processing steps have been performed.



(a) The original single channel.



(b) The channel with the decimation transferred.



(c) A reduced sample rate channel.

Figure 3.4: Sequence from standard to reduced sample rate channel.

The first step in implementing the reduced sample rate Leslie-Singh architecture is transferring the channel decimation to the left side of the demodulator. To do this the demodulation sequence and the input to the demodulator have to be decimated. The channel with the decimator transferred is shown in Fig. 3.4(b).

The final step is transferring the decimator inside the Leslie-Singh ADC to produce the reduced sample rate Leslie-Singh modulator. The channel is shown in Fig. 3.4(c).

By setting the decimation rate equal to the number of shared channels in the system,

and delaying the decimation in each channel by one clock cycle, the channels can share the second stage between two or more channels. By setting the decimation rate equal to the number of channels, the second stage can be shared between all the channels. This is shown in Fig. 3.5 for a four channel system.

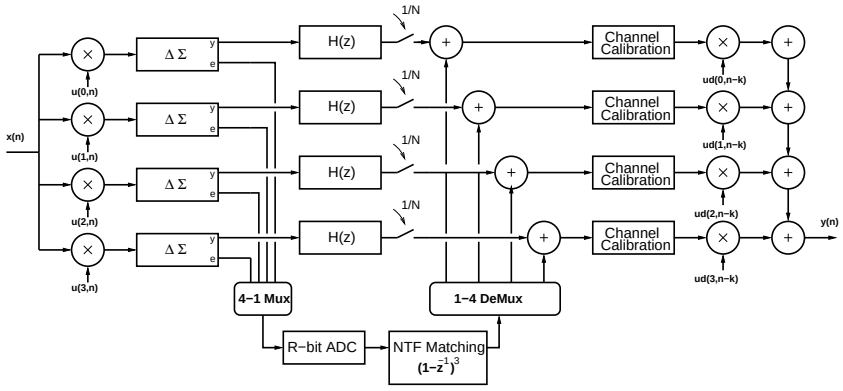


Figure 3.5: Complete parallel system.

This system minimizes the chip area and power needed for the converter while extending the bandwidth and resolution. The modular construction of the system and the programmable modulation sequences provide a design flexibility that is impossible for most converters. When integrating this ADC into a system which can modify its operation, for example a DSP engine, the ADC can then be modified to change the conversion bandwidth, perform additional signal processing using the modulation sequences, or to convert several signals at once. For example, by modifying the modulation sequence, quadrature modulation/demodulation can be performed at the input to the ADC.

3.4 Analysis

Predicting the overall system parallel $\Delta\Sigma$ ADC system performance is an important step in determining the optimum system configuration. Parameters such as number of parallel channels, OSR and channel order can be varied to find this optimum point. To determine the theoretical maximum SNR of the overall parallel $\Delta\Sigma$ ADC, the performance of a single channel is shown and the expanded to show the overall system performance.

For a single channel consisting of a reduced sample rate A/D converter [40], the SNR is given by

$$\begin{aligned} SNR =& 6.02(R + (L + 0.5)log_2 OSR - 0.5log_2 N) \\ &+ 20log\frac{\beta\sqrt{2L+1}}{\alpha\pi^L} + 1.76 \end{aligned} \tag{3.1}$$

where R is the resolution of the second stage, L is the order of the $\Delta\Sigma$ modulator, OSR is the oversampling ratio, N is the decimation between the first and second stage, and α and β are the MASH coefficients. From (3.1), the resolution of the A/D converter is a combination of R, the second stage ADC resolution, $(L + 0.5)log_2 OSR$, which is the resolution gain due to doubling the OSR, and $-0.5log_2 N$ which is the loss in resolution due to the decimation. The remainder of the equation gives an approximate starting point for a L-th order $\Delta\Sigma$ ADC.

When the reduced sample rate A/D converter stage is placed in an M channel parallel system, (3.1) must be modified. As stated before the resolution of the system is dependent on the number of channels, and the modulation sequence. Thus, for every

doubling of the number of channels for time-interleaved modulation, the resolution increases by $L - 0.5$. If the decimation between the first and second stages is equal to the number of channels, resulting in one shared second stage, then the decimation rate is M. Combining these two effects with the $-0.5log_2N$ from the above equation, the theoretical operation of the parllel $\Delta\Sigma$ system can be given by:

$$\begin{aligned} SNR =& 6.02(R + (L + 0.5)log_2OSR + (L - 1)log_2M) \\ &+ 20log\frac{\beta\sqrt{2L+1}}{\alpha\pi^L} + 1.76 \end{aligned} \tag{3.2}$$

where M is the number of channels and all other parameters are defined above.

3.5 Design Considerations

An architecture is needed that will obtain 16-bit resolution with a low oversampling ratio, while minimizing chip area, complexity, and power. The proposed architecture is configured as a four channel system using the time-interleaved modulation with an overall oversampling rate of 8. Each channel consists of a third-order modulator and digital filters. A single 9-bit pipeline A/D converter is shared between all of the channels. This basic architecture is show in Fig. 3.5. The channel calibration removes any gain and offset mismatches between the channels which would cause tones in the output signal. The channel calibration is implemented with some basic filtering and a simple digital $\Delta\Sigma$ modulator [41, 42]. These issues are described in more detail in Chapter 4.

3.6 Simulation Results

The system was simulated in both MIDAS and Matlab. The results are for a four channel, 3rd order, 8X OSR parallel $\Delta\Sigma$ modulator with a 9 bit second stage ADC. The spectrum is shown in Fig. 3.6 and the dynamic range plot is shown in Fig. 3.7. The spectrum is for a sinusoidal input signal with an input frequency at $\frac{1}{16}$ of f_s. The amplitude is at the maximum dynamic range point. The humps in the noise on this plot are normal in a parallel $\Delta\Sigma$ and are an artifact of the noise transfer functions of the individual channels and the multi-path nature of the system. Fig. 3.7 shows the dynamic range of the A/D converter. At the maximum dynamic range point, the system has 101dB of dynamic range or 16.7 bits.

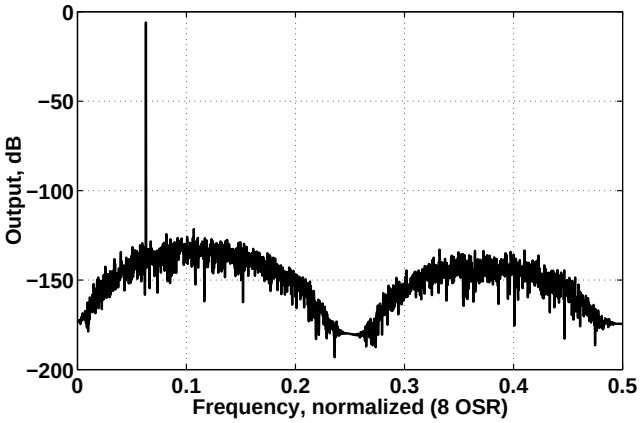


Figure 3.6: Power spectral density of the output with sinusoidal input.

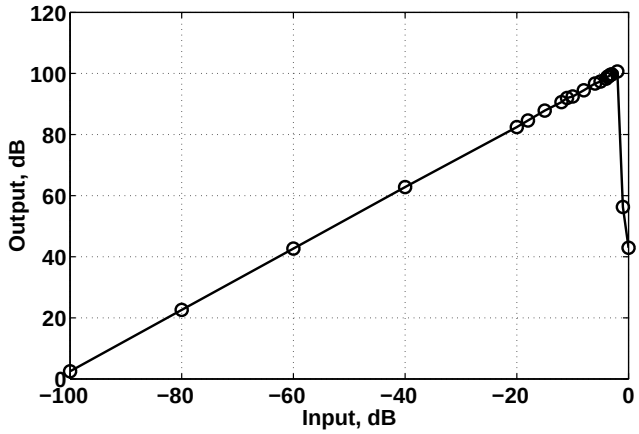


Figure 3.7: The dynamic range of the ADC.

3.7 Conclusions

By using a reduced sample-rate structure for the channels of the parallel ADC, this architecture provides an area and power efficient parallel $\Delta\Sigma$ ADC for high-speed and high-resolution applications. Inherent in this architecture is the added advantages of flexibility and adaptability. It is well suited to sub-micron process. by relying on $\Delta\Sigma$ modulators for process insensitive designs requiring minimal calibration. Being suited to a sub-micron digital process allows this A/D converter to be implemented on a chip with a digital signal processor, thus enabling the processor to adaptively change the operation of the A/D converter to provide the best performance for a variety of signal processing operations.

Chapter 4 – Implementation of a Parallel $\Delta\Sigma$ ADC Architecture

4.1 Introduction

Convergent systems, like the ones described in Chapter 1, require analog-to-digital converters (ADCs) that are high-speed and high-resolution to meet the flexibility and adaptability requirements of the next generation of communication systems. Customers have grown accustomed to a high rate of improvement in technology, especially in the communications markets. With each new version of hardware new specifications evolve to meet customer demands and include the need for new high performance ADCs. To this end, an efficient parallel $\Delta\Sigma$ ADC architecture has been designed that achieves high performance in digital processes, while also providing additional architecture adaptability and flexibility. This flexibility enables the ADC to work equally well over a range of resolutions and bandwidths. The architecture meets the goals of a high speed, high resolution ADC that is suited to demanding convergent systems. This design not only meets the performance specifications, but also provides a level of reconfigurablity and adaptablity not available in other types of converters.

The overall system is designed to provide 15 bits of resolution or 90 dB SNDR with a conversion bandwidth of 25MHz. The following sections describe the implementation of the system architecture. Section 4.2 describes the overall system design, giving specifications for each of the major blocks followed by the implementation details is Section

4.3. Section 4.4 discusses the how the overall system was simulated and shows the results of those simulations. The test bed and associated setup are discussed in Section 4.6 and the results of the experimental measurements are presented in Section 4.7.

4.2 System Design

As previously published in [43] and stated in Chapter 3, the $\Delta\Sigma$ modulator is a 2-1-1 architecture clocked at 100MS/s followed by a shared pipeline ADC and is shown in Fig. 4.1. The 2-1-1 architecture was chosen to make NTF matching possible with this shared last stage architecture. The pipeline ADC has 9-bit resolution and operates at 100MS/s. The calibration and other digital processing block were not implemented on the silicon die but instead in Matlab. This architecture is improved over the traditional parallel $\Delta\Sigma$ ADC by the addition of the blocks in the shaded region. As described in Chapter 3, parallel systems with multiple channels consume significant die area to achieve an increase in performance. A single $\Delta\Sigma$ channel is replicated four times to create a parallel $\Delta\Sigma$ ADC but the last block of each channel is only replicated once and shared between all $\Delta\Sigma$ channels. While the inital part of the parallel system is the same, the quantization error of each channel is fed to a 4-to-1 multiplexer which samples each channel every four clock cycles. The multiplexer output is quantized by the 9-bit pipeline ADC and demultiplexed by the 1-to-4 demultiplexer. This signal is summed with the filtered and decimated $\Delta\Sigma$ ADC output, demodulated, and combined with the signals from the other channels.

A single channel is shown in Fig. 4.2. It consists of integrator blocks, marked with

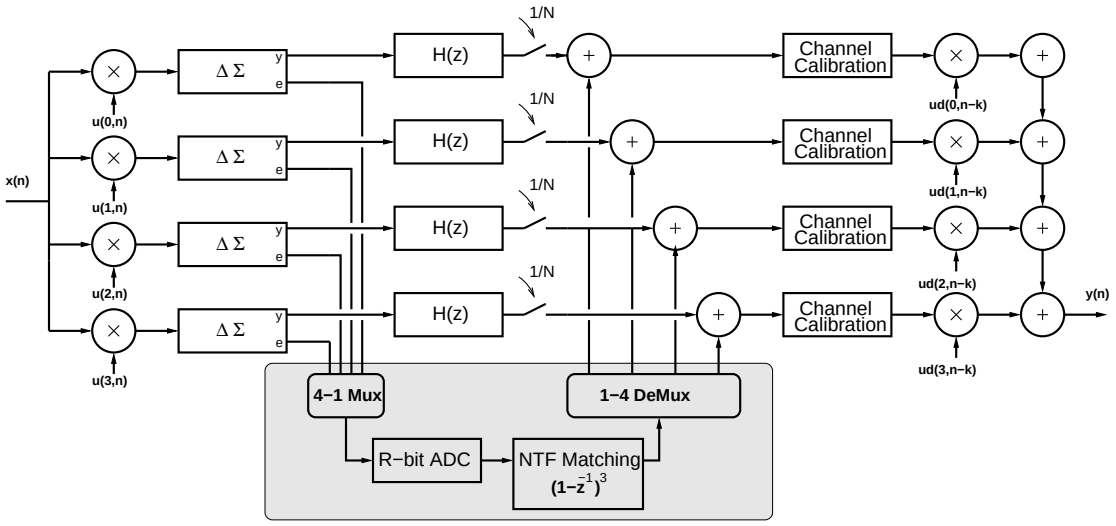


Figure 4.1: A complete parallel system showing shared last stage ADC.

an integration symbol and their scaling terms, quantizer blocks and DAC blocks. The first two integrators, the quantizer and DAC make up the first second-order $\Delta\Sigma$ modulator. The second $\Delta\Sigma$ modulator is first order and consists of an integrator, quantizer and DAC. The third $\Delta\Sigma$ modulator is identical to the the second one. The input signal, $x(n)$, passes through the modulation switches and enters the channel at the first integrator. The quantization error from the first quantizer is sent to the second $\Delta\Sigma$ modulator. The final first order $\Delta\Sigma$ modulator processes the quantization error of the second $\Delta\Sigma$ modulator. The quantization error of the final $\Delta\Sigma$ modulator is sent to the 1-to-4 multiplexer. The digital outputs of each $\Delta\Sigma$ modulator are annotated as $y_{1,2,3}(n)$ and values of the coefficients used in Fig. 4.2 are shown in Table 4.1.

When designing ADCs, there are areas that require special attention. In this design, switch on-resistance, switch signal dependent charge injection and opamp gain and bandwidth are critical specifications that require special attention. Designing switches

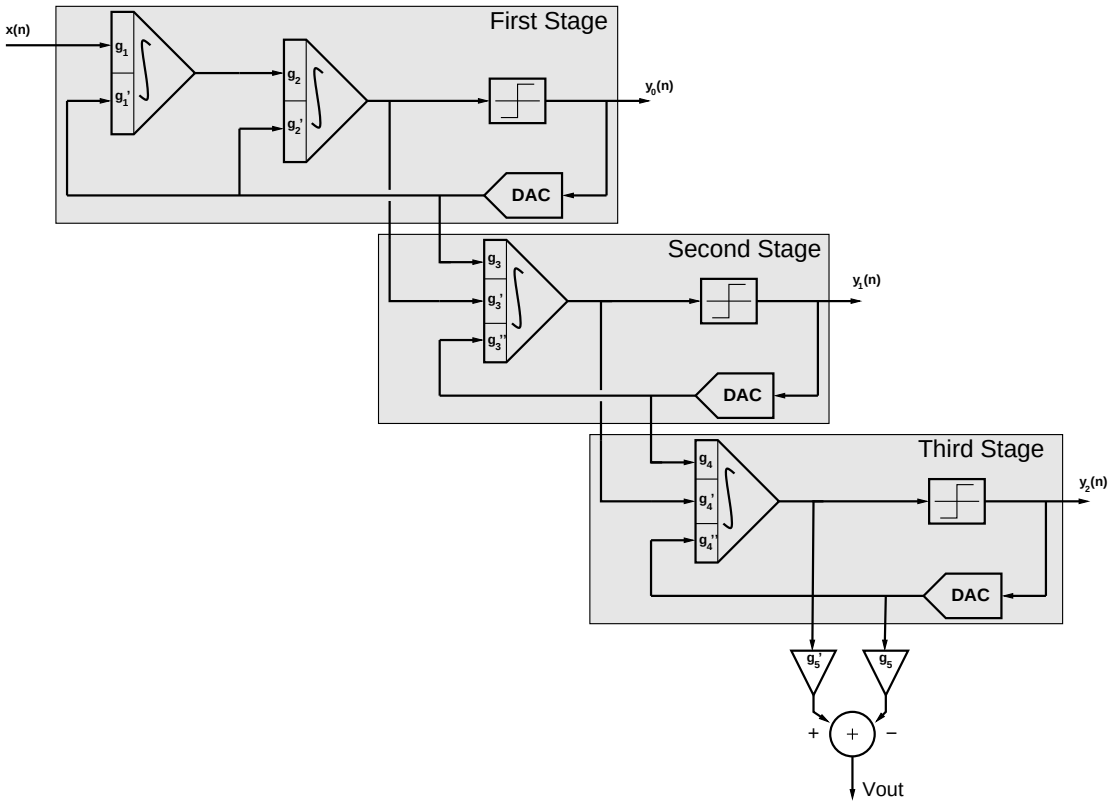


Figure 4.2: A $\Delta\Sigma$ modulator from a single channel of the parallel $\Delta\Sigma$ ADC.

with sufficiently low on-resistance to allow full settling in the required time while minimizing charge injection required the use of clock boosted switches. The opamp design is critical to achieving the overall system performance. This design relies on noise transfer function (NTF) matching to correctly cancel the quantization noise. Thus the opamp gain must be sufficiently high, since sufficient opamp gain is critical for good NTF matching. The opamp bandwidth is important to the performance of the integrators. Incomplete settling can cause coefficient changes for linear settling and an increase in distortion of nonlinear settling. Achieving these specifications required both careful

g_1	0.25	g_3	1.000	g_4'	0.5
g_1'	0.25	g_3'	0.375	g_4''	1.0
g_2	0.5	g_3''	0.25	g_5	2.0
g_2'	0.25	g_4	2.0	g_5'	-2.0

Table 4.1: Parallel ADC channel coefficients.

circuit design and innovative layout.

4.3 Implementation

To meet the desired specifications, the four channel parallel $\Delta\Sigma$ modulator was implemented in TSMC's 0.25um CMOS process. This process has 5 metal layers and 1 poly layer and also includes a MiM capacitor layer above metal 4. Each block in the system was designed to guarantee that the overall system performance meets specifications. The blocks of the parallel $\Delta\Sigma$ ADC, as implemented on the chip, are shown in Fig. 4.3. Each channel consists of the input modulation switches, discussed below, followed by the $\Delta\Sigma$ ADC. This $\Delta\Sigma$ ADC is shown in Fig. 4.2 and is also discussed later in the chapter.

The input signal, $x(t)$ shown entering at the left, passes immediately through the input modulation switches. The modulation switch configuration is shown in Fig. 4.4. The control signals, ϕ_p and ϕ_x, are synchronized with one of the main system clocks, ϕ_{1D}, used in the rest of the modulator. The switches are arranged such that the input signal can be connected directly to the $\Delta\Sigma$ (ϕ_p enabled - a modulation coding of '1'), reverse connected (ϕ_x enabled - a modulation coding of '-1') and not connected at all ($\phi_{x,p}$ disabled - a modulation coding of '0'). This provides a simple structure that not only corrects for switch feedthrough when all the switches are off but also provides a

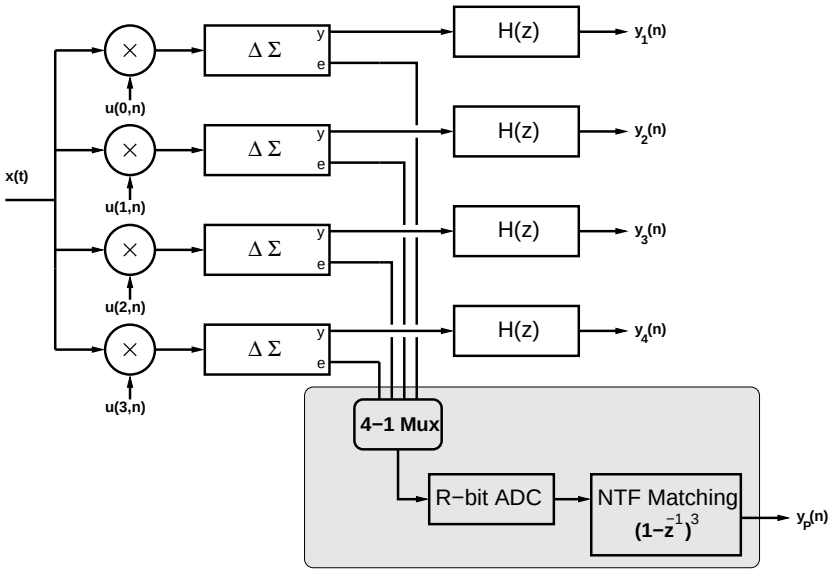


Figure 4.3: The $\Delta\Sigma$ ADC as implemented in silicon.

way of providing input signal modulation with modulation codes of ’0’, ’-1’ and ’1’.

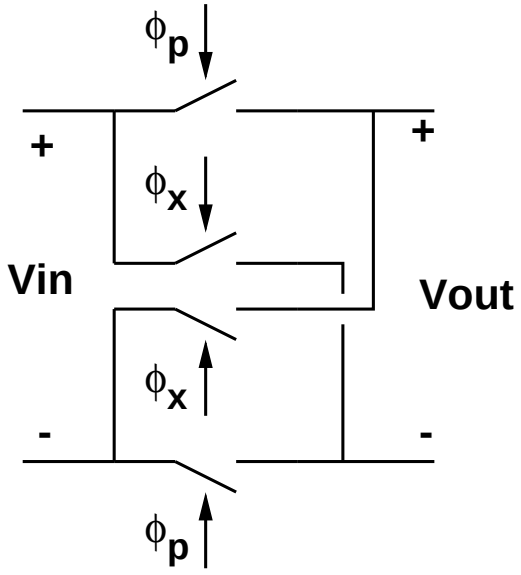


Figure 4.4: Front-end switch configuration.

Switch Type	On Resistance	Charge Injection	Complexity
Simple	Signal Dependant	Large Signal Dependant	Very Simple
Simple with Dummies	Signal Dependant	Medium Signal Dependant	Simple
Bootstrapped	Constant	Constant Signal Independant	Complex

Table 4.2: Switch comparison.

For a standard MOSFET switch the two main design factors of switch resistance and switch charge injection, are competing factors. As the switch size increases, resistance decreases, as desired. Unfortunately, as the switch gets larger, the charge stored under the gate increases as the gate area increases. This stored charge flows out of the switch as it turns off and into the integrator resulting in an error. To solve this problem a more complex switch is needed. These are compared in Table 4.2 [44].

The system specifications dictate both a switch on-resistance of less than 25 ohms and very low or signal independent charge injection. The low switch resistance requirement is a result of the integrator settling specification while the charge injection requirement is set by the overall distortion specifications. Since complexity is not a big issue, bootstrapped or clock-boosted switches are used. The bootstrapping circuit for the switch provides a large, constant V_{gs} to the switch transistor that is independant of the input voltage. Since the switch resistance is dependant on V_{gs}, and V_{gs} is constant and large, the switch can be much smaller for the same on-resistance when compared to non-bootstrapped methods. This size reduction also results in much less signal dependent charge injection when compared to a simple switch. The charge injection is also mostly signal independent due to the constant V_{gs}.

The switch used is shown in Fig. 4.5. Transistor M_1 is the switch element. When the Clk signal is low and the switch is off, transistors $M_{6,7}$ charge the capacitor, C_1 to V_{DD} and transistor M_{11} keeps the gate M_1 pulled low and securely off. When the switch is turned on, $M_{8,9}$ connect the capacitor between the signal input V_{in} and the gate of switch M_1, making the V_{gs} approximately equal to V_{DD}. M_{10} is used to prevent the gate-drain voltage of M_{11} from exceding the limits of the gate oxide and destroying the transistor. Transistors $M_{4,5}$ invert the input clock to control $M_{7,11}$. The switch is designed for a maximum on-resistance of 25Ω as verified by the simulation.

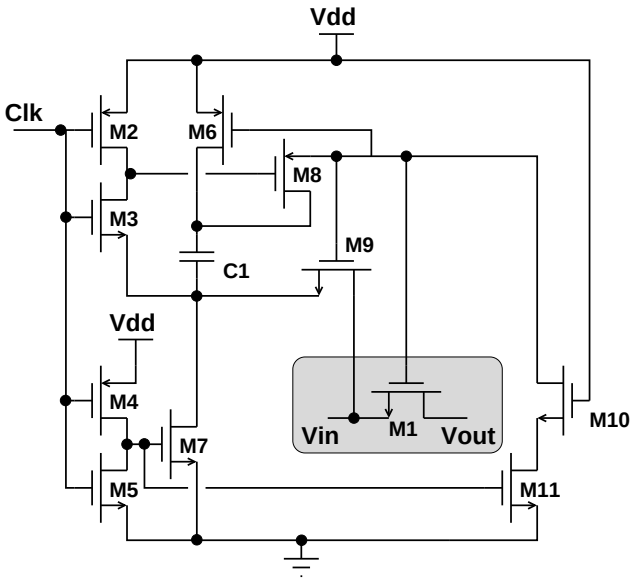


Figure 4.5: Bootstrapped Switch

After the modulation switches, the signal enters the first block of the $\Delta\Sigma$ modulator, shown in Fig. 4.2. This modulator is made of three distinct $\Delta\Sigma$ stages, an initial second order $\Delta\Sigma$ ADC which is followed by two first order stages. Starting with the first stage, a simplified schematic of this second order modulator is shown in Fig. 4.6. The signal

from the input modulation switches, taking the place of the standard $\Delta\Sigma$ modulator input switch, charges the sample capacitor C_{s1} during ϕ_{1D}. On the next clock phase, with the correct DAC feedback signal selected, the charge on the sample capacitor is transfered to the integrator capacitor with the aid of the opamp. The process is repeated for the second integrator. The output of the second integrator is fed into the next stage of the ADC and then into the quantizer. The quantizer compares the signal to a reference and outputs the correct digital bit, providing the signals to the DACs.

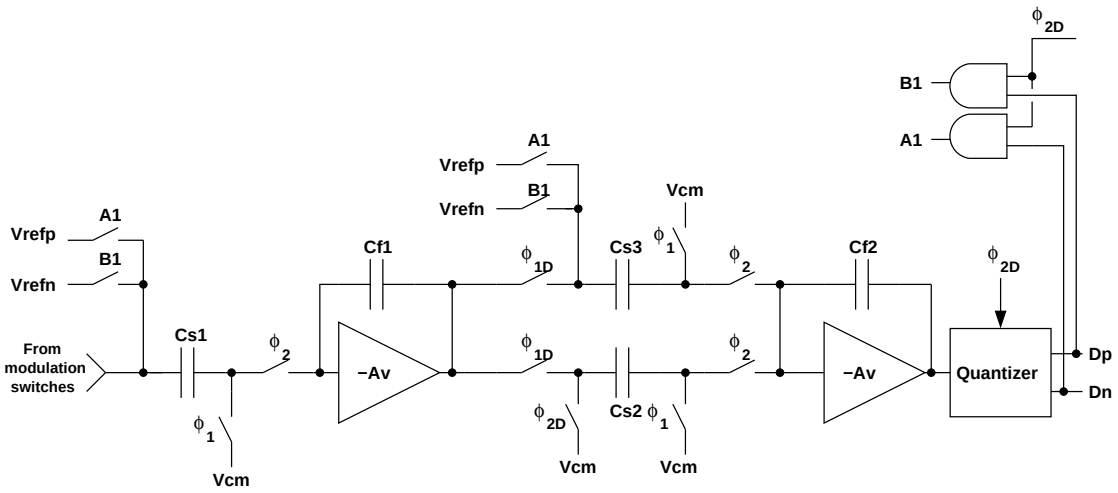


Figure 4.6: The second order $\Delta\Sigma$ ADC.

The sampling capacitor is sized based on the $\frac{kT}{C}$ requirements for the desired SNR performance. Using the equation ${v_n}^2 = \frac{4kT}{OSR*V_{ref}}$ with an OSR of 4, a input signal swing of $1V$, and SNR of 15.5 bits, the sampling capacitor size is calculated as 20pF. Considering a single channel instead of the overall system, the calculations result in the same capacitor size. This is due to the ratio between SNR and OSR remaining constant, since for a single channel the OSR is 4X higher or 16 and the SNR of each channel must

Capacitor	Unit Value	Capacitance
C_{s1}	1	10pF
C_{f1}	4	40pF
C_{s2}	1	10pF
C_{s3}	1	10pF
C_{f2}	4	40pF

Table 4.3: First $\Delta\Sigma$ modulator capacitor values.

be 4X higher to achieve the overall total system SNR. From this calculation and the modulator coefficients determined earlier, the capacitors values are shown in Table 4.3.

At the heart of each integrator is the amplifer. The design of the amplifiers for the first $\Delta\Sigma$ modulators is important to achieve the necessary performance specifications. In a $\Delta\Sigma$ modulator, the opamp design specifications most important to performance are opamp gain, bandwidth, slew rate and noise. In this design these specifications were determined from system level simulations in ASIDES [45] with non-ideal amplifiers, switches and quantizers.

For a 2-1-1 MASH style architecture, the system performance is dependent on the noise transfer function (NTF) matching. For NTF matching, the $\Delta\Sigma$ modulator NTF must be close to the ideal NTF, thus requiring amplifiers that are very close to ideal. From system simulations, the required amplifier gain is greater than 20,000 or 86dB. The bandwidth requirements fix the amplifier bandwidth at 800MHz at a minimum while driving a maximum total load capacitance of 45pF. For this design, in this process, the noise and slew rate requirements were inherently met when designing for the required gain and bandwidth.

To achieve the high gain needed for the MASH style structure in a 2.5V process,

folded cascode amplifiers with two embedded gain boosting amplifiers are used. The simplified schematic for this amplifier is shown in Fig. 4.7. The input devices, $M_{1,2}$, consist of two interdigitated, $\frac{1680\mu m}{0.48\mu m}$ NMOS transistors with each branch in the amplifier consuming 25mA. An amplifier with such large tail currents requires large transistors. For a fixed length transistor, as transistor size increases, the r_{ds} of the transistor decreases. Because of this, gain boosted amplifiers are necessary to increase the amplifier output resistance and gain. The main amplifier uses switched-capacitor common mode feedback with 135fF capacitors. The boost amplifiers are standard folded-cascode amplifiers with continuous-time common-mode feedback circuits.

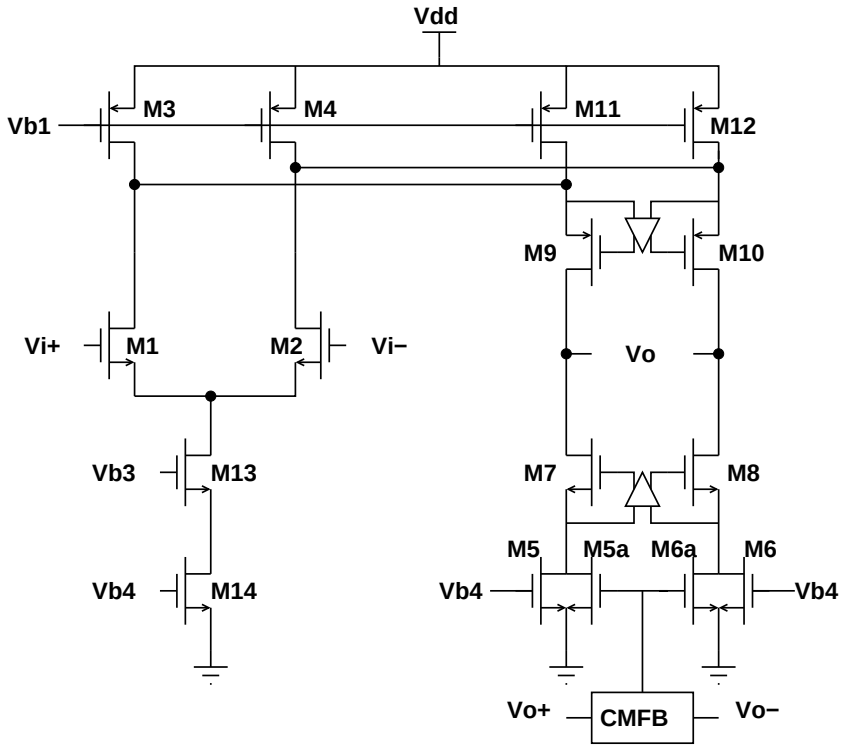


Figure 4.7: First Opamp - Folded-cascode with gain boosting.

The last block in the first $\Delta\Sigma$ modulator is the quantizer. The quantizer employed is a standard latch design as shown if Fig. 4.8 [46]. The first two differential pairs, $M_{1,2}$ and $M_{4,5}$, bias transistors $M_{3,6}$ and associated resistors, R_{1-6}, comprise the input buffer. The input buffer provides a gain of 20 and is followed by the latch. The latch consists of transistors M_{7-13} followed by the buffer inverters, M_{14-17}. The latch is reset by the clock signal Ck. When the clock is low, the latch is in reset mode and when the clock is high, it is in latch mode. The entire system has a decision time of 1ns at a minimum input voltage of $23\mu V$. This specification is of special importance for a $\Delta\Sigma$ modulator where the time to quantization is important. If the input voltage is too small for the quantizer to make a decision in time, the result has a 50% chance to be incorrect, preventing the ADC from achieving full performance. The entire quantizer consumes 400 μA of current at 2.5V resulting in a power consumption of 1 mW.

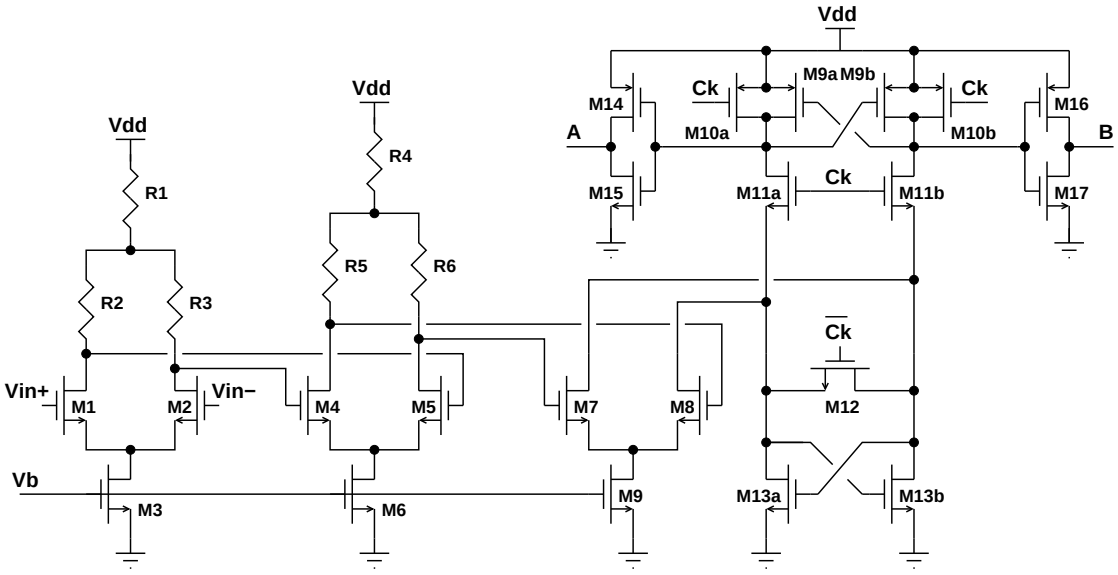


Figure 4.8: Comparator circuit including buffer amplifiers and latch.

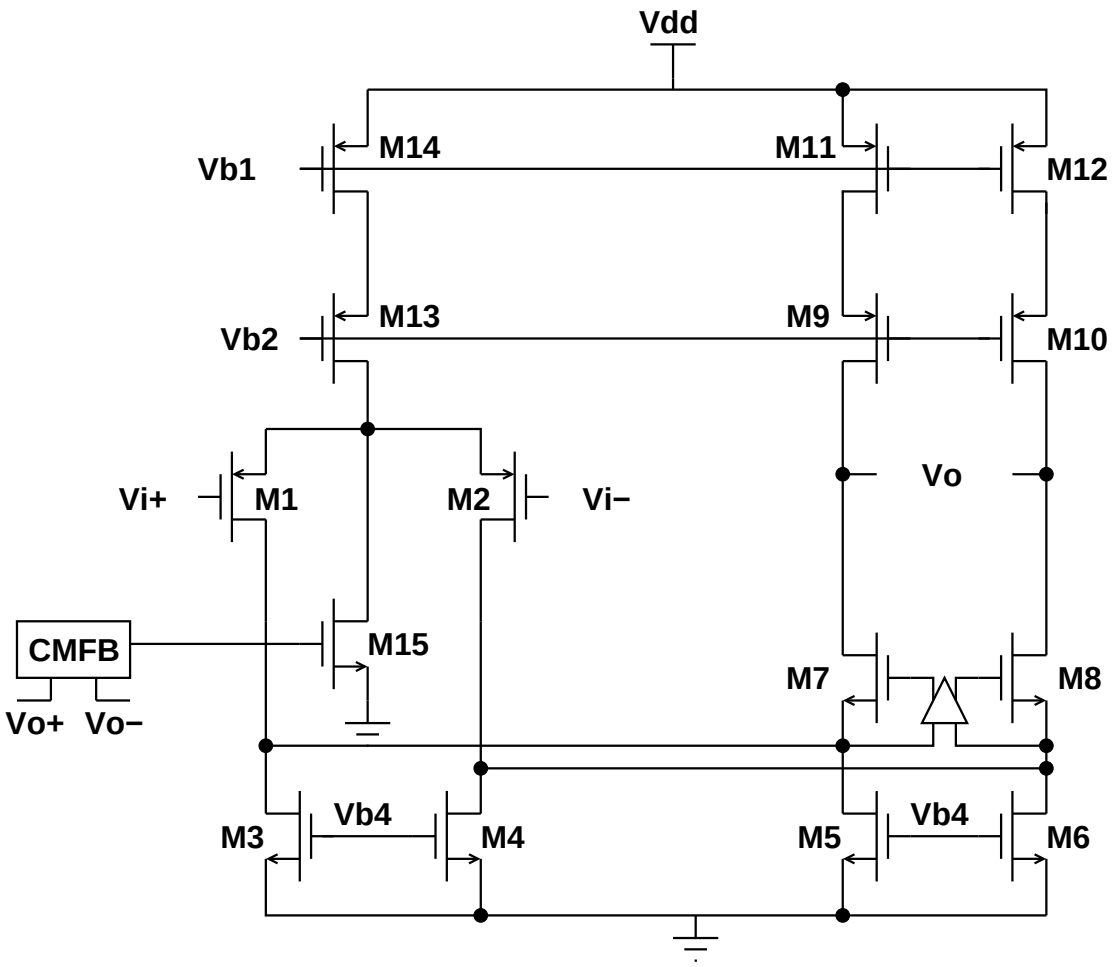


Figure 4.9: Second and third stage amplifier.

The quantization noise of the second order $\Delta\Sigma$ modulator is the input to the second $\Delta\Sigma$ modulator. Since the second and third $\Delta\Sigma$ modulators mainly process quantization noise, the performance requirements are greatly relaxed. This reduction in performance means the second and third $\Delta\Sigma$ modulators are identical first order modulators and use a sampling capacitor size of 1pF to meet the necessary kT/C noise requirements. From the sampling capacitor size and the system coefficients, the capacitors sizes were

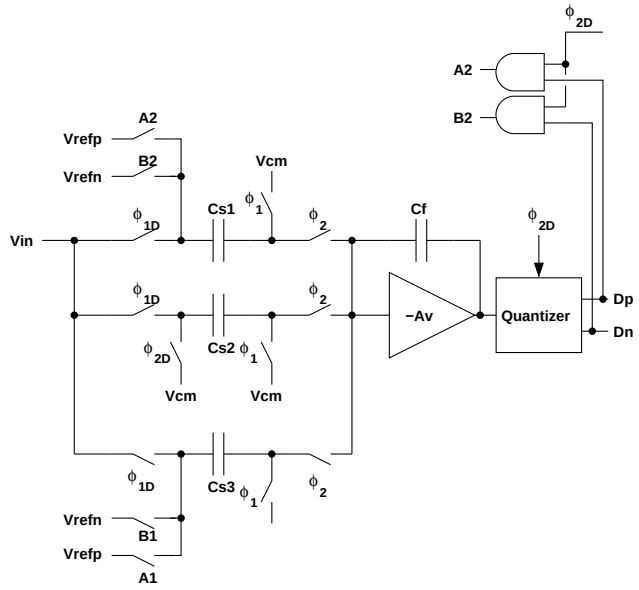
Second Modulator		
Capacitor	Unit Value	Capacitance
C_{s1}	2	660fF
C_{s2}	3	990pF
C_{s3}	3	990pF
C_f	8	2640fF
Third Modulator		
Capacitor	Unit Value	Capacitance
C_{s1}	1	990fF
C_{s2}	1	990pF
C_f	1	990fF

Table 4.4: Second and third $\Delta\Sigma$ modulator capacitor values.

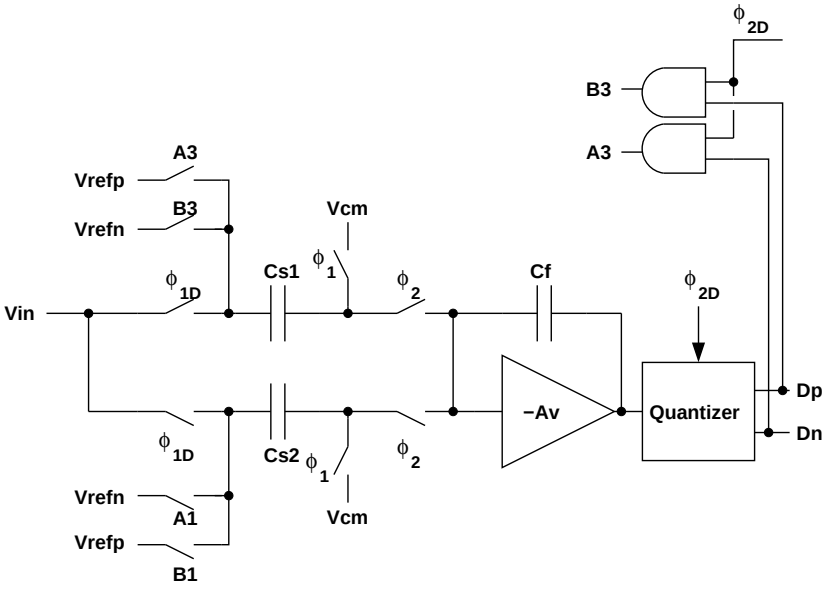
calculated and are shown in Table 4.4. The switches used in these stages are simple pass gate switches with a PMOS $\frac{W}{L}$ of $\frac{40u}{240n}$ and a NMOS $\frac{W}{L}$ of $\frac{9u}{240n}$. The opamp used is a standard PMOS input folded cascode with another folded cascode opamp for gain boosting on the NMOS cascode transistor. This amplifier is shown in Fig. 4.9. The comparator used is the same as used in the first $\Delta\Sigma$ modulator.

The final two blocks of Fig. 4.3, the multiplexer and the pipeline ADC, are the blocks that are shared by all the channels. The multiplexer, simplified to single-ended for illustration purposes and shown in Fig. 4.11, consists of a set of switches which direct the quantization noise output from one of the channels to the input of the pipelined ADC. The multiplexer is clocked at 100MS/s with each input connected to the output every four clock cycles. The switches of the multiplexer, since they are passing quantization noise, are the same ones used in the last two $\Delta\Sigma$ stages.

The output of the multiplexer is connected to the input of the pipeline ADC. This



(a) Second Modulator



(b) Third Modulator

Figure 4.10: The second and third $\Delta\Sigma$ modulators

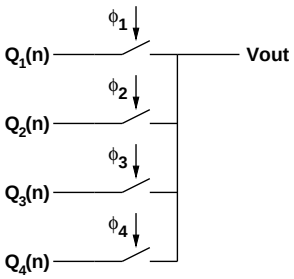
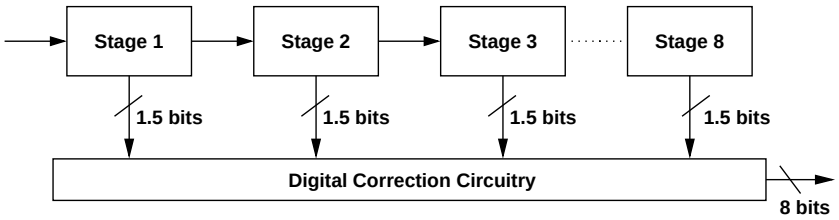
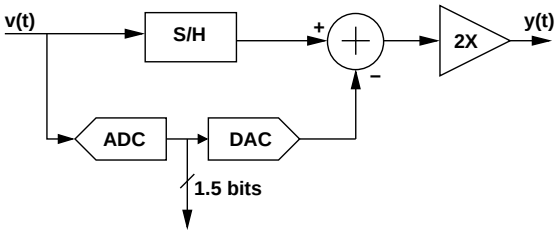


Figure 4.11: Shared system multiplexer block.

pipeline block performs the final quantization of the noise from the $\Delta\Sigma$ ADCs in each channel. The pipeline architecture is shown in Fig. 4.12. The pipeline is made of 9 idential 1.5 bit stages, using the extra 0.5 bit to provide error correction. The pipeline achieves 7.5 bits of resolution at 100MS/s.



(a) The overall pipeline block diagram.



(b) A single pipeline stage.

Figure 4.12: The pipeline ADC block diagram.

In this pipeline each stage uses the ADC block consisting of two comparators to quantize the input voltage, $v(t)$ as shown in Fig. 4.12(b),. If the voltage is above a

certain threshold, the DAC substracts a known reference voltage from the input signal and, after multiplying the signal by 2, sends it on to the next stage. The residue $y(t)$, the voltage presented to the next stage, can be calcuated for three different cases. If $v(t) > v_{ref}/2$, $y(t) = 2v(t) - v_{ref}$. For $|v(t)| < v_{ref}/2$, $y(t)$ is simply $2v(t)$. In the final case, when $v(t) < v_{ref}/2$, $y(t) = 2v(t) + v_{ref}$. The digital output is fed into the digital correction circuit which uses the extra 0.5 bits from each stage to correct for the analog processing errors in each stage [47].

This parallel $\Delta\Sigma$ ADC consumes significant power and die area. To prevent voltage sag and power line noise from limiting the performance of the ADC, the layout of blocks such as opamps and routing power to blocks becomes a non-trivial task. The metal routing in the amplifiers consumes more area than the active devices. This is shown in Fig. 4.13, where all the traces that can been seen are power routing. The horizonal traces across the top are the main power bus and the vertical traces provide power to the amplifier. The square blocks at the bottom are the capacitors. The active components are hidden below the power routing.

4.4 Simulation Results

The system was simulated in both MIDAS and Matlab. The results are for a four channel, 3rd order, 8X OSR parallel $\Delta\Sigma$ modulator with a 9 bit second stage ADC. The spectrum is shown in Fig. 4.14 and the dynamic range plot is shown in Fig. 4.15. The spectrum is for a sinusoidal input signal with an input frequency at $\frac{1}{16}$ of f_s. The amplitude is at the maximum dynamic range point. The humps in the noise on this plot are

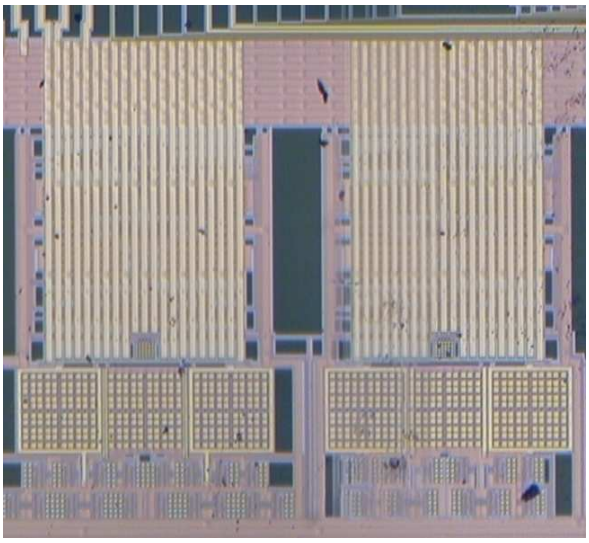


Figure 4.13: Power routing for the amplifiers.

normal in a parallel $\Delta\Sigma$ and are an artifact of the noise transfer functions of the individual channels and the multi-path nature of the system. Fig. 4.15 shows the dynamic range of the A/D converter. At the maximum dynamic range point, the system has 101dB of dynamic range or 16.7 bits.

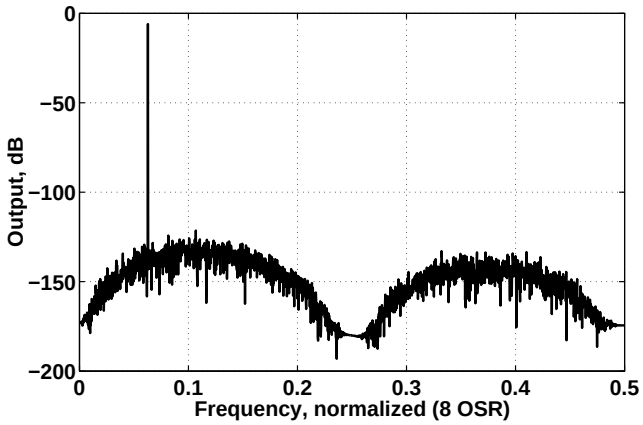


Figure 4.14: Power spectral density of the output with sinusoidal input.

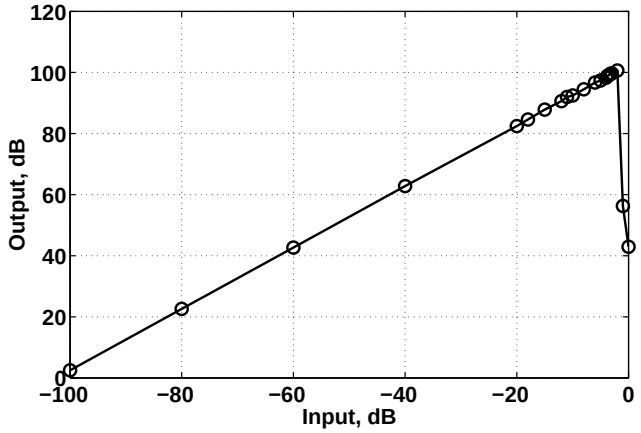


Figure 4.15: The dynamic range of the ADC.

4.5 Test System

To efficiently test the ADC, two circuits boards were designed. The first board, shown in Fig. 4.16, is the main board containing the major function support blocks for proper chip operation. These blocks include a high current power supply, an adjustable bias current section, a clock conditioning circuit, a basic output buffer, the voltage reference circuitry, the input conditioning and various connectors for modulation inputs, test connections and control signals. The power supply provides quiet 2.5V analog and digital supply voltages and a +/- supply connector to supply positive and negative 5V power to the other support circuitry. The adjustable bias current circuitry provides $100\mu A$ nominal bias currents with a $+/-20uA$ adjustable range to each block on the chip. The output buffer is not used during normal operation but provided as a buffer for muxed analog test signal from the chip and is only used for debugging. At the bottom of the board, the voltage reference circuitry provides adjustable clean voltage references for the chip. The clock circuitry level shifts the clock signal that is connected to the SMA

connector to a 1.25V midpoint to set the duty cycle to 50%. Input conditioning circuitry provides buffering, level shifting, some basic filtering and both single-ended to differential and differential to differnential operation. The other connectors on the board allow connection of the modulation inputs, provide reset and test signals, allow viewing of internal ADC nodes and an ability to check clock skew across the chip.

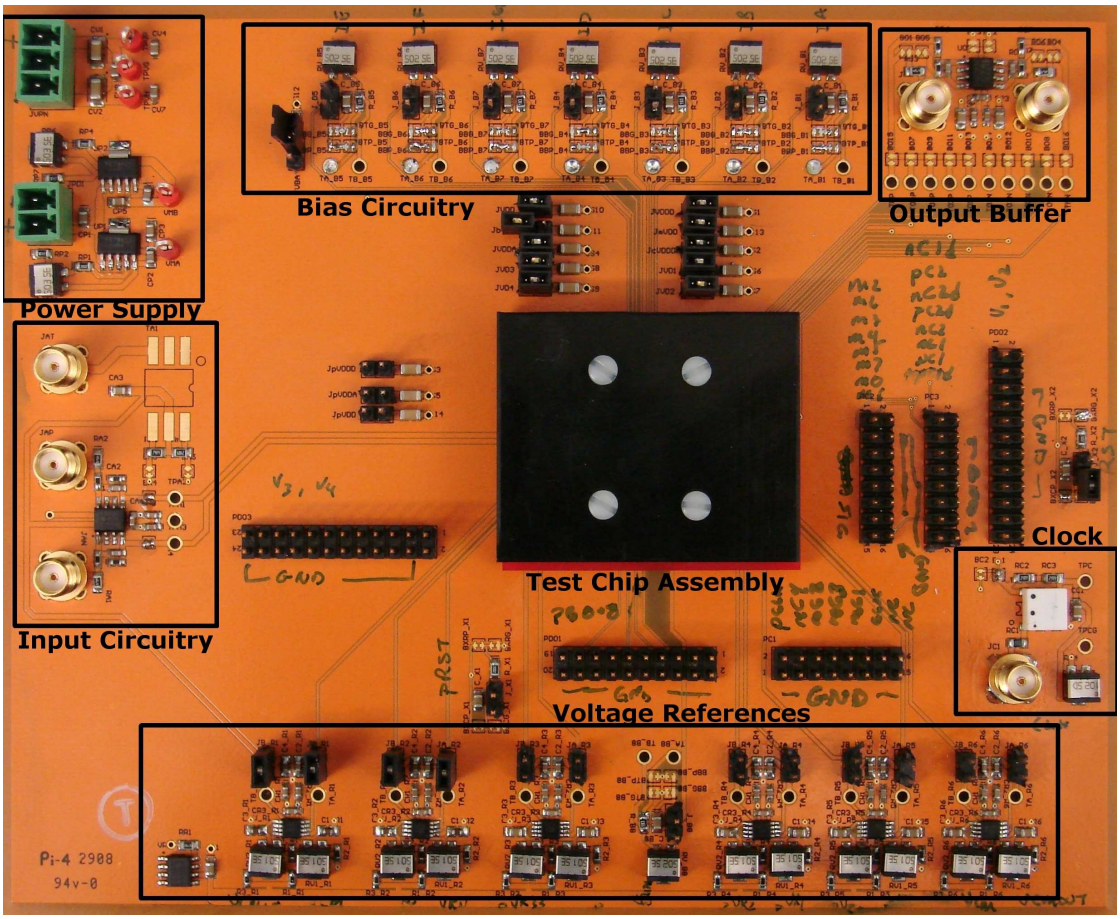
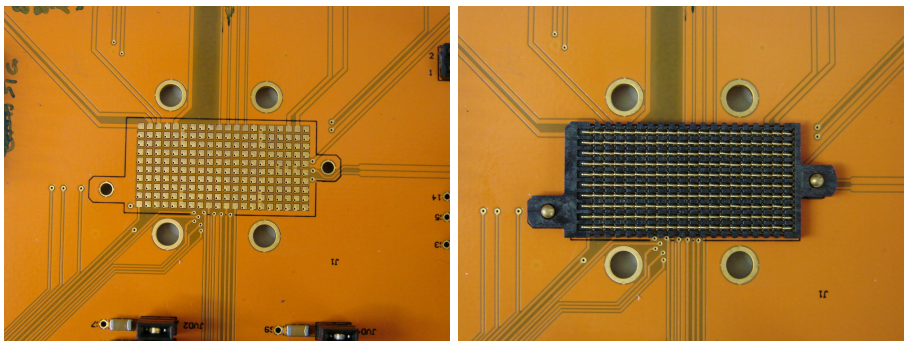


Figure 4.16: Test board showing functional blocks.

The device test setup consists of two boards, the main board discussed above and a daughter board containing the silicon die and various bypass and filter capacitors. The

boards are connected together with a SAMTEC Z-Beam board-to-board connector as shown in Fig. 4.17. This connector provides a very low parasitic, high density connection between the main board and the daughterboard. The connector used in this design has 200 pins arranged in a grid of 10X20 on a 0.050” pitch and a total height of 0.065”. Each pin has a current handling ability of 0.4A, an inductance of 1nH, a parasitic pin-to-pin capacitance of 150fF, a bandwidth of $> 3GHz$ and a pin-to-pin crosstalk at 3GHz of less than 40dB. The purpose of this type of configuration is to allow multiple chips to be tested with minimal expense, while avoiding packaging and socketing issues and providing the least amount of additional parasitics possible.



(a) (b)

Figure 4.17: High performance connector and PCB footprint.

Shown in Fig. 4.18 is the daughter board, mounted on the main board with the protective cover removed showing the die and the solder pads for the bypass and filter capacitors.

To avoid extra complexity and reduce the chance of design error, the digital signal processing blocks were not included on the chip. The digital bit stream from each channel is processed in a combination of ASIDES and Matlab. The processing block diagram

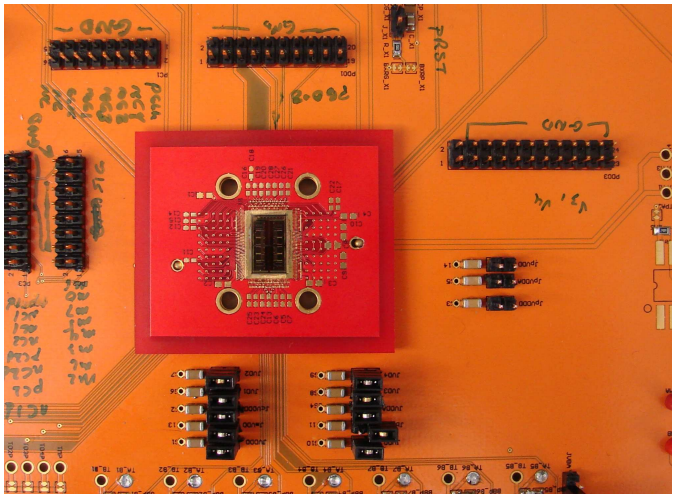


Figure 4.18: Test board with die exposed.

for each channel is shown in Fig. 4.19. Table. 4.5 lists the various filter equations and other variables.

The signal from each channel is modified by the calibration algorithm[48], summed together, filtered and decimated by the overall oversampling ratio.

Variable	Equation	Value
d_0	$1 - \frac{g_3'}{g_1 g_2 g_3}$	-1
d_1	$\frac{g_3''}{g_1 g_2 g_3}$	2
d_2	0	0
d_3	$\frac{g_4''}{g_1 g_2 g_3 g_4}$	2
$H_1(z)$	z^{-1}	
$H_2(z)$	$(1 - z^{-1})^2$	
$H_3(z)$	z^{-1}	
$H_p(z)$	$(1 - z^{-1})^3$	

Table 4.5: Digital signal processing coefficients and filter equations.

The lab test setup block diagram is shown in Fig. 4.20. The center block, DUT,

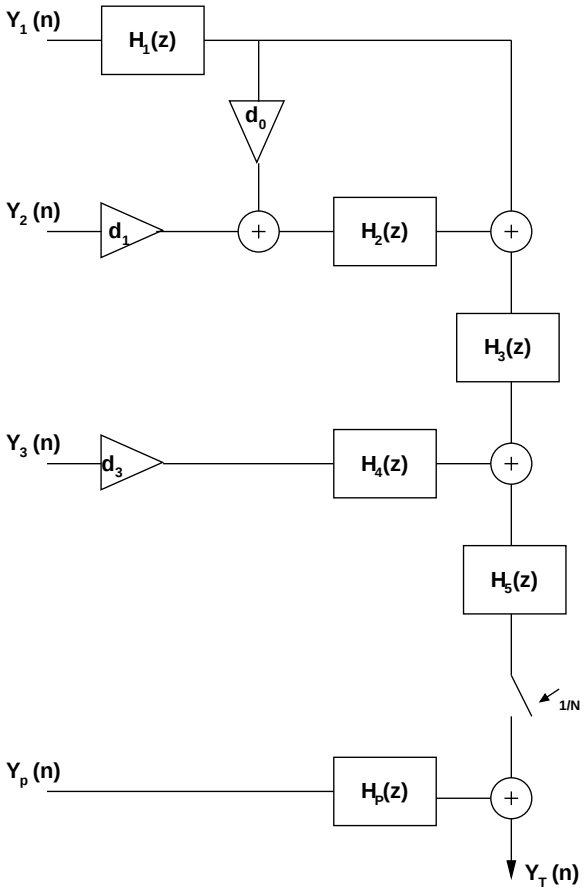


Figure 4.19: Digital signal processing for one channel.

is the circuit board with the attached ADC chip. The input signal is generated with the HP8643A, followed by a narrow-band bandpass filter with removes the large second harmonic and guarantees are clean input signal. The HP8665A, with the low phase noise option, provides a stable, under 0.5ps rms jitter, clock signal. This signal generator supplies the main system clock that controls the input sampling switches. This clock source is also phase locked with the pattern generator in a Tektronix TLA700 logic analyzer. The pattern generator output supplies the modulation sequence to the ADC.

The digital data from the ADC is captured by the Tektronix TLA700 logic analyzer.

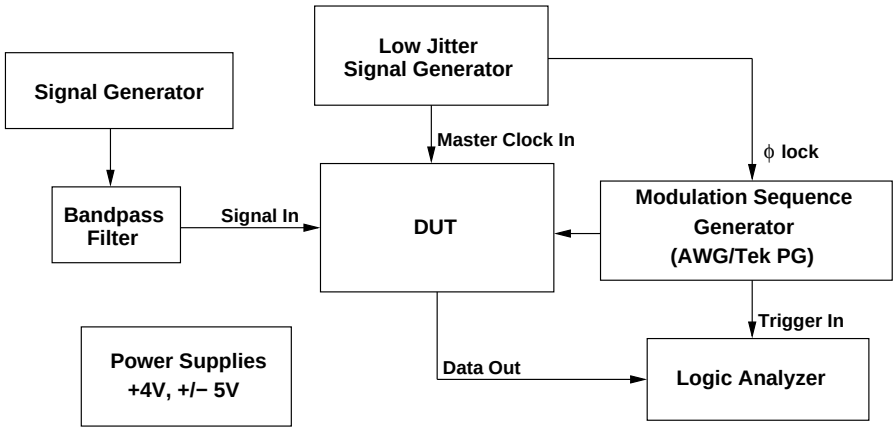


Figure 4.20: The ADC labratory test setup.

The system was tested under several conditions as outlined in Table 4.6.

Test #	Description	Results	SNDR
1	4X OSR	Fig. 4.22	13.8 bits
2	Narrowband - 8X OSR	Fig. 4.23	14.6 bits
3	Dualband - 8X OSR	Fig. 4.24	13.4 / 12.6 bits

Table 4.6: ADC tests performed and resultant SNDRs.

Fig. 4.21 shows the output of the ADC before calibration. The various tones shown are due to the gain and offset errors of each channel of the ADC. For this chip, the channel gain and offset values are given in Table 4.7. After calibration, the gain value is within $2^{-16.5}$ of 1.0 and the absolute value of the offset is less than $2^{-16.5}$. After the system is calibrated the tones due to the gain and offset mismatches are removed and the result is shown in Fig. 4.22. Fig. 4.23 shows the performance for a 8X OSR conversion.

Channel #	Gain	Offset
1	0.99923	-2.4mV
2	0.99807	5.4mV
3	0.99618	2.8mV
4	1.00671	-10.5mV

Table 4.7: ADC Channel gain and offset values.

The input signal is at 1MHz. Fig. 4.24 shows the results for the converter configured as two separate converters each converting a separate frequency range.

For applications such as radar and cognitive radio, where flexible bandwidth and resolution are key to system performance, the parallel $\Delta\Sigma$ architecture with its inherent flexibility is a excellent match. The dual band plot shows the output of the system when the 4 channels are used in two banks of two channels to convert two separate signal bands at the same time. The input signals were are 1MHz and 8MHz and the resulting demodulated signals show up in conversion bank 1 at 1MHz and in conversion band 2 at 2MHz. This is because the input modulation for band 2 downconverts the higher frequency input signal to 2MHz. The SNDR for each of the modulation sequences for the dualband system are

Channel 1	1 1 -1 -1 0 0 0 0 1 1 -1 -1 0 0 0 0
Channel 2	0 0 0 0 1 1 -1 -1 0 0 0 0 1 1 -1 -1
Channel 3	1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0
Channel 4	0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1

Table 4.8: ADC Dualband modulation sequences.

These key attributes make this architecture well suited to applications where rapidly shifting bandwidths and resolutions are key parts of the system performance. The programabilty of digital filters and ease of changing modulation sequences, as demon-

strated, make this ADC suited to convergent systems. A summary of the results is shown in Table 4.9.

4.6 Conclusions

Convergent systems require analog-to-digital converters (ADCs) that are high-speed, high-resolution, flexible and adaptive. An efficient parallel $\Delta\Sigma$ ADC architecture has been designed that achieves high performance in digital processes, while also providing additional architecture adaptability and flexibility. This flexibility enables the ADC to work equally well over a range of resolutions and bandwidths The architecture meets the goals of a high speed, high resolution ADC that is suited to demanding convergent systems. This design not only meets the performance specifications, but also provides a level of reconfigurablity and adaptablity not available in other types of converters.

Resolution @ 4X OSR	13.8 bits
SNDR @ 4X OSR	85.6 dB
SFDR @ 4X OSR	94 dB
Resolution @ 8X OSR	14.6 bits
SNDR @ 4X OSR	88 dB
SFDR @ 8X OSR	99 dB
Input Range	1 V
Clock Frequency	64 MHz
Signal Bandwidth @ 4X OSR	8 MS/s
Technology	0.25 μm CMOS
Power Supply	2.5 V
Power Consumption	1.8 W
Size	10.5 mm X 6.3 mm

Table 4.9: Summary of ADC Performance and Specifications.

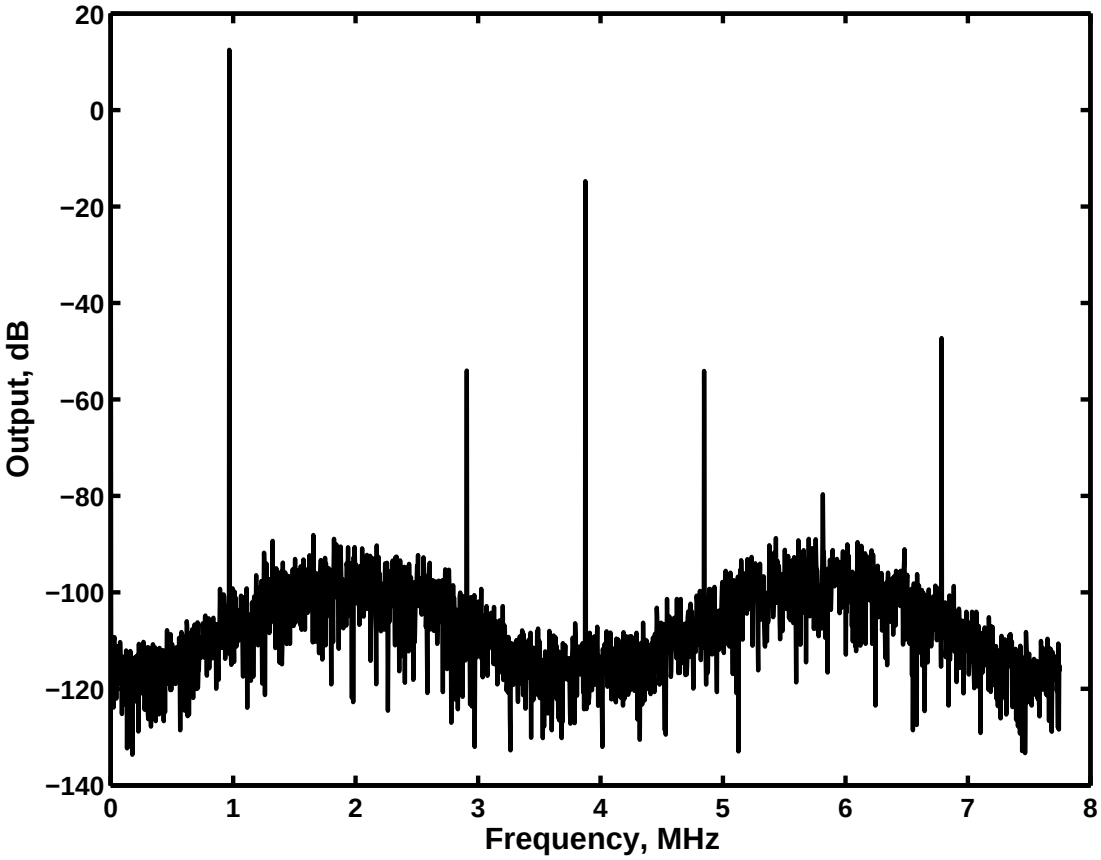


Figure 4.21: Uncalibrated measured test results for a 64MHz clock and a 1MHz input signal.

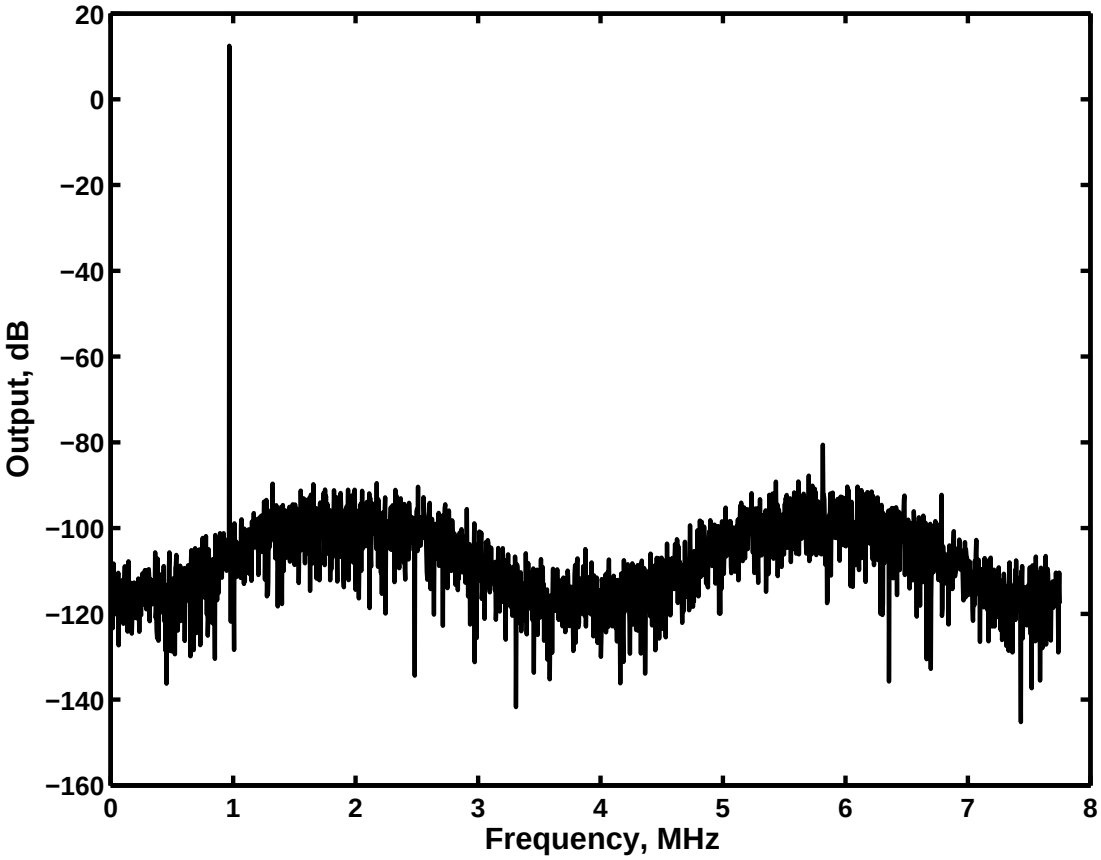


Figure 4.22: Calibrated measured test results for a 64MHz clock and a 1MHz input signal.

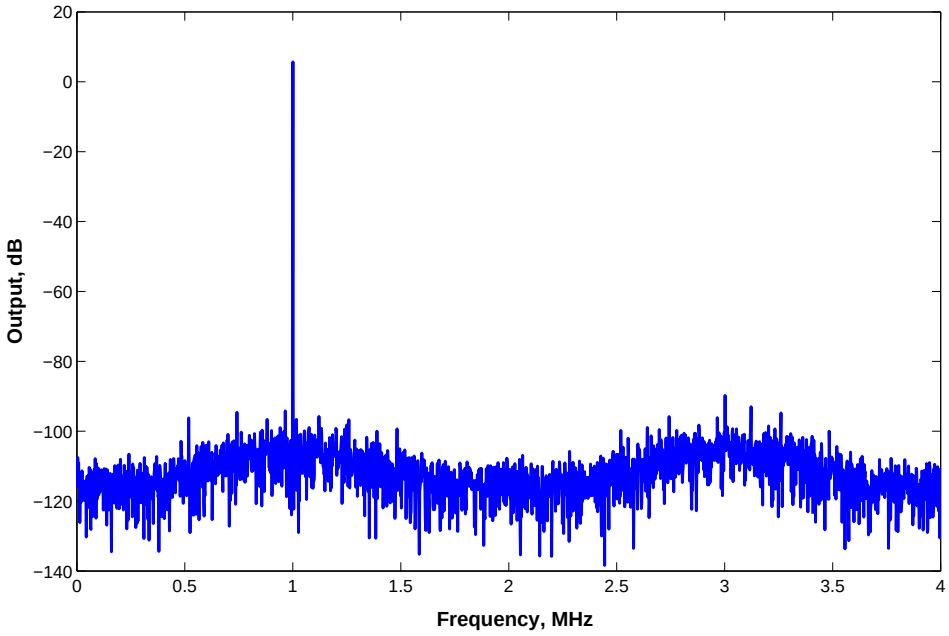
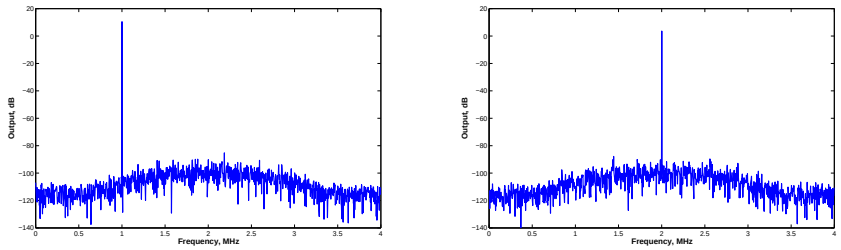


Figure 4.23: Calibrated measured test results for a 64MHz clock and 8X OSR.



(a) (b)

Figure 4.24: Calibrated measured test results for a 64MHz clock and dualband 8X OSR.

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