AN ABSTRACT OF THE THESIS OF

Joshua Kenneth Carnes for the degree of Master of Science in Electrical and Computer Engineering presented on January 16, 2007

Title: Low Voltage Techniques for Pipelined Analog-to-Digital Converters

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Un-Ku Moon

To realize pipelined ADCs in deep-submicron processes, low voltage techniques must be developed to work around problems created by limited supply voltages such as the floating switch dead zone, reduced SNR, and reduced OpAmp performance.

This thesis analyzes standard and low voltage design issues for pipelined ADCs and proposes a fully-differential implementation of the OpAmp Reset Switching Technique (ORST) as a suitable low voltage design solution. The technique uses a true fully differential MDAC structure with a switching common-mode feedback to achieve increased linearity and noise performance over the previously published ORST.

A pipelined ADC test chip is designed to implement the fully differential ORST technique as a proof of concept. The design also includes a simple, low power input sampling network that also allows an increased input signal range and saves power by removing the dedicated, front-end S/H.

Prototype performance demonstrates the fully differential ORST and shows sampling speeds of up to 60 MS/s, 51.4 dB SNR, 58.8 dB SFDR, and 49.7 dB SNDR for an 8-bit ENOB in a 0.18 μm CMOS process with a 1 V supply. Little change in distortion is observed up to 90 MHz input frequency, demonstrating operation without a S/H.

Low Voltage Techniques for Pipelined Analog-to-Digital Converters

by
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APPROVED:

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Dean of the Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Joshua Kenneth Carnes, Author

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1 Introduction

As essential devices in the analysis of data present in the tangible world, analog-to-digital converters enable the fast and cheap digital processing of large systems for a wide variety of modern applications. Among these applications, wireless digital communications systems, high definition video imaging, and medical instrument signal processing are pushing the requirements of analog-to-digital converters to very high speeds (> 100 MS/s) while maintaining medium resolution requirements (10-16 bits) [7] [20], leaving engineers to search for new ways to boost the performance. New emphasis on portability in the last decade has also led to the need for reduced power consumption, a requirement that is becoming increasingly difficult for analog circuits.

Process advancements enable increasing speed capability for analog circuits but often sacrifice the accuracy at higher speeds due to process limitations such as device mismatches and reduced transistor output impedance. This forces the evolution of analog circuit techniques to compensate for the new problems introduced by smaller dimensions and the interaction between analog and digital circuits in a monolithic environment.

The 2005 update to the International Technology Roadmap for Semiconductors estimates rapid process improvements, reporting that the supply voltages for high performance digital CMOS processes are to reduce to 1 V by 2008 and sub-1 V in 2012 with the 45 nm node as shown in Figure 1 [1]. Though “analog ready” processes lag behind digital processes by a few years, research is ongoing to address the difficulties of using low voltage supplies with analog integrated circuit as the supply nears 1 V.

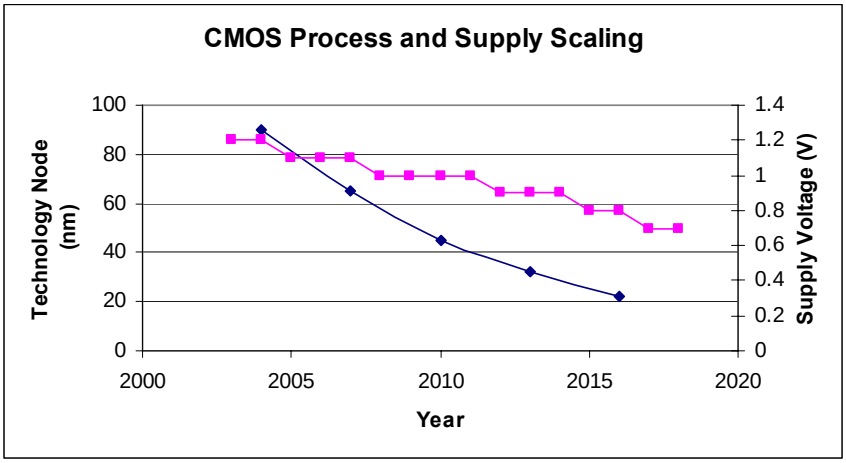


Figure 1: Dimension and voltage scaling forecast for digital CMOS processes

Pipelined analog-to-digital converters are an appropriate choice among the converter architectures for the sub-gigahertz speeds and medium resolutions but are not exempt from the difficulties of operating at low voltages. Floating switches, reduced headroom, reduced OpAmp performance, and process limitations all pose obstacles to the performance of these converters.

This research proposes a low voltage pipelined analog-to-digital topology that improves on the previously published OpAmp Reset Switching Technique (ORST) [11] by adapting it to a fully differential scheme thereby improving its noise and linearity performance while continuing to operate at low voltages. The new design also presents a fully differential common-mode feedback that includes a switching mechanism for compatibility with the ORST technique, and a highly linear track-and-reset (T/R) that avoids the use of a low voltage, front-end sample-and-hold circuit and allows increased input signal amplitude.

The contributions of this thesis include:

- Adaptation of the ORST technique to fully differential circuits and implementation of the topology in a low voltage, high speed pipelined ADC

- A CMFB switching mechanism that enables the fully differential ORST common-mode switching operation
- Analysis and implementation of a passive input network compatible with the fully differential ORST
- A form of CMFB loop gain reduction using both the positive and negative feedback from the CMFB comparison amplifier to stabilize the loop

This thesis is organized as follows. Chapter 2 reviews the functionality, basic circuit implementations, and evaluation of pipelined ADCs. Chapter 3 covers circuit-level design considerations including tradeoffs and sources of error. Chapter 4 details issues specific to low voltage designs and evaluates recently published techniques. Chapter 5 presents the new fully differential ORST topology along with additional techniques included in the design of a high-speed, 1 V, 10-bit pipelined ADC, reveals details of the design layout, and shows measurement results and observations. Chapter 6 finishes with design improvements, future work, and conclusions.

2 Pipelined Analog-to-Digital Converters

2.1 Functionality

A pipelined analog-to-digital converter uses a fusion of serialism and parallelism to convert analog signals into the digital domain and fundamentally trades increased hardware, power, and conversion latency for increased conversion rate and resolution. It is a compromise between a cyclical/algorithmic converter which uses a single stage to serially resolve the bits of a conversion over a number of clock cycles, and a flash converter which uses maximum parallelism to convert the input in a single cycle. The pipelined converter employs an assembly line of many cascaded stages to resolve many bits each clock cycle.

Each stage has the task of determining specific bits of the digital word, with the foremost stages deciding the most significant bits (MSBs) and the backend stage in the pipeline deciding the least significant bits (LSBs). With this architecture, the bit resolution is linearly related to the number of stages but a sample is generated every clock cycle, so the conversion rate is nearly independent of the resolution. The cost of using a pipelined architecture is the increased sample-to-data-ready latency because the sampled data must traverse the pipeline before the full digital word is formed, as well as the extra power and area that come with each cascaded stage.

2.1.1 Pipelined Stages

Each stage of a pipeline samples a signal from a previous stage, compares this value to a set of reference *thresholds* to decide the digital output bits, removes the equivalent analog value of the bits from the input signal, and then amplifies the result to create the output *residue*. This process is completed each clock cycle, at the end of which the residues are passed down the pipeline.

A block diagram of a stage, shown in Figure 2, illustrates how these tasks are performed by a sample-and-hold, a sub-stage ADC, a sub-stage DAC, and a difference

amplifier. To compensate the subtraction of the DAC value from the input, the amplifier boosts the value so that the residue utilizes the full output range of the stage. Errors occurring in later stages of the pipeline are reduced by this inter-stage gain when input referred, allowing the speed and accuracy requirements of backend stages to be reduced. Amplification also allows the sub-ADC and sub-DAC references to be reused in each stage, leading to a drastic reduction in the number of references compared to a flash ADC which requires an exponential increase in the threshold reference levels with increases in converter resolution. The final stage of the pipeline only requires a sub-stage ADC because no residue needs to be generated.

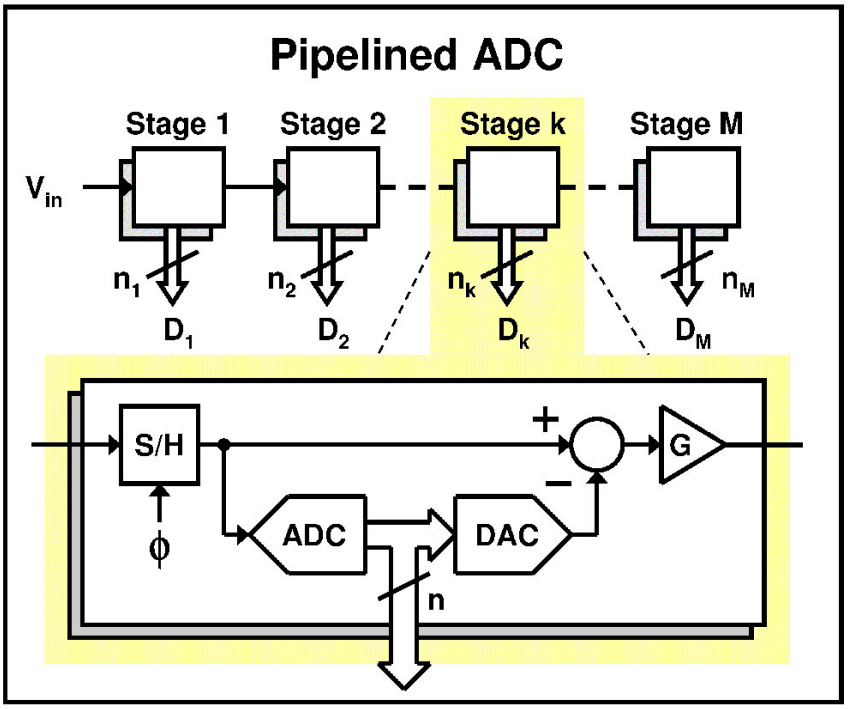


Figure 2: The structure of a basic pipelined ADC stage

2.1.2 Stage Transfer Function

The processing of a sample by a stage can be pictorially described by its static input to output transfer function. An example of a 2-bit pipeline stage transfer function is shown in Figure 3. To relate the figure to the stage architecture, it is seen that as the stage's sampled input value increases past a sub-ADC threshold value ($-1/2V_{REF}$, 0, $+1/2V_{REF}$), the digital bits increment and the sub-DAC subtracts from the residue. The thresholds divide the transfer function into regions with ideal width corresponding to 1 LSB for the stage.

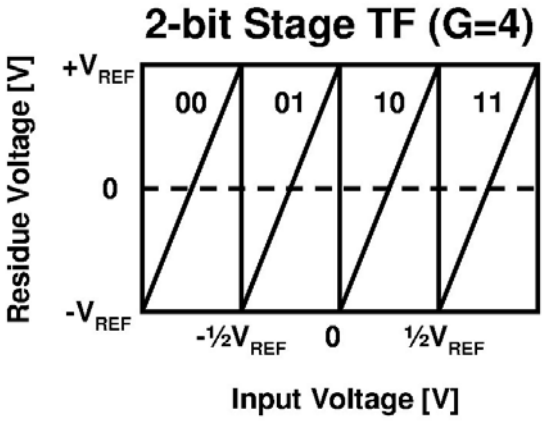


Figure 3: Static transfer function of an ideal, 2-bit stage

Equation (1) is the mathematical description for a simple stage transfer function where v_{res} is the stage output residue voltage, n is the number of bits resolved by the stage, D is the integer value of the sub-stage ADC output, v_{ref} is the peak input and output range of the stage, and k is the sample index. The output signal index shows how the residue is valid a half clock phase after the input is sampled, allowing the next stage to promptly acquire the residue. In this way, the conversion process of a data sample will pass through 6 stages in only 3 clock periods. Due to the half-cycle delay between stages, the bits must be re-aligned in a register bank and then combined in a weighted sum to form the complete digital word.

$$v_{res}\left[k+\frac{1}{2}\right]=2^{n}\left(v_{in}[k]-D\cdot\frac{2v_{ref}}{2^{n}}\right) \quad (1)$$

2.1.3 Digital Redundancy

Digital redundancy, also referred to as digital correction [29], is the most commonly used method for correcting circuit non-idealities in pipelined ADCs and is standard practice in the pipelined architecture because it requires little change from the basic structure. Many sources of error in pipelined converters can result in a saturation of the stage transfer function at the top or bottom output rail and directly lead to missing or extended codes. Redundancy alleviates these errors.

By resolving one additional bit per stage in the sub-stage ADC and increasing the resolution of the sub-stage DAC to compensate for the added bit without changing the stage gain, the output swing of the ideal stage transfer function is cut in half like the transfer function of Figure 4. The remaining portion is left as a buffer zone to allow errors such as sub-stage ADC threshold offsets. Figure 4 also shows how a moderate threshold offset forces the transfer function to move into the buffer zone without causing saturation. This extended portion of the transfer curve is still within the input range of the next stage so no error occurs as long as the offset satisfies (2) where n is the total number of output bits from the stage and ΔV_{thresh} is the distance of an input threshold from its ideal location. A bit value that is not accounted for in the stage output bits as a result of the threshold error will simply be accounted for in the bits of the next stage.

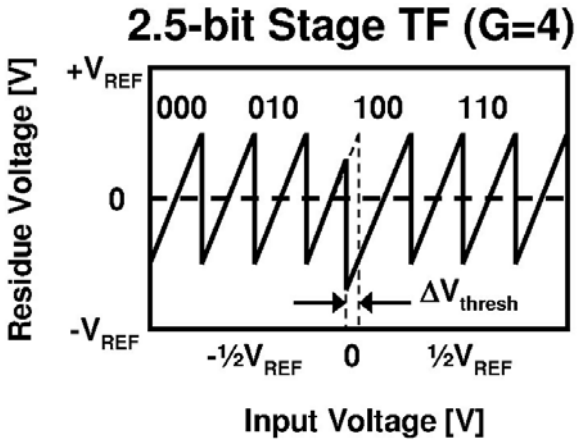


Figure 4: Transfer function of 2.5-bit stage with correctable threshold offset

$$\left|\Delta V_{thresh}\right| < \frac{1}{2}LSB = \frac{V_{ref}}{2^n} \tag{2}$$

Redundancy refers to this ability of adjacent stages to share the responsibility for converting bits of the digital word. To distinguish a stage with redundancy from a simple stage, a special name is given to it. A full 3-bit stage employing one bit of redundancy with its neighboring stages is often referred to as a 2.5-bit stage.

Output offsets in each stage are also corrected by digital redundancy as shown in Figure 5. Constant signal offsets at the output of a pipeline stage can be input referred leaving only an equivalent sub-ADC offset that is shown previously to be correctable with redundancy. Referring all offsets to the input of the converter yields a unified input offset that shifts the zero input code and slightly reduces the allowable input range instead of causing non-linearities.

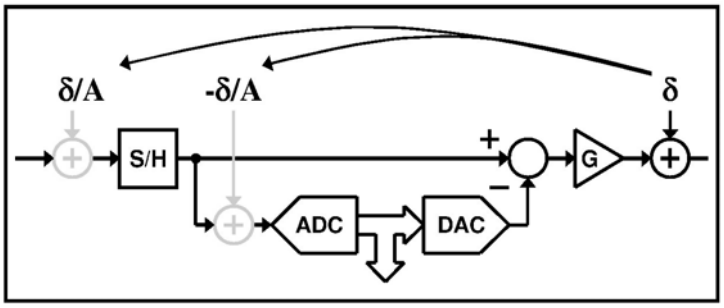


Figure 5: Input referral of stage output offsets

A popular implementation of digital redundancy involves an intentional shift of all threshold values by ½ LSB and removal of the outlying threshold level resulting in the transfer function of Figure 6. While still correcting moderate offsets, complexity is reduced by one threshold and mid-scale linearity is improved by offsetting the center threshold [29]. Other redundancy implementations require both addition and subtraction when combining the bits into the digital word, but this style of redundancy requires only addition. When the output bits from every stage are realigned in time, they are weighted so the redundant bits overlap and summed together like the example in Figure 7 of a 5-bit converter with three 1.5-bit stages and a final 2-bit flash ADC.

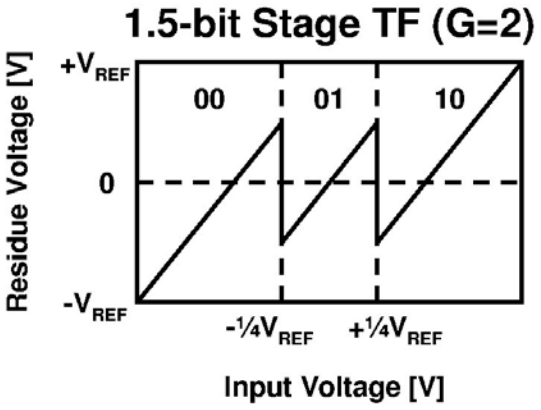


Figure 6: Transfer function of commonly used 1.5-bit stage

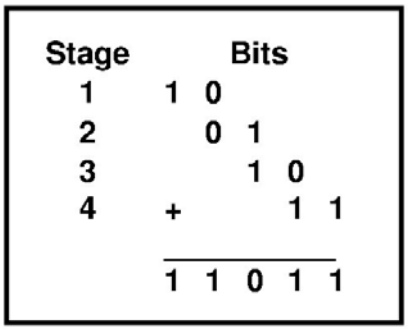


Figure 7: Recombination of stage bits using only addition to form the digital word

2.2 Basic Circuit Implementations

The functionality of a pipelined ADC stage is often implemented in two circuit blocks that can be called the subADC and MDAC. The sub-stage ADC of Figure 2 is implemented by a small flash comparator array referred to as the subADC while the sample-and-hold, sub-stage DAC, and difference multiplier are grouped into a switched capacitor (SC) circuit called a multiplying DAC (MDAC). Many designs also use a dedicated sample-and-hold at the front of the pipeline so that the first pipeline stage samples a DC value instead of a constantly varying input signal.

2.2.1 Circuit Timing

Operation of the stage occurs generally in two phases, the first for sampling the input and the second for resolving and amplifying the residue. For this purpose, non-overlapping clocks are generated and distributed to the stages so that the sampling phase clock (ϕ_S) of a stage is also the amplification phase clock (ϕ_A) of the following stage. *Primed* clocks, also called early clocks, are generated with early fall times to capture the residue before the amplification configuration of the MDAC changes and prevent SC sampling errors. Figure 8 and Figure 9 show the phase timing and a straight forward circuit for implementing the non-overlapping and early clocks. Additional inverters or capacitive loads can be inserted to modify the clock edges.

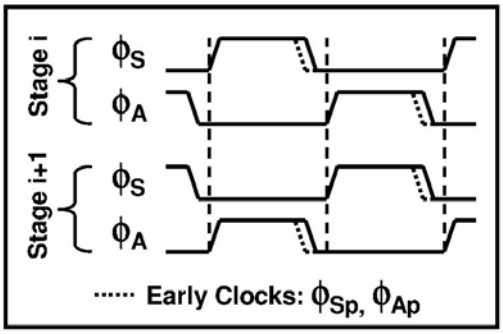


Figure 8: Non-overlapping clocks used to signal the sampling and amplification phases of the pipelined stages

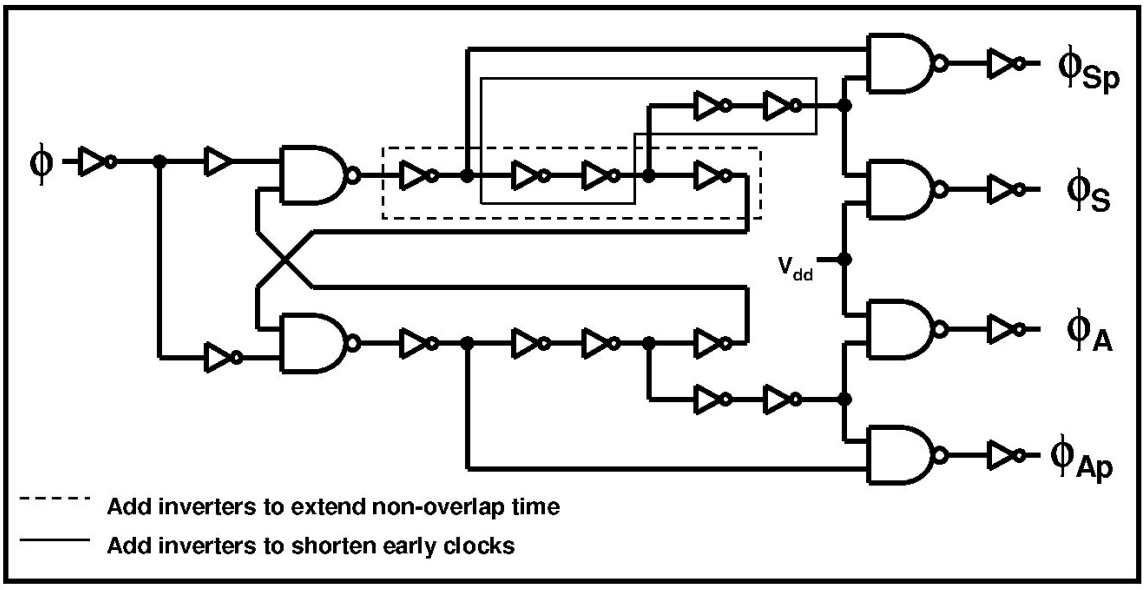


Figure 9: Generation of non-overlapping and early clocks

2.2.2 SubADC

The subADC flash array is composed of latching comparators with front-end SC networks. In the typical cell configuration of Figure 10, the SC network generates the difference between the threshold level and the input signal and the comparator amplifies and latches the difference to hold the decision. The thermometer coded flash output is then digitally manipulated to be used by the MDAC and saved in a register for assembling the output digital word. Threshold levels can be generated by a resistor string

or by scaling the converter reference level with capacitor ratios in the SC circuit when an additional set of capacitors is used. Alternative designs differ in the way the difference between the input the threshold is generated, the timing of the SC circuit, and the structure of the comparator. A digital encoder is also included with the subADC that uses the thermometer coded bits from the comparators to generate the MDAC control bits.

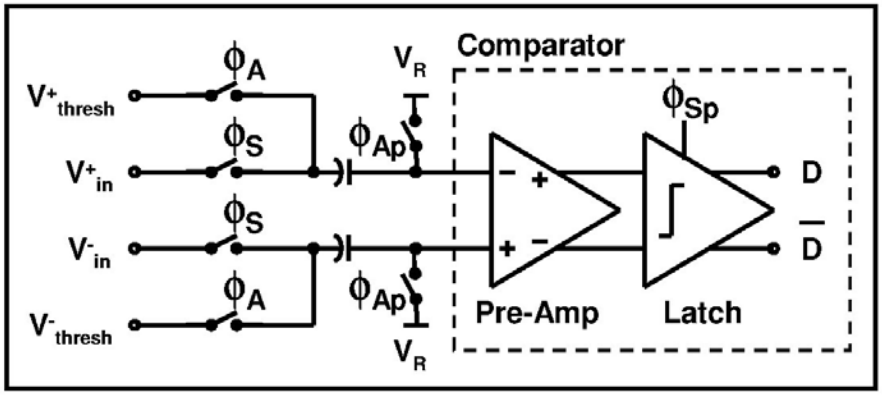


Figure 10: A cell of a basic subADC flash converter

2.2.3 MDAC

The MDAC encompasses the sampling, sub-stage DAC, and difference amplifier functions in a single, SC circuit. It is composed of an array of capacitive input sampling networks, an array of switched DAC capacitors controlled by the subADC, and an amplifier with a feedback capacitor. An efficient implementation shown in Figure 11 uses the same capacitors in the sampling and DAC array. During the sampling phase the MDAC samples the input signal by trapping charge on the top plate of the sampling capacitors (C_{Sx}) when the early clock falls. When the amplification phase begins, the sampling capacitors are connected to the DAC references and the top plate charge flows into the virtual ground of the amplifier to collect on the feedback cap. The ratio of the total sampling capacitance to the feedback capacitance decides the gain of the stage and the multiplexers in the DAC network use the subADC outputs to add or subtract the voltage reference.

An efficient change to this structure uses one of the sampling capacitors as the feedback capacitor by switching it over into feedback with the amplifier during the amplification phase [29]. This structure is sometimes referred to as the *flip-over* MDAC.

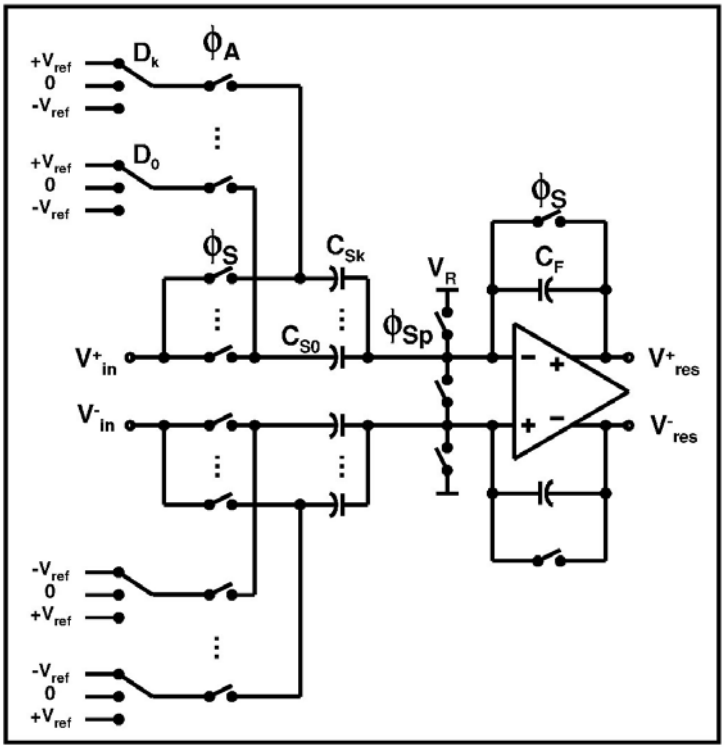


Figure 11: The MDAC performs the sampling, sub-stage DAC, and difference amplifier functions in a single, SC circuit

2.2.4 S/H

The front-end sample-and-hold can be composed of only an amplifier and a flip-over capacitor switching network. It is often used to ensure that there is no mismatch between the voltage captured by the first stage subADC and MDAC input sampling networks. Though the S/H is a simple circuit, suppressing non-linearity and noise errors has a high power cost, making it one of the most power hungry blocks in the converter. For this reason, previous designs propose removing the input S/H thereby significantly decreasing the power consumption of the ADC [32][37][7][20].

2.3 Sources of Error

The most common sources of error in Pipelined ADCs have been well known for some time [39] and many creative solutions in both the analog and digital domains have been proposed. Figure 12 shows the relationship between errors as they appear in the first stage transfer function and how they appear for the overall converter.

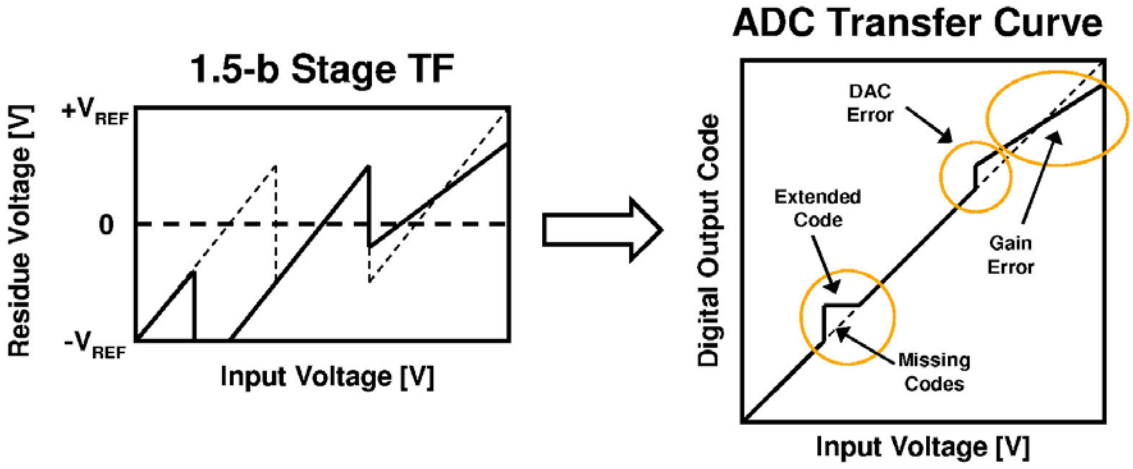


Figure 12: Errors in the 1st stage transfer function lead to distinguishable errors in the overall converter transfer function

2.3.1 Offset Errors

Small offset errors are correctable with redundancy, but a threshold offset that exceeds the digital redundancy range results in a saturation of the stage transfer function and possible extended or missing codes in the overall transfer function. This can be caused by comparator offsets, amplifier offsets, or switch charge injection that are consistent from sample to sample. When saturation occurs, the residue appears outside of the intended amplifier output swing. The resulting gain compression is not necessarily abrupt but accumulates and amplifies through each stage if the over-range signal is not brought back within the safe residue range.

2.3.2 DAC and Gain Errors

DAC errors appear if the transition jumps in the stage transfer function are not the correct height and gain errors are deviations of the gain radix from its ideal value. These errors can be caused by stage-to-stage reference variations, DAC capacitor mismatches, or finite OpAmp gain and are tightly coupled through the MDAC functionality such that a gain error can also cause a DAC error. A front-end S/H can exhibit gain errors but its transfer function is ideally linear so only a change in signal amplitude occurs, whereas gain errors in an ideally non-linear pipeline stage results in linearity problems in the overall conversion. On the other hand, higher order gain effects such as the gain compression of an OpAmp can lead to non-linearities through any transfer function.

Mismatch between capacitors poses an important design challenge because it often limits the achievable linearity of the ADC. DNL errors appear in the transition of one MDAC digital input to the next, or more precisely as the capacitors used in the MDAC change with the digital codes from the subADC. A gain error at the output of the MDAC is $\Delta C/C$ where C is the unit capacitor size of the stage and ΔC is the standard deviation of the unit capacitance. Referring the error to the input of the stage and relating the unit capacitance to the total input sampling capacitance of the stage (C_{tot}) and the stage resolution (m), the DNL resulting from capacitor mismatch in the first stage is known as

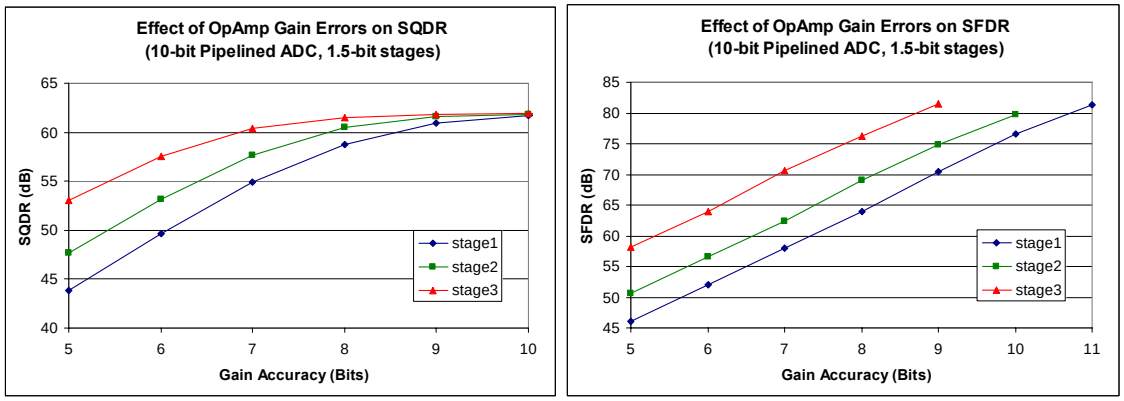
(3) [42] with *N* and *k* being the total ADC resolution and measurement-based matching constant in units of [$C^{1/2}$] respectively. It is shown that the DNL of an N-bit converter is improved by √2 for every additional bit resolved in the first stage or doubling of the total sampling capacitance.

$$\mathbf{DNL} = \mathbf{k}\frac{\mathbf{2}^{\mathbf{N}-\frac{\mathbf{m}}{\mathbf{2}}}}{\sqrt{\mathbf{C}_{\mathbf{tot}}}} \tag{3}$$

An upper bound INL estimation for capacitor errors in the first stage can be expressed similarly by accounting for the errors in all capacitors in the MDAC and assuming the INL errors across the transfer function occur in an even bow shape with 2^m thresholds, resulting in (4). Unlike the DNL, the INL does not depend on the stage resolution and can be improved by the designer only by increasing the total input sampling capacitance. It should be noted however that resolving more bits in the first stage reduces the impact of errors in later stages.

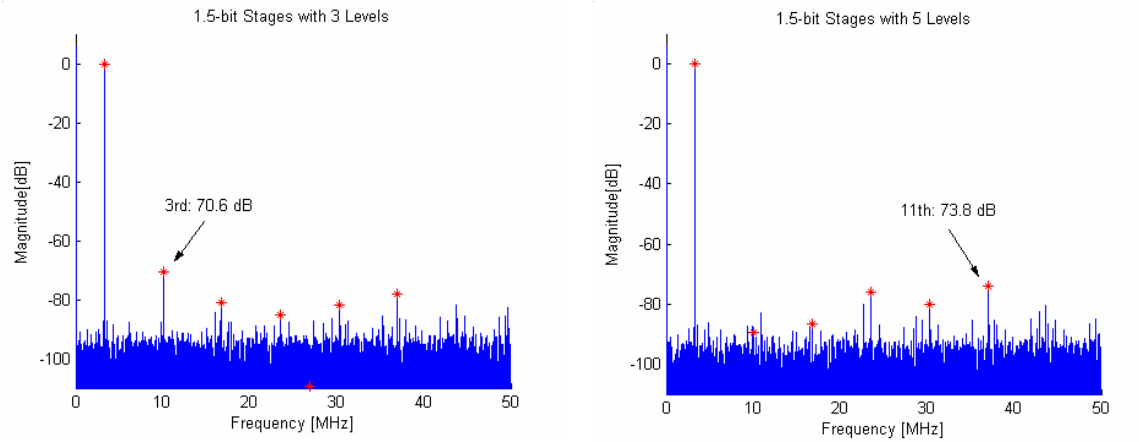
$$\mathbf{INL} \cong \mathbf{k}\frac{\mathbf{2}^{\mathbf{N}-\mathbf{1}}}{\sqrt{\mathbf{C}_{\mathbf{tot}}}} \tag{4}$$

The effect of gain errors at the output of a particular stage on the signal to quantization noise plus distortion ratio (SQDR) and spurious free dynamic range (SFDR) for a 10-bit pipelined ADC with 1.5-bit stages is found using a Simulink model and shown in Figure 13 (a) and (b) respectively. Note the effect of quantization limiting the upper bound for the SDR to just below 62 dB and that the SFDR graph can also be used for similar converters with different resolutions. (a) demonstrates that the gain accuracy must be greater than the conversion resolution of the following stages to not limit the SQDR but (b) shows that even more gain is needed for a SFDR greater than 70 dB. The dominating harmonic of distortion due to a gain error can depend on the subADC. Using a 3-level flash in a 1.5-bit stage shows a dominant 3rd harmonic but using a 5-level flash shows a dominant 9th harmonic with improved SFDR as seen in the FFTs of Figure 14 (a) and (b).



(a) (b)

Figure 13: (a) SDR and (b) SFDR performance of a 10-bit pipelined ADC with 1.5-bit stages and a gain error at the output of the 1st, 2nd, or 3rd stage



(a) (b)

Figure 14: Comparing the effect of 9-bit gain accuracy on a 1.5-bit 1st stage of a 10-bit converter with (a) 3 and (b) 5 levels

Viewed from the static perspective, gain errors cause large jumps in the INL and narrow codes in the DNL at the code locations of the subADC thresholds. There is no simple relationship between the harmonic content and the static linearity curves, but approximate trends are observable. For example, the DNL and INL of a 10-bit converter are shown in Figure 15. The converter uses 1.5-bit stages with 3-level flash subADCs and

has only 7-bit gain accuracy in both the 1st and 2nd stage, resulting in a +2/-1.6 INL with an observable 3rd order shaping. This corresponds to a 56 dB SFDR due to the 3rd harmonic and a 49 dB SDR.

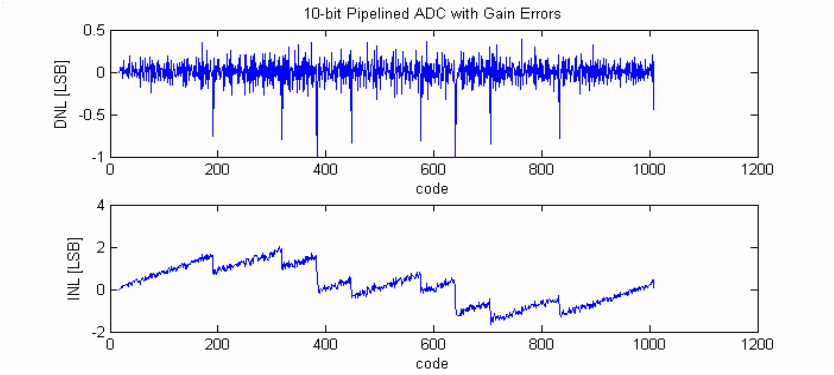


Figure 15: Static linearity measurements of a 10-bit pipelined ADC with 7-bit gain accuracy in the 1st and 2nd stage

3 Basic Design Considerations

A comprehensive study of pipelined ADCs reveals a long list of design considerations that result in tradeoffs in performance. As an example, the SNR is strongly tied to the amount of power spent and the capacitor sizes used, which then influences the design parameters for the OpAmp, and so on. The primary considerations include the choice of stage resolution, the design of OpAmps and comparators, the sizing of switches, and the budgeting of noise.

3.1 Stage Optimization for Speed, Power, and/or Linearity

Resolving more bits per stage has the advantage of reducing the effect of non-linearities and noise introduced later in the pipeline, allowing less power consumption in the backend. The reduced effect of noise in later stages due to the stage gain also enables capacitor scaling for further power savings down the pipeline. The drawback is the decreased OpAmp feedback factor that requires more power to achieve the desired speed, the exponentially increasing number of comparators used in the subADC, and the decreasing redundancy range.

These observations lead to optimizations of the pipeline stages. Considering conversion rate, die area, and power consumption as a balance between OpAmps and comparators, [28] argues that high speed pipelines converters with redundancy are optimized using the minimum resolution of 1.5-bit per stage. To the contrary, when considering settling time and the tradeoff between capacitance scaling and power, a “zeroth order” analysis reveals that scaling capacitors by the interstage gain and resolving more bits per stage optimizes the power [15]. This is due to the fact that for higher resolution converters the next stage capacitors, and not the comparators, tend to dominate the load of the OpAmp. An improved “first order” analysis by the same author that includes additional loads and parasitics suggests a scaling factor 1 to 1.5 times larger than the inter-stage gain and improved power performance with larger stage resolutions. Most

of the power saving occurs when transitioning from a 1.5 to 2.5-bit stage with diminishing returns for additional increases in resolution, and in fact, resolutions above 4.5-bits may increase the power due to parasitic and loading effects not accounted for in the optimization.

3.2 OpAmp Design

Nearly all the power and much of the added noise in the ADC are respectively dissipated and generated in the OpAmps of the first couple stages therefore it is essential to design using only enough power and bandwidth to safely meet the performance needs.

Due to the switched capacitor nature of the MDAC, the OpAmp must settle to its final value within certain accuracy during the amplification phase. To ensure accuracy greater than the remaining stages of the pipeline in the presence of a settling gain error, the basic minimum first stage OpAmp loop UGBW, f_u [Hz], is given by (5) where N is the converter resolution, m is first stage resolution, and $T_{1/2}$ is half of a clock period. The first stage finite OpAmp gain must also be above a minimum value given by (6) for the feedback factor β.

$$f_u > \frac{(N-m)\cdot \ln 2}{2\pi \cdot T_{1/2}} \tag{5}$$

$$A > \frac{2^{N-m}}{\beta} \tag{6}$$

The output swing of the OpAmp limits the dynamic range between the stages and is critical in low voltage designs where multi-stage OpAmp structures with common-source output stages are mandatory to maximize the output swing. On the other hand higher voltage processes or processes with thick gate oxide devices have plenty of headroom and can choose single stage structures with multiple cascodes or gain boosting, thereby using a simpler structure with better noise performance and often less power.

3.3 Comparator Design

The comparators of the subADC are responsible for making their bit decisions after the stage input is adequately settled but before the beginning of the amplification phase to allow as much time as possible for the OpAmp to settle. If the subADC is triggered at the end of the sampling phase, then the comparator must resolve the result within the non-overlapping time of the clocks, imposing high speed requirements on the comparator. Many comparator designs are composed of a fully differential, low gain, high speed preamp to suppress offsets and a latch to capture the decision similar to Figure 16.

Some designers instead argue that the signal can be sufficiently settled within the redundancy range mid-way through the sampling phase so the subADC can trigger its decision earlier as long as the kickback does not significantly disturb the MDAC sample, allowing the comparator to have reduced settling requirements [33].

The number of bits resolved by a stage largely influences the required complexity and power use of the subADC comparators. Large stage resolutions offer little redundancy range to correct offsets, so higher gain preamps or offset correction techniques are used. Low stage resolutions can take full advantage of the offset lenience afforded by redundancy and use a simple, single stage, dynamic latch to save power, sometimes using transistor ratios to embed the reference threshold levels used for comparison [14].

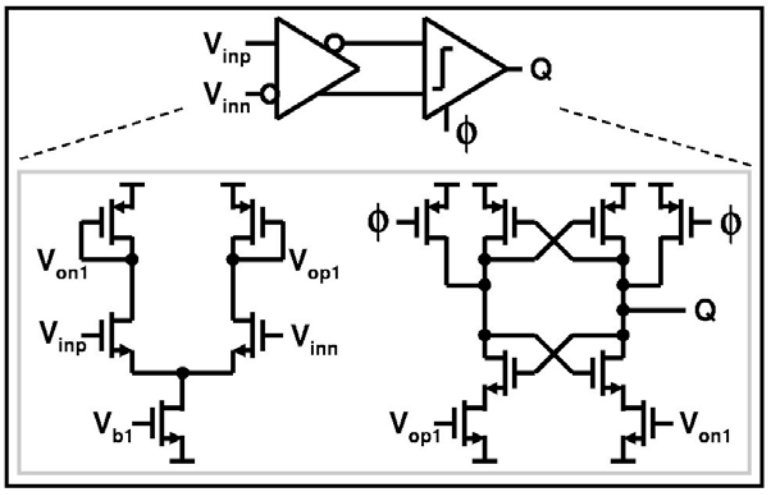


Figure 16: Basic comparator with preamp and latch

3.4 Switch Sizing

The impact of switch resistances on the settling response of the MDAC can be significant and should be accounted for early in the design process and designed to have desirable or insignificant effects on the response without introducing too much charge injection or too large of a load to the clock drivers. It is shown that for an MDAC with a single stage OpAmp, resistance in series with the feedback capacitor during amplification can lead to severe peaking whereas resistance in series with the input capacitors can serve to dampen the system as shown in Figure 17 [10]. It is recommended that the RC constants formed in each branch of the MDAC be designed to have bandwidths 3 times greater than the desired loop UGBW.

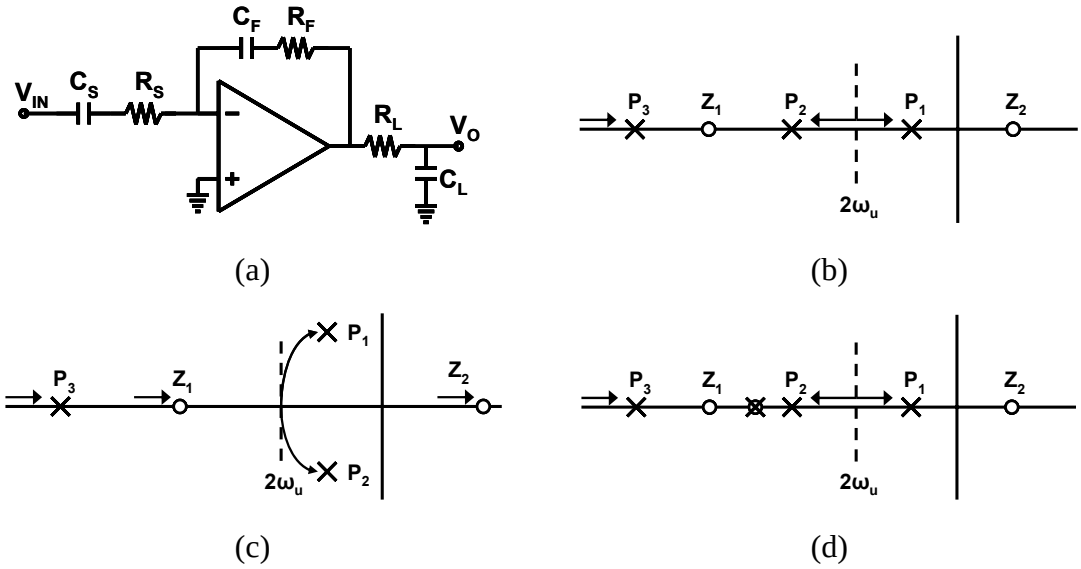


Figure 17: Effect of switch resistances on the poles/zeros of a (a) amplifying MDAC structure caused by resistances in the (b) sampling path – R_S, (c) feedback path – R_F, and (d) load path – R_L

3.5 Noise

For a given fabrication process and pipelined converter specification, the amount of necessary power is greatly decided through noise considerations. Using smaller capacitors for SC networks and OpAmp compensation fundamentally decreases the SNR

performance due to increased noise bandwidths. As a result, more power must be used to drive the larger capacitances when higher noise performance is desired. The most prominent noise sources in pipelined ADCs include quantization, sampling networks, OpAmps, input sampling clocks with jitter, and reference supplies. A noise budget assigns each source a portion of the total allowable noise for the desired performance.

3.5.1 Quantization Noise

Quantization noise is determined by the bit resolution of the converter and poses a fundamental limit to the SNR. The discontinuities of the ADC transfer function as the output changes from one LSB to the next effectively appear during dynamic operation as a white noise floor whose noise power is given for an N-bit ADC by (7) [23]. A simplified equation for the maximum achievable SNR is given by (8).

$$\overline{v}_{nQ}^{2} = \frac{(2V_{ref})^2}{2^{2N} \cdot 12} \tag{7}$$

$$SNR\,[dB] \leq 6.02 \cdot N + 1.76 \tag{8}$$

3.5.2 Sampled Thermal Noise

Sampling theory states that when a signal is sampled, its frequency spectrum is repeatedly copied in the frequency domain to every integer multiple of the sampling rate, creating aliasing for frequencies of the input signal greater than the Nyquist frequency. In a SC sampling network, the bandwidth created by the sampling capacitance and the switch resistance is typically well passed the Nyquist frequency, causing the entire spectrum of switch thermal noise to fold back into the base-band.

Integrating over the noise power spectrum and using the double sided spectral density of a resistor yields a total noise power given by (9). The resulting quantity is dependent only on the sampling capacitance for a given operating temperature, illustrating the need for larger capacitances to reduce sampling switch thermal noise

power. Due to the simplicity of the resulting quantity, sampled noise from RC band-limited structures is also referred to as *kT/C* noise.

$$\overline{v_{nS}^2} = \int_{-\infty}^{\infty} \frac{2kTR}{1+(2\pi f \cdot RC)^2} df = 2 \cdot 2kTR \frac{1}{2\pi RC} \cdot \frac{\pi}{2} = \frac{kT}{C} \tag{9}$$

3.5.3 OpAmp Noise

The evaluation of OpAmp noise in pipelined ADCs is important because it is often comparable in quantity to sampled switch thermal noise. Channel thermal noise generated by MOSFETs operating in saturation accounts for most OpAmp noise. With the noise bandwidth determined by the unity gain bandwidth of an OpAmp in the feedback configuration, integrating the PSD yields (10) with unity gain bandwidth ω_u, compensation capacitor $C_{C,}$ input pair transconductance $g_{mi,}$ and total OpAmp first stage equivalent thermal noise transconductance G_{n1}. The equivalence assumes a single stage or Miller compensation and a dominant pole system. Noise from any subsequent OpAmp stages are attenuated by the first stage gain and can often be ignored.

Reducing OpAmp noise for a given speed performance is accomplished by choosing simple OpAmp topologies such as the telescopic structure to minimize the number of noise sources, choosing an efficient MDAC structure to maximize the feedback factor, or increasing the input transconductance along with the compensation capacitor at the cost of increasing the power consumption for a given speed.

$$\overline{v_{nOPo}^2} \approx \frac{2}{3} kT \left(\frac{G_{n1}}{g_{mi}^2} \right) \frac{\omega_u}{\beta^2} \approx \frac{2}{3} \frac{kT}{C_C} \left(\frac{G_{n1}}{g_{mi}} \right) \frac{1}{\beta} \tag{10}$$

Flicker noise also contributes a non-ignorable amount of noise in pipelined ADCs but is not easily quantified in an SNR analysis due to its discontinuity at DC. From a low frequency perspective, flicker noise can be treated as a small signal offset and input referred to the front of the pipeline.

3.5.4 MDAC Noise analysis

The design of the MDAC in a pipelined ADC strictly depends on the allowable kT/C noise therefore proper analysis of the noise sources is essential. Designers sometimes use analysis equations that both overestimate (or underestimate) the noise and fail to identify the true source of the noise. The following general MDAC example gives an analysis identifying the cause and quantity of the noise sources, and then simplifies the analysis with approximations.

Figure 18 (a) and (b) show the configuration of a generalized, single-ended MDAC in its sampling and amplifying phases respectively. (a) shows three critical RC networks that result in sampled thermal noise when the sampling phase clocks de-assert. The noise charges sampled onto these capacitances move onto the feedback capacitor during the next phase resulting in a charge to voltage conversion and amplification by the capacitor ratios. (b) shows another set of RC networks during the amplification phase that transfer noise to the next pipeline stage sampling capacitor through a different bandwidth limitation. By conventional design, the time constants of the sampling, DAC, and feedback RC branches are greater than the unity gain frequency of the feedback loop to prevent parasitic poles. The OpAmp loop therefore defines the noise bandwidth of the switch thermal noise during the amplification phase. Ignoring the effect of the resistances on the closed loop system, these observations lead to output referred noise of (11) where the first term represents the noise sampled during the first phase transferred onto the feedback capacitor and the second term represents the OpAmp filtered switch thermal noise sampled by the next stage during amplification.

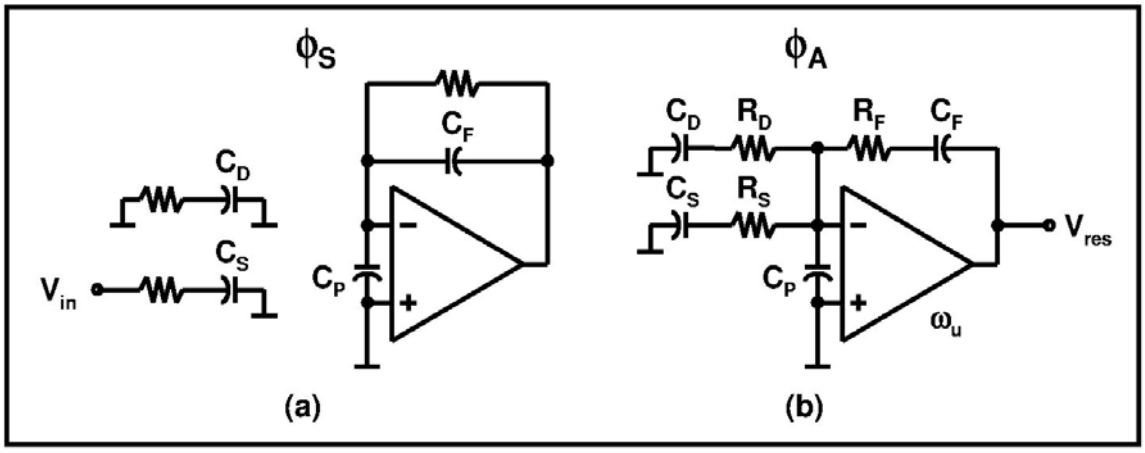


Figure 18: MDAC noise analysis models for the (a) sampling (b) amplification phases

$$\overline{v}_{nSo}^{2} = \frac{kT\left(C_S + C_D + C_P + C_F\right)}{C_F^2} + kT\omega_u\left[R_s\left(\frac{C_S}{C_F}\right)^2 + R_D\left(\frac{C_D}{C_F}\right)^2 + R_F\right] \tag{11}$$

$$\overline{v}_{nSo}^{2} = \frac{kT}{\beta_A C_F} + \frac{1}{\alpha}\cdot\frac{kT}{C_F}\left(\frac{C_S}{C_F} + \frac{C_D}{C_F} + 1\right) \tag{12}$$

$$\overline{v}_{nSi}^{2} \approx 2\frac{kT}{\beta_A C_F}\cdot\frac{1}{G^2} \tag{13}$$

Recognizing the amplification phase feedback factor β_A in the first term and expressing the RC bandwidths as α times larger than the unity gain bandwidth, the equation reduces to (12). Overestimating the noise by setting α=1, approximating the feedback factor in the second term, and input referring the noise to the stage input by dividing by the squared pipeline stage gain yields the “engineer friendly” approximation of (13). Note that a more appropriate value of α=2 to 3 yields a noise overestimation by 33% to 50%.

Simple techniques for reducing switch thermal noise in MDACs include using a flip-over style MDAC and reusing the sampling capacitors as the DAC capacitors. Using these techniques while ignoring the OpAmp input parasitic reduces the stage input referred noise to (14) which illustrates that the stage kT/C noise is dependent primarily on the total input sampling capacitance.

$$\overline{v}_{nSi}^{2} \approx 2\frac{kT}{C_S} \tag{14}$$

The OpAmp can also contribute noise during both phases. During the sampling phase the OpAmp noise is sampled onto the input parasitic capacitor while during the amplification phase the noise is sampled by the next stage. In this case, the output referred OpAmp noise is approximately given by (15). Once again, a flip-over style MDAC nearly reduces this quantity in half because OpAmp noise is not sampled by the feedback capacitor during the sampling phase.

Note that using a fully differential structure doubles the noise power quantities of this analysis but will ultimately increase the SNR by only √2 due to the increased signal swing.

$$\overline{v}_{nOPo}^{2} \approx \frac{2}{3}\cdot kT\left(\frac{\omega_{uS}}{1^2}\cdot\frac{C_p^2}{C_f^2}+\frac{\omega_{uA}}{\beta_A^2}\right)\cdot\frac{G_{n1}}{g_{mi}^2} \approx \frac{2}{3}\cdot\frac{kT}{C_C}\left(\frac{G_{n1}}{g_{mi}}\right)\cdot\left(\frac{C_p^2}{C_f^2}+\frac{1}{\beta_A}\right) \tag{15}$$

3.5.5 Sampling Jitter

The front-end of the converter is sensitive to variations in the periodicity of the sampling clock. Any noise jitter in the clock manifests as a signal frequency dependent noise source given by (16), limiting the SNR to (17) [40]. This poses a stringent limitation for high speed pipelined converters.

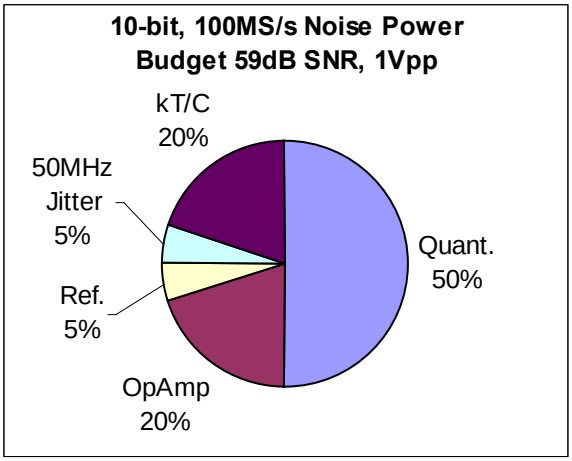
$$\overline{v}_{nJ}^{2} = \left(\frac{V_{in,p-p}}{2\sqrt{2}}\cdot 2\pi f_{in}\right)^2 \overline{\sigma}_{jitter}^{2} \tag{16}$$

$$SNR \le 10\log\left(\frac{1}{\omega_{in}^2\cdot\overline{\sigma}_{jitter}^{2}}\right) \tag{17}$$

3.5.6 Noise Budget and SNR

Figure 19 shows an example noise power budget for a 100MS/s data converter targeting 59 dB SNR performance with a 1 V peak-to-peak input range. Quantization

noise dominates for low resolution converters followed typically by OpAmp and kT/C noise though tradeoffs are made to make the use of lower power or higher speed components. Noise from the reference supplies is also given a portion of the budget. This budget is roughly achieved with 1.5-bit stages using 1 pF input sampling capacitors scaled down by 2 each stage and 800 fsec sampling jitter at the Nyquist frequency of 50 MHz.



Noise Sources	Percent of Noise Power	Noise Power [nV^2]
Quantization	50	78.5
kT/C	20	31.4
OpAmp	20	31.4
Jitter	5	7.9
References	5	7.9
Total	**100**	**157**

Figure 19: An example noise power budget for a 10-bit pipelined ADC

4 Low Voltage Pipelined ADC Design

Designing pipelined ADCs at low voltages presents many challenges that do not exist for higher voltage designs. Issues such as floating switches, reduced headroom, reduced OpAmp performance, and poor component matching limit the structural options of the converter, decrease most aspects of performance, and often require additional power and complexity to solve. Many creative solutions such as bootstrapping, the switched-OpAmp technique, the OpAmp reset switching technique, and the switched-RC technique have been proposed to solve these issues.

4.1 Design Issues

4.1.1 Floating Switches

A transistor switch placed in series with a large swing signal path is referred to as a *floating* switch because it operates in triode during the on state while its drain and source track the input signal. These exist frequently in switched-capacitor circuits at front end sampling networks and OpAmp outputs, posing severe limitations when supply voltages are reduced to around twice a transistor threshold value.

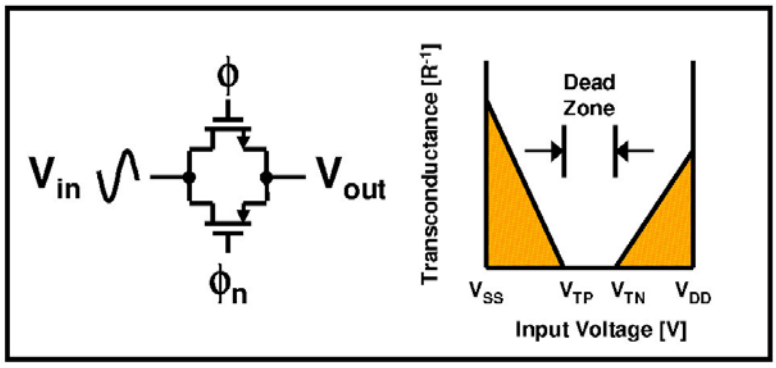


Figure 20: Dead zone of a floating transmission gate switch at low voltage supplies

Varying overdrive voltages on floating switches cause signal dependent sampling bandwidths resulting in non-linearities. In the extreme, limited overdrive can result in

dead zones for transmission gates, shown in Figure 20, preventing conductance at mid supply. Addressing the floating switch problem is a major structural concern for low voltage switched capacitor circuits. Critical switches in the basic MDAC of a pipelined ADC stage of Figure 21 are floating.

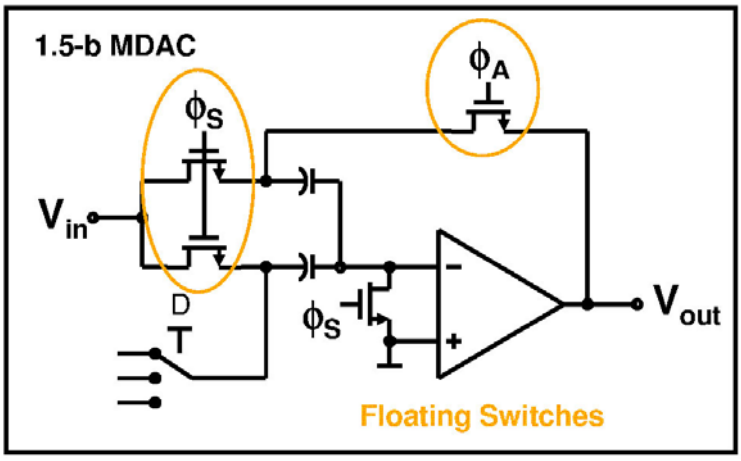


Figure 21: Floating switches present in a basic 1.5-bit MDAC

The insufficient overdrive can be alternatively viewed as a large threshold voltage issue, but reducing the threshold to allow more conduction trades one problem for another. Low thresholds prevent MOS devices from completely turning off, allowing charge to leak across the channel. With many data converter architectures relying on switched-capacitor circuits, this charge leakage compromises the accuracy.

4.1.2 Reduced Headroom

Reducing the supply for digital circuits is very desirable because the power is proportional to the voltage squared but a reduction in an analog supply voltage does not yield such a power savings advantage. Reducing the voltage will linearly decrease the power spent on the important transconductances that determine the circuit speed, but this also decreases the signal swing range, such as with the common-source output stage of Figure 22.

Maintaining the SNR and speed performance with the reduced headroom involves increasing capacitances, transconductances, and power. Due to headroom and structural limitations, maintaining the SNR for ultra-low voltage circuits can dissipate even more power than a circuit operating at a higher supply.

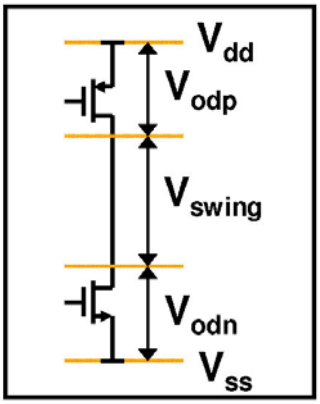


Figure 22: Limited headroom of a common-source output stage

4.1.3 Reduced OpAmp Performance

The number of transistors that will fit between the positive and negative rail is limited at low supply voltages. High performance OpAmp designs using telescopic structure with triple cascodes are no longer possible, leading to an increase in complexity, power, and noise. In addition, the switch type in low voltage SC circuits is preferably NMOS because of its higher electron mobility, which restricts OpAmp speeds further by requiring PMOS input differential pairs.

The low-voltage OpAmp of choice for many published designs [10] [11] [12] is the folded cascode input stage structure with a common-source output stage for wide output swing. Using both N- and P- cascades in a folded cascode structure, the minimum allowable supply voltage is (18) for the given threshold and overdrive voltages.

$$V_{ddmin} = \max\left[2V_{odp} + V_{tp}\,,\, 2V_{odp} + 2V_{odn} + V_{swing}\right] \tag{18}$$

Biasing transistors tightly under low voltages also leads to poor gain performance because of the limited V_{ds} voltages, especially for high speed designs where the necessity for minimum length devices and large currents already reduces the available output resistance. Achieving a gain much higher than 70 dB for high-speed CMOS designs requires either additional stages or gain boosting and solutions to stability issues that come with each technique.

4.1.4 Poor Component Matching

Random variations in components, as well as process related effects such as etching and local gradients become a more severe issue in processes with smaller dimensions, leading to matching problems between devices. Transistor threshold voltage offsets lead to input referred OpAmp offsets and threshold offsets in comparators that occupy the redundancy correction range of pipelined ADCs. Even worse, capacitor mismatches directly limit the linearity of the overall converter. High accuracy converters require the use of calibration to correct for mismatches that limit performance.

4.2 Low Voltage Design Solutions

4.2.1 Clock Boosting & Bootstrapping

Sampling non-linearity caused by a signal dependent, sampling network bandwidth is a direct result of insufficient overdrive voltage on a floating switch in the signal path. To eliminate this problem, the gate switch voltage can either be boosted to a voltage where the signal dependence is reduced or it can be *bootstrapped* so that the gate tracks the source, almost eliminating the signal dependence. Bootstrapping is performed by charging a capacitor during one phase and then placing it between the gate and source of the switch during the next phase as shown in Figure 23.

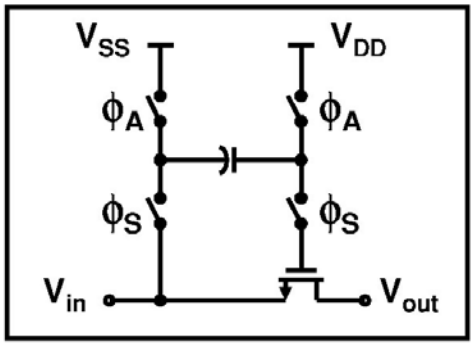


Figure 23: Basic bootstrapping concept

Voltage boosting suffers from severe reliability issues because the gate/source voltage can exceed the maximum reliable level every other phase, leading to oxide stress and breakdown over time. Boostrapping attempts to obviate reliability issues by preventing transients that break the reliable voltage levels. Figure 24 shows the bootstrapping circuit presented in [2] where M_{n1} is the bootstrapped switch and C_3 is the boosting capacitor. The circuit network containing C_1 and C_2 performs voltage boosting for charging C_3 while the remaining transistors contribute to switching C_3. M_{n3} and M_{n5} are added to protect M_{p1} and M_{n6} respectively from oxide stress. The remaining linearity limitations include non-linear drain and source capacitances and V_{gs} variations due to parasitic capacitances on the gate of the bootstrapped switch.

Though design can minimize oxide stress, the boosted voltage levels in the circuit may still pose potential reliability issues, especially as oxide thicknesses are reduced for faster processes.

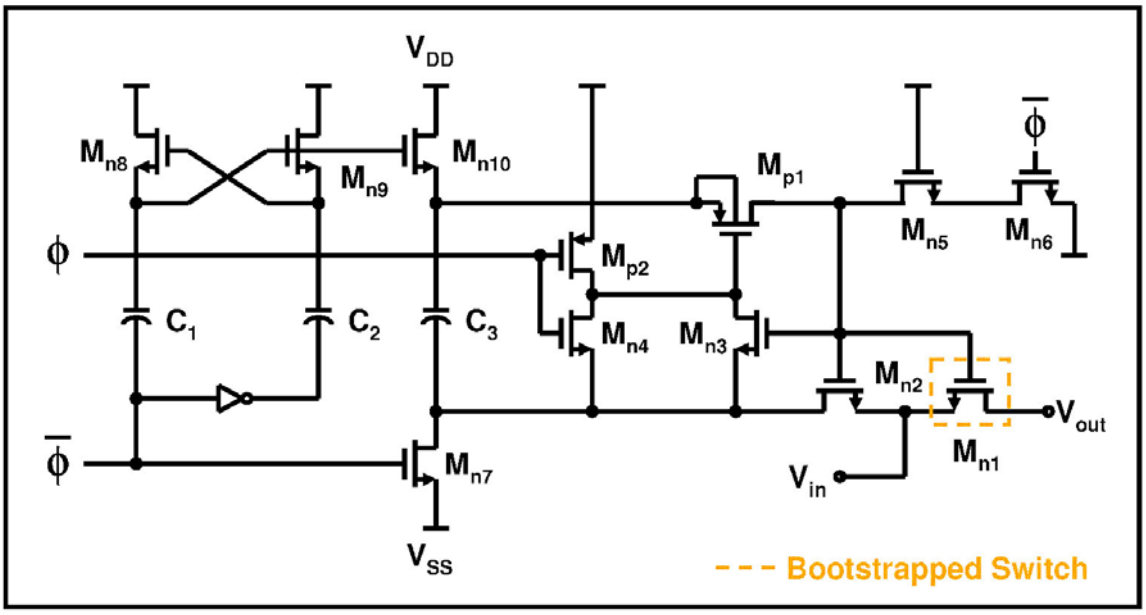


Figure 24: Bootstrapping circuit used in [2]

4.2.2 Switched OpAmp (SO) Technique

The switched OpAmp technique [17][41] solves the floating switch problem by removing the switch and providing isolation from the previous stage by momentarily turning the OpAmp off as shown in Figure 25. When the OpAmp is turned off, the output becomes a high impedance node that does not interfere with the reset. This technique also saves power because the OpAmp current is not used half of the time.

The major drawback of this technique is the inability of the output stage to quickly turn back on during amplification. For this reason, sometimes only the output stage is turned off and the input stage remains on for quicker recovery. A very high speed design using the switched OpAmp technique is demonstrated in [21] but its accuracy is limited to less than 10-bits.

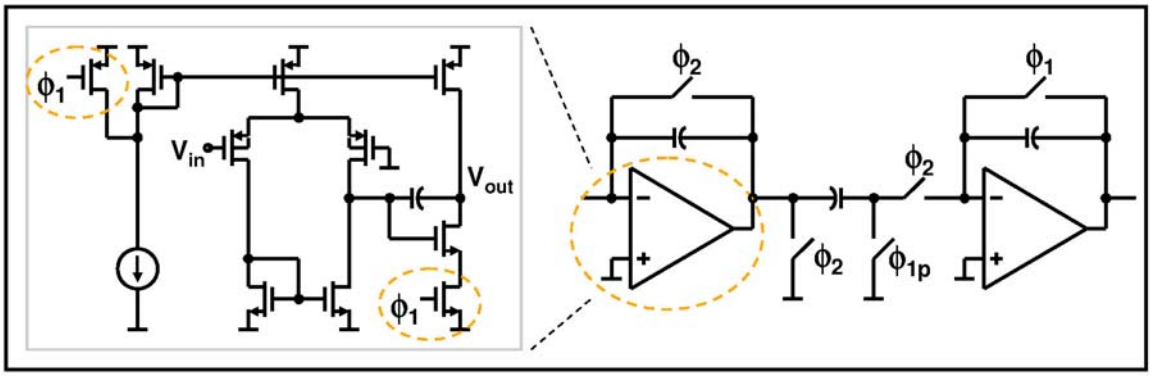


Figure 25: Switched OpAmp used in [17]

4.2.3 OpAmp Reset Switching Technique (ORST)

Originally proposed in [26], this technique is later developed and called the OpAmp Reset Switching Technique (ORST) [11] [12]. ORST solves the floating switch problem by removing both the floating switch and the reset switch on the top plate of the sampling capacitor and instead uses the previous stage OpAmp to perform the reset function. During the amplification phase (ϕ_2) of the simplified MDAC in Figure 26, the left amplifier is switched into unity gain configuration to provide a reset bias for the capacitor bottom plate. The technique is then improved further in [12] by placing the reset OpAmp in resistive feedback instead of unity gain configuration to relax the OpAmp stability requirements.

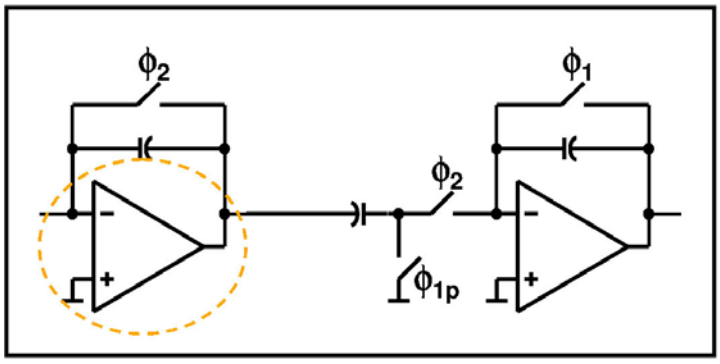


Figure 26: ORST Configuration

The primary functional challenge of this technique is the need to switch the output level of the amplifier between phases. This is necessary because the feedback switch is floating and requires a low OpAmp output voltage to conduct and reset the feedback capacitor therefore the output level is shifted to a lower level when in the reset mode. For a differential circuit, this means shifting the common-mode level between phases. To avoid using a fast CMFB circuit for a fully differential design, [11] and [12] use a pseudo-differential structure that accomplishes the common-mode shift simply by placing each OpAmp in feedback while the other input terminal is set to a low voltage. To reduce the common mode gain to one during the amplification phase, cross-coupled capacitors are used to introduce a small amount of positive feedback as a rudimentary form of common-mode feedback at the expense of decreasing the feedback factor. Using a pseudo-differential structure provides some even harmonic cancellation and supply rejection but is inferior to the rejection in fully differential circuits with common-mode feedback.

ORST also requires an input circuit that will perform the reset function for the first pipeline stage and sample a signal at mid-rail during one phase, and then provide a buffer of the sample during the next phase. This can be accomplished with a pseudo-differential implementation of [8] with enhancements.

Drawbacks include reduction in speed and increased noise. During the amplification phase, the settling properties of two amplifiers are linked together creating a two-real-pole system whose 10-bit settling time is about 1.34 times longer than the single pole system assuming the loop bandwidths of both OpAmps are equal. A large amount of noise from the reset OpAmp is also added to the residue output because it is amplified through the gain of the stage making the reset OpAmp more important than the stage OpAmp for noise considerations.

4.2.4 Switched-RC Technique

The Switched-RC technique [4] removes the floating switch and replaces it with a resistor. This resistance provides the isolation by sufficiently attenuating the differential signal of the previous stage OpAmp as shown in Figure 27. Using a resistor as the series device also has better sampling linearity than a transmission gate. Applied to a delta-sigma converter in the published work, the technique requires a trade-off between linearity and speed by choosing appropriate sizes for the resistor and the size of the reset switch. Insufficient attenuation of the signal by the reset switch does not lead to non-linearities, only a gain error in the integrator and its effect on the delta-sigma system.

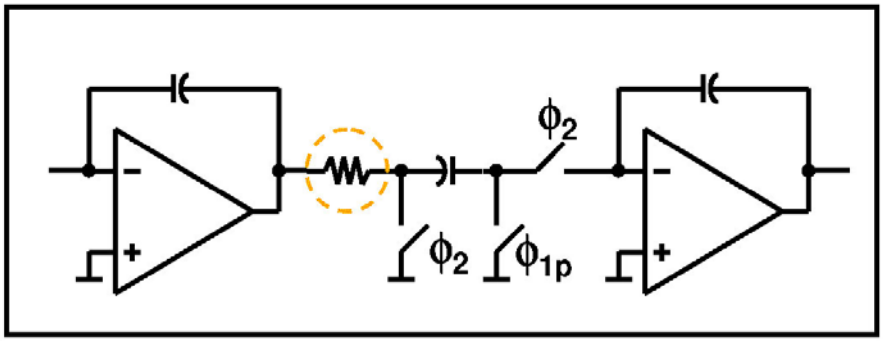


Figure 27: Switched-RC Configuration

Applied to a pipelined ADC, insufficient attenuation of the previous stage residue will lead to non-linearity in the conversion due to the nonlinear MDAC transfer function. Therefore, the output of the previous stage must be suppressed to accuracy greater than the back-end of the ADC and can be done by cascading multiple networks of resistors and shunt reset switches.

Adding additional resistance in series with the sampling capacitor in this way to provide attenuation for the switched-RC technique exacerbates the fundamental tradeoff between speed and accuracy. The tradeoff can be improved by decreasing the on resistance of the shunt switch in the switched-RC network but only to the point when the

parasitic capacitance begins to limit the bandwidth and the switches become too large to be driven by a reasonably sized clock buffer.

The switched-RC method also does not address the issue of resetting the feedback capacitor because it is developed for integrators. Recent work, similar to this author's proposed technique, uses a hybrid of the ORST and switched-RC techniques but uses actual resistors in feedback during the reset phase with switches at the virtual ground to activate the resistive feedback [5]. Described as merely the switched-RC technique applied to pipelined ADCs, the circuit requires accurate resetting of the OpAmp to remove the differential charge from the feedback capacitor, so it requires similar functionality as the ORST. The difference is that the common-mode does not need to change and the virtual ground bias is set by the ratio of the feedback resistors. These resistors must dominate over the activating switch resistance, imposing a greater speed limitation from the RC pole at the OpAmp input than for this author's proposed method.

4.2.5 Calibration

Digital calibration of pipelined ADCs is used to boost converter performance above process limitations. These techniques correct problems such as capacitor mismatch, reference errors, and first order as well as higher order OpAmp gain errors. Foreground calibration corrects the errors during startup using some form of trimming or self-calibration, but are unable to track variations such as environmental changes during normal converter operation. Background calibration provides the ability for real time tracking and is accomplished with additional analog correction circuitry, queue-based timing, skip-and-fill interpolation, or correlation based methods.

A desirable form of calibration for high speed, medium resolution converters operating with low supplies is gain correction, correcting both OpAmp gain deficiencies and linear settling errors concurrently. [34] demonstrates the use of correlation-based gain calibration to correct the non-linear errors of an open loop amplifier to the third order, allowing the use of extremely simple and low power OpAmps. Other forms of calibration consequently correct first order OpAmp gain errors as well as DAC errors by

effectively analyzing the jumps in the static transfer curve. To do this, codes are forced in the MDAC or pseudo-random sequences are added to the signal or injected through the subADC. The algorithms then realign the curve by providing a gain compensation term in the digital domain during digital correction [25][30].

5 Design of a 1 V 10-bit 100 MS/s Pipelined ADC

This research proposes a fully differential version of ORST to circumvent the speed limitations of the published switched OpAmp and switched RC techniques, the shortcomings of the pseudo-differential ORST, and the potential reliability issues of bootstrapping. The technique improves on the previously published ORST technique [11] [12] by restoring fully differential balance to the circuit and addressing the issue of common-mode switching. It also includes a non-critical switch-RC network to aid the OpAmp with the reset. As a proof of concept, the fully differential ORST technique is implemented in the design of a low-voltage, high speed ADC that also includes the use of a simple, highly linear input track and reset circuit with an increased input range instead of a dedicated sample and hold.

5.1 Fully Differential ORST

The main motivations for using a fully differential form of ORST instead of the pseudo-differential form are the advantages of a fully differential input pair and moderate gain common-mode feedback loop for better suppression of distortion and improved rejection of disturbances from the supplies.

There are many similarities to the previous ORST implementation. First, the floating switch is removed from the front of the stage, allowing the previous stage OpAmp to perform the reset after supplying the residue. Second, it uses a dedicated feedback capacitor that is reset with a shorting switch. The amplifier common-mode must therefore be lowered to move the switch out of the dead zone so that it can conduct. Third, the MDAC references are injected through a set of separate DAC capacitors. This is similar to the first adaptation of ORST to a pipelined ADC [11], but not for the calibrated, algorithmic implementation [12] that uses a “half-reference” technique and requires a look-ahead scheme to determine the DAC values. Finally, the OpAmp is reset with a resistive network of CMOS switches as shown in Figure 28. First used in the algorithmic implementation, this allows the OpAmp to have similar loop bandwidth characteristics

during both phases, alleviating the stability requirements of the OpAmp because it does not need to be stable for unity gain feedback.

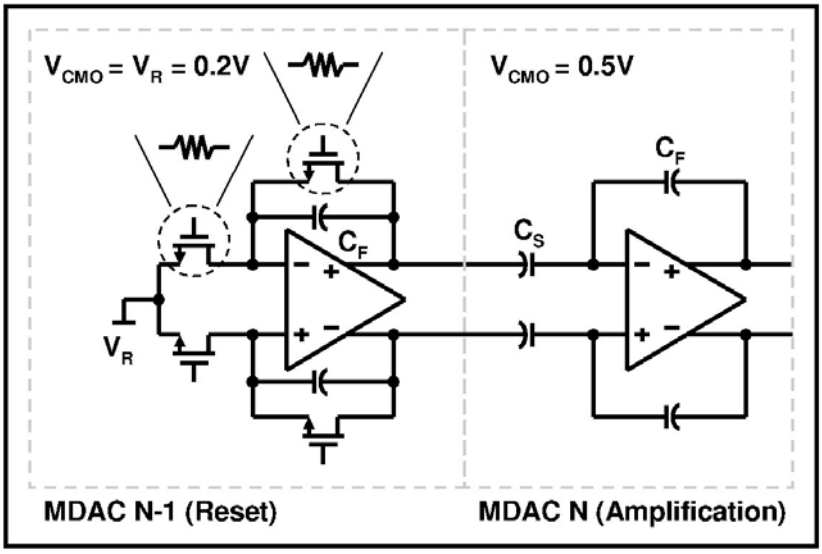


Figure 28: ORST uses resistive feedback during the reset phase to approximate the capacitive feedback during the amplification phase

The new, fully differential ORST implementation differs in the following ways. First, a traditional fully differential OpAmp is used instead of a pair of single ended OpAmps. Second, the common-mode switching is performed while still in differential mode, with a clocking mechanism built into the CMFB loop to switch the common-mode between phases. This loop has moderate gain for enhanced harmonic rejection while maintaining a desired bandwidth for switching speed. Third, the MDAC includes a single switched-RC network between the OpAmp output and the sampling capacitor to aid the OpAmp with the reset process. An MDAC schematic for a basic stage is shown in Figure 29.

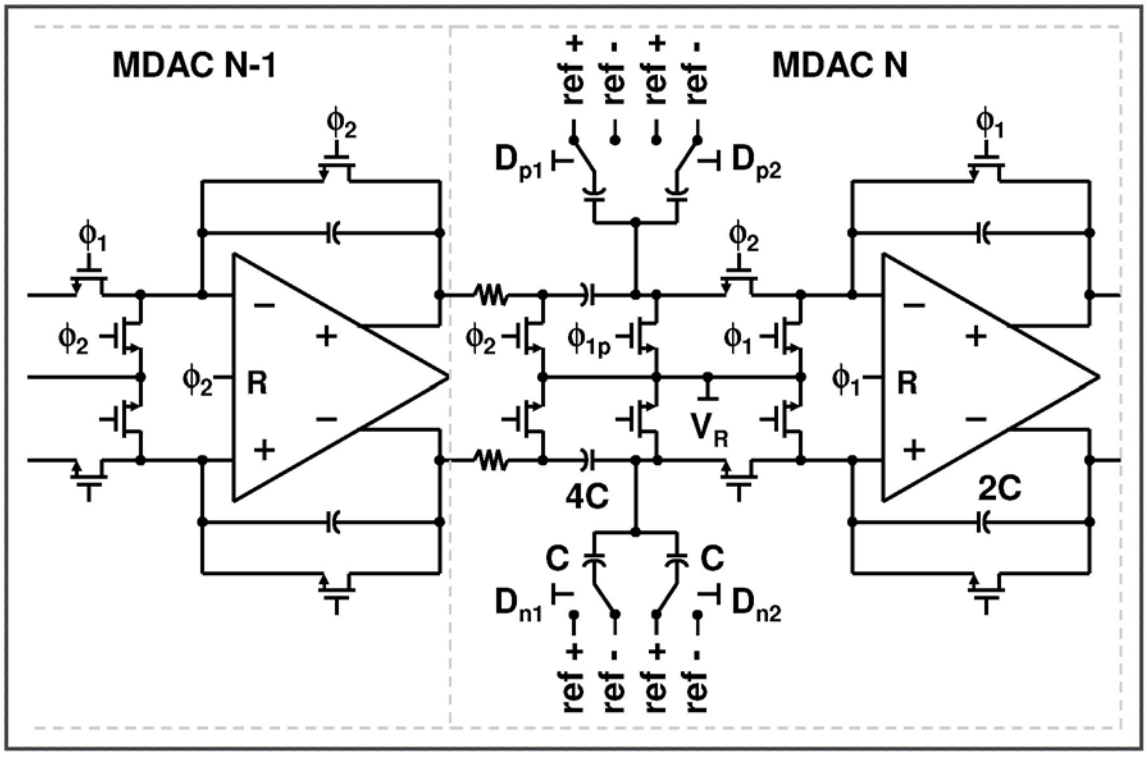


Figure 29: MDAC structure for the fully differential ORST

Critical nodes in the MDAC are designed to switch to the same DC bias during the reset phase. The resistive feedback, the OpAmp output common-mode level, and the switched-RC reset switch all use the same reference (V_R) of approximately 0.2 V, so there should be little DC current flow out of the OpAmp. This maintains the operational state of the OpAmp. Any current flow due to mismatches is not signal dependent as long as the OpAmp reset sufficiently settles in the allotted time, so it results in an input referred offset.

Using the switched-RC network in this way does not impose the speed limitation that it does if it is used as the primary resetting mechanism. It is added in this design to provide a small amount of attenuation (6-12 dB) of the OpAmp reset signal in the case of incomplete settling, but also to greatly reduce the noise (12-24 dB) that the resetting OpAmp adds to the residue.

Switching the common mode every phase causes a common mode shift error that must be considered. This is illustrated in the single ended simplification of Figure 30. The charge transfer onto feedback capacitor due to the CM shift at the input is matched partly by the shift at the output through the negative amplifier configuration, but the gain of two due to using a 1.5-bit stage tries to push the output further. The additional shift is rejected by the CMFB loop and is transferred to the input pair. Conveniently, the PMOS input pair with its high impedance current mirror easily rejects the shift and has no issue operating at a 0.1 V level as opposed to a 0.2 V level. Using the minimum stage resolution is advantageous in this respect as is seen by (19) which describes the input common-mode error caused by the input step with a stage gain of *G*. Using larger resolutions will create a larger step at the OpAmp input that must be corrected. A small error occurs for all stages except the first in this design, which has a gain of one due to the increased input range described in the next section.

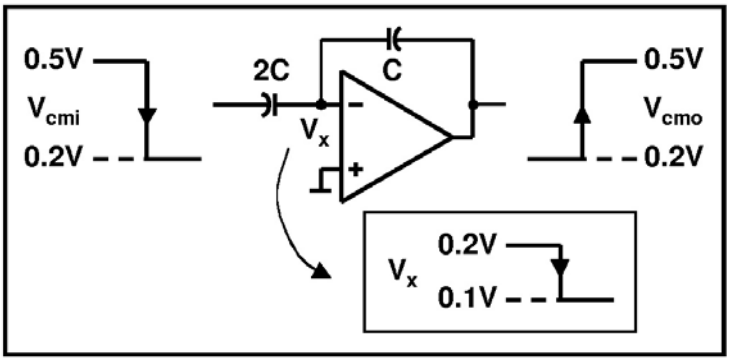


Figure 30: Common mode switching causes a shift at the OpAmp input pair

$$\Delta V_x \approx \frac{1-G}{1+G} \cdot \Delta V_{cmi} \tag{19}$$

To avoid the use of a switch that must conduct a mid-rail voltage, injecting the DAC references involves switching between a positive and negative reference level. This “double” reference injection is reduced to the proper level by decreasing the size of the

injection capacitor by two. The reference supplies can be set at 1 V and 0 V, but the resulting 8:1 capacitor spread raises capacitor matching concerns. Instead, the references are set at 0.75 V and 0.25 V for a 4:1 capacitor spread and no mid-rail references are required.

The first stage MDAC has a feedback factor of about 0.2, a loop unity gain bandwidth of 330 MHz, a loop gain of 72 dB, and requires 7 mW from a 1V supply at 100 MS/s in simulation.

5.2 Front-End T/R Network with Increased Input Range

Any active ADC sampling front-end such as a S/H must expend a significant amount of power to ensure that it does not limit the distortion or noise performance of the ADC, typically as much as or more than the power used in the first stage of a pipelined ADC. For this reason, it is desirable for the front-end to either be simple or optional. Opting to remove an input S/H altogether is attractive because it significantly reduces the power and improves the SNR performance but it requires attention to the resulting errors. This option is available for an ADC using the ORST, but another device is required to supply the reset for the first stage. In this design, a passive track and reset (T/R) is used for this purpose, and allows an increased input range.

5.2.1 Passive T/R

The input S/H is removed in this design and a passive T/R is used in its place to both reset the first stage sampling capacitors for proper operation of the ORST, as well as to provide isolation between the input source and the first stage MDAC during its amplification phase.

Shown in Figure 31 as a single ended simplification, the T/R is a cascade of networks composed of a series resistor and reset shunt switch, similar to a switched-RC block. The switches reset to the same V_R reference used by the ORST in the MDAC. During the track phase, the T/R reset switches are off, allowing the first stage to sample the input signal. During the reset phase, the reset switches turn on and reset the sampling capacitor as well as attenuate the input signal as it passes through the series of resistive voltage dividers. Using a larger number of cascades in the T/R gives more signal attenuation for a given total series resistance and switch area.

The use of such a device uses little additional power, adds no additional noise, provides kick-back isolation between the switches and the signal source, and is highly linear if designed properly because it is a passive circuit.

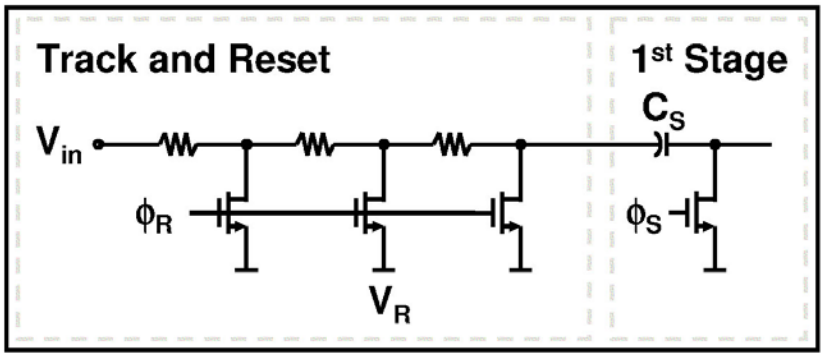


Figure 31: Front-end, passive, track and reset circuit

5.2.2 T/R Limitations and Tradeoffs

Though the T/R contains only passive elements, there are limitations and tradeoffs with its use. Specifically, the linearity of the device, the amount of resistive load on the source, the input bandwidth, and the required attenuation during reset present a complex set of tradeoffs.

These considerations determine the performance:

- Switch sizes must be small enough to prevent non-linearity.
- The resistive input load seen by the input source during reset must be large enough to not adversely affect the signal.
- The total series resistance must be small enough to recover from reset within the sampling time and allow the desired input bandwidth.
- Resistors and switches must be large to attenuate the input signal during the reset mode.

Linearity problems are caused by the non-linear drain capacitances of the reset switches in the T/R. As the switch sizes are increased to provide more attenuation of the input signal during reset, these parasitics become larger and foul the input signal. A graph of linearity versus input signal frequency for a test T/R is shown in Figure 32. Switching is not active during this test and an ideal S/H is used to capture samples so the poor

linearity is a direct result of the parasitic capacitance. This is also verified by disabling the parasitics at the drains of the transistors in the transistor models. The graph shows that linearity decreases for increasing input frequency until the -3 dB frequency of the T/R where the linearity increases due to reduction of the signal amplitude. For reasons described later in this section, a rail-to-rail input signal is used. It is found that a half scale range will yield much better linearity, suggesting that the use of the full scale range poses a design limitation for linearity. Using more cascades in the T/R helps to improve this by reducing the total switch area needed for the desired reset attenuation given a certain series resistance.

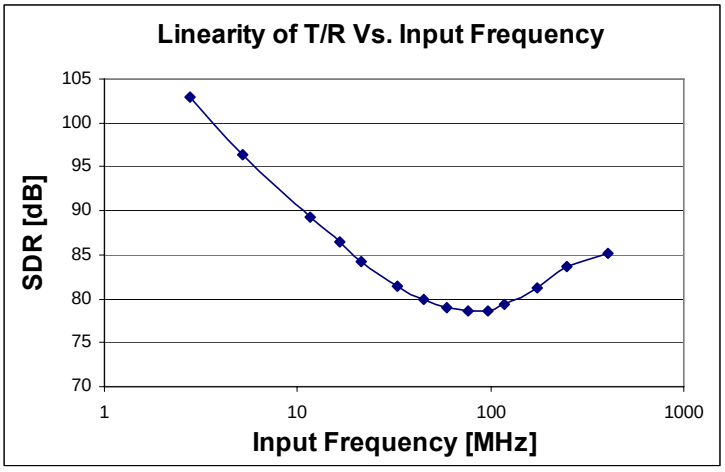


Figure 32: Linearity of T/R with full scale input

The T/R becomes a resistive load to the signal source during the reset mode and poses a lower limit on the size of the resistors used. The resistive loading only occurs when the input signal is not critical, but the source must be able to fully recover during the following phase.

Series resistance limits the input bandwidth of the ADC and prevents recovery from the reset phase, so a minimum amount is desired. The first case is signal frequency dependent attenuation whereas the second case is switching frequency dependent and can affect both the differential and common-mode signal. Placing the RC bandwidth greater than the desired clocking frequency of operation allows the common-mode to transition

at least 95% of the step response, attenuates the differential signal by less than 0.5 dB due to settling for all frequencies, and gives a frequency bandwidth greater than twice the Nyquist frequency.

Attenuating the input signal during the reset phase prevents the signal from propagating through the MDAC to the output residue of the first stage. The remaining small signal resulting from incomplete attenuation adds linearly with the residue output of the first stage because it is a time-advanced representation of the input, but is only allowed in a small amount. By input referring this small signal, the result is a slight shaping over the passband at the input of the ADC and a small modulation of the comparator thresholds which is correctable with redundancy. As long as the small signal is within the redundancy range, no errors will result. A caveat to this is the non-linearity of the small reset signal caused by the signal dependence of the shunt switch resistance. The signal is still large in the first cascade of the T/R, causing a modulation of the drain node and therefore the switch's on resistance. The resulting non-linearity of the attenuated signal adds directly to the residue, but only after the remaining cascades attenuate the signal further, so this source of error is not a concern in this design.

5.2.3 Increased Input Range

The inter-stage signal swing of the pipeline is limited by the output swing of the OpAmps, but the input signal swing is only limited by the specifics of the input sampling device. The passive T/R circuit allows an increased signal swing in this design due to the lack of a floating switch as shown in Figure 33. Increasing the input range can lead to performance benefits such as increased SNR and increased feedback factor due to the necessary reduction of gain in the first stage. The increased input range is proposed also in [35] and implemented in [43].

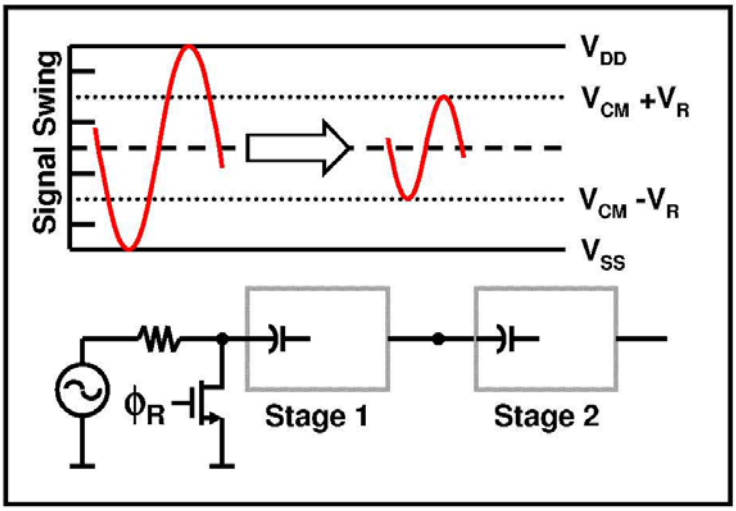


Figure 33: The passive T/R allows an input range that is double that of the stage to stage OpAmp signal swing

Possible increase in the SNR is due to the relative contribution of the input sampling capacitor kT/C noise to the signal swing at the input. If the swing is increased while the capacitor size stays the same, then the SNR increases. Though, due to a necessary reduction in the gain of the first stage to ensure that the residue is within the output swing of the OpAmp, all noise added to the signal aside from the first stage kT/C sampling noise is unaffected by the increase in the input range. This includes jitter on the sampling switch of the input stage which increases by the same amount that the signal increases. Therefore the increased input range can either yield an increase in the SNR or the reduction of the input sampling capacitance for equivalent SNR.

Considering only the first thee stages of the pipeline, the SNR increase benefit can be approximately calculated from (20) where x is the input range scaling factor (>1), α is the capacitor scaling factor (<1), G is the stage gain, and ρ is the fraction of kT/C noise in the total noise budget. If kT/C noise accounts for 20% of the noise budget, then a design with 1.5-bit stages and a 1.5x capacitance scaling factor can reduce the kT/C noise power by 49% and increase the SNR approximately 0.46 dB by doubling the input signal range. Higher resolution designs of 14 to 16 bits with large stage resolutions benefit the most

from a doubled input range, by as much as 3 dB practically, because kT/C noise typically dominates the noise budget instead of quantization noise. Unfortunately, designs with greater scaling factors relative to the stage gain yield less of an SNR increase due to the increased contribution of kT/C noise from later stages.

$$\Delta_{SNR}[dB] \cong 10\log\left(1-\rho+\frac{\frac{1}{x^2}+\frac{1}{\alpha\cdot G_1^2}+\frac{1}{\alpha^2\cdot G_2^4}}{1+\frac{1}{\alpha\cdot G_1^2}+\frac{1}{\alpha^2\cdot G_2^4}}\cdot\rho\right) \tag{20}$$

For this design, the increased range does not make a significant difference (~0.2 dB improvement) but is used for the following reasons. It allows reduction of the first stage sampling capacitance to relax the requirements of the T/R described earlier, reduces gain in the first stage to correct the common mode shift error, and increases the feedback factor for reduced noise.

With the extended input range, a larger reference must be subtracted in the residue, posing a possible problem with stage to stage variations of the reference voltage. This problem is addressed by scaling the reference from the first to second stage by controlling the capacitance ratio of the DAC capacitors to the feedback capacitors in the MDAC. The input range is increased by two in this design, so the reference scaling is ensured as long as capacitor matching is accurate enough and therefore no calibration of the references is needed.

5.2.4 Operating without a S/H

The power savings that can be achieved for a pipelined ADC operating without a front-end S/H is significant. Not only does it avoid the power use which can be comparable to the entire power used in the rest of the ADC, but it also relaxes capacitor size requirements because there is no longer kT/C noise added by the S/H sampling capacitors. At least half the power can therefore be avoided without a S/H. The tradeoff is compensation for the loss of the S/H.

Using a front-end S/H allows the first stage MDAC and subADC to sample a DC signal. When no S/H is used, the varying input signal can cause an error between the samples captured by the MDAC and subADC. This leads to design and layout efforts to match the sampling delays of the two paths. [32] accomplishes this by matching the RC sampling bandwidth of the MDAC to the comparator preamp bandwidth, whereas other approaches use the more feasible approach of modifiying the structure and timing of the subADC by creating a scaled replica of the sampling network that mimics the MDAC at the sampling instant. The latter approach requires either a reduction of the available sampling [20] or settling time [7].

Any MDAC and subADC path mismatches effectively result as offsets in the subADC and are correctable with digital redundancy. The errors can be due to bandwidth mismatches, clock routing mismatches, or latching delay errors. In this design, the large redundancy range of the 1.5-bit stage affords no special compensation techniques for the path mismatch errors.

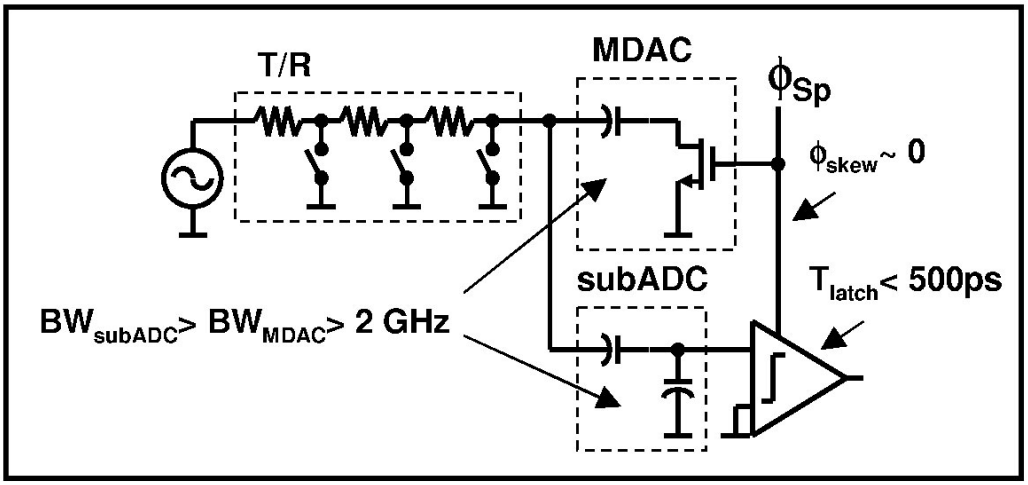


Figure 34: Removing the S/H requires careful attention to path mismatch errors between the MDAC and subADC of the first stage

To eliminate any delay caused by the series resistance of the T/R, the subADC input is tapped from the top plate of the MDAC input sampling capacitor just passed the

T/R as shown in Figure 34. Therefore, the RC bandwidths of the signal paths that need to be matched are large enough such that bandwidth errors are insignificant. The MDAC bandwidth in this case is above 2 GHz and requires less than 10% (17.6 mV) of the redundancy range to correct the resulting phase error for a Nyquist rate signal. The latching time of the dynamic latch in the subADC contributes the most error, though it is found in simulation that the amount of time required for the latch to enter strong regeneration is less than 500ps for large swing, Nyquist rate signals so it requires less than 65% of the redundancy range. Clock routing skew is negligible due to the proximity of the MDAC switches and latches in the layout, therefore the path mismatches in this design are completely correctable by the redundancy range for large Nyquist rate signals.

5.2.5 Design Implementation

The T/R in this design uses a cascade of three reset networks, each with 650 ohm series resistors and 20 um / 0.18 um shunt switches, equivalent to 140 ohms at the slow corner. This allows an input bandwidth of greater than 150 MHz with approximate parasitics, linearity greater than 75 dB, and input signal attenuation of 47 dB during the reset while using less than 2% of the 1^{st} stage redundancy range. The resulting ripple in the bandwidth is less than 0.1 dB.

5.3 Low Voltage OpAmp

The low transistor output impedance resulting from small drain to source voltages and large currents severely limits the gain of a high speed, low voltage OpAmp. Gain boosting is chosen to meet the desired >70 dB loop gain requirement for this design. Figure 35 shows a schematic of the OpAmp illustrating the gain boosting, cascode compensation, and a differential common-mode feedback technique.

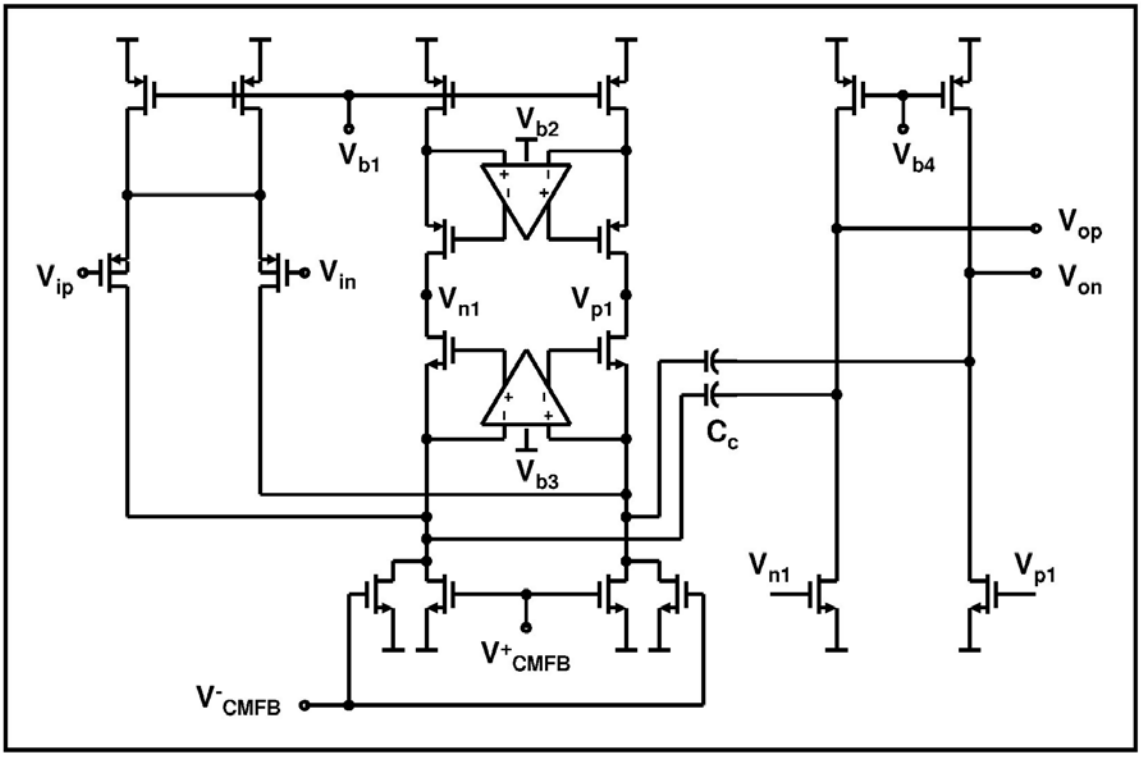


Figure 35: Low voltage OpAmp with cascode compensation and gain boosting

5.3.1 Gain Boosting

Gain boosting inherently introduces a pole/zero doublet in the open loop transfer function that can slow the overall response of the circuit if placed at a low frequency [24], so the UGBW of the gain boosting loop must be properly chosen [9]. A slow

booster response can also result in overshoot in the overall step response caused by the differential glitch at the virtual ground of the OpAmp. The UGBW of the boosting loop is therefore placed greater than the overall open-loop UGBW but sufficiently below parasitic poles in the signal path to avoid instability as shown in Figure 36. In the case of the folded cascode, the folded node presents a significant parasitic pole that appears in the booster loop.

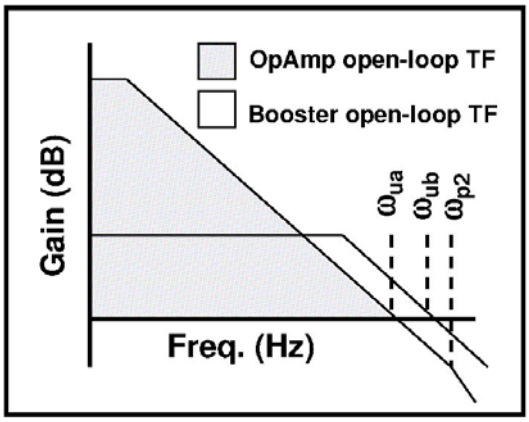


Figure 36: Proper gain booster design places the booster loop UGBW (ω_{ub}) between the OpAmp UGBW (ω_{ua}) and the next parasitic pole (ω_{p2}) in the loop [9]

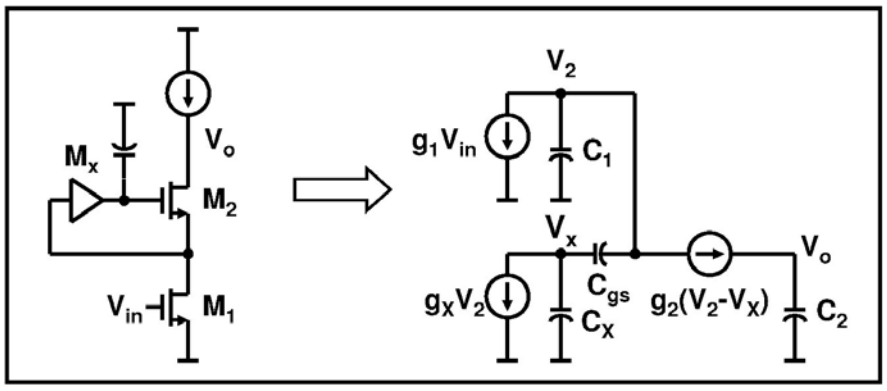


Figure 37: Small-signal model of a generalized gain boosting circuit

$$\frac{V_o}{V_{in}} = -\frac{g_1}{sC_2} \cdot \frac{s\frac{C_x}{g_x} + 1}{s^2 \frac{C_1(C_x + C_{gs}) + C_x C_{gs}}{g_x g_2} + s\left(\frac{C_x}{g_x} + \frac{C_{gs}}{g_2}\right) + 1} \tag{21}$$

Taking a simplified analysis approach by ignoring output impedances, one can derive (9) from the small signal model in Figure 37. From this equation it is shown that the doublet is associated with the shunt capacitance C_x at the gate of the cascode device and that the cascode node parasitic C_1 has a strong effect on spreading the pole/zero, preventing cancellation of the doublet. C_{gs} of the cascode device, often associated with a RHP zero in a common source amplifier due to the feed-forward coupling, modifies the poles and contributes to the zero of the doublet when output impedances are taken into consideration [18]. The suggested design methodology pushes the doublet to higher frequencies by increasing the speed of the booster until the pole of the doublet meets the parasitic pole. Each boosting amplifier must also be chosen carefully to take additional poles into account such as with the boosting structures in [38] and [16] that introduce mirroring poles.

Noise from the gain boosting amplifiers must also be considered. The boosting amplifiers have a gain of $\sim g_m/g_{ds}$ from the cascaded device gate to the output of the stage and larger bandwidth than the overall amplifier with smaller transistor sizes, so the additional thermal and flicker noise is not ignorable. These noise sources can be very significant if small, complicated, single ended boosters are used.

Simple cascoded, common-source boosting amplifiers [9] are incompatible with low voltage designs because they require the cascode node to be biased at $|V_t+V_{od}|$ from the supply which can be near mid-rail. This design uses two fully differential, single stage, folded cascode gain boosters to maximize cascode headroom, minimize the added noise, and to avoid mirroring poles in the booster loops and hence only the differential gain is boosted. The N-cascode booster is shown in Figure 38. A PMOS input pair is used to boost the N-cascode and vice-versa. Additional source followers and a replica amplifier are used for common-mode feedback.

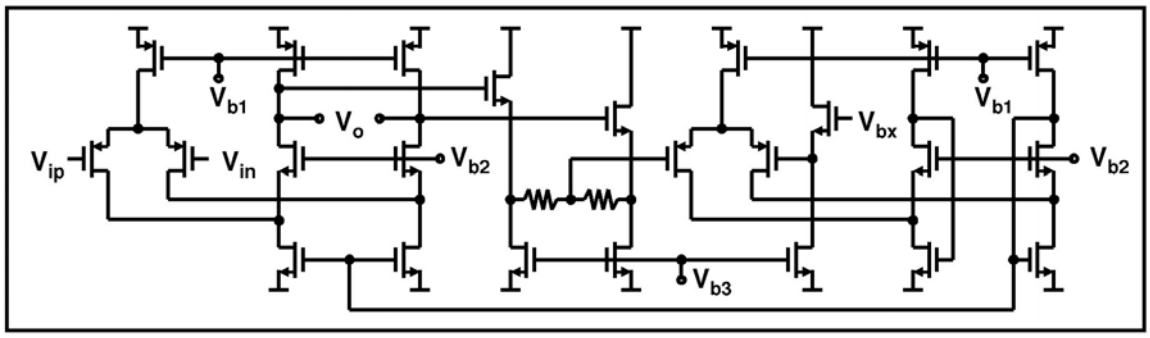


Figure 38: N-cascode booster amplifier with common-mode feedback

5.3.2 Cascode Compensation

Cascode compensation, proposed in [36], with an earlier idea credited to [6], is used to take advantage of its increased bandwidth and improved PSRR while suppressing the feed-forward path to the output. This technique provides compensation without the adverse effect of the right half plane zero suffered by Miller compensation and is characterized by the small-signal model of Figure 39 and transfer function (22). Though this technique does not provide analytical expressions for individual pole placement in terms of circuit properties, a basic design methodology is available [3] that can be used with Matlab to verify the desired response. Careful attention is paid to the transconductance of the cascode transistor. Inadequate g_{m2} leads to the influence of an ill-desired complex pole pair even when the system is overcompensated, leading to strange transient settling responses, whereas proper design ensures enough g_{m2} to push the complex pair to higher frequencies.

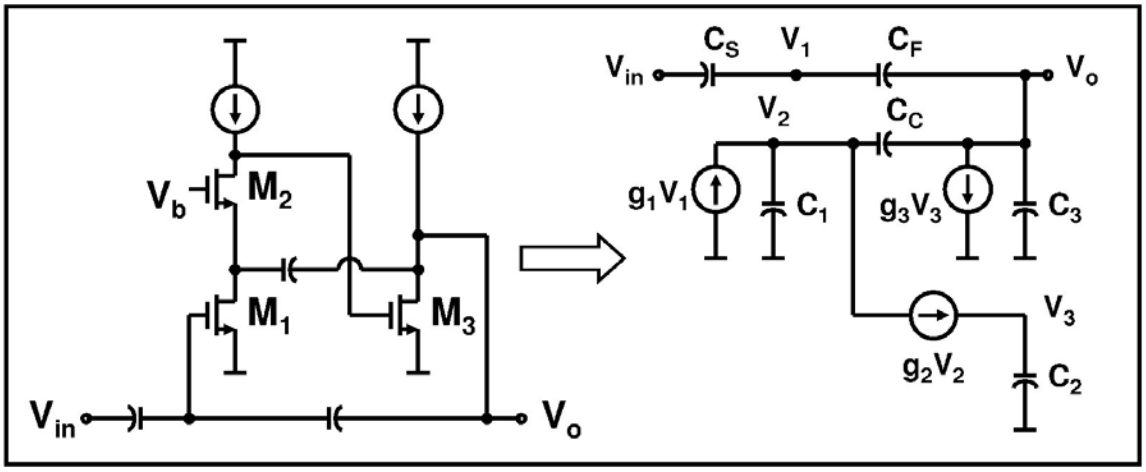


Figure 39: Small-signal model of a cascode compensated amplifier in capacitive feedback

$$\frac{V_o}{V_{in}} = -\frac{1-\beta}{\beta}\cdot\frac{1-s^2\frac{C_2}{g_3}\left(\frac{C_f}{g_1}+\frac{C_c}{g_2}\right)-s^3\frac{C_2C_fC_{L1}}{g_1g_2g_3}}{1+s\frac{C_c}{\beta g_1}+s^2\frac{C_2}{g_3}\left(\frac{C_{L2}}{\beta g_1}-\frac{C_c}{g_2}\right)+s^3\frac{C_2\left(C_cC_3+C_cC_\beta+C_1C_{L2}\right)}{\beta g_1g_2g_3}} \tag{22}$$

$$C_\beta = \frac{C_sC_f}{C_s+C_f} = \beta C_s$$
$$C_{L1} = C_c + C_1$$
$$C_{L2} = C_c + C_\beta + C_3$$

5.3.3 Common Mode Feedback and Loop Stabilization

Fully differential ORST requires a CMFB that switches between a mid-rail and low voltage level on different phases. The settling accuracy requirements are not as stringent as the differential settling, but it must be fast and stable enough to allow the differential mode to settle linearly with a mid-rail common mode. Switched capacitor CMFB might be better suited for this purpose but is not used to avoid floating switches. This design chooses a continuous time CMFB with a switching, resistive level shifter and a common-mode comparison amplifier as shown in Figure 40.

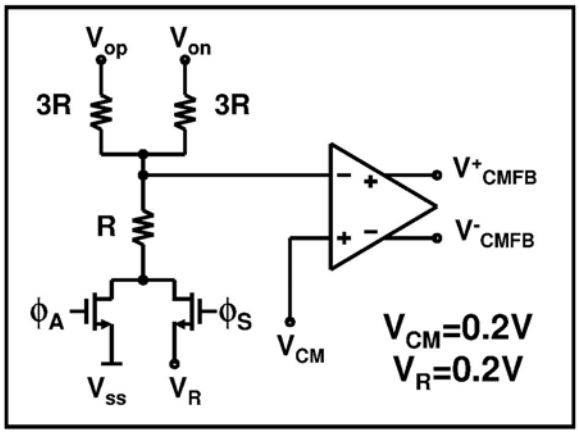


Figure 40: Continuous CMFB with common-mode switch for the ORST

The level shifter performs two duties. First, it reduces the level of the detected OpAmp output common mode to within the allowable range of the PMOS input pair. Second, by switching the tail resistor between ground and a reference supply of 0.2 V, the OpAmp output common-mode switches between 0.5 V and 0.2 V based on the ratio of the level shifting resistors. This method of common-mode switching allows similar CMFB loop characteristics during both phases to maintain a stable switching transient. The CM comparison amplifier compares the shifted common-mode level to a reference and controls the NMOS current sources in first stage of the main OpAmp.

The shifter and comparison amplifier add two poles to the two poles of the main OpAmp to make the CMFB loop a four pole system. These two added poles are due to the RC and g_m/C constants at the input and output of the comparison amplifier respectively. Their frequencies are inversely related by the size of the comparison amplifier such that a large size creates a low frequency RC pole and a high frequency g_m/C pole, so the optimal size places the poles at the same frequency. To make this frequency as high as possible, the level shifting resistors are reduced as far as possible while maintaining adequate amplifier gain, and minimum channel lengths are used for all transistors in the signal path.

To further stabilize the four pole system, the gain of the CMFB loop gain is reduced at the expense of reduced speed. The bandwidth need only be comparable to the

clocking frequency to settle the transient to a couple tens of millivolts so the speed reduction is allowed. Gain reduction compensation can be done in CMFB loops by splitting the transistor in the main amplifier that controls the common-mode and connecting one part to a DC bias. Due to the difficulties of current matching with sub-micron transistors, the comparison amp in the CMFB loop uses the same structure of the OpAmp first stage and both of its terminals are used to provide the gain reduction instead of using an extra replica bias that can introduce additional offset. Figure 41 shows how a small amount of positive feedback is used to partially cancel the negative feedback of the CMFB loop, thereby reducing the gain. The amount of gain reduction is determined by how the tail transistor is split and is easily done in layout using multiple device fingers.

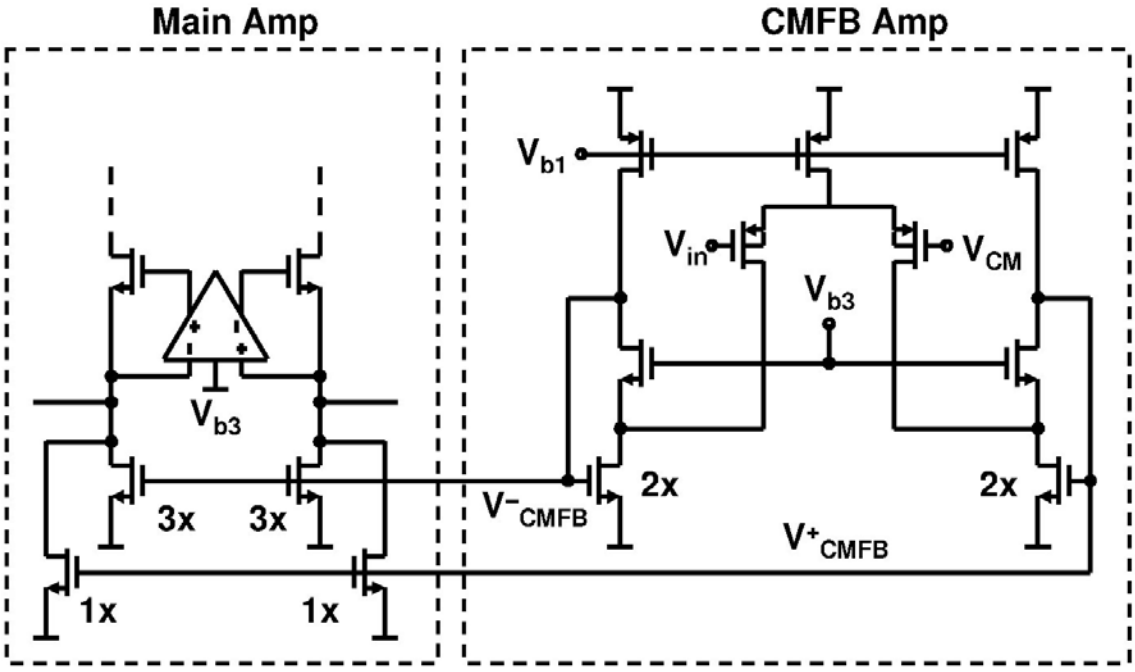


Figure 41: Differential CMFB is used to introduce a mild positive feedback for loop stabilization

5.4 SubADC Design with Dynamic Latch

The reference network of the subADC, shown in Figure 42, is reset during the amplification phase when the input signal is reset with the ORST. The reference is then injected during the sampling phase while another set of capacitors tracks the input. Near the end of the sampling phase, the latch is triggered by the early clock at the same time MDAC samples. To avoid using references near the mid-rail, a simplified scheme using only one low voltage reference (V_{rb}) of 0.125 V is used. Instead of switching from a mid-rail level to the reference, the capacitor bottom plate switches between ground and reference for one side of the differential circuit and from reference to ground for the other side. Switching from a high level to a low level is not preferable because it requires large signal coupling capacitors in the subADC that load the previous stage OpAmps. This is not a true fully differential operation, but with the large redundancy range offered by the 1.5-bit stage, the offset accuracy of the subADC and its comparators are relaxed. V_{rb} is supplied from off chip in this design but can be easily generated with a resistor string.

A dynamic latch is used to make the comparator decision. This makes the subADC simple, compact, and power efficient. During the sampling phase the latch is reset with the current source M1 turned off and the M4 switches grounding the outputs. When the latching clock falls, the reset switches turn off and the current source turns on to flood the output nodes with charge. As the common-mode level of the output reaches the turn on threshold of the M5 cross-coupled pair, the positive feedback amplifies the charge imbalance at the output nodes caused by the signal on the differential pair and regenerates the outputs to opposite supply rails. Cross-coupled M3 provides additional regeneration strength and impedes current flow after the decision is made. Buffer loading as well as parasitic capacitances at the latch outputs are minimized for faster latching decisions.

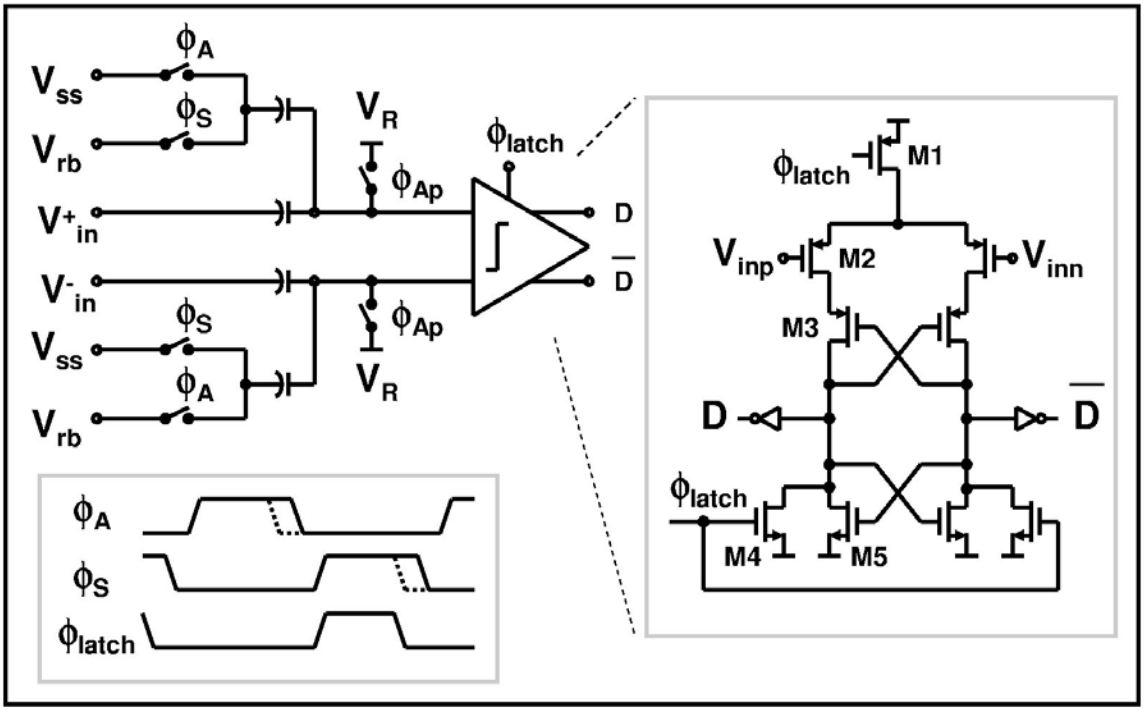


Figure 42: Structure and timing of the subADC and dynamic latch

5.5 Pipelined ADC Architecture

The pipelined ADC architecture contains eight stages, a front-end T/R, and a final 2-bit flash with standard thresholds as shown in Figure 43. All eight stages implement the fully differential ORST technique with the T/R providing the reset for the first stage and have 1.5-bit resolution to maximize speed and redundancy range.

The first stage has 300 fF input sampling capacitance, reduced from 600 fF due to the increased input range, while the sampling capacitances of the following stages scale by about 1.5x until the fifth stage capacitance of 200 fF. Operating in simulation at 100 MS/s, the analog core plus digital correction and output buffers are estimated to consume 36 mW and 3 mW respectively from a 1 V supply.

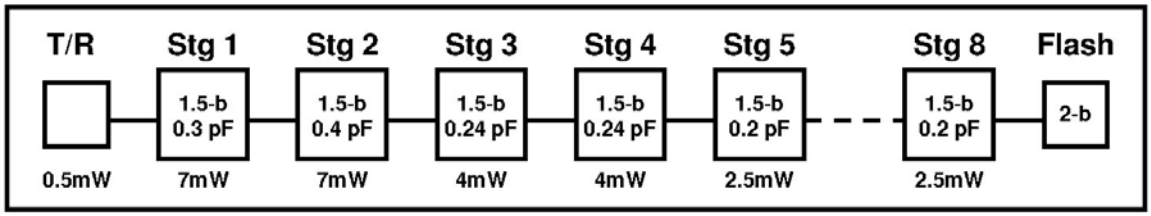


Figure 43: Pipelined ADC architecture including power consumption and sampling capacitor values

The kT/C noise is calculated with (23), accounting for 28% of the noise budget for a 59dB SNR. The front factor of 2 accounts for both sides of the differential structure, the factor of 2 in each term includes the kT/C noise on the feedback capacitor at the end of the sampling phase, and the final 1.5 factor accounts for the OpAmp filtered switch resistance noise. The squared gain factor in the first term is the advantage of using the extended input range.

$$\overline{v_{nSi}^2} = 2\left(2\frac{kT}{300f}\cdot\frac{1}{2^2} + 2\frac{kT}{400f}\cdot\frac{1}{2^2} + 2\frac{kT}{240f}\cdot\frac{1}{2^4} + 2\frac{kT}{240f}\cdot\frac{1}{2^6}\right)\cdot 1.5 = 44.3nV^2 \qquad (23)$$

The pipelined ADC is simulated with the SpectreRF periodic noise analysis to calculate the total OpAmp and kT/C noise performance and is limited to 55 dB SNR due mostly to OpAmp noise. Nearly 50% of the simulated noise power comes from transistors in the gain boosters.

5.6 Layout

5.6.1 Floor Plan

The pipeline core is laid out linearly across the die with the MSB (stg1) at the left and final flash stage (flash) at the right as shown in Figure 44. All stages have equal height to align the reference and supply distribution across the core but scales down in width as the capacitor array size reduces.

Four clock generators are positioned above the stages to supply the non-overlapping clocks. Each generator drives two adjacent stages such that the first generator (clk1) drives stages one and two. The last generator also controls the final flash stage.

The time aligning registers, digital correction logic (digcor) and digital output buffers (buff) are positioned above the LSB stages to minimize the effect of the substrate noise on the MSB stages. These blocks, as well as the clock generators, are surrounded by a continuous, grounded p-well to increase substrate resistivity between the analog and digital circuits. Substrate ties are placed on either side of the well, but are connected together outside of the chip to make a division between analog and digital substrates.

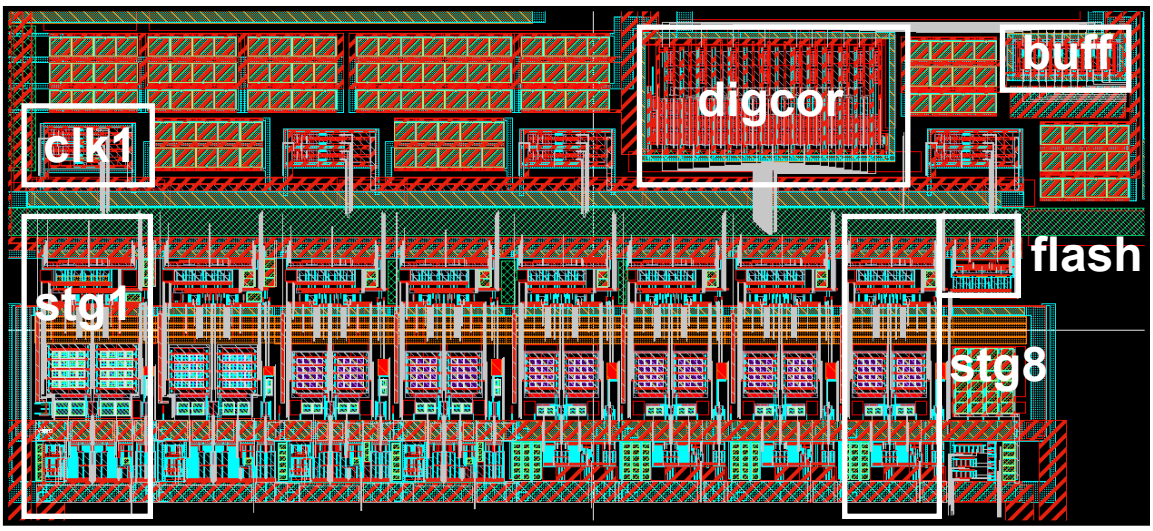


Figure 44: Floor plan of the pipelined ADC

Each stage is arranged vertically with the subADC at the top, followed by MDAC switches, references lines, the capacitor array, and then the OpAmp as shown in Figure 45. The stage input enters from the left below the capacitor array where it meets the T/R or switched-RC network and the output leaves the stage on the right side at the same height.

The pipelined ADC itself is 1.8 mm x 0.8 mm but the padring is 3 mm x 2 mm as shown in Figure 46. The remaining room is filled with supply and reference bypass capacitance as well as dummy filler to meet density requirements. The die photo is shown in Figure 47.

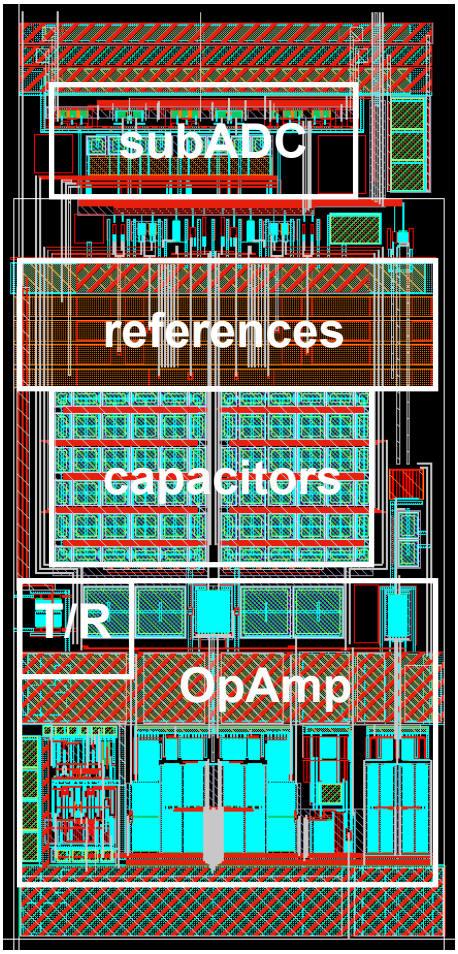


Figure 45: Stage floor plan

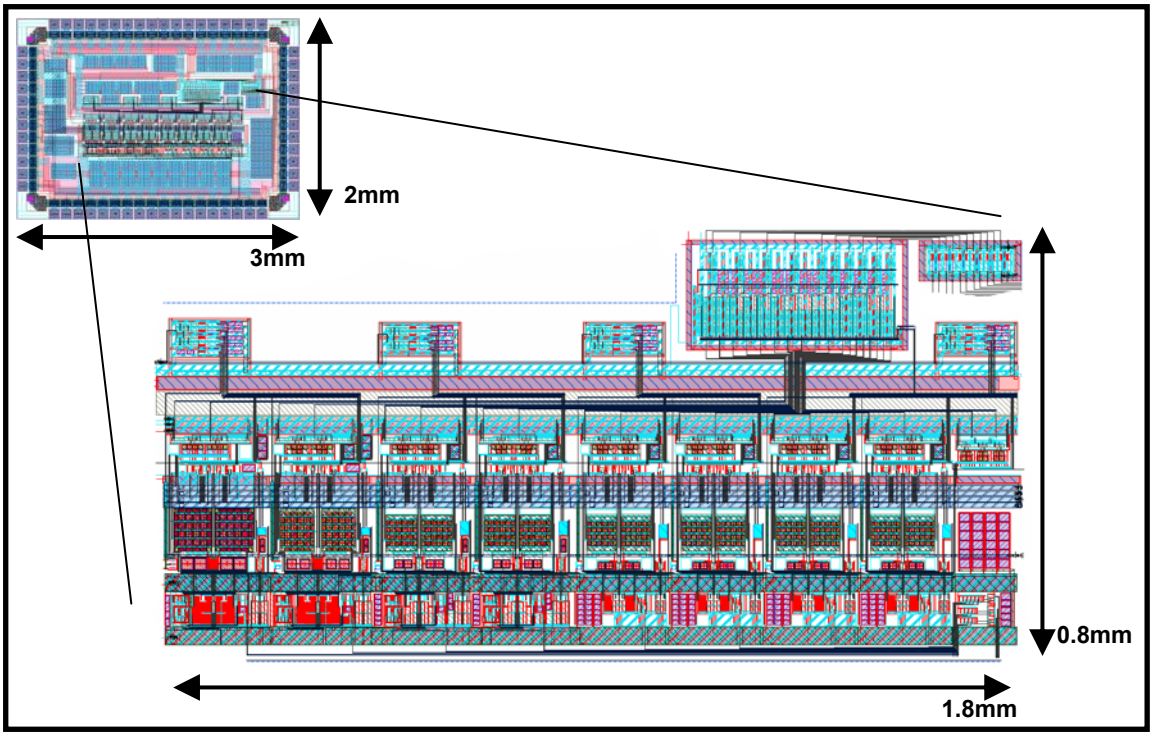


Figure 46: Full layout and dimensions

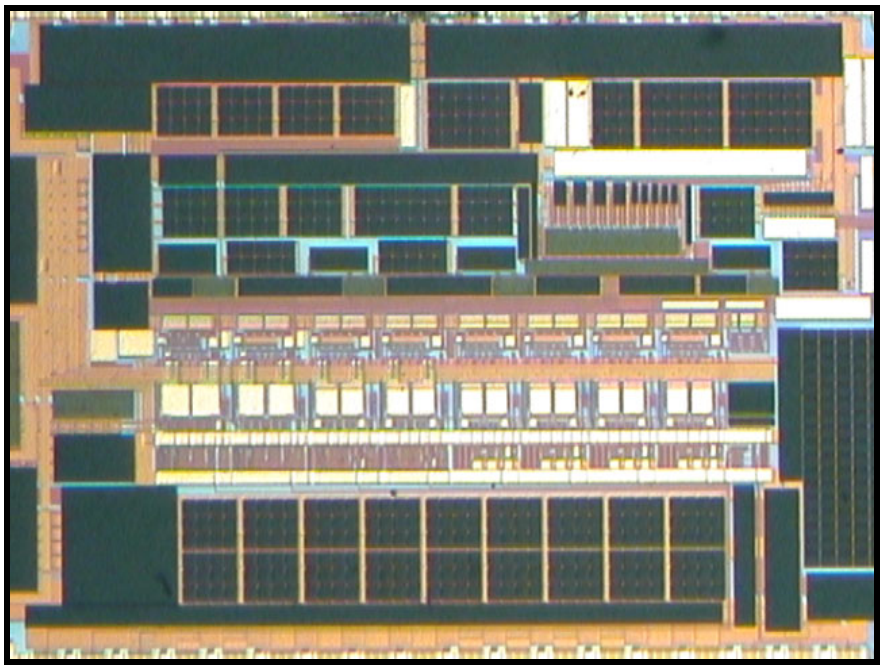


Figure 47: Die photograph

5.6.2 Capacitor Arrays

Capacitor arrays are placed just above the stage OpAmp but below the reference lines. They are arranged in a 4x4 common-centroid layout with reduced size dummy capacitors around the outside. Figure 48 shows the array of the first stage where the feedback (F) and sampling (S) capacitors are arranged in the outer unit ring and the positive (Rp) and negative (Rn) DAC reference capacitors are placed in the center units. From the second stage and on, the corner units are part of the sampling capacitor. Vertically adjacent capacitors share the same routing path such that bottom plates route together to the outside of the stage and top plates route together to the inside where they connect to the virtual ground nodes. This minimizes coupling between top and bottom plates to prevent capacitor matching errors.

The poly-poly caps also have cut corners, symmetric contact connectors, and a solid grounding plate above the entire array to improve matching.

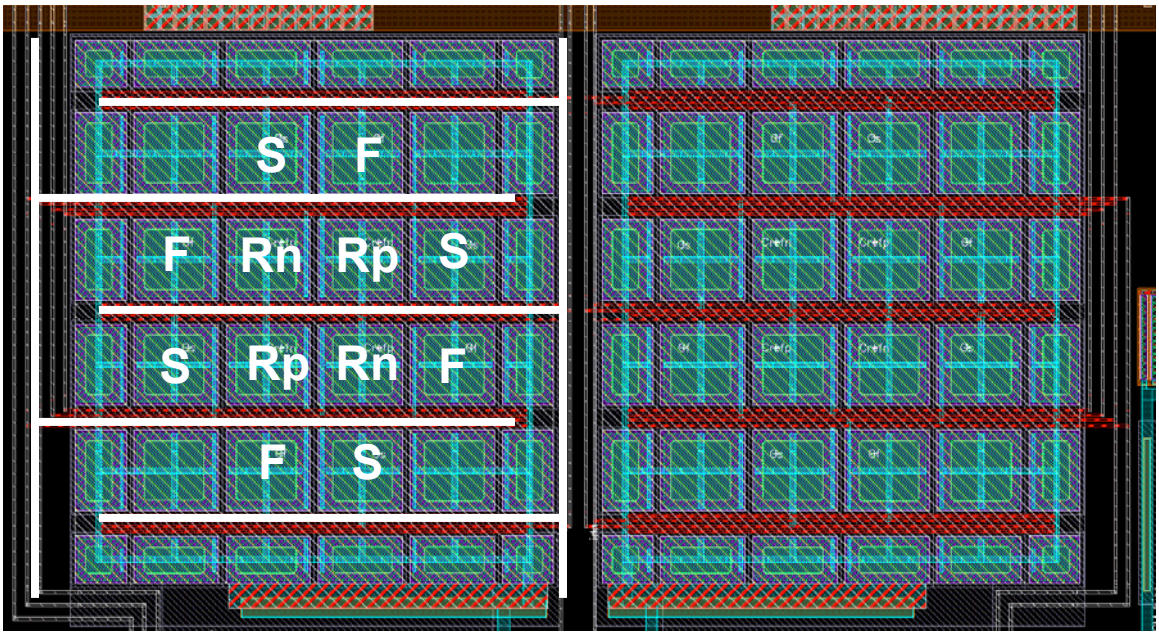


Figure 48: Common-centroid layout of the capacitor arrays

5.6.3 Clock Distribution

The input clock (clkref) is routed on the top metal layer above a grounded shield from the top of the die between the first and second clock generators and then split in a ‘T’ to traverse the width of the core. Shown in Figure 49, this routing minimizes the delay between the first two clock generators. Each generator drives two stages.

Non-overlapping clocks are routed from the generator above a grounded p-well to prevent coupling to the substrate, into the top right of the stage, and then across the stage between the subADC and MDAC switches to avoid crossing the analog reference lines supplied to the comparators that travel up the left side of the stage.

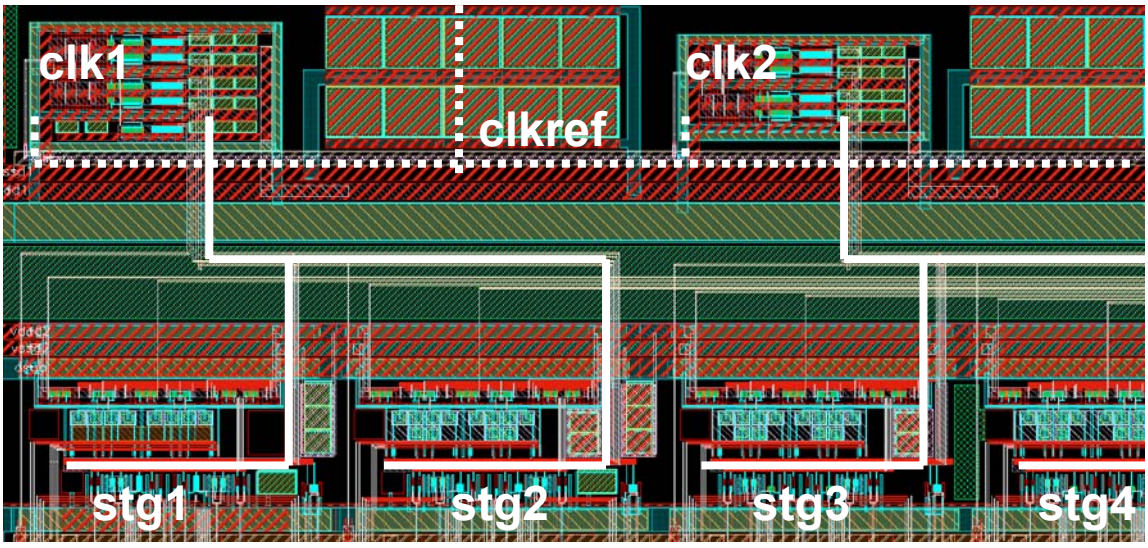


Figure 49: Clock distribution of the four MSB stages

5.6.4 OpAmp

The OpAmp, shown in Figure 50, is laid out in block segments at the bottom of each pipeline stage between the positive and negative (vss) supply rails. The first and second stage of the main amplifier (opamp) are placed together in the middle of the layout, with the n- (nbst) and p- (pbst) booster amplifiers placed to the left and the bias (bias) and common-mode feedback (cmfb) circuits placed to the right. The input pairs of the main amp and CMFB amp are brought above the negative rail to prevent coupling of the supply to the high impedance virtual ground. Conveniently, this allows the compensation capacitors (comp) to also lie above the supply rail.

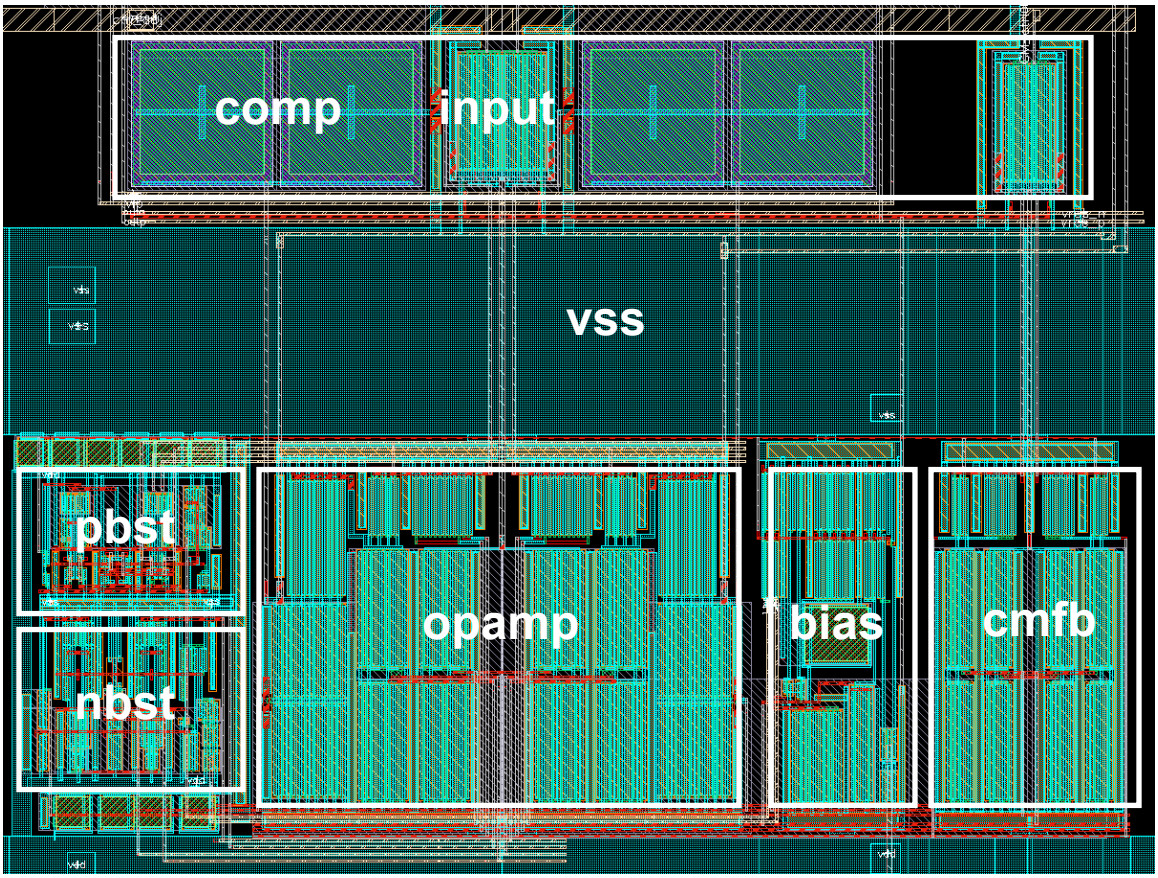


Figure 50: OpAmp layout

Drawing about 35 mA of current, the large voltage supply lines that traverse the pipeline are 36 um wide in a five metal stack with breaks in one layer to allow signal routing. The OpAmp supply rails are dropped down from the main supply rails and form a ‘T’ junction at the symmetry point to provide better fully differential operation.

Bias, CMFB, and booster lines are routed above and below the main amplifier to prevent coupling of the common-mode switching transients. The OpAmp output runs across the stage just below the input pairs. An additional pair of OpAmp output lines is also routed from the OpAmp output stage to the common-mode detecting resistors above the CMFB block, though not shown in the figure, to prevent a gain error at the input to the next stage due to the DC current flow.

The CMFB circuitry stretches the whole height of the MDAC from the switches that are aligned with the MDAC switches to the resistive common-mode level shifter along side the capacitor array and down to the input pair of the comparison amplifier. This is seen more easily on the right side of the stage in Figure 45.

5.7 Testing and Measured Results

5.7.1 Test Setup

The setup for testing the ADC is shown in Figure 51. Two different input signal generators are used to measure the performance. A low frequency differential signal generator is used to measure static linearity and low frequency functionality, whereas an RF generator supplies higher frequencies with the assistance of a 400kHz-800MHz balun on the PCB (Minicircuits ADT1-1WT). Bandpass filters are also used to improve the spectral purity of the input from around 50 dB to above 69 dB SFDR.

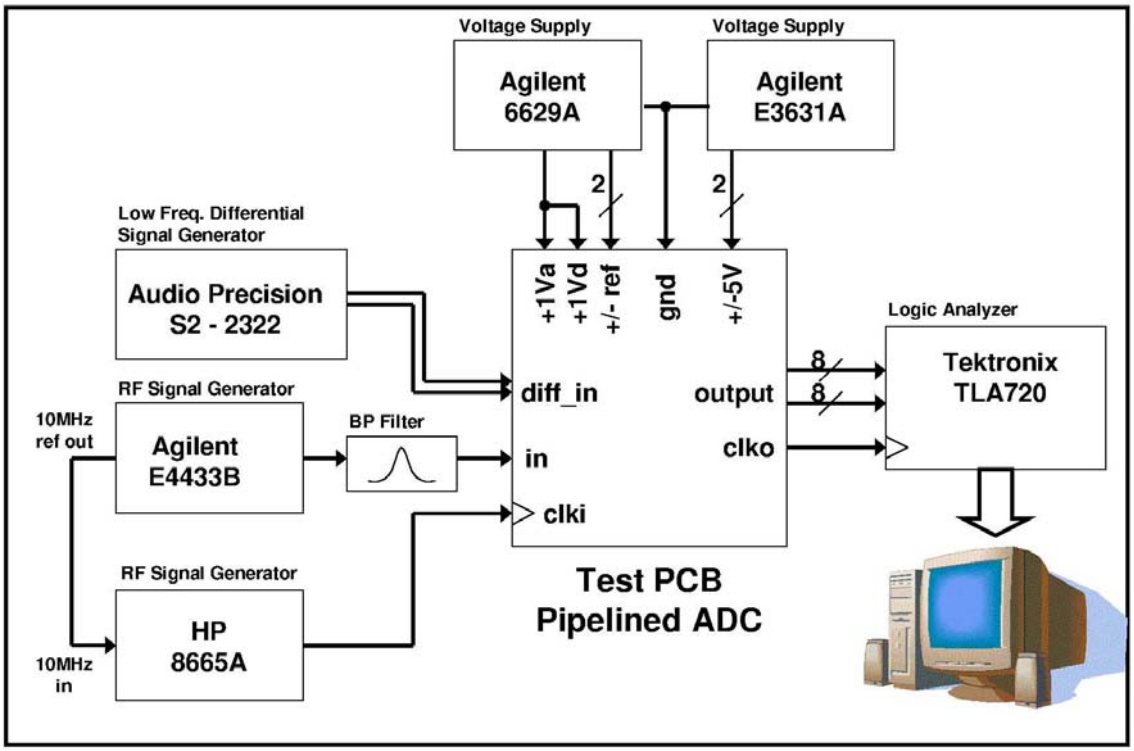


Figure 51: Setup for testing the pipelined ADC

An additional RF generator supplies the input clock for lower jitter performance. A 10 MHz reference supplied by the signal RF generator is connected to the clock generator to establish signal coherence between the signal input and the clock.

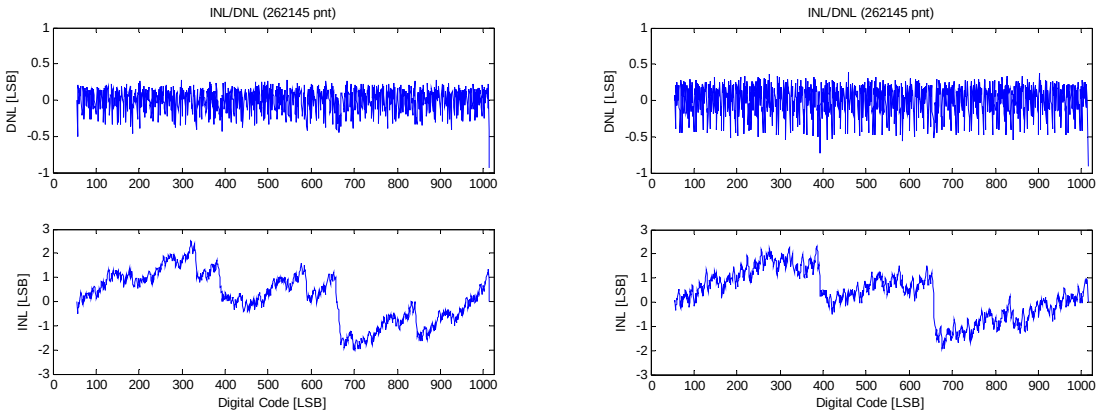
The logic analyzer collects the unbuffered, 1 V digital output data from the chip through two, 8-bit ports triggered with a synchronizing clock from the chip. The data rate from the ADC is decimated by 4 on-chip to reduce the substrate noise and to relax the speed requirements of the output buffers so they can drive the load of the logic analyzer probes.

Two separate voltage supply generators are used to generate the many supplies and references. +/- 5 V is used to supply the on-board reference generating OpAmps, +1 V is used for both the analog and digital supplies, and two more voltage levels are used for the off-board reference generation option. Reference buffers using the current feedback amplifier commonly used in previous OSU projects are available on the PCB but improved performance (~0.5 dB SNDR) is observed using the off-board references.

The 4-layer PCB is designed with a solid ground plane and separate supply planes but using separate supplies for the analog, digital, and output buffer power is observed not to improve performance. On-board potentiometers allow the configuration of the OpAmp bias currents, the OpAmp common-mode input and output, the subADC reference, and the optional on-board MDAC references.

5.7.2 Measurements, Observations, and Troubleshooting

Many observations are made from the DNL and INL of the converter at low and high speed measurements. A 10 MS/s sampling rate measurement using a 260,000 point cumulative histogram test with a 502.3 kHz input signal is shown in Figure 52 (a). The large jumps in the INL indicate linearity limiting gain errors in the 1^{st} and 2^{nd} stages greater than 1 LSB, but are not accompanied by missing codes with a -1 value in the DNL. These jumps all transition in the same direction and occur over a number of bins, giving the gain error jumps a “smeared” appearance. The DNL and INL at 60 MS/s, shown in Figure 52 (b), have a “noisier” appearance but similar INL shape and overall linearity performance. The DNL has varying degrees of “noisiness” depending on the comparator reference bias REFB, the current biases, and the chip being tested.

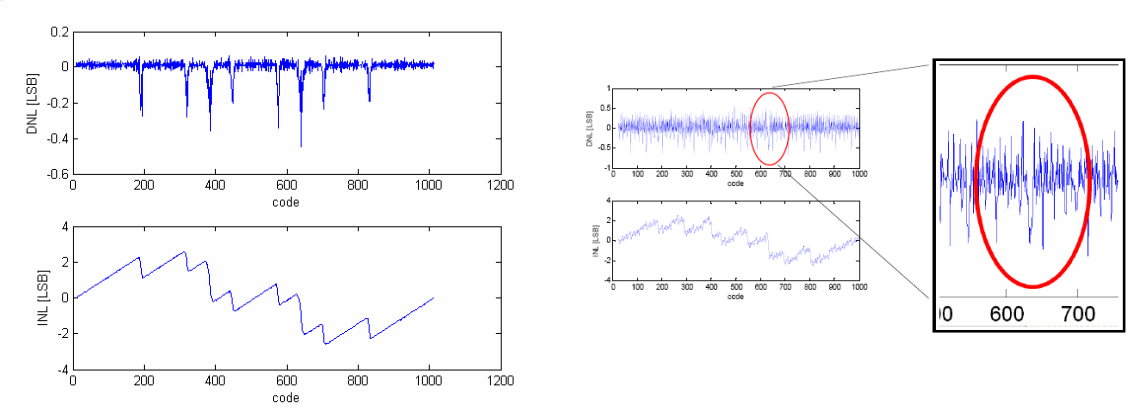


(a) (b)

Figure 52: DNL and INL for (a) 10MS/s and (b) 60MS/s sampling rate

The likely causes of these observations come from random comparator offsets and gain errors. Simulated in Simulink, a pipelined ADC with 40dB OpAmp gain and 10 mV, random comparator offsets in the 1st and 2nd stage yields Figure 53 (a) with large, smeared INL jumps and shallow DNL codes across many of bins. The OpAmp gain errors cause the ADC to have missing codes, but the random comparator offsets fill the codes back in. Figure 53 (b) shows a measurement with the same shallow DNL codes and similar distortion in the INL. The SDR and SFDR of the measured results and the simulated example are also similar.

Random comparator offsets in this design may be due to using the noisy, digital supply for the dynamic latch, or using analog ground as one of the references for the subADC. Using only a dynamic latch without a pre-amp also makes the comparator more susceptible to the random offsets. The random offsets in the pipeline stages do not degrade performance as long as the random offsets remain within the correctible redundancy range. In fact, for some signal amplitudes, the use of threshold dithering improves the SFDR in the presence of gain errors [19]. The exception is the final 2-bit flash, where the noisy threshold directly degrades the SNR, though this is not suspected to be the main SNR limitation of this design.



(a) (b)

Figure 53: (a) Simulated and (b) measured DNL and INL showing gain errors in the presence of random comparator offsets

Identifying the cause of a gain error is difficult because many different types of gain errors can result in a similar INL. The consistently downward jumps in the INL indicate that the gain is less than it should be, ruling out random mismatches in capacitors, but not parasitic or gradient mismatches. Top plate connection lines that run between capacitors in the common-centroid array may couple to the bottom plate of the capacitors to cause a gain error, requiring wider spacing between capacitors. The 0.18 μm National Semiconductor process used to fabricate this design is also known to have noticeable gradients across wafers, as well as matching errors due to variations in the structures that surround the capacitor array, even with the use of peripheral dummies in the capacitor array.

An OpAmp gain error is also a likely cause in this low voltage design. By varying the external reference CM_adj that controls the common-mode output of the OpAmps and observing the total distortion for different current biases, one can observe the change in transistor output impedance if the OpAmp gain is indeed the limiting error. A -8 dB signal and a 1.8 V supply are used to reduce the effect of limited output swing. Around the ideal operating region of CM_adj = 0.36 V, Figure 54 supports a gain error limitation because changes in the signal to total distortion ratio (SDR) are correlated to the changes

in the bias current. The steep left side of the graph likely occurs because the low common-mode both reduces the output stage g_m and increases the g_{ds} as the NMOS inputs operate in triode, whereas the right side corresponds to the reduction in the PMOS output impedance as the common-mode approaches the upper supply rail. Decreased gain with increased current can also indicate an IR drop. As mentioned before in section XXX, an IR gain error created by DC current flow from the OpAmp output to the common-mode feedback sensing resistors is avoided by using an additional set of output traces at the OpAmp output.

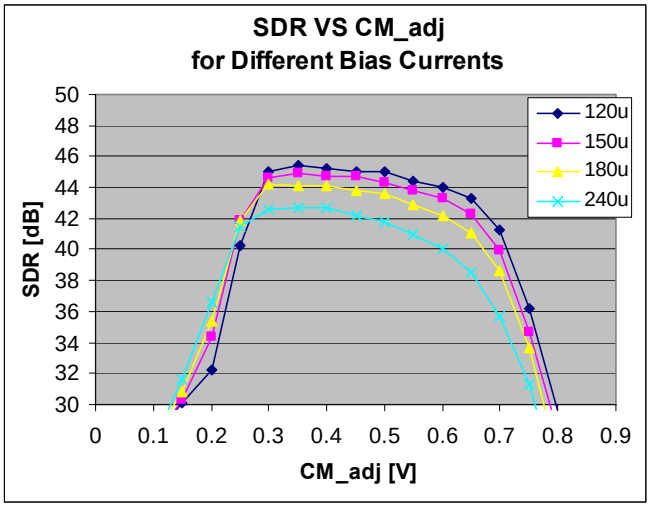


Figure 54: The effect of OpAmp bias current on the total measured distortion

Simulation shows 72 dB loop gain for the OpAmp using the National Semiconductor process models available during the design phase. Models acquired after tape-out show a typical gain of 64 dB, which still meets the gain requirement for the SFDR to be greater than 70dB. The additional 24 dB reduction in gain to account for the measured performance can be caused by a number of sources. Simulations with the new models also reveals variations in the NMOS threshold voltage that cause many transistors, including the second stage input devices and nearly every NMOS device in the boosting amps, to operate in sub-threshold leading to a loss of simulated speed in

addition to the reduced output impedance. A theoretical loss of the boosting gain enhancement while maintaining proper biasing can reduce the gain to around 40 dB, suggesting that the boosting amplifiers may be at fault.

Another observation that may explain the gain error is the difference between the positive and negative thresholds jumps that appear in the INL. Figure 52 shows how the gain error jumps at the positive threshold for both the 1^{st} and 2^{nd} stage appear larger than the negative threshold. This is observed in many chips as well as for different configurations of operation.

SNR performance degrades at high input signal frequencies, likely due to sampling clock jitter. Using a Tektronix AWG710B arbitrary waveform generator for a clock, the roll-off in the SNR leads to an estimated 10 ps jitter for the internal sampling clock. Using a full-scale sinusoid from the RF generator as the input clock improves the SNR roll-off for an estimated 5.5 ps jitter.

5.7.3 Performance Summary

A performance summary of the ADC is given in Table 1. The best presentable performance is observed with 30% less bias current than originally designed, yielding slightly varying results compared to operation using 100% bias current, particularly with the appearance of the DNL and INL.

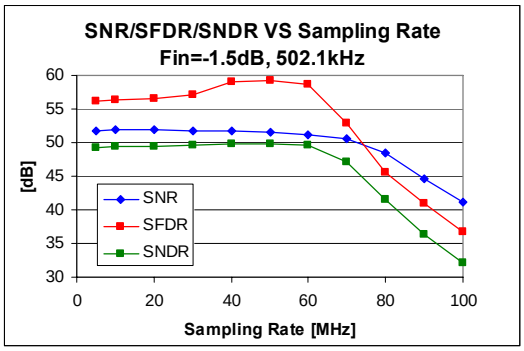
Table 1: Pipelined ADC measured performance summary

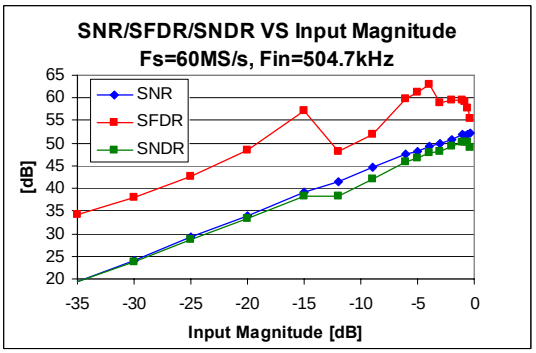
Technology	0.18 μm 5m CMOS
Supply	1 V
V_{tn}	~450 mV
Sampling Rate	60 MS/s
SNR (500kHz/50MHz)	51.4/50.4 dB
SDR (500kHz/50MHz)	54.5/55.1 dB
SFDR (500kHz/50MHz)	58.8/61.1 dB
SNDR (500kHz/50MHz)	49.7/49.3 dB
ENOB	7.96
Power	34 mW
DNL	+0.4/-0.7 LSB
INL	+1.5/-2.7 LSB
Input Bandwidth	200 MHz
Die size (no pads)	1.8 mm x 0.8 mm
$\mathbf{FOM} = \frac{\mathbf{P_{diss}}}{\mathbf{2^{ENOB} \cdot f_{samp}}}$	2.3 pJ/sample

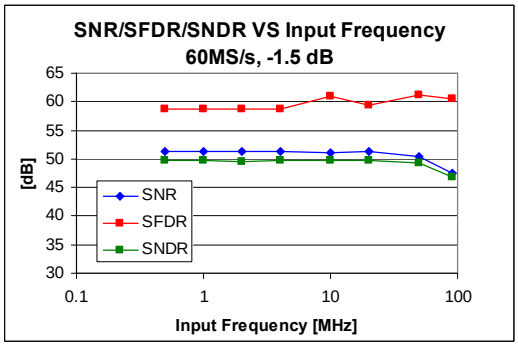
The linear performance of this design is limited most significantly by gain errors in the 1st and 2nd stage and achieves a typical SFDR between 55 dB and 62 dB for large signals up to 60 MS/s. OpAmp noise limits the noise performance to 52 dB SNR for a -1.5 dB signal which agrees with simulated results to within 1.5 dB. Frequency spectrums are harmonic rich, typically dominated by the 3rd tone for large amplitudes due to the 3rd order shaping of the INL though often dominated by higher order tones for smaller signals. The input bandwidth is about 200 MHz with little change in the distortion up to 90 MHz for a full swing signal, confirming the effectiveness of removing the S/H and using the T/R for these input frequencies. Measuring higher frequency signals accurately is not possible due to lack of appropriate filters. Using an unfiltered source with approximately 50 dB SFDR reveals a region of increased distortion around 150 MHz, suggesting that sampling errors between the MDAC and subADC of the first stage become greater than the redundancy range at this frequency.

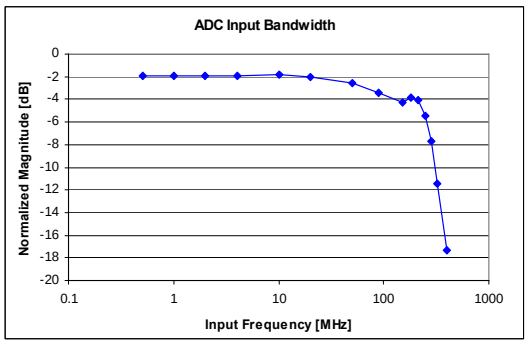
Table 2 is an arrangement of data characterizing the performance.

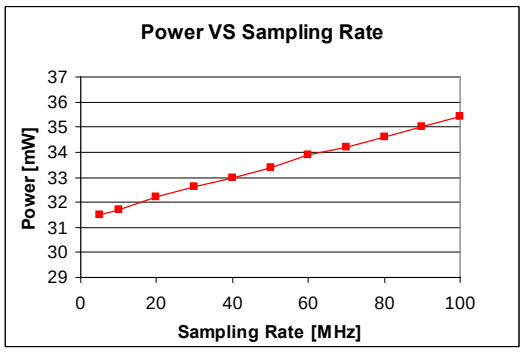
Table 2: Performance plots

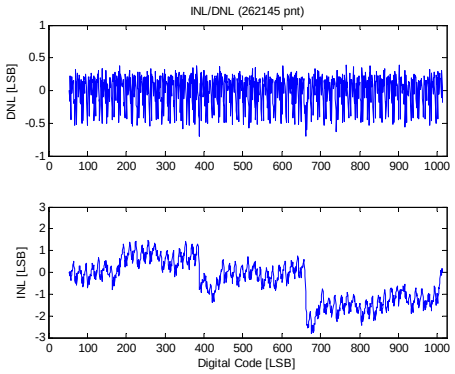


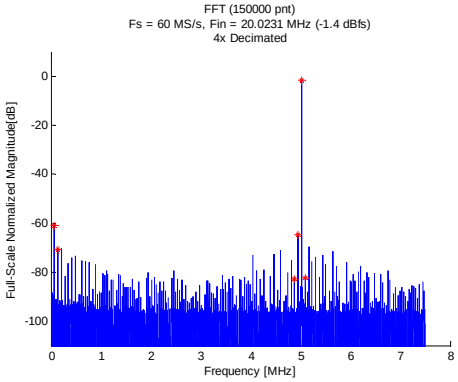


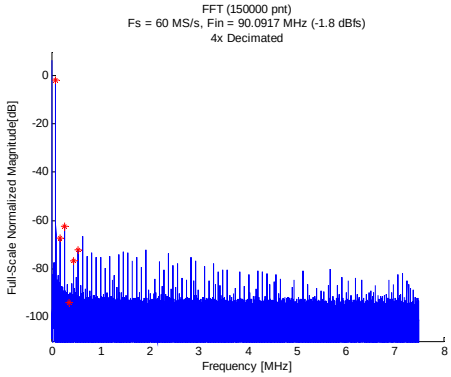









FFT (150000 pnt)
Fs = 60 MS/s, Fin = 20.0231 MHz (-1.4 dBfs)
4x Decimated
Full-Scale Normalized Magnitude[dB]
0
-20
-40
-60
-80
-100
0
1
2
3
4
5
6
7
8
Frequency [MHz]


FFT (150000 pnt)
Fs = 60 MS/s, Fin = 90.0917 MHz (-1.8 dBfs)
4x Decimated
Full-Scale Normalized Magnitude[dB]
0
-20
-40
-60
-80
-100
0
1
2
3
4
5
6
7
8
Frequency [MHz]

6 Conclusions

6.1 Evaluation of Design

Use of the fully differential ORST is demonstrated at the 8-bit ENOB level for a 60 MS/s sampling rate. Most of the distortion is suspected to come from other sources in the circuit, and speed is limited by the switch resistances because faster sampling rates near 100 MS/s are observed for larger supply voltages.

Removing the S/H and replacing it with the T/R is confirmed to create little distortion up to 90 MHz which is limited by the inability to generate pure sinusoids of higher frequencies with available equipment. The bandwidth is measured with a less than pure sinusoid to be near 200 MHz. The bandwidth is limited by the series resistance of the T/R and by the sampling rate of the converter because of the transient recovery time coming out of the reset mode.

Use of the extended input range for a 10-bit converter does not have a significant effect on the noise performance due to the dominant role of quantization noise in the noise budget. In the 10-bit case, kT/C noise possibly accounts for 20% of the total noise. This technique is more suited for high resolution converters of 14-16 bit where the kT/C noise can contribute near to 75% of the total noise. Use of the extended input range does help to correct the common-mode error and increase the feedback factor in the first stage.

Distortion in this prototype is suspected to come from lack of gain in the amplifier. This may be due to lack of accurate models, failure of the boosting amplifiers, or possibly an IR drop gain error.

Noise in this design is dominated by OpAmp noise and is within 1.5 dB of simulation results using the SpectreRF periodic noise analysis (PNOISE). Noise performance can be improved by 2-3 dB by reducing contributions from the boosting amplifiers.

The NSC 0.18 μm models provided at the time of design (R5.1) show reduced performance compared to the newly available models (R7). An estimated 7 dB of gain

and 20% g_m are lost in simulation using the new models. NMOS threshold voltages also vary greatly and compromise the biasing of the circuits. Large transistors with small overdrive experience V_t changes by as much as 87 mV from the old to new models.

6.2 Design Improvements and Future Work

Upon evaluation of the fabricated design and reflection on the design itself, the following improvements and future work are suggested:

- Scaled optimization of the front-end T/R cascades with overall reduction in the amount of signal attenuation needed during reset. The amount of redundancy range required to correct signal feed-through is insignificant in this design. Allowing less attenuation relaxes the other design requirements of the T/R.
- Separate common-mode feedback for the 1st and 2nd stage of the OpAmp to reduce common-mode transients in the input stage.
- Use larger boosting amplifiers with additional compensation to reduce both thermal and flicker noise from the boosters and reduce the effect of routing parasitics on the loop dynamics. Also add a configurable option to switch between using the boosters and a fixed bias. The extra capacitive parasitics of option switches merely compensate the booster loop.
- Optimize noise reduction of the OpAmp in reset mode using the switched-RC block between stages.
- Lay out the boosting amplifiers *between* the 1st and 2nd stage of the OpAmp on either side of the differential with booster biasing duplicated on both sides and common mode connections across the layout. If the common-mode feedback circuits for the 1st and 2nd stage are independent, then the common-mode switching transients will not affect the common-mode lines that stretch across the 1st stage.
- Simplify the common-mode feedback of the boosting amplifiers using only one additional transistor parallel to the booster input pair as in [13].

- Introduce a common-mode injection to eliminate the shifting input common-mode of the OpAmp input pair. This requires only a small decrease in the feedback factor with the addition of one extra capacitor on each side of the differential that need not be accurately matched to the capacitor array units.
- Use a resistor ladder to define the subADC reference based on an additional set of MDAC references. This should be more accurate and intuitively adjustable than simply adjusting the reference from the outside.
- Use an extraction tool to precisely design the capacitor array and account for parasitics in the rest of the design. Loading of the amplifiers due to routing between stages is a concern for this design with a two-stage amplifier and cascode compensation.
- Add more testing configurability, including a mode where the common-mode switching can be completely disabled when operating at a larger voltage supply.
- Apply a digital gain calibration scheme to relax the OpAmp requirements and complexity, thereby largely improving both the distortion and noise performance of the ADC.
- Higher speed operation can be demonstrated. Use new process models to more accurately simulate and use a larger over-design margin to push speed above 100 MS/s.

Bibliography

[1] "International Technology Roadmap for Semiconductors – Executive Summary," Available ONLINE http://www.itrs.net/statistics.html, pp. 81-81, 2005.

[2] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipelined Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 34, pp. 599-606, May 1999.

[3] A. M. Abo, "Design for Reliability of Low-Voltage, Switched-Capacitor Circuits," U. Cal. Berkley *Ph.D. Dissertation*, 1999.

[4] G.-C. Ahn *et al*, "A 0.6-V 82-dB Delta-Sigma Audio ADC Using Switched-RC Integrators," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2398-2407, Dec. 2005.

[5] G.-C. Ahn, "Design techniques for low-voltage and low-power analog-to-digital converters," Oregon State U. *Ph.D. Dissertation*, 2006.

[6] B. K. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 629-633, Dec. 1983.

[7] A. M. Ali *et al*, "A 14-bit 125MS/s IF/RF Sampling Pipelined ADC with 100dB SFDR and 50 fs Jitter," *IEEE J. Solid-State Circuits*, vol. 41, pp. 1846-1855, Aug. 2006.

[8] A. Baschirotto, R. Castello, and G. Montagna, "Active Series Switch for Switched-OpAmp Circuits," *Elec. Letters*, vol. 34, no. 14, pp. 1365-1366, Jul. 1998.

[9] K. Bult and G. J. G. Geelen, "A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1379-1384, Dec. 1990.

[10] J. Carnes and U.-K. Moon, "The Effect of Switch Resistances on Pipelined ADC MDAC Settling Time," Proc. *IEEE Int. Symp. Circuits and Systems*, DOI 10.1109/ISCAS.2006.1693817, May 2006.

[11] D.-Y. Chang and U.-K. Moon, "A 1.4-V 10-bit 25-MS/s Pipelined ADC Using

OpAmp-Reset Switching Technique," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1401-1404, Aug. 2003.

[12] D.-Y. Chang, G.-C. Ahn and U.-K. Moon, "Sub-1-V Design Techniques for High-Linearity Multistage/Pipelined Analog-to-Digital Converters," *IEEE Trans. Circuits Syst. I*, vol. 52, pp.1-12, Jan 2005.

[13] Y. Chiu, P.R.Gray and B. Nikolic, "A 14-b 12-MS/s CMOS Pipelined ADC With Over 100-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2139-2151, Dec. 2004.

[14] T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s 35 mW Pipeline A/D Converter," *IEEE J. Solid-State Circuits*, vol. 30, pp. 166-172, Mar. 1995.

[15] D. W. Cline and P. R. Gray, "A Power Optimized 13-b 5 Msamples/s Pipelined Analog-to-Digital Converter in 1.2 um CMOS," *IEEE J. Solid-State Circuits*, vol. 31, pp. 294-303, Mar. 1996.

[16] A. Coban and P. Allen, "A 1.75-V Rail-to-Rail CMOS Opamp," Proc. *IEEE Int. Symp. Circuits and Systems*, vol. 5, pp. 497-500, Jun. 1994.

[17] J. Crols and M. Steyaert, "Switched-OpAmp: An Approach to Realize Full CMOS Switched-Capacitor Circuits at Very Low Power Supply Voltages," *IEEE J. Solid-State Circuits*, vol. 29, pp. 936-942, Aug. 1994.

[18] M. Das, "Improved Design Criteria of Gain-Boosted CMOS OTA With High-Speed Optimizations," *IEEE Trans. Circuits Syst. II*, vol. 49, pp. 204-207, Mar. 2002.

[19] H. S. Fetterman, D. G. Martin and D. A. Rich, "CMOS Pipelined ADC Employing Dither to Improve Linearity," Proc. *IEEE Cust. Int. Circuit. Conf.*, pp. 109-112, May 1999.

[20] K. Gulati *et al.*, "A Highly Integrated CMOS Analog Baseband Tranceiver with 180 MSPS 13-bit Pipelined CMOS ADC and Dual 12-bit DACs," *IEEE J. Solid-State Circuits*, vol. 41, pp. 1856-1866, Aug. 2006.

[21] H.-C. Kim, D.-K. Jeong and W. Kim, “A 30mW 8b 200MS/s Pipelined CMOS ADC Using a Switched-OpAmp Technique,” Proc. *IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, vol. 1, pp. 284-285, Feb. 2005.

[22] H. Ishii, K. Tanabe and T. Iida, “A 1.0V 40mW 10b 100MS/s Pipeline ADC in 90nm CMOS,” Proc. *IEEE Cust. Integrated Circuits Conf*., vol. 1, pp. 395-398, Sep. 2005.

[23] D. A. Johns and K. Martin, “Analog Integrated Circuit Design,” John Wiley & Sons, Inc., R.R. Donnelley, Crawfordsville, 1997.

[24] B. Y. Kamath, R. G. Meyer and P. R. Gray, “Relationship Between Settling Response and Settling Time of Operational Amplifiers,” *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 347-352, Dec. 1974.

[25] A. N. Karanicolas, H.-S. Lee and K. L. Bacrania, “A 15-b 1-Msample/s Digitally Self-Calibrated Pipeline ADC,” *IEEE J. Solid-State Circuits*, vol. 28, pp. 1207-1215, Dec. 1993.

[26] M. Keskin, U.-K. Moon and G. C. Temes, “A 1-V 10-MHz Clock-Rate 13-Bit CMOS Δ-Σ Modulator Using Unity-Gain-Reset Opamps,” *IEEE J. Solid-State Circuits*, vol. 37, pp. 817-824, Jul. 2002.

[27] H.-S. Lee, “Fundamental Limits and Practical Design Issues in A/D Converters,” Proc. *IEEE Int. Solid-State Circuits Conf*., Short Course Tutorial, pp. 7, Feb. 2006.

[28] S. H. Lewis, “Optimizing the Stage Resolution in Pipelined, Multistage, Analog-to-Digital Convertes for Video-Rate Applications,” *IEEE Trans. Circ. Sys. II*, vol. 39, Aug. 1992.

[29] S. H. Lewis, H. S. Fetterman, G. F. Gross Jr., R. Ramachandran and T. R. Viswanathan, “A 10-b 20Msample/s Analog-to-Digital Converter,” *IEEE J. Solid-State Circuits*, vol. 27, pp. 351-358, Mar. 1992.

[30] J. Li and U.-K. Moon, “Background Calibration Techniques for Multistage Pipelined ADCs with Digital Redundancy,” *IEEE J. Solid-State Circuits*, vol. 50, pp. 531-538, Sep. 2003.

[31] J. Li, G.-C. Ahn, D.-Y. Chang and U.-K. Moon, “A 0.9-V 12-mW 5-MSPS Algorithmic ADC with 77-dB SFDR,” *IEEE J. Solid-State Circuits*, vol. 40, pp. 960-969, Apr. 2005.

[32] I. Mehr and L. Singer, “A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC,” *IEEE J. Solid-State Circuits*, vol. 35, pp. 318-324, Mar. 2000.

[33] B.-Y. Min, P. Kim, F. W. Bowman, D. M. Boisvert and A. J. Aude, “A 69-mW 10-bit 80-MSample/s Pipelined CMOS ADC,” *IEEE J. Solid-State Circuits*, vol. 38, pp. 2031-2039, Dec. 2003.

[34] B. Murmann and B. E. Boser, “A 12-bit 75-MS/s Pipelined ADC Using Open-Loop Residue Amplification,” *IEEE J. Solid-State Circuits*, vol. 38, pp. 2040-2050, Dec. 2003.

[35] C. G. Myers, “Design of High-Performance Pipeline Analog-to-Digital Converters in Low Voltage Processes,” Oregon State U. *Masters Thesis*, pp. 51-60, Feb. 2005.

[36] D. B. Ribner and M. A. Copeland, “Design Techniques for Cascoded CMOS Op Amps with Improved PSRR and Common-Mode Input Range,” *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 919-925, Dec. 1984.

[37] E. Siragusa and I. Galton, “A Digitally Enhanced 1.8-V 15-bit 40-MSample/s CMOS Pipelined ADC,” *IEEE J. Solid-State Circuits*, vol. 39, pp. 2126-2138, Dec. 2004.

[38] L. Sumanen, M. Waltari and K. A. I. Halonen, “A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter,” *IEEE J. Solid-State Circuits*, vol. 36, pp. 1048-1055, Jul. 2001.

[39] S. Sutarja and P. Gray, “A Pipelined 13-bit, 250ks/s, 5-V Analog-to-Digital Converter,” *IEEE J. Solid-State Circuits*, vol. 23, pp.1316-1323, Dec. 1988.

[40] E. J. van der Zwan and E. C. Dujkmans, “A 0.2mW CMOS Sigma-Delta Modulator for Speech Coding with 80 dB Dynamic Range,” *IEEE J. Solid-State Circuits*, vol. 31, pp. 1873-1880, Dec. 1996.

[41] M. Waltari and K. A. Halonen, “1-V 9-bit Pipelined Switched-OpAmp ADC,” *IEEE J. Solid-State Circuits*, vol. 36, pp. 129-134. Jan. 2001.

[42] W. Yang, D. Kelly, I. Mehr, M. T. Sayuk and L. Singer, “A 3-V 340-mW 14-b 75Msamples/s CMOS ADC with 85-dB SFDR at Nyquist Input,” *IEEE J. Solid-State Circuits*, vol. 36, pp. 1931-1936, Dec. 2001.

[43] M. Yoshioka, M. Kudo, K. Gotoh and Y. Watanabe, “A 10b 125MS/s 40mW Pipelined ADC in 0.18um CMOS,” Proc. *IEEE Int. Solid-State Circuits Conf*., vol. 1, pp. 282-283, Feb. 2005.