AN ABSTRACT OF THE THESIS OF

Iranpour Khormaei for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on November 22, 1994.

Title: High Resolution Electroluminescent Display Using Active Matrix Approach.

Abstract approved: _____

John F. Wager

An approach to a high resolution display based on electroluminescent (EL) technology is developed. In this approach, a silicon wafer with integrated high-voltage EL drivers and low-voltage line drivers is used for the EL thin-film substrate. New approaches in circuit design and thin-film processing are developed in order to achieve an active matrix electroluminescent (AMEL) display providing the capability and flexibility required for various head-mounted display applications. A zener transistor concept is incorporated into the pixel design to allow for the achievement of a pixel pitch of 24 μm. The EL processing is adjusted to allow for the use of IC processing already available in a commercial silicon foundry. These EL processing modifications include the use of atomic layer epitaxy (ALE) thin-films to achieve conformal coating requirements, modification of the EL thin-film stack structure to avoid thin-film stress problems, and changes in the process flow to allow for the use of Al conductors. Furthermore, to achieve the desired high brightness levels, the drive frequency is increased to about 5 kHz, from a typical value of 60 Hz. Brightness saturation problems associated with driving the AMEL device at such a high frequency are investigated and resolved. To achieve 64 levels of gray scale, a new digital gray scale approach is successfully incorporated into the display operation. The improvements are demonstrated in the realization of a 1280 x 1024 AMEL display.

High Resolution
Electroluminescent Display Using Active Matrix Approach

by
Iranpour Khormaei

A THESIS
submitted to
Oregon State University

in partial fulfillment of
the requirements for the
degree of

Doctor of Philosophy

Completed November 22, 1994
Commencement June, 1995

Doctor of Philosophy thesis of Iranpour Khormaei presented on November 22, 1994

APPROVED:

Redacted for Privacy

Major Professor, representing Electrical and Computer Engineering

Redacted for Privacy

Head of Department of Electrical and Computer Engineering

Redacted for Privacy

Dean of Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Redacted for Privacy

Iranpour Khormaei, Author

Dedicated to my mother and memory of my father
whose visions and self sacrifices made it all possible

ACKNOWLEDGMENTS

I would like to express my gratitude to Professor John F. Wager and Dr. Christopher N. King for their guidance and encouragement throughout my graduate studies. Without their energetic support and the many fruitful discussions, the completion of this work would not have been possible.

I would like to thank Dr. Thomas Plant, Dr. Jack Kenney, and Dr. Robert Burton for serving on my Ph.D. committee. I would also like to thank the members of Advanced Technology group at Planar Systems and especially the AMEL team whose dedication and hard work made the final results possible. The financial assistance for the AMEL work, provided by Advanced Research Project Agency (ARPA) under the contract MD972-92-C-0037, along with the efforts from various companies under this contract are greatly appreciated.

Thanks are also due to my brother and his wife, for their support and guidance since the start of my university studies. Special thanks are due to my wife who patiently supported me in the pursuit of this degree. Her devotion and quality time sacrifices during our first year of marriage will always be on my mind and appreciated.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

Page

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

LIST OF TABLES

Page

High Resolution
Electroluminescent Display Using Active Matrix Approach

Chapter I. INTRODUCTION

Recent technical advances require better user interfaces to allow for a more efficient use of complex systems. Displays are one of the most common interfaces. As such, display issues are of major importance for applications ranging from industrial and military to medical and entertainment fields. Despite their varied usage, displays can be categorized in one of several ways. One such category is that of portable systems. Such systems are now well accepted in the marketplace for applications such as laptop computers. In the near future, such portable systems are expected to allow accessibility to technical data for technicians or warehouse workers via a complete computer system on their belt. In the medical field, portability is a desired characteristic for systems used for monitoring vital signs or for providing a patient's medical information. A second display category is that of high resolution systems. This type of display is best exemplified by the well publicized high definition television (HDTV) or by displays planned for X-ray result viewing in hospitals. This type of high quality application requires displays with high resolution and a large number of pixels (on the order of 2000 x 2000). Another display category is associated with applications in which computer-generated data can be displayed in such a manner that the viewer can simultaneously observe the actual surroundings.[1] In the medical field, such displays could increase the accuracy or speed of surgical operation procedures where separately acquired, or computer generated, data are presented to the surgeon, e.g. endoscopic surgery.[2] Finally, rirtual reality (VR) applications fall in a separate category.[3] VR, expected to be an important part of the future of the entertainment business, requires displays with resolutions and brightnesses that allow a wide viewing angle without sacrificing the details of the picture. These requirements are based on VR's eventual goal of providing computer generated graphics so realistic that the user would be able to interact with a fully or partially synthesized world. All of these applications require display devices with capabilities beyond those available with present day technology.

Research in a number of display technologies has intensified in order to satisfy the demands of these new applications and to capture a corresponding market share. The main display technologies include cathode ray tube (CRT), liquid crystal display (LCD), plasma display (PD), and electroluminesence (EL). CRT, which is used in household

televisions, is the most mature technology and is accepted as the display with the best optical performance. However, CRTs suffer from being heavy, having large dimensions and requiring the use of high internal voltages. These CRT shortcomings have opened up opportunities for other display technologies which fall in the "flat-panel" category. As the name implies, flat panel displays (FPDs) have the common characteristic of being thin. LCD is the most common flat panel display technology and enjoys the widest application range and the lowest cost. It is basically a light modulating device where an external light source is used to illuminate the display and the display blocks or passes the light depending on the desired display pattern. The need for an external light source and the slow speed of the patterns on the display are among the limitations of this type of display. Plasma displays are light-emitting and operate in a similar manner as fluorescent lamps. This technology has demonstrated large areas and high brightness; however, unresolved issues remain in power consumption, color, and high resolution capabilities. Electroluminescent displays are also light-emitting and are based on a fully solid state structure. This technology has demonstrated good optical appearance and high resolution; however, compared with other technologies, it suffers from higher power, difficulty with color, and higher cost. These technologies are reviewed in more depth in Chapter 2.

Reviewing the applications enumerated earlier, varied and sometimes conflicting requirements must be met. These requirements include high brightness, low power, low cost, high resolution, and easy portability. HDTV and other high resolution display applications appear to require large displays. For this reason, projection CRTs or plasma screens have been viewed as the only possible display options. In the portable system category, displays with compact size, low cost, and low power are of primary concern. These requirements make LCDs the primary contestant. Finally, VR-type applications are based on providing appropriate images which depend on the user's viewing direction. This requirement appears to leave no practical solution other than a head-mounted display (HMD) approach where the display is coupled to the user's head, e.g. installed on a helmet.[4,5] Due to the low weight and small size requirements, obvious constraints for an HMD device, a flat panel display is required for this application but no technology has taken the lead yet. To meet the requirements for each display category, extensive work is ongoing worldwide in each of the technologies.

An ideal and cost effective approach would be to find a display system that could meet the requirements for most of the different applications. Since such a display technology does not exist and is not likely to be developed, other approaches need to be considered. A potential candidate to meet these varied requirements is a single display in a HMD format. In HMD applications, the viewing angle and optical appearance could be controlled primarily by the optics. The display is coupled with the appropriate optics to

provide the desired image to the eye. The user sees an image of the display at the desired distance and dimensions. A single display technology could be used with appropriate resolution and display format, to allow applications ranging from portable computers to HDTV or VR. To be effective and truly versatile, such a display should have low weight, low power, small thickness, small peripheral dimensions, extremely high resolution, and high brightness. Due to these extreme requirements for the display, HMD systems have not received wide spread usage.

The goal of this dissertation is to demonstrate a display that meets the requirements previously enumerated for a HMD. In addition to HMD applications, such a display could find applications for use in direct view products. The approach pursued here is to optimize EL display performance aimed at initial use in HMD systems. As stated earlier, the standard approach to EL, like other technologies, would not allow achievement of the high performance display requirements. To meet the desired performance and versatility, the voltage driving waveform and the fabrication techniques are modified in a manner to utilize the basic EL strengths, while overcoming EL shortcomings, through the addition of necessary circuits.

The specific approach chosen here is to combine the driving circuitry and the EL stack on the same substrate. Instead of having the EL film on a separate glass substrate and then connecting it to external high voltage drivers, the goal here is to use a silicon wafer that holds the driving circuitry as the EL substrate. This technique, commonly referred to as an "active matrix" approach, removes the need for a large number of interconnects and provides various electrical and optical advantages, as discussed in Chapter 2.

EL technology's advantages for use in HMD applications include its solid state nature and its fast screen update rate. The solid state structure of EL displays allows for a very small thickness (about 1 μm for the EL stack and <40 mil for the substrate). In addition, there is no need for a large volume to encapsulate a gas or liquid, as in plasma and LCD displays. The solid state nature of the EL display also implies the need for only a single substrate and no need for another high quality substrate to be thermally matched and aligned. The fast screen update rate allows changing the data on the screen at rates above 60 Hz. This fast screen speed makes EL displays optically acceptable for HMD video applications. Furthermore, this characteristic allows a new digital gray scale approach to be implemented, with a corresponding potential for higher performance and smaller peripheral area (these issues are discussed in Chapter 3). Additionally, EL technology has demonstrated long lifetimes and is used in manufacturing environments worldwide. These general characteristics have made the EL technology a good potential candidate for HMD applications.

However, there are three main areas in which standard EL displays would not meet HMD requirements and would require use of the active matrix approach. First is the requirement for a small number of interconnects. Second are the high brightness and low power requirements for this application. The third requirement involves implementation of a new gray scale approach. These requirements are met in the work presented in this dissertation through the use of active matrix circuitry. The active matrix technique, by combining the drivers and the EL stack, allows separation of the addressing function, which is maintained at a 60 Hz frame rate, from the illumination pulses, set at a high frequency. Higher brightness is achieved by increasing the illumination frequency and lower power is achieved in this active matrix scheme due to the removal of unwanted coupling capacitance present in the standard display addressing technique. The use of a silicon substrate allows fabrication of the line drivers directly on the display substrate. This integration of the display and the drivers removes the need for interconnects to each row and column. Therefore, the addition of an active matrix scheme to the EL display resolves the concerns over the high resolution, high brightness, and low power requirements needed for HMD applications.

The final goal of the work described herein is demonstration of a monochrome display. The device is a 1280 x 1024 (i.e. the number of columns by the number of rows) display at a pixel resolution of approximately 1000 lines per inch (lpi). A color display can be fabricated using a process flow and drivers similar to the monochrome process. To achieve the full color display, a white emitting EL stack can be used with a color filter to provide the required primary colors, as discussed in Chapter 6. The characteristics of the completed monochrome display are described in Chapter 5.

The process flow for the fabrication of this display begins with silicon-on-insulator (SOI) wafers (see Fig. 1). These SOI wafers, which have a small silicon thickness for optimal device operation, are then processed in a silicon foundry for fabrication of the drivers. The IC processing employed is relatively advanced with 4 layers of metal, design rules down to 1.2 μm, and processing unique to SOI material. The processed wafer is then taken through the EL film deposition and patterning steps, including the required Al processing steps. After the EL processing, wafers are tested and diced. Individual displays are then mounted on a ceramic substrate and bonded to a cable for connection to the required external circuitry. This display is then provided to the HMD system designers for incorporation into an optics system specifically designed for this flat panel display.

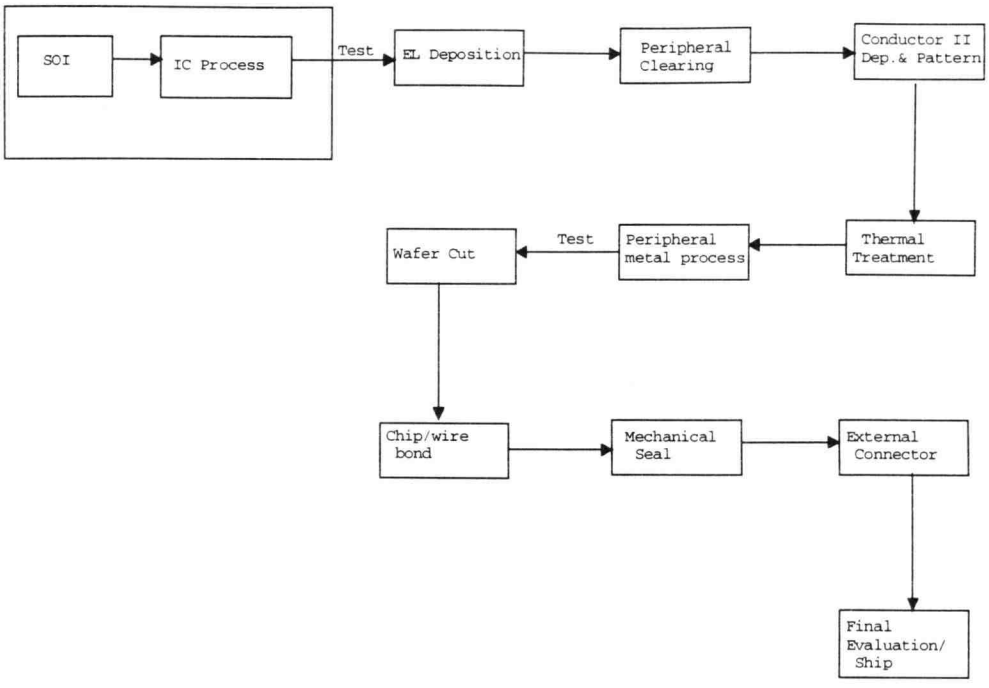

Figure 1: General EL process flow for the fabrication of an AMEL display.

The author's contributions to the fabrication of such an AMEL display are directly related to EL operation and process, as described in this dissertation. Special pixel design and low voltage transistor concepts are employed in order to obtain a smaller area pixel and, hence, the required high resolution. A new process flow is established to allow for the use of aluminum (i.e. the peripheral metal in Fig. 1) in spite of the high temperatures associated with the EL deposition process. The EL deposition process is optimized to allow for fabrication of EL devices on Si substrates without cracking of the EL film; such cracking arises from the Si and EL stack thermal coefficient of expansion mismatch. Deposition approaches are investigated to allow coverage of IC topography. A gray scale approach is developed to utilize the flexibility provided by employment of the AMEL scheme. Finally, the behavior of the EL device is investigated and the standard processing is modified to remove the brightness limitation observed in displays when driven at high excitation levels. These innovative approaches are incorporated into the final displays, as reported in Chapter 5.

To successfully produce such an AMEL system, various additional innovative designs and processes were developed in parallel with the work reported herein. The

design and lay-out of the drivers were accomplished at David Sarnoff Research Center by Dr. Fu-Lung Hsueh, Dr. Gary Dolny, Dr. Al Ipri and Mr. Roger Stewart. The silicon foundry responsible for the integrated circuit processing was Allied-Signal where developments were led by Dr. Tom Keyser, Mr. Gerry Becker, and Mr. Dan Kagey. The high resolution patterning for the EL processing was mainly developed by Mr. Ken Ping and Ms. Jacqui Knight at Planar Systems. The drive electronics for the evaluation of the displays was designed by Mr. Monte Rhoads, also at Planar Systems. These novel designs and processes were used to complete an operational AMEL display for use in an HMD system.

An outline of the dissertation is as follows. A literature overview is included in Chapter 2 in order to introduce the structure and physical operation of EL devices as well as previous work involving the active matrix scheme. The transistor requirements, circuits required in each pixel, and the gray scale approach are discussed in Chapter 3. EL compatibility issues with the silicon substrate and integrated circuit compatibility with EL processing are covered in Chapter 4. The EL physical characteristics and brightness saturation issues are also addressed in Chapter 4. The calculated electrical and optical characteristics of the AMEL display are provided in Chapter 5 and are subsequently compared with measurements of the final devices. The conclusions of this research program and potential future research directions are presented in Chapter 6. Portions of this work have been previously published or presented. [6-35]

Chapter II. LITERATURE REVIEW

The goal of the work described in this dissertation is to develop a display technology appropriate for high performance, small displays. In the previous chapter, the motivation for such a display is discussed. Developments in various technologies are required to be able to manufacture such a display. In this chapter, a review of previous relevant display work, specifically focusing on EL and active matrix, is reviewed. This background sets the stage for the remainder of this dissertation which details the developments required to realize the actual display.

II.1. Flat Panel Display Technologies

As discussed in the previous chapter, applications like HMD or small, direct view displays require flat panel displays in order to minimize weight, size, and power. There are three main flat panel technologies currently in production: liquid crystal display (LCD), plasma display, and electroluminescent (EL) display.[36] The most prominent technology is LCD. This technology is based on encapsulating liquid crystal material between two pieces of glass. Polarizers with perpendicular axes of polarization are placed on each side of the display such that with no liquid crystal material the display would not pass any light. Under normal conditions the liquid crystal molecules are aligned such that polarized light changes orientation and passes through the second polarizer and leaves the display. When a voltage (5-10 V range) is applied across the material, the liquid crystal alignment is disturbed and the light through the first polarizer is blocked by the second polarizer, resulting in a pixel that is off.[37] One of the issues limiting the use of LCD displays for HMD applications is the need for light transmission through the display, which limits the potential resolution when a high transmission and lack of diffraction patterns is desired. Another issue is the limited operating temperature range of the LCD display due to the liquid crystal's characteristic dependence on temperature. A third issue is the mass and heat generated by the required backlight.

A second flat panel technology is plasma display. The basic structure of these devices consists of two glass plates with patterned row and column electrodes encapsulating a gas (typically He and Xe). The application of a voltage across the electrodes results in a gas discharge and concomitant light emission.[38] These displays are suited for large area applications with relatively low information content. A fundamental

issue for using these displays for high resolution applications is that the gas glow covers a large area compared to the desired pixel area. The addition of barriers to confine the gas could be a solution to this problem but would require complicated processing and additional area.

II.2. AC Thin-Film Electroluminescence

The display technology used in this work is AC thin-film electroluminescence (abbreviated here to EL). An EL device is fabricated by sandwiching a light-emitting phosphor layer between two insulators. This structure is placed between two conductors which provide the necessary high voltage waveforms, as shown in Fig. 2. The light emitted in the phosphor layer exits the glass side through the transparent lower electrode (normally indium tin oxide, ITO).[39,40,41,42]

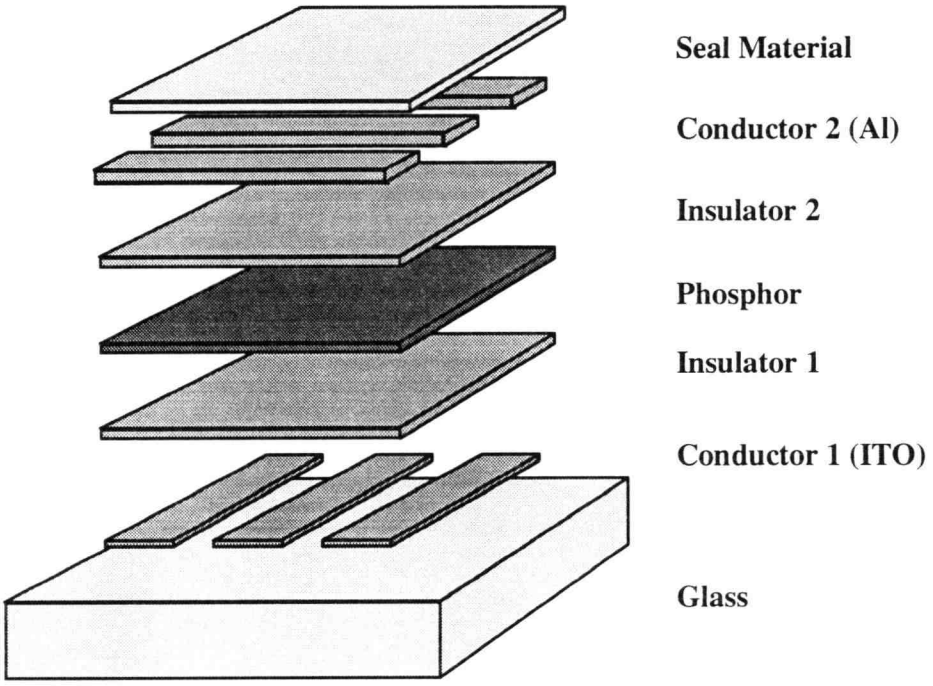

Figure 2: EL device structure.

The EL device operates via the application of alternating polarity high voltage pulses (usually between 150 and 250 volts) across the two conductors. The externally

applied voltage results in a voltage across the phosphor layer, establishing an alternating field in the phosphor. An energy band diagram for the device subject to a high voltage pulse is shown in Fig. 3. When the phosphor field reaches an adequately high level (approximately 1.8 MV/cm for ZnS), a large number of electrons emit from deep interface states and accelerate in the field. When these electrons reach adequate energies (approximately 2.2 eV), they can impact excite luminescent centers (e.g. manganese, Mn^{2+}, or terbium, Tb^{3+}). The luminescent centers then can de-excite back to their ground states, resulting in light emission. For Mn centers, the emission peak is mainly from the $^4T_1$ to $^6A_1$ transition.[42,43] ZnS:Mn light emission has a broad spectrum centered at 585 nm, i.e. a yellow-colored light. For Tb centers, the main peak is the result of the $^5D_4$ to $^7F_6$ transition.[44,45] This results in the emission peak at 545 nm, i.e. green emission. A certain percentage of the accelerated electrons reach high enough energy and ionize the valence electrons to the conduction band. All the electrons are stopped at the opposite interface and stored until the process repeats when the field is reduced, and eventually reversed, across the phosphor layer due the opposite polarity of the external ac voltage.

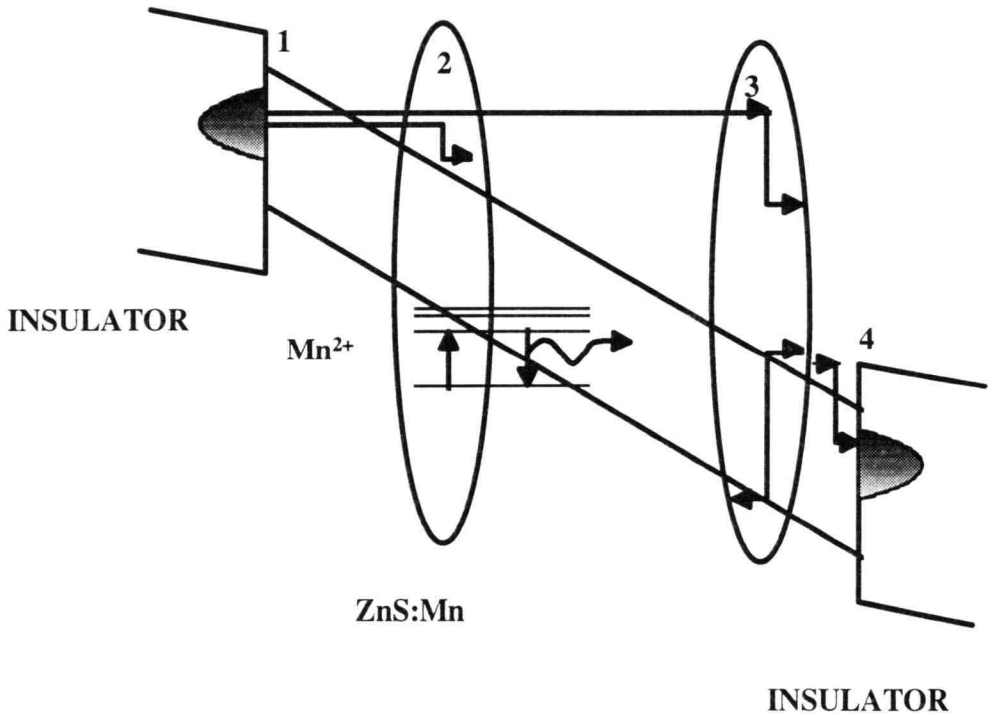

Figure 3: Energy band diagram used to explain EL operation.

As discussed above, each one of the alternating pulses results in light emission. The driving waveform typically has a rectangular pulse shape (Fig. 4a). The resulting light emission has a decay time which depends on the probability of de-excitation of the luminescent centers. The light pulses are shown in Fig. 4b. In actual applications, the human eye averages these light pulses over time. Since the luminance peak intensity increases with increasing applied voltage, the observed luminance can be plotted as a function of the maximum amplitude of the external voltage, as shown in Fig. 4c. The luminance-voltage plot exhibits a sharp turn-on characteristic common to EL devices. The steep turn-on allows use of low voltages of about 40 V to modulate pixels from on to off, even though the total applied voltage remains high, at around 200 V.

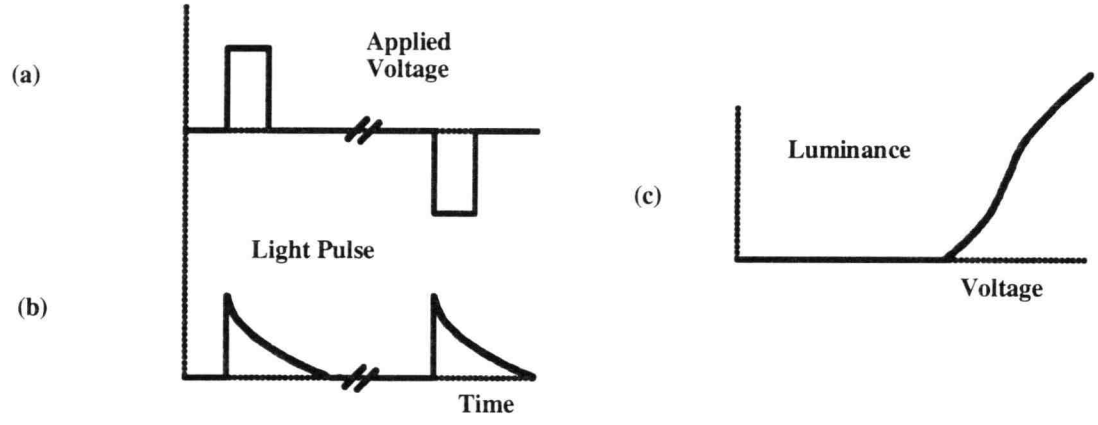

Figure 4: Light emission in relation to the applied voltage.

Various techniques have been developed for the deposition of thin film layers used in an EL stack. The most widely reported techniques are evaporation, sputtering and atomic layer epitaxy (ALE). The physical deposition approaches, evaporation and sputtering, are attractive due to their wide usage and ease of transition to a production environment.[22,46,47] However, thin films, especially insulators, deposited by physical deposition processes are more likely to have microscopic defects and typically nonconformally coat a rough surface. For these reasons, in the work described herein the ALE approach is used for the deposition of both insulators and phosphor. All three layers are deposited without a vacuum break to minimize defects and film degradation possible by exposure to air.

II.3. Atomic Layer Epitaxy For EL Applications

The ALE approach was developed by Dr. T. Suntola and colleagues at Lohja Co., currently Planar International Oy.[48,49] This deposition process is based on depositing material one atomic layer at a time. As an example, the deposition process for ZnS is illustrated in Fig. 5. The Zn element in the form of a $ZnCl_2$ gas is introduced into the deposition chamber, Fig. 5a. The temperature of the substrate and the gas flow are set to allow approximately one monolayer of $ZnCl_2$ to cover the substrate surface. Then the excess $ZnCl_2$ gas is purged by nitrogen flow through the reaction chamber Fig. 5b. The next step is the introduction of sulfur in the form of H_2S gas, Fig. 5c. H_2S reacts with the $ZnCl_2$ on the substrate to result in ZnS growth on the surface of the substrate until approximately one monolayer of ZnS is grown. The byproducts of the reaction (i.e. HCl) are pumped out with the N_2 gas flow, Fig. 5d. The choice of substrate temperature and the reaction species are crucial in the ALE process. The temperature should be high enough such that it limits the growth to only one monolayer, see the drawing on the right side of Fig. 5. At the same time, the temperature has to be low enough to avoid re-evaporation of the material from the substrate surface. The reactants need to be chosen to allow an adequate processing temperature window. The result of this ALE process is a conformal, high quality film with a low concentration of microscopic defects and voids. These characteristics have made the ALE deposition technique the approach of choice for the work of this thesis.

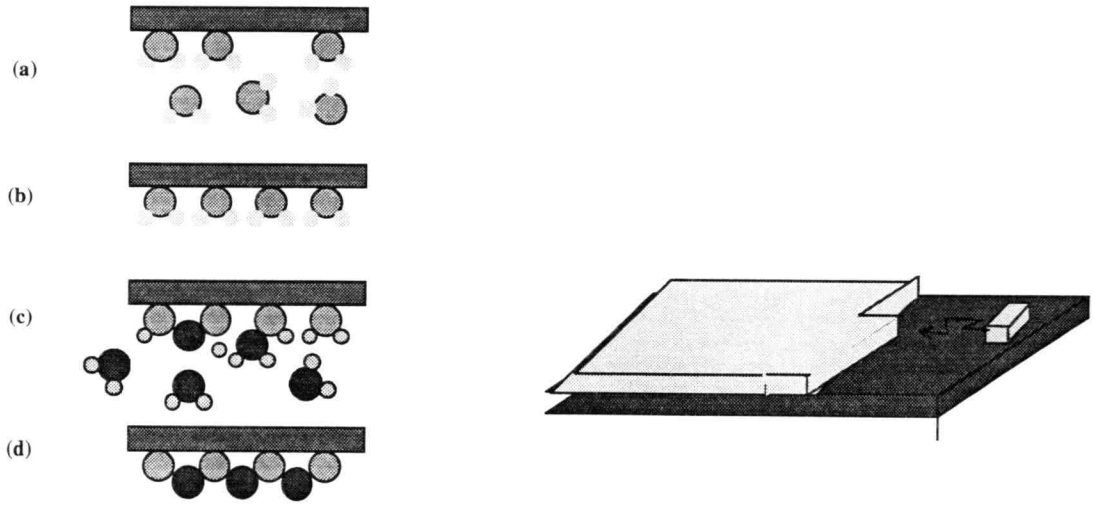

Figure 5: The ALE deposition approach.

II.4. "Inverted" EL Structure for AMEL

The normal approach for EL processing is to start with a transparent electrode on a glass substrate, as shown in Fig. 2. This approach results in light emission being viewed from the first-grown, i.e. the glass, side. However, in some applications, including the subject of this dissertation, either the substrate or the bottom electrode cannot be transparent. In such applications, the ALE process allows the use of an "inverted structure" by placing the ITO electrode on top of the display, instead of the Al electrode shown in Fig. 2.[50] For displays fabricated via physical deposition, microscopic defects initiate burn-outs. The Al electrode acts as a fuse by evaporating when excessive current flows through these defects; however, the ITO electrode does not have this fusing property and burn-outs tend to propagate. Therefore, the ALE process with its low defect density allows use of ITO instead of Al as a top electrode. In the case of the AMEL approach pursued herein, the substrate is an opaque silicon wafer; therefore, use of this inverted structure is essential.

II.5. Active Matrix Electroluminescence

To operate a matrix display, voltages are provided from the edge of the rows and columns. The standard driver approach is to apply voltages to a row at a time. For each row selected, the column voltages are set such that the net voltage across the pixel causes the pixel to turn on or remain off. This process is repeated for consecutive rows until the whole display is addressed. In this "line-at-a-time" approach, the addressing and illumination functions occur simultaneously. The combination of these two functions limits the illumination frequency since the majority of time is spent in writing the data for the rest of the rows in the display.

To allow for higher brightness and a reduced number of interconnects, Dr. Peter Brody and colleagues at Westinghouse in the early 1970's demonstrated the concept of "active matrix EL" (AMEL) for the first time.[51] The active matrix approach includes the addition of a storage and a drive element per pixel. The active matrix liquid crystal display (AMLCD) has been widely pursued, especially in Japan, since its inception in the early 1970's.[52,53] In contrast, the active matrix approach for EL has been investigated to only a minimal degree. Notable contributions to active matrix EL have been made by researchers at Westinghouse[51,54], Fujitsu Laboratories,[55] Fuji Xerox Co.[56], NTT electrical communication laboratories,[57] and the University of Gent.[58,59] This list of

efforts, and the present dissertation, are all based on a 2-transistor concept where one transistor allows storage of the data required to control the high voltage transistor. This concept is discussed further in Chapter 3. None of the previously referenced work led to continued research due to issues such as transistor or EL reliability, and high voltage transistor requirements.

Previous research on AMEL can be divided into two categories based on the material used for transistor fabrication. The first category, pursued by researchers at Westinghouse and the University of Gent, utilized CdSe for circuit fabrication. The original drive for using CdSe material instead of silicon was its potentially low processing cost.[60] The source of continued interest for CdSe is its capability for high voltage transistor fabrication. However, the poor reliability of CdSe transistors, speed and density limitations, and the non-standard processing for the Si-based industry have made this material an undesirable choice for integrated AMEL display applications. For these reasons, CdSe is not used in this dissertation.

The second category of AMEL research, pursued by the remaining research centers previously enumerated, employs Si for circuit fabrication. This choice is prompted by the excellent and well-known characteristics of Si for processing the required high speed and high voltage circuitry. Furthermore, a large amount of effort has been spent on the AMLCD approach based on Si. It is possible to use AMLCD experience to further the development of AMEL displays. The primary problems encountered previously in silicon-based AMEL applications include: EL film adhesion due to thermal coefficient of expansion mismatch; reliability issues due to the substrate topography; lack of high resolution capability; and the required high voltages.

II.6. Gray Scale and Color Capabilities

The ability to display pixels at different brightness levels, i.e. the achievement of a "gray scale", is one of the desired characteristics not demonstrated previously in AMEL displays. For standard EL displays, various gray scale schemes such as amplitude modulation, pulse-width modulation and others have been suggested.[61-64] The common characteristic of all of these approaches is the fact that they effectively lower the voltage across the phosphor layer. Due to thin film non-uniformity and the non-linear turn-on characteristic of the EL luminance-voltage curve, the brightness non-uniformity and instability is accentuated at the lower voltage levels required by these gray scale schemes.

In this dissertation, as detailed in Chapter 3, an approach is used that allows gray scale while keeping the voltage across the phosphor layer at the full "on" level.

In today's commercial market place, full-color capability is very desirable. Previous AMEL work has not dealt with this issue. For standard EL displays, the traditional approach has been to deposit and pattern three phosphors separately to achieve the three primary additive colors (red, green and blue).[65,24] The task of patterning three phosphors at 1000 lines per inch resolutions is a very difficult one. Another approach used for standard displays is to use a broad-band, "white", phosphor and to filter the light to achieve the primary colors.[66] The drawback of this approach is the need to pattern the color filters on a separate piece of glass and to then align them to the display with 1000 lpi resolution. This issue is resolved by depositing and patterning color filters directly onto the display.[29] The fabrication of color AMEL displays is left as a recommendation for future work, as described in Chapter 6.

There are several requirements for a head-mounted display, i.e. the goal of this dissertation, that have not been achieved in previous work. Silicon-on-insulator substrates (SOI) are used to allow for high resolution and for the integration of peripheral circuitry (see Chapter 3). In this work, the circuitry is designed to allow one of highest resolution displays ever made (see Chapter 3).[67] For the first time, ALE is used to successfully deposit EL thin films onto Si, as discussed in Chapter 4. For the first time, a gray scale approach unique to AMEL is utilized to allow high performance video displays (see Chapter 3). And finally, this work establishes the basis for use of a broad-band phosphor and ALE process to allow for the realization of the first full color AMELs (see Chapter 6).

Chapter III. ELECTRONICS APPROACH

As described in Chapters 1 and 2, the goal of this dissertation is to demonstrate the feasibility of a compact, high performance device for head-mount display applications. To achieve this goal, and yet ensure that the resulting display is manufacturable, an active matrix EL approach using a SOI substrate is chosen. The active matrix approach is selected in order to realize a display with high brightness and low power. The use of a single crystal Si (in this case SOI substrate) allows integration of the display and the high speed peripheral circuitry, which results in a compact display. The display/driver integration is essential in order to keep the display size to a minimum, reduce the number of interconnects, and improve the display reliability. The use of Si also allows display fabrication to be accomplished in a standard IC foundry; this is in contrast to the situation which occurs when CdSe, amorphous Si, or poly Si are employed as the active driver material. In the following discussion, the pixel circuit design, the transistor choice, and the gray scale approach are discussed.

III.1. The AMEL Structure

The structure of a standard ACTFEL matrix display consists of two orthogonal sets of electrodes across the EL stack, as shown in Fig. 6a. Addressing this matrix display is accomplished by the application of appropriate voltages to both rows and columns such that only the desired pixels are illuminated while the rest of the pixels remain unaffected. In contrast, for the AMEL approach, the high voltage addressing circuit is specific to each pixel. This addressing characteristic allows modification of the first electrode to be a square which defines the pixel. The top electrode is a common electrode for all pixels. A high voltage ac illumination pulse is applied to this common electrode and the selection is performed by each individual pixel circuit. Further discussion of the circuit operation is found in Section III.2.

The use of an opaque substrate, i.e. Si, requires the display to be viewed from the film side instead of the standard way of viewing the display through the glass substrate. As shown in Fig. 6a, the standard structure is based on the use of a transparent material, e.g. glass, as the substrate. The transparent substrate allows light emission from the substrate side and the use of Al as the top conductor. Metal electrodes, such as Al, are desirable since they allow a fusing action in case there is a defect in the EL film. In the

AMEL case, however, the opaque substrate requires the use of an inverted structure, as described in Chapter 2. The resulting AMEL structure is shown in Fig. 6b.

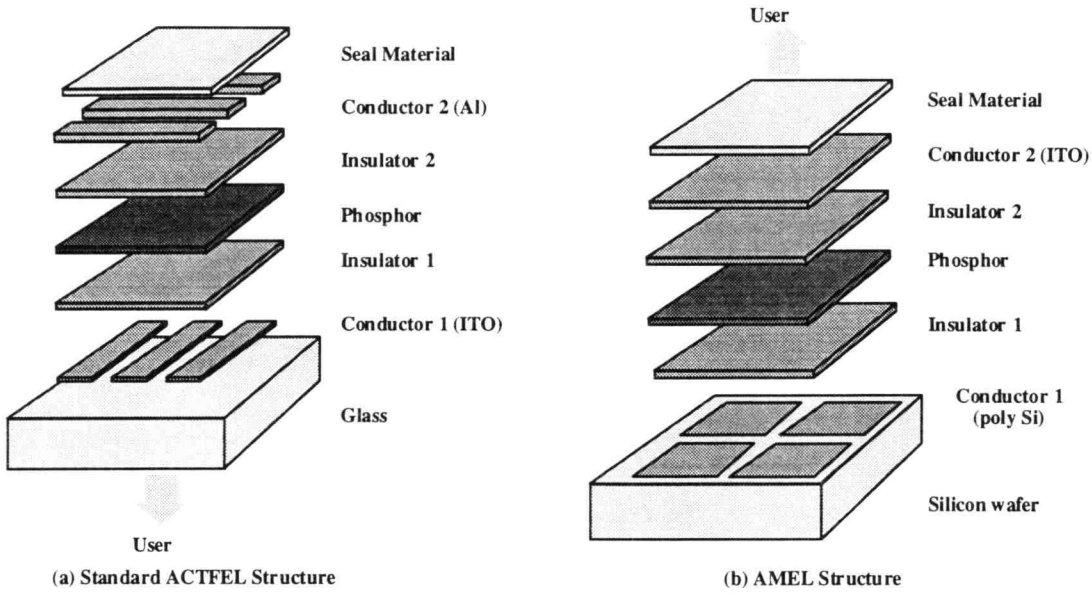

Figure 6: Comparison of standard EL and AMEL structures.

III.2. Pixel design

As discussed in Chapter 1, the traditional method for illuminating an EL display is based on a line-at-a-time addressing approach. In this approach, a voltage is applied to the selected row for a given time, while other rows are left floating. Subsequently, an appropriate voltage is applied to each column to turn on or off the desired pixel. After the row time has elapsed, such that one row has been addressed, the same procedure is repeated for the second row. This line-at-a-time addressing is continued until the whole display is addressed. The duration required to address the entire display once is referred to as the frame time. The same procedure is then repeated for the following frames. In this approach, the signal that selects the pixel is identical to the high voltage illumination pulse. Therefore, the frame update rate is limited by the maximum rate possible for addressing the whole frame. In a typical display, the maximum addressing rate is about 60 Hz, limiting the illumination frequency to 60 Hz.

In contrast, the active matrix approach allows separation of the addressing from the illumination function. To achieve this separation, the low voltage data needs to

control the pixel state independently of the high voltage illumination pulse. A low voltage transistor can be included in each pixel with the function of storing the data at each pixel. This data is then available to control the high voltage transistor and, hence, the state of the pixel. The pixel design implemented uses one low voltage transistor and one high voltage transistor to achieve separation of addressing from illumination.[51] The circuit employed for this work is shown in Fig. 7, where M1 is the low voltage transistor and M2 is the high voltage transistor.[68,6-11] The function of M1 is to store the desired pixel data onto the capacitor, Chold, based on the appropriate external control provided by the select and data lines. The high voltage transistor, M2, can act as an open or a short, depending on the voltage stored at Chold. The drain of M2 is connected to the lower EL pixel electrode. The other EL node is connected to the common ITO electrode which is driven by a high voltage ac driver; see Fig. 6b.

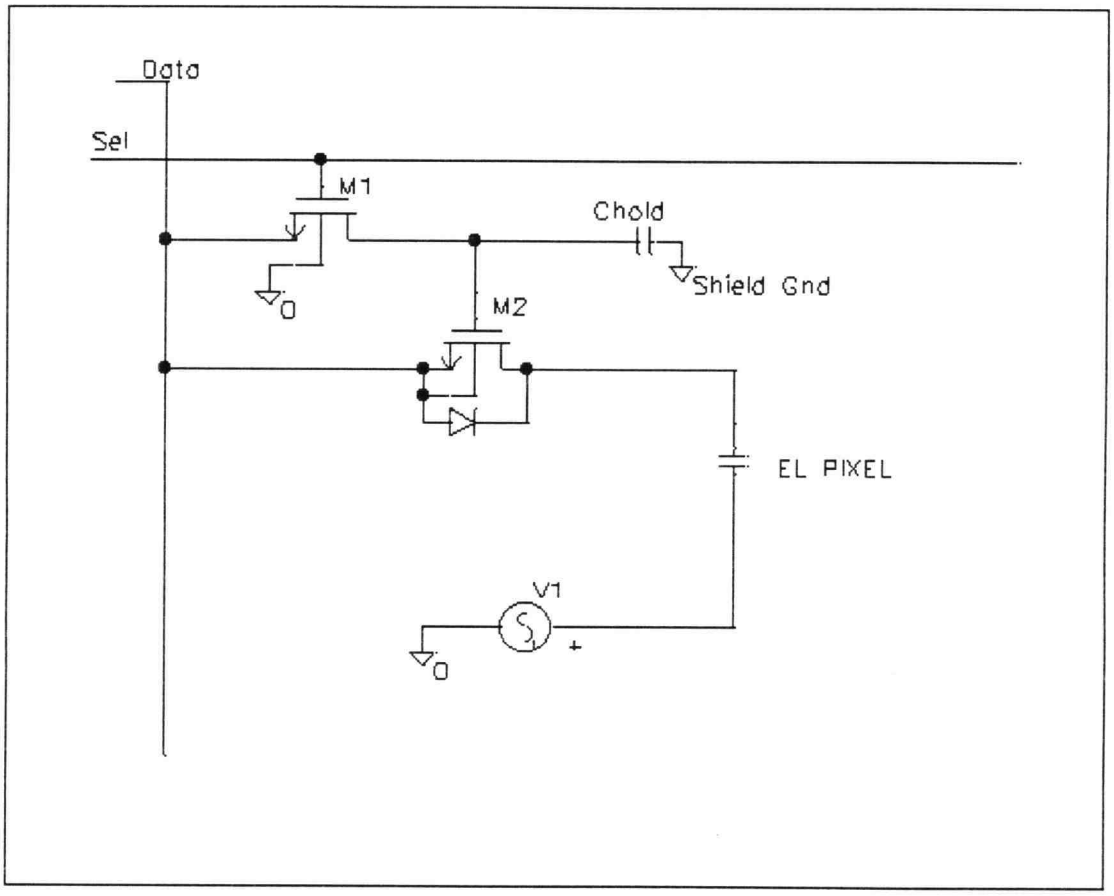

Figure 7: The AMEL pixel circuit.

The operation state of the pixel is controlled by the voltage stored at the Chold node. If the stored voltage is high, the M2 transistor is turned on and the lower EL electrode is effectively grounded. With the high voltage drive applied to the common ITO electrode, the pixel experiences a full voltage across it and emits light. On the other hand, when a low voltage is stored at the Chold node, the M2 transistor is turned off and the lower EL electrode is effectively floating. In this case, the lower EL electrode voltage follows the drive voltage and results in no voltage across the EL pixel and, hence, no light emission.

With the use of this general AMEL circuit approach, two issues surface. The first issue is the need for a high voltage transistor, of about 250 V, that would fit into the 24 μm pitch required here. The 250 V is the peak voltage applied to the EL stack for light emission while the display pitch is only 24 μm and the whole circuitry needs to fit in an area less than 24 μm x 24 μm. The second issue involves minimizing the number of the components to allow all of the circuitry to fit into the pixel area while not sacrificing the stability or reliability of the EL device.

III.3 The High Voltage Transistor

The approach normally taken in AMEL applications is to use a circuit that fully blocks the high voltage EL drive (of about 250 V) for the off pixels. This approach results in the desired effect of the off pixels experiencing no voltage. The challenge associated with this approach is to fit the high voltage transistor and the associated circuitry within the pixel area. The theoretical breakdown voltage for Si is about 22 V/μm; this number reduces to about 15 V/μm in practical devices.[69] For 250 V EL excitation, this implies a separation of approximately 15 μm from any high to any low voltage point. Therefore, ignoring all other circuit components or design rules, a simple circuit would require a separation between pixels of over 30 μm (15 μm separation on each side of the high voltage contact). In actual practice (e.g., typical EL row drivers), the required silicon area per pixel for digital addressing circuitry, standard junction isolation, and the spacing required to separate low and high voltage points would allow a pixel pitch of only 100 μm, i.e. 250 lines/inch.[70] Obviously, the required size of this transistor (over 30 μm), precludes accommodation of the transistor and other circuitry within the 24 μm pixel area (i.e. above 1000 lines/inch).

The approach adopted in this work is to use the "modulation voltage" concept, already in use for passive matrix displays, in order to facilitate the use of a lower voltage transistor. The luminance-voltage characteristic of EL devices is non-linear, see Fig. 8.

The device is fully off for applied voltages up to about 180 V; such a voltage is typical of the threshold voltage. An EL device is defined as fully on when the applied bias is 40 V in excess of the threshold voltage, typically 220 V. In passive matrix EL displays, a typical high voltage of about 180 V, is applied to the rows. If the pixel needs to be on, a voltage is applied to the corresponding column to change the net voltage across the pixel to 220 V. Therefore, this approach allows the pixel state to be controlled by a column modulation voltage of only 40 V.

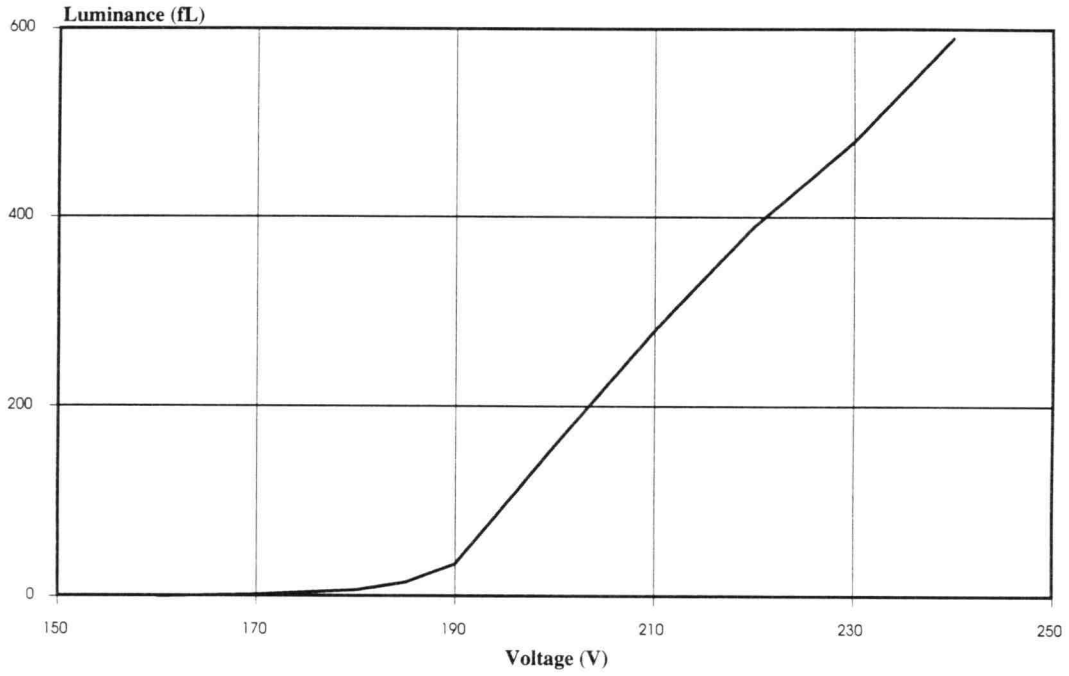

Figure 8: Typical L-V characteristic of an EL device subjected to a pulse voltage waveform at 1000 Hz.

Utilizing the same modulation voltage technique for the AMEL pixel, the high voltage requirement of the transistor is reduced. Instead of attempting to block off the whole voltage (about 220 V), only the modulation voltage (about 40 V) needs to be blocked off. Therefore, if the transistor can hold off this smaller voltage, the voltage across the pixel can be controlled from below threshold to the full on state. This lower voltage block is achieved with a zener diode in parallel with the transistor. In practice, a zener diode occupies additional silicon area and, therefore, is not practical. However, a high voltage transistor acts as a zener diode by breaking down when a high enough voltage is applied. This breakdown will not be catastrophic if the current is limited.

This "zener" transistor can be designed by lowering the voltage capability of the transistor to a level desired for the pixel operation.

The breakdown voltage of the transistor is defined by adjusting the drift region length, i.e. the separation length of the gate and drain of the high voltage transistor (see Section III.4). The rest of the transistor fabrication process can remain the same. To ensure the reliability of this device, the current in the high voltage transistor needs to be limited to below that of catastrophic breakdown of the transistor. In the design chosen for this dissertation, the EL device is used as the current limiting element. The 24 μm x 24 μm EL pixel results in a capacitance of about 150 fF. For the ac voltage waveforms used here, i.e. a 200 V, 10 kHz sine wave, the peak currents are:

$$i = C \times dV/dt$$
$$= (150 \times 10^{-15}) \times (200 \times \omega \times \cos(\omega t)) \quad \text{where } \omega = 2\pi \times \text{frequency}$$
$$\Rightarrow I_{peak} = 2\ \mu A$$

A transistor capable of handling a current of above 100 μA without undergoing catastrophic breakdown can be easily designed for operation at the desired breakdown voltage. Since the current is limited to about 2 μA by the EL capacitance, the high voltage transistor never enters into a destructive breakdown mode.

Based on the above discussion, the difference between a pixel's on and off voltage is determined by the transistor breakdown characteristics. Therefore, a higher breakdown voltage increases the difference between the on and off states. The approach utilized in this work to increase the transistor's voltage capability is to use SOI wafers for the IC processing. The SOI substrate allows isolation of the high voltage transistors by a grown or deposited silicon oxide layer under the active Si layer. This increased voltage capability is mainly due to the extra separation between the high voltage region and the common ground plane, i.e. the Si bulk. This separation from the common plane allows the high field to be more uniformly distributed.[71] Furthermore, use of SOI also allows for a lateral separation of the high voltage transistors by oxide trenches. This SOI approach allows much higher integration densities than obtainable from junction isolation or from the use of a semi-insulating (i.e. intrinsic) silicon substrate.[72] The desired transistor blocking voltage depends on the required modulation voltage and the pixel circuit design, as discussed in the next section.

III.4. Pixel Circuit Design

The discussion in the previous section focuses on a circuit approach which allows for the use of a lower voltage transistor which occupies less silicon area. The task of defining the pixel circuitry remains. The circuit must be simple enough to allow fabrication of all the components in a 24 μm x 24 μm area while not compromising the operation of the EL device. The simplest pixel design would be to employ one low voltage transistor for storage of data and only one high voltage transistor for control of the EL pixel; see Fig. 7. Not only is this the simplest approach but also this is the only design that permits achievement of the density goal of 1000 lines per inch. Utilization of this circuit design, especially after combining it with the "zener" transistor concept, leads to several concerns regarding the AMEL pixel reliability. These concerns include the brightness stability of the EL device due to the use of asymmetric drive voltages and the exact voltage requirement for the high voltage transistor.

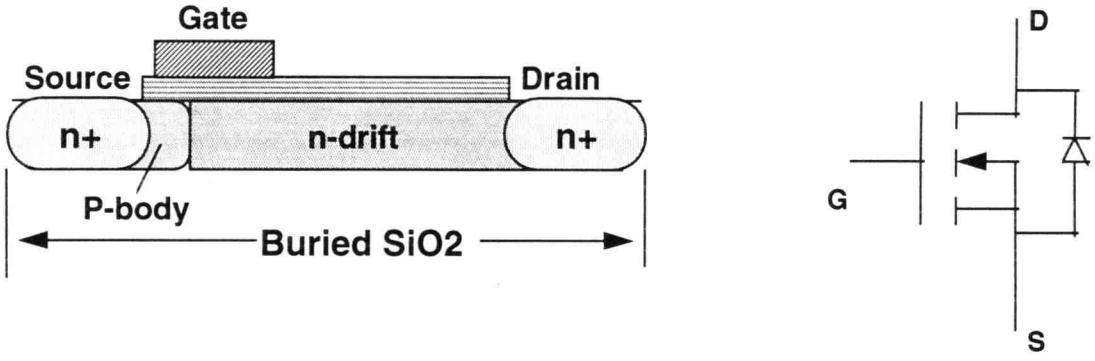

Figure 9: A cross-section and circuit schematic for a DMOS transistor.

The AMEL pixel circuit used in this work and shown in Fig. 7 results in an asymmetric voltage across the EL stack. The high voltage transistors used in this work are a double diffused MOS (DMOS) type. In DMOS transistors, the high voltage capability is achieved by dropping the voltage in a lightly doped region, denoted the drift region; see Fig. 9. This voltage drop allows for application of a high voltage at the drain contact while a low voltage of only 5 to 10 V is seen across the gate oxide. The n^+ source is shorted to the p-body by a separate conductor layer not shown in the cross-section of Fig. 9. This connection results in a p-n junction from source to drain, as represented in the circuit drawing of the DMOS transistor shown in Fig. 9. Due to this

body diode, only the positive voltage on the drain of the transistor is blocked.[73] When a negative voltage is applied to the drain, the diode turns on and clamps the drain voltage at the source potential. Therefore, with the transistor in an off state, the positive voltage is blocked, while for the negative voltage current flows from the grounded source and keeps the drain at a near-ground level. This operation clearly results in an asymmetric off voltage across the EL pixel for the circuit shown in Fig. 7. The consequences of such an asymmetric waveform are discussed in the following sections.

III.4.1 EL Device Operation

The operation of an EL device can be represented by a charge versus voltage (Q-V) plot. Such a plot indicates the amount of charge that flows to the EL device as a function of the applied voltage. For an "off" pixel, the Q-V plot (Fig. 10) is a straight line since below the breakdown voltage (i.e. the threshold voltage, Vth), the EL device acts as a simple capacitor, i.e. see the F-A-B line in Fig. 10.[74] After a sufficiently large voltage is applied, the phosphor layer breaks down and charge flows in the phosphor layer (resulting in light emission).

To understand the significance of the Q-V plot, the operation of the EL device subject to a symmetric voltage pulse, such as shown in Fig. 4a, can be followed. For on pixels, the magnitude of the applied pulse is a modulation voltage, Vm, greater than Vth. For the first segment of the voltage waveform, which is the positive pulse, the Q-V plot follows a straight line until Vth is reached (i.e. segment A-B in Fig. 10). At this voltage , the ZnS layer breaks down and acts as a conducting zener diode, increasing the device capacitance (i.e. point B in Fig. 10), see Fig. 11. This increase in capacitance is manifest as a change of the slope of the Q-V diagram at point B compared to the slope before breakdown, at point H, for example. For the initial positive pulse, the Q-V curve follows the A-B-C-D line in the Q-V plot, Fig. 10. When the applied voltage returns to zero, an internal charge is left on the ZnS layer, as shown by the non-zero value of charge at point D. This stored charge is a result of the transferred charge being trapped at the opposite interface. With a negative voltage pulse of magnitude Vth+Vm, the curve follows the D-E-G-H line. The change in the slope at point E signifies the initiation of conduction current through the ZnS layer and, hence, light emission. The lower turn-on voltage (Vto) at point E, compared to the threshold voltage (Vth) at point F, is due to the stored internal charge (i.e. the polarization charge). With the application of steady-state bipolar pulses of magnitude Vth+Vm, the Q-V curve follows the C-E-G-I parallelogram.

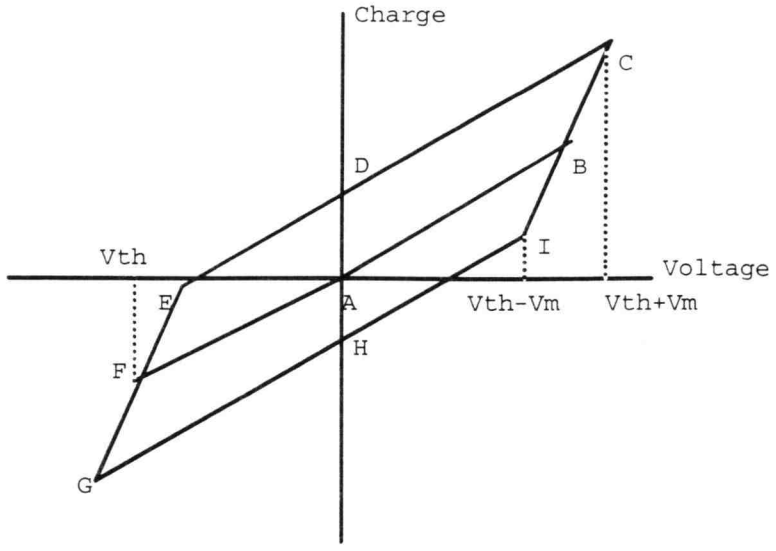

Figure 10: Charge versus voltage characteristic of an ACTFEL device.

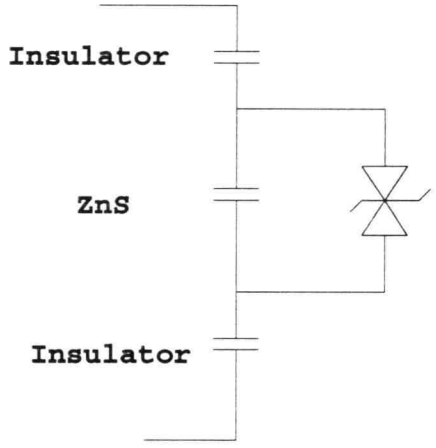

Figure 11: Electrical circuit model for the EL device.

III.4.2 EL Operation Using the Two-Transistor Pixel Circuit

In the case of the AMEL pixel shown in Fig. 7, asymmetric voltages are applied to the off pixel. The reason for the asymmetric voltage is the non-symmetric behavior of the DMOS transistor, as discussed earlier in this chapter. The pixel circuit is simulated using SPICE simulation. The parameters for M1 and M2 are based on experimental data.[75] The EL device parameters are also based on experimental data. The capacitance and breakdown voltages are estimated from capacitance-voltage plots for EL samples on glass substrates.[17,18] A summary of the parameters used is shown in Table 1. The SPICE file used is included in Table 2 while a schematic of the AMEL pixel circuitry, including the EL device electrical model, is shown in Fig. 12.[19-22] Note that these parameters and SPICE file are chosen in order to establish general trends, which is an adequate goal for the work in this dissertation. Further work is required to reach a fully acceptable DMOS model.

Parameter	Value
M1 threshold	0.9V
M1 length/width	2 μm/4 μm
M2 threshold	1.6 V
M2 length/width	2 μm/3 μm
ZnS breakdown voltage	140 V
ZnS capacitance	40 fF
Insulator capacitance	130 fF
Applied voltage	10 kHz sine, 240 V peak

Table 1: Summary of device parameters used for the pixel SPICE simulation.

```
.MODEL NE NMOS(LEVEL=3 VTO=0.929 TOX=6.5E-8 KP=1.9E-5 RSH=40
+ NSUB=1.0E16 XJ=1.0E-7 LD=5.0E-7 UO=6.5E2 GAMMA=1.0
+ VMAX=1.0E5 DELTA=0 ETA=0 KAPPA=2.9865E-1 TPG=1
+ CGSO=1.65E-10 CGDO=1.65E-10 CJ=1.0E-14 CJSW=1.0E-15
+ MJ=0.53 MJSW=0.1 PB=0.7)
.MODEL NH NMOS(LEVEL=2 VTO=1.58 TOX=5E-8 RSH=32016
+ NSUB=5.5E15 XJ=1.0E-7 LD=4.0E-7 UO=4.9E2 UCRIT=2.47E15 UEXP=1.2
+ CGSO=2.15E-9 CGDO=2.15E-10 CJ=2.0E-14 CJSW=2.0E-14
+ MJ=0.53 MJSW=0.1 PB=0.7)
.MODEL DZEN D (BV=100)
.MODEL DZEL D (BV=155)
.OPTIONS ITL5=1E6 RELTOL=5E-5 ABSTOL=5E-4
VNTOL=1E-6 LIMPTS=5E5 TRTOL=2.75 OPTS
```

Table 2: SPICE file for the AMEL pixel simulation.[75]

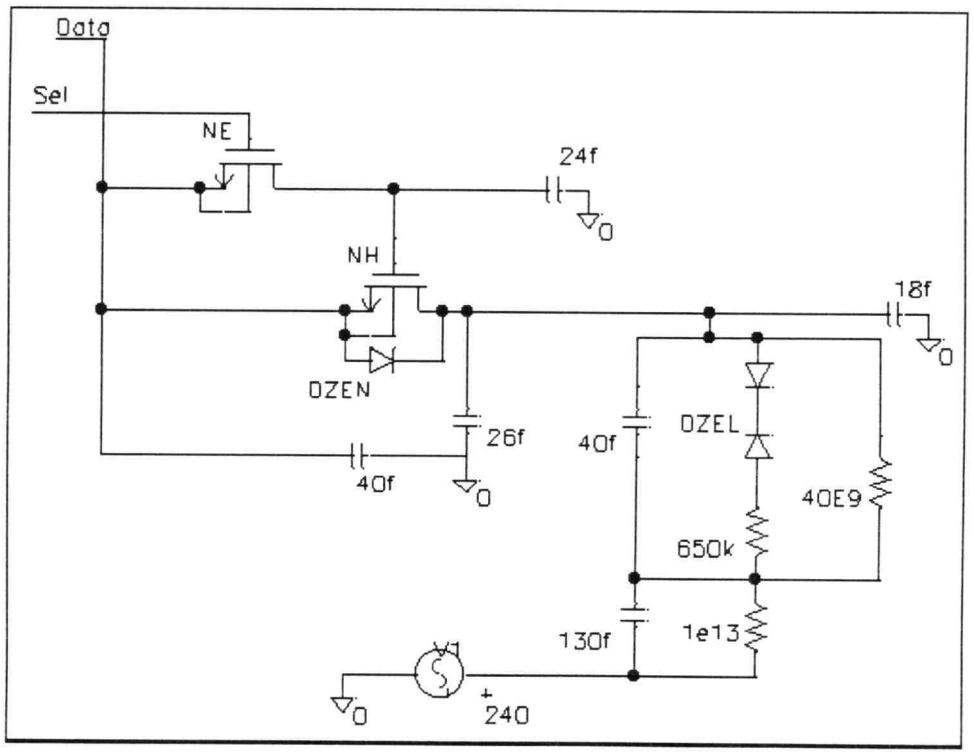

Figure 12: Circuit diagram for the AMEL pixel.

The waveforms resulting from the simulation are shown in Fig. 13. The three curves correspond to the applied voltage, which is the voltage applied to the common ITO connection, the voltage on M2, which is the blocked drain voltage of the high voltage transistor, and the EL voltage, which is the voltage that the EL pixel experiences. When the voltage at the drain of M2 (i.e. the blocking voltage) is large enough, the voltage across the EL device becomes small such that no charge flow in the EL device occurs, and, hence, there is no light emission. One result of the simulation is the clear asymmetric nature of the waveform across the off EL pixel. Since the transistor blocks only a part of the positive part of the waveform, the EL pixel experiences a reduced positive voltage but the full negative voltage.

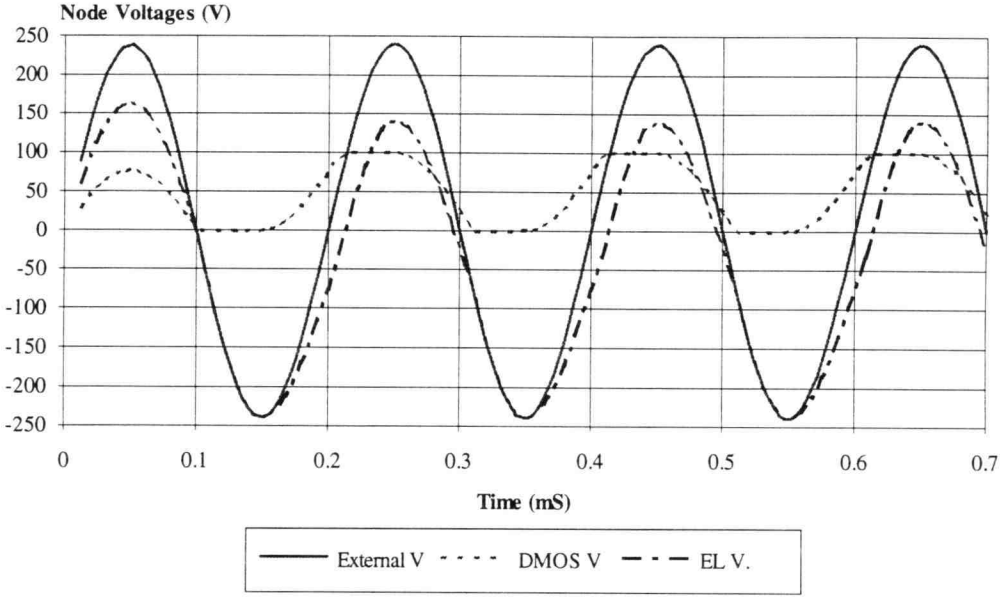

Figure 13: SPICE simulated voltage waveforms of an off AMEL pixel.
Note that EL V = Extenal V - DMOS V

For the EL device to be maintained in an off state, the voltage across the pixel needs to be kept below the turn-on voltage. For a positive voltage, this is achieved by simply having the M2 blocking voltage higher than the modulation voltage. However, the full amplitude of the negative pulse would normally turn the device on. Light emission during the negative pulse can be eliminated by decreasing the positive voltage across the EL device to Vth-Vm,[26,27] as explained in the following. Utilizing the Q-V plot (Fig. 10) again, the starting point for a virgin sample is point A. With the first

negative pulse of amplitude Vth+Vm, the curve follows segment A-F-G-H. The negative pulse is followed by a positive pulse of amplitude Vth-Vm. The positive pulse with this amplitude results in a Q-V curve which follows the segment H-I. Since the amplitude Vth-Vm is not large enough to breakdown the ZnS layer, there will be no charge flow in the ZnS and, hence, there will be no light emission. With subsequent pulses of positive amplitude Vth-Vm and negative amplitude of Vth+Vm, the Q-V curve follows the straight line G-H-I and corresponds to an off pixel.

Based on the above argument, the blocking voltage of M2 needs to be such that it results in a positive amplitude of Vth-Vm or lower. To reach the desired EL voltage of Vth-Vm with an applied voltage of Vth+Vm, the transistor is designed to block twice the modulation voltage. For the case simulated in Fig. 13, the blocking voltage of M2 is 100 V (2 x Vm) resulting in a positive voltage across the EL stack of Vth-Vm (140 V) while the negative EL voltage is the full external voltage of magnitude Vth+Vm (-240 V). For this EL waveform (with a voltage magnitude of positive Vth-Vm and negative Vth+Vm), the Q-V plot follows the segment G-H-I in Fig. 10. The M2 breakdown voltage can be adjusted for a trade-off between the off pixel brightness and the transistor size. For example, increasing the size of the transistor to allow for a blocking voltage larger than 100 V would result in the amplitude of the positive voltage for the off state to further decrease. This lower positive voltage would result in the pixel becoming more "off" and emitting less light. The lower positive voltage for off pixels has the additional advantage of ensuring that pixels remain off even with some IC or EL processing variations.

III.5. Stability of the EL Device

As discussed in the previous section, the voltage across the EL device is not symmetric for the pixel circuit design employed. The use of asymmetric pulses to drive ACTFEL devices has been demonstrated to degrade the aging stability of these devices. This relationship between the use of asymmetric drive and device instability is strong enough that it has forced commercial manufacturers to move to fully symmetric EL drivers.[76,77]

To evaluate the brightness stability as a function of aging time when using an asymmetric voltage waveform, several experiments are performed. The first test involves a standard pulse, as shown in Fig. 4a, with a small DC voltage continuously applied to the pixel. The experiment is repeated with bias voltages ranging from 2 V to 15 V. The devices are evaporated ZnS:Mn EL devices with sputtered SiON insulators

on a glass substrate. The result shows that any bias voltage above 5 V results in an excessive brightness instability. A second experiment is performed on the same type of device by aging the test sample with a positive pulse larger in magnitude than the negative pulse. The results are similar in that the aging is severe, even when the magnitude of the positive and negative voltage pulses only differed by 5 V.

In the AMEL pixel design, options for making symmetric voltages for off pixels are limited. The only direct approach to ensure that a symmetric voltage is applied to the EL device would be to add a second transistor to block the voltage in the opposite direction. This is not a desirable approach due to a combination of pixel area constraint and processing considerations. An additional high voltage transistor would double the required area and would not fit in the 24 μm pixel pitch, even if the zener-transistor approach is used. Furthermore, the additional transistor would require additional IC processing which would substantially degrade the final device yields. Therefore, for a successful display, a design using one high voltage transistor, as shown in Fig. 7, remains the optimal one.

The common explanation for EL device aging, and the drive electronics solutions to circumvent aging, rely on the explanation that the electric field in the EL device modifies the charge distribution in the ZnS layer.[12-14,16,78-80] This explanation then implies that to avoid aging problems all the waveforms for on and off pixels need to be symmetric.[16,76,77] Explanations for aging such as sulfur vacancy migration,[16] are consistent with the instability observed in association with the asymmetric voltages, as described in the beginning of this section. The improvement in device operation observed by making the voltage waveform symmetric in the commercial displays also support this assertion.[76]

Several experiments are performed to evaluate the assumption that waveform symmetry is required for the chosen AMEL pixel design, as shown in Fig. 7. The relationship between voltage asymmetry and instability is of great important since in this pixel design, the off pixels experience a very asymmetric voltage, as shown in Fig. 13. Surprisingly, **the experiments show that, unlike for on pixels, waveform symmetry is not required for the off pixels to assure that device stability is achieved.**

The first experiment involves the use of standard, evaporated ZnS EL devices with sputtered insulators on a glass substrate. The applied waveform is modified to be only a series of positive pulses with an amplitude of 40 V above the device threshold voltage. In the presence of a negative pulse of the same magnitude, the device would normally emit light; however, with this unipolar waveform, no light emission is seen since after the first pulse the charge is simply accumulated at one interface. This

unipolar waveform is chosen since it is an extreme case of asymmetry. The luminance-voltage (L-V) behavior of this device is measured before the start of the experiment. Then the unipolar pulse is applied at a frequency of 1000 Hz. The L-V curve is measured using the standard bipolar waveform initially and after 1 hour, 3 hours and 10 hours of aging. No change in the L-V characteristics is observed.

A second experiment is performed using the AMEL waveforms, as per the simulation results shown in Fig. 13. The EL device for this experiment is fabricated using the ALE process so that this experiment is more representative of the operation of an actual AMEL device. The substrate for this experiment is again glass. The EL voltage waveform for an off pixel, as shown in Fig. 13, with a positive voltage of 50 V below Vth and a negative voltage of 50 V above Vth, i.e. a 100-V asymmetry, is applied to the test device. As expected, the pixel remains off for the aging period. A standard pulse waveform is used to measure the L-V characteristics at 0, 1 hour and 10 hours of aging. Again no change in the luminance characteristics of this device is observed.

Based on the results of these two experiments, it is concluded that asymmetry of the applied voltage waveform for an off device does not result in instability problems. This conclusion, in turn, implies that the AMEL device with one high voltage transistor will not exhibit instability problems associated with voltage pulse asymmetry. Therefore, the design illustrated in Fig. 7 is used for the work described in this dissertation.

With regard to the instability mechanism, this finding implies that the postulation that the migration of charged centers, such as sulfur vacancies, due to the internal field is the source of the instability does not explain the aging behavior as previously thought.[12,13,16] If the migration of charged center by the internal field is the source of instability, a large asymmetry in the field should result in a higher rate of brightness change during the device operation. However, observing that light emission is required for aging supports the postulate that hot electron transport is required for the EL aging to occur. The hot electrons could assist in ion migration or could change the interface distribution of traps and cause the observed aging behavior.

III.6. Pixel Circuit Timing

One remaining concern inherent in the circuit design used in the work described herein is that the illumination pulses can be applied only when the data is not being written. This creates a problem which is related to the use of a data line for connection

to the sources of both the low and the high voltage transistors. The pixel circuit operation requires storage of the appropriate voltage at the Chold node; see Fig. 7. The state of the pixel depends on the voltage between the gate and source of the high voltage transistor, M2. Since the M2 source is connected to the data line, the gate-source potential changes while data is being written to other lines in the display. Therefore, the EL control would change if the illumination and addressing occur simultaneously.

This concern is resolved by separating the addressing time from the illumination time, i.e. storing the data for all the pixels in the display and then applying the common ac voltage. The solution of separating the timing allows the source of the DMOS transistor to be grounded via the data line when the high voltage is applied. This separation in time reduces the available time for both illumination and addressing. However, this reduction in available time does not affect the operation of the AMEL device significantly and all the display goals can still be achieved. Therefore, the AMEL pixel is implemented as shown in Fig. 7.

In future designs, a simple solution to this timing constraint is to connect the M2 high voltage transistor's source to a ground plane as shown in Fig. 14.[28] This connection to ground can be made by a via to the existing ground shield plane. This circuit modification will allow a complete separation of the addressing path, which is through select and data lines, from the illumination path, which follows the external ac drive through M2 to ground. The separate paths will allow a continuous ac drive for EL illumination while the addressing is ongoing. Furthermore, since the high ac currents no longer have to be sunk by the data drivers, the restrictions on data-line circuitry and line resistance are reduced. This design is not used for the work described herein due to the desire to have a very simple circuit with minimal connections and components.

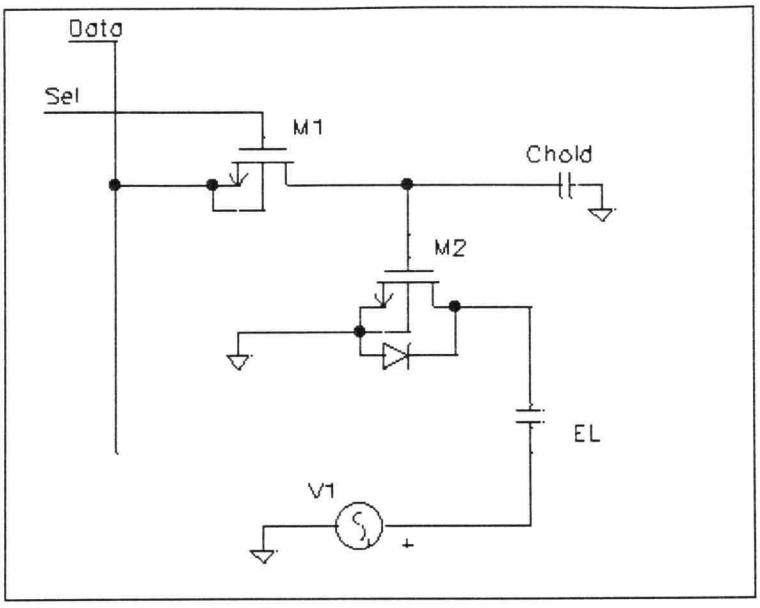

Figure 14: Grounded high voltage DMOS transistor used to separate the illumination voltage from data path.

III.7. The Gray Scale Approach

The standard gray scale approaches used for EL displays are reviewed in Chapter 2. Previous AMEL research has not dealt with the issue of gray scale due to the infancy of the AMEL approach to date. In general for EL displays, it can be said that a method of achieving gray scale is desired that maintains the operation of the EL device with full charge flow across it. Full charge flow allows for optimal performance in brightness uniformity across the display and in long-term display stability. Analog approaches, such as amplitude modulation and pulse width modulation, do not have this characteristic. It would be possible to build the AMEL display based on one of the existing gray scale approaches; however, since AMEL displays are completely new, the potential for improved gray scale approaches exist and are investigated, as described below.

III.7.1. Limitations of Traditional Gray Scale Approaches

In addition to the disadvantages mentioned for analog approaches, the AMEL architecture introduces new limitations. One of the first AMEL-specific disadvantages is that a larger area for the data and select line drivers in the periphery of the display is

required. For example, in an amplitude modulation approach, an analog voltage needs to be stored at each pixel. This requires an analog-to-digital converter (ADC) circuit to be available for each column. Utilization of an ADC for each column, and the attainment of a high pixel pitch, is a difficult task which requires a complex design. The addition of such a circuit is possible only if more peripheral area is sacrificed; however, this is not desirable for HMD applications where a minimum display size is required.

A second limitation of the analog gray scale approach is that of high voltage coupling from the EL electrodes, which are subjected to voltages in excess of 100 V. The low voltage circuitry that stores a voltage less than 10 V needs to be shielded from the high voltage EL drive. The high voltages can easily couple to the storage node, i.e. Chold in Fig. 7. This coupled voltage can cause voltage changes, resulting in a change of the stored data. For example, in a 64-level gray scale system using 10 V storage for the maximum gray level, each linear gray scale step corresponds to about 150 mV (10 V/64). To avoid a change in the gray level, the voltage stored at the pixel needs to stay at the original voltage with a less than 150 mV change. In another words, this stored voltage needs to be shielded from voltage swings of about 100 V seen at the lower EL electrode. Such a requirement implies reducing the voltage coupling to less than 1000 to 1, which, in turn, implies a capacitive ratio of 1000 to 1 which is impractical for normal IC processing.

Yet another issue of relevance for the use of standard analog gray scale approaches in AMEL displays is related to the driving approach used in the pixel design. The EL control is achieved in the AMEL pixel design by the storage of an appropriate voltage at the gate of the high voltage transistor. This stored voltage controls the drain current of the high voltage transistor. The relationship between the gate voltage and the drain current is very non-linear (actually, it is close to exponential). Therefore, linear current control of the output requires control of the gate voltage in a logarithmic manner. This logarithmic gate voltage control requirement means that a very small noise (much lower that 150 mV, as calculated earlier) coupled to the stored data can lead to a change in the gray level. Besides noise considerations, simply writing the voltage to the desired degree of accuracy is an impractical task.

A final issue with regard to the use of analog approaches for the attainment of the gray scale is the non-uniformity of the transistor characteristics across the device. The operation of an analog circuit relies on transistor parameters such as threshold voltage, Vt, and drain currents, Id. A reliable analog design needs to rely only on relative device parameters in order to remain functionally independent of always present processing variations. However, in EL analog gray scale approaches, the voltage stored at the pixel

is an absolute voltage which is dictated by the system input. The same voltage has different effects on the EL pixel operation, depending on the value of Vt and Id at the pixel location on the wafer. Therefore, to pursue an analog approach, the processing has to be done such that Vt and other transistor characteristics remain constant to within 2% across the display. This is an impractical constraint to impose on any circuitry processed on bulk silicon; it is an impossible requirement when SOI substrates are utilized. The concerns enumerated above motivated a search for an alternate approach to the achievement of gray scale operation.

III.7.2. The Temporal Gray Scale Approach

As discussed in Section III.2, the normal addressing scheme used for standard EL matrix displays is a line-at-a-time technique where the illumination occurs only once per frame time. As before, the frame time is defined as the time between consecutive refreshing pulses of the data on a pixel in the display. In the line-at-a-time approach, the maximum illumination frequency is limited by the time required to update the data for all the pixels. However, in AMEL addressing, the addition of a low voltage storage transistor and a high voltage transistor allows separation of the low voltage addressing function from the high voltage illumination pulses. This separation allows the data to be transferred to the pixel at low rates while the pixel illumination occurs at high frequencies in order to achieve the desired brightness levels.[30,31,68]

The basic concept of the "temporal" AMEL gray scale approach pursued in this work involves controlling the number of pulses applied to the pixel during each frame time. The brightness of the EL device depends on the number of the pulses applied to it. In this time-domain gray scale approach, the frame time is divided into several "sub-frames". The number of sub-frames is the same as the number of gray scale bits desired. In each sub-frame, the pixels are controlled to be either on or off. After writing the data, the high voltage pulses are applied. The number of pulses applied depends on the brightness desired for the corresponding gray scale bit.

To clarify this approach, an example of a 4-bit (i.e. 16-level) gray scale is presented. For this case, the frame time is divided into 4 sub-frames. The data is written for the most significant gray scale bit (MSB) during the first sub-frame, followed by the other bits, until the least significant bit (LSB) is written last. After the data is written to

the whole screen in each sub-frame, the illumination pulses corresponding to the desired level are applied. For example, after the MSB is written to the whole screen, 8 pulses are applied. This process continues for the other bits until the LSB is written, which is followed by one pulse. The timing is illustrated in Fig. 15.

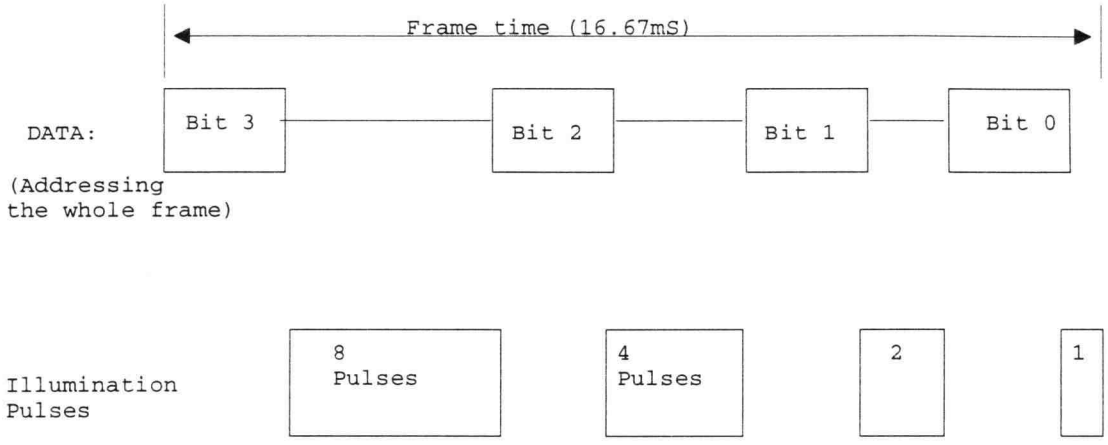

Figure 15: An example of gray scale timing for a 4-bit system.

III.7.3. Possible Variations of the Time-Domain Gray Scale Approach

The discussion in the previous section covered the basic time-domain gray scale approach. This approach allows control of the brightness for each bit separately. The illumination pulses following each gray level bit can be customized externally to provide the desired brightness. This flexibility is attractive, especially for applications that require non-linear brightness-gray scale characteristics. There are several variations of the time-domain approach possible:[30,31]

A. Timing: The illumination and addressing can be simultaneous or separated in time, depending on the time allotted for each gray level bit. In the work described in this dissertation, a separated case (as shown in Fig. 15) is pursued. This choice was dictated by circuit design and timing limitations, as described in Section III.6.

B. Order: The gray bits do not have to follow any specific order. The order chosen here, as shown in Fig. 15, is from MSB to LSB; however, the order is

controlled by the system and its choice does not diminish the performance of the display.

C. Gray level brightness: The brightness for each gray level can be independently controlled. This control can be accomplished through a variety of standard gray scale techniques including the number of pulses, amplitude, pulse width, or frequency of the waveform applied in each sub-frame. The brightness control chosen for this work is the amplitude for the LSB and the number of pulses for the higher bits. As illustrated in Fig. 15 for a display using the number of pulses to achieve 4-bit gray scale, the MSB corresponds to 8 pulses followed by other bits down to the LSB which corresponds to a single illumination pulse.

For the work described in this dissertation, the number of gray levels is 64, i.e. 6-bits. Therefore, each frame time is divided into 6 sub-frames corresponding to the MSB to the LSB. In each sub-frame the corresponding data bit is written for all the pixels. After the entire screen is updated with the data bit, illumination pulses are applied to turn the display on to the appropriate brightness. For example, for the linear gray scale approach developed herein, the MSB sub-frame addressing is followed by 16 pulses (each pulse defined as a period of sine wave). The bit 0 sub-frame addressing is followed by one pulse with a lower amplitude to achieve one half of the luminance resulting from a pulse with the full amplitude. The bit 1 EL drive contains one pulse at the fulll amplitude followed by other gray bit sub-frames having 2, 4, 8, and 16 pulses at the full amplitude. This approach results in the MSB sub-frame to correspond to a luminance level 32 times the luminace corresponding to the LSB sub-frame.

III.8. Overall Display Organization

Earlier in this chapter, the basic AMEL structure and the pixel circuitry are described. To improve the performance of the display for HMD applications, the circuitry that provides the select and data signals is fabricated on the same silicon substrate. Integration of these drivers, and the associated digital controls, reduces the size of the display and also allows a minimal number of interconnects to the external system. Instead of connections to each row and column, with integrated drivers only the data and control signals need to be delivered from the system. In summary, the overall organization of the AMEL display pursued in this dissertation is shown in Fig. 16. The

input signals from the system include the desired data and control signals as well as the high voltage ac signal.

In this chapter issues and solutions related to AMEL pixel circuitry and gray scale have been discussed. In the next chapter, fabrication details of the EL device appropriate for AMEL use are reviewed. The final results of this AMEL work are discussed in Chapter 5.

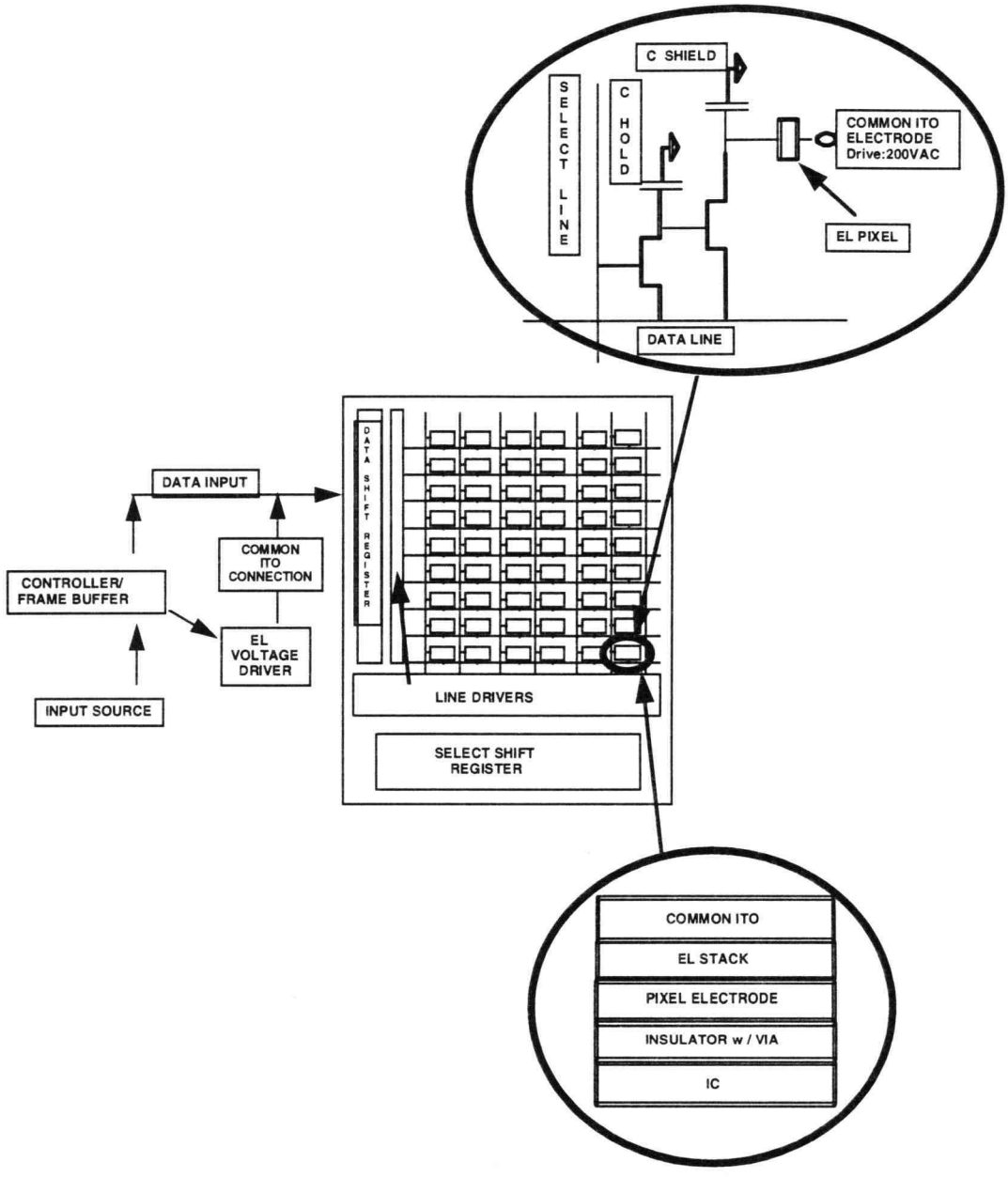

Figure 16: AMEL display organization.

Chapter IV. THIN FILM DEPOSITION

AMEL functionality can be divided into two categories: display electronics and EL thin-film operation. In the previous chapter, the display electronics approach is discussed. As presented in Chapter 1, Fig. 1, the IC processing is accomplished on the Si substrate prior to the EL deposition step. To achieve a functional AMEL display, the nature and process technology used for deposition and patterning of the EL thin-film on the Si substrate is optimized. The EL thin-film deposition process is further modified to preclude any damage to the completed IC. Finally, the high brightness and high resolution goals affect the choice of the EL thin-film. In this chapter, performance and processing issues are reviewed and the EL thin-film approach pursued in this work is described.

IV.1 EL Thin-Film Requirements for AMEL Displays

The use of a silicon wafer instead of the standard glass substrate requires new considerations for EL processing. The first issue is that the emitted light now has to be viewed from the EL film side due to the use of an opaque silicon substrate. In standard EL displays, light is viewed from the substrate side since a transparent glass substrate is used. In the AMEL case, since the light emerges from the EL film side, a new EL stack structure with a transparent top electrode is required. In a standard display, a defect in or under the EL film can be "fused" by the use of metals, such as Al, as the top electrode. Defects cause shorts between the Al electrode and the bottom electrode. With the application of a high voltage pulse, a large current flows through these shorts which results in local heating, a so-called burn-out. The large amount of heat dissipated concomitantly with the flow of a large current causes the Al metal to evaporate in a region near the defect, thereby isolating the defect and preventing the burn-out from being catastrophic to the pixel. This type of non-catastrophic burn-out is referred to as a self-healing burn-out which can be observed visually as microscopic, opaque spots on the pixel. Due to the small size of these localized burn-out spots, they are not resolved by the viewer when the pixel is turned on. However, the opaque Al metal, which allows self-healing breakdown to occur, cannot be used in AMEL displays.

The problem with using a standard EL structure in which light is emitted from the film side is that transparent electrodes, such as indium tin oxide (ITO), with typical thicknesses of at least 500 Å, do not exhibit this fusing characteristic. Thus, catastrophic

breakdown occurs when defects are present in the thin-film if ITO is the top electrode. Evaporated and sputtered TFEL devices possess defects and are prone to self-healing breakdown if an upper Al electrode is employed. In contrast, ALE TFEL devices do not exhibit similar breakdown problems and, therefore, appear to be comparatively defect free. Due to this fact, an approach based on the use of ALE is preferred. Researchers at Planar International have developed an EL structure in which light emission is viewed from the last-deposited, i.e. top electrode.[50] This structure, denoted as an inverted structure and described in Section II.4, is based on the use of ALE for the deposition of the EL thin-film. The ALE approach has proven to yield a minimal number of defects, even for large-area displays. The lack of these defects removes the need for fusing Al electrodes and allows for the use of the inverted structure.

A second reason for the use of ALE as an EL thin-film process technology is its conformal coating capability. This characteristic is important due to the rough topography created by high resolution IC processing which results in sharp edges on the Si surface. These edges lead to high electric field regions. In addition, these edges would be of non-uniform thickness if not coated conformally in the first place. In the AMEL displays discussed in this dissertation, the ALE deposition technique is utilized to allow a conformal film, as discussed further in Section IV.2.

Another issue in regard to the use of silicon substrates is the mismatch between the coefficient of thermal expansion (CTE) of silicon and the EL thin-film stack. The reported silicon CTE is approximately 4 $x10^{-6}/°C$,[81] while CTEs for the EL thin-films are expected to be much higher. Since the EL thin-film exhibits good thermal matching to the soda lime glass substrate, the CTE of EL ALE films is expected to be approximately 6-8 x $10^{-6}/°C$. During high temperature deposition of the thin-film or during subsequent thermal annealing, a large difference in the CTE causes stress in the thin-film stack. The EL thin-film structure is modified in this work, as described in Section IV.3, to provide for a low-stress EL thin-film on top of the silicon substrate.

IV.2. The Use of ALE Thin-Films on the Processed IC Wafer

As mentioned in the previous section, ALE processing is chosen for AMEL display fabrication to allow for conformal coating and for the use of an inverted structure. The ALE process relies on the achievement of saturated monolayer coverage on the substrate surface. As per the discussion in Section II.3, Zn is introduced as $ZnCl_2$ to the surface of the substrate. Then S is introduced using H_2S gas. This gas reacts with the

$ZnCl_2$ leaving ZnS on the substrate and releasing HCl vapor as a byproduct. This sequential process continues on a saturated monatomic layer basis until the thin-film deposition is completed. Dopants are introduced in a sequential, gas phase manner, normally using a Thd (Tri-tetra methyl heptane dionato) compound as the dopant gas. ALE deposition is ideal for meeting the conformal coating and low defect density requirements necessary for the achievement of an inverted structure.

The conformal coating requirement is of crucial importance given the rough surface texture of the Si substrates used in this work after IC processing. To achieve the desired AMEL system functionality, the IC process flow includes 4 conductor layers and vias with a near 1 μm depth and a 2 μm width. To keep the pixel size to a minimum, the electrode and silicon patterning is performed in a manner which leads to surface features with sharp edges. Therefore, IC processing results in a very rough starting surface upon which the EL thin-film must be deposited. The conformal coating capability of the ALE process allows for excellent step coverage of sharp edges. Without this type of step coverage, the thinner portions of the thin-film near edges would breakdown under high applied voltages and, thus, would severely degrade the device reliability.

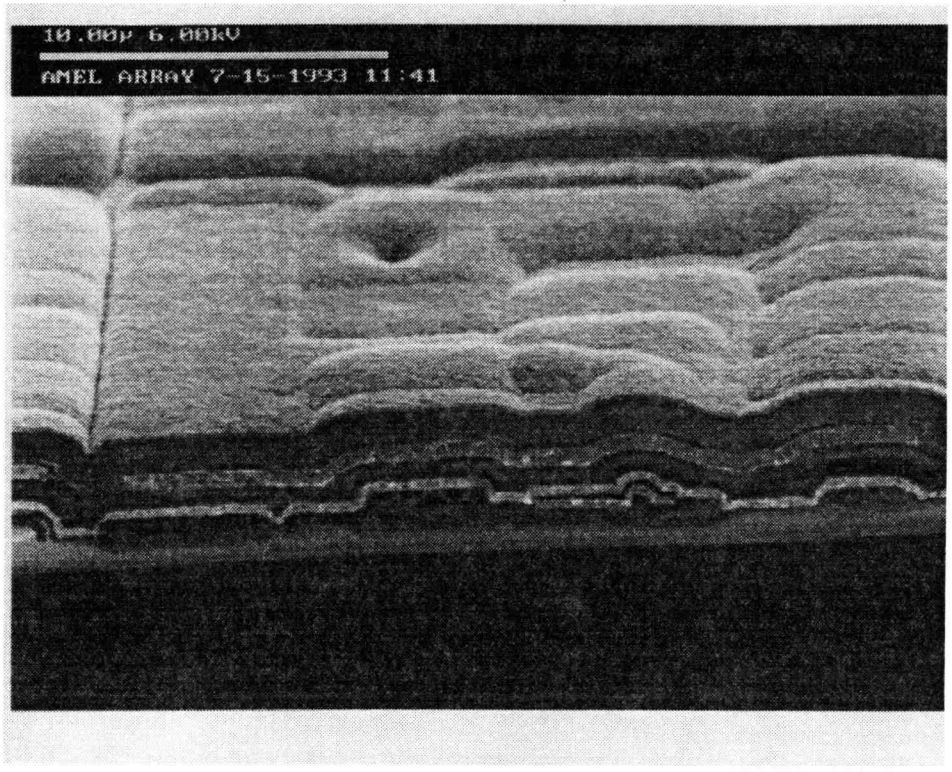

Figure 17: Cross-sectional SEM micrograph of a completed AMEL display.

To evaluate ALE capability for conformally covering the substrate topography, several tests are performed. These experiments include the use of glass substrates and silicon wafers with patterned first conductors. The devices deposited onto glass substrates are operated and stressed with high ac voltages and are found to survive voltages in excess of 250 V. EL thin-films are then deposited onto an IC processed Si substrate. A cross sectional SEM micrograph of such a completed AMEL structure is shown in Fig. 17.[82] As can be seen from this picture, the ALE EL thin-film has conformally covered all the steps with no gaps to allow breakdown.

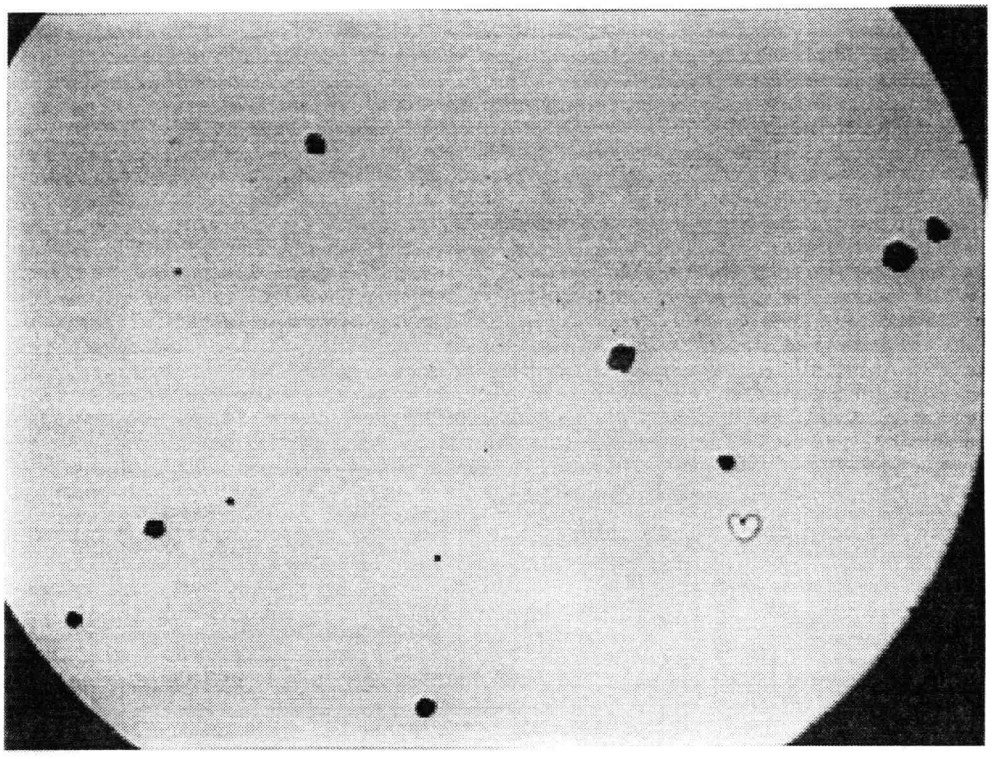

Figure 18: Photograph of an EL device with an Al top electrode exhibiting fusing (65X).

The other requirement for an EL thin-film is that it be defect-free to allow for the use of an inverted structure on the Si substrate. The ALE fabrication process meets this requirement, as evidenced by the thousands of large area ALE displays produced annually at Planar International. In contrast, films fabricated by sputtering or evaporation possess microscopic particles and voids. These kinds of defects do not affect the visual appearance of the display or its operation since they are fused at an early stage and remain

microscopic. A photograph of pixels showing this fusing action is included in Fig. 18. Such a self-healing effect is not observed in inverted structure films. A burn-out in the ALE inverted structure EL thin-film does not fuse and, thus, precludes an operational display. An example of such a burn-out is shown in Fig. 19. In summary, the successful operation of inverted-structure AMEL devices indicates defect-free EL thin-films, suitable for inverted- structure applications, may be fabricated by ALE.

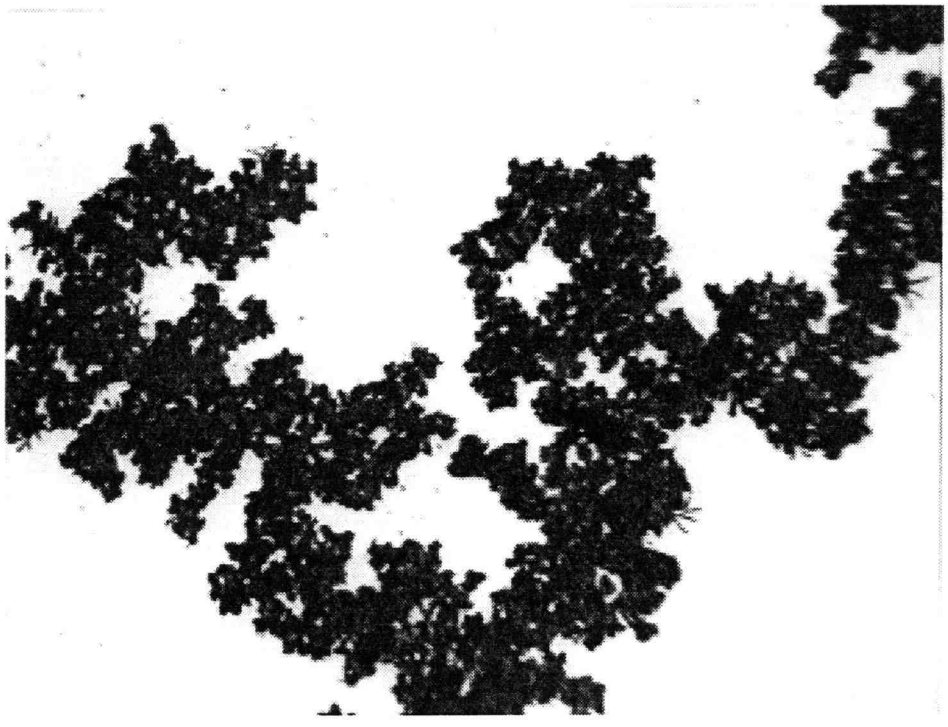

Figure 19: Photograph of an ALE EL device exhibiting catastrophic burn-out (65X).

IV.3. Stress in EL Thin-Films on Silicon Substrates

As mentioned previously, a fundamental problem associated with depositing an EL thin-film on top of Si is that the CTEs of the EL thin-films and the Si are very different. For Si, the CTE is approximately $4x10^{-6}$ /°C [81] whereas the CTE for the EL thin-film is about 2 times higher than that of Si. This large CTE difference causes film stress. Such a stress problem exists for all fabrication techniques. ALE deposition is normally performed at a high temperature of about 500 °C. Since the EL film shrinks more than the adjacent

Si substrate when cooled, the final EL thin-film at room temperature is under a tensile stress. This tensile stress results in film separation, i.e. film cracking, as shown in Fig. 20. The burn-out caused during the operation by the film cracking is also shown in Fig. 20. The evaporation or sputtering approaches provide the option of depositing the EL films at lower temperatures, in the range of 200 °C. These low temperature deposited films do not show stress-induced defects after deposition; however, these processing techniques require a thermal anneal step subsequent to deposition to improve the brightness. Thermal annealing is normally accomplished above 450 °C. For post-deposition thermal annealing, since the EL thin-film expands at a greater rate, a compressive stress is developed when the film reaches the high annealing temperature. Such a compressive stress results in film buckling, which is also detrimental to the operation of the device. An example of an EL thin-film, with an evaporated ZnS phosphor and sputtered SiON insulators, under compressive stress is shown in Fig. 21. The remainder of this section focuses on solving the stress problem of ALE thin-films deposited on Si substrates.

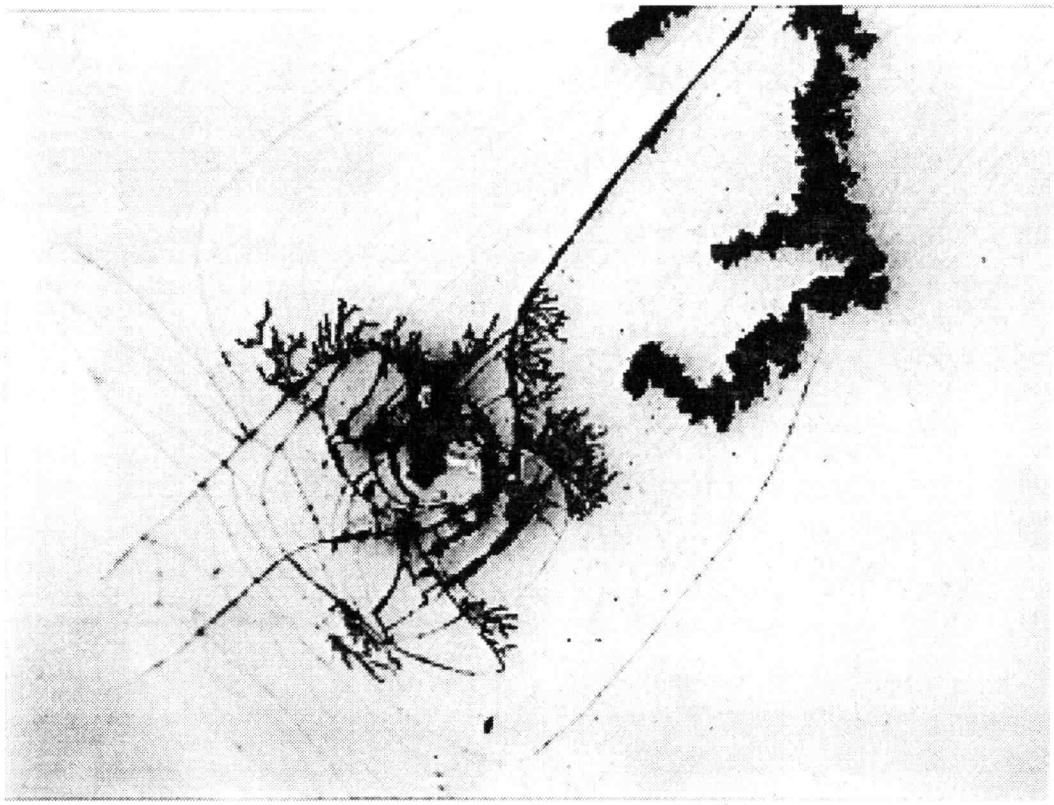

Figure 20: Cracking of an ALE-deposited thin-film (65X).

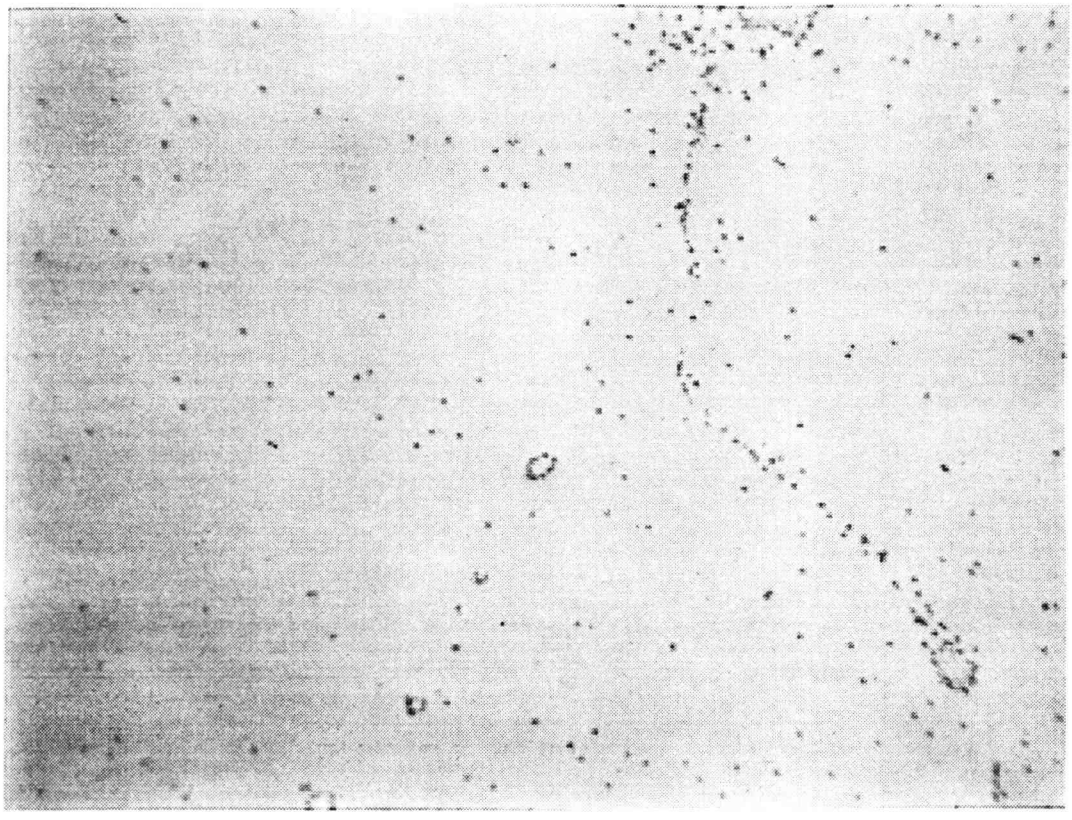

Figure 21: Buckling in an evaporated EL thin-film after the anneal step (65X).

The total stress in a thin-film is a combination of three factors:[83]

Stress (σ) = $\sigma_{ext} + \sigma_{int} + \sigma_{th}$

where σ_{ext}: any external stress

σ_{int}: intrinsic stress due to the film structure

σ_{th}: thermal stress imposed by film-substrate bonding

$= (\alpha_f - \alpha_s) * \Delta T * E_f$

α_f , α_s : CTE of film and substrate

ΔT : difference between deposition and measurement T

E_f : Young's modulus of the film

In the case of AMEL device fabrication, the factors of interest involving thin-film stress and which can be controlled are the thermal stress, σ_{th}, and the intrinsic stress, σ_{int}. As the final equation above shows, the thermal stress directly depends on the CTE

differences and on the deposition temperature. The intrinsic stress is a less well understood factor which depends on the deposition parameters.[83]

IV.3.1 Reducing the Thermal Stress

To reduce the thermal stress, the first approach taken is to reduce ΔT by lowering the deposition temperature. The normal deposition temperature for the ALE insulators, composed of a multi-layer of Al_2O_3 and TiO_2 layers, and denoted as ATO, is 500 C. The deposition temperature is reduced to 450 °C, which is the same deposition temperature as that used for the ZnS layer. It was anticipated that the lower deposition temperature may cause reliability problems due to the possibility of enhanced chlorine trapping in the thin-film from the $AlCl_3$ reactant. However, the 50 °C decrease in deposition temperature did not lead to any noticeable problems in terms of optical measurements of completed EL devices or with respect to index of refraction and dielectric constant measurements of the ATO thin-films.

A second method pursued for reducing the thermal stress is to modify the film's CTE, α_f, to a value closer to that of the substrate. Since the choice of a Si substrate and its CTE is set, the only modification possible is to reduce the CTE of the EL film. The EL film is compromised of three primary materials: ZnS, Al_2O_3 and TiO_2. The relative CTE for each of these ALE films was not found in the literature and, thus, needed to be measured, as described in the following section.

IV.3.2 Measurement of the Stress of the EL Thin-Film

To evaluate the stress of the constituents of the EL thin-film, three separate standard films are evaluated initially. Since the goal is to reduce the stress, only relative stress values are measured. The test silicon wafers are first measured using a commercial laser wafer-flatness measuring system.[84] This base line measurement is used as a correction to the stress measured on the Si wafers coated with the EL thin-film stack. The first three films investigated are ZnS, Al_2O_3, and ATO. Stress in TiO_2 is inferred from a difference of the measured stress of ATO and Al_2O_3 thin-films; it is not measured directly since it is known that TiO_2's physical characteristics drastically change as a function of its thickness.[85] The results of these stress measurements, in relative units, are included in Table 3. The results show that the TiO_2 film has the largest CTE mismatch. To improve

matching to the silicon substrate, the TiO_2 thickness needs to be reduced. This goal is achieved by increasing the Al_2O_3/TiO_2 thickness ratio by about 20% while keeping the total ATO thickness unchanged.[86] The number of TiO_2 deposition cycles in the ATO is reduced from 100 cycles to 60 cycles for every 120 cycles of Al_2O_3. The stress of the re-engineered film is then measured. The stress measurement indicates a dramatic improvement, as shown in Table 3.

Material	Structure	Relative stress
ZnS	213 Å of Al_2O_3 for starting surface 7550 Å of ZnS 107 Å of Al_2O_3 for protection	1
Al_2O_3	1750 Å	0.6
Standard ATO	1600 Å	2.4
Modified ATO	1600 Å	1.6

Table 3: Stress measurements of EL thin-films deposited onto Si substrates.

IV.3.3 Reducing the Intrinsic Stress

Further improvement in the total stress is achieved by reducing the intrinsic stress. As mentioned earlier, this stress component is dependent on the processing conditions such as the deposition rate, pressure, film preparation prior to deposition, and film thickness.[83] Modification of most of these processing conditions, without an adverse effect on the display operation, requires extensive experimentation. The simplest parameter to modify is the film thickness. To improve the brightness as well as to reduce the intrinsic stress, the thickness of the ATO insulator is reduced while the ZnS thickness is set at 6000 Å. For the work reported here, the ATO thickness is reduced to 1900 Å from a standard value of 2700 Å. This reduction did not result in any reliability problems for the voltage range of interest, i.e. maximum voltages below 250V.

After decreasing the deposition temperature, modifying the ATO structure, and reducing the ATO thickness, the EL devices are repeatably deposited onto Si substrates without any evidence of cracking problems. Furthermore, these films are subjected to a

rapid thermal anneal (RTA) for 2 minutes at 720 °C without any sign of stress-related problems.

IV.4. The Choice of ALE Green

The previous section lists reasons for choosing the ALE approach, as well as enumerates the modifications required for the use of ALE thin-films on Si substrates. Currently, there are three ALE phosphor thin-films readily available. These three ALE phosphors are ZnS:Tb for green, ZnS:Mn for yellow, and ZnS:Mn/SrS:Ce for white. Based on optical requirements, ZnS:Tb phosphor is chosen as the monochrome phosphor for this development project.

There are three main reasons for choosing the green ZnS:Tb ALE phosphor. First, ZnS:Tb ACTFEL devices exhibit brightness linearity with frequency and high brightness levels at frequencies up to 10 kHz. The luminance versus frequency characteristics for the green ZnS:Tb and yellow ZnS:Mn phosphors are shown in Fig. 22. Note the onset of the saturation of the luminance of the yellow ZnS:Mn device at frequencies above approximately 2 kHz. The white SrS:Ce/ZnS:Mn phosphor, suffers from the same type of saturation trend since it contains the yellow ZnS:Mn phosphor as one of its components. The blue SrS:Ce phosphor could not meet the brightness requirement of this work; in this developmental work, one of the goals is to achieve a brightness level of above 1000 fL for see-through HMD applications. This high brightness level is only achievable with high frequencies. As seen from Fig. 22, the brightness of the green ZnS:Tb device is higher than that of the yellow ZnS:Mn phosphor for frequencies in excess of 5 kHz, whereas at lower frequencies the brightness trend is reversed. To achieve the 1000 fL brightness and the 64-level gray scale goals (as discussed in Section III.7.2), a drive waveform comprised of 10 kHz sine bursts is used for this work.

A second reason for the desirability of a linear luminance vs. frequency relationship, as exhibited by the green phosphor, is with respect to the achievement of gray scale. As described in Section III.7, the time domain gray scale approach used here achieves different gray levels by changing the number of applied pulses per frame time. This approach is effectively the same as changing the applied frequency. If the brightness of the device saturates at higher frequencies, then a linear increase in the number of pulses does not result in a linear increase in the brightness. In turn, this has adverse effects on the monotonicity of the display's gray scale. The linear relationship of luminance vs. frequency for the green ZnS:Tb ALE device circumvents this problem.

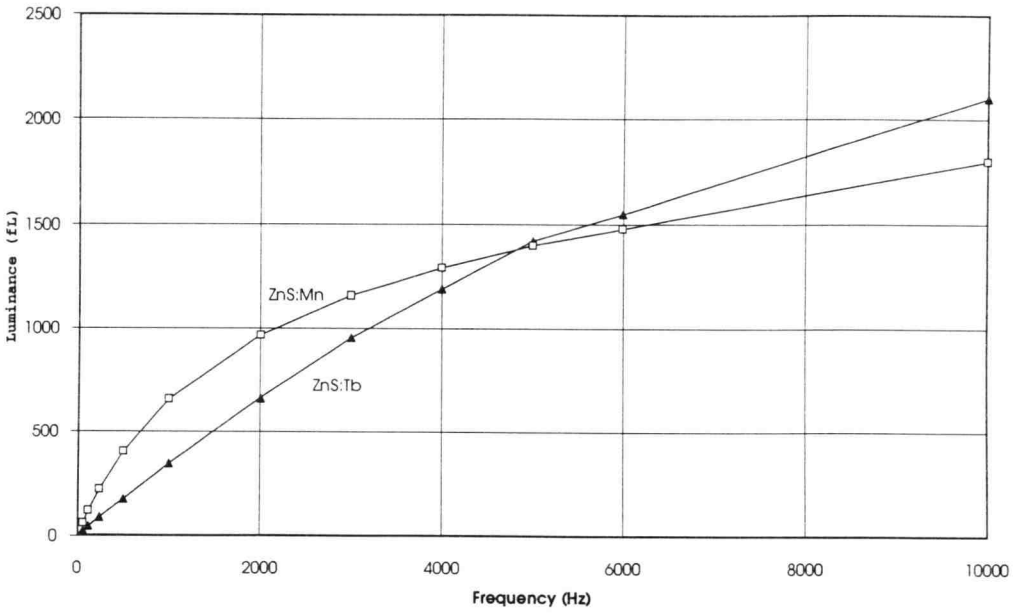

Figure 22: Luminance versus frequency characteristics of green ZnS:Tb and yellow ZnS:Mn films on glass substrates.

Another reason for the use of the ALE green ZnS:Tb phosphor is related to the optical design of the head-mount system. A narrow emission band results in a simpler and more efficient optical design. A narrower emission band allows for easier focusing, simpler modifications of the optical path, less critical requirements for the optical coatings, and a minimal optical loss.[87] The green ZnS:Tb phosphor has a narrower emission band spectrum compared to that of the yellow ZnS:Mn phosphor and, obviously, to that of the white SrS:Ce/ZnS:Mn phosphor. The emission spectra for the green and yellow phosphors are shown in Figs. 23 and 24. In conclusion, the narrow emission band makes the ZnS:Tb green device more suitable for the intended head-mounted display application.

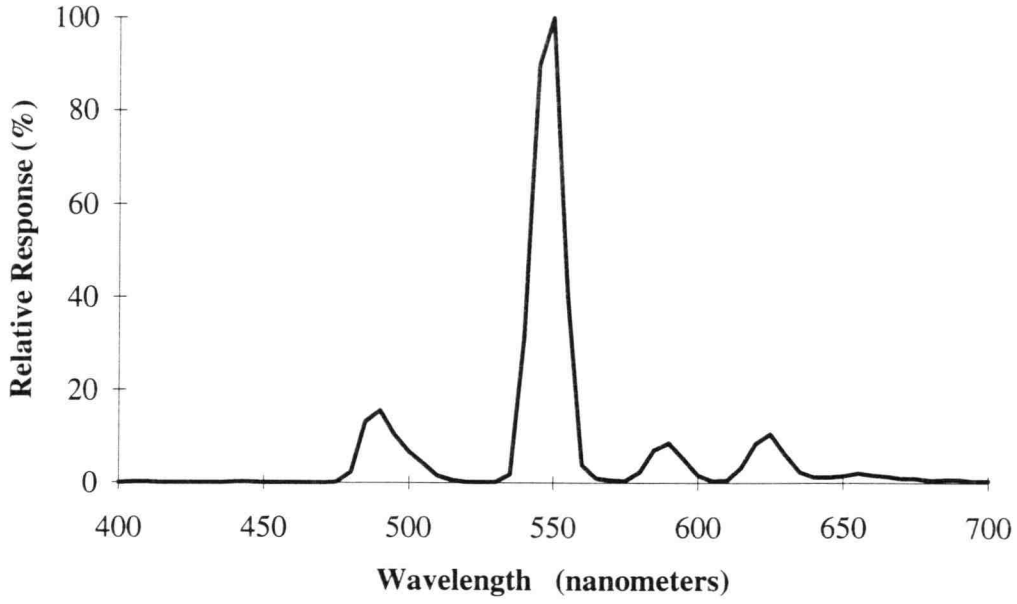

Figure 23: Emission spectrum of the green ZnS:Tb ACTFEL device.

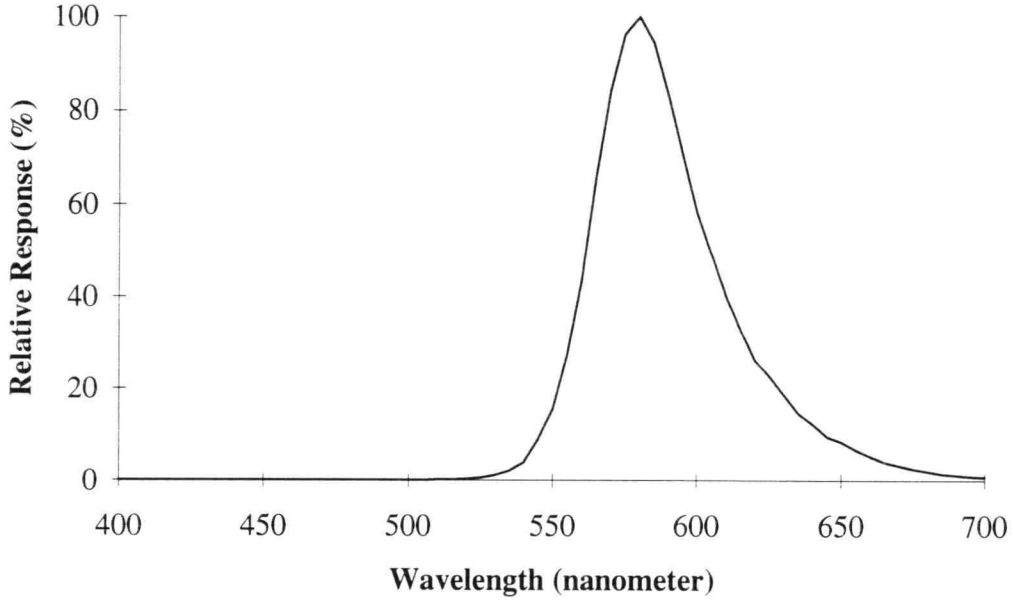

Figure 24: Emission spectrum of the yellow ZnS:Mn ACTFEL device.

IV.5. Physical Characterization of the EL Thin Film

For reasons described in the last section, the ALE ZnS:Tb green EL phosphor is chosen for this work. The remainder of this chapter focuses on the optical and electrical characteristics of this EL thin-film in AMEL applications. The basic characteristics of the ALE green EL device, which establishes the basis for the AMEL brightness and power performance discussed in the next chapter, is discussed. The measurements are performed on test devices fabricated on a 2" x 2" glass substrate, with an ITO bottom electrode, and an Al top electrode.

As discussed in the last section, the drive waveform for the AMEL display is high frequency pulses with, for example, a sine wave shape. The L-V characteristic of an AMEL device under a 1000 Hz sine wave excitation is shown in Fig. 25. The threshold voltage of this device is approximately 155 V. A 40 V modulation voltage is adequate for differentiating the on versus off states, as shown in Fig. 25. Another waveform, which is normally used for testing, is comprised of bipolar rectangular pulses with 5 μs rise and fall times and a 30 μs pulse width. Due to the fast transitions associated with the rising and falling edges of the bipolar pulses, this bipolar pulse waveform can provide more detailed information on the electrical parameters of an AMEL device.

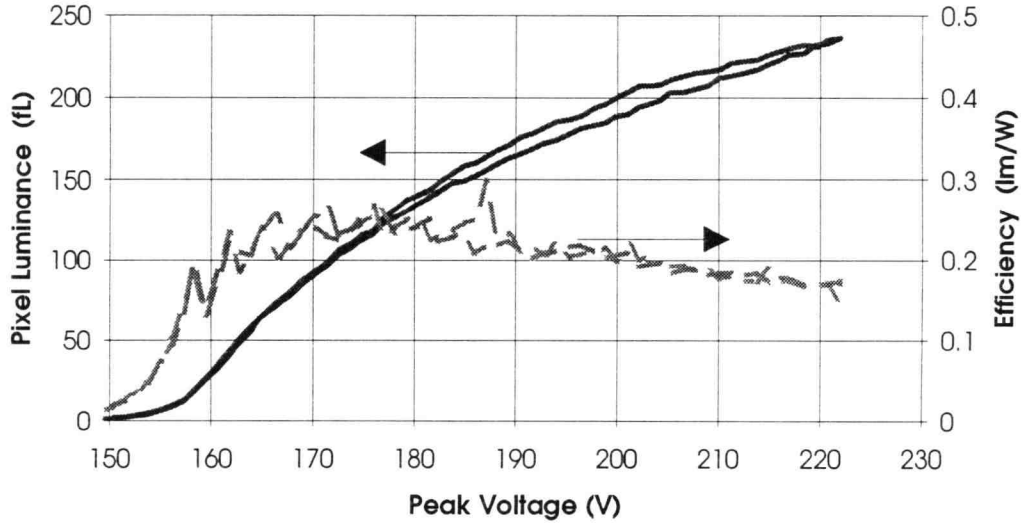

Figure 25: L-V and efficiency curves for an ALE green device subjected to 1000 Hz sine wave excitation.

The capacitance versus voltage (C-V) measurement can provide insight into the electrical operation of the device.[17-20] A C-V plot, using a pulse waveform of amplitude 210 V for the EL device used in this work, is shown in Fig. 26. From this curve, various parameters can be extracted. Some of these are summarized in Table 4 and compared with values calculated from the known thicknesses and dielectric constants of the layers or from other measurements. The values of the parameters in Table 4 are used in the design and performance predictions of the AMEL display. The capacitance values, along with the Vto value, for example, are used in the EL model, as described in Sections III.4.1 and III.4.2, to predict the power and relative optical performance. The good agreement of the calculated to the measured values from the C-V plot shows the accuracy of the C-V method for finding these parameters. Since the C-V measurement is a simpler method of establishing the device structure after the full fabrication, it is used throughout this work for the input parameters to the design.

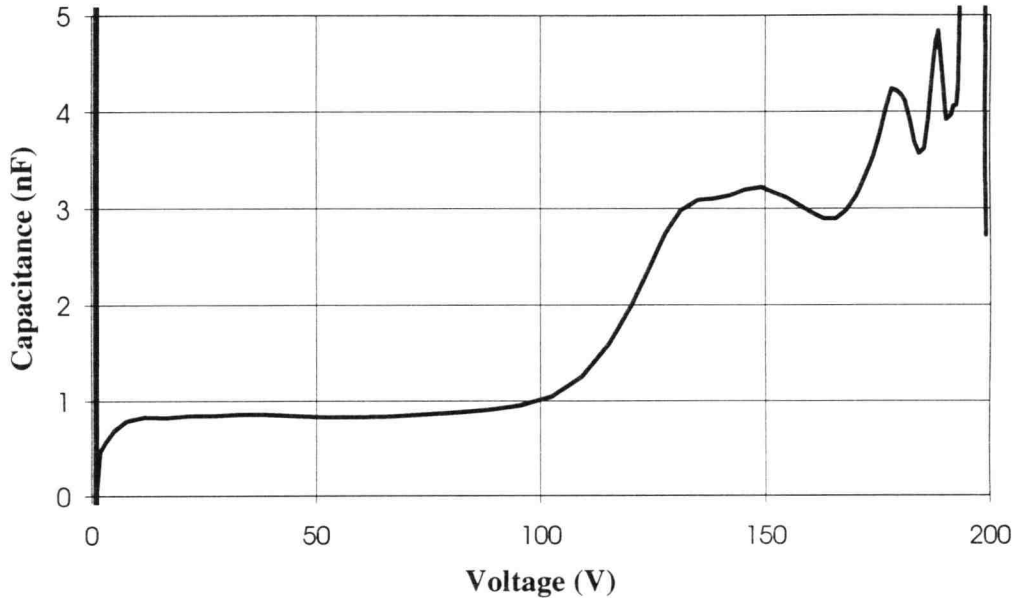

Figure 26: C-V plot for an ALE green AMEL device with Vmax = 210 V (positive pulse to top Al electrode).

Parameter	Value from C-V	Calculated
Capacitance below turn-on	0.8 nF	0.75 nF *
Insulator capacitance	3.0 nF	2.86 nF *
ZnS capacitance	1.1 nF	1.01 nF *
Vto	120V	130V **
Vth	165V	170V ***

Table 4: Summary of data from the C-V plot (average of measurements from positive and negative pulses).

* ZnS thickness: 5900 Å; relative dielectric constant: 8.5
ATO thickness: 2200 Å thickness of Al2O3; relative dielectric constant: 9.

** Calculated from Vth and maximum applied voltage values.

*** Extracted from L-V curve.

IV.6 Physical Characteristic Changes as a Function of the Drive Frequency

As per discussions in Section IV.4, the display needs to be operated at frequencies near 10 kHz bursts to achieve the desired 1000 fL brightness levels. A standard EL display's illumination frequency is 60 Hz. The 10 kHz rates used in this AMEL display have not been previously used for EL device excitation. L-V measurements using high frequency, continuous sine wave excitation are performed on the ALE ZnS:Tb EL devices. An L-V curve for a test device subjected to 5 kHz continuous sine wave excitation is shown in Fig. 27. Note that the luminance saturates at about 20 V above threshold and remains at the same level with higher amplitudes of the applied voltage. As the voltage is reduced, the brightness is constant until about 20 V above threshold and then follows the same path as the initial increasing voltage. This saturation in the brightness is a source of performance limitation.

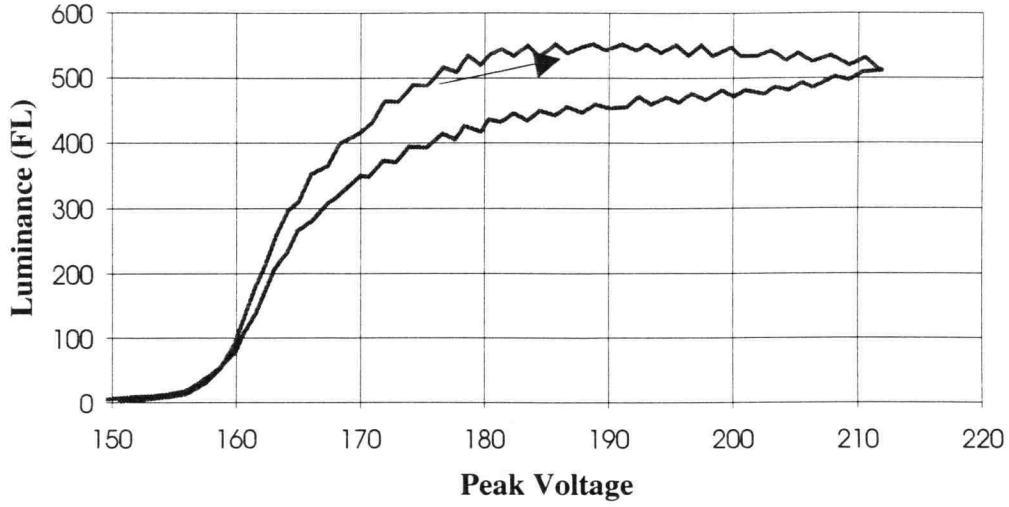

Figure 27: L-V curve for an ALE green device subjected to 5 kHz sine wave excitation.

Further investigation of this brightness saturation is performed by studying the electrical characteristics during the brightness saturation. The conduction charge is measured by integrating the current flow to the device in half of the sine wave period. Simultaneously, the temperature of the device is measured by an IR thermometer. The normalized conduction current, brightness, and temperature as a function of time are shown in Fig. 28.[88] The measurements in Fig. 28 are performed at 10 kHz using a sine wave with a peak voltage of 190 V, which is Vth + 20 V for the sample when a pulse excitation is used. Higher frequencies or voltages result in a similar trend but with a shorter transient duration. The measurement results in Fig. 28 show that an increase in conduction current, an increase in temperature, and a decrease in brightness as a function of time when the AMEL device is driven by a high frequency waveform. This result suggests that the brightness saturation observed in Fig. 27 may be mediated by an increase in temperature. Also, the increase in the conduction current shown in Fig. 28 appears to be linked to the brightness saturation of Fig. 27 because of similar trends in the conduction charge and brightness shown in Fig. 28.

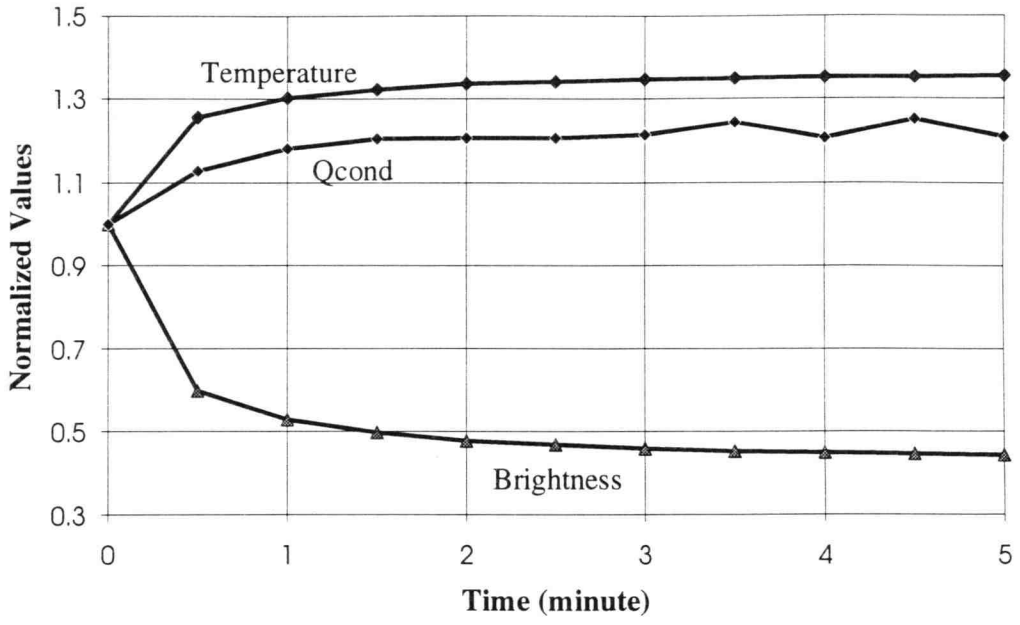

Figure 28: Normalized trends of conduction charge, brightness, and temperature as a function of excitation time subsequent to the application of a 10 kHz sine wave excitation.

Normalized Luminance to 812 fL
Conduction charge to 180nC
Temperature to 294 K

IV.7 Empirical Solution to the Brightness Saturation Problem

Several approaches are investigated for resolving the problem associated with brightness saturation at higher frequencies. The most direct solution is to remove the heat from the device in order to prevent the device from entering into what appears to be a thermal run away situation. Initial tests to deduce the role of temperature in determining the brightness saturation are performed by spraying a coolant directly onto the device. Thus, it is found that the brightness saturation problem is avoided if the temperature of the device is maintained near room temperature. Now that it is established that the saturation problem can be avoided by preventing the device temperature from increasing, a more practical solution to this problem is to bond the Si substrate onto a ceramic carrier. Since the EL thin-film is in direct contact with the Si substrate, the idea is that heat is taken away from the EL device and transferred to the ambient via the ceramic carrier. This solution,

although it can prevent the occurrence of brightness saturation symptoms, does not resolve the fundamental brightness saturation problem.

Other ZnS-based EL thin-films are tested to determine whether the brightness saturation problem is related to the basic ZnS phosphor. The two other phosphors evaluated are yellow ALE ZnS:Mn and green sputtered ZnS:Tb. The test results show that neither of these two EL thin-films exhibit the brightness saturation problem which is observed in the ALE ZnS:Tb devices. The lack of this saturation effect in the ALE ZnS:Mn device indicates that the ALE ZnS itself is not the source of the brightness saturation. The lack of this problem in sputtered ZnS:Tb suggests a source other than the Tb dopant as the source of the saturation problem. Therefore, the experimental results point to some factor peculiar to the ALE ZnS:Tb process or thin-film structure as the source of the saturation problem.

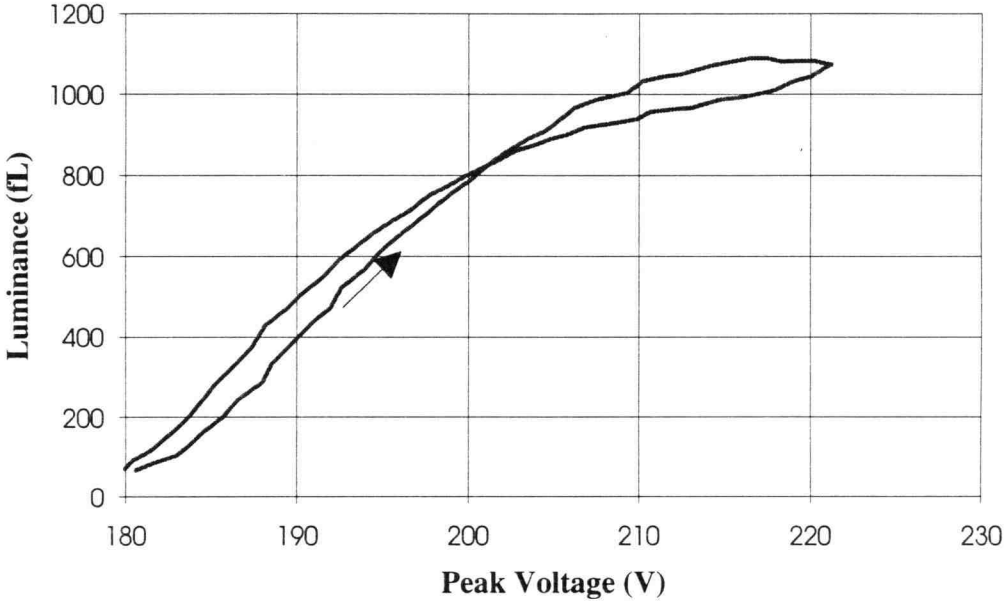

Figure 29: L-V curve for an ALE green device subjected to a 740 °C RTA treatment.

Addition of a rapid thermal anneal (RTA) step shows a significant improvement in the device operation. An L-V curve for a device subjected to a 2 minute RTA treatment at 740 °C is shown in Fig. 29. The excitation waveform is a sine wave of frequency 5 kHz,

which is the same waveform used for the non-RTA sample shown in Fig. 27. Comparing Fig. 29 to Fig. 27, the improvement in saturation and the resulting increase in the brightness is evident. This RTA solution to the brightness saturation problem proved to be both effective and also helpful in elucidating the physical understanding of the saturation mechanism, as is discussed in the next section.

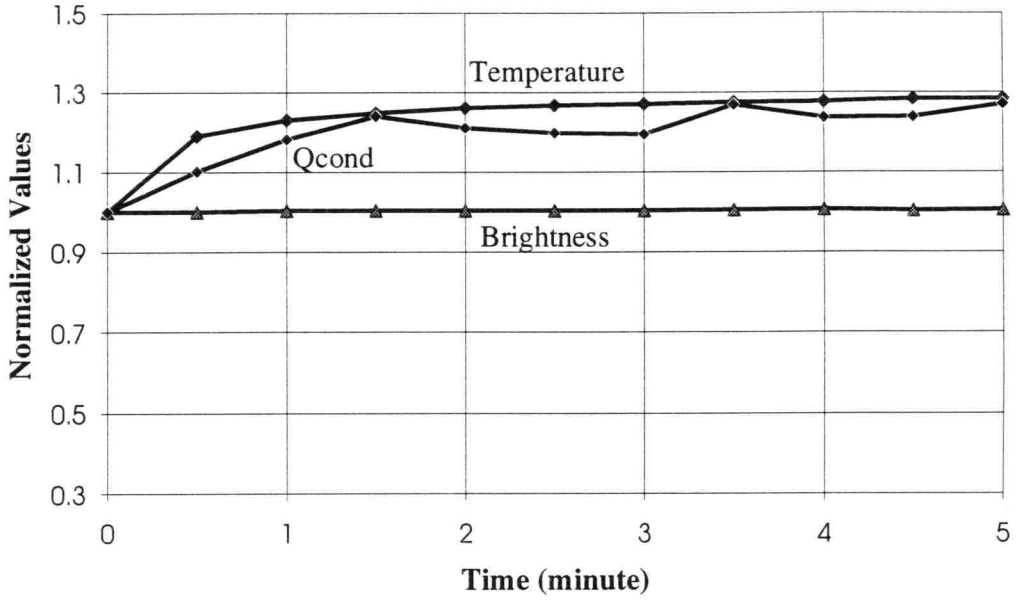

Figure 30: Normalized trends of conduction charge, brightness, and temperature as a function of excitation time for an ALE green EL sample subjected to a 740 °C RTA step.

Normalized Luminance to 1000 fL
Conduction charge to 113 nC
Temperature to 293 K

To better understand the device behavior, brightness, conduction charge, and temperature trends of an EL test device on a glass substrate are measured as a function of operation time while applying the high frequency excitation, as indicated in Fig. 30 for an EL device subjected to an RTA treatment. The results of an identical measurement are shown in Fig. 28 for a non-RTA EL sample. To allow a direct comparison of the RTA and non-RTA samples, the sine wave excitation waveform is maintained at a frequency of

10 kHz and at an amplitude of Vth + 20 V, which is 205 V for this sample under a pulse excitation. As illustrated in Fig. 30, the brightness is constant with time for the RTA device which is in dramatic contrast to Fig. 28 in which the brightness decreases to about 50% with time for the non-RTA device. Note that Figs. 28 and 30 show identical trends for the conduction charge and temperature for the non-RTA and RTA EL devices. Thus, although Fig. 28 suggests that the decrease in brightness is directly correlated to an increase in the temperature and conduction charge, the distinctly different brightness trend exhibited in Fig. 30 indicates the involvement of another factor. Further discussion of the brightness saturation mechanism is found in the next section.

IV. 8. Physical Mechanism of Brightness Saturation

The phenomenon of interest in this section is the brightness saturation. This saturation behavior can be caused by one of several possible sources. These sources are first enumerated and then each one is evaluated based on the measured data from the previous section. Additional data is provided to allow a more detailed evaluation of each factor. The possible sources of the brightness saturation include:

1. Decrease in the field across the ZnS phosphor film: If the phosphor field is reduced significantly over time by the excessive flow of conduction current, or by the increased temperature, a lower brightness is expected.

2. Excited Tb centers: If the excited Tb centers are ionized due to, for example, an increase in the device temperature, there are less Tb centers available for radiative de-excitation and, thus, there is a reduction in brightness. Alternatively, the long decay time of the Tb centers could result in brightness saturation when a high frequency excitation is used.

3. Temperature increase: An increase in temperature could cause a reduction in the brightness due changes in the thin-films. This decrease in brightness could be related to sources such as a change in the thin-film dielectric constant, or a lower electron transport efficiency as a function of temperature.

4. Lower de-excitation efficiency with increased temperature: The brightness saturation could be related to a high rate of non-radiative de-excitation, possibly due to the structure of the ALE ZnS:Tb film.

A decrease in the phosphor field is consistent with the expectation that an increase in the conduction charge can reduce the ZnS breakdown field. A larger conduction current can fill the more shallow traps, resulting in interface state emission at lower fields. Due to the lower energy of these electrons, the impact excitation process would not be as efficient. To establish the field of the ZnS layer, the charge flow in the device as a function of the ZnS field ($Q\text{-}F_p$) is measured, as shown in Fig. 31.[89] The breakdown field is initially about 1.85 MV/cm and reduces to about 1.81 MV/cm after 1 minute of operation with the 10 kHz sine wave excitation.

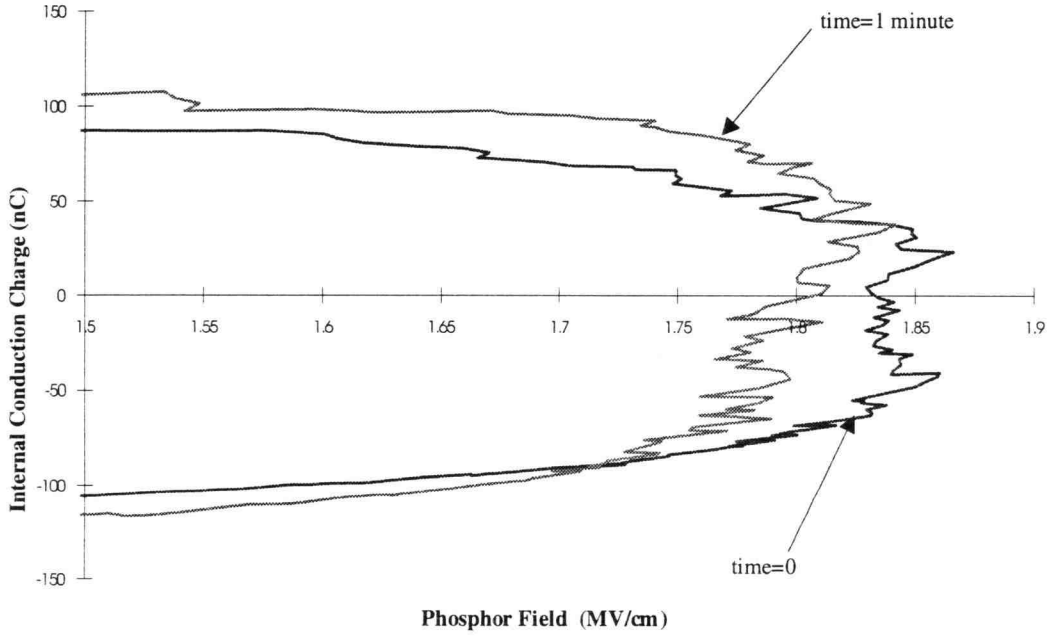

Figure 31: $Q\text{-}F_p$ plot for an ALE green ZnS:Tb EL device.

The observed decrease in the phosphor field cannot be the source of brightness saturation for two reasons. First, a similar decrease in the phosphor field is observed for the RTA samples. Since the RTA samples do not exhibit the saturation, the ZnS field

drop cannot be the cause of the brightness saturation. The second reason is that a phosphor field decrease of less than 0.04 MV/cm along with an increase in the conduction charge is not likely to cause a 50% brightness decrease.

The second potential source of the brightness saturation problem is related to the Tb excited centers. The Tb ionization explanation is consistent with the observed conduction charge increase and brightness decrease. However, the Tb-ionization explanation is inconsistent with the observation that RTA treated samples do not exhibit the brightness saturation even though they have the same Tb concentration and conduction charge increase as the non-RTA samples. Another possible source of brightness saturation is the long Tb decay time (of about 400 μS) compared with the time period between the light pulses (of about 50 μS). This possible source can also be eliminated as the source of the brightness saturation since the Tb centers exhibit similar decay time constants in the non-RTA and RTA samples.

The third potential source of the brightness saturation is associated with temperature-dependent changes in the properties of the EL stack thin-film. Based on the results shown in Figs. 28 and 30, the temperature and conduction current increases in the RTA and non-RTA samples are similar. Therefore, any decrease in the brightness as a result of a temperature effect related to changes in the thin-film dielectric constants or to a decrease in the electron transport efficiency should be the same for the RTA or the non-RTA sample. Since brightness saturation is not observed in RTA treated samples, simple temperature-dependent changes in the physical properties of the thin-film layers may be eliminated as a possible source of the brightness saturation problem.

The remaining possible source for the brightness saturation is the low de-excitation efficiency of Tb centers in the ALE film at high temperature and excitation levels. With the high frequency excitation waveform, a large number of Tb centers are excited and can interact with each other or couple to phonon modes resulting in a high probability for non-radiative de-excitation. To evaluate this potential source of brightness saturation, the de-excitation efficiency is measured.

The de-excitation efficiency is measured using a technique discussed by Dr. E. Briguier.[90] The total number of centers de-excited radiatively are measured by integrating the light output from one pulse, which is designated S. The total light output is equal to the product of the peak light output, L_0, and the effective time constant of the light decay, τ. If all of the centers decay radiatively, an exponential decay of the light pulse is expected with the total number of excited centers, n_0, equal to the product of L_0

and the radiative time constant τ_0. Therefore, the fraction of centers with non-radiative de-excitation, designated as f, can be found as follows:

$$S = L_0\tau$$
$$n_0 = L_0\tau_0$$
$$\Rightarrow f = S/n_0 = \tau/\tau_0$$

The de-excitation efficiency change during EL device operation is monitored as a function of temperature. In this work, only the relative de-excitation efficiency is of interest; therefore, there is no need to know the value of τ_0 since the relative de-excitation efficiency can be monitored by measuring τ. The normalized value of τ (S/L_0) is calculated and plotted along with the conduction charge as a function of the device temperature and is shown in Fig. 32. The measured results for a sample with no RTA treatment and a sample with a 740 °C RTA treatment are included in Fig. 32. The measurements are performed at temperatures up to 110 C (383 K) since the device temperature during device operation remains below this value as shown in Fig. 29.

An increase in the non-radiative de-excitation of the non-RTA sample is evident from the decrease in the de-excitation efficiency with temperature illustrated in Fig. 32. However, such a decrease is not observed for the RTA sample. Now in order for the increase in the non-radiative de-excitation to be established as the source of the brightness saturation, the difference in brightness saturation behavior between RTA and non-RTA samples needs to be explained.

The Tb de-excitation efficiency depends strongly on the atomic environment of the surrounding lattice. There are various examples in the literature which support this assertion. For example, the decay time constant, which is a parameter directly related to the de-excitation efficiency, does not have as strong relationship to the doping density as in the case with Mn doping; however, the decay time constant is significantly affected by incorporatin of a F^- co-dopant.[90-92] One major difference between the ALE and sputtered ZnS:Tb phosphor is the location of the dopants. In sputtered films, the Tb dopant is incorporated into the sputtering source and is deposited onto the substrate uniformly throughout the film thickness. However, in the ALE ZnS:Tb deposition process, the Tb dopant is incorporated in concentrated layers separated from pure ZnS layers. Therefore, a lower de-excitation efficiency at high excitation levels should be expected for the ALE ZnS:Tb phosphor since the Tb atoms are in extreme close physical proximity and Tb-Tb interactions are more likely. Since the Tb atom is much larger than the Zn atom, whose lattice site Tb substitutes for, the high local concentration of Tb results

in a change in the local atomic geometry of the lattice. This change in the atomic environment could also increase the interaction between the excited Tb centers and the phonon modes resulting in a decreased de-excitation efficiency.

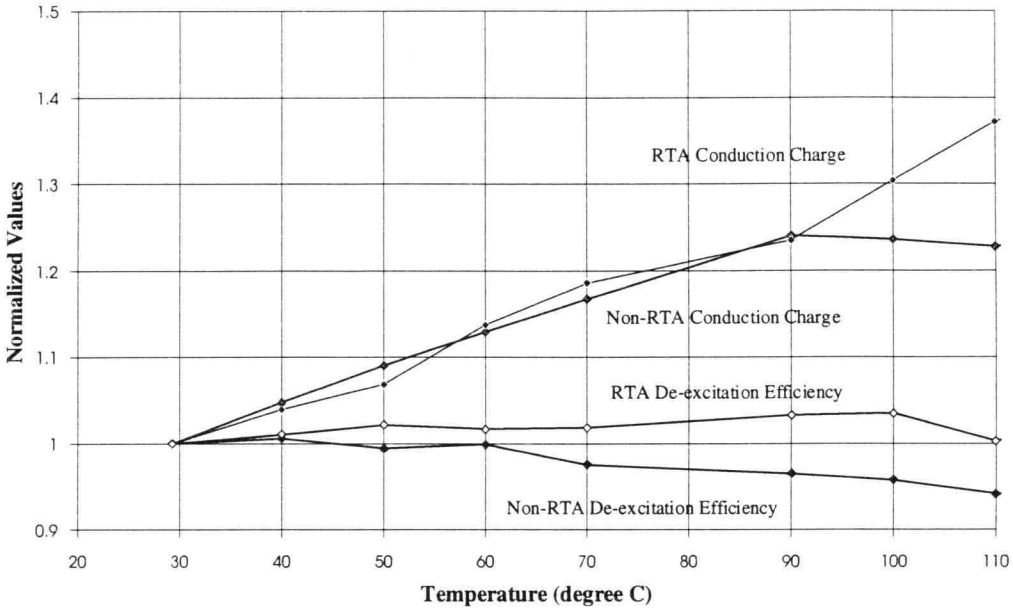

Figure 32: Normalized conduction charge and de-excitation efficiency as a function of temperature.

To explain the improvement associated with the RTA treatment, it is expected that due to the RTA process step a redistribution of the Tb centers, and hence its surrounding in the lattice, has occurred . To test this hypothesis, Auger sputter profile experiments are undertaken. However, since the dopant layer thickness is normally about 5 Å and are separated by about 60 Å of ZnS, detection of a change in the Tb concentration profile would be exceedingly difficult for typical analytical measurement techniques. To ease this measurement difficulty, a special ZnS:Tb film is fabricated with a thicker Tb dopant layer and a thicker separation between the doping layers to allow for the detection of any movement of the constituent atoms. The test structure consists of three ZnS layers of about 500 Å each separating two 200 Å dopant layers. One sample is subjected to 2 minutes of 720 °C RTA treatment while the other one is maintained as a control and is not annealed. The results of the Auger measurements using this special test structure show a large decrease in the Tb/Zn ratio in the TbS layer after the RTA step, as shown in Table

5.[93,94] The decrease in the Tb/Zn ratio and the decrease in the Tb/S indicates a redistribution of ZnS into the TbS doping layer, or, alternately, a redistribution of Tb into the ZnS layer.

The change in the elemental concentration indicates a more uniform distribution of the Tb dopant within the ZnS film subsequent to the RTA treatment. This finding is consistent with the earlier postulate that the high local Tb concentration in the non-RTA samples results in more efficient non-radiative de-excitations paths, a decrease in the emission efficiency, and a concomitant decrease in the brightness. The exact nature of the non-radiative paths in the device with the concentrated doping layer is not clear. It could be associated with the exacerbated Tb-Tb interactions or an increased rate of non-radiative recombination via phonon dissipation. In either case, it has been shown that maintaining a low device temperature and redistribution of Tb centers via an RTA step reduces the non-radiative recombination rate.

Parameter	No RTA	720 C RTA
Tb/Zn	7.7	2
Tb/S	1.2	0.7

Table 5: Approximate atomic concentration ratios in the TbS dopant layer, as estimated by Auger sputter profiling.

Based on the experimental results discussed above, a 720 to 740 °C RTA step is added for the ZnS:Tb-based thin-film used in AMEL applications. The completed displays are then assembled onto a ceramic carrier for the removal of heat generated during device operation. With these two modifications, AMEL displays are fabricated which do not exhibit the brightness saturation problem.

In this chapter, EL thin-film deposition and processing issues for AMEL applications, as well as issues involving driving the AMEL device at high excitation frequencies, are discussed. Solutions to the identified problems of utilizing an inverted structure on a Si substrate, obtaining conformal coatings, thin-film cracking, and brightness saturation at high frequencies are presented along with a discussion of the underlying physical processes responsible for these problems. In the next chapter, the final AMEL display performance is discussed. Fabrication of the final display is based on the approaches and solutions discussed in this and the previous chapter.

Chapter V. OPTICAL AND ELECTRICAL CHARACTERIZATION OF THE AMEL DISPLAY

In the previous chapters, the electrical circuit and EL thin-film processing approach for the AMEL display is developed. In this chapter, the optical and electrical characteristics of the AMEL display are reported and compared with the performance estimates obtained from simulation and measurements of test samples. The characteristics of interest in this display include brightness, contrast ratio, gray scale, stability with aging time, and power consumption. These parameters are discussed in the first part of the chapter followed by a summary of the display characteristics.

Each display characteristic is discussed separately in the following sections. In the first part of each section, the expected performance based on simulation or measurements of the test samples is included. The passive test samples are the same as the ones referred to in the earlier chapters. EL thin-films in these test samples are deposited on top of an ITO electrode on a glass substrate followed by the deposition of an Al top electrode. This test device allows evaluation of the EL thin-film without complications arising from the addition of the AMEL circuitry. A sine wave frequency of 4.5 kHz is employed in tests on the AMEL display reported in this chapter. A higher driving frequency would result in better performance; however, due to the internal resistance of the data lines, the higher current from a higher drive frequency would result in an excessive voltage drop in the data lines and would interfere with the correct operation of the display. The number of pulses in the sine burst is 32 for every 16.7 mS frame time (60 Hz cycle). The 32-pulse sine wave burst at a 4.5 kHz frequency provides enough remaining time in each frame time to write the 6 bit data to the whole display, as described in Section III.7 and later in Section V.3. The measured AMEL performance is based on a 1280 column by 1024 row AMEL display with a 24 μm pixel pitch and complete peripheral circuitry.

V.1. Luminance

The luminance performance is the most common characteristic specified for any display. In this AMEL display, the goal is to achieve the maximum luminance. Initial tests are performed with the passive test samples using a continuos sine wave at 4.5 kHz. The test samples on a glass substrate provide information with respect to the EL thin-film brightness performance. The brightness level of an actual AMEL display is lower than

that of a passive test device due to several factors. First, a decrease in the AMEL display brightness results from a smaller number of pulses applied to the AMEL display compared to a continuous series of pulses. Due to the gray scale approach adopted, see Sections III.7 and V.3, only about 43% of the frame time is available for the drive waveform. The waveform used for the AMEL display is 32 pulses at 4.5 kHz repeated every 16.7 mS (60 Hz). The brightness at Vth+40 V measured for a passive sample (sample #66R) with the adopted thin-film process, as described in Chapter IV, is about 280 fL with a threshold voltage of 145 V. Since a reflective Al electrode is not used in the AMEL display, a 50% reduction in the measured brightness is expected in the AMEL display compared to the passive test sample. This would be expected to reduce the brightness to 140 fL. Furthermore, the light emitting area in the AMEL display does not include a 2 μm separation between the pixels (which have 24 μm pitch). The fill factor, i.e. the ratio of light emitting area to the total display area, is $22^2/24^2$ or 84%, resulting in a final expected brightness of 120 fL in the AMEL display.

Another brightness factor that makes it difficult to estimate the AMEL performance based on the measurement of passive test samples is the roughness of the display surface. Due to the difference between the ZnS index of refraction (n=2.3) and the index of refraction of air (n=1.0), some of the light is trapped in the ZnS layer due to total internal reflection. Based on Snell's Law (i.e. $n_1 x \mathrm{Sin}\theta_1 = n_2 x \mathrm{Sin}\theta_2$), the critical angle is 26° for the ZnS case.[95] This light travels parallel to the display surface instead of contributing to the observed light. In an AMEL display, due to the topography created by the IC processing, as shown in Fig. 17, some of this trapped light is reflected to the surface. The extent of this reflected light translates into a brightness increase from the luminance estimated earlier from passive test sample measurements.

The luminance performance of the AMEL display as a function of the applied voltage is shown in Fig. 33.[96] The display used is from wafer 14166.1-02B, which is from the same run as the glass sample #66R. As described earlier, the applied waveform is 32 pulses of a 4.5 kHz sine wave in every 16.7 mS (60 Hz) time interval. The measured threshold for this AMEL device is 138 V while the brightness at Vth + 40 is 140 fL. The higher measured luminance compared with the estimated value of 120 fL can be explained by the improved light outcoupling due to the surface topography. The lower Vth observed in the AMEL display, compared with the 145V measured for glass sample, is also consistent with having a rougher surface in the AMEL case; a non-unifrom surface topography results in regions of electric field enhancement which is manifest as a reduction of the threshold voltage.

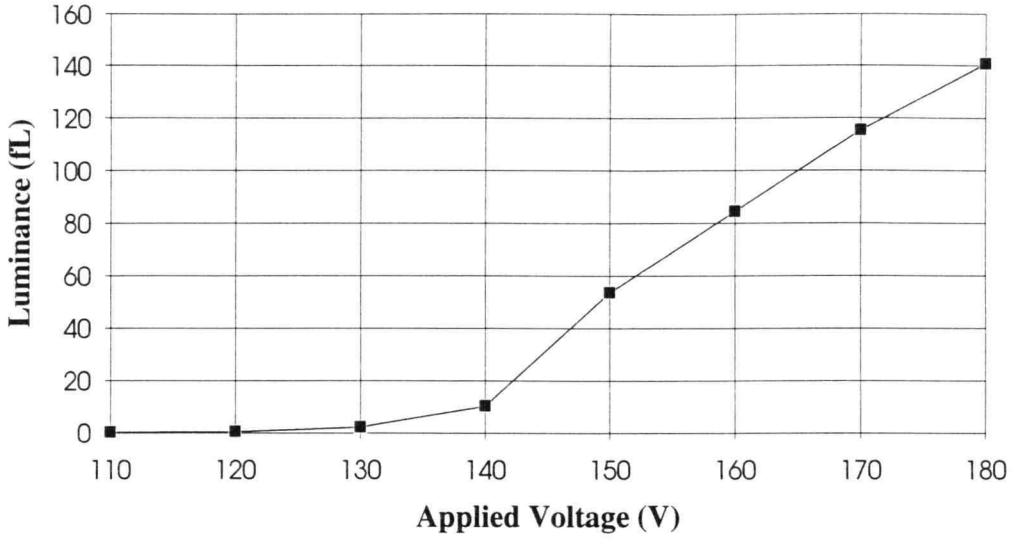

Figure 33: L-V curve of an EL film in an AMEL display.

V.2. Contrast Ratio

A second important display characteristic is the contrast ratio. The contrast ratio is a measure of how readable the display is. It is defined as the ratio of the luminance of an "on" pixel divided by the luminance of an "off" pixel. The technical display standard requires measurement of the contrast ratio between the off pixel inside the loop of the letter "e" and the adjacent on pixel.[97] However, the display industry follows a less stringent definition which is the ratio of display brightness with a full on pattern to the brightness with a full off pattern. In this work, the latter definition is employed.

In an AMEL display, the voltage difference between on and off pixels is defined by the transistor breakdown voltage. Based on the discussions of Section III.3, the difference in the applied voltage is one half of the breakdown voltage of the high voltage transistor, which is the DMOS transistor labeled M2 in Fig. 7. Based on I-V measurements of individual DMOS test transistors, a breakdown voltage of about 100 V is expected. This breakdown voltage implies a difference in the effective on versus off drive voltage of 50 V. This estimated voltage implies that the contrast ratio should be the ratio of luminance at Vth + 40, i.e. 140 fL, and the luminance at Vth - 10, i.e. 2 fL. Therefore, the expected contrast ratio with a voltage amplitude of 180V is about 70:1.

This contrast ratio is changed if the pixel operation is affected by the other circuitry in the array.

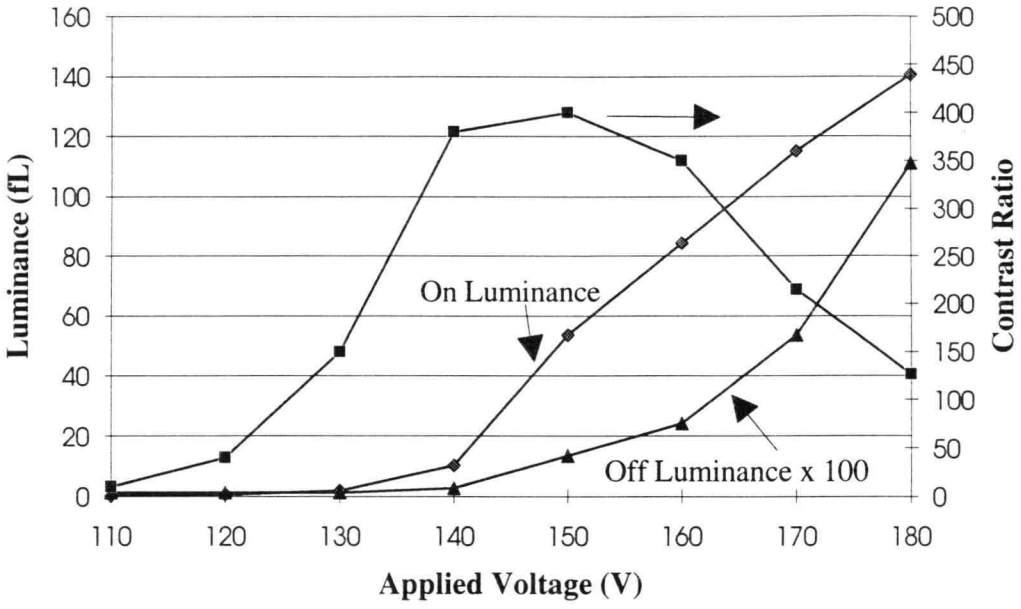

Figure 34: AMEL display contrast ratio as a function of applied voltage. Note that the off luminance has been multiplied by a factor of 100 in order to plot it on the same scale as on luminance.

The L-V curves for full on and full off screens are measured using the same waveform as used in the last section. The ratio of these two brightnesses at any particular voltage is the contrast ratio. The resulting curve for the display is shown in Fig. 34.[96] This figure also includes the on and off luminance plots. As expected, the contrast ratio improves for the lower drive voltages (i.e. up to 150 V) due to the low off brightness. However, as the drive voltage is increased to above 150 V, the off brightness increases, and the contrast ratio drops, due to the limited blocking voltage capability of the high voltage transistors. The luminance measurements show that the off pixels achieve the same level of brightness as the on pixels with about 55 V higher voltage to achieve the same level of brightness as the on pixels. For example, a voltage of 180 V is required for the off pixels to achieve the same brightness as 125 V applied to the on pixels. This difference of 55 V implies a DMOS blocking voltage of about 110 V. This is slightly

higher than, but comparable with, the 100V blocking predicted based on the break-down measurement of the discrete test transistors, as described earlier. As shown in Fig. 34, the contrast ratio obtained using a Vth + 40 V, i.e. 180 V, drive voltage is above 120:1. This measured contrast ratio is higher than the 70:1 value estimated earlier. This larger value of contrast ratio is consistent with the larger blocking voltage obtained from the luminance measurements and is consistent with the variations due to IC processing and unexpected coupling within the pixel circuitry.

V.3. Gray Scale and Dimming

Another characteristic of interest for the AMEL display is the gray scale. The goal of this work is to achieve a display in which every pixel can independently have 64 different brightness levels, or so called gray levels. The gray scale is achieved by applying an appropriate number of pulses to the pixel, as discussed in Section III.7. The luminance versus frequency of an ALE ZnS:Tb EL device is linear, as shown in Fig. 22. This linear behavior should result in a linear luminance versus gray level when for each brighter gray level, a full period is added to the waveform. With the chosen gray scale approach, the linear luminance characteristic allows for a monotonic gray scale.

As described in the beginning of this chapter, due to the data line resistance in the actual display, a 4.5 kHz sine wave drive corresponds to the maximum current permitted in the data lines for proper display operation. This waveform allows time for only 32 periods (i.e. 7.1 mS) since the remainder of the 16.7 mS frame time needs to be used for writing the 6 bits of data to the display. As described in more detail in Section III.7.3, a sine wave cycle with an amplitude of Vth + 20 is used for the illumination pulse corresponding to the bit 0, see Fig. 15. The rest of the gray levels follow the approach described in Section III.7.3 with bit 1 having one cycle of sine wave at full voltage (i.e. Vth + 40) followed by other bits up to bit 5 which has 16 cycles of sine wave. The luminance as a function of gray level is measured on the AMEL sample and is shown in Fig. 35.[96] As expected from the luminance-frequency behavior of the ZnS:Tb EL device, the luminance-gray level curve shown in Fig. 35 is linear. This temporal gray scale approach does not result in a flickering display since even with the lowest gray level, the light is emitted at a frequency of 60 Hz. It should be added that due to the limitations of the test equipment for the measurements shown in Fig. 35, the LSB sub-frame also has an amplitude of Vth + 40 when the desired gray level is 2 or higher. In the final product, this shortcoming will be corrected.

In most applications, a lower maximum brightness, i.e. dimming, is required for use of the displays in-door or at night. To dim the display, the applied voltage amplitude is decreased by the same amount for every pulse. At the lower brightness levels, a linear gray scale is still observed.

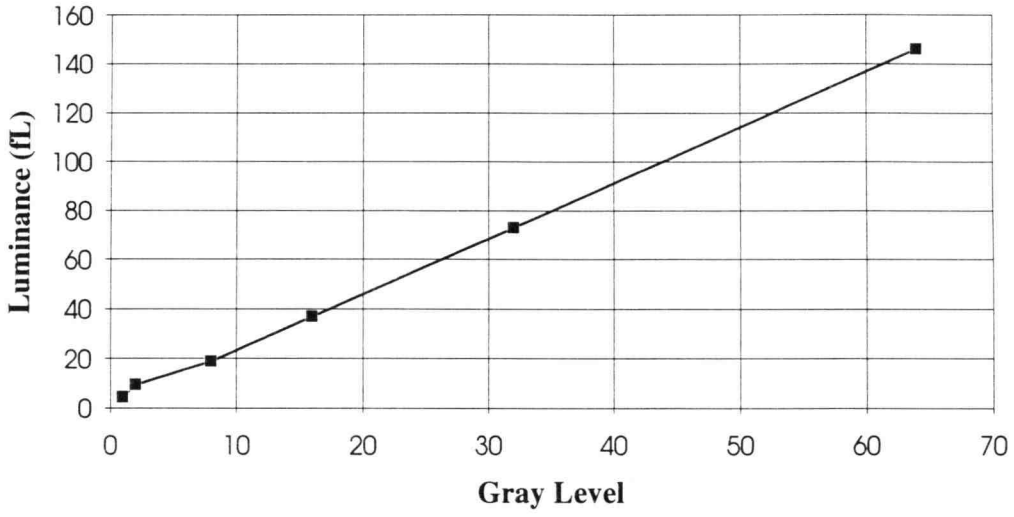

Figure 35: Luminance versus gray level .

V.4. Stability

Every display technology suffers from luminance change after long operation times. Different display technologies refer to this phenomenon with different names: burn-in for CRTs; sticking effect in LCDs; and latent image in EL devices. Silicon-based transistors also had experienced aging effects in their I-V characteristics. This IC aging was later found to be associated to mobile ion migration or similar factors; now this problem is for the most part solved in commercial silicon industry. In the case of AMEL, the EL display combined with the IC substrate introduces new processing steps and a corresponding potential for stability problems. In the processing of these AMEL devices, efforts are made to prevent aging. The IC processing is kept close to standard silicon processing in a commercial clean room facility. The processed IC wafers are covered with 9000 Å of PECVD SiO_2 before the EL's first electrode is deposited. A full cleaning procedure is included prior to the EL deposition. Furthermore, the EL thin-film process

technology employed is kept close to the standard process used to successfully fabricate commercial displays. The goal is to keep the aging of the AMEL display at the same level as that of a standard commercial EL display.

To establish the standard EL aging trend, a passive EL test sample is aged with the AMEL waveform of 32 pulses of a 4.5 kHz sine wave. The brightness at Vth + 40 V is measured and plotted as a function of time in Fig. 36. The luminance aging trend is also measured for an AMEL display using the same sine burst waveform as for the passive device. The result of this measurement is shown in Fig. 36. As the aging trends for these two devices show, the active matrix circuitry has not resulted in additional brightness instability to the device. A further long-term measurement of on brightness and contrast ratio performed on several devices is required in the future to establish the suitability of the present structure and process for a manufacturable device. However, the present data indicates the general stability of the display for most applications.

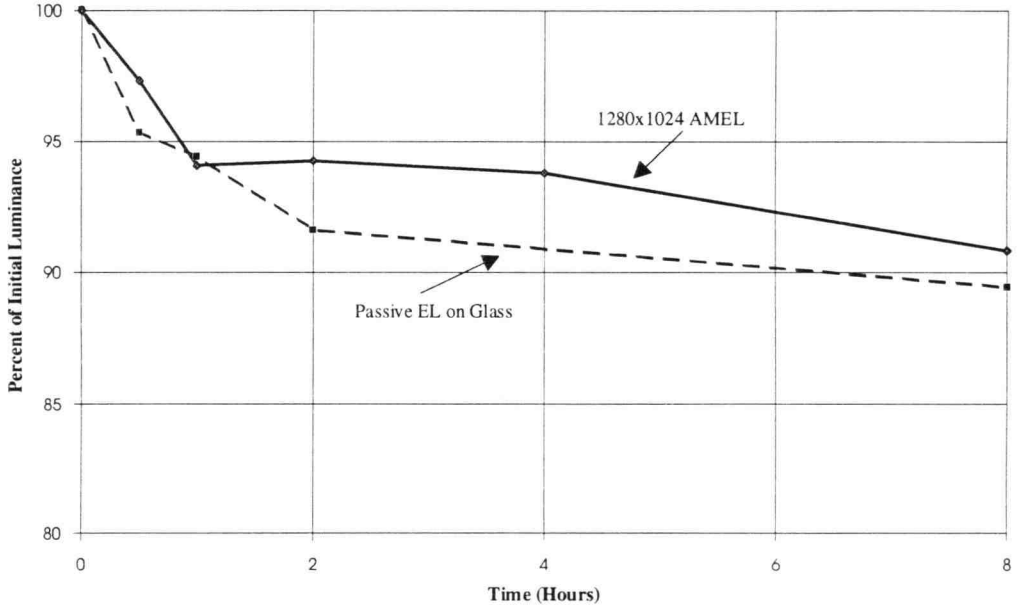

Figure 36: Aging trends for the AMEL sample and the passive EL test sample with high frequency drive.

V.5. Power

An electrical parameter of interest is the power consumption of the display. In AMEL displays, the power consumption depends on the percentage of the display illuminated; maximum power consumption occurs for a full-on display set at the highest gray level. The AMEL display power consumption depends on many factors including the maximum voltage, number of pulses applied, frequency and wave shape of the applied voltage, EL capacitance below and above its turn-on voltage, EL threshold, DMOS transistor resistance, ITO resistance, and data line resistance. The power consumption is estimated for the EL portion of the AMEL device alone since the resistance of IC components is relatively small. The tests are first performed on a passive EL sample on a silicon substrate with a similar area to the 1280 x 1024 display. In both the simulation and measurement of the test sample, the dissipated power, also called the real power, is evaluated. These power estimates, extrapolated to the same area as that of the 1280 x 1024 sample, are shown in Table 6.[98] The power values in Table 6 are based on 4.5 kHz sine wave bursts with 32 pulses of amplitude Vth + 40 V applied to the 1280 x 1024 AMEL display. The simulated power value from SPICE agrees with the passive sample to within experimental uncertainties associated with processing. Power measurements for the actual AMEL device (sample #14166.1-02A) show a lower power consumption than expected from SPICE simulation or from measurements of a passive test structure on silicon. This lower value can be explained by the fact that, as explained in the beginning of this chapter, due to the data line resistance the 1280 x 1024 display is not at full brightness across the whole display. Since the portion of the display away from the driving end remain partially off, the total power consumption is lower than estimated. The total system power is not estimated since this actual power depends on the design of the power recovery circuit. In theory, all the reactive part of the power (which could even be larger than the real part) can be recovered leaving the real part as the only power lost.

Method used	Power with Full "on" Pattern
SPICE	6.0 W
Passive sample on Si	7.2 W
1280x1024 AMEL	5.5 W

Table 6: Worst case power estimates for the 1280 AMEL display.

V.6. 1280 x1024 AMEL Display Results

The performance of the resulting AMEL technology from this work is demonstrated with the realization of a 1280 x 1024 display. The operational display mounted on the test system is shown in Fig. 37. Due to the high display resolution, a high magnification of the display, as shown in Fig. 38, is needed to allow the individual pixels to be resolved.

Various optical and electrical characteristics of the completed 1280 x 1024 AMEL display are measured, as discussed in previous sections of this chapter. The measurement results along with the physical characteristics of the display are summarized in Table 7. These measured values demonstrate the success of this development work in achieving the first AMEL display suitable for HMD applications.

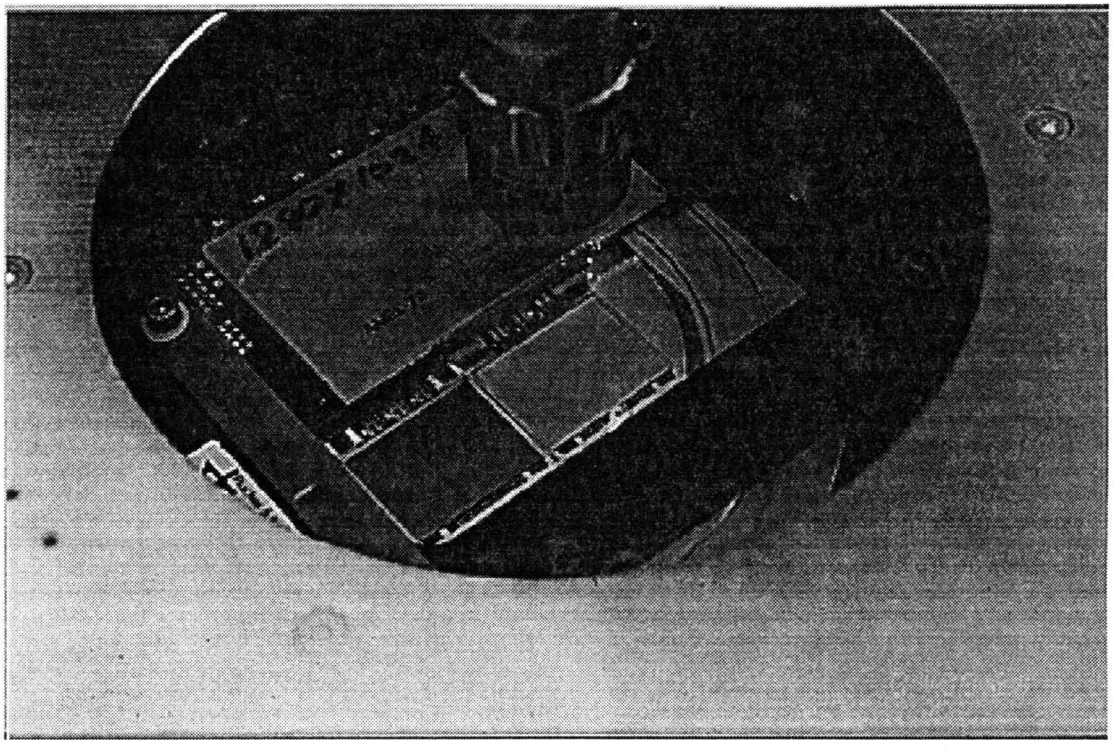

Figure 37: Operational AMEL display in the test system.

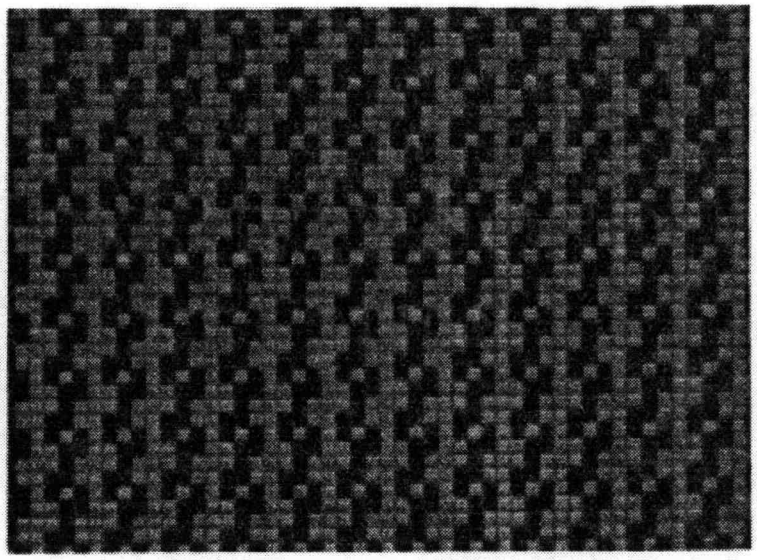

Figure 38: High magnification of the AMEL display.

Parameter	Condition	Value
Dimensions	Pixel Array Viewable Area Total Dimension	1280 by 1024 1.2 in. by 1.0 in. 1.3 in. by 1.1 in.
Resolution	Pixel Density Pixel pitch	1080 lines per inch 24 μm
Weight	Packaged Display	6 grams
Refresh Rate	Data	60 Hz
Illumination Frequency		4.5 kHz sinusoidal 180 V amplitude
Illumination Rate	Max. Brightness Operation	1920 pulses/sec.
Display Power Dissipation (Worst Case)	Max. Bright./All On	6 W
Max. Luminous Output	Areal	150 fL
Luminous Efficiency	Green EL Device	0.25 L/W
Gray Scale	Resolution Capability	6 bits
Contrast Ratio	Off luminance/On luminance	>100:1
Interface	Voltage Bit Length Lead Count HV Control Timing System	0 to 5 volts all digital 40 bits data bus 59 external controlled external
Stability	"On" brightness change	<15%

Table 7: Summary of the AMEL characteristics.

Chapter VI. CONCLUSION AND RECOMMENDATIONS FOR FUTURE WORK

This work has demonstrated a fully operational AMEL display suitable for head-mounted display (HMD) applications. The developments described herein have allowed for the fabrication of EL displays for the first time with the following desirable and unique characteristics:

1. Very high resolution: Fabricated displays with over 1000 lines/inch resolution (24 μm pixel pitch) allow for the realization of a 1280 x 1024 AMEL display within a 1.3" x 1.1" area. The high resolution is achieved due to the employment of a special pixel design utilizing the zener transistor concept.

2. Integrated drivers and EL thin-films: Row and column drivers are incorporated onto the same Si wafer as is used for the EL substrate. This is achieved by utilizing ALE processing and by modifying the standard process to allow for the deposition of EL thin-films directly onto a silicon substrate.

3. Use of commercial IC processing: The IC processing sequence used is very close to that used for commercial silicon products. The use of standard silicon IC processing, which allows the achievement of high yield and low cost, is made possible by modifications of the process flow to allow for Al processing after EL thin-film deposition.

4. High brightness: A high brightness level is realized. High brightness is achieved by solving the brightness saturation problem associated with driving the ALE ZnS:Tb EL films at a high frequency.

5. High quality gray scale: A 64-level gray scale is demonstrated. A new digital gray scale technique is utilized to allow for a linear gray scale while driving the display at a high illumination frequency and the desired voltage.

This work has concentrated on identifying and resolving problems associated with each of the above five goals. The high resolution display goal introduces the issue of placing a high voltage DMOS transistor within the 24 μm x 24 μm pixel area. This

problem is resolved primarily by designing the DMOS transistors on SOI material with a lower voltage capability and operating the DMOS transistor in its breakdown region. The small capacitance (i.e. about 40 fF) of the EL pixel acts as a current limiting element and prevents the transistor from undergoing catastrophic breakdown. A second challenge introduced due to the small pixel pitch is associated with the topography created by the high resolution photolithography steps. This problem is resolved through the use of ALE processing so that the EL thin-film stack could be deposited conformally. At the same time, the process flow is modified to allow for the use of standard silicon IC processing by deposition of Al interconnects after the high temperature EL deposition.

In order to achieve a low number of interconnects and a minimum total display area, it is necessary to incorporate a Si-based peripheral driver. The Si wafer is then used as the EL substrate. The main challenge of using a silicon wafer as the display substrate is to deposit the EL thin-film stack onto the silicon without cracking of the thin-film caused by differences in the thermal coefficients of expansion. The TiO_2 component of the ATO insulator is found to be the main source of the thermal coefficient of expansion mismatch. The thermal coefficient of expansion compatibility problem is resolved by reducing the thickness of the TiO_2 layers in the ATO thin-film, reducing the deposition temperature, and reducing the total EL thin-film thickness.

The high brightness goal is achieved with a minimum power consumption due to the ability to drive the AMEL display with a high frequency waveform. The active matrix approach allows for the separation of the low-voltage addressing waveforms from the high-voltage illumination pulses. The independence of the illumination waveform from the data writing function provides the capability of exciting the pixels with 10 kHz pulses to achieve high brightness levels. A green ALE ZnS:Tb phosphor is chosen for this work due to its linear luminance vs. frequency characteristic. The problem of device heating and brightness saturation is found to be related to the clustering of Tb luminescent impurities in the as-grown ALE phosphor film. This problem is solved by the addition of an RTA step and the associated redistribution of Tb luminescent impurities. Furthermore, a ceramic carrier is used in direct contact with the silicon substrate to remove the generated heat and maintain the display temperature at close to the ambient temperature.

Finally, to achieve an EL display with high quality gray scale performance, a new digital gray scale approach is developed. This gray scale technique is based on dividing each frame into sub-frames and switching the pixels between full-on and full-off stages in each sub-frame separately. The brightness of each pixel is modulated to achieve the desired gray level by adjusting the length of the time that the pixel remains on as well as the amplitude of the applied voltage. This approach utilizes the active matrix approach to

achieve a gray scale while switching the EL pixel only between the on and the full off stages.

These developments have been integrated together in order to fabricate a 1280 x 1024 AMEL display. This display demonstrates a 1000 lpi light emitting display appropriate for a wide range of applications. The combination of EL and active matrix addressing has resulted in a compact, low weight display which provides high brightness at low power levels and a wide operating temperature range. These characteristics not only are ideal for commercial and military HMD applications but also open up the opportunity for direct-view applications such as personal digital assistant (PDA) systems.[99]

Although the work reported in this dissertation demonstrates significant progress in the realization of AMEL displays, further work is required to explore and incorporate additional capabilities and new characteristics. The availability of a color display is always desired by the market and is required for the long term success of any display technology. Lower cost, lower power and higher resolution characteristics would make the display more attractive for large commercial markets. Finally, improvements in device reliability become more crucial as the display moves into a production environment.[32-35] Several suggestions for future work are provided as follows.

1. Replacement of the SOI wafers with other silicon-based substrates: High display cost remains a barrier to large commercial markets. A significant portion of the display cost (over 20%) is based on the use of SOI substrates which cost approximately $250-$350 per wafer. The high substrate cost is further compounded by the fact that SOI processing is specialized and has lower processing yields. As demonstrated in this work, the transistor breakdown voltage only needs to be in the range of the desired modulation voltage, i.e. twice the voltage difference between full-on and full-off. By modifying the EL L-V curve such that a modulation voltage of 20 V is needed, the transistor breakdown voltage can be reduced to as low as 40 V. A transistor with such a breakdown voltage can be fabricated using a bulk silicon substrate and yet achieve a 1000 lpi resolution. This modification allows for the use of lower cost silicon substrates (at a cost of about $20 per wafer) and conventional IC processing which translates into a lower over all display cost. For direct-view applications requiring larger displays, the use of silicon wafers would be prohibitive due to high cost. For large area displays, poly- or amorphous silicon circuitry processed on a cheaper substrate, which could be opaque, would allow for the achievement of an economical final display.

2. Fabrication of full color AMEL: Full color AMEL displays can be achieved by replacing the green-emitting EL phosphor layer with a white phosphor and by adding appropriate filters. Red, green, and blue filters could be distributed in a quad format as shown in Fig. 39. This approach would require a minimal development time since it would use the same silicon substrate as used for monochrome AMEL displays.

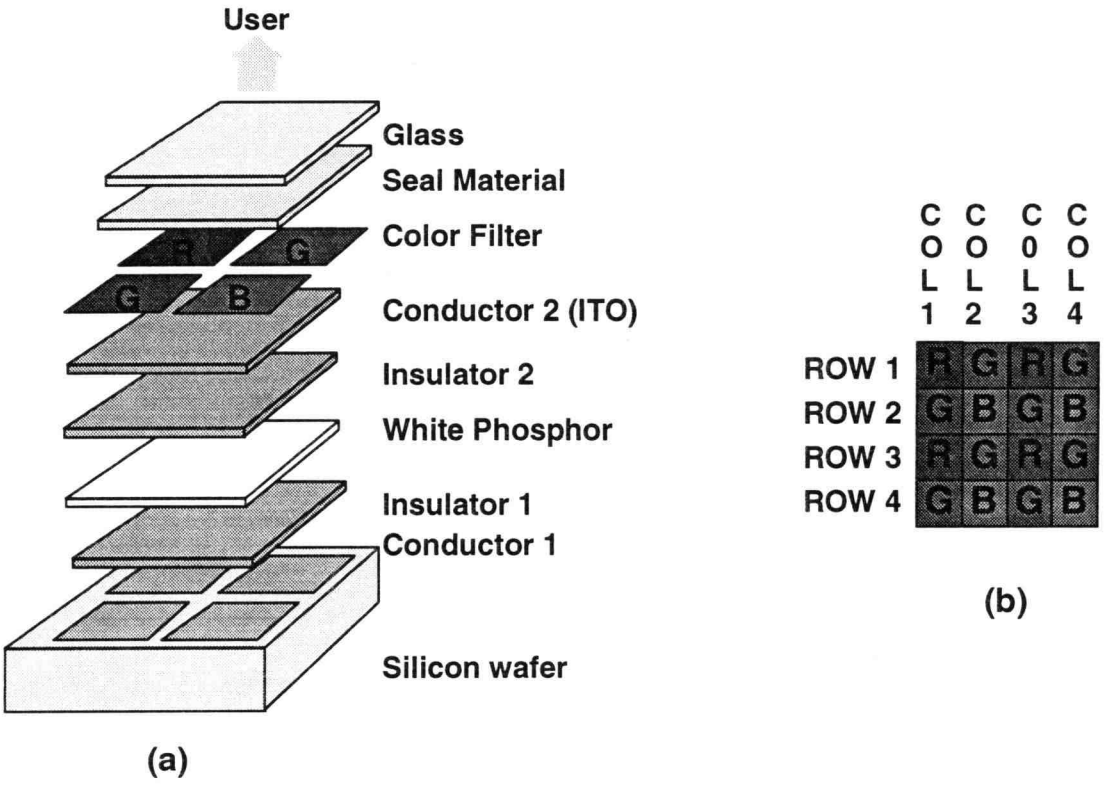

Figure 39: AMEL full color display structure: (a) cross section; (b) top view.

A broad-band phosphor consisting of ZnS:Mn/SrS:Ce is already demonstrated by Planar International researchers.[100] This phosphor is appropriate for use in an AMEL display. Since the EL display is based on solid state thin-films, it is possible to deposit and pattern the color filters directly onto the EL thin-film stack.[23] Fabrication of color filters directly upon the silicon substrate allows for simple alignment since standard aligners can be used.

Furthermore, color filter patterning at the wafer stage of manufacturing allows for the completion of the color filter processing steps on multiple displays on the wafer simultaneously and, hence, a higher throughput.

3. Increased display resolution: A higher display resolution would translate into lower display cost, lower power consumption, and the potential for more compact optics. At 1000 lpi, it is possible to place only four 1280 x 1024 displays on to each wafer. Increasing the resolution will allow for smaller displays to be fabricated with a constant display format. Since the cost of IC processing is primarily dependent on the required silicon area to be processed, a reduction in the display area would reduce the cost. The EL power is directly related to the display area. Therefore, an increase in the resolution by a factor of two will decrease both the cost and power of the display by about a factor of four. Depending on the desired field-of-view, the smaller display size could provide the opportunity to use more compact optics and lower cost lenses. Modified packaging approaches allow the dimensions of the overall display to remain low.[33,34] Finally, a smaller pixel pitch would allow fabrication of multiple displays with larger numbers of pixels, e.g. 2560 x 2048, on a standard silicon wafer.[101]

4. Modifying the insulator structure to allow for a better match between the EL thin-film stack and the Si substrate: In the future, a higher fabrication or RTA temperature, and a thicker EL thin-film stack might be desired to allow for the achievement of a higher brightness. A more optimized choice of the TiO_2 thickness and its location in the ATO layer could be achieved by a systematic study. The goal of this investigation would be to achieve a better CTE match between the EL thin-film and the silicon substrate as well as to evaluate the use of Al_2O_3 between the TiO_2 and Si as a buffer layer to absorb the difference in the dimension changes.

5. Modifying the pixel circuit design: The illumination and addressing paths can be completely separated by connecting the source of the high voltage transistor to ground. If this ground connection is made to the shield or bulk silicon, it would allow a very low resistance path for the current. This modification will allow the display to be driven at even a higher frequency and a higher voltage level. With this modification, the data and illumination voltage paths would be completely separated. This separation allows for the application of high voltage while the data

is being updated, thereby, allowing for a longer time for both illumination pulses and data update. Furthermore, due to the reduced resistance in the path, the efficiency of the power recovery circuit would increase. This modification would, therefore, allow for the realization of a display with higher brightness and reduced power consumption.

REFERENCES

1. J. Gunther, S. Kantyra, and R. Langreth,"The Digital Warrior," Popular Science, p.60, Sept. 1994.

2. Private communications with Dr. Scott Nelson, Honeywell Inc., 1994.

3. T. Perry, "The Media Event," IEEE Spectrum, p. 21, Jan. 1994.

4. A. Pratt, "Weapon," US patent no. 1,183,492, 1916.

5. R. Fischer, "Optics for Head-Mounted Displays," Information Display, 7&8, 1994.

6. R. Khormaei, S. Thayer, K. Ping, C. King, G. Dolny, A. Ipri, F-L Hsueh, R. Stewart, T. Keyser, G. Becker, D. Kagey, M. Spitzer, " High Resolution Active Matrix Electroluminescent Display," Society for Information Display Digest, p. 137, 1994.

7. R. Khormaei, S. Thayer, K. Ping, C. King, G. Dolny, A. Ipri, F-L Hsueh, D. Furst, R. Stewart, T. Keyser, G. Becker, D. Kagey, M. Spitzer, M. Batty, "High Resolution AC Thin Film Electroluminescence Using Active Matrix on Si Substrate," SPIE HMD Conference Proceedings, Vol. 2218, p. 25, April 1994.

8. R. Khormaei, "The Common Display from Portable Computers to HDTV and Virtual Reality: Active Matrix EL," Invited Talk, Oregon Center for Advanced Technology Education's series on advances in display technology, Feb. 18, 1994.

9. G. Dolny, A. Ipri, F-L Hsueh, R. Stewart, R. Khormaei, S. Thayer, T. Keyser, G. Becker, M. Spitzer, M. Batty, "High Density Active Matrix Electroluminescent Display Using Single Crystal Silicon-on-Insulator High-Voltage IC Technology," IEDM Technical Digest, p. 930, 1993.

10. G. Dolny, A. Ipri, F-L Hsueh, R. Stewart, J. Atherton, D. Jose, M. Spitzer, D-P. Vu, M. Batty, R. Khormaei, S. Thayer, T. Keyser, G. Becker, M. Tilton, R. Rhoades, R. Ellis, H. Franklin,"The Application of Silicon-on-Insulator (SOI) Technology for the Fabrication of Fully Scanned Active Matrix Flat Panel Displays," IEEE International SOI Conference Proceedings, p. 97, 1994.

11. R. Khormaei, K. Ping, M. Rhoads, B. Aitchison, C. King, G. Dolny, A. Ipri, F-L Hsueh, R. Stewart, T. Keyser, G. Becker, D. Kagey, M. Spitzer, " A 1280x1024 active matrix EL with 1000 lpi resolution," 1995 Society for Information Display Conference, to be submitted.

12. I. Khormaei, J. Wager, C. King, "Improved Stability of ZnS:Mn ACTFEL Devices", Society for Information Display Digest, p. 66, 1989.

13. R. Khormaei, C. King, R. Coovert, J. Wager, "Stabilization of ZnS:Mn ACTFEL Devices through Processing Modifications" Society for Information Display Digest, p.74, 1991.

14. J. Davidson, J. Wager, I. Khormaei, C. King, "Aging Instabilities of ZnS:Mn AC Thin-Film Electroluminescent Devices," ACTA Polytical Scandinavia ph170, p. 185, 1990.

15. D. Morton, J. Koh, C. Hogh, R. Khormaei, "Study of the Effects of Aging on the Relaxation Luminance in Atomic Layer Epitaxy ZnS:Mn Alternating-Current Thin-Film Electroluminescent Devices," Appl. Phys. Lett. 63(7), P. 863, 1993.

16. I. Khormaei, "Improvement in Stability of ACTFEL Devices," M.S. Thesis, Oregon State University, June 1989.

17. R. McArthur, J. Davidson, J. Wager, I. Khormaei, C. King, "Capacitance - Voltage Characteristics of AC Thin-Film Electroluminescent Devices," Appl. Phys. Lett. 56, p. 1889, 1990.

18. R. McArthur, J. Davidson, J. Wager, I. Khormaei, C. King, "Characterization of ZnS:Mn AC Thin-Film Electroluminescent Devices by Capacitance-Voltage Analysis," ACTA Polytical Scandinavia ph170, p. 181, 1990.

19. J. Davidson, J. Wager, I. Khormaei, "Electrical Characterization and SPICE Modeling of ZnS:Mn ACTFEL Devices," Society for Information Display Digest, p. 77, 1991.

20. J. Davidson, J. Wager, R. Khormaei, C. King, R. Williams, "Electrical Characterization and Modeling of Alternating Current Thin-Film Electroluminescent Devices," IEEE Transactions on Electron Devices, Vol. 39, p. 1122, 1992.

21. M. Åberg, R. Khormaei, C. King, "A Large Area 1024 x 768 Line ACTFEL Display with Non-Split Columns," Proceedings of the sixth international workshop on electroluminescence, p.352, 1992.

22. M. Åberg, R. Khormaei, "A Large Area 1024 x 768 Line ACTFEL Display with Non-Split Columns," Scientific Report, Technical Research Center of Finland (VTT), p. 8, 1991.

23. S. Sun, R. Khormaei, "Variation of the characteristics of ZnS:Mn AC Thin Film Electroluminescent Devices with Insulators," SPIE Proceedings-High resolution display and projection systems, Volume 1664, p. 48, 1992.

24. C. Laakso, R. Khormaei, C. King, G. Harkönen, A. Pakkala, T. Pitkänen, M. Surma-aho, R. Törnqvist, "A 9 Inch Diagonal, Compact, Multicolor ACFEL Display,"

Conference Record of the International Display Research Conference Proceedings, p. 43 , 1991.

25. R. Khormaei, C. Walker, "Modeling the Electron Emission in ZnS:Mn ACTFEL," Conference Record of the International Display Research Conference Proceedings, p. 233, 1994.

26. I. Khormaei, "Compensation Drive Approach for ACTFEL Displays"; US. Patent, Pending, Serial No. 08/216,246.

27. I. Khormaei, "Compensation Drive Approach for ACTFEL Displays"; Japanese Patent, Pending, Serial No. 286,676/93.

28. I. Khormaei, "An Approach for Active Matrix EL Cell Design," US Patent, Pending, Serial No. 08/293,144.

29. I. Khormaei, K. Ping, S. Thayer, "Direct Patterning of Color Filters Over Electroluminescent Displays," US patent, pending, Serial No. 08/258,533.

30. I. Khormaei, and C. King, "Time Multiplexed GS Approach," US patent, pending.

31. I. Khormaei, and C. King, "Temporal gray scale approach for Passive Matrix Displays," US patent, pending.

32. K. Ping, I. Khormaei, and C. King, "Methods for Isolation of the Burnouts in Active Matrix Electroluminescent Displays," US patent application in progress.

33. C. King, I. Khormaei, B. Aitchison, and M. Rhoads, "Use of MCM Substrate as Carriers for EL Displays," US patent application in progress,.

34. A. Friedman, I. Khormaei, and K. Boris, "Compact Packaging for AMEL Displays," US patent application in progress.

35. S. Thayer, I. Khormaei, "Use of Topography to Increase Light Outcoupling in AMEL Displays," US patent application in progress.

36. K. Werner, "The Flat Panel's Future," IEEE Spectrum, p. 18, Nov. 1993.

37. T. Scheffer, "Direct-Multiplexed Liquid-Crystal Displays," SID seminal lecture notes, p. 4/1-34, 1987.

38. S. Mikoshiba, "Plasma Displays," SID seminal lecture notes, p. F-2/1-31, 1993.

39. M. Aven and J. Prener, Editors, Physics and Chemistry of II-VI compounds, John Wiley & Sons, Inc., pp. 613-658, 1967.

40. M. Russ, and D. Kennedy, "The Effects of Double Insulating Layers on the Electroluminescence of Evaporated ZnS:Mn Films," J. Electrochem. Soc., p. 1066, 1967.

41. T. Inoguchi, M. Takeda, Y. Kakihara, and M. Yoshida, " Stable High Luminance Thin-Film Electroluminescent Panels," Society for Information Display Digest, p. 86, 1974.

42. P. Alt, "Thin Film Electroluminescent Displays: Device Characteristics and Performance," SID Seminal Lecture Notes, pp. 1.2/1-57, 1983.

43. A. Marfnin (translated by N. Egorova, and A. Mishchenko), Physics of Minerals and Inorganic Materials, Springer-Verlag, pp. 46-64, 1979.

44. R.Boyn, "4f-4f Luminance of Rare-Earth Centers in II-VI Compounds," Phys. Stat. Sol. (b), 148, p. 11, 1988.

45. D. Kupra, "Hot-Electron Impact Excitation of Tb^{3+} Luminescence in ZnS:Tb^{3+} Thin Films ," J. Appl. Phys. 43(2), p. 476, 1972.

46. K. Chopra, Thin Film Phenomena, Robert E. Krieger Publishing Company, pp. 11-22, 1979

47. J. Vossen, and W. Kern (Editors), Thin Film Processes, Academic Press, pp. 131-170, 1978.

48. T. Suntola and M. Antson, "Method for Producing Compound Thin Films," U.S. Patent No. 4,058,430, 1977.

49. T. Suntola, "Atomic Layer Epitaxy", Material Science Reports, volume 4, Number 7, p. 266, Dec. 1989.

50. R. Törnqvist, T. Harju, J. Honkala, J. Vilijänen, M. Åberg, and H. Kattelus, "Low-Power Thin-Film Electroluminescent Display," Society for Information Display Digest, p.63, 1991.

51. T. Brody, F. Luo, Z. Szepesi, and D. Davies, "A 6x6-in 20-lpi Electroluminescent Display Panel," IEEE transactions on electron devices, Vol. ED-22, No.9, p.739, 1975.

52. B. Lechner, F. Marlowe, E. Nester, and J. Tults, "Liquid Crystal Matrix Displays," Proceedings of the IEEE, Vol.59, No. 11, p. 1566, 1971.

53. W. Howard, "Active Matrix LCDs," SID Seminar Lecture Notes, p F-2/3, 1992.

54. Z. Kun, F. Luo, and J. Murphy, "Thin-Film Transistor Switching of Thin-Film Electroluminescent Display Elements," Proceedings of the SID, Vol.21/2, p. 236, 1980.

55. K. Oki, Y. Ohkawa, K. Takahara, and S. Miura, " MOS-EL Integrated Display Device," Society for Information Display Digest, p. 266, 1982.

56. T. Suzuki, Y. Uno, J. Sakurai, Y. Sato, S. Kyozuka, N. Hiji, and T. Ozawa, "The Fabrication of TFEL Displays Driven by a-Si TFTs," Society for Information Display Digest, p. 344, 1992.

57. T. Unagami, and O. Kogure, "High Voltage TFT Fabrication in Recrystallized Polysilicon," IEEE Transactions on Electron Devices, Vol. 35, No. 3, p. 314, 1988.

58. J. Vanfleteren, P. Visschere, J. Baets, I. Rycke, J. Doutreloigne, and M. Maenpaa, "Active Matrix CdSe TFT Addressed Electroluminescent Displays," Conference Record of the International Display Research Conference Proceedings, p. 75, 1988.

59. J. Vanfleteren, J. Capon, J. Baets, I. Rycke, H. Smet, J. Doutreloigne, A. Van Calster, P. Visschere, K. Sallmén, R. Graeffe, " Evaluation of a 64x64 CdSe TFT Addressed ACTFEL Display Demonstrator," Conference Record of the International Display Research Conference Proceedings, p. 134, 1991.

60. Private Communications with Dr. Peter Brody, Active Matrix Associates, 1994

61. S. Steiner, and H. Tsoi, "High-Performance Column Driver for Gray-Scale TFEL Displays," Society for Information Display Digest, p. 31, 1988.

62. M. Åberg, "Charge Modulation Gray-Scale Method with Profiled Current Pulses for ACTFEL Displays," Society for Information Display Digest, p. 765, 1993.

63. M. Åberg, " An Electroluminescent Display Simulation System and its Application for Developing Grey Scale Driving Methods," ACTA Polytical Scandinavica, Electrical Engineering Series No. 74, 1993.

64. C. Jung, T. Gielow, and R. Holly, "Enhanced Shading on TFEL Displays," SID Digest, p. 236, 1990.

65. W. Barrow, R. Coovert, E. Dickey, C. King, C. Laakso, S. Sun, R. Tuenge, R. Wentross, J. Kane, "A New Class of Blue TFEL Phosphors with Application to a VGA Full-Color Display," Society for Information Display Digest, p. 761, 1993.

66. J. Haaranen, R. Törnqvist, J. Koponen, T. Pitkänen, M. Surma-aho, W. Barrow, and C. Laakso, "A 9-in.-Diagonal High-Contrast Multicolor TFEL Display," Society for Information Display Digest, p. 348, 1992.

67. Y. Tsuchiya, S. Miyamoto, T. Kuki, S. Okamoto, K. Kobayashi, S. Takahashi, T. Ishida, S. Morokawa, "20 μm Pitch ZnS:Tb TFEL Displays," Eurodisplay Conference Proceedings, p.225, 1993.

68. R. Stewart, "Active matrix Electroluminescent Display and Method of Operation", US Patent No. 5,302,966, 1994.

69. Private communications with Dr. Gary Dolny, David Sarnoff Research Center, 1992.

70. Private communications with Mr. Ben Choy, Supertex Inc., 1992.

71. Based on PISCES simulation performed by Dr. Gary Dolny, David Sarnoff Research Center, 1992.

72. S. Wolfe and R. Tauber, Silicon Processing for the VLSI Era, Volume 1, Lattice Press, pp. 66-83, 1990.

73. S. Sze, Physics of Semiconductor Devices, John Wiley & Sons, pp. 489-490,1981

74. D. Smith, "Modeling AC Thin-Film EL Devices", J. of Luminescence, 23, p.209, 1981.

75. Private communications with Dr. Fu-Lung Hsueh, David Sarnoff Research Center, 1992.

76. R. Flegal and C. King, "Differential Aging Effects in ACTFEL Displays," Society for Information Display Digest, p. 177, 1988.

77. R. Flegal, "Transformer-Coupled Drive Network for a TFEL Panel," US Patent No. 4,733,228.

78. P. Alt, D. Dove, and W. Howard, "Experimental Results on the Stability of AC Thin Film Electroluminescent Devices," J. Appl. Phys. 53(7), p. 5186, 1982.

79. K. Taniguchi, K. Tananaka, T. Ogura, Y. Kakihara, S. Nakajima, and T. Inoguchi, "EL Device with Stable Memory Effect," Proceedings of the SID, Vol. 26/3, p. 231, 1985.

80. M. Nishikawa, T. Matsuoka, T. Toka, Y. Fujita, J. Kuwata, and A. Abe, "A Highly Stable TFEL Panel with CaS Buffer Layer," Society for Information Display Digest, p. 19, 1988.

81. S. Wolfe and R. Tauber, Silicon Processing for the VLSI Era, Volume 1, Lattice Press, p. 42, 1990.

82. SEM was performed by Dr. Tom Keyser, AlliedSignal Aerospace, 1993.

83. S. Wolfe and R. Tauber, Silicon Processing for the VLSI Era, Volume 1, Lattice Press, pp. 114-117, 1990.

84. Private communications with Dr. Tom Keyser, AlliedSignal Aerospace. The stress measurements were performed at AlliedSignal MTC plant, MD, 1994.

85. Private communications with Mr. Eric Dickey, Planar Systems Inc., 1993.

86. Also based on private communications with Dr. Runar Törqvist, Planar International Oy., 1993.

87. Private communications with Dr. Bernard Fretz, Honeywell Inc.

88. Measurements were performed with assistance from Mr. Long Pham, Oregon State University, 1994.

89. A. Abu-Dayah, S. Kobayashi, and J. Wager, "Internal Charge-Phosphor field Characteristics of Alternating-Current Thin-Film Electroluminescent Devices," Appl. Phys. Lett., 62, p. 744, 1993.

90. E. Bringuier, "Tentative Anatomy of ZnS-type electroluminescence," J. Appl. Phys. 75(9), p. 4291, 1994.

91. A. Mikami, T. Ogura, K. Taniguchi, M. Yoshida, and S. Nakajuma, "Excitation Process of Tb emission center in a ZnS:Tb,F thin-film electroluminescent device", J. Appl. phys. 64(7), p. 3650, 1988.

92. Private communications with Dr. Dick Tuenge, Planar Systems, Inc., 1994.

93. D. Briggs, and M. Seah (Editors), Practical Surface Analysis, John Wiley and Sons, Inc., 1983.

94. The fabrication and Auger interpretations were done with assistance from Dr. Dick Tuenge and Mr. Eric Dickey, Planar Systems Inc., 1994.

95. P. Tipler, Physics, Second Edition, Volume 2, Worth Publishers, Inc., pp. 858-862, 1982.

96. Measurements were performed with assistance from Mr. Brad Aitchison, Planar Systems, Inc., 1994

97. J.M. Cone, "Survey of Display Ergonomic Standards and Requirements," SID seminal lecture notes, pp. F-6/1, 1994.

98. Power estimates were completed with assistance from Mr. Monte Rhoads, Planar Systems Inc., 1994.

99. T. Halfhill, " PDAs Arrive: But Aren't Quite Here Yet," BYTE, p. 66, 1993.

100. M. Leppänen, G. Harkonen, A. Pakkala, E. Soinen, R. Tornqvist, "Broadband Double Layer Phosphor for an Inverted Filtered RGB Electroluminescent Displays," EuroDisplay, p. 232, 1993.

101. Team of companies with Kopin Corporation as prime contractor, "Development of Advanced Technology for 2000 DPI Head-Mounted Displays," ARPA Contract no. MDA972-94-C-0023, 1994.