AN ABSTRACT OF THE THESIS OF

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Title: Design of a Low Jitter Digital PLL with Low Input Frequency

Abstract approved:

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Complex digital circuits such as microprocessors typically require support circuitry that has traditionally been realized using analog or mixed-signal macros. PLL circuits are used in many integrated applications such as frequency synthesizers and inter-chip communication interfaces. As process technologies advance and grow in complexity, the challenge of maintaining required analog elements and performance for use in circuits such as PLLs grows. Recently, digital PLL (DPLL) has emerged as an alternative to analog PLL to overcome many constraints such as low supply voltage, poor analog transistor behavior, larger area due to integrated capacitor and process variability. However, DPLLs have high deterministic jitter due to quantization noise of time-to-digital converter (TDC) and digitally-controlled oscillator (DCO) and struggle with random jitter of oscillator.

In this thesis, hybrid analog/digital proportional/integral control is used to suppress TDC quantization error and digital phase accumulation techniques to mitigate DCO quantization error. VCO phase noise was reduced using an embedded voltage-mode feedback. This feedback loop is implemented by using a switched-C circuit which converts frequency to current. Designed in a 130nm CMOS process, the proposed DPLL generates more than 1GHz output frequency with low input frequency and achieves superior jitter performance compared to conventional DPLL in simulations.

Design of a Low Jitter Digital PLL with Low Input Frequency

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APPROVED:

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Seokmin Jung, Author

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1 Introduction

Complex digital circuits such as microprocessors typically require support circuitry that has traditionally been realized using analog or mixed-signal macros. A critical example of such a support circuit is the phase-locked loop (PLL). PLL circuits are traditionally used in many integrated applications such as frequency synthesizers and inter-chip communication interfaces [2, 5]. As process technologies advance and grow in complexity, the challenge of maintaining required analog elements and performance for use in circuits such as PLLs grows. For example, a charge pump PLL (CPPLL) is commonly used to synchronize a pixel clock to the horizontal sync signal in flat panel display [1]. Due to the leakage current in the filter capacitor, the total jitter of the CPPLL is greatly increased. And there are other constraints such as low supply voltage, poor analog transistor behavior, larger area due to integrated capacitor and process variability. To overcome these problems, digital PLL (DPLL) [3, 4, 9, 15] has recently emerged as an alternative to analog PLL. A digital loop filter is used in a DPLL with all-digital implementation that avoid the poor analog transistor behavior and intrinsic technology limitation. However, DPLLs have higher deterministic jitter due to higher quantization noise of time-to-digital converter (TDC) and digitally-controlled oscillator (DCO) and struggle with random jitter of oscillator.

1.1 Overview of Digital PLL

Conventional 3rd order type II PLL architecture consists of a phase frequency detector (PFD), a charge pump (CP), a 2nd order loop filter (LF), a Voltage-Controlled Oscillator (VCO), and a feedback divider as shown in Fig. 1.1.

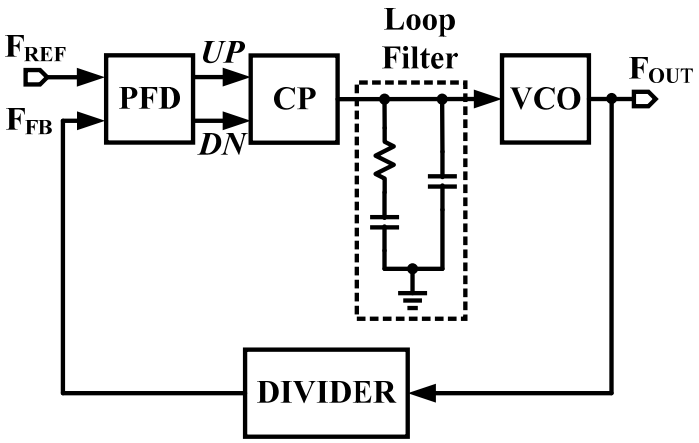

Figure 1.1: Conventional 3rd order type II PLL architecture.

A PFD compares the phase and frequency difference between F_{REF} and F_{FB} and then sends information about phase or frequency difference to the CP through UP and DN outputs. When close to lock, only phase differences are detected. When out of lock, the PFD also detects frequency differences in order to prevent harmonic locking. The CP is comprised of two switched current sources, providing charging current and discharging current to the loop filter. The current sources are activated through two switches which are controlled by the output of the PFD. A net charge is dumped into or withdrawn from the LF, which contains a charge-integrating capacitor, depending on the phase difference information. If F_{REF} leads F_{FB}, the CP receives an UP signal and current is driven into the LF. Conversely, if F_{REF} leads F_{FB}, it receives a DN signal and current is drawn from the LF. The LF filters out jitter by removing glitches from the CP and preventing voltage over-shoot. In order to stabilize the system, a zero must be introduced into the loop, by adding a resistor in series with the filter capacitor. The combination of CP and LF is an integrator that generates an average value proportional to phase and frequency error. Based on the average control voltage, the VCO oscillates at a higher or lower frequency, which affects the phase and frequency of the feedback signal. When phase is locked, the phase error is zero and control voltage remains stable, along with the VCO output frequency. The divider in the feedback path divides down F_{OUT} to a lower feedback clock

frequency F_{FB} and achieves phase lock with F_{REF}. Therefore F_{OUT} is N times larger than F_{REF}.

An alternative PLL design is digital PLL. The simplified block diagram of DPLL [6] is shown in Fig. 1.2. The PFD and CP in analog PLL are replaced with a time-to-digital converter (TDC) that converts the phase difference into digital output. A bang-bang phase detector (BBPD) that is implemented by a simple D flip-flop (DFF) is a 1bit TDC. The digital output of TDC is filtered by the digital loop filter (DLF) and then to control the input digit of digitally-controlled oscillator (DCO). DCO can be implemented with different ways. For a ring oscillator based DCO, digital control can be realized by tuning on and off the switches or tri-state inverters. For a LC based DCO [10, 19], frequency tuning is done by selecting the tank capacitor bank. Besides, using a digital-to-analog converter (DAC) in front of a VCO to convert digital input to voltage or current is also a practical way to design a DCO.

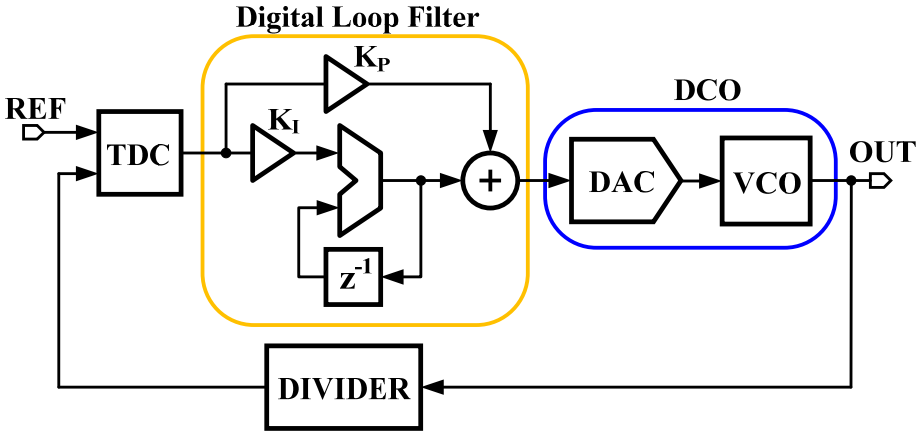

Figure 1.2: DPLL Block Diagram.

Deterministic jitter (DJ) is a jitter source PLL design, which mainly comes from the reference spur, loop latency, quantization error, etc. Reference spur are spurious emissions that occur from the carrier frequency at an offset equal to the channel spacing. These are usually caused by leakage and mismatch in the charge pump of a CPPLL. The loop latency causes delay in PLL loop response and dithering jitter at the output.

Quantization errors coming from TDC and DCO usually exist in the digit-assisted PLL that is raised by the finite resolution in digital circuits.

Phase Noise is another essential parameter for PLL design that determines root-mean-square (rms) jitter. The phase noise spectral density of a PLL system refers to the noise power of the PLL versus the offset frequency. Close to the carrier, within the loop bandwidth of the PLL, this noise is commonly dominated by the PD, and farther out, it is typically dominated by the VCO. The PLL loop bandwidth is optimally chosen to minimize rms phase error.

1.2 Motivation

In spite of many advantages of the DPLL, the DPLL presents several circuit design bottlenecks that have limited its usage in high performance applications. The key performance limiting factors of the DPLL are discussed next.

First, conventional TDCs quantize the phase error in steps of an inverter delay and this TDC quantization error affects deterministic jitter at DPLL output. The DJ caused by TDC quantization error is proportional to the proportional path gain. In order to reduce the DJ, it is necessary to design the TDC with small step size, that is, high resolution TDC and optimize the proportional path gain in case of using large divider value.

The second challenge is the design of a high resolution DCO. One way to implement DCO is to utilize a DAC in front of the VCO. As a result, the finite resolution of the DAC manifests itself as frequency quantization error. Furthermore, the DCO suffers from an inconvenient tradeoff between frequency resolution and tuning range. For instance, with a given DAC resolution of L+1 bits and a required frequency resolution of ΔF, the DCO tuning range is limited to $\pm 2^{L} \times \Delta F$.

Finally, the DPLL also suffers from an inherent noise bandwidth tradeoff: suppression of the large phase noise of ring-based DCO requires a wide loop bandwidth, while it can be easily shown that a low loop bandwidth is needed to mitigate the TDC quantization

error. In order to reduce the burden of optimum bandwidth, DCO is needed to get excellent phase noise. For example, in [19] an LC-based DCO is combined with a very low PLL bandwidth to suppress the TDC quantization error.

This thesis is targeted to analyze the noise factor for output jitter and improve the design bottlenecks of conventional DPLL, explore the design techniques of low jitter DPLL.

1.3 Thesis Organization

This thesis is organized as follows:

Chapter 2 presents a jitter analysis for design method of low jitter digital PLLs. Each noise sources are analyzed and solutions are discussed. So, we are able to suggest the proposed architecture for low jitter digital PLL.

Chapter 3 discusses the circuit implementation of proposed architecture and presents simulation results of low jitter digital PLL. Hybrid analog/digital proportional/integral control is used to suppress TDC quantization error and digital phase accumulation techniques to mitigate DCO quantization error. VCO phase noise was reduced using an embedded voltage-mode feedback. This feedback loop is implemented by using a switched-C circuit which converts frequency to current.

Finally, the thesis is concluded in Chapter 4 by providing a summary of the contributions and directions for further research.

2 Jitter Analysis in digital PLL and Proposed Architecture

2.1 Digital PLL Noise Model

In order to quantify the DPLL phase noise and identify the noise contributions from each noise source, a frequency domain analysis of a closed-loop PLL is needed. The noise sources of a typical DPLL are shown in Fig. 2.1 [6, 18].

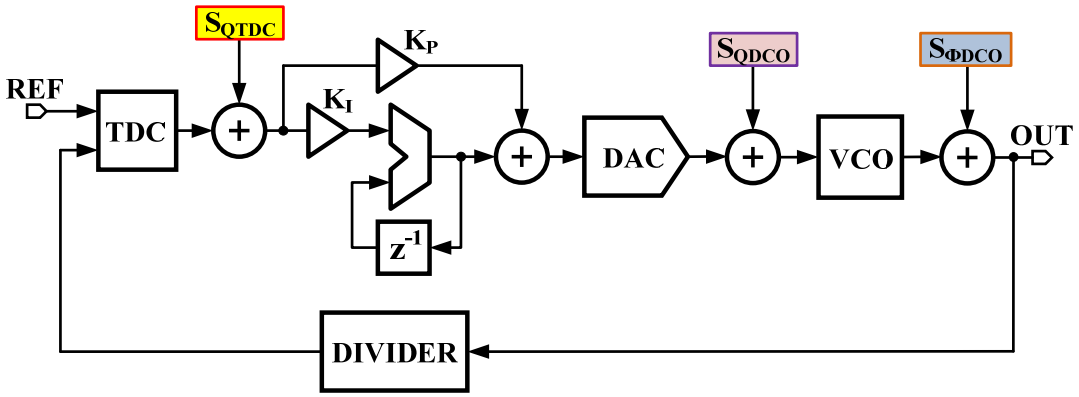

Figure 2.1: Noise Sources in DPLL.

The main DJ sources are the TDC quantization error S_{QTDC} and DCO quantization error S_{QDCO}. S_{QTDC} and S_{QDCO} are caused by limited resolution in the circuit. Assuming uniform distribution for the quantization error, it can be easily shown that

$$S_{Q_{TDC}} = \frac{\Delta\Phi^2}{12F_{REF}}, \quad S_{Q_{DCO}} = \frac{\Delta F^2}{12F_{REF}} \tag{2.1}$$

where $\Delta\Phi$ and ΔF are the resolution of the TDC and the DCO, respectively [20]. F_{REF} is the DPLL reference frequency.

The RJ sources are mainly the results of intrinsic noise sources such as thermal and flicker noise, including TDC noise, DLF noise and DCO noise $S_{\Phi DCO}$. It's easy to prove that $S_{\Phi DCO}$ is the dominant noise source for RJ, so we consider only $S_{\Phi DCO}$ in this analysis.

2.2 Deterministic Jitter

Deterministic jitter is a type of jitter with a known non-Gaussian probability distribution. The peak-to-peak value of this jitter is bounded, and the bounds can be observed, repeated and predicted. In the DPLL design, the quantization error dominates DJ performance. There are two quantization error sources in DPLL: TDC quantization error and DCO quantization error.

2.2.1 TDC Quantization Error

The TDC quantizes the time difference between reference clock F_{REF} and feedback clock F_{FB} and converts it to a digital format. The delay line based flash TDC [13] is composed of a string of non-inverting delay elements (such as buffers), a number of registers (such as D flip-flops) and a thermometer-to-binary code convertor. The TDC quantizes the phase error in steps of an inverter delay. As can be seen, the TDC quantization error is proportional to its resolution, while the resolution is limited to the minimum achievable inverter delay in a given process. For example, even in a 90nm CMOS processes, the TDC step size is only about 20ps. This rather poor resolution manifests itself as phase-quantization error which, if left unfiltered, appears as deterministic jitter at the DPLL output.

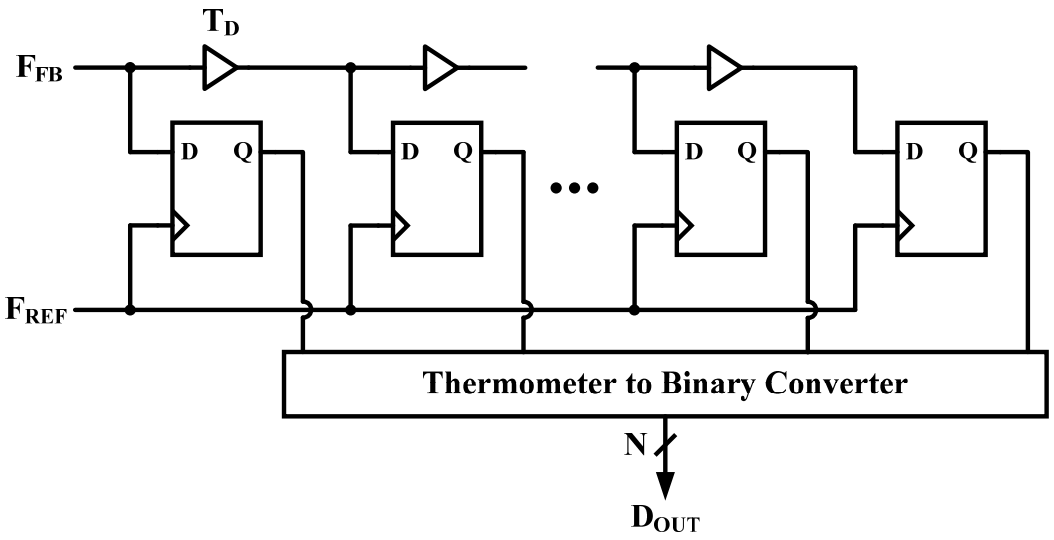

Figure 2.2: Delay line based flash TDC.

Alternative approaches of TDC architecture are reported in recent publications [7, 11] to achieve high resolution and small quantization error. [7] proposed a Vernier delay line based TDC to achieve a resolution better than a single delay element. However, a calibration method has to be used to improve the TDC linearity due to the matching of multiple delay lines. [11] uses alternative architectures to achieve high resolution TDC that is not constrained by invertor delay, however it increases the circuit complexity and power consumption in a great amount.

Another issue is TDC quantization error affects the output jitter through the proportional path as illustrated in Fig. 2.3.

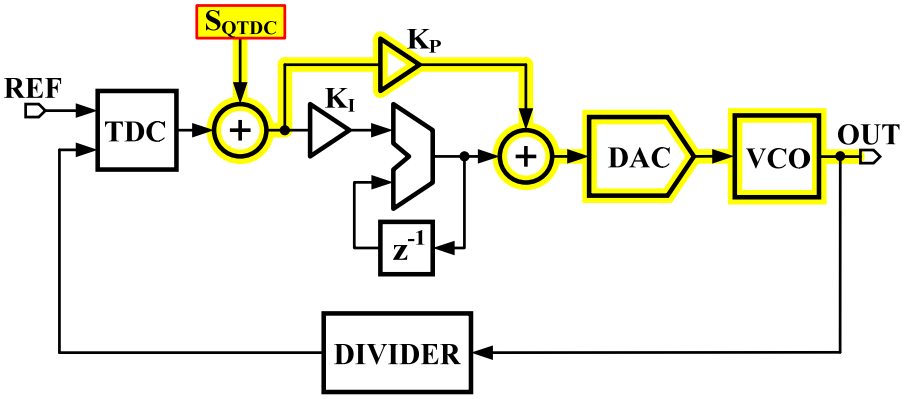

Figure 2.3: TDC quantization error effect.

The DJ is proportional to the proportional path gain, which is composed of K_P, K_{DCO} and N. For example, if the $K_P \times K_{DCO}$ is 100kHz and N is 1000 at 1GHz output frequency then the DJ equals to 100ps. Conventional digital PLL is using small N value to avoid this problem. However, N should be a large number in video pixel clock generation applications because of low input frequency.

To reduce the DJ in DPLL, we can remove K_P from the feed-forward as illustrated in Fig. 2.4.

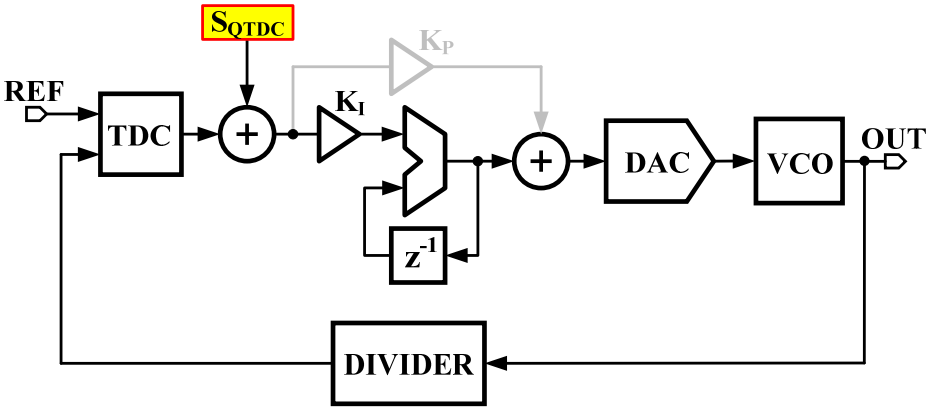

Figure 2.4: Remove K_P from feed-forward path.

However, this structure gives rise to the stability issue in DPLL. There are two integrators in this loop. One is digital accumulator in the digital loop filter and another is phase integrator in VCO. Because of these two integrators, the loop becomes unstable.

We are able to recall the conventional compensation [16] to solve the stability problem. The feed-forward path should be added across the digital accumulator as illustrated in Fig. 2.5.

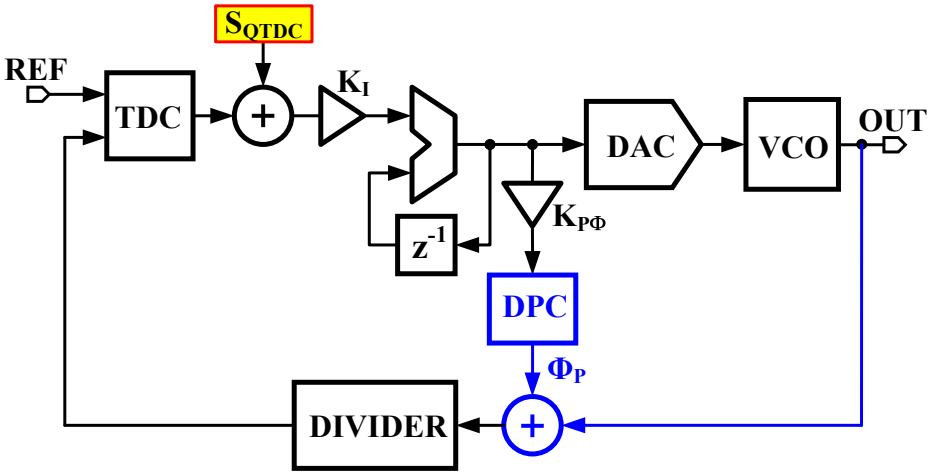

Figure 2.5: Phase-domain proportional path.

Phase-domain proportional control should be needed to connect the feed-forward path because the VCO output is phase in s-domain. The digital-to-phase converter changes the digital output ($K_{P\Phi}$) of digital filter to phase (Φ_P). The stability of this loop can be guaranteed by ensuring the output phase change due to the proportional path dominates the phase change due to the integral path. A large ratio of the proportional path gain over the integral path gain ensures that loop dynamics are dominated by the proportional path, thereby achieving an under-damped response. Therefore, the integral path gain is much smaller than of the proportional path gain and the proposed DPLL can suppress the TDC quantization error by removing K_P from the feed-forward path.

2.2.2 DCO Quantization Error

The DCO quantization error is another source of DJ that is limited by the design requirement of a high resolution DCO. As a DCO is normally designed with a DAC and a VCO, thus the requirement becomes to implement a high resolution DAC. The finite resolution of the DAC manifests itself as DCO frequency quantization error, which is another important source of deterministic jitter, while as known a high resolution DAC is a challenging design task. The DJ is proportional to the frequency step size, update rate and loop latency. So, the DJ can be shown that

$$DJ \approx \frac{F_{LSB} \cdot N}{F_{OUT}^2} \tag{2.2}$$

where F_{LSB} is frequency resolution of DCO, N is divider ratio and F_{OUT} is output frequency.

When F_{OUT} is 1GHz and N is 1024, the DJ is illustrated in Fig. 2.6. In order to reduce the DJ, we have to apply the low frequency resolution.

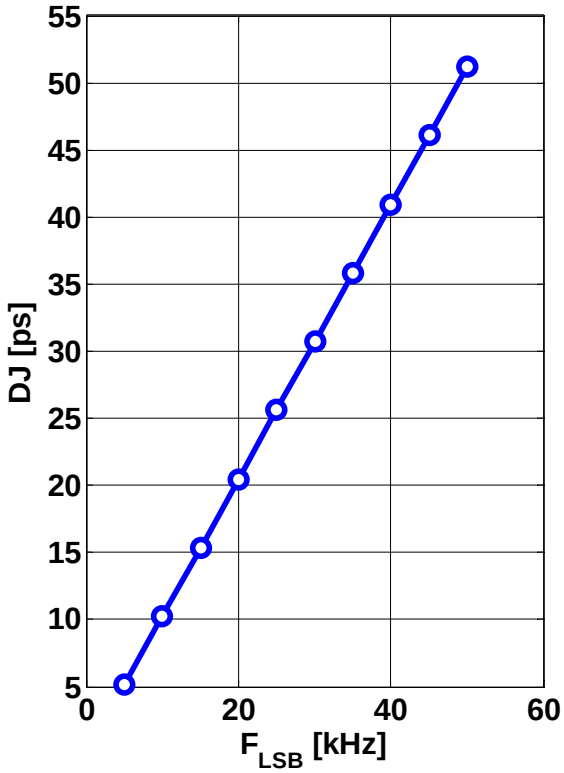

Figure 2.6: DJ vs. F_{LSB}.

There are considerations to get a required DCO resolution. As the N is increased, the F_{LSB} should be decreased for a fixed DJ of 5ps at 1GHz output frequency as illustrated in Fig. 2.7.

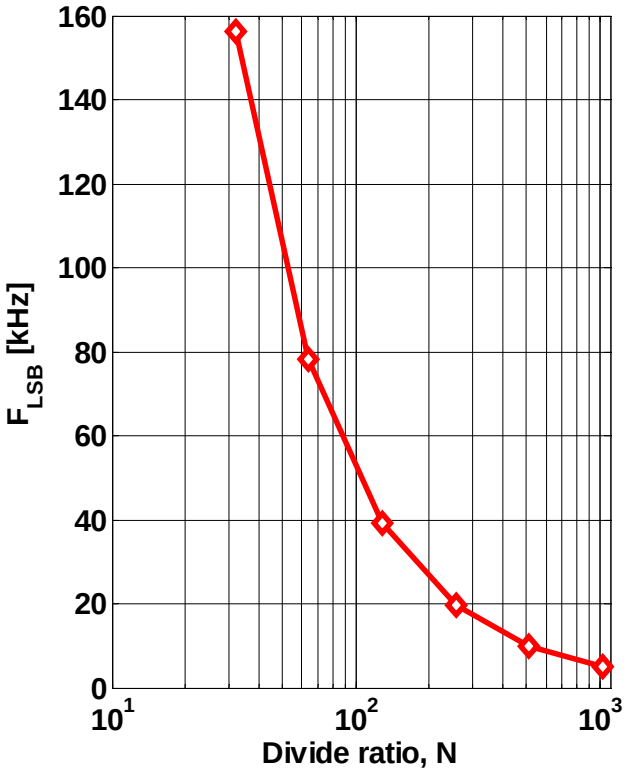

Figure 2.7: DCO resolution tradeoff – F_{LSB} vs. divider ratio.

Furthermore, as a wide tuning range is always necessary in a digital PLL design, there exists a tradeoff between the DCO frequency resolution and tuning range [8]. For instance, with a given DAC resolution of L+1 bits and a required frequency resolution of ΔF, the DCO tuning range is limited to ±2L × ΔF. So, the DAC resolution should be increased to get a wide tuning range for a fixed DJ of 5ps at 1GHz output frequency as illustrated in Fig. 2.8. Hence, a DAC with large number of bits is needed to achieve a low frequency resolution of DCO and high DAC resolution for a low DJ and wide tuning range. However in this way it greatly increases the circuit complexity and power consumption and degrades the figure of merit of the DPLL design.

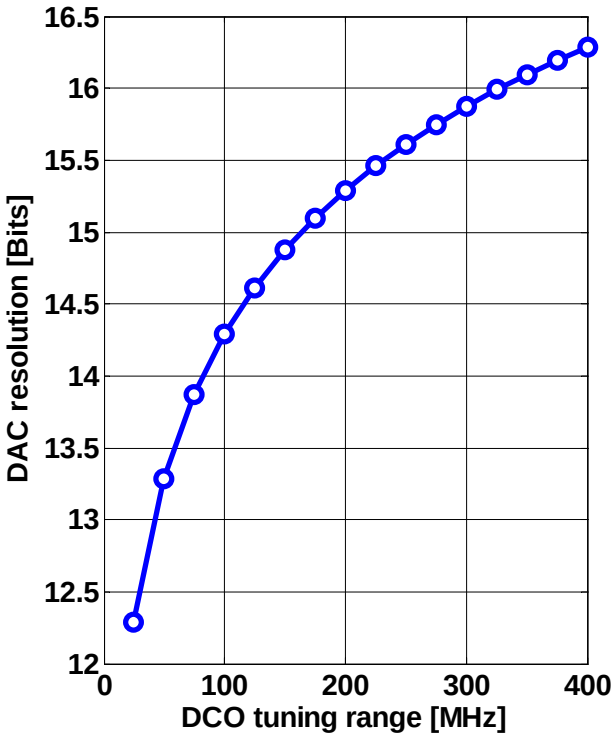

Figure 2.8: DCO resolution tradeoff – DAC resolution vs. DCO tuning range.

An alternate method for implementing a DPLL is to use a digital phase accumulator (DPA) in place of the DCO [20]. An analog oscillator generates the frequency output by differentiating the phase output. The phase response of analog oscillator is illustrated in Fig. 2.9.

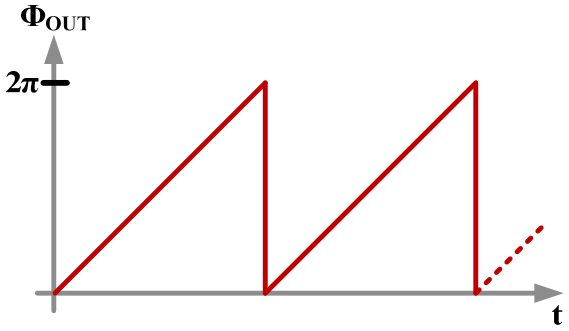

Figure 2.9: Phase response of analog oscillator.

$$\omega_{OUT} = \frac{d\Phi_{OUT}}{dt} \tag{2.3}$$

Analogous to the analog oscillator, the DPA implements the digital-to-frequency function by explicitly accumulating phase in an unlimited fashion. The phase response of DPA is similar with analog oscillator, which guarantees an average gain of 2π radians over the total number of control bits as illustrated in Fig. 2.10.

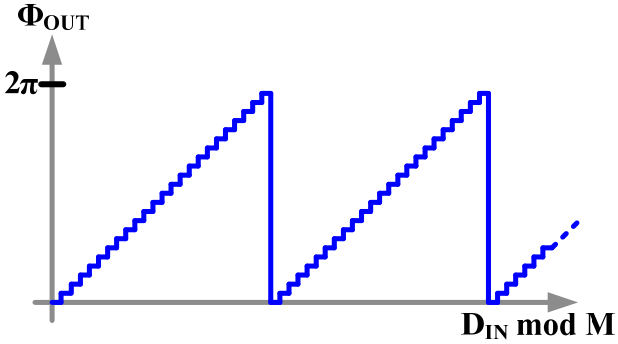

Figure 2.10: Phase response of DPA.

$$\omega_{OUT} = \frac{\Delta\Phi_{OUT}}{\Delta T} = \frac{2\pi}{M \cdot T_{UPDATE}} \tag{2.4}$$

In order to implement the DPA-based high resolution DCO, the DPA is composed of digital accumulator and digital-to-phase converter (DPC) as illustrated in Fig. 2.11 [12]. The rate of output phase change is controlled by the input control word and, therefore, determines the DPA's frequency resolution.

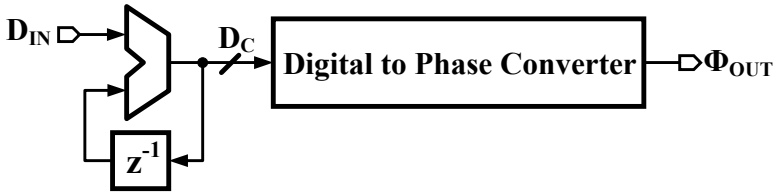

Figure 2.11: Digital phase accumulator.

A more commonly used DPC architecture combines the phase selecting multiplexer with a phase interpolator as illustrated in Fig. 2.12. The most significant bits (MSBs) of the input digital word are used to select two adjacent phases, Φj, Φj+1, from the N phases using an N:2 multiplexer (mux). These two phases are interpolated by a phase interpolator controlled by the least significant bits (LSBs) to generate the required output phase Φ_{OUT}. As a result of phase interpolation, the resolution of this DPC is not limited by the minimum inverter delay.

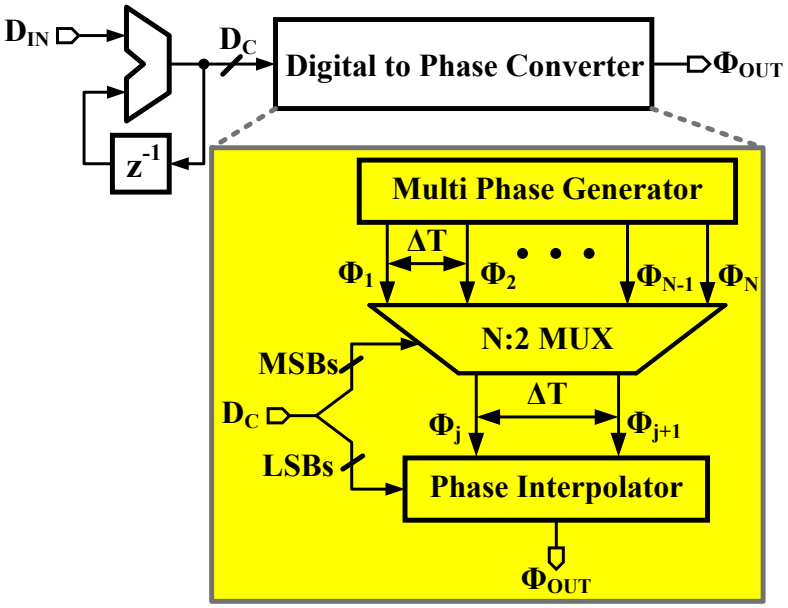

Figure 2.12: Digital to phase converter in DPA.

We can recall the design of a conventional analog PLL used to generate a 100MHz clock using a very low-frequency 100kHz reference signal. One application of such a PLL is to generate a pixel clock from the low-frequency hsync signal in display drivers. There are two major difficulties in implementing such a PLL: (1) large VCO noise due to the low PLL bandwidth (< 10kHz) and (2) large silicon area to implement the low-frequency loop filter. The DPA based DPLL overcomes these two drawbacks by suppressing the VCO phase noise with the large bandwidth of the analog PLL and by employing a digital loop filter to implement the low-frequency filter, thereby reducing silicon area.

2.3 Proposed Architecture

The proposed DPLL replacing DCO with DPA is illustrated at Fig. 2.13.

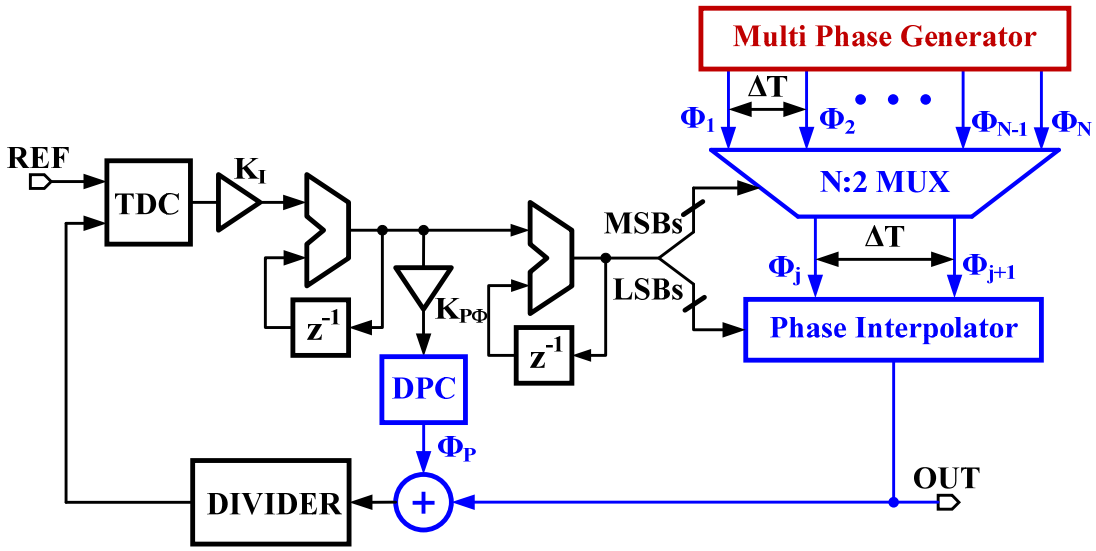

Figure 2.13: Proposed DPLL architecture.

This structure mitigates TDC quantization error and DCO quantization error. Hybrid analog/digital proportional/integral control is used to suppress TDC quantization error and digital phase accumulation techniques to mitigate DCO quantization error.

Digital frequency locked loop (FLL) is used for generating multi-phase. The digital FLL [17] is the same as the digital PLL except that the PFD is replaced with a frequency detector, denoted as FD in the Fig. 2.14.

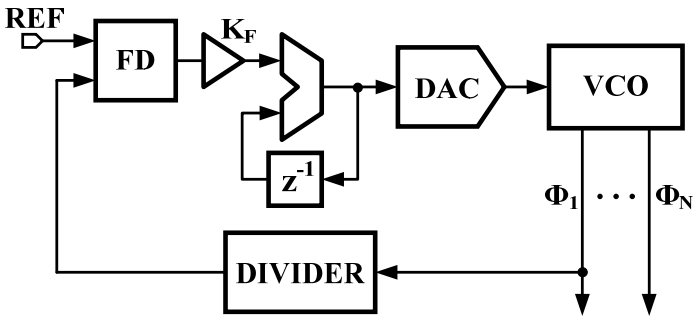

Figure 2.14: Frequency locked loop.

The main purpose of the FLL is to bring the VCO close to desired frequency within 1000ppm and to generate equally-spaced phases for phase shifting multiflexer.

The complete digital PLL is illustrated in Fig. 2.15. Even though the deterministic jitter is reduced with this structure, we have to consider the random jitter of the oscillator.

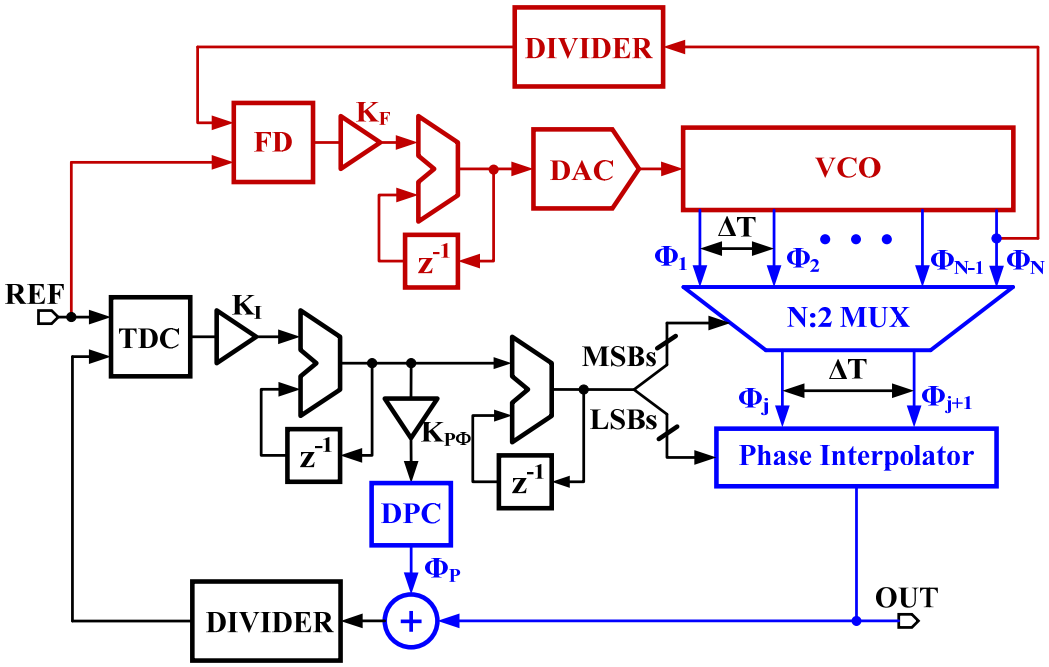

Figure 2.15: Complete digital PLL.

2.4 Random Jitter

The other major class of jitter is non-deterministic, or random jitter. It is unpredictable electronic timing noise and typically follows a Gaussian distribution. The noise sources of random jitter (RJ) include extrinsic noise sources and intrinsic noise sources. The extrinsic noise sources are deterministic noises from the interference of other noise sources, such as supply noise, substrate noise and coupling from undesired signals. The intrinsic noise sources are the random noise from the interior of the circuits, for instance, thermal noise and flicker noise. In this analysis, we will focus on intrinsic noise since the target of this chapter is to analyze the performance limitations and explore the design techniques for the intrinsic circuits of DPLL.

2.4.1 DCO Phase Noise

Phase noise is formed by the random phase modulation mainly coming from the oscillator. The phase modulation is caused by both the noise figures of the oscillator and the MOS transistors used in the circuit. It can be measured in the frequency domain. The phase noise of an open-loop oscillator is revealed in Fig. 2.16.

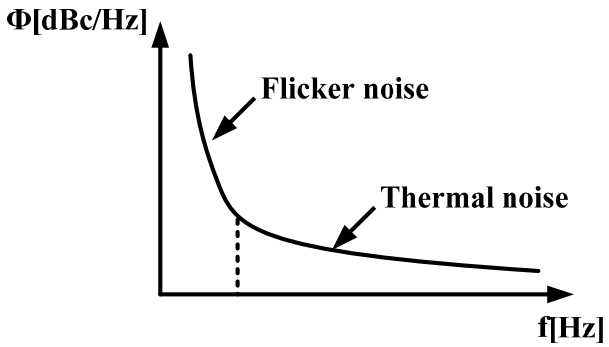

Figure 2.16: Phase noise of open loop oscillator.

At the frequency close-in to the carrier (usually 5-500Hz), the phase noise is dominated by flicker noise. While at the frequency beyond that (typically 5KHz), phase noise is a function thermal noise and driven by the oscillator transistors.

The conventional DPLL usually suffers from an inherent noise bandwidth tradeoff that deteriorates the random jitter at DPLL output. As shown in Fig. 2.17, the DCO phase noise has a high pass transfer characteristic, therefore a high loop bandwidth is required to suppress the large phase noise of ring-based DCO. On the other hand, the TDC quantization noise exhibits a low pass transfer characteristics, therefore a low loop bandwidth is needed to mitigate the quantization error of the TDC.

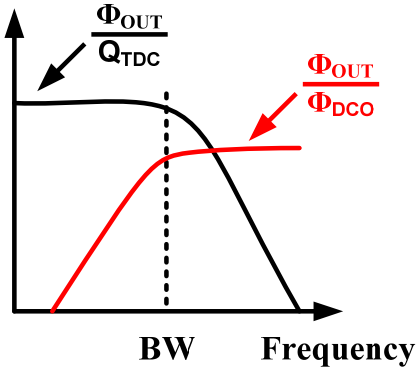

Figure 2.17: Noise bandwidth tradeoff.

This raises a contradiction in conventional DPLL design. As DCO phase noise is the dominant noise source for random jitter, it's necessary to set the loop bandwidth relatively high to obtain a good random jitter performance. However, the TDC quantization noise determines the DJ. Therefore a low bandwidth is also necessary. Normally, a relatively low bandwidth is chosen to mitigate the TDC quantization error for the sake of deterministic jitter in a DPLL design. However this brings on a challenge on the DPLL phase noise performance.

In order to achieve a low phase noise oscillator, we proposed an embed VCO in voltage-mode feedback as illustrated in Fig. 2.18.

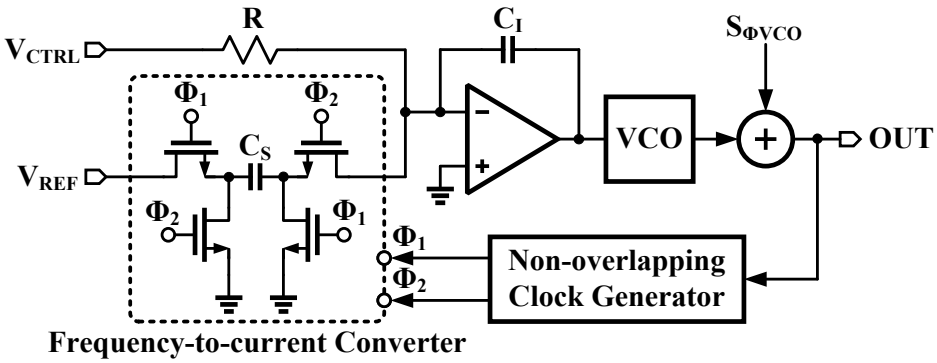

Figure 2.18: Closed-loop VCO.

Switched-capacitor resistor is implemented to convert frequency to current. The output current of frequency-to-current converter (FCC) is proportional to the frequency of the VCO. The difference between the current coming from input control voltage (V_{CTRL}) and the current coming from FCC is integrated by the integrator providing at its output a voltage. Because of the negative feedback system, the input current coming from V_{CTRL} and the feedback current coming from VCO are equal at steady state. The output frequency is presented in the following equation.

$$\frac{V_{CTRL}}{R} = F_{OUT} \times C \times V_{REF} \Rightarrow F_{OUT} = \frac{V_{CTRL}}{V_{REF}} \times \frac{1}{RC} \tag{2.5}$$

In order to quantify the VCO phase noise and identify the noise contributions from each noise source, a phase domain analysis of a closed-loop VCO is needed. The small-

signal model of the closed-loop VCO is shown in Fig. 2.19. Each of the noise sources are represented by their power spectral densities (PSD). For example, the current noise PSD of the resistor and the voltage noise PSD of the integrator are represented by S_{IR} and S_{VINT}, respectively.

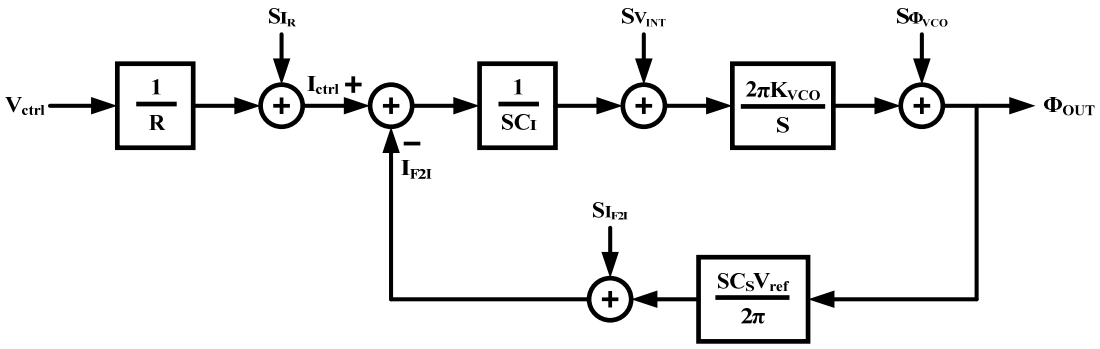

Figure 2.19: Linear model of closed-loop VCO.

The noise sources depicted in Fig. 2.19 are shaped differently by the closed-loop, determined by the noise transfer functions (NTF) associated with each of the noise sources. Similar to the noise analysis of analog PLL, the impact of each of the noise sources on the output can be evaluated using the transfer function analysis. The open loop gain and feed-forward path gain is presented in the following equation, respectively.

$$\mathrm{LG(s)} = \frac{\mathrm{K_{vco}} \cdot \mathrm{C_s V_{ref}}}{\mathrm{sC_I}}, \quad \mathrm{K_{FF}} = \frac{2\pi \mathrm{K_{vco}}}{\mathrm{s^2 C_I R}} \tag{2.6}$$

The input control voltage noise transfer function can be derived as,

$$\frac{\Phi_{\mathrm{OUT}}}{\mathrm{V_{ctrl}}} = \frac{\mathrm{K_{FF}}}{1 + \mathrm{LG}} = \frac{2\pi}{\mathrm{RC_s V_{ref}}} \cdot \frac{1}{\mathrm{s}\left(1 + \dfrac{\mathrm{s}}{\dfrac{\mathrm{K_{vco}} \cdot \mathrm{C_s V_{ref}}}{\mathrm{C_I}}}\right)} \tag{2.7}$$

The input control voltage noise transfer function has a 2nd order low-pass transfer characteristic. The VCO phase noise transfer function is expressed as,

$$\frac{\Phi_{OUT}}{S_{\Phi_{vco}}} = \frac{1}{1+LG} = \frac{C_I}{K_{vco} \cdot C_s V_{ref}} \cdot \frac{s}{1+\frac{s}{\frac{K_{vco} \cdot C_s V_{ref}}{C_I}}} \quad (2.8)$$

Here, this noise transfer function shows a high-pass transfer characteristic. Intuitively, the VCO noise at low frequency can be corrected by the relatively fast feedback loop, while the loop is not fast enough to correct the error at high frequency, thus high frequency noise is passed to the output. Also the integrator noise transfer functions is expressed as,

$$\frac{\Phi_{OUT}}{S_{V_{INT}}} = \frac{\frac{2\pi K_{vco}}{s}}{1+LG} = \frac{2\pi C_I}{C_s V_{ref}} \cdot \frac{1}{1+\frac{s}{\frac{K_{vco} \cdot C_s V_{ref}}{C_I}}} \quad (2.9)$$

The integrator noise transfer function has a low-pass transfer characteristic. We can derive the resistor noise and FCC noise transfer function as follows,

$$\frac{\Phi_{OUT}}{S_{I_R}} = \frac{\Phi_{OUT}}{S_{I_{FCC}}} = \frac{\frac{2\pi K_{vco}}{s^2 C_I}}{1+LG} = \frac{2\pi}{C_s V_{ref}} \cdot \frac{1}{s\left(1+\frac{s}{\frac{K_{vco} \cdot C_s V_{ref}}{C_I}}\right)} \quad (2.10)$$

From these equations, we can calculate the bandwidth of closed-loop VCO as follows,

$$\omega_p = \frac{K_{vco} \cdot C_s V_{ref}}{C_I} \ [\text{rad/sec}] \quad (2.11)$$

The total output phase noise is expressed as

$$S_{\Phi_{OUT}}^{TOTAL}(s) = S_{\Phi_{OUT}}^{\Phi_{VCO}}(s) + S_{\Phi_{OUT}}^{I_R}(s) + S_{\Phi_{OUT}}^{I_{FCC}}(s) + S_{\Phi_{OUT}}^{V_{INT}}(s) \quad (2.12)$$

where each of the individual terms is equal to the product of noise PSD with the squared magnitude of the corresponding NTF. For example, $S_{\Phi_{OUT}}^{\Phi_{VCO}}$ is calculated as follows:

$$S_{\Phi_{OUT}}^{\Phi_{VCO}}(s) = S_{\Phi_{VCO}} \cdot |NTF_{VCO}(s)|^2 \tag{2.13}$$

The final result obtained from the noise bandwidth optimization simulations is presented in Fig. 2.20.

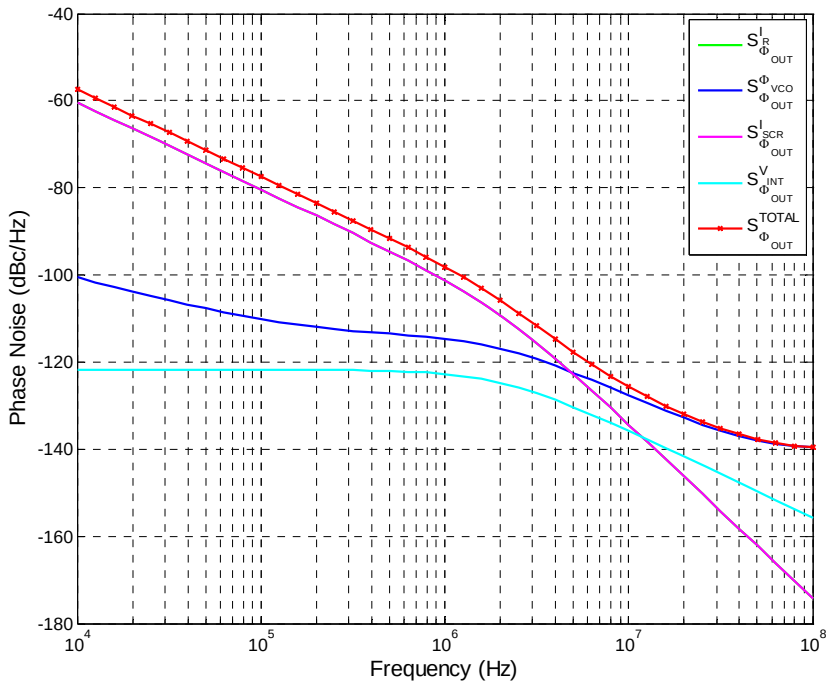

Figure 2.20: Contribution of individual noise sources to the total output phase noise.

The total output phase noise at low frequency is dominated by the resistor noise and FCC noise. Because the VCO phase noise transfer function has a high-pass transfer characteristic and the negative feedback suppresses the VCO phase noise, closed-loop VCO phase noise is much reduced compared to open loop VCO phase noise.

3 Circuit Implementation and Simulation Results

3.1 Proposed DPLL Architecture

The design of the individual building blocks in the proposed DPLL as shown in Fig. 3.1 is discussed in detail in this section.

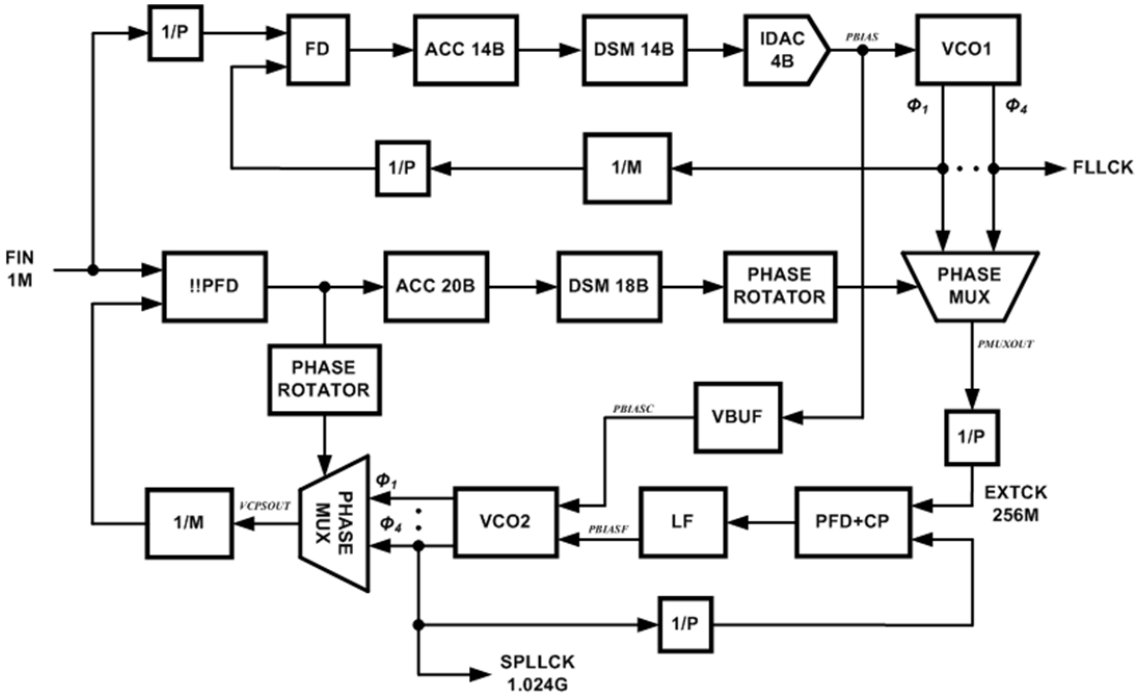

Figure 3.1: Block diagram of the proposed DPLL.

There are three loops in the proposed architecture. First, the main DPLL is composed of proportional and integral path. The proportional path contains the phase rotator and phase mux block, and the integral path composes of the accumulator, delta-sigma modulator, phase rotator, phase mux and sub-PLL. A TDC is implemented with a bang-bang PFD, which is composed of a PFD and a bang-bang PD. In order to reduce the TDC quantization error, the phase-domain proportional path is just across the bang-bang PFD. The phase rotator has the same function with the accumulator for integrating the phase.

Hence, by using phase rotator, we can implement the phase-domain proportional path before the accumulator. Also, we are able to use the same circuit of phase rotator and phase mux at the integral path. Second, there is a FLL which is composed of frequency detector, accumulator, delta-sigma modulator and DCO. This DCO contains the DAC and closed-loop VCO which is implemented for mitigating the VCO phase noise and denoted as VCO1. Third, the sub-PLL exists at the integral path. The sub-PLL has a role of low-pass phase filtering of delta-sigma modulation. The sub-PLL is implemented with the conventional charge-pump PLL. Voltage buffer has a role of buffering bias voltage between output voltage of FLL and input voltage of main digital PLL.

In order to check the functionality, the top simulation was done with Matlab simulation. The model diagram of proposed DPLL is illustrated in Fig. 3.2.

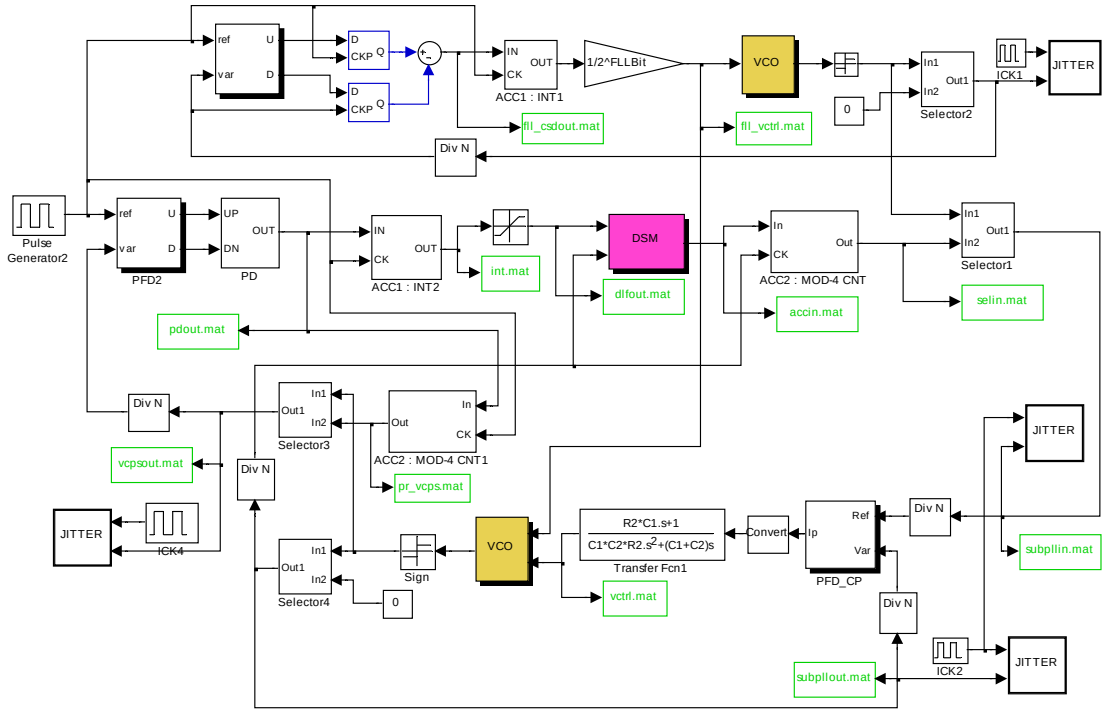

Figure 3.2: Matlab Simulink model.

We are using input frequency 1MHz and 1024 divider value, so that the output frequency is 1.024GHz. The digital LF output, that is delta-sigma modulator input, is shown in Fig. 3.3.

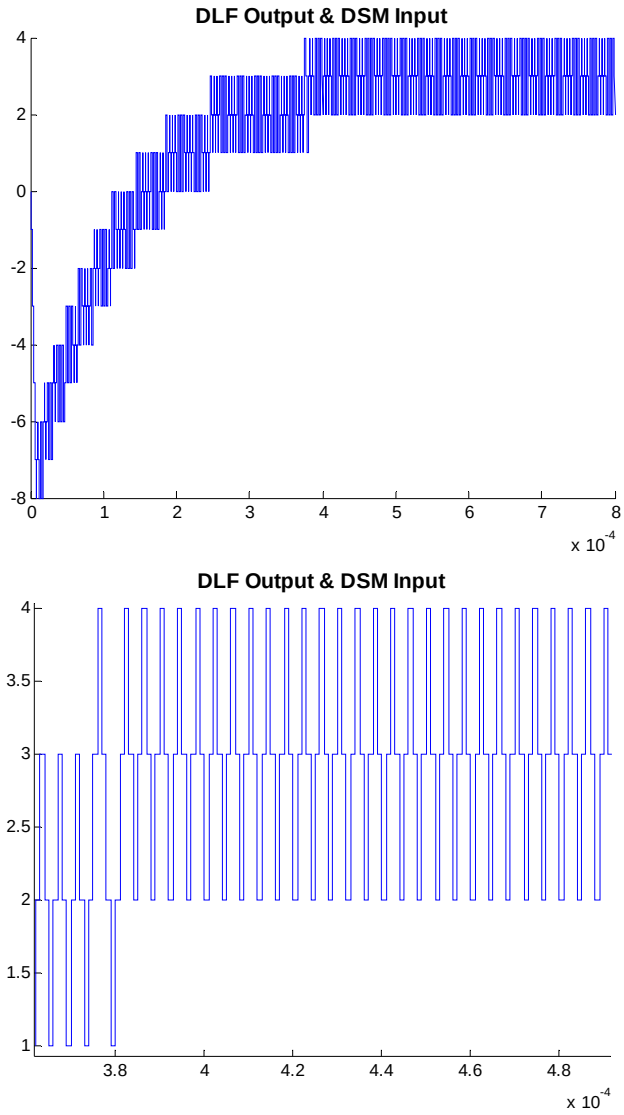

Figure 3.3: Digital loop filter output.

DPLL is locked with 3 steps which matched with calculated value. The output frequency of sub-PLL is shown in Fig. 3.4.

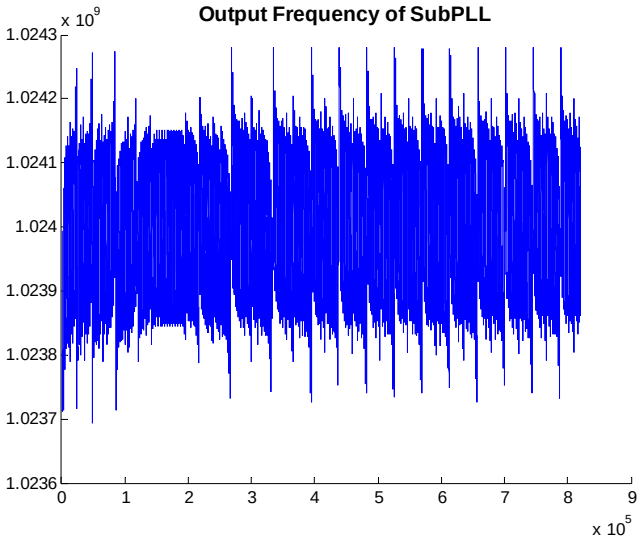

Figure 3.4: Output frequency of sub-PLL.

The target frequency, 1.024GHz, is generated at lock state. The output frequency of proportional path is illustrated in Fig. 3.5. This frequency is dithering because of bang-bang characteristics of PD.

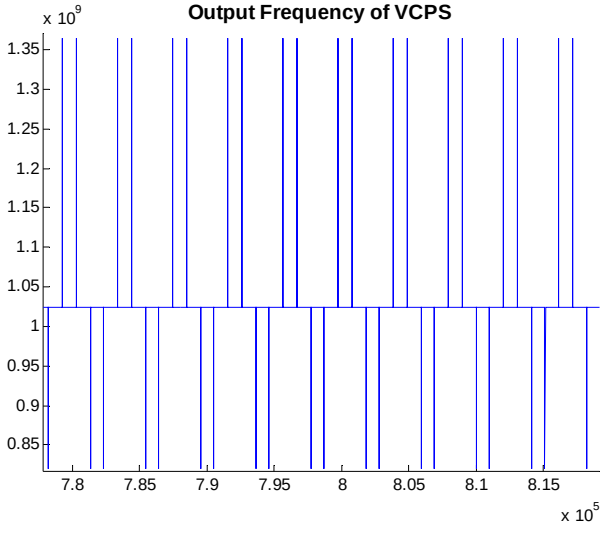

Figure 3.5: Output frequency of VCPS.

3.2 DPA

DPA is composed of the digital accumulator and DPC, which is used for mitigating DCO quantization error. DSM, phase rotator and phase mux are implemented for high resolution DPA.

The phase rotator which is implemented by the circular shift register (CSR) shown in Fig. 3.6 [20]. If FREF leads FV then accumulator output increases and the DSM output (DSMOUT) shifts the register contents left corresponding to a DSMOUT of -1. Therefore, the frequency of DPA will increase. The CSR contents are held in the same state if the DSMOUT is equal to 0.

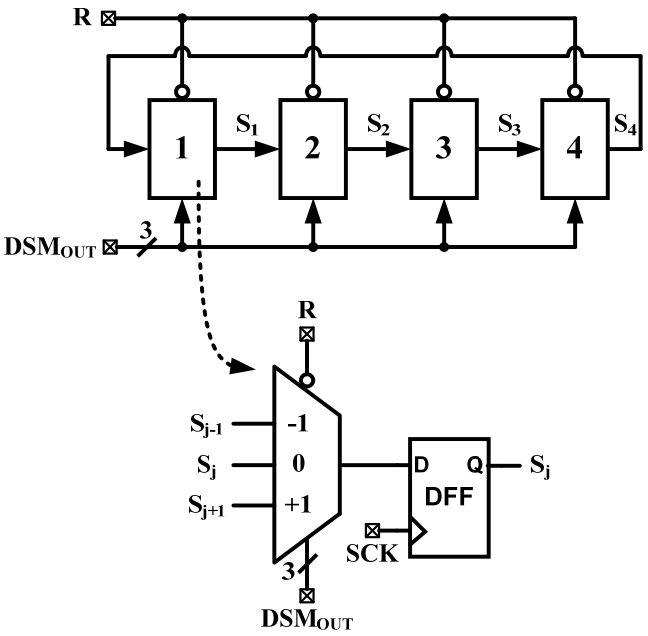

Figure 3.6: Circular shift register.

The phase mux is implemented with a digital phase-switching control circuit, transmission gate and retimer circuit to achieve glitch free operation as illustrated at Fig. 3.7. The select control signals EVEN and ODD are generated and one of the outputs of the two multiplexers is then selected by a glitch-free retimer circuit based on the control signal S_{ODD}/S_{EVEN}.

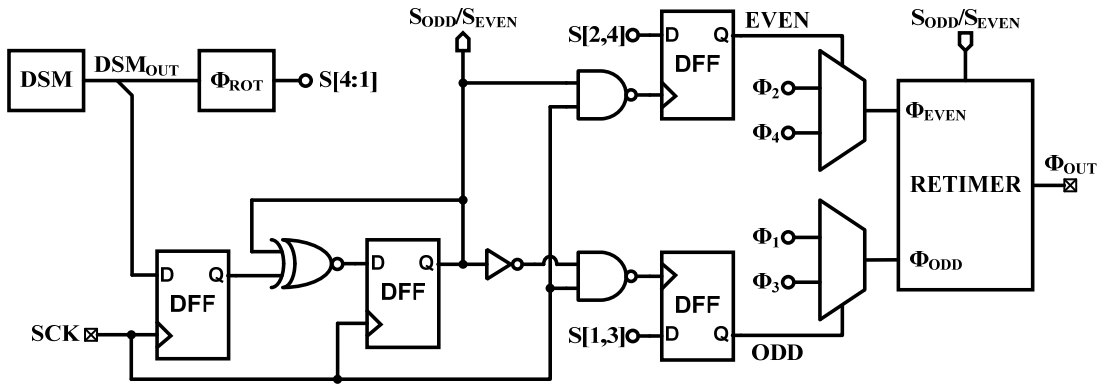

Figure 3.7: Phase switching control circuit.

The delta sigma modulator (DSM) used in this design employs a single-loop second-order error feedback architecture with a 3-level internal quantizer [20]. In this architecture, the quantization error is fed back to the input through a simple loop filter implemented by two delay elements. The input to the DSM is a 14-bit word and the internal operations are performed using 18-bit arithmetic to prevent saturation. The DSM is clocked at one eighth of the operating frequency of the DPC. To allow for such a high frequency clock, the adders in the DSM were built using carry save, carry select, and carry look-ahead techniques.

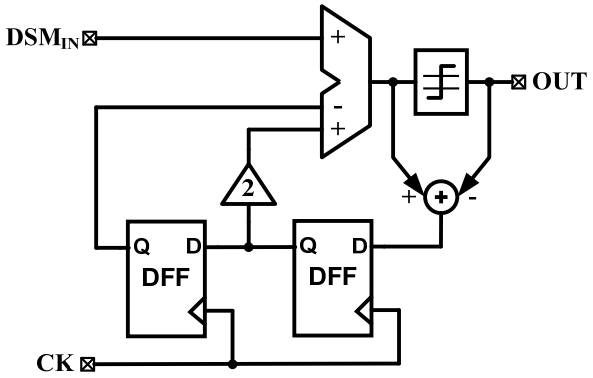

Figure 3.8: Error feedback delta-sigma modulator.

3.3 Sub-PLL

As a result of delta-sigma truncation at DPA, the resulting quantization error is shaped to high frequencies and by the virtue of phase selection using the DSM output, this quantization error appears as shaped phase noise at the output of the phase mux. In order to achieve a precise phase adjustment, we need to filter this high-frequency phase noise. Therefore, the sub-PLL is selected for a low-pass phase filter. There is a tradeoff between signal to quantization noise ratio (SQNR) of DSM and VCO noise of sub-PLL to determine the bandwidth of sub-PLL. If the bandwidth is too high then SQNR is small, and if the bandwidth is too low then VCO noise is dominant noise source. In our design, the sampling frequency of DSM is 125MHz and the bandwidth of sub-PLL is 1MHz. The OSR is 62.5 because of this equation $F_S/2/F_{BW}$ and SQNR is 80dB, hence the DSM is needed over than 13bit.

Sub-PLL is implemented with charge-pump PLL which consists of a phase frequency detector (PFD), a charge-pump (CP), a low-pass loop filter realized using passive components R, C_1, and C_2, VCO, and a frequency divider.

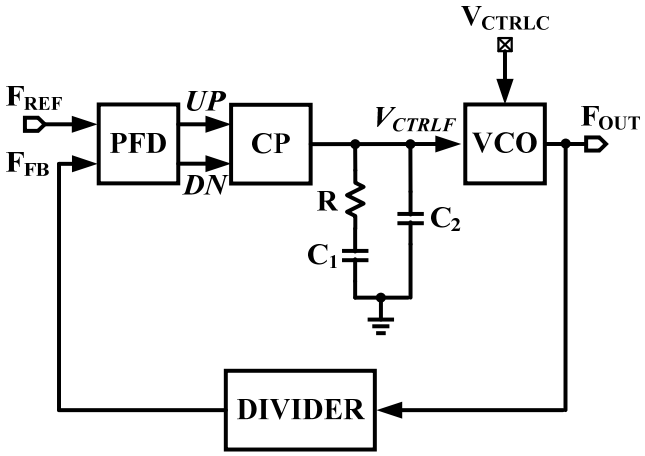

Figure 3.9: Sub-PLL.

Since we employ a glitch-latch PFD, it has a reset pulse of 130psec and the dead zone effects was not a problem, and no extra delay in the PFD reset path required. The

schematic of the charge-pump circuit is shown in Fig. 3.10. It utilizes a single-ended source-switched architecture for high-speed operation. A reference current, I_{REF} , is mirrored to the output current source transistors MP and MN with a mirror ratio of 10 to minimize power consumption in the bias branches. The output currents are turned ON or OFF by controlling switches S1 and S3 with PFD outputs, UP and DN, respectively. Switches S2 and S4, controlled by the complimentary PFD outputs UP and DN, are included to minimize the current mismatch due to charge-sharing [21]. To account for the drop across switches S1 and S3, and to improve the current-mirroring accuracy; dummy switches S5, S6, and S7 are used in the bias branches. VCO has the same structure which is used at open loop VCO in FLL. The VCO input has two control voltages. A coarse control voltage is coming from LF of FLL and a fine control voltage is coming from internal CP. Due to the coarse control voltage, we are able to achieve the small K_{VCO}. Hence, the size of C_1 is greatly reduced.

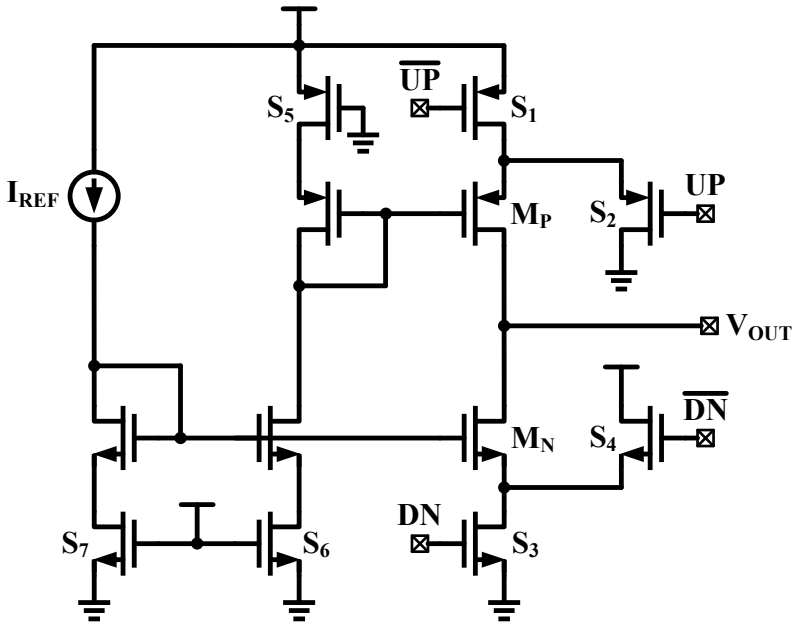

Figure 3.10: Charge pump circuit.

The fine control voltage is locked to 0.61V as shown in Fig. 3.11 with simulation conditions of 1MHz bandwidth, 256MHz input frequency, 4kΩ resistor, 147pF C1 capacitor, 11.5pF C2 capacitor, 12uA charge pump current, K_{VCO} 600MHz/V and phase margin 60degree.

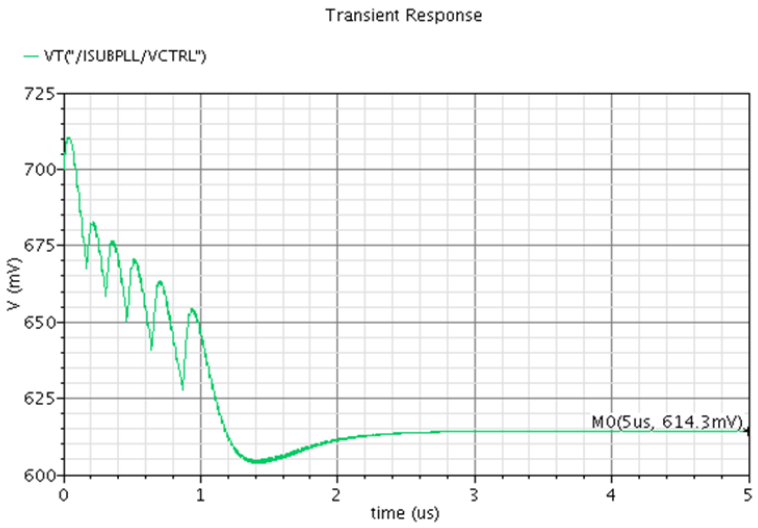

Figure 3.11: Simulated fine control voltage.

The DJ is 0.4psec at the eye-diagram as shown in Fig. 3.12 and the rms jitter is 1.1% without input clock jitter. The current consumption of sub-PLL is 1.1mA.

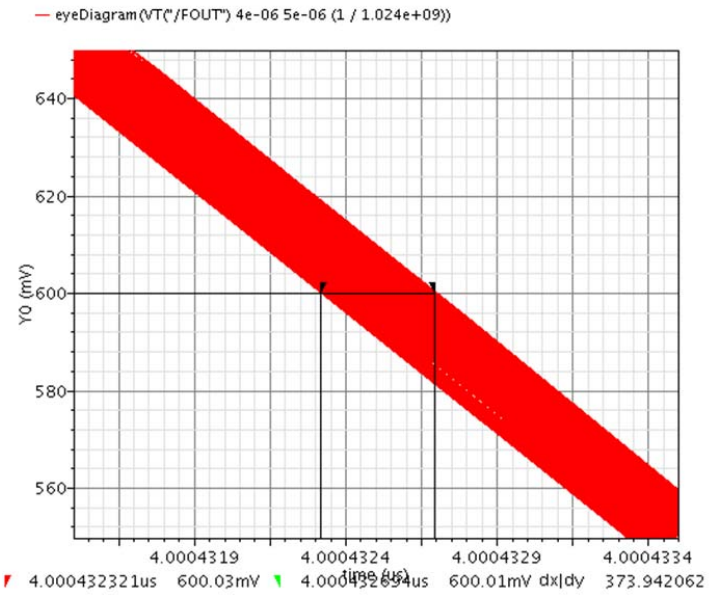

Figure 3.12: Eye-diagram of sub-PLL.

3.4 DJ Simulation Result

Fig. 3.13 shows DJ simulation result. The conventional case is measured at VCPS output, because conventional DPLL output is affected both the proportional and integral path. The proposed case is measured at sub-PLL output, because proposed DPLL output is affected just the integral path. The bang-bang characteristic of proportional path causes to jump a large jitter value. Hence, the DJ of proposed DPLL is greatly reduced compared to conventional DPLL.

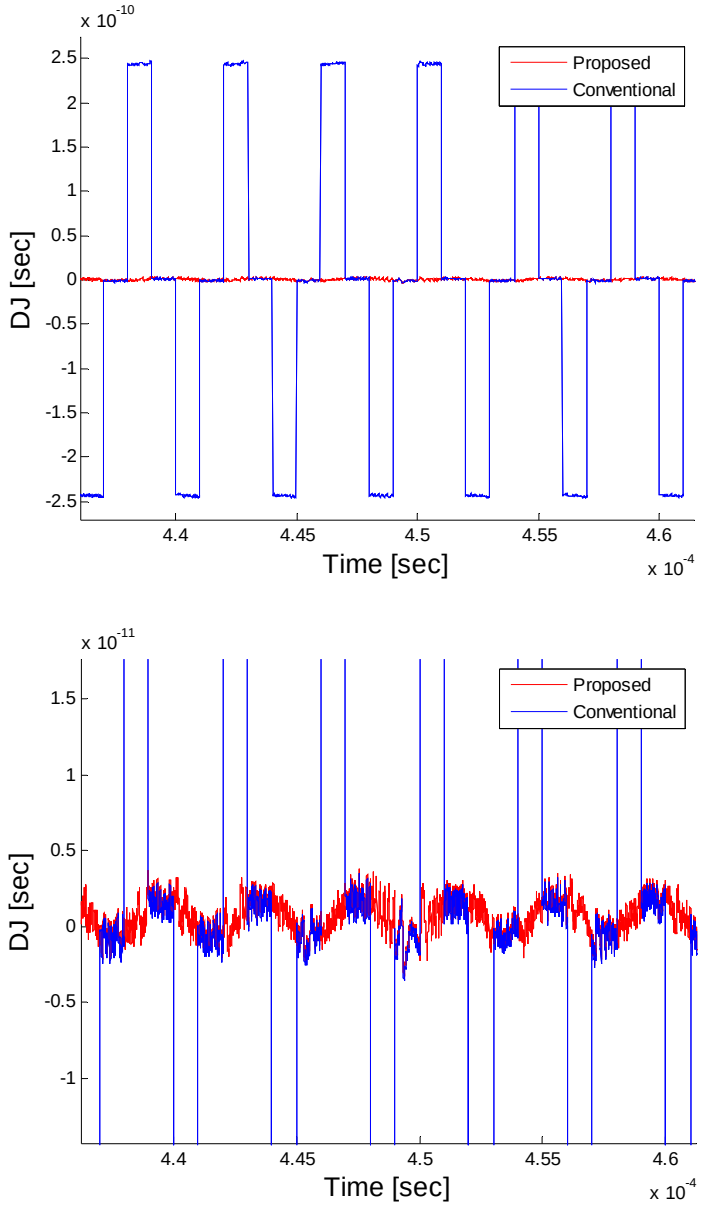

Figure 3.13: DJ Comparison.

3.5 Closed-loop VCO

Closed-loop VCO is implemented for reducing the VCO phase noise and composed of open loop VCO, switched-capacitor resistor, integrator and non-overlapping clock

generator. Open loop VCO is implemented using four current-starved pseudo-differential stages connected in a ring oscillator topology, as shown in Fig. 3.14 [3]. The delay cell consists of two inverters whose outputs are coupled in a feed-forward manner through the NMOS/PMOS pass transistor pair. This coupling ensures differential operation of the oscillator. The output swing depends on the size of the pass transistor MOSFETs relative to that of the inverters. In our design, pass transistors were sized ten times smaller than the devices of the inverters. Fig. 3.15 shows the voltage to frequency and K_{VCO} curve. 1GHz frequency is generated at 0.6V and K_{VCO} is about 3GHz/V.

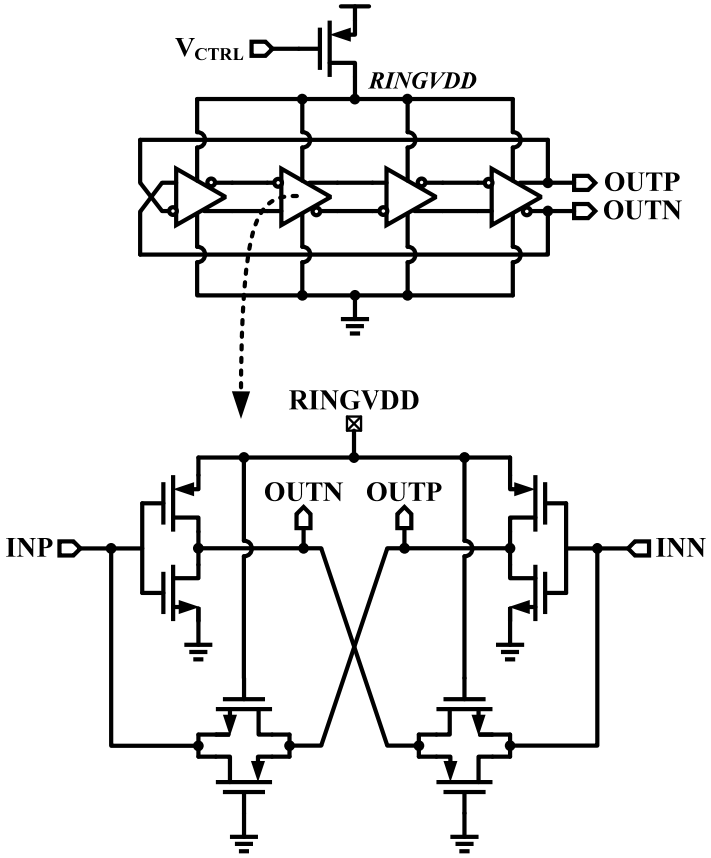

Figure 3.14: Open loop VCO.

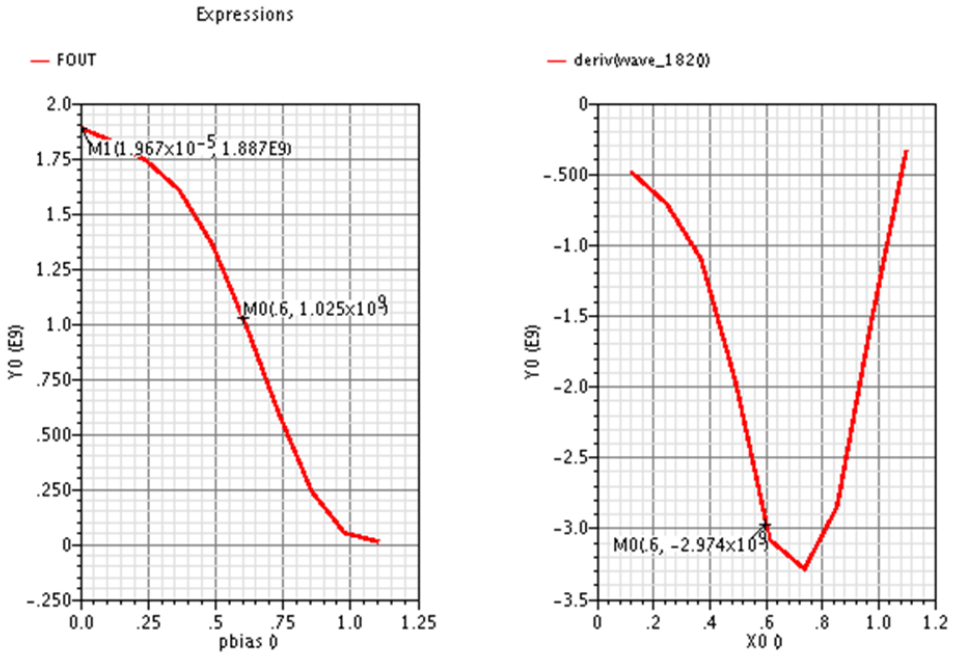

Figure 3.15: Voltage to frequency and K_{VCO} curve.

Switched-capacitor resistor is implemented for converting frequency to current. Switched-capacitor based FCC consists of switches and sampling capacitor (C_S) as shown in Fig. 3. An equivalent resistance Req= $(F \times Cs)^{-1}$ [14]. It is clear that output current of the FCC is a linear function of frequency. In order to achieve low on-resistance of switch, we implement the switch with complimentary NMOS/PMOS transistor. The optimum size of transistor is considered for time constant of stable settling time. The reference voltage (V_{REF}) can control the bandwidth of closed-loop VCO as shown in equation 2.11. Resistor size is determined for both resistor itself noise and noise transfer function.

A telescopic topology is used for op-amp of integrator in order to achieve the characteristics of low noise and high bandwidth. The output swing range from 0.25V to 0.73V should cover the input control voltage of open loop VCO to generate the target frequency. Integrator capacitor (C_I) is used to control the bandwidth of closed-loop VCO. So, we are able to control the values of C_I with on/off switches which are implemented

with transmission gate. A non-overlapping clock generator is used to generate the non-overlapping clocks for FCC block. This circuit realized through chain of inverters and few NAND/NOR.

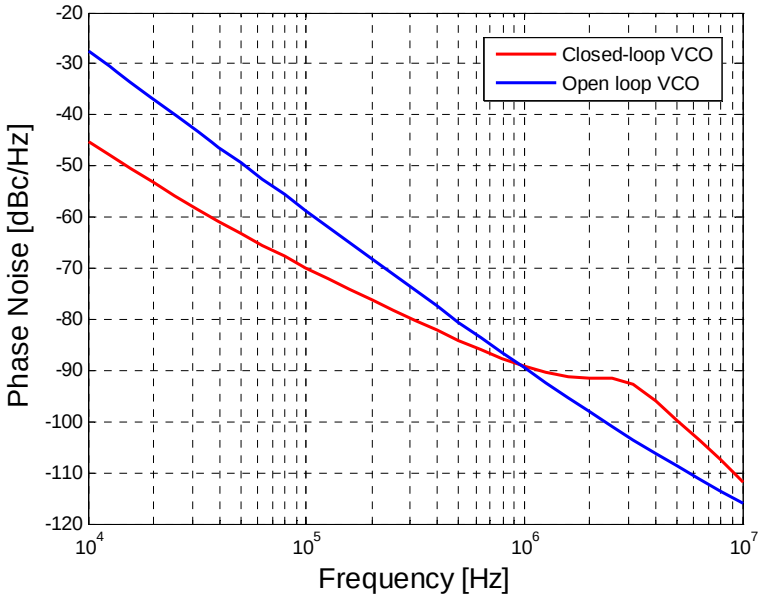

Figure 3.16: Comparison of phase noise.

Fig. 3.16 shows the comparison of phase noise between open loop and closed-loop VCO. The bandwidth of closed-loop VCO is about 3MHz. The rms jitter using closed-loop VCO is 10% less than the rms jitter using open loop VCO. Even though the VCO phase noise is greatly compressed with the bandwidth, the resistor noise is dominant source at low frequency and this noise cannot be suppressed with the bandwidth. Therefore, there is a limitation to improve the phase noise with closed-loop VCO.

3.5 Chip Results

A prototype of the proposed DPLL has been fabricated in a 130nm CMOS process. Fig. 3.17 shows the die photograph of the prototype and occupies an active area of $0.4mm^2$ (800µm × 500µm).

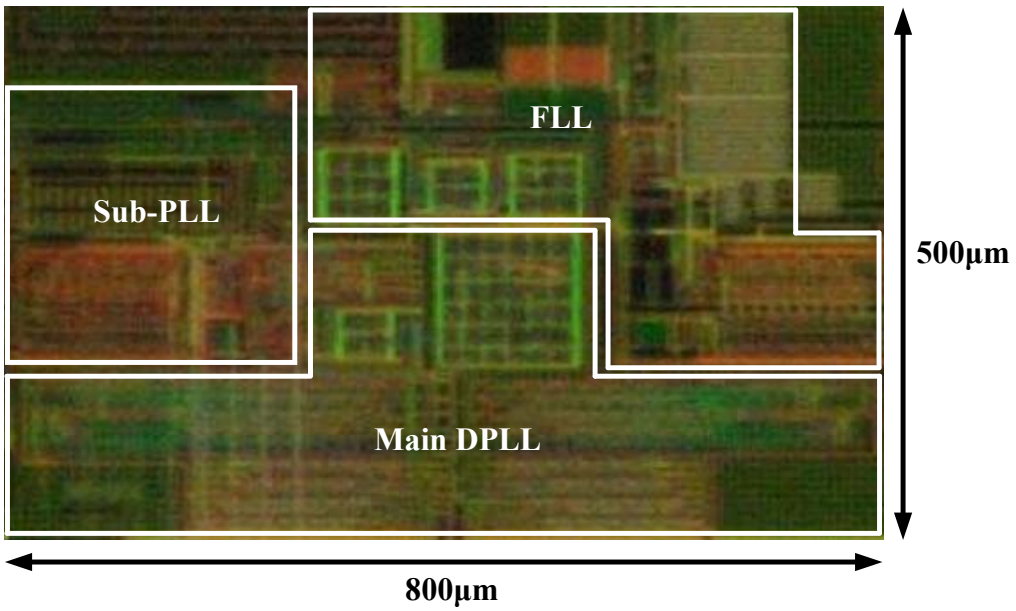

Figure 3.17: Chip die photograph.

Because of divider problem, the chip has not operated. The divider used in this DPLL divides the output by 1024 by using 10 D-FF arrays implemented with true single-phase clocked (TSPC) logic. TSPC D-FF is a fast and simple structure that uses a single-phase clock. But this circuit does not operate at low input frequency, below 50MHz, because of latch characteristic. Since the feedback divider does not generate output frequency, the loop tries to increase the feedback frequency then the output generates its maximum frequency.

Table 3.1: Performance summary

Technology	130nm CMOS
Supply Voltage	1.2V
Input Frequency	1MHz
Output Frequency	256MHz, 512MHz, 1.024GHz
Divider Value	256, 512, 1024
Simulated Deterministic Jitter	3.5psec @1.024GHz
Simulated Random Jitter	12.5psec @1.024GHz
Power Consumption	4.1mW
Die Area	$0.4mm^2$

4 Conclusion

4.1 Summary

The demand for a low-power, low-cost, and small-footprint high-speed clock generator design from applications for communication equipments, consumer electronics, and computing systems is increasingly stronger. The performance of the clock generator greatly depends on how well the jitter is controlled. Therefore a noise-robust design becomes extremely useful to be used in today's highly-integrated mixed-mode System on Chip (SoC).

This thesis explored the design approaches and circuit techniques for low jitter digital PLL in sub-micron process. In chapter 2, DPLL noise model is analyzed in order to quantify each noise source. The main DJ sources are the TDC and DCO quantization error, and the main RJ source is DCO phase noise. A hybrid analog/digital proportional/integral control is suggested to suppress TDC quantization error and digital phase accumulation technique is proposed to mitigate DCO quantization error. VCO phase noise is reduced using an embedded voltage-mode feedback. Chapter 3 shows the circuit implementation and simulation results. The phase rotator and phase mux are used for the proportional path. The digital phase accumulator is implemented to achieve high resolution DCO. Closed-loop VCO is implemented to suppress the VCO phase noise. Because of the resistor noise, there is a limitation to improve the VCO phase noise. Even though there is a failure at divider due to using TSPC at low frequency, the simulated DJ illustrates superior jitter performance compared to conventional DPLL.

4.2 Future Work

First, the resistor noise is a dominant noise source at closed-loop VCO. Therefore it's necessary to find the method to reduce this resistor noise or investigate low noise current source to replace with the resistor.

Second, this closed-loop VCO is similar with a phase locked loop with respect to using negative feedback and open loop VCO. Because digital-enhanced circuits to assist analog design have become more and more necessary and exhibit many performance enhancement, digital-enhanced closed-loop VCO or closed-loop DCO to mitigate the DCO phase noise is considerable in future design.

Bibliography

[1] Herve Marie and Philippe Belin, “R, G, B Acquisition Interface with Line-Locked Clock Generator for Flat Panel Display”, IEEE J. Solid-State Circuits, vol. 33, no. 7, pp. 1009-1013, Jul. 1998.

[2] Inchul Hwang et al., “A Digitally Controlled Phase-Locked Loop with Fast Locking Scheme for Clock Synthesis Application”, IEEE International Solid-State Circuits Conference, 2000, pp. 168–169.

[3] W. Yin et al., “A 1.6mw 1.6ps-rms-jitter 2.5ghz digital pll with 0.7-to-3.5ghz frequency range in 90nm cmos”, Custom Intergrated Circuits Conference, pp. 243-246, Sep. 2010.

[4] T. Watanabe and S. Yamauchi, "An all-digital PLL for frequency multiplication by 4 to 1022 with seven-cycle lock time", IEEE J. Solid-State Circuits, vol. 38, no. 2, pp. 198-204, Feb., 2003.

[5] Craninckx, J. and Steyaert, M.S.J., “A fully integrated CMOS DCS-1800 frequency synthesizer”, IEEE J. Solid-State Circuits, vol. 33, no. 12, pp. 2054-2065, Dec., 1998.

[6] P. Hanumolu et al., “Digitally-enhanced phase-locking circuits”, Custom Integrated Circuits Conference, pp. 361-368, Sep. 2007.

[7] P. Dudek et al., “A high-resolution cmos time to digital converter utilizing a vernier delay line”, IEEE J. Solid-State Circuits, vol. 35, pp. 240-247, Feb. 2000.

[8] Minyoung Song et al., “A 10mhz to 315mhz cascaded hybrid pll with piecewise linear calibrated tdc”, Custom Integrated Circuits Conference, pp. 243-246, Sep. 2009.

[9] J. Lin et al., "A PVT tolerant 0.18MHz to 600MHz self-calibrated digital PLL in 90nm CMOS process", IEEE International Solid-State Circuits Conference, 2004, pp. 488-541.

[10] Song-Yu Yang et al., "A 7.1mW 10GHz all-digital frequency synthesizer with dynamically reconfigurable digital loop filter in 90nm CMOS", IEEE International Solid-State Circuits Conference, 2009, pp. 90-91.

[11] Minjae Lee and Asad Abidi, “A 9 b, 1.25 ps Resolution Coarse–Fine Time-to-Digital Converter in 90 nm CMOS that Amplifies a Time Residue”, IEEE J. Solid-State Circuits, vol. 43, pp. 769-777, Apr. 2008.

[12] P. Hanumolu et al., “A Sub-Picosecond Resolution 0.5–1.5 GHz Digital-to-Phase Converter”, IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 414-424, Feb. 2007.

[13] Robert Staszewski et al., “1.3 V 20 ps Time-to-Digital Converter for Frequency Synthesis in 90-nm CMOS”, IEEE Transactions on Circuits and System-II: Express Briefs, vol. 53, pp. 220-224, Mar. 2006.

[14] Nguyen Phuong Thi Le et al., “High linearity voltage-controlled oscillator”, ASIC, 2009. ASICON '09, pp. 363-366, Mar. 2009.

[15] H.-R. Lee et al., "A PVT-Tolerant Low-1/f Noise Dual-Loop Hybrid PLL in 0.18μm", IEEE International Solid-State Circuits Conference, 2006, pp. 2402-2411.

[16] T. H. Lee and J. F. Bulzacchelli, “A 155-MHz clock recovery delay-and phase-locked loop”, IEEE J. Solid-State Circuits, vol. 27, pp. 1736–1746, Dec. 1992.

[17] R. Inti et al., “A highly digital 0.5-to-4Gb/s 1.9mW/Gb/s Serial-link Transceiver using current-recycling in 90nm CMOS”, IEEE International Solid-State Circuits Conference, 2011, pp. 152–153.

[18] M. Mansuri and C.-K. K. Yang, “Jitter optimization based on phase-locked loop design parameters”, IEEE J. Solid-State Circuits, vol. 37, pp. 1375–1382, Nov. 2002.

[19] R. Staszewski et al., “All-Digital PLL and Transmitter for Mobile Phones”, IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2469-2482, Dec., 2005.

[20] P. Hanumolu et al., “A Wide-Tracking Range Clock and Data Recovery Circuit”, IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 425-439, Feb., 2008.

[21] P. Larsson, “A 2-1600 MHz 1.2-2.5 V CMOS clock-recovery PLL with feedback phase-selection and averaging phase-interpolation for jitter reduction”, IEEE International Solid-State Circuits Conference, 1999, pp. 356–357.