# AN ABSTRACT OF THE THESIS OF

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Title: Design Techniques for Low-Power Multi-GS/s Analog-to-Digital Converters.

Abstract approved:

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Patrick Y. Chiang

Ultra-high-speed (>10GS/s), medium-resolution (5~6bit), low-power (<50mW) analog-to-digital converter can find it application in the areas of digital oscilloscopes and next-generation serial link receivers. There are several challenges to enable a successful design, however. First, the time-interleaved architecture is required in order to achieve over 10GS/s sampling rate, with the trade-off of the number of the channels and the sampling rate in each channel. Phase misalignment and channel mismatch must be considered too. Second, timing accuracy, especially dynamic jitter of sampling clock becomes a major concern at ultra-high frequency, and certain techniques must be taken to address it. Finally, to achieve low power consumption, Flash architecture is not suitable to serve as the sub-ADC, and a low-power sub-ADC that can work at relatively high speed need to be designed.

A single channel, asynchronous successive approximation (SA) ADC with improved feedback delay has been fabricated in 40nm CMOS. Compared with a

conventional SA structure that employs a single quantizer controlled by a digital feedback logic loop, the proposed SA-ADC employs multiple quantizers for each conversion bit, clocked by an asynchronous ripple clock that is generated after each quantization. Hence, the sampling rate of the 6-bit ADC is limited only by the six delays of the Capacitive-DAC settling and each comparator's quantization delay, as the digital logic delay is eliminated. Measurement results of the 40nm-CMOS SA-ADC achieves peak SNDR of 32.9dB at 1GS/s and 30.5dB at 1.25GS/s, consuming 5.28mW and 6.08mW respectively, leading to FoM of 148fJ/conversion-step and 178fJ/conversion-step, in a core area less than 170µm by 85µm.

Based on the previous work of sub-ADC, a 12-GS/s 5-b 50-mW ADC is designed in 40nm CMOS with 8 time-interleaved channels of Flash-SA hybrid structure each running at 1.5GS/s. A modified bootstrapped switch is used in the track-and-hold circuit, introducing a global clock signal to synchronize the sampling instants of each individual channel, therefore improve the phase alignment and reduce distortion. The global clock is provided by a CML buffer which is injected by off-chip low-noise sine-wave signal, so that the RMS dynamic jitter is low for better ENOB performance. Measurement results show that the 12GS/s ADC can achieve a SNDR of 25.8dB with the input signal frequency around DC and 22.8dB around 2GHz, consuming 32.1mW, leading to FoM of 237.3fJ/conversion-step, in a core area less than 800µm by 500µm.

# Design Techniques for Low-Power Multi-GS/s Analog-to-Digital Converters

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Major Professor, representing Electrical and Computer Engineering

Director of the School of Electrical Engineering and Computer Science

Dean of the Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Tao Jiang, Author

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It is hard to describe my feeling right now, when finishing the dissertation body and starting this acknowledgement part. Six years in pursuing the degree, which is almost one fifth of my current life, is not a short period of time. I value all the experience I have been through, and hope it can make me a qualified Doctor of Philosophy.

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# Design Techniques for Low-Power Multi-GS/s Analog-to-Digital Converters

## 1. Introduction

### 1.1.Motivation

As CMOS technology scales down to the magnitude of nanometer, digital signal processing becomes increasingly more powerful because greater amount of transistors and logic gates can be integrated on a single chip with even less cost. As a result, it is a growing tendency to process the analog signal in the digital domain after appropriate data conversion, and analog-to-digital converters (ADC) have been widely employed in various applications with different requirements for resolution and sampling rate [1]. To satisfy such requirements, multiple ADC architectures have been developed, which was summarized in [2] and is quoted in Figure 1.1 as below.

Although most of the existing architectures, such as sigma-delta, flash, pipeline and

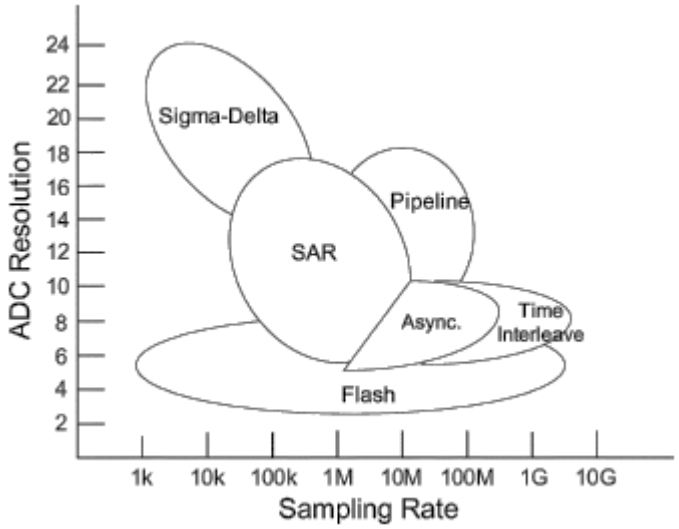



Figure 1.1: ADC architectures and their respective fields of application. [2]

SA, have been intensively studied due to their popularity in most commonly-seen areas, it is only since recent years that the multiple-giga-sample-per-second ADCs have drawn people's attention. The consistently increasing process speed in certain applications requires higher and higher data rate for the ADC employed, while on the other hand the demand for low power consumption places additional stringent requirement for the circuit design.

It is of great interest to systematically study and discuss some design methodology for such multi-GS/s, low power ADCs, and before that it is necessary to introduce some background on the applications where such ADCs are used.

## 1.2. Application Background

### 1.2.1. SerDes Circuits

Serializer/deserializer (SerDes, also referred as serial link or wireline), is a critical component in the high-speed I/O interfaces which are widely employed in the commonly used computer systems nowadays. For example, in Figure 1.2 [3] a block diagram consisting of an Intel® Core™ i7 Processor, an X58 chipset (acting like the north bridge), and an ICH10R I/O Controller Hub (ICH, as the south bridge) is shown, demonstrating a typical computer architecture released by Intel in 2008. Different interconnect standards are used in order to communicate the X58 chipset with other blocks: the QuickPath Interconnector (QPI) is employed to connect the processor, the Direct Media Interface (DMI) is to connect the ICH, and the Peripheral Component

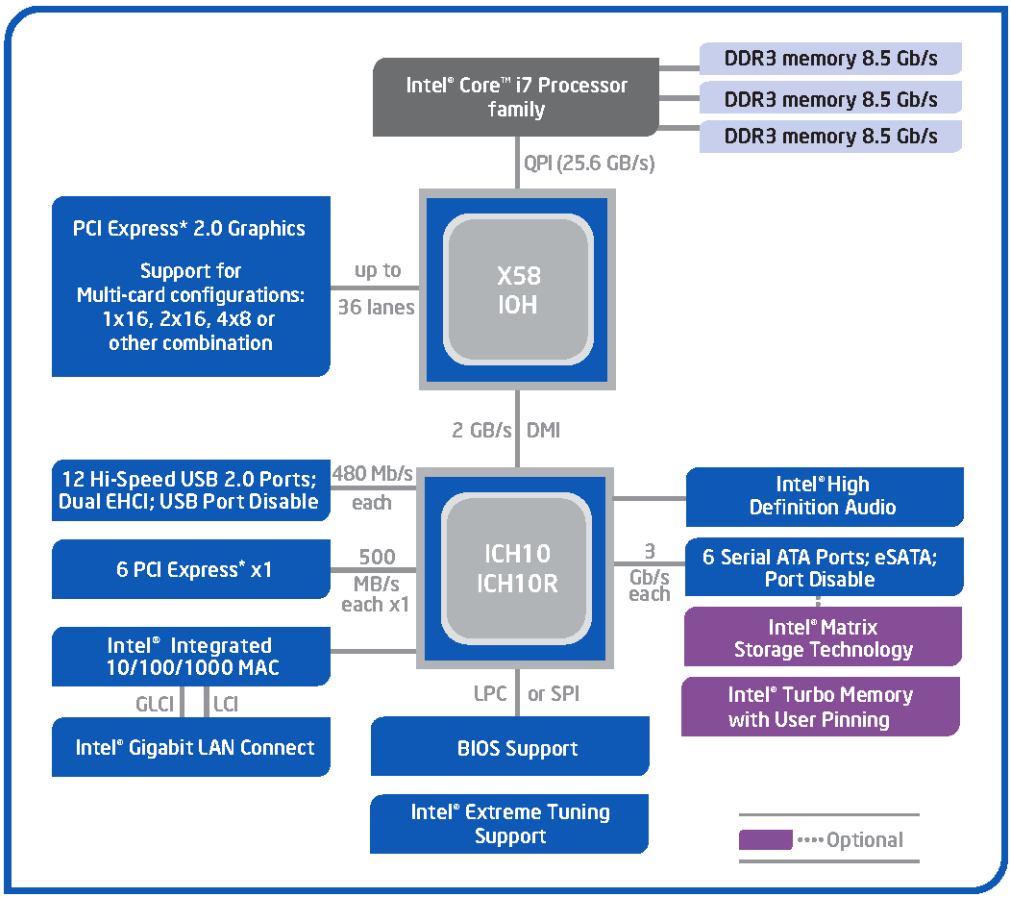



Figure 1.2: Intel® X58 express chipset block diagram.

Interconnect Express (PCIe) to the graphics. Even more peripherals are connected to the ICH10R via other serial links, including the Universal Serial Bus (USB) 2.0 to external devices, and the Serial AT Attachment (SATA) to mass storage devices such as hard disk drives and optical drives.

A typical SerDes architecture is shown in Figure 1.3(a), with the emphasis on the transmission channel and the receiver (RX) equalizer. It is noteworthy that in the high-speed SerDes application, transmission channel can no longer been viewed as an

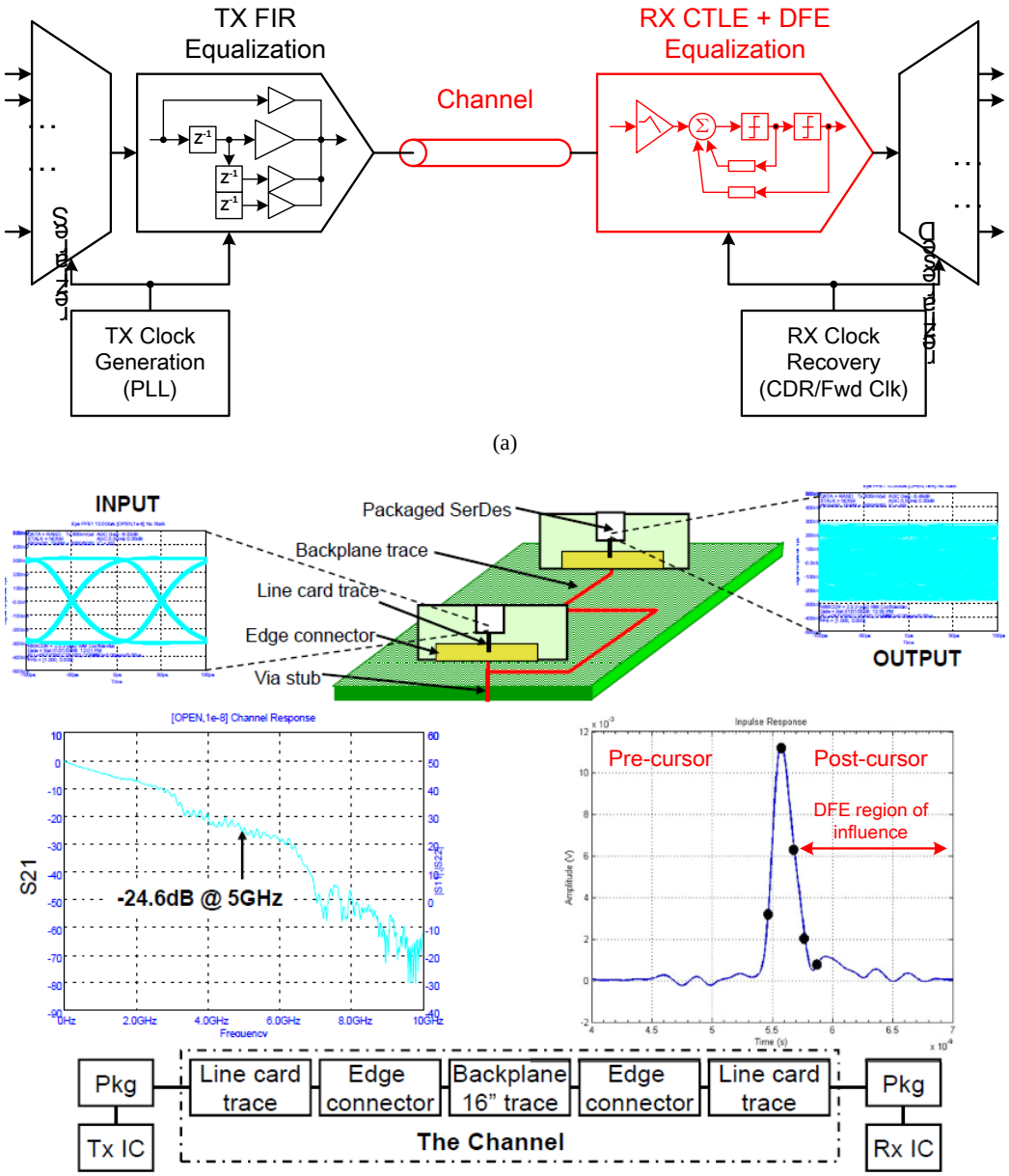



Figure 1.3: (a) Typical SerDes architecture; (b) Transmission channel impairment.

ideal wire. Instead, it is usually in the form of an electrical backplane consisting of IC chip packages, PCB traces (including via stubs), and edge connectors, as shown in

Figure 1.3(b) [4]. Such non-idealities introduce significant frequency dependent loss, such as dispersion and reflection, and co-channel interference, such as far-end (FEXT) and near-end (NEXT) crosstalk, causing degraded channel response and distorted pulse response. As the result, a wide open eye diagram appearing at the output end of transmitter (TX) becomes a close one at the input end of RX, making it impossible to correctly resolve the transmitted signal bits. In order to mitigate the channel loss, certain equalization techniques must be taken, including the feed-forward equalizer (FFE) at the TX end, the continuous-time linear equalizer (CTLE) and the decision feedback equalizer (DFE) at the RX end [5].

Among all the above equalization techniques, DFE has been widely used due to its many advantages. For example, unlike FFE it boosts high frequency content instead of attenuating the low frequency one; and unlike CTLE it does not amplify noise or

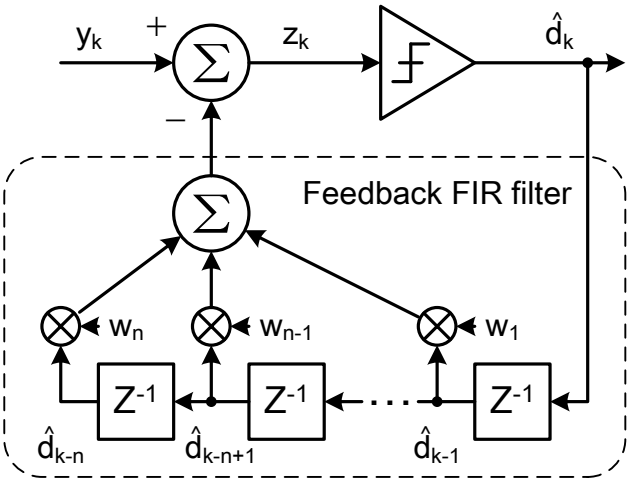



Figure 1.4: Conceptual block diagram of DFE.

crosstalk. The main concept of DFE is to subtract the inter-symbol interference (ISI) directly from the incoming signal via a feedback FIR filter (as shown in Figure 1.4), and the equalization equation can be given as:

$$z_k = y_k - w_1\hat{d}_{k-1} - \cdots - w_{n-1}\hat{d}_{k-n+1} - w_n\hat{d}_{k-n} \tag{1.1}$$

where $y_k$ and $z_k$ are analog signals before and after equalization, $w_i(i = 1, 2, \cdots, n)$ are feedback FIR tap coefficients which models channel response, and $\hat{d}_{k-i}(i = 1, 2, \cdots n)$ are symbol decision (digital outputs) of previous bits.

Traditionally, the DFE operation was in the analog circuit domain, based on CML [4] or switched-capacitor [6] summation. And with the data rate becoming higher, half-rate [4] or quad-rate [6] architecture with first feedback tap speculation [4][6] was introduced to ease the requirement for the settling time of the critical path. Recently, architectures that implemented the DFE operation in the digital domain have been published [7][8], the comprehensive theory of which has also been presented and discussed [9][10][11][12]. The block diagram is shown in Figure 1.5, with the assistant of an ADC to convert the analog incoming signal to a digital one with

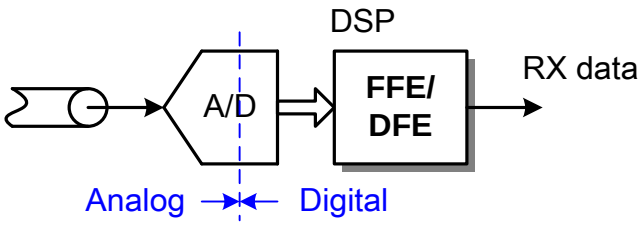



Figure 1.5: Block diagram of ADC-based receiver.

adequate resolution. Such ADC-based receiver brings several benefits: first, besides the DFE which cannot cancel pre-cursor ISI (Figure 1.3(b)), an RX-side FFE can be easily employed. Second, in the digital domain it is more flexible to program the FFE/DFE coefficients to take care of different transmission channel degradation.

As the data rates of the mainstream SerDes circuits reach tens-of-giga-sample-per-second, the demand for the ADC for the aforementioned purpose also becomes high. Several ADCs for the receiver side of the SerDes have been published, including a 24-GS/s 6-bit 1.2-W ADC in 90nm CMOS [13], a 40-GS/s 6-bit 1.5-W ADC in 65nm CMOS [14], and a 56-GS/s 8-bit 9-W ADC in 65nm CMOS (scaling with technology to 63-GS/s 8-bit 5-W in 40nm CMOS) [15]. As the application of such over-10GS/s medium-resolution ADCs becomes wider, it is of great interest and importance to study and research on the related design techniques.

### 1.2.2. Digital Storage Oscilloscope

Test instrument must keep pace with new communications standards that continue to push higher data rates with increasingly tight timing margins, among which the digital storage oscilloscope (DSO) is often counted on to isolate circuit problems, debug system failures, and verify compliance to standards. The DSO features an ADC to convert the analog signal to digital data, which can be stored in memory as much as required, as well as processed by some digital signal processors. As a key selection criterion, the sampling rate of a "real-time" DSO, which is also that of the embedded ADC, needs typically to be 5 to 10 times of the input bandwidth. Sometimes a

variation of DSO called the *digital sampling oscilloscope* is used for the high-speed communication where the waveform consists of repeating pulses, sampling at a low rate deliberately and then uses signal processing to reconstruct a composite view of a typical pulse (i.e. eyediagram). Today, the best oscilloscopes in the market from the giant manufacturers feature an input signal bandwidth of 33GHz with sampling rate up to 100GS/s from Tektronics, and a signal bandwidth of 63GHz with sampling rate up to 160GS/s from Agilent.

The first GS/s ADC fabricated in CMOS technology for the oscilloscope purpose was published in 2002 [16] by Agilent, which was a 4-GS/s 8-bit ADC in 0.35μm CMOS. Another 20-GS/s 8-bit ADC in 0.18μm CMOS was published by the same group in 2003[17]. In general, power consumption is not a major consideration for the ADC designed for such purpose, while bandwidth, noise floor, time-interleaved matching and added jitter are all more important factors. To realize over 100GS/s operation, integrated circuits fabricated in silicon germanium (SiGe) or even indium phosphide (InP) technologies are used to form the heart of oscilloscopes[18].

## 1.3. Thesis Organization

The dissertation begins with an overview of the traditional techniques enabling time-interleaved ADC, including the possible implementations for the sub-ADC and the track-and-hold circuits, in Chapter 2. Due to its advantages and popularity, the successive-approximation (SA) architecture will be emphasized and discussed.

Chapter 3 introduces a single-channel, 1.25-GS/s 6-bit asynchronous SA ADC with improved capacitive DAC delay. The main purpose is to explore an architecture which can achieve fast SA conversion with acceptable power efficiency, which can be further time-interleaved to achieve even higher sampling rate. By using multiple comparators to account for each individual bit conversion, conventional digital logic in the single-comparator SA architecture can be removed, and the feedback loop from the comparator output to capacitive DAC input is essentially reduced. Theoretically in an architectural point of view, the proposed work is the fastest possible 1-bit/step SA ADC that can be realized.

Chapter 4 describes a 12-GS/s 5-bit 8-channel time-interleaved ADC with a global sine-wave clock for sampling instants synchronization. With the slight modification in the track-and-hold circuits as proposed, the timing skew in the multi-phase clock will not cause significant distortion in the reconstructed waveform, and the dynamic jitter is also reduced due to the nature of the sine-wave clock. Besides, by using a Flash-SA-hybrid architecture, the sub-ADC employed is also modified to achieve adequately fast conversion speed.

Chapter 5 summarizes the presented work, and proposes some suggestion for future work.

# 2. Traditional Approaches

Before presenting my own work, it is very necessary and helpful to review the existing techniques that enable the design of multi-GS/s ADCs. This includes two parts, the high-speed sub-channel ADC (sub-ADC) and the track-and-hold circuits (T/H, or sample-and-hold, S/H). The advantages and disadvantages of each structure will be discussed, so the space for possible improvement can be understood.

## 2.1. State-of-the-Art >10GS/s ADCs

Features and performances of state-of-the-art ADCs running faster than 10GS/s are summarized in Table 2.1.

As listed in Table 2.1, there could be various options for the sub-ADC structure and the number of channels. To achieve the same ultra-high sampling rate, the trade-off between the circuit complication and power consumption of the sub-ADC and the clock generation and distribution must be considered when making the choice.

Generally, if the conversion speed that a single sub-ADC can achieve is low, then a large number of such sub-ADCs have to be time-interleaved to meet the total sampling rate requirement. The power consumed by the sub-ADC may be small, but the cost is the clock generation and distribution, as well as the phase error calibration circuits have to be complicated. Sometimes, the power dissipated in the clock portion may

Table 2.1 Summary of the state-of-the-art ADCs over 10GS/s

| | [17] | [13] | [19] | [8] |
|---|---|---|---|---|
| No. of bits | 8 | 6 | 6 | 6 |
| Speed [GS/s] | 20 | 24 | 10.3 | 10.3 |
| T/H No. | 80 | 16 | 8 | 4 |
| Sub-ADC | Pipeline @250MS/s | TI of 10 SAR @150MS/s | Pipeline @1.3GS/s | Flash @2.5GS/s |
| Power [W] | 10 | 1.2 | 1.6 | 0.33 |
| ENOB [bit] | 6.5 @500MHz<br>4.6 @6GHz | 4.8 @8GHz<br>4.1 @12GHz | 5.8 @100MHz<br>5.1 @5GHz | 4.9 @100MHz<br>4.5 @5GHz |
| Process [nm] | 180 | 90 | 90 | 65 |
| FoM [pJ/conv] | 20.50 | 2.93 | 4.56 | 1.42 |
| | [14] | [15] | [20] | [21] |
| No. of bits | 6 | 8 | 5 | 6 |
| Speed [GS/s] | 40 | 56 | 12 | 16 |
| T/H No. | 16 | 4 | 8 | 8 |
| Sub-ADC | TI of 10 SAR @250MS/s | TI of 80 SAR @175MS/s | Flash @1.5GS/s | Flash @2GS/s |
| Power [W] | 1.5 | 9 | 0.081 | 0.435 |
| ENOB [bit] | 4.5 @10GHz<br>3.9 @18GHz | >5.7 | 4.3 @10MHz<br>3.9 @6GHz | 4.8 @170MHz<br>4.4 @3GHz |
| Process [nm] | 65 | 65 | 65 | 65 |
| FoM [pJ/conv] | 2.51 | 3.09 | 0.46 | 0.96 |
| | [22] | [23] | | |
| No. of bits | 6 | 6 | | |
| Speed [GS/s] | 10.3 | 8.5 – 11.5 | | |
| T/H No. | 4 | 4 | | |
| Sub-ADC | Flash @2.5GS/s | Rectified Flash @2.1~2.9GS/s | | |
| Power [W] | 0.24 | 0.195 | | |
| ENOB [bit] | 5.1 @5GHz | 4.6 @5GHz | | |
| Process [nm] | 40 | 40 | | |
| FoM [pJ/conv] | 0.70 | 0.59 | | |

even be dominant. On the other hand, if a small number of time-interleaved channels are employed, the sub-ADC has to handle very high conversion speed, usually leading

to significant power dissipation itself. Such option may be even harder if the speed requirement for the sub-ADC is beyond its ability.

The above analysis is also supported by Table 2.1, if more details are looked into. Among all the 10 works reported, [17] is the only one that utilizes more than 16 time-interleaved channels, using an 80-channel time-interleaved structure with a 250MS/s pipeline ADC digitizing input analog signal in each channel. Similar structure has not been reported thereafter, probably because there are so many channels that design complexity of the delay-locked loop (DLL), interpolators and dividers in the clock part is huge.

In the remaining works, some interesting facts can be found if the total sampling rate of 20GS/s is used as a boundary. The ADCs [13][14][15] working at higher speed than 20GS/s all employ the very similar architecture, that a small number (no more than 16) of distributed first-stage time-interleaved channels are selected, while each individual channel is made up of multiple SA ADCs which are time-interleaved in a second-stage to meet the extremely high speed requirement for sub-ADC. A smaller channel number may be preferred because the design complexity in the first-stage phase calibration circuit can be much relieved, but the penalty is that for each channel the bandwidth need to be larger and the time-interleaved sub-ADC has to implement more second-stage channels. Since the signal that each sub-ADC processes is steadily held by the first-stage T/H circuits, theoretically the phase misalignment of the multi-phase clocks inside the sub-ADC won't affect the overall performance. As can be

expected, in such cascaded time-interleaved architecture, the power consumed in the clock portion dominates over that in the bottom SA ADCs, but that is inevitable for such high-speed converters.

All the other converters running at lower than 20GS/s sampling rate, employ the one-stage distributed time-interleaved architecture. Flash structure is mostly used as the sub-ADC, mainly due to its unique robust ability to handle high sampling rate. As technology scales, the sub-ADC is able to work faster than before, and it is a trend now to further reduce the number of channels to save the resource invested in the clock portion. As is listed in Table 2.1, before 2010 most works published employed 8 channels while in 2013 the latest two both employed only 4 channels.

## 2.2. High-Speed Sub-channel ADC

### 2.2.1. Flash Architecture

Flash is the simplest ADC architecture. To achieve $N$ bit resolution the input voltage is simultaneously compared with $2^N$-1 of evenly spaced reference voltages, usually generated by a resistor ladder, by means of $2^N$-1 comparators which are parallel placed. The block diagram is shown in Figure 2.1.

The direct benefit from the flash architecture is it can achieve very high conversion speed, since all the $2^N$-1 comparisons take place at the same time. The conversion period is the time for one comparison plus that for the digital encoding. Because of

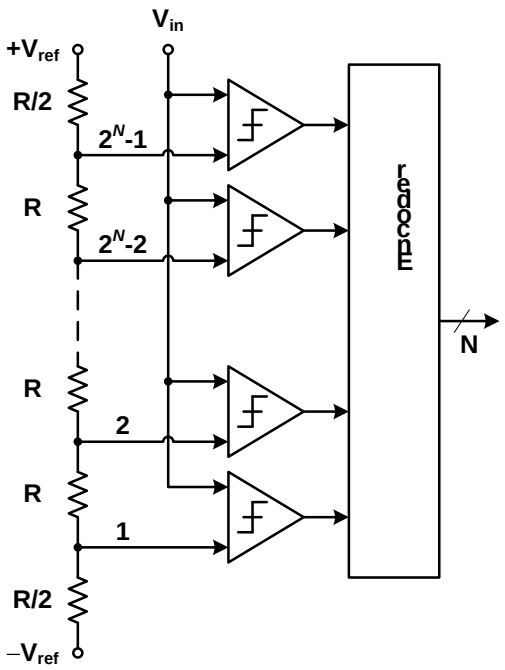



Figure 2.1: Typical architecture of *N*-bit Flash ADC

this reason, the flash architecture has been exclusively used for high-speed ADCs with conversion rate above 500MHz [24][25][26][27][28].

On the other hand, the drawbacks of the flash architecture are obvious too. As the number of comparators a flash ADC employs increases exponentially with the desired resolution, the resource it consumes becomes enormous. Even though with the offset calibration techniques, each comparator size can be made relatively small, the silicon area the whole ADC occupies is still considerably large, and the power consumption it uses is still significant. What is more, the input capacitance contributed by the large number of comparators is usually so great as to limit the signal bandwidth, and make time-interleaving multiple flash ADCs to obtain even higher sampling rate impractical.

It is noteworthy however, that 2-bit flash ADC is one special case as it only has 3 comparators for the 2-bit conversion, which seems promising in power efficiency. As a matter of fact, according to [29], the flash architecture may be more energy efficient than SA (to be discussed later) if the number of bits is smaller than a certain threshold, as illustrated in Figure 2.2(Fig. 4a in [29]). Therefore, considering one SA conversion process as a cascade of multiple SA conversion processes with a smaller number of bits, it can be seen the possibility of increasing sampling frequency and/or power efficiency by replacing each sub-conversion process with the flash architecture [30].

### 2.2.2. SA Architecture

Successive-approximation architecture is widely used due to its remarkable power efficiency. To the first order, the power consumption of SA scales linearly with its

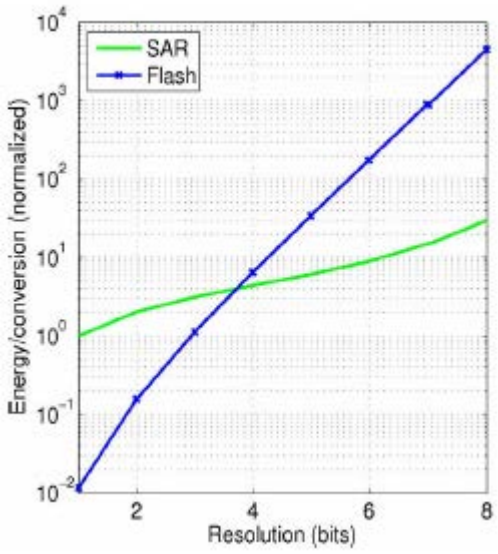



Figure 2.2: Modeled SA and flash ADC energies vs. resolution. [29]

resolution, making it an attractive candidate in the medium-resolution ADC applications. As technology scales from 130nm CMOS to 40nm, the ability of achieving faster processing speed of SA has been improving, therefore SA has also become increasingly popular in some high-speed ADC applications.

The conventional architecture of high-speed SA ADCs is illustrated in Figure 2.3, which consists of a single comparator to compare the analog signal with certain reference voltages bit by bit, a capacitive digital-to-analog convertor (DAC) to generate the successively-approximated reference voltages for each bit comparison, and a digital logic that both decodes the corresponding comparator outputs and

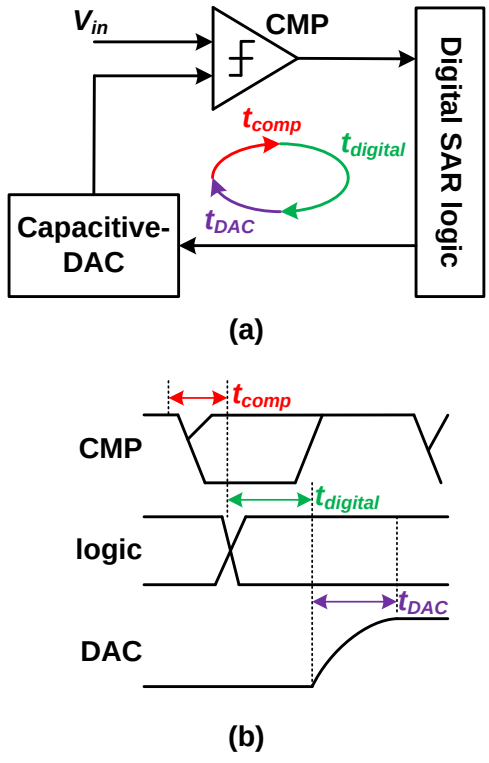



Figure 2.3: Conventional SA architecture with critical path.

controls the switching of the capacitive DAC in the critical path. The total conversion time to fulfill a single bit comparison is the sum of the time required for the comparator to resolve the current bit $t_{comp}$, the delay through the SA algorithm digital logic $t_{digital}$, and the settling time for performing the charge sharing within the capacitive DAC $t_{DAC}$:

$$T_{critical} = t_{comp} + t_{digital} + t_{DAC} \tag{2.1}$$

Among the above three terms in (2.1), $t_{comp}$ for a typical StrongARM latch-type dynamic comparator is divided into several phases (as shown in Figure 2.4[31]) [32], and expressed as follows:

$$t_{comp} = \underbrace{\frac{2C_L V_{thp}}{I_o}}_{t_o} + \underbrace{\frac{C_L}{g_{m,eff}} \ln\left(\frac{1}{V_{thp}}\sqrt{\frac{I_o}{2\beta}\frac{\Delta V_{out}}{\Delta V_{IN}}}\right)}_{t_{latch}} \tag{2.2}$$

In (2.2), the first term represents the time taken to discharge the differential outputs

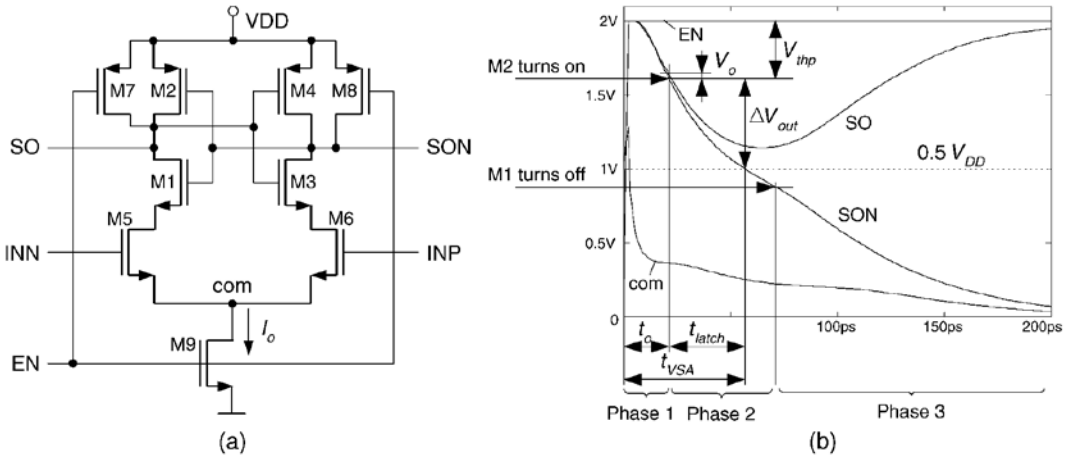



Figure 2.4: (a) StrongARM comparator; (b) its transient behavior. [31]

SO/SON from the preset value *VDD* to $VDD-V_{thp}$ at which point transistor M2 is barely turned on. $C_L$ is the loading capacitance at the outputs SO/SON, $I_o$ is the tail current during the discharging phase, and $V_{thp}$ is the threshold voltage of PMOS. The second term represents the time taken in the regeneration phase during which a positive feedback is performed. $\Delta V_{IN}$ is the input difference between INP and INN, $\Delta V_{out}$ is the voltage swing at the output at any instant of interest, $g_{m,eff}$ is the effective transconductance of the cross-coupled inverters, and $\beta$ is the technology-related constant. Obviously, $t_{comp}$ is input- and technology- dependent, and is constraint by power budget $I_o$. Even if the power budget can be ignored, its value is still bounded by the intrinsic parasitic capacitance contained in $C_L$. Therefore, there is always a lower limit for $t_{comp}$ once the precondition is set.

It is difficult to give quantitative estimation for the second term in (2.1), because such value will be different depending on various structures of the selected digital SA logic, which is employed to process the results of the current quantized bit and then controls the switches in the capacitive DAC based upon its state machine to generate corresponding analog reference voltages for the next bit comparison. The digital logic requires that the switches that have been previously set must maintain their state until the end of the entire conversion period; otherwise, the final generated digital output will be incorrect. An example given in [30] shows that this logic gate delay consumes up to 75% of the conversion period, thereby limiting any possibility for future speed improvements required for multi-gigahertz sampling rates.

Finally the third term in (2.1), the settling time of the capacitive DAC can be generally derived as below, assuming $R_{eff}$ and $C_{eff}$ are the effective on-resistance of the MOS switches and capacitance of the capacitive network. For the minimum amount of accuracy $V_{LSB}$ required, sufficient settling time must be allocated such that the residual error is small:

$$t_{DAC} = R_{eff}C_{eff} \ln \frac{|V_{step}|}{V_{LSB}} \tag{2.3}$$

In (2.3), $V_{step}$ is the voltage step size required for the current stage to settle, and $V_{LSB}$ is the LSB voltage determined by the full-scale input swing and the required resolution. With improved technology, the unit capacitance can be made extremely small (< 1fF in [33]). However, this trend of decreased capacitor size is limited by thermal noise, as well as layout complexity and uncertainty in parasitic capacitances. Moreover, the on-resistance of the MOS switches cannot be infinitely small either; otherwise the sizes of the switches have to be too large. Therefore, $t_{DAC}$ value is also constrained.

In order to improve the SA performance in term of operational speed, power consumption and accuracy, many techniques have been proposed in the past decade. Therefore it is of great benefit to review those techniques and have some discussion on their advantages and disadvantages.

*A) Synchronous vs. Asynchronous Conversion*

Architecture wise, the SA can be divided into synchronous [30] and asynchronous processing [2][34], which is illustrated in Figure 2.5. The synchronous processing

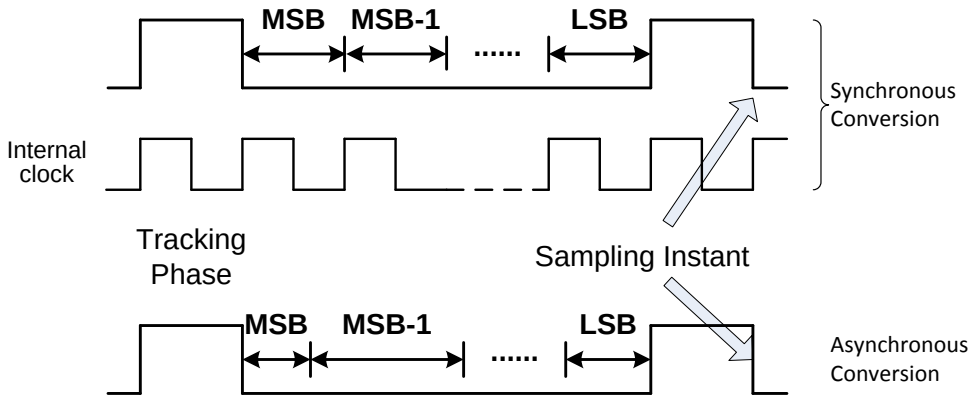



Figure 2.5: Synchronous and asynchronous SA comparison.

features an internal high-frequency clock which will trigger each bit comparison, and then reset the comparator. Typically, if the sampling rate of the ADC is $F_S$, and the targeted resolution is $N$, then the frequency of such internal clock need to be at least $(N+1)\cdot F_S$. On the other hand, the asynchronous processing does not require any internal clock, while every bit comparison is triggered by the completion of a preceding event (which can either be the sampling phase, or the last bit comparison).

According to (2.1) and (2.2), only the comparator delay $t_{comp}$ is dependent on the comparator input signal values. Due to the nature of the SA algorithm only one of these values will fall into the small region of ±1/2 LSB, which will lead to very long comparison delay and consequently very long conversion time $T_{critical}$. Therefore, as for the synchronous conversion, since the repeating internal clock has to make sure every bit conversion is fully complete, its period must be longer than the only and the largest $T_{critical}$. This will clearly cause a waste of time because other than the longest

conversion bit, the circuits will idle there waiting for the next rising edge of the internal clock to come, even though the current bit conversion is already settled. From this point of view, the asynchronous architecture takes great advantage of faster processing cycles, because once the current bit conversion is complete the next will be started and no time is spent waiting.

*B) Comparator offset calibration*

The input referred offset of the comparator used in the ADC will possibly degrade the overall ADC performance, so it is better to be minimized. Such offset is primarily a function of threshold mismatch and transistor dimension as below:

$$\sigma_{V_t} = \frac{A_{V_t}}{\sqrt{W \cdot L}} \tag{2.4}$$

Obviously, in order to reduce the offset by 2 times, the transistor size need to be increased by 4 times. Such calculation shows that it is not practical due to the excessive area and power consumption cost, and offset calibration is necessary to efficiently achieve good accuracy.

The basic idea for the calibration is to deliberately introduce some imbalance to compensate for the offset. Such imbalance can be either by capacitance loading [35] or current injection[36], or even voltage difference [30]. To calibrate the offset, the differential inputs of the comparator are usually tied together to a certain common-mode voltage, which should be the same as that when the comparator is really working, and the comparator output is monitored and fed back to the state machine which

controls the imbalance. When the offset is well compensated, the digitized output should have almost equal chance of logic 0's and 1's.

Depending on when the calibration is performed, the calibration structure can be divided into foreground [35][36] and background [30]. In the foreground structure, the calibration will be performed before the real circuit operation, during which the imbalance for compensation will be obtained and used all the way through the following operation. Such method is less complicated, but cannot account for any change of offset due to the long term drift of circuit voltage or temperature. Therefore, it is suitable for the application that does not require very accurate offset compensation. On the other hand, the calibration will be performed during the real circuit operation in the background structure, so that it can timely cancel the offset whenever it is drifting and is much more accurate. However, the cost is that a separate calibration phase is required every one or several period, which will affect the overall conversion speed.

*C) Capacitive network (DAC) solutions*

Several architectural possibilities exist for the capacitive DAC. By connection style it can be divided into parallel [37] and serial [2][33][34] structures, and by radix into binary [34][37] and non-binary [2][33] structures.

Most parallel capacitive DACs are binary ($\alpha$=2 in Figure 2.6(a)), which is the first structure used in SA ADC as well as the most straightforward. As is well known, such DAC generates a voltage that increases or decreases by half of the reference voltage for the first step, then by a value which is half of the previous one for the followings.

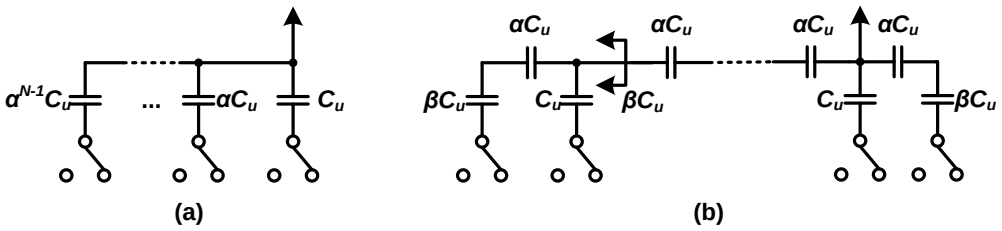



Figure 2.6: (a) Parallel connection; (b) serial connection of capacitive DAC.

For such structure, it is relatively easy to make the capacitors inside the DAC well matched to achieve good accuracy and linearity, and the effect of any parasitic capacitance can be minimized by connecting the switches to the bottom plates of the capacitors. However, the penalty is that the total capacitance of the DAC will increase exponentially with the resolution *N*, which will lead to large loading for preceding stage and cause significant power consumption. To reduce the power consumed by dynamic switching in the DAC, some energy-efficient structures such as capacitor-splitting [38][39] and junction-splitting [40][41] have been presented.

The schematic of a serial-connected capacitive network is shown in Figure 2.6(b). To perform successive approximation procedure, it is wanted that:

$$\begin{cases} \beta = 1 + \alpha \parallel \beta \\ Radix = 1 + (\beta/\alpha) \end{cases} \tag{2.5}$$

where the operator ∥ is defined as $x \parallel y = x \cdot y/(x + y)$. When α=β=2, the radix is 2 and the capacitive network is binary, otherwise it is non-binary. Non-binary network actually has a radix less than 2, which introduces redundancy to allow decision errors for faster settling. The overlapped search range can compensate for wrong decisions

made in earlier stages if they are within the error tolerance range. It can be calculated that no matter how large the resolution *N* is, the total input capacitance of the serial-connected capacitive network $C_{in}$ does not increase:

$$C_{in} = [1 + 2 \cdot (\alpha \parallel \beta)] \cdot C_u \tag{2.6}$$

Despite the benefit of its small loading capacitance for fast settling, the series capacitive network heavily suffers from the parasitic capacitance. Considering the parasitic capacitance from interconnects and the top and/or bottom plates of capacitors themselves, (2.5) must be modified [2][34] accordingly. Even though, such parasitics is non-consistent thus it is impossible to accurately determine their values in the design/layout phase. Calibration based on the LMS algorithm [2] is required.

*D) SA logic improvement*

Several methods have been proposed to reduce the delay of the digital SA logic, such as employing flip-flop bypass SA logic [30] and a semi-closed digital loop [34]. The former technique removes a D-flip-flop between the comparator outputs and the capacitive network, but still requires a mux to select different control bits depending on the state machine. The latter technique enables some overlapping between the comparison time and the SA logic processing time to expedite the processing.

### 2.2.3. Binary-Search Architecture

Binary-search ADC [42][43] can be viewed as a transitional structure between flash and SA ADCs. As shown in Figure 2.7, it consists of $2^N$-1 comparators as in the

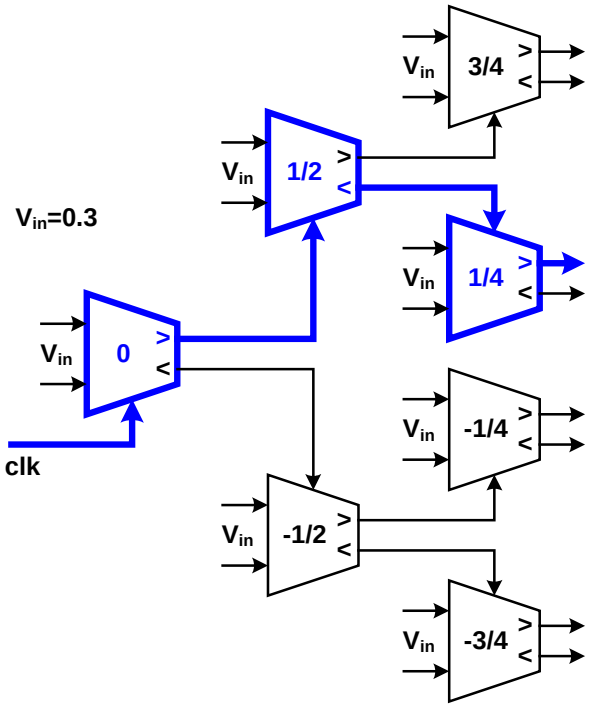



Figure 2.7: Block diagram of binary-search architecture.

flash structure, but only *N* of them are really activated during every *N* bit conversion as the SA approach. Similar to the flash ADC, the reference level of each comparator can be provided by a resistor ladder, therefore it can save the settling time from the capacitive DAC as in the SA ADC. Theoretically, the binary-search architecture takes the advantages of both flash and SA, and achieves the balance between high operational speed and low power consumption. However, some disadvantages from the flash remain for the binary-search structure, including the large area and consequently large loading for preceding stage.

## 2.3. Time-Interleaved Track-and-Hold Circuit

### 2.3.1. Overview and Quantitative Analysis

To achieve the high sampling rate of over 10GS/s, the time-interleaved (TI) architecture is the only solution. As is shown in Figure 2.8, a time-interleaved ADC is an ADC that cycles through a set of *N* sub-ADCs, such that the aggregate sampling rate is *N* times that of the individual sub-ADCs.

In the time domain, ignoring quantization, each sub-ADC output can be expressed as:

$$y_i[n] = x\big((nN + i)T_s\big) \tag{2.7}$$

In (2.7), $T_s$ is the sampling period of the time-interleaved ADC, *N* is the number of sub-channels (so that $N \cdot T_s$ is the sampling period of a single sub-ADC), and *i*=0, 1, …,

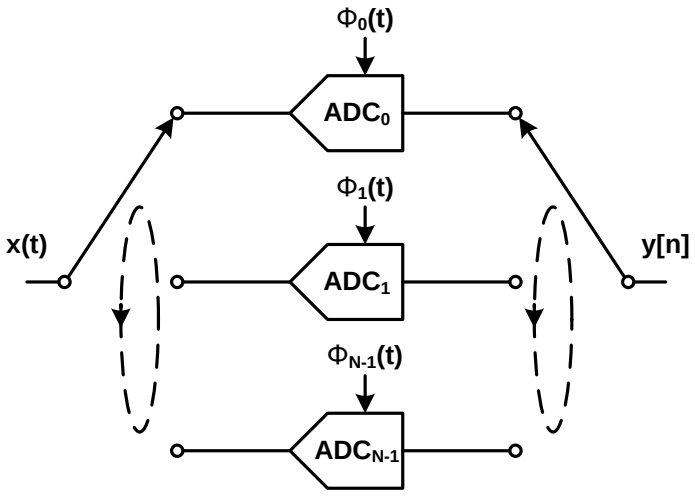



Figure 2.8: Block diagram of time-interleaved architecture.

*N*-1 denotes the sequence of the channel. By using multiplexer at the output side, the streams from all the *N* channels are combined such that

$$y[n] = [y_0[0], y_0[0], \cdots, y_{N-1}[0], y_0[1] \cdots] = y_i\left[\frac{n-i}{N}\right], i = n \bmod N \quad (2.8)$$

Combining (2.7) and (2.8), we have:

$$y[n] = x(nT_s) \quad (2.9)$$

which is the same output as a single ADC with the sampling rate of $1/T_s$.

On the other hand, in the frequency domain, discrete Fourier transform (DFT) can be applied to each individual sub-ADC outputs (sampled at the sampling rate of the time-interleaved ADC), and the results add up to that when DFT is applied to the time-interleaved ADC. Given a discrete set of real number $x[n]$, the DFT of $x[n]$ is:

$$X(\omega) = \sum_{n=-\infty}^{+\infty} x[n]e^{-i\omega n} \quad (2.10)$$

and in theory the following equation holds:

$$Y[f] = \sum_{i=0}^{N-1} Y_i(f) \quad (2.11)$$

in which $Y_i(f)$ is the DFT of the upsampled sub-ADC output, and $N$ is the channel number.

In practice, however, there exist a lot of non-ideal errors in the time-interleaved channels, including the voltage offset, gain, timing skew, bandwidth and nonlinearity, as shown in Figure 2.9. Such errors result from PVT (process, voltage, temperature) variation, layout nonidealities, and mismatch in capacitance and so on, all of which will limit the overall ADC performance. For example, the offset differences in each

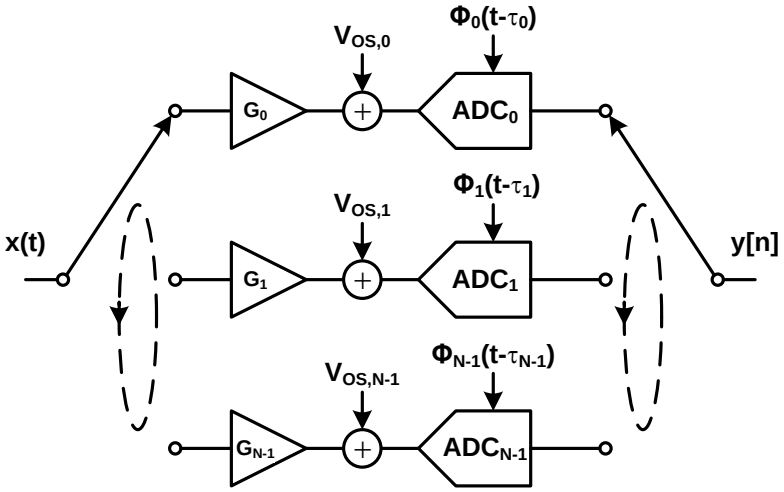



Figure 2.9: Time-varying errors in TI ADC: offset, gain and timing skew.

channel will introduce spurs at frequencies $i \cdot f_s/N$, and the gain differences and timing skews will cause spurs at $f_{in}$-$i \cdot f_s/N$. While it is possible to insert a programmable gain amplifier (PGA) in each sub-channel to compensate for offset and gain mismatch [8], it is more challenging to deal with the static timing skew or phase mismatch.

Mismatches in different time-interleaved channels in offset, gain, and sampling phase will cause degradation in the SNDR (signal to noise and distortion ratio) performance. In [44] the quantitative results of the bound on the offset, the gain, and the timing skew have been derived:

$$\sigma_{offset} = \sqrt{\frac{N}{N-1} \cdot \frac{A^2}{3 \cdot 2^{2B}}} \tag{2.12}$$

$$\sigma_{gain} = \sqrt{\frac{N}{N-1} \cdot \frac{2}{3 \cdot 2^{2B}}} \tag{2.13}$$

$$\sigma_{timing} = \sqrt{\frac{N}{N-1} \cdot \frac{2}{3 \cdot 2^{2B} \cdot (2\pi f_{in})^2}} \tag{2.14}$$

where $N$ is the number of time-interleaved channels, $A$ is the input signal amplitude, $f_{in}$ is the input signal frequency, and $B$ is the desired number of bits. According to (2.14), the relation between the ADC resolution and the standard deviation of timing skew for different input signal frequency can be plotted as in Figure 2.10 ($N$=8).

Besides the static errors as described above, the dynamic sampling clock jitter can also cause noise at the T/H output. Unlike the static errors that can be eventually calibrated, the clock jitter is more intrinsic. The SNR of T/H output due to the sampling clock jitter with RMS value of $\varepsilon_{rms}$ is given by [1] as below:

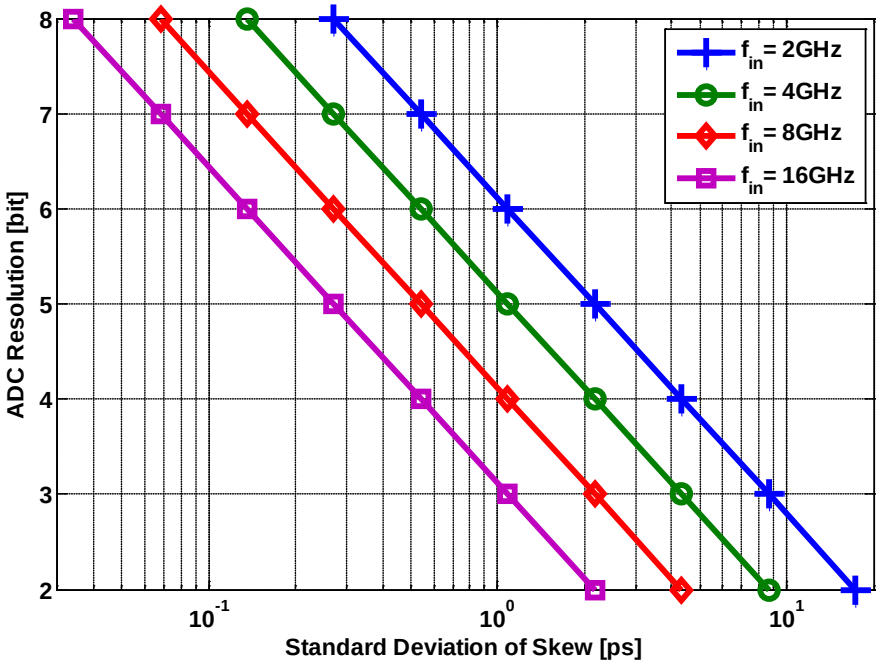



Figure 2.10: ADC resolution vs. timing skew standard deviation.

$$\mathrm{SNR} = -20\log(2\pi \cdot f_{in}\varepsilon_{rms}) \tag{2.15}$$

where $f_{in}$ is the input sinusoidal signal frequency. Based on (2.15) the relation between the ENOB (effective number of bits) of ADC and the RMS jitter can also be obtained and plotted in Figure 2.11.

### 2.3.2. Global Architecture

In general, there are two types of time-interleaved T/H circuits, namely the global and the distributed architecture. The global T/H as shown in Figure 2.12 features a global buffer running at the highest sampling frequency of $f_s$ in the front-end, whose

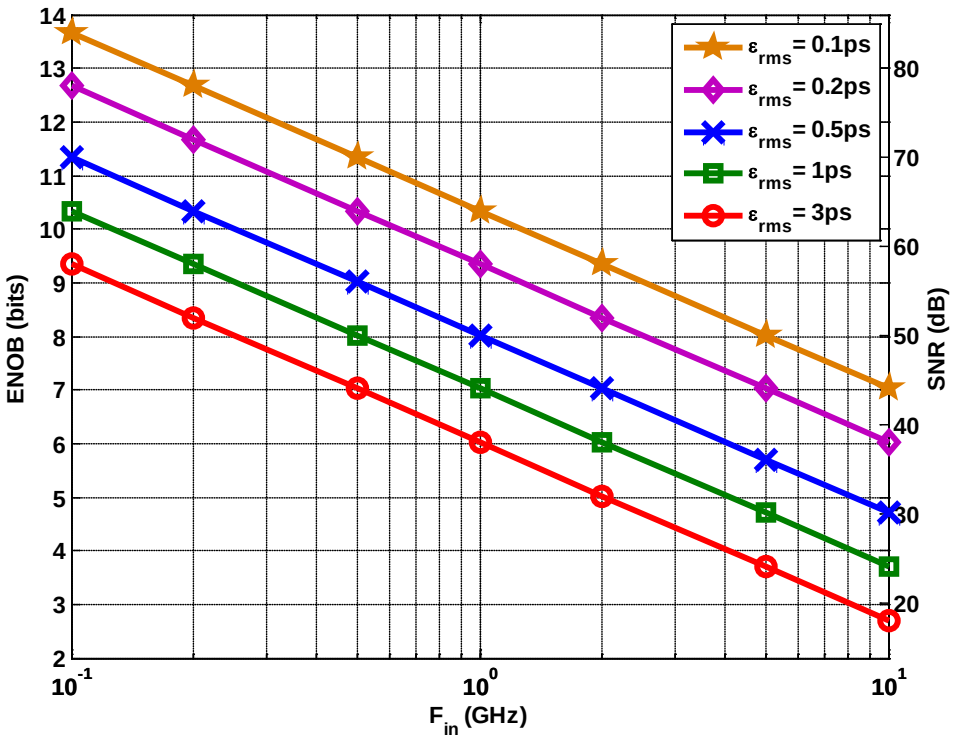



Figure 2.11: ENOB and SNR vs. clock jitter and input frequency.

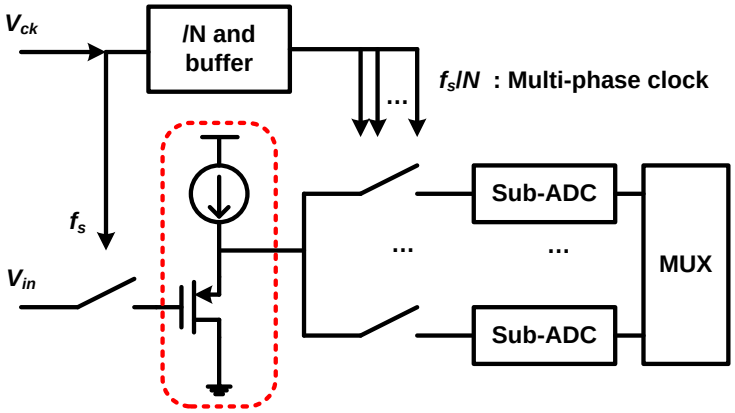



Figure 2.12: Global time-interleaved track-and-hold topology.

output is sampled again by the multi-phase clock running at the low sampling frequency of $f_s/N$ for the array of $N$ sub-ADCs. Because the signal at the buffer output has already been held, the timing error in the following time-interleaved T/Hs is no longer a problem.

However, the immunity to multi-phase timing skew of the global time-interleaved T/H structure is obtained at the cost of the very high requirement for the global buffer. The buffer must be able to handle the full tracking bandwidth while driving a considerably large loading caused by multiple sub-ADCs. Besides, such buffer needs to provide very good linearity, depending on the resolution specification of the ADC. For a typical circuit used as such buffer, the source follower suffers from the nonlinearity resulted from the threshold voltage and the channel length modulation effect. In order to mitigate such problems, techniques such as replica well-biasing[45] and constant $V_{DS}$ by additional clamping[46] have been proposed.

Because of the difficulty designing a perfect buffer at high frequency as discussed above, the global time-interleaved T/H structure is mainly used in the applications less than or around 1-GS/s sampling rates [30][33][46][47], while for multi-GS/s sampling ADCs, distributed time-interleaved T/H is more frequently employed.

### 2.3.3. Distributed Architecture

Distributed time-interleaved T/H driven by multi-phase clocks is a more power-efficient architecture (Figure 2.13). But the problem in this topology is the sampling timing error, which is usually caused by the mismatch in the multi-phase clock paths as well as in different signal channels, need to be minimized. Therefore complicated calibration techniques are required to detect and compensate the timing errors.

For example, [17] presents a foreground phase error calibration. Pulse train with fast edges is applied to the time-interleaved ADC, and based on FFT results phase delay of T/H is detected and adjusted. Such procedure is repeated until the phase

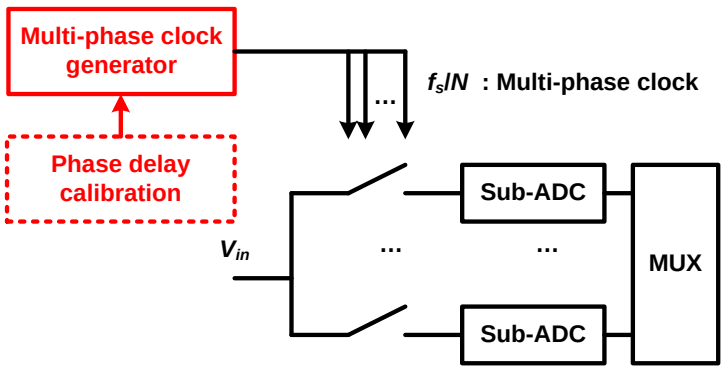



Figure 2.13: Distributed time-interleaved track-and-hold topology.

alignment is optimized. In [48] another foreground calibration based on histogram counting is proposed. Two quantizer-based phase detectors sample the outputs of adjacent track/hold circuits, detecting any phase offsets arising from process and dimension mismatches both in the clock path and the T/H switches. Finally, a background timing skew calibration is introduced in [20]. An extra channel with a 1-bit ADC is added, and the correlation between that extra ADC and each sub-ADC is measured. The timing skew is detected in the digital domain and minimized by adjusting digitally controlled delay lines when the correlation is maximized.

# 3. A Single-Channel Asynchronous Successive-Approximation ADC with Improved Feedback Loop

## 3.1. Proposed Architecture

As already discussed in Section 2.2.2, in the conventional structure, the aforementioned three SA operations occur successively in time. Because the comparator must wait for the capacitive DAC to be fully settled before it can start the comparison, $t_{comp}$ and $t_{DAC}$ cannot occur simultaneously. However, the digital logic processing does not necessarily require separate time durations other than $t_{comp}$ and $t_{DAC}$. In order to explore the timing benefits of performing the digital SA algorithm at the same time while the capacitive DAC is settling, an asynchronous SA ADC with improved feedback delay is proposed, as shown in Figure 3.1 [49].

The proposed SA ADC architecture features two new techniques. Unlike a conventional architecture that uses a single comparator followed by digital logic to determine, store, and transfer the comparison results, the new architecture uses $N$ comparators for $N$-bit conversion, storing each comparison result into the digital output of each comparator. These digital outputs are utilized simultaneously in two parallel paths: one is directly to the capacitive DAC, such that the DAC can respond to the results promptly and generate the successively-approximated analog signal quickly without being delayed by any digital logic; the other is to a digital clock generator that detects the completion of the current quantization and then generates a “ready” signal

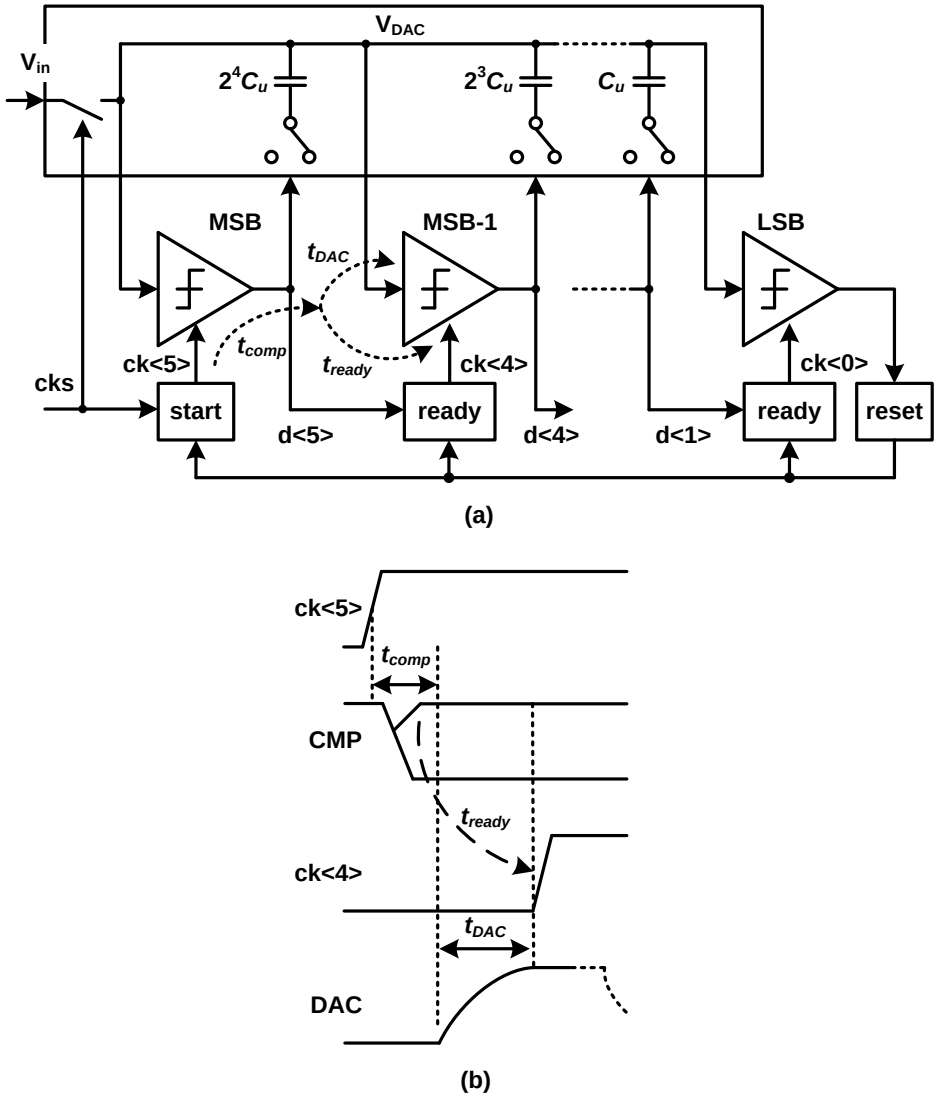



Figure 3.1: (a) Proposed architecture of the asynchronous SA ADC with improved feedback delay; (b) critical path for a one-bit conversion.

to clock the next quantization. Both paths occur simultaneously, so that the critical path is reduced to:

$$T_{critical} = t_{comp} + \max[t_{ready}, t_{DAC}] = t_{comp} + t_{ready} \quad (3.1)$$

In order to improve the conversion as much as possible, any unnecessary buffer delays are to be avoided. Therefore, all digital logic gates were customized using logical effort [50] to optimize the gate delay and power consumption. Note that the time delay required for generating the ready signal must be made adequately longer than the settling time of the DAC. Compared to (2.1), the critical path in the proposed design is significantly improved over a conventional SA-ADC.

Second, the proposed structure makes it natural to adopt asynchronous processing, taking advantage of the average quantization delay as opposed to the worst-case delay, as there will only be one quantization when the input level is less than 1/2 LSB due to the binary SA algorithm. After the completion of the front-end track and hold, which is determined by the global periodic clock *cks*, the quantization of the MSB cell is initiated, followed by the proceeding quantizations from MSB-1 to LSB, triggered like dominoes from the outputs of the ready logic. The *reset* signal, generated from the LSB cell, will then precharge all the comparators and the capacitive DAC, preparing the entire SA-ADC for the next conversion. One additional benefit of the proposed architecture is that the resolution of the SA ADC can be easily digitally programmed by disabling the last LSB cell, using the *ready* signal of the LSB-1 cell as the *reset* signal. This programmability may be useful for applications where higher sampling rate is preferred over higher resolution.

Signal voltages for a typical conversion period of the 6-bit SA ADC are simulated and shown in Figure 3.2. After the falling edge of the *cks* signal, the clocks that

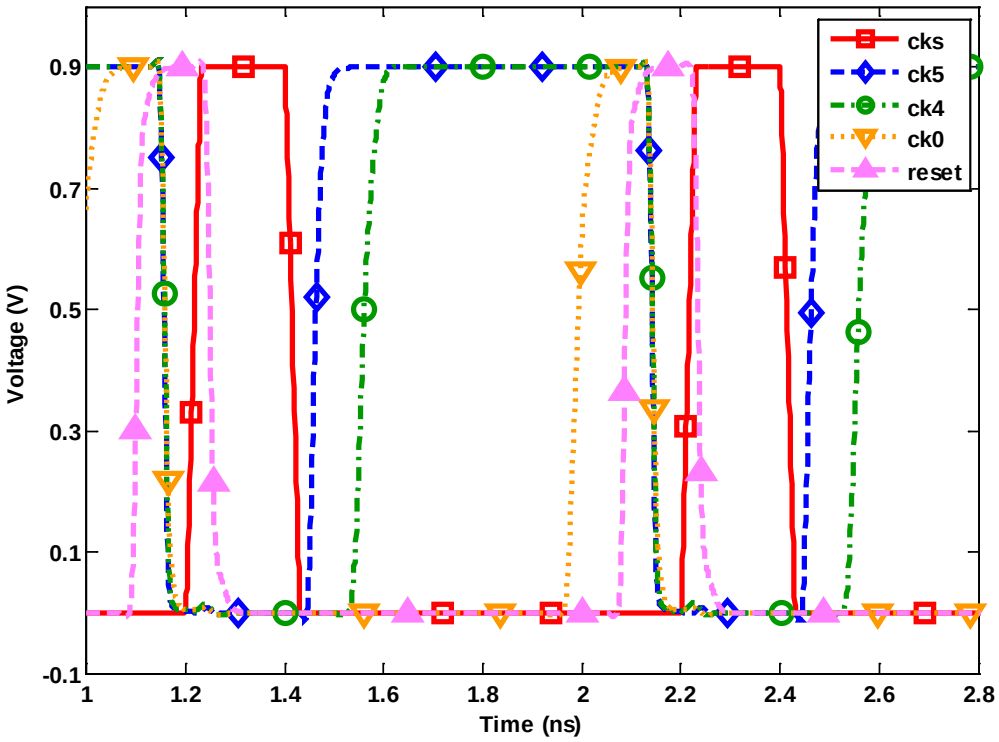



Figure 3.2: Simulated waveforms for one single conversion period of the proposed SA ADC.

trigger the comparison from MSB to LSB are generated sequentially. These clocks will maintain their logic high state until the *reset* signal is generated to pull them down to a logic low value. The final *reset* signal will be disabled at the beginning of each period so as not to impact normal operation.

Besides the features previously discussed, there are some other important considerations. First, each of the six comparators starts its own quantization triggered by the preceding *ready* signal, but all quantizers are precharged and reset only when the LSB comparison is completed. During every conversion period, each of the six

comparators only makes one quantization, and afterwards they each hold the comparison results for the rest of the period to ensure that the DAC performs correctly. In comparison, a conventional 6-bit SA ADC consists of only one comparator, but that comparator performs quantization six times. Therefore, the energy consumption in the above two cases is comparable, as the static energy consumption for a dynamic comparator is negligible at this sample rate. Second, the comparison results of each comparator will be passed through an R-S latch which is not within the critical path, with all six outputs retimed as the final digital bits.

## 3.2. Circuit Implementation

Several critical circuit blocks are described in detail in the following sections.

### 3.2.1. Capacitive DAC

A conventional parallel binary capacitive DAC (Figure 3.3) is employed, except with one minor change -- the capacitor directly connected to ground is made $17C_u$ rather than $C_u$. Considering the parasitic capacitance $\Delta C$ contributed by the six paralleled comparators is considerable, the real reference voltage should be adjusted as follows:

$$V_{ref} = 1.5 \times V_{FS} \times (1 + \Delta C/48C_u) \quad (3.2)$$

In this way, the reference voltage is deliberately set to be over 750mV, while the full-scale input voltage is 500mV as defined by the system specifications. The bottom

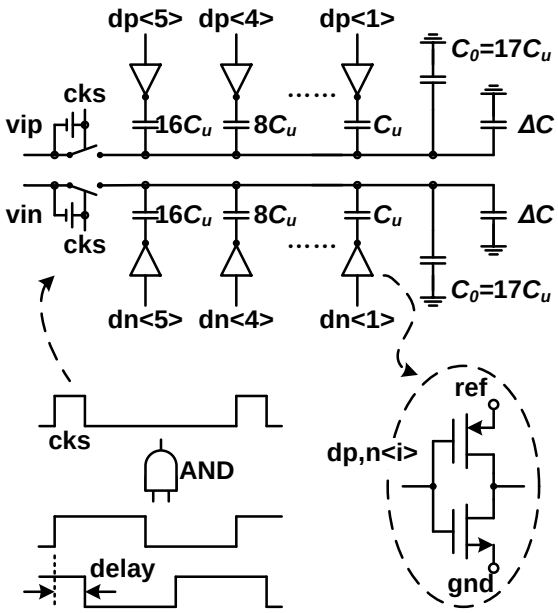



Figure 3.3: Schematic of the capacitive DAC, and generation of the sampling clock.

plates of the binary weighted capacitors are connected to ground through NMOS switches and to the reference voltage through PMOS switches, such that parasitic MOS switch capacitances do not affect the final accuracy of the DAC settling. Each pair of the MOS switches is gated by the same control signal which is either the positive or negative output of a corresponding comparator, so that the connection is similar to an inverter with the reference voltage as its supply. The reference voltage is preferred to be made large in order to improve the switching speed of the PMOS. To reduce design complexity, all the switches were designed to be the same size, even though the binary-weighted capacitors they connected varied significantly in size. For an improved future design, power consumption can be further reduced if both the

switches and the corresponding comparators are sized accordingly based on the different capacitor values. One drawback of the DAC used in the design, however, is that only one of the positive and negative outputs of the DAC is increased by the ratio of the reference voltage, making the overall differential output change up or down. Hence, while the differential voltage is generated correctly, the common-mode voltage may actually drift. This will cause the comparator offset to vary for different input common-mode values, leading to uncompensated offset for particular input voltage levels.

Given the limited time to perform data conversion when the frequency is high, the time allocated for signal sampling and conversion has to be compromised. Depending on the number of bits needed to be resolved, the on-resistance of the T/H switch *R*, and the loading capacitance *C*, the required time taken for adequate sampling can be estimated. Unfortunately, due to process variations the exact values of *RC* delay cannot be known, so that it is necessary to provide some calibration of the clock pulse externally. This optimized pulse width can be selected at startup, when the best SNDR performance is evaluated and then statically set.

### 3.2.2. Bootstrapped Switch

Bootstrapped switches are employed (Figure 3.4) in the sampling circuit in order to achieve both smaller on-resistance and minimal signal-dependent sampling distortion. As was previously illustrated in [51], when the sampling clock *cks* is low, the switch $M_0$ is shorted to ground and the capacitor is charged to near the supply voltage. When

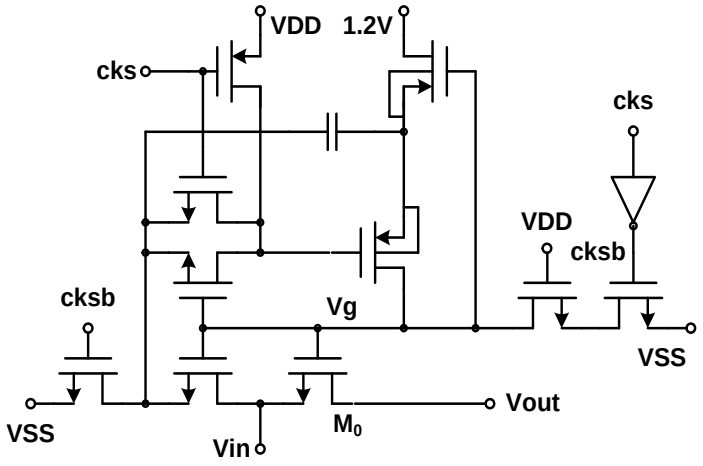



Figure 3.4: Bootstrapped switch used in the capacitive DAC

*cks* is high, the large voltage difference across the capacitor will be added to the input signal and then applied to the gate of the pass switch, making the gate-source voltage of the NMOS close to that high voltage constantly. In order to reduce the on-resistance of the bootstrapped switch such that the T/H circuit can meet the hard timing requirement, a 1.2V external supply voltage is used for charging the capacitor. This circuit is carefully designed so that no voltage difference between any two nodes of a single MOS transistor is larger than the nominal voltage of 1V for the technology.

### 3.2.3. Comparator with Offset Cancellation

Six StrongARM comparators with offset cancellation [35] (Figure 3.5) are used for the entire 6-bit quantization. When the clock *ck* is reset to ground, both the positive and negative outputs are shorted to the supply voltage, shorting all the bottom plates of the capacitors in the DAC to ground. Clocked by the ready signal from the preceding

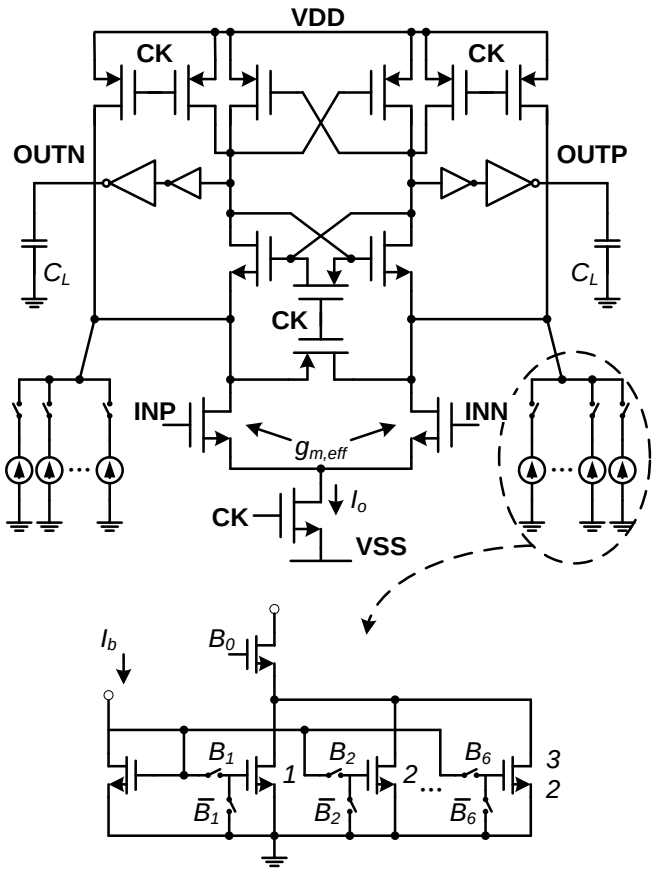



Figure 3.5: Comparator design with current steering offset cancellation circuit.

conversion, each comparator evaluates the analog input signal and the corresponding differential outputs begin to split to the supply voltage and ground, respectively. Buffered by two stages of inverters, the regenerated outputs are directly sent to the switch gates of the capacitive DAC, and are kept high until reset occurs at the end of the 6-bit conversion. The two inverters are sized such that they can provide enough drive ability while minimizing the loading seen by the regeneration nodes. To mitigate hysteresis during the quantization, all the internal nodes are also shorted to

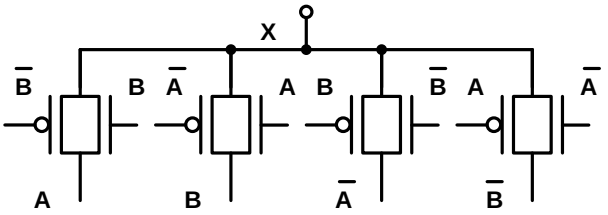
the supply voltage during the precharge phase. Unlike a conventional structure where only one comparator is used, each of the six comparators exhibit a different mismatch such that the offset is no longer a systematic error that can be subtracted during post-processing. Therefore, foreground offset calibration for each comparator is performed at startup, where an offset cancellation circuit composed of two sets of 7-bit binary current sources is used [36]. Since this 6-bit ADC has a relatively large LSB (approximately 15mV), the calibration requirements are not very strict. During calibration, the ADC is fed with the differential voltages that cause metastability to a specified comparator. The corresponding comparator digital output is monitored on the oscilloscope, and the control bits are tuned until metastability is observed. Current imbalance using a digitally-controllable current mirror is used, such that the effect on the regeneration speed due to the added capacitance is minimized. In addition, pseudo-common-gate isolation reduces the effect of parasitic loading on the comparator speed. In this design, the transistors in the comparator were sized large, such that the 3-sigma Monte Carlo offset was simulated to be within 50mV. In the simulation, offsets ranging from 1mV to 50mV can be cancelled when turning ON and OFF corresponding current sources. Although there will be some static current through the offset cancellation circuit during the precharge phase since the current mirror is pulled up to supply, the injected current is minor and negligible. According to simulations, the LSB value in the binary current source is around 2μA for cancelling the offset voltage.

### 3.2.4. Digital Logic

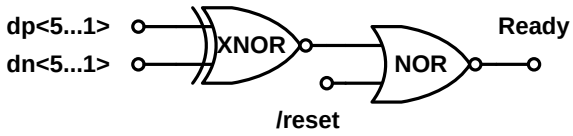
As shown in Figure 3.1, each of the six comparators is followed by a digital detection circuit that determines if the current quantization is complete, followed by generation of an asynchronous clock to trigger the next quantization. The comparator in the first MSB cell is triggered by the falling edge of the sampling clock *cks*, while the other five comparators are triggered by the *ready* signals from each preceding cell. The LSB cell generates a *reset* signal that is used to reset all of the six comparators, shorting the bottom plates of the capacitors in the capacitor network to ground during the next sampling phase.

Since the comparator is precharged to the supply voltage every reset interval, its differential outputs can only exhibit “11” to “10” or “01”. In a time-constrained system such as a high-speed ADC, a NAND gate for the ready logic might be preferred due to its single-stage delay. However, the NAND must be carefully designed in order to minimize the probability of making a wrong decision. For example, if the comparator is metastable, it will take a long time for its differential outputs to split, such that it is possible for both differential outputs to briefly become lower than the threshold voltage. Hence, the comparator outputs will be “00”, and therefore erroneously generate the *ready* signal, even if the comparison is far from complete. On the other hand, an XOR gate, typically formed by two cascaded stages of NAND gates, may be more robust since it will not generate a clock under the “00” situation, but suffers from relatively long delay. Therefore, a double-pass-transistor

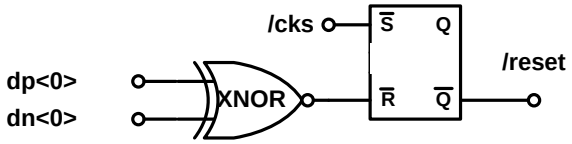
logic (DPL) circuit [52], generated by only one stage of pass-gates, is employed to reduce the gate delay while making the correct decisions. The final ready logic is designed according to De Morgan's law and shown in Figure 3.6. Instead of using an XOR and an AND gate, an XNOR and NOR gate are used to remove one-stage of




(a)




(b)




(c)

| XNOR | | |
|---|---|---|
| A | B | X |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

| RS latch | | |
|---|---|---|
| $\overline{S}$ | $\overline{R}$ | $\overline{Q}$ |
| 0 | 0 | X |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | keep |

(d)

Figure 3.6: (a) Schematic of the DPL XNOR; (b) the "ready" signal generator; (c) the "reset" signal generation circuit; (d) truth tables of the XNOR and RS latch.

delay. The output of the XNOR and the complementary /*reset* signal are passed through the NOR gate, generating the trigger signal for clocking the next quantization. The generation of the /*reset* signal is slightly different. The /*reset* signal should only be pulled up until all the *ready* signals are reset to zero. Since all the differential outputs of the comparators are precharged to the supply voltage, the outputs of all the XNOR gates are reset to the supply voltage, and the */reset* signal must be pulled down again. Otherwise, the *ready* signals will be always kept low. Therefore, an RS latch is used, using the supplementary sampling clock (*/cks*) to reset the */reset* signal at the beginning of each period.

## 3.3. Metastability Detection

Metastability occurs when the input signal level is so small that the comparator consumes an excessive amount of time to complete a quantization. An asynchronous approach is one way to mitigate metastability issues, when compared with its synchronous counterparts. With synchronous processing, the next bit quantization will be periodically reset by an external clock regardless of whether the current bit quantization has completed. On the other hand, with the asynchronous design, the next bit of quantization will not take place until the current one is completed, no matter how long it will take. Therefore, if metastability can be detected as early as possible, the digital ADC outputs can be forced to exact values without completing the remaining quantizations, improving delay as well as power consumption.

In [34], an off-line correction of metastability is proposed, where an on-chip circuit is utilized to count the number of conversions completed in each period, and is then post-processed accordingly. In this work, an on-chip metastability detector [53] is designed to detect the occurrence of the metastability, stop the current conversion, and then force the remaining quantizers' outputs to one digital "1" for the current, and all digital "0"s for the rest bits. In this manner, a one-bit error at various input levels will be deliberately introduced, such that the probability of a metastable occurrence preventing further quantizations is minimized.

If the value of the differential input voltage to the comparator is smaller than a particular reference value, the time consumed to resolve that input will take longer than the time needed to resolve the reference voltage. Therefore, by comparing two delays, the relation between two voltages can be known. Based on this idea, the block diagram of the *i*th cell with the proposed metastability detector is proposed (Figure 3.7), with two timing paths that are generated from the input clock. The top path is the operational delay that includes the comparator and the ready signal generator, while the bottom one is a tunable reference delay path. When the input signal level is small enough to be essentially ignored, the delay in the top path will be longer than that in the bottom one, such that the phase detector will generate a flag signal indicating the occurrence of metastability. This flag signal will be processed in the metastability detection logic and then fed back to the current bit, with each of the subsequent unit cells forced to a preselected output. In this design, for simplicity, a D flip-flop is used

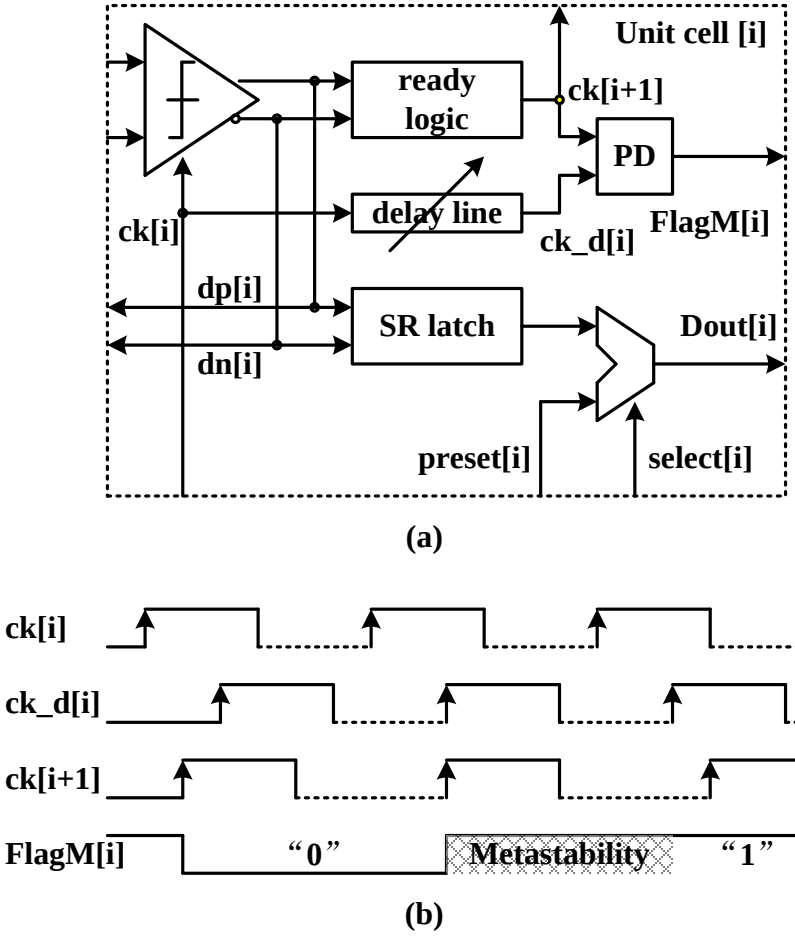



Figure 3.7: (a) Schematic of the *i*th cell with the metastability detector circuit; (b) the illustration of the detector flag signal.

as the phase detector, with *ck*[*i*+1] as its input and *ck_d*[*i*] as its clock. In this way, the D flip-flop is designed to make a quick decision at the penalty of tolerable inaccuracy, as the input voltage is already very small. As shown in the figure, if the rising edge of *ck*[*i*+1] comes later than that of *ck_d*[*i*], the flag signal *FlagM*[*i*] will become high and the conversion will be stopped; otherwise, the entire conversion will not be

interrupted. Unfortunately, this metastability detector also heavily relies on the performance of the phase detector itself. Although the D flip-flop is carefully designed, it is still possible that the D-FF phase detector itself may enter metastability and take a very long time to generate the flag signal, if *ck*[*i*+1] and *ck_d*[*i*] arise too close to each other. An estimation of the probability of metastability occurrence for the comparator in the voltage domain and the flip-flop in the time domain can be derived (See Appendix A: Metastability in the Voltage and Time Domain).

Measurement waveforms are shown in Figure 3.8, indicating how this metastability detector operates. A small differential ramp signal from -20mV to 20mV is injected, with the sampling clock running at 800MS/s, and the waveforms of the first four bits of the ADC are recovered using an oscilloscope. It is observed that when the metastability detector is turned OFF, and the offset cancellation has tuned the

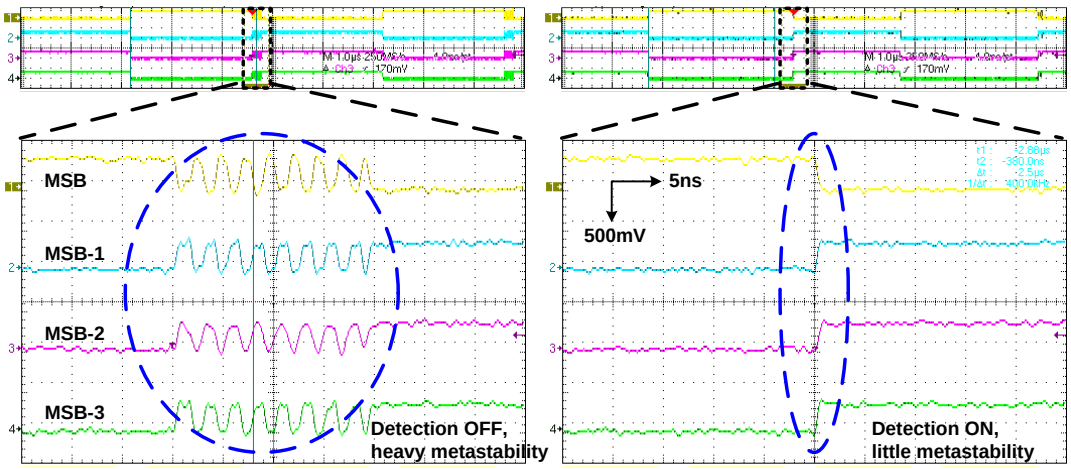
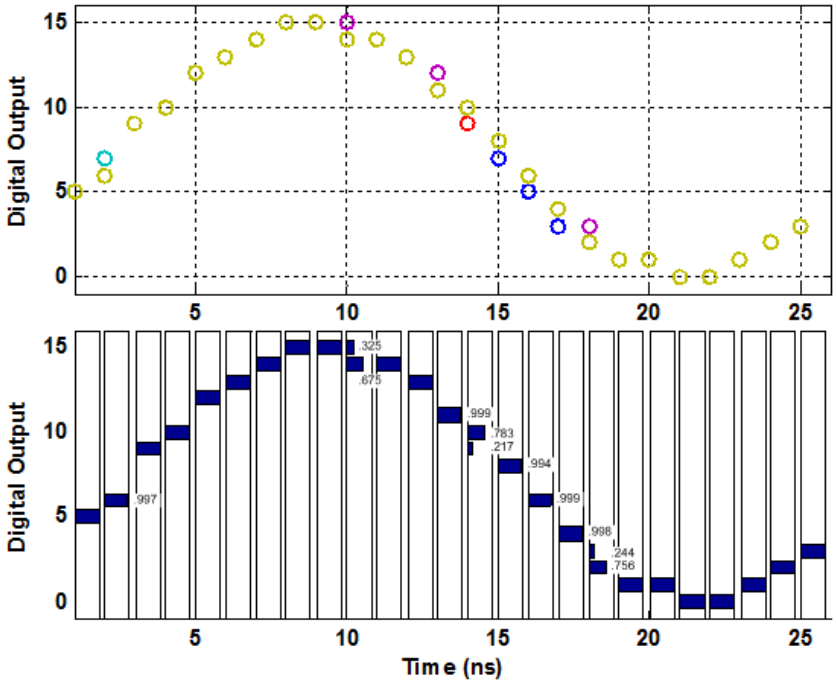


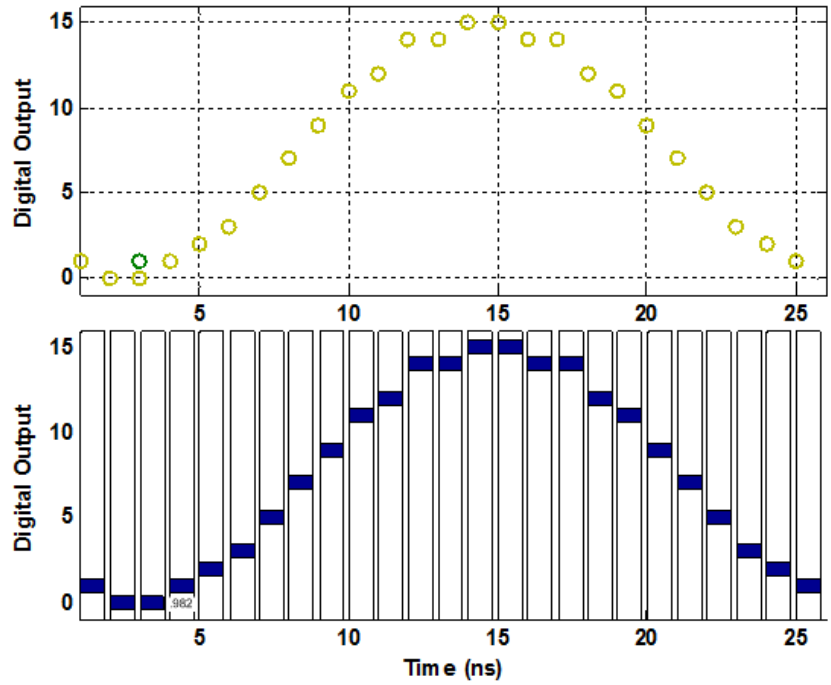

Figure 3.8: Measured waveforms of the first four bits without (left) and with (right) the metastability detection.

remaining quantizer offset to 2mV, heavy metastability is exhibited. On the other hand, if the metastability detector is turned ON, any input signal whose absolute value is smaller than about 5mV will force a preset output “1000”, and from the zoomed-in view, it can be seen that little metastability is manifested.

It is difficult to quantify the improvement in ENOB performance with the above metastability detector, because a FFT measurement acts like an averaging calculation, and the possibility of metastability is low. To better demonstrate the improvement of the proposed technique, a synchronous repetitive measurement using a histogram was performed (Figure 3.9). In this measurement, the sampling clock frequency was set to be 1GS/s, and the frequency of the input sine wave set to 40MHz. The clock and the input signal were synchronized such that for every period of the sampled signal, 25 fixed voltage levels were converted into 4-bit digital outputs. The input signal was quantized, with all the digital outputs utilized to reconstruct the original input, where the reconstructed waveform was folded into one single period, similar to eye diagram. Therefore, after each of the 25 fixed voltages within one period was converted 1000 times, a histogram analysis was performed to obtain the probability and distribution for each point. As can be observed in Figure 3.9(a), when the metastability detection was disabled, 1 LSB deviation occurred frequently at 8 of the total 25 voltage levels (three levels are easily discernible). While in Figure 3.9(b), when the detection was enabled, only 1 of the 25 voltage levels shows that a 1 LSB deviation occurred, and its probability was rare.




(a)



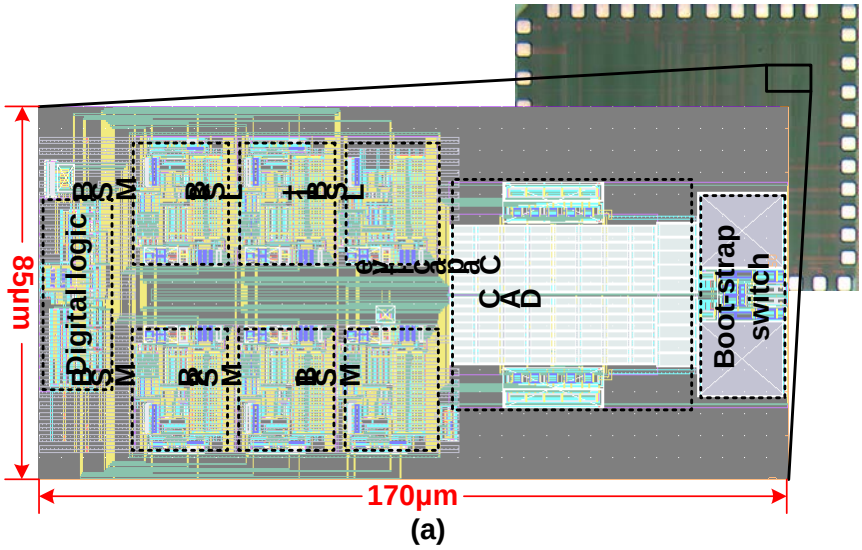

(b)

Figure 3.9: Reconstructed sine wave of 40MHz sampled at 1GS/s with the metastability detector is (a) OFF and (b) ON.

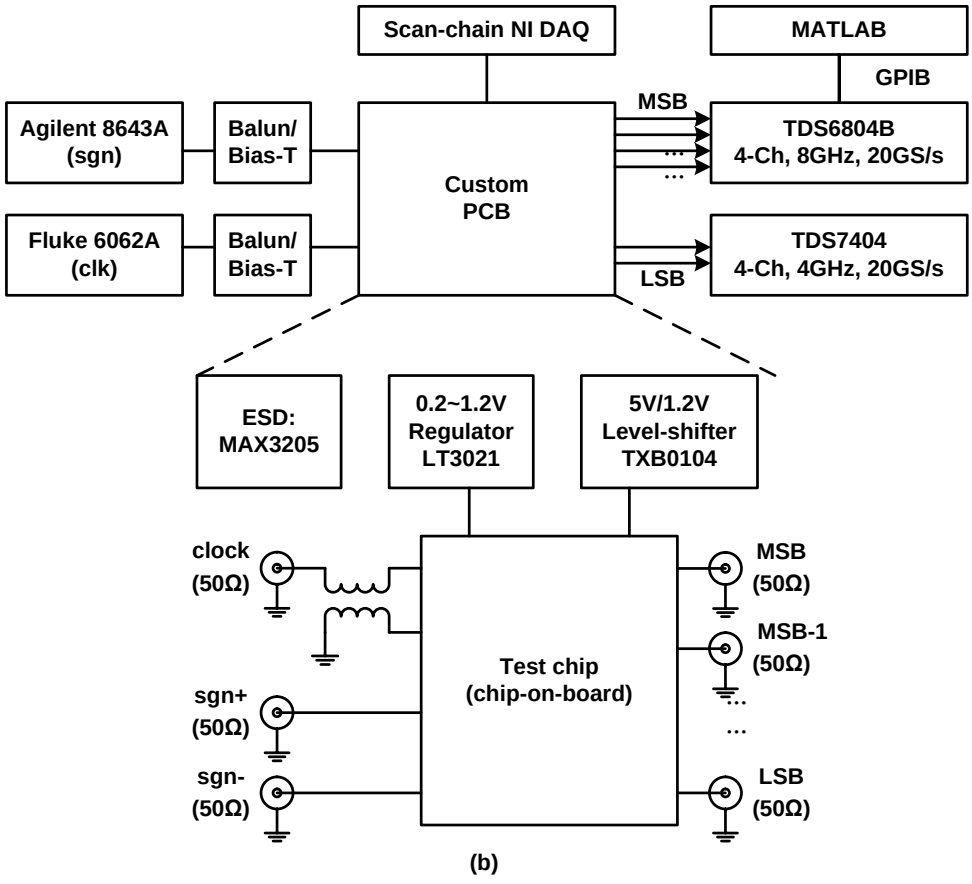
## 3.4. Measurement Results

The SA ADC is fabricated in a 1V, 40nm CMOS process, with the die photo and measurement setup shown in Figure 3.10. The active area is only 170μm by 85μm, with a total die size of 1.8mm by 1.5mm. Since the chip is operating at a multi-gigahertz frequency, its outputs are collected using two synchronized real-time oscilloscopes through open-drain buffers, with all six outputs read into a computer and processed by MATLAB.

The measurements are performed with different supply voltages and across varying sampling rates in order to explore the chip's maximum performance. Least mean square (LMS) offline calibration [2] is first performed by injecting a slow ramp signal into the converter, using the output code to determine the bit weights that best correspond to the known input. Because all six comparators connect to the output of the capacitive DAC, the large input gate capacitances all contribute as undesired parasitics and capacitive kick-back, increasing the distortion and non-linearity of this ADC versus a conventional structure. LMS calibration improves the performance considerably, as can be observed in Figure 3.11, where the SNDR is improved by 2.7dB at a sampling rate of 1GS/s. The improvement is not as large as observed in simulation, due to the previously mentioned common-mode voltage drift that affects the comparator offset. For the same reason, the ADC cannot achieve the $6^{th}$ bit consistently through the entire input range. The DNL and INL for the first 5-bits of the ADC are shown in Figure 3.12, with the $6^{th}$ bit acting as redundancy. ADC output




(a)




(b)

Figure 3.10: (a) Chip die photo and core circuit layout; (b) the measurement setup.

spectra with near-DC and near-Nyquist input frequencies at a rate of 1GS/s are shown in Figure 3.13.

The SA-ADC operates at 1GS/s with a 1V supply, consuming 1.25mW, 2.76mW and 1.15mW, distributed between the analog comparators, digital logic and internal

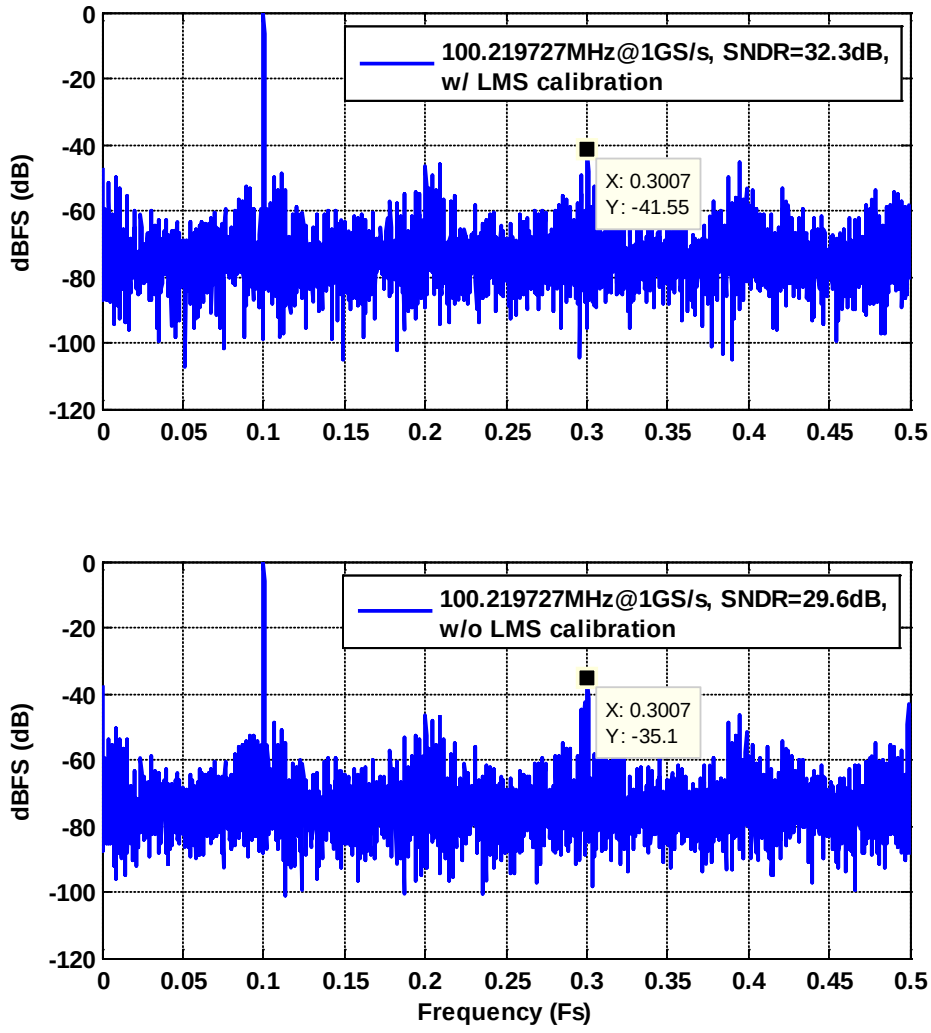



Figure 3.11: ADC output spectra with and without LMS calibration.

clock driver, and the capacitive DAC, respectively. The ADC output spectra for different input frequencies are shown in Figure 3.14, indicating a peak SNDR of 32.9dB around DC and 27.3dB around the Nyquist frequency, resulting in an overall FoM of 148fJ/conversion-step and 278fJ/conversion-step. When the sampling rate is increased to 1.25GS/s, the peak SNDR is 30.5dB around DC and 26.8dB around the Nyquist frequency, with a total power consumption of 6.08mW, resulting in an overall FoM of 178fJ/conversion-step and 272fJ/conversion-step. Another reason for the SNDR loss from DC to Nyquist is due to imperfection in the clock generator used within each conversion, resulting in increased sensitivity to supply noise and poor jitter performance. While capacitive parasitics contribute to the SNDR losses at low frequency, the ability to reduce to 5b conversion enables operation well above 1.5GHz at Vdd=1.1V.

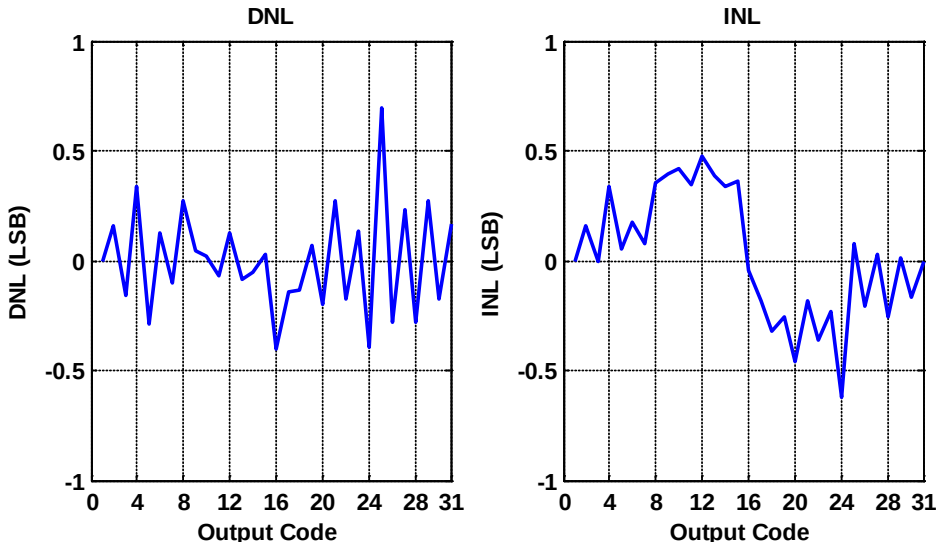



Figure 3.12: DNL and INL performance after LMS calibration (5 bit).

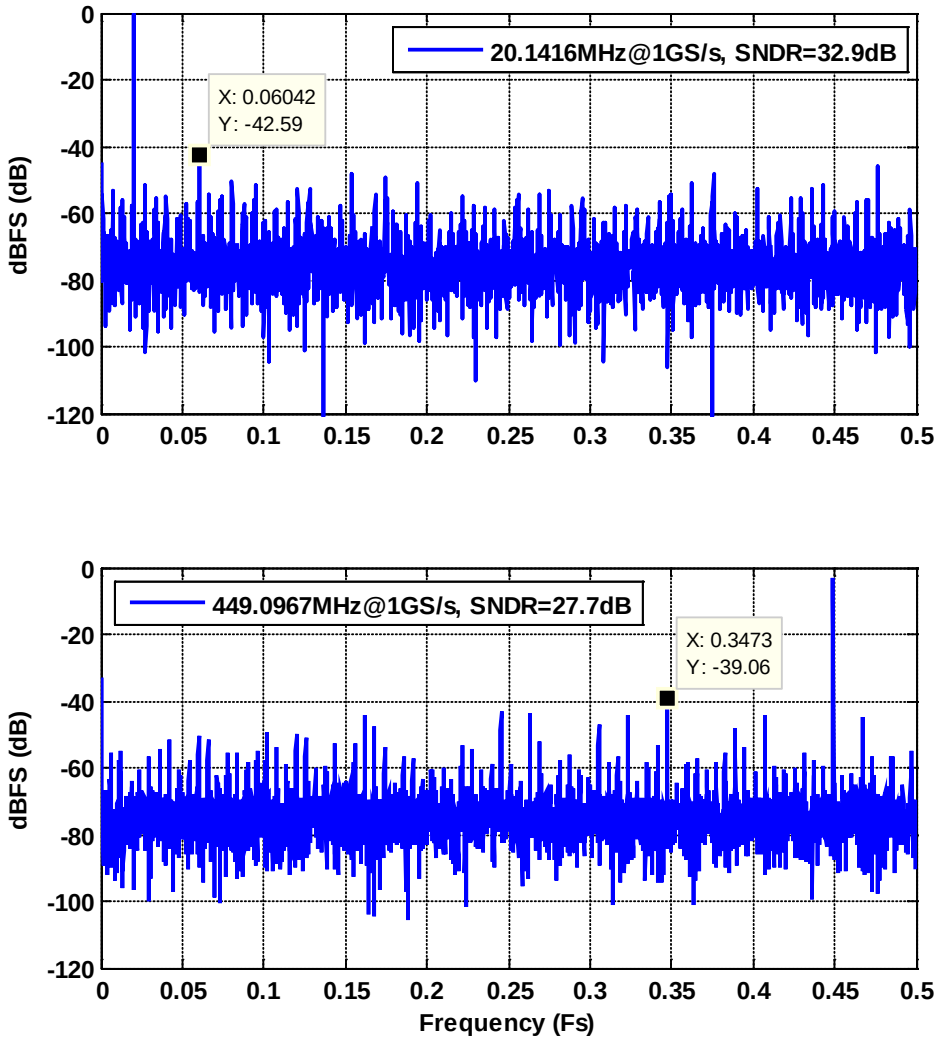



Figure 3.13: ADC output spectra for different input frequencies with 1GS/s rate.

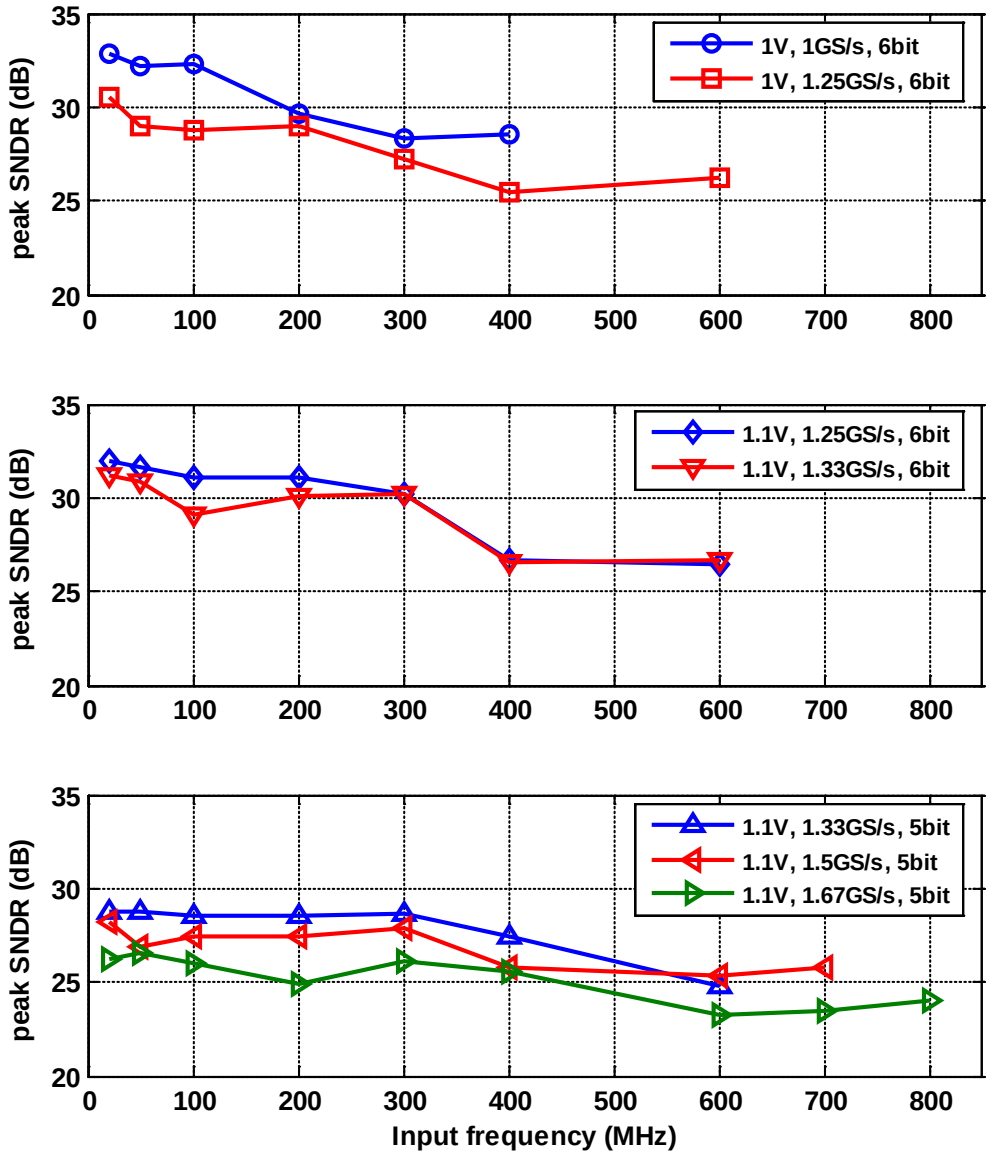



Figure 3.14: Measured SNDR versus input frequency for ADC under different supplies, sampling rate, and number of bits.

## 3.5. Summary

A novel SAR architecture with improved feedback delay is proposed. With the comparator outputs directly fed back to the capacitive DAC, the digital FSM logic delay is eliminated, thereby greatly increasing the sample rate. Fabricated in a 40nm CMOS process, the ADC achieves a sampling rate over 1.25GS/s for a single channel. Measurement results are summarized in Table 3.1, along with a performance comparison versus recent >1GS/s SA-ADC designs.

Table 3.1: Comparison with Previous Works

| | [2] | [30] | [43] | [34] | This work | | | |
|---|---|---|---|---|---|---|---|---|
| Technology (nm) | 130 | 130 | 65 | 65 | 40 | | | |
| Area ($mm^2$) | 0.12 | 0.09 | 0.018 | 0.11 | 0.014 | | | |
| Resolution (bit) | 6 | 6 | 5 | 6 | 5 or 6 Programmable | | | |
| Channel No. | 2 | 2 | 1 | 2 | 1 | | | |
| Sample rate (GS/s) | 0.6 | 1.25 | 0.8 | 1 | 1 | 1.25 | 1.25 | 1.33 |
| Peak SNDR (dB) | 34 | 34.9 | 28.2 | 31.5 | 32.9 | 30.5 | 31.8 | 31.3 |
| FoM (fJ/conv) | 220 | - | 116 | 210 | 148 | 178 | 183 | 188 |
| Supply (V) | 1.2 | 1.2 | 1 | - | 1 | 1 | 1.1 | 1.1 |
| | | | | | Extra 1.2V for bootstrapped switch | | | |
| Power (mW) | 5.3 | 32 | 1.97 | 6.7 | 5.28 | 6.08 | 7.26 | 7.52 |

# 4. A Time-Interleaved ADC with Distributed Track-and-Hold Circuits Synchronized by a Global Sine-Wave Clock

A 12-GS/s 5-b <50-mW ADC is designed for the application of high speed (12GHz) serial link to convert the analog signal at the receiver side for DFE in the digital domain. High speed and low power are two important performances in this design. The target specifications are listed in Table 4.1.

Table 4.1: Target specifications

| | |
|---|---|
| Resolution | 5-bits |
| Sampling rate | 12-GS/s |
| Input range | 1.0-Vpp differential |
| Supply voltage | 1V |
| Power consumption | < 50mW<br>including clock distribution and CML buffer |
| Process | TSMC 40nm CMOS |

## 4.1. Proposed Architecture

As is discussed in Section 2.1, previous ADCs running around 10GS/s usually employed a distributed time-interleaved architecture with small channel number, and utilized the Flash structure as the sub-ADC to achieve the high sampling rate. This is a smart choice, but certain improvement still can be made in two aspects. Firstly, the timing skew in the multi-phase clocks for the distributed T/H circuits can be treated in a cleverer fashion with less resource spending. Secondly, as technology scales, it is

possible for certain structures with better power efficiency to achieve the high speed specification required for the sub-ADC. The proposed design will try to provide solutions for the above two questions.

Although the distributed time-interleaved T/H is usually preferred for the multi-GS/s ADC applications, yet the advantage of the global time-interleaved T/H is impressive that it does not require phase calibration at all for the multi-phase clock. Fancy is if there is a structure that can combine the advantages of both, that employs less complicated calibration for the multi-phase clock while avoiding using the power-hungry global T/H buffer.

A global passive sampling technique [54] for the time-interleaved ADC based on bottom-plate sampling was firstly experimented. As is illustrated in Figure 4.1, the proposed sampling circuit is controlled by a global clock phase $\Phi$ which defines the sampling instant. Theoretically, when the global clock phase $\Phi$ and the individual clock phase $\Phi_i$ are both high, the input signal is tracked by the $i$-th sub-ADC. When

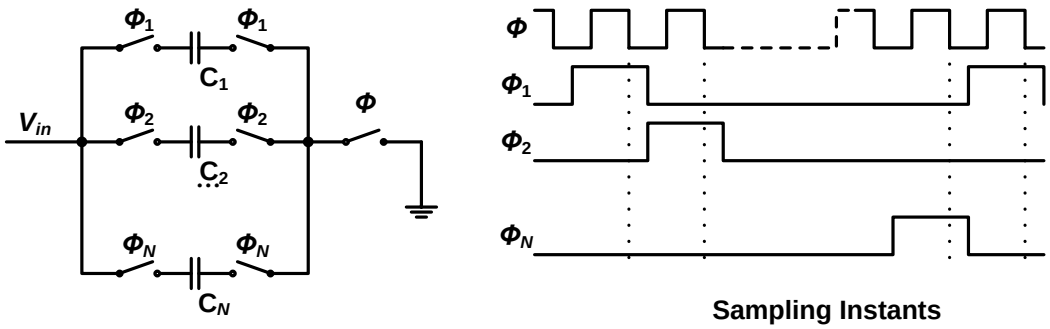



Figure 4.1: Global passive sampling based on bottom-plate sampling.

the global clock phase $\Phi$ goes low, the analog value is sampled onto the sampling capacitor because the bottom plate of the capacitor is floating. The individual clock phase $\Phi_i$ always goes low after the global clock phase. Therefore, even if there are large phase skews between successive clock phases $\Phi_i$, they do not significantly affect the sampling instants. However, such technique is proven by simulation not suitable for high-speed sampling circuits due to the following reasons. First, the three MOS switches in series for each sub-channel will cause larger on-resistance, leading to poorer *RC* constant than the conventional one-switch topology. Second, as already stated in [54], the parasitic capacitance of the MOS switches will degrade the ultimate effect of such global sampling. What is worse, in order to meet the high demand for channel bandwidth, the MOS switch sizes need to be made quite large to achieve small enough on-resistance, which will result in substantial parasitic capacitance.

Although the global bottom-plate sampling technique is not practical for high-speed time-interleaved T/H, the idea to employ a global clock phase to determine the sampling instant for each individual channel and reduce phase skew influence is still of great importance. Based on such idea, an 8-channel time-interleaved ADC is proposed to achieve the targeted 12GS/s sampling rate, with a global sine-wave clock applied to each individual T/H switch to synchronize the sampling instants. As shown in Figure 4.2, each switch is not only controlled by one of the multi-phase clocks $ck[i]$, but also synchronized by the highest-frequency ($f_s$) sine-wave clock. Because $ck[i]$ only determines the instant that each T/H channel starts the tracking phase, sub-

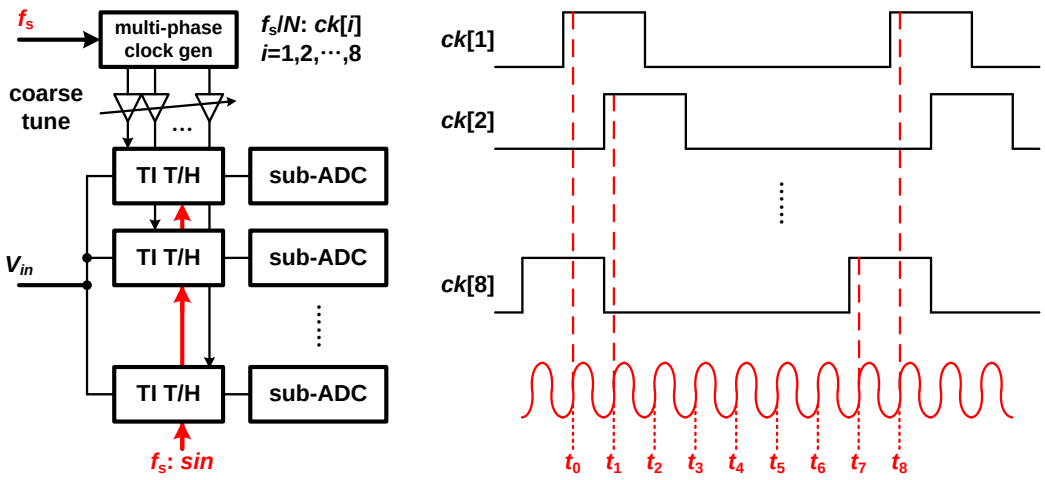



Figure 4.2: Proposed time-interleaved T/H with a global sine-wave clock.

channel phase accuracy requirement is significantly relaxed as long as the tracking duration is sufficient. The sampling instant when the input signal is held onto the loading capacitors $C_L[i]$ is defined by the global clock *sin*, such that there is minimal static phase error between each individual T/H channel. Finally, the *sin* signal is directly generated from a clean sinusoidal source through a CML buffer, therefore has better dynamic jitter merit because the supply-induced jitter is reduced. The duty cycle of each individual clock is 1/4 so that at any time only two channels of the eight are connected to the front-end in order to reduce the capacitive loading.

## 4.2. Track-and-Hold Circuit

To implement the function described above, a bootstrapped switch modified from [51] is designed (Figure 4.3), where the discharge path connects the gate of the pass

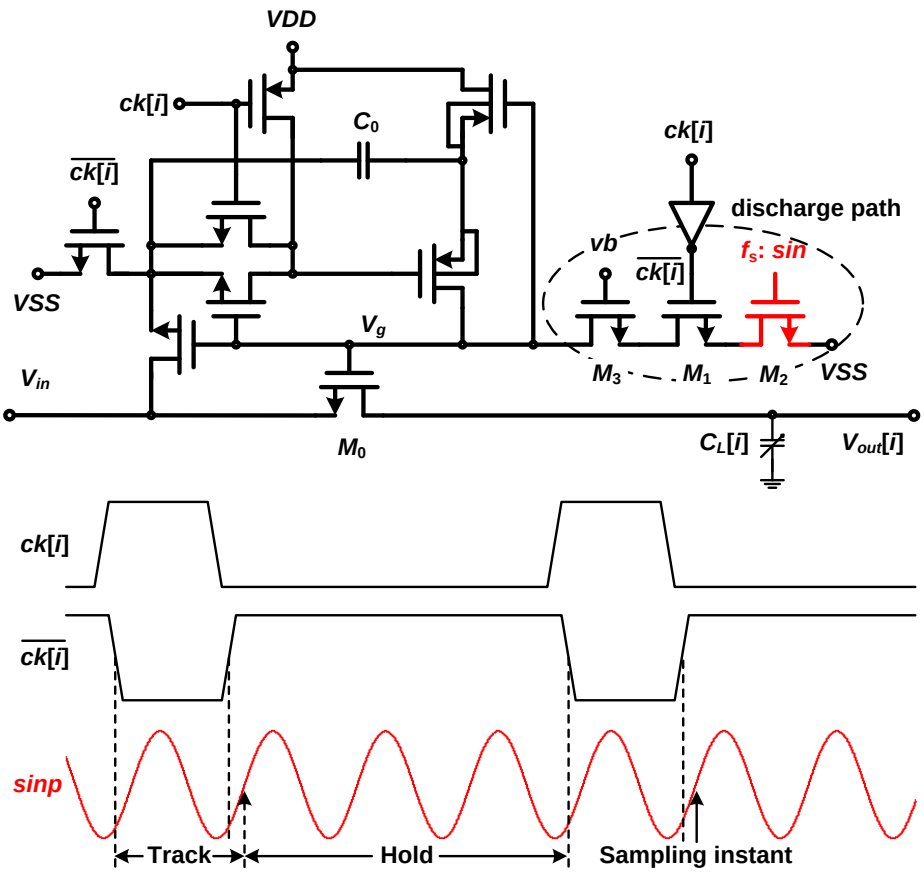



Figure 4.3: Modified bootstrapped switch enabling global clock synchronization.

transistor $M_0$ to ground in order to turn it OFF. During the tracking phase when $ck[i]$ is high, the bootstrapped switch operates normally, with the gate-source voltage of $M_0$ equal to the constant voltage difference previously stored across the capacitor $C_0$. However, by connecting the NMOS $M_1$ which is gated by the complement of $ck[i]$ and the NMOS $M_2$ which is gated by the global clock *sin* in series, the gate of $M_0$ will be shorted to ground only after both the complementary $ck[i]$ and the global *sin* reach the threshold to turn ON $M_1$ and $M_2$ respectively. As illustrated in Figure 4.3, if the

moment when *sin* turns ON $M_2$ takes place later than that the complementary *ck*[*i*] turns ON $M_1$, then the sampling instant is defined by the global signal *sin* instead of the multi-phase clock *ck*[*i*]. The effect is that the sampling instants of all T/H channels are evenly spaced, regardless of static timing errors between the multi-phase clocks. Besides, since the source of $M_2$ is at ground, signal-dependent sampling distortion is also avoided.

In this design, instead of using a single phase of a sine wave clock with frequency of $f_s$ (as denoted in Figure 4.2 and Figure 4.3), differential phases of a sine wave clock with frequency of $f_s/2$ is employed for the odd and the even number channels respectively. The benefit is the frequency requirement for the global clock is relaxed, while the penalty is that the differential clock path needs to be made as symmetric as possible. To compensate for any possible *RC* mismatches between the delay paths of different sub-channels, a third NMOS $M_3$ is added, whose gate voltage can be digitally programmed by an on-chip 8-b DAC.

## 4.3. Multi-Phase Clock Generation and Distribution

In this design, the half-frequency differential sine-wave clock needed for the global synchronization is generated by injecting a single-ended 6-GHz external clock onto an on-chip CML buffer. The CML buffer employs thick-gate devices and works under 1.8V supply, so that its output sine-wave signal is near rail-to-rail for the 1V operation of other blocks in the clock portion.

The 8-phase 1.5GHz clock generator is designed using a flip-flop loop. The duty cycle of the output phase is 1/4, which means about 160ps is allocated for the track phase while about 480ps is for the hold phase and signal conversion. TSPC (true single phase clock) structure is used for the flip-flop circuit to ensure fast enough speed. The phase of each output clock can be tuned roughly by a delay line. The whole clock generation and distribution circuits are shown in Figure 4.4.

The external 6GHz signal is generated from a 12GS/s AWG (arbitrary waveform generator), whose jitter performance is shown in Figure 4.5. The RMS clock jitter is around 800fs, which can be used for estimation for the global sine-wave clock.

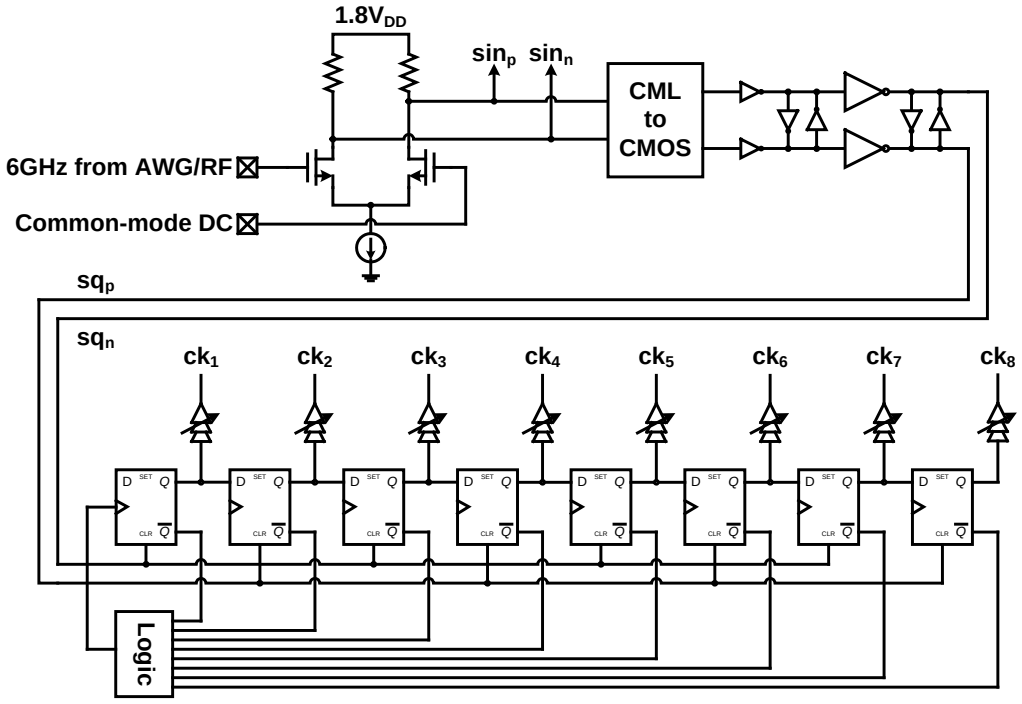



Figure 4.4: CML clock buffer and multi-phase clock generation.

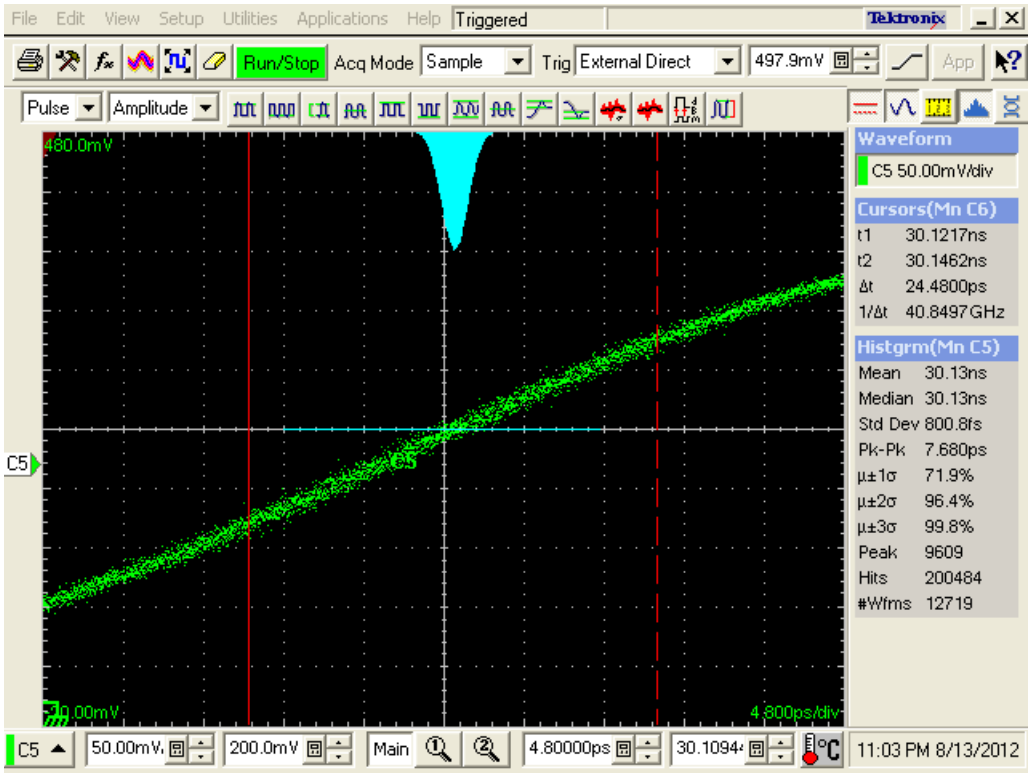



Figure 4.5: Measured dynamic jitter performance of the injected global clock.

## 4.4. Sub-Channel ADC Design

To meet the specification, each sub-ADC needs to achieve a sampling rate of 1.5GS/s, which is faster than the work presented in [49]. Therefore, it is necessary to modify the sub-ADC designed before to further improve its speed.

### 4.4.1. Flash-SA Hybrid Structure

To expedite the conversion speed of the sub-ADC, a hybrid structure with a 2-bit Flash and 3-bit asynchronous SA is employed (as shown in Figure 4.6). The 2-bit Flash converts the first two bits simultaneously, requiring only one more comparator

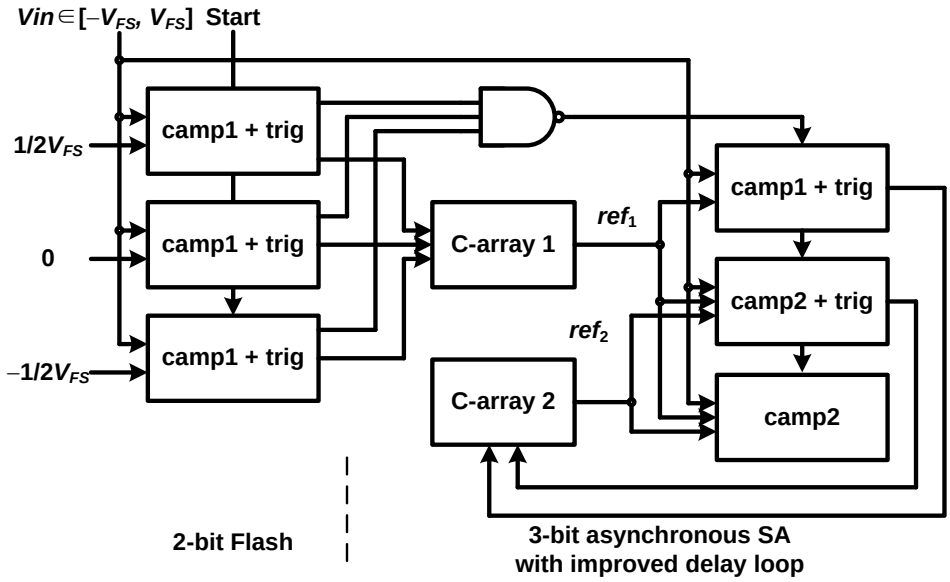
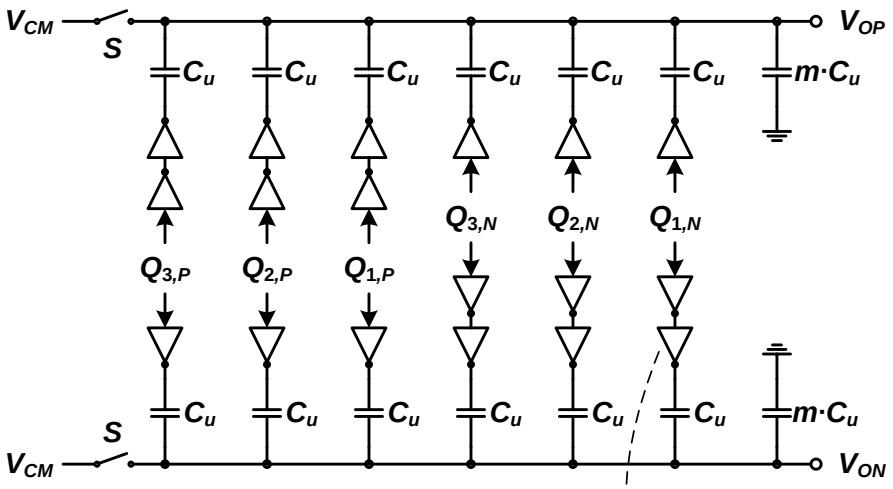



Figure 4.6: The Flash-SA hybrid structure of the sub-ADC.

than a conventional 2-bit SA. These three comparators compare the differential input signal with the reference levels of -1/2$V_{FS}$, 0 and 1/2$V_{FS}$, where $V_{FS}$ is the maximum absolute value of the differential input signal. Their outputs are fed into a capacitive network (C-array 1) to generate a reference voltage $ref_1$, whose possible values are ±1/4$V_{FS}$ and ±3/4$V_{FS}$ for the subsequent SA conversion. The 3-bit asynchronous SA, using the same architecture as in [49], is triggered upon the completion of the 2-bit Flash. The 3 comparators in the SA compare the input signal with the sum of $ref_1$ and $ref_2$ successively, in which $ref_2$ is generated by a binary SA capacitive DAC (C-array 2). Because the SA converts the signal starting from the 3$^{rd}$ bit, the total capacitor size and power consumption of C-array 2 are all reduced by 4 times.

### 4.4.2. Capacitive networks

Two capacitive networks are used to provide the reference voltage $ref_1$ and $ref_2$ as mentioned in Section 4.4.1. Based on the thermal code converted by the 2-bit Flash ADC, C-array 1 shown in Figure 4.7 provides a fixed differential voltage of $\pm 1/4V_{FS}$ and $\pm 3/4V_{FS}$ for the SA conversion. At first the top plates of the capacitors $V_{OP}$ and $V_{ON}$ are shorted to the common-mode voltage $V_{CM}$, and the bottom plates are to the supply voltage $V_{DD}$ or ground through the inverters respectively. Note at this moment all the $Q_{i,P}$ and $Q_{i,N}$ (i=1,2,3) are shorted to ground because the three comparators in the 2-bit Flash have not evaluated yet. Later the switches $S$ are open, while the




| $Q_{3,P}$ | $Q_{2,P}$ | $Q_{1,P}$ | $Q_{3,N}$ | $Q_{2,N}$ | $Q_{1,N}$ | $V_{OP}-V_{ON}$ | |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 0 | 0 | $\frac{3}{4}V_{FS}$ | |
| 0 | 1 | 1 | 1 | 0 | 0 | $\frac{1}{4}V_{FS}$ | |
| 0 | 0 | 1 | 1 | 1 | 0 | $-\frac{1}{4}V_{FS}$ | $V_{DD} = n \cdot V_{FS}$ |
| 0 | 0 | 0 | 1 | 1 | 1 | $-\frac{3}{4}V_{FS}$ | $m = n \cdot 8 - 6$ |

Figure 4.7: Schematic of the capacitive network C-array 1.

potential $V_{OP}$ and $V_{ON}$ will shift accordingly based on the comparison results $Q_{i,P}$ and $Q_{i,N}$ (i=1,2,3) .

The second capacitive network shown in Figure 4.8 is a normal 2-bit binary DAC with 1/4 smaller total capacitor size compared to that for a normal 5-bit SA ADC. Learning a lesson from the previous design which has common-mode voltage drifting problem due to the asymmetric DAC topology, the new capacitive DAC is modified that the differential outputs will shift in the opposite direction so that its output common-mode voltage does not change much. The reference voltage for such DAC is calculated to be $1/8V_{FS}$.

### 4.4.3. Comparator Design

A dynamic double-tail latch-type comparator [55] is shown in Figure 4.9, with only one phase clock used. As illustrated in Figure 4.6, two different topologies are used. The one used for the 2-bit Flash and the MSB of the 3-bit SA (camp1) has two input

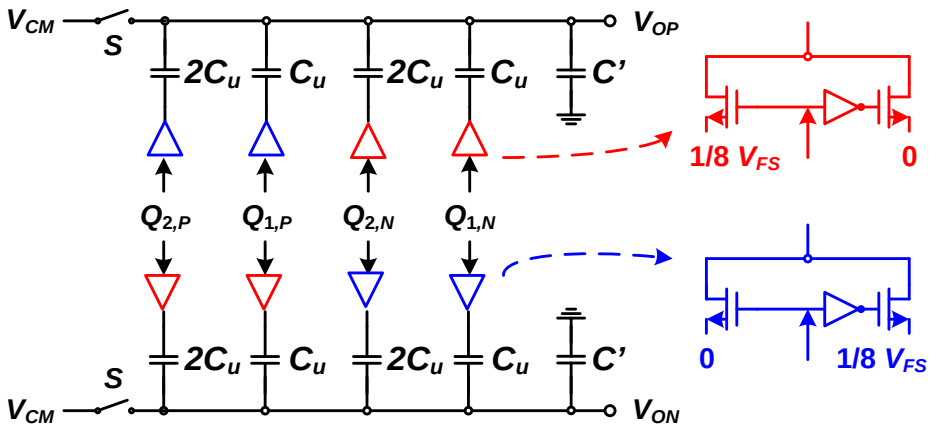



Figure 4.8: Schematic of the capacitive DAC C-array 2.

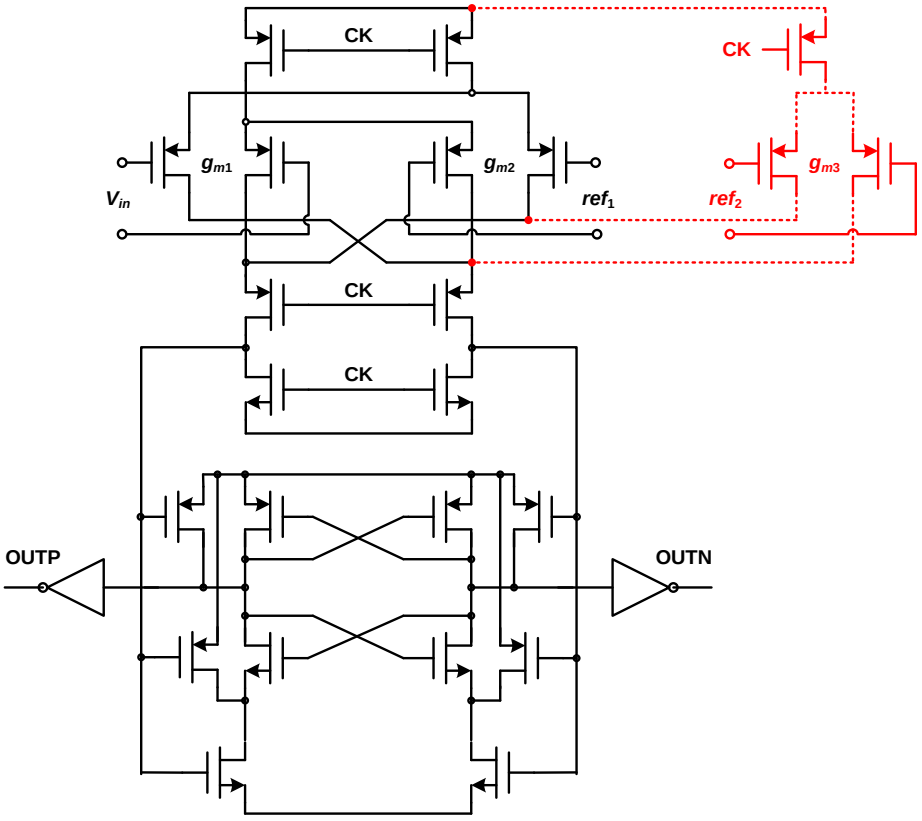



Figure 4.9: Schematic of the designed comparator.

pairs, comparing the differential signal with one reference voltage. The other used for the rest bits of the SA (camp2) has three input pairs, comparing the signal with the sum of two reference voltages $ref_1$ and $ref_2$. One issue for camp2 need to be attended, however, as will be discussed as below.

As shown in Figure 2.4(b) and according to [31][32], the comparison of input voltages actually occurs in phase 1, during which the differential outputs discharge from the supply voltage at different currents estimated the products of the voltages applied onto the input devices and the transconductances of the devices. Once one of

the outputs reaches the potential that is one PMOS threshold below the supply voltage, the irreversible regeneration phase takes place. Therefore, to correctly compare the voltages applied onto the gates of the input devices, it is necessary to make sure the transconductances of the input devices are the same.

Unfortunately, the large-signal transconductance $G_m$ of the input devices in the CML-type first stage of the comparator varies significantly with the differential input, as shown in Figure 4.10 [56][57]. Considering the operation of the SA, it can be found that while the voltages $V_{in}$ and $ref_1$ can span the whole range, the voltage $ref_2$ is always in the zone Z1 with the largest transconductance. Therefore, if $V_{in}$ and $ref_1$ are in the zones of Z2, Z3 or Z4, the induced currents by the input devices cannot reflect the real relation between $V_{in}$ and the sum of $ref_1$ and $ref_2$. To compensate for this variation, in each different zone, the value of $C'$ (as in Figure 4.8) is calibrated so that the value of $ref_2$ is decreased accordingly.

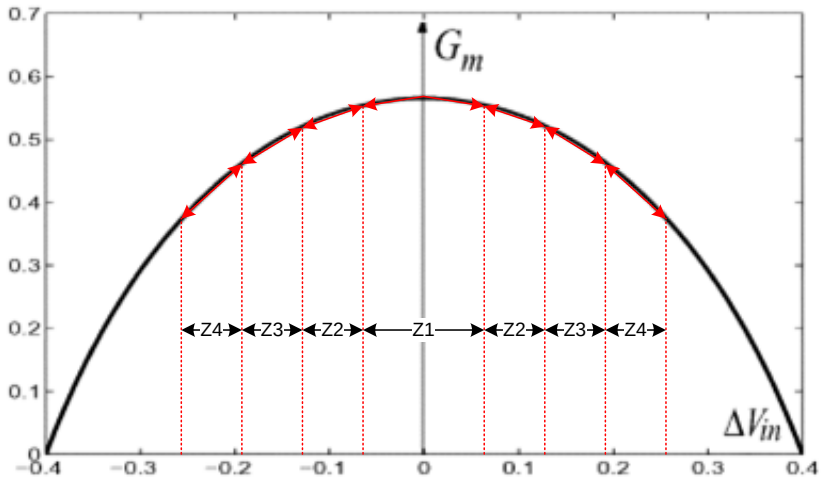



Figure 4.10: Large-signal $G_m$ as a function of the differential input.

## 4.5. Measurement Results

The measurement setup is similar to that used for the single-channel ADC testing. MATLAB script is used to collect the output waveform data from two synchronized oscilloscope Tektronix 8GHz 20GS/s TDS6804B and 4GHz 20GS/s TDS7404, via GPIB. The clock signal is provided by the Tektronix 12GS/s arbitrary waveform generator AWG7122B, and the input signal is by the HP/Agilent 0.1~4.2GHz RF signal generator 8665A. The precise DC voltage for offset calibration is provided by the Agilent precision system power supply 6629A, and the control bits (total 928 bits) for on-chip scan chain are injected by the NI DAQ USB-6051.

Foreground offset calibration is firstly performed for all the 6 comparators of sub-ADC in each of the 8 channels. The capacitance *C'* in the capacitive DAC C-array 2 to compensate for transconductance variation as mentioned in Section 4.4.3 is also calibrated. Unfortunately, in the measurement it is found that two mistakes were made during the designing, leading to some imperfection. First, the calibration range of *C'* is set smaller than enough, therefore when the differential input voltage is large, the calibration effect is not good enough. Second, because of the variation in $G_m$ with differential input voltage, the offset also varies. Therefore, the offset of the three-input comparator (camp2) cannot be well calibrated.

After the DC calibration, dynamic calibration is also tuned by injecting a sine-wave signal and roughly changing the phase delay of each individual channel to maximize the measured sub-ADC SNDR. It is found that within a considerably large range of

the phase delay, the SNDR of each sub-ADC will not change much, which is well as expected for the proposed global synchronization technique.

The output spectra of one sub-ADC running at 1.5GS/s with input frequencies near DC and at around 3.5GHz are shown in Figure 4.11.

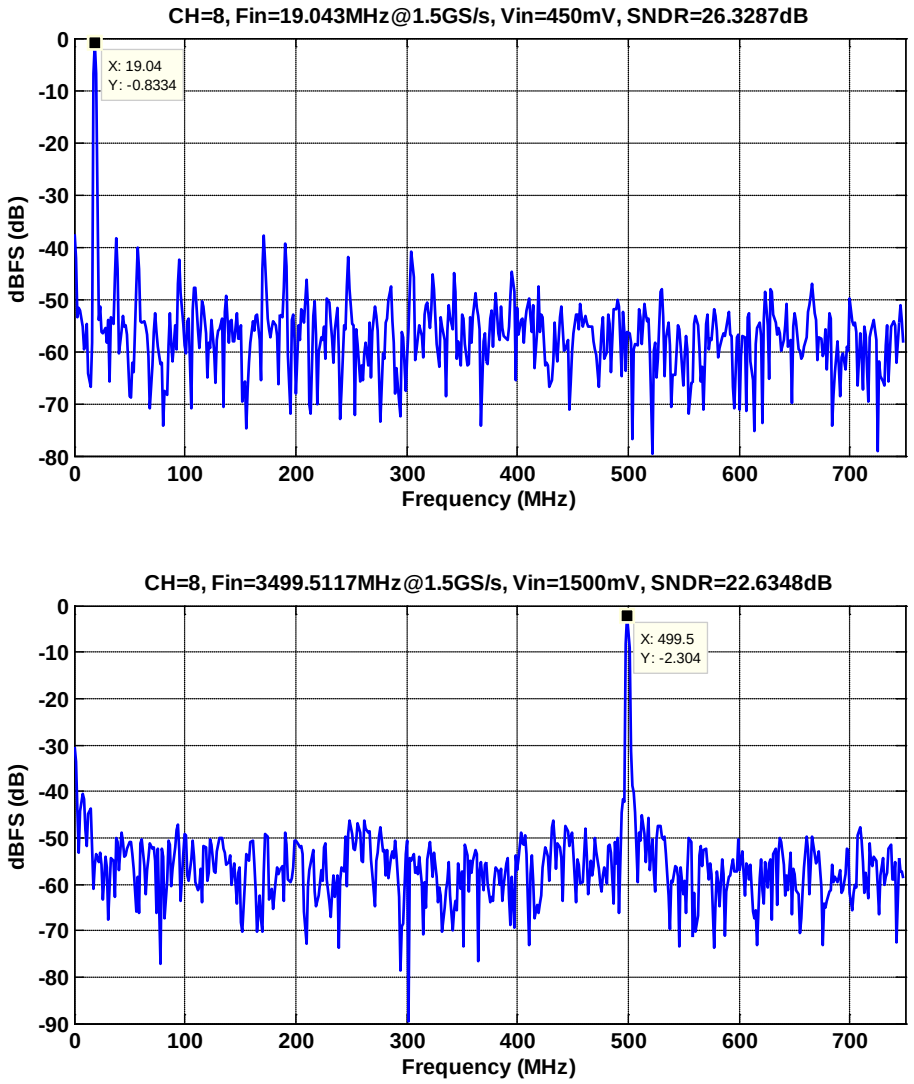



Figure 4.11: Output spectra of sub-ADC (CH=8) running at 1.5GS/s with input signal frequency of 19MHz and 3.5GHz. .

The SNDR of each sub-ADC running at 1GS/s and 1.5GS/s with different input frequencies are plotted in Figure 4.12. As can be seen, starting from input frequency around 3GHz, the SNDR performance for sub-ADC is already degrading.

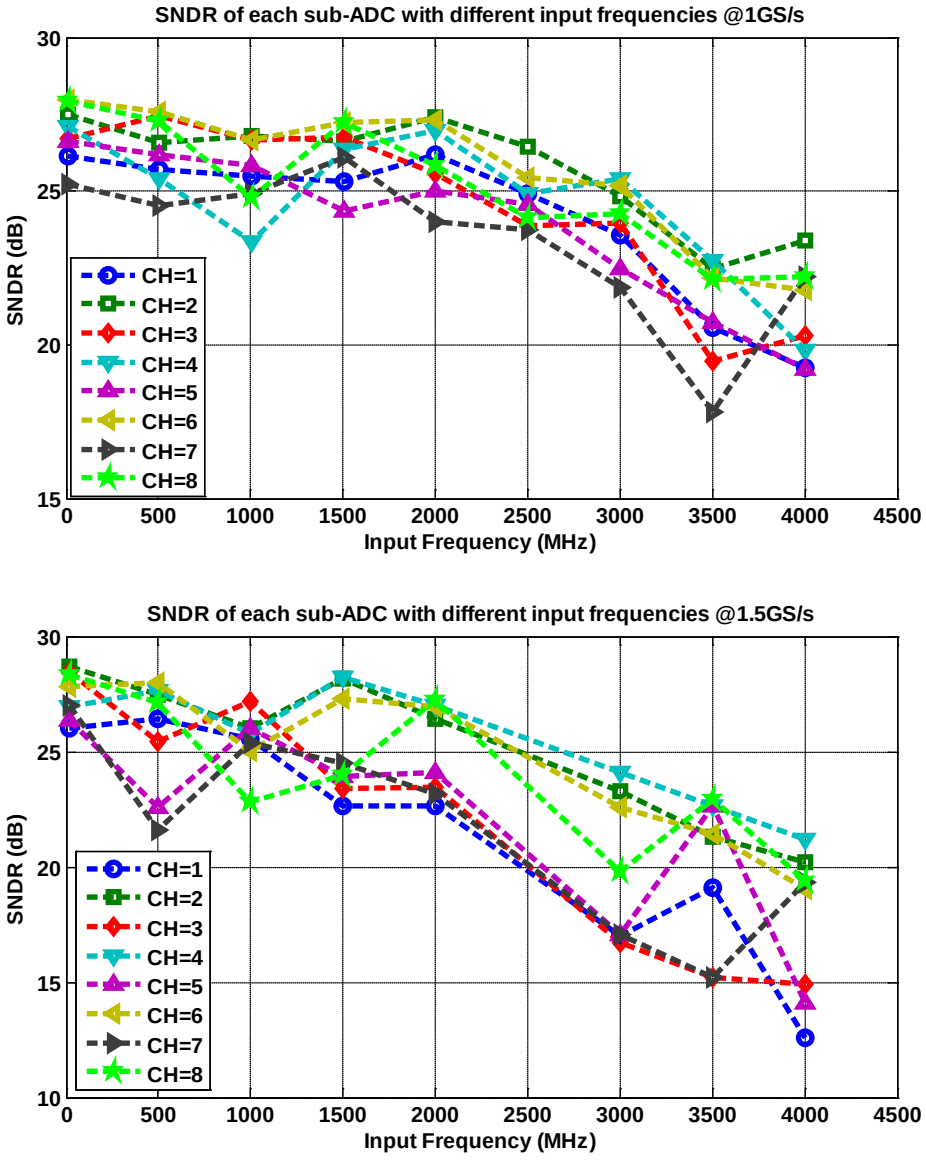



Figure 4.12: SNDR of sub-ADC running at 1GS/s and 1.5GS/s with different input frequencies.

The output spectra of the time-interleaved ADC running at 12GS/s with input frequencies near DC and at around 2GHz are shown in Figure 4.13. The output waveforms of each sub-ADC are separately collected, digitized and then combined in

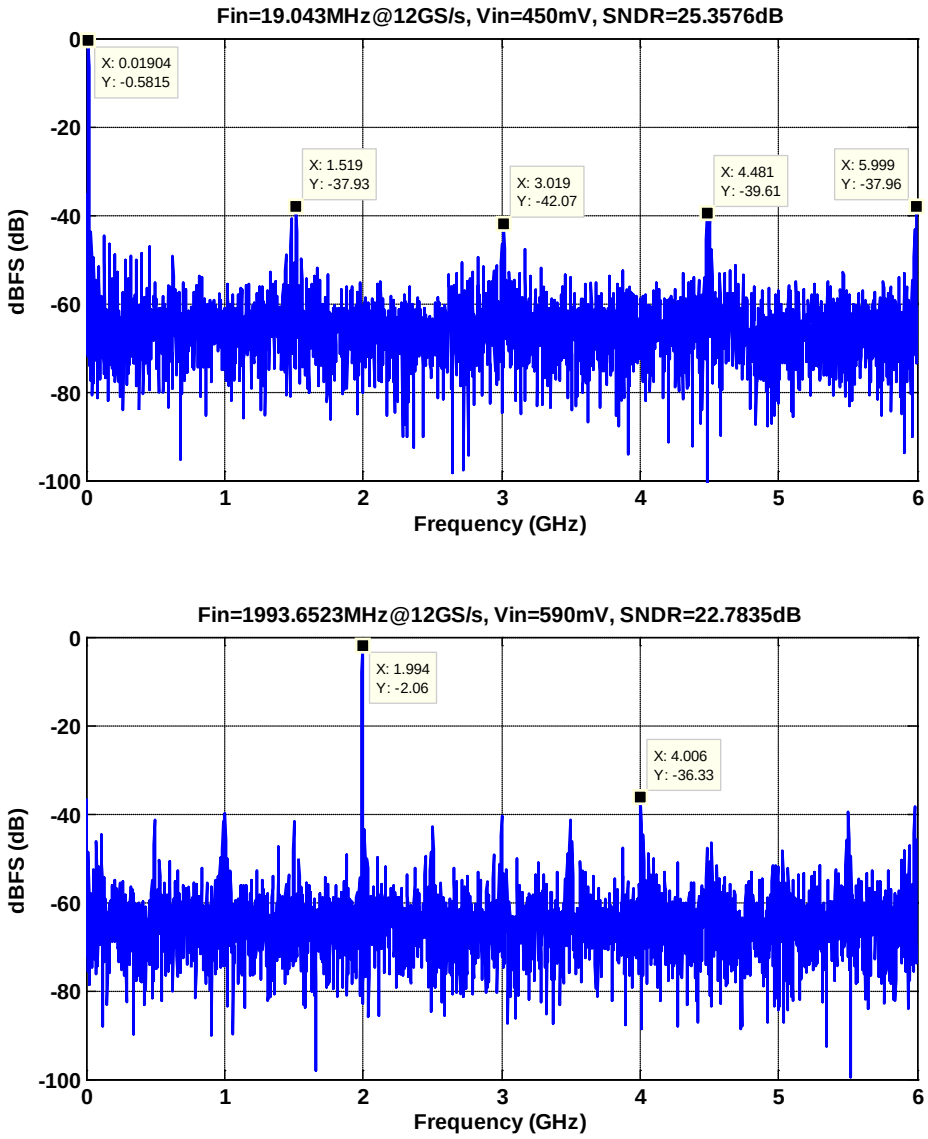



Figure 4.13: Output spectra of the time-interleaved ADC running at 12GS/s with input signal frequency of 19MHz and 2GHz.

a time-interleaved manner, to reconstruct the final output as sampled at 12GS/s. To ensure the synchronization of each sub-ADC digital output, a clock signal with frequency of 12GHz/8192, in which 8192 is the number of FFT points, is used to trigger the two oscilloscopes. The digital outputs of each sub-ADC can be calibrated on offset and gain mismatch in the digital domain. The SNDR of the time-interleaved ADC running at 8GS/s, 10GS/s and 12GS/s with different input frequencies are plotted in Figure 4.14. When the input signal frequency is near DC, its SNDR can reach 26dB. However, as the input frequency increases, the dynamic performance decreases fast, probably due to the degradation of the input signal because of the signal path reflection and distortion.

The test chip die photo is shown in Figure 4.15, and the ADC performance is

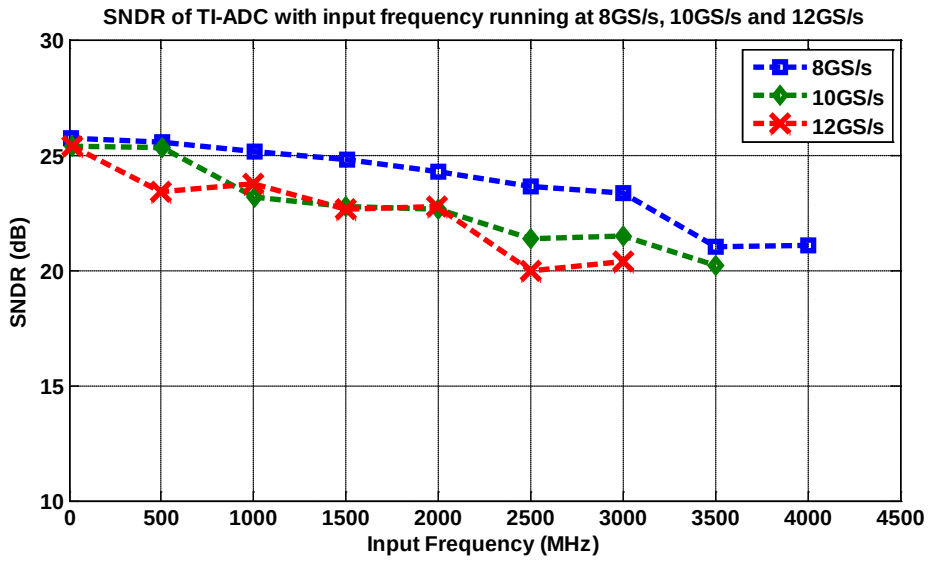



Figure 4.14: SNDR of time-interleaved ADC running at 8GS/s, 10GS/s and 12GS/s with different input frequencies.

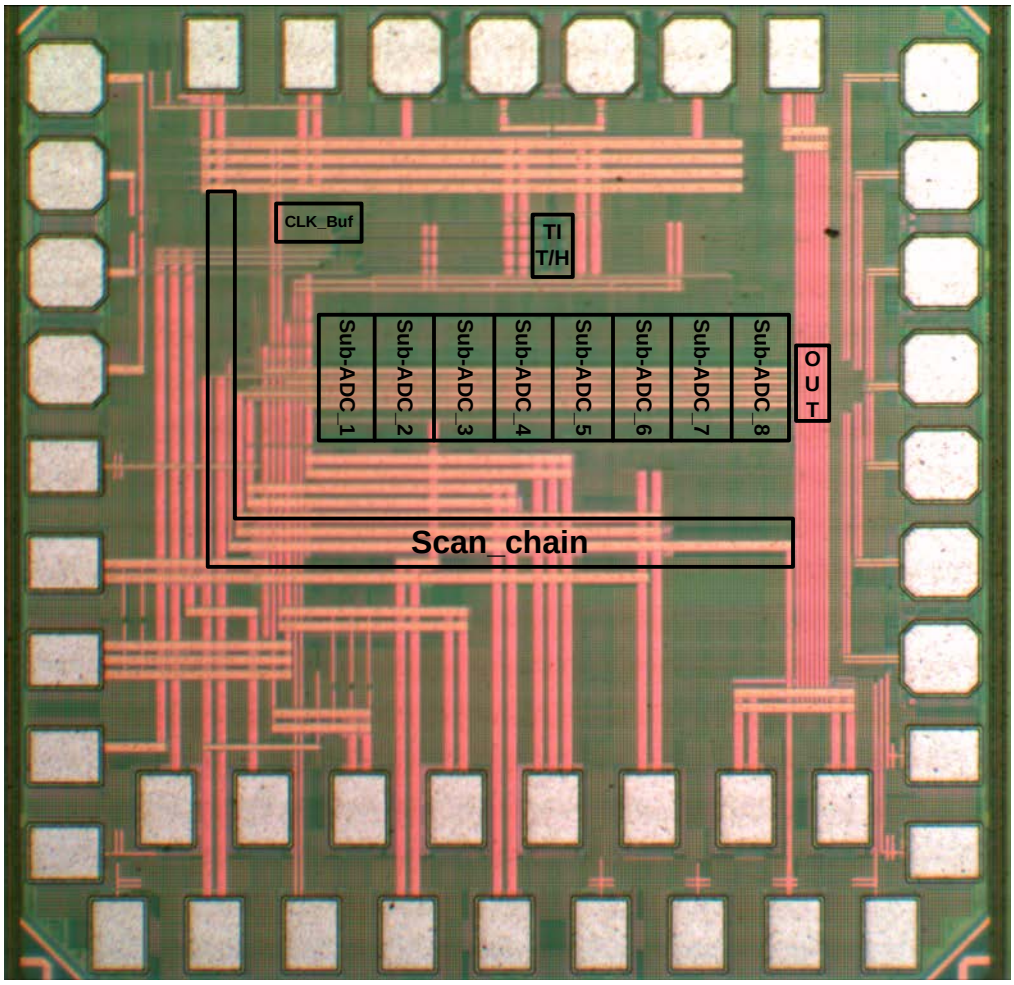



Figure 4.15: Test chip die photo (1mm by 1.5mm, core area 800µm by 500µm).

summarized in Table 4.2. The entire ADC occupies a core area of 800µm by 500µm in 40nm-CMOS technology, and consumes 32.1mW at 12GS/s, excluding the power consumed by the input clock buffer and the output drivers. The peak SNDR achieved is 25.7dB, resulting in a FoM of 169fJ/conversion-step.

Table 4.2: ADC performance summary.

| Technology | TSMC 40nm CMOS | | | |
|---|---|---|---|---|
| Active Area | 800μm × 500μm | | | |
| Full Scale | 600mV | | | |
| Resolution | 5 bit | | | |
| VDD | 1.8V for input clock buffer, 1V for others | | | |
| Sample Rate | 8GS/s | | 12GS/s | |
| Total Power | 20.1mW | | 32.1mW | |
| T/H:<br>Sub-ADC:<br>Clock: | 2.88mW<br>9.54mW<br>7.64mW | | 2.88mW<br>20.88mW<br>8.34mW | |
| $F_{in}$ | 12MHz | 4GHz | 19MHz | 2GHz |
| SNDR | 25.8dB | 21.1dB | 25.4dB | 22.8dB |
| FoM | 105fJ/conv-step | 181fJ/conv-step | 176fJ/conv-step | 237fJ/conv-step |

## 4.6. Discussion

The proposed track-and-hold circuit integrates one additional transistor controlled by a global low-jitter clock into the time-interleaved switches, such that the sampling instant of each sub-ADC is synchronized without requiring a high power global buffer. Such technique provides a power-efficient solution for the time-interleaved ADC with adequate accuracy.

As measured, the designed 12GS/s 5bit ADC partially meets the specification, while consuming significantly low power. When the input signal frequency is low, it can achieve about 4 bit ENOB. The loss in resolution is mainly due to the nonlinearity and the offset in the comparator design caused by the transconductance variation with the differential input voltage. Although the capacitive DAC was re-designed according to previous experience in the single-channel ADC design, and the common-

mode voltage drifting problem was solved, the new issue was not realized and caused trouble. One possible solution for this problem is to introduce the source degeneration in the first stage of the comparator to improve linearity.

Meanwhile, when the input signal frequency is high, the measured dynamic performance of the ADC further degrades. Especially when the input frequency is larger than 3GHz, the amplitude of the digitized output waveform does not increase with the input amplitude. Such problem is marginally improved when probe station is used to directly feed the signal to the on-chip pad, replacing the non-ideal PCB traces. It is suspected that some layout issues lead to such problem but it is unclear yet.

Despite the above two imperfection, one merit is its low power consumption due to the less complicated track-and-hold and clock distribution circuit, as well as the power-efficient sub-ADC design. Comparison with the state-of-the-art ADC with the closest specification [20] is listed in Table 4.3. Possible improvement can be further made by increasing the dynamic range to reduce the offset's impact and by increasing the supply voltage to achieve even higher sampling rate.

Table 4.3: Comparison with previous work [20].

| | [20] | | This work | |
|---|---|---|---|---|
| Technology | TSMC 65nm GP | | TSMC 40nm GP | |
| Active Area | 0.44mm$^2$ | | 0.4mm$^2$ | |
| VDD | 1.1V | | 1.8V for input clock buffer, 1V for others | |
| Full Scale Range | 590mV | | 600mV | |
| Resolution | 5bit | | 5bit | |
| Sample Rate | 12GS/s | | 12GS/s | |
| Input Capacitance | 1.1pF | | about 20fF | |
| | $f_{in}$=10MHz | $f_{in}$=6GHz | $f_{in}$=19MHz | $f_{in}$=2GHz |
| SNDR | 27.5dB | 25.1dB | 25.4dB | 22.8dB |
| FOM | 350fJ/conv-step | 460fJ/conv-step | 176fJ/conv-step | 237fJ/conv-step |
| Power | 81mW excluding digital backend, clock buffer etc. | | 32.1mW excluding clock buffer and output drivers | |
| Time-Interleaved T/H | Distributed time-interleaved T/H with background timing skew calibration | | Distributed time-interleaved T/H with global sampling instants synchronization | |
| Sub-ADC | 5-bit Flash | | 2-bit Flash and 3-bit SAR | |

# 5. Conclusion

Multi-GS/s medium-resolution ADCs have been and will continuously be widely employed in the high-speed SerDes and oscilloscope applications. Depending on the application specification, the sampling rate of 20GS/s can be generally used as a boundary. Above 20GS/s, the popular architecture up to date is to time-interleave a few time-interleaved sub-ADCs usually consisting of a large number of low-speed low-power SA ADCs. Below 20GS/s, it is a general trend to time-interleave a few single-channel high-speed sub-ADCs which are commonly implemented by the Flash structure. This dissertation tries to find a possible solution for the latter circumstance.

The performance of the time-interleaved ADC suffers from the mismatch in gain, offset, and phase skew between different individual channels. Two structures, the global and the distributed, both have their own advantages and disadvantages. Many calibration schemes have been proposed to reduce the phase error in the distributed time-interleaved structure. This dissertation proposes one distributed time-interleaved architecture with global sampling instant synchronization, which does not require the global T/H buffer or complicated phase calibration scheme.

As CMOS technology scales, the ability of a single-channel SA ADC to achieve high sampling rate improves. Due to its superior power efficiency over the normally used Flash, it is promising to use such structure for the sub-ADC to achieve better FOM. This dissertation proposes two versions of single-channel SA ADC based on

the improved asynchronous structure to reduce the feedback delay, which can also be used in other applications requiring a sampling rate from 1GS/s to 1.5GS/s.

Two test chips have been fabricated to verify the proposed architectures. A single-channel 1.25-GS/s 6-bit asynchronous SA ADC was fabricated in 40nm CMOS, achieving 30.5dB peak SNDR while consuming 6.08mW power. Another 8-channel 12-GS/s 5-bit time-interleaved ADC fabricated in 40nm CMOS achieves 25.4dB peak SNDR while consuming 32.1mW power. Although some mistakes have been made in certain building blocks which affect the final performance, the general idea is verified.

Future work could be focused on the improvement for accuracy, including the calibration for parasitic and mismatch in the capacitive network, and the background offset cancellation for comparator. It is promising to combine the techniques presented by [30] and [49], to implement a 2-bit/step asynchronous SA ADC with improved feedback loop which has the potential to achieve even higher sampling rate with outstanding balance power efficiency.

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# Appendices

# Appendix A: Metastability in the Voltage and Time Domain

As discussed in Section 3.3, the metastability detection proposed actually moves the metastability from the voltage domain to the time domain. Therefore, it is helpful to statistically derive the probability of the metastability occurrence in both the voltage and time domain, respectively.

In the voltage domain, the input voltage range of the comparator of interest is equal to the dynamic range of the designed ADC, denoted as $V_{FS}$. Suppose the time allocated for one-bit comparison is $t_{max}$, which is determined by the speed specification, it is defined metastability occurs when the input voltage is smaller than $V_m$ that the evaluation time is longer than $t_{max}$. According to (2.2),

$$t_{max} = \underbrace{\frac{2C_L V_{thp}}{I_o}}_{t_o} + \underbrace{\frac{C_L}{g_{m,eff}} \ln\left(\frac{1}{V_{thp}}\sqrt{\frac{I_o}{8\beta}}\frac{V_{DD}}{V_m}\right)}_{t_{latch}} \tag{A-1}$$

where it is assumed that when the output differential voltage exceeds half of the supply voltage the input value is successively resolved. For the same comparator, especially when the input voltage is small, the first term $t_o$ is almost a constant for different input values so that it is safe to rewrite the equation (A-1) as,

$$t'_{max} = \underbrace{\frac{C_L}{g_{m,eff}} \ln\left(\frac{1}{V_{thp}}\sqrt{\frac{I_o}{8\beta}}\frac{V_{DD}}{V_m}\right)}_{t_{latch}} \tag{A-2}$$

in which $t'_{max} = t_{max} - t_o$, and

$$V_m = \frac{V_{DD}}{V_{thp}}\sqrt{\frac{I_o}{8\,\beta}}\exp\left(-\frac{t'_{max}\cdot g_{m,eff}}{C_L}\right) \tag{A-3}$$

Simply assuming a uniform distribution for the input voltage, the probability that the comparator enters metastability is:

$$P_{m,voltage} = \frac{V_m}{V_{FS}} = \frac{1}{V_{FS}} \cdot \frac{V_{DD}}{V_{thp}} \sqrt{\frac{I_o}{8\beta}} \exp\left(-\frac{t'_{max} \cdot g_{m,eff}}{C_L}\right) \quad \text{(A-4)}$$

On the other hand, the flip-flop as the phase detector in the proposed metastability detection enters metastability when the input to the flip-flop changes during the window defined by the flip-flop setup time $t_{su}$ and the hold time $t_h$, both of which are determined by the flip-flop design.

In the metastability detection proposed, the rising time of the flip-flop input is related to the comparator resolving time $t$ (assuming the time spent in the ready logic is very short), while the rising time of the clock is set to be $t'_{max}$. Therefore, what is to found is the probability that $t$ is within the range of $[t'_{max} - t_{su}, t'_{max} + t_h]$.

Given the probability density function of the comparator input voltage is

$$f_V(v) = \frac{1}{V_{FS}}, v \in [0, V_{FS}] \quad \text{(A-5)}$$

According to (A-3) and again neglecting the variation in the $t_o$ term, the relation between the input voltage $v$ and the time taken to resolve $t$ is as below:

$$v = g(t) = \frac{V_{DD}}{V_{thp}} \sqrt{\frac{I_o}{8\beta}} \exp\left(-\frac{t \cdot g_{m,eff}}{C_L}\right) \quad \text{(A-6)}$$

Therefore, the probability that the flip-flop enters metastability is

$$\begin{aligned} P_{m,time} &= F_T(t'_{max} + t_h) - F_T(t'_{max} - t_{su}) \\ &= P(T < t'_{max} + t_h) - P(T < t'_{max} - t_{su}) \end{aligned}$$

$$= P\left(V > g(t'_{max} + t_h)\right) - P\left(V > g(t'_{max} - t_{su})\right)$$

$$= \left[1 - P\left(V < g(t'_{max} + t_h)\right)\right] - \left[1 - P\left(V < g(t'_{max} - t_{su})\right)\right]$$

$$= \frac{1}{V_{FS}} \cdot \frac{V_{DD}}{V_{thp}} \sqrt{\frac{I_o}{8\,\beta}} \cdot \left[\exp\left(-\frac{(t'_{max} - t_{su}) \cdot g_{m,eff}}{C_L}\right) - \exp\left(-\frac{(t'_{max} + t_h) \cdot g_{m,eff}}{C_L}\right)\right] \quad \text{(A-7)}$$

Based on (A-4) and (A-7), an estimation of the relation between the probability of metastability occurrence for the comparator in the voltage domain and the flip-flop in the time domain can be obtained.

# Appendix B: ATE (Automatic Test Equipment) Script

Automatic Test Equipment (ATE) is any apparatus that performs tests on a device, known as the Device Under Test (DUT), using automation to perform measurements and evaluate the test results quickly and efficiently. In the measurement of the two integrated circuit (IC) chips presented in this dissertation, MATLAB® is employed to contact with the on-chip scan chain, control the DC power supply, the RF signal generator, and the digital oscilloscope, as well as collect data from the oscilloscope for further signal processing.

## Appendix B-1: Contact with On-Chip Scan Chain

The on-chip scan chain provides a method to digitally control certain parameters in the designed circuit, such as bias current, phase delay, and loading capacitance, by turning ON or OFF the corresponding switches. During the measurement, a set of digital 0's and 1's called control bits are injected into the IC chip in a serial manner.

In this measurement, a multifunction DAQ NI USB-6501 is used to contact with the on-chip scan chain. It is required to generate four digital signals: *ck*1 and *ck*2 is a pair of non-overlapping clocks to trigger the flip-flop inside the scan chain, *din* is the set of control bits to be injected, and *load* is the signal enabling the flip-flop outputs.

The script compiled in MATLAB® R2001a is as follows:

```
function scan_in(CB)
% this function uses NI-DAQ USB-6501 to scan in control bits

if (~isempty(daqfind))
    stop(daqfind)
end
```

```
dio = digitalio('nidaq', 'Dev1'); % initiate the device

addline(dio, 0:1, 0, 'Out'); % port 0, line 1 & 0 FOR ck 1 & 2
addline(dio, 3, 0, 'Out');   % port 0, line 3 FOR load
addline(dio, 2, 0, 'Out');   % port 0, line 2 FOR din

N=length(CB);     % CB is the set of control bits to be injected

putvalue(dio.Line(3), 0);

for kk=N:-1:1
    putvalue(dio.Line(4), CB(kk)); % control bit being effective

    flag=0;
    for ii=1:4                     % generate non-overlapping clock
        switch flag
            case 0
                putvalue(dio.Line([1 2]), [0 0]);
                flag=1;
            case 1
                putvalue(dio.Line([1 2]), [0 1]);
                flag=2;
            case 2
                putvalue(dio.Line([1 2]), [0 0]);
                flag=3;
            case 3
                putvalue(dio.Line([1 2]), [1 0]);
                flag=0;
        end
    end
end

putvalue(dio.Line(3), 1);          % enable the flip-flop outputs

delete (dio);
clear dio;
```

## Appendix B-2: Control the Oscilloscope and Collect Data

In this measurement, two digital oscilloscopes Tektronix TDS6804B and Tektronix TDS7404 are used to collect the analog output waveforms, which are transferred to a PC via GPIB, and digitized using MATLAB®. The instrument control toolbox in MATLAB® and the TekVISA developed by Tektronix must be installed beforehand.

The script to set up the TDS6804B scope is as follows:

```
function [Obj1] = init_TDS6804B()

Obj1 = instrfind('Type', 'visa-tcpip', 'RsrcName',
'TCPIP::192.168.1.1::gpib0,1::INSTR', 'Tag', ''); % TDS6804B

if isempty(Obj1)
    Obj1 = visa('TEK', 'TCPIP::192.168.1.1::gpib0,1::INSTR');
else
    fclose(Obj1);
    Obj1 = Obj1(1);
end

set(Obj1,'InputBufferSize',4e6);

fopen(Obj1); % open the connection to the equipment
fprintf(Obj1,'ACQUIRE:STATE OFF');
fprintf(Obj1,'HEADER OFF');
fprintf(Obj1,'DATA:ENCDG SRIBINARY');
fprintf(Obj1,'DATA WIDTH 2');
fprintf(Obj1,'ACQUIRE:MODE SAMPLE');
fprintf(Obj1,'TRIGGER:A:MODE NORMAL');
fprintf(Obj1,'TRIGGER:A:HOLDOFF:BY AUTO');
fprintf(Obj1,'TRIGGER:A:EDGE:COUPLING DC');

fprintf(Obj1,'HORIZONTAL:DELAY:MODE ON');
fprintf(Obj1,'HORIZONTAL:DELAY:POSITION 50');
fprintf(Obj1,'HORIZONTAL:DELAY:TIME 0');
fprintf(Obj1,'HORIZONTAL:MAIN:POSITION 0');
fprintf(Obj1,'HORIZONTAL:MAIN:SAMPLERATE 10e9'); % sample rate 10GS/s
fprintf(Obj1,'HORIZONTAL:MAIN:SCALE 10e-7');
fprintf(Obj1,'HORIZONTAL:MAIN:UNITS "s"');
fprintf(Obj1,'HORIZONTAL:RECORDLENGTH 10e4'); % record length 100,000

fprintf(Obj1,'CH1:OFFSET 0');
fprintf(Obj1,'CH1:POSITION -3');
fprintf(Obj1,'CH1:SCALE 0.1'); % vertical scale 100mV

% fprintf(Obj1,'TRIGGER:A:EDGE:SOURCE LIN'); % triggerred by self
% fprintf(Obj1,'TRIGGER:A:EDGE:SLOPE RISE');
% fprintf(Obj1,'TRIGGER:A SETLEVEL'); % trigger level 50%
% fprintf(Obj1,'ACQUIRE:STOPAFTER SEQUENCE'); % continuous run

fprintf(Obj1,'TRIGGER:A:EDGE:SOURCE AUX'); % triggerred by AUX
fprintf(Obj1,'TRIGGER:A:EDGE:SLOPE FALL');
fprintf(Obj1,'TRIGGER:A:LEVEL 1'); % trigger level 1V
fprintf(Obj1,'ACQUIRE:STOPAFTER RUNSTOP'); % single run
fprintf(Obj1,'ACQUIRE:STATE RUN');
```

The script to get waveform from the oscilloscope is as follows:

```
function[y] = get_waveform(channel,instrument,recordLen)

fprintf(instrument,'DATA:START %d', 1);
fprintf(instrument,'DATA:STOP %d', recordLen);

src=sprintf('DATA:SOURCE CH%d',channel);
fprintf(instrument,src);

% Issue the curve transfer command.
fprintf(instrument, 'CURVE?');
waveform_raw = binblockread(instrument, 'int16');

ymult = query(instrument,'WFMOUTPRE:YMULT?','%s','%e');
yoff = query(instrument,'WFMOUTPRE:YOFF?','%s','%e');
yzero = query(instrument,'WFMOUTPRE:YZERO?','%s','%e');
y = ymult*(waveform_raw - yoff) + yzero;
```