AN ABSTRACT OF THE THESIS OF

SEUNG-HAN ANN for the degree of Master of Science in Electrical and Computer Engineering presented on May 23,1988.

Title: A Chopper-Stabilized CMOS Operational Amplifier.

Abstract approved: Redacted for privacy

David J. Allstot

The chopper-stabilized operational amplifier has good low frequency noise properties. Unfortunately a simple technique for simulation of the chopper-stabilized operational amplifier has not been available.

This thesis describes the implementation of a differential amplifier using chopper stabilization and its circuit modeling for the SPICE simulation. This circuit has been designed using a 3-um p-well CMOS technology. The chopper amplifier has 89 dB dc gain and an output voltage swing from 0.3V to 12V with a 12V power supply. The equivalent input noise is only 12 $nV/\sqrt{Hz}$ at 1 Hz with 10 $nV/\sqrt{Hz}$ as the thermal noise.

A Chopper-Stabilized CMOS Operational Amplifier

by

Seung-Han Ann

A THESIS

submitted to

Oregon State University

in partial fulfillment of

the requirement for the degree of

Master of Science

Completed May 23, 1988

Commencement June 1989

APPROVED :

Redacted for privacy

Professor of Electrical and Computer Engineering in charge of major

Redacted for privacy

Head of department of Electrical and Computer Engineering

Redacted for privacy

Dean of Graduate School

Date thesis is presented May 23, 1988

ACKNOWLEDGEMENT

I would like to express my sincere gratitude to my advisor, Dr. David J. Allstot, for his advice, guidance and encouragement. My last 2 years research experiences with him have been deeply influenced on me. I am further grateful to professor Rudolf S. Engelbrecht, professor James C. Looney and professor Joel Davis for serving on my graduate commitee.

I would like to take this opportunity to give my sincere thanks to Magnavox Co. for support and guidance. My thesis research was sponsored by Magnavox Co.

Finally, I would like to express my deepest appreciation to my parents and my wife. Their endless love and support have encouraged me through all these years.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

Symbol	Description	Unit
a_{cm}	Common-mode gain	
a_{dm}	Differential-mode gain	
AF	Flicker noise parameter	
CMMR	Common-mode rejection ratio	dB
C_{ox}	Gate-oxide capacitance per unit area	F/cm^2
f_{chop}	Chopping frequency	Hz
f_k	Corner frequency	Hz
g_{ds}	Output conductance	S
g_m	Transconductance	S
k	Boltzmann constant	J/K
KF	Flicker noise parameter	
W_u	Unit-gain bandwidth	Hz
λ	Channel-length modulation parameter	1/V
μ	Mobility of majority carrier	$cm^2/V\text{-}s$

A CHOPPER-STABILIZED CMOS OPERATIONAL AMPLIFIER

I. INTRODUCTION

It is well known that the noise of a MOSFET at low frequencies is very high due to the dominant contribution of flicker noise, by which highly sensitive CMOS amplifiers are always limited [1]. Chopper stabilization is a frequency modulation circuit technique that has been successfully employed in switched-capacitor filters to eliminate the effects of low frequency MOSFET flicker noise. Good low frequency noise was achieved by Hsieh et al. [2] in a CMOS chopper-stabilized differential amplifier for switched-capacitor filters. The equivalent input noise was 40 nV/$\sqrt{\text{Hz}}$ with a chopper frequency of 128 KHz. The equivalent input noise was 63 nV/$\sqrt{\text{Hz}}$ and free from flicker noise in [1] by using a chopper amplifier with a 3-um p-well CMOS technology. Even though the chopper-

stabilized SC circuit has a good noise performance, its simulation has not been available by a simple technique.

This thesis describes a chopper-stabilized differential amplifier and its circuit modeling for SPICE simulation. This work is based upon the previous work of Fisher [3] in modeling conventional unchopped switched-capacitor filters. A 3-um p-well CMOS technology is adapted for circuit fabrication. CMOS technologies have some disadvantages of fabrication complexity and device area compared to NMOS. Complementary MOS is preferred for its low power consumption, its fast rise time and its wide operation range. Silicon-gate CMOS is more complex to manufacture, but has significantly higher circuit density and better high-speed performance [4]. Higher packing density, low noise performance, improvement of latch-up and independent threshold adjustment are achieved by the p-well process [5]. A class AB output stage with added common-source circuit is adapted for the output stage of the amplifier to improve its frequency characteristics, minimization of power dissipation

and high output voltage swing.

In section II, the noise of an operational amplifier and its reduction technique are discussed. The discussion is included so that the importance of the flicker noise in a switched-capacitor filter can be well understood. In section III, the modeling circuits with and without the chopper stabilization are presented and parameters for the SPICE2 program are also discussed. The implementation of a chopper-stabilized circuit including output circuit, chopping circuit and feedback circuit is presented in section IV. The properties of the amplifier which include ac gain, unity-gain, bandwidth, CMRR and noise analysis are discussed in section V. Finally, the noise performance using chopper stabilization is presented in section VI.

II. AMPLIFIER NOISE AND ITS REDUCTION AT LOW FREQUENCY

A.Operational Amplifier Noise

Electronic devices exhibit random fluctuations in voltage or current, and these fluctuations are referred to as noise. The noise in an electronic circuit often imposes a practical limit to the performance of the circuit [6]. There are many kinds of noise in an electronic circuit. There are three main noise sources in switched-capacitor circuits [7] :

1. Clock feedthrough noise;
2. Noise from power, clock, groundlines and from the substrate;
3. Thermal, flicker and aliased noise.

Thermal noise and flicker noise are dominant in an MOS operational amplifier. A typical equivalent input noise spectrum is shown in fig. 1. The thermal noise is generated by random

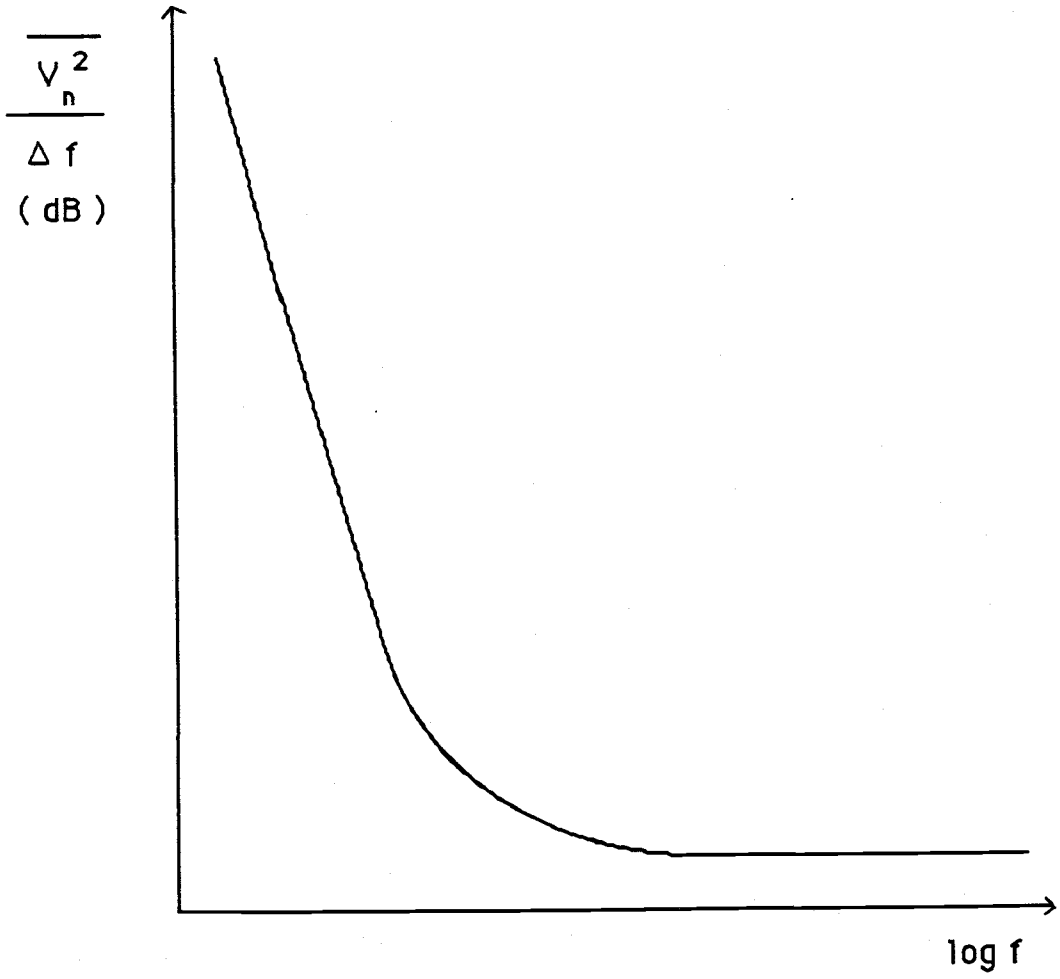

Fig. 1. Typical equivalent input noise spectrum.

thermal motion and the noise voltage power is given by [7]

$$\overline{V_{th}}^2 = \frac{8\ kT}{3\ g_m}\ \Delta f \qquad (2.1)$$

with

$$g_m \equiv \frac{\partial\ I_d}{\partial\ V_{GS}} \mid V_{DS} = \text{constant} \qquad (2.2)$$

$$= \frac{\partial}{\partial\ V_{GS}} \left\{ \frac{1}{2}\ \mu\ C_{ox}\ (\ V_{GS} - V_T\ )^2\ (\ 1 + \lambda\ V_{DS}\ ) \right\}$$

where k is Boltzmann's constant, f is the bandwidth in which the noise is measured in Hz, μ is the surface mobility of majority carriers in the channel region, C_{0x} is gate-oxide capacitance per unit area, and λ is the channel-length modulation parameter. The power spectral density of the thermal noise source, $\overline{V_{th}}^2 /$ f, is independent of frequency from equation (2.1). In practice, the spectral density decreases with increasing frequency by other physical phenomena at very high

frequencies. It is very complicated to analyze the thermal noise by the fact that the frequency independence of this noise is valid up to a frequency much greater than the sampling frequency. As a result, the effect of this noise source will be extended into the passband even after chopping [1].

Another major source of noise is the flicker noise which is dominant at low frequencies. Many papers have explained this noise phenomenon without a clear definition because of its complexity and diversity. This noise is caused by a random trapping of free electrons at the boundary between different materials(silicon and silicone dioxide) because extra electron energy states exist at the boundary. This noise phenomenon was well explained in [8] by combining the carrier-density fluctuation model, based upon McWorter's work and the mobility fluctuation model, based upon Hooge's empirical relationship. Those works are explained by a tunneling mechanism and by homogeneous semiconductors and devices, respectively. This total noise power is expressed by

$$\overline{V_{1/f}}^2 = \frac{C_1}{f\,W\,L}\left(\frac{q}{C_{ox}}\right)^m (V_{GS} - V_T) + \frac{C_2}{f\,W\,L}\left(\frac{q}{C_{ox}}\right)^2 \qquad (2.3)$$

and $m = 0.7 - 1.2$ for typical devices,

where, V_{GS} is gate-source voltage, V_T is threshold voltage and W and L are the channel width and length of the device, respectively. Equation (2.3) explains that the flicker noise is a function of carrier-density fluctuation (C_2 term) and mobilty fluctuation (C_1 term) and is proportional to the effective gate-source voltage, and the interface state density, and is inversely proportional to the gate-oxide capacitance [9]. Since this noise power is dependent on frequency, we can reduce the flicker noise by shifting this noise source outside of the passband under the assumption that the noise energy associated with the flicker noise lies below the chopping frequency. This is the objective of the chopper stabilization.

The principle of noise analysis is shown in fig. 2. A simple

common-source amplifier circuit is adapted for explaining the noise analysis. This circuit is divided into two parts: noise sources (Fig. 2b) and ideal noiseless devices (Fig. 2c). The input noise is multiplied by the device gain and the output noise power of Fig. 2b is given by:

$$\overline{V_{out}}^2 = \left(\frac{g_{m1}}{g_{out}}\right)^2 \overline{V_{n1}}^2 + \left(\frac{g_{m2}}{g_{out}}\right)^2 \overline{V_{n2}}^2 \qquad (2.4)$$

When the input noise is referred to the gate of device M_1, the circuit is divided into noiseless devices and an equivalent input noise source (fig. 2c)

$$\overline{V_{out}}^2 = \left(\frac{g_{m1}}{g_{out}}\right)^2 \overline{V_{eq}}^2 \qquad (2.5)$$

Since equations (2.4) and (2.5) must be equal,

$$\overline{V_{eq}}^2 = \overline{V_{n1}}^2 + \left(\frac{g_{m2}}{g_{m1}}\right)^2 \overline{V_{n2}}^2 \qquad (2.6)$$

where, $\overline{V_{eq}}^2$ is the equivalent input noise power.

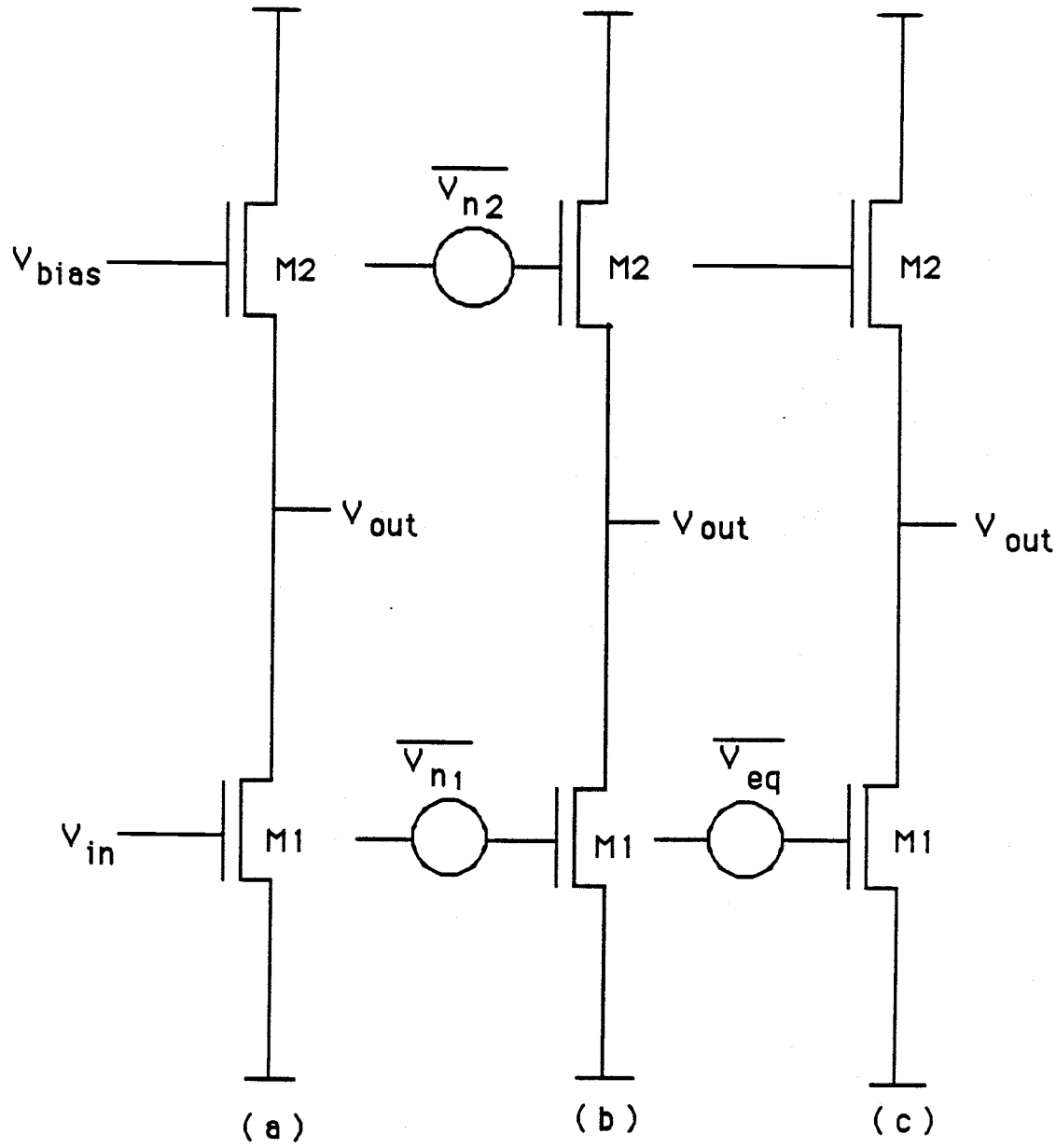

Fig. 2. (a) Common-source circuit; (b) with noise sources;

(c) noiseless devices and equivalent input noise source.

B. The Reduction of Flicker Noise [1]

The flicker noise which is dominant at low frequencies is a function of the process technique, the circuit design, and the gate sizes of the devices used. One approach to reduce this noise is simply to use large input device sizes because this noise is inversely dependent on gate area. This approach was used in the past but is extremely uneconomical for applications requiring high dynamic range. Another approach is to use CMOS transistors operated in the lateral bipolar mode. This technique showed better noise properties than with a conventional MOS amplifier [10]. The operational amplifier using this technique obtained an equivalent input noise density as low as $11nV/\sqrt{Hz}$ at 1 Hz. The flicker noise is reduced as much as 46 dB compared with the conventional MOS operational amplifier by the elimination of surface effects. In addition, gain is increased up to 12 dB by the higher transconductance. The process complexty of this technique is removed by the lateral bipolar technique [10]. But this technique is not reasonable for switched-

capacitor filters because of input base current which discharges capacitors [1], [11]. Another approach is to use the chopper-stabilized switched-capacitor filtering technique which translates the noise energy from a low frequency to a higher frequency so that it does not affect the signal. This technique has been used in the design of precision dc amplifiers and is well introduced by [1]-[2]. The principle of the chopper stabilization is shown in fig 3., and explained with a two stage amplifier, a voiceband input signal and a square-wave of amplitude +1 and -1 at the chopper frequency. At the first multiplier, the input signal is multiplied by the square-wave modulation signal $m_i(t)$, and the signal is translated to the odd harmonic frequencies at the chopping frequency and amplified by the a_1 stage. At the second multiplier, the input signal is demodulated back to the original signal. Since the bandwidth of amplifier is limited by the chopper frequency, the output signal has spectral components around the even harmonics of the chopper frequency. On the other hand, the noise signal is modulated to the odd harmonic frequencies of the square-wave at the sampling frequency by

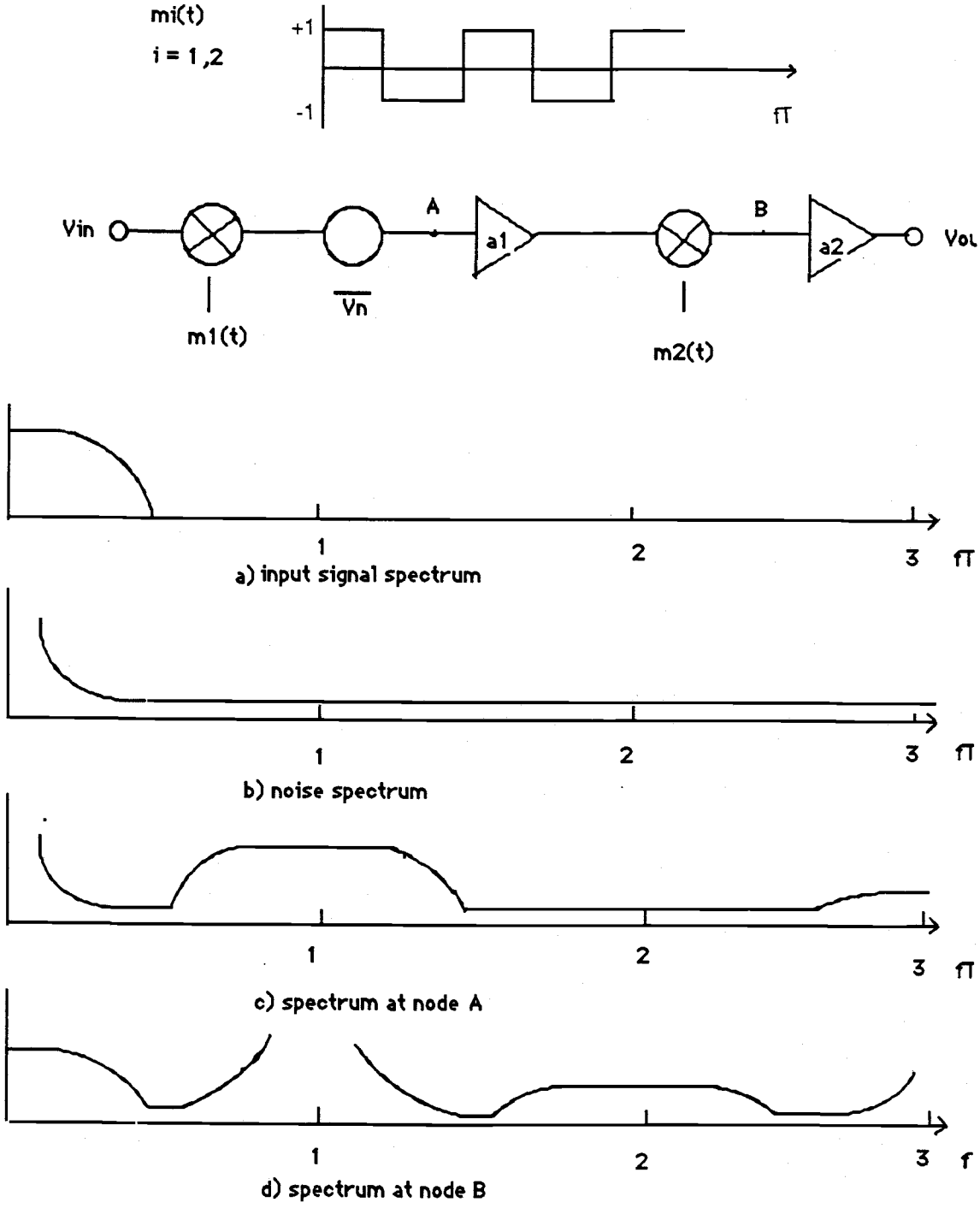

Fig. 3. The principle of chopper stabilization.

the second multiplier only. If the sampling frequency is much higher than the signal bandwidth, the flicker noise will be reduced by this technique. The flicker noise will remain at very high frequencies and can be removed by a low-pass filter. This chopper-stabilized technique can be applied to an MOS operational amplifier where the multipliers are replaced by two cross-coupled switches which are controlled by two nonoverlapping clocks. The implementation is shown in fig 4. By changing phase ϕ_{p1} to ϕ_{p2}, the chopping technique is simply done.

When ϕ_{p1} is on and ϕ_{p2} is off (fig. 4a), the equivalent input noise is the equivalent input noise of the first stage plus that of the second stage divided by the gain of the first stage [2]. When the phase is reversed, the equivalent input noise of the first stage has the negative value of the previous stage (fig. 4b) The total equivalent input noise is twice the equivalent of the second stage divided by the gain of the first stage. Since the equivalent input noise of the second stage is very small, the equivalent input noise can be neglected if the gain of the first stage is high enough.

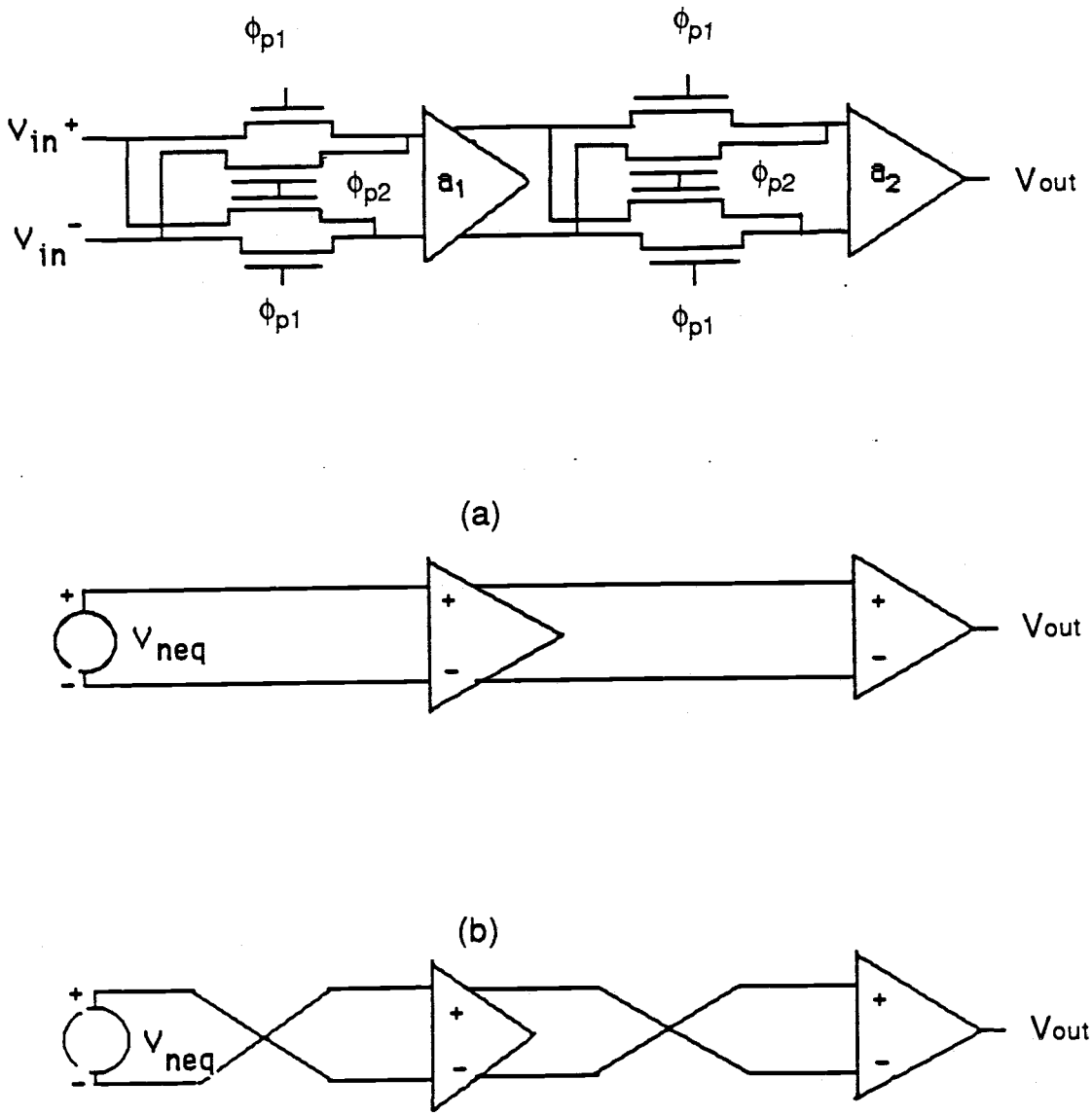

Fig. 4. The application of a chopper-stabilized technique for MOS operational amplifier.

III. CIRCUIT MODELING FOR SPICE SIMULATION

Chopper stabilization has good properties for the reduction of the flicker noise and is well employed in switched-capacitor filtering circuits. Unfortunately a simple technique for simulating the expected performance of chopper-stabilized switched-capacitor circuits has not been available. To simulate the noise performance of this technique using the SPICE2 program, a circuit modeling technique is needed. This work is based upon Fisher's noise model [3] for unchopped switched-capacitor filtering circuits. The modeling circuit for noise analysis is shown in fig. 5. The modeling circuit has two poles to explain the frequency characteristics of the two stage amplifier. The thermal noise source and the flicker noise source are shown in fig. 5 (a) and 5 (b), respectively. Two resistors (R_a and R_b) connected in parallel are used to describe the thermal noise, which is to be matched with the measured equivalent input flat band noise of the operational amplifier. This noise power is expressed by [7]

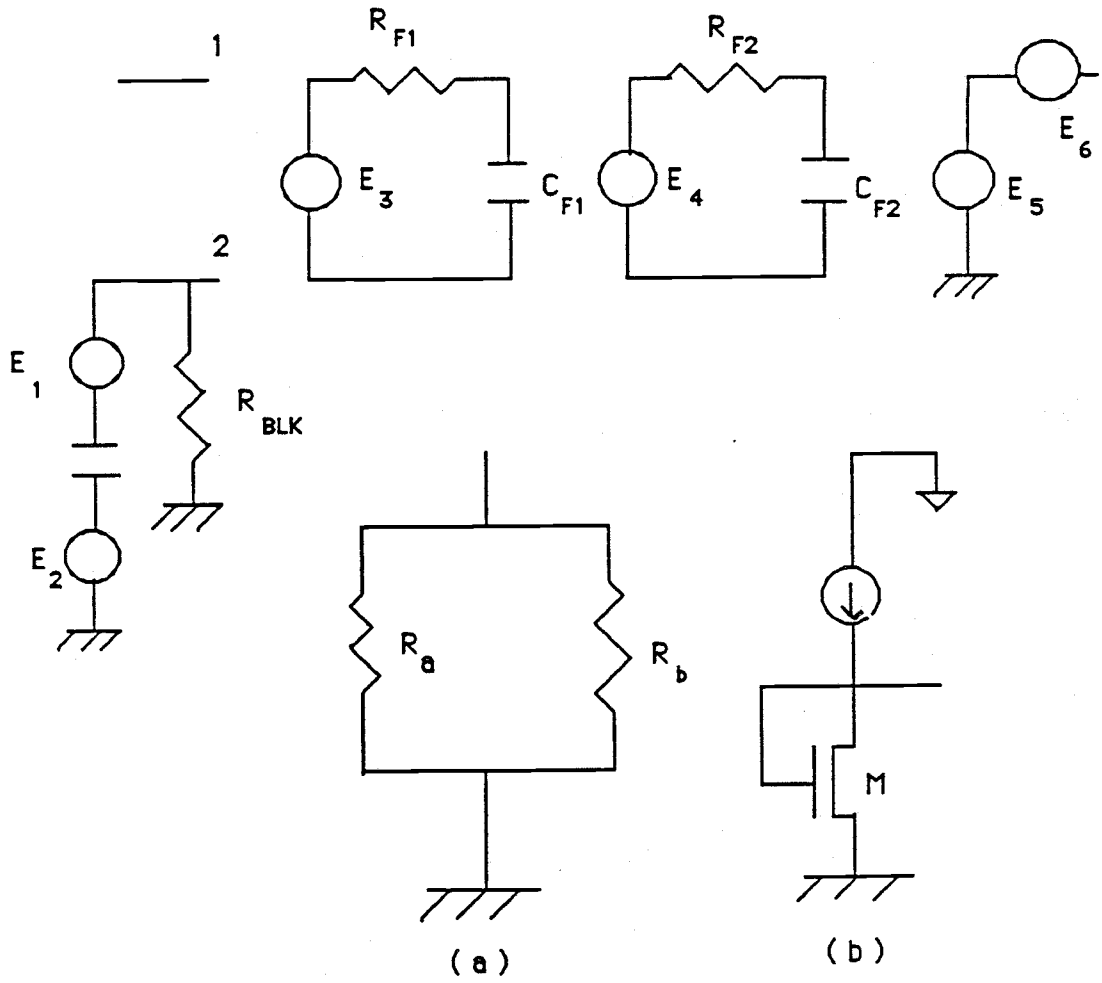

Fig. 5. Noise analysis circuit: (a) Thermal noise source.

(b) Flicker noise source

$$\overline{V_{th}}^2 = 4\ kTR\ \Delta f \qquad (3.1)$$

$$\text{and } R = \frac{R_a R_b}{R_a + R_b}$$

A voltage-controlled voltage source (E_1) with unity gain is selected to apply the thermal noise into the modeling circuit. Enhancement mode device (M) is used to model the flicker noise. The diode connection ensures that this device is always in the saturation region. The noise power is expressed by

$$\overline{V_{1/f}}^2 = \frac{KF\ I^{AF}}{g_m{}^2\ C_{ox}\ L^2\ f}\ \Delta f \qquad (3.2)$$

where AF and KF are the flicker noise parameters. The voltage-controlled voltage source (E_2) is selected to apply the flicker noise into the model. Since the flicker noise is to be injected into the noninverting terminal of a operational amplifier, a blocking circuit (R_{BLK} and C_{BLK}) is needed to block the dc bias voltage at the drain, and the flicker noise source is also

expressed using a voltage-controlled voltage source as an ideal unity gain buffer [3]. Finally to decide the frequency characteristics of the operational amplifier, R_F and C_F are caculated by

$$W_o = \frac{W_u}{a_o} = \frac{2\,\Pi f_o}{a_o} = \frac{1}{R_F C_F} \qquad (3.3)$$

$$\text{and } C_F = \frac{a_o}{2\Pi f_o R_F}$$

where, f_o is unity-gain frequency and a_o is the open-loop gain at 1Hz. R_{F1} and C_{F1} model the frequency characteristics of the first stage, and R_{F2} and C_{F2} model the other stages.

Each node and source is defined below as:

E_1 : The thermal noise source

E_2 : The flicker noise source

E_3 : The gain of the first stage

E_4 : The gain of the other stage

E_5 : Unity gain buffer

E_6 : Foldover factor

Node 1 : Inverting terminal

Node 2 : Noninverting terminal

Node 3 : Output terminal

To reduce the thermal noise effect of device (M), a large device W/L ratio is selected, and then the bias current is selected. With the selected parameters, adjust the flicker noise parameter KF to match the measured equivalent input noise spectrum of the operational amplifier to that of the modeling circuit.

Now the chopper stabilization technique is applied and another voltage-controlled voltage source (E_5) is added. This voltage-controlled voltage source is selected to describe the foldover effect using the bandwidth of the amplifier, and its voltage gain has the value of the foldover parameter (K), which

is calculated by [3]:

$$K = \sqrt{\frac{2\,BW_n}{f_{sampling}} - 1} \tag{3.4}$$

By applying the chopper stabilization, the flicker noise is removed with the cost of increasing the thermal noise. To verify this effect, the voltage gain of the voltage-controlled voltage source (E_1) is changed to compensate for the thermal noise difference due to folding effects. The voltage gain is calculated by [2]

$$\sqrt{1 + \frac{17\ f_K}{2\ \Pi f_{chop}}} \tag{3.5}$$

where f_K means the corner frequency of the amplifier. The value of 1 ohm is given to R_{BLK} for the simulation of the modeling circuit to analyze the chopping effect of the operational

amplifier. With the feedback circuit which has large resistors the input voltage is attenuated by the resistors of the feedback circuit and a very small voltage is biased into the noninverting terminal. A very large value of the R_{BLK} is chosen to bias the input voltage into the non-inverting terminal. The modeling circuit of the chopper stabilization is shown in fig. 6.

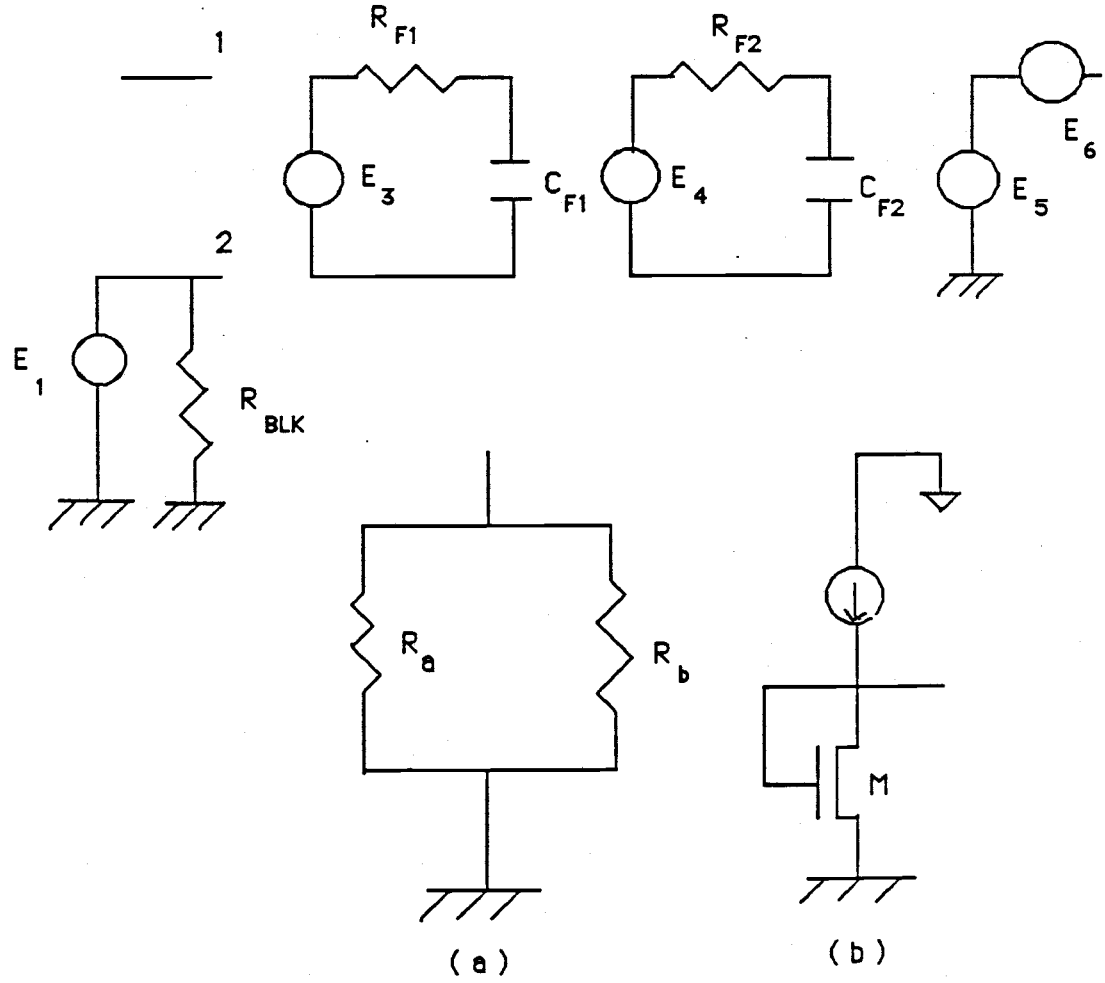

Fig. 6. Noise analysis of chopper stabilization.

IV. DIFFERENTIAL CHOPPER-STABILIZED OPERATIONAL AMPLIFIER

A. Output Stage

Class AB output stages are widely used in MOS circuit design to minimize power dissipation. They have very desirable frequency characteristics in the form of one pole and one zero at very high frequencies. The most widespread application of this output stage is in an output buffer [12]. This output stage has very high output voltage swing with respect to the low power supply. But the swing is limited to more than a V_{DS} from the high power supply. By adding a simple common-source circuit connected in parallel, both the advantage of the common- source output stage, high gain, and that of class the AB output stage, low power dissipation and low output impedance, are obtained [13]. In addition, high voltage swing is obtained by connecting two poles. This output stage is shown in fig. 7. Under low input voltage, M_4 and M_8 are turned off in the quiescent state. All the

output current flows through M_6 and high output voltage can be obtained. When high input voltage is applied, M_4 and M_8 are both turned on. Since M_6 is turned off, most of the current flowing M_5 flows through M_4 and the saturation voltage of M_8 is dominantly reduced, then very low output voltage is obtained. At each step, the quiescent current flowing through the output stage is well controlled by current mirrors. Since the output swing is nearly equal to the supply voltage, this output stage is attractive for a switched-capacitor circuit with a large capacitive load.

B. Feedback Circuit

The feedback circuit for a low noise operational amplifier which consists of 6 resistors and 2 capacitors is shown in fig. 8. To calculate the loop gain of the feedback circuit, small-signal ac analysis is performed. Since the voltage of node 5 is equal to the voltage of node 6 and the sum of the current at node 5 is zero,

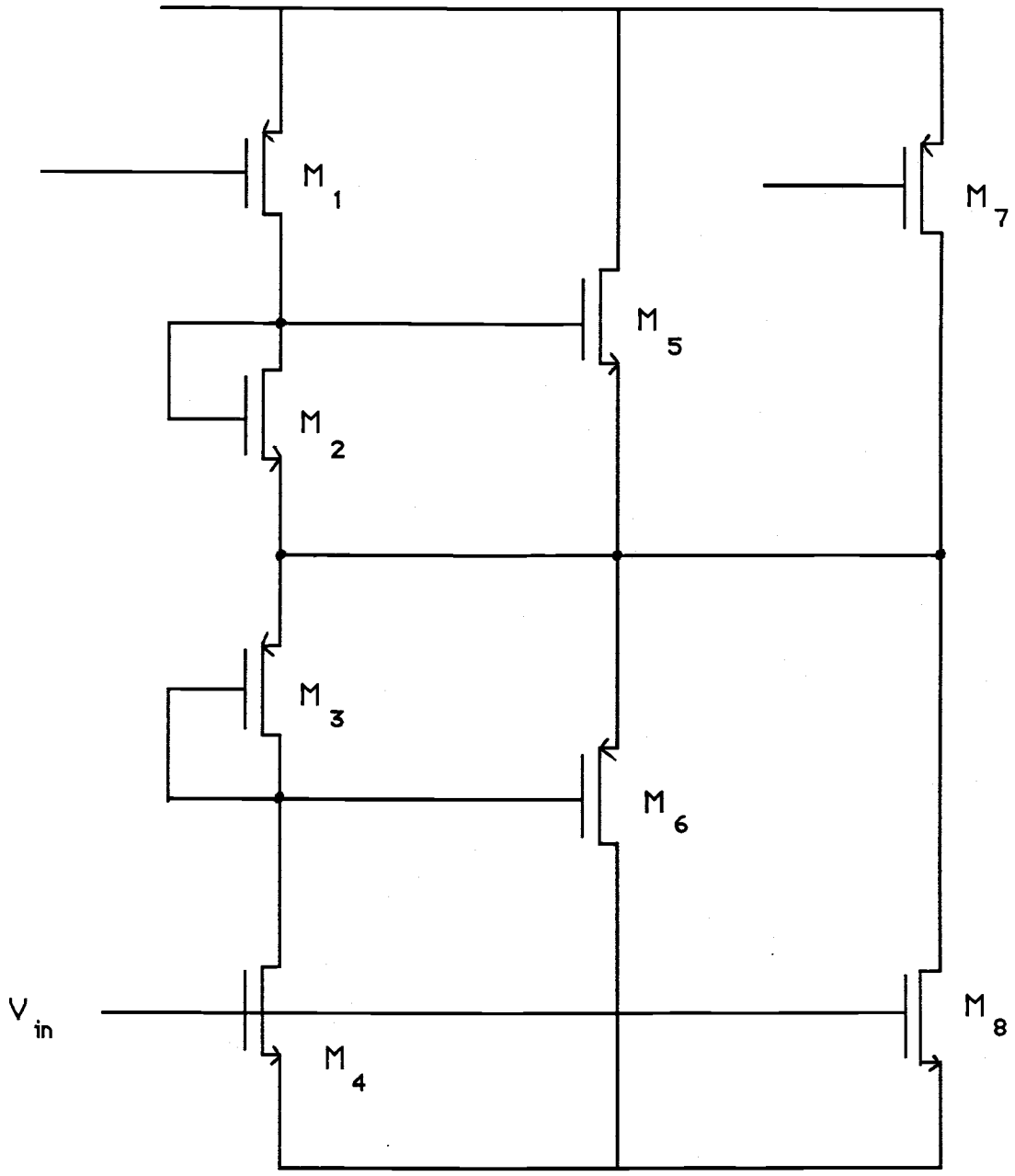

Fig. 7. Output stage.

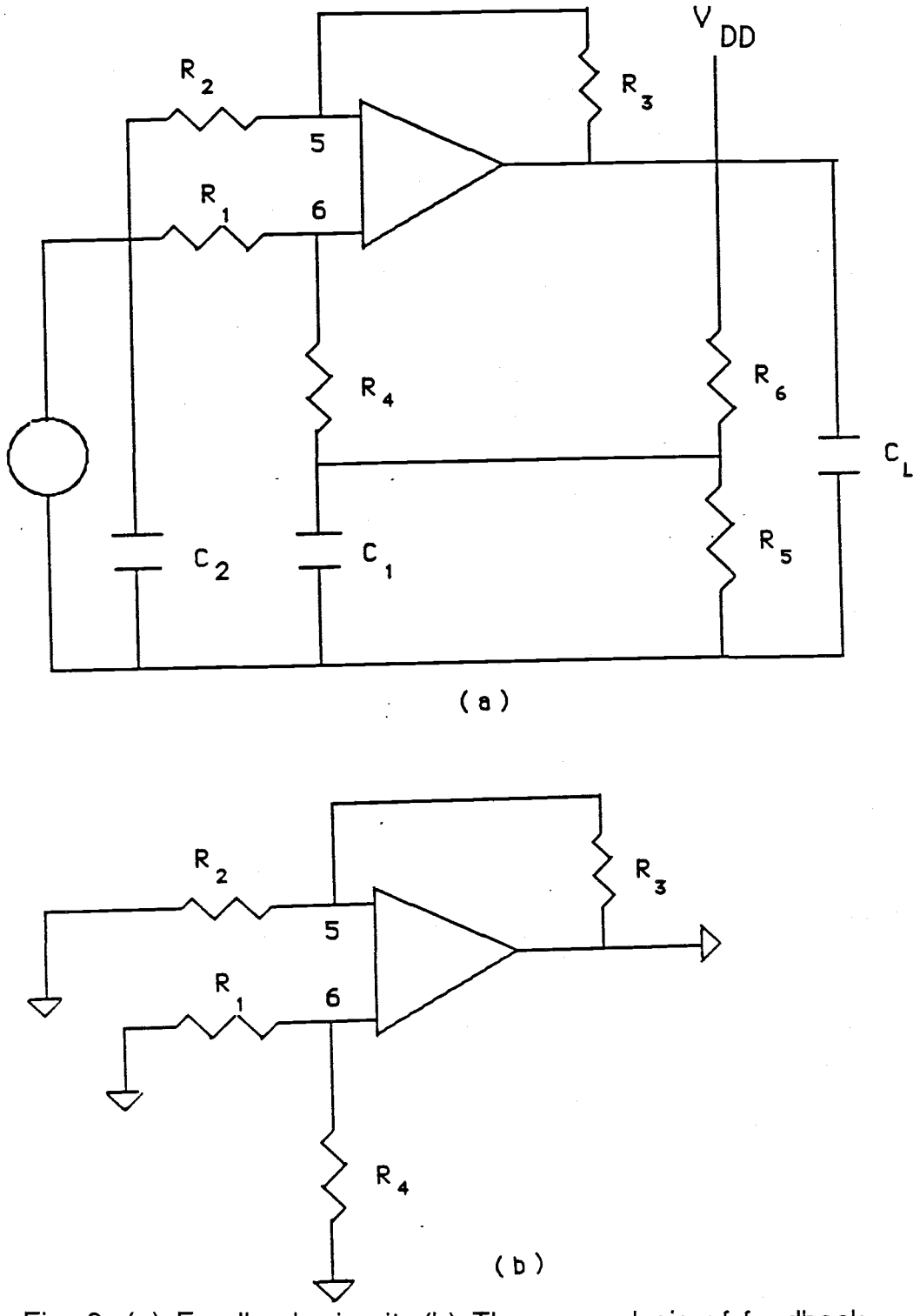

Fig. 8. (a) Feedback circuit. (b) The ac analysis of feedback circuit.

$$V_5 = V_6 = \frac{R_4}{R_1 + R_4} V_{in} \tag{4.1}$$

$$\frac{V_5}{R_2} + \frac{V_5 - V_{out}}{R_3} = 0 \tag{4.2}$$

From equations (4.1) and (4.2), the loop gain of feedback circuit is obtained:

$$\frac{R_4 V_{in}}{R_2 (R_1 + R_4)} + \frac{R_4 V_{in} - (R_1 + R_4) V_{out}}{R_3 (R_1 + R_4)} = 0 \tag{4.3}$$

$$\frac{V_{out}}{V_{in}} = \frac{R_4 (R_2 + R_3)}{R_2 (R_1 + R_4)} \tag{4.4}$$

C. The Implementation of Operational Amplifier with Feedback.

The operational amplifier whose two related differential pairs are well balanced is needed for the chopper stabilization technique. A folded-cascode amplifier meets this requirement

and has a good phase margin. Since it has a very low frequency pole, its phase is shifted in the voiceband. In addition, it has nearly fixed gain with a low value at the first chopping stage. The gain of the first chopping stage should be high to reduce the low frequency noise using chopper stabilization. A two stage amplifier satisfies these requirements except for the phase margin. It has two balanced chopping pairs and good phase characteristics in the voiceband. By modulating the W/L ratio of the devices, high gain is obtained at the first stage.

The key point of the circuit implementation is combining the double-input double-ended stage and double-input single-ended stage, output stage, two cross-coupled choppers and feedback circuit. The implementation of the circuitry using balanced cross-coupled analog switches is shown in fig. 9. Transistors M_{c1}-M_{c4} and M_{c5}-M_{c8} form two cross-coupled choppers which are controlled by two nonoverlapping clocks. Transistors M_1-M_5, M_5 - M_{10} and M_{11}-M_{18} are input, gain, and output stages, respectively. To adjust the current flowing in

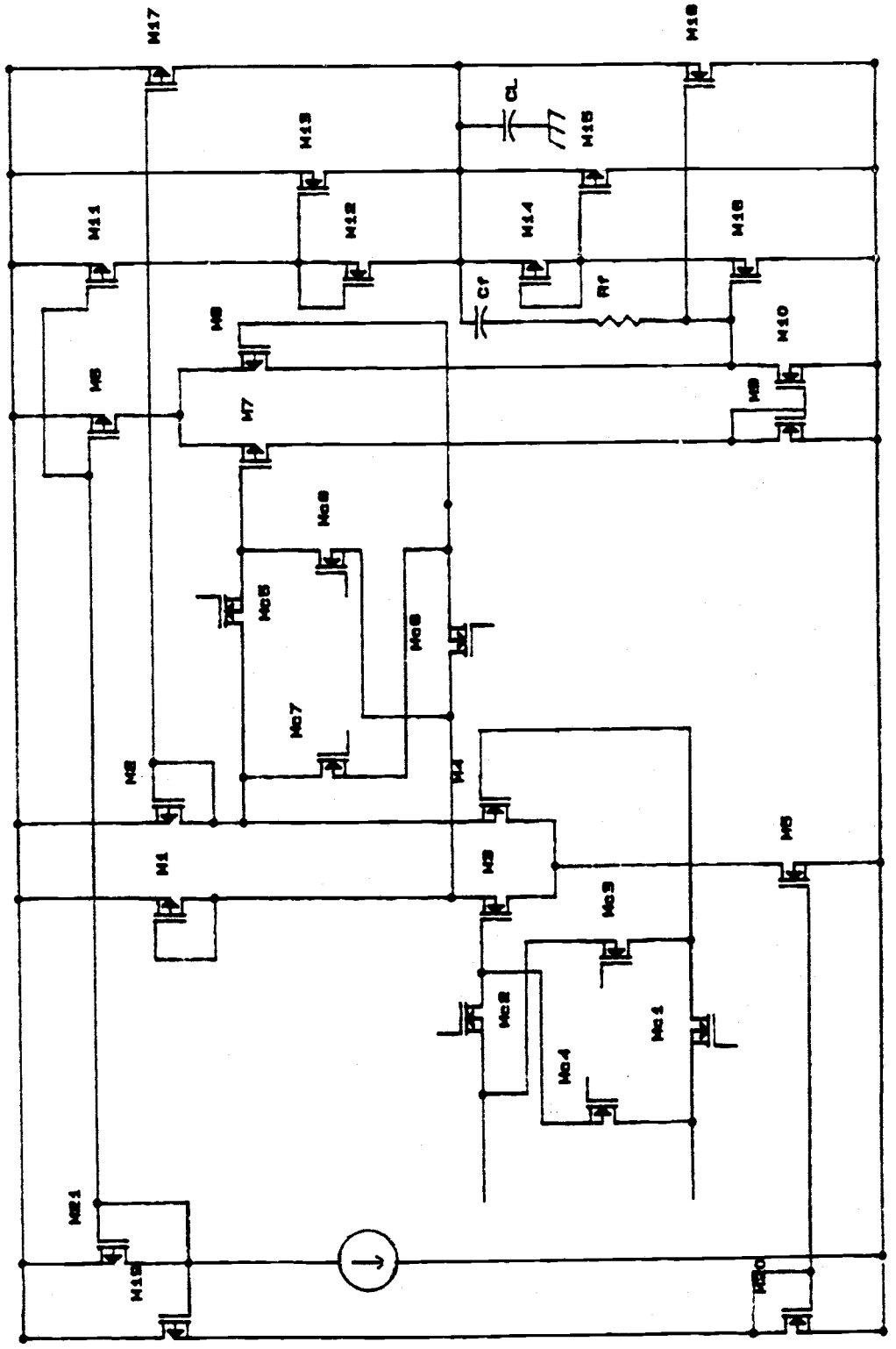

Fig. 9. The circuitry of chopper-stabilized operational amplifier.

the circuitry, six current mirrors are used.

Since the unity-gain bandwidth is increased by the second stage, frequency compensation is needed for the two stage amplifier. It is very difficult to analyze the output stage, which combines the class-AB source follower and the common-source circuit. Since nodes 10 and 13 have high impedance and low frequency poles, RC frequency compensation is established between these two nodes. Even though a good phase margin is obtained because the second low frequency pole is moved into high frequency region, the phase characteristics in the voiceband are deteriorated because the first low frequency pole is shifted into the low frequency region. Since no phase shift is needed in the voiceband, the sacrifice of the phase margin is be obtained because the second low frequency pole is moved into high frequency resion, the phase characteristics in the voiceband are deteriorated because the first low frequency pole is shifted into the low frequency region. Since no phase shift is needed in the voiceband, the sacrifice of the phase margin is

inevitable. Within the limitation of no phase shift in the voiceband, the frequency compensation is established.

V. THE PROPERTIES OF THE AMPLIFIER

1) Open-loop gain

$$A_{vo} = A_{v1} \times A_{v2} \times A_{v3} \tag{5.1}$$

where, A_{v1}, A_{v2} and A_{v3} are the gains of the first stage, the second stage and the output stage. Approximately the gain (A_{vo}) is:

$$\frac{g_{m3}}{g_{m1}} \times \frac{1}{2}\left(\frac{g_{m7}}{g_{ds7}+g_{m9}} \times \frac{g_{m10}}{g_{ds8}+g_{ds10}} + \frac{g_{m8}}{g_{ds8}+g_{ds10}}\right)$$

$$\times \frac{g_{m16}+g_{m18}}{g_{ds(eff)}} \tag{5.2}$$

2) Noise power ($\overline{V_n^2}$)

$$2\left[\overline{V_{n3}}^2 + \left(\frac{g_{m1}}{g_{m3}}\right)^2 \overline{V_{n1}}^2\right] + \frac{1}{a_{v1}}\left[\overline{V_{n7}}^2 + \left(\frac{g_{m10}}{g_{m7}}\right)^2 \overline{V_{n10}}^2 + \overline{V_{n17}}^2\right] +$$

$$\frac{1}{a_{v1}}\left(\frac{g_{m18}}{g_{m17}}\right)^2 \overline{V_{n18}}^2 + \frac{1}{a_{v1} x a_{v2}}\left[\overline{V_{n18}}^2 + \left(\frac{g_{m17}}{g_{m18}}\right)^2 \overline{V_{n17}}^2\right] \tag{5.3}$$

with $\overline{V_n{}^2} = \overline{V_{th}{}^2} + \overline{V_{1/f}{}^2}$ (5.4)

where the subcripts mean the number of the device.

3) Unit-gain bandwidth

$$W_u = \frac{g_{m(eff)}}{C_L} \tag{5.5}$$

$$g_{m(eff)} = g_{m3} \times \frac{\text{W/L ratio of } M_1}{\text{W/L ratio of } M_7}$$

where C_L is load capacitor.

4) Differential-mode gain (a_{dm})

The differential-mode circuit and its half-circuit are shown in fig.10.

$$a_{dm} = \frac{\Delta V_{od}}{\Delta V_{id}}$$

$$= \frac{g_{m3}}{g_{m1}} \tag{5.6}$$

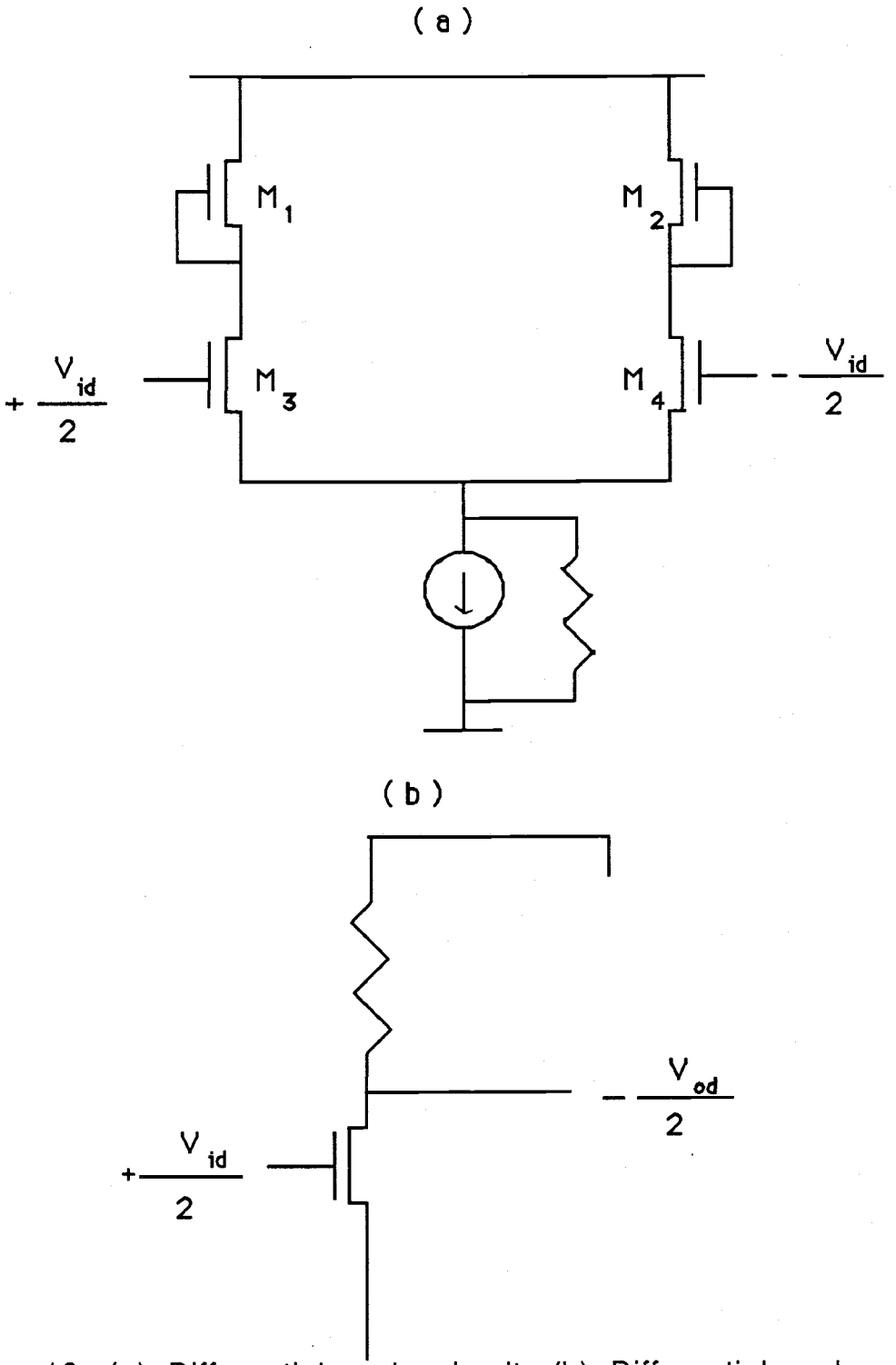

Fig. 10. (a) Differential-mode circuit; (b) Differential-mode half-circuit.

5) Common-mode gain (a_{cm})

The input common-mode circuit and its common-mode half-circuit are shown in fig. 11.

$$a_{cm} = \frac{V_{oc}}{V_{ic}} \tag{5.7}$$

$$= \frac{g_{m3} \dfrac{1}{g_{m1}}}{1 + (g_{m3} + g_{ds3}) \dfrac{2}{g_{ds5}} + \dfrac{g_{ds1}}{g_{m1}}}$$

6) Common-mode rejection ratio (CMRR)

$$CMRR = 20 \log | a_{dm} / a_{cm} | \tag{5.8}$$

where, a_{dm} and a_{cm} are differential gain and common-mode gain of amplifier, respectively.

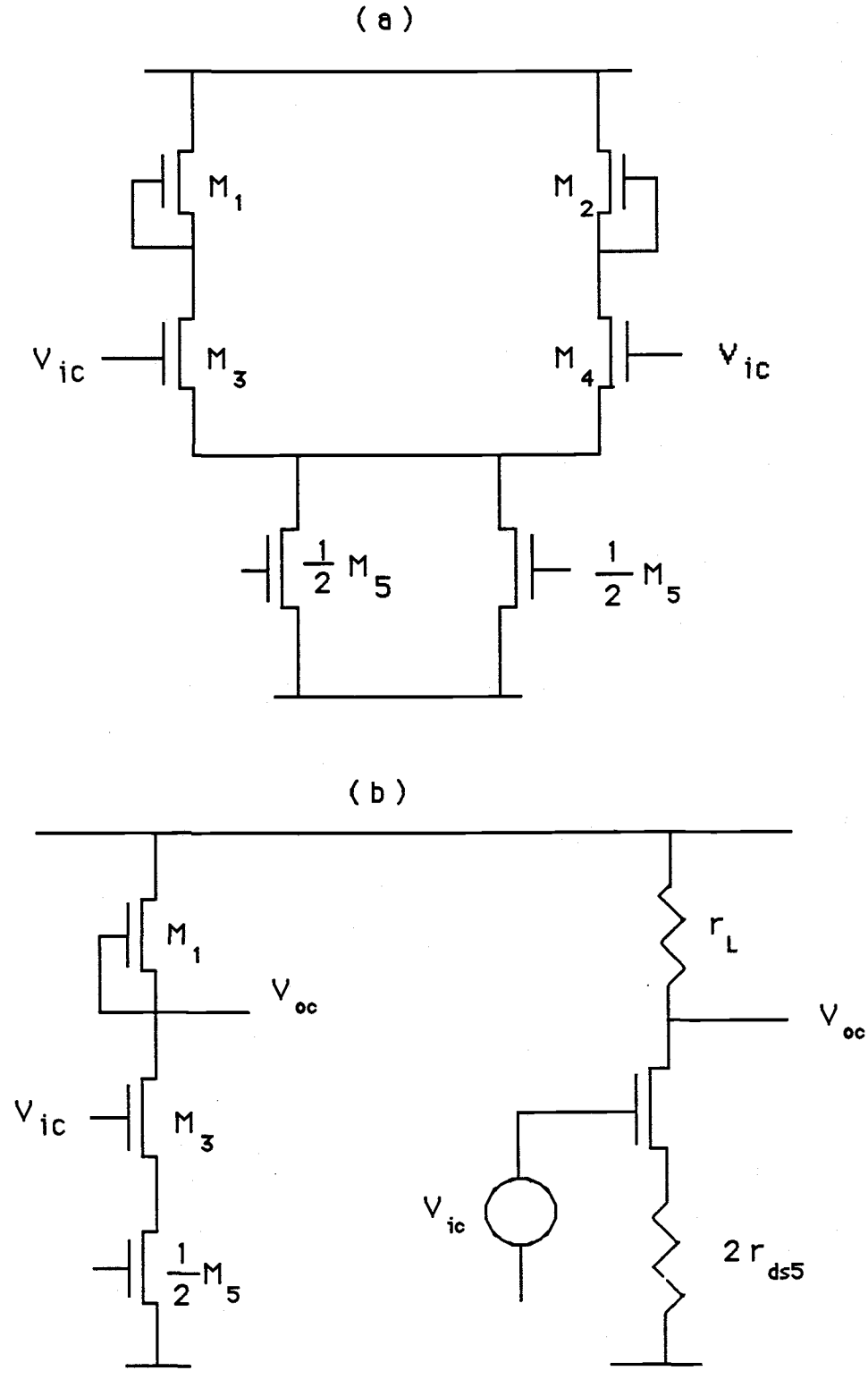

Fig. 11. (a) Common-mode circuit; (b) Common-mode half-circuit.

VI. RESULTS

The differential chopper-stabilized operational amplifier device sizes are shown in Table 1 and SPICE program is attached in the Appendix. The modeling circuit is well matched with the operational amplifier. The noise analysis and the frequency characteristics are shown in figs.12 - 17. To reduce the flicker noise, the differential amplifier is chopped at a frequency close to the corner frequency (60 KHz). The noise performance using the chopper stabilization is shown in figs. 18 and 19. The flicker noise is dominant in the operational amplifier without chopper operation, and the thermal noise is dominant with chopper operation. When the chopping frequency is close to the corner frequency, the equivalent input noise is reduced. By chopper stabilization, the equivalent input noise of the operational amplifier is reduced from -115 dB to -159 dB at 1 Hz. The common-mode range is 2V to 12V and common-mode rejection ratio is 78 dB (Fig. 20). The output voltage swing is 0.3 V to 12V using the advanced output stage (Fig. 21). Open-loop gain is 89

dB and loop gain is 40 dB. Details are presented in Table 2 and figures.

TABLE 1

DEVICE SIZE (W / L , um)

M_1	15/15	M_{16}	30/8
M_2	15/15	M_{17}	11/10
M_3	443/8	M_{18}	31/8
M_4	443/8	M_{19}	12/10
M_5	90/8	M_{20}	25/20
M_6	40/10	M_{21}	8/10
M_7	140/10	M_{C1}	30/6
M_8	140/10	M_{C2}	30/6
M_9	19/20	M_{C3}	30/6
M_{10}	19/20	M_{C4}	30/6
M_{11}	77/10	M_{C5}	26/6
M_{12}	102/8	M_{C6}	26/6
M_{13}	102/8	M_{C7}	26/6
M_{14}	37/10	M_{C8}	26/6
M_{15}	37/10		

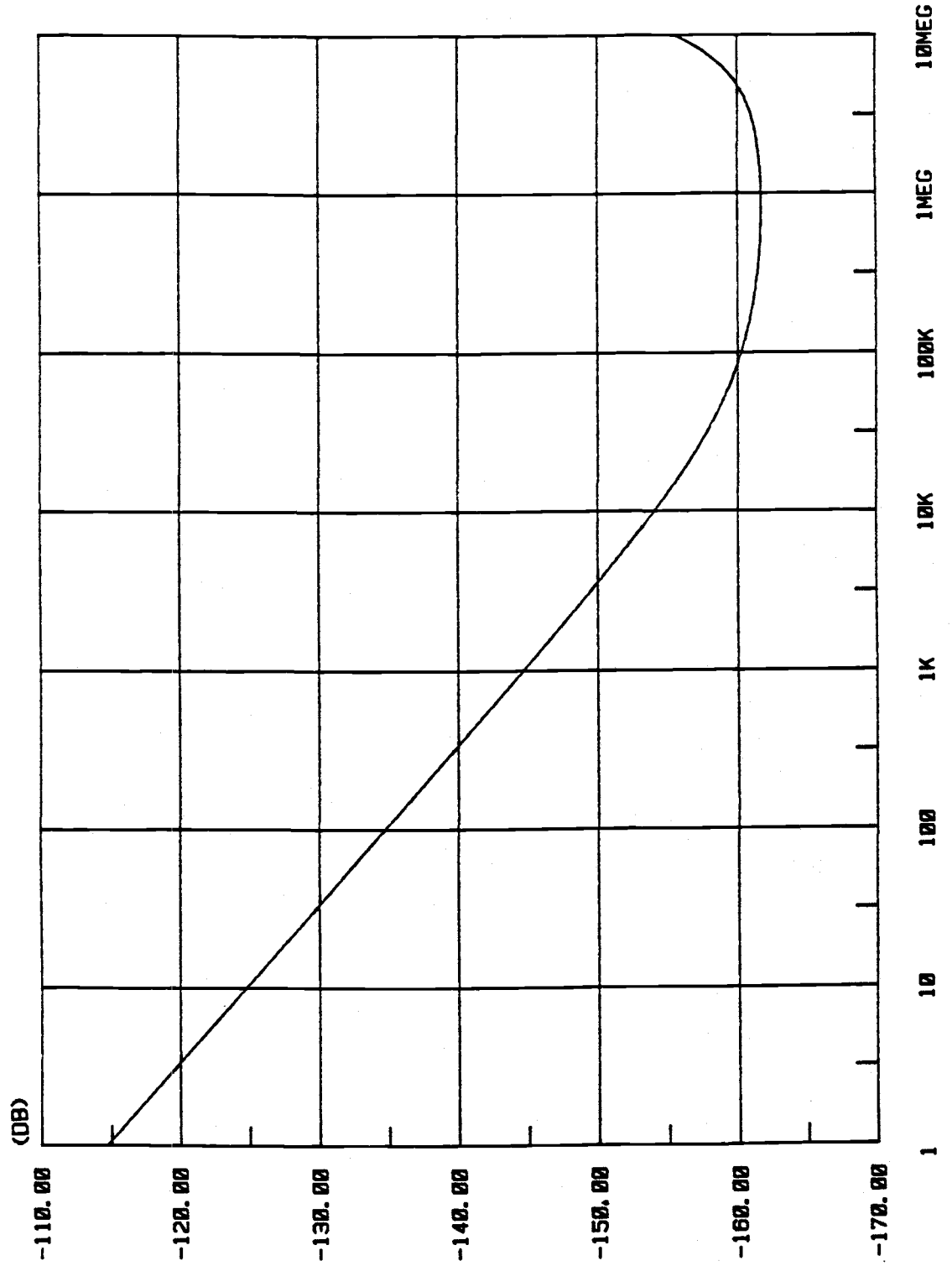

Fig. 12. Noise spectrum of operational amplifier.

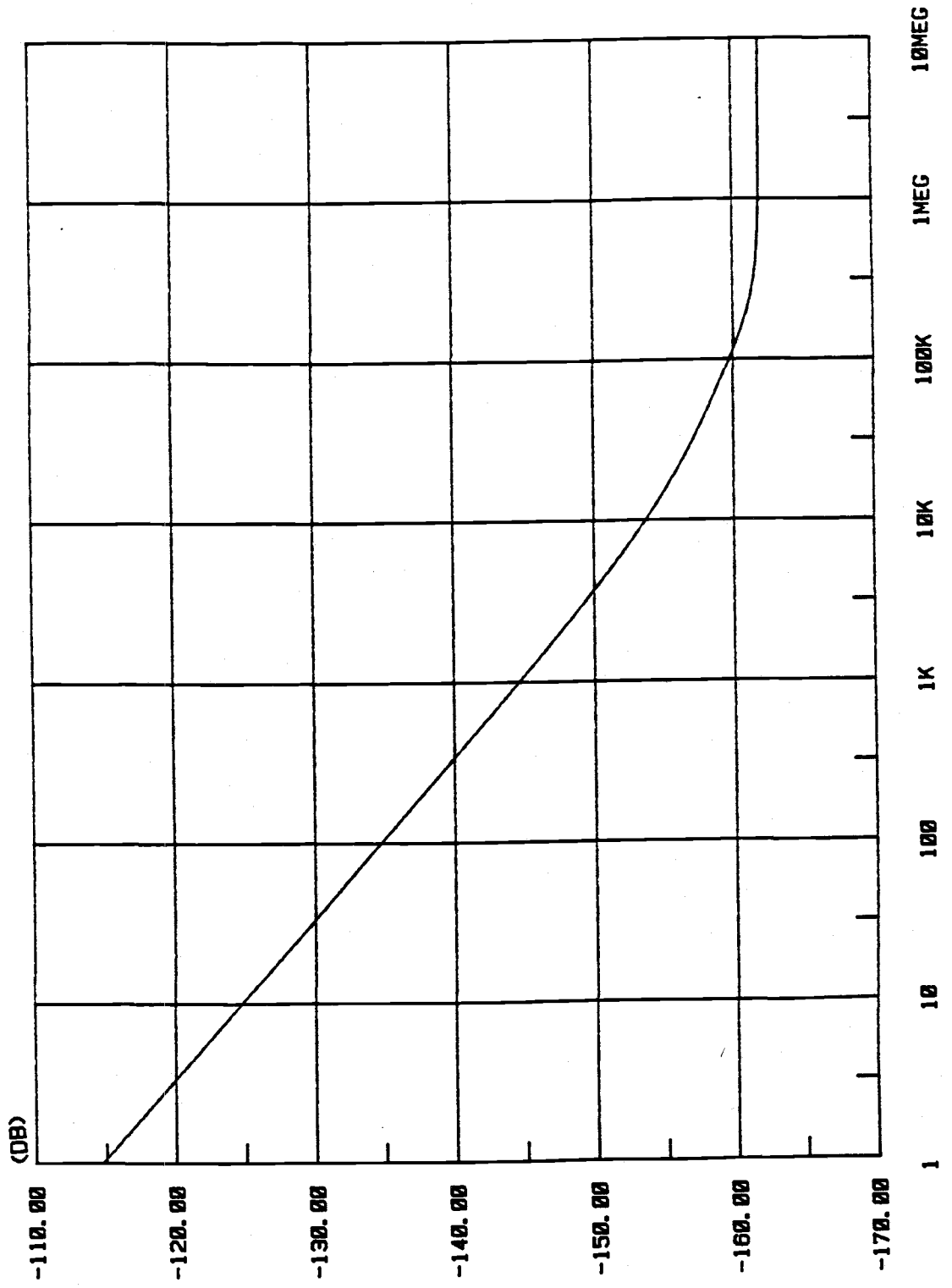

Fig. 13. Noise spectrum of modeling circuit.

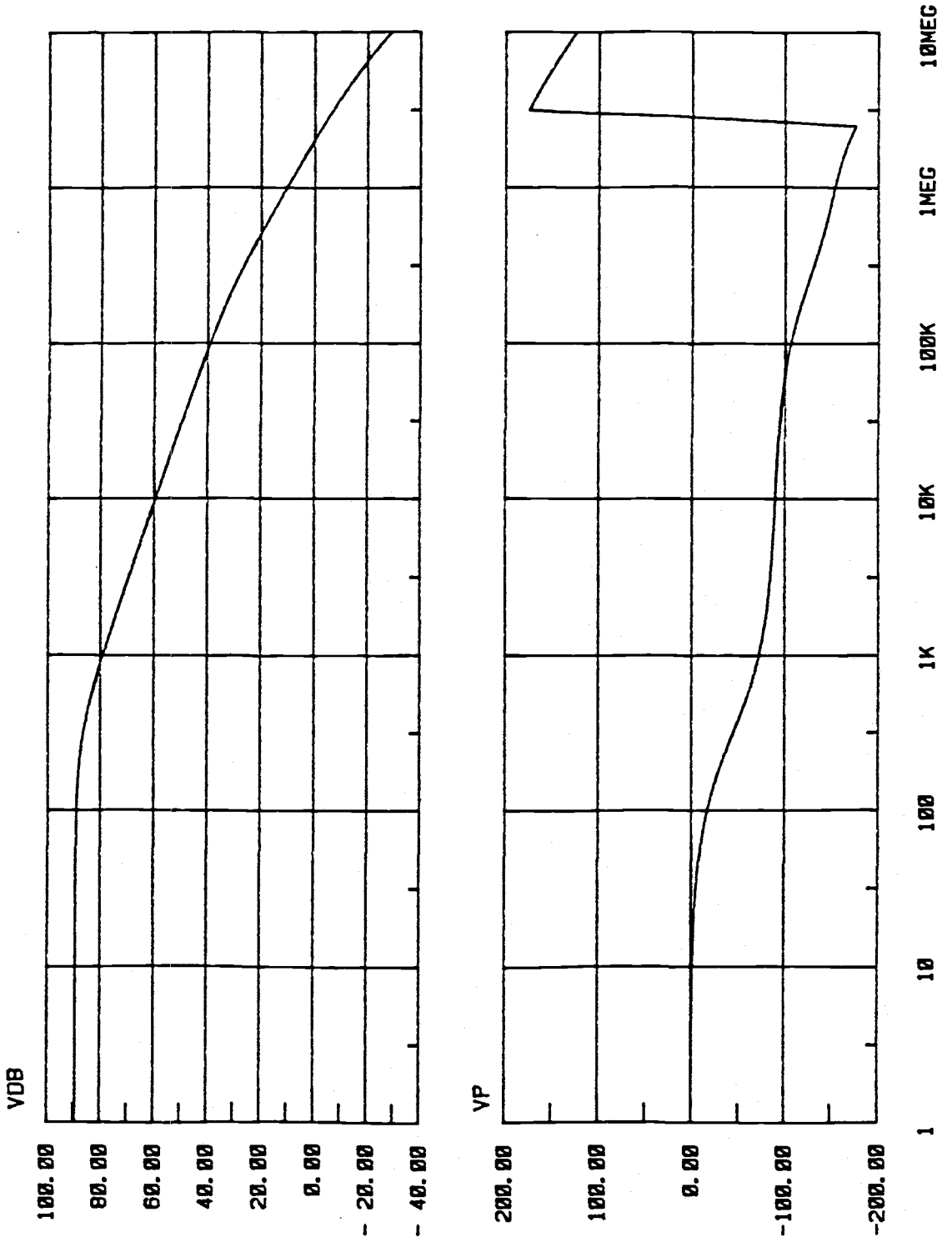

Fig. 14. Frequency characteristics of operational amplifier.

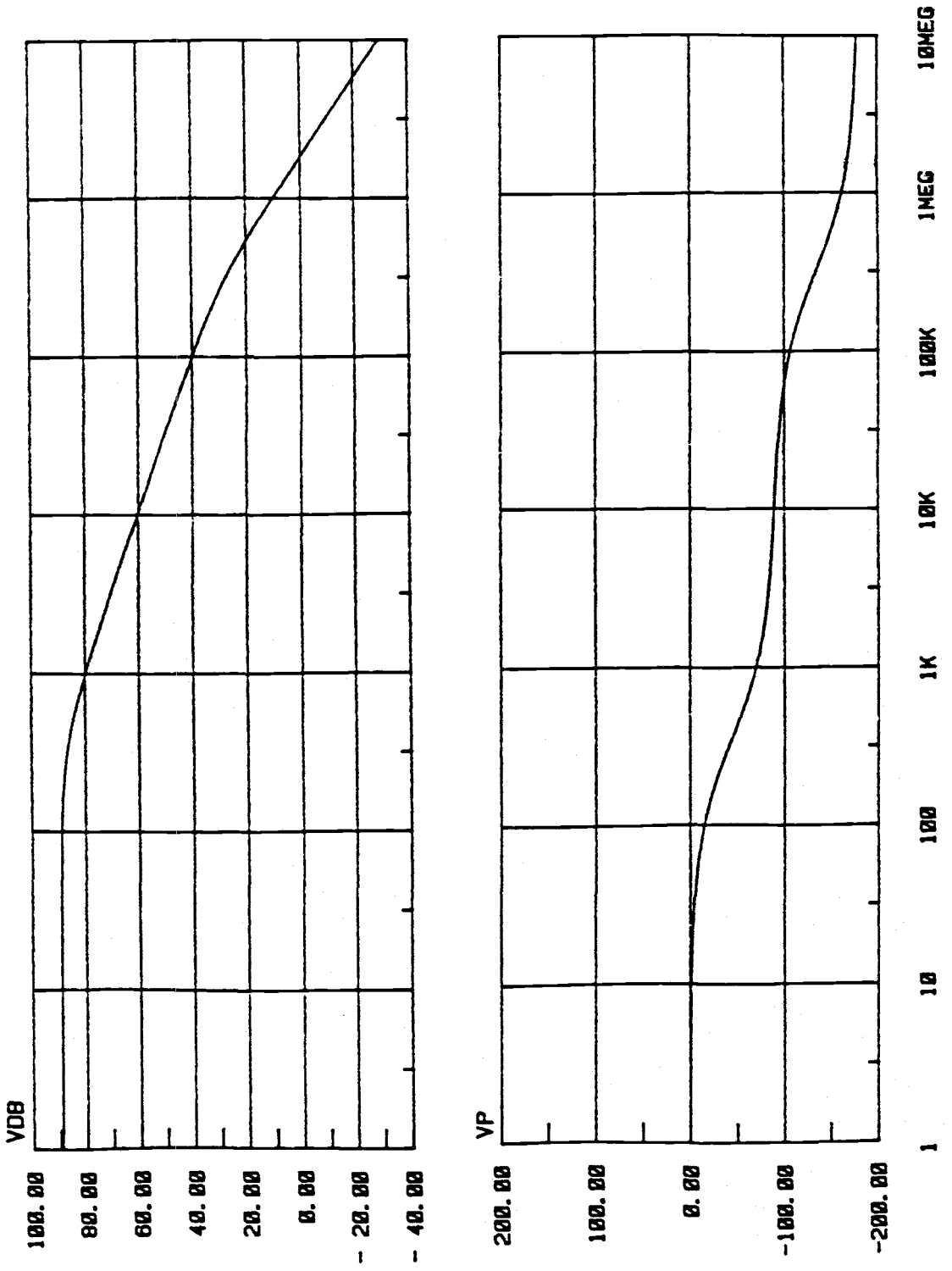

Fig. 15. Frequency characteristics of modeling circuit.

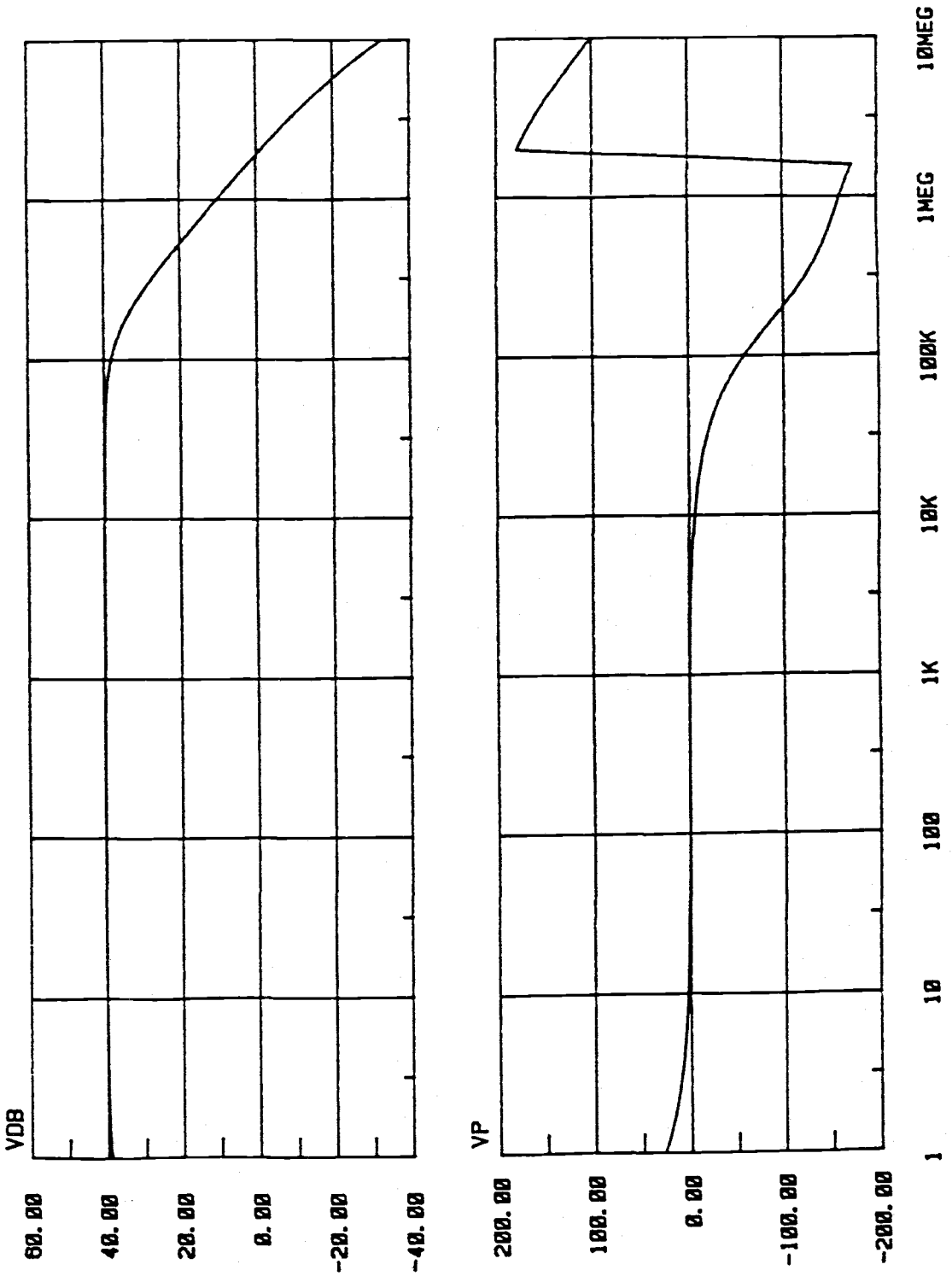

Fig. 16. Frequency chraracteriastics of operational amplifier with feedback circuit.

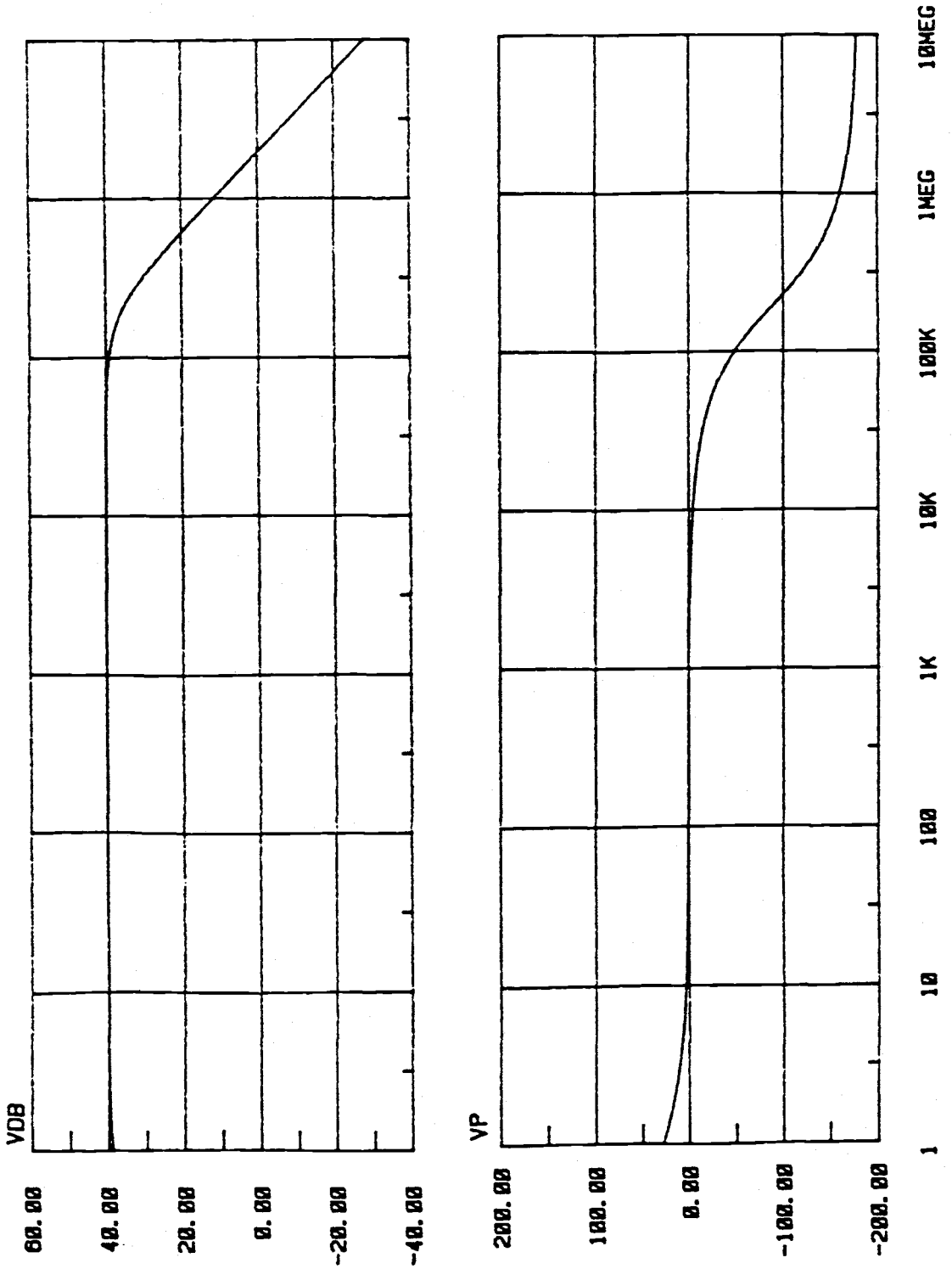

Fig. 17. Frequency characteristics of modeling circuit for feedback circuit.

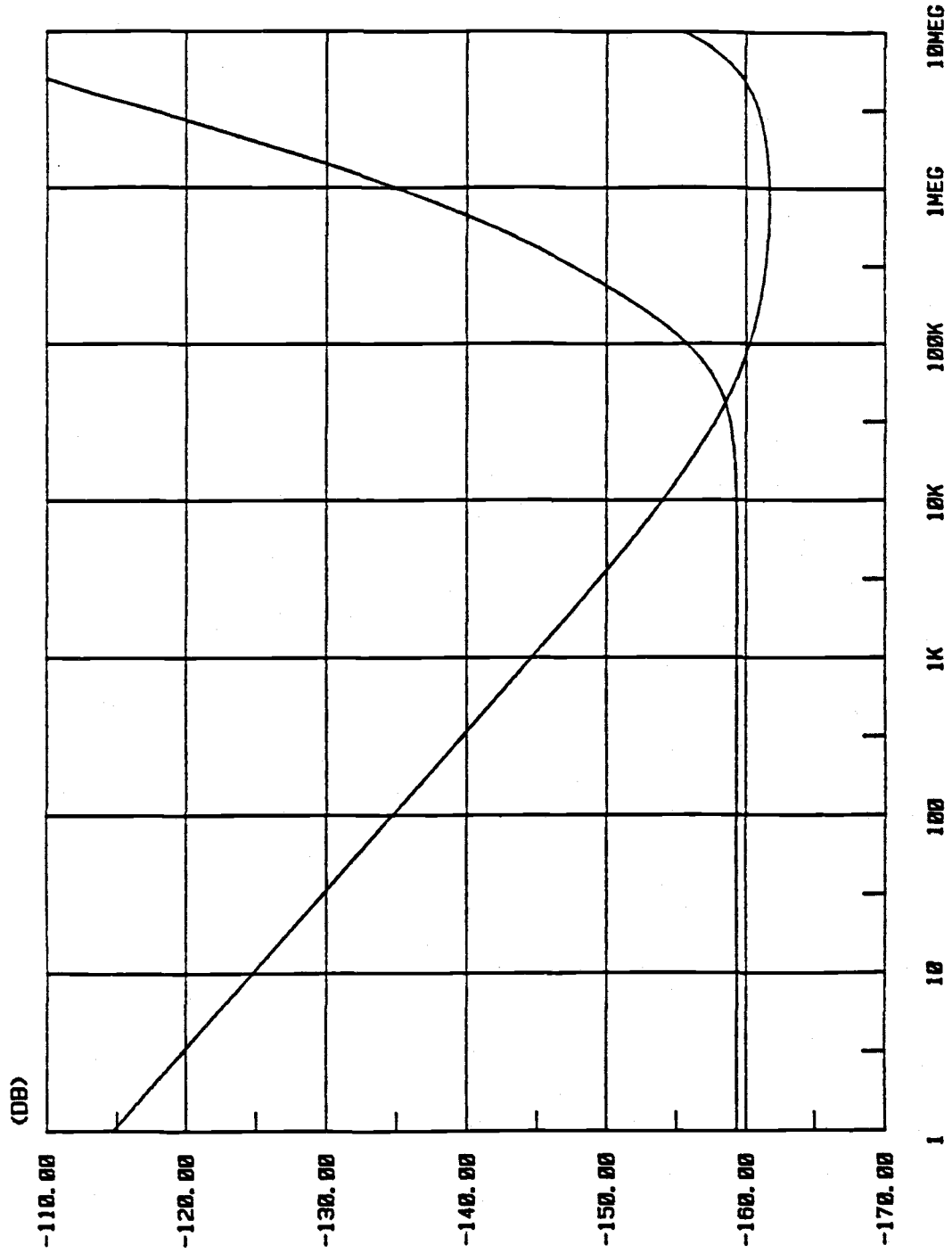

Fig. 18. Noise performance of chopper stabilization for operational amplifier.

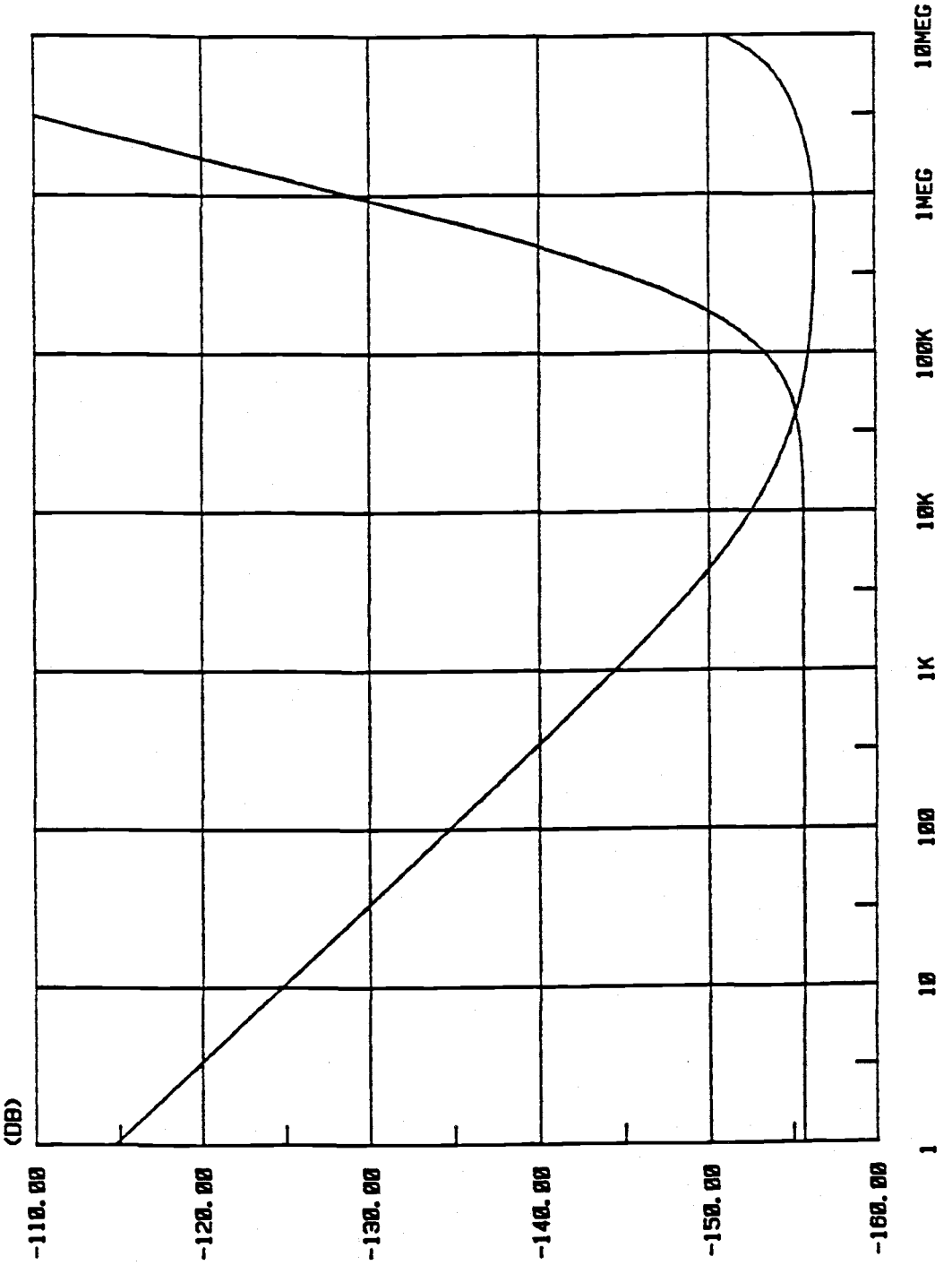

Fig. 19. Noise performance of chopper stabilization for operational amplifier with feedback circuit.

TABLE 2

Chopper amplifier performance summary

(f_{chop} = 60 KHz)

Parameters	Results
Power supply	0 -12 Volts
Open-loop gain	89 dB
CMRR	78 dB
Bandwidth(CL=220PF)	2.5 MHz
Power dissipation	6.96 mW
Output swing	0.3 - 12 Volts
Input common-mode range	2 - 12 Volts
Equivalent input noise (1 Hz)	
without chopper	-115 dB
with chopper	-159 dB

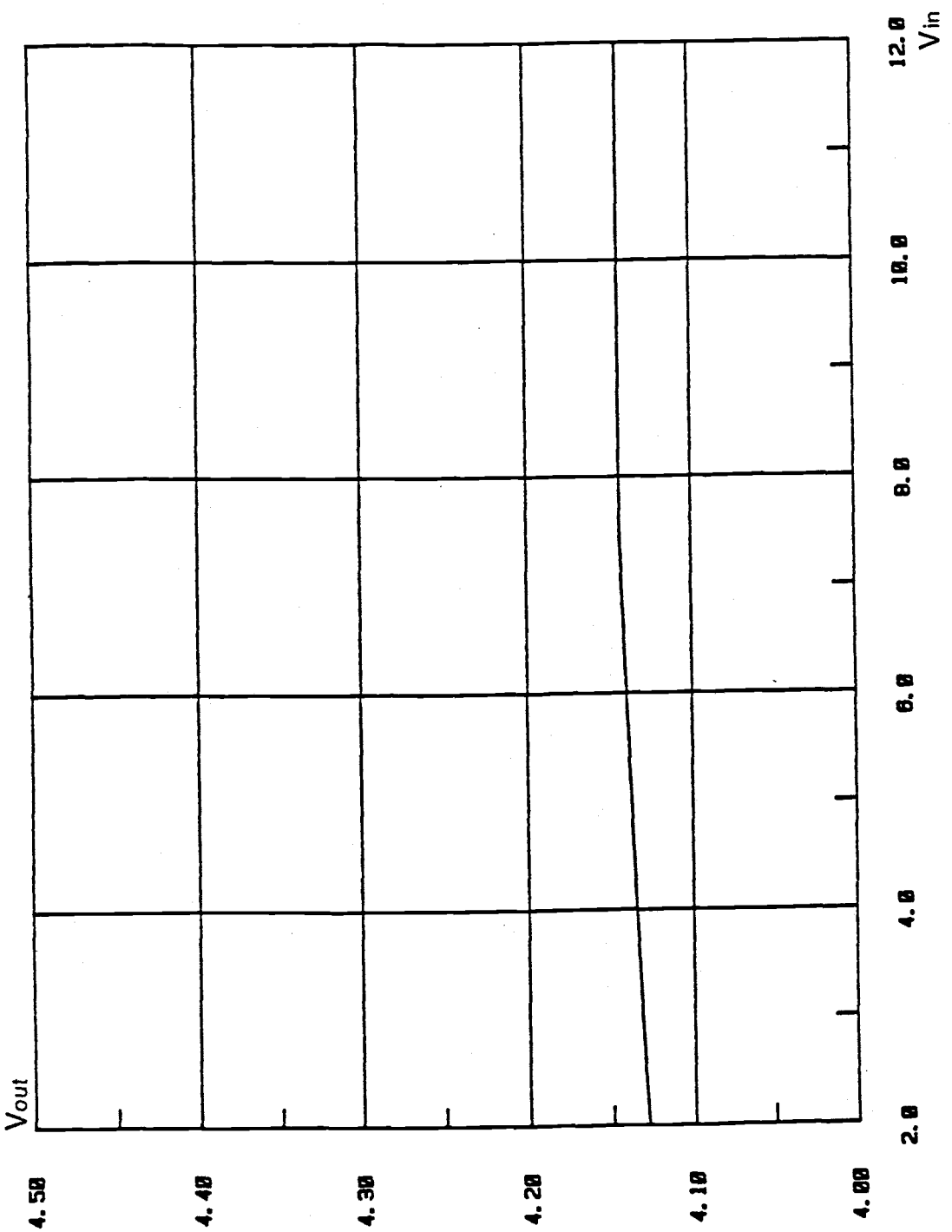

Fig. 20. Input common-mode characteristics.

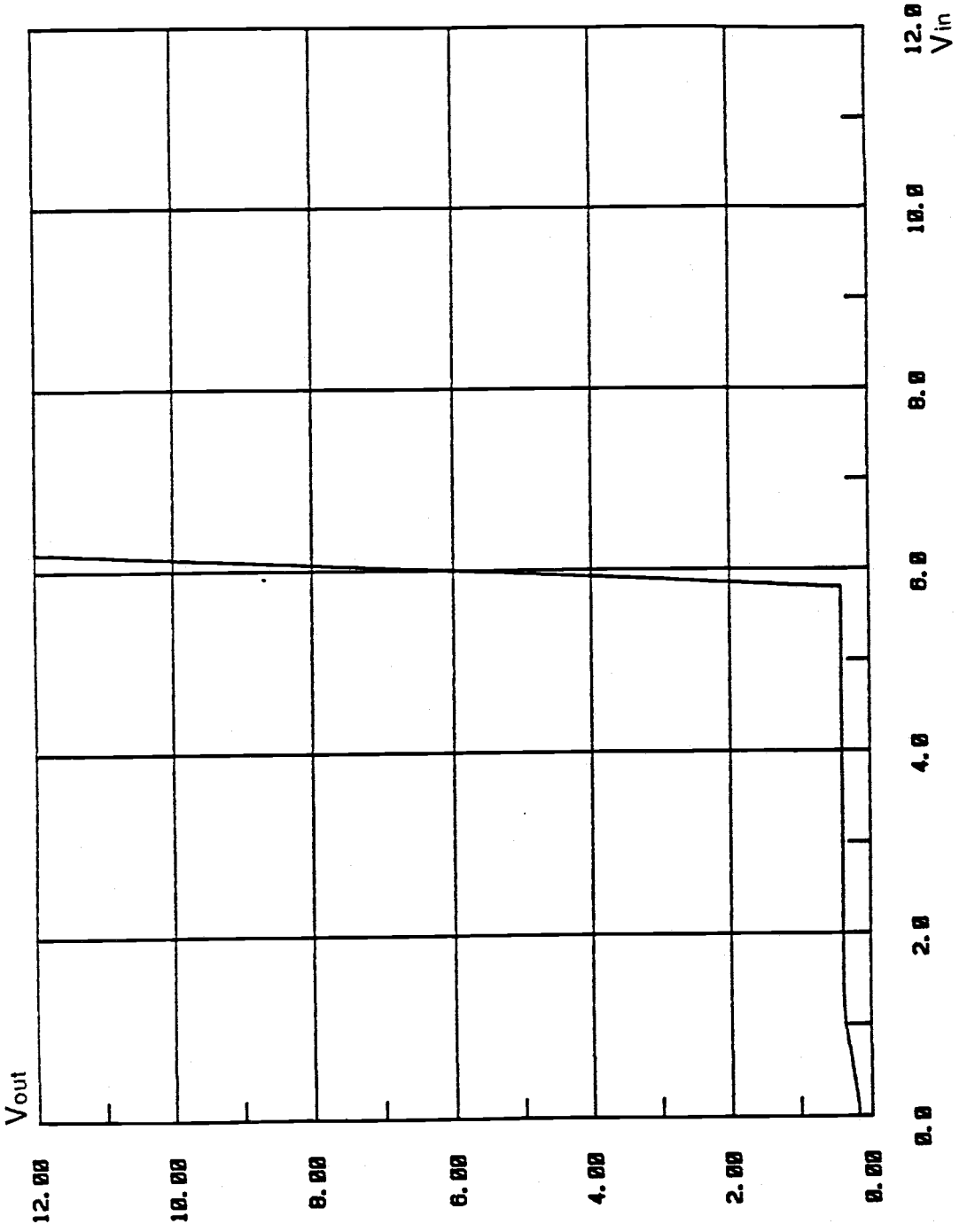

Fig. 21. Output voltage swing.

VII. CONCLUSION

A differential chopper-stabilized operational amplifier and its modeling circuit have been discussed. Even though the chopper stabilization reduces the flicker noise contribution to the total noise of the amplifier at low frequency, we previously could not verify this good performance by a simple method. Since the modeling circuit is well matched with the expected results, it is a reasonable application method to use the modeling circuit to analyze the chopper-stabilized amplifier. To minimize the contribution of the flicker noise to the chopper amplifier residual noise, the chopper frequency is close to the amplifier corner frequency. The implemented chopper amplifier has high dc gain, high output voltage swing and good low frequency characteristics. The equivalent input noise is equal to 12 nV/$\sqrt{Hz}$ at a frequency of 1Hz.

REFERENCES

[1] C. C. Enz et al., "A CMOS chopper amplifier," IEEE J. Solid-State Circuits, Vol. SC-22, No. 3, pp. 335-342, June 1987.

[2] K. C. Hsieh et al., "A low-noise chopper-stabilized differential switched-capacitor filtering technique," IEEE J. Solid-State Circuits, Vol. SC-16, No. 3, pp. 708-715, DEC. 1981.

[3] J. H. Fisher, "Noise source and calculation techniques for switched capacitor filters," IEEE J. Solid-State Circuits, Vol. SC-17, No. 4, pp. 258-268, Aug. 1982.

[4] D. A. Hodges and H. G. Jackson, Analysis and design of digital integrated circuits, : McGraw Hill, 1985.

[5] N. Weste and K. Eshraghian, Principles of CMOS VLSI design, : Addison-Wesley, 1985.

[6] M. J. Buckingham, Noise in electronic devices and systems, England : Ellis Horwood, 1983.

[7] R. Gregorian and G. C. Temes, Analog MOS integrated circuits for signal processing, : Wiley-interscience, 1986.

[8] H. Mikoshiba, "1/f noise in n-channel silicon-gate MOS transitor," IEEE Trans. Electron Devices, Vol Ed-29, No. 6, pp. 965-970, June 1982.

[9] F. M. Klassen, "Characterization of low 1/f noise in MOS transistors," IEEE Trans. Electron Devices, pp. 887-891 Oct. 1971.

[10] E. A. Vittoz, "MOS transitor operated in the lateral bipolar mode and their application in CMOS technology," IEEE J. Solid-State Circuits, Vol. SC-18, No. 3, pp. 273-279, June 1983

[11] H. Momose et al., "1.0-um n-well CMOS/Bipolar technology," IEEE J. Solid-State Circuits, Vol. SC-20, No.1, pp. 137-143, Feb. 1985.

[12] P. R. Gray and R. G. Meyer, Analysis and design of analog integrated circuits, : John Wiley & Sons,1984.

[13] J. A. Fisher, "A high performance CMOS power amplifier," IEEE J. Solid-State Circuits, Vol, SC-20, No. 6, pp. 1200-1205, Dec. 1985.

APPENDICES

A. Input Program of Amplifier

```
************************************
**SPICE INPUT PROGRAM OF AMPLIFIER**
************************************
VDD 1 0 12
VIN 6 0 6.0000 AC 1
V5 5 0 5.9999
IR 2 0 10U
CL1 14 0 220PF
RF1 10 70 15K
CF1 70 14 15PF
VP1 31 0 12V
VP2 32 0 0V
**********************************************************************
**INPUT DEVICE**
**********************************************************************
M1   3 3 1 1      P15 W=15U   L=15U AD=135P  AS=135P  PD=33U   PS=33U
M2   4 4 1 1      P15 W=15U   L=15U AD=135P  AS=135P  PD=33U   PS=33U
M3   3 35 7 7     N08 W=443U  L=8U  AD=3987P AS=3987P PD=461U  PS=461U
M4   4 36 7 7     N08 W=443U  L=8U  AD=3987P AS=3987P PD=461U  PS=461U
M5   7 8 0 0      N08 W=90U   L=8U  AD=810P  AS=810P  PD=108U  PS=108U
M6   9 2 1 1      P10 W=40U   L=10U AD=360P  AS=360P  PD=58U   PS=58U
M7   11 34 9 9    P10 W=140U  L=10U AD=1260P AS=1260P PD=158U  PS=158U
M8   10 33 9 9    P10 W=140U  L=10U AD=1260P AS=1260P PD=158U  PS=158U
M9   11 11 0 0    N20 W=19U   L=20U AD=171P  AS=171P  PD=37U   PS=37U
M10  10 11 0 0    N20 W=19U   L=20U AD=171P  AS=171P  PD=37U   PS=37U
M11  12 2 1 1     P10 W=77U   L=10U AD=693P  AS=693P  PD=96U   PS=96U
M12  12 12 14 14  N08 W=102U  L=8U  AD=918P  AS=918U  PD=120U  PS=120U
M13  1 12 14 14   N08 W=102U  L=8U  AD=918P  AS=918U  PD=120U  PS=120U
M14  15 15 14 14  P10 W=37U   L=10U AD=333P  AS=333P  PD=55U   PS=55U
M15  0 15 14 14   P10 W=37U   L=10U AD=333P  AS=333P  PD=55U   PS=55U
M16  15 10 0 0    N08 W=30U   L=8U  AD=270P  AS=270P  PD=48U   PS=48U
M17  14 4 1 1     P10 W=11U   L=10U AD=99P   AS=99P   PD=29U   PS=29U
M18  14 10 0 0    N08 W=31U   L=8U  AD=279P  AS=279P  PD=49U   PS=49U
M19  8 2 1 1      P10 W=12U   L=10U AD=108P  AS=108P  PD=30U   PS=30U
M20  8 8 0 0      N20 W=25U   L=20U AD=225P  AS=225P  PD=43U   PS=43U
M21  2 2 1 1      P10 W=8U    L=10U AD=72P   AS=72P   PD=26U   PS=26U
MC1  6 31 36 36   N06 W=30U   L=6U  AD=270P  AS=270P  PD=48U   PS=48U
MC2  6 32 35 35   N06 W=30U   L=6U  AD=270P  AS=270P  PD=48U   PS=48U
MC3  5 31 35 35   N06 W=30U   L=6U  AD=270P  AS=270P  PD=48U   PS=48U
MC4  5 32 36 36   N06 W=30U   L=6U  AD=270P  AS=270P  PD=48U   PS=48U
MC5  3 31 33 33   N06 W=26U   L=6U  AD=234P  AS=234P  PD=44U   PS=44U
MC6  3 32 34 34   N06 W=26U   L=6U  AD=234P  AS=234P  PD=44U   PS=44U
MC7  4 31 34 34   N06 W=26U   L=6U  AD=234P  AS=234P  PD=44U   PS=44U
MC8  4 32 33 33   N06 W=26U   L=6U  AD=234P  AS=234P  PD=44U   PS=44U
**********************************************************************
**PMOS SPICE PARAMETERS**
**********************************************************************
.MODEL P15 PMOS(LEVEL=2 VTO=-.894654 KP=15.26452U GAMMA=.879
+TOX=50N UCRIT=16376.5 UEXP=.15344 XJ=.4U CJ=2E-4 CJSW=4.5E-10
+CGDO=.52N CGSO=.4N AF=1.25 KF=1.5E-27 NFS=8.78862E11 MJSW=.33
+NSUB=1.21088E14 UO=100 DELTA=1.93831 VMAX=1E5 NEFF=1.0001E-2
+MJ=.5 LAMBDA=9.41731E-3 LD=.28U TPG=-1 RSH=95 PHI=.6)
.MODEL P10 PMOS(LEVEL=2 VTO=-.894654 KP=1.526452E-5 GAMMA=.879
+TOX=50N UCRIT=16376.5 XJ=.4U LD=.28U CJ=2E-4 CJSW=.45N RSH=95
+CGDO=.52N CGSO=.4N AF=1.25 KF=1.5E-27 NFS=8.788617E11 TPG=-1
+LAMBDA=1.41259E-2 PHI=.6 UEXP=.153441 NEFF=1.001E-2 MJ=.5
```

```
+NSUB=1.121088E14 DELTA=1.93831 VMAX=1E5 MJSW=.33 UO=100)
.MODEL P08 PMOS(LEVEL=2 LD=.28U TOX=50N NSUB=1.121088E14
+VTO=-.894654 KP=1.526452E-5 LAMBDA=1.76574E-2 UEXP=.153441
+UO=100 UCRIT=16376.5 DELTA=1.93831 VMAX=1E5 XJ=.4U GAMMA=.879
+NFS=8.788617E11 NEFF=1.E-2 TPG=-1. RSH=95 CGSO=.4N CGDO=.52N
+CJ=2E-4 MJ=.5 CJSW=.45N MJSW=.33 AF=1.25 KF=1.5E-27 PHI=.6)
*****************************************************************
**NMOS SPICE PARAMETERS**
*****************************************************************
.MODEL N20 NMOS(LEVEL=2 VTO=.827125 KP=32.86649U GAMMA=1.3596
+TOX=50N UCRIT=999000 LD=.28U CJ=3.2E-4 CJSW=.9N RSH=25 XJ=.4U
+CGDO=.52N CGSO=.52N AF=1.25 KF=1.E-27 MJ=.5 MJSW=.33
+DELTA=1.2405 VMAX=1E5 NFS=1.234795E12 NEFF=1.001E-2 NSUB=1E16
+LAMBDA=2.40747E-3 PHI=.6 UO=200 UEXP=1.001E-3 TPG=1)
.MODEL N08 NMOS(LEVEL=2 VTO=.827125 KP=32.86649U GAMMA=1.3596
+TOX=50N UCRIT=999000 LD=.28U CJ=3.2E-4 CJSW=.9N RSH=25 XJ=.4U
+CGDO=.52N CGSO=.52N KF=1.E-27 AF=1.25 MJ=.5 MJSW=.33
+NSUB=1.E16 DELTA=1.2405 NFS=1.234795E12 NEFF=1.001E-2 TPG=1.
+LAMBDA=6.01868E-3 PHI=.6 UO=200 UEXP=1.001E-3 VMAX=1E5)
.MODEL N06 NMOS(LEVEL=2 VTO=.827125 KP=32.86649U GAMMA=1.3596
+TOX=50N UCRIT=999000 LD=.28U CJ=3.2E-4 CJSW=.9N RSH=25 XJ=.4U
+CGDO=.52N CGSO=.52N AF=1.25 KF=1.E-27 MJ=.5 MJSW=.33
+NSUB=1.E16 DELTA=1.2405 NFS=1.234795E12 NEFF=1.001E-2 TPG=1.
+LAMBDA=8.02491E-3 PHI=.6 UO=200 UEXP=1.001E-3 VMAX=1E5)
.MODEL N10 NMOS(LEVEL=2 VTO=.827125 KP=32.86649U GAMMA=1.3596
+TOX=50N UCRIT=999000 LD=.28U CJ=3.2E-4 CJSW=.9N RSH=25
+CGDO=.52N CGSO=.52N AF=1.25 KF=1.E-27 MJ=.5 MJSW=.33 XJ=.4U
+NSUB=1.E16 DELTA=1.2405 NFS=1.234795E12 NEFF=1.001E-2 TPG=1
+LAMBDA=4.81494E-3 PHI=.6 UO=200 UEXP=1.001E-3 VMAX=1E5)
*****************************************************************
**OUTPUT PROGRAM**
*****************************************************************
.AC DEC 10 1HZ 10MEGAHZ
.NOISE V(14) VIN 10
.GRAPH NOISE INOISE(DB)
*.DC VIN 0 12 .2
*.GRAPH DC V(14) VIN
*.PLOT NOISE INOISE(DB)
.TF V(14) VIN
.OPTIONS GMIN=1E-10
*.NODESET V(14)=5.9999
.GR AC VP(14) VDB(14)
.OPTIONS NOMOD
*.OPTIONS LIMTIM=50
*.OPTIONS ITL4=2
.END
```

B. Input Program of Amplifier with Feedback Circuit

```
****************************************
**SPICE INPUT PROGRAM OF AMP(FEEDBACK)**
****************************************
VDD 1 0 12
VIN 21 0 6.0000 AC 1
IR 2 0 10U
CL1 14 0 220PF
RF1 10 70 15K
CF1 70 13 15PF
VP1 31 0 12V
VP2 32 0 0V
*********************
**FEEDBACK CIRCUIT**
*********************
R1 21 6 2200
R2 22 5 7500
R3 5 14 750K
R4 6 23 1E8
R5 23 0 510K
R6 1 23 510K
C1 23 0 22UF
C2 22 0 40UF
*****************
**INPUT DEVICE**
*****************************************************************************
M1   3 3 1 1      P15 W=15U   L=15U AD=135P   AS=135P   PD=33U   PS=33U
M2   4 4 1 1      P15 W=15U   L=15U AD=135P   AS=135P   PD=33U   PS=33U
M3   3 35 7 7     N08 W=443U  L=8U  AD=3987P  AS=3987P  PD=461U  PS=461U
M4   4 36 7 7     N08 W=443U  L=8U  AD=3987P  AS=3987P  PD=461U  PS=461U
M5   7 8 0 0      N08 W=90U   L=8U  AD=810P   AS=810P   PD=108U  PS=108U
M6   9 2 1 1      P10 W=40U   L=10U AD=360P   AS=360P   PD=58U   PS=58U
M7   11 34 9 9    P10 W=140U  L=10U AD=1260P  AS=1260P  PD=158U  PS=158U
M8   10 33 9 9    P10 W=140U  L=10U AD=1260P  AS=1260P  PD=158U  PS=158U
M9   11 11 0 0    N20 W=19U   L=20U AD=171P   AS=171P   PD=37U   PS=37U
M10  10 11 0 0    N20 W=19U   L=20U AD=171P   AS=171P   PD=37U   PS=37U
M11  12 2 1 1     P10 W=77U   L=10U AD=693P   AS=693P   PD=96U   PS=96U
M12  12 12 13 13  N08 W=102U  L=8U  AD=918P   AS=918U   PD=120U  PS=120U
M13  1 12 14 14   N08 W=102U  L=8U  AD=918P   AS=918U   PD=120U  PS=120U
M14  15 15 13 13  P10 W=37U   L=10U AD=333P   AS=333P   PD=55U   PS=55U
M15  0 15 14 14   P10 W=37U   L=10U AD=333P   AS=333P   PD=55U   PS=55U
M16  15 10 0 0    N08 W=30U   L=8U  AD=270P   AS=270P   PD=48U   PS=48U
M17  14 4 1 1     P10 W=11U   L=10U AD=99P    AS=99P    PD=29U   PS=29U
M18  14 10 0 0    N08 W=31U   L=8U  AD=279P   AS=279P   PD=49U   PS=49U
M19  8 2 1 1      P10 W=12U   L=10U AD=108P   AS=108P   PD=30U   PS=30U
M20  8 8 0 0      N20 W=25U   L=20U AD=225P   AS=225P   PD=43U   PS=43U
M21  2 2 1 1      P10 W=8U    L=10U AD=72P    AS=72P    PD=26U   PS=26U
MC1  6 31 36 36   N06 W=30U   L=6U  AD=270P   AS=270P   PD=48U   PS=48U
MC2  6 32 35 35   N06 W=30U   L=6U  AD=270P   AS=270P   PD=48U   PS=48U
MC3  5 31 35 35   N06 W=30U   L=6U  AD=270P   AS=270P   PD=48U   PS=48U
MC4  5 32 36 36   N06 W=30U   L=6U  AD=270P   AS=270P   PD=48U   PS=48U
MC5  3 31 33 33   N06 W=26U   L=6U  AD=234P   AS=234P   PD=44U   PS=44U
MC6  3 32 34 34   N06 W=26U   L=6U  AD=234P   AS=234P   PD=44U   PS=44U
MC7  4 31 34 34   N06 W=26U   L=6U  AD=234P   AS=234P   PD=44U   PS=44U
MC8  4 32 33 33   N06 W=26U   L=6U  AD=234P   AS=234P   PD=44U   PS=44U
```

```
**********************************************************************
**PMOS SPICE PARAMETERS**
**********************************************************************
.MODEL P15 PMOS(LEVEL=2 VTO=-.894654 KP=15.26452U GAMMA=.879
+TOX=50N UCRIT=16376.5 UEXP=.15344 XJ=.4U LD=.28U CJSW=4.5E-10
+CGDO=.52N CGSO=.4N AF=1.25 KF=1.5E-27 NFS=8.78862E11 MJSW=.33
+NSUB=1.21088E14 UO=100 DELTA=1.93831 VMAX=1E5 NEFF=1.0001E-2
+MJ=.5 LAMBDA=9.41731E-3 RSH=95 TPG=-1 CJ=2E-4 PHI=.6)
.MODEL P10 PMOS(LEVEL=2 VTO=-.894654 KP=1.526452E-5 GAMMA=.879
+TOX=50N UCRIT=16376.5 XJ=.4U LD=.28U CJ=2E-4 CJSW=.45N RSH=95
+CGDO=.52N CGSO=.4N AF=1.25 KF=1.5E-27 NFS=8.788617E11 TPG=-1
+LAMBDA=1.41259E-2 PHI=.6 UEXP=.153441 NEFF=1.001E-2 MJ=.5
+NSUB=1.121088E14 DELTA=1.93831 VMAX=1E5 MJSW=.33 UO=100)
.MODEL P08 PMOS(LEVEL=2 LD=.28U TOX=50N NSUB=1.121088E14
+VTO=-.894654 KP=1.526452E-5 LAMBDA=1.76574E-2 UEXP=.153441
+UO=100 UCRIT=16376.5 DELTA=1.93831 VMAX=1E5 XJ=.4U GAMMA=.879
+NFS=8.788617E11 NEFF=1.E-2 TPG=-1. RSH=95 CGSO=.4N CGDO=.52N
+CJ=2E-4 MJ=.5 CJSW=.45N MJSW=.33 AF=1.25 KF=1.5E-27 PHI=.6)
**********************************************************************
**NMOS SPICE PARAMETERS**
**********************************************************************
.MODEL N20 NMOS(LEVEL=2 VTO=.827125 KP=32.86649U GAMMA=1.3596
+TOX=50N UCRIT=999000 LD=.28U CJ=3.2E-4 CJSW=.9N RSH=25 XJ=.4U
+CGDO=.52N CGSO=.52N AF=1.25 KF=1.E-27 MJ=.5 MJSW=.33
+DELTA=1.2405 VMAX=1E5 NFS=1.234795E12 NEFF=1.001E-2 NSUB=1E16
+LAMBDA=2.40747E-3 PHI=.6 UO=200 UEXP=1.001E-3 TPG=1)
.MODEL N08 NMOS(LEVEL=2 VTO=.827125 KP=32.86649U GAMMA=1.3596
+TOX=50N UCRIT=999000 LD=.28U CJ=3.2E-4 CJSW=.9N RSH=25 XJ=.4U
+CGDO=.52N CGSO=.52N KF=1.E-27 AF=1.25 MJ=.5 MJSW=.33
+NSUB=1.E16 DELTA=1.2405 VMAX=1E5 NFS=1.234795E12 NEFF=1.E-2
+LAMBDA=6.01868E-3 PHI=.6 UO=200 UEXP=1.001E-3 TPG=1)
.MODEL N06 NMOS(LEVEL=2 VTO=.827125 KP=32.86649U GAMMA=1.3596
+TOX=50N UCRIT=999000 LD=.28U CJ=3.2E-4 CJSW=.9N RSH=25 XJ=.4U
+CGDO=.52N CGSO=.52N AF=1.25 KF=1.E-27 MJ=.5 MJSW=.33
+NSUB=1.E16 DELTA=1.2405 VMAX=1E5 NFS=1.234795E12 NEFF=1.E-2
+LAMBDA=8.02491E-3 PHI=.6 UO=200 UEXP=1.001E-3 TPG=1)
.MODEL N10 NMOS(LEVEL=2 VTO=.827125 KP=32.86649U GAMMA=1.3596
+TOX=50N UCRIT=999000 LD=.28U CJ=3.2E-4 CJSW=.9N RSH=25 XJ=.4U
+CGDO=.52N CGSO=.52N AF=1.25 KF=1.E-27 MJ=.5 MJSW=.33
+NSUB=1.E16 DELTA=1.2405 VMAX=1E5 NFS=1.234795E12 NEFF=1.E-2
+LAMBDA=4.81494E-3 PHI=.6 UO=200 UEXP=1.001E-3 TPG=1)
**********************************************************************
**OUTPUT PROGAM**
**********************************************************************
.AC DEC 10 1HZ 10MEGAHZ
.NOISE V(14) VIN 10
.GRAPH NOISE INOISE(DB)
*.DC VIN 0 12 .2
*.GRAPH DC V(14) VIN
*.PLOT NOISE INOISE(DB)
.TF V(14) VIN
.OPTIONS GMIN=1E-10
.NODESET V(14)=5.9999
.GR AC VP(14) VDB(14)
.OPTIONS NOMOD
*.OPTIONS LIMTIM=50
*.OPTIONS ITL4=2
.END
```

C. Input Program for Noise Analysis

```
************************************
**INPUT PROGRAM FOR NOISE ANALYSIS**
************************************
.SUBCKT NOIMO 8 12 15 16
*****************************************************************
.MODEL N10 NMOS(LEVEL=2 VTO=.827215 KP=32.86649U GAMMA=1.3596
+TOX=50N UCRIT=999000 LD=.28U CJ=3.2E-4 CJSW=.9N RSH=25 XJ=.4U
+NSUB=1.E16 DELTA=1.2405 VMAX=1E5 NFS=1.234795E12 NEFF=1.001E-2
+TPG=1. CGDO=.52N CGSO=.52N MJ=.5 MJSW=.33 AF=1.25 KF=7.50E-27)
*****************************************************************
VDD 1 0 6V
VSS 3 0 -6V
IR 1 2 40U
RN1 5 0 7625
RN2 5 0 7625
RF1 13 14 1
CF1 14 0 5.E-7
RF2 21 22 1
CF2 22 0 4.5E-4
M1 2 2 3 3 N10 L=10U W=90000U
RBLK 11 0 1
CBLK 10 9 1
E1 11 10 5 0 1
E2 9 8 2 0 1
E3 13 0 11 12 12
E4 21 0 14 0 2396
E5 15 0 22 0 1
E6 15 16 5 0 158
RO1 16 16 1
RO2 17 17 1
.ENDS NOIMO
************************
.SUBCKT CHOP 8 12 15 16
************************
VDD 1 0 6
VSS 3 0 -6
IR 1 2 40U
RN1 5 0 7625
RN2 5 0 7625
RF1 13 14 1
CF1 14 0 5.E-7
RF2 21 22 1
CF2 22 0 4.5E-4
M1 2 2 3 3 N10 L=10U W=90000U
RBK 11 0 1
E1 11 8  5 0 1.364
E3 13 0 11 12 12
E4 21 0 14 0 2396
E5 15 0 22 0 1
E6 15 16 5 0 158
RO1 16 16 1
*****************************************************************
.MODEL N10 NMOS(LEVEL=2 VTO=.827215 KP=32.86649 GAMMA=1.3596 MJ=.5
+TOX=50N UCRIT=999000 XJ=.4U LD=.28U CJ=3.2E-4 CJSW=.9N NEFF=1.E-2
+CGDO=.52N CGSO=.52N KF=7.50E-27 AF=1.25 NFS=1.234795E1 RSH=25
+NSUB=1.E16 DELTA=1.2405 VMAX=1E5 TPG=1 MJSW=.33)
```

```
**********************************************************************
.ENDS CHOP
********************
VIN 76 0 DC 0 AC 1
R5 75 75 1
V75 75 0 0
R78 78 78 1
R77 77 77 1
X1 76 75 77 78 CHOP
************************
.AC DEC 10 1HZ 10000KHZ
.GR AC VDB(78) VP(78)
.NOISE V(78) VIN 20
.OPTIONS GMIN=1E-10
*.NODESET V(76)=-.0001
.OPTIONS NOMOD
.GR NOISE INOISE(DB)
.END
```

D. Input Program for Noise Analysis with Feedback Circuit

```
**********************************************
**INPUT PROGRAM FOR NOISE ANALYSIS (FEEDBACK)**
**********************************************
.SUBCKT NOIMO 8 12 15 16
*********************************************************************
.MODEL N10 NMOS(LEVEL=2 VTO=.827215 KP=32.86649U GAMMA=1.3596
+TOX=50N UCRIT=999000 LD=.28U CJ=3.2E-4 CJSW=.9N RSH=25 XJ=.4U
+NSUB=1.E16 DELTA=1.2405 VMAX=1E5 NFS=1.234795E12 NEFF=1.001E-2
+TPG=1. CGDO=.52N CGSO=.52N MJ=.5 MJSW=.33 AF=1.25 KF=7.50E-27)
*********************************************************************
VDD 1 0 6V
VSS 3 0 -6V
IR 1 2 40U
RN1 5 0 7625
RN2 5 0 7625
RF1 13 14 1
CF1 14 0 5E-7
RF2 21 22 1
CF2 22 0 4.5E-4
M1 2 2 3 3 N10 L=10U W=90000U
RBLK 11 0 1
CBLK 10 9 1
E1 11 10 5 0 1
E2 9 8 2 0 1
E3 13 0 11 12 12
E4 21 0 14 0 2396
E5 15 0 22 0 1
E6 15 16 5 0 158
RO1 16 16 1
.ENDS NOIMO
************************
.SUBCKT CHOP 8 12 15 16
************************
VDD 1 0 6
VSS 3 0 -6
IR 1 2 40U
RN1 5 0 7625
RN2 5 0 7625
RF1 13 14 1
CF1 14 0 5E-7
RF2 21 22 1
CF2 22 0 4.5E-4
M1 2 2 3 3 N10 L=10U W=90000U
RBK 11 0 100MEGA
E1 11 8 5 0 1.364
E3 13 0 11 12 14
E4 21 0 14 0 2396
E5 15 0 22 0 1
E6 15 16 5 0 158
RO1 16 16 1
*********************************************************************
.MODEL N10 NMOS(LEVEL=2 VTO=.827215 KP=32.86649 GAMMA=1.3596 MJ=.5
+TOX=50N UCRIT=999000 XJ=.4U LD=.28U CJ=3.2E-4 CJSW=.9N NEFF=1.E-2
+CGDO=.52N CGSO=.52N KF=7.50E-27 AF=1.25 NFS=1.234795E1 RSH=25
+NSUB=1.E16 DELTA=1.2405 VMAX=1E5 TPG=1 MJSW=.33)
*********************************************************************
```

```
.ENDS CHOP
********************
VIN 86 0 DC 0 AC 1
CL 78 0 220PF
VDD 1 0 12V
R1 86 76 2200
R2 85 75 7320
R3 75 78 730K
R4 76 81 1E8
R5 1 81 510K
R6 81 0 510K
C1 81 0 20UF
C2 85 0 40UF
R78 78 78 1
R77 77 77 1
X1 76 75 77 78 CHOP
************************
.AC DEC 10 1HZ 10000KHZ
.GR AC VDB(78) VP(78)
.NOISE V(78) VIN 20
.OPTIONS GMIN=1E-10
*.NODESET V(76)=-.0001
.OPTIONS NOMOD
.GR NOISE INOISE(DB)
.END
```