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Title: Design of 28 GHz Low-Power Phased-Array Receiver Frontend in CMOS

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This work presents the design and implementation of a low power phased-array receiver frontend at 28 GHz in 65 nm CMOS. The frontend incorporates a low-power low-noise amplifier(LNA) and a passive reflection-type phase shifter (RTPS) capable of providing 360° phase shift with 5-bit phase resolution and low loss variation. Passive phase-shifters in the literature suffer from trade-offs between finite phase resolution, insertion loss and phase shift range, and hence do not provide 360° phase range with uniform, low loss across phase shift settings. The proposed systematic design and load optimization approach leads to the RTPS achieving state-of-art performance in terms of insertion loss with 360° phase shift range, loss variation across phase shift and rms phase error. The low-power LNA is based on a transformer-coupled neutralization architecture that increases gain in each LNA stage, allowing for lower power consumption.

The phased-array frontend is designed for Ka-band applications and has been characterized in 65nm CMOS from 26 GHz -30 GHz. The measured RTPS achieves 360° phase shift with -7.75±0.3 dB and rms phase error of 0.3° at 28 GHz. The low power phased-array receiver frontend has overall gain of 9.5 dB, gain variation of ∼0.4 dB and measured noise figure of 4.9 dB at 28 GHz. The receiver frontend consumes 10 mW from a 0.9 V supply with phase shifter and LNA active area of

0.16 mm^2 and 0.32 mm^2 respectively in 65nm CMOS, demonstrating its suitability for integration into low-power phased array receivers for emerging high data rate 5G wireless communication applications at 28 GHz.

Design of 28 GHz Low-Power Phased-Array Receiver Frontend in CMOS

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

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I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Robin Garg, Author

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Chapter 1: Introduction

In modern day high-speed wireless communications, the data rate requirements have boomed, and consequently operating frequencies of wireless systems have increased to mmWave range to accommodate for higher bandwidths and to provide better quality of transmission. Furthermore, the mmWave IC design techniques have enabled the use of multiple-array systems due to compact antenna size and inter-elemental spacing. Multiple antenna systems are capable of achieving higher SNR requirement and data rates while providing higher isotropic radiated power. Modern day radar techniques provide with electronically controllable beam-forming systems, which is instrumental in ensuring real time beam steering with flexibility [1].

High resolution and wide-bandwidth short range automotive radar systems have been assigned 22 GHz-29 GHz frequency band. There is great amount of interest in the research community about 5th generation(5G) mobile networks, also known as 5G systems, which is expected to be allocated bandwidth around 28 GHz. While modern day automotive radar systems find applications in blind-spot detection, lane departure warning etc, the 5G systems are expected to revolutionize the cellular communication by increasing data rates several times the existing rates and will enable high resolution video conferencing, enhanced gaming experience on cell phones. Concept of multiple antenna systems find applications in automotive radar and the 5G system design, where beam-forming is helpful in tracking/communicating of multiple targets accurately and providing high date rates with high quality. In section 1.1 we will discuss the special type of multiple antenna systems known as phased-array systems.

1.1 Introduction to Phased-array Systems

Phased-array receivers as shown in Fig. 1.1, are special type of multiple antenna systems which behave like directional antennas that can be steered electronically for beam-forming. While many spatial arrangements of the antennas are possible in these systems, the 1-dimensional antenna configuration has been analyzed in this section. It can easily be deduced from the Fig. 1.1 that the spatially separated antennas receive the radiated signals at different times [2]. As the signal combining takes place in the RF path, it will be shown that the coherence of received signal is of utmost importance in phased-array receivers.

Equations governing the beamsteering in phased-array receiver: For a N-element, 1-D phased-array as shown in (1.1), assuming the d to be the spatial distance two array elements and θ_{in} to be the angle of incidence, (1.1) shows the relationship between d, θ and time delay of arrival, τ [2].

$$\tau = d\left(\frac{sin(\theta_{in})}{c}\right) \tag{1.1}$$

Where c is the speed of light. Assuming that the $a(t)$, $\phi(t)$ and w_c are the received signal instantaneous amplitude, phase and frequency respectively, we can write for the kth element of the array:

$$A_k(t) = a(t - k\tau)cos(w_c t - kw_c\tau + \phi(t - k\tau)) \tag{1.2}$$

From (1.2), it can be inferred that the coherent combining of the signal can achieve maximum possible voltage output as given in (1.3). However, to achieve $A_{sum,max}$ there is a need for adjustable delay elements in the RF path. An ideal delay element in the RF path exhibits characteristics of infinite bandwidth, zero loss, low phase resolution and high uniform loss.

$$A_{sum,max} = Na(t)cos(w_c t + \phi(t)) \tag{1.3}$$

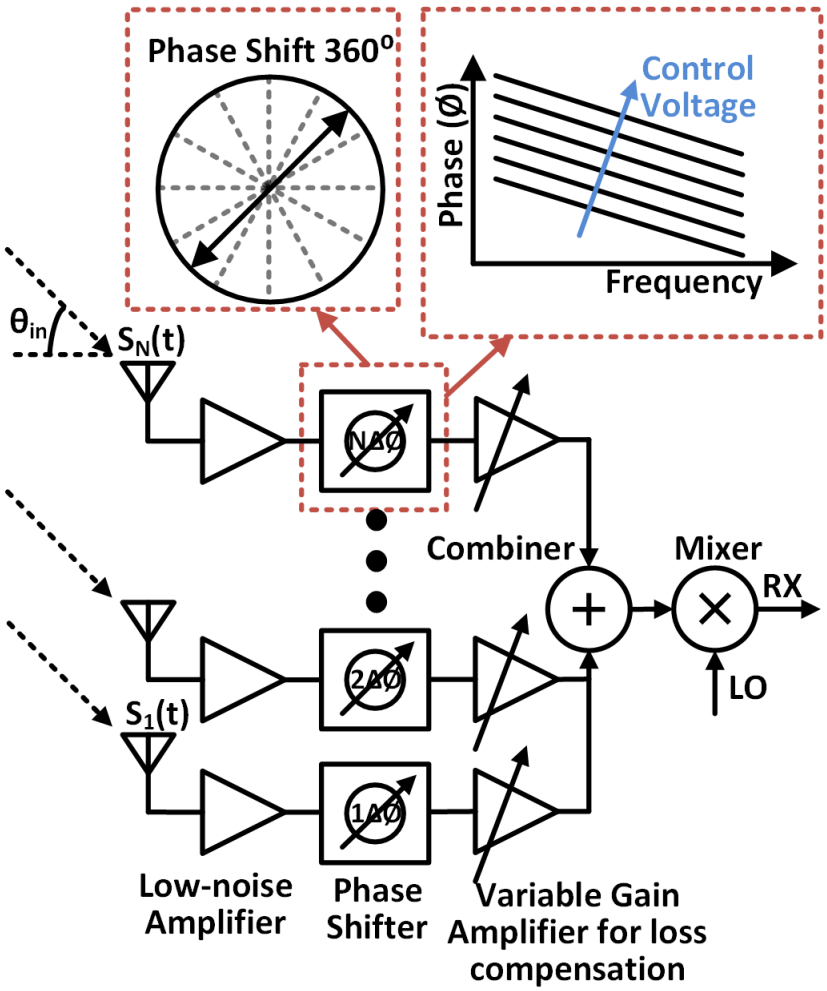

Figure 1.1: Phased-array receiver architecture and desired phase shifter characteristics

The requirement of infinite bandwidth can be relaxed under the narrow-band signal assumption, because it can be safely assumed that a(t) remains relatively constant for a small change is τ and :

$$a(t) \sim a(t - k\tau) \tag{1.4}$$

Similarly, it can be shown that with N-element linear phase array receiver the SNR improves by a factor of N and consequently the receiver sensitivity improves by $10log(N)$. Additionally, the inherent directional filtering reduces the interference power in the receiver [2].

The above mentioned properties of the phased-array receivers make their use lucrative in building systems with high sensitivity and SNR and high data rates. In section 1.2, the requirements and limitations of the phased-array will be discussed.

1.2 Applications of Phased-array Receivers

Phased-array receivers (RX) as shown in Fig. 1.1 are a subset of multiple antenna systems that enable electronically-steerable beam-forming, thereby providing higher effective isotropic radiated power in transmitters and improved SNR in receivers [3, 4]. The availability of large spectrum at mm-wave and the increasing interest in 5G applications has led to research on integrated phased arrays for the past decade with initial array demonstrations at 24 GHz and 77 GHz [3, 5–7] translating to large, scalable arrays at mm-wave frequencies such as 60 GHz [8] and 94 GHz [9, 10]. Given the interest in applying such arrays to high-data rate mobile communications in 5G networks [11], the array RX must provide SNR improvements, while simultaneously achieving low power consumption, sufficient gain and low NF. In particular, large-scale arrays in massive MIMO applications [12] require even lower power consumption in each individual element. This has led to increasing implementations of RF-path phase shifting since it promises the lowest area and power consumption.

1.3 Motivation

The critical building block in the RF-path phase shifted array RX is the variable phase shifter (VPS) that compensates for the phase shift introduced due to the time difference of arrival of signal at different elements. In order to ensure coherent combining across all angles of incidence, the VPS must provide 360° phase-shift range. In addition, since the VPS is in the signal path, it must achieve low insertion loss, high linearity and low power consumption. State-of-the-art mm-wave VPS approaches include vector-modulator (VM) based active [10, 13–15] and reflection-type phase shifter (RTPS) [16] & switched-transmission line phase-shifter (STPS) [17] type passive phase shifters. The inherent linearity and zero power consumption of passive VPS make them attractive - however, passive VPS must ensure (a) small area, (b) uniform loss across phase shift to prevent beam pattern degradation and/or eliminating the need for a variable-gain block preceding or succeeding it and (c) high phase-shift resolution to ensure accurate beam-forming [1].

In this work, we present a systematic approach to optimize the performance of a mm-wave RTPS targeting full 360° phase shift with 5-bit phase resolution at 28 GHz. With this approach, we achieve 7.75 $\pm$.3 dB insertion loss in a commercial 65 nm CMOS process at 28 GHz while achieving 5-bit phase resolution, demonstrating the feasibility of our approach while achieving targeted phase shift range. A single channel prototype of low-power receiver frontend consisting of a 3-stage single ended neutralization LNA and RTPS has also been demonstrated targeting 5G applications. The overall gain of the 10 mW frontend working on 0.9 V supply is 9.5$\pm$0.4 dB and the measured noise figure is 4.9 dB at 28 GHz.

1.4 Organization of Thesis

Chapter 2 details active and passive VPS and the design challenges involved, and finally placing this work in the context of state of the art. The proposed approach to overcome non-uniform phase shifter loss and achieve 360° phase shift range with low loss is described in Chapter 3. A specific implementation of the receiver

frontend at 28 GHz in a 65 nm CMOS process using the approaches is described in Chapters 3 & 4 respectively. Measurement results is presented in Chapter 5, along with a comparison of the proposed VPS with current state of the art. Finally, conclusion and future avenues of research are highlighted in Chapter 6.

Chapter 2: Overview of Phased Array Receiver Frontend

Phased-array receiver consisting of LNA, RF phase shifters, combiner and down-conversion mixer has been discussed in Chapter 1, while establishing the desired characteristics of a phase shifter. This work mainly focuses on the demonstration of the frontend of a receiver chain, i.e. LNA and phase shifter design, with proposed design technique for the state-of-the-art RTPS capable of providing 360° phase shift, with low and relatively constant insertion loss. In this chapter we discuss the existing state-of-the-art VPS design approaches and results.

2.1 Active and Passive Phase-Shifting Array RX Architectures

As mentioned in Chapter 1, state-of-the-art mm-wave VPS approaches include VM-based active and STPS/RTPS type passive phase shifters. Building on the critical design parameters discussed in Chapter 1, detailed analysis of the limitations of the state-of-the-art VPS will be performed in the Sections 2.2, 2.3 & 2.4, to develop possibilities for improved phase-shifter performance.

2.2 Vector Modulator Based Active Phase Shifters

Typical architecture of an active phase shifter (APS) employing vector modulator architecture to achieve the desired phase shift of 360° is shown in Fig. 2.1 [18]. The system consists of 4-stages, where signal transverses through the I/Q splitter based on quadrature coupler, differential Variable Gain Amplifier (VGA) stage, the signal combining stage and a buffer drives the output. VGA gains can be controlled independently by the DAC logic. Desired phase shift at the output is achieved by weighted sum of the I/Q signals. Being a passive stage the first stage effectively attenuates the signal while providing the I/Q outputs, ensuring the need

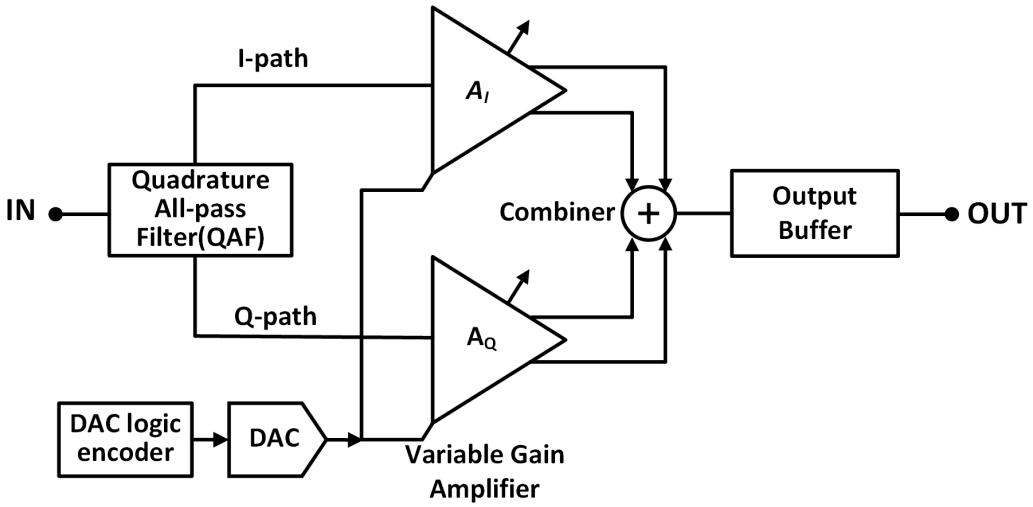

Figure 2.1: Architecture of vector modulator based active phase shifter

of a VGA. The overall system can be set to gain ≥ 0 dB by setting the appropriate VGA control voltage.

VM based VPS provide high gain but are often considered to be unattractive given their unidirectional nature, higher power consumption and poor linearity performance. High power consumption makes it less preferable to implement APS in battery operated hand-held devices and low power applications. The issue becomes even more significant in large-element phased-array receivers where multiple APS operate at the same time before the signal combining stage. State-of-the-art VM is reported to have current consumption of 11 mA per channel, excluding the combiner circuit, for 0 dB gain at 24 GHz in 0.13 μm CMOS [19].

2.3 Passive phase shifters for RF/mmWave beamforming

Passive phase shifters provide high linearity apart from zero DC power consumption and are hence attractive for integrated arrays targeted at consumer applications. Integrated passive VPS can be broadly divided into two classes - STPS [17] Fig. 2.2 and RTPS [16] Fig. 2.4. In the following sections we will discuss the two

types of passive VPS.

2.3.1 Switched t-line based phase shifters

STPS as shown in Fig. 2.2, is capable of switching to either of the two transmission lines of different lengths connected between the input and output ports, thus providing an electronically controllable phase change. Alternatively, phase shifting can be achieved with high-pass/low-pass select T-network, which advances or delays the phase depending on the mode selection. The STPS can be represented as a chain of phase shifters, where each stage has a well-defined phase shift resolution and insertion/switch loss associated with it. While cascading of these individual phase shifters allows the system to achieve the desired phase shift and phase resolution, the system insertion loss increases as the number of stage increase.

The improving f_T and switch time-constant for CMOS transistors has translated to low loss in STPS (6.1-7.6 dB at 60 GHz [20], 5.6 dB - 7.6 dB at 28 GHz [11]) - however, the resolution of a STPS is limited by the number of switches in the signal path (Fig. 2.2). Therefore, achieving high resolution (5-bit) implies higher path loss and larger area [21]. In addition to the low insertion loss, the STPS design approach must balance switch losses such that different switch states lead to uniform loss across all phase shift settings. It is worth to note that the reported STPS in [11] suffers from low bandwidth (850 MHz), high rms phase error of 8.98° and loss variation of 2 dB.

2.3.2 Reflection-type Phase Shifters(RTPS)

Second major approach to achieve bi-directional passive phase shifters is RTPS based on coupled transmission lines (t-line) shown in Fig. 2.5(a). As the name suggests, the RTPS works fundamentally on the concept of reflection at open or short load connected to a 50 Ω t-line. A coupled t-line connected to a variable reflective load generates different values of reflection coefficients Γ_T, this fact is utilized in many applications to build power splitters, balanced mixers, balanced

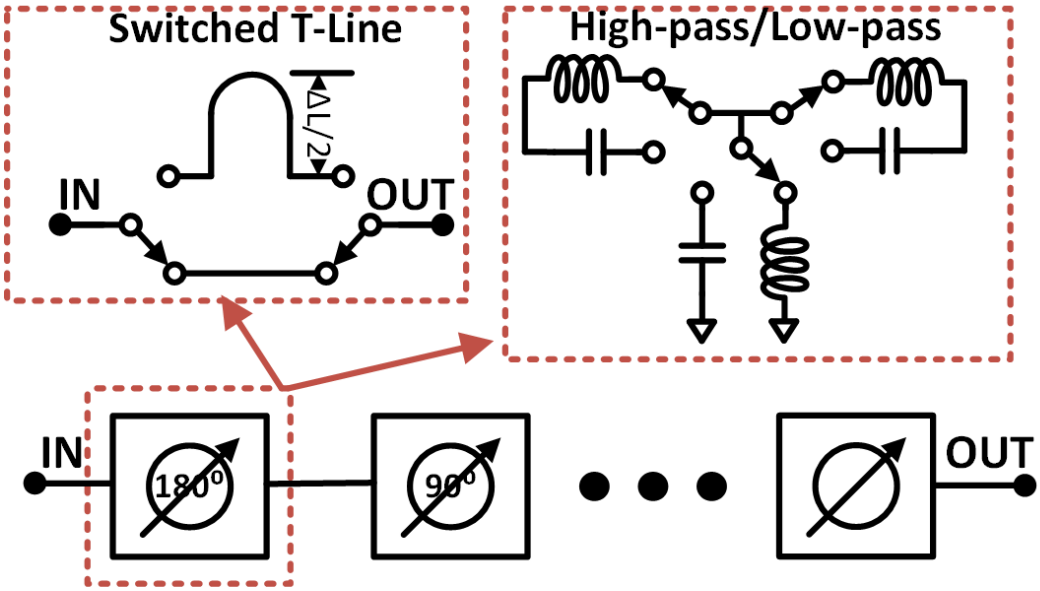

Figure 2.2: Architecture of switched t-line based N-bit phase shifter

amplifiers, phase shifters and attenuators, etc. Equations governing the relationships between phase shift, insertion loss and Γ_T have been discussed in section 2.3.2.

Reflective loads like MOS varactor load and a resonant LC load have been compared with the performance of RTPS with π load in [22]. RTPS with π load as shown in Fig. 2.4 fabricated in 130 nm BiCMOS, is reported to have measured insertion loss of 7.5 dB with 11.25° resolution in [22]. We will discuss the existing RTPS architectures, design of their building blocks and also the limitations of current approaches in the following Section 2.3.2. In Chapter 3, we will develop a systematic design approach to solve the existing limitations.

Lumped Element Based 3 dB Quadrature Coupler: Couplers, as shown in Fig. 2.3 [23] are 4-port passive monolithic integrated microwave circuits (MMIC) with applications in the design of power splitters, balanced mixers, balanced amplifiers, phase shifters, attenuators, etc [24]. The four ports known as input, isolated,

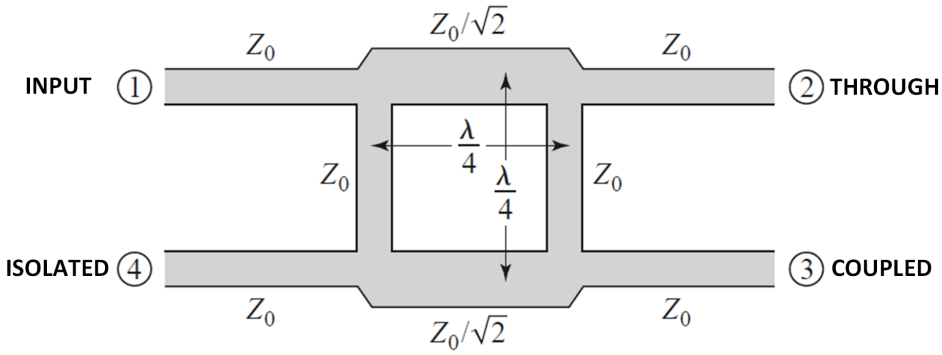

Figure 2.3: Schematic of branch-line hybrid coupler

coupled and through ports, exhibit a property that if the through and coupled ports are matched to 50 Ω, incident input signal power distributes equally to coupled and through ports and isolated port observes a power null. The four-port network has the s-parameter matrix given as:

$$\left[S\right] = \frac{1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \tag{2.1}$$

While the above property is utilized in power splitter design, another very important property of total incidence power reflection to the isolated port if the coupled and through ports are open, is used widely in designing RTPS.

Fig. 2.4 shows a general implementation of a passive RTPS. For balanced through and coupled port loads along with 50 Ω load at isolated port, (2.8) and (2.9) can be easily derived by using Kirchoff's voltage/current laws and along with the microwave theory of incidence and reflected voltages/currents. Eqns. (2.8) and (2.9) show that the isolated port effectively witnesses incidence voltage at the input port multiplied by the Γ_T, where Γ_T is reflection coefficient at the through and isolated ports. Variation in Γ_T, also varies the $\angle\Gamma_T$ and $|\Gamma_T|$, hence creating variable phase shift and insertion loss. This property has been utilized to design the

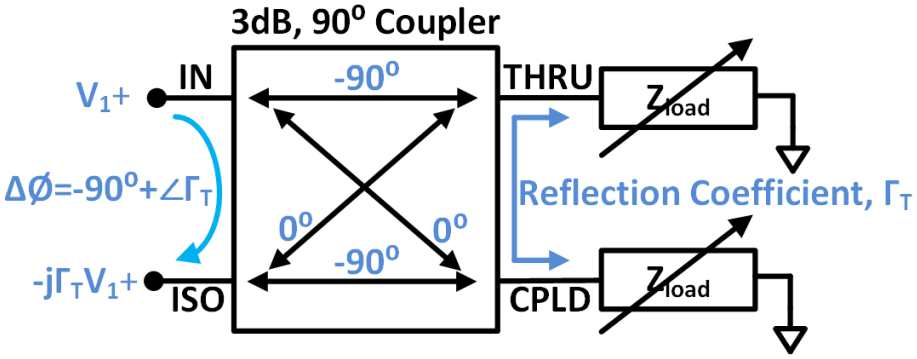

Figure 2.4: Architecture of reflection-type phase shifter

quadrature coupler based phase shifter at mm-wave frequencies. Eqns. (2.2-2.8) govern the incidence and the reflection voltage behavior at all the ports.

$$V_1^+ = V_0; \tag{2.2}$$

$$V_1^- = \frac{-j}{\sqrt{2}} V_2^+ + \frac{-1}{\sqrt{2}} V_3^+; \tag{2.3}$$

$$V_2^+ = \Gamma_2 V_2^-; \tag{2.4}$$

$$V_2^- = \frac{-j}{\sqrt{2}} V_1^+; \tag{2.5}$$

$$V_3^+ = \Gamma_T V_3^-; \tag{2.6}$$

$$V_3^- = \frac{-1}{\sqrt{2}} V_1^+; \tag{2.7}$$

$$V_4^+ = 0; \tag{2.8}$$

$$V_4^- = -j\Gamma_T V_1^+; \tag{2.9}$$

Design of Coupled Line Coupler: Fig. 2.5(a) shows the coupled t-line and Fig. 2.5(b) shows the loaded lines along with the source of incidence. Coupled line can be analyzed using even and odd mode modeling of the circuit. Derived equations can be compared with the coupler design equations to arrive at the conclusion that this structure can be used as a quadrature coupler. The equations governing the quarter wave long ($\lambda/4$) coupled lines are given by:

$$\frac{V_2}{V_0} = -j\sqrt{1-C^2}; \tag{2.10}$$

$$\frac{V_3}{V_0} = C; \tag{2.11}$$

$$Z_{0e} = Z_0\sqrt{\frac{1+C}{1-C}}; \tag{2.12}$$

$$Z_{0o} = Z_0\sqrt{\frac{1-C}{1+C}}; \tag{2.13}$$

where V_0, V_2, V_3 are the incidence, through port and coupled port voltages respectively, C is the coupling coefficient and Z_0 is the characteristic impedance. As mentioned before the isolated port sees a power null. Eqns. (2.12), (2.13), describe the characteristics impedances for even and odd mode excitation and their relationship with Z_0. Lumped element model of the coupled line based coupler has been used in the RTPS implementation. Parameters C, Z_{0e} and Z_{0o} will be utilized in Section 4.1 to calculate the values of lumped coupler components.

2.4 Limitations of State-of-Art RTPS/STPS

Integrated RTPS can achieve targeted phase shift by varying the impedance of terminations at the through and coupled ports of a quadrature 3-dB coupler [25]. As

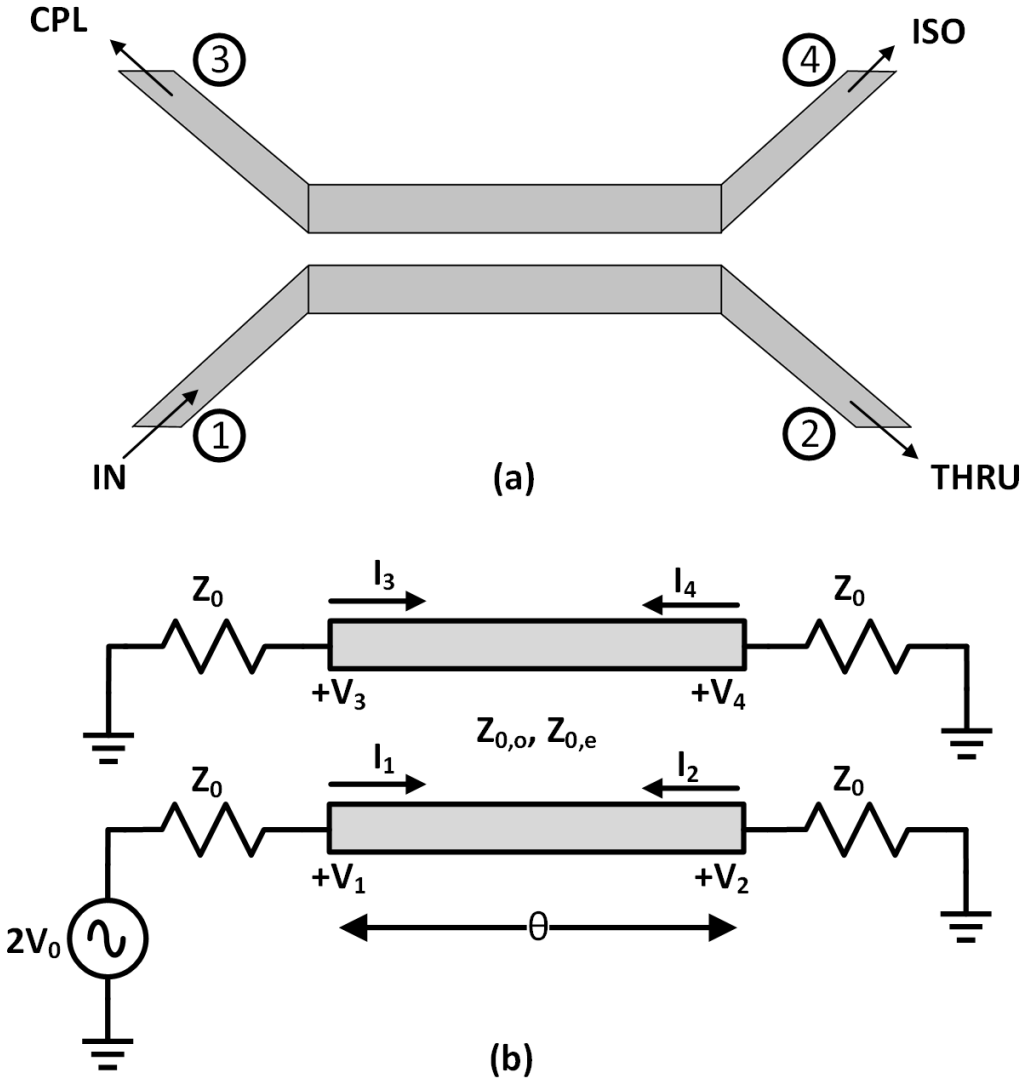

Figure 2.5: Coupled line coupler

shown in Fig. 2.4, varying the reflection coefficient of the coupled and through port loads leads to varying phase shift between the input and output (input and isolated ports, respectively, of the hybrid coupler). Typically, the variable termination impedance is achieved by changing the control voltage across a varactor. Therefore, high resolution can be achieved without any area or loss penalty, particularly with on-chip implementations, which allow CMOS DACs with very high voltage resolution. However, the varactor quality factor, Q, and loss vary across capacitance settings leading to phase shift dependent loss in the RTPS [26]. As suggested in [22], variable loss across phase shift can be avoided by independently controlling two varactors in a π-network variable load. However, achieving sufficient varactor variation to ensure 360° phase shift is challenging - state-of-the-art on-chip implementations target smaller $\sim$180° phase shift range while adopting higher-order loads such as a shunt-LC [26], π-network [16, 27], or cascading RTPS [28, 29] with other active phase shifters or STPS [30, 31]. Hence the RTPS is followed by an active 0/180° stages in such implementations. If the discrete 0/180° phase shift is achieved using an active stage, the resultant non-linearity/power consumption reduces some of the advantages of using a passive VPS. In this work, we extend the approach in [22] by developing a systematic design methodology that reduces loss and ensures desired 360° phase shift.

Chapter 3: Proposed Low-power 28-GHz RX Array Frontend Architecture

3.1 Design of 28-GHz Reflection-type Phase Shifter

Our objective is to achieve 360° phase shift range at 28 GHz while minimizing insertion loss, targeting phased arrays for future 5G applications [32]. As shown in Fig. 2.4, assuming an ideal hybrid coupler, the phase shift, $\Delta\Phi$, and insertion loss (in dB), IL, through a reflection-type phase shifter is provided by,

$$\Delta\Phi = -90^\circ + \angle\Gamma_T \tag{3.1}$$

$$IL = -20\log\left(|\Gamma_T|\right) \tag{3.2}$$

Where Γ_T is the reflection coefficient at the coupled and through ports. Therefore, ensuring $|\Gamma_T| = 1$, and $\angle\Gamma_T$ range = 360°, ensures lossless operation across entire phase shift range. However, in practice, performance is limited by coupler insertion loss, finite isolation between input and isolated ports, and loss/phase variation limits in the variable reflective load. It can be shown that a termination with a single varactor cannot achieve 180° phase shift range in the presence of parasitics. This necessitates a higher-order load to achieve large phase shift variations. In the following, we develop constraints on RTPS design parameters to minimize insertion loss for 360° phase shift range. These constraints are described in the context of Π-network reflective load shown in Fig.3.2. A similar approach can be adopted for other reflective loads as well.

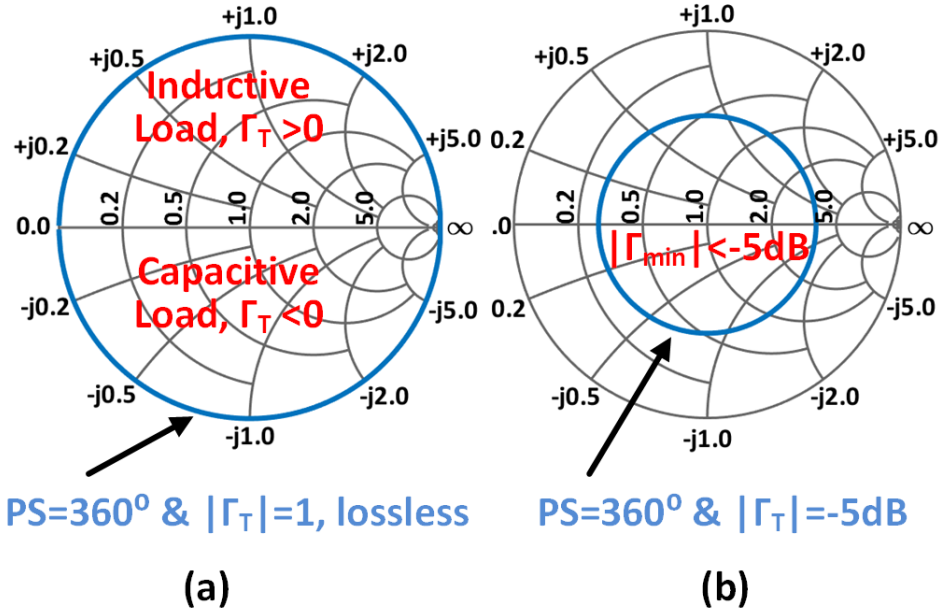

Figure 3.1: Representation of desired & practical Γ on Smith chart (a) Ideal $|\Gamma_T|$=0 dB circle (b) $|\Gamma_T|$= -5 dB circle

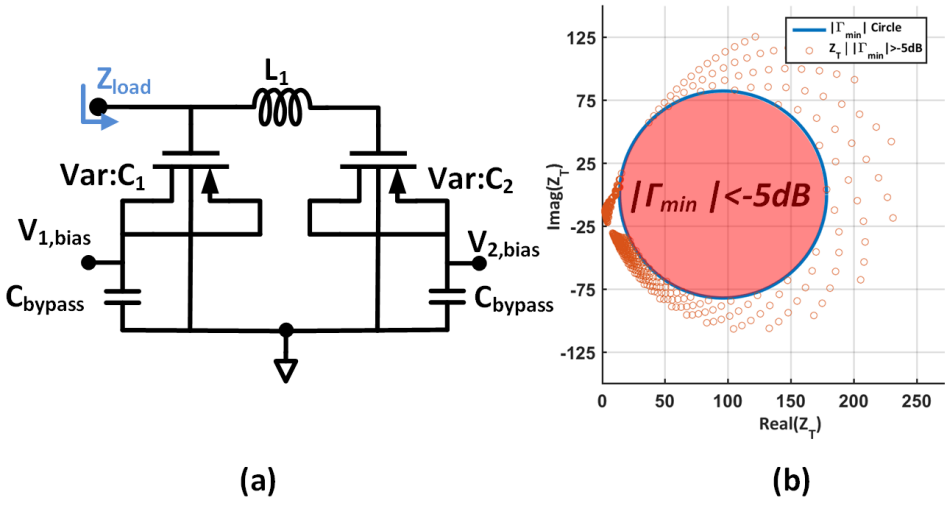

Figure 3.2: (a) Variable Π load based on varactors (b) Impedance circles corresponding to $|\Gamma_T|$=-5 dB

3.1.1 Impact of varactor and inductor loss:

Losses in the varactor and inductor lead to $\Gamma_T < 1$, implying loss even if an ideal coupler is assumed. Based on (3.2), a targeted loss metric, requires $|\Gamma_T| > |\Gamma_{min}|$ as shown in Fig. 3.1(b). Assuming the Π-network shown in Fig. 3.2(a), the Z_T and Γ_T, are given by,

$$Z_T = \frac{1 + s^2 L_1 C_2}{s(C_1 + C_2) + s^3 L_1 C_1 C_2}, \tag{3.3}$$

$$\Gamma_T = \frac{Z_T - Z_0}{Z_T + Z_0}, \tag{3.4}$$

As noted in [22], C_1 and C_2 can be varied independently to minimize loss across phase shift. From (3.4), assuming $Z_T = R_T + jX_T$, it can be shown that to ensure $|\Gamma_T| > |\Gamma_{min}|$,

$$(R_T - A)^2 + X_T^2 > R^2, \tag{3.5}$$

Where;

$$A = Z_0 \frac{1 + |\Gamma_{min}|^2}{1 - |\Gamma_{min}|^2}, \tag{3.6}$$

$$R = 2Z_0 \frac{|\Gamma_{min}|}{1 - |\Gamma_{min}|^2}, \tag{3.7}$$

Therefore, the Γ_T constraint translates graphically to Fig. 3.2(b) , where acceptable values of Z_T that ensure $\Gamma_T > \Gamma_{MIN}$ lie outside the circle defined by (3.5).

For instance, in this work, we target 28 GHz operation in 65 nm CMOS technology. Representative simulations with $L_1 = 390$ pH, $C_1 = 80\ fF \rightarrow 280\ fF$, and $C_2 = 45\ fF \rightarrow 157\ fF$ show that it is feasible in this case for Z_T to satisfy $\Gamma_T > \Gamma_{MIN}$ across the entire phase shift range. This can also be represented

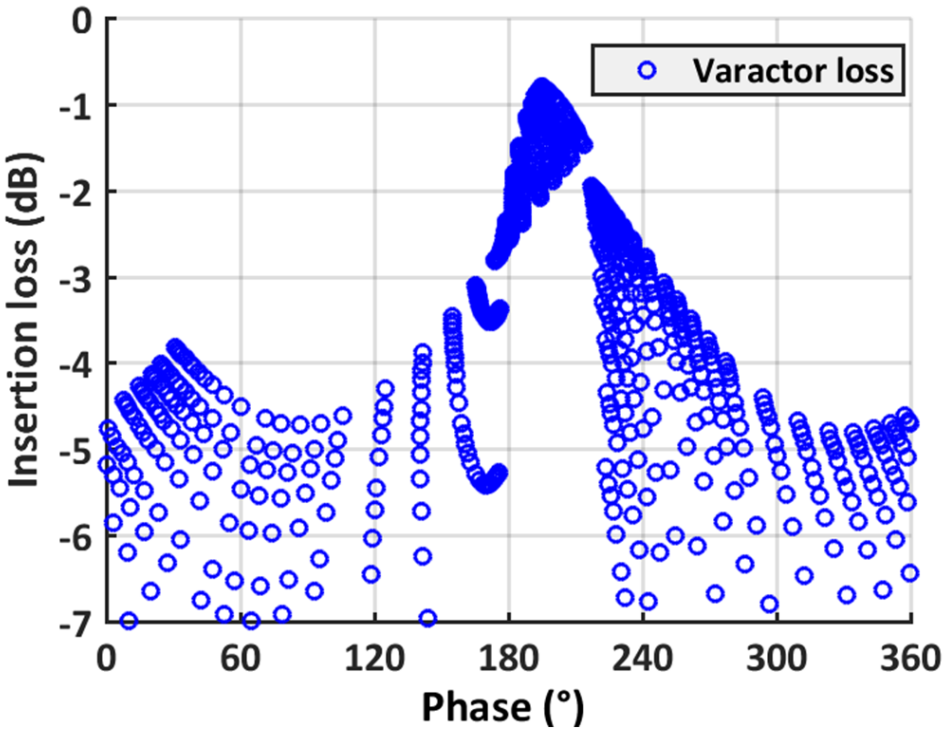

Figure 3.3: Π-load insertion loss variation with phase shift across varactor codes

graphically in terms of the insertion loss across C_1 and C_2 settings as shown in Fig. 3.3. finite varactor Q ($Q_{min} = 10$) leads to varying insertion loss as capacitances are varied - however, it is feasible to select C_1, C_2 such that all phase shift settings are achieved with ∼-5 dB insertion loss. Notably, the targeted uniform loss is limited by the *worst-case loss* - C_1 and C_2 values for all phase shifts are selected to achieve this loss. This is also true for other phase shifters - for example, STPS equalizes loss for ON and OFF settings, or active phase shifters equalize loss by discarding high gain settings. Therefore, minimizing insertion loss requires that the worst-case loss must be minimized.

3.1.2 Impact of isolation in coupler:

In addition to losses associated with the variable terminations, an RTPS with integrated hybrid coupler has two additional sources of loss - firstly, coupler dielectric/metal losses lead to insertion loss from input to coupled and through ports. Additionally, finite isolation between input and isolated port ($\sim$ 17.7 dB at 28 GHz) leads to phase-shift dependent loss through the RTPS. Fig. 3.4 compares the loss because of the coupler with the best-case variable termination losses across RTPS phase-shift settings (obtained from Fig. 3.3). Worst-case RTPS insertion loss can be improved by aligning the phase shift setting corresponding to the lowest termination-loss with the phase shift corresponding to the highest loss due to the coupler as shown in Fig. 3.4.

Since the loss due to finite coupler isolation is highest for $\Phi = 180°$, applying (3.4), L_1,C_1, and C_2 must be selected to achieve lowest insertion loss at $\Phi = 180°$. Fig. 3.5 plots the loss across C_1 and C_2 demonstrating that minimum loss occurs when C_1 is at its maximum and C_2 is at its minimum. Our objective is to ensure that this corresponds to the phase shift with highest coupler insertion loss, which imposes the following constraint,

Constraint 1: The value of L_1 and the varactors determining C_1 and C_2 must be selected such when $C_1 = C_{1,min}$ and $C_2 = C_{2,max}$, the phase shift through the RTPS, $\Delta\Phi \sim 180°$.

Additionally, as shown in Fig. 3.4 insertion loss due to varactor losses shows two local minima. It is also desirable to balance the insertion loss in these two cases to improve worst case performance. For instance, for the set of values in Fig. 3.5, these local minima occur at ($C_1 = C_{1,min}, C_2 = C_{2,mid}$) and ($C_1 = C_{1,mid}, C_2 = C_{2,max}$). Therefore, an additional design constraint can be imposed,

Constraint 2: The range of C_1 and C_2 should be selected to equalize the two minima in the varactor loss curve in Fig. 3.4 are balanced to minimize worse-case loss.

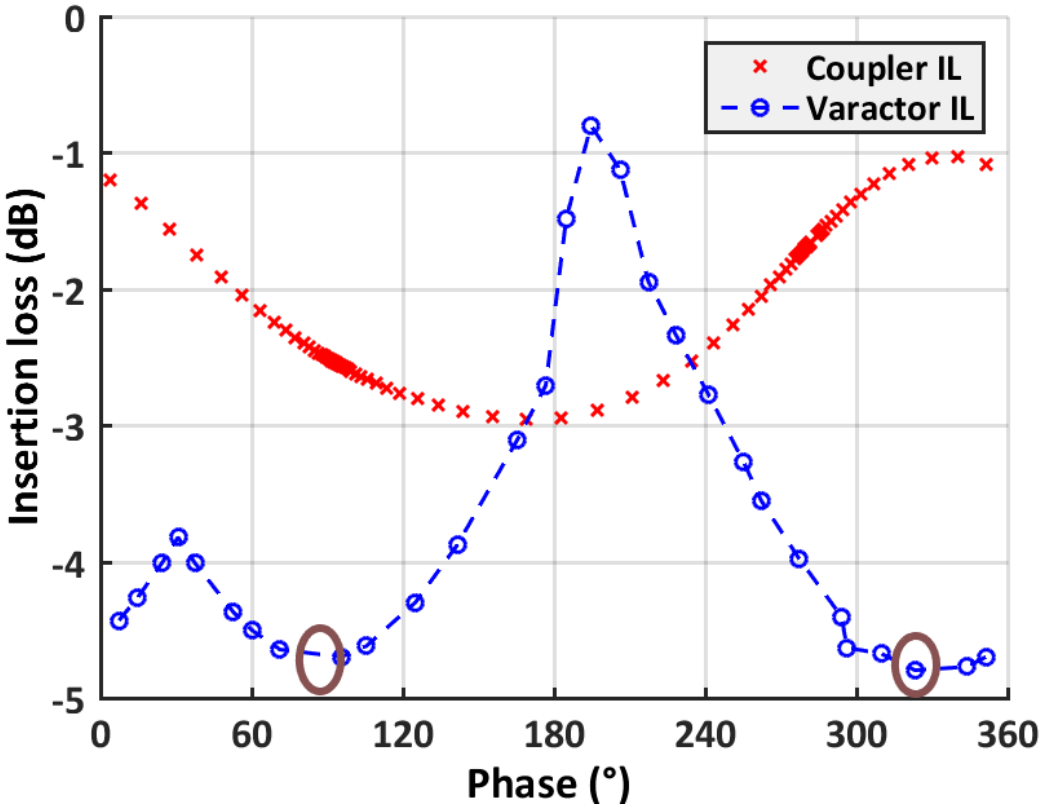

Figure 3.4: Coupler and Π load insertion losses with phase shift for selected varactor code

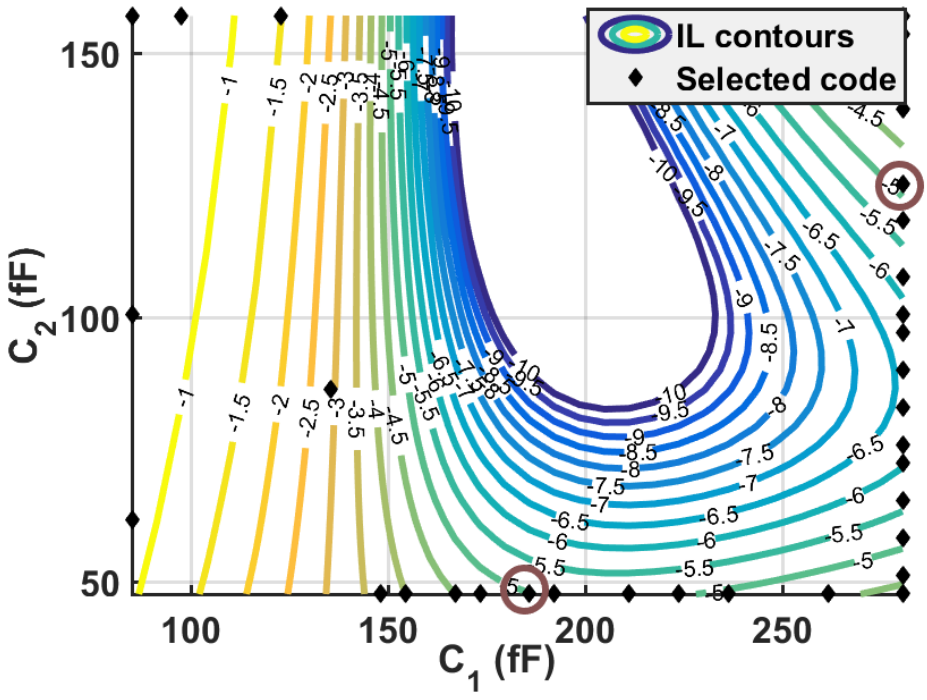

Figure 3.5: Insertion loss contours for different values of C_1 and C_2 and the selected code for minimum loss across phase shift range

3.1.3 Phase shift variation requirements:

The constraints associated with insertion loss must be satisfied in the context of the targeted phase shift range. Defining $K = C_{min,1}/C_{min,2}$ and assuming that a varactor in the selected technology provides $C_{max}/C_{min} = 3.3$ at 28 GHz, the phase shift when both varactors are at their minimum setting, $\Gamma_{T,1}$ is,

$$\angle\Gamma_{T,1} = 2tan^{-1}\left(\frac{\omega Z_0 C_{MIN,1}(K+1)\left(P\frac{K}{K+1}-1\right)}{1-PK}\right); \tag{3.8}$$

Where $P = \omega^2 L_1 C_{min,1}$ and the phase shift at the maximum capacitance setting $(C_{max,1}, C_{max,2})$ is provided by

$$\angle\Gamma_{T,2} = 2\tan^{-1}\left(\frac{\omega Z_0 3.3 C_{min,1}(K+1)\left(P\frac{3.3K}{K+1}-1\right)}{1-P3.3K}\right); \tag{3.9}$$

Fig. 3.6 plots the contours of phase shift range, $(\angle\Gamma_{T,1} - \angle\Gamma_{T,2})$, across K and P for different values of C_1, based on (3.8) and (3.9). Notably, only certain combinations of K and P achieve targeted phase shift for given C_1. Imposing the following constraint ensures targeted 360° phase shift range

Constraint 3: The choice of K and $\omega^2 L_1 C_{min}$ must ensure targeted 360° phase shift range at frequency of interest.

3.2 LNA Design

Proposed low-power receiver frontend has been demonstrated with an extremely low power gain boosted low-noise amplifier (LNA). Since mobile communications in 5G networks require high data rate, the targets for SNR while maintaining the lower power and sufficient gain, are stringent. LNA being the frontend module of the receiver determines the overall NF of the system, hence the gain/power consumption vs NF tradeoff becomes critical design parameter in the LNA design. This work is focused on obtaining maximum possible gain from the LNA in a power efficient way, maintaining low NF at the same time.

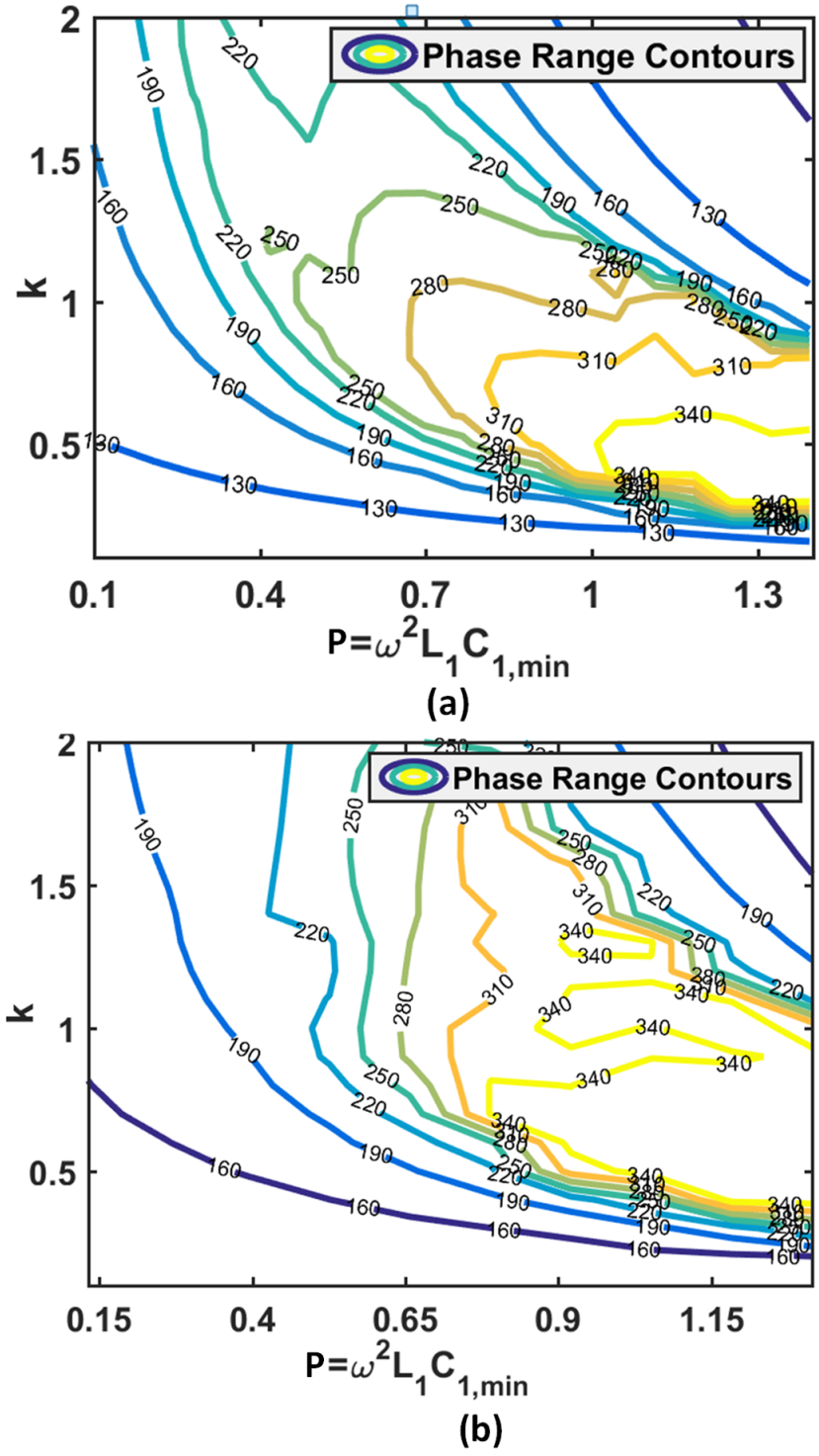

Figure 3.6: Phase range contours for different values of K and P and (a) $C_{1,min}$=45 fF (b) $C_{1,min}$=85 fF

3-stage single ended low-power neutralization LNA: The frontend in this work is targeted for low-power receive elements at 28 GHz. The LNA in this work precedes the passive phase shifter and hence must provide sufficient gain to achieve overall low noise figure. Therefore, the 65 nm CMOS LNA is designed to operate with low power while providing $>$ 19 dB gain at 28 GHz.

Single-stage amplifier gain at mm-wave in 65 CMOS is limited by the feedback capacitance between gate and drain, C_{GD}. A neutralization technique based on capacitive feedback through transformer coupling to achieve low-power by gain boosting the LNA has been presented in [33] at frequency range of 57 GHz-66 GHz to cater to WiHD, WiGig and 802.15c standards. Fig. 3.7(a),(b) shows other neutralization based techniques like split-feedback inductor tuning based architecture [34], transformer feedback to gate/drain [35, 36] are also available in the literature, but capacitive feedback through transformer coupling technique as shown in Fig. 3.7(c) has been reported to achieve optimal gain and phase conditions for maximum available power gain [33]. The approach in [33] aims to simultaneously achieve wide bandwidth (60 GHz, 14 %) and low power consumption using neutralization - therefore the gate-drain neutralization is done using capacitive feedback and the interstage transformer matching.

In this work, relatively narrow bandwidth at 28 GHz ($\sim$3 GHz) is acceptable. We modify the topology in Fig. 3.7(c) to tap the output to the next stage from the primary of the feedback transformer, which helps avoid the losses due to finite coupling coefficient between primary and secondary. Therefore, as shown in Fig. 3.7(d) we adopt a topology where the neutralization is done to achieve higher gain. The three-stage LNA adopts a common-source amplifier in each stage to minimize supply voltage ($\sim 0.9\ V$) and power consumption ($\sim$10 mW).

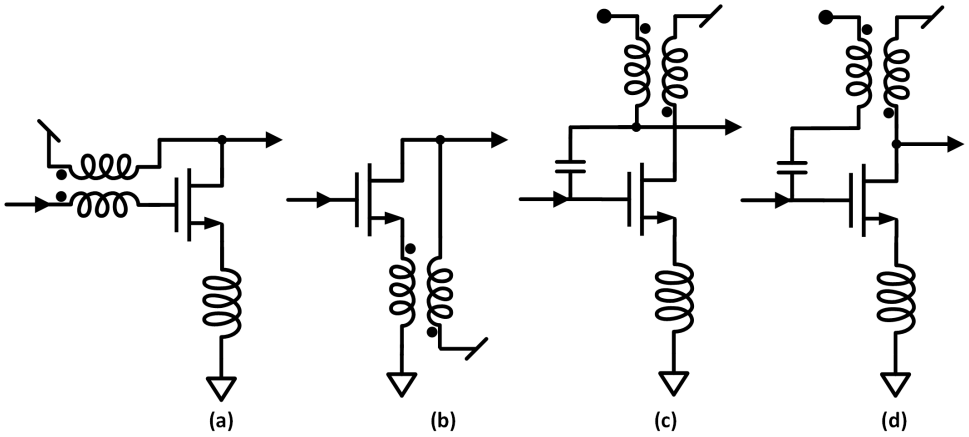

Figure 3.7: (a,b) Gain boosting through transformer feedback from drain to gate/-source (c,d) Neutralization with C_{GD} cancellation through transformer feedback

Chapter 4: Circuit Implementation

4.1 28-GHz RTPS design in 65 nm CMOS

In the following section, we discuss the design of a 28-GHz RTPS in the context of the constraints described above to minimize insertion loss across phase shift range. The three design variables, $C_{1,min}$, $C_{2,min}$ and L_1 are transformed to the variables $C_{1,min}, K$ and P.

The phase shift for given C_1, C_2 and L_1 is given by,

$$\angle\Gamma_T = 2tan^{-1}\left(\frac{\omega Z_0(C_1+C_2)\left(\omega^2 L\frac{C_1C_2}{C_1+C_2}-1\right)}{1-\omega^2 L_1 C_2}\right); \tag{4.1}$$

Therefore, satisfying constraint 1 in Section 3.1.2, implies,

$$1-\omega^2 L_1 C_{2,max} = 1-3.3P\cdot K = 0 \tag{4.2}$$

However, as shown in Fig. 3.6(a,b) for $C_{1,min} = 45\ fF$ & $C_{1,min} = 85\ fF$ respectively, P and K must also satisfy constraint 3.

From (4.2), a definite relationship between K and P to satisfy constraint 3 can be established. As can be seen from Fig. 3.6, range of K to meet close to 360° phase shift is approximately $0.3 \leq K \leq 0.6$ for $C_{1,min} = 45\ fF$ and $0.4 \leq K \leq 1.0$ for $C_{1,min} = 85\ fF$ and hence, the range of desirable P from (4.2) translates to $0.5 \leq P \leq 1.0$ and $0.3 \leq P \leq 0.75$ respectively. Also, from Fig. 3.6, it is impossible that this range of values of P can meet the phase shift range requirements as such. Under the practical constraints and keeping in mind that for $P > 0.7$, required $L_1 \geq 500\ pH$, we reject $C_{1,min} = 45\ fF$. The closest possible value of P to the above mentioned range and K has been chosen to satisfy both the constraint 3 and phase shift range= 360°.

Since, the K has been selected based on Fig. 3.6, the only remaining variables are m and $C_{1,min}$. Limiting the L_1 to accurately realizable inductance of $\leq 500\ pH$ at 28 GHz, limits the $C_{1,min}$ to a smaller set of values. Further, $C_{1,min}$ can be selected to satisfy constraint 2.

Based on these constraints a design approach at 28 GHz yields $C_{1,min} = 45\ fF$, $C_{2,min} = 85\ fF$ and $L1 = 425\ pH$ values. The design was implemented based on the schematic in Fig. 4.1, which includes component parameters. The coupler was designed to achieve a characteristic impedance of 50 Ω. EM simulations were carried to model the inductor and the coupler - both of which were implemented using the top metal layer of thickness 3.4 μm. RTPS simulations that include both coupler and varactor are presented along with measurements in Chapter 5.

Fig. 4.1 shows the lumped element quadrature hybrid coupler based on transformer & capacitors implemented in [37], [24], and the lumped element components values are given by,

$$L_p = \frac{Z_{0e} + Z_{0o}}{4\pi f}; \tag{4.3}$$

$$C_Y = \frac{1}{Z_{0e} 2\pi f}; \tag{4.4}$$

$$M = \frac{Z_{0e} - Z_{0o}}{4\pi f}; \tag{4.5}$$

$$C_X = (\frac{1}{Z_{0o}} - \frac{1}{Z_{0e}})\frac{1}{4\pi f}; \tag{4.6}$$

To achieve a coupling coefficient of 0.7 and 50 Ω characteristic impedance, $Z_{0o} = 16.10\ \Omega$ and $Z_{0e} = 217.30\ \Omega$.

Varactor π load includes a pdk inductor of $L = 425\ pH$. Moscap has been used with minimum capacitor values of $C_1 = 80\ fF$ & $C_2 = 45\ fF$. Length of 300 nm for the moscap is selected based on the ON/OFF ratio and quality factor tradeoffs. The coupler capacitor values to ground $C_1 = C_2 = C_3 = C_4 = 35.27\ fF$, and the coupling capacitor values are $C_5 = C_6 = 92.20\ fF$. The coupling transformer has value $L_p = L_s = 325\ pH$ and it is custom designed using ie3d modeling.

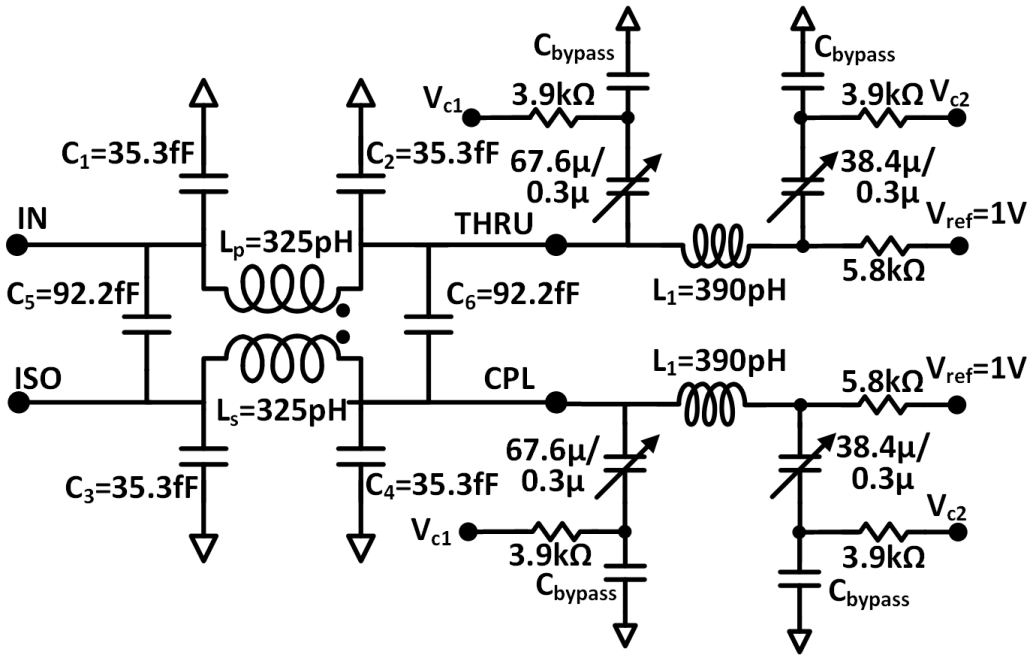

Figure 4.1: Implementation of RTPS in 65 nm TSMC

4.2 Low noise amplifier

Proposed low-power receiver frontend has been demonstrated in 65 nm CMOS with an extremely low power gain boosted low-noise amplifier(LNA) as shown in Fig. 4.2. While the first stage is a common source stage with source degeneration for input matching, the following two stages don't use degeneration to obtain maximum available gain. First stage has been optimized for low NF of ∼4.5 dB while consuming ∼3.5 mA current from a 0.9 V supply. Neutralization technique has been implemented using a customized transformers with a coupling coefficient 0.66 and a MOS varactor to ensure stability and programmability. Values of all the components has been shown in Fig. 4.2 and the transformer and gate/source inductors are routed in the highest thickness metal layer to ensure higher Q. The transformer model has been modeled in EM extraction tool and yields effective Q of 13 and the gate/source inductors have been modeled with a slightly pessimistic Q of 12.

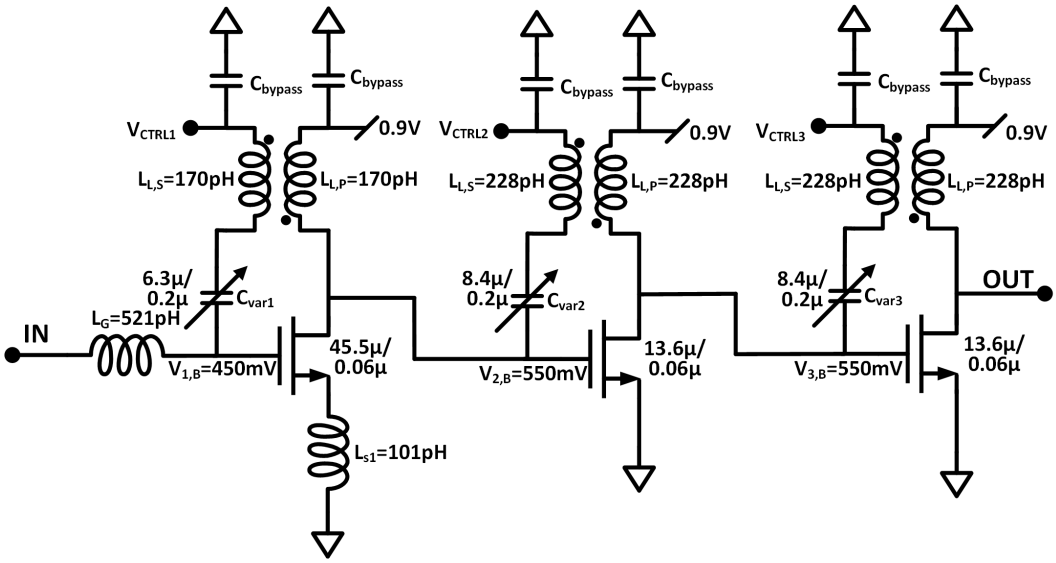

Figure 4.2: 3-stage neutralization LNA

Chapter 5: Measurement Results

The frontend of the phased-array receiver fabricated in TSMC 65 nm, as shown in Fig. 5.1, consists of a stand-alone RTPS and a frontend receiver consisting of low-power LNA followed by the RTPS. The performance of the front end has been measured using the Agilent 5227a PNA and a 67 GHz probe station. 2-port s-parameter measurements are performed using a 67 GHz GSG-100 infinity probes. The calibration of the PNA uses cascade 110 GHz ISS and the SOLT method.

5.1 Stand-alone RTPS Measurement Results

The phased-array receiver frontend (Fig. 5.1) was implemented in a 65-nm CMOS process with 3.4-μm thick top metal layer. The frontend s-parameters are measured using a probe-based setup with a Keysight 5227A network analyzer. The IC included a stand-alone test structure for characterizing the RTPS (Fig. 5.1).

Fig. 5.2 plots the measured stand-alone RTPS performance at 28 GHz as Z_{T1} and Z_{T2} are varied. The varactor control voltages are assumed to vary with 12.5-mV step size across a 0 V to 2 V range (7.3 bits). As shown in Fig. 5.2, a subset of these settings can be selected to acheive uniform insertion loss and full 360° phase shift. Fig. 5.3 compares the results of the same algorithm based on simulated and measured data, demonstrating good match across insertion loss and phase shift.

Stand-alone RTPS phase shift and insertion loss across frequency is shown in Fig. 5.4(a,b), demonstrating 5-bit resolution from 27 GHz to 29 GHz

Phase shift with 5-bit resolution is measured across frequency range of (27 GHz-29 GHz) has been shown in the Fig. 5.4 with the varactor code $[C_1, C_2]$ optimized for best performance at 28-GHz and rms phase error restricted to 0.3° across all frequencies. While Fig. 5.4 plots the phase shifter assuming fixed settings at 28GHz, Fig. 5.5 across insertion loss and phase shift performance where optimal

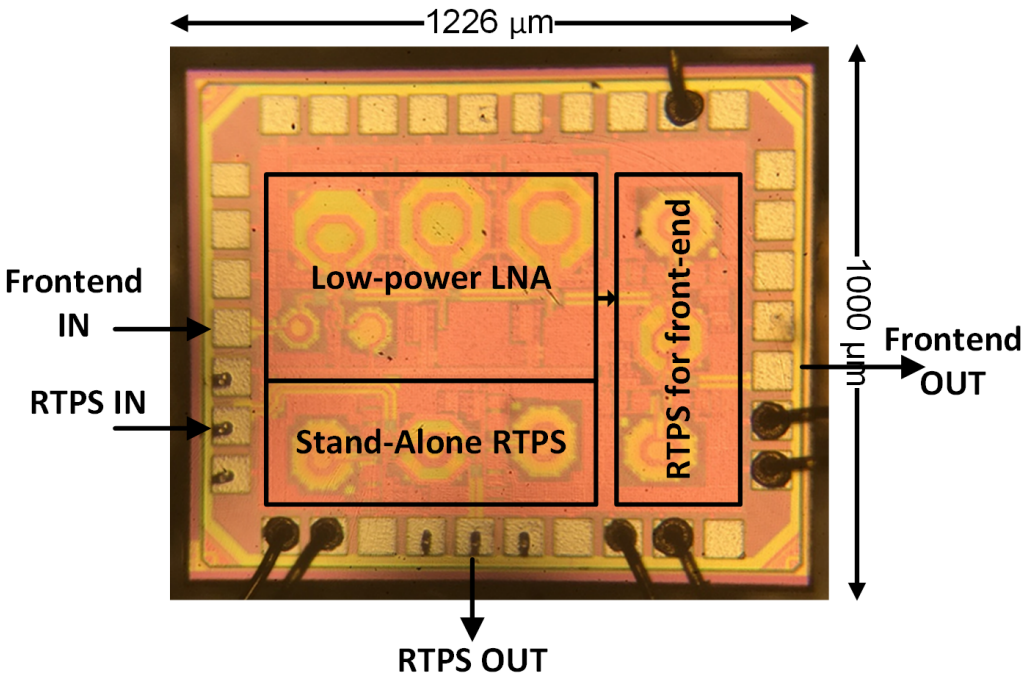

Figure 5.1: Micro-photograph of wire-bonded die - Stand-alone RTPS case

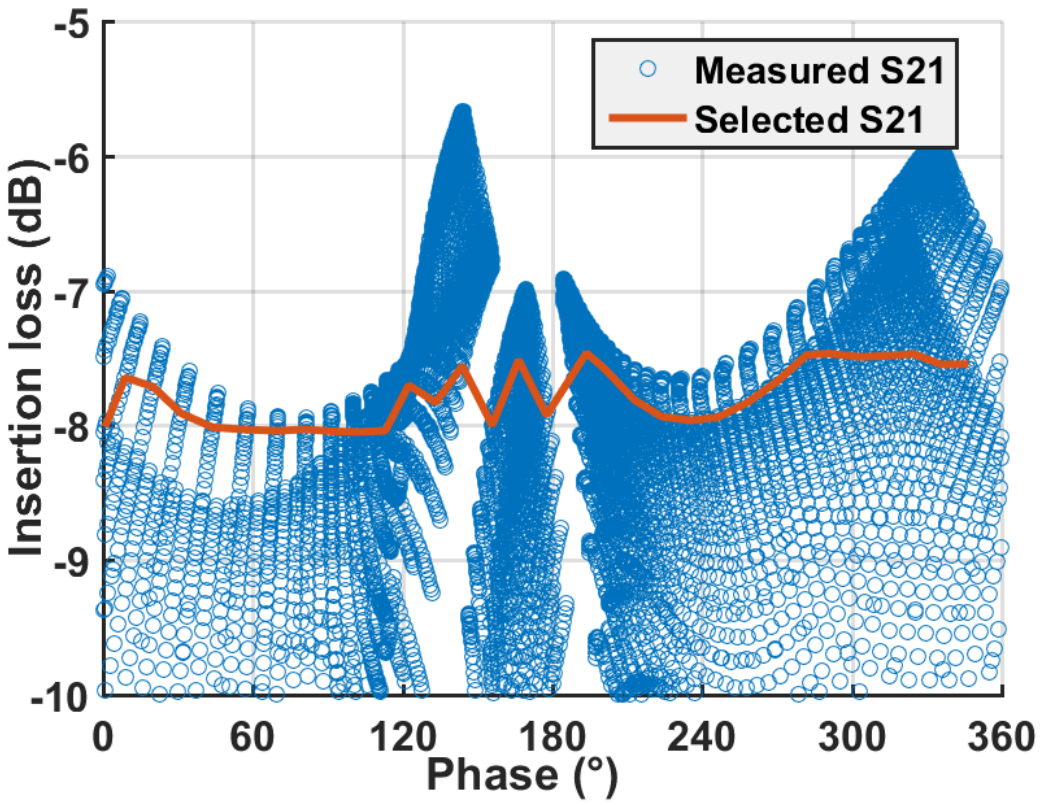

Figure 5.2: Measured stand-alone RTPS insertion loss and phase shift across load settings at 28 GHz.

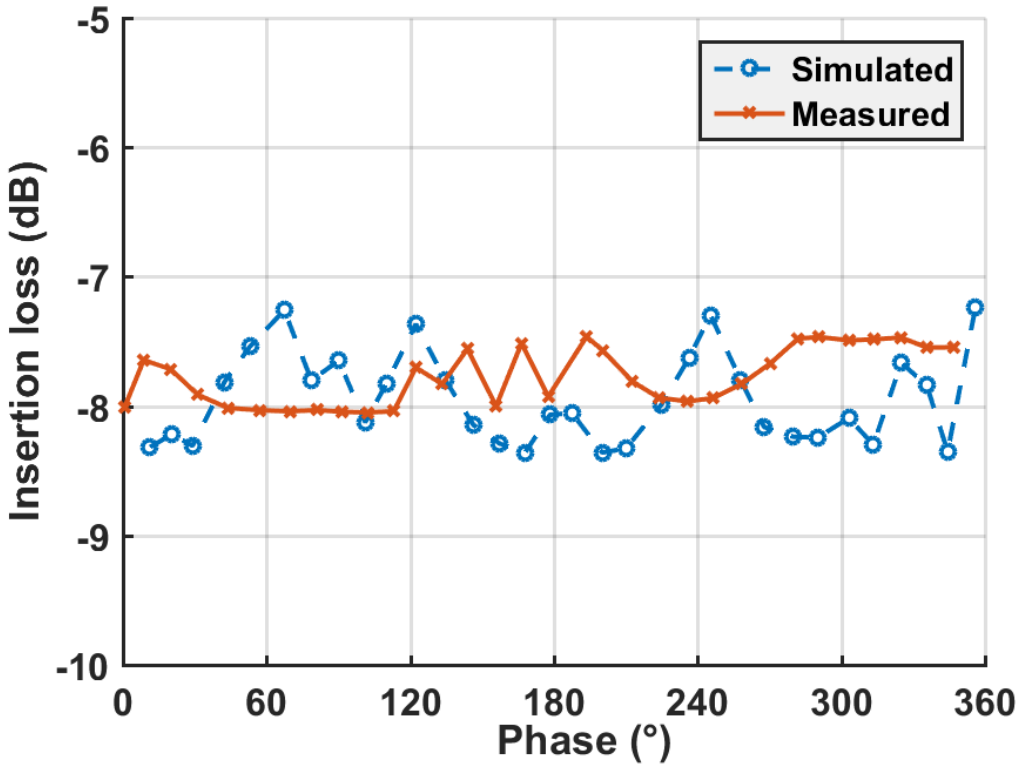

Figure 5.3: Measured vs. simulated performance for stand-alone RTPS at 28 GHz

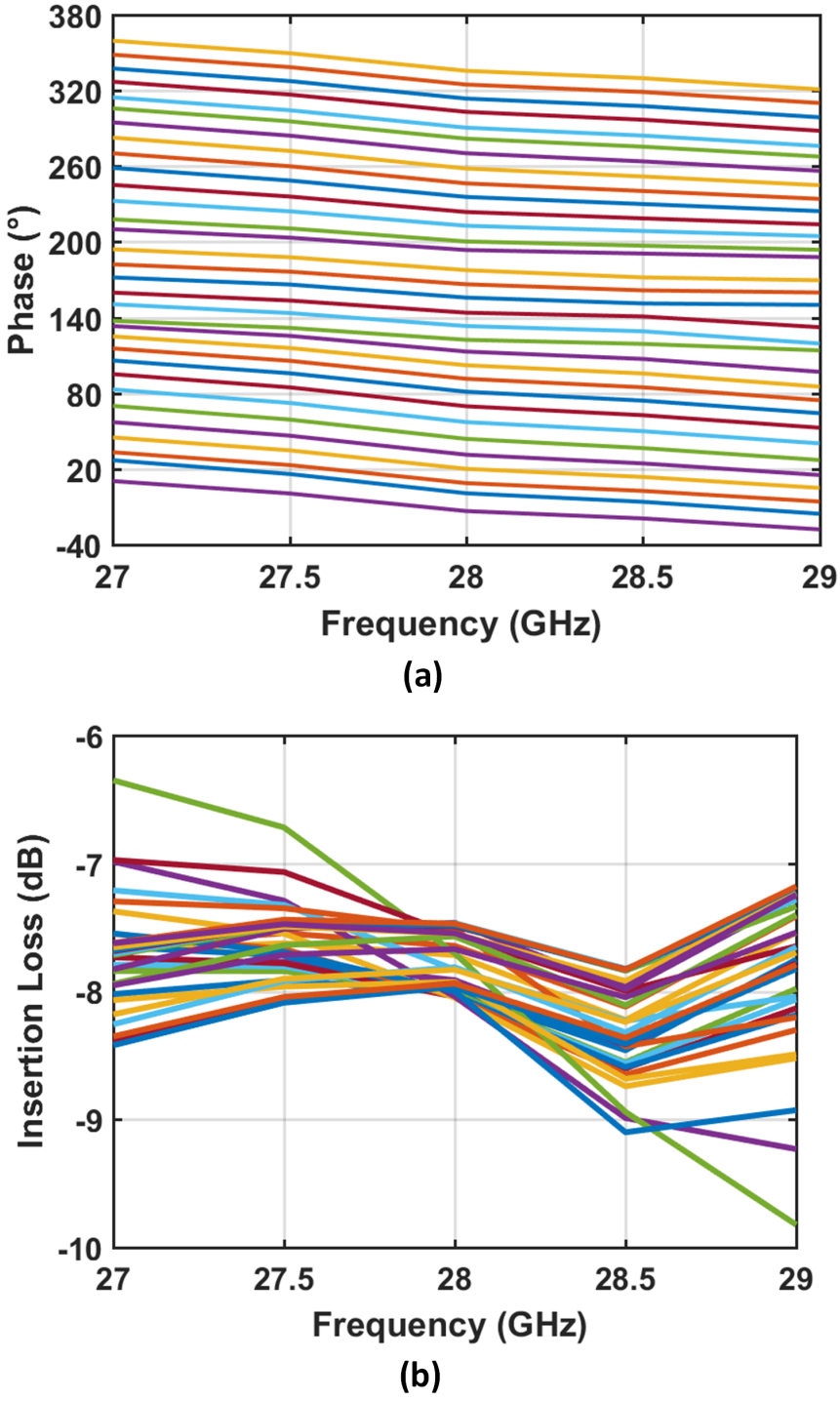

Figure 5.4: Measured stand-alone RTPS (a) phase shift (b) insertion loss, across frequency for best performance at 28 GHz

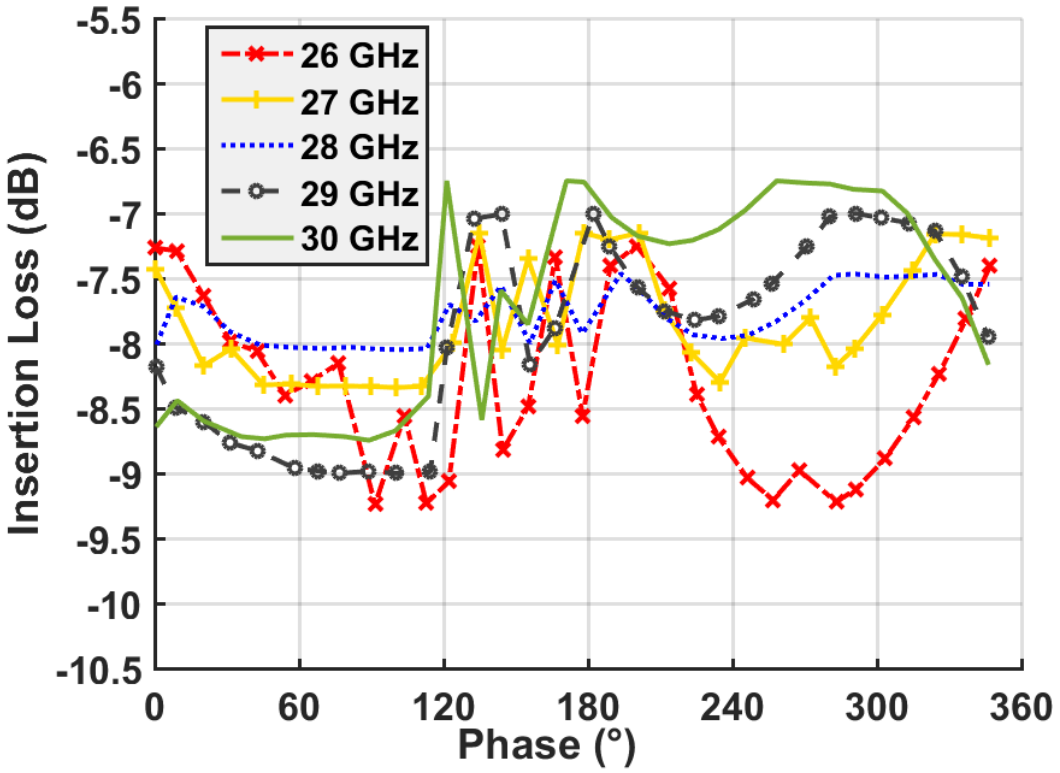

Figure 5.5: Measured RTPS insertion loss with phase shift across frequency

settings are recalculated. As shown in Fig. 5.5, recalculating phase shift settings can result in 8±1.25 dB insertion loss from 26 GHz to 30 GHz while achieving 5-bit resolution and 360° range. As shown in Table 5.1 the RTPS has a wide tuning band of 26 GHz-30 GHz.

The performance of the stand-alone RTPS is compared across state-of-art in Table 5.2. The proposed RTPS achieves lower insertion for full 360° range (the loss is comparable to [22] which has 180° range). The insertion loss is comparable to state-of-art STPS [11], however the proposed RTPS achieves higher resolution, smaller area and better performance across frequency as discussed in Chapter 2

Table 5.1: RTPS PERFORMANCE ACROSS FREQUENCY

[This work] Freq. (GHz)	Phase Shift Range (°)	Avg. IL (dB)	IL Variation (dB)	Max. Phase Err (°)
26	360°	8.25	±1	2.5°
27	360°	7.75	±0.6	2.5°
28	360°	7.75	±0.3	2.5°
29	360°	8	±1	2.5°
30	360°	7.75	±1	2.5°

Table 5.2: STATE-OF-THE-ART mm-WAVE PHASE SHIFTERS

Approach [Ref.]	Process	Freq. (GHz)	Bandwidth (GHz)	Phase Range (°)	Rms Error (°)	Resolution (°)	Max Loss (dB)	Loss Var. (dB)	Area (mm^2)
Series RTPS [16]	180 nm CMOS	24	0.8	360°	NA	Cont.	12.5	2.4	0.33
Hybrid [38]	65 nm CMOS	60	7	360°	4.4°	11.25°	16.3	4	0.094
RTPS [22]	130 nm BiCMOS	94	10	180°	2.5°	11.25°	7.9	1	0.12
STPS [11]	65 nm CMOS	28	0.85	360°	8.98°	22.5°	7.6	2	0.23
RTPS [This work]	65 nm CMOS	28	4	360°	0.3°	11.25°	8.05	0.6	0.16

5.2 Frontend Measurement Results

In this section we present the overall frontend measurement results and the comparison with the simulated results. Two-port s-parameter measurements were performed with the varactors $[C_1, C_2]$ codes. Simulated results are compared with the measuremed s-parameter in Fig. 5.6. The comparison demonstrates good match for the input matching from the LNA as well as the gain performance of the frontend. Measured phase of S_{21} has also been plotted in Fig. 5.8 to demonstrate the continuity in the phase. Fig. 5.7 shows the frontend insertion loss across corners and the selected code for low loss variation. Overall gain of 9.5 dB with gain variation of ± 0.4 dB with 0.4° has been measured at 10 mW power and 0.9 V supply. Noise figure measurement have been preformed using Y-factor method. The measured noise figure of the system has been plotted against the simulated noise figure in Fig. 5.9. Front-end of the phased-array receiver has overall measured NF of 4.9 dB at 28 GHz.

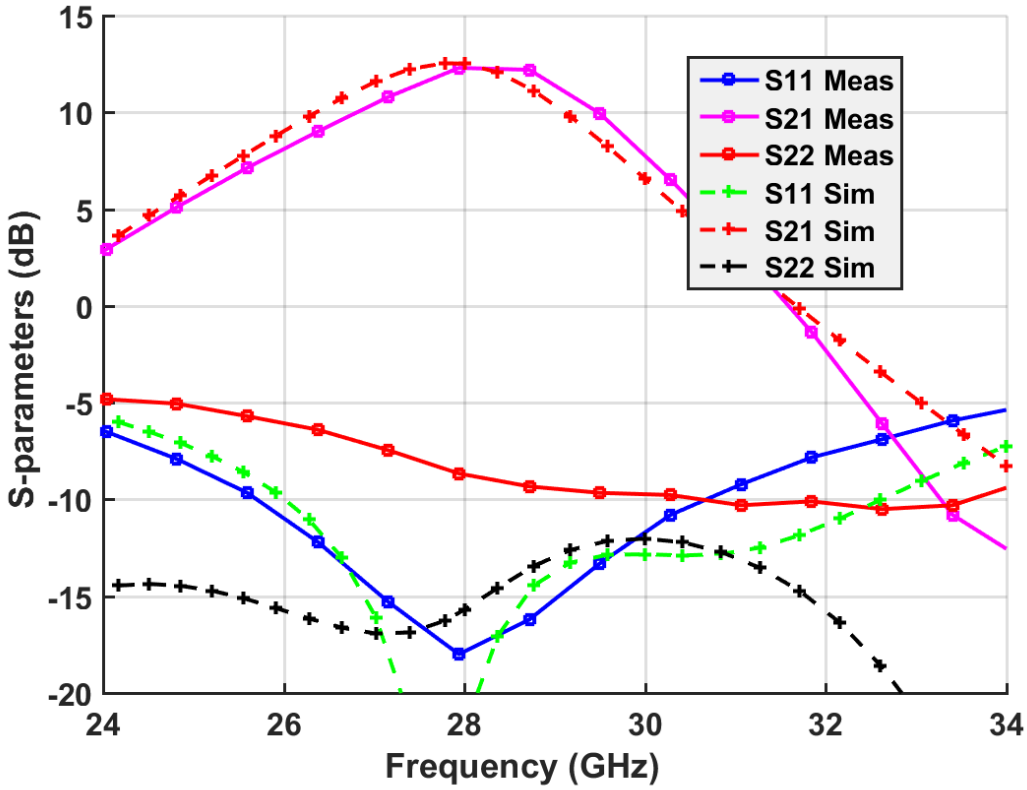

Figure 5.6: Comparison of measured and simulated S-parameters for the frontend for $[C_{1,max}, C_{2,max}]$

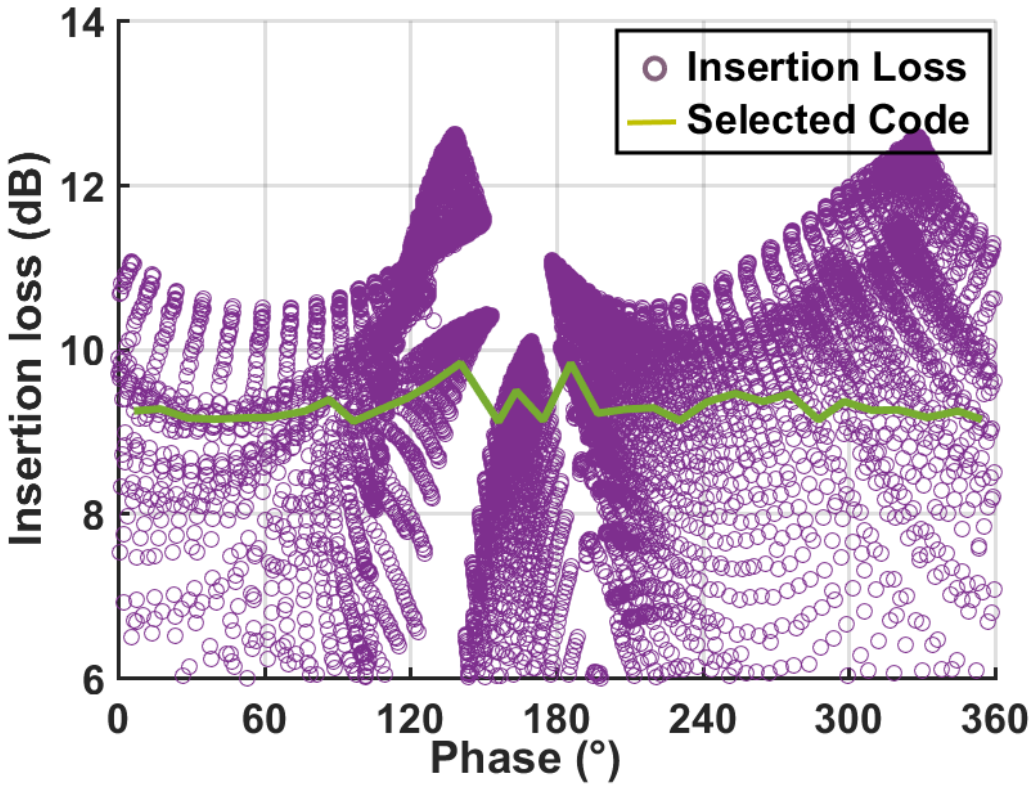

Figure 5.7: Frontend measured loss across $[C_1, C_2]$ corners and the selected output

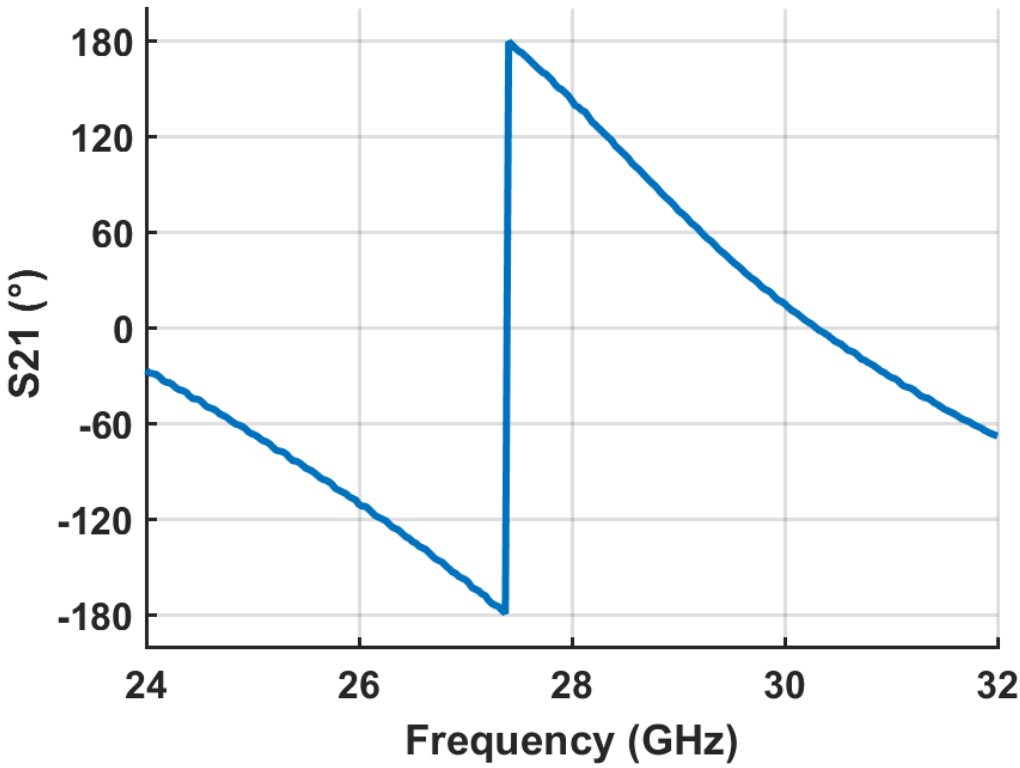

Figure 5.8: Measured S_{21} phase across frequency for $[C_{1,max}, C_{2,max}]$

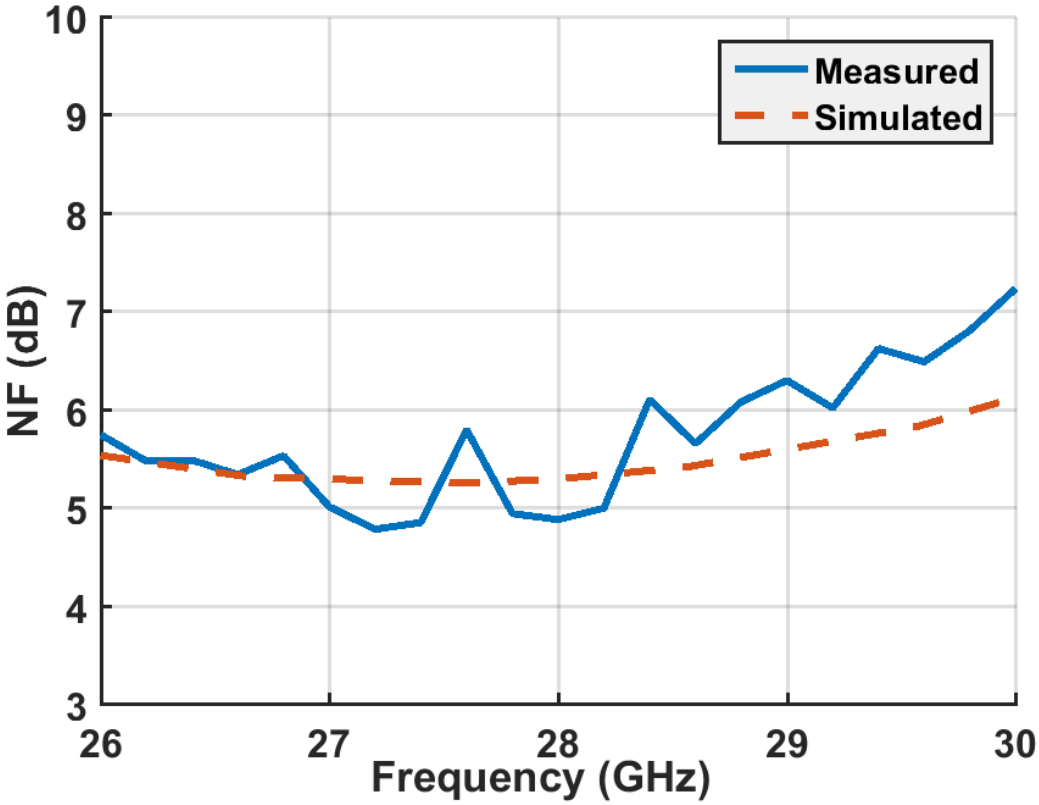

Figure 5.9: Comparison of measured and simulated noise figure for the frontend for $[C_{1,max}, C_{2,max}]$

Chapter 6: Conclusion

This work demonstrates a single-channel prototype of a integrable low-power phased-array receiver front end in 65 nm CMOS. The design and implementation of a low power phased-array receiver frontend at 28 GHz in 65 nm CMOS. The low insertion loss and fine phase resolution along with 360° phase shift range from the proposed systematic design and load optimization approach, enables the integration of passive phase shifters in emerging high data rate 5G wireless communication applications at 28 GHz. The proposed state-of-the-art RTPS with -7.75±0.3 dB insertion loss and rms phase error of 0.3° across 360° phase shift range at 28 GHz, is suitable for the accurate beamforming for Ka-band applications. Low power phased-array receiver front end demonstrates overall gain of ∼9.5±0.4 dB and measured noise figure of 4.9 dB at 28 GHz with 10 mW power consumption from a 0.9 V supply.

References

[1] M. Skolnik, *Radar Handbook, Third Edition.* McGraw-Hill Education, 2008.

[2] X. Guan, H. Hashemi, and A. Hajimiri, "A fully integrated 24-GHz eight-element phased-array receiver in silicon," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2311–2320, Dec 2004.

[3] H. Hashemi, X. Guan, and A. Hajimiri, "A fully integrated 24 GHz 8-path phased-array receiver in silicon," in *IEEE Int. Solid-State Circuit Conf. Dig. Tech. Papers*, pp. 390–534 Vol.1, Feb 2004.

[4] A. Hajimiri, A. Komijani, A. Natarajan, R. Chunara, X. Guan, and H. Hashemi, "Phased array systems in silicon," *IEEE Commun. Mag.*, vol. 42, pp. 122–130, Aug 2004.

[5] A. Babakhani, X. Guan, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon: Receiver and Antennas," *IEEE J. Solid-State Circuits*, vol. 41, pp. 2795–2806, Dec 2006.

[6] W. Roh, J. Y. Seol, J. Park, B. Lee, J. Lee, Y. Kim, J. Cho, K. Cheun, and F. Aryanfar, "Millimeter-wave beamforming as an enabling technology for 5G cellular communications: theoretical feasibility and prototype results," *IEEE Commun. Mag.*, vol. 52, pp. 106–113, February 2014.

[7] S. Rangan, T. S. Rappaport, and E. Erkip, "Millimeter-Wave Cellular Wireless Networks: Potentials and Challenges," *Proceedings of the IEEE*, vol. 102, pp. 366–385, March 2014.

[8] S. Zihir, O. Gurbuz, A. Karroy, S. Raman, and G. Rebeiz, "A 60 GHz 64-element Wafer-Scale Phased-Array with Full-Reticle Design," in *IEEEMTT-S Int. Microw. Symp. Dig.*, 2015.

[9] A. Natarajan, A. Valdes-Garcia, B. Sadhu, S. Reynolds, and B. Parker, "W-Band Dual-Polarization Phased-Array Transceiver Front-End in SiGe BiCMOS," *IEEE Trans. Microw. Theory and Techn.*, vol. 63, pp. 1989–2002, June 2015.

[10] F. Golcuk, T. Kanar, and G. M. Rebeiz, "A 90 - 100-GHz 4 x 4 SiGe BiCMOS Polarimetric Transmit/Receive Phased Array With Simultaneous Receive-Beams Capabilities," *IEEE Trans. Microw. Theory and Techn.*, vol. 61, pp. 3099–3114, Aug 2013.

[11] G. S. Shin, J. S. Kim, H. M. Oh, S. Choi, C. W. Byeon, J. H. Son, J. H. Lee, and C. Y. Kim, "Low Insertion Loss, Compact 4-bit Phase Shifter in 65 nm CMOS for 5G Applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, pp. 37–39, Jan 2016.

[12] A. Natarajan, A. Komijani, and A. Hajimiri, "A fully integrated 24-GHz phased-array transmitter in CMOS," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2502–2514, Dec. 2005.

[13] K. J. Koh and G. M. Rebeiz, "0.13-μ m CMOS Phase Shifters for X-, Ku-, and K-Band Phased Arrays," *IEEE J. Solid-State Circuits*, vol. 42, pp. 2535–2546, Nov 2007.

[14] S. Shahramian, Y. Baeyens, N. Kaneda, and Y. K. Chen, "A 70-100 GHz Direct-Conversion Transmitter and Receiver Phased Array Chipset Demonstrating 10 Gb/s Wireless Link," *IEEE J. Solid-State Circuits*, vol. 48, pp. 1113–1125, May 2013.

[15] A. Asoodeh and M. Atarodi, "A Full 360° Vector-Sum Phase Shifter With Very Low RMS Phase Error Over a Wide Bandwidth," *IEEE Trans. Microw. Theory and Techn.*, vol. 60, pp. 1626–1634, June 2012.

[16] J.-C. Wu, C.-C. Chang, S.-F. Chang, and T.-Y. Chin, "A 24-GHz full-360; CMOS reflection-type phase shifter MMIC with low loss-variation," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, pp. 365–368, June 2008.

[17] D. Parker and D. C. Zimmermann, "Phased arrays-part II: implementations, applications, and future trends," *IEEE Trans. Microw. Theory and Techn.*, vol. 50, pp. 688–698, Mar 2002.

[18] H. Zijie and K. Mouthaan, "A 0.5-6 GHz 360° vector-sum phase shifter in 0.13-μm CMOS," in *IEEEMTT-S Int. Microw. Symp. Dig.*, pp. 1–3, June 2014.

[19] T. Yu and G. M. Rebeiz, "A 4-channel 24 GHz -27 GHz CMOS differential phased-array receiver," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, pp. 455–458, June 2009.

[20] W. H. Woods, A. Valdes-Garcia, H. Ding, and J. Rascoe, "CMOS millimeter wave phase shifter based on tunable transmission lines," in *IEEE Custom Integr. Circuits Conf. Dig. Tech. Papers*, pp. 1–4, Sept 2013.

[21] W. T. Li, Y. H. Kuo, Y. M. Wu, J. H. Cheng, T. W. Huang, and J. H. Tsai, "An X-band full-360 degree; reflection type phase shifter with low insertion loss," in *42nd IEEE European Microwave Conf. (EuMC)*, pp. 1134–1137, Oct 2012.

[22] A. Natarajan, A. Valdes-Garcia, B. Sadhu, S. K. Reynolds, and B. D. Parker, " W -Band Dual-Polarization Phased-Array Transceiver Front-End in SiGe BiCMOS," *IEEE Trans. Microw. Theory and Techn.*, vol. 63, pp. 1989–2002, June 2015.

[23] D. Pozar, *Microwave Engineering*. Wiley, 2004.

[24] J. Lange, "Interdigitated Strip-Line Quadrature Hybrid," in *IEEE Trans. Microw. Theory and Techn.*, pp. 10–13, May 1969.

[25] M. D. Tsai and A. Natarajan, "60GHz passive and active RF-path phase shifters in silicon," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, pp. 223–226, June 2009.

[26] H. Krishnaswamy, A. Valdes-Garcia, and J. W. Lai, "A silicon-based, all-passive, 60 GHz, 4-element, phased-array beamformer featuring a differential, reflection-type phase shifter," in *Proc. IEEE Int. Symp. Phased Array Syst. Tech.*, pp. 225–232, Oct 2010.

[27] H. Zarei and D. J. Allstot, "A low-loss phase shifter in 180 nm CMOS for multiple-antenna receivers," in *IEEE Int. Solid-State Circuit Conf. Dig. Tech. Papers*, pp. 392–534 Vol.1, Feb 2004.

[28] M. Tabesh, A. Arbabian, and A. Niknejad, "60GHz low-loss compact phase shifters using a transformer-based hybrid in 65nm CMOS," in *IEEE Custom Integr. Circuits Conf. Dig. Tech. Papers*, pp. 1–4, Sept 2011.

[29] W. T. Li, Y. C. Chiang, J. H. Tsai, H. Y. Yang, J. H. Cheng, and T. W. Huang, "60-GHz 5-bit Phase Shifter With Integrated VGA Phase-Error Compensation," *IEEE Trans. Microw. Theory and Techn.*, vol. 61, pp. 1224–1235, March 2013.

[30] J. Y. Lyu, S. C. Huang, and H. R. Chuang, "K-band CMOS phase shifter with low insertion-loss variation," in *IEEE Proc. Asia-Pacific Microw. Conf.*, pp. 88–90, Dec 2012.

[31] C. H. Wu, W. T. Li, J. H. Tsai, and T. W. Huang, "Design of a K-band low insertion loss variation phase shifter using 0.18-μ CMOS process," in *IEEE Proc. Asia-Pacific Microw. Conf.*, pp. 1735–1738, Dec 2010.

[32] A. Bleicher, "The 5G phone future [News]," *IEEE Spectrum*, vol. 50, pp. 15–16, July 2013.

[33] E. Cohen, O. Degani, and D. Ritter, "A wideband gain-boosting 8mW LNA with 23dB gain and 4dB NF in 65nm CMOS process for 60 GHz applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, pp. 207–210, June 2012.

[34] O. Momeni and E. Afshari, "A high gain 107 GHz amplifier in 130 nm CMOS," in *IEEE Custom Integr. Circuits Conf. Dig. Tech. Papers*, pp. 1–4, Sept 2011.

[35] D. J. Cassan and J. R. Long, "A 1-V transformer-feedback low-noise amplifier for 5-GHz wireless LAN in 0.18- μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, pp. 427–435, Mar 2003.

[36] M. P. van der Heijden, L. C. N. de Vreede, and J. N. Burghartz, "On the design of unilateral dual-loop feedback low-noise amplifiers with simultaneous noise, impedance, and IIP3 match," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1727–1736, Oct 2004.

[37] J. Hogerheiden, M. Ciminera, and G. Jue, "Improved planar spiral transformer theory applied to a miniature lumped element quadrature hybrid," *IEEE Trans. Microw. Theory and Techn.*, vol. 45, pp. 543–545, Apr 1997.

[38] F. Meng, K. Ma, K. S. Yeo, and S. Xu, "A 57-to-64-GHz 0.094-mm2 5-bit Passive Phase Shifter in 65-nm CMOS," *Proc. IEEE Symp. VLSI Circuits,*, vol. 24, pp. 1917–1925, May 2016.