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With advancements in CMOS technology, high speed analog circuits that were traditionally implemented with discrete circuit components can now be made monolithically. Antialiasing filters for video signals as well as signal conditioning filters in high speed communication channels are examples of applications where high frequency integrated circuits are now feasible. Transconductance-Capacitor or Gm-C filters are well suited to these applications as they operate in the continuous-time domain and are able to overcome the high-frequency and noise limitations imposed by clocked filter topologies.

This thesis covers the design of a programmable fourth-order Chebychev filter with a 50MHz passband using the transconductance-C technique. A previously proposed transconductor based upon a CMOS inverter is used to implement the filter. Since this transconductor has no internal nodes, it can achieve extremely high bandwidths. However, it requires a variable power source for programming. Thus, a wide-band, on-chip, variable BiCMOS power supply is presented as the method for setting the transconductance. Practical design issues are addressed as well as many methods for compensating non-idealities. Simulations of the filter as well as some parametric measurement of the filter structures are presented.

A Programmable BiCMOS Transconductance-Capacitor Filter for High Frequencies

by

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A Programmable BiCMOS Transconductance-Capacitor Filter for High Frequencies

Chapter 1. Introduction

The goal of the work in this thesis is to produce a programmable lowpass filter with a passband to 50MHz. Programmability, in this context, means that some control is given to various filter parameters such as passband gain, filter Q, and cutoff frequency. In order to achieve the high bandwidth required for this filter, a continuous-time approach was selected using the transconductance-C technique.

1.1 Motivation

Many applications exist that require very high-speed integrated filters. Flash A/D converters and digital video are just two applications that require antialiasing circuitry above 10MHz. Furthermore, areas such as digital communications and data storage find uses for high-speed analog signal conditioning circuitry and equalization filters.

Many continuous-time transconductance-C filter designs have been published within the last decade [1], [3], [7-8], [10-12], [14], [16-17]. A variety of methods have been used for both transconductance elements as well as filter topologies. Passbands have been reported from several megahertz to several hundred megahertz. Automatic on-chip tuning has also been successfully used in many of the designs, mostly in filters with passbands below 20MHz.

In [14], an eighth-order transconductance-C bandpass filter is presented in full CMOS. This filter has a center frequency of 4MHz and phase-locked control circuitry to stabilize the center frequency over process variation. A cascade of four biquads was used to achieve the eighth-order Chebychev bandpass response.

In [3], the authors designed a 5-volt transconductance-C filter for the specific application of anti-aliasing for digital video processing. A seventh-order elliptic filter using a leapfrog topology was implemented and characterized. A passband of 4MHz was achieved with a signal to noise ratio of 61dB. The transconductor was constructed using a folded-cascode architecture in 1μm CMOS, and an automatic on-chip master-slave tuning scheme was included.

In [8], Khoury designed a transconductance-C filter for a disk-drive read channel. For this application, a fifth-order Bessel filter with a 15MHz passband was implemented achieving a dynamic range of 55dB and a total harmonic distortion of 41dB with a 1-volt peak-to-peak differential input. In addition, special tuning circuitry was designed to switch the filter's passband down to 6MHz. This was done to accommodate variable data rates in the read channel. The transconductor for this filter, again, uses a folded-cascode architecture but this time in a .9μm CMOS process.

In order to achieve even higher operating frequencies, Snelgrove and Shoval propose using a differential pair as the transconductor [16]. The tuning range of a biquad filter using these transconductors in a .9μm CMOS process is shown to span the VHF range from 30MHz to 450MHz. This was accomplished by switching in banks of capacitors. The dynamic range of this filter, however, is only 33dB. Manual tuning of the Q and operating frequency was used as opposed to automatic on-chip tuning.

The filter designed in [12] uses an inverter structure as the transconductance element in a third-order elliptic filter with manual tuning. Because of the simplicity of the transconductor used in the design of the filter, accurate magnitude reponse to 100MHz in a 3μm CMOS process has been achieved. More of this work is presented in Chapter 3.

This thesis proposes to implement a tunable filter with a cutoff frequency of 50MHz. Such a filter has applications in disk-drive read channels where programmable signal conditioning is sometimes desirable. To achieve programmability, manual tuning or adaptive tuning of the filter's transfer function must be viable. To this end, the proposed filter has control voltages to vary critical parameters such as cutoff frequency,

passband gain, and Q. To achieve the frequency response, the simple structure of the transconductor presented by Nauta has been employed.

1.2 Thesis Overview

This thesis covers the design and implementation of a 4th-order Chebychev low-pass filter with a passband of 50MHz. A wide-band on-chip tunable power supply is presented as well as a previously introduced high frequency transconductor. Practical design issues are addressed as are methods for compensating non-idealities.

This thesis is ordered as follows. Chapter 2 is the background section which provides a short tutorial explaining how transconductance filters work. Integrator non-idealities are discussed here as well as some methods for designing filters. Chapter 3 describes the functional blocks of the fourth-order filter and steps through the design of the transconductor and the variable power supply. The transconductor is one previously introduced by Bram Nauta [12], and is based on an inverter. The variable power supply is used to tune the transconductors and uses a bipolar transistor as the power device. Simulation results are presented to support the design procedures. Chapter 4 discusses the filter synthesis and final circuit design. Simulation results reveal the programmability of the filter in terms of frequency, gain, and Q. Experimental results are also presented in this chapter to verify some of the circuits designed in Chapter 3. Chapter 5 presents a summary of the project and draws conclusions based upon the simulations and measured results. Areas for future work are also pointed out.

Chapter 2. Background

This chapter presents the basic building block in the construction of transconductance-capacitor filters, the continuous-time integrator. Since the integrator must be implemented with practical circuits, the non-idealities encountered in the design of continuous-time integrators are explored and analyzed. Ladder and biquad filter synthesis methods are briefly discussed as well to give some idea of the tradeoffs associated with each.

2.1 The Ideal Transconductance-Capacitance Integrator

Integrators can be built simply with a voltage-to-current converter and a capacitor as shown in Figure 2.1. The describing equation for this circuit is:

$$\frac{V_o(\omega)}{V_i(\omega)} = \frac{g_m}{j\omega C}. \tag{2.1}$$

Note that the transfer function of the circuit has a pole at DC and a unity-gain frequency of g_m/C. Inherent to this transfer function is the fact that the DC gain is ∞. Also, since $\mathrm{Im}(\omega)/\mathrm{Re}(\omega)$ of such a circuit determines the Q, the Q for an ideal integrator is ∞. Many non-idealities exist, however, in the practical implementation of such a circuit, degrading ideal performance. These non-idealites are discussed in the following section.

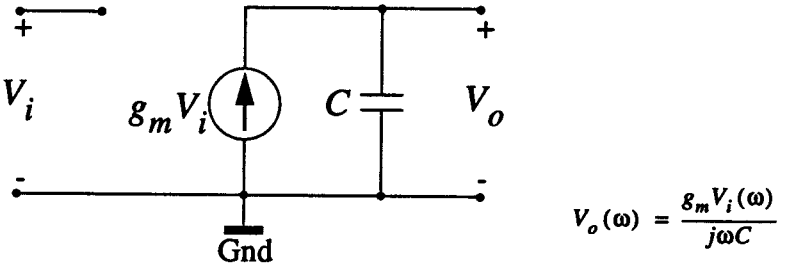

Figure 2.1: Transconductance-C Integrator.

2.2 Integrator Non-Idealities

This section will discuss the non-idealities of a transconductance-C integrator. As discussed earlier, an integrator is simply a pole at $\omega = 0$. This, however, implies that the integrator must have infinite DC gain. In addition, the phase of the integrator must lag by exactly 90 degress at all frequencies. Of course, these specifications are not achieveable with practical integrated circuit designs due to mismatches and parasitic elements. Figure 2.2 shows the magnitude and phase responses of both an ideal integrator (light lines) and a non-ideal integrator (dark lines). It is important to note, first, that the integrator cannot have infinite DC gain in practice because any transconductor used to build a contiuous-time integrator is bound to have a non-zero output conductance.

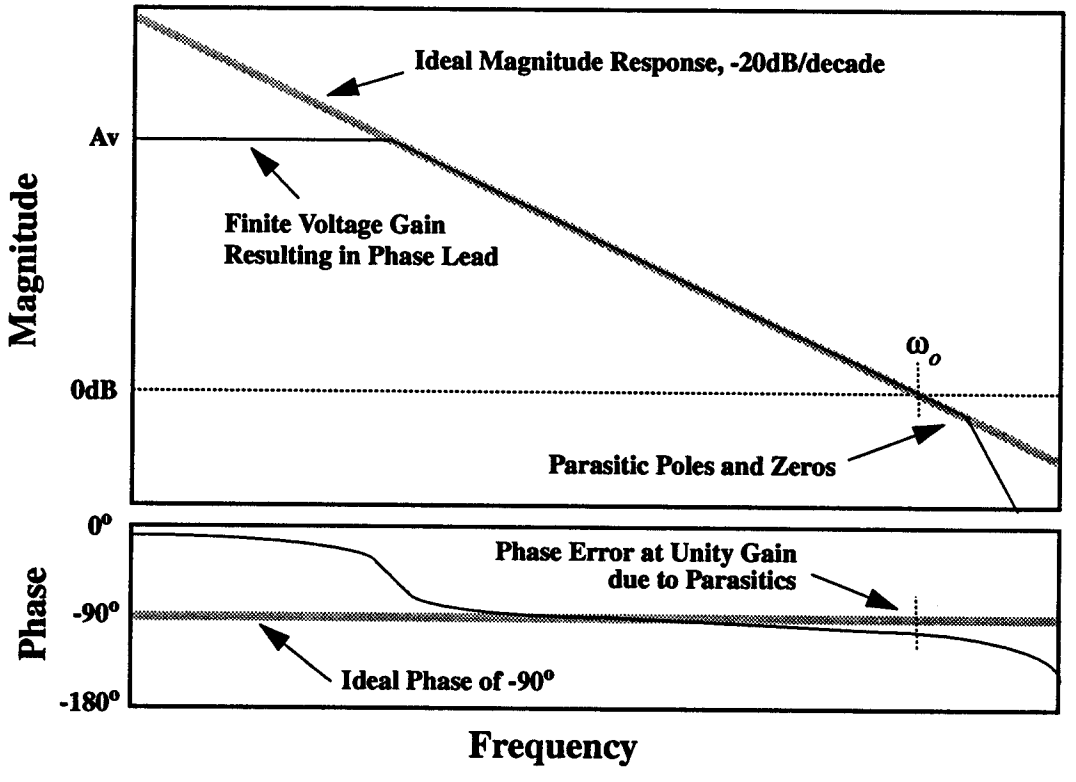

Figure 2.2: Integrator Non-Idealities.

Second, parasitic capacitances between critical nodes in the transconductor limit

its maximum achieveable bandwidth. A suitable model for describing the effects of integrator non-idealities is constructed in Figure 2.3.

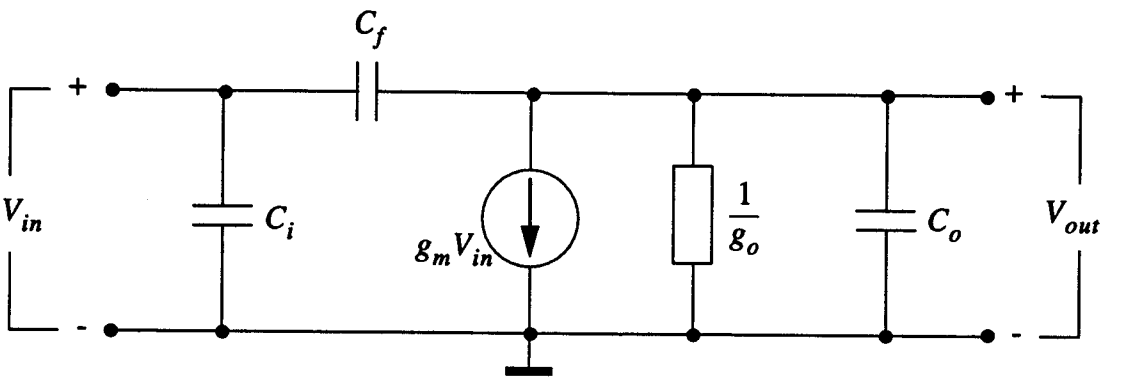

Figure 2.3: Model for the Non-Ideal Integrator.

From Figure 2.3, the Kirchhoff current equation at the output node leads to:

$$V_{out}(g_o + sC_o) = V_{in}(sC_f - g_m) - V_{out}sC_f, \tag{2.2}$$

which can be rewritten as an input-output relationship:

$$\frac{V_{out}}{V_{in}} = -\frac{g_m(1 - sC_f/g_m)}{g_o(1 + s(C_o + C_f)/g_o)}. \tag{2.3}$$

Analyzing Eq. (2.3), we find that the DC gain of the non-ideal integrator is $-g_m/g_o$. In addition, a LHP pole is produced as a result of the non-zero output conductance and its location is $\omega_{pole} = g_o/(C_o + C_f)$. Also introduced is a RHP transmission zero which is due to the feedthrough capacitance, C_f. Cleary, this zero lies at $\omega_{zero} = g_m/C_f$. Note that C_i will only add non-ideal effects if it happens to be at the filter input terminals. Otherwise, it can be considered part of the integrating capacitance of driving transconductors. Assuming the source driving the filter is 50Ω, the pole at the input is around 300MHz for an input capacitance of 10pF.

In addition to these effects, there are an infinite number of non-dominant high-frequency poles that arise from the transmission line characteristics within the MOS

transistor. In general, these poles are in the gigahertz range and do not significantly affect the operation of integrators with unity-gains in the megahertz range [12]. In fact, the dominant high-frequency limitation is imposed by the zero in Eq. (2.3). This is because the phase deviation from -90 degrees at unity-gain can be quite significant if the location of the zero lies within a factor of 100 of the unity-gain frequency. Finally, it can also be shown that the unity-gain frequency for a given transconductance, g_m, is limited by the sum of all parasitic capacitances and this frequency is:

$$\omega_u = \frac{g_m}{C_o + C_f}. \tag{2.4}$$

Clearly, from these examples of transconductor non-idealities, there is a need to make transconductors with high bandwidths and high DC gain.

2.3 Filter Networks

The ideal integrator is the core of numerous filter topologies including ladder simulation and biquadratic filters. Each synthesis method has advantages as well as disadvantages but, in general, the ladder synthesis method is preferred to biquad filters for integrated technology. In the following discussion of both types of filters, however, it will become clear why the biquad filter topology was selected for the filter design in this thesis.

2.3.1 Ladder Simulation Filters

In the design of a transconductance-capacitor filter from a given ladder prototype, a signal flow graph or element substitution may be used. Using a signal flow graph, all voltage and current relationships in the ladder prototype are implemented with transconductors and capacitors. Using element substitution, grounded and floating

inductors can be replaced by capacitively loaded gyrators and resistors can be replaced by transconductors. A simple gyrator for simulating a grounded inductor is shown in Figure 2.4.

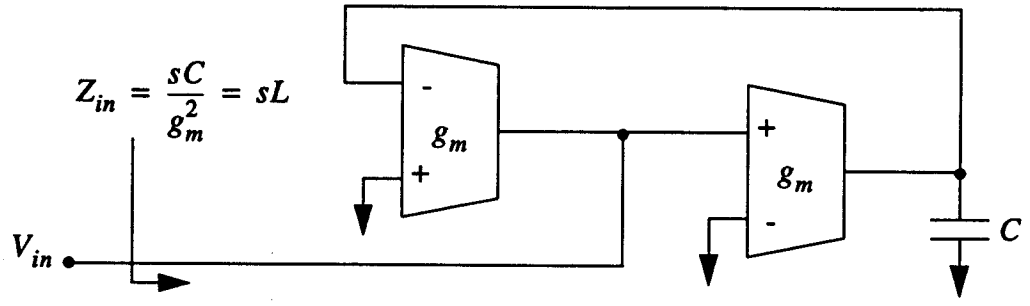

Figure 2.4: Simple Gyrator.

Ladder simulation filters have many advantages that make them suitable for integrated filter design. The synthesis method for designing ladder simulation filters is very simple and systematic. Low sensitivity to component mismatch and tolerance makes ladder simulation filters ideal for monolithic integration [15]. Finally, the ability to use identical g_m values throughout the filter allows quick design from a given prototype and eliminates multiple transconductor designs. One disadvantage, however, is that ladder simulation filters *require* an LC-ladder prototype filter. Ladder simulation filters do not easily lend themselves to programmable filters where coefficients in a transfer fuction must be individually specified. Biquad filters offer much more flexibility in terms of specifying an arbitrary transfer function.

2.3.2 Biquad Filter Structures

A 'biquad' filter structure is commonly used to implement filters that have arbitrary transfer functions. A biquad is so named because it can implement any second-order or biquadratic function within physical component limits. An advantage of the biquad is that it implements functions which are easily modified with direct tuning.

Biquad sections can also be cascaded as shown in Figure 2.5 to produce higher order functions. The expression to describe this figure is given in Eq. (2.5) where each biquad may have second order terms in both the numerator and denominator.

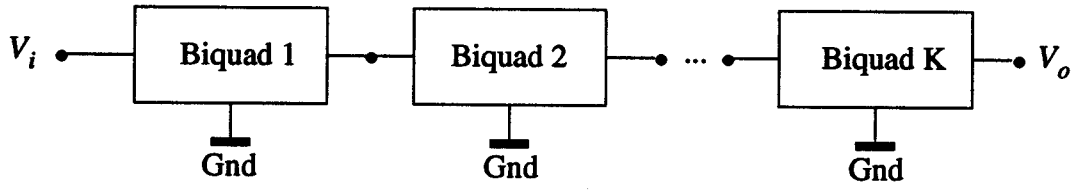

Figure 2.5: Cascade of Biquads.

$$H(s) = \frac{N(s)}{D(s)} = \prod_{i}^{K} \frac{A_i(s^2 + b_{zi}s + c_{zi})}{(s^2 + b_{pi}s + c_{pi})} \tag{2.5}$$

A physical biquad section constructed from transconductors and capacitors is shown in Figure 2.6. The biquad has one input, a lowpass output, and a bandpass output.

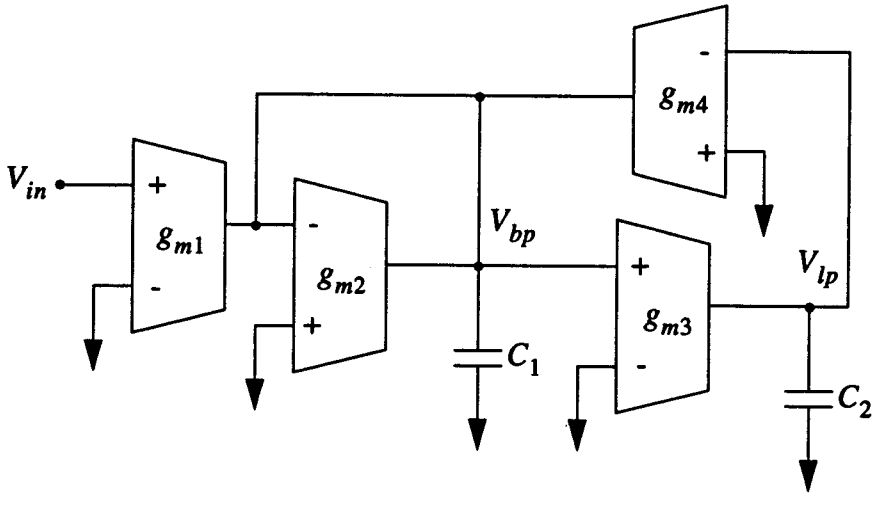

Figure 2.6: Biquadratic Section #1.

The transfer functions for the lowpass and bandpass outputs are given in Eq. (2.6) and Eq. (2.7), respectively.

$$H_{LP}(s) = \frac{\frac{g_{m1}g_{m3}}{C_1C_2}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}}, \tag{2.6}$$

and

$$H_{BP}(s) = \frac{s\frac{g_{m1}}{C_1}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}}. \tag{2.7}$$

Higher order terms in the numerator can be implemented simply by applying the input voltage to any capacitor terminal that was grounded [15]. Another biquad circuit is presented for variety in Figure 2.7. Like biquad #1, biquad #2 has two outputs,one low-pass and one bandpass. These functions are given in Eq. (2.8) and Eq. (2.9), respectively.

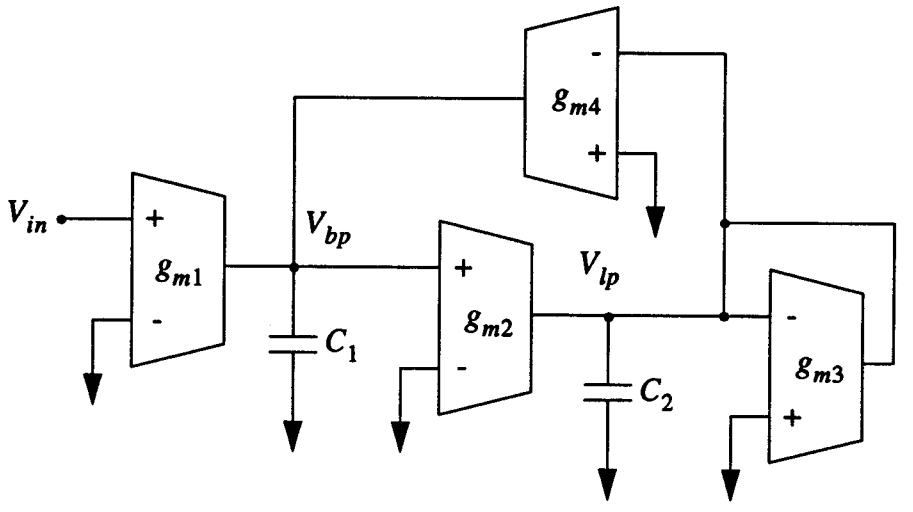

Figure 2.7: Biquadratic Section #2.

$$H_{LP}(s) = \frac{\frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + s\frac{g_{m3}}{C_2} + \frac{g_{m2}g_{m4}}{C_1C_2}}, \tag{2.8}$$

and

$$H_{BP}(s) = \frac{s\frac{g_{m1}}{C_1} + \frac{g_{m1}g_{m3}}{C_1C_2}}{s^2 + s\frac{g_{m3}}{C_2} + \frac{g_{m2}g_{m4}}{C_1C_2}}. \tag{2.9}$$

Although these two biquad circiuts do not appear to be very different from each other in function, the way that each of them is constructed can have different effects on dynamic range, DC gain error, and component matching in a filter. In any case, it is evident from both circuits that programmability is readily achieveable by simply tuning individual g_m or C values. Since the denominator of a biquad can also be written as:

$$D(s) = s^2 + s\frac{\omega_o}{Q} + \omega_o^2, \tag{2.10}$$

it is obvious that ω_o, Q, and passband gain can each be controlled independently by tuning individual g_m values.

Although biquad filters are easily programmed, they are not without shortcomings. First, biquads are more sensitive to g_m and C errors than are ladder simulation filters. Highly accurate integrated filter functions are difficult to achieve, especially with higher order and high Q filters. Second, cascaded biquad sections tend to load one another at high frequencies, again making accurate filters difficult to realize.

Chapter 3. Design of the Functional Blocks

In this chapter, the design of the functional blocks of a fourth-order Chebychev filter will be presented. These two blocks are the transconductance-C integrator and the on-chip power supply. The actual filter design will be discussed in Chapter 4. Throughout the design of these blocks, the main objective is to make the filter operate successfully at the highest possible frequency.

3.1 The Transconductance-C Integrator

High quality integrators are the foundation for any successful filter design. As discussed in Chapter 2, however, the ability to produce such integrators in silicon is hampered by a myriad of design constraints. Factors such as non-zero drain conductance, parasitic capacitance, and device nonlinearity greatly limit how ideal an integrator can be made. These innate characteristics will always result in performance sacrifices such as lower integrator DC gain, reduced bandwidth, and increased distortion. The following design of a transconductance-C integrator is based upon the design proposed by Nauta. This approach was selected for its ability to produce filters with passbands exceeding 100MHz in a 3μm CMOS technology.

Since the targetted bandwidth of the proposed filter is about 50MHz, some integrator properties are of particular interest. First, the integrator should have a high DC gain as suggested in Chapter 2. This will reduce the amount of positive phase error created at the unity-gain frequency by the dominant low-frequency pole. The integrator should also be fast. In other words, the unity-gain bandwidth of the integrator needs to be greater than 50MHz to realize passbands at that frequency. As the filter will operate at such a high frequency, the dominant high-frequency zero as found in Chapter 2 should be made as high as possible by reducing the value of any feedthrough capacitance from the input to the output. In fact, all parasitic poles or zeros should lie at least a factor of

100 beyond the integrator's unity-gain frequency so as not to introduce excessive negative phase error. Another property the integrator must possess is tunability. Although it is conceiveable for tuning to take place through either the transconductance or the capacitive elements, it is generally much easier and more practical to apply tuning to the transconductors, [15]. Tunability provides a means of cancelling all on-chip component tolerances as well as aging and temperature effects. Secondary considerations include the dynamic range and the linearity of the transconductor. Since these requirements are usually somewhat relaxed for high-speed communication channels, optimizations for them are not as important.

3.1.1 Transconductance Methods.

Many methods exist in the literature for converting an input voltage into a proportional output current [1], [8], [16]. A common OTA such as the one shown in Figure 3.1 may seem to be an attractive choice for high frequency applications as it is a simple, one-stage design. However, the DC gain of this amplifier is limited and

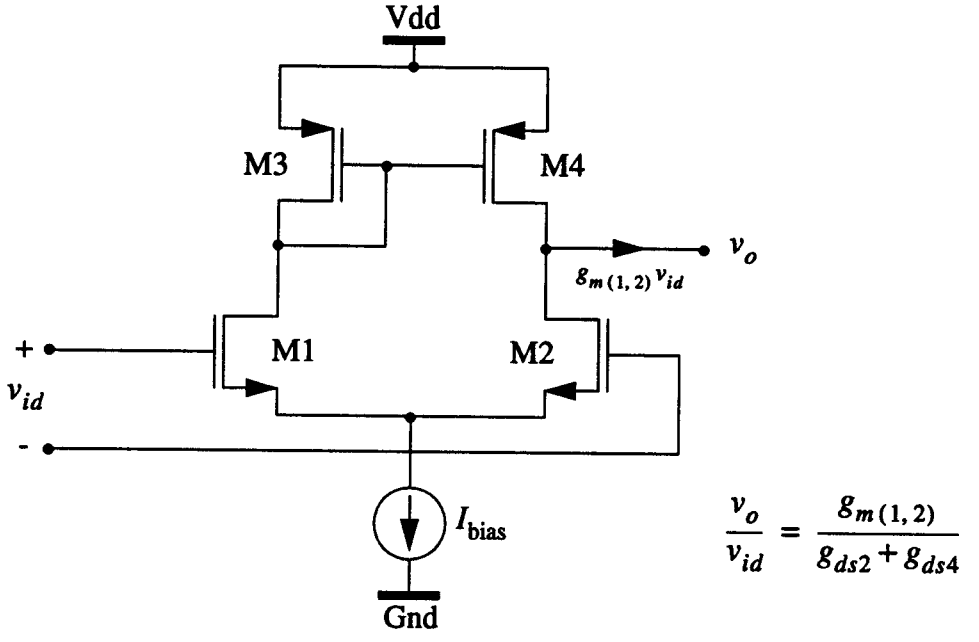

Figure 3.1: Operational Transconductance Amplifier.

unacceptable for filter applications which typically require more than 40dB of DC gain. Another problem with this amplifier is the fact that it is single-ended. Differential circuitry is critial in reducing power supply coupling and common-mode noise at high frequencies.

The folded-cascode OTA in Figure 3.2 exhibits a very high DC gain, but it also has many parasitic poles which limit its effective bandwith for use as a high-frequency continuous-time integrator [5]. Isolated signal-carrying nodes at the sources of transistor M7 and M8 as well as the node at the drain of M5 each contribute a parasitic pole that will tend to cause negative phase shift at the integrator's unity-gain frequency. These parasitic poles are typically located around a gigahertz indicating that this transconductor could be suitable for filters between 10 and 20 megahertz.

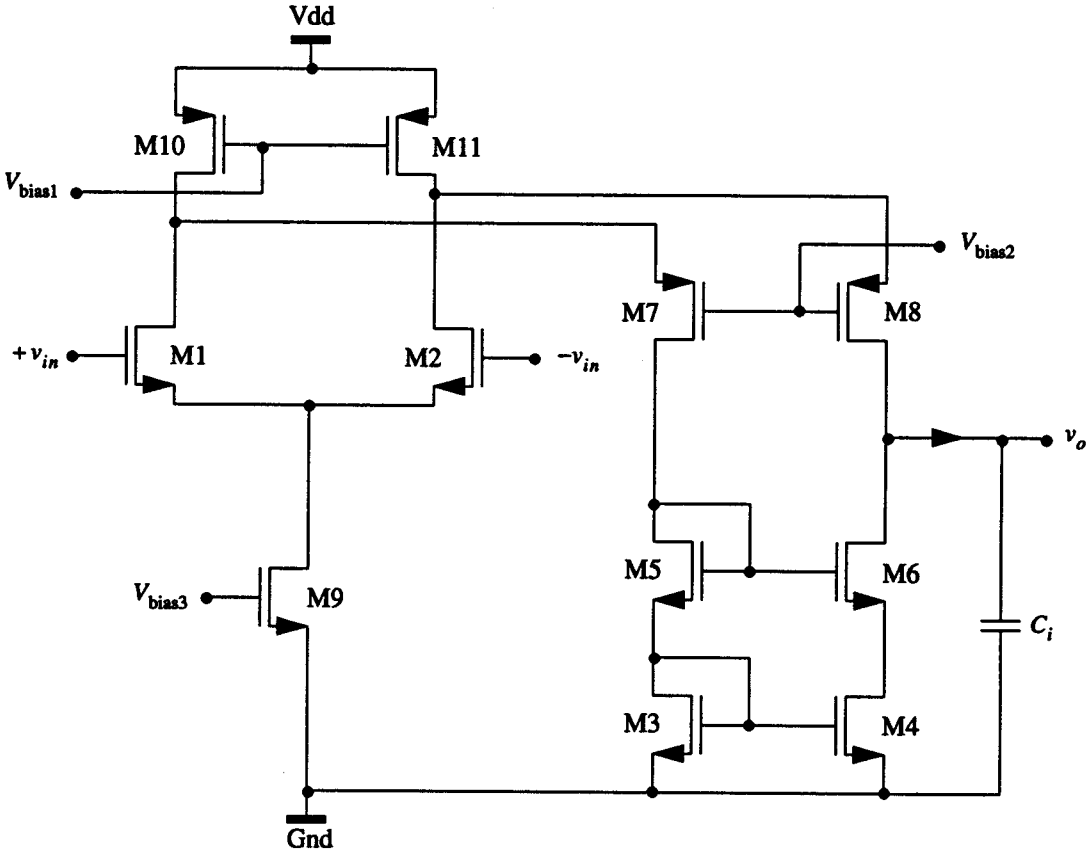

Figure 3.2: Folded-Cascode OTA.

For high-frequency applications, simple structures prove to be the most effective in achieving high gain-bandwidth products with relatively little phase error at unity-gain. Consider the inverter of Figure 3.3. Since the input and output make up the only nodes in the circuit (apart from power and ground), there are no internal nodes. What this means is that the only parasitic elements in the structure arise from the non-zero transit times in the MOS transistors and the gate-to-drain overlap capacitances connecting the input to the output. As stated before, the intrinsic time constants within the MOS transistor produce poles which are typically located in the gigahertz range. These poles do not affect the operation of the filter in the megahertz range. The dominant limiting factor at high frequency is, therefore, the gate-to-drain overlap capacitance of the n-type and p-type transistors.

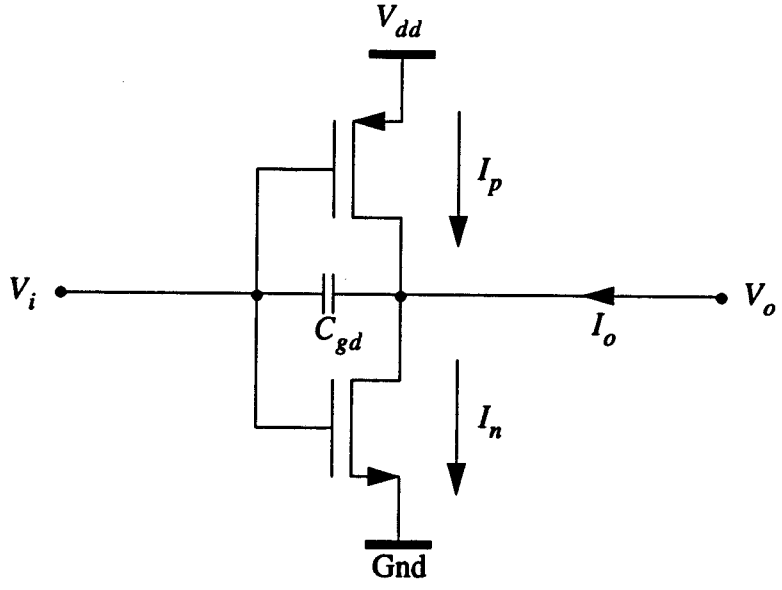

Figure 3.3: Inverter Transconductor.

The synthesis of a high-frequency voltage-to-current converter based on the inverter begins with current summing at the output node. If the output voltage, V_o, and the input voltage, V_i, of the inverter both sit at a common-mode level of approximately $V_{dd}/2$, then both transistors will operate in saturation and strong inversion making the

relations for the transistor currents around that common-mode level easily obtainable. For the p-channel device:

$$I_p = \frac{\beta_p}{2}(V_{dd} - V_i - |V_{T_p}|)^2, \tag{3.11}$$

where $\beta_p = \mu_p C_{ox}(W_p/L_p)$ and V_{T_p} is the threshold voltage of the p-channel transistor. Likewise, for the n-channel device:

$$I_n = \frac{\beta_n}{2}(V_i - V_{T_n})^2, \tag{3.12}$$

where $\beta_n = \mu_n C_{ox}(W_n/L_n)$ and V_{T_n} is the threshold voltage of the n-channel transistor. Thus, the output current is simply:

$$I_o = I_n - I_p. \tag{3.13}$$

Substituting Eq. (3.11) and Eq. (3.12) into Eq. (3.13), we have a quadratic in V_i:

$$I_o = aV_i^2 - bV_i - c \tag{3.14}$$

where $a = (\beta_n - \beta_p)/2$ and $b = \beta_n V_{T_n} - \beta_p(V_{dd} - |V_{T_p}|)$. We will see that the value of c is not important as it is cancelled in the next step. Note that Eq. (3.14) is not a linear voltage-to-current conversion. The conversion can be made linear, however, if a differential inverter pair is used instead of a single-ended inverter. This circuit is shown in Figure 3.4. Substituting a differential input, $V_{cm} \pm V_{id}$ for V_i in Eq. (3.14) and taking the difference between the inverter output currents it can be shown that the constant term, c, is cancelled, and that a linear expression results:

$$I_{od} = V_{id}(2aV_{cm} - b). \tag{3.15}$$

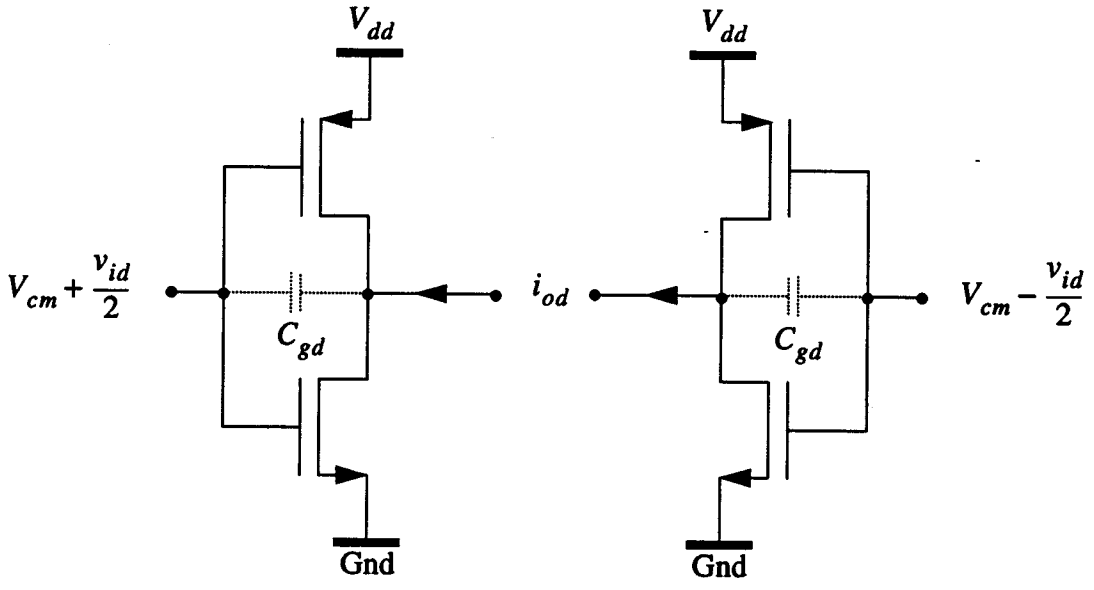

Figure 3.4: Differential Inverter Transconductor.

This linearization technique is commonly known as "square-law linearization". It follows that the transconductance of this circuit is given by:

$$g_m = 2aV_c - b. \tag{3.16}$$

Replacing a and b with their previous values in Eq. (3.14) and assuming that β_n can be made equal to β_p through proper device ratioing, the expression for g_m is simply:

$$g_m = -\beta\left(V_{dd} - V_{T_n} - |V_{T_p}|\right). \tag{3.17}$$

Even if β_n cannot be made equal to β_p, it has been shown by Nauta that the transconductance, g_m, is still linear where β is simply the geometric mean of β_n and β_p. Note that the value of g_m has a dependence upon V_{dd}. This dependence is used to tune the transconductance of this circuit. Figure 3.5 shows the complete integrator circuit with inverters 1 and 2 representing the differential structure presented in Figure 3.4 and inverters 3 through 6 comprising the common-mode control. Note that this additional

common-mode control circuitry does not introduce any additional nodes to the circuit and the good frequency properties of the differential inverter are thus preserved. Also note that inverters 1, 2, 3, and 6 have a common supply voltage, Vdd1, which is used to set the transconductance while inverters 4 and 5 have a separate supply, Vdd2, to control these transconductances independently. The reasons for this will become clear in the explanation of the common-mode control and DC gain enhancement.

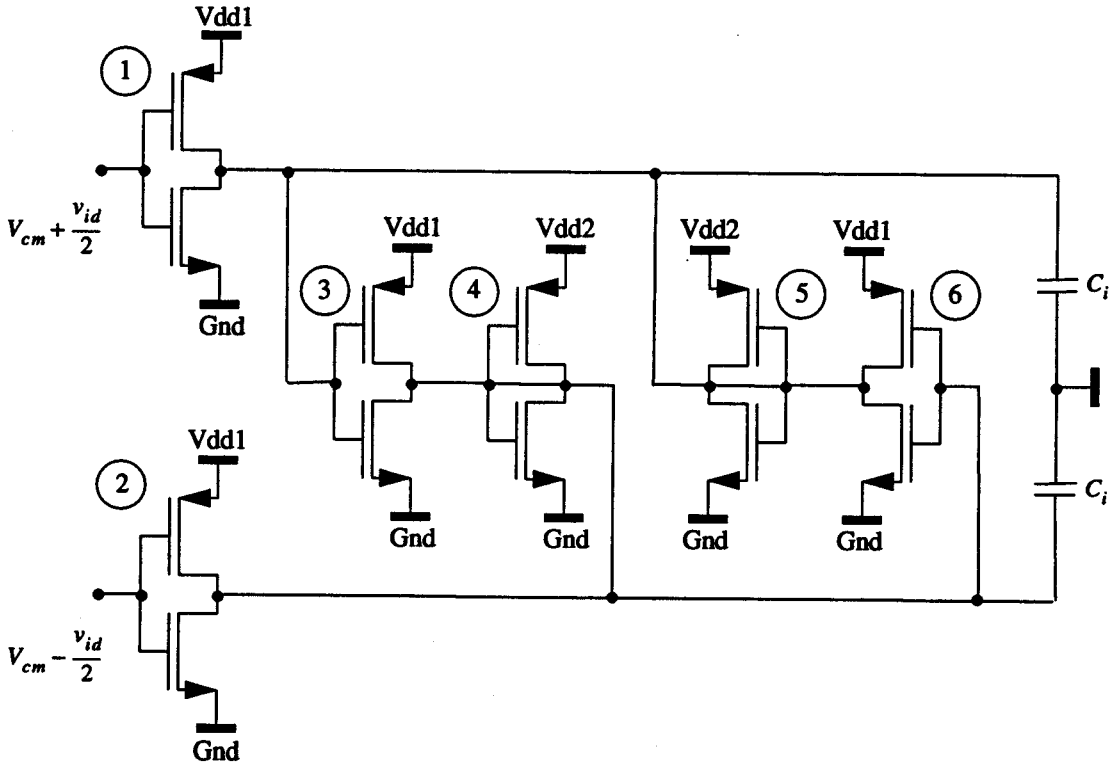

Figure 3.5: Complete Transconductor Circuit.

The idea of the common-mode control circuitry is to provide a very high impedance between the output terminals for differential signals, while maintaining a very low impedance between the output terminals for common-mode signals. With the aid of Figure 3.6 and Figure 3.7 the analysis for both types of signals is presented. In these figures, only a half-circuit of the common-mode control is shown and inverters 3 and 4 are modelled as transconductors. Figure 3.6 illustrates the case when there is a common-

mode signal at the output nodes. Both output terminals have the same

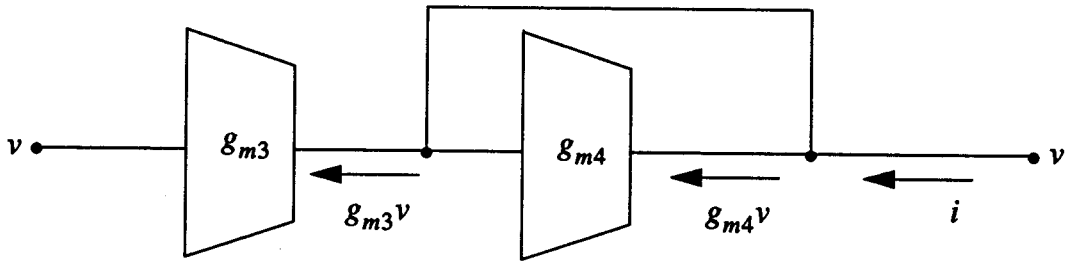

Figure 3.6: Common-mode Control (common-mode Signals).

voltage, v, and there is an impedance seen from one output terminal to the other. This impedance is equivalent to v/i in the figure and when solved for yields a low impedance:

$$Z = \frac{1}{g_{m3} + g_{m4}}. \tag{3.18}$$

Figure 3.7 shows the same analysis for differential signals and the impedance seen between the output terminals for this case is:

$$Z = \frac{1}{g_{m4} - g_{m3}}. \tag{3.19}$$

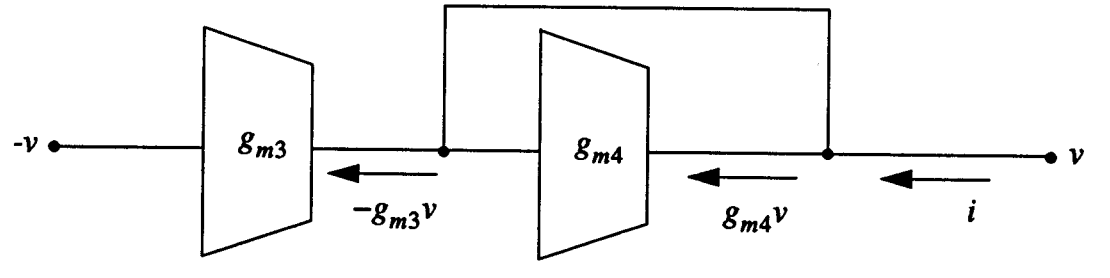

Figure 3.7: Common-mode Control(Differential Mode Signals).

Eq. (3.19) is quite useful due to the subtraction in the denominator. It is obvious

that the differential mode resistance can be made infinite if inverter 3 is perfectly matched to inverter 4. Furthermore, if the transconductance of inverter 3 is slightly greater than that of inverter 4, the differential resistance of the common-mode network is made negative. This negative impedance on the output nodes can then be used to cancel the output impedance of inverters 1 and 2, thus providing a high DC gain. Figure 3.8 shows how the DC gain can theoretically be made infinite by loading the output terminals with an equivalent g_o of negative value. In the circuit, this can be accomplished by ratioing the sizes of inverters 3 and 6 slightly larger than those of inverters 4 and 5 in Figure 3.5. In addition, the use of a separate supply voltage for inverters 4 and 5 in Figure 3.5 will allow fine tuning of the negative output impedance, $-g_o$.

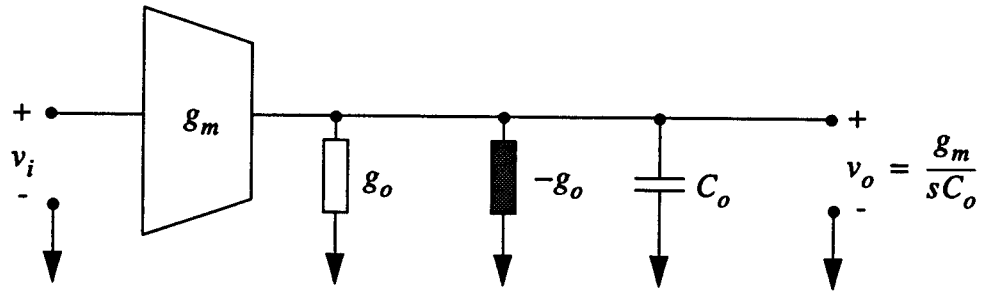

Figure 3.8: DC Gain Enhancement via Negative Impedance.

Of course, there is a limitation to the amount of gain that can be achieved using this technique. This level of performance is dependent upon the matching between the transconductors and the precision with which inverters 4 and 5 can be tuned. For this application, all tuning voltages are manual and, thus, assumed to be accurate, so the maximum DC gain will be limited solely by matching. If the net output impedance becomes negative, the stand-alone integrator will become unstable due to the RHP pole. However, a filter built with such transconductors will only become unstable if the filter Q becomes negative or infinite [11].

For this filter design, the transconductor described in [12] is used. This transconductor exhibits extremely good high-frequency characteristics and is suitable for high

frequency filters. This particular transconductor also has a simple means of tuning the value of its transconductance. Transistor sizes for this transconductor design are given in Table 1 and the motivation for the particular size ratios are given here. The design of the transistor sizes begins with making all channel lengths in the circuit the minimum size of 2μm. This is done to reduce as much gate-to-source capacitance as possible so as to achieve the highest possible unity-gain frequency. Next, the widths for inverters 1 and 2 are selected to give a transconductance that corresponds to a reasonable capacitor value[1] in the construction of an integrator with a 50MHz unity-gain frequency. Assuming a small integrating capacitor of 2pF, and a tuned supply voltage of 4 volts, a 50MHz unity-gain frequency requires a transconductance of 628μA/V. Solving for the size of the n-channel transistor using Eq. (3.17), we have:

$$W = \frac{2\mu m\,(628\frac{\mu A}{V}) / (49.8\frac{\mu A}{V^2})}{(4 - 0.844 - 0.944)\,V} \cong 11\mu m \qquad (3.20)$$

Since the mobility of the p-channel devices are about three times as small as that of the n-channel devices in this process, they were ratioed 3 times as large. Overall, however, the sizes for these inverters were kept as small as possible to reduce the amount of parasitic feedthrough capacitance from the gate to the drain. Next, the values for inverters 4 and 5 were chosen. These widths were originally selected to be minimum size, however, subsequent simulations showed that distortion could be reduced with larger than minimum size transistors for these inverters. The sizes for the transistors in inverters 3 and 6 were chosen slightly larger than those in inverters 4 and 5 to enhance the DC gain of the transconductor as explained previously. The transconductor schematic is duplicated here for clarity, and layout of the transconductor cell is shown in Appendix A, Fig. A.2, as a subcell to a biquad section.

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1. A reasonable capacitor value for the process used is $1pF < C < 5pF$.

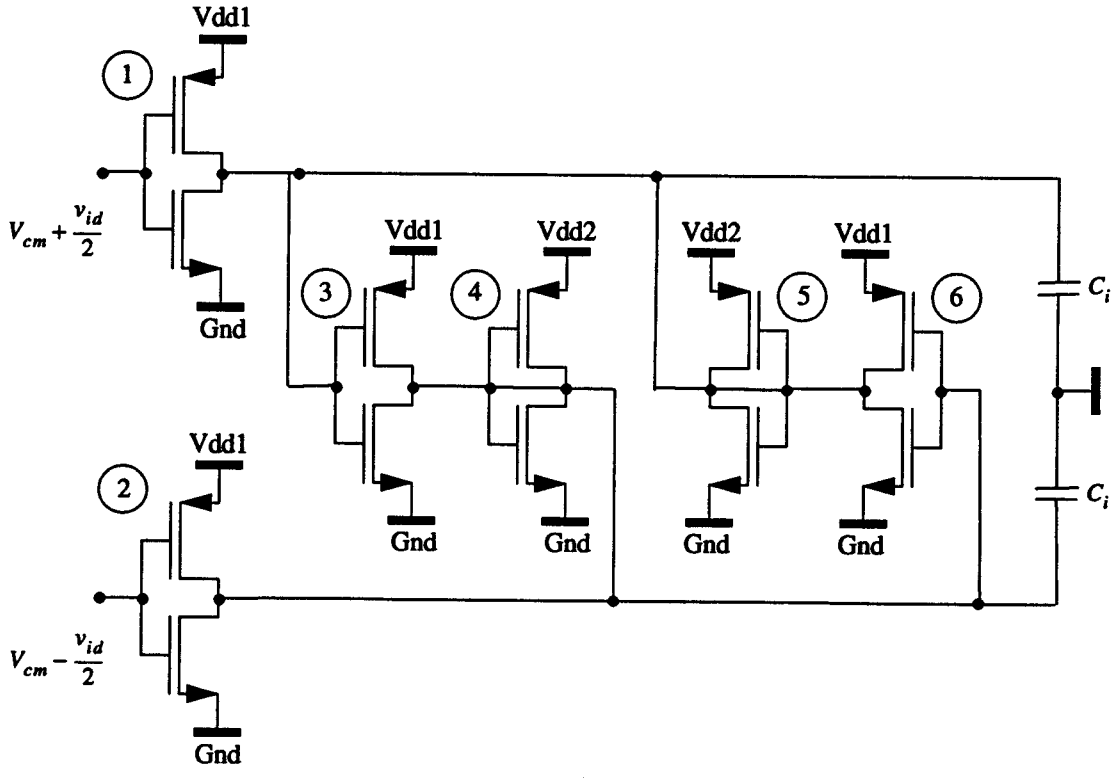

Figure 3.9: Complete Transconductor Circuit.

Table 1: Transistor Dimensions (W/L) for the Transconductor Circuit.

Transistor W/L, (μm)	p-channel	n-channel
Inverters 1 & 2	$\frac{33}{2}$	$\frac{11}{2}$
Inverters 3 & 6	$\frac{24}{2}$	$\frac{8}{2}$
Inverters 4 & 5	$\frac{18}{2}$	$\frac{6}{2}$

This transconductor circuit was also simulated using HSPICE to verify that the transconductance was close to the designed value and to measure the performance of the

DC gain enhancement. Figure 3.10 shows how the transconductance of the circuit can be changed simply by varying the value of V_{dd1}. Note that the transconductance values are slightly higher than what was predicted by Eq. (3.20). This is due to the fact that simulations included the effects of process variation, i.e. delta length and width.

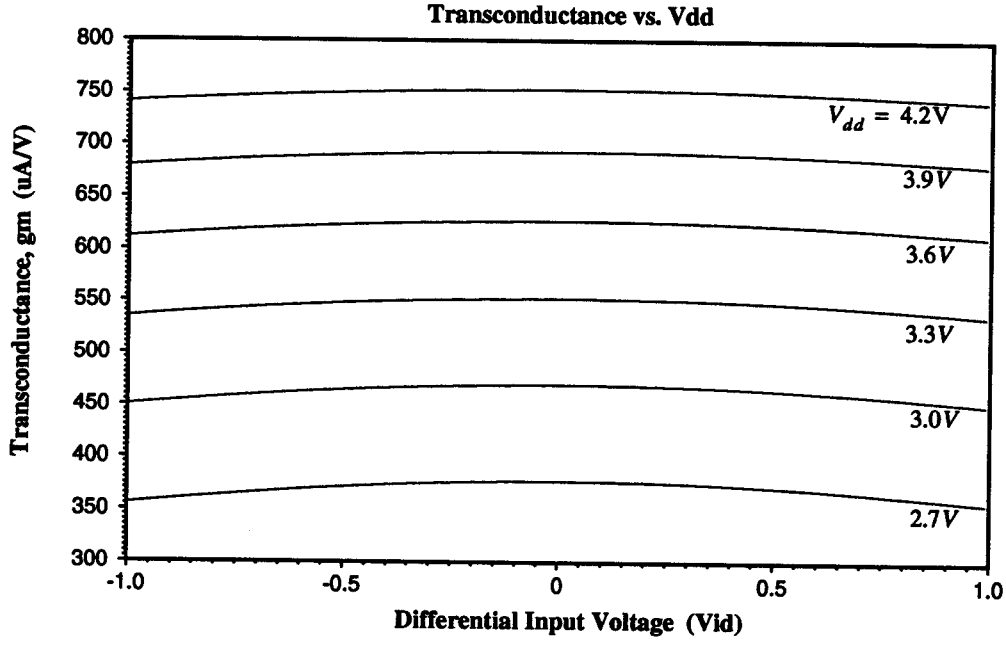

Figure 3.10: Simulated Transconductance Values.

Figure 3.11 shows how the DC gain of the transconductor can be increased by fine-tuning the transconductance of inverters 4 and 5 with the value of V_{dd2}. The sensitivity of the DC gain to mismatch is also shown in Figure 3.12. A 0.05% mismatch in the transistor lengths for inverters 1 and 2 causes the DC gain to fall from 75dB to 48dB. Note that a further 0.05% increase in the mismatch between transistor sizes only causes the gain to drop another 4dB.

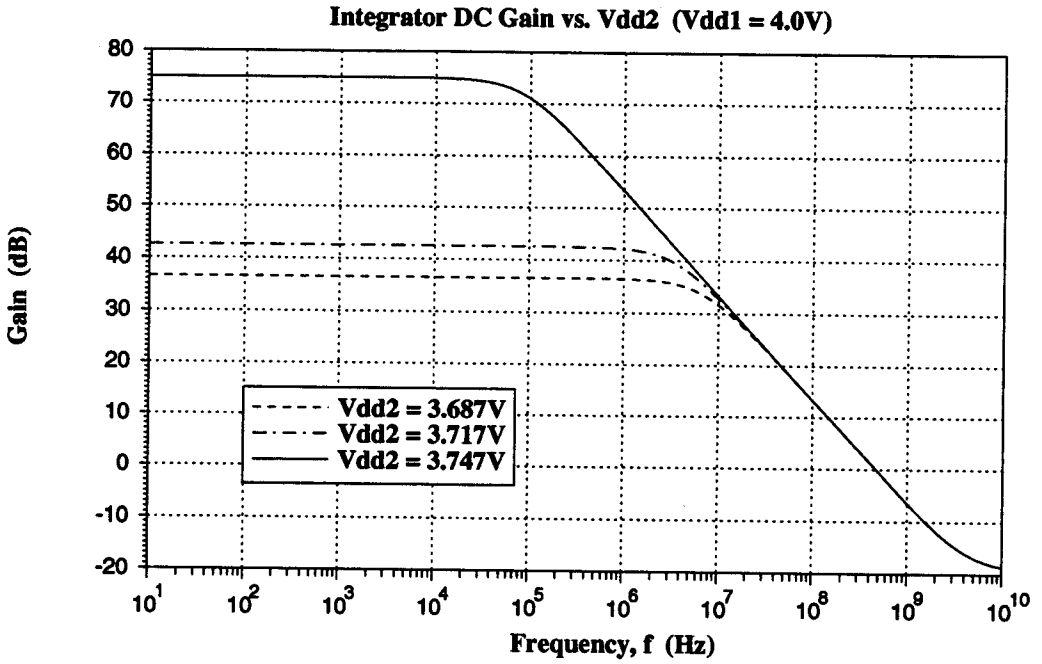

Figure 3.11: Simulation of the Transconductor showing Tunable DC Gain.

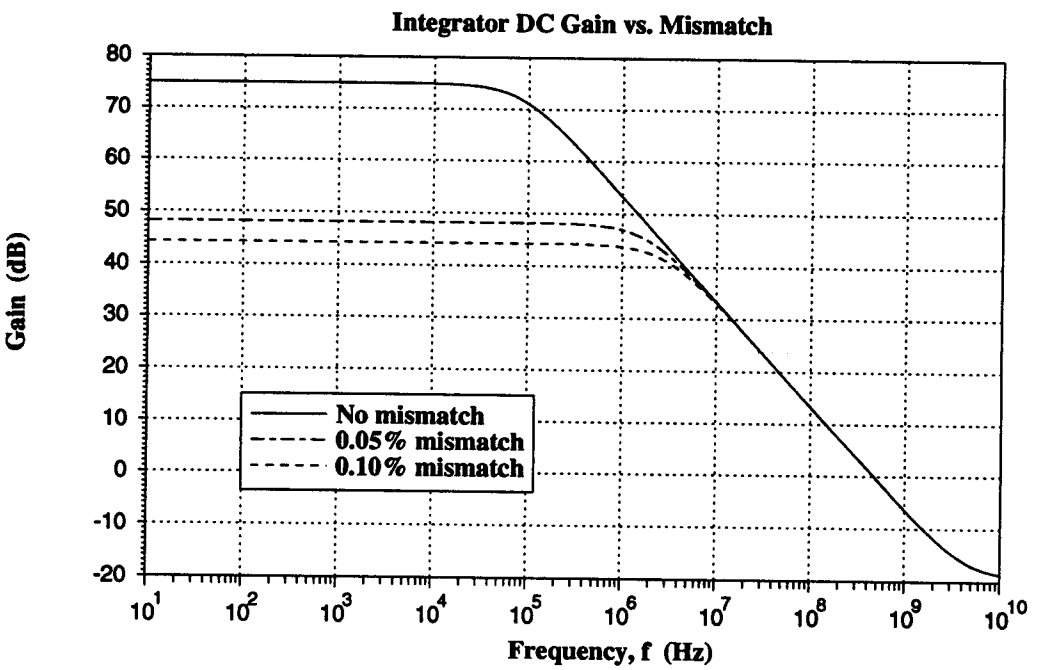

Figure 3.12: Simulation of Transistor Length Mismatch in the Transconductor.

3.1.2 *High Frequency Considerations*

Figure 3.13 shows the complete high frequency model of the differential transconductor. C_i is the input capacitance of the integrator resulting from the gate-to-source capacitances of inverters 1 and 2. C_f is the aforementioned feedthrough capacitance associated with the gate-to-drain overlap capacitances of inverters 1 and 2. C_d is the differential capacitance seen between the output nodes of the transconductor and is comprised of the gate-to-drain overlap capacitances of inverters 3 and 6. Finally, C_o is the output capacitance or integrating capacitance. This value is made up of the gate-to-source capacitances of inverters 3-6 and the drain-to-backgate capacitances of all inverters. It is with this model that a simple equation describing the high frequency effects of all the various parasitics can be determined.

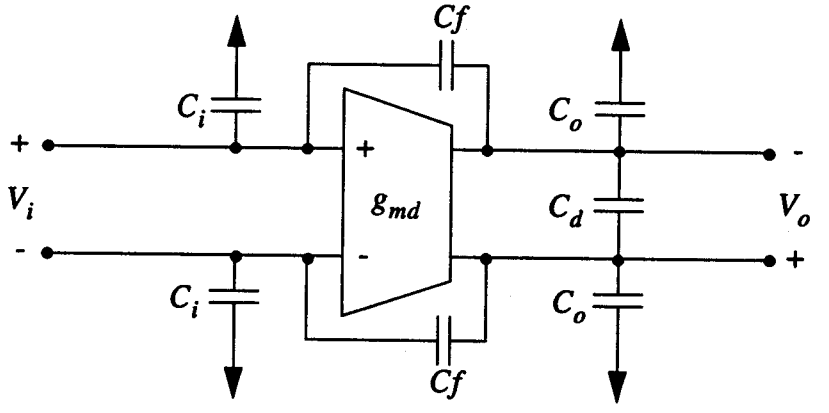

Figure 3.13: High Frequency Model of the Transconductor.

In the following analyses, it will be shown that the parasitic capacitors, C_f and C_d, simply shift the position of the unity-gain frequency, while the RHP zero created by C_f can be cancelled by adding small capacitances to the circuit. Figure 3.14 shows the single-ended version of Figure 3.13 for finding the high frequency transfer function of the non-ideal transconductor. The input capacitor has been left out of the single-ended

model because it can usually be considered to be lumped with the integrating capacitor of a driving transconductor. The differential capacitance, C_d, has been doubled and grounded to make the circuit single-ended. Also in this analysis, the output conductance, g_o, is assumed to be nulled by the DC gain enhancement circuitry.

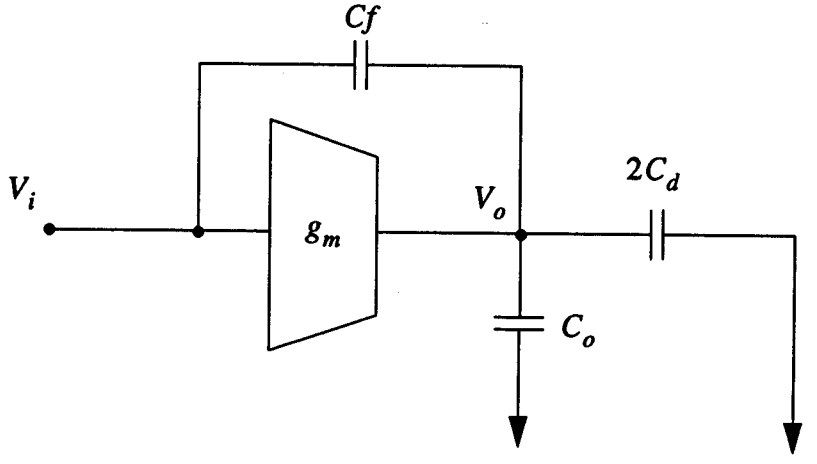

Figure 3.14: Single-ended Transconductor with Parasitics.

Summing currents at V_o gives:

$$g_m V_i + (V_i - V_o)\, sC_f = V_o s\,(C_o + 2C_d) \tag{3.21}$$

Rearranging Eq. (3.21) into the form of a transfer function, we have:

$$\frac{V_o}{V_i} = -\frac{1 - s\,(C_f/g_m)}{s\,((C_o + C_f + 2C_d)/g_m)}. \tag{3.22}$$

Equation (3.22) reveals that the effective differential capacitance, $2C_d$, is simply added to the integrating capacitor to shift the unity-gain to a lower frequency. C_f is also added to the integrating capacitor resulting in the same sort of effect but also introduces the RHP zero as discussed in Chapter 2.

The input impedance of the integrator is also affected by the feedthrough capaci-

tance. Solving for the input impedance to the circuit in Figure 3.14, we have:

$$Z_{in} = \frac{1 + (C_d + C_o)/C_f}{g_m(1 + s(C_d + C_o)/g_m)}. \tag{3.23}$$

At frequencies below $g_m/(C_d + C_o)$, the value of the impedance can be approximated by a resistance of:

$$R_{in} \cong \frac{C_d + C_o}{g_m C_f}. \tag{3.24}$$

In a filter, this will cause loading effects between transconductors resulting in filter gain errors and roll-off errors at the passband edges. Although this undesirable effect could be compensated in a filter by the DC gain enhancement circuitry of a preceeding transconductor, each transconductor in the circuit would need its own tuned DC gain control. Compensation for this nonideal effect has not been implemented, thus, errors can be expected in the passband for a filter built with this integrator. However, a theoretical way to compensate the feedthrough-induced phase caused by the RHP zero has been achieved.

We have shown that a RHP zero exists in the transconductor due to a feedthrough capacitance, C_f, connecting the non-inverting input to the inverting output of the integrator. This zero is the most dominant parasitic beyond the unity-gain frequency and its corresponding negative phase shift at the unity-gain frequency is significant if the two frequencies are within a factor of 100 of each other. This feedthrough capacitance is given by the gate-to-drain overlap capacitances in inverters 1 and 2 and is on the order of 20fF. Figure 3.15 shows these parasitics in the transconductor (C_f) as well as capacitors that are used to compensate for the unwanted phase effects (C_c).

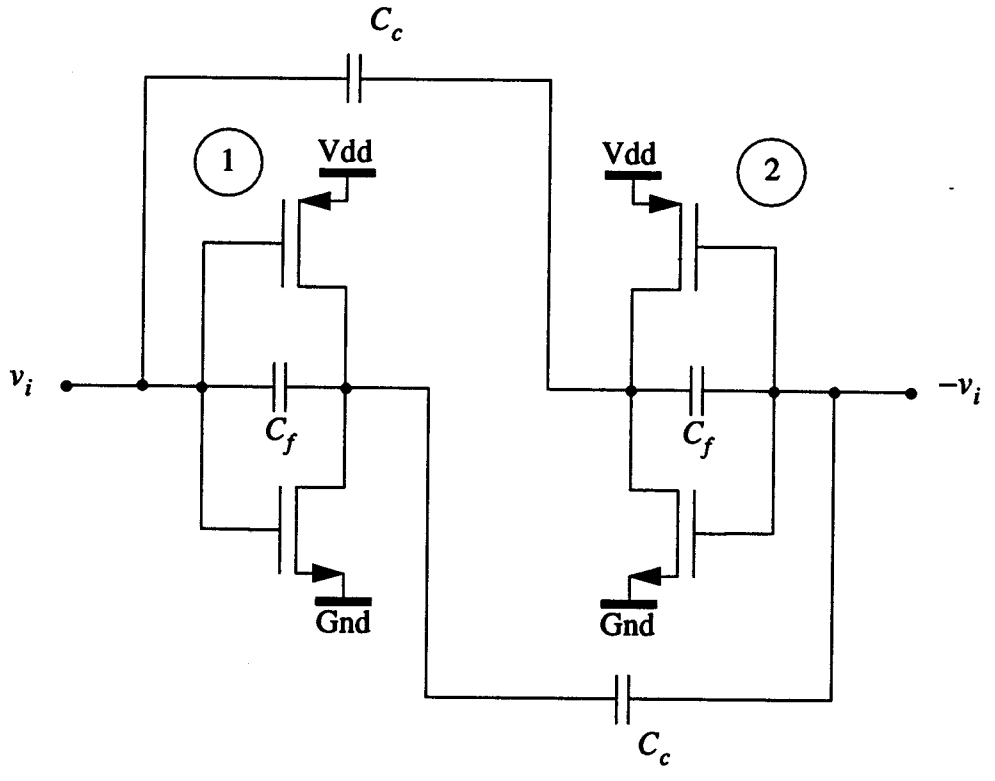

Figure 3.15: Differential Inverter with Compensation Capacitors.

Again, representing the inverter as a simple transconductor and analyzing only half of the circuit, we can illustrate the compensating effect of C_c.

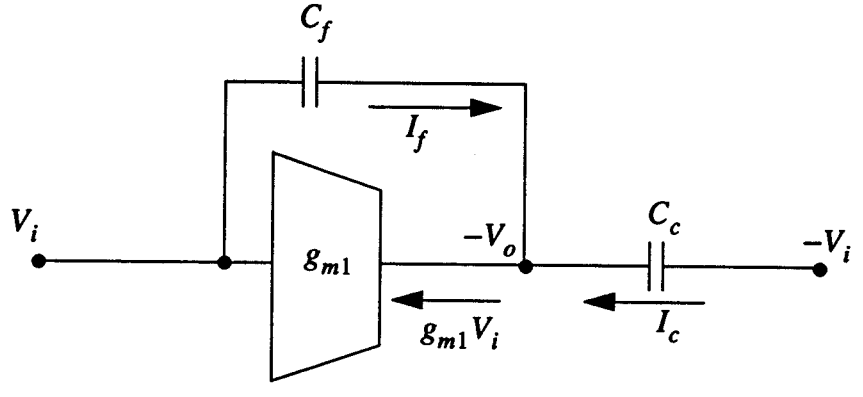

Figure 3.16: Single-Ended Analysis of Figure 3.15.

Summing currents at the $-V_o$ node in Figure 3.16 we have:

$$g_{m1}V_i = (V_o - V_i)sC_c + (V_o + V_i)sC_f, \tag{3.25}$$

and, solving Eq. (3.25) for a V_o/V_i relationship, we get:

$$\frac{V_o}{V_i} = -\frac{g_m + s(C_c - C_f)}{s(C_c + C_f)}. \tag{3.26}$$

Thus, if the value of the compensating capacitance, C_c, can be made the same as the parasitic capacitance, C_f, the feedthrough zero is completely cancelled. The only other effect that is brought about by the additional compensation capacitance is, again, a downward shift in the unity-gain frequency. The compensation capacitor simply appears as though it were in parallel with the integrating capacitor, so the unity-gain frequency is reduced accordingly. Previously, the unity-gain frequency was given in Eq. (2.4). The new unity-gain frequency, with the introduction of the compensation, becomes:

$$\omega_u = \frac{g_m}{C_o + C_f + C_c + C_d} \tag{3.27}$$

So, the unity gain frequency is affected by all but the input capacitance, C_i. As transconductors are cascaded, however, C_i usually appears as a load to one or more other transconductors. To show that this technique for compensating the effects of the feedthrough capacitance is valid, HSPICE simulations were performed to show the compensation of the excess phase at high frequencies. Figure 3.17 shows how the excess phase of the RHP zero is compensated with the addition of 25fF capacitors to the transconductor. This value was determined by looking in the HSPICE output file for the gate-to-drain capacitances in inverters 1 and 2.

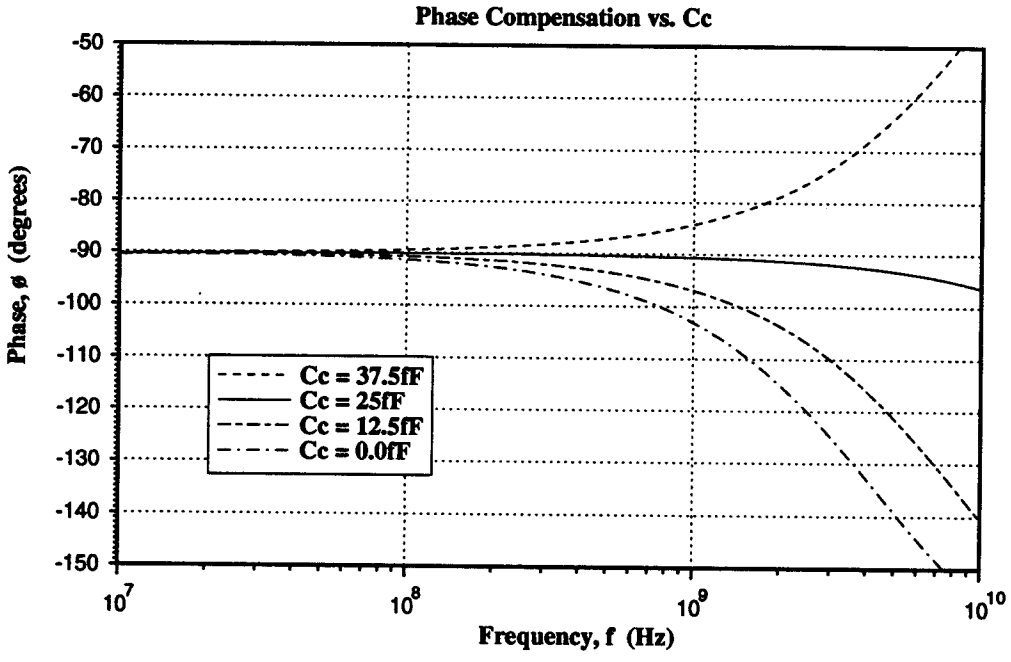

Figure 3.17: Simulation of the Phase Compensation.

Figure 3.17 shows how the excess phase has been compensated for without losing a significant amount of bandwidth. With no compensation, the unity-gain frequency is 475MHz while the additional 25fF capacitors only reduce the bandwidth to 425MHz. Notice that the phase at the unity-gain frequency is now very close to -90 degrees with the addition of the 25fF capacitors. A practical means of implementing these capacitors has yet to be developed.

3.2 The Tunable Power Supply

Section 3.1 described a way of making a very wide bandwidth integrator using only inverters. Unfortunately, the simplicity of the design has left little room for another critical parameter, namely, tunability. Eq. (3.17) points out, however, that the value of the integrator's transconductance is directly dependent upon the value of the supply voltage,

V_{dd}, and it is this fact that can be exploited to tune the transconductance. Also in section 3.1, it was shown that the integrator's DC gain could be made very high by loading the output nodes with a negative resistance and that this could be achieved by varying the transconductance of inverters 4 and 5. Here again, the strategy is to modify the value of the supply voltage, and in doing so, provide a variable negative resistance to the integrator's output nodes.

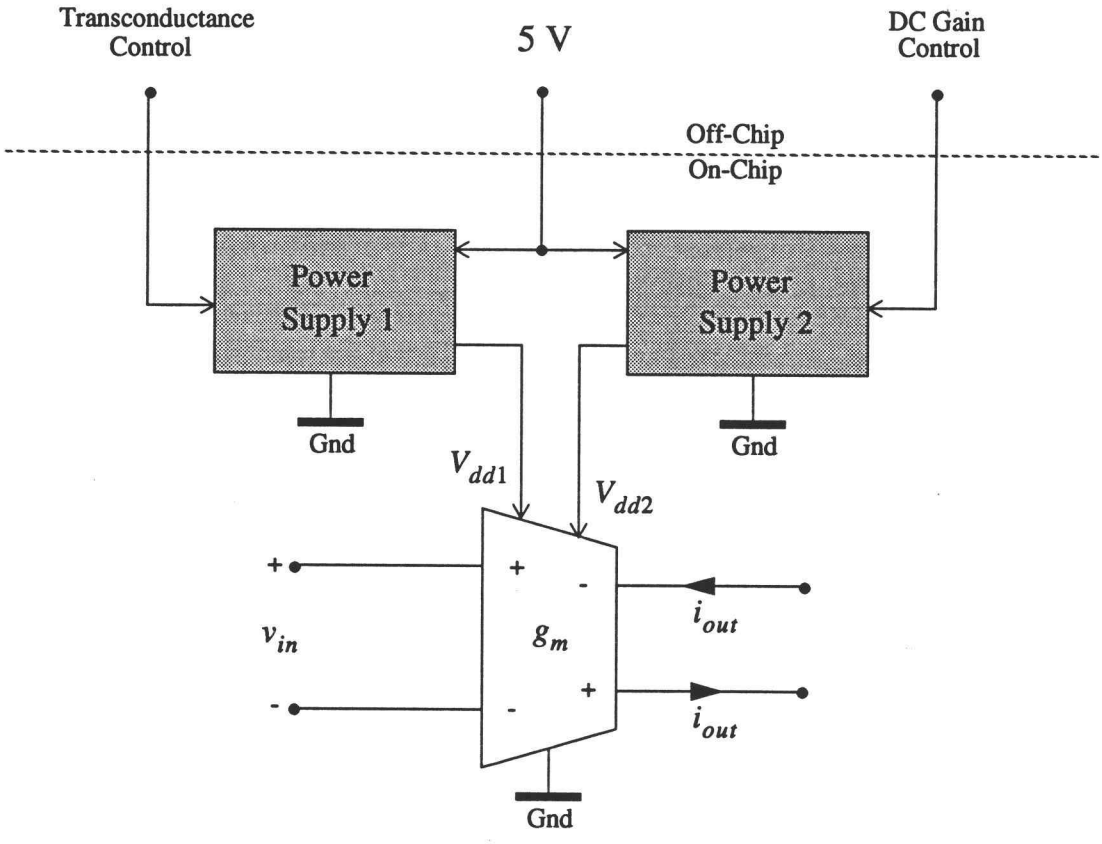

Figure 3.18: Transconductor with Tunable Power Supplies.

Figure 3.18 gives the conceptual idea of creating on chip voltage supplies to control both the transconductance and DC gain. Note that both on-chip power supplies have the same master supply, but each is independent of the other. Although the sizes of inverters 4 and 5 were ratioed slightly smaller than inverters 3 and 6 to enhance the DC gain, the second on-chip power supply is needed to fine tune the value of the negative

output impedance. This will ensure that the DC gain of the transconductance-C integrator is made to be the highest possible value. The construction of the on-chip variable power supply is based upon a well-known feedback technique providing high input impedance and low output impedance. This structure is shown in Figure 3.19.

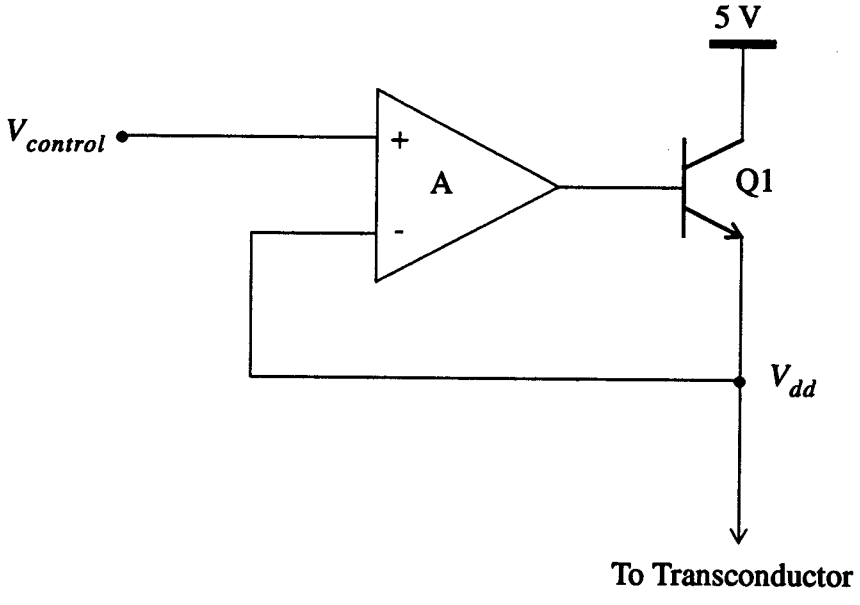

Figure 3.19: Tunable Power Supply with Low Output Impedance.

Clearly, the non-inverting input to the amplifier in Figure 3.19 is a high impedance node that can be used to control the voltage at the output node, V_{dd}. Also, the output impedance of the supply seen by the load at node V_{dd} is that of the emitter of a bipolar transistor which is quite low. Assuming that the forward-biased base-to-emitter junction in the bipolar transistor is nominally 0.7 volts, we can proceed with the DC analysis of this circuit. First, the voltage at the opamp's output is given by $A_o(V_{control} - V_{dd})$. This same voltage can be expressed as $V_{dd} + 0.7\text{V}$. Solving for the output voltage, V_{dd}, in terms of the control voltage, $V_{control}$, we have:

$$V_{dd} = \frac{A_o}{A_o + 1} V_{control} - \frac{0.7\text{V}}{A_o + 1}. \tag{3.28}$$

The point here is that the output voltage can be better matched to the control voltage using an amplifier with high gain. Although there will always be a constant error term between V_{dd} and $V_{control}$, an amplifier gain of 100 or so should be good enough in this application, since the proper operation of the transconductor does not rely on the value of V_{dd} matching that of $V_{control}$. More crucial is the fact that this circuit maintain a low output impedance over a wide bandwidth.

3.2.1 Amplifier Design.

It is apparent in Figure 3.18 that the tunable power supply should be able to provide a sufficient output level to ensure proper operation of each inverter in the transconductor. In fact, it is desirable for the power supply to produce output levels all the way up to the master supply voltage of 5 volts. This is not possible, however, due to the forward-biased junction potential between the base and emitter that must be overcome in the bipolar transistor. In addition, for this application, the common-mode input levels on the amplifier must rest between 3 and 5 volts. Standard amplifier gain stages with n-channel input devices would not work here simply because the common-mode input levels are too high. On the other hand, p-channel input devices would run the risk of cutoff at high common-mode input levels above 3.5 volts or so. Therefore, either level-shifted common-mode inputs or dynamic common-mode inputs are required. The gain of such an amplifier should be greater than 100 to give reasonable conformity of the output voltage to the control voltage although, as stated previously, this is not imperative. The amplifier of Figure 3.20 provides the solution with dynamic common-mode inputs. This means that the amplifier will work over a wide range of common-mode voltages without adverse bias problems. Transistors M9 and M10 make up the output stage of this amplifier. The output stage is used to provide a wide output swing range and to reduce the amount of output resistance.

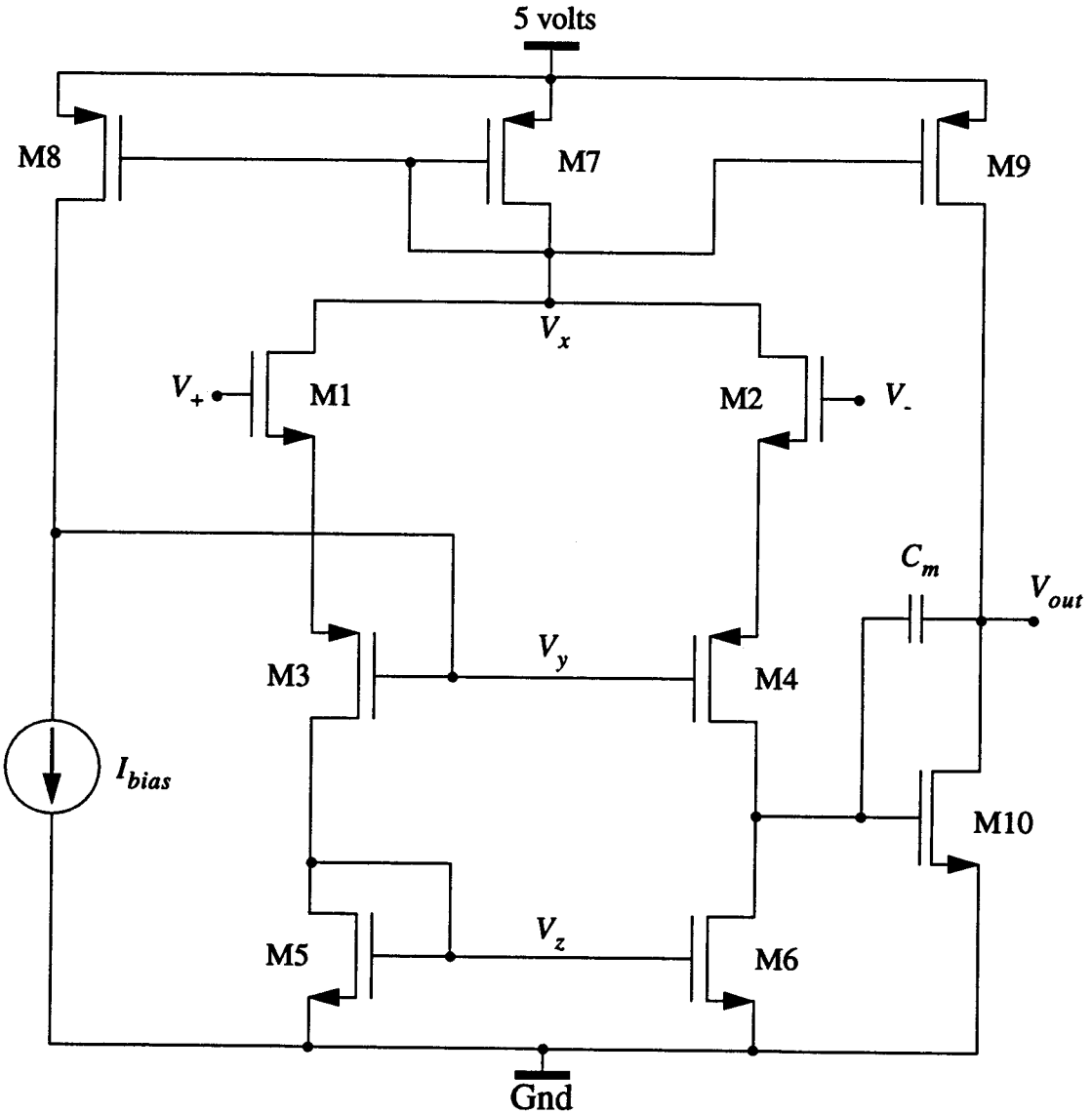

Figure 3.20: Schematic of the Amplifier in Figure 3.19.

The operation of the amplifier presented in Figure 3.20 is as follows. The bias current, I_{bias}, flows through transistor, M8. This current is mirrored to M7 setting the bias current for both legs of the amplifier. As the common-mode voltage on the input nodes is increased, more current begins to flow through M7, causing a tiny drop in the voltage at V_x. Transistor M8 provides inverting gain from V_x to V_y and V_y rises to a new

level, keeping the bias current constant in transistors M1 - M4. When the common-mode level at the input nodes falls, the current in M7 decreases slightly causing V_x to rise. Again, the inverting gain from V_x to V_y causes the high impedance node, V_y, to keep transistors M1 - M4 biased with $I_{bias}/2$. This is the reason for the term dynamic common-mode inputs. The common-mode inputs can vary over a wide range, however, the bias voltages and currents remain unchanged for the input devices.

It can be shown that the gain of the amplifier shown in Figure 3.20 is approximately:

$$A_v \cong \frac{g_{m2}g_{m4}}{g_{m2}(g_{ds4}+g_{ds6})+g_{m4}g_{ds6}} \times \frac{g_{m10}}{g_{m9}+g_{m10}}, \qquad (3.29)$$

where the first term is the gain of the first stage and the second term is the gain of the second stage.

The output stage is just a simple single-ended common-source nmos amplifier that provides some gain, a low output impedance, and is miller compensated for closed-loop stability. Starting with the output stage, the W/L ratios of these transistors should be large to yield a low output impedance. M9, which acts as a current source to bias M10, is ratioed 10 times as large as M7. The drain of M9 was not shielded because of the need for the output to swing as close to the positive rail as possible. The W/L ratio of M10 was made large to give a high transconductance and a low output impedance.

The sizing of the first stage begins with the selection of V_{dsat} for transistors M5 and M6. This voltage specifies how low the output can swing without shifting M5 or M6 into the linear region of operation. Taking the saturation voltage of transistors M5 and M6 in the first stage to be 0.45 volts, the size of these transistors can be calculated:

$$\frac{W}{L}(\text{M5,'M6}) = \frac{I_{bias}}{K_{p_n}(V_{dsat(5,6)})^2} \cong \frac{50\mu\text{A}}{49.8\frac{\mu\text{A}}{\text{V}^2}(0.45\text{V})^2} \cong 5. \qquad (3.30)$$

Transistors M3 and M4 must be sized more carefully than M5 or M6. The output of the first stage must be able to swing high enough to bias M10 in its saturation region and provide signals large enough to make the output of the second stage operate at full scale. Another issue to be considered here is the minimum level of the common-mode inputs. The choice of W/L ratios for M3 and M4 will directly influence the minimum allowable common-mode input level that is needed to keep M3 and M4 in saturation when the output of the first stage swings up to its maximum level. For that matter, the aspect ratios for M1 and M2 play an important role as well. In this application, the supply level for the transconductor described in the previous section should be able to go as low as 3.4 volts. At the same time, the output of the first amplifier stage should be able to rise to a maximum of 1.6 volts to drive the second stage. This gives a difference between the common-mode input level and the maximum first stage output level of 1.8 volts. This voltage drop must account for the gate-to-source voltage of the input devices M1 and M2 and the drain to source saturation voltage, $V_{dsat}$of the p-channel devices, M3 and M4. If we choose $V_{dsat\,(3,\,4)}$ equal to .75 volts, we can calculate the device ratios for transistors M3 and M4:

$$\frac{W}{L}(\mathrm{M3,'M4}) \cong \frac{50\mu\mathrm{A}}{17.6\frac{\mu\mathrm{A}}{\mathrm{V}^2}(0.75\mathrm{V})^2} \cong 5, \tag{3.31}$$

and this leaves about 1.05 volts for the for the gate-to-source voltage of the input device whose ratio is then calculated as:

$$\frac{W}{L}(\mathrm{M1,'M2}) \cong \frac{50\mu\mathrm{A}}{49.8\frac{\mu\mathrm{A}}{\mathrm{V}^2}(1.05\mathrm{V}-0.85\mathrm{V})^2} \cong 25. \tag{3.32}$$

To keep the input devices in saturation, the voltage at V_x cannot drop below the highest possible common-mode voltage minus a threshold of the input devices. Given that the highest common-mode voltage that will be applied is about 4.25 volts, and the

value of V_{T_n} is about .85 volts, V_x must stay above 4.25V - .85V = 3.40V. This means the maximum gate potential on M7 is 1.60V. Using this to calculate the transistor's size for the 50μA bias current, we have:

$$\frac{W}{L}(\text{M7,'M8}) \cong \frac{50\mu\text{A}}{8.8\frac{\mu\text{A}}{\text{V}^2}(1.60\text{V} - 0.95\text{V})^2} \cong 14. \qquad (3.33)$$

The size of M7 was copied to M8 because this drain current is supposed to be mirrored from one transistor to the other. A summary of device ratios can be found in Table 2. A layout of the amplifier cell can be found in Appendix A as part of the power supply layout, Fig. (A.1).

Table 2: Transistor Dimensions (W/L) for the Amplifier of Figure 3.20.

Transistor size (μm)	M1, M2	M3, M4	M5, M6	M7, M8	M9	M10
$\frac{W}{L}$	$\frac{60}{2}$	$\frac{30}{6}$	$\frac{30}{6}$	$\frac{20}{2}$	$\frac{200}{2}$	$\frac{100}{2}$

Miller compensation was necessary to make the amplifier stable in the unity-gain feedback configuration. As shown in Figure 3.20, a compensation capacitor, C_m, was connected between the gate and drain of M10.

Initial simulation of the amplifier's open-loop gain without the compensation, as shown in figure Figure 3.21, reveals that the low frequency gain is good enough, but the phase margin of the amplifier is less than 45 degrees. The dominant pole in this figure is at 200kHz and is approximated by the time constant at the output of the gain stage:

$$f_{p1} \cong \frac{(\frac{g_{ds4}}{2}) + g_{ds6}}{2\pi C_{gs10}} \cong \frac{(2.34\times10^{-7} + 6.35\times10^{-7})\,\text{A/V}}{2\pi \times (3.75)\times10^{-13}\text{F}} \cong 366\text{kHz}, \qquad (3.34)$$

which corresponds to the 3dB frequency as shown in the simulation.

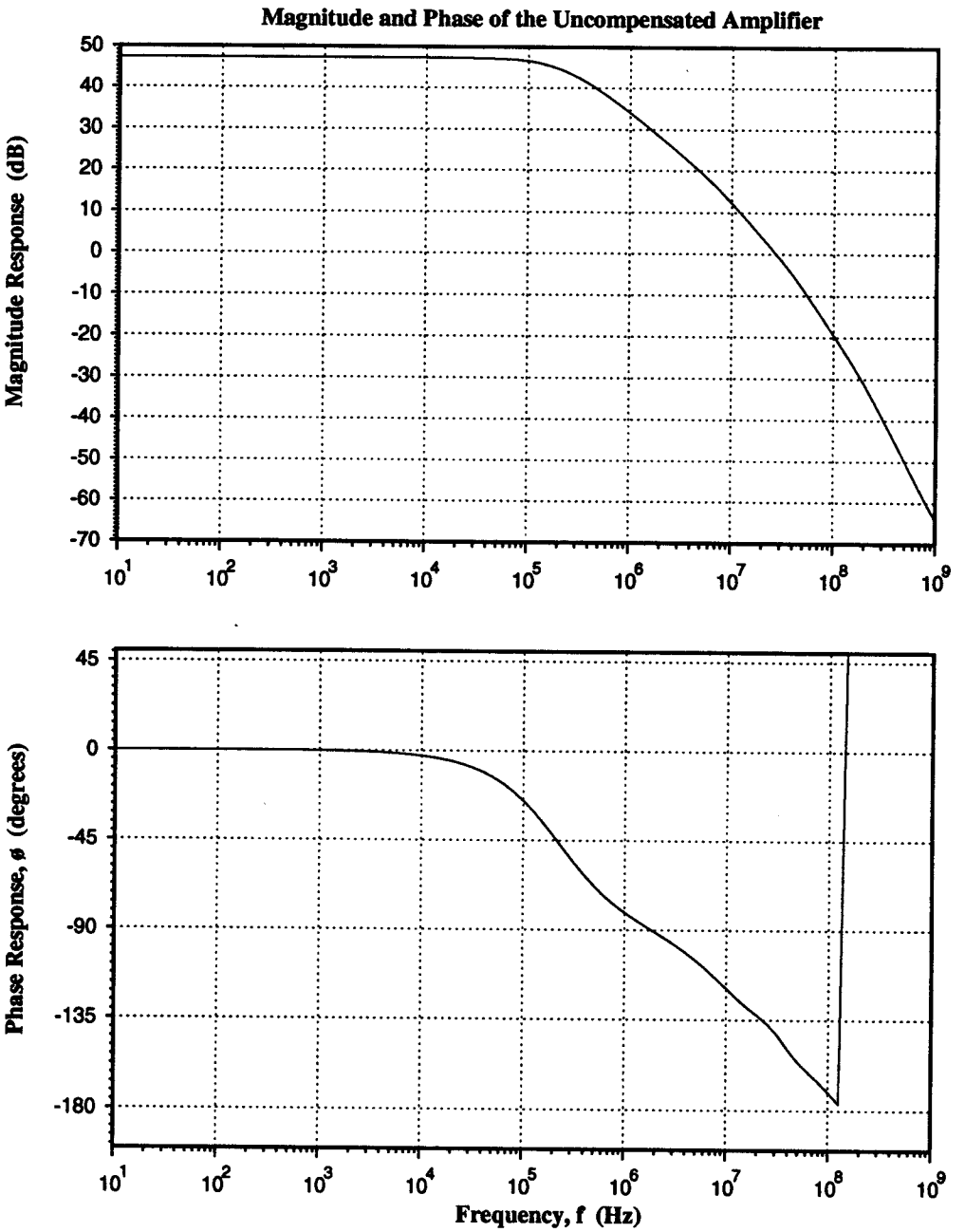

Figure 3.21: Simulated Response of the Uncompensated Amplifier.

The second pole is approximated by the time constant at the output of the second stage as:

$$f_{p2} \cong \frac{g_{ds9} + g_{ds10}}{2\pi C_{\text{load}}} \cong \frac{(8.50\times10^{-5} + 6.18\times10^{-5})\ \text{A/V}}{2\pi \times (3.85)\times10^{-13}\text{F}} \cong 61\text{MHz} \qquad (3.35)$$

which, again, corresponds reasonably well with the simulated value. When the Miller compensation capacitor is added to the circuit, these two poles split apart as described in [4] and the new pole locations become:

$$f_{p1} = \frac{(g_{ds4} + g_{ds6})\ (g_{ds9} + g_{ds10})}{2\pi g_{m10} C_m} \cong 7\text{kHz} \qquad (3.36)$$

and

$$f_{p2} = \frac{(g_{m10} C_m) / (2\pi)}{C_m (C_{gs10} + C_{\text{load}}) + C_{gs10} C_{\text{load}}} = 272\text{MHz} \qquad (3.37)$$

This pole splitting can be seen in the simulation of Figure 3.22. A zero is also created by the compensation capacitor. This a very similar effect to the one described in the feedthrough analysis of section 3.1.2. The location of this zero is:

$$f_z = \frac{g_{m10}}{2\pi C_m} \cong 80\text{MHz}. \qquad (3.38)$$

This is also quite clear from Figure 3.22. Note that the phase margin has improved to almost 90 degrees and, using Eq. (3.37), that a load capacitance of over 80pF is needed to bring the output pole from 272MHz down to the unity gain frequency of 2Mhz. Keep in mind that moving the output pole to the unity-gain frequency will cause a phase shift of approximatey -135 degrees at this frequency and may cause stability problems. As a conclusion, load capacitances of less than 50pF or so will surely guarantee the stability of the amplifier in the unity gain configuration. It can also be said that this amplifier has two poles and one zero below 100MHz.

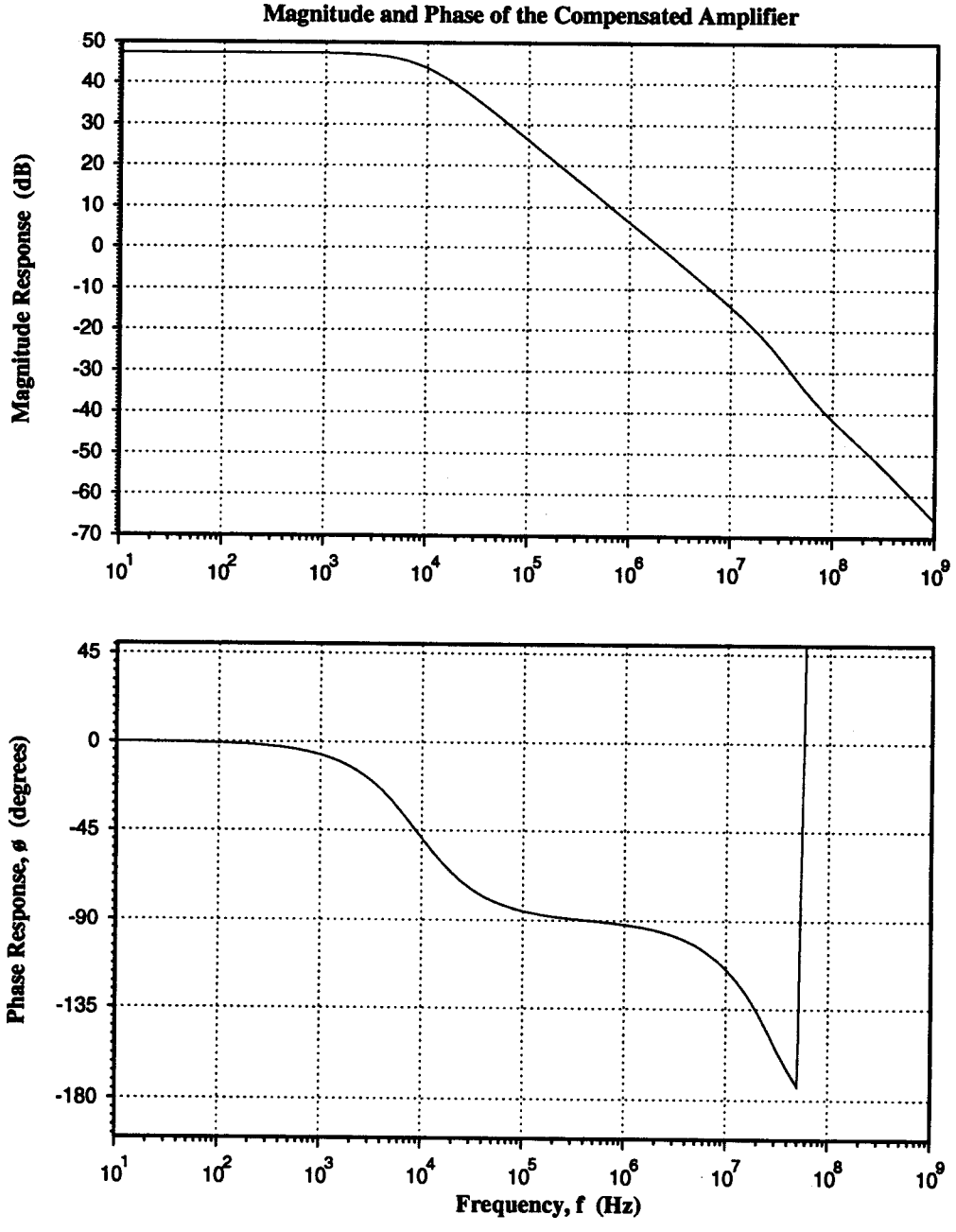

Figure 3.22: Simulated Response of the Miller-compensated Amp.

3.2.2 High Frequency Analysis

Since the transconductors have input signals in the megahertz range, the power

supply must react quickly to the dynamic load. This will ensure that the output voltage of the supply as well as the transconductance of the transconductor is held nearly constant. This can be achieved by making the output impedance of the power supply very low over the frequency range of interest. Although the amplifier has a rather poor frequency response, it will be shown that other factors in the power supply circuit make up for the amplifier's lack of speed resulting in a power supply that has low output impedance up to 100MHz. The following is a frequency analysis carried out in HSPICE of the proposed power supply topology. This analysis includes non-idealities in both the amplifier and the bipolar transistor. Figure 3.23 shows a small-signal model of the power supply for finding the output impedance as a function of frequency. The most dominant components of the BJT model are included here.

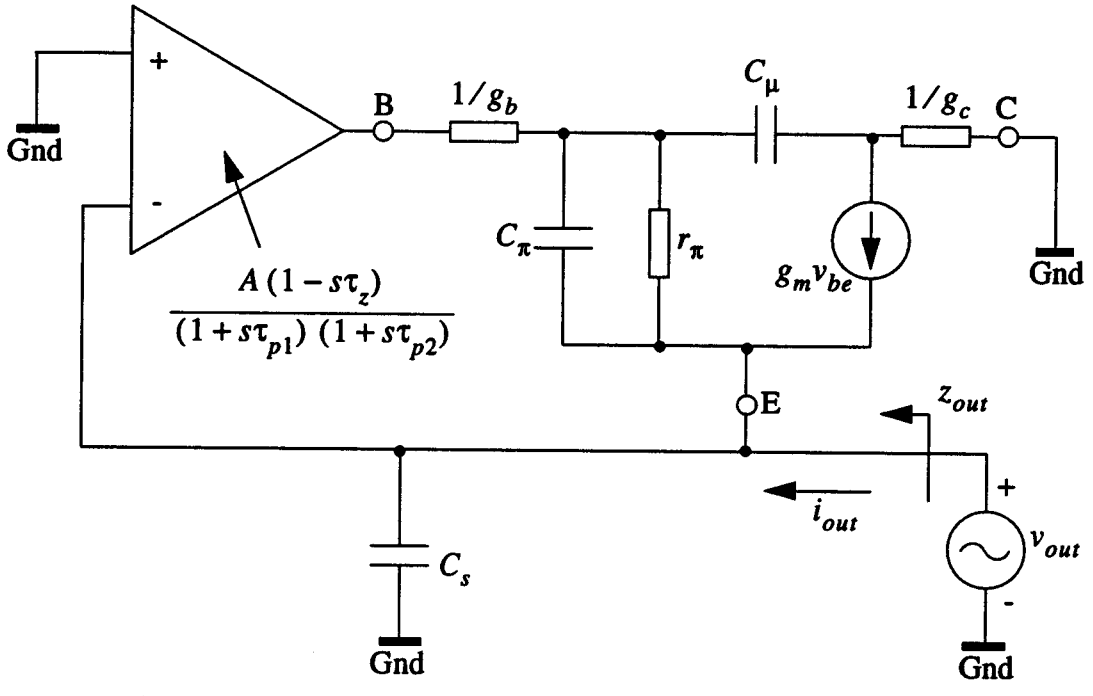

Figure 3.23: Small-Signal Representation of the Power Supply.

The HSPICE model for the bipolar transistor used in this process is not a proven model, yet, it was the only source of information available. Simulations of the power

supply with the given bipolar transistor model have, however, shown that this transistor is well suited to making a wide-band on-chip supply for the transconductors. Figure 3.24 clearly shows that the power supply output impedance is very low up to 100MHz for the entire range of possible control voltages. Other simulations will show that these impedance levels are quite acceptable and provide good regulation at the V_{dd} node.

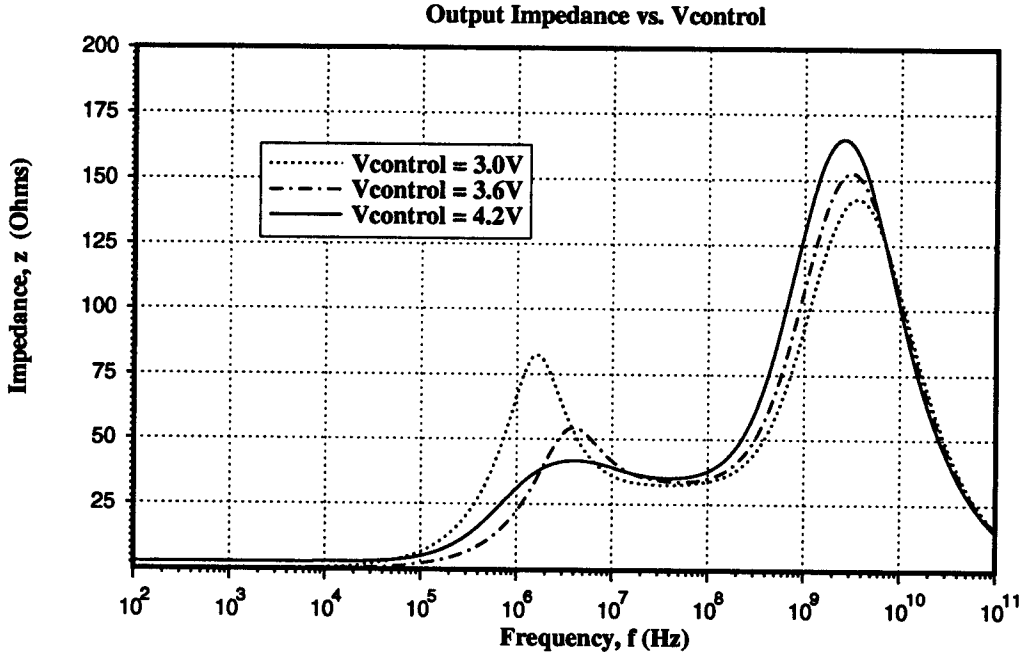

Figure 3.24: Power Supply Output Impedance for Values of Vcontrol.

The peaking in the output impedance between 1MHz and 4MHz results from resonance that occurs at the output node. Different common-mode levels on the amplifier change the effective inductive and capacitive impedances at the output node causing variations in the level of the peaking.

The reason for using a bipolar transistor instead of a MOS device in this application becomes very clear when the performance-per-area is analyzed. For a typical control voltage of 3.9V, a comparison was made between a bipolar transistor and an NMOS transistor. The bipolar transistor was assumed to have an area of 2,530 square microns with a

base resistance of 500 ohms and a collector resistance of 500 ohms. These are, of course, approximations as hard process data was not available. The NMOS device was simply a minimum length transistor with a width of 500μm. The area of the NMOS device was nearly twice that of the bipolar at 4,620 square microns. Figure 3.25 illustrates the dramatic difference in the performance of the two devices. The enhanced performance of the bipolar device with respect to the NMOS device is partly due to the greater transconductance in the bipolar. For a given current, g_m is about six times larger for the bipolar transistor than for the NMOS transistor.

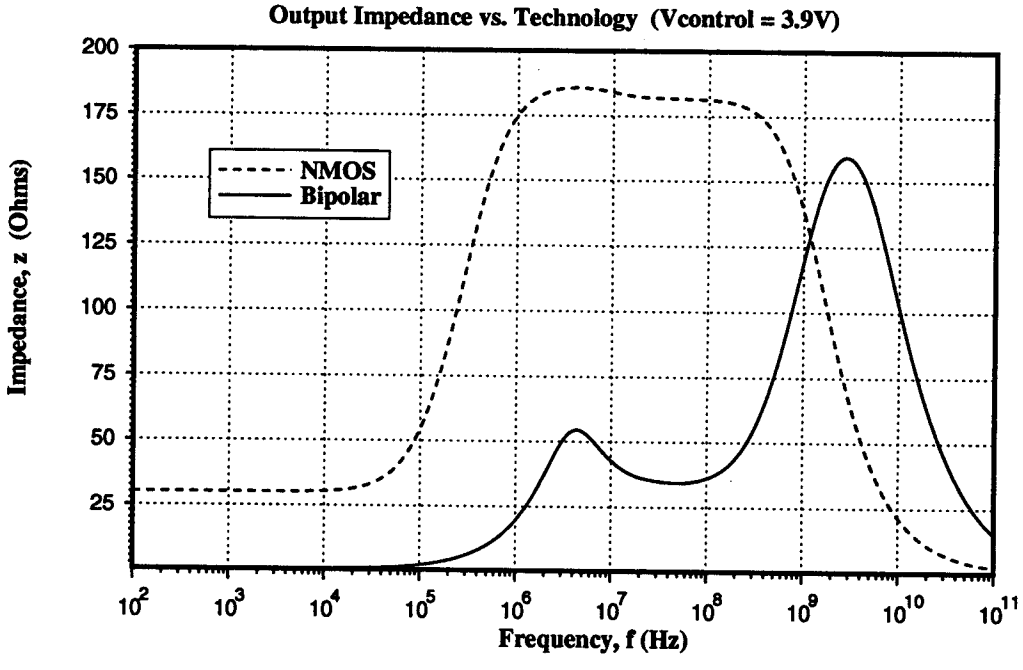

Figure 3.25: Power Supply Output Impedance for NMOS and Bipolar.

The maximum output level of a supply built with an NMOS transistor can not match that of one built with the bipolar transistor either. The maximum output level of the supply is given by the maximum output level of the amplifier minus the threshold that must be overcome in the device to provide a particular supply current. In the bipolar transistor, this threshold is typically between 0.65V and 0.75V for a wide range of sup-

ply currents while the NMOS transistor needs at least .85V to even turn on, plus some ΔV_{gs} which is a function of the supply current to be sourced. Lower output impedance and greater headroom makes the bipolar transistor a much more attractive choice for the power supply than does the NMOS transistor.

Although the value of the base resistance in the bipolar transistor should be as small as possible to get the lowest output impedance possible, a far more limiting factor lies in the value of the collector resistance. If the value of the collector resistance is too high, the base-collector pn junction in the bipolar transistor can become forward biased, moving its region of operation from forward active to heavy saturation, [13]. When this happens, the emitter of the bipolar transistor faithfully remains at one saturation voltage below the voltage at the collector, even when the collector current varies substantially.

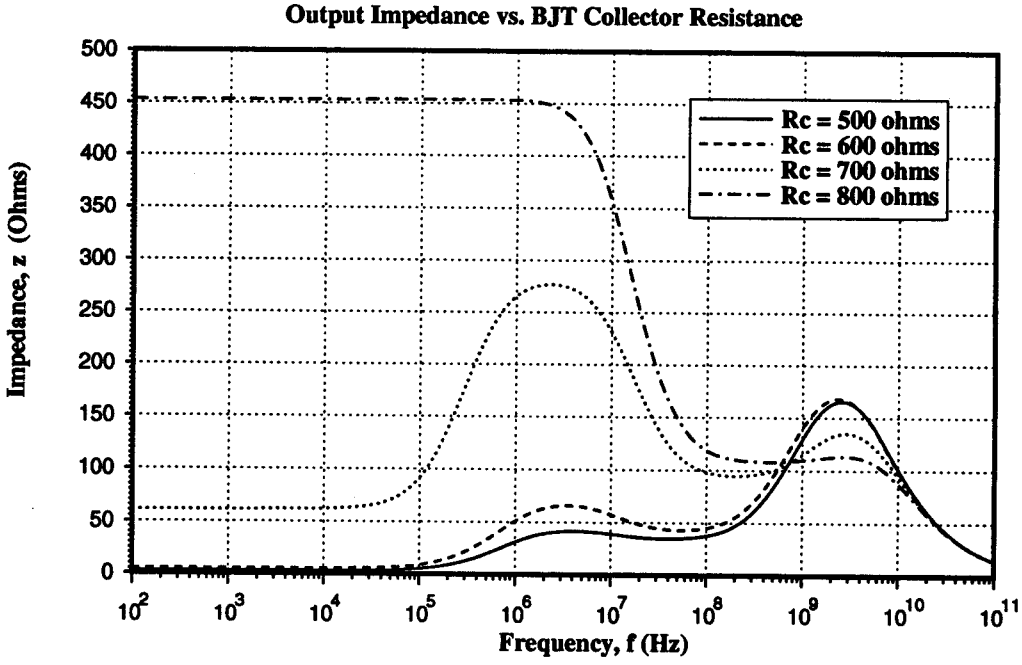

Figure 3.26: Power Supply Output Impedance for values of Collector Resistance.

The result is a high impedance at the output of the power supply which is undesirable. This phenomenon is illustrated in Figure 3.26 where the output impedance becomes

quite high for a collector resistance of 800 ohms. This hazard concerning the collector resistance provides ample motivation to use a bipolar transistor with low collector resistance.

3.2.3 Practical Considerations

Since the output impedance of the power supply for the transconductors is not ideal for frequencies up to 100MHz, it is instructive to examine the effects produced on the operation of the transconductors themselves due to this non-ideality. As shown in Figure 3.24, a large peak in the power supply output impedance exists at a frequency of

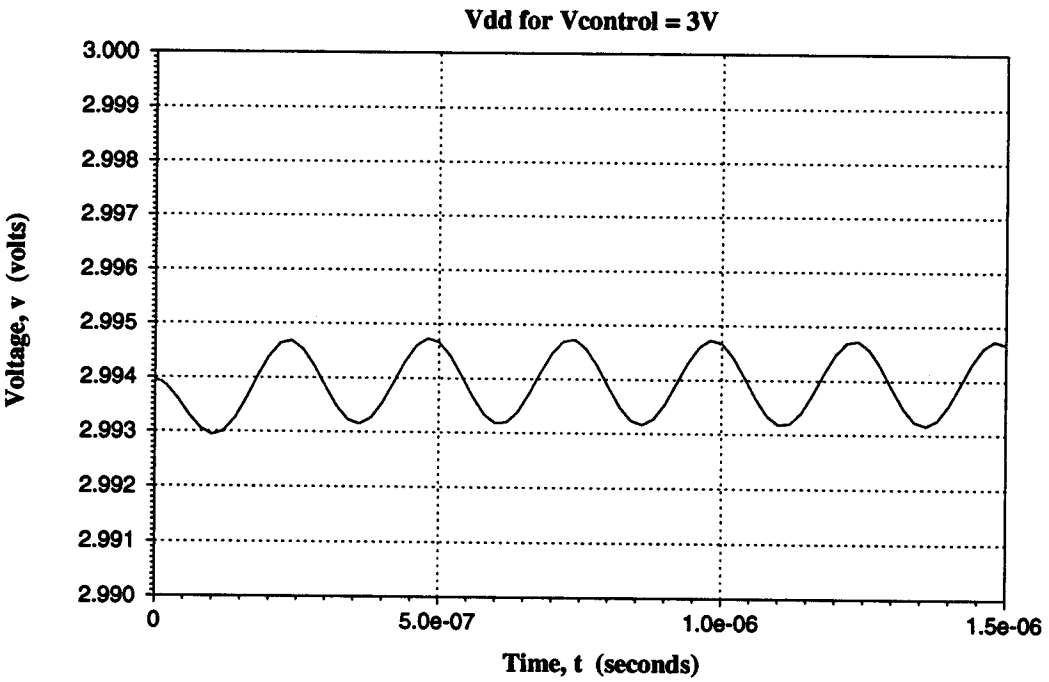

Figure 3.27: Power Supply Ripple due to Non-Ideal Source Impedance.

2MHz for the lowest control voltage of 3V. Figure 3.27 shows that some ripple is generated at the V_{dd1} node when a 2MHz signal is applied to the input of the transconductor with an amplitude of 1Vpp. This ripple in V_{dd1} will have a direct impact on the transconductance of this circuit causing some distortion, however, Nauta mentions that

the distortion caused by even several millivolts of fluctuation in either V_{dd1} or V_{dd2} is small. During this simulation, the outputs of the transconductor were tied to V_{cm} as would be done for the measurement of the transconductance. Note that with the outputs of the transconductor tied to V_{cm}, no perturbation of V_{dd2} will occur. Also note that the frequency of the ripple in Figure 3.27 is 4MHz, twice that of the input signal. This is due to the fact that the signal dependant portion of the the supply current is a function of the square of the input signal. Further analysis can be found in [11].

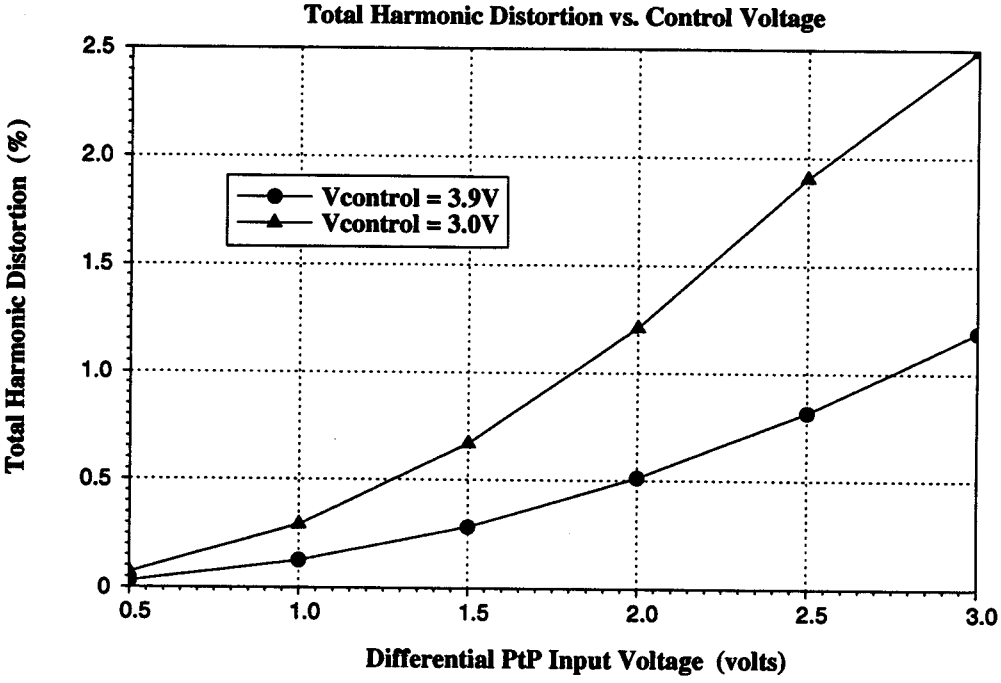

Figure 3.28: Total Harmonic Distortion in the V/I Conversion.

Figure 3.28 shows the total harmonic distortion in the output current as a function of the input voltage. The total harmonic distortion for this voltage-to-current converter is good (less than 1%) at 1.8 volts peak-to-peak, even for the lowest possible control voltage, $V_{control}$ = 3V.

Chapter 4. The Fourth-Order Programmable Filter

This Chapter is concerned with the design of the programmable filter. The filter was synthesized to verify that a high frequency tunable filter could be realized using the elements presented in Chapter 3. A fourth-order lowpass Chebychev filter with a .1dB ripple was chosen as the prototype and a biquad topology was used for easy programmability.

4.1 Filter Topology and Component Selection

In Chapter 2, the biquad topology shown in Figure 2.6 (biquad #1) was found to have less passband gain error for a given transconductor DC gain. Thus, it was chosen over biquad #2 as the building block for the programmable filter. To reduce common-mode noise and increase the power supply rejection of the filter, differential circuitry was also employed. A differential version of biquad #1 is shown in Figure 4.1. Differential circuitry also allows higher input signal levels to the circuit, thereby increasing the overall dynamic range of the filter.

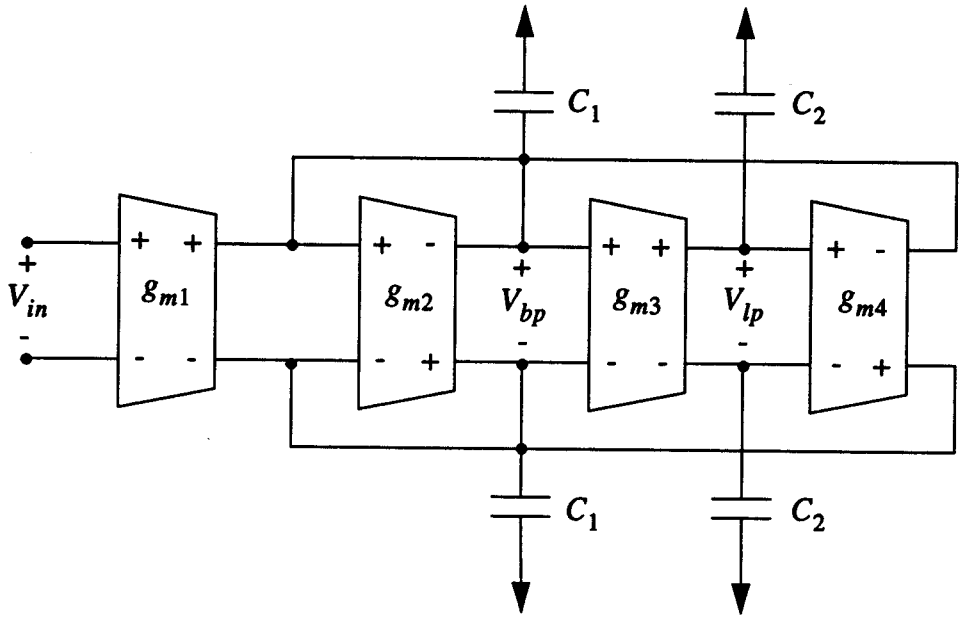

Figure 4.1: Differential Biquad Section (biquad #1).

To construct a fourth-order filter, two biquad sections are required. These sections are cascaded to yield the fourth-order Chebychev function. From a table of normalized Chebychev transfer function coefficients found in [2], the following fourth-order normalized Chebychev transfer fuction was synthesized:

$$H(s) = \frac{1.33 \times 0.6229}{(s^2 + 0.5283s + 1.33)\,(s^2 + 1.2755s + 0.6229)}. \qquad (4.1)$$

This normalized filter transfer function has a passband frequency of 1 rad/sec and a DC gain of 1 (0dB). Since the filter we want to design needs a passband of 50MHz, it is necessary to first, 'denormalize' the transfer function, $H(s)$, to 50MHz. This is accomplished in [6] by making the substitution, $s = s/\omega_o$, where $\omega_o = 2\pi(50\times10^6)$. This substitution yields two biquadratic functions that can each be implemented with the circuit of Figure 4.1:

$$H_1(s) = \frac{1.313\times10^{17}}{s^2 + 1.660\times10^8 s + 1.313\times10^{17}} \qquad (4.2)$$

and

$$H_2(s) = \frac{6.148\times10^{16}}{s^2 + 4.007\times10^8 s + 6.148\times10^{16}}. \qquad (4.3)$$

In Chapter 3, a simulation of the transconductance element was performed over its tunable range. At 3.9 volts, the transconductance of this element was found to be 687μA/V. By choosing the same value of transconductance for all the transconductors in the filter, one transconductor design can be used and all of the transconductors can use the same control voltages. Thus, a common value of 687μA/V was used for all of the transconductors. Recalling the transfer function for the lowpass output of biquad #1 in Chapter 2:

$$H(s) = \frac{\frac{g_{m1}g_{m3}}{C_1C_2}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}}, \tag{4.4}$$

it is easy to equate terms between $H_1(s)$ and $H(s)$ to find values for g_m and C in the first biquad section. The easiest term to start with is the linear term in the denominator,

$$\frac{g_{m2}}{C_1} = 1.660\times10^8\text{rad}. \tag{4.5}$$

Given that all g_m values are 687μA/V, the capacitance values for the first biquad section are simply:

$$C_1 = \frac{687\mu\text{A/V}}{1.660\times10^8\text{rad}} = 4.139\text{pF} \tag{4.6}$$

and

$$C_2 = \frac{(687\mu\text{A/V})^2}{(1.313\times10^{17}\text{rad}^2)\ (4.139\text{pF})} = 0.869\text{pF}. \tag{4.7}$$

Likewise, for the second biquad section:

$$C_1 = \frac{687\mu\text{A/V}}{4.007\times10^8\text{rad}} = 1.714\text{pF} \tag{4.8}$$

and

$$C_2 = \frac{(687\mu\text{A/V})^2}{(6.148\times10^{16}\text{rad}^2)\ (1.714\text{pF})} = 4.478\text{pF}. \tag{4.9}$$

A summary of the component values for the fourth-order Chebychev filter can be found in Table 3. The 4th-order filter is shown in Fig. (4.2).

Table 3: Biquad Component Values for the Fourth-Order Chebychev Filter.

	Section 1	Section 2
g_{m1}	687μA/V	687μA/V
g_{m2}	687μA/V	687μA/V
g_{m3}	687μA/V	687μA/V
g_{m4}	687μA/V	687μA/V
C_1	4.139pF	1.714pF
C_2	0.869pF	4.478pF

Since the capacitances in the filter are relatively small, some portion of each capacitance value will consist of a parasitic capacitance, however, each parasitic is made up mostly of gate-oxide capacitance and is consequently quite linear. Although gate-oxide capacitance also has a tendency to vary with process, g_m in a filter is approximately proportional to C_{ox}. Thus, a given spread in C_{ox} causes only a small spread in g_m/C for filters that operate mainly on parasitics [11]. The added capacitors in the filter are double-poly capacitors, hence, they are expected to be linear and accurate.

Table 4: % of Capacitance made up from Parasitics.

	Section 1	Section 2
C_1	24%	42%
C_2	54%	14%

A method exists for making each parasitic the same fraction of the total capacitance at each node [6]. Using dummy transconductors to equalize the percentage of parasitic capacitance at each node, the relative position of all filter poles and zeros is fixed and can be tuned during operation with g_m. No dummy devices were added to this filter, thus, some error in the passband can be expected due to process variation.

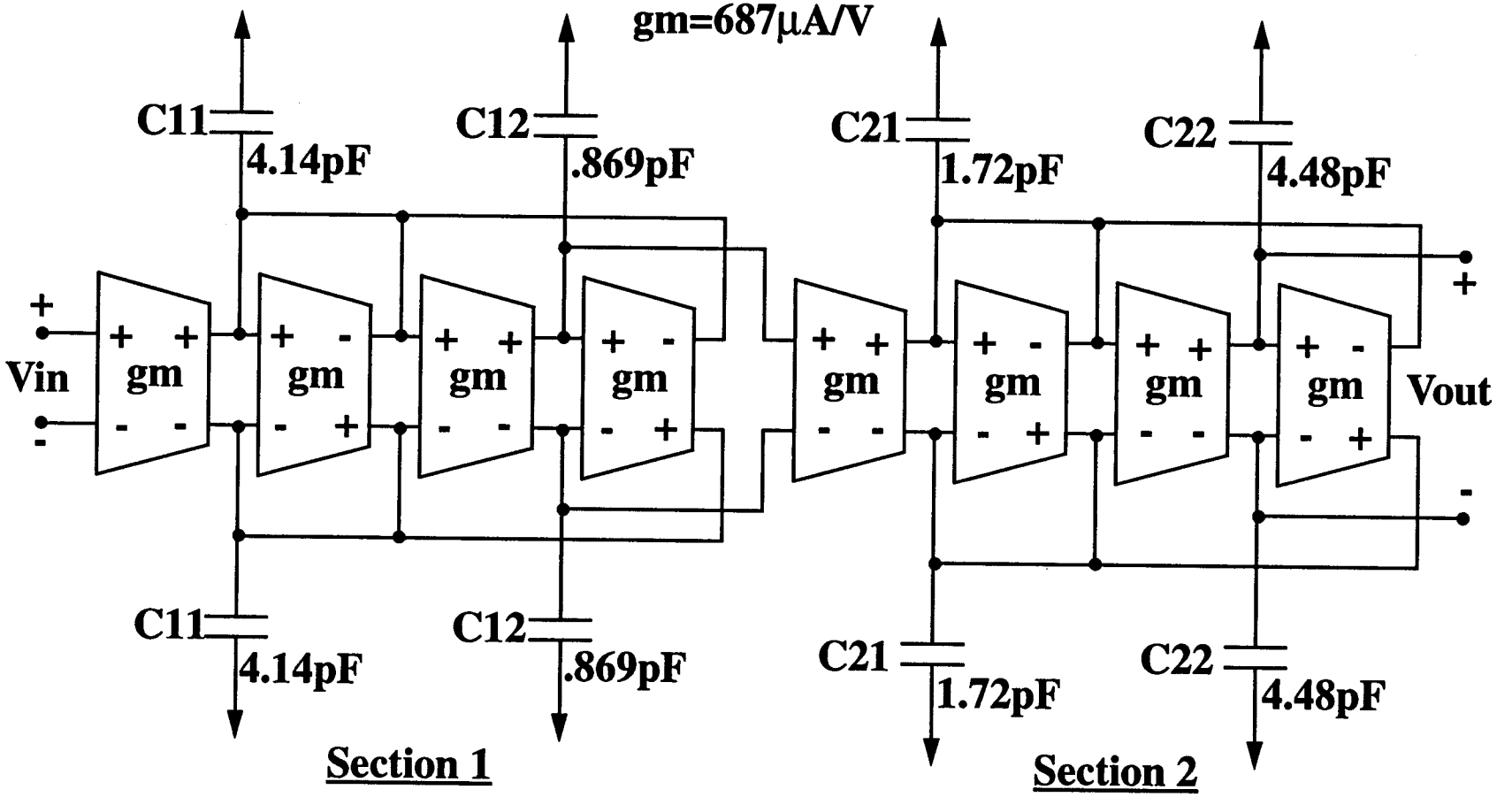

Figure 4.2: 4th-Order Chebychev Filter.

4.2 Simulation Results

The control voltage for V_{dd1} is used to tune the filter parameters. Since a separate V_{dd1} may be used for each transconductor , the filter's cutoff frequency, passband gain, and Q can each be tuned independently. The control voltage for V_{dd2} is assumed to be generated automatically using a method of automatic tuning described in [1], [8], or [10].

Figure 4.3 shows the ideal and simulated responses of the fourth-order Chebychev filter. For the simulation, V_{dd1} = 3.90V and V_{dd2} = 3.675V. It is clear that the simulated filter cuts off at the desired frequency of 50MHz and has a low frequency passband gain very close to 0dB. The passband error in the filter was not expected, however. It is suspected that this error exists because no excess phase compensation or compensation for the non-ideal input impedance in the transconductors was applied.

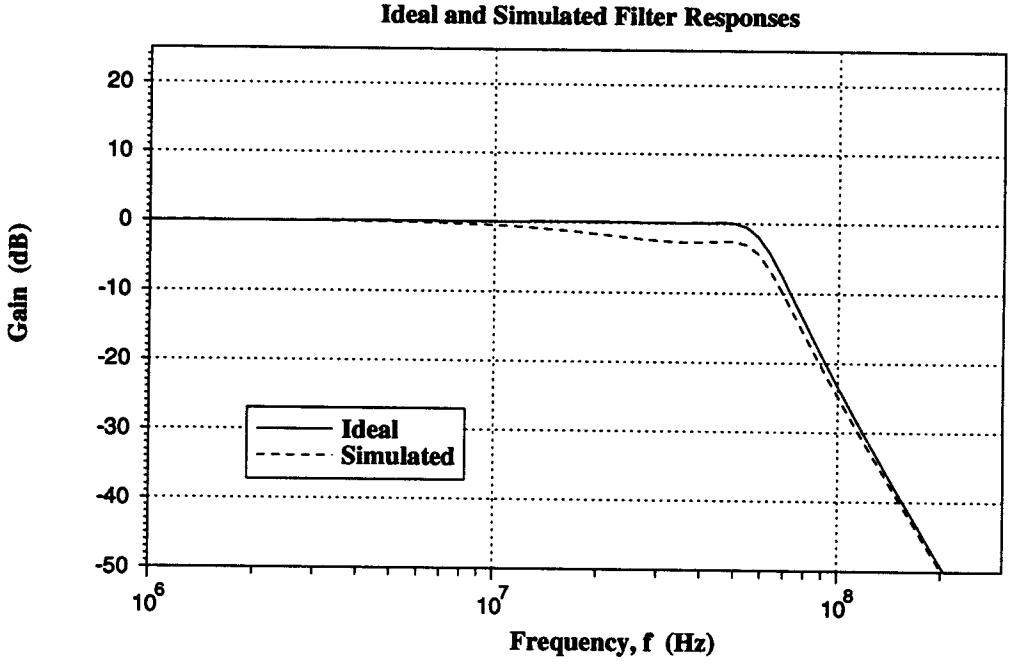

Figure 4.3: Ideal and Simulated Filter Responses for the 50MHz Filter.

These possibilities were explored in Figure 4.4 where resistances were added to the inputs of the ideal transconductors and node capacitances were modified to duplicate the effects produced by the capacitances C_f and C_d in Figure 3.13. Resistances were calculated using Eq. (3.24) and were variable from 60kΩ to 230kΩ. The similarity between the non-ideal and simulated responses indicates that the passband errors encountered in the filter are, in fact, a result of the purely lossy nature of the transconductor's input impedance as well as errors in the capacitance values at the nodes. One may propose to use the tunable output impedance of a driving transconductor to compensate for the loading in the filter, however, this would require individual tuning for each transconductor. In any case,the purely lossy transconductor input impedance is a problem in this filter that has not been handled thus far.

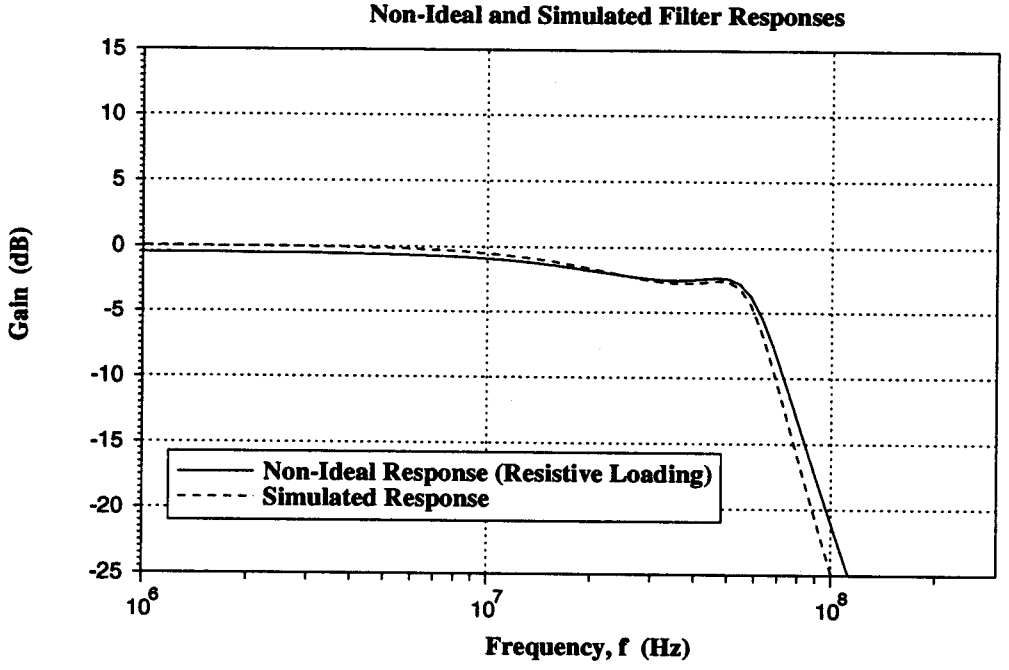

Figure 4.4: Comparison of Simulated and Non-Ideal Filter Responses.

To illustrate the programmability of the filter, further simulations were run to show how the cutoff frequency as well as the passband gain could each be tuned through a control voltage. Figure 4.5 shows how, by varying all the transconductors in unison,

the cutoff frequency can be tuned from 39MHz to 61MHz over the 1.2V range of the transconductance control voltage. This tuning range could actually be guessed beforehand by finding the range of g_m in Figure 3.10. This figure shows that, over the range of control voltage from 3V to 4.2V, the transconductance changes from 475μA/V to 750μA/V indicating that the cutoff frequency of the filter can be tuned a factor of 1.58. In fact,

$$\frac{61\text{MHz}}{39\text{MHz}} \cong \frac{750\mu\text{A/V}}{475\mu\text{A/V}}. \tag{4.10}$$

Thus, for frequency programming, only one control voltage is needed.

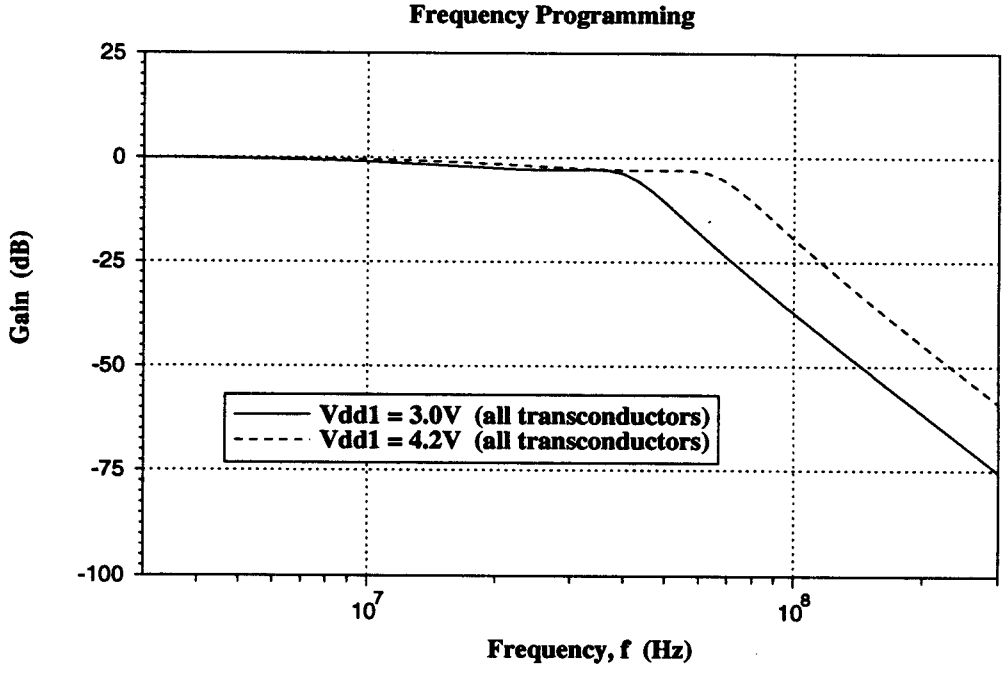

Figure 4.5: Simulation of Voltage-Controlled Frequency Programming.

Examining the biquad transfer function once again, it is clear that gain programming can be easily accomplished by varying the value of g_{m1}.

$$H(s) = \frac{\frac{g_{m1}g_{m3}}{C_1C_2}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}} \tag{4.11}$$

Gain programmability is illustrated in Figure 4.6. In this simulation, the control voltage for transconductors 2-4 in each biquad was held constant at the nominal value of 3.9V while a separate control voltage was applied to transconductor 1 in each biquad. The passband gain is tunable over 10dB simply by varying the value of g_{m1} over its tunable range 475μA/V - 750μA/V. Again, the tuning range of the filter can be related to that of the transconductor. 10dB corresponds to a relative gain of 3.16 indicating that each biquad adds a gain of $\sqrt{3.16}$ or 1.78. This corresponds somewhat to the tuning scale of 1.58.

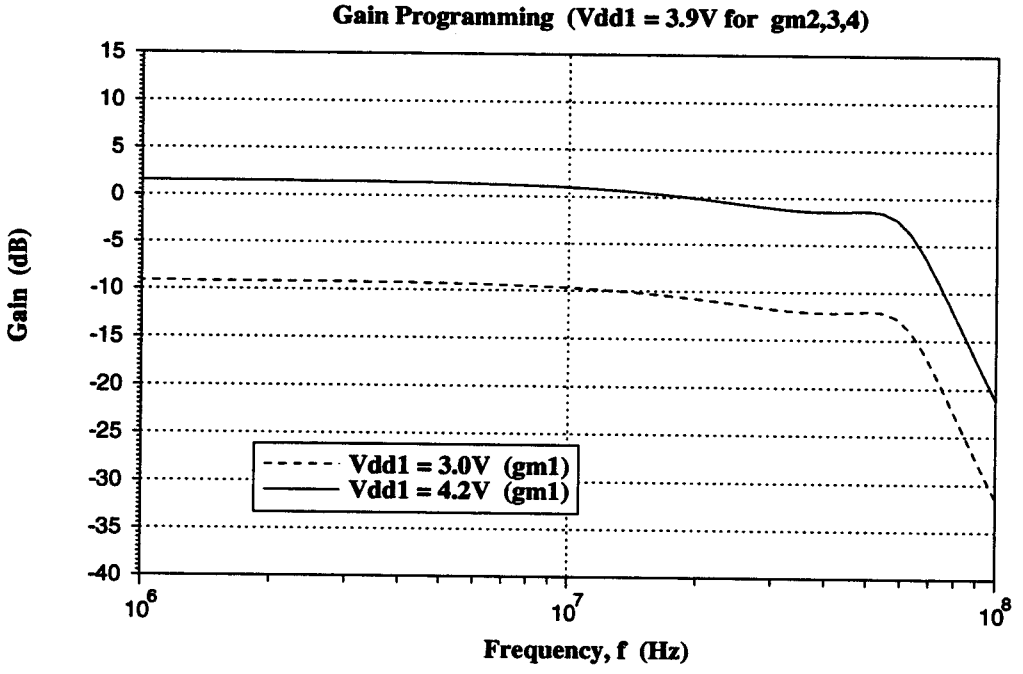

Figure 4.6: Simulation of Votage-Controlled Gain Programming.

Finally, the filter Q can be tuned as well. To tune the filter Q, the value of g_{m2} is

varied. From Eq. (4.11),

$$\frac{g_{m2}}{C_1} = \frac{\omega_o}{Q}, \tag{4.12}$$

so that a change in g_{m2} will cause a reciprocal change in Q.

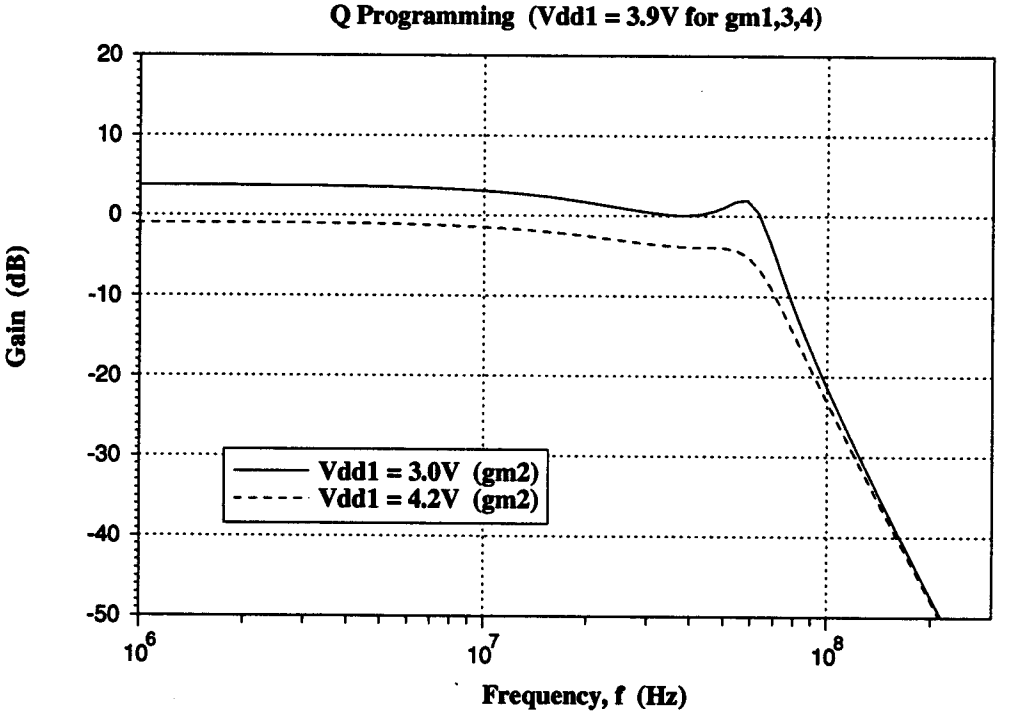

Figure 4.7: Simulation of Voltage-Controlled Q Programming.

4.3 Measurements

An experimental test chip was fabricated through MOSIS using a 2μm, double-metal, double-poly, n-well process. This process also offered bipolar transistors that could be used for making the on-chip wide-bandwidth power supplies. Integrated circuits on the chip included stand-alone versions of the transconductor and amplifier, each designed in Chapter 3, a single bipolar transistor, and the fourth-order programmable filter. Since suitable equipment for high-frequency measurements was not available, no

high frequency measurements for the filter were recorded. Care was taken in the board layout to ensure proper operation of the filter IC at high frequencies, however, noise was prevalent on the board's ground plane and efforts to remove it were not successful. Other problems included converting the single-ended input signal to a differential input signal and converting the differential output signal to a single-ended output signal. Measurements made at low frequency included the transconductance of the transconductor and the amplifier's gain response. The filter was also measured at low frequencies revealing that the filter was operational in the passband, but the frequency of the roll-off characteristic was beyond the capabilities of the test instruments at hand.

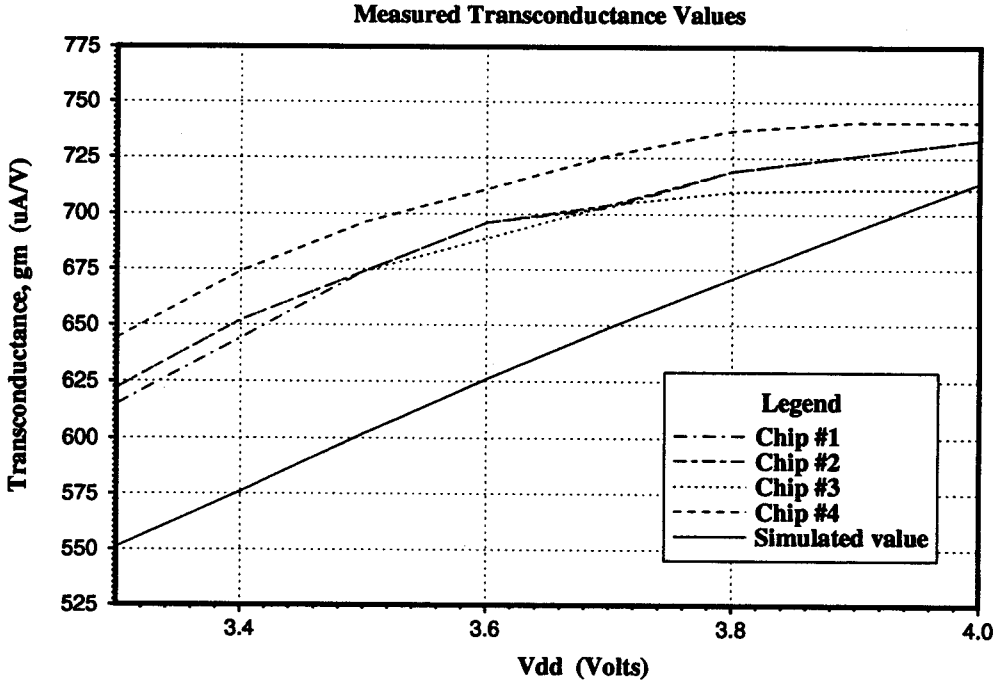

Figure 4.8: Transconductance Measurements from the Experimental Test Chip.

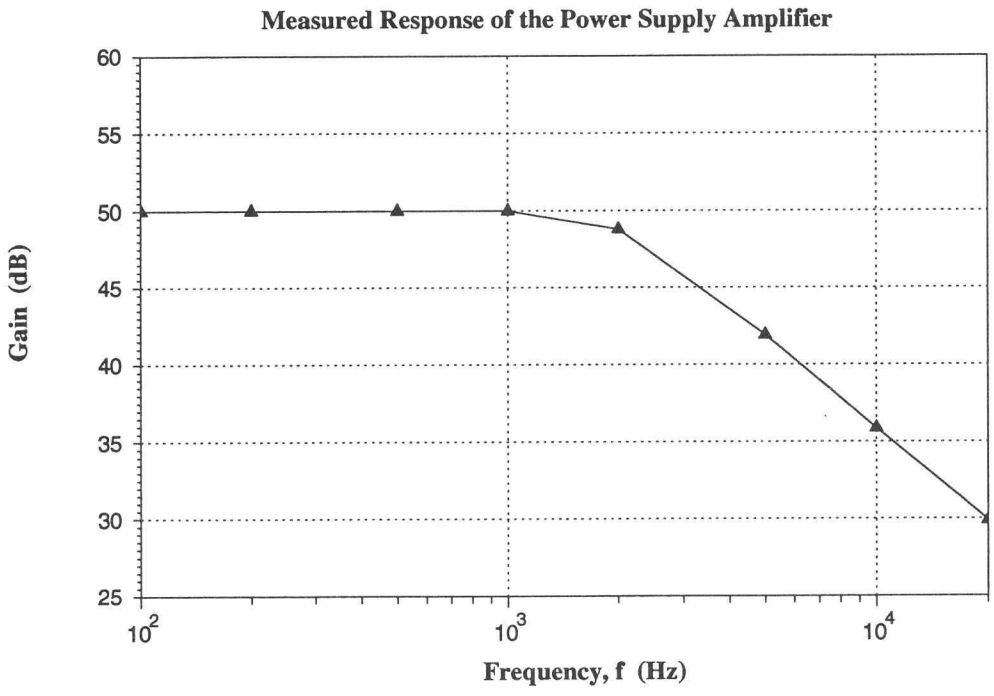

Figure 4.9: Measured Gain Response of the Power Supply Amplifier.

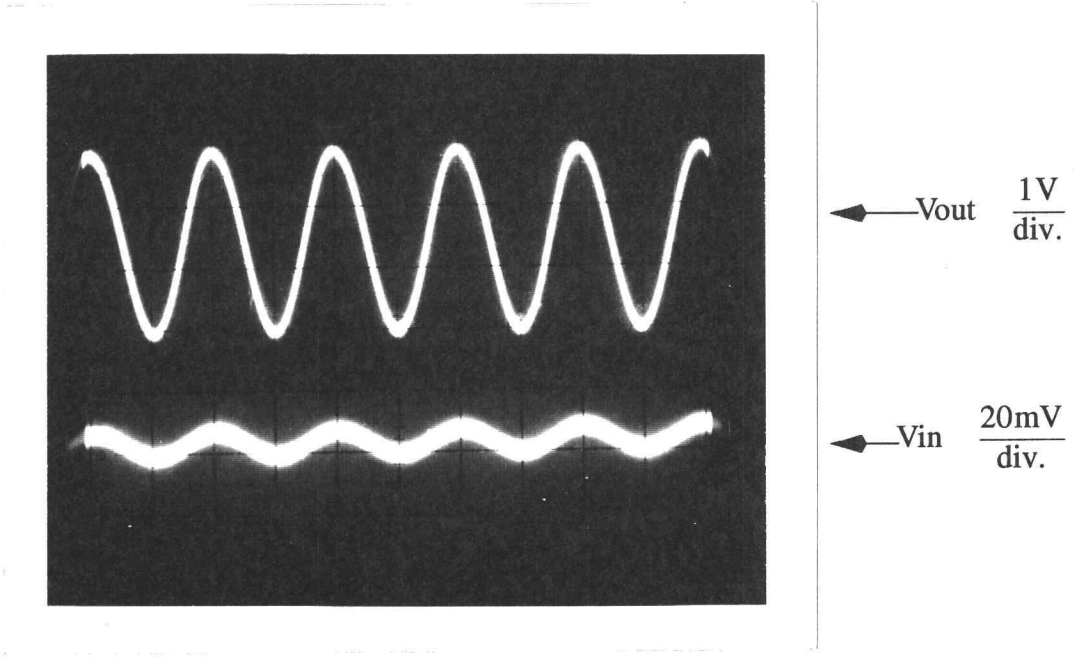

Figure 4.10: Amplifier Gain with 1kHz Signal (Ibias = 130μA, Vcm = 4V).

Chapter 5. Conclusions and Future Work

5.1 Conclusions

A programmable fourth-order continuous-time filter using the transconductance-C method has been simulated. This filter was realized as a cascade of biquadratic sections, and used manual programming. Although the passband gain error proved to be significant, it has been shown, nonetheless, that the filter can be programmed in numerous ways. The cutoff frequency of the filter was tunable from 39MHz to 61MHz. Passband gain was tunable over ten decibels. Pole Q's of the filter were tuned as well with Q values ranging from 2.00 to 3.15 in the first biquad and 0.57 to .90 in the second biquad. It has also been shown in the simulation that the passband error is due, in part, to the purely lossy effects causing loading problems within the biquad structures. Errors in the capacitances at the nodes may also have an effect on the passband error.

A power supply for powering the transconductors has been presented. This power supply has a low output impedance up to 100MHz and can be tuned with a single control voltage. A specialized amplifier has been designed for the power supply as well. Using a 5 volt supply, this amplifier can provide a gain of more than 45dB with common-mode levels between 3 and 5 volts. Since this amplifier is Miller-compensated, it has a low-frequency dominant pole which is around 7kHz.

The transconductors themselves are based on simple inverters and have no internal nodes, thus, they can achieve very high bandwidths. Simulation in this thesis has revealed a unity-gain bandwidth greater than 400MHz for this transconductor topology.

Measurements from the test chips have shown that the transconductance values of the transconductors are close to the ones that were simulated using HSPICE. The nominal value in the simulations is 687μA/V while that in the experimental test chip is around 720μA/V. The error is suspected to be from a simulation error in gate length. The power supply amplifier has also proven functional, although the measured dominant pole

is different from the simulated value. This discrepancy could be from inaccuracy in the Miller capacitor itself, or from a lower-than-expected g_m in the output stage.

5.2 Future Work

There is much future work to be done. First, the experimental filter on the test chip must be tested in full capacity. The high frequency roll-off characteristic of the filter has not been measured accurately. This is because of limitations in the present test setup. Also, a further analysis of the bipolar transistor on the test chip will uncover critical values such as collector resistance and BETA. More iterations on the power supply design should prove fruitful. It is believed that a better amplifier can be designed for this application with a higher bandwidth and a lower output impedance.

A method for compensating the resistive loading effects in biquad filters using this transconductor technique must be found. If the resistive loading effects are not compensated properly, filters using this biquad topology will always have passband gain errors. A practical way to implement the phase compensation in Chapter 3 must also be devised. Although it is easy to run the simulation and show that the effects can be compensated, it is quite another thing to practically implement it.

Automatic tuning circuitry must be added to the filter to automatically tune the value of V_{dd2}. Although the value of V_{dd1} is manually programmable for all the transconductors, the simulations have assumed that V_{dd2} is correct. On-chip automatic tuning circuitry will be able to fine tune the value of V_{dd2} based upon the manual programming voltage of V_{dd1}.

Finally, work toward a fully adaptive analog filter can begin. Using the ideas developed in this paper, it is conceivable that a fully adaptive analog filter can be designed. The biquad structure lends itself very nicely to gain, frequency, and Q tuning, and applications that require adaptive control over these parameters will greatly benefit

from future work in this area. In fact, it has been shown by Johns [9], that some of the non-ideal integrator effects discussed in this thesis can actually be obviated with the use of adaptive tuning.

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APPENDICES

APPENDIX A: Cell Layouts

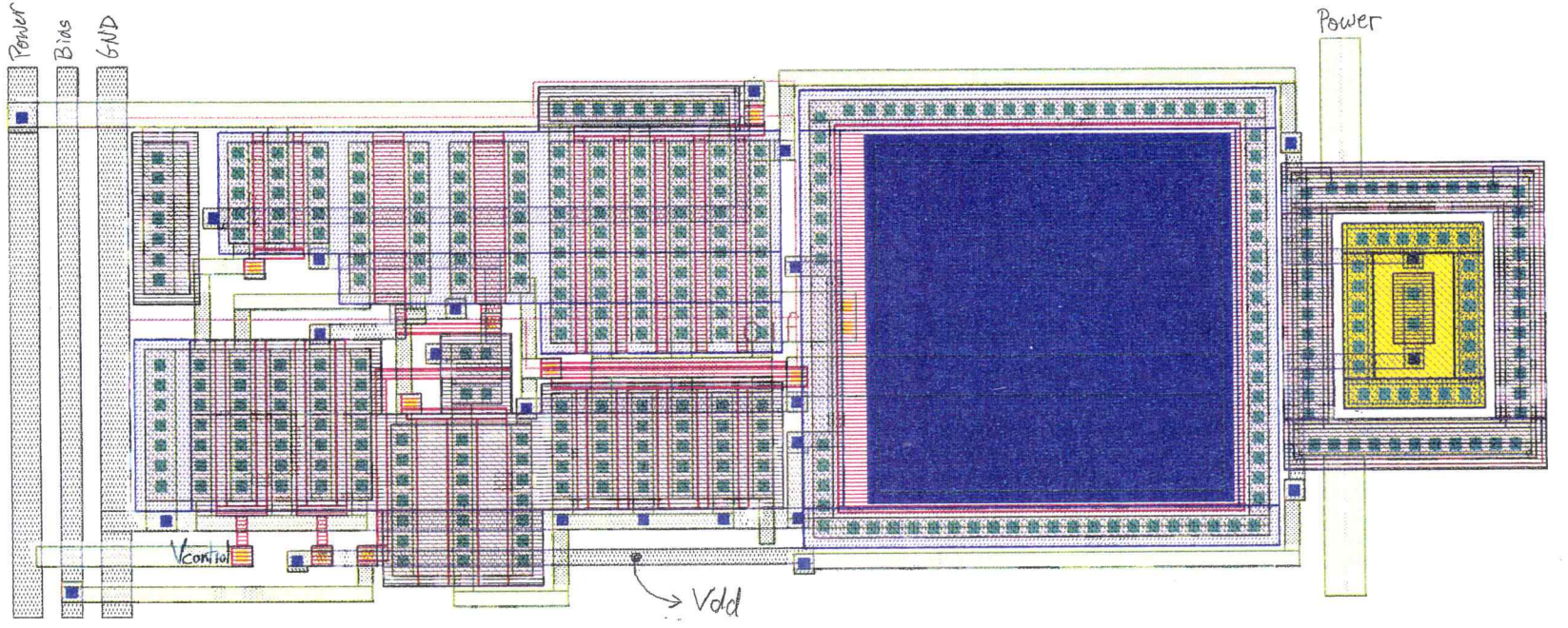

Figure A.1: Layout of the Power Supply

Figure A.2: Layout of a Biquad