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The primary objective of this thesis is to develop a process for fabricating integrated circuits based on thin-film transistors (TFTs) using zinc tin oxide (ZTO) as the channel layer. ZTO, in contrast to indium- or gallium-based amorphous oxide semiconductors (AOS), is perceived to be a more commercially viable AOS choice due to its low cost and ability to be deposited via DC reactive sputtering. In the absence of an acceptable ZTO wet etch process, a plasma-etching process using Ar/CH_4 is developed for both 1:1 and 2:1 ZTO compositions. An Ar/CH_4 plasma etch process is also designed for indium gallium oxide (IGO), indium gallium zinc oxide (IGZO), and indium tin oxide (ITO). Ar/CH_4 dry etches have excellent selectivity with respect to SiO_2, providing a route for obtaining patterned ZTO channels. A critical asset of ZTO process integration involves removing polymer deposits after ZTO etching without active layer damage.

A ZTO process is developed for the fabrication of integrated circuits which use ZTO channel enhancement-mode TFTs. Such ZTO TFTs exhibit incremental and average mobilities of 23 and 18 $cm^2V^{-1}s^{-1}$, respectively, turn-on voltages approximately 0 to 1.5 V and subthreshold swings below 0.5 V/dec when annealed in air at 400 °C for 1 hour. Several types of ZTO TFT circuits are realized for the first time. Despite large parasitic capacitances due to large gate-source and gate-drain overlaps, AC/DC rectifiers are fabricated and found to operate in the MHz range. Thus, they are usable for RFID and other equivalent-speed applications. Finally, a ZTO process for simultaneously fabricating both enhancement-mode and depletion-mode TFTs on a single substrate using a single target and anneal step is developed. This dual-channel process is used to build a high-gain two-transistor enhancement/depletion inverter. At a rail voltage of 10 V, this inverter has a gain of 10.6 V/V, the highest yet reported for an AOS-based inverter. This E/D inverter is an important new functional block which will enable the realization of more complex digital logic circuits.

Zinc Tin Oxide Thin-Film Transistor Circuits

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I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Daniel Philip Heineck, Author

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1. INTRODUCTION

Amorphous oxide semiconductors (AOS), have captured manufacturers interest as both a replacement for hydrogenated amorphous silicon (a-Si:H) in flat screen displays and for high-volume reel-to-reel processing applications involving flexible substrates. AOSs consist of the combinations of several optically-transparent transition and post-transition metal oxides with $(n-1)\mathrm{d}^{10}n\mathrm{s}^{0}$ (where $n \geq 4$) cation electronic configurations. These oxides derive their conduction bands from the cation's ns orbital, which is spherically-symmetric with a large orbital radius. High electron mobilities with low sensitivity to crystalline disorder are found in these AOS materials as a result of the significant overlap between these large-radius ns orbitals. The most common AOS materials are synthesized from Ga_2O_3, In_2O_3, SnO_2, and ZnO into multicomponent oxides such as indium gallium oxide (IGO), indium gallium zinc oxide (IGZO), zinc indium oxide (ZIO), and zinc tin oxide (ZTO). AOS thin-films remain atomically smooth over a wide range of processing conditions.

As the complexity of these AOS systems increases, tighter control over device parameters and fabrication processes are necessary. Presently, all reported AOS circuits use thin-film transistors (TFTs) with IGO or IGZO channels. Cost is a critically important factor in many of the potential AOS application spaces. Both indium and gallium are expensive materials. ZTO, which shows equivalent, if not superior TFT performance to In- and/or Ga-based AOS alternatives, employs inexpensive atomic constituents and is able to be deposited by DC reactive sputtering. The primary goal of this thesis is to develop a ZTO TFT circuit fabrication process. The second goal of this thesis is examine a route to synthesizing both enhancement- and depletion-mode TFTs on a single substrate in order to fabricate an enhancement/depletion (E/D) inverter.

The organization of this thesis is as follows. Chapter 2 introduces the technical background necessary and examines relevant literature in this field. Chapter 3 explains the experimental techniques and measurement systems used. Chapter 4 presents an etch study of ZTO and other materials, and the process integration details necessary to synthesize ZTO AC/DC rectifier circuits. This chapter then compares ZTO TFT circuit results with IGO-based rectifiers fabricated using the same integrated circuit mask set. Chapter 5 describes further ZTO TFT processing development and the fabrication and electrical characterization of ZTO enhancement-depletion inverters. Chapter 6 gives conclusions and recommendations for future work.

2. LITERATURE REVIEW & BACKGROUND

This chapter examines prior literature and knowledge of etching and integrating amorphous oxide semiconductors (AOS) for the fabrication of integrated circuits. Viable plasma etch chemistries for AOS layers are shown and the etch mechanisms involved are described. Careful documentation of known indium tin oxide (ITO) and zinc oxide (ZnO) etch gas feeds provides insight into the anticipated results presented in Chapter 4. Thin-film transistors are introduced and given a basic description. Additionally, zinc tin oxide (ZTO) and indium gallium zinc oxide (IGZO) are discussed as an active channel material in thin-film transistors.

2.1 Amorphous Oxide Semiconductor Plasma Etching

While wet etch chemistries can be designed to have near infinite etch selectivity, they suffer from high material cost, expensive waste management, poor sidewall behavior, and sensitivity to material crystallinity and grain boundaries [1, 2, 3]. Wet etching ITO in either HCl or aqua regia ultimately leaves a conductive residue behind [1, 4]. Dry etches use a higher percentage of their reactive feedstock for etching, can be highly anisotropic, which allows for sidewall profile engineering, and are relatively insensitive to grain boundaries. Since AOS materials come from only a selected portion of the periodic table, their etch mechanisms are similar and, thus, the etch literature for ZnO, indium zinc oxide (IZO) and ITO serves to predict results given in Chapter 4 for IGO, IGZO, ITO, and ZTO.

Table 2.1: Boiling points for gallium, indium, tin and zinc volatile compounds at 1 atmosphere pressure. Boiling points at atmospheric pressure from expected plasma etch products provide insight into their volatility which, in turn, is useful for predicting the efficacy of reactive gases in etching AOS materials. Since etch product desorption is the rate-limiting step in AOS etching, products with lower boiling temperatures yield higher vapor pressures and etch rates for RIE systems [5].

Compound Name	**Chemical Formula**	**Boiling Point °C**
gallium(III) hydride	H_3Ga	0
dimethyl zinc	C_2H_6Zn	46
trimethylgallium	C_3H_9Ga	55.7
tetramethyltin	$C_4H_{12}Sn$	74-78
tin(IV) chloride	Cl_4Sn	114.1
trimethyl indium	C_3H_9In	135.8

Continued on next page

Table 2.1 Continued

Compound Name	Chemical Formula	Boiling Point °C
chlorotrimethylstannane	C_3H_9ClSn	148-156
trimethyltin bromide	C_3H_9BrSn	164
methyltin trichloride	CH_3Cl_3Sn	171
hexamethyldistannane	$C_6H_{18}Sn_2$	182
triethyl indium	$C_6H_{15}In$	184
gallium(III) chloride	Cl_3Ga	201
tin(IV) bromide	Br_4Sn	202
dimethyltin dibromide	$C_2H_6Br_2Sn$	208-213
gallium(III) bromide	Br_3Ga	278-279
gallium(III) iodide	I_3Ga	345
tin(IV) iodide	I_4Sn	364
gallium(II) chloride	Cl_2Ga	535
indium(I) chloride	ClIn	608
stannous bromide	Br_2Sn	619.9
zinc bromide	Br_2Zn	649.9
indium(I) bromide	BrIn	656
tin(II) iodide	I_2Sn	714-717
zinc chloride	Cl_2Zn	732
indium(III) chloride	Cl_3In	800
tin(II) fluoride	F_2Sn	850
indium(III) fluoride	F_3In	1200
zinc fluoride	F_2Zn	1500

Table 2.1 shows many of the volatile metal-halide and organometallic compounds for gallium, indium, tin, and zinc, all of which have high boiling points at atmospheric pressure, necessitating either heating, physical sputtering, or both to remove reacted species from the surface. Fluorine and iodine chemistries have nominally higher boiling points than bromine and chlorine chemistries, but the organometallic species, especially those with methyl ligands, show the greatest promise [5]. Three interlinked and simultaneous processes are responsible for etching amorphous oxides: metal reduction by oxygen removal, volatilization of metals from reactive neutrals and ions, and

sputtering. Ultimately, the greatest challenge in etching AOS materials is overcoming the low volatility of their reaction products, while minimizing etch damage and achieving material etch selectivity. Studies reported in this section propose etch solutions by using the gases in the following list:

- BBr_3 [6]
- BCl_3 [7, 8, 9]
- BI_3 [6, 10]
- CF_4 [11, 12, 13]
- CF_3Cl and CF_2Cl_2 [11]
- CH_4 [3, 4, 6, 9, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22]
- CHF_3 [12]
- Cl_2 [6, 7, 8, 9, 12, 19, 23, 21]
- H_2 [3, 6, 9, 14, 15, 16, 17, 18, 19, 21, 22]
- HBr [2, 4, 24]
- HCl [4]
- IBr [6, 10]
- ICl [6]
- $SiCl_4$ [13]

and combinations thereof, with or without the use of argon as a sputter gas in their feedstocks.

2.1.1 Indium Tin Oxide Etches

This section discusses the significant results presented in the ITO etch literature. Several common traits are immediately noticed in these studies, such as the preferential etching of tin and oxygen. This effect is likely due to the higher volatility of tin halides and tetramethyl tin relative to indium-containing compounds [4, 5, 15, 20]. In several studies, H_2 shows no positive etch benefit in comparison to either CH_4 or Ar [3, 14, 17]. In the Ar/CH_4 chemistries, peak etch rates occur at low methane concentrations, ranging from 10% [17, 20] to 35% [14]; Kim shows a comparable peak etch rate with a gas flow composition of 20/60/20 sccm of $Ar/H_2/CH_4$ [15]. Higher methane concentrations yield polymer formation, and a decrease in etch rate results as the polymer film competes for surface area, so high argon concentrations are necessary to break up the film's growth and accelerate etch product desorption. Hydrogen bromide and hydrogen chloride chemistries, with their obvious benefit of reduced residues, are also studied. These hydrogen halide gas feeds provide slightly decreased etch rates in comparison to methane-based chemistries, but nevertheless are another viable option [2, 4, 24]. High ion bombardment energies greatly accelerate etch processes due to both higher sputter yields and increased substrate temperature, but no data

is found on the electrical effects of the increased etch damage as a result of the higher ion energies [2, 3, 13, 15, 16, 17, 18, 24]. In capacitively-coupled plasma (CCP) systems, etch rate increases with input power due to both higher plasma densities and higher incident ion energies.

H_2/CH_4: Mohri *et al.*, 1990 With a fixed throttle and a constant flow of 10 sccm of H_2, the effects of varying CH_4 flow on etch rate are reported, yielding a peak etch rate at 1 sccm of CH_4. This result appears more pressure dependent than gas composition dependent, since the etch rate rises again after a minimum at 4 sccm CH_4 flow. Both power and substrate temperature are varied, resulting in a linear power and an exponential temperature response [18].

CF_4, CF_3Cl, and CF_2Cl_2: Kuo, 1990. Kuo examines these gases for effects on surface chemistry rather than etch rate. He observes a severe drop in the Sn:In ratio during etching, and notes that the effect is greater with Cl than F. Consistent with other sources, the surface is oxygen deficient after all three etches. Etch rate increases along with Cl, F and O surface concentrations when the gas is changed to 20/80 N_2/CF_2Cl_2. Similar surface concentrations are noted with Ar instead of N_2, but the etch rate is even higher for a 20/80 Ar/CF_2Cl_2 gas ratio. A 65/35 N_2/CF_2Cl_2 stream exhibits a lower etch rate due to nitride growth on the surface, which acts as an etch block [11].

H_2/CH_4: Adesida *et al.*, 1991. Adesida reports a broad peak in etch rate starting at a 50/50 H_2/CH_4 gas ratio and peaking at a 20/80 H_2/CH_4 feed. While virtually no polymer formation is measured between pure H_2 and a 50/50 H_2/CH_4 ratio, the formation rate increases linearly with higher CH_4 concentration, giving the etch near-perfect selectivity against GaAs. Between 25 mTorr and 150 mTorr, the etch rate for a 75/25 H_2/CH_4 gas feed increases linearly with pressure, likely due to an increase in plasma density and reactive neutral density. Likewise, etch rate increases linearly with substrate power, which suggests that both ion density and velocity each cause the etch rate to linearly increase [16].

HBr: Tsou, 1993. In his examination of etch characteristics of pure HBr, Tsou uses an OES to measure the 325 nm line intensity, which correlates to atomic indium. A slow etching induction period occurs before the line intensity spikes, which correlates to a rapid increase in etch rate. The increase in substrate temperature from 50 °C to 75 °C, shortens the induction period from 64 s to 48 s, and the total etch time for a 110 nm ITO film decreases from 136 s to 114 s. Due to system capability, an Ar plasma bombardment before the HBr etch is applied to heat the wafer. With the additional substrate temperature acquired during a 60 s or longer

Ar bombardment, the induction period disappears. Line intensity, which correlates with etch rate, shows a linear dependance on RF power in the post-Ar bombardment HBr etch step, likely due to both plasma density and ion bombardment energy. Lastly, etch selectivity of ITO compared to both photoresist and SiO_2 increases with RF power [24].

H_2/CH_4: Nakamura *et al.*, 1994. A positive correlation between etch rate and CH_4 percentage is reported, and the highest rate is observed in a pure CH_4 feed. Etch rate shows a moderate temperature dependence. The substrate temperature rises from 99 °C to 145 °C as electrode bias increases from -160 V to -400 V, implying that an increase in both ion energy and substrate temperature yield an increase in etch rate [3].

HBr: Takabatake *et al.*, 1995. In examining HBr as an etch gas, Takabatake *et al.* observe a linear relationship between electrode power density and etch rate for both amorphous and polycrystalline ITO. Etch rate increases with gas flow at low flows due to higher pump speeds at constant pressure. However, etch rates decrease at high flow rates due to the pumping of reactive species before they can impinge on to the surface. A relationship in which lower pressure results in an increase in etch rate is also demonstrated [2].

$SiCl_4$, $SiCl_4/CF_4$, $SiCl_4/CH_4$, and $SiCl_4/CF_4/CH_4$: Kuo, 1997. Under otherwise identical conditions, Kuo reports the following gases etch ITO in increasing order: $SiCl_4$, $SiCl_4/CF_4/CH_4$, and $SiCl_4/CF_4$. The use of $SiCl_4$ results in Si deposition, which serves to mask the surface, thus CF_4 is introduced to remove the Si contamination. The introduction of CH_4, described as an ineffective etchant in this system, does not materially reduce the etch rate, yet it serves to protect the photoresist from $SiCl_4$ and CF_4 attack. A thick residue of Si, C, and O is observed on the surface after $SiCl_4/CH_4$ etching, whereas a much thinner layer is noted after $SiCl_4/CF_4$ etching. Lastly, results show a high correlation between etch rate for $SiCl_4/CF_4/CH_4$ and electrode power [13].

HCl/CH_4 and HBr/CH_4: Kuo and Tai, 1998. Kuo and Tai vary CH_4 percentage in both HCl/CH_4 and HBr/CH_4 gas chemistries after heating the substrate to 250 °C in order to improve etch product desorption. Peak etch rate occurs at a 60/40 HCl/CH_4 gas ratio, and decreases rapidly in both directions. This HCl/CH_4 combination is approximately 2.5x faster than the fastest HBr/CH_4 composition, which maintains its maximum between 100% HBr and 60/40 HBr/CH_4 before declining. A pure HBr gas stream etches ITO faster than pure a pure HCl gas stream, however. Like other sources, the surface is Sn deficient, due to preferential etching. A significant loading factor is noted near photoresist edges, where CH_3

polymerizes rapidly on the photoresist, which lowers the local CH_3 concentration. In the case of a 20/80 HBr/CH_4 gas stream, ITO surfaces close to photoresist features are etched due to the lower local CH_3 concentration, but a significant polymer growth and little ITO etching is reported in areas remote to photoresist patterns, such as large openings [4].

Ar/CH_4 and Ar/H_2: Park *et al.*, 2000. In a comparison of Ar/CH_4 percentage versus etch rate, a minor peak at a ratio of 65/35 is observed which strongly decreases by 40/60 and reaches its minimum with pure CH_4. Etch selectivities (e.g. relative etch rate of one material compared to another) are respectively ∼5 and ∼9 for SiO_2 and Si_3N_4 at a 65/35 Ar/CH_4 composition. When measured using a quadrupole mass spectrometer (QMS), the 65/35 Ar/CH_4 feed resides on a local peak in CH_3 concentrations and is very near the atomic hydrogen (H) peak, which occurs at an Ar/CH_4 ratio of 70/30. OES intensity measurements bear out a similar relationship in H concentrations, but the intensity of the CH line increases with CH_4 concentration until 50/50 Ar/CH_4, where it saturates. The decrease in etch rate beyond 35% CH_4 is likely due to polymer formation, which inhibits both chemical reaction and ion bombardment. In the Ar/H_2 experiment, etch rates decrease monotonically with an increase in H_2 concentration and both QMS and OES measurements show that H concentration increases from pure Ar to 70/30 Ar/CH_4 ratio and saturates thereafter. It does not appear that H_2 has a significant positive impact on the etch rate [14].

Ar/CH_4: Lee *et al.* 2001. The relationship between etch rate and CH_4 concentration is examined along with the rate effects of substrate material and thickness. Like Meziani, the peak etch rate occurs at 90/10 Ar/CH_4, and a higher etch rate is observed in thinner substrates, where a 0.7 mm glass, and both a 0.5 mm and a 0.18 mm polycarbonate substrate are tested. Post-etch surface roughness increases markedly at 70/30, where polymer formation becomes significant. The surface also becomes Sn and O deficient due to preferential etching [20].

Ar/H_2, Ar/CH_4, and H_2/CH_4: Meziani *et al.*, 2006. Unlike Park, et al., Meziani *et al.* do not observe a decrease in etch rate until 50/50 Ar/H_2, where it begins to linearly decline with further increases in H_2. Both H_2/CH_4 and Ar/CH_4 exhibit their peak etch rates at a 90/10 gas composition, but the Ar/CH_4 combination is ∼10x faster than H_2/CH_4 under the same conditions. A logarithmic relationship between CH_4 percentage in an Ar/CH_4 feed and the H and CH OES line intensities is reported, but these line intensities never saturate. A Langmuir probe analysis shows an exponentially decreasing relationship between plasma density and CH_4 concentration. Successful endpoint detection is realized using the intensity

of the 410.18 nm In line relative to the 415.86 nm Ar reference line. No noticeable surface roughening is observed after etching [17].

$Ar/H_2/CH_4$: Kim *et al.* 2008. An effectively infinite etch selectivity between ITO and photoresist is observed at 20/60/20 sccm gas composition due to polymer formation on the photoresist. Further increases in CH_4 concentration results in polymer formation on all surfaces, stopping the etch outright. Using a constant flow of 20 sccm Ar and varying H_2 and CH_4, the line intensities decrease and increase, respectively with an increase in CH_4 concentration, showing that H generated from CH_4 dissociation is significantly lower than H_2 dissociation. Tin, followed to a lesser degree by oxygen is preferentially etched from the surface, with the In:Sn ratio increasing with electrode bias. The electrode bias dependence indicates that reacted tin species have higher volatilities and sputter yields [15].

2.1.2 Zinc Oxide and Indium Zinc Oxide Etches

A summary of selected literature on ZnO and IZO etch experiments is presented in this section. For ZnO and IZO etching, methane and chlorine-based (BCl_3, Cl_2, HCl) gas feeds are most effective. Several studies note significant sidewall roughening when a large percentage of the stream is Cl_2-based [8, 23], surface pinholes for BCl_3-based feeds [7, 9], and surface nodules using a $Ar/H_2/CH_4$ gas composition [21]. As in ITO etches, ion bombardment is critical to the removal of reacted species from the surface, given their low volatilities: $(CH_3)_2Zn$ has a vapor pressure of 301 Torr at 20 °C, Cl_2Zn is 1 Torr at 428 °C, and F_2Zn is 1 Torr at an impossibly high temperature of 1243 °C [12]. For IZO etching, methane-based gas feeds are preferred to chlorine-based feeds due to their higher etch rates. Indium is preferentially etched in IZO, which is counterintuitive based on the information given in Table 2.1. IZO etch rates are shown to be relatively independent of crystallinity [6, 10, 21].

H_2/Cl_2, H_2/CHF_3, H_2/CF_4, and H_2/CH_4: Lee *et al.*, 2001. A H_2/CH_4 combination is noted to etch 6x faster than both H_2/Cl_2 and H_2/CHF_3, and ∼5x faster than that of H_2/CF_4, under otherwise identical conditions. The gas composition is a 2:1 ratio of the selected etch gas and H_2. With the inclusion of Ar to H_2/CH_4, the etch rate of a 16/8/30 sccm $Ar/H_2/CH_4$ gas feedstock linearly increases with electrode bias, indicating a strong dependence on ion assisted removal of $(CH_3)_2Zn$ from the surface [12].

Ar/Cl_2: Lim *et al.*, 2003. Lim, *et al.* note $ZnCl_2$ desorption has a strong temperature dependence. Etch rate and Cl surface concentration respectively increase and decrease with an

increase in temperature. A 300 °C etch results in rough and undercut sidewalls, whereas 150 °C etches are relatively smooth [23].

Ar/BCl_3, $Ar/BCl_3/Cl_2$, and $H_2/BCl_3/CH_4$: Kim *et al.*, 2003 and 2004. Kim *et al.* determine that BCl_3 is the major etch gas in ZnO, since maximum etch rate occurs with pure BCl_3 for both the $Ar/BCl_3/Cl_2$ and Ar/BCl_3 gas feeds [7]. Later, BCl_3 percentage is varied in a $H_2/BCl_3/CH_4$ gas feed where the H_2:CH_4 ratio is held at 1:3. Etch rate increases until reaching a 60% BCl_3 content, where the rate saturates [9]. The pure BCl_3 feed for ZnO shows the following characteristics: a weak, but positive temperature dependence over the 25-250 °C range, a linear relationship between electrode power and etch rate, and a peak etch rate at 5 mTorr. A pure BCl_3 etch also creates pinholes on the surface, likely due to oxygen vacancies [7, 9].

Ar/Cl_2, Ar/BCl_3, and $Ar/BCl_3/Cl_2$: Na *et al.*, 2006. The peak etch rate of an Ar/Cl_2 feedstock in this study occurs at 80% Cl_2, but the etch rate is relatively constant between 80/20% and pure Cl_2. There is an initial increase between pure Ar and 80/20 Ar/Cl_2, however. Chlorine ion and radical optical emission intensities saturate beyond 20% Cl_2, indicating that the Cl–Zn surface interaction is a more significant process than Ar sputtering. The Ar/BCl_3 etch rate peaks at a 80/20 composition. When 5-10% Cl_2 is also introduced to this gas composition, a small increase in rate occurs, but any additional Cl_2 decreases the rate, suggesting that ∼70/30% Ar/BCl_3, which was not tested, may actually be nearer to the optimum etch Ar/BCl_3 composition. The peak Ar/Cl_2 gas stream etch rate is higher than the peak Ar/BCl_3 gas flow, but the 20/80 Ar/Cl_2 combination shows significant surface and sidewall roughness [8].

Ar/Cl_2, Ar/BI_3, Ar/IBr, Ar/ICl, Ar/BBr_3, and $Ar/H_2/CH_4$: Lim *et al.*, 2006 and 2007a. Of all the gas streams tested in this study, only the Ar/Cl_2 and $Ar/H_2/CH_4$ gas streams report an etch rate faster than that of pure Ar sputtering. Lim *et al.* again examine amorphous and polycrystalline IZO, with respective 2:3 and 3:1 In:Zn ratios, for their etch rate compared to single crystal ZnO. In varying Ar percentage in the gas stream, Lim *et al.* report a peak ZnO etch rate at 30/70 Ar/Cl_2 flow ratio. The etch rate for ZnO plateaus between 40/46/14 $Ar/H_2/CH_4$ and 100% Ar, but no data exists between these two points [21]. The $Ar/H_2/CH_4$ feed etches the two IZO films fastest, slowly increasing in etch rate until 40% Ar. Again, no data is provided between 40% Ar and 100% Ar [6]. Under the same conditions, a-IZO etches slightly faster than poly-IZO, which is attributed to the

higher In content in the supplied a-IZO film, and both films etch faster than ZnO [6]. Surface nodules are noted in the images of an etch using a 8/10/3 sccm $Ar/H_2/CH_4$ gas stream and to a lesser extent in a 8/10 sccm Ar/Cl_2 system as well. These nodules are either due to preferential indium etching or polymer formation [21].

Ar/BI_3 and Ar/IBr: Lim *et al.*, 2007b. Comparing the etch rates of single-crystal ZnO to different stoichiometries and degrees of crystallinity for IZO, Lim *et al.* find that both BI_3 and IBr have ∼3-5x slower etch rates than pure Ar sputtering under the same conditions. Etch rate in Ar increases with the film's indium content, where the etch rate of In:Zn 1.44:1 is higher than 0.33:1, and both polycrystalline IZO films have higher etch rates than a-IZO, which has an In:Zn ratio of 2:3. Crystalline ZnO has lowest etch rate, significantly slower than a-IZO. Etch rate of BI_3 and IBr were linear to the square root of the electrode DC bias, implying that ion bombardment energy is critical to the etch performance [10].

2.1.3 Common Etch Characteristics

While specific gas chemistries ultimately yield different results, general trends from all selected prior literature are extracted, showing some major mechanisms. In inductively-coupled plasma (ICP) based etchers, an increase in coil power at a constant substrate electrode power yields a linear increase in etch rate [6, 7, 9, 10, 12, 15, 17]. Increased plasma density yields higher ion and reactive neutral fluxes to the surface of the substrate, which pushes the reaction towards products. The linear increase in etch rate with coil power indicates that the etched surface does not become saturated with reacted species, such as those listed in Table 2.1. Na *et al.*, however, report a reduced etch rate with coil power, due to an increase in plasma density causing a higher ion flux to the surface. Under a constant electrode power, higher ion currents require less DC substrate bias. The lower DC bias reduces average ion bombardment energy, lowering the sputter effect [8].

Desorption of these reacted species from the surface is likely the rate-limiting step, given their low vapor pressures. Thus, an increase in ion flux to the surface enhances etch product removal via increased sputtering or physical heating. The substrate bias at a constant coil power is gas feedstock-dependant, yet all noted ICP-based etch literature which compares etch rate to substrate bias show a positive correlation between etch rate and substrate power [3, 6, 7, 8, 9, 10, 12, 15, 17, 19, 23]. Lastly, ITO and ZnO etch processes prove to be highly dependent on temperature, largely following an Arrhenius relationship between temperature and etch rate [3, 7, 13, 18, 23, 24].

2.1.4 Oxygen Removal Mechanisms

From the gas feedstocks listed at the end of Section 2.1, several chemical mechanisms are proposed which could liberate oxygen from the surface, and thus reduce metal on the surface. Other than sputtering and displacement by a more reactive species, e.g., fluorine radicals displacing oxygen according to $2ZnO+4F \rightarrow 2ZnF_2(s)+O_2(g)$, gases containing boron, carbon, and hydrogen reduce metal oxides by producing volatile species. Boron reacts with oxygen to create B_xO_y, nominally x=1 and y=2. In the case of BCl_3 chemistries, oxygen is removed as BOCl or $(BOCl)_3$ [7, 8, 9]. Carbon favorably reacts to reduce metal oxides, devolving as CO or CO_2 [25]. The reaction between atomic hydrogen and oxygen predictably yields water vapor.

In general, the oxygen surface concentration remains the same or decreases after etching, suggesting that oxygen removal is not the rate-limiting step in AOS etching. Kim *et al.* show lower contact resistance between ZnO and a Ti/Au stack after a 30 second BCl_3 treatment, which is attributed to an increase in oxygen vacancies at the interface, effectively doping the surface more n-type [9]. Kuo, in an etch study using different freon gas feedstocks reports that the oxygen concentration decreases dramatically after etching [11]. In etching ITO with an Ar/CH_4 feedstock, Lee *et al.* find that the percentage of oxygen decreases with an increase in CH_4 concentration [20]. Lim *et al.* do not note a change in ZnO surface chemistry in an Ar/IBr gas feed, but this is not unexpected, given the absence of a major reducing agent [10]. In an Ar/Cl_2 gas feed, both Lim *et al.* [23] and Na *el al.* [8] report an increase in the Zn:O ratio, suggesting that chlorine radicals displace oxygen. Na finds that the Zn:O ratio decreases in a pure argon plasma, implying that zinc is preferentially removed from the surface under pure sputtering conditions [8]. Ip *et al.*, however, report no such stoichiometric change in his surface Zn:O ratios after etching in an $Ar/CH_4/H_2$ plasma [19]. As an exception, Kim *et al.* show an increase in oxygen compared to indium and tin in etching ITO with the same $Ar/CH_4/H_2$ gas combination. However, the surface oxygen is tied up in C-O bonds, suggesting surface contamination [15].

2.1.5 Conclusion

A study of the literature of ZnO, IZO and ITO shows a great diversity in etch parameters and gas feeds. The etch gases that most consistently result in high etch rates are chlorine-based (BCl_3, Cl_2 and HCl), methane, and hydrogen bromide, or combinations thereof. Argon as a sputter gas is critical to volatilizing etch products by providing significant energy to the surface. This concludes the introduction of prior plasma etch literature on AOS materials.

2.2 Thin Film Transistors

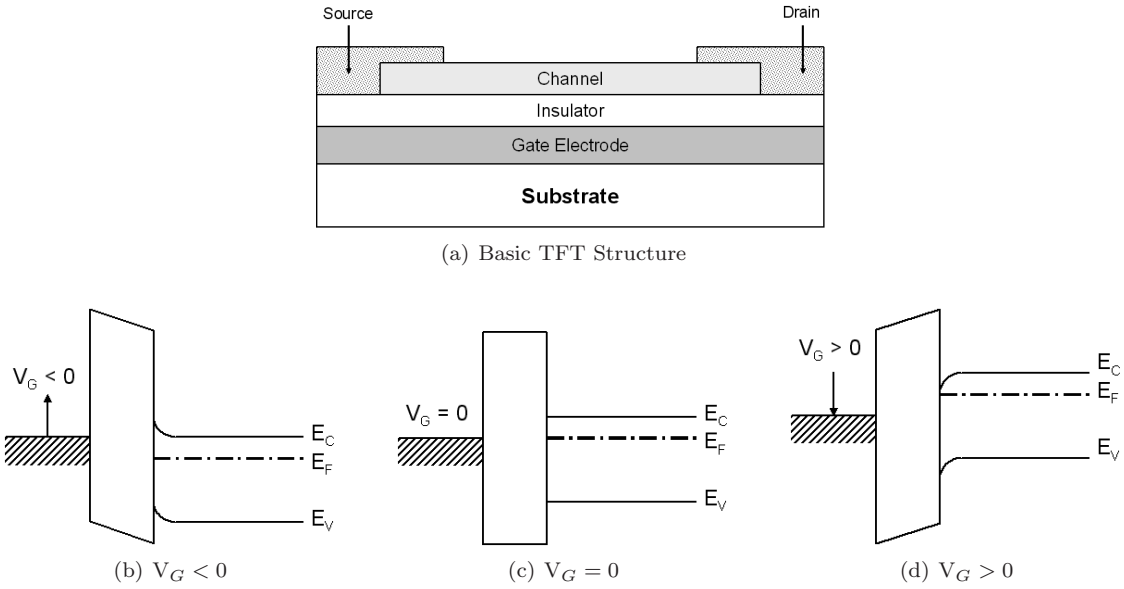
The basic premise of a thin-film transistor was first patented by J.E. Lilienfeld in 1934 [26] and developed more completely by P.K. Weimer in 1962 [27]. TFTs have been made using CdS, CdSe, hydrogenated amorphous silicon (a-Si:H), and polycrystalline silicon (poly-Si) as the active channel material. Best known for their use in active-matrix liquid crystal displays (AMLCD), the typical range of mobilities for a-Si:H, and poly-Si are 0.5-1.0, and 10-80 $cm^2V^{-1}s^{-1}$, with maximum processing temperatures around 300 °C and 500-600 °C, respectively [28]. More recently, paper and conference proceedings from major semiconductor manufacturers discussing AOS channel materials, such as IGZO, ZIO, and ZTO have been been published.

A simple description of TFT electrical operation and major TFT structural designs serve to inform further discussion of TFT-based integrated circuits and AOS channel materials.

2.2.1 Basic TFT Electrical Behavior

Thin-film transistors are field-effect devices. Therefore, much of the knowledge of MOS/MIS devices can be applied to TFTs. Figure 2.1 shows a basic TFT structure (2.1(a)) with a n-type channel and band diagrams of the structure under reverse bias, at equilibrium, and under forward bias. Figure 2.1(c) shows an idealized equilibrium energy band diagram with no band bending, and thus interface charge, at zero gate bias. In reality, bulk and interface traps, along with trapped and mobile charges in both the insulator and semiconductor significantly affect the gate voltage necessary to achieve a flat-band condition. Channel materials discussed herein are all unipolar since, given their wide bandgaps, intrinsic carrier concentrations are vanishingly small ($n_i \approx 10^{-8}$ cm^{-3}). Inversion of such wide bandgap channel layers is impossible given the presence of of band tail states and deep level traps and the magnitude of the surface potential modulation required before inversion is possible [29].

In reverse bias, Fig. 2.1(b) shows that delocalized electrons in the semiconductor are swept away from the channel–insulator interface, thus depleting the semiconductor, as indicated by the bending of the conduction band (E_C) upwards, away from the Fermi level (E_F). The positive space charge region at the interface results from a balance ($Q_M = -Q_S$) between the metal gate charge (Q_M) and the semiconductor charge (Q_S). For the scope of this thesis, the semiconductor charge is assumed to be a sheet of charge located at the semiconductor–insulator interface, since all channel conduction occurs within approximately 3 nm of the interface [30]. The opposite arises in Fig. 2.1(d)in forward bias beyond V_{ON} where mobile electrons are accumulated at the channel-insulator interface, as evident by the conduction band bending downwards, towards the Fermi level.



(a) Basic TFT Structure

(b) $V_G < 0$ (c) $V_G = 0$ (d) $V_G > 0$

Figure 2.1: Basic TFT structure and the idealized energy band diagrams of the gate, insulator and n-type semiconductor. Energy band diagrams show the gate under (b) reverse bias ($V_G < 0$), (c) equilibrium ($V_G = 0$), and (d) forward bias ($V_G > 0$).

As shown in Fig. 2.1(b) under reverse gate bias, electrons are depleted from the channel. Thus, mobile charge is unavailable to support the flow of drain current. Ideally the channel resistance (R_{CH}) in the cutoff regime is infinite. The domain of this region defines V_{ON} since V_{ON} is empirically defined by the onset of drain current: $I_D = 0$ for $V_{GS} < V_{ON}$ [31]. Under forward gate bias, the channel has a finite resistance, permitting the injection of electrons from the grounded source electrode into the channel, with subsequent extraction from the drain, if there is a positive drain-to-source voltage (V_{DS}). As V_{DS} increases, the depletion region around the drain becomes significant, and the resulting I_D is no longer linear with respect to V_{DS}. Eventually, I_D saturates when the channel region around the drain becomes completely depleted of carriers, or pinched-off.

The two main regimes of TFT device operation are appropriately called pre-pinch-off and post-pinch-off, and are defined by the square-law model [29]. For the pre-pinch-off regime,

$$I_D = \frac{W}{L}\mu C_G[(V_{GS} - V_{ON})V_{DS} - \frac{V_{DS}^2}{2}] \,, \tag{2.1}$$

where $\frac{W}{L}$ is channel width-to-length ratio, μ is the mobility (see Section 3.3.3 for more details), and C_G is the gate capacitance density, given in units of F cm^{-2}. The voltage necessary to saturate I_D is defined by V_{DSAT} and serves to separate the two major regimes of TFT device operation. Beyond V_{DSAT}, drain current ideally becomes independent of V_{DS}, and this effective V_{DS} is pinned to

$V_{GS} - V_{ON}$, i.e., $V_{DSAT} = V_{GS} - V_{ON}$. By substituting the effective V_{DS} back into Eq. 2.1, the post-pinch-off regime is obtained as V_{DSAT},

$$I_D = \frac{W}{2L}\mu C_G(V_{GS} - V_{ON})^2 \ . \tag{2.2}$$

V_{DSAT}, and thus I_{DSAT} are dependent on the gate voltage, since further accumulation requires a higher drain voltage to deplete the channel, and vice-versa.

A subset of the pre-pinch-off regime is the linear regime, where under very low V_{DS} bias, on the order of several k_BT, the drain depletion region is nonexistant and the $\frac{V_{DS}^2}{2}$ term is neglible, yielding

$$I_D = \frac{W}{L}\mu C_G(V_{GS} - V_{ON})V_{DS} \ . \tag{2.3}$$

The accumulated channel charge density, Q_{CH}, is equal to $C_G(V_{GS} - V_{ON})$ in units of Coul cm^{-2}, and the channel resistance is $R_{CH} = \frac{W}{L}\mu Q_{CH}$. In the linear regime, the injection and extraction of carriers from the channel is drift-dominated, and is governed by a linear relationship between I_D and V_{DS} as given by,

$$I_D = \frac{V_{DS}}{R_{CH}(V_{GS})} \ , \tag{2.4}$$

where R_{CH} is dependent on V_{GS} [29].

TFTs which require a negative bias to be driven into cutoff are defined as depletion-mode devices. An ideal V_{ON} for a n-channel TFT is zero. Non-idealities, such as insulator charges nominally associated with flatband voltage correction in MOS technologies, and bulk and interface trap charges in the channel, shift V_{ON}. Flatband voltage correction is beyond the scope of this thesis. The reader is encouraged to refer to Sze & Ng [32] for further information on this subject.

2.2.1.1 Discrete Trap Model

Although bulk and interface traps can occur over a energy continuum, a discrete trap model simplifies computation and aids in the interpretation of trap effects on TFT performance. Given the unipolar nature of the channel materials considered herein, traps are assumed to only interact with conduction band electrons. This means that the trap-related parameters of interest are trap ionization energy (E_T), electron capture cross section (σ_n), and trap density (N_T). With a given nominal conduction band electron velocity ($\bar{\nu}$) and a constant capture cross-section (σ_n), the conduction band capture velocity is proportional to the conduction band electron density (n_c) and the empty trap density ($N_T - n_t$), where n_t is the density of occupied traps. The capture velocity is given by $\bar{\nu}\sigma_n(N_T - n_t)n_c$, and the emission rate from trapped electrons is modeled as $\bar{\nu}\sigma_n n_t n_1$.

The variable n_1 expresses the conduction band electron density when $\mathrm{E}_F = \mathrm{E}_T$. It is defined by,

$$n_1 = N_c \exp^{\frac{-E_T}{k_B T}} \ , \tag{2.5}$$

where k_B is the Boltzmann constant, and N_c is the conduction band effective density of states [33].

By applying the $C = Q \times V$ relationship to the discrete trap model, all channel charge is assumed to be concentrated at the the insulator-semiconductor interface. Likewise, any gate voltage induced charge must be distributed to both unoccupied traps states and conduction bands states according to,

$$q(n_c + n_t) = q(n_{c0} + n_{t0}) + q(\Delta n_c + \Delta n_t) \ , \tag{2.6}$$

where n_{c0} and n_{t0} are zero-bias conduction band and trap densities, respectively. By using the definition $(n_c + n_t) = 0$ when $V_{GS} = V_{ON}$, turn-on voltage is given by,

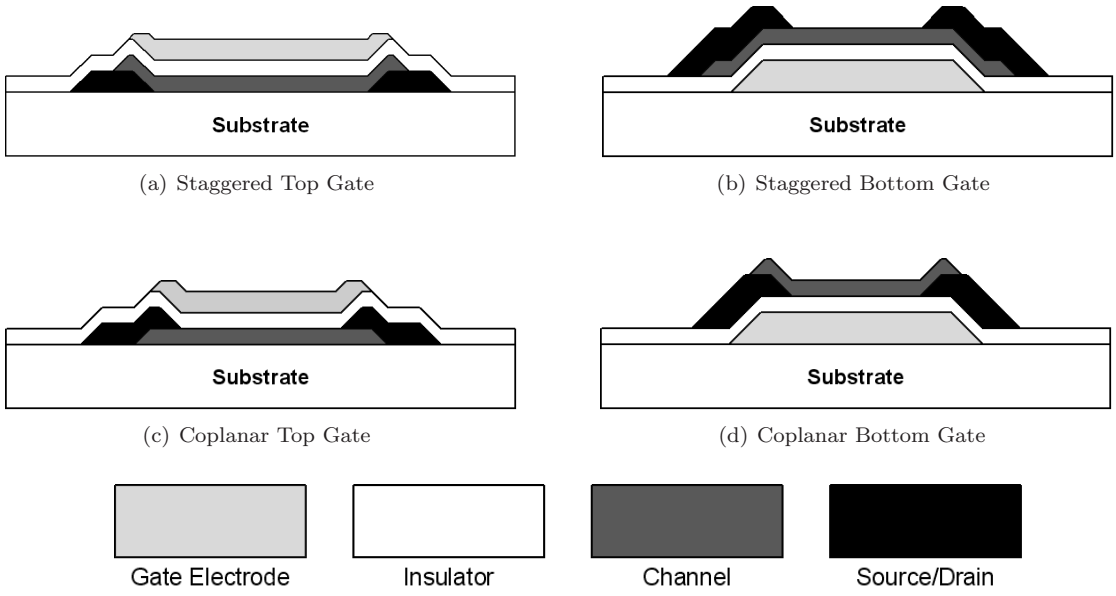
$$V_{ON} = -\frac{qh}{C_G}(n_{c0} + n_{t0}) \ , \tag{2.7}$$

where h is the channel thickness [33]. As V_{GS} is increased past V_{ON}, E_F approaches both E_C and E_T, and both conduction band and trap occupancy increase. Thus, the current increase from additional carriers is mediated by steady-state trapping, yielding a non-zero subthreshold swing value, and giving rise potentially to a "kink" in a $\log(I_D)$-V_{GS} curve, if N_T is significant. Threshold voltage, by definition within the discrete trap model, is the gate voltage necessary to fill all trap states. When $V_{GS} \geq V_T$ thin film transistors experience trap-free operation according to this model [33].

2.2.2 Basic TFT Structures

The major difference in a basic structure, i.e., that defined by a coplanar versus a staggered and a bottom-gate versus a top-gate, is established by the order in which the layers are deposited. Figure 2.2 shows the four major structure types. Staggered devices place the source/drain contacts furthest away from the channel–insulator interface, and benefit from lower contact resistance due to their larger effective contact area. Coplanar devices place source/drain contacts nearest to the interface, theoretically allowing for completely 2-D carrier transport along the channel–insulator interface, but at the cost of a smaller contact area. Coplanar devices also suffer the risk of causing damage to the semiconductor–insulator interface during source/drain deposition.

In both bottom-gate structures the gate electrode is directly followed by the insulator layer, whereas top-gate structures deposit the gate electrode onto the insulator. Since the insulator layer



(a) Staggered Top Gate

(b) Staggered Bottom Gate

(c) Coplanar Top Gate

(d) Coplanar Bottom Gate

Figure 2.2: The four basic thin-film transistor configurations are (a) staggered top-gate, (b) staggered bottom-gate, (c) coplanar top-gate, and (d) coplanar bottom-gate. The configurations are largely defined by the order in which the gate electrode, insulator, channel, and source/drain electrodes are deposited onto the substrate. The most commonly used configuration herein is the staggered bottom-gate structure.

typically involves the highest temperature and/or highest power density deposition process, channel materials must be quite robust in top-gate structures in order to provide an optimal interface. TFTs benefit from complete isolation since the substrate is typically insulating. However, since deposited films are amorphous or polycrystalline, device performance is typically not as high as for single-crystal devices. Likewise, more of the TFT is exposed to either the ambient atmosphere or the passivation layer, making both major surfaces of the channel significant to carrier transport [34].

2.3 Amorphous Oxide Semiconductors

Amorphous oxide semiconductors consist of several transition and post-transition metal oxides with $(n-1)\mathrm{d}^{10}n\mathrm{s}^{0}$ (where $n{\geq}4$) cation electronic configurations. Optically transparent, these oxides derive their conduction bands from the metal's ns orbital and their valence band largely from oxygen's $2\mathrm{p}^{6}$ orbital. The large radius and spherically-symmetric ns shells result in significant overlap, yielding a set of materials with high electron mobilities which are relatively insensitive to crystalline disorder. This is in contrast to materials like silicon, where electron propagation is very sensitive to crystallinity, due to their sp^{3} hybrid orbital derived valence and conduction bands [35]. Compared to binary oxides, multicomponent metal oxides largely remain amorphous, and thus atomically smooth, over a wider range of processing conditions and allow

for more control over electrical properties via changes in film stoichiometry. Discussed below are the electrical properties of the channel materials zinc tin oxide (ZTO) and its derivatives, and indium gallium zinc oxide (IGZO), in anticipation of integrated circuit applications in Chapter 4 and Chapter 5.

2.3.1 Zinc Tin Oxide

In 2005, Chiang *et al.* reported the first TFT with a ZTO channel layer [36]. A staggered bottom-gate structure is used for both ITO/ATO (aluminum titanium oxide) and Si/SiO_2 gate stacks. ZTO is sputtered onto the substrate, which is held at ∼175 °C, in a 90/10 Ar/O_2 atmosphere, and then subsequently annealed for one hour at temperatures up to 600 °C, where the channel material remains amorphous. Finally, ITO source and drain contacts are sputtered in pure argon onto the substrate, which is again held at ∼175 °C. Target stoichiometries with $ZnO:SnO_2$ ratios of 2:1 and 1:1 (Zn_2SnO_4 and $ZnSnO_3$, respectively) are synthesized from commercial and in-house suppliers. According to this study, there is little to no performance difference between the targets. Typical 600 °C annealed devices have a range of V_{ON} between -5 to 5 V, I_D on-to-off ratios between 10^7 and 10^8, and incremental field-effect mobilities (μ_{inc} or μ_{FE}) between 20 and 50 $cm^2V^{-1}s^{-1}$. TFTs annealed at 300 °C demonstrate incremental mobilities between 5 and 15 $cm^2V^{-1}s^{-1}$, although no other electrical parameters are noted. The increase in mobility from the 300 °C anneal to the 600 °C anneal is attributed to an increase in local order or a change in the semiconductor–insulator interface.

Later in 2005, Hong and Wager present ZTO channel TFTs utilizing a thermally evaporated SiO_2 passivation layer on staggered bottom-gate structured devices [37]. The ZTO channel layer is sputter-deposited from a 2 inch diameter Zn_2SnO_4 target at 50 W RF power with a 7.5 cm target-to-substrate distance in a 5 mTorr 90/10 Ar/O_2 atmosphere onto a p-type doped silicon substrate with a 100 nm thermally grown SiO_2 gate insulator. ITO source and drain contacts are subsequently sputtered in pure argon at 30 mTorr from a 3 inch diameter target and the whole stack is then furnace annealed at various temperatures using an 1 h. ramp up, 10 min. hold, and 5 h. ramp down scheme. An ∼100 nm thermally-evaporated SiO_2 passivation layer is then deposited onto the stack and annealed again at either 300 °C or 600 °C using the same ramp/hold scheme mentioned above. Unpassivated (no SiO_2 layer) 300 °C and 600 °C annealed devices exhibit incremental mobilities of ∼3 and ∼20 $cm^2V^{-1}s^{-1}$and turn-on voltages of 2 V and 1 V, respectively. The unpassivated ZTO channels are assumed to behave like that of ZnO, where chemisorbed atmospheric oxygen depletes the top surface of the channel, severely restricting upper surface conduction [38].

All devices tested using both a pre-passivation and post-passivation anneal are first annealed to 600 °C, and then measured after no intentional annealing or a post-deposition anneal of 200, 300, or 600 °C. The no intentional anneal and the 200 °C post-passivation anneal lead to an immeasurable (highly negative) V_{ON}. TFTs exhibit V_{ON}'s of -1 V and -2 V for 300 °C and 600 °C, respectively, post-passivation anneals. Incremental mobilities are reported as 20, 18, 26 and 15 $cm^2V^{-1}s^{-1}$for the 0, 200, 300, and 600 °C post-passivation annealing. Devices made using solely a post-passivation anneal of 300 °C and 600 °C result in μ_{inc} and V_{ON} values of 4 $cm^2V^{-1}s^{-1}$and 2 V and 9 $cm^2V^{-1}s^{-1}$and -2 V, respectively. Thus, the gate insulator-channel interface is not affected by the passivation, since the incremental mobility of devices with or without passivation is similar.

Jackson *et al.* demonstrate ZTO TFTs on a flexible polyimide substrate with a maximum processing temperature of 300 °C [39]. The bottom-gate structures begin with a sputter-deposited aluminum gate, followed by a 375 nm thick SiON gate dielectric grown at 300 °C via PECVD. The dielectric's capacitance density is 15 nF cm^{-2}, which indicates that the relative dielectric constant is roughly 6.35. A 50 nm thick ZTO channel layer is sputtered from a 1:1 ZnO:SnO_2 target and annealed at 250 °C for 10 minutes. Both ITO and aluminum source/drain contacts are tried, but aluminum contacts exhibit a contact resistance of roughly 30 kΩ compared to ∼1 kΩ for ITO. The subthreshold swing S is reported to be 1.65 V/decade, threshold voltage V_T is -8.8 V, V_{ON} is -17 V, μ_{inc} is 14 $cm^2V^{-1}s^{-1}$, and the I_D on-to-off ratio is 1.4 x 10^6. The low frequency transition from depletion to accumulation occurs within ∼3 V, indicating low bulk and interface trap densities. Lastly, problems with heat dissipation on insulating substrates are noted.

Hoffman presents a study on the effects of ZTO channel stoichiometry and anneal temperature on TFT electrical performance [40]. The staggered bottom-gate devices start with heavily-doped Si substrates with a 100 nm layer of thermal SiO_2 grown on top. A 50 nm thick ZTO channel is then sputter-deposited onto the SiO_2, followed by ITO/Ta/Au source/drain contacts. The entire stack is then annealed between 200 °C and 800 °C, using a ramp rate of 2 °C/min. and a dwell time of 1 h. The chosen 3 inch diameter ZTO target stoichiometries are 0, 0.33, 0.5, 0.67, and 1.0 Zn/(Zn + Sn), and the deposited channel layer stoichiometries closely match their respective targets. Channel sputter deposition occurs in a 90/10 Ar/O_2, 5 mTorr atmosphere, and a RF power of 100 W. Devices with a pure SnO_2 channel (Zn/(Zn + Sn) = 0) do not turn off within the -30 to 30 V V_{GS} sweep, but show peak incremental mobilities after a 500 °C anneal. All channel stoichiometries exhibit a decreasing V_{ON} trend with increased temperature except the 0.33 Zn/(Zn + Sn) devices, which are immeasurably negative at 500 °C, but then increase to -15 V and ∼0 V at 600 °C and 800 °C, respectively. Peak incremental mobilities for the 0.33, 0.5, and

0.67 ratios increase rapidly with anneal temperature and reach their maximum mobility (∼25-30 $cm^2V^{-1}s^{-1}$) roughly between 400 °C and 600 °C, whereas the mobility of pure ZnO increases monotonically through 800 °C, where it peaks at ∼13 $cm^2V^{-1}s^{-1}$. Devices using a 0.33 Zn/(Zn + Sn) channel exhibit a "kink" in their 600 °C I_D-V_{GS} sweeps, which is associated with positive interface traps [29].

With an eye towards an entirely transparent display, Görrn *et al.* report a ZTO TFT directly driving an organic-LED (OLED) [41]. The gate structure of the staggered bottom-gate transistor is a glass substrate with an ITO gate electrode covered by an ATO insulator. The ZTO channel is then deposited via plasma-assisted pulsed laser deposition (PA-PLD) from a 1:1 ZnO:SnO_2 target onto a 150 °C heated substrate in an oxygen ambient. No intentional annealing occurs thereafter. The virgin devices exhibit a V_{ON} of -1 V, a V_T of -0.5 V, a saturation mobility of 11 $cm^2V^{-1}s^{-1}$, and an I_D on-to-off ratio of 10^4. The OLED structure is then built on top of the drain contact, and emits ∼700 cd/m^2 with a V_{DS} of 20-25 V and a V_{GS} of 5 V.

Leveraging one of the benefits of ZTO-based channel TFTs, Hong *et al.* demonstrate devices synthesized from a 2 inch diameter metallic 1:1 Zn:Sn target [42]. The gate electrode is the same as his previous study: a p-type silicon wafer with a 100 nm layer of thermal SiO_2 grown on top. The 50 nm thick channel is rf magnetron sputter deposited at 50 W in a 30 mTorr atmosphere using a flow of 20 sccm of argon and varying amounts of oxygen. Devices are then annealed to either 300 °C or 500 °C, and afterwards aluminum source/drain contacts are thermally evaporated to complete the devices. For the 300 °C and 500 °C anneals, S is ∼500 mV/decade, $I_D^{ON-OFF} = 10^7$, V_{ON} values are 2 V and -2 V, incremental mobilities are 11 and 32 $cm^2V^{-1}s^{-1}$, and μ_{avg} are 6 and 25 $cm^2V^{-1}s^{-1}$, respectively. Using a 5 mTorr deposition pressure instead of 30 mTorr, peak mobility occurs at a P_{O_2} of 0.8 mTorr, which correlates to a gas flow of 20/3.8 sccm of Ar/O_2. Devices synthesized via DC magnetron sputtering at 30 mTorr and annealed at 300 °C and 500 °C exhibit S of 600 mV/decade, I_D on-to-off ratios of $>10^7$, a $V_{ON} \approx 0$ V, and respective μ_{inc} values of 8 and 31 $cm^2V^{-1}s^{-1}$.

Chang *et al.* report ZTO TFTs spin-coated from a acetonitrile dissolved 0.015 M $SnCl_2$ and 0.015 M $ZnCl_2$ solution [43]. The 55 nm thick ZTO film is annealed at 600 °C for one hour and has a Zn:Sn ratio of 1.08 and 1.56 at the surface and 40 nm from the top, respectively. Devices exhibit a V_{ON} of 2 V, an I_D on-to-off ratio of 10^5, and a (μ_{FE}) of 16 $cm^2V^{-1}s^{-1}$. While W/L is rated as 7, the ratio is highly suspect due to major fringing current from the unpatterned channel layer, which overestimates μ_{FE}.

In 2007, Görrn *et al.* present two papers: one examines the effects of long-term bias stress [44] and the other covers the effects of visible light on transistor performance [45]. Devices are

synthesized using the same process as described above in Görrn's previous work [41], except the substrate temperature is varied between 250 °C and 450 °C and the ZnO:SnO_2 ratio is varied between 1:2 and 2:1. Long-term testing is applied for 6 x 10^4 s, interrupted every 100 s to measure the I_D-V_{GS} transfer curve. While minimal change in mobility is measured over the duration of the test, V_T moves significantly. Devices with Zn cation percentages between 38% and 65% exhibit a negative ΔV_T, whereas devices outside this region show a positive ΔV_T over the length of the sweep. The most stable transistors are those deposited while the substrate is held at 450 °C, with ΔV_T values between 0 V and +0.5 V. Devices with a negative ΔV_T exhibit a non-rigid shift in their transfer curve over the course of the bias stress, showing a significant decrease in subthreshold swing, while maintaining nearly identical current drive at higher V_{GS} values. Transistors with a positive ΔV_T show a rigid shift over the duration of the test.

Devices tested optically are stimulated with 628, 525, 470, and 425 nm wavelength LEDs, and exhibit a recovery lifetime (τ_{REC}) of roughly 20 h. Sensitivity for all devices is highest in the blue region, which always shows a negative V_T shift, but the sensitivity decreases significantly with increased substrate temperature during deposition. Films deposited at 250 °C and 350 °C with higher zinc content (∼66%) are less sensitive to blue light than films with lower zinc content (∼33%), but sensitivity at longer wavelengths is composition independent. Substrates deposited at 450 °C show no Zn concentration dependance under optical stimulus. At a constant 470 nm stimulus, the 450 °C devices have a non-rigid shift in their I_D-V_{GS} transfer curve and a dramatic increase in $I_{D,OFF}$ with increasing illumination intensity. This effect, however, saturates at around 1 mW/cm^2. Likewise, at a constant optical intensity of 1 mW/cm^2, the 450 °C devices show no response to 628 nm illumination, but a ΔV_T of -2 V for both 525 nm and 470 nm light, and a strong, non-rigid shift with 425 nm light results in a $\Delta V_T < -6$ V . Higher temperature devices are more optically stable due to their lower bulk defect density which in turn decreases optical carrier generation.

2.3.2 Zinc Tin Oxide Derivatives

Unlike both gallium and indium, the raw material cost of zinc and tin is inexpensive and readily available. Therefore, researchers are motivated to realize some of the benefits of gallium oxide (stabilizes oxygen defects) and indium oxide (large 5s shell yields high mobilities at low temperatures), without the full cost of these materials by alloying these oxides with ZTO. Both Grover *et al.* [46] and Saji *et al.* [47] investigate zinc indium tin oxide (ZITO) as a route to low temperature devices, and Ogo *et al.* [48] study tin gallium zinc oxide (SGZO) as a low-cost analog to IGZO.

Using a 2 inch diameter sputter target with a composition of 5:20:75 ZnO:In_2O_3:SnO_2, Grover *et al.* examine the temperature effects of a post-channel anneal on electrical properties. P-type silicon coupons with a 100 nm layer of SiO_2 serve as both the substrate and the gate electrode for the TFTs. The 60-80 nm thick ZITO layer is deposited at 100 W in a 90/10 Ar/O_2, 5 mTorr atmosphere where the substrate is held ∼100 °C. Channel anneals vary between 100 °C and 300 °C, which is followed a thermally evaporated aluminum layer to define the staggered source and drain contacts. The ZITO layer itself remains amorphous until 600 °C. Transistors annealed at 200 °C operate in depletion mode, since V_{ON} is -11 V; μ_{inc} and μ_{avg} are 15 and 6 $cm^2V^{-1}s^{-1}$, respectively, and the I_D on-to-off ratio is 10^7. Incremental mobility monotonically increases from 5 to 20 $cm^2V^{-1}s^{-1}$and V_{ON} changes from -4 V to -17 V as anneals increase from 100 °C to 300 °C.

Saji *et al.* cosputter a ZnO target and an $In_2Sn_2O_7$ target to examine the effects of ZnO concentration on transistor performance. The 45 nm thick ZITO channel is deposited on top of silicon substrates with a 100 nm layer of thermally grown SiO_2. Operating in a 1 Pa (7.5 mTorr) pure argon atmosphere, the ITO target is DC sputtered at 125 W, while the ZnO target is RF sputtered between 25 W and 200 W. During deposition, the substrates are placed 4 cm away from the target faces on a 50 RPM rotating holder. Finally, the source and drain contacts are made using a Ti/Au metal stack. Annealing the channel film at 300 °C for 1 h. reduces the carrier concentration two orders of magnitude from $\sim 10^{20}$ cm^{-3} to $\sim 10^{18}$ cm^{-3}, with a small decrease in Hall mobility. Devices annealed after source/drain deposition are significantly worse (i.e., show kinks and other nonidealities) than transistors annealed immediately after channel deposition. Field-effect mobility decreases with increasing ZnO percentage, varying from 12.4 to 3.4 $cm^2V^{-1}s^{-1}$as ZnO concentration changes from 5 to 48%. Threshold voltage increases and S decreases with ZnO content. The latter two effects are attributed to a decrease in interface trap density.

Ogo *et al.* use PLD to compare tin gallium zinc oxide (SGZO) with IGZO to determine if a tin cation can be used as an inexpensive substitute for the indium cation. A 1:1:1 cation ratio target is used in a 2 Pa oxygen atmosphere to deposit a 50 nm thick channel layer onto a silicon substrate with a 150 nm layer of SiO_2, which doubles as the gate electrode. After annealing, a 20/40 nm Al/Au metal stack is deposited to make the source and drain contacts. Phase segregation is noted in the films after a 700 °C anneal, and subgap states decrease markedly with increasing anneal temperature. Transistors tested without an anneal show barely any field-effect, whereas devices with a 300 °C anneal exhibit I_D on-to-off ratio of 10^3 and a V_T of 2.5 V. Transistors annealed at

400 °C have a I_D on-to-off ratio of 10^6, a V_T of ~5.5 V, a S of 500 mV/decade, and a μ_{SAT} of 2 $cm^2V^{-1}s^{-1}$.

2.3.3 Indium Gallium Zinc Oxide

In a letter to *Nature* in 2004 [35] and again in the *Japanese Journal of Applied Physics* in 2006 [49], Nomura *et al.* present IGZO-channel TFTs synthesized entirely via PLD on a flexible PET substrate. The coplanar top-gate transistors use ITO for the gate electrode, a 140 nm thick Y_2O_3 gate insulator with an ε_R of 16, and a 30 nm thick IGZO channel layer. ITO is also used for source/drain contacts and no intentional annealing is applied to the device stack. The TFTs have the have the following electrical characteristics: $\mu_{SAT} = 8.3$ $cm^2V^{-1}s^{-1}$, $\mu_{FE} = 5.6$ $cm^2V^{-1}s^{-1}$, $I_D^{ON-OFF} = 10^3$, and $V_T = 1.6$ V. The electrical properties degrade only slightly when the substrate is bent at a radius of 30 mm.

Measured channel stoichiometry from the $InGaZnO_4$ target is 1.1:1.1:0.9 In:Ga:Zn, and the material remains stable up through a 500 °C anneal. Film conductivity is modulated via oxygen pressure during deposition, yielding a conductivity of $< 10^{-5}$ S/cm for a $P_{O_2} > 6$ Pa (45 mTorr). Carrier concentration decreases from 10^{20} cm^{-3} to $< 10^{14}$ cm^{-3} with a P_{O_2} range of 0.1 Pa to 7 Pa (0.75 to 52.5 mTorr), respectively. Mobility markedly increases ($\mu_{HALL} > 10$ $cm^2V^{-1}s^{-1}$) with carrier concentrations greater than 10^{18} cm^{-3}. A target using Al_2O_3 instead of Ga_2O_3 is used in [49], where the Al_2O_3 is shown to stabilize V_{ON} as effectively as Ga_2O_3, but at a greater loss in Hall mobility.

Motivated by the commercial viability of sputtering compared to PLD, Yabuta *et al.* demonstrate sputter-deposited TFTs using the same device stack that Nomura *et al.* demonstrated previouslly [50]. Instead of ITO gate and source/drain electrodes, e-beam deposited stacks of Ti/Au (5/40 nm) are used. The 50 nm thick IGZO layer is deposited on glass from a 4 inch diameter $InGaZnO_4$ target at 300 W in 530 mPa (4 mTorr) 95/5 Ar/O_2 atmosphere. Substrate temperature rises 40 °C during the 5 min. deposition, and the deposited film stoichiometry is 1:0.9:0.6 In:Ga:Zn. The Y_2O_3 insulator is sputtered at 500 W in a 0.67 Pa (5 mTorr) 40/60 Ar/O_2 atmosphere for 50 minutes, heating the substrate 140 °C over the course of the run. The resulting layer is 140 nm thick and has a ε_R of 14. No intentional annealing is applied to the stack and the electrical conductivity decreases monotonically on a log scale with P_{O_2}. Transistors with channels sputtered at $P_{O_2} < 17$ mPa (<0.128 mTorr) yield I_D^{ON-OFF} ratios of $\geq 10^4$. A channel deposited at $P_{O_2} = 18$ mPa (0.135 mTorr) results in a TFT with a I_D on-to-off ratios of 10^8, S of 200 mV/decade, μ_{FE} of around 12 $cm^2V^{-1}s^{-1}$, and a V_T equal to 1.4 V.

Kang *et al.* report the effects of atmospheric conditions on IGZO-channel (GIZO in the paper) TFTs [51]. The staggered bottom-gate structure uses a 200 nm thick Mo gate electrode, followed by a 200 nm thick SiN_X dielectric deposited at 250 °C via PECVD. The 90 nm IGZO channels are RF sputtered at 200 W in a 7 mTorr, 98/2 Ar/O_2 atmosphere, and Ti/Pt bilayer source/drain electrodes are deposited before the entire stack is annealed at 350 °C in nitrogen for one hour. Transistors measured at room temperature in air have a V_{ON} of -7 V, S = 200 mV/decade, and a μ_{inc} of around 10 $cm^2V^{-1}s^{-1}$. The samples are then measured at pressures ranging from 760 Torr to 8.5 x 10^{-6} Torr, where V_{ON} shifts from -7 V to -54 V. The effect is attributed to oxygen adsorption where, like ZnO, the oxygen chemisorbs and thus depletes carriers from the exposed channel surface, removing a major conduction pathway [38]. Results extrapolated to a 150 Torr oxygen atmosphere, an equivalent P_{O_2} to ambient air, yield a -3 V difference in V_{ON}, where the discrepancy is attributed to adsorbed water.

Iwasaki *et al.* examine the effect of channel stoichiometry on IGZO channel-based TFTs by cosputtering separate 2 inch diameter In_2O_3, Ga_2O_3, and ZnO targets [52]. The 3 inch diameter silicon wafer with a 100 nm thermal SiO_2 layer serves as both the substrate and gate electrode. The RF power for each target is varied from 30 W to 60 W, and the maximum temperature of the stack is 120 °C during photoresist baking. The total pressure is 360-380 mPa (2.70-2.85 mTorr) during deposition, where a P_{O_2} is set to both 1.3 mPa and 2.6 mPa (0.00975 and 0.01950 mTorr) with an argon balance. Films remain amorphous over the 20-60 atomic % range measured on the wafer, and chemical variation over the channel dimensions are estimated as less than 0.2 %. Films rich in Ga_2O_3 exhibit a poor field-effect response due to their low μ_{SAT} values, and mobility rises with increasing ZnO concentration at a constant In_2O_3 percentage. In_2O_3-rich devices have high mobilities and carrier concentrations but are too conductive to be effectively turned off. ZnO-rich films yield small subthreshold swings, which is attributed to a change in shallow subgap states in the bulk and/or to a decrease in insulator–channel interface states. A constant In:Ga ratio yields a constant V_T line when deposited at 2.6 mPa P_{O_2}, but not at 1.3 mPa P_{O_2}, suggesting that Ga_2O_3 effectively compensates In_2O_3-derived carriers by reducing oxygen vacancies in the film, given sufficient oxygen is available during deposition. The best performing device has an In:Ga:Zn ratio of 37:13:50, resulting in a μ_{SAT} of 12 $cm^2V^{-1}s^{-1}$, V_T of 3 V, and an I_D on-to-off ratio of 7 x 10^7.

Kumomi *et al.* compare the results presented by Yabuta [50] and Iwasaki [52] with three additional staggered bottom-gate IGZO-based TFT structures [53]. The first novel structure uses a PET substrate with a 25 nm layer of ITO as the gate electrode. On this a 150 nm Y_2O_3 film is sputtered, followed by a 60 nm IGZO layer, and then Ti/Au (5/40 nm) source/drain contacts. No

intentional annealing is used in the fabrication of the three structures. The PET substrate devices have a V_T of 1.4 V, μ_{SAT} = 3.9 $cm^2V^{-1}s^{-1}$, I_D^{ON-OFF} of 1.7 x 10^7, and a S of 200 mV/decade. The inferior results compared to Yabuta [50] are attributed to the much rougher Y_2O_3 dielectric layer on PET than on glass.

The second structure uses an silicon wafer with a 100 nm thermally grown SiO_2 layer as a gate stack. The 50 nm IGZO and Ti/Au (5/40 nm) layers are deposited as above. TFTs synthesized on silicon wafers exhibit a V_T of 3.7 V, a μ_{SAT} of 13.4 /mobility, $I_D^{ON-OFF} = 10^{10}$, and a S of 470 mV/decade.

The third structure starts with a glass substrate onto which a Ti/Au/Ti (5/40/5 nm) gate metal stack and a RF sputtered 100 nm thick SiO_2 layer are deposited. On top of the gate insulator the IGZO and Ti/Au films are deposited as above. IGZO is sputtered at 300 W in a 530 mPa (4 mTorr) atmosphere with a P_{O_2} of 19.7 mPa (∼0.15 mTorr) from a 4 inch diameter target. A 40/60 Ar/O_2, 670 mPa (5 mTorr) atmosphere is used to sputter the Y_2O_3 target at 500 W of RF power. Devices made on this $Ti/Au/Ti/SiO_2$ gate stack have a V_T of 1.7 V, μ_{SAT} = 4.8 $cm^2V^{-1}s^{-1}$, $I_D^{ON-OFF} = 10^9$, and the S is 390 mV/decade.

Kim *et al.* present a staggered bottom-gate IGZO TFT with a PECVD SiO_X etch stop/passivation layer [54]. On glass, a 200 nm MoW gate electrode is deposited and patterned, followed by a 200 nm thick, 330 °C PECVD SiN_X film. An $In_2Ga_2ZnO_7$ (2:2:1) target is sputtered at 450 W in a 65/35 Ar/O_2 ambient, yielding a film stoichiometry of 2.2:2.2:1 In:Ga:Zn. The SiO_X film is deposited via PECVD and dry etch patterned in a Ar/CHF_3 feedstock. Lastly the MoW source/drain contacts are sputtered and dry etched in a SF_6/O_2 gas combination. The entire stack is then annealed at 350 °C for 1 hour. Transistors without the SiO_X etch stop layer show significantly worse performance (μ_{FE} = 5 $cm^2V^{-1}s^{-1}$, S = 3.5 V/decade) than those with the etch stop layer (μ_{FE} = 35.8 $cm^2V^{-1}s^{-1}$, S = 0.59 V/decade). The etch stop devices also report a V_T of 5.9 V and a I_D^{ON-OFF} of 4.9x10^6. The μ_{FE} of the passivated transistors changes from 35.8 to 14.8 $cm^2V^{-1}s^{-1}$as the channel length decreases from 50 μm to 10 μm, at a constant 10 μm channel width. The effect is associated with high contact resistance (R_{SD}), as it becomes a larger percentage of lumped on-channel resistance ($R_{CH,ON}$) as channel length decreases. $R_{SD}W$ is estimated as 101 Ω-cm, and ρ_{CH} is approximately 1.7 x 10^{-2} Ω-cm. A high measured carrier concentration of 3.7 x 10^{19} cm^{-3} is a result of hydrogen incorporation from the SiN_X layer.

Chiang *et al.* examine the effects of sputtering conditions and anneal temperatures on device performance and long-term stability [55]. The substrate, which doubles as the gate electrode, is p-type silicon with a 100 nm thermal SiO_2 gate insulator; a staggered bottom-gate structure is used. A 3 inch diameter $InGaZnO_4$ target is sputtered at target-to-substrate distance of 10 cm

in an argon balanced 5 mTorr atmosphere with a varying P_{O_2} of 0.5, 0.25, and 0 mTorr, and at varying RF powers (75, 100, and 125 W). After channel deposition, the substrates are annealed between 200 °C and 800 °C for one hour. The source/drain contacts are either a 200 nm thick ITO (90:10) or ZIO ($ZnIn_4O_7$) films. Devices annealed at 175 °C result in the following electrical characteristics: $V_{ON} \approx 0$ V, S = 600 mV/decade, $I_D^{ON-OFF} = 10^7$, $\mu_{inc} = 17$ $cm^2V^{-1}s^{-1}$, and $\mu_{avg} = 14$ $cm^2V^{-1}s^{-1}$. Non-annealed TFTs do not show significant field-effect, and are thus not reported.

Incremental mobility increases at lower anneal temperatures (< 500 °C), decreasing P_{O_2}, and increasing RF power. An increase in anneal temperature results in higher μ_{inc} values until 500 °C, where it peaks. V_{ON} is roughly inversely related to μ_{inc} at lower anneal temperatures; it decreases in value as P_{O_2} decreases and RF power increases. Lower P_{O_2} values result in higher carrier concentrations, raising the Fermi level above the trap level, whereas higher powers nominally increases the kinetic energy of impinging ions and neutrals onto the substrate, allowing for more adatom mobility, and thus higher local order. Improvements due to increased anneal temperature are associated with increased local order and a reduction in interface states, until IGZO crystallization and phase segregation become significant at 600 °C and beyond. Transistor μ_{inc} and V_{ON} values converge at an anneal temperature of 500 °C regardless of the sputter conditions, indicating that the anneal is the dominant process at 500 °C and above.

Various channel layer thicknesses (10-150 nm) are tested for shelf-life stability and other effects. Devices synthesized with a 10 nm channel exhibit a $V_{ON} \approx 0$ with a 325 °C anneal, but are highly positive when annealed at 175 °C in either nitrogen or ambient air. Thicker transistors do not share the same phenomena. Devices with channel thicknesses of 10, 25, and 50 nm are annealed at 175 °C and tested every week for 18 weeks. The 10 nm thick TFTs exhibit a significant (> 3 V) and variable shift in V_{ON} as compared to their initial test, whereas the 25 nm thick devices exhibit a relatively constant V_{ON} shift of 2 V. At a channel thickness of 50 nm, the devices remain shifted at a constant 0.5 V from their initial measurement, indicating nearly perfect shelf life.

IGZO TFTs using a channel deposited at 125 W in a 5 mTorr Ar/O_2 atmosphere with an anneal of 300 °C are tested using a constant bias stress test ($V_{GS} = V_{DS} = 30$ V) for 1000 minutes. Initial V_{ON} values are varied by sweeping P_{O_2} from 0 to 0.20 mTorr in 0.05 mTorr increments during channel deposition. Devices exhibit greater stability as their initial V_{ON} values converge to 0 V. TFTs sputtered in pure argon ($V_{ON,INIT} = 0$ V) show no degradation in current over the entire length of the bias stress test, whereas the normalized I_D of the other devices follows an exponential decay with time.

Lim *et al.* present staggered bottom-gate IGZO channel TFTs with a maximum processing temperature of ∼70 °C [56]. RF sputter power to a 3 inch diameter $InGaZnO_4$ target in a 10 mTorr argon ambient is varied from 75 W to 300 W to create ∼50 nm thick IGZO films, which are then measured for resistivity. Films sputtered below 150 W exhibit high resistivity, > 100 Ω-cm, whereas films deposited at 150 W or above are ≤ 1 Ω-cm.

Transistors are made on a glass substrate: a 150 nm film of IZO is sputtered for the gate metal followed by a 90 nm thick PECVD SiN_X deposited at 70 °C. The 50 nm thick IGZO layer is sputtered at 140 W in a 10 mTorr argon ambient. During deposition, the substrate rises to roughly 40 °C and the resulting film has a resistivity of ~ 1 Ω-cm and a carrier concentration around $6.5\text{x}10^{17}$ cm^{-3}. On top of the channel, ZIO is deposited to define the source and drain contacts with a W/L of 100/6. The rated V_T is 2.1 V, $\mu_{SAT} = 17$ $cm^2V^{-1}s^{-1}$, S = 500 mV/decade, and I_D^{ON-OFF} is 10^5. Devices with thicker channels have higher off currents, and thus lower I_D on-to-off ratios. Like Kim *et al.* [54], a range of channel lengths are tried at a constant channel width, yielding a similar result to above, where mobility appears to decrease at higher W/L ratios due to the relative increase in source/drain contact resistance compared true channel resistance. Finally, devices with a W/L of 100/6 are tested at a V_{GS} of 6 V and an unknown V_{DS} for 500 hours with little change in both μ_{SAT} and V_T.

2.4 Conclusion

This chapter summarizes prior literature related to both AOS etching and AOS channel materials. Etching properties of ITO and ZnO over a wide gamut of etch gas feedstocks are compiled and common trends are extrapolated. A basic explanation of TFT operation and device structures is provided. Both ZTO and IGZO are carefully examined as channel materials in anticipation of ZTO circuit integration development, which is the primary focus of this thesis. The following chapter discusses the basics of plasma processing, along with other semiconductor processing techniques and experimental methods used to accomplish this thesis research.

3. EXPERIMENTAL TECHNIQUES

This chapter provides an overview of the experimental methods and equipment necessary to fabricate and electrically characterize TFTs and TFT-based circuits. The basics of plasma processing are introduced in light of their importance in the deposition and etching of thin-films within the device stack. TFT-based circuit fabrication techniques, such as annealing, evaporation, sputtering, plasma-enhanced chemical vapor deposition, and photolithography are briefly introduced. The extrapolation of the electrical parameters from DC I-V curves, e.g., threshold voltage, output conductance, transconductance and channel mobility, are then discussed.

3.1 Plasma Processing Basics

In discussing plasma processing, it is best to first introduce some theory in order to give proper basis for understanding specific challenges related to the development of AOS materials. To begin, a plasma is an electrically neutral amalgamation of charged particles moving independently in all directions. Given the neutrality of the plasma, positively charged ion density is approximately equal to the electron density, i.e., $n_i \approx n_e$. Plasmas of interest within the context of this thesis are cold and weakly ionized, which means that they are electrically driven, have boundaries with significant surface losses, do not maintain a thermal equilibrium between electrons and ions, are nominally electrically neutral in the bulk, and are derived largely from electron–neutral collisions [57]. Ultimately, the ions and reactive neutrals generated in these electron-neutral collisions are the species that impinge and etch the surface of interest through chemical reaction, sputtering or both.

Plasma theory is overviewed by briefly summarizing general traits of cold, weakly ionized plasmas and by reviewing the kinetics of electrons and gases, sheath characteristics, RF plasmas, and high-density plasma sources. Treatment of these topics will help to elucidate the etching mechanisms which occur at the surface of AOS materials along with insight into sputter and plasma-enhanced chemical vapor deposition (PECVD).

3.1.1 General Semiconductor Plasma Characteristics

Figure 3.1 shows a cross-sectional schematic of a planar RF diode plasma system. The top platen and the entire periphery of the chamber is typically grounded, leaving only the bottom platen biased to a negative potential. The specific configuration of Fig. 3.1 has dielectric walls, where only the passive electrode is grounded. The highest electric field is established in the plasma sheath surrounding the driven electrode, with a much smaller sheath surrounding the passive electrode and

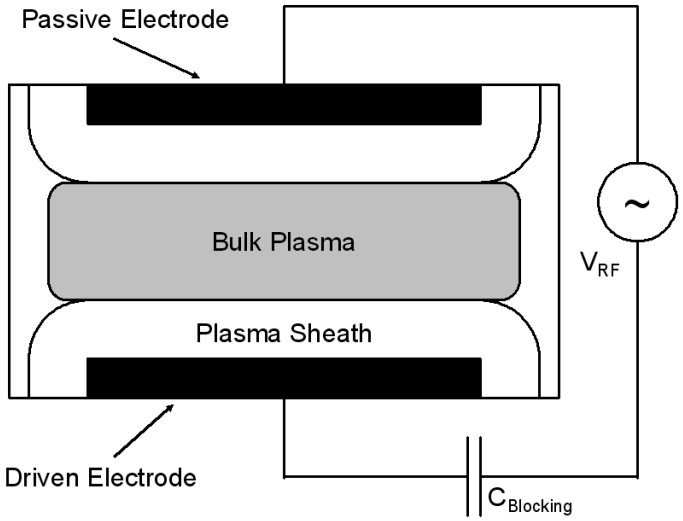


Figure 3.1: The RF planar diode uses capacitive coupling to energize the sheath regions in which electrons are accelerated to sufficiently high energies to ionize neutral species in the bulk, thereby sustaining the bulk plasma. The driven electrode is coupled to a RF generator through a blocking capacitor, which allows the electrode to naturally float up to the DC potential, which equalizes ion and electron fluxes to the electrode surface. The upper, passive electrode is typically grounded and designed as a showerhead, thus allowing the process gases to evenly diffuse into the chamber. A DC planar diode plasma system is very similar in configuration, realized by removing the blocking capacitor and using a DC power supply instead of a RF supply. The sheath surrounding the driven electrode in a DC system is significantly larger than the passive electrode, whereas in a symmetric RF system, as shown here, the passive and driven sheaths have identical areas. However, many systems tie the chamber and the upper electrode to ground, thereby intentionally imbalancing the sheath areas [57, 58, 59].

leaving the bulk essentially free of fields. Ionization and dissociation energies are quite high, and few electrons have sufficient kinetic energy to transfer in collisions, even in plasma systems designed to generate high electron temperatures. Therefore, few neutral species experience ionization. An average primary electron must have ∼200 eV of energy even though argon's first ionization energy is 15.76 eV, due to the high number of inelastic collisions before a successful ionization collision [59]. Therefore, a small percentage ($\frac{n_i}{n_g} \approx 10^{-4}$) of the gas species ionize and create a current pathway through the plasma in a planar diode configuration [58]. High density plasmas, discussed later, generate much higher ion densities. Unlike thermal plasmas, where interatomic collisions ionize gas species and distribute the kinetic energy evenly, free electrons in weakly ionized plasmas are liberated during impact ionization, whether from an electron's collision with a wall or a neutral gas particle.

Typical pressure ranges for semiconductor plasma processes are between 0.5 mTorr and 1 Torr [57, 58]. The mean free path, a measure of the average distance a gas specie travels before colliding with another, is inversely proportional to the gas density. For argon at 300 K and 1 mTorr, the mean free path is ∼8 cm [58]. Lower pressures and thinner sheaths increase anisotropy due

to reductions in ion scattering during ion acceleration through the sheath [57]. Scattered ions are much more likely to approach the substrate from non-normal angles. The low end of the processing pressure range approaches the molecular flow regime, where ions and neutrals are more likely to strike the walls of the chamber than strike another gas particle. A more careful examination of electron and gas kinetics follows.

3.1.2 Electron and Gas Kinetics

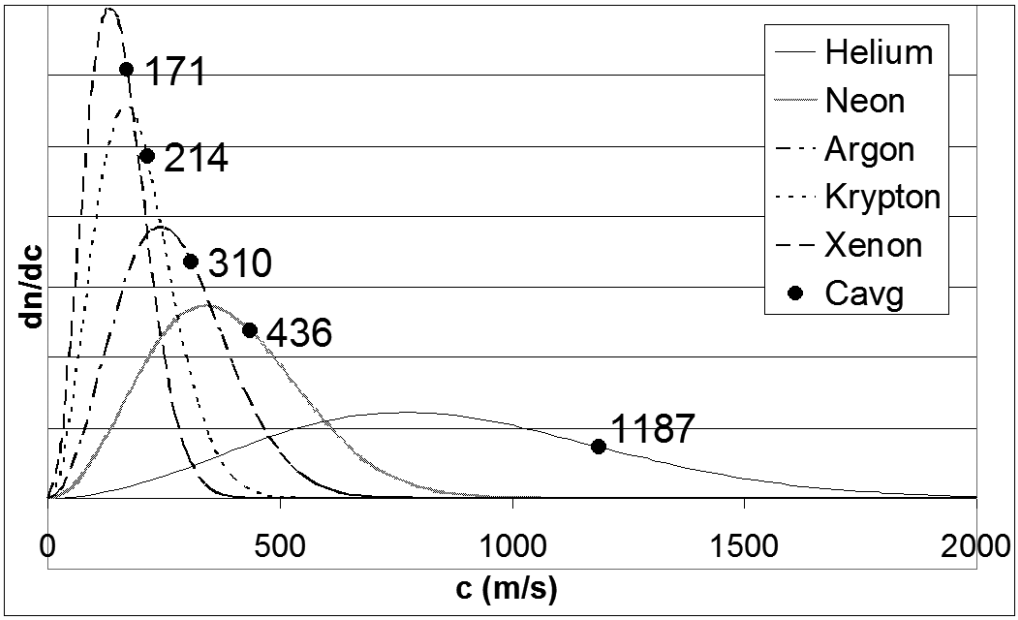


Figure 3.2: For a Maxwell-Boltzmann distribution, the velocity profile is strongly dependent on particle mass; heavier particles have a narrower peak that is centered at a lower energy. C_{avg} gives the average velocity (m/s) for each noble gas at 300 K. Neutrals and ions in the bulk of the glow discharge maintain thermal equilibrium, and thus follow this distribution. Electrons in the bulk, even in the absence of thermal equilibrium, also follow the Maxwell-Boltzmann distribution closely, greatly simplifying calculations related to their kinetics [57, 58, 60, 61].

In a simplified model of a weakly ionized plasma, ions and neutrals are assumed to be describable according to the kinetic theory of gas in thermal equilibrium, thus reducing their energy distributions to a Maxwellian distribution. Figure 3.2 shows the Maxwell-Boltzmann distribution for the noble gases at 300 K, where it is noticed that the majority of the distribution occurs near the peak, decreasing to 0 at both $c = 0$ and $c = \infty$ m/s [58]. This distribution is asymmetric with an extended tail at higher velocities. Lower mass particles have a flatter Maxwell-Boltzmann distribution with a higher average velocity than do heavier particles, all else being equal. Electrons can be defined as a gas within the bulk of the glow discharge as well, and have a velocity distribution close to ideal except in the high velocity tail. Ultimately, three Maxwell-Boltzmann distributions can be separated: neutrals, ions, and electrons, in order of increasing average energy. Less focus is

paid to neutrals and ions, due to their much lower temperatures, roughly room temperature, 300 K and 500 K, respectively [58].

To first order, an electron-gas description makes sense, but given that electrical stimulus drives these plasmas, electrons are not in true thermal equilibrium within a system, which is the basis of the Maxwell-Boltzmann distribution. In fact, fast electrons receive the greatest portion of the energy input from the electric field, since, $work = \overrightarrow{F} \cdot \overrightarrow{d} = -q\overrightarrow{\varepsilon} \cdot \overrightarrow{d}$. Fast electrons travel a greater distance, $\overrightarrow{d}$, along the field, $\overrightarrow{\varepsilon}$, before a scattering event occurs. Thus, the electric field does more work on these high energy electrons. These fast electrons then distribute their energy via collision events with walls, neutrals, ions, and other electrons. However, given that electron-neutral inelastic collisions are the primary mechanism to create ions and or reactive neutrals, and thus maintain glow discharge, a decrease in electron density at energies greater than the gas feedstock's ionization and/or dissociation energy is expected. Ultimately, in the context of this thesis, interest in electrons within the plasma is limited to their collisions with neutrals to create ions and reactive neutrals.

Other energetic phenomena associated with neutrals are excited and metastable species, photoionization, recombination and relaxation. Not all electron-neutral collisions transfer sufficient energy to ionize a species, but may excite an electron to a higher energy level. For example, argon has two metastable states at 11.5 and 11.7 eV; these metastable states require significantly less energy to ionize than does a completely neutral argon atom, whose first ionization energy is 15.76 eV [58, 60]. Inevitably, many of these excited species relax, lowering their electronic configuration to their ground state and releasing a photon to conserve energy. The emission spectrum of the plasma can be measured to identify specific spectral lines of the gas species present, employing a technique called optical emission spectroscopy (OES). Some photons with energies greater than the ionization energy are emitted in electron-neutral collisions when an inner electron is liberated and the subsequent relaxation releases a high-energy photon. While many of these high-energy photons are absorbed by the walls, a significant percentage impinge on neutrals in the glow discharge and thus induce ionization [58]. Electrons released via photoionization typically absorb the excess photon energy as well, exiting the atom with significant kinetic energy.

Beyond inelastic electron-neutral collisions, other mechanisms serve to thermalize the electron temperature as well. Fast electrons create a significant number of secondary electrons in collisions which, in general, leave an atom with 2-8 eV of kinetic energy [62]. Subsequent scattering of primary and secondary electrons in the bulk of the glow discharge ultimately cause electrons to reach a modicum of thermal equilibrium, yielding an experimentally confirmed near Maxwell-Boltzmann distribution [58]. Knowing the distribution makes it easier to qualify and quantify the

ionization and dissociation of gas species due to electron-neutral collisions in the bulk and gives insight into electron behavior in the bulk of the glow discharge. The existence of a near-equilibrium distribution also serves to reinforce the quasistatic nature of the glow discharge, given the time required to establish thermal equilibrium. The boundary between the plasma and the walls, the plasma sheath, does not follow such a distribution, however.

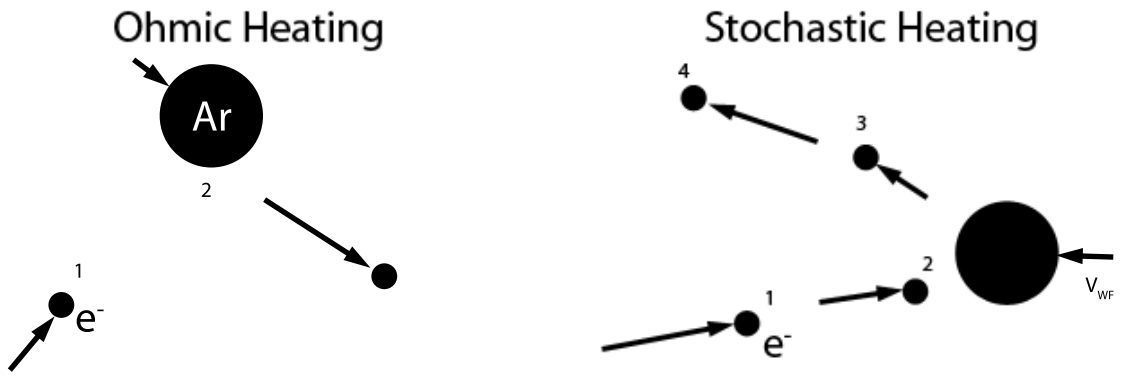


Figure 3.3: In ohmic heating, an incident electron (1) elastically collides with a gas (2), an argon atom in this example, and due to conservation of momentum, is reflected with a significant increase in kinetic energy. Ohmic heating is due to dramatic differences in mass between gas particles and electrons, where a small momentum impulse from a collision positively affects the electron's kinetic energy. In the example of stochastic heating, (1) an incident electron is initially drawn to the right due to the electric field at $\overrightarrow{V}_{inc}$, (2) experiences the polarity change in the sheath, (3) effectively collides with the incident edge of sheath wavefront, which is moving at $\overrightarrow{V}_{WF}$, and (4) is finally accelerated away from the sheath wavefront at twice the wavefront velocity, $\overrightarrow{V}_F = \overrightarrow{V}_{inc} + 2\overrightarrow{V}_{WF}$ [57, 58].

Figure 3.3 shows ohmic and stochastic heating processes, two significant electron heating processes which occur at the edge of the plasma sheath. In ohmic heating, neutrals serve to raise the bulk electron temperature through electron-neutral elastic collisions, where electrons are reflected back into the bulk at higher than their initial velocities. This process can be the dominant heating mechanism at higher pressures, where the electron mean free path, λ_e, is less than the discharge length [57]. In radio frequency and microwave plasmas, another source of heating exists from the oscillating edge of the sheath, which causes electrons to "bounce" off the incident sheath wavefront into the bulk at their incident velocity plus twice the wavefront velocity [57, 58]. Further discussion regarding sheath characteristics follows in the next section.

3.1.3 Plasma Sheath Characteristics

An electric field must be established at the boundaries of the plasma in order to reconcile differences in mobilities between positive ions, negative ions and electrons, thus ensuring that charge is conserved at a neutral boundary [57]. While positive ion densities are much higher due

to impact ionization, highly electronegative elements are often found as negative ions within the plasma, which may dramatically affect the plasma behavior. Since electrons achieve much higher velocities than ions, thus impinging at boundaries at a much higher rate, the bulk of the plasma maintains a positive bias compared to the boundary. In other words, even in a neutral plasma, the sheath region must be electron-poor to balance ion and electron fluxes to the walls. Ions entering the sheath accelerate towards the wall, while electrons are repelled; only electrons with sufficient energy and direction strike the wall, whereas the rest are scattered.

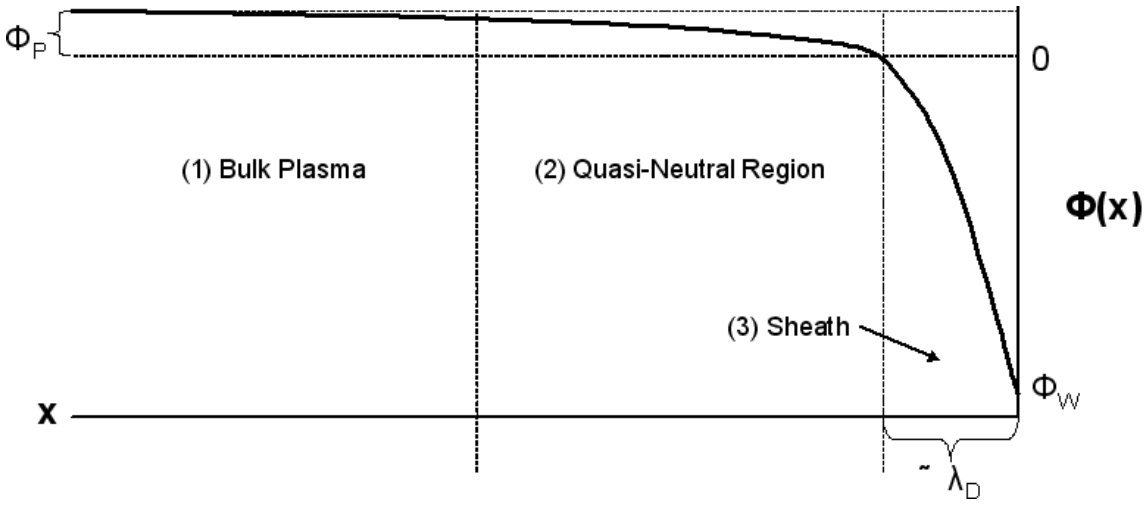


Figure 3.4: Three regions of interest exist along the boundary: (1) the bulk plasma, where $n_i \approx n_e$, (2) a quasi-neutral transition region to satisfy the Bohm sheath criterion, and (3) the plasma sheath [57, 58]. The bulk plasma maintains the highest potential in the system, the quasi-neutral region serves to preserve ion velocity continuity by beginning ion acceleration towards the sheath, and the sheath itself is where the majority of the potential is dropped, serving to equalize flux between the electrons and ions on the surface. In a negatively biased wall, the majority of the current is due to the ion flux.

Figure 3.4 shows the potential across the sheath region of a DC glow discharge, where three regions can be defined as (1) the bulk plasma, which has the most positive potential in the system, (2) the quasi-neutral transition region, where the plasma potential, Φ_P, is dropped, and (3) the sheath region, which can vary from a few to dozens of Debye lengths long, and across which the entire wall potential, Φ_W is dropped [57, 58]. Debye length, given in units of cm is a characteristic length over which an electrical disturbance is shielded,

$$\lambda_D = \sqrt{\frac{\epsilon_0 T_e}{q n_e}}\ , \tag{3.1}$$

where T_e is in units of eV. Debye length for a plasma with an average electron energy of 2 eV and density of 10^{10} cm^{-3} is about 105 μm [58]. Sheath width to first order follows the square root of

the bias voltage,

$$s = \lambda_D \sqrt{\frac{2\Phi_W}{T_e}} \,, \tag{3.2}$$

thus allowing the negative sheath to acquire significant length – on the order of 1.8 mm when $\Phi_W = -300$ V given the above Debye length [57]. The bulk of the plasma, as stated before, is nearly neutral and has no permanent electric field within it, except for the quasineutral region, which satisfies the Bohm criterion [58]. The Bohm criterion is necessary to maintain ion velocity continuity as an ion passes from the neutral bulk into the non-neutral sheath region. This said, the Bohm criterion does not account for a decrease in ion density in the sheath as ions accelerate across the high-voltage sheath in the absence of electrons, yielding a space-charge-limited-current, which is defined by the Child law [57]. The result of this law is a increase in the negative sheath to near-centimeter lengths, since,

$$s = \lambda_D \frac{\sqrt{2}}{3} (\frac{2\Phi_W}{T_e})^{0.75} \,, \tag{3.3}$$

according to the Child law [57]. The extra $(\frac{2\Phi_W}{T_e})^{0.25}$ compared to Eq. 3.2 dramatically affects the sheath length, doubling it to 3.57 mm in our example. This effect also gives the characteristic dark space near the cathode in standard plasma processes due to a lack of electrons, and thus collisions in the region. These sheath length calculations ignore weak pressure dependencies by assuming a collisionless sheath, where the mean free path is longer than the sheath length ($s > \lambda_i, \lambda_e$). Sheath length is, however, weakly dependent on pressure, decreasingly slightly with an increase in pressure [57].

A probe that measures electron and ion temperatures, plasma density, and plasma potential can be made by varying the wall potential of a wire or some conductive surface inserted into the bulk of the plasma. The random flux impinging on a surface is $n_e\overline{c_e}/4$, and $n_i\overline{c_i}/4$ for electrons and ions, respectively, which gives the upper limits to these respective fluxes [58]. A Langmuir probe, as it is called, provides an estimate of the electron and ion flux by measuring probe current as a function of its wall potential. Respective positive and negative saturation currents yield the random flux impingement rates given above for electrons and ions, and the plasma potential, Φ_P, is found by linearly fitting the natural logarithm of the sum of ion and electron currents,

$$\ln(\frac{qn_i\overline{c_i}}{4} - j) = \ln(\frac{qn_e\overline{c_e}}{4}) - \frac{q(\Phi_P - V_{Probe})}{T_e} \; and \tag{3.4}$$

$$\ln(\frac{qn_e\overline{c_e}}{4} + j) = \ln(\frac{qn_i\overline{c_e}}{4}) - \frac{q(V_{Probe} - \Phi_P)}{T_i} \,, \tag{3.5}$$

for $V_{Probe} < \Phi_P$ and $V_{Probe} > \Phi_P$, respectively. Units of eV are used for T_e and T_i in this equation.

Major complications with regard to this probe are with respect to its loading of the plasma, especially with regard to electrons, and that the sampled surface area is the outer diameter of the probe's sheath, which is modulated by the probe's potential [58]. Contamination and substrate shadowing are two other critical problems involving the use of these probes. Regardless, Langmuir probes provide an excellent means of measuring plasma conditions within a glow discharge.

3.1.4 RF Plasma Systems

A biased, insulating surface in a plasma will attain a floating potential, Φ_F, on the exposed surface in order to balance incident ion and electron flux and ensure zero net current through the insulator. Unlike actively driven conductive walls, such as a negatively biased metal cathode, an insulating surface will likely extinguish a glow discharge once the surface achieves equilibrium after the initial build up of negative charge. If, however, the bias is changed to a positive polarity, electrons will again bombard the surface and the process is restarted. At sufficiently high switching frequencies, the glow discharge is sustained, because the ion impingement velocity is too slow to drop the insulating surface potential below the sustaining voltage before switching again. Experimentally, it is found that a glow discharge is more or less stable at switching frequencies above 100 kHz [58].

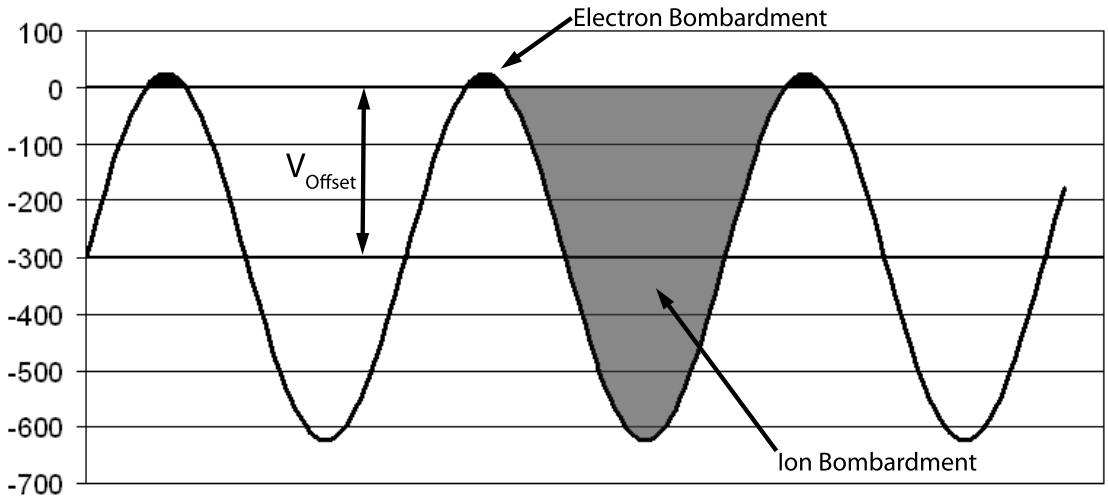


Figure 3.5: Since electron mobility is so much greater than ion mobility within the plasma, a very small percentage of the waveform needs to be positive in order to restore charge balance to the cathode surface. The grey area is the negatively biased part of the waveform which accelerates positive ions to the surface, whereas the black regions are positive biased and accelerate electrons [57, 58].

Typical RF plasma systems commonly work at 13.56 MHz, a frequency left available for industrial applications by the FCC [59]. One would expect that ion bombardment will only occur during the negatively biased half wave, but due to the great disparity between ion and electron inertia, the ions are not be able to reverse direction fast enough in the quickly changing fields. Still, electron and ion flux must be balanced over time, even in an oscillating field. Due to the higher electron mobility, a shorter period of positive bias is needed in order to equalize ion and electron current. Figure 3.5 shows the DC bias which is established to balance the time-averaged ion and electron fluxes to the surface. The magnitude of the DC bias is nearly half the peak-to-peak voltage of the RF stimulus, where only the very top of the signal is positive [58]. Even though ion flux is non-negligible during the entire period, capacitively-coupled systems operating at 13.56 MHz are inferior to systems designed around higher frequencies, from 30 MHz to 150 MHz, which appears to constitute an approximate upper limit. Higher frequencies lower the discharge sustaining voltage, so equal ion densities are generated at lower drive voltages. Likewise, the sheath depth decreases, increasing the glow discharge volume and anisotropy, since ions in the sheath experience less scattering. The plasma uniformity also increases across the electrode, which is beneficial since it lowers substrate damage and simplifies processing [59].

RF capacitively-coupled plasmas (CCP) suffer from relatively low plasma densities ($n_i \approx 10^9 - 10^{10}$ cm^{-3}), very high sheath voltages, and an intrinsic coupling between ion flux and incident ion bombardment energy [57]. Large sheath potentials are typically of significant length, on the order of several centimeters, and accelerate ions to very high velocities. Long sheath lengths severely decrease the anisotropy of the incident ions, since ions are readily scattered by neutrals in the sheath instead of impinging normal to the surface. Higher velocity ions may severely damage the surface or become implanted without an appreciable increase in sputtering yield; pitting is also common. Off-axis impingement trajectories coupled with overly high velocity ions leads to significant sidewall damage, which may affect the electrical properties of a film. Lastly, RF energy in CCP systems is converted to ion kinetic energy in the sheath, which ultimately manifests itself as thermal energy in the walls and substrate as opposed to increased ionization [57]. The reactive ion etcher available here at OSU is a PlasmaTherm System VII, a 6 inch CCP system capable of 4 simultaneous individual gas feeds and a 550 W RF power supply.

3.1.5 High Density Plasma Sources

Many types of systems exist to enhance ion densities, lower sheath voltages, and separate the generation of ions from their bombardment energy. Those discussed herein are DC and RF magnetron systems, inductively-coupled plasmas (ICP), electron cyclotron resonance systems (ECR)

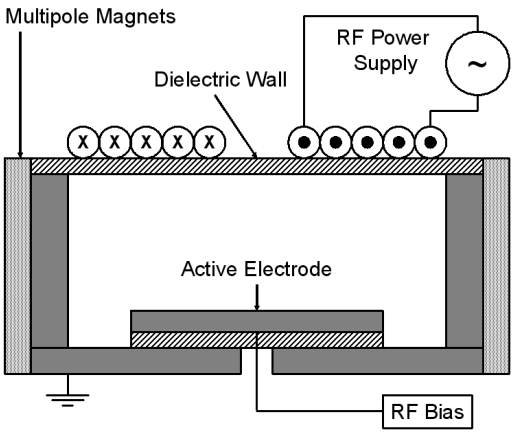
and helicon systems. Schematic diagrams of a planar ICP, a helical ICP, a close-coupled ECR, and a helicon system are shown in Fig. 3.6. The basic planar diode system described in the previous sections is shown in Fig. 3.1; a magnetron system is identical to a planar diode system except for the addition of a permanent magnet placed beneath the active electrode.

3.1.5.1 RF and DC Magnetron Systems

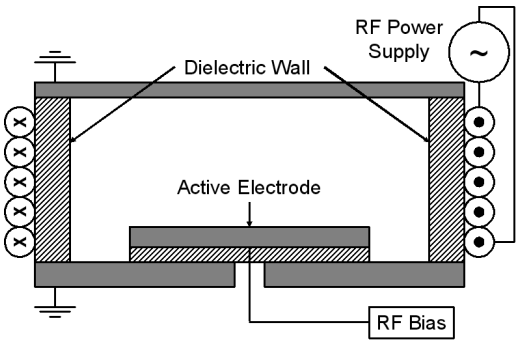
Both RF and DC glow discharges can be magnetically enhanced via a weak to moderate DC magnetic field placed in parallel to the surface of the active RF electrode. The DC magnetic field entrains the plasma to a smaller volume directly above the electrode, increasing ion density, and constraining electron motion to paths more orthogonal to the electric field lines, thereby reducing nonambipolar losses [57]. The constrained plasma in a RF magnetron system experiences increased stochastic heating since an electron has a gyrating path in the magnetic field, meaning that it strikes the sheath wavefront multiple times, greatly increasing the energy of the electron. DC and RF magnetrons benefit from increased ohmic heating due to higher electric fields in the plasma itself [57]. Unfortunately, DC and RF magnetron systems suffer from nonuniformity across the electrode surface, even when the magnetic field is rotated around the primary axis of the electrode. This gives the characteristic "racetrack" pattern on sputter targets, where an annular region of higher ion density impinges on the target; etching systems also experience higher rates in an annular region near the edge [58].

3.1.5.2 Inductively-Coupled Plasmas

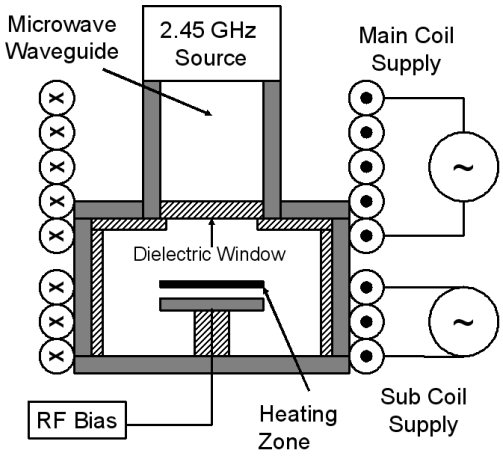
Inductively coupled plasma systems permit the separate generation of ion species and bombardment energy by using a RF generator to drive a solenoid which is isolated from the vacuum chamber via a dielectric window. This is different from CCP systems, which are directly connected, as as seen in Figs. 3.6(a) and 3.6(b) [57]. The acceleration of ions to the surface of the active electrode is controlled via a second independent capacitively-coupled RF or DC source. Plasma ignition is understood to begin via simple capacitive coupling from the inductor through the dielectric wall until a sufficient density of electrons are present in the sheath. As the sheath achieves a certain level of conductivity, the magnetic field more closely couples to the free electrons and the coil voltage lowers, since the magnetic field energy is finally absorbed [57, 59]. The plasma, now effectively a conductor, resists the magnetic field along its skin by inducing a counter-rotating current which opposes the field. This occurs within a characteristic skin depth, which is the distance that the field decreases to $1/e$ of its initial value. The skin depth is inversely proportional to both the frequency of the field and the conductivity of the plasma; the smaller the skin depth, the higher



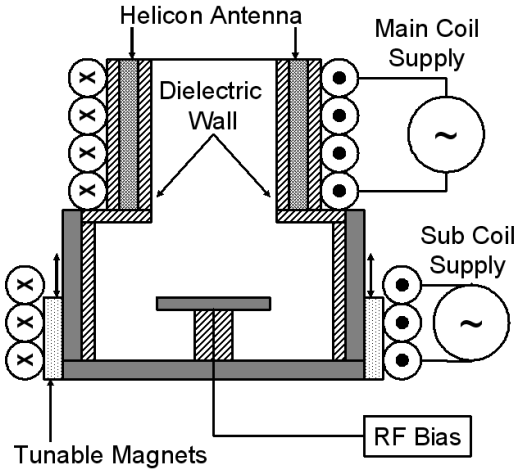
(a) Planar Inductively-Coupled Plasma System



(b) Helical Inductively-Coupled Plasma System



(c) Close-Coupled Electron Cyclotron Resonance Plasma System



(d) Helicon Plasma System

Figure 3.6: In both inductively-coupled plasma (ICP) systems, the plasma is energized through magnetic coupling across the dielectric window from the solenoid. The plasma, effectively a conductor, resists the electromagnetic radiation within its skin depth, thus heating up electrons in this region. A separate DC or RF power supply is attached to the active electrode to independently control the ion bombardment energy. In an electron cyclotron resonance system (ECR), emitted microwave radiation is first channeled through the waveguide and dielectric window. In the vacuum chamber proper, electrons experience a cyclotron resonance along the right hand polarized radiation, where the microwaves couple their energy to electrons through collisionless Landau dampening, which heats nonthermal electrons preferentially by accelerating electrons to the phase velocity of the wavefront. The presence of a magnetic field increases the minimum frequency necessary to excite a cyclotron resonance, i.e., a 2.45 GHz microwave will cause resonance in a ∼875 G field. The region of resonance can be modulated in location to affect etch or deposition characteristics; extra permanent magnets or electromagnets are used to confine the cone of the discharge (heating zone). A helicon system excites transverse mode whistler waves via a RF antenna. Energy absorption mechanism is identical, but helicon absorption occurs throughout the chamber. Ionization in both ECR and helicon systems can be realized remotely, greatly lowering the number of high-energy electrons and ions impinging onto the substrate at the cost of ion and reactive neutral density loss [57, 59].

the coupling of magnetic energy from the inductive source to the electron gas, which ultimately drives the ionization of the plasma [59, 63].

ICP systems have much lower sheath potentials, around 20-40 V, even when the inductor has an equivalent RF bias, due to the very small capacitive coupling of the coils to the sheath [57]. There is very little ion loss to the walls as a result, since the ion impingement velocity to a insulating surface is quite low, making ICP systems much more efficient at ion generation in the bulk. ICPs operate with ion densities $\sim 10^{11}$ to 10^{12} cm^{-3}, yielding nearly a hundredfold increase over CCP systems at the same pressure [57, 58]. Ultimately, ICP etchers operate at lower pressures, thereby increasing etch anisotropy, since the mean free path of ions increases in proportion to the sheath length.

3.1.5.3 Wave Heated Plasmas

Electron cyclotron resonance systems rely on the coupling between incident electromagnetic waves and nonthermal electrons to energize the plasma [57, 59]. Like ICPs, ECR-generated plasmas have low sheath voltages (10 to 15 V), and the substrate platen is driven independently of the ionization source [57]. ECR systems typically use 2.45 GHz microwave generators due to the availability of high power generators designed for this frequency. Compared to ICP systems, ECRs generate higher nominal plasma densities (10^{12} to 10^{13} cm^{-3}) at lower pressures (0.3 to 10 mTorr) [59]. That said, even the most simple ECR etcher is more complicated than an ICP system.

Electrons experience a cyclotron resonance when excited by an electromagnetic wave in the presence of a magnetic field according to the relationship,

$$\omega_{ce} = \frac{q|B|}{M_e}, \tag{3.6}$$

or more simply, $F_{ce}(MHz) = 2.79|B|$, where B is the magnetic flux density in units of Gauss and M_e is electron rest mass in units of kilograms [57, 59]. Electrons largely absorb the incident microwave energy via Landau damping, a collisionless process in which charged particles are accelerated to the phase velocity of the radiation. Coupling follows the right hand rule: Landau damping for electrons can only occur with right hand polarized wave packets [57, 59].

While the cyclotron resonance frequency is notably lower under free-field conditions, both penetration of the electromagnetic wave into the plasma and the chamber sensitivity suffer, which ultimately limits the plasma density. The introduction of a non-uniform magnetic field along the axis of wave propagation allows the radiation to penetrate a high density plasma and be absorbed at the desired location, called the magnetic beach [57, 59]. Magnetic fields can guide ions from the

electron heating zone to the substrate, but axial diffusion will spread the beam, lowering the ion density and increasing losses to the wall while concomitantly increasing uniformity at the substrate. Increasing bias to the substrate can compensate for some of the ion density loss, but at the cost of increasing the ion bombardment energy. These high aspect ratio systems enjoy lower magnetic fields within the chamber, since the magnetic beach is placed just within the source chamber and funneled magnetically to the process chamber.

While early ECR designs placed the ion generation site remote from the substrate, modern designs have moved towards close-coupled systems, as shown in Fig. 3.6(c), where the process and source chambers are combined and the heating zone is placed nearly directly over the substrate. Advantages of a closed-coupled system are many: higher ion and reactive neutral densities at the substrate, lower ion bombardment energy, lower ion and reactive neutral losses to walls, and a decrease in tool size. Disadvantages of a close-coupled system include the necessity of maintaining the correct proximity between the heating zone and the substrate, and maintaining uniformity across the substrate [57, 59].

Like ECRs, helicon systems heat the electron distribution by exciting an electron resonance mode. Figure 3.6(d) shows a generic helicon system, where a driven helical RF antenna generates a quasistatic transverse wave inside the magnetically-confined cylindrical chamber, whose energy is then absorbed by free electrons. The primary radiation absorbtion mechanism for both ECRs and helicons is Landau dampening, which is described above and is well suited to low pressure operation. Helicon systems typically operate at RF frequencies, often using a 13.56 MHz source, thus greatly reducing their magnetic field requirements to 100-300 G as opposed to 875 G for a 2.45 GHz ECR system [59]. Like ECRs and ICPs, a helicon system can control ion densities and bombardment energies through a separate substrate supply.

Helicons have higher plasma generation efficiencies than ECRs, ionizing more species for the same source power than any other system. This yields the highest nominal plasma density for any system, which is in the range of 10^{13} to 10^{14} cm^{-3} for an argon feedstock with 1-2 kW of RF power [59]. Given the columnar nature of the discharge, the radial plasma density function throughout the excitation volume is relatively uniform, except at the sheath. Lastly, the entire chamber lining can be fabricated using ceramics, thereby greatly lowering substrate contamination from metals via sidewall sputtering.

3.1.6 Conclusion

In this section an overview is provided of the basic mechanisms present in an electrically driven plasma and of various plasma processing technologies presently in use. In the examination of

ITO, IZO and ZnO etch literature, ICP systems are commonly used due to their higher ion densities at lower pressures, simplicity of use, independently driven substrate bias, and lower sheath voltages. CCP and ECR systems are also common and systems which use multiple CCP and ECR plasma generators are available for large-area applications. Few commercial helicon systems exist at the moment, but given their efficiency and benefits, will likely become a significant technology. The thin films used in LCD and other TFT applications (<200 nm, typically) obviate the need for low damage, uniform etches over large areas.

3.2 Thin Film Processing

3.2.1 Thermal Evaporation

Aluminum and other metals with low melting and evaporation temperatures can be deposited onto the substrate via thermal evaporation. Electrical current is supplied to a resistive wire coil or basket made nominally of W or Mo, which heats and evaporates the metal of interest. Refractory materials cannot be deposited via thermal evaporation due to high power requirements and the lack of refractory crucibles capable of managing the necessary temperature without contamination while effectively conducting the heat to the target material. Electron beam evaporation (EBE) and sputtering are more suitable deposition methods for refractory materials.

3.2.2 Plasma-Enhanced Chemical Vapor Deposition

Low temperature, high quality films can be grown via plasma-enhanced chemical vapor deposition (PECVD) at much lower temperatures than conventional CVD. A glow discharge is used instead of purely thermal energy to generate the reactive species that deposit onto the surface. For example, the activation energy of silane (SiH_4) is 1.5 eV for high-temperature CVD and 0.025-0.1 eV for PECVD [57]. Additional substrate heat is used to improve reaction speed, film density, local crystalline order, and conformality. PECVD-based SiO_2 is provided by Hewlett-Packard using silane at 350 °C.

3.2.3 Sputtering

Incident ions impinging on a surface involve one or more of the following mechanisms: reflection and likely neutralization, secondary electron emission via impact ionization, implantation, structural reorientation, or sputtering [58]. Reflection and secondary electrons are discussed in Section 3.1.2. Implantation occurs when an incident ion becomes permanently embedded in the film. Sputtering is a process where one or several molecules is ejected from a surface after an incident ion impinges on the surface with sufficient energy. The energy from the incident ion is

imparted to target species which can travel up to the surface and may ultimately aid in the ejection of one or more atoms from the surface, in the same manner as a cue ball in billiards [58]. The threshold energy for sputtering is around 20-30 V, but sputter yields increase until several hundred volts of ion energy, where implantation becomes significant [57].

Crystalline defects created along the propagation path of the impinging ion reorient the structure, largely amorphizing the near-surface, which lowers the atomic density and the surface binding energy. Damaged surfaces have higher surface reaction rates due to improved thermodynamics: the reduction in surface binding energy ultimately lowers the free energy needed for the reaction. While high-energy neutral atoms impinging on the surface render the same effects, few exist in a nearly room temperature distribution. Ions accelerating across the sheath gain the necessary energy to initiate these mechanisms. Argon is the primary gas used for sputtering, due to its relatively high sputter yields, low cost, low chemical reactivity, and the fact that most ionic molecules fragment upon contact with the surface [57].

For sputter deposition, a target is used as the actively driven electrode, where positive ions impinge and vaporize the target surface, creating a plume of effluents that are intentionally deposited onto a substrate. Sputtered films maintain excellent stoichiometric control, especially in comparison to an electron beam or thermally evaporated material. Highly electronegative elements, such as oxygen or fluorine are found as negative ions in the plasma and, like electrons, accelerate towards the grounded surfaces of the chamber, which commonly includes the substrate, and may lead to substrate sputtering, which may dramatically affect the deposited film quality. As described in Section 3.1.4, DC sputtering is used only for conductive targets, and RF sputtering must be used with insulating targets, such as the AOS materials used in this thesis, but may be used on conductive targets as well. At Oregon State, there are two sputtering systems available, an in-house built system capable of both RF (13.56 MHz) and DC magnetron sputtering which houses two 3 inch diameter targets and three 2 inch diameter targets, and a Control Process Apparatus sputter tool.

3.2.4 Reactive Ion Etching

Reactive ion etching uses a glow discharge to create reactive species, which upon impinging the surface of the substrate, create volatile species. Physical sputtering assists in the reaction, as described in Section 3.2.3, and also aids in devolving reacted species from the surface. The reactive ion etcher available at OSU is a PlasmaTherm System VII, a 6 inch CCP system capable of delivering 4 simultaneous individual gases and a 550 W RF power supply.

3.2.5 Thermal Annealing

At higher temperatures, deposited AOS films appear to undergo some local reordering, which may affect crystallinity and stoichiometry. Substrates experience some heating during film deposition. In-situ heating is typically insufficient to effect the necessary changes in film properties. Therefore, deliberate post-deposition anneals are used to change crystallinity and stoichiometry of films. Several ambient air furnaces are used to anneal samples. Nominal ramp rates are 5 °C/min. Usual hold times at maximum temperature are 1 hour.

3.2.6 Photolithography

By exposing a photosensitive organic film (photoresist) to ultraviolet (UV) light through an opaque mask, and subsequently developing the film in solution, a pattern can be transferred into the organic film. This patterned film is then used as an effective mask for other processes. Lift-off is a process whereby photoresist is first deposited and patterned and then the material of choice is deposited. The photoresist is then dissolved away, liberating the film on top in the process and leaving material only in mask openings. Likewise, an opposite pattern in photoresist protects the surfaces of interest from etching. The photoresist used at OSU is Shipley 1818 photoresist, which is spun on to samples and baked at 85 °C before and after exposure. A Karl Suss MJB-3 is used for alignment and exposure.

3.3 Thin Film Transistor Characterization

3.3.1 Current-Voltage Measurements

A suite of DC I-V measurements are used to determine the electrical properties of TFTs. A linear regime I-V measurement is used to extract mobility and output conductance. While sampling I_D, V_{DS} is held constant at 1 V and V_{GS} is swept from nominally -10 V to 40 V in 0.5 V increments. A second test, identical to the aforementioned sweep except that $V_{DS} = 30$ V, is used to estimate threshold voltage and turn-on voltage. Either test may be used to determine the subthreshold swing. Last, a series of I_D-V_{DS} ($0 \leq V_{DS} \leq 40$ V, in 1 V steps) sweeps are measured at several V_{GS} values ($-10 \leq V_{GS} \leq 40$ V, in 10 V steps), where general transistor behavior is noted and ultimate output current is extracted. Measurements are made using an Agilent 4155c semiconductor parameter analyzer and samples are loaded into a dark chamber, unless otherwise noted.

3.3.2 Threshold Voltage Extrapolation

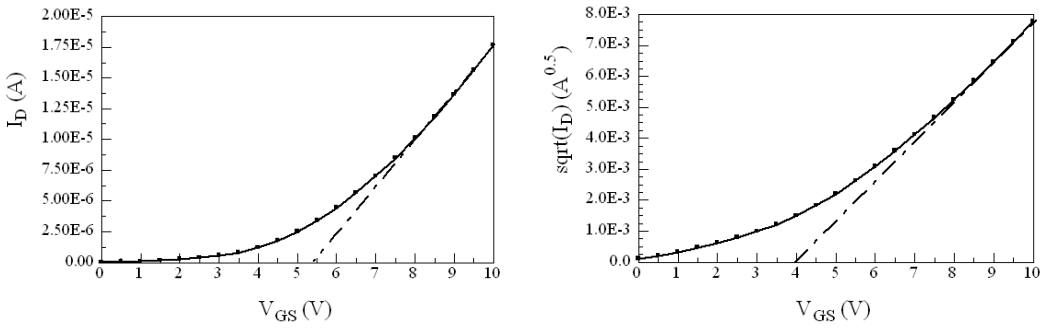
In a standard square-law model for a MOSFET, the pre-pinch-off (3.7) and post-pinch-off (3.8) I_D equations are,

$$I_D = \frac{W}{L}\mu C_G((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}) \tag{3.7}$$

$$I_D = \frac{W}{2L}\mu C_G(V_{GS} - V_T)^2 \ , \tag{3.8}$$

respectively. Therefore, as shown in Fig. 3.7 for a ZTO-based TFT, an estimate of V_T is obtained by plotting either I_D-V_{GS} or $\sqrt{I_D}$-V_{GS} in the pre-pinch-off or post-pinch-off regime, respectively. Extrapolating the linear part of these two curves to the x-intercept extracts the threshold voltage. V_T for the given example is $\sim$ 5.5 V and 4 V using for the pre-pinch-off and post-pinch-off methods, respectively. Differences between the two values is likely due to mobility degradation and series resistance effects in the pre-pinch-off regime [64].

While typically defined as a discrete electrical parameter, V_T is quite ambiguous and has little physical meaning, since V_T indicates the onset of "strong inversion" in MOS technologies and "strong accumulation" in TFT technologies, due to the presence of significant subthreshold current [64]. A more accurate parameter is turn-on voltage, V_{ON}, which is the gate voltage necessary to begin channel conduction. V_{ON} is indicated by a sharp increase in current along a log(I_D)-V_{GS} curve. The independence of V_{ON} from V_{DS} and the simplicity of directly extracting V_{ON}, as opposed to a linear extrapolation, make V_{ON} an attractive model parameter in comparison to V_T. While V_{ON} may be a better parameter to describe the physical operation of the transistor, V_T is often used in circuit modeling and is frequently reported in AOS literature.



(a) V_T Pre-pinch-off

(b) V_T Post-pinch-off

Figure 3.7: V_T extrapolation methods for (a) pre-pinch-off and (b) post-pinch-off regimes for a ZTO-based TFT operated at a V_{DS} of 1 V and 30 V, respectively.

3.3.3 Carrier Mobility

In the most basic definition, mobility is described as the the proportionality constant between the carrier drift velocity and the electric field. Traditionally in MOSFET technologies, three major mobilities are specified in order of physical significance: field-effect, effective, and saturation [64]. For both μ_{eff} and μ_{FE}, measurements are made at low drain voltages to maintain a near-uniform channel charge density across the channel [64]. Effective mobility is extracted from the drain conductance ($g_d = \frac{\partial I_D}{\partial V_{DS}}|_{V_{GS}}$) at a given channel charge concentration ($Q_{CH} = C_G(V_{GS} - V_T)$), and is defined by,

$$\mu_{eff}(V_{GS}) = \frac{g_d(V_{GS})}{\frac{W}{L}Q_{CH}(V_{GS})} = \left.\frac{\frac{\partial I_D}{\partial V_{DS}}|_{V_{GS}}}{\frac{W}{L}C_G(V_{GS} - V_T)}\right|_{V_{DS}\to 0}. \tag{3.9}$$

Effective mobility is highly sensitive to effective gate capacitance, effective channel width and length dimensions, and series resistance effects, but provides the best prediction to circuit performance [64, 33]. Field-effect mobility is derived from the transconductance ($g_m = \frac{\partial I_D}{\partial V_{GS}}|_{V_{DS}}$) instead of the drain conductance. Extracting g_m from the drain current equation in the pre-pinch-off regime (Eq. 3.7) results in the field-effect mobility equation,

$$\mu_{FE}(V_{GS}) = \frac{g_m(V_{GS})}{\frac{W}{L}C_G V_{DS}} = \frac{\frac{\partial I_D}{\partial V_{GS}}|_{V_{DS}}(V_{GS})}{\frac{W}{L}C_G V_{DS}}. \tag{3.10}$$

As opposed to μ_{FE} and μ_{eff}, μ_{sat} is extracted from post-pinch-off data. Thus, problems associated with contact and other series resistance effects are minimized. However, μ_{sat} has the least physical meaning [64]. An estimate of μ_{sat} is obtained from an extraction of the slope of the straight line section of an $I_D^{0.5}$ versus $(V_{GS} - V_T)$ curve [64]. The slope, m, then replaces $(I_D^{0.5})/(V_{GS} - V_T)$, yielding the equation,

$$\mu_{sat} = \frac{2m^2}{\frac{W}{L}C_G}. \tag{3.11}$$

While mobility values are typically given as a single constant, voltage-dependent phenomena such as interface scattering, carrier trapping, quantization, and velocity saturation strongly affect mobilities. In MOSFETs, μ_{FE} is typically lower than μ_{eff} due to a nonlinear decrease in μ_{eff} with increasing V_{GS}, whereas the opposite trend is noted in TFTs [33, 64].

While much of the AOS transistor literature report μ_{FE}, μ_{eff}, and μ_{sat}, average mobility, μ_{avg}, and incremental mobility, μ_{inc}, are considered preferable for TFTs, due to having physical significance in TFT carrier transport. Average mobility examines nominal mobility of the entire carrier volume within the channel. Like μ_{eff}, μ_{avg} is derived from g_d, but uses V_{ON} in place of

V_T, yielding,

$$\mu_{avg}(V_{GS}) = \left.\frac{g_d(V_{GS})}{\frac{W}{L}Q_{CH}(V_{GS})}\right|_{V_{DS}\to 0} = \left.\frac{\frac{\partial I_D}{\partial V_{DS}}|_{V_{GS}}}{\frac{W}{L}C_G(V_{GS}-V_{ON})}\right|_{V_{DS}\to 0}. \tag{3.12}$$

Assuming carriers already in the channel remain at a constant mobility, incremental mobility reports the mobility of the carriers added to the channel as the gate drive increases (i.e., increasing V_{GS} for n-type materials) [33, 31]. Thus, incremental mobility, which is defined as,

$$\mu_{inc}(V_{GS}) = \left.\frac{\frac{\partial g_d}{\partial V_{GS}}(V_{GS})}{\frac{W}{L}C_G}\right|_{V_{DS}\to 0}, \tag{3.13}$$

correlates more closely with carrier transport within the channel. The peak average mobility for a TFT is lower than peak incremental mobility for a given device since μ_{avg}, which is defined as the average of the all incremental mobility values from the onset of current [31], i.e.,

$$\mu_{avg}(V_{GS}) = \frac{1}{V_{GS}-V_{ON}}\int_{V_{ON}}^{V_{GS}} \mu_{inc}(V)\partial V. \tag{3.14}$$

Low incremental mobilities are expected at near turn-on gate voltages, since most initially injected carriers are captured in traps. As gate voltage increases, traps are filled, thus yielding increases in incremental mobilities until second-order effects such as series resistance or interface scattering become significant. While incremental mobility gives insight into carrier transport across the transistor, μ_{avg} is a more appropriate parameter for assessing circuit performance, since it accounts for the entire channel carrier volume.

3.4 Conclusion

After a basic discussion of electrically driven plasmas, this chapter provides an overview of processing techniques used in this thesis such as thermal evaporation, plasma-enhanced chemical vapor deposition, sputtering, reactive ion etching, thermal annealing, and photolithography. Finally, an explanation of threshold voltage and several carrier mobility extraction techniques is given. Discrete device performance is presented in terms of V_{ON}, μ_{avg}, and μ_{inc}. For circuit performance, V_T and μ_{avg} appear most significant.

4. AOS ETCHING & ZTO PROCESS INTEGRATION

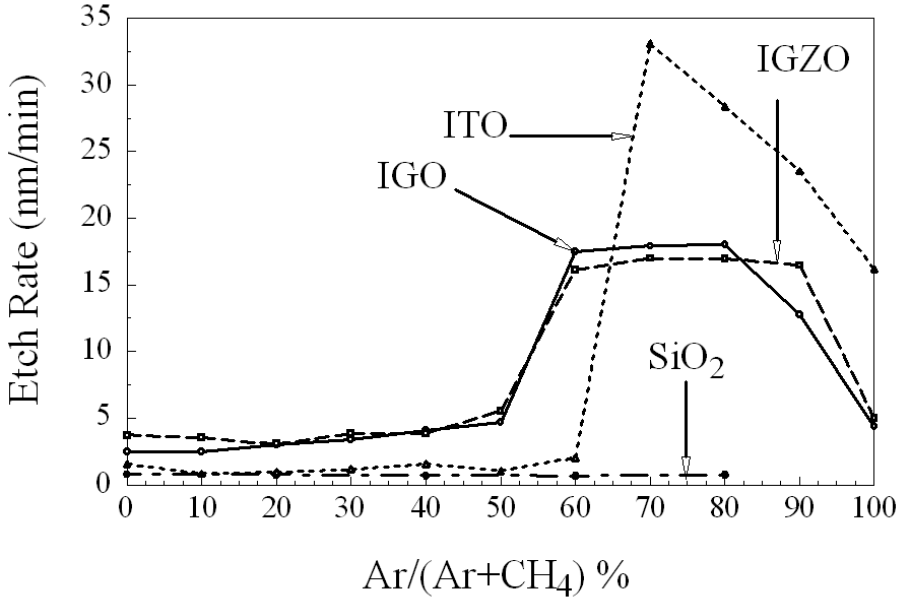
This chapter discusses process integration of zinc tin oxide (ZTO) as an active channel material in thin-film transistor based circuits. First, the results of an amorphous oxide semiconductor (AOS) dry etch study using an Ar/CH_4 gas stream are reported. Leveraging the knowledge gained with respect to AOS etching, a process is developed to integrate ZTO for integrated circuit applications. Subsequently, ZTO TFT AC/DC rectifier circuits are fabricated, evaluated, and compared to recently realized IGO TFT AC/DC rectifier circuits.

4.1 Amorphous Oxide Semiconductor Plasma Etching

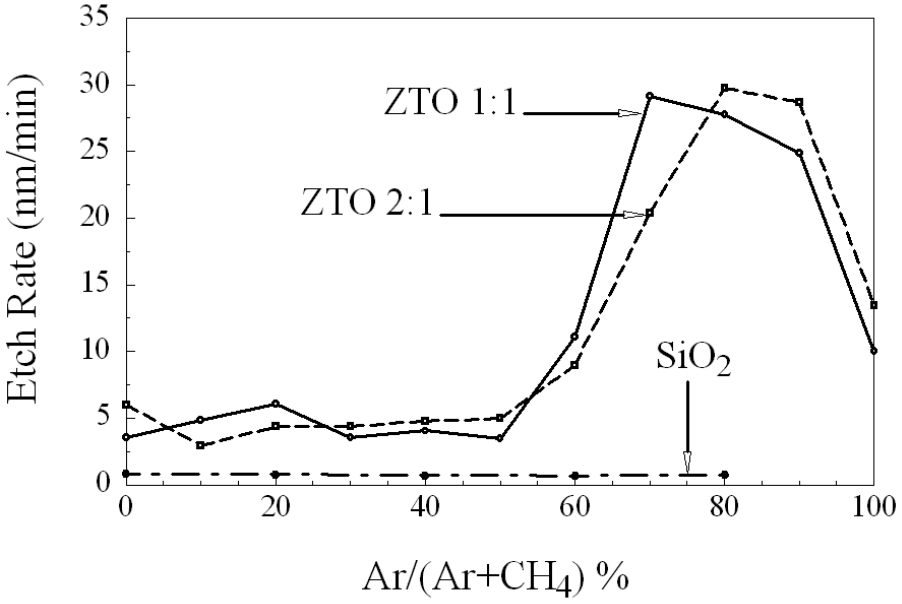
An etch study involving several AOS materials and polycrystalline ITO is conducted over a range of argon and methane (Ar/CH_4) ratios in order to determine the maximum etch rate for each material. All materials except ITO (90:10 In:Sn) are tested on 10 x 15 mm^2 substrates masked with Kapton tape, while ITO is tested using 12.5 x 12.5 mm^2 substrates. Materials tested are 1:1 IGO, 1:1 ZTO, 2:1 ZTO, 1:1:1 IGZO and 90:10 ITO, where X:Y is the cation ratio of the material. Both ZTO stoichiometries are deposited from 2 inch diameter targets at 75 watts, in a 90/10 Ar/O_2 atmosphere at 5 mTorr. The IGO deposition is identical except that the Ar/O_2 ratio is 95/5. The 3 inch diameter IGZO target is sputtered in pure argon at 100 watts and 5 mTorr, and the 180 nm thick ITO is purchased from Delta Technologies on 25 x 25 mm^2 Corning 1737 substrates, which are then cleaved into quarters. No intentional annealing is done before etching. The nominal thickness of all AOS layers sputtered in-house is greater than 120 nm.

The study is conducted using a Plasmatherm System VII parallel plate reactive ion etcher operating at 150 W (0.6 W/cm^2) of RF power, 100 mTorr of pressure, and with 25 sccm of combined flow for 3 minutes. ITO is etched for 5 minutes, due to its greater thickness. A 3 minute O_2 plasma treatment is accomplished immediately after the Ar/CH_4 etch in order to remove polymer deposits from the chamber. After etching, the Kapton tape is removed and samples are rinsed in acetone and isopropanol to clean off any adhesive residue. A Tencor Alphastep profilometer is used to measure the step height of the etched part at four roughly equidistant locations on the substrate. At least two independent etch runs are accomplished at each measured Ar/CH_4 ratio and a third or fourth run is conducted if the results of the first two points are appreciably different.

As shown in Fig. 4.1, excellent etch selectivity with respect to thermally-grown SiO_2 is obtained across the range of 0% to 80% Ar, except for ITO etching at $Ar/(Ar + CH_4)$ percentages less than about 60%. AOS materials are not selective with respect to each other. Etch rates peak



(a) Indium-containing Compounds



(b) ZTO Compounds

Figure 4.1: Etch rate versus gas composition for 1:1 IGO, 1:1:1 IGZO, 90:10 ITO, thermal SiO_2, 1:1 ZTO, and 2:1 ZTO in an Ar/CH_4 stream. Plasma etching is accomplished in a 100 mTorr atmosphere at 150 watts with 25 sccm total gas flow for 3 minutes. ITO is etched for 5 minutes due to its greater thickness. Excellent etch selectivity respect to thermally-grown SiO_2 is obtained across the range of gas compositions, except for ITO at $Ar/(Ar + CH_4)$ ratios $\leq 60\%$.

between 60/40 and 90/10 Ar/CH_4. Methyl species, i.e., CH_3, are obtained from electron-methane collisions, e.g., $CH_4 + e^- \rightarrow CH_3 + H + e^-$. At high methane gas concentrations, low etch rates are realized since CH_3-based polymer deposition outpaces its own removal and eventually masks the surface. At higher argon concentrations, additional sputtering and substrate heating associated with argon bombardment increases the polymer removal rate and assists in volatilization of the methyl-metal species. Indium gallium zinc oxide (IGZO) (1:1:1) and indium gallium oxide (IGO) (1:1) etch in a virtually identical manner. Ga_2O_3, In_2O_3, and ZnO all appear to etch at nearly the same rate in an Ar/CH_4 mixture. Tin-bearing AOS materials etch at higher rates, even for low tin concentrations. ITO is completely removed from the unmasked surface at a relative flow of 70/30 Ar/CH_4, so that its actual etch rate is at least 33 nm/min. Grain boundaries in polycrystalline ITO are likely attacked more aggressively by CH_3, which ultimately increases the etch rate.

4.2 ZTO Circuit Process Integration

To date, AOS-channel based TFT circuits have been fabricated using either IGO [65, 66] or IGZO [67, 68, 69, 70]. Given the high material cost of both indium and gallium, these AOS channel materials are less attractive for high volume manufacturing applications such as LCD panels. ZTO has not been used in circuits, largely due to the lack of a selective wet etch chemistry, in spite of its similar device performance compared to IGO and IGZO. ZTO is a compelling choice since it is inexpensive. Another advantage of ZTO is that it can be deposited from a metal target via DC reactive sputtering [42], which affords higher deposition rates, greater target purity, and superior manufacturablity. In contrast, gallium- and indium-based AOS compounds must be sputtered via RF magnetron sputtering using ceramic targets.

ZTO circuits are realized using the knowledge obtained from the previously described AOS dry etch study (Section 4.1). The following sections describe process integration considerations relevant to the fabrication of bottom-gate ZTO TFT AC/DC rectifier circuits. The reader is invited to read Brian McFarlane's M.S. thesis [66], which covers circuit design, layout, and measurement techniques used to synthesize and test equivalent IGO AC/DC rectifier circuits. The work presented herein replicates McFarlane's work, using the same mask set, but substituting ZTO as the channel layer material.

ZTO circuit process integration can be separated into the following major components:

1. Substrate: ~180 nm thick ITO deposited onto 25 x 25 x 1.1 mm^2 Corning 1737 glass
2. Gate stack synthesis

    (a) Substrate cleaning

(b) Pattern gate electrode (ITO) via wet etch (Mask 1)
(c) PECVD 100 nm SiO_2 layer

3. Channel deposition

(a) Substrate cleaning
(b) Sputter deposit 50 nm ZTO channel layer
(c) Pattern channel via plasma etch (Mask 2)
(d) Photoresist removal

4. Via etch

(a) Wet etch pattern vias through SiO_2 (Mask 3)
(b) Photoresist removal and plasma ashing

5. Anneal
6. Source/Drain lift-off

(a) Pattern for source/drain lift-off (Mask 4)
(b) Thermally evaporate 200 nm aluminum layer
(c) Photoresist removal and metal release
(d) Substrate cleaning

4.2.1 Gate Stack Synthesis

Delta Technologies supplied Corning 1737 substrates coated with a ∼180 nm thick ITO layer are first rinsed in 18.2 MΩ water (referred to simply as deionized (DI) water for the remainder of the thesis) and placed in an ultrasonic cleaner containing 45 °C Contrad 70 detergent for 45 to 60 minutes. After sonication, substrates are rinsed with DI water and then quickly sprayed with acetone, isopropanol, and DI water. Samples are blown dry using nitrogen then placed in a ∼125 °C oven for at least 10 minutes to dehydrate, and then left in air to cool before patterning.

Photolithography begins by spin coating substrates with Shipley 1818 photoresist at 4000 rpm for 20 s, yielding a 1.8-2.0 μm film. The soft bake is 2 minutes at 85 °C on a hot plate, followed by gate mask alignment and an 8 second exposure. The post-exposure bake is 85 °C for 4 minutes on a hot plate. Samples are soaked in a solution of 4 parts DI water and 1 part Microposit 351 developer for roughly 20-35 seconds until patterns are well defined. A final bake is 2 minutes long on the same 85 °C hotplate. The ITO is wet etched using ∼12 M hydrochloric acid (HCl) for 5 minutes. The edges are then electrically probed to ensure that the unmasked ITO is completely removed. Again the samples are rinsed in acetone, isopropanol, and DI water to remove the photoresist and then placed in a dehydration oven.

The substrates are then delivered to Hewlett-Packard, for deposition of a 100 nm thick SiO_2 silane-based PECVD SiO_2 layer.

4.2.2 Channel Deposition

After receiving samples back from HP, the substrates are rinsed with DI water to remove any particulate and dehydrated at 125 °C for at least 4 hours. A significant decrease in particles is noted after rinsing in DI water under 50x optical magnification. Various other cleaning methods were attempted on Si/SiO_2 coupons with unsatisfactory results, i.e., ZTO TFTs exhibited a "kink" and other non-idealities in their $\log(I_D)$-V_{GS} transfer curves. Likewise, sample preparation using anything other than DI water yielded a high variability in TFT performance.

Two substrates are loaded into the sputter tool, which is pumped down to a maximum base pressure of 2 x 10^{-6} Torr. A 2 inch diameter 2:1 $ZnO:SnO_2$ target is pre-sputtered for 10 minutes at 75 watts after a ramp up from 50 watts at 10 watts per minute in a 20/2.2 sccm (90/10) Ar/O_2, 5 mTorr ambient. The substrates are sputter deposited for 7 minutes with a ∼10 cm substrate-to-target distance. During deposition, substrates are translated over a 4 inch range to improve thickness uniformity. The resulting ZTO film is ∼60 nm thick.

Upon removal from the sputter deposition tool, samples are rinsed with DI water to remove dust particles and placed on a 85 °C hot plate for at least 10 minutes. Using the same photolithography steps described above, but with a 4 min. long final bake, the substrates are patterned using a channel etch mask. Samples are loaded into a RIE system where they are etched for 6 minutes in a 20/5 sccm (80/20) Ar/CH_4, 100 mTorr plasma at 150 watts (0.6 W/cm^2). The Ar/CH_4 etch plasma both deposits a significant polymer film onto all non-etched surfaces and causes the photoresist to harden dramatically, which requires a multi-step cleaning process to remove. Thus, samples are ashed for 3 minutes at 100 W in a 100 mTorr 2/1/25 sccm $Ar/CHF_3/O_2$ gas stream prior to venting the RIE. Substrates are then rinsed in acetone, isopropanol, and DI water before being ultrasonically agitated in Shipley 1165 photoresist stripper for 6 minutes. The photoresist stripper is rinsed off with DI water and blown dry with nitrogen. Samples are reloaded into the RIE and a 15 minute 900 mTorr, 100 sccm O_2, 400 watt ash is conducted to remove any hardened photoresist and polymer from the substrate surface. Section 4.3.1 discusses photoresist and polymer ashing procedure development and its electrical effects.

4.2.3 Via Etching

After the ash, the samples are rinsed again with DI water to remove particles, blown dry, and placed on a 85 °C hot plate for dehydration. Like the ZTO channel etch, photolithography finishes with a 4 minute final bake. Both a buffered HF etch for 45 seconds and a 5 minute, 15 sccm CHF_3, 30 mTorr, 75 watt plasma etch demonstrated a complete opening of the SiO_2 vias. However, the wet etch is used. After etching, samples are rinsed clean of photoresist using an

acetone, isopropanol, DI water rinse and again ultrasonically agitated in 1165 photoresist stripper for 5 minutes. Substrates are rinsed with DI water and loaded into the RIE for a 30 minute, 900 mTorr, 100 sccm O_2, 400 watt ash. Samples are removed from the RIE and ultrasonically agitated in DI water for 30 seconds to remove any lodged particulate and then blown dry.

4.2.4 Anneal

Anneal temperature has a significant effect on device performance; the mobility increases significantly and the subthreshold swing decreases dramatically with increased anneal temperature. Turn-on voltage, however, becomes more negative at a higher annealing temperature. The best compromise between device quality and turn-on voltage is realized using a 450 °C anneal for 1 hour and a 5 °C per minute ramp rate.

4.2.5 Source/Drain Lift-off

Upon removal from the oven, samples are rinsed in DI water and dehydrated for 10 minutes at 85 °C. The photolithography process described above in Section 4.2.1 is used, except that the final bake step is omitted in order to keep the photoresist relatively soft for lift-off. Samples are then loaded into a thermal evaporation chamber, which is evacuated to 15-30 mTorr before a 200 nm aluminum layer is deposited. Substrates are then soaked in acetone for 1 to 3 hours, whereupon they are ultrasonically agitated for 15-30 seconds, or until all excess aluminum is released. Samples are subsequently cleaned using acetone, isopropanol, and DI water and then placed in a dehydration oven for 30-45 minutes.

Prior to introducing this dehydration step, some ZTO TFT $\log(I_D\text{-}V)_{GS}$ transfer curves are found to have "kinks" and turn-on voltages ≤ -20 V, but otherwise normal characteristics beyond the threshold voltage, i.e. for $V_{GS} \geq 5$ V. Other ZTO TFTs show normal transistor action for $V_{GS} \geq 5$ V, but have I_D on-to-off ratios less than 100. After dehydration, turn-on voltages are significantly more positive (e.g., $V_{ON} \geq -10V$) and on-to-off ratios are typically 10^7 for working devices. The effect of the dehydration bake is ascribed to a desorption of water and organic species from the top channel surface since the insulator/channel interface is protected by the bulk of the channel and the source/drain contacts.

4.3 ZTO Process Development

4.3.1 Post-Etch Cleaning & Anneal

While final circuits are realized using an ITO/SiO_2 gate stack, most process development is accomplished using highly p-type doped silicon substrates (25 x 25 mm^2) with a thermally

grown 100 nm SiO_2 layer. While slight differences are noted between the two gate stacks for discrete transistor performance, all process trends appear to track between ITO/SiO_2 and Si/SiO_2 derived devices. Only discrete transistors can be measured on the silicon wafer coupons, so discrete transistor performance is used as the performance metric for development.

Electrical assessment is accomplished exclusively from $\log(I_D)$-V_{GS} transfer curves at V_{DS} = 1 V. The V_{GS} sweep is from -20 V to 40 V to -20 V in 0.5 V increments. V_{GS} is initially held at -20 V for 1 second and each subsequent data point is held for 0.2 seconds. All unbroken or uncontaminated substrates show I_D on-to-off ratios in excess of 10^7. Gate leakage in all measured transistors is neglible, owing to the excellent quality of the 100 nm thick thermal SiO_2 gate insulator. Samples found contaminated by photoresist or polymer residue either exhibit resistor-like behavior, or very negative turn-on voltages with a dramatic "kink" in their $\log(I_D)$-V_{GS} transfer curves.

Several iterations are conducted on Si/SiO_2 substrates to maximize mobility while maintaining a near-zero V_{ON} and an abrupt subthreshold swing. The via etch step is skipped in order to simplify process development and to reduce the number of confounding variables. The primary goal in this subsection is the removal of the hardened photoresist and polymer deposits from the channel surface after the ZTO etch. A two-step process is undertaken where substrates are first soaked in solvent to remove the bulk of the resist and are then placed in a RIE for a plasma ashing. Acetone is found to be an ineffective solvent for hardened photoresist removal, whereas photoresist stripper is found to work well. However, isolated islands of photoresist remain after 6 minutes of ultrasonic agitation in stripper. As a second step, an O_2/CHF_3/Ar, 100 watt, 200 mTorr plasma ash is found to be very effective at removing hardened photoresist and polymer, but it also etches exposed SiO_2 at too high of a rate. Instead, a 100 sccm O_2, 400 watt, 900 mTorr plasma ash is chosen as a preferred method to remove the final residue. Samples agitated in photoresist stripper and exposed to the oxygen plasma ash for at least 30 minutes measure smooth after cleaning, indicating either complete removal of the polymer film, or a thickness below the resolution of the profilometer.

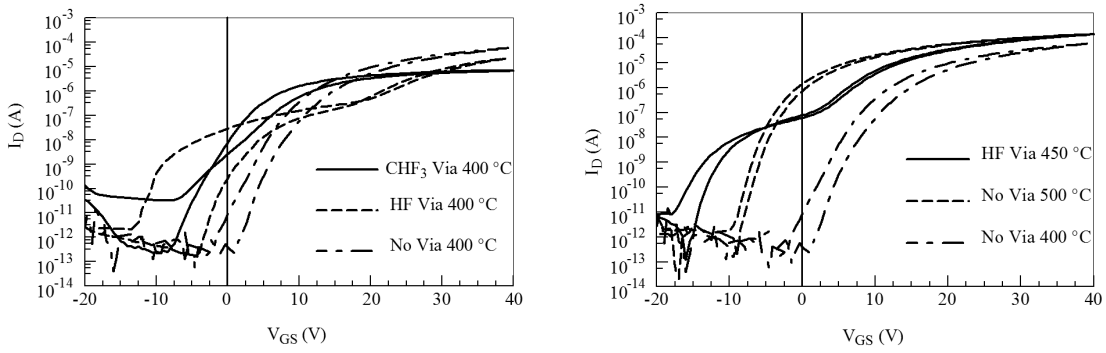
Another iteration of substrates is synthesized to examine the effect of deposition time (5 minutes versus 7), anneal temperature (400 °C versus 500 °C), and O_2 plasma ash duration (30 min. versus 60 min) on electrical performance. There appears to be no strong correlation between TFT performance and ash duration. Plasma exposure has a negative effect on ZTO TFT performance, and thus should be minimized as much as possible. There is no improvement in TFT devices by doubling the ash time from 30 minutes to 60 minutes, and substrates measure smooth after 30 minutes. Thus, further investigation into ash durations less than 30 min. is recommended. By finding the minimum necessary time to effectively remove all photoresist, the ZTO channel layer

is exposed to the least plasma exposure. Also, the power density of the O_2 ash is quite high (1.6 W cm^{-2}), so a reduction in power may lower plasma-derived channel surface damage. Like ash duration, sputter deposition time shows no significant effect on the TFT behavior.

Anneal temperature shows a significant effect on TFT performance, where 500 °C annealed transistors show a much higher mobility, equivalent I_D on-to-off ratios, a more abrupt subthreshold swing, and a more negative turn-on voltage than equivalent 400 °C annealed TFTs. TFTs annealed at 500 °C show improved consistency, but possess turn-on voltages centered around -10 V, which is too negative for most circuit applications. In contrast, substrates annealed at 400 °C exhibit near-ideal turn-on voltages centered around 0 V, but suffer from poor subthreshold swing and lower current drive capability. In a compromise between TFT performance and turn-on voltage, a 450 °C is preferred.

4.3.2 SiO_2 Via Etch Effects

The addition of the SiO_2 via etch step and subsequent cleaning causes a dramatic degradation in TFT performance. Figure 4.2 shows the effects of wet and dry via etching on Si/SiO_2 substrates. Wet-etched samples are submerged in buffered HF for 1 minute, whereas dry-etched substrates are placed in a 15 sccm CHF_3, 30 mTorr, 75 watt plasma for 5 minutes. Via-etched substrates are then cleaned with a 6 min ultrasonic agitation in photoresist stripper, followed by a 30 minute, 100 sccm O_2, 400 watt, 900 mTorr plasma ash.



(a) Via Etch, 400 °C Samples

(b) Via Etch 450 °C Annealed Sample

Figure 4.2: Via etch effects on I_D-V_{GS} transfer curves at V_{DS} = 1 V for ZTO circuit stacks. Buffered HF-etched samples are submerged for 1 minute, and the CHF_3-etched substrate is exposed to a 75 W plasma for 5 minutes. Processing is otherwise identical to the "No Via" samples. A 450 °C "No Via" sample is not produced, so the nearest two baseline substrates are provided. There is a significant change in the I_D-V_{GS} curves from the HF via etch, as a severe "kink" in the current response and a dramatic decrease in turn-on voltage.

In Fig. 4.2(a), substrates etched in a buffered HF solution and a CHF_3 plasma etch are compared to an unetched substrate. All three samples are annealed at 400 °C for 1 hour. Etched substrates exhibit more negative turn-on voltages than unetched substrates, along with a significant increase in hysteresis. CHF_3 plasma-etched transistors show clockwise hysteresis with an increase in the off-current on the return sweep due to an increase in gate leakage. The peak incremental and average mobilities are also much lower. HF wet-etched 400 °C TFTs exhibit a strong "kink" centered at 20 V and counter-clockwise hysteresis, but with gate leakages equivalent to the unetched substrate. Mobility also decreases slightly compared to unetched TFTs.

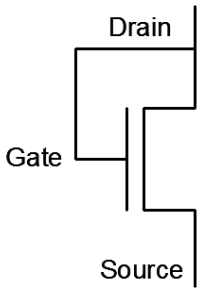
Figure 4.2(b) shows the curve for a HF wet-etched, 450 °C annealed substrate versus unetched 400 °C and 500 °C annealed substrates. The 450 °C, wet-etched sample has a peak incremental mobility of ~ 16 $cm^2V^{-1}s^{-1}$and an average mobility of ~ 7 $cm^2V^{-1}s^{-1}$, which is equivalent to the 500 °C unetched substrate, but the HF-etched sample suffers from a significant "kink" in its $\log(I_D)$-V_{GS} curve centered around 5 V and a much lower turn-on voltage. The significant "kink" does not dramatically affect the threshold voltage in this case, as the device is already well behaved by $V_{GS} = 5$ V.

The dramatic deleterious effects found from the SiO_2 via etch are determined to be a result of over-aggressive cleaning practices since similarly prepared samples employing a different photoresist clean step do not show these effects. While substrates presented herein are post-etch cleaned with a 6 minute ultrasonic agitation in photoresist stripper and a 30 minute oxygen plasma, later developments show a $\geq$30 minute soak in photoresist stripper followed by a 5 minute ultrasonic agitation to be superior in terms of TFT mobility, hysteresis, traps, and turn-on voltage. See Section 5.2.1 for more details.

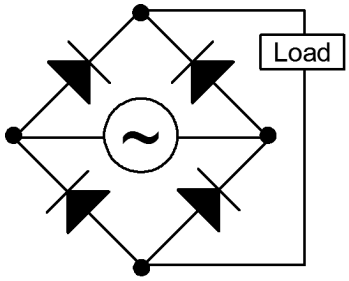
4.4 ZTO AC/DC Circuit Results

This section presents the output characteristics of bridge-tied and cross-tied AC/DC rectifier circuits synthesized using the process described in Section 4.2 to fabricate ZTO TFTs.

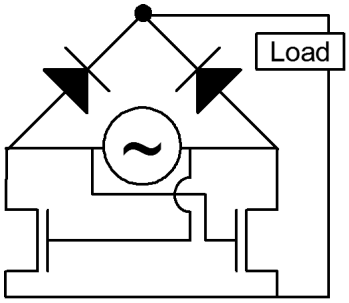
Figure 4.3 is a schematic of the the different circuits. A diode-tied transistor is a transistor with the gate and drain tied together, as seen in Fig. 4.3(a). The bridge-tied configuration of Fig. 4.3(d) uses four diode-tied transistors arranged into a bridge rectifier. In the bridge rectifier, T1 and T4 are both positively biased when node 1 is higher than node 2, and current flows through the load from node 3 to node 4. When node 2 is higher than node 1, T3 and T2 becomes positively biased, and again current flows through the load from node 3 to node 4.



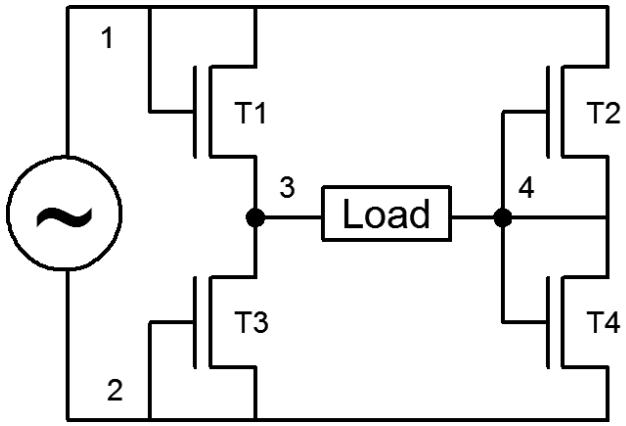
(a) Diode-tied transistor



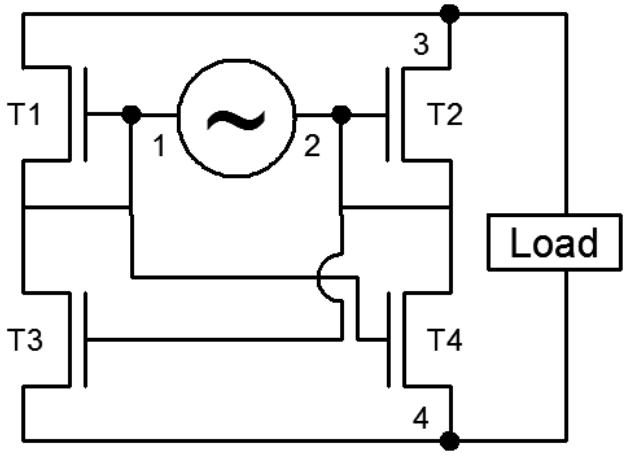
(b) Bridge-Tied Overview



(c) Cross-Tied Overview



(d) Bridge-Tied Circuit

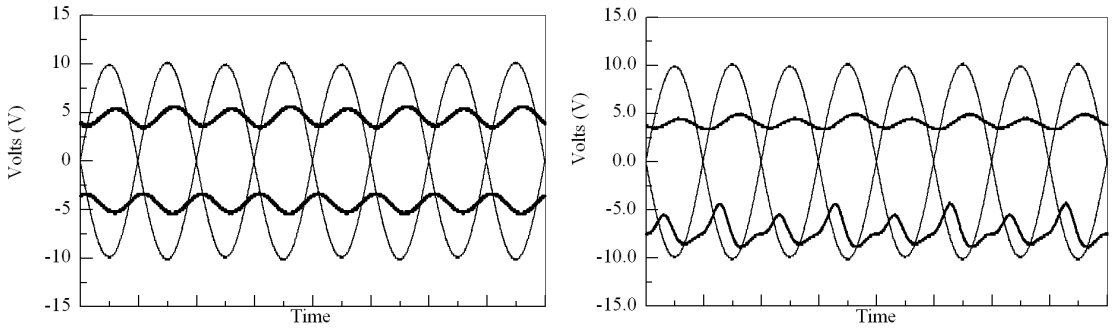


(e) Cross-Tied Circuit

Figure 4.3: Circuits schematics for (a) a diode-tied transistor, (b) a bridge rectifier using diode-tied n-type TFTs, and (c) a cross-tied rectifier using n-type TFTs. Figures (d) and (e) are the transistor level equivalent of (b) and (c), respectively. By tying the drain to the gate, a TFT exhibits 2-terminal diode-like I-V behavior, where current only flows from the drain to the source.

The cross-tied configuration uses two diode-tied transistors in the top portion of the circuit, but the gates of the bottom transistors are tied to the sources of the opposite diode-tied transistor. As shown in Fig. 4.3(e), the bottom two transistors are no longer diode-tied, but rather are connected to the opposite side of the differential voltage source. Thus, V_{GS} is the full differential voltage, and the transistor is driven hard into saturation, since $V_{GS} = 2V_{DS}$, lowering the voltage drop across the channel. Thus, a higher fraction of the differential source's potential is dropped across the load.

All circuits presented herein use TFTs with a W/L of 10 in order to compare to equivalently fabricated IGO-based circuits reported by McFarlane [66], as the mask set is the same. Circuits are measured using an active probe setup which loads the circuit with a 2 MΩ, 0.05 pF load. Figure 4.4 shows waveforms for ZTO-based TFT rectifier circuits using both a cross-tied and a bridge-tied configuration. The bridge-tied circuit operates as expected, where the positive and negative rails are symmetric and the ripple follows the input rails exactly. Voltage drop across the diode-tied transistors is slightly greater than the threshold voltage of the transistors, and each transistor drops ∼5 V. The cross-tied transistors on the lower rail do in fact operate at lower voltages, as shown by the lower rail's proximity to the input signal.



(a) ZTO Bridge-Tied Output, 1 MHz

(b) ZTO Cross-Tied Output, 1 MHz

Figure 4.4: 1 MHz waveforms for bridge-tied and cross-tied ZTO-channel circuits with a W/L ratio of 10. A capacitor in parallel with the load would serve to reduce ripple in the output.

The $\log(I_D)$-V_{GS} transfer curves of discrete TFTs measured on a circuit substrate are shown in Fig. 4.5. It is assumed that the discrete and integrated TFTs behave the same. These discrete transistors suffer from a poor subthreshold slope, a "kink" centered around $V_{GS} = 3$ V, and low mobility. A sharper subthreshold slope would lower the threshold voltage dramatically, which would improve circuit operation by lowering the diode-tied transistor voltage drop. The extrapolated threshold voltage is 5.5 V, which correlates well to the voltage drop witnessed by the circuit performance shown in Fig. 4.4. The highly negative turn-on voltage is likely related to the "kink",

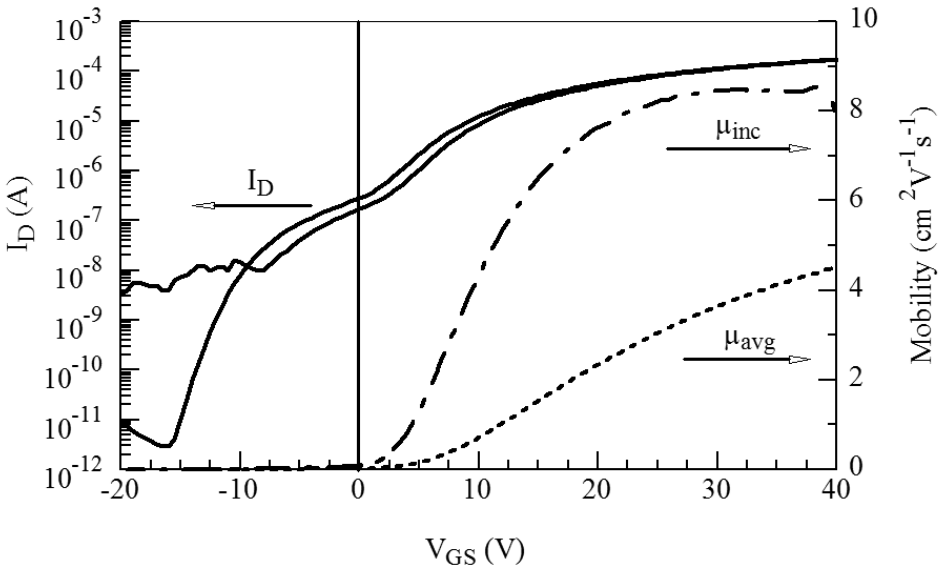


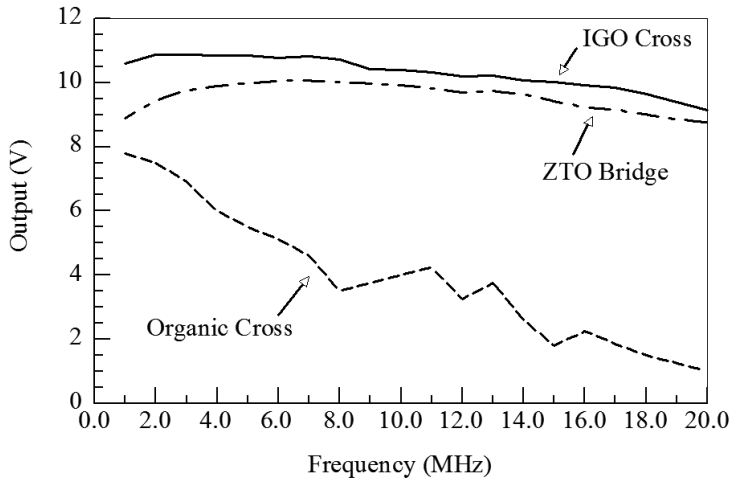
Figure 4.5: Discrete TFT log(I_D)-V_{GS} transfer curve at $V_{GS} = 1$ V on the final circuit substrate. The peak incremental mobility and average mobility are 7.9 and 4.5 $cm^2V^{-1}s^{-1}$, respectively, and the turn-on voltage is -15 V

which is usually ascribed to acceptor-like traps [29], and is likely due to non-optimal cleaning and plasma ash damage. TFT hysteresis is clockwise, indicating electron trapping, rather than ion migration. The high off-current on the return sweep is due to gate leakage. The gate insulator begins breaking down at a $V_{GS} = 30$ V on the forward sweep and gate leakage does not appreciably decrease on the return sweep (i.e., dielectric does not recover). Fortunately, the maximum potential measured across the insulator of an integrated circuit TFT is 20 V, so that the dielectric remains stable. Multiple TFTs on this substrate show similar I_D-V_{GS} performance.

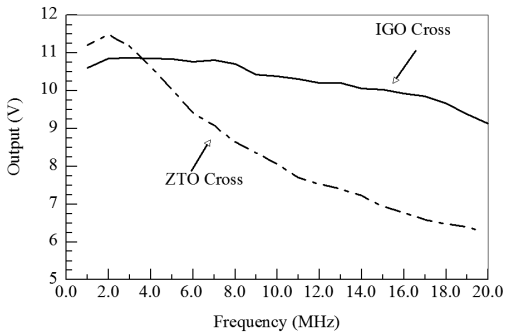
Figure 4.6(a) shows an output comparison between IGO, ZTO, and organic TFT-based AC/DC rectifiers. The IGO circuits, presented by McFarlane [66], are synthesized using the same mask set, so this comparison is truly between materials and their respective processes. Comparing cross-tied configurations in Fig. 4.6(b), the IGO-based circuit maintains a higher output over the measured range of frequencies, since the ZTO cross-tied transistors fail to keep up at higher frequencies. The cross-tied ZTO TFTs likely suffer from gate leakage. Since these TFTs are not switching, the lower rail floats up to effectively 0 V. The ZTO bridge circuit, as seen in Fig. 4.6(c) has a much higher output across the frequency range than the IGO circuit, likely due to a significantly lower threshold voltage (5.5 V versus ∼6.5 V).

Both AOS-based materials are capable of higher output voltages than the organic TFT-based circuit, as seen in Fig. 4.6(a). The IGO cross-tied circuit slightly outperforms the ZTO

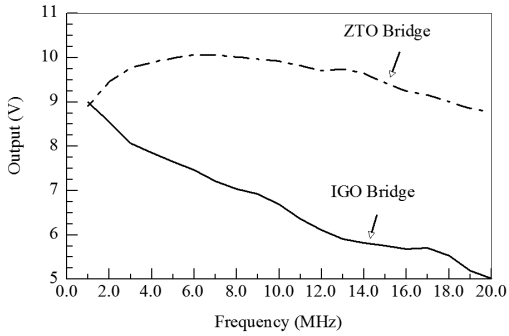
bridge circuit. Both AOS circuits are capable of rectifying a 13.56 MHz signal for applications involving AC/DC power conversion at RF frequencies.



(a) ZTO Bridge vs. IGO Cross vs. Organic Cross



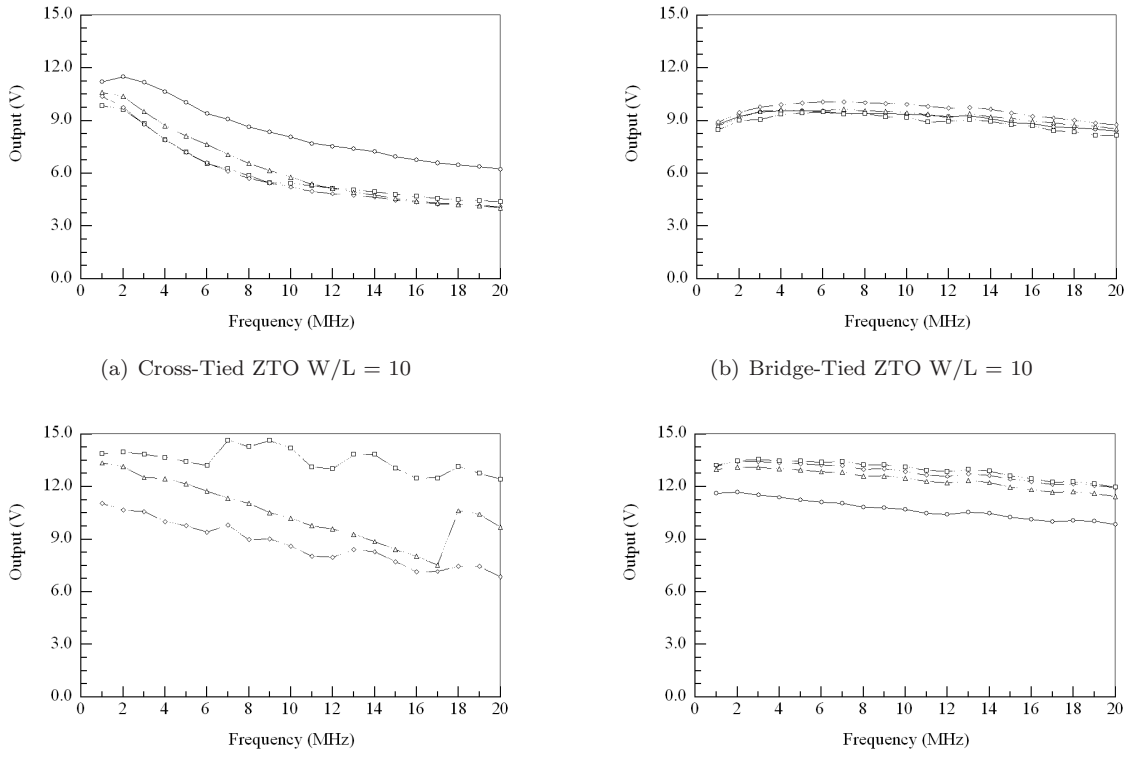
(b) W/L=10 Cross Circuits



(c) W/L=10 Bridge Circuits

Figure 4.6: Output voltage versus frequency for IGO and ZTO AC/DC rectifier circuits using both cross-tied and bridge-tied configurations into a 0.05 pF, 2 MΩ load. The cross-tied organic-based transistor curve is normalized to an equivalent 20 V_{p-p} input signal, which is applied to the IGO and ZTO circuits [71]. The W/L ratios of the IGO, ZTO, and organic TFT-based circuits are 10, 10 and 48, respectively.

Sixteen individual circuits are tested on a single substrate to determine yield and consistency. Figure 4.7 shows frequency-output curves for 15 circuits, since one of the W/L = 100 cross-tied circuits failed. The failed circuit, a W/L = 100 cross-tied circuit suffered from a severe transistor mismatch or a gate leakage problem. Circuits with higher W/L ratios exhibit higher output voltages, due to their higher drain current drive. Only the larger cross-tied circuit exhibits a high output variance. The consistency across the 25 x 25 mm^2 substrates is promising, especially given that this is the first report of an operational ZTO circuit.



(a) Cross-Tied ZTO W/L = 10

(b) Bridge-Tied ZTO W/L = 10

(c) Cross-Tied ZTO W/L = 100

(d) Bridge-Tied ZTO W/L = 100

Figure 4.7: ZTO TFT AC/DC rectifier circuit-to-circuit output consistency across a single substrate for both cross-tied and bridge-tied configurations using W/L = 10 and W/L = 100. Out of the 16 circuits tested on this one substrate, 15 of them demonstrated rectification.

4.4.1 Conclusion

In this chapter, the development and characterization of ZTO TFT AC/DC rectifier circuits is discussed. A plasma etch study using an Ar/CH_4 gas stream of varying gas compositions is investigated for polycrystalline ITO, and for three AOS materials, IGZO, IGO, and ZTO. From this study a first-order ZTO etch recipe is devised for process integration. A cleaning process is developed to remove hardened photoresist after ZTO plasma etching. The effect of the SiO_2 via etch step, where a number of non-idealities are introduced, is electrically characterized. The first reported to date ZTO TFT circuits are fabricated using the techniques developed in this chapter. These bridge- and cross-tied AC/DC rectifier circuits demonstrate similar performance to that of equivalent IGO rectifiers.

5. ZTO TFT ENHANCEMENT/DEPLETION-MODE INVERTERS

This chapter discusses the development of high-gain ZTO-based enhancement/depletion-mode (E/D) inverters for digital logic circuits using n-type only AOS materials. Further development of ZTO-based integrated circuit processing is also reported. Several novel deposition schemes to achieve enhancement-mode (E-mode) and depletion-mode (D-mode) bottom-gate TFTs using a single ZTO sputter target are examined. Finally, the first AOS-based E/D inverter is demonstrated.

5.1 Basic E/D Inverter Electrical Behavior

Figure 5.1 shows the basic schematic for an n-type E/D inverter. The electrical operation of the inverter is rather simple, with the upper D-mode load transistor acting effectively as a current source load for the lower E-mode drive transistor. The load transistor always operates at $V_{GS} = 0$ V since the gate and source are tied together, and the drive transistor operates at either $V_{GS} = V_{GND}$ or $V_{GS} = V_{DD}$, except for the short time that V_{IN} is in transition. The design allows the output high (V_{OH}) to reach V_{DD} and the output low (V_{OL}) to approach the lower rail voltage. V_{OL} is ultimately limited by the ability of the E-mode transistor to sink the current source at a low V_{DS}. Please refer to B. McFarlane's M.S. Thesis for more information on inverter operation in the context of AOS TFTs (i.e., IGO is used as a channel layer) [66].

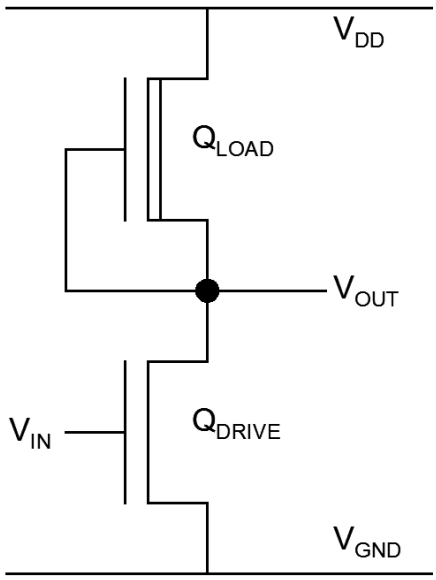


Figure 5.1: n-type enhancement-mode/depletion-mode (E/D) inverter schematic. The upper D-mode "load" transistor's gate is tied its source, thus providing a dynamic load (current source) to the lower E-mode "drive" transistor. An E/D inverter offers high gain (≥10-15 V/V) while maintaining a simple, 2 transistor design. To pull the output voltage low, the E-mode driver TFT must sink current delivered from both the current source and the load attached to V_{OUT}.

5.2 ZTO-Based Circuits Process Development

5.2.1 Improved Cleaning Procedures

Carrying on from the ZTO development presented in Chapter 4, a more robust fabrication process is realized. The most significant change in processing is the post-photolithographic patterning cleaning procedure. The Ar/CH_4 etch steps used in the fabrication of ZTO circuits is quite punishing to the photoresist, necessitating the use of an aggressive hard bake, which makes the resist more difficult to remove. Instead of ultrasonically agitating substrates in photoresist stripper for 6 minutes and O_2 ashing for 30 minutes, as proposed in Chapter 4, the new procedure involves merely soaking the substrates in the stripper for at least 30 minutes, followed by a 5 minute ultrasonic agitation. Samples are then thoroughly rinsed with DI water and either placed on a 85 °C hotplate for 10 minutes or loaded into a 125 °C oven overnight, depending on whether further processing is to be accomplished immediately after cleaning. No measured effect on transistor performance from different dehydration schemes is observed. The new cleaning method is developed as a consequence of testing several samples with decreasing ash power and duration. As the ash time is decreased, an improvement in device performance is observed. Ultimately, it was concluded that the best process is to remove the ash step entirely.

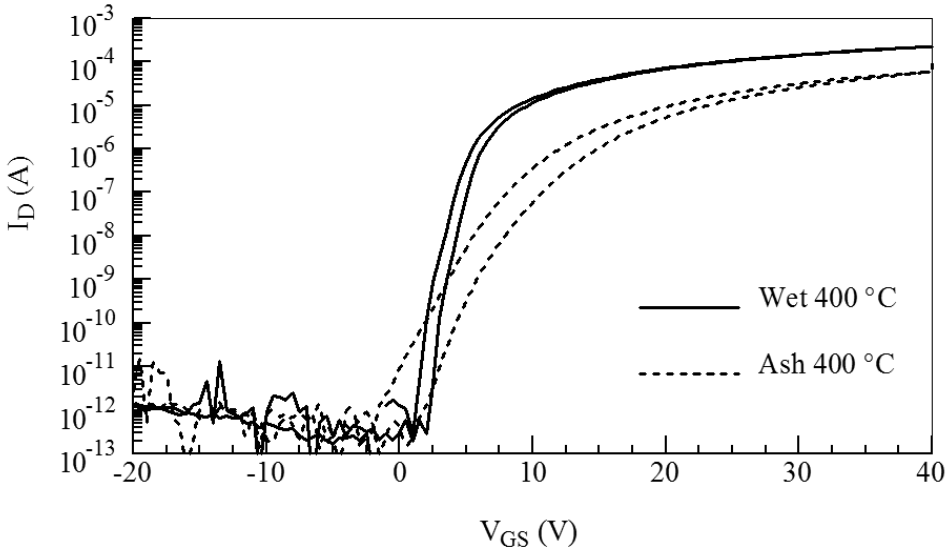


Figure 5.2: I_D-V_{GS} transfer curves at $V_{DS} = 1$ V for wet photoresist strip versus oxygen plasma ash. While the turn-on voltages of the two samples are nearly the same, the "Wet 400 °C" device possesses a significantly improved subthreshold swing and mobility compared to that of the "Ash 400 °C".

Figure 5.2 shows I_D-V_{GS} transfer curves for both a chemical photoresist strip sample and a O_2 plasma-ashed sample . The "Wet 400 °C" sample is soaked in 1165 photoresist stripper for ≥30 minutes and then ultrasonically agitated for 5 minutes while the "Ash 400 °C" substrate is ultrasonically agitated in photoresist stripper for 6 minutes without prior soaking and O_2 plasma-ashed at 400 W in a 900 mTorr ambient for 60 minutes. By soaking substrates in photoresist stripper for longer than 30 minutes, the photoresist is completely removed, as confirmed by profilometry. Thus, O_2 plasma-ashing is deemed unnecessary. The "Wet 400 °C" substrate also experiences two more photolithography steps than the "Ash 400 °C" sample: a ZTO lift-off deposition and a SiO_2 via etch before annealing. The via etch step and clean is shown to degrade performance, as discussed in Section 4.3.2.

The non-ashed sample clearly shows an improvement of ∼ 4x in subthreshold swing (0.44 V/decade versus 1.78 V/decade), a ∼ 3x increase in incremental mobility (23 $cm^2V^{-1}s^{-1}$ versus 8.4 $cm^2V^{-1}s^{-1}$) and a ∼ 4x gain in average mobility (18 $cm^2V^{-1}s^{-1}$ versus 4.3 $cm^2V^{-1}s^{-1}$). Clearly the pure chemical strip process is superior to the strip/ash process employed previously. The degradation of the strip/ash process is attributed to the high power of the ash plasma. If the ZTO AC/DC rectifier from Chapter 4 is used as a component in a RFID circuit, its performance should be greatly improved using the new ZTO integration process.

5.2.2 E/D Channel Development

The processing steps for E/D inverter circuits are nearly identical to those given in Section 4.2, with an additional sputter deposition and patterning step. The basic steps for the full circuit stack is gate stack synthesis, ZTO deposition 1, channel patterning 1, ZTO deposition 2, channel patterning 2, via etch, anneal, and source/drain lift-off. The ultimate goal of this project is to simultaneously synthesize both an enhancement-mode bottom-gate ZTO TFT with a turn-on voltage of ∼0 V and a depletion-mode bottom-gate ZTO TFT with a turn-on voltage approximately -5 V on a single substrate using a single target and one anneal step.

Preserving the channel-insulator interface is one of the most important aspects of TFT fabrication, since the majority of transistor action occurs within approximately 1-3 nm of this interface. The best ZTO TFT results are obtained by sputter depositing onto a pristine as-deposited or as-grown insulator surface. The channel-insulator interface of a second ZTO channel deposition is not expected to be as ideal as the first ZTO deposition due to photoresist contamination, sputter damage, plasma damage, and/or incomplete cleaning of the insulator surface. The second channel deposited is expected to suffer from lower mobility, an extreme turn-on voltage ($V_{ON} \leq -20$ V or $V_{ON} \geq 20$ V), and a large density of interface traps.

Using a single target composition, turn-on voltage is modulated through a combination of deposition conditions, plasma treatment, channel thickness, and anneal parameters. Since a single anneal is used, the difference in the E-mode and D-mode TFT's turn-on voltage is established during the channel deposition. Different deposition strategies are tried in order to find the best compromise between TFT performance (mobility, hysteresis/traps, and subthreshold swing) and realizing E-mode and D-mode turn-on voltages of 0 V and ∼-5 V, respectively. The four depositions schemes proposed are plasma-treated (Fig. 5.3), depletion-first (Fig. 5.4), enhancement-first (Fig. 5.5), and dual channel-first (Fig. 5.6).

For the development work of this section E-mode transistors are deposited at 75 W in a 90/10 Ar/O_2, 5 mTorr atmosphere whereas the D-mode transistors are deposited at 100/0 Ar/O_2 to decrease their turn-on voltage [55]. The anneal remains constant at 400 °C for 1 hour. Table 5.1 summarizes the basic TFT performance metrics for E/D circuit blocks synthesized on p-type silicon substrates with a thermally-grown 100 nm thick SiO_2 layer for the four different deposition schemes. Lift-off patterning of the enhancement channel was not attempted since the appropriate mask was not acquired.

5.2.2.1 Argon Plasma Treatment

Samples "1DC" and "2DC" from Table 5.1 are exposed to an argon plasma treatment in a RIE, as seen in Fig. 5.3. By establishing both the E-mode and D-mode channel in the first deposition, a near-ideal channel-insulator interface is hopefully preserved. The plasma treatment is motivated by a paper by Park *et al.*, where IGZO channels exposed to an Ar plasma for 30 seconds are found to exhibit a higher channel conductivity and a lower threshold voltage [72]. The D-mode channel on the substrate "1DC" is exposed to a 1 minute, 0.6 W/cm^2, 10 mTorr Ar plasma, and exhibits dramatically lower turn-on voltage of -17 V, but so does the photoresist masked E-mode device. "2DC" is identically processed except that the duration of the Ar plasma is 5 minutes. It shows a much higher turn-on voltage of -1 V, which is not expected but is likely a processing error. While successful channel conductivity and turn-on voltage modulation is realized using an Ar plasma treatment, further experiments are not pursued, since there is no V_{ON} separation between the E-mode and D-mode TFTs.

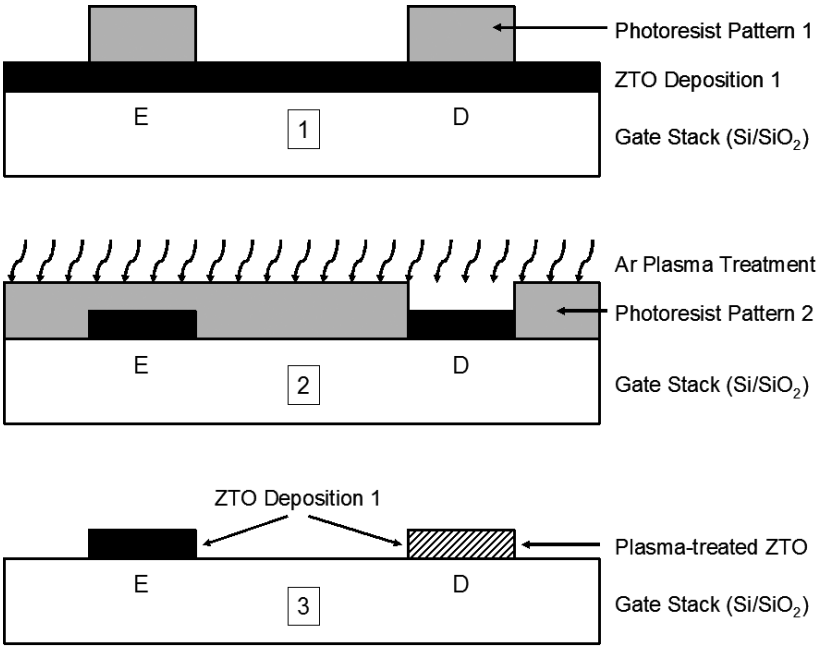


Figure 5.3: Argon plasma treatment fabrication scheme for an E/D inverter. Cross-section [1] shows the stack after ZTO sputter deposition and photoresist etch mask patterning. In [2] the ZTO is patterned and the D-mode lift-off photoresist mask is applied. An argon plasma treatment is accomplished to push the turn-on voltage of the D-mode TFT more negative. Cross-section [3] shows the transistor before source/drain liftoff.

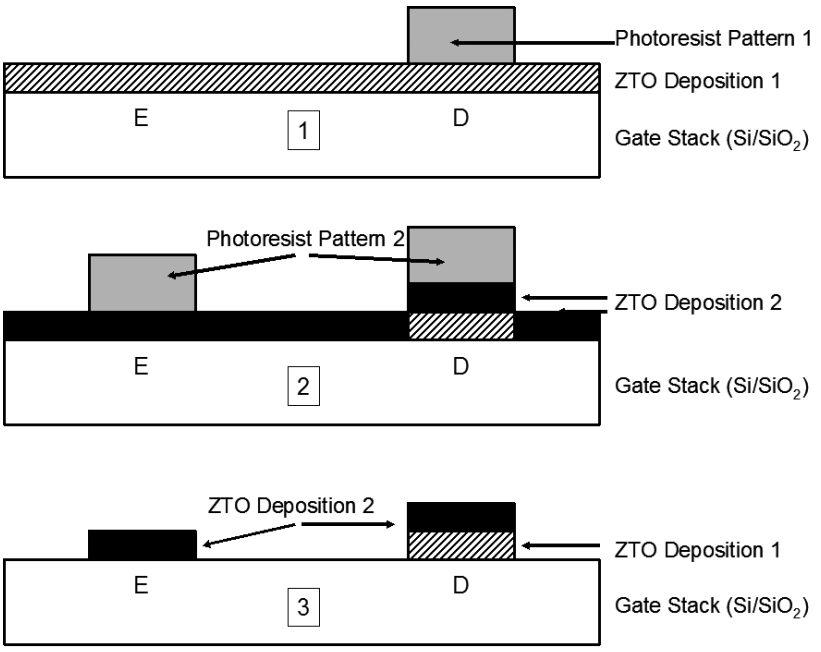


Figure 5.4: Depletion-first fabrication scheme for an E/D inverter. A ZTO channel sputter deposition is accomplished and the D-mode channel is etch masked in [1]. Cross-section [2] is after the first ZTO patterning, a second ZTO deposition, and a dual-channel etch mask is applied. The second ZTO etch step is completed and the photoresist mask is stripped in [3].

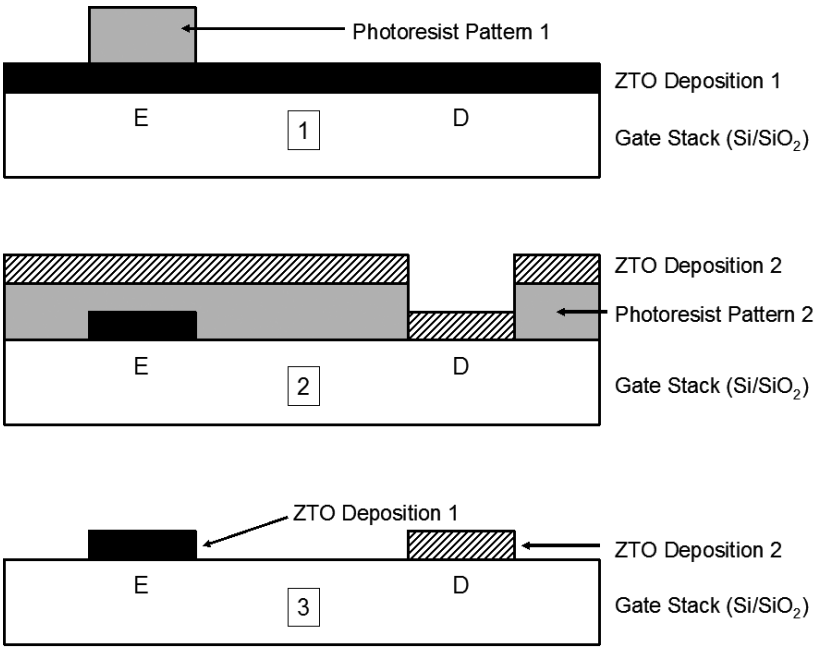


Figure 5.5: Enhancement-first fabrication scheme for an E/D inverter. In cross section [1] a ZTO channel layer is sputter deposited and the E-mode channel etch mask is patterned. Cross-section [2] is after the E-mode ZTO channel etch, the D-mode lift-off mask application, and the second ZTO deposition. The stack in [3] is after the D-mode channel lift-off.

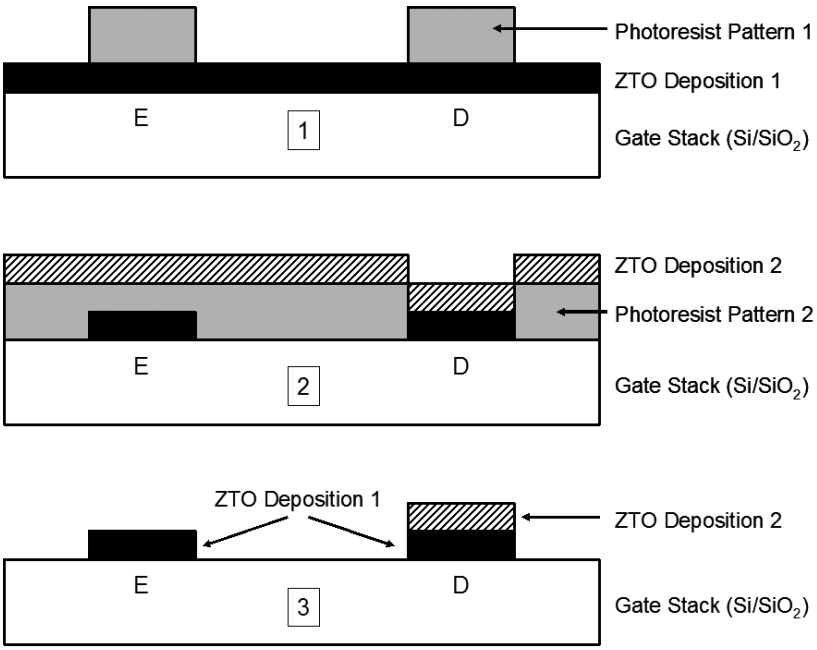


Figure 5.6: Dual channel-first fabrication scheme for an E/D inverter. A ZTO sputter deposition is accomplished, followed by a dual channel etch mask in [1]. For [2], the ZTO channels are etched, a D-mode lift-off mask is patterned, and a second ZTO layer is deposited. The second ZTO layer is lifted off, leaving cross-section [3].

ID	Mode	V_{ON}	μ_{inc}	μ_{avg}	S ($\frac{V}{dec}$)	Deposition 1	Pattern 1	Deposition 2	Pattern 2	Via Etch
Figure 5.3 deposition process										
1DC	E	-17	25.48	14.46	3.08	90/10, 75W, 8'	Dual Channel Etch	Ar Plasma 1'	Depletion Lift-Off	None
1DC	D	-17	20.43	12.91	2.76					
2DC	E	-1	22.47	15.23	0.58	90/10, 75W, 8'	Dual Channel Etch	Ar Plasma 5'	Depletion Lift-Off	None
2DC	D	-1	21.27	16.39	0.55					
Figure 5.4 deposition process										
1DE	E	6.5	13.61	10.24	0.58	100/0, 75W, 8'	Depletion Etch	90/10, 75W, 8'	Dual Channel Etch	None
1DE	D	-4	22.93	16.23	1.44					
Figure 5.5 deposition process										
1EE	E	-1.5	22.71	16.52	0.65	90/10, 75W, 8'	Enhancement Etch	100/0, 75W, 8'	Depletion Lift-Off	None
1EE	D	6.5	9.50	7.97	0.52					
EDA	E	-0.5	20.88	16.65	0.48	90/10, 75W, 8'	Enhancement Etch	100/0, 75W, 8'	Depletion Lift-Off	After Anneal
EDA	D	3	6.37	4.78	0.70					
EDB	E	1.5	23.15	17.10	0.49	90/10, 75W, 8'	Enhancement Etch	100/0, 75W, 8'	Depletion Lift-Off	Before Anneal
EDB	D	6.5	6.19	4.54	0.56					
Figure 5.6 deposition process										
DCA	E	0.5	23.01	18.05	0.44	90/10, 75W, 8'	Dual Channel Etch	100/0, 75W, 8'	Depletion Lift-Off	After Anneal
DCA	D	-1.5	22.58	17.76	0.68					
DCB	E	1.5	23.20	16.79	0.58	90/10, 75W, 8'	Dual Channel Etch	100/0, 75W, 8'	Depletion Lift-Off	Before Anneal
DCB	D	-1	24.05	18.22	0.63					

Table 5.1: Processing parameters and resulting transistor performance metrics for E/D inverter synthesis. All sputter runs above are from a 2 inch diameter ZTO (2:1) target at 75 watts in a 5 mTorr ambient. These depositions are presputtered for 10 minutes at 75 watts in a 5 mTorr, 90/10 Ar/O_2 atmosphere. For the 100/0 Ar/O_2 runs, the oxygen is removed immediately before the substrate is exposed to the plasma. Two 25 x 25 mm^2 substrates are loaded into the sputter system simultaneously and the substrate holder is translated during deposition to improve ZTO channel thickness uniformity. All substrates above are annealed at 400 °C for 1 hour using a 5 °C/min ramp rate. The "Dual Channel" mask is used to protect both the enhancement-mode channel and the depletion-mode channel during etching. Any lift-off patterning occurs before the deposition. The SiO_2 via is either omitted, etched before the anneal, or etched after the anneal. For "1DC" and "2DC", the second deposition is replaced with a Ar plasma treatment (10 mTorr, 0.6 W/cm^2) in a RIE.

5.2.2.2 Depletion-First Deposition

As seen in Fig. 5.4, by depositing the D-mode channel first, "1DE" from Table 5.1 exhibits a near-specification turn-on voltage for the D-mode transistor of -4 V. Unfortunately, subsequent deposition of the E-mode channel results in a significant decrease in mobility and too high of a turn-on voltage. The E-mode transistor on "1DE" also shows significant hysteresis in its I_D-V_{GS} curve. This non-ideal E-mode transistor behavior is attributed to insulator-channel interface states created during the deposition, etching, and/or cleaning of the first channel layer. While the D-mode transistor is effectively ideal for this circuit, this scheme is abandoned due to poor quality of the more-critical E-mode transistor performance.

5.2.2.3 Enhancement-First Deposition

The substrates "1EE", "EDA", and "EDB" (Table 5.1) are synthesized from the enhancement channel-first scheme shown in Fig. 5.5. "1EE" experiences no via etch, while the via-etch for "EDA" occurs after the anneal, and the via-etch for "EDB" is accomplished before the anneal. TFT characteristics are quite similar between the three substrates, with minor variations in turn-on voltage likely due to operator variability in the process. The etch-after-anneal TFT ("EDA") exhibits a slightly lower mobility and a more negative turn-on voltage than the "EDB" TFT, indicating that some via etch damage is mitigated during the anneal. All three enhancement-first substrate's depletion channels (i.e., "1EE", "EDA", and "EDB") exhibit similar high turn-on voltages and degradation in mobility and subthreshold swing. These effects are likely due to insulator surface damage during the first channel deposition and patterning. Although a rather large amount of clockwise hysteresis is noted in D-mode transistors, the highly negative turn-on voltages and severe "kinks" in $\log(I_D)$-V_{GS} transfer curves observed in Chapter 4 are not found in these samples.

5.2.2.4 Dual-Channel Deposition

Figure 5.6 illustrates deposition and patterning steps for the fabrication of "DCA" and "DCB" (Table 5.1). Both E-mode and D-mode ZTO layers remain after the first channel deposit and pattern step. A second, more conductive channel is then patterned and deposited via lift-off on top of the existing depletion channel in order to move the turn-on voltage more negative without negatively affecting the channel-insulator interface. Thus, both E-mode and D-mode TFTs should exhibit similar high mobilities and abrupt subthreshold swings with a difference only in turn-on voltage.

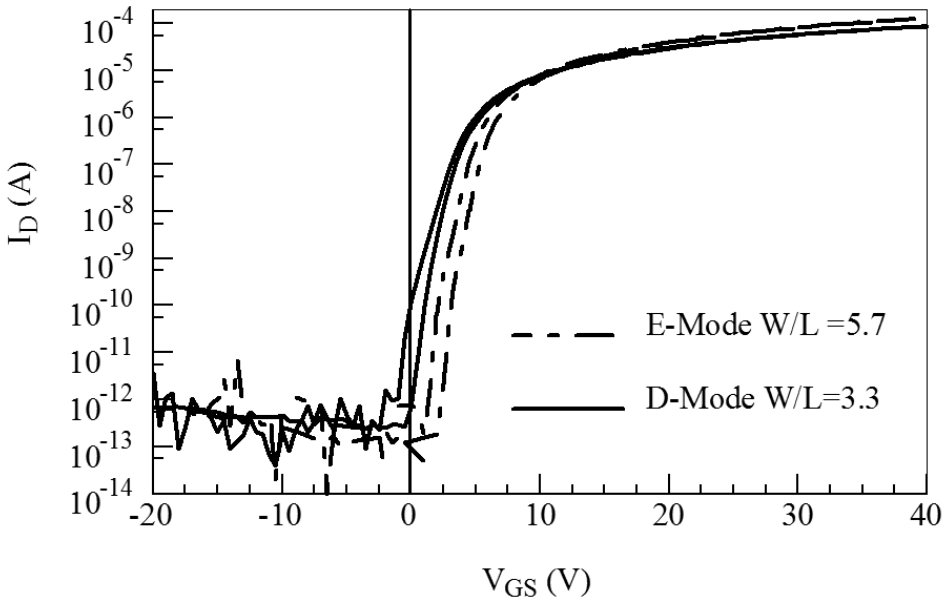


Figure 5.7: E-mode and D-mode TFT log(I_D)-V_{GS} transfer curves for a dual channel-first substrate "DCB" (i.e., Fig. 5.6. Processing parameters and TFT metrics for these devices are given in Table 5.1. E-mode and D-mode transistors turn-on voltages are 1.5 V and -1 V, respectively. Mobilities are the same between samples and the subthreshold swing of the E-mode transistor is sharper than that of the D-mode transistor.

As noted in Table 5.1 the mobility of both channels in "DCA" and "DCB" are nearly the same and the turn-on voltages of the D-mode transistors are $\sim$ 2 V less than the E-mode transistors. Figure 5.7 shows the log(I_D)-V_{GS} transfer curves for discrete TFTs on substrate "DCB". The subthreshold swings of the E-mode transistors are less than the D-mode transistors, as expected. Both E-mode and D-mode TFTs exhibit good transistor behavior and the turn-on voltage of the enhancement-mode transistor is nearly ideal for this inverter circuit application. A more negative turn-on voltage for the D-mode TFT is necessary for the current source however.

5.2.2.5 Conclusions

Despite problems noted in Section 5.2.2.3, either the depletion-first (Fig. 5.4) or the enhancement-first (Fig. 5.5) deposition schemes are likely to result in the best E/D process. The greatest demerit associated with these two deposition schemes is the damage to the insulator surface after the first channel deposition and patterning. With sufficient development and appropriate equipment, an optimized ZTO etch recipe and subsequent cleaning process could be designed such that the dielectric surface is returned to a pristine condition before the second channel deposition. Since the two channels are deposited separately, the sputter recipes for each channel could be individually optimized to yield the desired turn-on voltages. If this surface cleaning issue can

be successfully addressed, the enhancement-first and the depletion-first schemes would offer more processing flexibility than the dual-deposition scheme.

While the extra-thick depletion channel layer in the dual-channel deposition scheme (Fig. 5.6) yields a larger volume of free electrons, the channel material nearest to the channel-insulator interface electrically shields the rest of the bulk channel from significant gate-modulated conduction. Therefore, the sputtering conditions of the second channel do not have too strong of an influence on the turn-on voltage of the D-mode TFT, since free electrons present in the upper portion of the channel are not drawn strongly to the interface, where channel conduction primarily occurs. Subthreshold swing increases slightly as a result of the loss of gate control of channel electrons remote from the interface. Therefore, the dual-channel deposition scheme presented here compromises on the ability to separate E-mode and D-mode TFT turn-on voltages by more than ∼5-7 V in order to reduce process complexity and maintain channel-insulator interface quality.

Within the scope of the results shown in Table 5.1, the use of a second channel deposition on top of the ZTO channel (Fig. 5.6) to modulate the turn-on voltage shows the best performance of the schemes investigated. The final ZTO E/D inverters on the ITO/SiO_2 gate stack use a modified form of the process flow from "DCB", as described in the next section.

5.3 ZTO E/D Inverter Results

5.3.1 Final Process Optimization & TFT Results

Process	**Substrate "EDB" (Si/SiO_2)**	**E/D Inverter Stack (ITO/SiO_2)**
Deposition 1	8', 90/10 Ar/O_2, 75 W	8', 90/10 Ar/O_2, 50 W
Pattern 1	Dual Channel Etch	Dual Channel Etch
Pattern 2	D-Mode Liftoff	D-Mode Liftoff
Deposition 2	8', 100/0 Ar/O_2, 75 W	8', 100/0 Ar/O_2, 88.5 W
Via Etch	1' Buffered HF	45 s Buffered HF
Anneal	400 °C 1 h.	450 °C 1 h.
V_{ON} E/D	1.5 / -1 V	-3 / -8.5 V

Table 5.2: Process parameters for test substrate "EDB" and the E/D inverter stack.

Motivated by the 3 V separation in turn-on voltage between the E-mode and D-mode TFTs developed in "DCB" from Section 5.2.2, the final circuits use different ZTO deposition parameters. The ultimate goal is to have D-mode and E-mode TFTs with turn-on voltages of approximately -5 V and -1 V, respectively. Therefore, both transistors need to be made more conductive. In order to increase the turn-on voltage difference, the first ZTO sputter run (E-mode) is reduced in power from 75 W to 50 W. The second deposition (D-mode) is increased to 88.5 W from 75 W.

The presputter for the second ZTO sputter run is changed to 90/10 Ar/O_2 for 5 minutes and pure argon for an additional 5 minutes (5' 90/10 Ar/O_2 + 5' 100/0 Ar/O_2). The presputter recipe for "DCB" is 10 minutes in 90/10 Ar/O_2. The anneal is also increased from 400 °C to 450 °C for 1 hour. The PECVD SiO_2 gate insulator is deposited in-house instead of at HP, as discussed in Chapter 4. The final process flow is described in Appendix A.

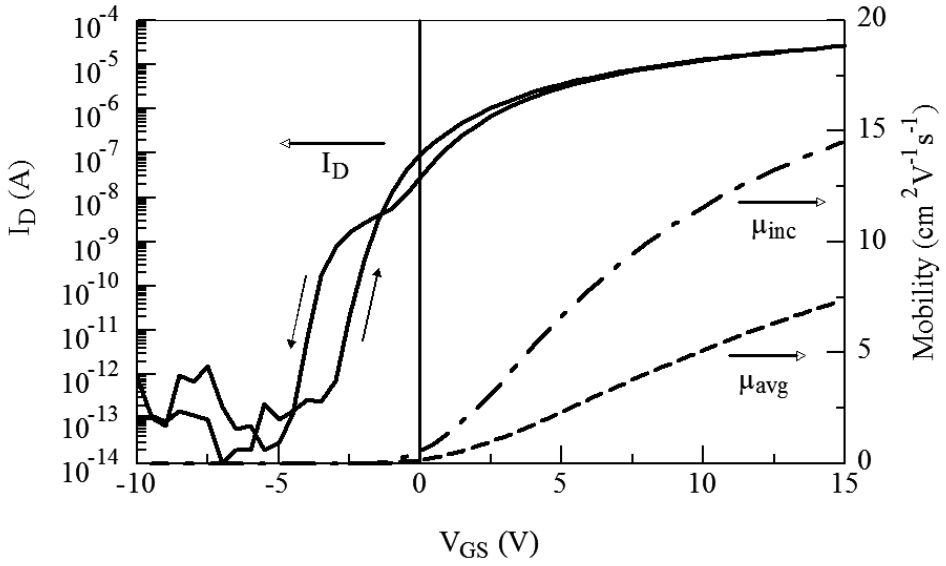


Figure 5.8: Integrated circuit E-mode TFT $\log(I_D)$-V_{GS} transfer curves and mobility plots. The integrated circuit transistor is swept between $-10 \leq V_{GS} \leq 15$ V. The positive sweep behavior of the E-mode TFT is relatively trap-free but the negative sweep appears to be likely affected by acceptor-like traps, as evident from the presences of the "kink" at $V_{GS} = -1$ V in the $\log(I_D)$-V_{GS} curve. The counter-clockwise hysteresis present in I_D below the "kink" is likely due to the unintended presence of mobile ions.

The lower-power first deposition nominally increases V_{ON}. This V_{ON} increase is due to both a decrease in the ZTO channel layer thickness and also a to reduction in the electron concentration in the ZTO channel [55]. An increase in RF power in the second deposition is used to further decrease the D-mode TFT turn-on voltage. The post-deposition anneal temperature is increased in order to reduce the turn-on voltage of both the D-mode and the E-mode TFT to that corresponding to the specification (-6 V and -1 V, respectively). The higher anneal temperature also yields TFTs with higher mobilities and reduced trap-related problems.

Figure 5.8 shows the $\log(I_D)$-V_{GS} and mobility curves for an integrated circuit E-mode TFT. While the positive sweep appears to be relatively trap-free, the negative sweep exhibits a distinct "kink" in the $\log(I_D)$-V_{GS} curve around $V_{GS} = -1$ V. Counter-clockwise hysteresis below the "kink" is attributed to mobile ion drift, likely from surface contamination during processing. D-mode TFTs do not exhibit counter-clockwise hysteresis, but show a "kink" associated with

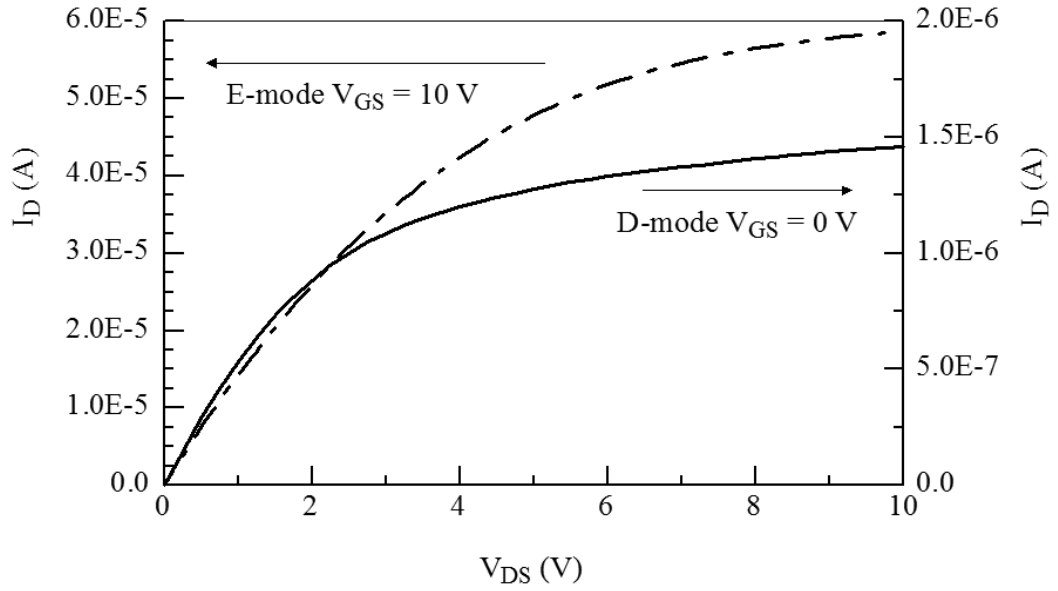


Figure 5.9: I_D-V_{DS} output curve for final circuit E/D inverter TFTs. The E-mode TFT output curve (left scale) is measured at $V_{GS} = 10$ V and the D-mode TFT I_D-V_{DS} curve (right scale) is measured at $V_{GS} = 0$ V.

acceptor-traps centered around $V_{GS} = 1.5$ V. The turn-on voltage for D-mode TFTs is $\sim$ -8 V and the threshold voltage is $\sim$ -4 V. The E-mode device's V_{ON} is $\sim$-2.5 V with a threshold voltage of $\sim$ 4.5 V. Similar acceptor trap and mobile ion effects as just described are also present in the log(I_D)-V_{GS} curves of TFTs fabricated using Si/SiO_2 substrates which are synthesized alongside ITO/SiO_2 circuit stacks. Thus, these non-idealities are not derived from the gate stack itself but instead from subsequent processing.

While log(I_D)-V_{GS} transfer curves are valuable for mobility modeling and switching assessment, I_D-V_{DS} output curves are more relevant for other types of circuit applications. For an E/D inverter, the most useful E-mode drive TFT I_D-V_{DS} curve is when V_{IN} is high, i.e., when $V_{GS} = V_{IN} = V_{DD}$. In contrast, the D-mode load TFT always operates at $V_{GS} = 0$ V, since the gate is tied to the source. The load TFT operates at $V_{DS} = V_{DD} - V_{OUT}$ and the drive TFT operates at $V_{DS} = V_{OUT} - V_{GND}$, where V_{GND} is typically 0 V. Figure 5.9 shows I_D-V_{DS} output curves corresponding to discrete E/D TFTs on the final circuit substrate. The E-mode TFT output curve (left) is measured at $V_{GS} = 10$ V and the D-mode TFT output curve (right) is measured at $V_{GS} = 0$ V since $V_{DD} = 10$ V for the E/D inverter shown in Section 5.3.2. The E-mode TFT output curve at $V_{GS} = 0$ V is not shown, since $I_D \approx 10^{-9}$ A for $0 \leq V_{DS} \leq 10$ V. Both the E-mode and the D-mode TFT show transistor-like behavior, although neither TFT is completely saturated

at $V_{DS} = 10$ V. Unlike the log(I_D)-V_{GS} transfer curves of Fig. 5.8, neither mobile ion effects nor evidence of acceptor-like traps are observed in these output curves.

5.3.2 Inverter Results

Figure 5.10 shows the input-output curve for a ZTO channel TFT enhancement/depletion inverter with $V_{DD} = 10$ V and Table 5.3 summarizes the results for 4 inverters on one substrate. The result shown in Fig. 5.10 corresponds to the best inverter, but gains for all four inverters measured are fairly consistent. The input-high voltage (V_{IH}) and the input-low voltage (V_{IL}) are defined as the voltages at which the input-output curve has a slope of -1, indicating unity gain. V_{IL} and V_{IH} are the maximum and minimum input voltages, respectively, which the inverter interprets as a logic low or as a logic high, thus defining the borders of the transition region [73]. The gain is obtained in the transition region by calculating the average slope of the transfer curve over a 0.5 V range centered approximately at $V_{OUT} = V_{DD}/2 = 5$ V.

With $V_{DD} = 10$ V, an excellent gain of 10.6 V/V is obtained, with a high-output voltage (V_{OH}) of 10 V at $V_{IN} = 0$ V and a low-output voltage (V_{OL}) of 0.116 V at $V_{IN} = 10$ V. The low noise margin (i.e., $N_{ML} = V_{IL} - V_{OL}$) and high noise margin (i.e., $N_{MH} = V_{OH} - V_{IH}$) are equal to the range over which the input voltage can fluctuate before the inverter interprets the input incorrectly, e.g., a logic "0" input is no longer interpreted by an inverter as a logic "1" output [73]. For this circuit the noise margins are asymmetric, since $N_{ML} \approx 2.1$ V and $N_{MH} \approx 5.9$ V. An ideal inverter would have equal noise margins.

#	**Gain (V/V)**	$\mathbf{V_{OL}}$ **(V)**	$\mathbf{V_{IH}}$ **(V)**	$\mathbf{V_{IL}}$ **(V)**
1	**10.6**	0.116	4.08	2.21
2	9.2	**0.097**	3.91	2.09
3	7.6	0.293	**4.85**	**2.60**
4	10.3	0.166	4.22	2.28

Table 5.3: E/D inverter performance summary at $V_{DD} = 10$ V. All inverters tested demonstrate a $V_{OH} = 10$ V. V_{IL} and V_{IH} are found using extrapolation. Figure 5.10 shows the transfer curve of inverter #1.

The highest AOS inverter gain was previously reported by Ofuji *et al.* in 2007 [68]. It is cited as a gain of 1.7 V/V with $V_{DD} = 18$ V using an enhancement/enhancement inverter architecture and an IGZO channel. In 2005, R.E. Presley *et al.* reported a gain of ∼1.5 at $V_{DD} = 30$ V with an IGO channel and an enhancement/enhancement inverter architecture [65]. Even though inverter gain increases with increasing V_{DD}, the E/D inverter shown herein demonstrates much higher performance at a lower rail voltage. This leads to lower power consumption.

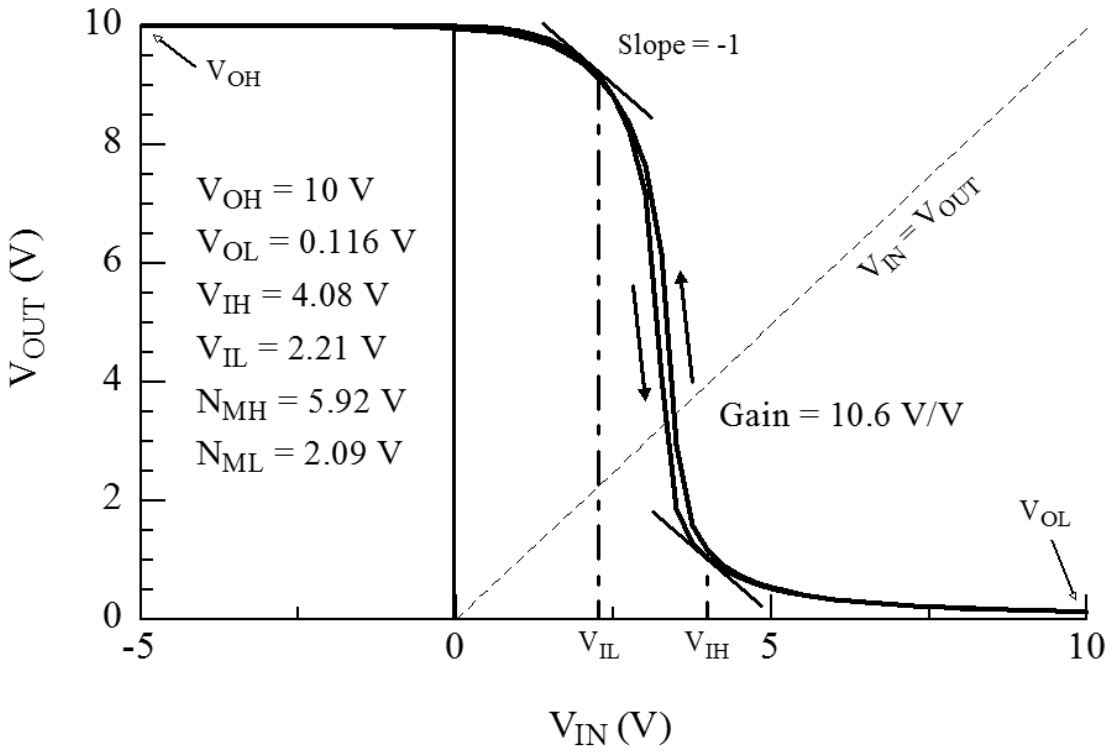


Figure 5.10: E/D inverter transfer curve for a ZTO TFT circuit when V_{DD} = 10 V. A gain of 10.6 V/V is found and the small amount of hysteresis is counter-clockwise. V_{IL} and V_{IH} are are the input-low and input-high voltages, respectively, which are identified by a slope of -1 on the transfer curve.

A high inverter gain ensures that switching occurs abruptly, which aids in establishing a larger noise margin. The inverter transfer curve exhibits minimal hysteresis between forward and reverse sweeps. Ideally, the high-to-low transition voltage of an inverter is near the center of the rail voltage (e.g., 5 V for V_{DD} = 10 V). This is not the case for the inverter reported herein since the load transistor sources insufficient current to the drive transistor. However, the inverter in its present state is still quite usable for digital logic applications. Gain, V_{IL}, V_{IH}, V_{OL}, and V_{OH} are all affected by adjusting the threshold voltages and the W/L ratios of the drive and load transistors. The load (D-mode) and drive (E-mode) TFT W/L ratios also affect the output drive capability of the inverter. Thus, a circuit designer has several variables to change for circuit optimization. The inverter demonstrated here is designed with a $W/L_{load} = 2.5$ and a $W/L_{drive} = 5$, which is rather compact compared to Ofuji's design using $W/L_{load} = 4$ and $W/L_{drive} = 20$ [68].

5.4 Conclusion

In this chapter, n-type enhancement/depletion inverter circuits are introduced and demonstrated. Integrated ZTO TFT development is continued from Chapter 4, and new cleaning methods have enabled improved transistor performance. The first AOS demonstration of intentional, simultaneous enhancement-mode and depletion-mode TFTs on a single substrate is realized using a novel deposition scheme and only one sputter target. ZTO channel TFT E/D inverters are synthesized and measured, resulting in the highest inverter gain for an AOS material reported to date by a 6x margin.

6. CONCLUSIONS & FUTURE WORK

6.1 Conclusions

The primary focus of this thesis is to develop a process to fabricate zinc tin oxide (ZTO) TFT circuits. As no satisfactory ZTO wet etch is known, a plasma-etch study using various ratios of Ar/CH_4 as the feedstock is investigated in order to devise a selective etch recipe for two stoichiometries of ZTO (1:1 and 2:1 Zn:Sn). Indium gallium oxide (IGO), indium gallium zinc oxide (IGZO), indium tin oxide (ITO) are also explored in this etch study. The Ar/CH_4 gas composition shows excellent etch selectivity with respect to SiO_2, thus providing a route to selective patterning of ZTO channels on SiO_2. A process is designed to remove problematic plasma-hardened photoresist and polymer deposits after ZTO etching without damaging active layers. A central focus of this thesis involves devising appropriate ZTO cleaning processes and assessing their viability with respect to ZTO integrated circuit fabrication.

AC/DC rectifier circuits, as designed by B. McFarlane in his MS thesis [66], are realized using a ZTO channel. This appears to be the first reported ZTO-based circuit. Even though the ZTO TFTs used in these circuits suffer from significant plasma-ash related damage due to the use of a non-optimal cleaning recipe, they show similar output performance to IGO-based circuits. These rectifiers operate effectively in the MHz range despite possessing high parasitic capacitances. Thus, ZTO and IGO appear to be suitable for RFID circuits and other similar-speed applications.

Further refinement of the ZTO process recipe yielded a dramatic improvement in integrated circuit transistor performance, with TFTs annealed at 400 °C for 1 hour showing incremental and average mobilities of 23 and 18 $cm^2V^{-1}s^{-1}$, respectively, turn-on voltages between approximately 0 and 1.5 V and subthreshold swings below 0.5 V/dec . Although not pursued, ZTO-based AC/DC circuits using the best optimized recipe are expected to show improved voltage rectification and high frequency performance compared to the ZTO rectifiers of Chapter 4, and to also outperform previously-reported IGO-based rectifiers [66].

A second circuit realized herein involves both an enhancement-mode and a depletion-mode TFT, which are fabricated simultaneously on a single substrate using a single target and a single post-deposition annealing step. Both E-mode and D-mode TFTs fabricated on a thermal silicon dioxide substrate display performance comparable to that of shadow mask patterned devices. This process is then used to build a high-gain enhancement/depletion (E/D) inverter. This E/D inverter could serve as a functional block for making more complex digital logic circuits. At a rail voltage

of 10 V, the inverter has a gain of 10.6 V/V, an output-high voltage of 10 V and an output-low voltage of 0.116 V. This is the highest gain yet reported for an AOS inverter.

The demonstrated high performance of this inverter bodes well for future digital logic applications using AOS materials. This result can be extended to the development of a toolbox of logic elements, such as multiplexors/demultiplexors, flip-flops, registers, and read-only memory blocks.

6.2 Recommendations for Future Work

While existence proofs of excellent ZTO device and circuit performance are demonstrated in this thesis, significant processing and process and integration development is required before AOS materials are ready for high-volume manufacturing. Perhaps the most important message of this thesis is that ZTO appears to be a very attractive AOS candidate material for commercial applications. With this in mind, the following research is recommended for future work.

6.2.1 Plasma-Etch Development

The plasma etch study undertaken in this thesis only examined etch rate for gas compositions at 100 mTorr and 150 W on small samples. To guarantee full patterning, the recipe used to etch ZTO channel layers in this thesis overetches any channel with a thickness less than 75 nm, thus exposing the SiO_2 beneath to significant plasma exposure. While this process works, it is not optimized. Improving the ZTO etch process might reduce polymer formation problems and decrease SiO_2 surface damage. The development of dry etch recipes for SiO_2 and ITO is recommended to improve run-to-run process consistency and throughput, and increase laboratory safety. Research and characterization of etch sidewall profiles for ITO gates may serve to improve PECVD-SiO_2 coverage, reducing dielectric leakage problems.

6.2.2 Photolithography and Cleaning

Improving photolithography and cleaning steps is necessary to in order to improve run-to-run consistency. Future process recipes will require much higher yields for the fabrication of more complex circuits. Developing an optimized hard-bake recipe for photoresist is important in order to decrease minimum dimensions while maintaining clearly defined edges, especially for subsequent plasma processing and etching. Cleaning procedures, the single greatest challenge faced in this thesis, need to be improved.

6.2.3 Passivation

As circuits become more complicated, the need for additional metal layers to route interconnects and maintain a high packing density becomes critical. Likewise, to remove environmental variables from affecting the circuit and to improve mechanical and chemical robustness, encapsulation is necessary. Hong and Wager [37] demonstrated a SiO_2 passivation layer on ZTO, but developing a passivation recipe that has a lower temperature budget than 600 °C and gives consistent results is necessary for circuit processing and use as an interlayer dielectric. Other passivation materials, especially a robust low-k dielectric should also be pursued.

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APPENDICES

ZTO E/D Inverter Process Flow

1. Substrate: ∼180 nm thick ITO deposited onto 25 x 25 x 1.1 mm^2 Corning 1737 glass
2. Gate stack synthesis
   (a) Scribe sample identification
   (b) Substrate cleaning:
      i. Spray rinse 18.2 MΩ water (DI water)
      ii. 45-60 min. ultrasonic bath in Contrad70 at 45 °C
      iii. Spray rinse DI water, N_2 blow dry
      iv. Dehydrate 10 min. at 85 °C hotplate
   (c) Pattern gate electrode (ITO) by wet etch (Mask 1)
      i. Spin coat, expose, and develop photoresist gate etch mask
      ii. 6 min. hard bake, 85 °C hotplate
      iii. Soak 8-10 min. in concentrated HCl, or until ITO removed from unpatterned areas
      iv. Spray rinse DI water, N_2 blow dry
      v. Soak in 1165 photoresist stripper for 30 minutes
      vi. Ultrasonically agitate 1165 stripper for ∼ 5 minutes
      vii. Spray rinse DI water, N_2 blow dry
      viii. Dehydrate ≥1 hour in 125 °C oven
   (d) PECVD 100 nm SiO_2 layer
3. First ZTO Channel deposition
   (a) N_2 blow to remove particulate
   (b) Sputter deposit 70 nm ZTO channel layer
      i. Pump to 2 x 10^{-6} Torr
      ii. Presputter 10 minutes, 50 W, 5 mTorr, 90/10 Ar/O_2
      iii. 8 minute deposition while translating substrate over a 4 in. path
   (c) Pattern dual channel layer by plasma etch (Mask 2)
      i. Spin coat, expose, and develop photoresist dual-channel etch mask
      ii. 6 min. hard bake, 85 °C
      iii. Plasma etch 7-10 minutes, 150 W, 100 mTorr, 80/20 Ar/CH_4
      iv. Without breaking vacuum, plasma ash 3-4 minutes, 100 W, 100 mTorr, 1/1/25 $Ar/CHF_3/O_2$ (Complete recipe: 50nmZTO)
      v. Soak in 1165 photoresist stripper for ≥30 minutes
      vi. Ultrasonically agitate in 1165 stripper for ∼ 5 minutes
      vii. Spray rinse DI water, N_2 blow dry

viii. Dehydrate ≥1 hour in 125 °C oven

4. Second ZTO Channel Deposition

   (a) N_2 blow to remove particulate

   (b) Pattern channel 2 layer by liftoff (Mask 3)

      i. Spin coat, expose, and develop photoresist channel 2 lift-off mask

      ii. No post-develop hard bake

   (c) Sputter deposit 70 nm ZTO channel layer

      i. Pump to 2 x 10^{-6} Torr base pressure

      ii. Presputter 5 minutes, 88.5 W, 5 mTorr, 90/10 Ar/O_2 plus 5 minutes, 88.5 W, 5 mTorr, 100/O Ar/O_2

      iii. 8 minute deposition while translating substrate over a 4 in. path

   (d) Soak in acetone ≥1 hour for lift-off

   (e) Ultrasonically agitate until ZTO film releases

   (f) Spray rinse acetone, isopropanol, DI water

   (g) Dehydrate 10 min., 85 °C hotplate or ≥1 hour, 125 °C oven

5. Wet etch pattern vias through SiO_2 (Mask 4)

   (a) Spin coat, expose, and develop photoresist gate etch mask

   (b) 6 min. hard bake, 85 °C

   (c) Soak 40-50 seconds in buffered HF, or until SiO_2 removed from exposed windows

   (d) Spray rinse DI water, N_2 blow dry

   (e) Soak in 1165 photoresist stripper for 30 minutes

   (f) Ultrasonically agitate in 1165 stripper for ∼ 5 minutes

   (g) Spray rinse DI water, N_2 blow dry

6. Anneal in air at 450 °C for 1 hour with 5 °C/min. ramp rates

7. Source/Drain lift-off

   (a) Spray rinse Di water, N_2 blow dry

   (b) Dehydrate 10 min., 85 °C hotplate

   (c) Pattern for source/drain by lift-off (Mask 5)

      i. Spin coat, expose, and develop photoresist source/drain lift-off mask

      ii. No post-develop hard bake

   (d) Thermally evaporate 200 nm aluminum layer

      i. Load single full Al clip

ii. Pump to 4 x 10^{-5} mBar base pressure

(e) Soak in acetone $\geq$1 hour for lift-off

(f) Ultrasonically agitate until aluminum film releases

(g) Spray rinse acetone, isopropanol, DI water

(h) Dehydrate 30 to 45 minutes, 125 °C oven