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Farhad Farahbakhshian for the degree of Master of Science in

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Title: An Enhanced Swing Differential Colpitts CMOS VCO for Low-Voltage Operation

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Terri S. Fiez Kartikeya Mayaram

An enhanced swing differential Colpitts VCO (ESDC-VCO) dramatically improves the swing of a Colpitts VCO by allowing the signal to swing below ground and above the supply voltage. Fabricated in a 1P8M 0.13 μm CMOS process, the ESDC-VCO operates at 4.9GHz with a 0.475-V supply and consumes 2.7mW. The measured phase noise is -136.2 dBc/Hz at a 3-MHz frequency offset. The ESDC-VCO employs digital amplitude control and achieves a figure of merit (FOM) of 196.2 dBc/Hz, making it the highest performing integrated LC oscillator to date.

An Enhanced Swing Differential Colpitts CMOS VCO for Low-Voltage Operation

by

Farhad Farahbakhshian

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APPROVED:

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AN ENHANCED SWING DIFFERENTIAL COLPITTS CMOS VCO FOR LOW-VOLTAGE OPERATION

1 INTRODUCTION

As the field of wireless communication progresses, the demand for low-cost low-power solutions in wireless systems grows. Wireless standards such as Bluetooth, wireless local area network (WLAN), wireless personal area network (WPAN) [1], and wireless sensor networks [2], require low-power RF integrated circuit designs to reduce cost. CMOS is an attractive choice because it facilitates system-on-chip integration with digital circuits, resulting in significant area savings.

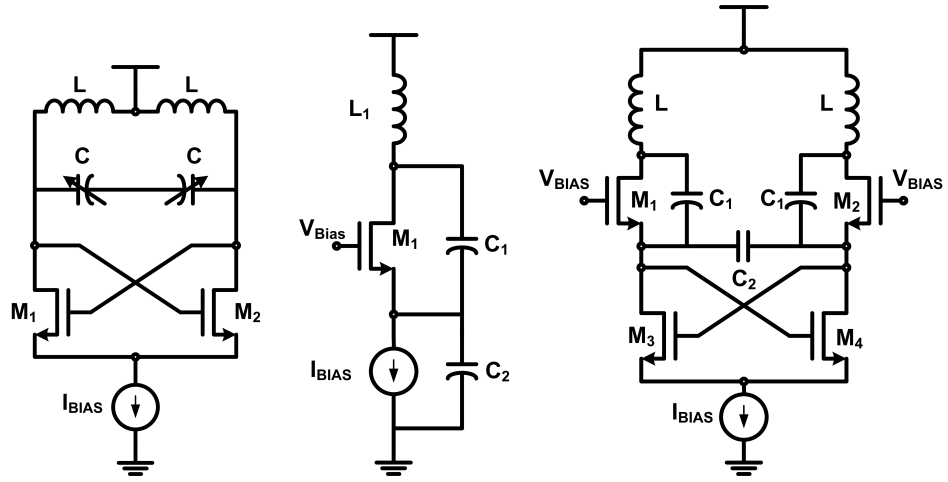
In order to reduce power consumption in wireless systems, supply voltages in integrated circuits have reduced significantly. However, this reduction in supply voltage introduces new design challenges. Specifically, a reduction of signal amplitude in turn reduces the signal-to-noise ratio, degrading the system performance. One of the most crucial and power hungry blocks in RF front ends, the voltage-controlled oscillator (VCO) in particular suffers from supply voltage reduction because decreases in voltage swing lead to significant phase noise degradation. For this reason, high performance low-voltage VCO's that can operate at multi-gigahertz frequencies are needed.

Published VCO's strive to improve the overall performance, as measured by their FOM [3], in terms of some combination of noise, frequency, swing, supply voltage, and power consumption. Low voltage designs attempt to reduce power by enhancing the swing and not increasing the current draw [4, 5]. Conversely, others strive to improve the noise of oscillators properties [6, 7]. Combining both approaches, as this work does, provides for further improvements in the overall VCO performance.

This paper presents the design of an enhanced swing differential Colpitts voltage controlled oscillator (ESDC-VCO) with digital amplitude control in a 1P8M 0.13μm CMOS process. The proposed VCO has many advantages over conventional VCO's. The most important of which is that the signal amplitude is not limited by the supply voltage, and

is able to swing below the ground potential as well as above the supply voltage. This extra signal swing leads to a significant improvement in the oscillator phase noise performance. Additionally, by employing the Colpitts type feedback, the proposed topology achieves excellent cyclo-stationary noise properties, and consequently, improves phase noise for a given power consumption.

The remainder of the paper is outlined as follows. Section 2 describes conventional VCO topologies and their properties. Section 2.1 presents the proposed VCO topology, describing the advantages and some important design procedures. Section 3 presents the design of the digital amplitude control loop. The experimental results are presented in Section 4 and the conclusion follows in Section 5.



(a) (b) (c)

FIGURE 2.1: Schematic of conventional VCO's. (a) Cross-coupled VCO. (b) Colpitts VCO. (c) Differential Colpitts VCO.

2 CONVENTIONAL VCO'S

VCO performance is determined by the design of both the tank and the feedback structure that produces the negative conductance. Improvements in the tank are mainly due to advances in process technology. However, changes can be made in the feedback structure that result in improvements in the VCO phase noise performance.

A complementary cross-coupled LC VCO is shown in Fig. 2.1(a). It consists of a tuned LC tank and a cross coupled NMOS (or PMOS) pair which produce a negative conductance to cancel out the losses in the tank. The cross-coupled VCO has become a popular choice due to its ease of design and small capacitive loading on the tank. However, the phase noise in the cross-coupled VCO suffers from poor cyclo-stationary noise alignment [6]. This emanates from the noise generated by the active devices in the cross coupled VCO entering the tank when the oscillator phase is most sensitive to

perturbations.

In a Colpitts VCO, Fig. 2.1(b), the maximum noise is injected in the tank when the oscillator phase is least sensitive to perturbations. The Colpitts oscillator also has much lower flicker noise up conversion than the cross coupled VCO [6]. For these reasons, better phase noise performance can be achieved with the Colpitts oscillator. However, the Colpitts structure is single ended in nature, which makes the phase noise performance of the VCO very sensitive to supply noise. The structure also has unreliable start-up properties and a lower start-up gain for a given power consumption compared to the cross coupled structure.

The VCO shown in Fig. 2.1(c), is a differential adaptation of the Colpitts oscillator [6]. This topology is less sensitive to supply noise and has more start-up gain than the traditional Colpitts VCO. The drawback to this structure is that the headroom is considerably reduced due to the number of stacked transistors. This decreases the amplitude in the oscillator which results in an increase in phase noise.

One common limitation of the VCO's in Fig. 2.1 is that they cannot sustain a single ended tank voltage amplitude greater than the supply voltage. The oscillator tank voltage amplitude has an important effect on phase noise. Using Leeson's linear analysis [8], the single-sideband oscillator phase noise $L\{\Delta\omega\}$, at a frequency offset $\Delta\omega$ from the carrier frequency ω_0 is:

$$L\{\Delta\omega\} = 10\log\left[\frac{2FkT}{P_{sig}}\left(1+\frac{\omega_0}{2Q_{Tank}\Delta\omega}\right)^2\right], \tag{2.1}$$

where F is an empirical parameter (also known as the excess noise factor), k is the Boltzmanns constant, T is the absolute temperature in degrees Kelvin, Q_{Tank} is the quality factor of the tank (also known as the loaded Q), and P_{sig} is the oscillation signal power. The signal power may approximated as:

$$P_{sig} \approx I_{Bias}V_{Amp}, \tag{2.2}$$

where I_{Bias} is the current being used by the oscillator and V_{Amp} is the single ended tank

voltage amplitude of the oscillator. Since $L\{\Delta\omega\}$ is inversely proportional to the signal amplitude, minimization of the phase noise requires maximizing the VCO single ended amplitude. The maximum single ended amplitude of a VCO will be referred to as V_{limit}.

The respective V_{limit} for the three oscillators shown in Fig. 2.1 is:

$$V_{limit} = V_{DD} - V_{DSAT} - V_{IBias}, \tag{2.3}$$

where V_{DD} is the supply voltage, V_{DSAT} is the minimum drain-source voltage required to keep transistors M1 and M2 in the active region and V_{IBias} is the voltage drop across their current sources. From Eq. (2.3), V_{limit} of the oscillators is limited by the active devices entering the triode region at the peak of the voltage swing. The large voltage swing reduces the drain-source voltages of the transistors below their V_{DSAT}, forcing them to operate in the triode region. Once the transistors are in the triode region, an increase in current does not produce an increase in the signal amplitude. Architectural changes to the VCO structure are required to enable signal swing enhancements.

2.1 New Topology

Shown in Fig. 2.2 is the topology of the new ESDC-VCO that incorporates Colpitts-type feedback in a fully differential structure. The proposed VCO uses the additional inductor, L_2, to boost the start-up gain of the Colpitts structure and also to increase the V_{limit} of the oscillator, allowing a single ended amplitude much greater than V_{DD} as shown in Fig. 2.3(a). To eliminate additional noise sources and reduce the required supply voltage, a tail current source is not used. Collectively, this leads to considerable improvements in the close-in phase noise of the oscillator [7]. The current in the VCO is controlled by a bias at the gates of M_1 and M_2.

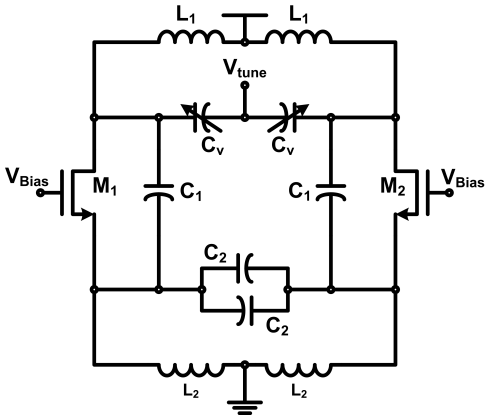


FIGURE 2.2: Schematic of the new ESDC-VCO.

As discussed in Section 2, phase noise is inversely proportional to oscillation amplitude. Therefore, it is beneficial to maximize V_{limit} in oscillators. The ESDC-VCO achieves a much higher V_{limit} than the conventional VCO's. Effectively, the oscillation amplitude is enhanced and the supply voltage can be reduced, lowering the power consumption, while maintaining the same phase noise. Design insight that quantifies the swing to supply voltage and power trade-off of the ESDC-VCO is apparent by solving for the maximum single-end swing, V_{limit}.

Equating the drain-source signal amplitude at a given point in the period, such as a trough for mathematical convenience, to the transistor V_{DSAT} provides V_{limit}. At the drain, $V_D = V_{DD} - V_{DA}$, where V_{DA} is the amplitude at the drain. Since the source has only AC components, $V_S = -V_{SA}$, where V_{SA} is the source amplitude. Colpitts feedback directly relates the source amplitude to the drain amplitude by a capacitive voltage divider:

$$V_S = \frac{V_D}{1 + \frac{4C_2}{C_1}}. \tag{2.4}$$

Solving for V_D when $V_{DS} = V_{DSAT}$, results in V_{limit}:

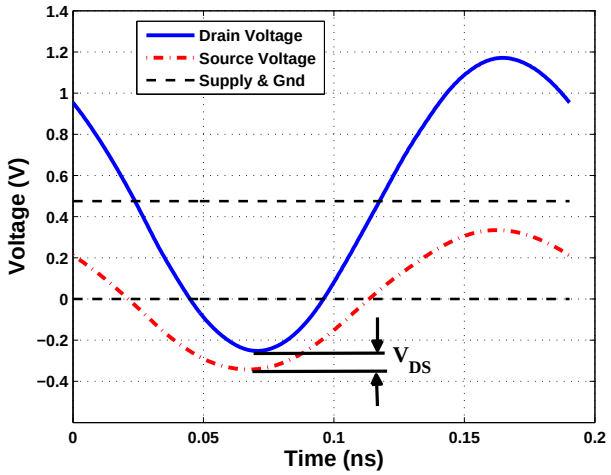
$$V_{limit} = \frac{V_{DD} - V_{DSAT}}{1 - \frac{1}{1+\frac{4C_2}{C_1}}}. \tag{2.5}$$

From (2.5), it is clear that the denominator will always be less than one. Regardless of the ratio of C_1 and C_2, the ESDC-VCO will have a larger V_{limit} than the conventional VCO's. Thus, the supply voltage required for a given swing is scaled by this capacitive ratio, reducing the oscillator power consumption. Fig. 2.3(a) shows a numeric example of the swing in the ESDC-VCO.

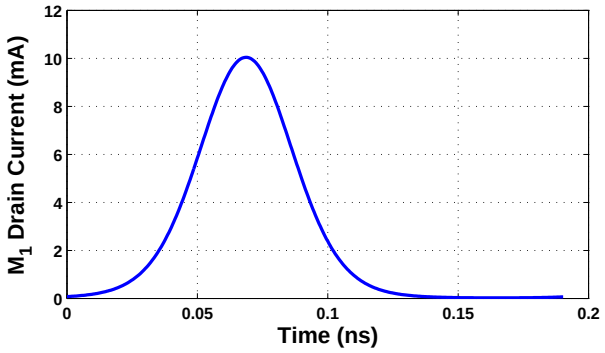
In Colpitts VCO's, the transistor only turns on at the trough, when the oscillator is least sensitive to phase perturbations. Fig. 2.3(b) plots the drain current associated with the drain voltage shown in Fig. 2.3(a). Reducing the duty cycle of this current pulse while keeping the energy to the tank unaltered reduces the duration in which noise is injected by the transistor into the tank. In order to reduce the duty cycle of the current pulse, the gate bias voltage or W/L of M_1 and M_2 need to be increased. However, an increase in the transconductance of M_1 and M_2 also leads to an increase in their thermal noise. Thus, the W/L of M_1 and M_2 need to be optimized by taking into account the trade-off between the duty cycle and the transistor thermal noise.

2.11 Startup Condition

An analysis of the start-up condition is important to ensure that the oscillator will operate over the desired tuning range and different process corners. In addition, since



(a)

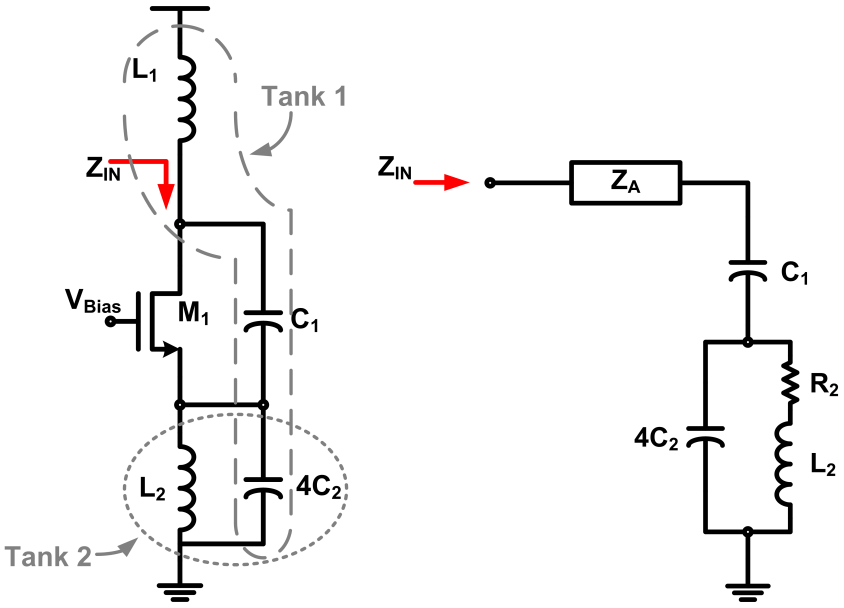


(b)

FIGURE 2.3: Simulated waveforms of the ESDC-VCO. (a) Voltage swing. (b) Transistor M_1 current.

there are two resonant tanks in the circuit, Tank 1 consisting of L_1, C_1 and C_2, and Tank 2 consisting of L_2 and C_2 as shown in Fig. 2.4(a), it is necessary to understand the influence of Tank 2 for start-up.

Using the one-port view of the circuit shown in Fig. 2.4(a), the start-up of the oscillator can be analyzed by determining the equivalent series impedance that the ESDC architecture provides. In order to start oscillations in Tank 1, the magnitude of the



(a) (b)

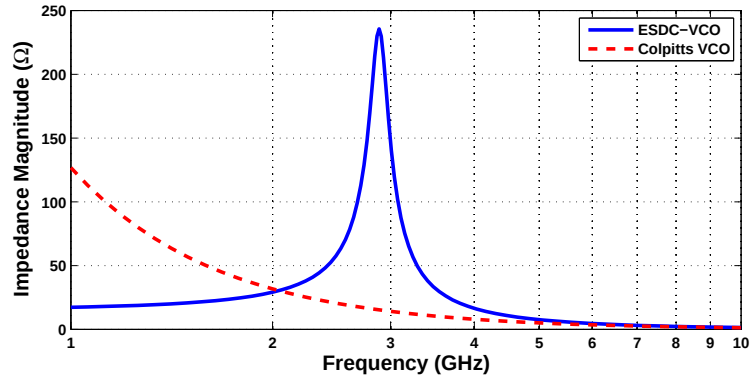
FIGURE 2.4: (a) Half circuit view of the ESDC-VCO, Tank 1 consisting of L_1, C_1 and C_2, and Tank 2 consisting of L_2 and C_2. (b) Simplified small-signal equivalent circuit for Z_{IN}, where R_2 is the series resistance of inductor L_2 and Z_A is the impedance which provides the ESDC negative resistance.

negative impedance must be greater than the losses in the tank. Looking down from L_1 in Fig. 2.4(a), the expression for the small-signal impedance Z_{IN} is:

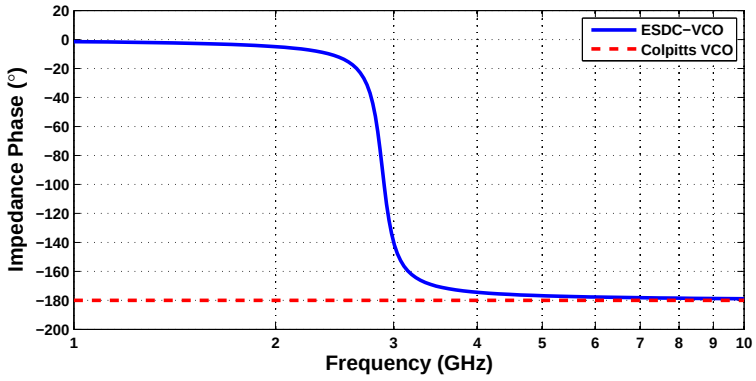
$$Z_{IN} = \frac{g_{m1}(\frac{1}{s4C_2} \| sL_2 \| Q_2^2 R_2)}{sC_1} + \left(\frac{1}{s4C_2} \| sL_2 \| Q_2^2 R_2 \right) + \frac{1}{sC_1}, \tag{2.6}$$

where g_{m1} is the small-signal transconductance of M_1, Q_2 is the quality factor of L_2, and R_2 is the series resistance of L_2. After collecting the terms in Z_{IN}, the reduced circuit model in Fig. 2.4(b) can be obtained, from which the term, Z_A, that provides the ESDC negative resistance at resonance is defined as

$$Z_A = \frac{g_{m1}(\frac{1}{s4C_2} \| sL_2 \| Q_2^2 R_2)}{sC_1}, \tag{2.7}$$



(a)



(b)

FIGURE 2.5: Series impedance of the ESDC-VCO and Colpitts VCO. (a) Magnitude. (b) Phase.

In order for Z_A to be a negative resistance, Tank 2 needs to resonate and become capacitive so that there is capacitive feedback from the drain of M_1 to its source. Thus, L_2 needs to be sized significantly larger than L_1 to ensure that Tank 2 resonates at a lower frequency than Tank 1. Fig. 2.5 shows the series impedance of the ESDC-VCO compared to the Colpitts VCO with the same power consumption, transistor size (M_1), and primary tank (Tank 1). As shown in Fig. 2.5(b), the series impedance of the ESDC-VCO is effectively a negative resistance after the peak which is caused by the resonance

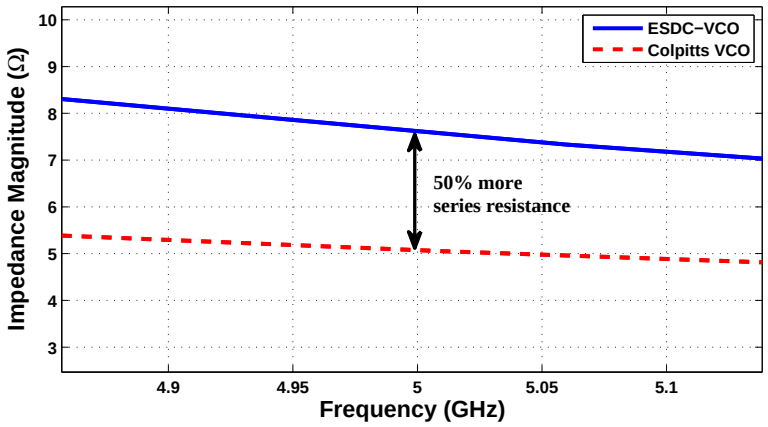


FIGURE 2.6: Expanded view of the series impedances at 5 GHz.

of Tank 2 that occurs at about 3GHz. Since the desired oscillation frequency of Tank 1 is 5GHz, the resonant frequency of Tank 2 is chosen to be 2GHz lower to ensure that the phase is $-180°$ at the oscillation frequency of Tank 1.

Fig. 2.6 shows an expanded view of the series impedance at 5 GHz. The ESDC-VCO provides more than 50% additional negative resistance than the Colpitts VCO at the oscillation frequency. Increases in the negative resistance directly lead to an increase in the oscillator start-up gain. This can be very beneficial, especially in a CMOS oscillator where the start-up gain is proportional to $\sqrt{I_d}$. Consequently, the ESDC-VCO uses less than half the current to obtain the same start-up gain, making it more efficient in terms of power consumption.

2.12 Tank Design

The LC tank is very critical to the design of the VCO since the phase noise is inversely proportional to the square of Q_{Tank}, as seen from (2.1). Thus high values of Q_{Tank} are desired and the LC tank needs to be carefully designed. Fig. 2.7 shows a simplified version of the ESDC-VCO resonant network, where the drains and sources of M_1 and M_2 connect to d_1, d_2, s_1, s_2, respectively.

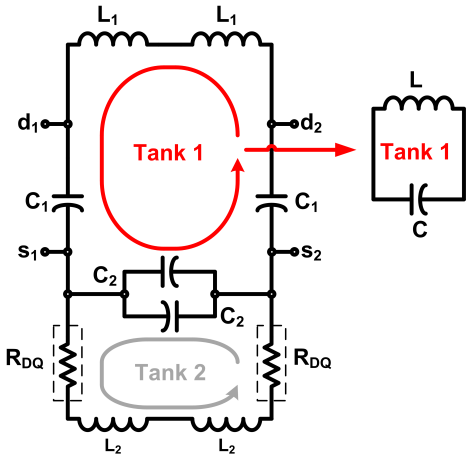


FIGURE 2.7: Simplified circuit for the ESDC-VCO tank.

The addition of inductor L_2, allows a second tank to be formed with L_2 and C_2 that could potentially be the primary resonant circuit for oscillations. This can completely alter the oscillation frequency of the circuit. In order to prevent this, an additional resistance R_{DQ} is added in series with L_2 to reduce the Q of Tank 2, hence increasing the gain needed to start oscillations within Tank 2. Reducing the Q of Tank 2 does not affect the Q of Tank 1 because the additional resistance is added in series with L_2 and not C_2 which is shared with Tank 1.

Examining the resonant frequencies of the two tanks mathematically shows how they can be decoupled. The resonant frequency of Tank 1, also the frequency of oscillation is given by,

$$\omega_{osc} = \frac{1}{2\sqrt{L_1 \frac{C_1 C_2}{C_1 + 4C_2}}}. \tag{2.8}$$

the resonant frequency of Tank 2 is given by:

$$\omega_{T2} = \frac{1}{2\sqrt{L_2 C_2}}. \tag{2.9}$$

In order to fully decouple and separate the tanks, the resonant frequencies of Tank 1 and Tank 2 are chosen to be far apart. As stated in Section 2.11 the resonant frequency of

TABLE 2.1: ESDC-VCO tank component values

Component	**Value@5GHz**	**Q@5GHz**
$2L_1$	$1.4nH$	18
$2L_2$	$2.5nH$	14
C_1	$1.85pF$	60
C_2	$0.68pF$	60

Tank 2 is chosen to be 2 GHz lower than Tank 1. Once Tank 2 resonates, its impedance becomes capacitive and inductor L_2 will not have any effect. Thus at ω_{osc}, L_2 will not affect the oscillations in Tank 1.

It should be noted that increasing L_1 for a given area constraint to maximize the $\sqrt{\frac{L}{C}}$ of the primary tank does not necessarily lead to improvements in oscillator phase noise [11] because an increase in L_1 also increases the series parasitic resistance in L_1. Hence, a decrease in the Q of the inductor and eventually the tank Q occurs, setting an upper bound on L_1. Therefore, finding the optimum value for L_1 becomes an iterative process.

L_1 is realized with a two turn differential center-tapped octagonal spiral inductor. In order to achieve optimum phase noise, the components in Tank 1 need to have their peak Q at the operating frequency of the oscillator. C_1 and C_2 are realized with MIM capacitors and C_V is realized with MOS varactors. The component that has the most effect on Tank 1 Q is L_1, since integrated inductors have very low Q's compared to the MIM capacitors and MOS varactors. Table 2.1 shows typical component and Q values.

3 DIGITAL AMPLITUDE CONTROL

To ensure proper start-up, oscillators must be designed with excess loop gain. This can eventually lead to degradation in phase noise and an increase in unwanted harmonics in the oscillator. In most practical oscillator designs, the loop gain must be greater than 1.5 at all process corners. In one corner the oscillator might barely start up. While in another corner the oscillator may have a loop gain 10 and dissipates excess power. This can lead to significant over-design, or excess power consumption in the oscillator. For MOS devices the power consumption is even higher since the start-up gain is proportional to $\sqrt{I_d}$. An amplitude control mechanism can ensure that the oscillator will start up, by increasing the current flowing into the oscillator until the desired amplitude of oscillation is reached. Conventional amplitude control schemes demonstrated in [12–14] use continuous feedback methods which contribute noise that feeds back to the oscillator.

In this work, an amplitude control mechanism is proposed that eliminates the deficiencies in the conventional approach, by breaking the noise feedback loop. Fig. 3.1 shows a simplified block diagram of the digital amplitude control scheme that consists of a peak detector, comparator, digital state machine, and a programable bias voltage (PBV). The ESDC-VCO's amplitude is captured by the peak detector and then compared with the desired amplitude V_{Cont} as shown in Fig. 3.1. The comparator output is then analyzed by the state machine that decides whether to update the PBV, which controls the current in the ESDC-VCO. The advantage of digital amplitude control is that it is only active during the calibration of the oscillator current. Thus, the noise in the loop does not feed back in the VCO and degrade its phase noise. Furthermore, the digital amplitude control can work with supply voltages as low as 0.4 V.

The power consumed by the amplitude control circuits is less than 10% of the power consumed by the oscillator during the calibration. Once the oscillator is calibrated,

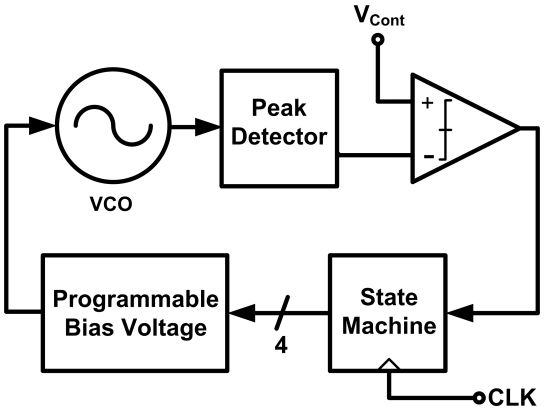


FIGURE 3.1: Digital amplitude control system architecture.

the amplitude control circuits consume between $2-6\%$ of the oscillator power. This is a significant power saving compared with over designing the oscillator with excess loop gain. The following sections describe in detail the design of the blocks in the digital amplitude control system.

3.1 Peak Detector

The criterion for choosing the topology of the peak detector is that it must operate at very low voltages. Designing a low voltage peak detector can be very difficult, since most conventional peak detectors as shown in Fig. 3.2 need a minimum of a diode voltage drop at the input to operate. Therefore, the peak detector output voltage needs to be proportional to the input amplitude without requiring a diode voltage drop.

The peak detector shown in Fig. 3.3 can work with supply voltages as low $0.25V$. The PMOS devices M_1 and M_2 turn on as the input voltage decreases. A growth in amplitude results in a lower minimum input voltage. Thus, as the amplitude increases, M_1 and M_2 go deeper into the active region causing more current to flow in R_P. As a result, the output voltage of the peak detector is proportional to the input amplitude.

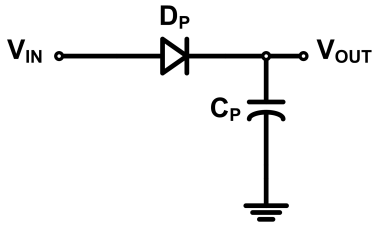


FIGURE 3.2: A conventional peak detector.

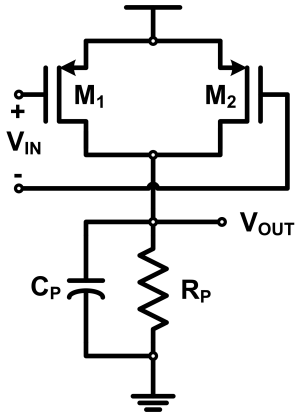


FIGURE 3.3: Schematic of the peak detector.

The gates of M_1 and M_2 in the peak detector are connected to the sources of M_1 and M_2 in the ESDC-VCO. This maximizes the V_{GS} of M_1 and M_2 in the peak detector, which ensures that they turn on even at small input amplitudes. C_P is used to filter the second harmonic that is created by the switching of M_1 and M_2 in the peak detector. The output voltage of the peak detector is set by the value of R_P. If the output voltage increases beyond $V_{DD} - V_{DSAT}$, M_1 and M_2 enter the triode region and the peak detector ceases to work. Therefore, the value of R_P needs to be chosen to ensure that M_1 and M_2 stay in the active region for all input amplitudes. Fig. 3.4 shows the transfer relationship between the input amplitude and the output DC voltage for different values of R_P. An R_P of 900Ω is chosen because it keeps M_1 and M_2 safely in the active region and also complies with the input common mode range of the comparator. The final design of the

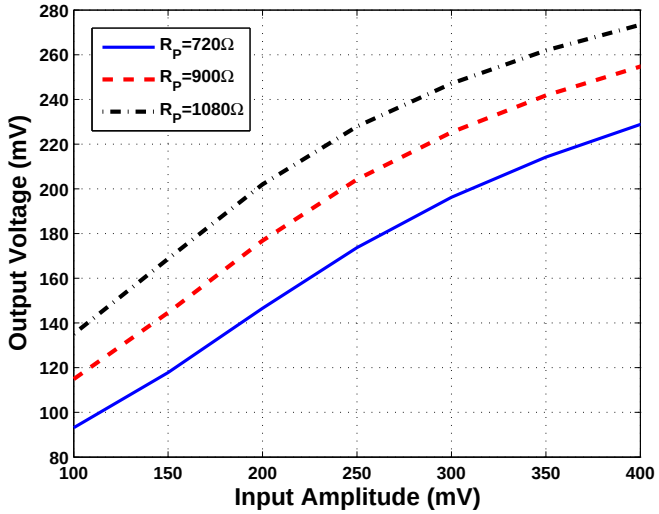


FIGURE 3.4: Simulated peak detector transfer curve.

peak detector consumes $100\mu A$ of current from a $0.4V$ supply.

3.2 Comparator

A schematic of the comparator is shown in Fig. 3.5. The traditional comparator architecture is tailored for low-voltage/power operation. In order to reduce the headroom needed for the comparator, the MOS devices were designed with large lengths to reduce their threshold voltages. To obtain a low offset voltage, the input devices were sized to be relatively large and operate in the sub-threshold region. PMOS inputs are chosen since the peak detector output voltage is very close to ground. Additionally, two inverters act as buffers and square up the signal sent to the digital state machine. The comparator can work with voltages as low as $0.4V$.

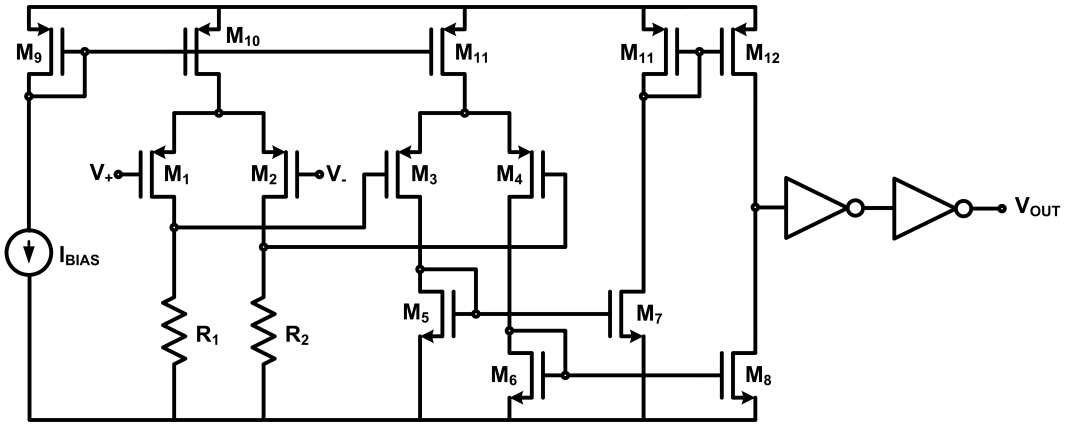


FIGURE 3.5: Schematic of the comparator.

3.3 Digital State Machine

The digital state machine consists of a 4-bit up/down counter and combinational logic. When the input is high, the counter counts up and when the input is low, the count does not change. The output of each bit in the digital state machine is buffered in order to drive the switches in the voltage DAC.

3.4 Programmable Bias Voltage

The PBV is designed to take a digital code from the state machine and control the current in the ESDC-VCO. Fig. 3.6 shows a simplified schematic of the PBV. The output voltage of the PBV is connected to the gates of M_1 and M_2 in the ESDC-VCO. Switches $S_1 - S_4$ are connected to the output of the digital state machine.

The PBV has a minimum voltage corresponding to the minimum current, I_{MIN}. The switchable currents are binary weighted. Hence the current through M_1 will increase linearly as the switches $S_1 - S_4$ close in a binary manner. Fig. 3.7 shows the simulated output of the PBV as $S_1 - S_4$ are switching. The large negative peaking behavior at 0.4

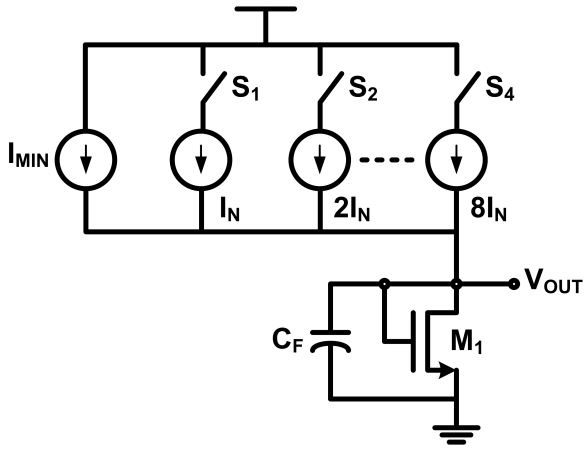


FIGURE 3.6: Schematic of the programmable bias voltage.

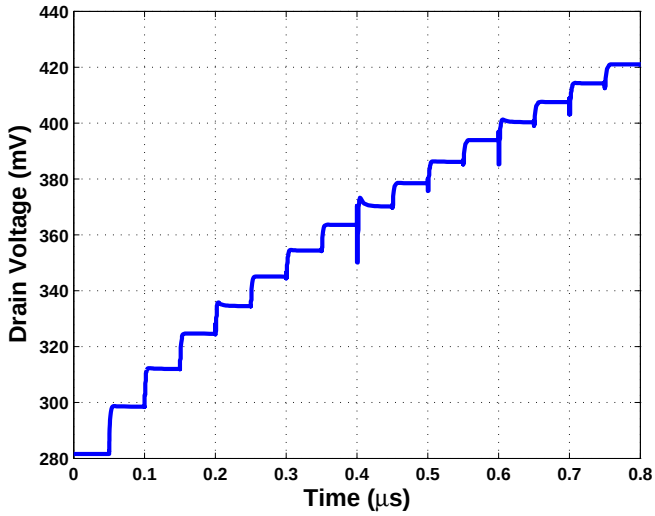


FIGURE 3.7: Simulated voltage DAC output as $S_1 - S_4$ switch in a binary manner.

μs and 0.6 μs is due to the break before make behavior of the switches and does not effect the performance of the loop.

The size of M_1 is chosen to give a control voltage that will start up the oscillator under all operating conditions. C_F is used to filter the noise from M_1 and the current source transistors. C_F should be sized relatively large so that the noise from the voltage

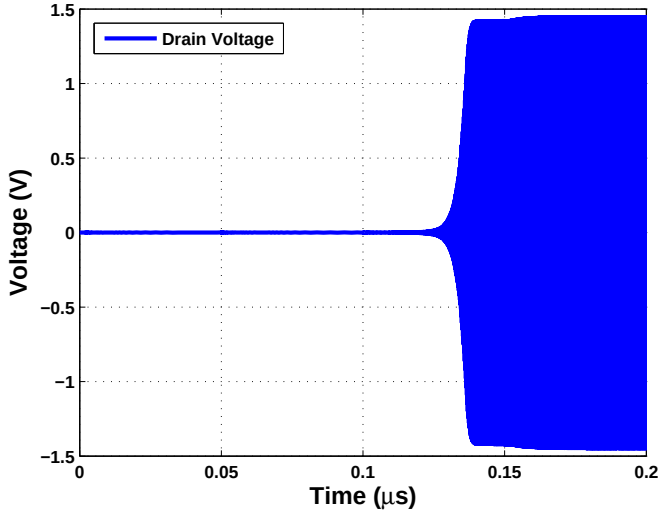


FIGURE 3.8: Simulation of the amplitude control loop for starting up the ESDC-VCO.

DAC does not degrade the phase noise performance of the oscillator. However, there is a trade-off between the amplitude control loop speed and the size of C_F. In order to improve the filtering, a low-pass RC filter can also be used at the output of the voltage DAC.

3.5 Loop Performance

The amplitude control loop is designed to operate at frequencies up to 10MHz. Fig. 3.8 shows the simulated ESDC-VCO outputs as the amplitude control loop starts up the oscillator and maintains oscillations.

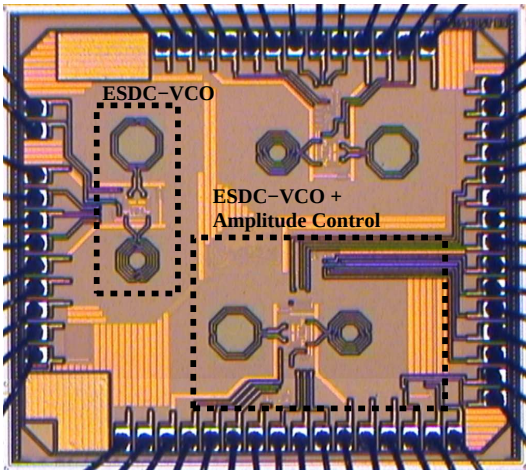


FIGURE 4.1: Chip microphotograph of the 2.2mm x 1.9mm die.

4 EXPERIMENTAL RESULTS

The ESDC-VCO with its digital amplitude control was fabricated in a 1P8M 0.13μm CMOS process. The die photo is shown in Fig. 4.1. All external pins are fully ESD protected. The chip was bonded to a MLF48 package, a standard leadless QFP type package. A standard FR4 circuit board was used for lab testing. The ESDC-VCO outputs are buffered differentially by open-drain NMOS transistors to drive an external 50Ω load. The RF signals are routed on 50Ω transmission lines to maximize signal integrity.

A calibrated Agilent E5052A signal analyzer was used to measure the phase noise of the ESDC-VCO with an external LNA to further boost the signal power from the oscillator. Table 4.1 shows the measured performance of the ESDC-VCO for five different supply voltages. Fig. 4.2 shows the measured phase noise of the 4.9GHz ESDC-VCO for a supply voltage of 0.475V. The frequency in the ESDC-VCO is tuned from 4.85-4.97 GHz by a 0-0.4 V tuning voltage, which corresponds to a tuning range of 2.5%. The limited tuning range is primarily due to the low supply voltage. The peak VCO gain is

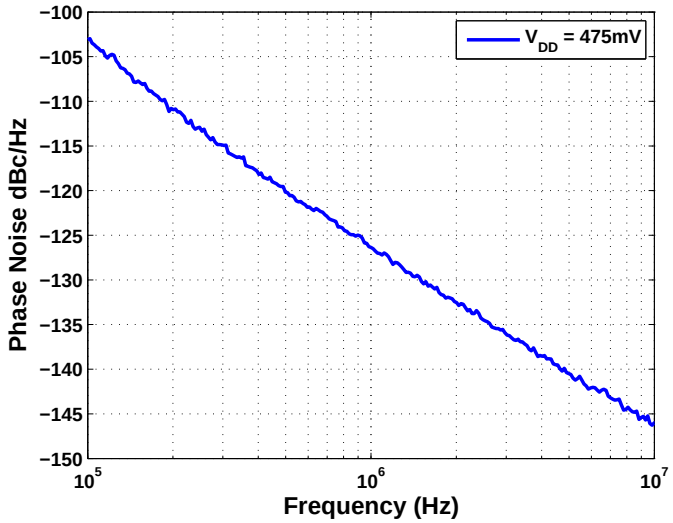


FIGURE 4.2: Measured phase noise of ESDC-VCO.

TABLE 4.1: ESDC-VCO performance

V_{DD} (mV)	400	425	450	475	500
I_{DC} (mA)	4.8	5.1	5.4	5.7	6.0
Phase Noise @ 3MHz (dBc/Hz)	-132.6	-133.0	-135.5	-136.2	-135.7
FOM (dBc/Hz)	193.9	193.9	195.9	196.2	195.2

240 MHz/V.

To compare the performance of the ESDC-VCO, a figure of merit (FOM) defined in Eq. (4.1) is used [3].

$$FOM = 20\log\left(\frac{\omega_0}{\Delta\omega}\right) - 10\log\left(\frac{P_{DC}}{1mW}\right) - L\{\Delta\omega\}, \tag{4.1}$$

where P_{DC} is the DC power consumed in the oscillator. The ESDC-VCO achieves a maximum FOM of 196.2 dBc/Hz at a supply voltage of 0.475V . Table 4.2 summarizes the performance of this work and compares it with recent state-of-the-art high performance VCO's. Plotting the FOM vs. supply voltage, Fig. 4.3, clearly demonstrates the improved

TABLE 4.2: Comparison of Performance of Most Recent High Performance VCO's

	Units	This Work	[15]	[4]	[16]	[17]	[18]	[5]	[19]	[7]
Min Feature Size	μm	0.13	0.13	0.18	0.35	0.18	0.18	0.18	0.18	0.18
Freq./Offset Freq.	GHz/MHz	4.9/3	4.9/3	5.6/1	2.3/1	5.25/1	4.8/1	3.8/1	2.0/1	1.2/3
Tuning Range	%	2.5	14	6.4	3.0	8.0	4.3	3.0	3.0	18
Phase Noise	dBc/Hz	-136.2	-132.8	-114	-135	-127	-120	-119	-123	-153
Supply Voltage	V	0.475	1.0	0.4	2.5	1.0	1.5	0.5	1.25	2.5
DC Power	mW	2.7	1.4	1.1	10	4.2	3.0	0.6	1.0	9.3
FOM	dBc/Hz	196.2	195.5	188.2	191.6	195.2	189.0	193	189.3	195.4

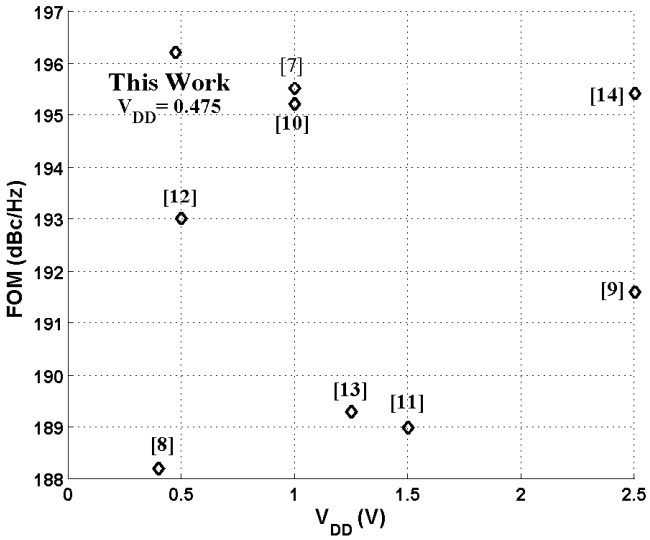


FIGURE 4.3: Comparison of FOM's of VCO's at different supply voltages.

performance at low supply voltages that is achieved by this work.

The amplitude control loop worked successfully to start-up the oscillator and maintain steady state oscillations. The loop functionality was analyzed at a frequency of 10MHz. Table 4.3 shows the measured power for each block in the amplitude control loop. The amplitude control loop consumes between 5-8% of the VCO power.

TABLE 4.3: Amplitude control loop power consumption

Circuit Block	I_{DC} (μA)	V_{DD} (V)	Power (μW)
Peak Detector	85	0.4	34
Comparator	65	0.4	26
Digital State Machine	1	0.4	1
Voltage DAC	100-400	0.4	40-160

5 CONCLUSION

A new enhanced swing differential Colpitts voltage-controlled oscillator (ESDC-VCO) for low-power, low-voltage, low-phase noise applications is described. The enhanced swing allows the VCO to operate at very low supply voltages while enabling a single-ended swing that exceeds the supply voltage and the ground potential. The ESDC-VCO is realized in a 1P8M 0.13 μm CMOS process and operates at supply voltages as low as 0.4V. The figure of merit of the ESDC-VCO is the best reported to date for any integrated LC VCO.

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