AN ABSTRACT OF THE THESIS OF

Benjamin Jann for the degree of Master of Science in Electrical and Computer Engineering presented on September 8, 2005.

Title: Implementation of an Ultra-Wideband Transceiver for Sensor Applications

Abstract approved: _____

Huaping Liu

Ultra-wideband (UWB) radio is the transmission of data using an extremely wide bandwidth and very low power spectral density. In this thesis, the merits and challenges of UWB architectures versus conventional narrowband architectures will be compared. Pulsed UWB systems can be implemented with very simple architectures. These advantages make UWB well suited for short range, battery powered applications where a high bit rate is still needed.

A prototype transceiver for a radio frequency identification (RFID) tag has been developed and its implementation and performance will be discussed. The prototype is used to demonstrate the feasibility of a pulsed UWB architecture and illustrate the advantages of UWB targeted to this application. The design will be covered from architectural choices, component selection, PCB design through lab experiments and optimization.

Implementation of an Ultra-Wideband Transceiver for Sensor Applications

by

Benjamin Jann

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Presented September 8, 2005
Commencement June 2005

Master of Science thesis of Benjamin Jann presented on September 8, 2005.

APPROVED:

Major Professor, representing Electrical and Computer Engineering

---

Director of the School of Electrical Engineering and Computer Science

---

Dean of the Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Benjamin Jann, Author

ACKNOWLEDGEMENTS

First and foremost I give all honor back to the One who gave me the talent and strength to guide me through graduate school.

I would like to thank my wife Monica for supporting me through frustrating nights in the lab and hours at the keyboard with encouragement and back rubs even though she had her own finals to deal with. She always believes in me even when I'm not sure myself. Also if it wasn't for her I would probably forget to eat and sleep.

My appreciation goes out to my advisor Huaping Liu for supporting me both in terms of tuition and guidance through the many hoops one must jump through to graduate.

You wouldn't be reading this right now if it wasn't for the help of Joe Long who showed me how to trick Microsoft Word into doing what I want it to do.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

1 Introduction

1.1 ULTRA-WIDEBAND OVERVIEW

Although the concept of directly radiated pulses using wide bandwidth is far from new, significant research and commercial activities in UWB systems did not occur until February 2002 when the FCC allowed ultra-wideband (UWB) transmission under part 15 rules [4], giving 7.5 GHz of unlicensed spectrum. UWB was originally developed for radar and covert communications out of research into time domain analysis of electromagnetics [2]. So what is UWB? The FCC defines UWB as transmission with a fractional bandwidth of greater than 20 % or an absolute bandwidth greater than 500 MHz. A power spectral density mask as shown in Figure 1 is also given so that UWB signals do not interfere with other devices.

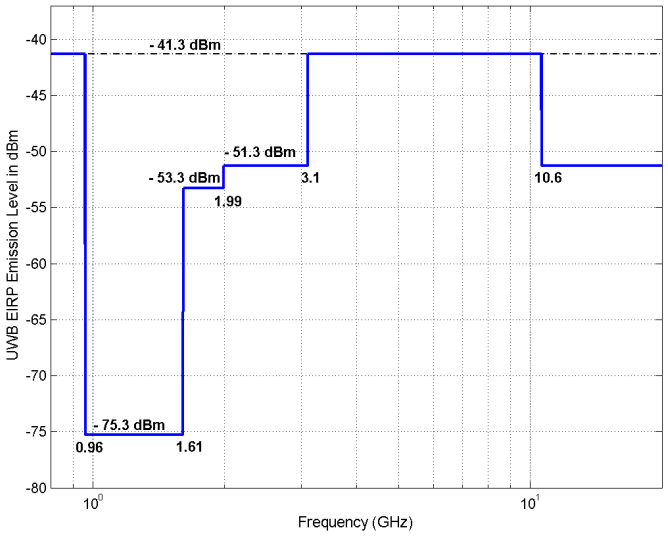


Figure 1: FCC UWB PSD Mask

There are many ways to satisfy these requirements, but this thesis will focus on impulse radio, where data is transmitted by directly radiating short-duration pulses with wide spectrums. Each pulse is shaped to have a power spectral density (PSD) occupying a band of frequencies within the FCC mask. Most devices will be operating between the frequencies of 3.1 and 10.6 GHz as shown in Figure 1. The most popular pulse shape is the Gaussian monopulse, the first derivative of a Gaussian pulse as seen in Figure 2, because of its ease in implementing. However, to satisfy the FCC rule, these "baseband" pulses must be processed, e.g., through carrier modulation or bandpass filtering, before radiation. At the 3.1-10.6 GHz band, the pulse energy is easily radiated when applied to a wideband antenna.

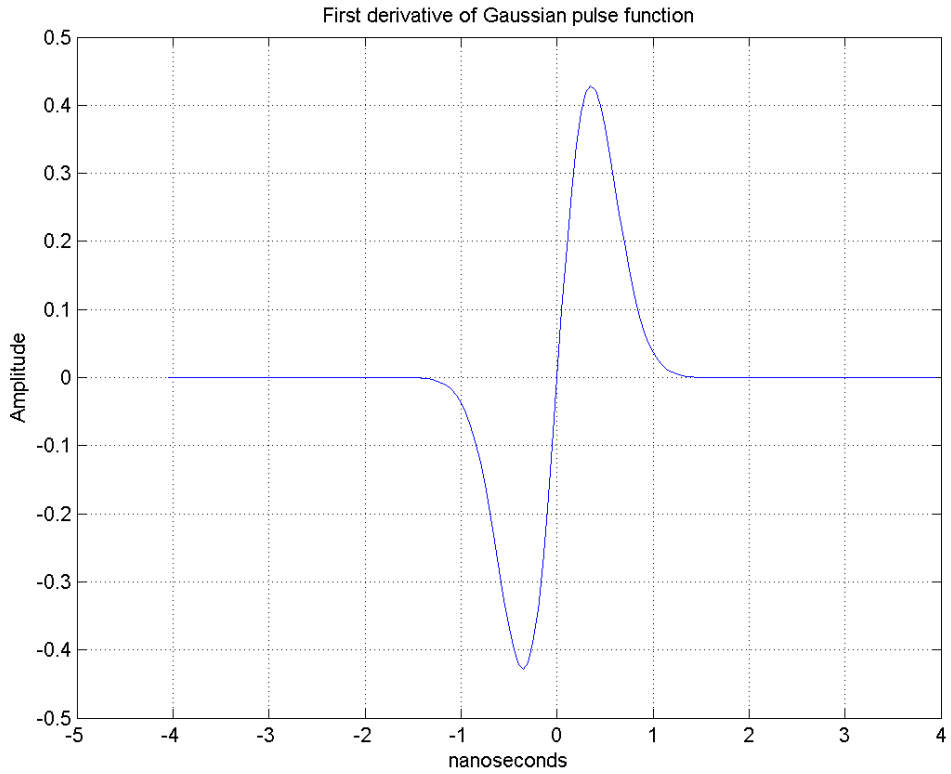


Figure 2: Gaussian Monopulse

1.2 THESIS ORGANIZATION

Chapter 2 outlines the many virtues of UWB and why there has been so much research interest in this area. Chapter 3 covers the challenges facing designers of UWB systems. Chapter 4 compares the different implementations of UWB receivers and transmitters. Chapter 5 provides details of the design of a prototype UWB receiver and chapter 6 shows the lab results from testing the prototype. Chapter 7 discusses improvements to the current design and future areas of research for new designs.

2 Advantages of UWB

2.1 COMPLEXITY, POWER AND COST

The transmit power of UWB is regulated to be very low so as to not interfere with other devices that share the same spectrum. With low transmit power and a lack of mixers, frequency synthesizer or power amplifier, an ultra-wideband transceiver can be designed to dissipate very little power. FCC part 15 rules limit UWB transmission to a power spectral density of –41.3 dBm/MHz [4]. With such a low transmit power, a power amplifier typically is not needed for most applications. This removes perhaps the most difficult and power consuming part of a conventional radio transmitter. The lack of carrier wave removes the need for up and down conversion, which requires mixers and a frequency synthesizer. UWB signals have extremely low duty cycles, typically on the order of one in a hundred or even a thousand, in contrast to conventional radio, which must continuously transmit signals. For the vast majority of the time a UWB transmitter is inactive allowing for power saving measures to be implemented such as a shutdown mode. The receiver can also be designed to dissipate less power in the time between pulses.

As stated above, many components used in conventional narrowband radios are not needed in UWB. This allows for a simple, low component count design. With the decrease in components, there is a potential for a cheap implementation. Another advantage of low component count is that it allows for tighter integration. Single chip solutions allow for further cost reductions and allow for a much smaller footprint. Both of these considerations are becoming very important for today's pocket sized consumer electronics.

2.2 HIGH PERFORMANCE

UWB pulses only occupy a very small portion of the bit period. As long as the delay spread is less than the bit period, signals from one bit should not significantly interfere with another. Delay spreads have been measured to be 5 to 40 ns for UWB [9]. When the pulse repetition frequency (PRF) is low, then the time between pulses is large and the system will have no inter-symbol interference (ISI). For a 40 ns delay spread it is possible to use a PRF as high as 25 MHz. ISI is a major problem in conventional radios where bandwidths are much narrower and tradeoffs between efficient bandwidth use and ISI must be considered. Another advantage of UWB is that due to the short duration of each signal replica, multipath components can be individually resolved and combined to increase diversity gain and received signal energy.

Shannon's formula for the capacity of an additive white Gaussian noise channel gives $C = W \log(1 + \frac{P}{N_0 W})$ where C is the channel capacity in bits per second, W is bandwidth, P is signal power and N_0 is the noise power spectral density. Because the log function grows slowly, the channel capacity increases as the bandwidth is increased. In the case of UWB the channel capacity can be very large even when the signal power is small.

Spread spectrum modulation schemes use more bandwidth than is required for transmission. The advantage to using excess bandwidth is that when the signal is despread, an increase in signal-to-noise ratio (SNR) can be gained. This increase in SNR is called the processing gain. Signals can be spread in several different ways.

One way is called direct sequence, where the data is modulated or multiplied by a pseudo-noise (PN) pattern. Multiplication in the time domain results in convolution in the frequency domain. The spectrum of a PN sequence is spread across a baseband bandwidth equal to the chip rate, or a factor equaling the number of chips per bit. The convolution operation spreads the spectrum of the data so that it uses much more bandwidth. The receiver consists of a correlator and an identical PN-pattern to that used in the transmitter. When time aligned, the normalized PN-pattern multiplied by itself is always equal to unity after an integrator so the original signal is reconstructed. When a narrowband interferer is present, its spectrum is spread and most of its energy is out of band and can be filtered out. The spreading factor, or the factor by which the spectrum has been expanded, gives the reduction of in-band interference. This reduction in interference also equals the processing gain. Another way of spreading the spectrum is frequency hopping, where the frequency of the RF signal is hopped using a PN pattern. In UWB, the signal is spread by using very low-duty-cycle pulses. The narrow pulses have a wide bandwidth and a low power spectral density, far wider than that of either the traditional direct sequence or frequency hopping spectrum systems. Because of the extreme ratio of required bandwidth to actual RF bandwidth needed, UWB is able to attain very large processing gains. In the case of a 1 ns pulse with a pulse repetition frequency of 1 MHz, yielding a bit period of 1 microsecond, the processing gain is 1000 or 30 dB.

Figure 3: Processing Gain

Processing gain in UWB systems can be best explained in the time domain. The pulse energy is concentrated over a very short time period, whereas the noise or interference energy is spread evenly over the bit period. Using synchronization it is possible to look at the signal only during the pulse period. During this window, the SNR after a matched filter is increased by the processing gain. It can be seen in Figure 3 that there is very little overlap of noise over the pulse duration, Tp. The total pulse energy is $A_p^2 T_p$. If the noise is multiplied by a template pulse, such as in a correlation receiver, only the noise during the duration of the pulse is left because of the multiplication by zero outside of the pulse duration. This leaves the noise energy to be $A_n^2 T_p$. If signal energy is divided by the noise energy the result is $\frac{A_p^2}{A_n^2}$. To compare a system with an equivalent received signal power with the exception that pulse energy is spread over the entire bit period then the SNR would be calculated as

follows. Because the total signal energy must be equivalent when comparing systems, the signal energy remains $A_p^2 T_p$. The difference is that the noise is now active during the whole bit period with energy of $A_n^2 T_n$. The SNR is $\frac{A_p^2 T_p}{A_n^2 T_p}$. The new SNR is the same as the previous one except that the UWB SNR is a factor of $\frac{T_n}{T_p}$ better than the normal SNR. This is the processing gain of UWB.

2.3 UNLICENSED SPECTRUM

In the United States, the FCC has allocated the 3.1 GHz to 10.7 GHz band for UWB without license. To implement a UWB network, there is no need to purchase expensive spectrum similar to IEEE 802.11 WiFi, which uses the unlicensed industrial, scientific, and medical (ISM) band. In contrast, the 3G mobile wireless spectrum has been auctioned off for billions of dollars in the US. With the explosion of WiFi and the less than enthusiastic roll out of 3G wireless, it is easy to see why there is excitement about the current regulatory environment for UWB.

2.4 PRECISE RANGING

Because of the fine temporal resolution of very narrow pulses, it is possible to locate objects with very fine spatial resolution. Originally UWB was used for radar applications because of this property. If the pulse is considered to move at a velocity through air of 0.3 meters/ns, a sub-nanosecond pulse can achieve a spatial resolution of better than 30 cm.

3 UWB Challenges

3.1 REGULATIONS

The power spectral density of UWB is regulated by the FCC to be extremely low. The drawback of low power transmission is that either the pulse rate must be lowered to increase processing gain and energy per pulse, or the range must be limited to very small distances. The result of this is that pulse amplitude cannot be continually increased while reducing the pulse repetition frequency to meet the average power density limit. Outside of the US UWB has not been given spectrum yet. Until other regulatory bodies around the world set policies for UWB, there will not be much traction in developing systems for those markets.

3.2 SYNCHRONIZATION

Very low duty cycle signals make synchronization very difficult. Common synchronization schemes work by calculating the timing of a rising or falling edge in the signal. UWB signals have low duty-cycles and edges do not occur frequently. This gives much less information for synchronization algorithms to work with. Another difficulty with UWB related to synchronization is that for many receiver architectures it is essential to have accurate timing. In the case of analog correlation the timing must be close to perfect or the signal will be lost completely. If a pulse is 1 ns wide and the majority of the pulse energy is near the center of the pulse then timing inaccuracies on the order of picosecond could cause significant loss of signal power or the signal could be lost completely. Given that the pulse repetition period is 1 μs, timing needs to be accurate to near 10 parts/million. With such fine time increments

needed to synchronize the receiver to the received pulses, it is not feasible to sample the data fast enough to use digital algorithms. Analog methods such as a phase lock loop are necessary.

3.3 STRINGENT COMPONENT REQUIREMENTS

UWB may have a low component count but the components that are needed have very stringent requirements. A major advantage of narrowband systems is that they can leverage resonant circuits at a single frequency to obtain high gains, low noise figures and selective filters. Broadband circuits are difficult to design and often require resistors and the thermal noise and power dissipation that comes with them. Designing filters with GHz of passband and flat frequency responses is extremely difficult and requires complex circuits. Antennas also need to radiate efficiently across a wide band and maintain a flat frequency response. Because UWB requires time domain processing and fine temporal resolution, phase response is also very important. If the group delay is not flat across the band of interest distortion will occur and the signal will be dispersed in time. UWB not only requires large bandwidths, but operates at high frequencies, requiring carefully impedance matching. Matching 50 ohms across the entire band of interest is difficult and will again often require noisy resistors. Another inherent property of UWB signals is that they have a very large peak-to-average-power ratio (PAPR). Components are much less linear at high signal amplitudes and will introduce distortion. Large amplitudes also require higher power supply voltages, which may limit process choices for integrated circuits. CMOS technology is by far the cheapest method to manufacture integrated circuit. As

CMOS is scaled ever smaller the supply voltages continue to shrink and may not be able to process the large amplitude signals required of UWB. Lastly it is important to keep components in their linear range as discussed above so automatic gain control (AGC) is needed to keep a relatively constant amplitude. Fading is a problem with wireless channels and is due to Doppler shift and multi-path. The received signal will change power level during operation and it is important to compensate. However when the signal is on during a small fraction of the time it is practically impossible to measure and compensate for power changes with analog circuitry. Decision based algorithms can be used by measuring the false alarm rate and increasing power gain until the rate drops to an acceptable level. This method requires knowledge of the bit error rate at the receiver, which can only be done if a known signal is transmitted. Attaching a predetermined preamble to each data frame sent is one way of sending known data. Much of the cost savings of UWB will be lost through solving the design challenges of these difficult components.

4 Comparison of UWB Transmitter and Receiver Architectures

4.1 MULTIBAND

Conventional radio frequency (RF) and spread spectrum methods can also be used to implement a UWB system. The UWB spectrum can be divided into sub-bands as long as the bands are larger than 500 MHz to meet FCC regulations. Each band could be further divided into separate equally spaced sub-carriers [11]. Direct sequence spread spectrum or frequency hopping can be used to spread the spectrum and reduce lines in the spectrum. This thesis focuses on impulse radio technology but UWB camps seem to be evenly divided on whether a multiband OFDM or an impulse radio will be the dominant form in the future.

4.2 ALL DIGITAL

The all-digital receiver consists of an antenna to receive the signal, a band-pass filter to remove out of band noise and to prevent aliasing, a low noise amplifier to boost the signal so that an analog-to-digital converter (ADC) can digitize the signal. After the signal has been digitized all processing is done with a digital signal processor (DSP) including matched filtering or correlation. Advantages of all-digital receivers include low part count and flexible signal processing. The receiver can be reconfigurable in software adding further flexibility to the design. The all-digital architecture can combine multipath components to increase signal power using a RAKE receiver architecture. Another benefit of the digital receiver is that channel estimation and equalization may be done to remove distortions in the signal due to the channel. The major detracting feature of the all-digital receiver is the necessity of a

super fast ADC. UWB pulses have major spectral contents up to 4.6 GHz in our system. In order to sample at the Nyquist rate the ADC would have to be capable of at least 8.2 GSps, far beyond the capabilities of a standard processor or off-the-shelf component. To process the signal digitally after sampling requires significant computational power. It may be quite some time into the future before components can be made to meet the specifications required for the ADC and DSP in this architecture.

4.3 ANALOG CORRELATOR RECEIVER

A matched filter receiver is theoretically optimal for an additive white Gaussian noise channel. A matched filter can be implemented using correlation. As discussed for the all digital receiver, sampling a UWB signal is not yet reasonable. Correlating the signal using analog, continuous time techniques can be done with much less difficulty. In this receiver implementation the correlator is moved from the digital domain to before the ADC in the analog domain. The pulse template must also be analog, requiring a pulse generator in the receiver. When correlating over an entire pulse period it is possible to combine multipath components to improve signal power. Another advantage is that an ADC that samples at the pulse rate can be used, drastically relaxing the ADC requirements. Disadvantages of this architecture include the use of high speed analog correlators and template pulse generators that can consume significant power. Because correlation is done in the time domain it is important that the group delay of the analog components is flat across the band of interest or distortion will occur. Another problem with the analog correlator receiver

is that the local pulse template will not exactly match the distorted received pulse, reducing correlation between the two. Probably the most difficult area of design in the analog correlation receiver is synchronization. If the template pulse is not very precisely synchronized with the received pulse correlation will be reduced. Synchronization is especially important with a pulse position modulated signal, where pulse timing determines the bit value. To improve correlation many pulses can be used for one bit at the cost of a reduced bit rate. This architecture is well suited for integration in a standard process but unfortunately standard off-the-shelf parts could not be found. Creating a PCB layout to accommodate the stringent timing requirements would be difficult.

4.4 ANALOG PULSE DETECTION

Analog pulse detection is perhaps the simplest implementation of a UWB receiver. Pulses are received from the antenna, filtered, amplified and then a simple threshold detector is used. The lack of ADC and DSP can significantly reduce complexity, power and cost. Another benefit is that this receiver can be implemented in current off-the-shelf components, eliminating the need for custom integrated circuits. With such simplicity and availability of components, this receiver has the potential to be the cheapest and lowest power. The analog pulse detector is also capable of detecting a bit for every pulse. The drawback to using a pulse detector is that it is not possible to collect multipath energy. With less energy available, the range or bit rate must be reduced to maintain the same error rate. Another requirement for the analog pulse detector is that a very high speed comparator is needed. Once the

comparator converts the signal to digital it must latch the signal until lower speed digital logic can clock the data. Processing gain is dependent upon precise synchronization so that the detector is desensitized to false triggers when a pulse is not expected. This receiver is also susceptible to interference from other UWB transmitters.

4.5 OTHER RECEIVER IDEAS

Some other ideas to get around the high sampling requirements of the all-digital receiver and stringent analog specifications of the other receivers have been suggested. Due to the fact that the signal is bandpass in nature it is possible to use sub-sampling to convert the bandpass signal to baseband. If the sampling rate is chosen correctly a bandpass signal can be sampled at twice the bandwidth instead of twice the highest frequency content with no aliasing. The upper or lower frequency band must be chosen to be an integer multiple of the signal bandwidth. A drawback to this method of downconversion is that the signal may only occupy a single band but noise and interference will not. Signals outside the band of interest will be aliased into the signal band [14]. Although the ADC sampling requirements are somewhat relaxed by this method, they are still extremely high. Sampling at twice the signal bandwidth of a 1 GHz signal requires a 2 Gsps ADC.

A single ADC may not be able to sample the signal fast enough, but a bank of ADCs in parallel with each sampling instant skewed from the others can accomplish sampling at the Nyquist rate [8]. The drawback to this type of sampling is that it is very difficult to get the timing between ADCs correct. Also the power consumption of

many ADCs will be very high. Another idea is to break the signal into frequency bands with a filter bank. Each band can be downconverted and processed separately at a much lower sampling rate. If the filters allow only one frequency through sampling can be done in the frequency domain and the filters can be much more easily implemented [8].

4.6 TRANSMITTER ARCHITECTURES

One of the advantages of UWB over conventional narrowband architectures is the simplicity of the transmitter. There is no need to upconvert the signal and the low transmit power removes the requirement for a power amplifier. Designing a UWB pulse generator can be a difficult task however. One possible pulse generator architecture uses a step recovery diode and a short circuit transmission line. Digital data triggers the step recovery diode on during its rising edges. This generates a pulse that travels down the short-circuited transmission line and is reflected back. The reflected pulse has the opposite polarity as the original pulse and cancels the original pulse when it returns to the input, creating a very narrow pulse with a duration equal to twice the propagation time of the transmission line. The difficulty with using step recovery diodes and transmission lines is that both cannot be easily integrated into a standard silicon CMOS process.

The Gaussian monopulse waveform can be approximated as a positive digital pulse followed by a negative pulse. The two pulses are combined using a differential mixer to create the monopulse. The opposite monopulse polarity can be generated by reversing the order of the positive and negative pulses [10]. The approximation will

not have as flat a spectrum as an ideal monopulse but has a major advantage in its ability to be implemented in IC form.

4.7 MODULATION SCHEMES

4.7.1 On-Off Keying

On-Off Keying (OOK) is the simplest modulation scheme to implement. A digital '1' is implemented by the presence of a pulse where the absence of a pulse represents a '0'. Because the pulse polarity and phase are constant OOK only needs a minimum of circuitry. OOK is a good solution for non-coherent receivers where only the signal energy is detected over a bit period and the phase and timing of the signal are ignored.

4.7.2 Biphase Modulation

Biphase modulation (BPM) is implemented by transmitting either a positive pulse or a negative pulse each pulse period. A positive pulse represents a '1' whereas a negative pulse represents a '0'. BPM performs 3 dB better than both OOK and pulse position modulation because of the larger distance in signal constellations [10]. BPM requires two pulse generators, one for the positive pulses and one for the negative pulses. The signal is demultiplexed between the two pulse generators depending on the bit value. The major drawback is easily the fact that the transmitter requires twice the hardware.

4.7.3 Pulse Position Modulation

Pulse position modulation (PPM) encodes the data in the timing of the pulses. If a pulse is transmitted early in reference to a standard timing it represents a one. If a pulse is late then it represents a zero. This modulation scheme has been implemented in the Time Domain Corp. PulsOn chipset. PPM requires very accurate synchronization to be able to detect a late or early pulse. The transmitter has the added requirement of an accurate timer to shift the pulse early or late.

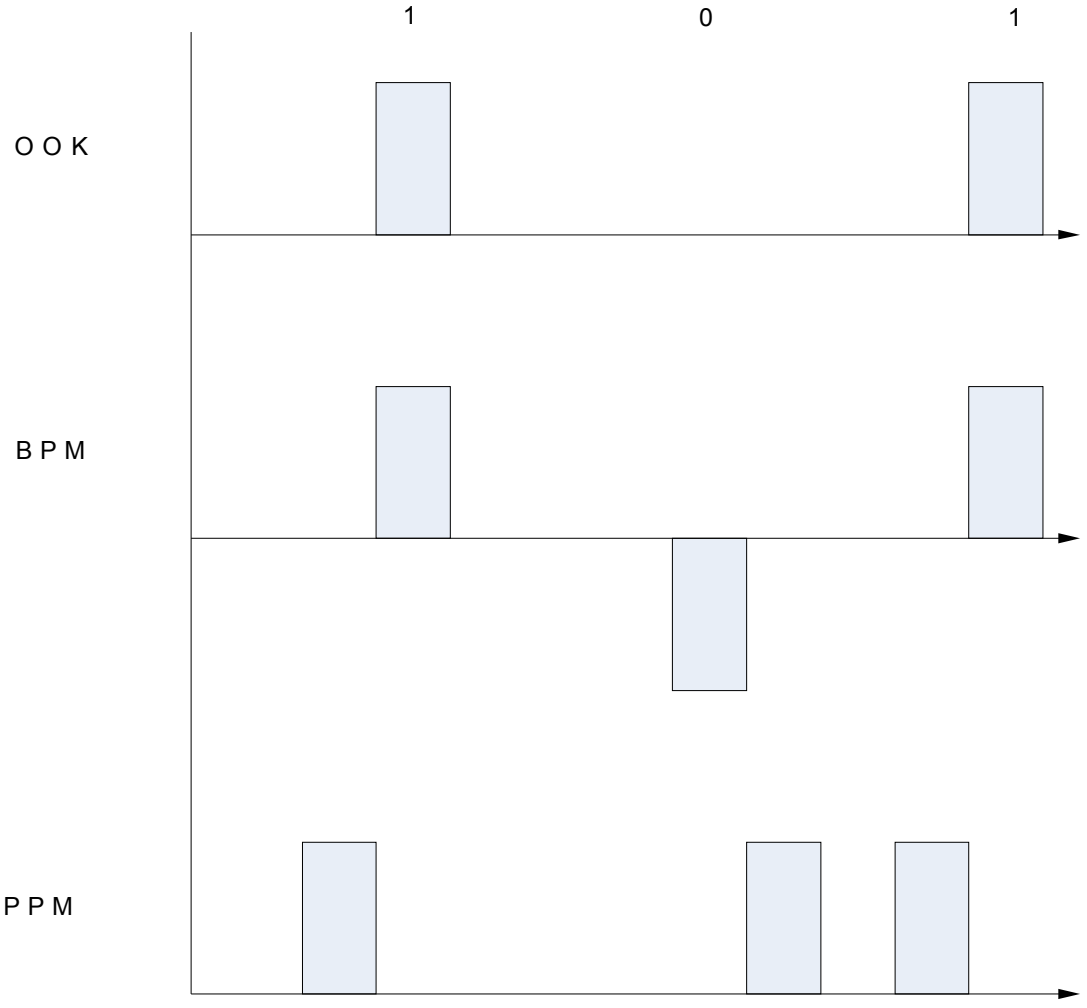


Figure 4: Comparison of Modulation Schemes

4.7.4 Multi-Access

In order for a network to allow multiple users, it is important that each user doesn't interfere with the others. Two ways to provide for multi-access are direct sequence spread spectrum and time hopping. As described previously multiplying a signal by a PN sequence will make the signal look like noise except for receivers with a matching PN sequence. In the case of UWB each bit is multiplied by a PN sequence to generate 2^N chips. Each chip is transmitted as a pulse modulated by the PN sequence most likely using BPM. Another multi-access method is time hopping. The time period in which a pulse is expected is modulated using a PN sequence.

Perhaps the simplest way to allow a small number of users to operate at once is frequency division multiplexing. The UWB spectrum is split into separate frequency bands that each transmitter can operate in. Because of the wide bandwidth required for each transmitter, not many bands would be available. This scheme also requires different filters for each band.

5 Design of a Prototype UWB Transceiver

5.1 APPLICATION

The specific application for the transceiver design is an RF identification tag. The tag will be used in metal containers so multipath will be significant. In order to be used at a distance, the system needs to operate at a range of up to 10 meters with a BER of 10^{-5} or less. A data rate of 1 Mbps was chosen to allow for sufficient bandwidth even after coding overhead is added. Because the tag is battery powered it is very important that it consumes as little power as possible to extend its life. It is also a design goal to make the cost as low as possible. 50 milliwatt or less is acceptable. Lastly, it is important that the entire tag have a small footprint. A target of 2 square inches or less is desired.

5.2 LINK BUDGET CALCULATIONS

Before design of a wireless system starts it is important to calculate a link budget. A link budget takes the transmitted power and adds gains and subtracts losses. Losses include path loss through the wireless channel and component losses in the receiver as well as degradations in the signal to noise ratio (SNR). The remaining quantity gives the margin of SNR. Without sufficient SNR a receiver will not work. The transmitted power can be calculated by multiplying the power spectral density of –41.3 dBm/MHz, regulated by the FCC, by the system bandwidth of 1000 MHz. The resulting transmitted power is –11.3 dBm.

Much research has been done in creating empirical channel models for UWB. One path loss model gives the path loss as $PL(d) = PL_o + 10\gamma \log_{10}(\frac{d}{d_o}) + S$ where d is the distance from the transmitter, PL_o is the path loss at a reference distance, γ is the slope of the average loss with dB distance, d_o is a reference distance and S is a zero mean Gaussian random variable that gives the deviation in path loss from its median value [9]. Using a network analyzer and two UWB antennas a meter apart the path loss was measured to be 40dB at 3.6 GHz, the center frequency of the signal. For a non-line of sight (NLOS) application in a commercial setting γ is 2.95 and to simplify the equation S is set to zero, its mean value. Using these values the path loss at 10 meters is 69.5 dB. The signal power at 10 meters can be calculated as the transmitted power minus the loss of the channel to be –80.8 dBm. The power spectral density of the noise at the receiver input is –174 dBm/Hz. The total noise power at the receiver input can be found by multiplying be the bandwidth in Hertz giving –84 dBm. The resulting SNR is calculated by subtracting the noise power in dB from the signal power, which gives 3.2 dB. The SkyCross antennas used in the prototype have a gain of 1.1 dB to 2.2 dB across the frequency band of interest. The center frequency has a gain of 2 dB and will be used for this analysis. If a method is used to sensitize the receiver to pulses only during the expected pulse time, processing gain can be achieved as discussed earlier. If the processing gain is 30 dB then the SNR will be increased to 35.2 dB. Devices in the receiver generate noise and degrade the SNR. Noise near the input to the receiver is the most critical because it will get amplified through the rest of the

receiver along with the signal. This is why it is important to have a low-noise amplifier (LNA) near to the input of the receiver. The LNA will boost the signal and only add a small amount of noise of its own. Noise figure is a measure of the degradation of SNR and is defined as $10\log_{10}(\frac{SNR_{in}}{SNR_{out}})$. The noise figure of a filter is simply the insertion loss. The Tiayo Yuden 3.1 to 4.6 GHz filter used has an insertion loss at the center frequency of 1.68 dB. The Picosecond Pulse Labs amplifier has a noise figure of 7 dB. Without a reliable model for the tunnel diode it is impossible to predict the noise figure for this part of the receiver. Tunnel diodes are supposedly low-noise devices, so for this analysis its effect will be neglected leaving a slightly optimistic number for overall noise figure. In order to calculate the total system noise figure, the gain of each stage must be taken into account. The total noise factor can be calculated, assuming each stage is matched, by $NF_{tot} = NF_1 + \frac{NF_2 - 1}{A_{p1}} + ... + \frac{NF_m - 1}{A_{p1}A_{p(m-1)}}$ where NF denotes the noise factor or linear noise figure of each stage and A is the power gain of each stage [12]. It can be seen from the equation that large gains in the beginning of the chain reduce the overall noise factor. The noise figure for the prototype receiver is calculated to be 8.7 dB. Now the link margin can be calculated as the excess SNR left. There is 26.5 dB of link margin with the full processing gain and no noise attributed to the tunnel diode. If the synchronization is less than 100% and the diode noise is significant then this number will drop. As it is there is plenty of margin for other unforeseen non-idealities. However if no attempt is made to design

in circuits to add processing gain then there will be no SNR left and the system will not work at the intended range of 10 m.

5.3 PROTOTYPE ARCHITECTURE AND IMPLEMENTATION

5.3.1 Comparison of Architectures for RFID Application

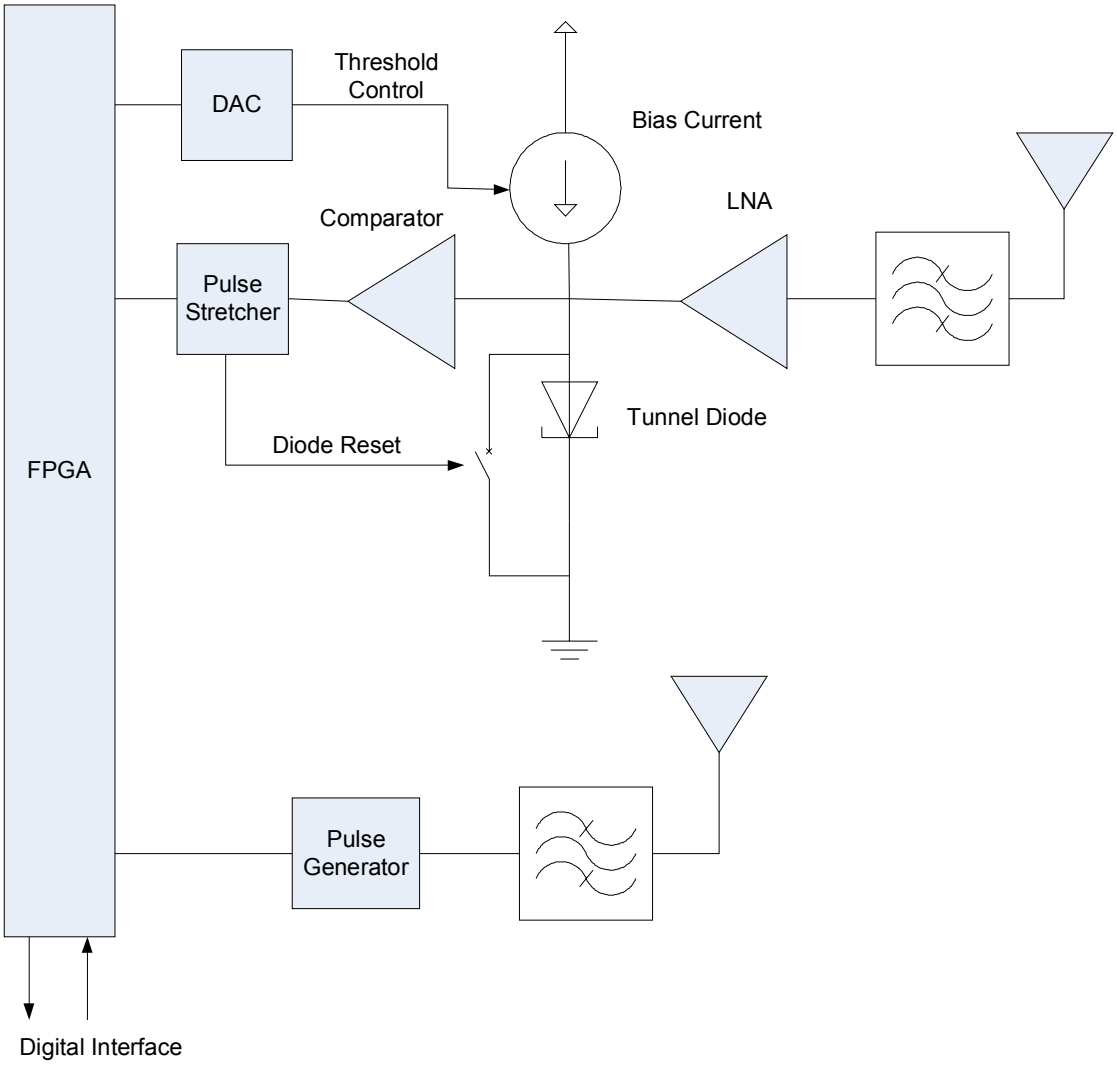


Figure 5: Complete Transceiver Architecture.

The implementation was chosen to meet the design goals and specifications discussed previously. Another deciding factor was the limitation to currently available off the shelf discrete components. With these design parameters the best architecture for this application was chosen to be the analog pulse detector. Current ADC technology does not allow Nyquist rate sampling of the signal. This rules out using an all digital receiver.

Analog correlators could be implemented using high speed mixers. Most mixers are designed for narrowband applications and not well suited for the frequencies needed for a UWB receiver. Another difficulty would be the requirement of generating a local pulse template that is perfectly matched and in phase with the received pulse. The precise nature of the timing would require very exact PCB trace lengths making the routing of the PCB difficult. Even with precise trace delays on the PCB, a complex timing recovery algorithm would need to be implemented to initially calibrate the template phase to match that of the received pulse. This receiver architecture is much better suited for implementation in a custom IC, which is too costly for this project. The template pulse generator and mixer would consume a significant amount of power making it difficult to meet the power budget.

Given the above constraints the optimum architecture for this application is the analog pulse detector. This architecture is well suited for discrete component implementation and parts are readily available. Without power hungry ADCs or correlators, the receiver can be designed to consume little power. Without the cost of custom parts the receiver can be manufactured at a low cost.

For the prototype transceiver a MultiSpectral UWB pulse generator was purchased to generate the UWB pulses. The pulse generator is edge triggered and will generate a pulse on the rising edge of digital data. The output pulse is a Gaussian monopulse with peak amplitude of 6V, a duration of less than 1 nanosecond and has a wide PSD. In order to be compliant with the FCC part 15 power spectral density mask a bandpass filter was used with the passband spanning 3.1 to 4.6 GHz. After filtering, the pulse amplitude is reduced to 600 mV because much of the signal power is out of the band of interest. The signal is then radiated using a UWB antenna from SkyCross.

On the receive end an antenna identical to that of the transmitter is used to captured the radiated energy. Next in the receive chain is a bandpass filter, also identical to the one in the transmitter. The bandpass filter removes out of band noise and sets the noise power for SNR calculations. After the filter is a Picosecond Pulse Labs amplifier. The amplifier has a gain of 22 dB and a bandwidth of 8.5 GHz. After the amplifier the signal is boosted to levels where it can be processed by less sensitive devices. All devices are connected together via SMA coaxial connectors. Following the amplifier is the prototype receiver PCB.

5.3.2 Tunnel Diode

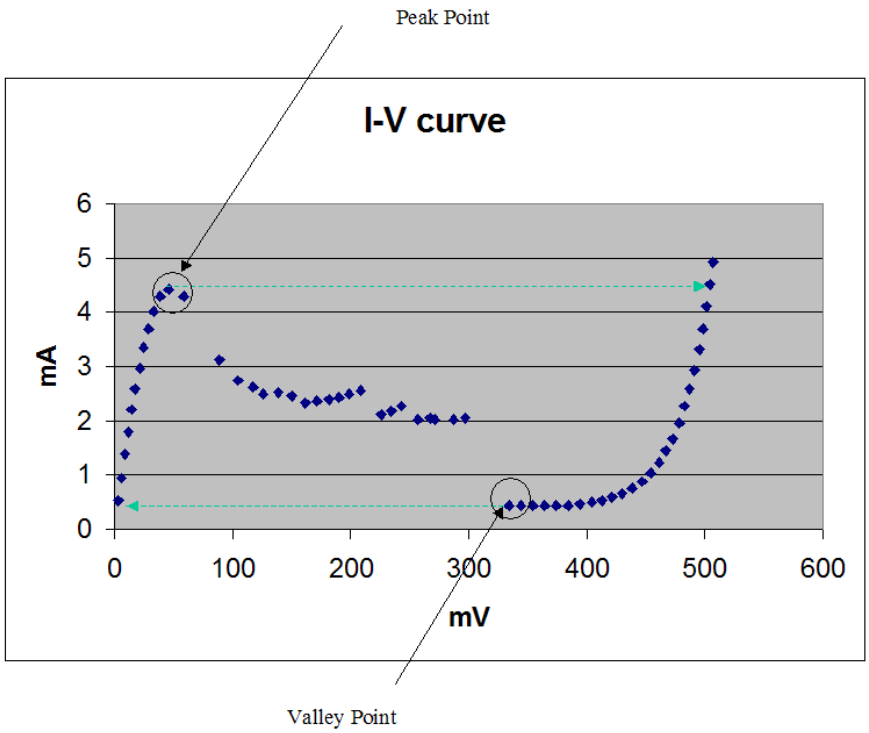


Figure 6: Tunnel Diode I-V Curve.

The heart of the analog receiver is the tunnel diode. A tunnel diode is able to perform ultra-high speed comparator operations and latching. The tunnel diode has been used as a pulse detector going back to some of the first implementations of UWB for radar [2]. A tunnel diode has a normal current to voltage (I-V) curve for a diode

with the exception of a current peak due to quantum tunneling before the exponential diode behavior dominates. The semiconductor material is heavily doped compared to a normal diode to encourage tunneling [1]. Figure 6 is an I-V curve measured from a 1N3717 tunnel diode from American Microsemiconductor. This particular diode has a peak current of 4.7 mA and a valley current of 0.6 mA. After the peak there is a negative resistance region because of the falling slope of the I-V curve. Negative resistance creates instability and leads to fast switching times but can also be used to create oscillators, intentional or otherwise. Measurements of the diode characteristics in this region are difficult because oscillations will build and give erratic readings by the voltmeter as seen in Figure 6. Another use for this I-V characteristic is to create a comparator. The tunnel diode is not stable in the negative resistance region and will move to the nearest stable region to the right or left of the curve in a small amount of time. If the diode is biased at a current near the peak current, a small amount of signal will push the diode from the lower stable state to the higher state causing a large jump in the voltage across the diode. As seen in Figure 6, the peak voltage is about 60 mV. When the diode jumps to the same current level on the high side of the curve the voltage across the diode is 510 mV. When a received pulse or noise pushes the diode from the low to the high state, a voltage step from 60 to 510 mV is output. The threshold of the comparator is set with a bias current. If the diode is biased exactly at the peak point and signal including noise will trigger the diode into the high state. In order to reduce the rate of false triggers the bias can be lowered so that larger amplitude signals are needed before the diode is pushed into the high state. Once in the high state the current must be pulled below the valley current

before the diode will reset to the low state. In the case of the 1N3717, the diode current must be nearly completely shut off before the diode will be reset. This behavior is useful in generating a latch. An equivalent comparator and latch may be found implemented in ECL logic but the sensitivity, noise and speed would be lower and the power dissipation would be significant. The Analog Devices ADCMP567 comparator is capable of detecting a pulse with 200 picosecond minimum pulsewidth but dissipates 858 mW of power. The latching circuitry also requires more ECL logic to implement the reset. Clearly the power dissipation of this solution is unacceptable for battery powered applications where each milliwatt is precious. An equivalent tunnel diode circuit can be designed with a bias current of 4.7 mA, dissipating 14 mW from a 3 volt supply. Tunnel diodes with peak currents of 1 mA are also available further reducing power consumption. Another advantage of the low component count is that noise is reduced.

5.3.3 RF Issues

The tunnel diode receiver design is not without its difficulties. As with all high frequency designs, impedance matching is critical. The trace from the SMA connector to the tunnel diode was designed to be 50 ohms. FR-4 board material was used with a dielectric constant of 4.6. Copper thickness on the outer layers is 1.25 ounce copper per square foot or 43.75 micron. The dielectric spacing of the outer layers is .012 inches. This information was entered into Agilent ADS's Lincalc and it was calculated that the trace width for a 50 ohm line is 0.022 inches. The loss tangent of FR-4 at GHz frequencies is about 0.012. Because FR-4 is very lossy at high

frequencies it is best to keep traces as short as possible. A board material with better loss characteristics such as GeTek or one of Rogers Corporation's materials could be used, but would lead to a much higher cost. To reduce reflections, the end of the transmission line should be matched to the impedance of the line. The tunnel diode has a very low impedance so a series resistance can be added to terminate the line. Stubs on the transmission line will also create reflections so it is important to terminate the line as close to the end as possible. The leads of the tunnel diode were cut short so that the stub length would be less than a wavelength of 6 cm. To test the impedance matching of the board a TDR was used. The board interfaces to the LNA and filter through an edge mounted SMA connector. The edge mounted connector maintains a constant 50 ohm impedance from the cable to the board trace and it is important not to add too much solder to the middle conductor. From the TDR there is still some discontinuity at the SMA but the termination is very well matched. The board stack up for the design was a 4 layer board with signal layers on the outside and DC plane layers on the inner two layers. The board was fabricated by ExpressPCB.

Another important PCB design issue is to make sure the power supply is free of noise. The board is powered from a DC power supply via wires that can pick up radiation in the room. After the supplies are attached to the board with terminal blocks they are connected to power plane layers through a large inductor to remove any AC signals. A large 4.7 μF capacitor shunts the supply to give a low impedance path for AC noise. For each IC on the board a ceramic 1 μF capacitor was used near the power pin to maintain a ripple free supply for each part and isolate noise from one part to another.

5.3.4 Reset and Threshold Circuit Design

The tunnel diode detector's threshold is set by setting the bias current near the peak point of the I-V curve. The closer to the peak point the more sensitive the receiver is. Unfortunately if the detector is made too sensitive it can have false triggers due to noise. The optimal threshold is set where the occurrence of a false trigger due to noise is rare so that a BER of 10^{-5} is achieved. Noise sources can vary in power over time so it is important to design an adaptive circuit to set the threshold. Another important part of the tunnel diode design is a circuit to reset the diode back into the low state. Because the tunnel diode has such a large amount of hysteresis it must be shorted to ground for a time interval long enough to remove all charge from it. Once the diode is reset it must be restored to normal bias conditions to arm it to trigger on the next pulse. If the reset is released too hard or the bias circuit is abruptly switched back without removing any residual voltage it is possible that the diode will retrigger to the high state. To reset the diode it must be shorted to ground. The switch must let microwave frequencies through when on and pull the diode all the way to ground when off. Another requirement of the switch is that it must be able to switch on and off several times in one micro-second. Relays are not able to switch fast enough so a semiconductor switch is a requirement. Galium-Arsenide switches can have a very flat frequency response over large frequencies. However they can be fairly expensive. CMOS switches have begun to allow bandwidths in the gigahertz and cost more than an order of magnitude less. The Analog Devices ADG902 offers a -3dB bandwidth of 4.5 GHz. Unfortunately, the frequency response rolls off somewhat over the band of interest and may cause some distortion by attenuating the

higher frequency part of the signal. Insertion loss will also cause a loss of signal power and reduce the signal to noise ratio and sensitivity.

5.3.5 Current Source Design

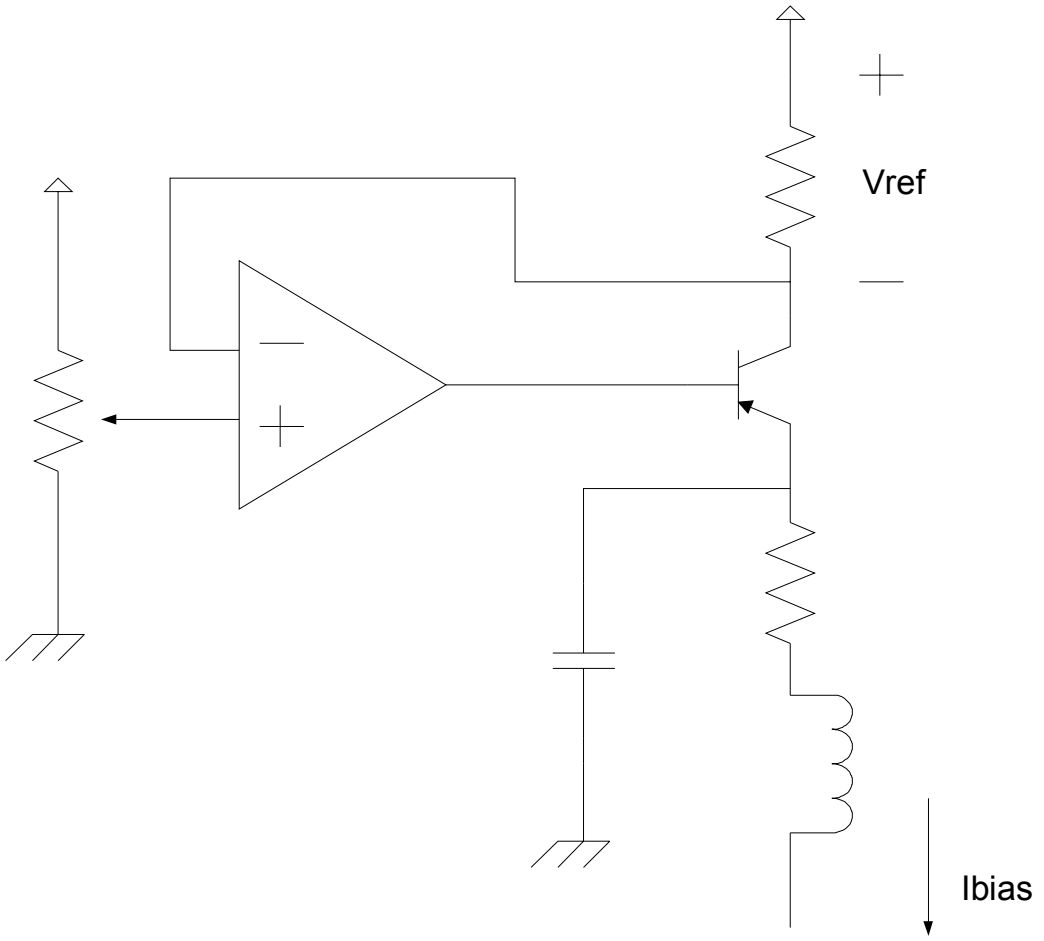


Figure 7: Current Source.

Bias current is generated by setting a reference voltage across a resistor. Two current circuits each similar to Figure 7 are connected in parallel to sum to one current. One current is a course adjust, the other is used for fine adjustments. This arrangement allows small adjustments and allows the threshold to be set as close to optimal as possible. The reference voltage is maintained across the resistor using a

circuit that senses the voltage across the resistor, compares it with the reference voltage using an op-amp and drives a transistor to set the current through the resistor. The reference voltage can be set using a potentiometer or a DAC. Initially to test the circuit the potentiometer was used. Later the DAC can be used as part of the adaptive threshold feedback loop. A bias tee was designed so that RF power would not leak into the current source and bias current would not leak into the RF path. A 1 microfarad capacitor was used as a DC block connecting the RF input from the SMA connector to the diode and two 0.1 micro-Henry inductors were used as a RF choke to connect the current source to the diode. At the lowest signal frequency, 3.1 GHz, the impedance to the capacitor is only $\frac{1}{2\pi fC} = 5x10^{-5}$ ohms and is effectively a short circuit. At the lowest frequency the inductors have impedance of $2\pi fL = 1948$ ohms each, which is much larger than 50 ohms and only a small fraction of the RF signal will take this path. The series resistance of the inductors is 6 ohms so the voltage drop will not affect the bias circuit. Another important parameter is the self resonant frequency. This is the frequency at which the inductive reactance is equal to the parasitic capacitive reactance. After this frequency the impedance of the inductor begins to drop and it loses effectiveness as a RF choke. The inductors used have a self resonant frequency of 1 GHz so the actual impedance will be somewhat smaller than calculated above but still much greater than 50 ohms. A 10 ohm sense resistor was added in series with the inductors so that the bias current could be measured by dividing the voltage across the resistor by 10.

5.3.6 Digital Conversion

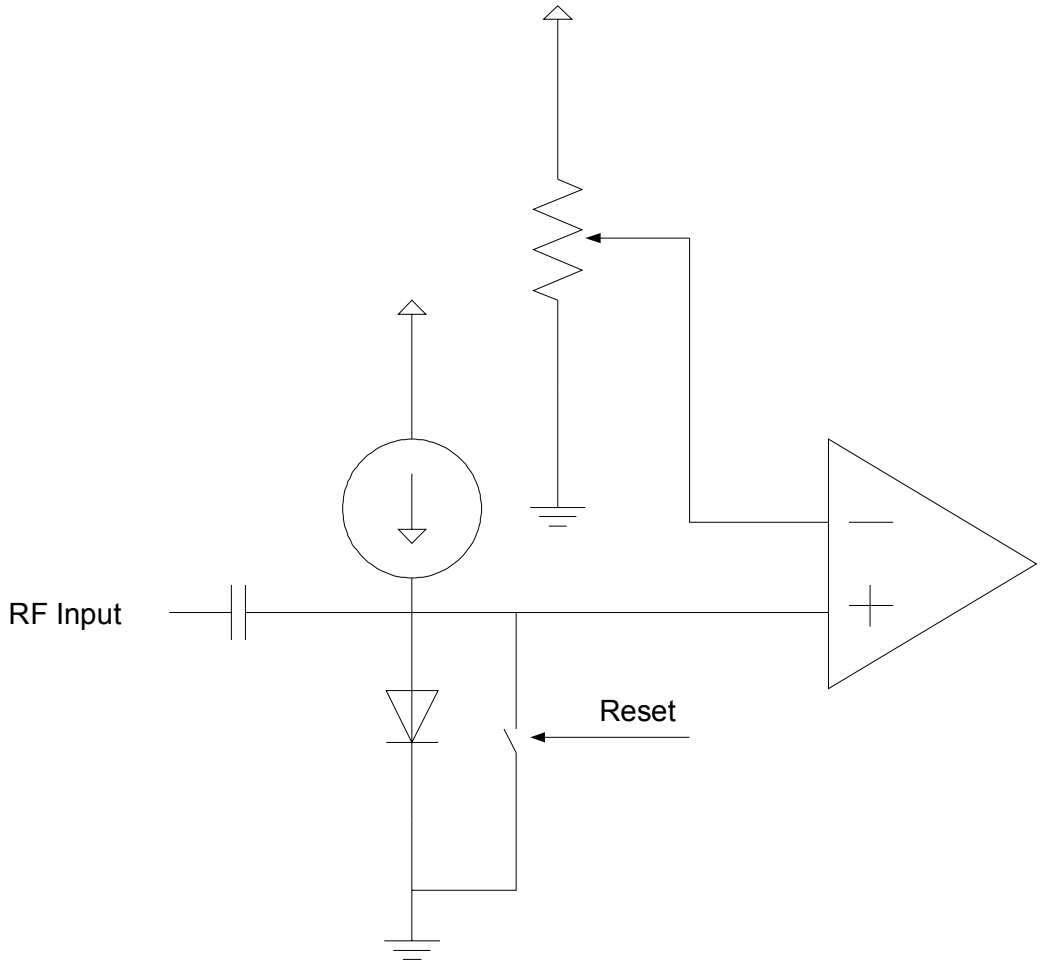


Figure 8: Comparator Circuit

After the tunnel diode, a comparator converts the signal to digital levels. The tunnel diode voltage is compared to a reference voltage provided by a potentiometer. The reference voltage is set between the low and high states of the diode, typically 200 mV. When the diode is in the low state a digital '0' is output and when the diode is in the high state a digital '1' is output. The key requirement of the comparator is that it should be able to switch faster than the bit rate. The Maxim MAX999 comparator only consumes 5 mA of current from a 3.3V supply for a power dissipation of 15 mW.

For applications where the system can be put into sleep mode a version of this comparator is available with a shutdown mode.

Once the signal has been converted to digital levels, the pulse is extended so that processing can be done at a lower frequency closer to the bit rate. The pulse is stretched using a monostable multivibrator or "one shot". The operation of the one shot is as follows. When a rising edge is detected the output goes high. An RC circuit is discharged to a known voltage level. The RC circuit is then charged up according to the RC time constant of the circuit. Once the RC circuit has been charged above a threshold, the output of the part goes low again. The timing of the output pulse can be set by calculating the RC product. The resistor was implemented using a potentiometer so the output pulsewidth can be tuned. The Toshiba TC7WH123 is capable of detecting input pulsewidths as small as 5 ns. After the pulse has been extended, it is used for the tunnel diode reset. The extended pulse allows for more time for the diode to discharge to make sure a re-trigger event doesn't occur.

5.4 DIGITAL SECTION

The digital section is responsible for detecting the stretched pulses and interfacing the received digital data with the appropriate client such as a PC. All digital interfaces are controlled with an FPGA. Data to be transmitted from sources such as a sensor, interface the transmitter through the FPGA. The FPGA also processes the rate at which pulses are received and decides if false alarms are being detected. If the false alarm rate is too high then the FPGA changes the threshold of the tunnel diode detector via a digital-to-analog converter (DAC). All coding and

decoding of data is done by the FPGA also. In the current prototype the FPGA resides on a development board purchased from Xilinx. The development board interfaces to the prototype PCB via square pin sockets and wires. Later all digital circuitry and the transceiver can be integrated onto the same board. The development board has a USB interface to a PC where data can be downloaded or uploaded as well as a breadboard for attaching sensors.

6 Lab Results

6.1 SIGNAL WAVEFORMS

Digital data from the FPGA is sent to the MultiSpectral pulse generator. On the rising edges of the data a pulse is generated. Figure 9 shows the signal at the output of the pulse generator. The peak voltage of the signal is over 7 V and the main pulsewidth is only about a quarter of a nanosecond. The pulse shape is somewhat close to an ideal Gaussian monopulse although there is some ringing after the main pulse.

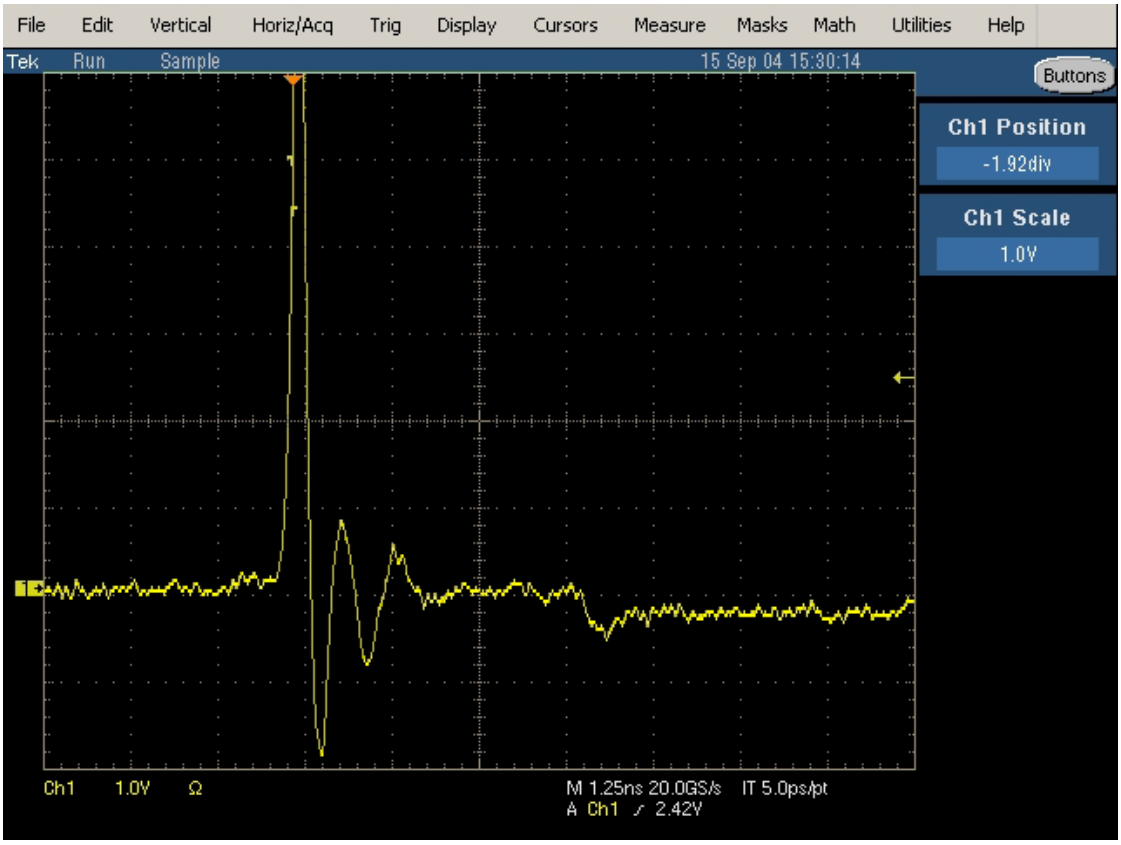


Figure 9: Pulse Generator Output.

Once the pulse has been bandpass filtered to meet the spectrum requirement, the amplitude is much less, down to about 600 mV. Most of the signal power from the pulse generator is outside of the passband of the filter. The pulse duration however is much longer, spreading the signal energy over more time. There appears to be an echo of the pulse 3 ns after the first pulse. Variations in the group delay of the filter is up to 2.5 ns as the passband edges. This could explain why there are echoes.

Figure 10: Bandpass Filtered Pulse.

Figure 11 shows the whole prototype transmitter chain. All of the components are connected with SMA coaxial connectors for good high speed impedance matching.

The input to the pulse generator is BNC coax which can be connected to either a arbitrary waveform generator or an FPGA board as a data source.

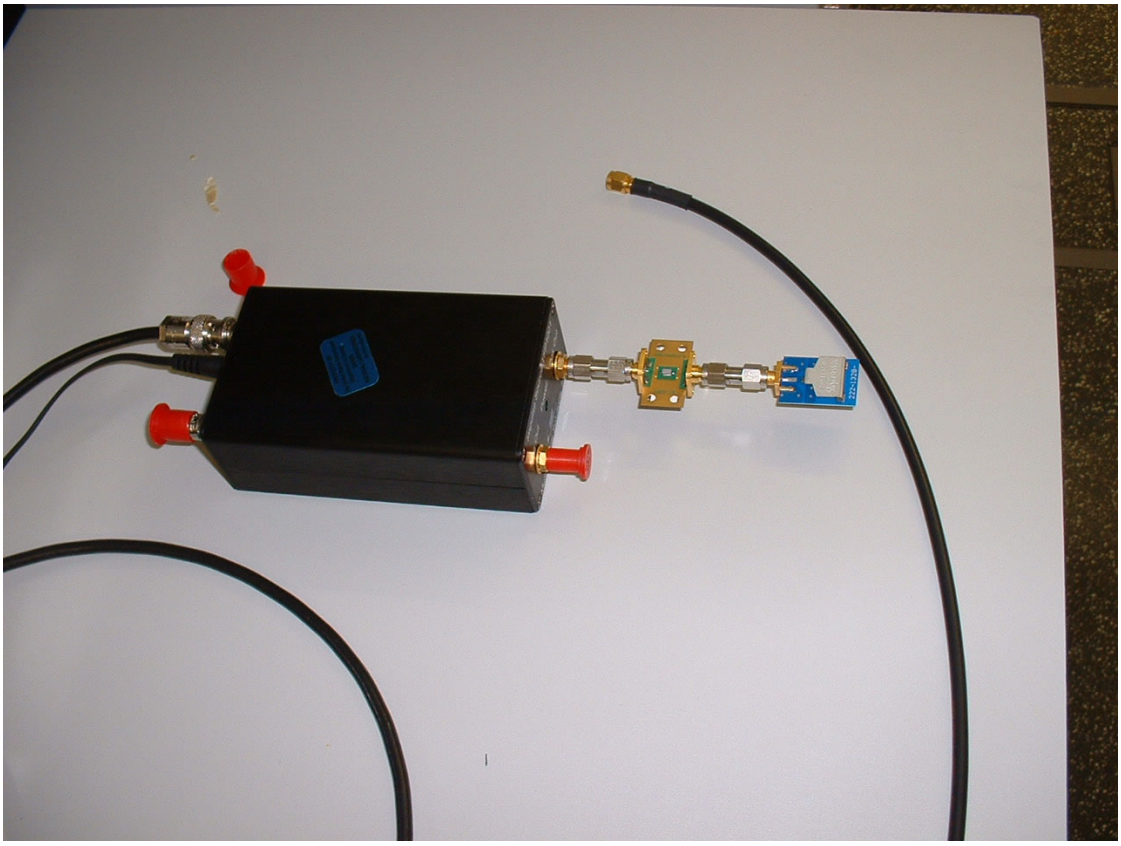


Figure 11: Prototype Transmitter.

6.2 WIRELESS CHANNEL

The channel between the two antennas has path loss due to radiated energy traveling in all directions. Both antennas have a small amount of directionality that can focus their signal power in one direction. This provides some signal gain because less power is lost traveling in other directions. Other power is absorbed by objects in the path of the transmitter and receiver. Another problem is fading where signals can take multiple paths to the receiver and add out of phase or destructively. To

characterize the channel a network analyzer was swept over the 3 to 5 GHz band and the two antennas were connected to the input and output ports by coaxial cable. The two antennas were held one meter apart. The network analyzer was first calibrated with the same two pieces of coax connected together to remove their effect. After finding the magnitude spectrum the impulse response of the channel can be found by taking the inverse Fourier transform.

6.3 SENSITIVITY

Sensitivity measures the smallest signal power needed to obtain an acceptable bit error rate such as 10^{-5}. Test patterns are sent from the transmitter, received at the receiver and compared to the original pattern. Figure 12 demonstrates the received signal coming from the prototype PCB. The test pattern used is a repeating 1111000011001010, which can be seen to be detected error free. Data was transmitted at a rate of 1 Mbps. In this case the transmitter and receiver are space only a meter apart. In future tests, an adaptable threshold, lower noise LNA and board design without hand modification as well as longer high quality cabling should greatly extend the range of the system. The duty cycle of the digital signal can be tuned with a potentiometer. The duty cycle was left at less than 50% so that many pulses can be detected during a bit period and the noise level can be easily detected by the presence of false triggers or more than one trigger per bit period. In order to synchronize the pattern with the oscilloscope so that it can be displayed a digital pulse must be supplied by the digital data source once per pattern. This pulse is used on a separate

oscilloscope channel as a trigger source. The trigger pulse can be seen in Figure 12 on channel one.

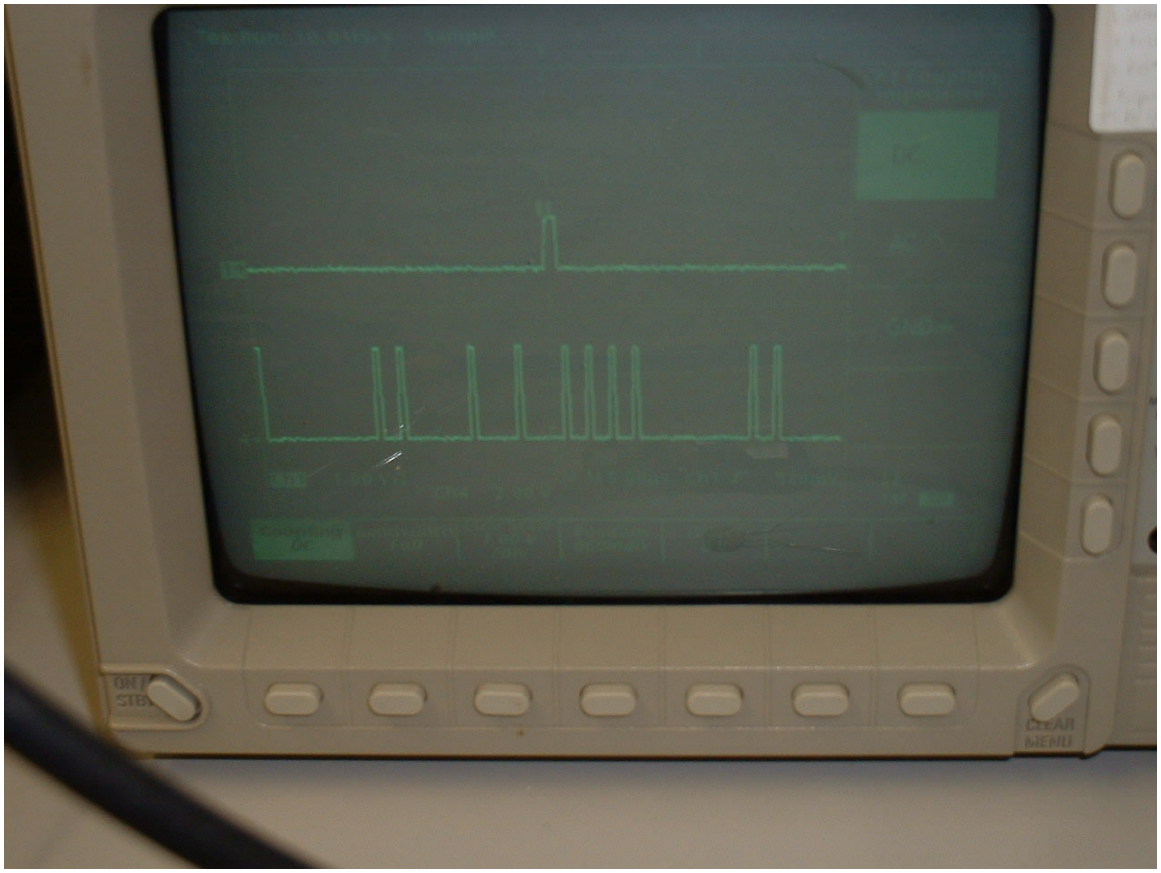


Figure 12: Oscilloscope Waveform of Received Signal.

One way of doing a BER test is to zoom the oscilloscope out so that a large number of bits can be seen. Then the samples can be downloaded from the scope, imported into Matlab, sampled once per bit and compared to the transmitted pattern. This method is limited by the sampling rate and memory depth of the oscilloscope. If only 100 bits can be stored in the oscilloscope's memory then the best BER measurable would be .01. If a bit-error-rate tester (BERT) is available it can be used to transmit data patterns, compare the received signal and read out a BER. Because of

the lack of a BERT BER testing for this research was limited to the above BER threshold.

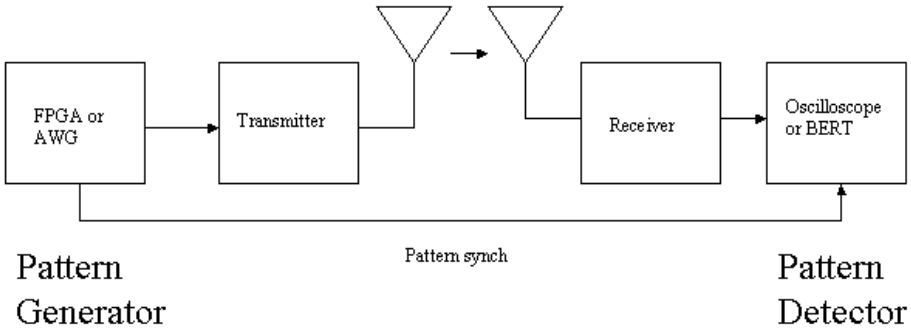


Figure 13: Test Setup

Because an FPGA is used to interface with data sources and communicate with the UWB radio it can also be used to generate test patterns. PN patterns can easily be generated with a shift register and XOR gates tapped from certain bits in the shift register [13].

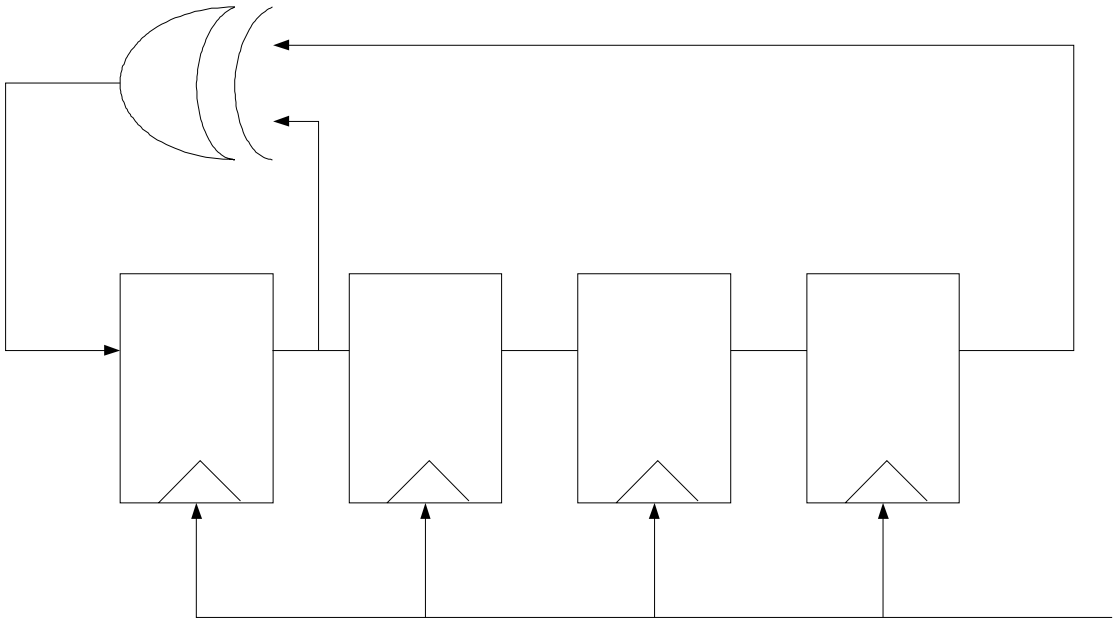


Figure 14: 4 Bit LFSR.

It can be seen from Figure 15 that many modification have been done to the PCB by the many blue wires attached. Due to the lack of complete models and non-linear behavior it is difficult to predict functionality before experimenting. Unfortunately this can lead to some trial and error but empirical data leads to better modeling and understanding of circuit behavior.

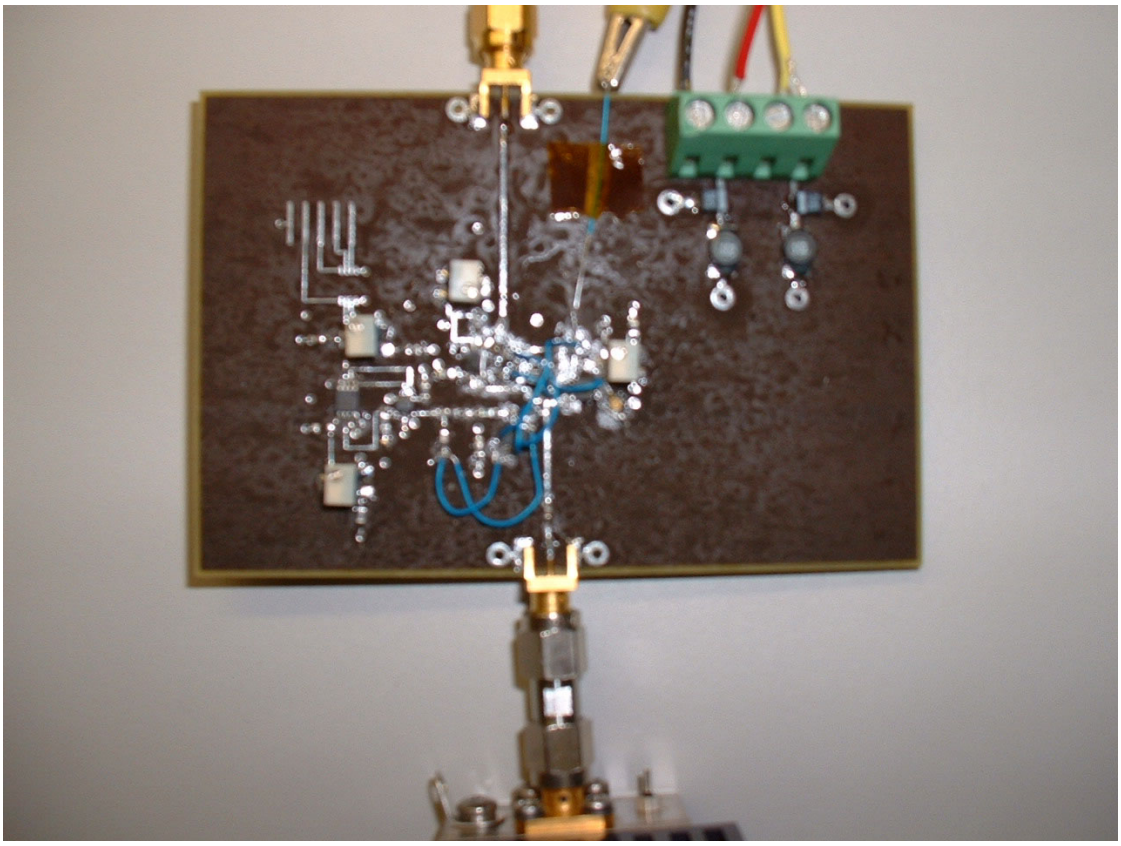


Figure 15: Prototype PCB.

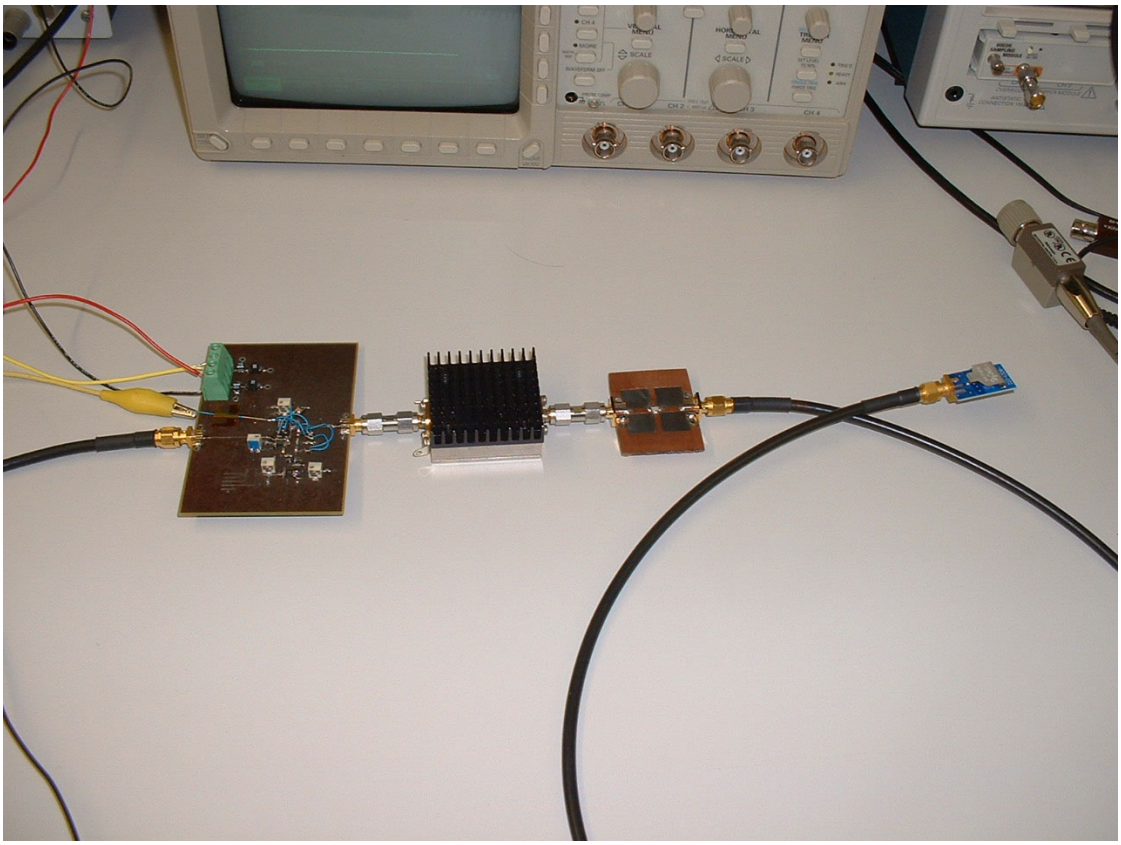


Figure 16: Complete Receiver Chain.

7 Prototype Improvements and Future Research

7.1 THRESHOLD CONTROL ALGORITHM

Receiver functionality is highly dependent on the correct setting of the threshold level. The noise power level can be measured by the number of false triggers. False triggers can be detected in this architecture with no knowledge of the actual data pattern. If the pulse width is tuned to be less than a full bit period, this allows the one shot to be triggered multiple times during one bit period. The detection of multiple bits during one bit period indicates that the threshold is near or below the noise floor. Because the threshold can be controlled digitally with a DAC, it is possible to create a mixed-signal feedback loop to raise the threshold when needed. Obviously if the threshold is raised too high, neither noise nor data will ever cause a triggering event. To safeguard against raising the threshold too high, the algorithm will lower the threshold if no triggering event has occurred over a set amount of time. If no data is present to be received then the threshold should slowly move slightly above and below the noise level searching for the acceptable false alarm rate.

7.2 CHANNEL CODING

Another improvement that can be derived from digital processing is channel coding. Channel coding introduces redundancy into the data stream so that errors can be corrected for. Channel coding can be implemented using a 1/3 rate convolutional encoder. The improved BER gained from channel coding can be used to increase the range of the transceiver above 10 m. The only drawback to a 1/3 rate convolutional encoder is that the bit rate has been reduced by a factor of three. If range is of more

importance than bandwidth, then channel coding is a good solution. As seen in Figure 17, a convolutional encoder can easily be implemented with a shift register and XOR gates to execute additions. For every bit that enters the shift register three come out of the encoder. On the receive side a maximum likelihood decoder such as a Viterbi decoder can be implemented in digital logic to decode the data and recover the original bit stream.

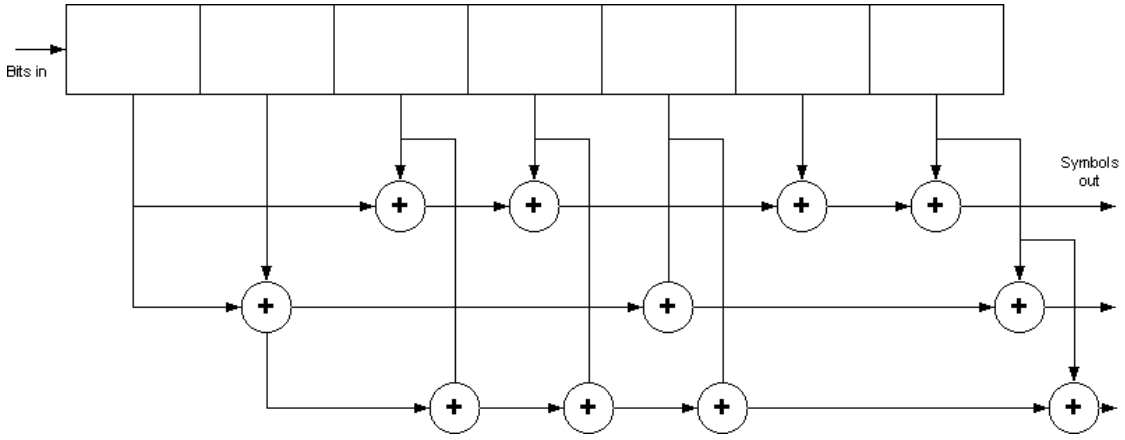


Figure 17: Convolutional Encoder.

7.3 IMPROVEMENT OF RF ISSUES

As seen in Figure 15, the PCB has been highly modified and many connections are made with narrow inductive wires. It is almost certain that receiver sensitivity and range are degraded by the lack of a continuous 50 ohm environment. A new spin of the board will roll the modifications into a clean design and also roll in design improvements discovered during the testing phase such as the removal of stubs and improved switches.

7.4 IC INTEGRATION ISSUES

It is always desirable to implement the entire system on one chip. In the case of UWB the low component count bodes well for integration. However the difficult specifications for UWB components somewhat offsets this advantage. Broad bandwidths make gains, noise figures and matching a major headache. For the prototype, design goals were definitely not met when the only amplifier with sufficient bandwidth for UWB costs $700, consumes over a Watt of power and has a high noise figure. For all UWB architectures it is required to have a LNA. Part of the reason that the LNA was not ideal for a UWB application is that it was not targeted for the desired specifications. The bandwidth goes from DC to 8.5 GHz allowing excess noise through and needlessly consuming extra power. In order to integrate the whole transceiver onto one chip it will be necessary to design an LNA in CMOS technology that can meeting the stringent requirements. Fortunately research into this area is showing that this is possible [3]. Research has also found that it is possible to integrate tunnel diodes with CMOS [7], allowing the prototype architecture in this thesis to be implemented on one chip.

8 Conclusion

At this time significant research has been published on the topic of UWB. Unfortunately there are only a few cases where actual hardware is used. Most work has been done using Matlab models with picosecond sample spacing. The use of a real system will allow research into areas that ideal simulations will not allow. It is the author's hope that this prototype will be used as a research vehicle for real world examination of UWB systems.

It was shown that UWB can be a very advantageous technology to use for applications that require low power, low cost and high bit rate application over short ranges. It is certain that there will be applications in the future to which UWB will be the optimum communications technology. UWB can be implemented using current technology and off the shelf parts. There are still obstacles in building a commercially feasible product using the current prototype such as finding an affordable LNA with lower power and noise figure. With future integration and economies of scale it is possible that UWB will be competing with traditional radio technologies in the very near future.

9 Bibliography

[1] American Micro Semiconductor, "Tunnel Diode and Back Diode Tutorial," http://www.americanmicrosemi.com/tutorials/tunneldiode.htm

[2] C. L. Bennett and G. F. Ross, "Time-Domain Electromagnetics and Its Applications," Proceedings of IEEE, Vol. 66, No. 3, Mar. 1978.

[3] A. Bevilacqua, A. M. Niknejad, "An Ultra-Wideband CMOS LNA for 3.1 to 10.6 GHz Wireless Receivers," Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International.

[4] Federal Communications Commission, "Revision of Part 15 of the Commission's Rules Regarding Ultra-Wideband Transmission Systems," First Report and Order, FCC 02-48, Apr. 2002.

[5] R. J. Fontana, "Recent system applications of short-pulse ultra-wideband (UWB) technology," IEEE Transactions on Microwave Theory and Techniques, Volume: 52, Issue: 9, Part 1, pp. 2087- 2104, Sept. 2004.

[6] J. Han, C. Nguyen, "Ultra-Wideband Electronically Tunable Pulse Generators," IEEE Microwave and Wireless Components Letters, Vol. 14, No. 3, pp. 112-114, March 2004.

[7] S. Kurinec, J. Kempisty, K.D. Hirschman, N. Jin, S. Chung, P. Berger and P. Thompson, "Integration of Silicon Based Tunnel Diodes with CMOS: An RIT-OSU-NRL-NSF Effort," IEEE UGIM Symp. Proc. 14, 74 (2001).

[8] H.-J. Lee, D. S. Ha, and H.-S. Lee, "Toward Digital UWB Radios: Part I – Frequency Domain UWB Receiver with 1 bit ADCs," IEEE Conference on Ultra Wideband Systems and Technologies, pp. 248-252, May 2004.

[9] A. F. Molisch, J. R. Foerster, and M. Pendergrass, "Channel models for ultra-wideband personal area networks," IEEE Wireless Communications, vol. 10, pp. 14-21, Dec. 2003

[10] I. Oppermann, M. Hamalainen, J. Linatti, "UWB Theory and Applications," Wiley, 2004, pp. 47-51.

[11] J. G. Proakis, M. Salehi, "Communication Systems Engineering", Prentice Hall 2001, pp. 556-557.

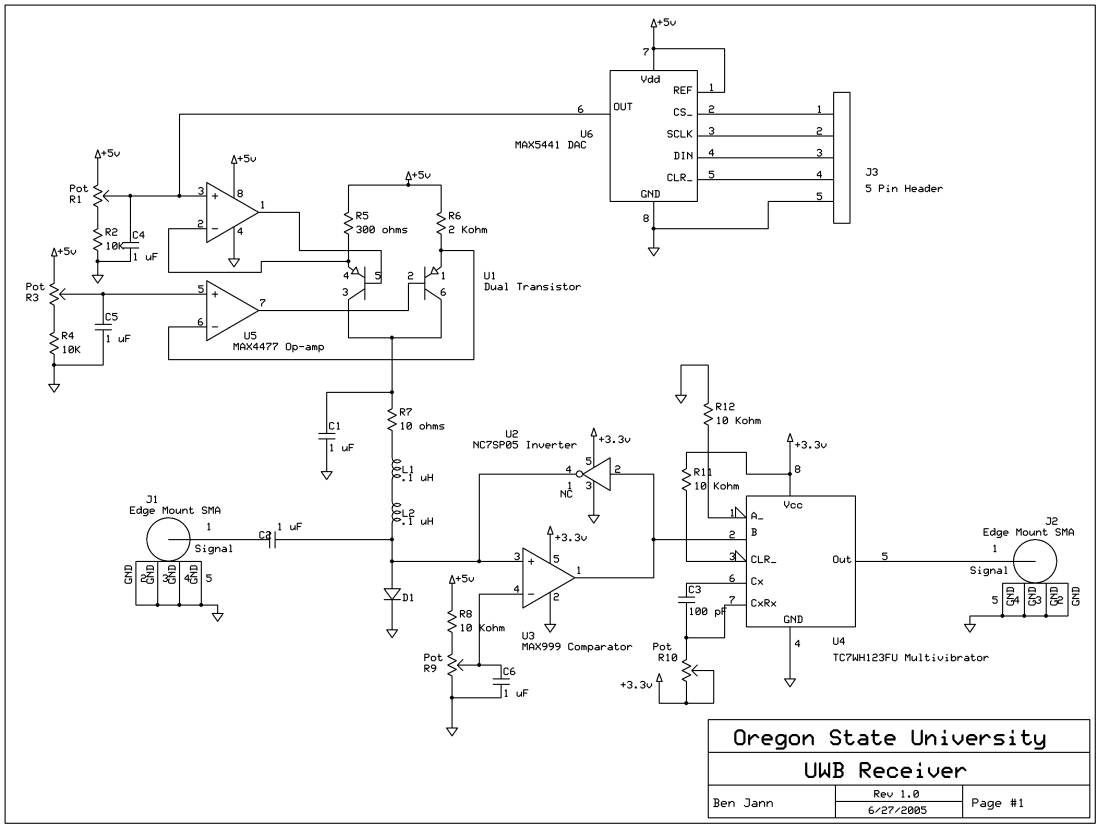
[12] B. Razavi, "RF Microelectronics," E. Prentice Hall 1998, pp. 45.

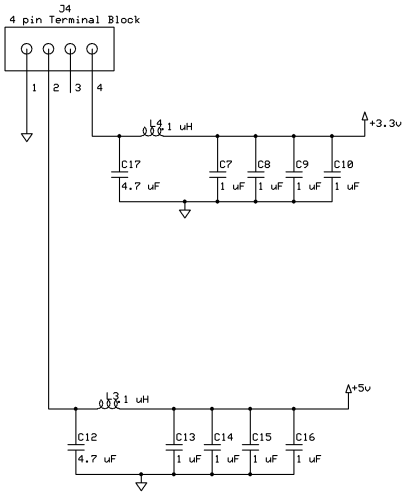
[13] D. J. Smith, "HDL Chip Design", Doone Publications 1996, pp. 179-185.

[14] Chen, M.S.-W.; Brodersen, R.W., “A subsampling UWB radio architecture by analytic signaling,” Acoustics, Speech, and Signal Processing, 2004. Proceedings. (ICASSP '04). IEEE International Conference on, Volume 4, 17-21 May 2004

Appendices

Appendix A Board Schematic





Oregon State University		
UWB Receiver		
Ben Jann	Rev 1.0 7/4/2005	Page #2

Appendix B Board Layout