AN ABSTRACT OF THE DISSERTATION OF

Hyuk Sun for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on December 8, 2016.

Title: A Wide Modulation Range and PVT-Tolerant Spread-Spectrum Modulation Clock Generator

Abstract approved:

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Un-Ku Moon

This dissertation presents a phase domain in-loop-bandwidth spread-spectrum clock generation technique. In this proposed technique, a charge-based discrete-time loop filter is proposed to enable the phase domain in-loop-bandwidth spread-spectrum modulation without a delta-sigma modulator or time-to-digital converter. The in-loop-bandwidth modulation technique maximizes the loop bandwidth to improve phase noise suppression in a ring-based voltage-controlled oscillator. The phase domain modulation is established to eliminate a delta-sigma modulator that presents an undesirable power and noise trade-off. An analog-domain phase modulation in this proposed modulation technique eliminates a time-to-digital converter that results in inevitable quantization noise.

The proposed technique delivers a wide spread-spectrum modulation range with significantly relaxed PVT sensitivity. Since the proposed discrete time loop filter acquires and filters signals in the charge domain, this loop filter supports good linearity for a wide modulation range. PVT variations in the loop filter and the voltage-controlled oscillator are attenuated by the loop gain. The nonlinearity of the voltage-controlled oscillator gain (K_{VCO}) and loop filter is also attenuated due to the loop gain. In addition, a correlated double sampling technique is leveraged to minimize 1/f noise and DC offset of the proposed discrete-time loop filter.

This dissertation discusses design trade-offs: between reference frequency and spread-spectrum modulation range, and between the spread-spectrum modulation range and jitter performance. From time and spectral measurements for various reference frequencies, a higher reference frequency results in better jitter performances, but also a narrow spread-spectrum modulation range. Time domain jitter measurements are compared to spectral domain jitter calculations to observe design intuitions.

This wide modulation range and PVT-tolerant spread-spectrum modulation technique is implemented in a 0.18μm CMOS, while consuming 9.93mW with a 1.8V power supply. The proposed charge-based discrete time loop filter consumes less than 10% of the total power, and the spread-spectrum modulation component requires less than 5% of the total power. This wide range spread-spectrum clock generation technique achieves 0.8% and 3.2% spread-spectrum modulation range with 22.76dB and 26.51dB spread-spectrum attenuation for 2MHz and 8MHz reference frequencies, respectively. The measured absolute jitter is $62.72ps_{rms}$ and $18.72ps_{rms}$ for 2MHz and 8MHz reference frequencies, respectively. The measured period jitter is $961.2fs_{rms}$ and $988.1fs_{rms}$ for 2MHz and 8MHz reference frequencies, respectively. Finally, a 142% change in K_{VCO} results in less than 298ppm modulation range error, which confirms the PVT-tolerant modulation.

A Wide Modulation Range and PVT-Tolerant Spread-Spectrum Modulation Clock Generator

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

Director of the School of Electrical Engineering and Computer Science

Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Hyuk Sun, Author

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Chapter 1 - Introduction

A serializer/deserializer (SerDes) technique is pervasively used to trade speed overhead for physical overhead in a modern wireline communication system. This technique reduces the number of transceivers, but also requires a higher transmission rate. The basic idea behind this technique is to serialize the multi-bit data to a single-bit stream at a transmitter, and then deserialize this single-bit stream back to the original multi-bit data at a receiver. The transmission rate has to be faster than the multi-bit data rate for the equivalent throughput. However, a single transceiver can be used to send the multi-bit data. This significantly relaxes hardware design overheads such as I/O pin count, number of traces, and physical footprint.

Western Digital introduced a parallel advanced technology attachment (P-ATA) interface standard in 1986 for the connection of storage devices such as hard disk, floppy disk, and optical disc drives in a computer. The specifications for this interface standard were initially a 16-bit data width at a rate of 16.7MB/sec without the SerDes technique from Table 1-1. In addition, the P-ATA ribbon cable has 40-pin connectors to send a 16-

	Mode	# of pins	Data width	Line encoding	Transmission rate	Data rate
Parallel ATA[(1)]	Ultra DMA -1	40	16 bits	N/A	16.7 MT/s*	16.7 MB/s
	Ultra DMA -2	40	16 bits	N/A	33.3 MT/s*	33.3 MB/s
	Ultra DMA -4	40	16 bits	N/A	66.7 MT/s*	66.7 MB/s
	Ultra DMA -5	40	16 bits	N/A	100 MT/s*	100 MB/s
	Ultra DMA -6	40	16 bits	N/A	133 MT/s*	133 MB/s
	Ultra DMA -7	40	16 bits	N/A	167 MT/s*	167 MB/s
Serial ATA[(2)]	Revision 1.0	7	16 bits	8b/10b	1.5 GT/s*	150 MB/s
	Revision 2.0	7	16 bits	8b/10b	3.0 GT/s*	300 MB/s
	Revision 3.0	7	16 bits	8b/10b	6.0 GT/s*	600 MB/s
	Revision 3.2	7	16 bits	128b/130b	16 GT/s*	1969 MB/s

* MT/GT = Mega-transfer/Giga-transfer
(1) https://en.wikipedia.org/wiki/parallel_ATA
(2) https://en.wikipedia.org/wiki/serial_ATA

Table 1-1: Comparison between Parallel- and Serial-ATA.

bit data. Without the SerDes technique, this parallel transmitting protocol requires an individual physical channel (or pin connector) for each transmitting bit, and the transmission rate is equivalent to the data rate.

Since its first invention, there have been six revisions on this P-ATA standard. From Table 1-1, examination of the data rate reveals a 10× improvement from 16.7 MB/sec (Ultra DMA-1) to 167 MB/sec (Ultra DMA-7). However, the maximum achievable data transfer rate on a traditional P-ATA ribbon cable was limited to less than 66MB/sec. Then, several design innovations in both hardware and software had been proposed to overcome this speed limitation, such as differential signaling, equalization, encoding/decoding, and error detection. The speed enhancement from these innovations increased the design complexity and cost of a transceiver as well as its size. On the other hand, the maximum achievable data transfer rate in a mechanical hard disk drive was around 150MB/sec at that time. This speed bottleneck in the hard disk drive made further speed improvement in the data rate less attractive. Therefore, the SerDes technique was leveraged to increase the transmission rate (instead of the data rate) with a single advanced transceiver (instead of 16 transceivers) over a pair of transmission lines (instead of 40-pin connector cable). This SerDes technique saves significant hardware design resources, which is critical for a highly-integrated wireline communication system.

The first transition from the P-ATA (Ultra DMA-7) to the serial-ATA (S-ATA) revision 1.0 was made in 2003. Since the first S-ATA standard was equipped with the SerDes technique, the number of pins went down from 40 to 7, and the transmission rate increased from 167MT/sec to 1.5GT/sec with a similar data rate. The continual increase in the data rate has been empowered thanks to recent technological advances in a storage device such as a high-speed solid-state drive. Following this data rate improvement, the transmission rate has to be increased. This is possible due to the recent advances in the transceiver design mentioned before.

The SerDes technique has been used in almost every modern wireline communication system, such as peripheral component interconnect (from PCI to PCI-

express), and universal serial bus (USB). The brief historical developments of popular interface standards are summarized in Table 1-2. The S-ATA and PCI-express (or PCIe) were evolved from their prior standards, P-ATA and PCI, and both have the SerDes capability. Every revision almost doubles the transmission and date rate simultaneously, and the latest specifications for both standards are the 16GT/sec transmission rate and 1969MB/sec data rate, respectively. This implies that there has been a significant and continual increase at the hardware design overhead for a high-performance application. Therefore, the SerDes technique is essential to relax this hardware overhead. In addition, a very high-speed transceiver design with the SerDes technique becomes an economical solution because a single fast versatile transceiver can replace an array of transceivers.

	Revision	**Line encoding**	**Transmission rate**	**Data rate**
S-ATA	1.0	8b/10b	1.5 GT/s	150 MB/s
	2.0	8b/10b	3.0 GT/s	300 MB/s
	3.0	8b/10b	6.0 GT/s	600 MB/s
	3.2	128b/130b	16 GT/s	1969 MB/s
PCIe[(1)]	1.0	8b/10b	2.5 GT/s	250 MB/s
	2.0	8b/10b	5 GT/s	500 MB/s
	3.0	128b/130b	8 GT/s	984.6 MB/x
	4.0	128b/130b	16 GT/s	1969 MB/s
USB[(2)]	1.1	N/A	12 MT/s	1.5MB/s
	2.0	N/A	280 MT/s	35 MB/s
	3.0	8b/10b	4 GT/s	400 MB/s
	3.1	128b/132b	10 GT/s	1.21 GB/s

[(1)] https://en.wikipedia.org/wiki/PCI_Express
[(2)] https://en.wikipedia.org/wiki/USB

Table 1-2: SerDes scheme comparions for wireline communication systems.

Fig. 1-1 describes general SerDes operation. In the transmitter side, multi-bit data (8-bit in this example) is updated from a data bus, and delivered to the serializer. The serializer is the parallel-in serial-out (PISO) block, and multiplexes the parallel data into a

single serial bit steam at a rate of 8× faster than the original update rate f_0. This serialized stream is sent to the receiver over a single channel. The received bit stream is recovered to the original parallel data using a deserializer, which is the serial-in parallel-out (SIPO) block. Therefore, this SerDes technique basically trades the physical overhead with the speed overhead. There are several SerDes techniques described in [1]. They include i) parallel clock SerDes, ii) 8b/10b SerDes, iii) embedded clock bits SerDes, and iv) bit interleaving SerDes. In the parallel clock SerDes technique, the clock signal is transmitted in a separated channel to synchronize wireline systems. In the embedded clock bits SerDes technique, the clock signal is embedded in the data stream. In order to obtain DC balance, extra line encoding bits are added using an encoding algorithm in the 8b/10b SerDes technique. Lastly, in the bit interleaving SerDes technique, several slower serial data streams are interleaved into a faster serial stream.

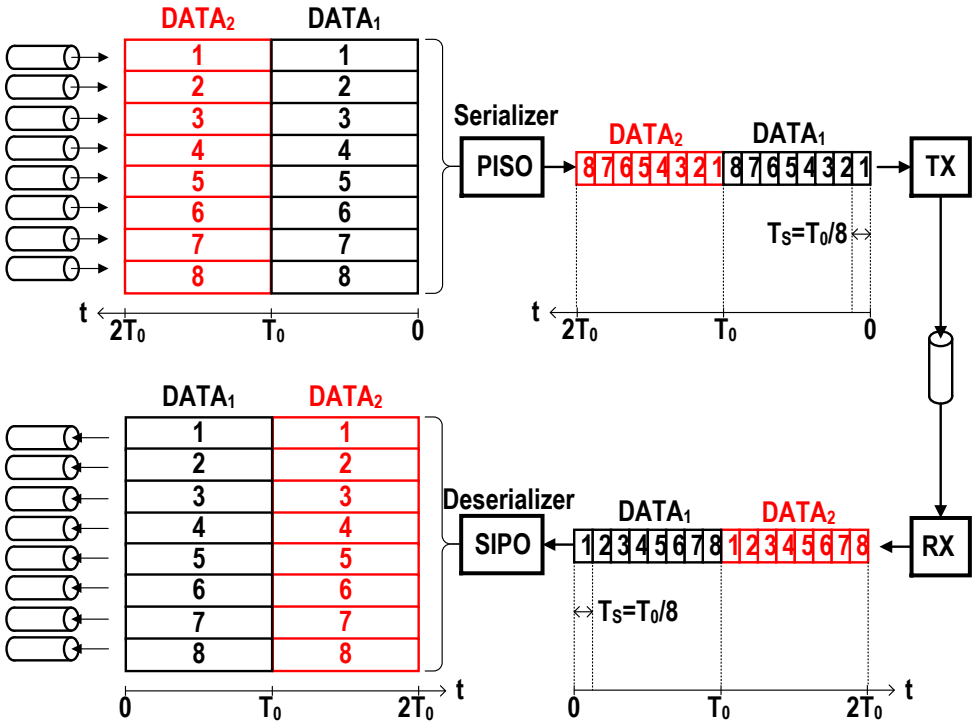


Figure 1-1: Conventional serializer and deserializer operation.

One major drawback of the SerDes technique is that they exacerbate electromagnetic interference (EMI) since a higher transceiver rate creates stronger radiated emission to adjacent systems [2]. The definition of the EMI from [3] is *"the impairment of the extraction of information from a wanted electromagnetic signal caused by electromagnetic noise, where the electromagnetic noise is all electromagnetic energy from both intentional and unintentional radiators except the desired signal for a specific system of interest."* In general, interference can be categorized into conducted disturbances and radiated disturbances, and the radiated disturbance can be distinguished into capacitive and inductive couplings. From a crosstalk example between two parallel traces on a printed circuit board (PCB) in [2], voltage disturbance at a victim's trace is proportional to incident frequency and capacitive coupling coefficient. As seen from Table 1-2, the transceiver rates (for both S-ATA and PCI express) are increasing up to 16GT/sec, which is more than 100× increase from the first revision (SATA revision 1.0). The USB, which is the most popular interface system, can support up to 10 GT/sec. This rate is 1/6 of the radiating frequency in an mmWave radar system.

In addition, the capacitive coupling coefficient has been increasing, too. The capacitive coupling coefficient is a function of physical proximity and relative permittivity in a PCB. Following miniaturizing integrations in a PCB, the pitch size of chips and the width of traces has been scaling down. To keep the same characteristic impedance in traces, the thickness of the dielectric has been decreasing, whereas the relative permittivity of a dielectric has been increasing. This results in an inevitable increase of the capacitive coupling coefficients among traces and chips. Therefore, regulating EMIs and isolating cross-couplings in multiple high speed clocks/signals across a jammed PCB module is very critical and demanding in a modern highly-integrated wireline system. There are several pervasive remedies: shielding [4], pulse shaping or slew rate control [5], low-voltage differential signaling (LVDS), staggering, special layout techniques, and spread-spectrum clocking (SSC) [6]. Particularly, the SSC technique becomes an essential solution to mitigate EMI issues.

1.1 Spread-spectrum Clock (SSC)

The SSC technique modulates the output frequency of a clock generator, and this is a variant of a frequency modulation. This technique slowly modulates the output frequency with a designated frequency modulation profile, and spreads the output power spectral density (PSD) into the designated frequency modulation range.

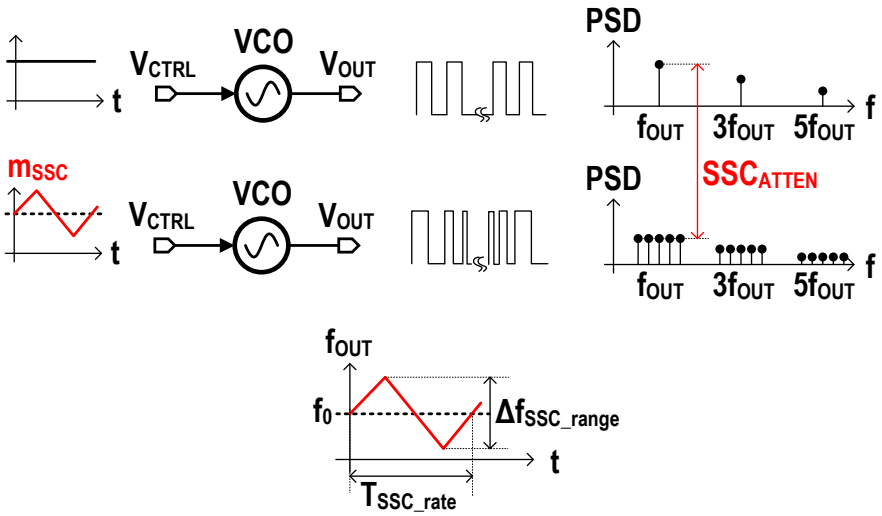


Figure 1-2: Open-loop oscillator with and without the SSC modulation.

In an open-loop clock generator as shown in the top of Fig. 1-2, if the nominal input of a VCO is constant, it generates the unmodulated PSD tones at not only the output frequency (f_{OUT}), but also odd harmonics ($3\times f_{OUT}$, $5\times f_{OUT}$, and so on). As shown in the bottom of Fig. 1-2, if the modulating SSC signal ($m_{SSC}(t)$) is superimposed on top of the nominal input at the control voltage (V_{CTRL}), this modulation signal stimulates the VCO to deviate the output frequency from the center frequency and spread the output tone along the SSC modulation range.

The SSC modulation range (Δf_{SSC_range}) determines how wide the output tones are spread. The SSC modulation rate (f_{SSC_rate}) determines how fast the SSC modulation signal changes. In addition, the amount of attenuation due to the SSC is the SSC attenuation (SSC_{ATTEN}). For example, if there is a carrier at 1GHz with the total power of

0dBm, and one can evenly spread this single tone into ten multiple spreading tones (from 0.91GHz to 1.09GHz with a 20MHz step), the output PSD of the spreading tones becomes -10dBm. Then, this results in the 10dB SSC_{ATTEN} from the SSC technique. In the S-ATA, Δf_{SSC_range}, f_{SSC_rate}, and SSC_{ATTEN} specifications are +0.035~-0.5%, 30~33kHz, and ≥7dB, respectively.

Although the shape of $m_{SSC}(t)$ is a triangular waveform in Fig. 1-2, there are three popular types of $m_{SSC}(t)$: sinusoid, triangular, and cubic (Hershey kiss).

1.2 Qualitative Analysis for the SSC

Since the SSC is one special case of the frequency modulation, the qualitative analysis for the SSC can be borrowed from the wideband frequency modulation bandwidth analysis [7]. Let $m_{SSC}(t) = A_{SSC} \times \cos(\omega_{SSC\_rate} t)$, which is the sinusoid SSC modulation. The output of the clock ($V_{OUT}(t)$) is written as:

$$V_{OUT}(t) = A_{OUT} \cdot \sum_{n=-\infty}^{+\infty} J_n(\beta) \cdot \cos(\omega_{OUT} + n\omega_{SSC\_rate})t \quad (1)$$

where $J_n(\beta)$ is the Bessel function of the first kind and the n-th order, β is $K_{VCO} \times A_{SSC\_rate}/\omega_{SSC\_rate}$, which is equivalent to $0.5 \times \Delta f_{SSC\_range}/f_{SSC\_rate}$, A_{OUT} is the amplitude of the output $V_{OUT}(t)$, and K_{VCO} is the frequency gain of a VCO in rad×Hz/Volt. There are two observations from (1): i) the magnitude of the sidebands is $J_{-n}(\beta)$, and $J_n(\beta)$ is negligible for $n>\beta+1$, and ii) there are infinite sidebands through $f_{OUT,0} \pm n \times f_{SSC\_rate}$, where $f_{OUT,0}$ is the center frequency of $V_{OUT}(t)$. From the first observation, the SSC modulation bandwidth (BW_{SSC}) is written as:

$$BW_{SSC} \cong 2 \cdot (\beta + 1) \cdot f_{SSC\_rate} = 2 \cdot \left(\frac{\Delta f_{SSC\_range}/2}{f_{SSC\_rate}} + 1 \right) \cdot f_{SSC\_rate} = \Delta f_{SSC\_range} + f_{SSC\_rate} \quad (2)$$

Since Δf_{SSC_range} is generally much larger than f_{SSC_rate}, BW_{SSC} is approximately equal to Δf_{SSC_range}. From the second observation, the SSC modulation tones are allocated every f_{SSC_rate} step through the BW_{SSC}. Therefore, the total number of the spreading tones is $\Delta f_{SSC\_range}/f_{SSC\_rate}$. Then, if the modulated output tones are evenly spread through BW_{SSC},

the SSC_{ATTEN} can be written as:

$$SSC_{ATTEN|dB} = 10 \cdot \log_{10}\left(\Delta f_{SSC\_range} / f_{SSC\_rate}\right). \quad (3)$$

These results for the sinusoidal SSC modulation can be applicable to both the triangular and cubic SSC profiles, which are easily decomposed into $\pm n \times \omega_{SSC\_rate}$ sinusoidal tones from the Fourier series analysis.

The output SSC PSD results for three different SSC profiles are shown in Fig. 1-3, which are plotted using 5.34kHz of the resolution bandwidth (RBW), 11.35kHz of f_{SSC_rate}, and ±3% (or ±10.5MHz) of Δf_{SSC_range}. From (2)-(3), BW_{SSC} and SSC_{ATTEN} are calculated to 21MHz and 32.67dB, respectively. The flatness of the spread spectrum is dependent on how to set the higher order Fourier series coefficients in the SSC profile. By tailoring the higher order terms, one can engineer the shape of the spread spectrum. In addition, in order to obtain further dispersed spread tones, the work in [8]-[9] superimposed a random dithering signal on top of the deterministic SSC modulation signal.

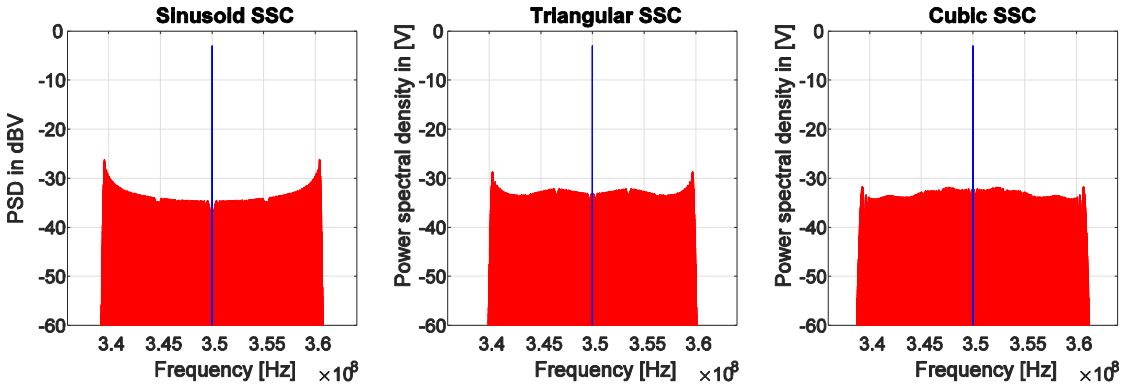


Figure 1-3: Simulated SSC spectrum for different SSC modulation profiles: sinusoid, triangular, and cubic (Hershey Kiss).

1.3 Definition of the Loop Bandwidth (BW) in a PLL

Achieving an accurate and reliable clock above a few hundred MHz generally requires a negative feedback loop. From a crystal reference clock source, which is supposed to be very accurate and reliable, the negative feedback loop in a PLL tries to lock the output phase (ϕ_{OUT}) of a VCO to the clean reference phase (ϕ_{REF}) as shown in Fig. 1-4. The PLL generally consists of a phase detector (PD), loop filter (LF), VCO, and frequency divider (FD). Two phases (ϕ_{OUT} and ϕ_{REF}) are compared in the PD, and the resulting phase error (ϕ_E) is filtered through the loop filter. The filtered output appears at the control voltage (V_{CTRL}), which drives the VCO. When the loop is locked properly, the control voltage V_{CTRL} sets the divided average frequency of the VCO output ($=f_{OUT}/M$) to the input frequency (f_{REF}).

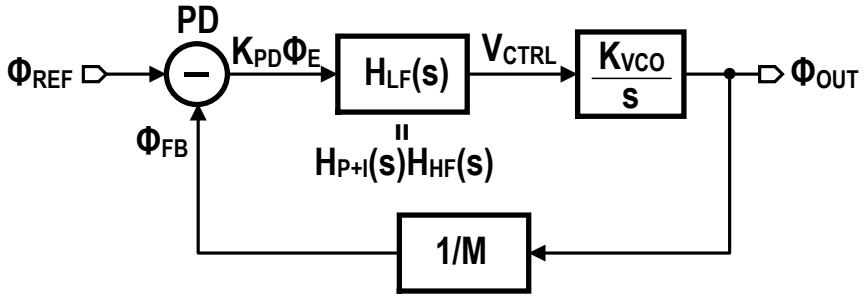


Figure 1-4: Basic block diagram of a PLL.

In wireline communication systems, designing a PLL strongly relies on jitter specifications, and the loop bandwidth (BW) is a key design parameter to optimize these jitter specifications. It is well-known that a wider loop BW is desirable to give larger suppression of the VCO phase noise, whereas a narrower loop BW is preferred to attenuate jitter contributions from a reference clock, phase detector, and loop filter. This is because if the phase noise from the VCO is fluctuating slower than the loop BW, the negative loop can track this noisy output phase ϕ_{OUT} and correct it with respect to the clean input reference phase ϕ_{REF}. However, if the output phase noise is moving faster

than the loop BW, the negative loop cannot correct the noisy output phase due to insufficient loop gain and tracking speed. Therefore, The VCO phase noise, which disturbs faster than the loop BW, directly appears at the output phase ϕ_{OUT} without noise filtering, indicating that the frequency response from the VCO phase noise (ϕ_{VCO}) to the output phase ϕ_{OUT} is a high-pass response. On the other hand, if the reference phase noise is perturbing faster than the loop BW, this noisy perturbation is filtered out at the loop filter, indicating that the frequency response from the input reference phase noise to the output phase ϕ_{OUT} is a low-pass response. Therefore, the loop BW is a critical design variable to determine rolling-off frequency for both phase noise transfer functions. In general, a wider loop BW is typically preferred in a PLL with a ring-based VCO, whereas a narrow loop BW is preferred in a PLL with a low noise LC VCO.

There is no single definition of the loop BW to fulfill for all purposes, and natural frequency, loop gain, noise bandwidth, and 3-dB bandwidth can be a reasonable candidate [10]. However, as following [10], a loop gain (K_{LG}) is defined as the loop BW in this work. The definition of the loop gain K_{LG} is the proportional path gain coefficient in the loop. In general, the loop filter can be formulated into the combination of a low frequency loop filter, which consists of proportional and integral filters ($H_{P+I}(s)$), and high frequency loop filter ($H_{HF}(s)$). The proportional and integral filter combination $H_{P+I}(s)$ is dominant below the loop BW because their poles and zeros are located in relatively less or equal to the loop BW. This low frequency loop filter $H_{P+I}(s)$ can be rewritten as K_1+K_2/s in a Type-II PLL. On the other hand, since the high frequency loop filter $H_{HF}(s)$ has poles and zeros in higher frequencies, which are much larger than the loop BW, this filter can be approximated to $H_{HF}(0)$ inside the loop BW. Then, the loop BW (or loop gain K_{LG}) can be written as:

$$K_{LG} = K_{PD} \cdot \frac{K_{VCO}}{2\pi} \cdot K_1 \cdot H_{HF}(0) / M \tag{4}$$

where K_{PD}, K_{VCO}, K_1, and M are the phase detector gain, the VCO gain, the proportional path gain, and the frequency division ratio in the frequency divider, respectively. The

loop gain K_{LG} has a dimension of Hz, whose unit is equivalent to the loop BW. In addition, the gain crossover frequency (Hz) in an open-loop bode plot is approximately same to K_{LG} [10].

1.4 Prior SSC Architectures

The next question is how to inject the SSC modulation signal inside a PLL. The SSC modulation signal $m_{SSC}(t)$ is generally a periodic signal with a finite BW, and the SSC modulation signal needs to be properly placed inside the pass band of SSC transfer function (TF_{SSC}). The SSC transfer function TF_{SSC} is from the modulation signal $m_{SSC}(t)$ to the output clock frequency f_{OUT}. Since the transfer function TF_{SSC} relies on the loop BW, one needs to set the loop BW by taking into account both the phase noise transfer functions and the SSC transfer function TF_{SSC}.

There are three popular ways to generate a SSC modulation: out-of-loop-BW direct SSC modulation, in-loop-BW SSC modulation, and two-point SSC modulation.

1.4.1 Out-of-Loop-BW Direct SSC Modulation

The most convenient method to implement the SSC modulation is to directly inject the SSC modulation signal at the control voltage V_{CTRL} of a VCO. This SSC scheme is called the out-of-loop-BW direct SSC modulation [11]-[13]. As shown in Fig. 1-5, the SSC modulation signal directly modulates the V_{CTRL} of the VCO, and the returning phase modulated signal $\Delta\phi_{SSC}$ is attenuated in the narrow BW loop filter. Therefore, the SSC modulation signal has to be carried outside of the loop BW. In other words, the loop BW has to be sufficiently smaller than the SSC modulation pass band. Because the SSC modulation rate f_{SSC_rate} is around 10kHz to 300kHz, the loop BW in this out-of-loop-BW SSC modulation technique must be sufficiently smaller than the lowest bound of the modulation pass band, which is 10kHz in this work. This results in a prohibitively large loop filter and limited suppression of the VCO phase noise. Another critical drawback of this direct SSC modulation technique arises because the SSC modulation range changes as the VCO gain K_{VCO} varies due to PVT variations.

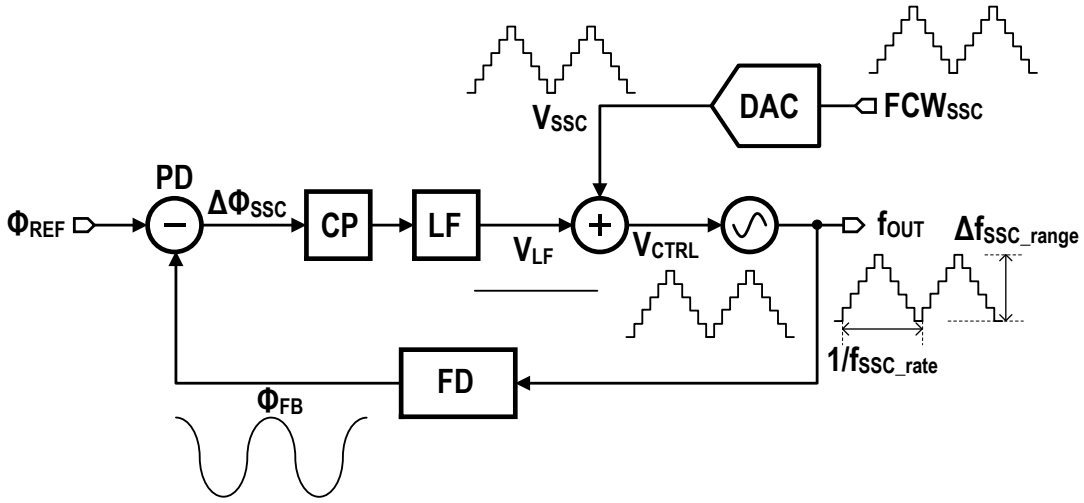


Figure 1-5: Block diagram of an out-of-loop-BW direct SSC modulation.

1.4.2 In-Loop-BW SSC Modulation

The in-loop-BW SSC modulation technique employs either frequency domain SSC modulation with a delta-sigma modulator (DSM) [14]-[17] or phase domain SSC modulation with a time-to-digital converter (TDC) in all-digital PLLs [18]-[19]. In this in-loop-BW SSC modulation technique, the SSC modulation signal is injected inside the loop BW.

Fig. 1-6 shows the in-loop-BW frequency domain SSC modulation with a DSM. The SSC modulation frequency control word (FCW_{SSC}) drives the DSM, which determines the frequency division ratio for the multi-modulus frequency divider (MMFD). This dithered instantaneous frequency division ratio, which is an integer ratio, is averaged to a fractional ratio through the loop filter. Based on this fractional-N frequency synthesis technique, one can obtain the target SSC frequency modulation by using the frequency control word FCW_{SSC}. One drawback is that all in-band DSM dithering noise leaks inside the loop BW and appears at the control voltage (V_{CTRL}). This results in a trade-off between the VCO phase noise and DSM dithering noise. By

increasing the loop BW, one can increase the suppression of the VCO phase noise while the DSM dithering noise leaks more inside the loop BW, and vice versa.

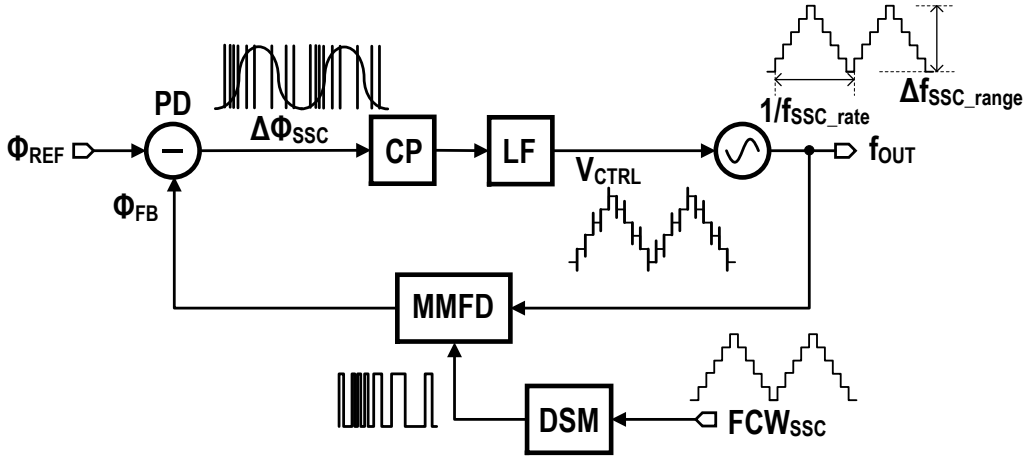


Figure 1-6: Block diagram of an in-loop-BW frequency domain SSC modulation.

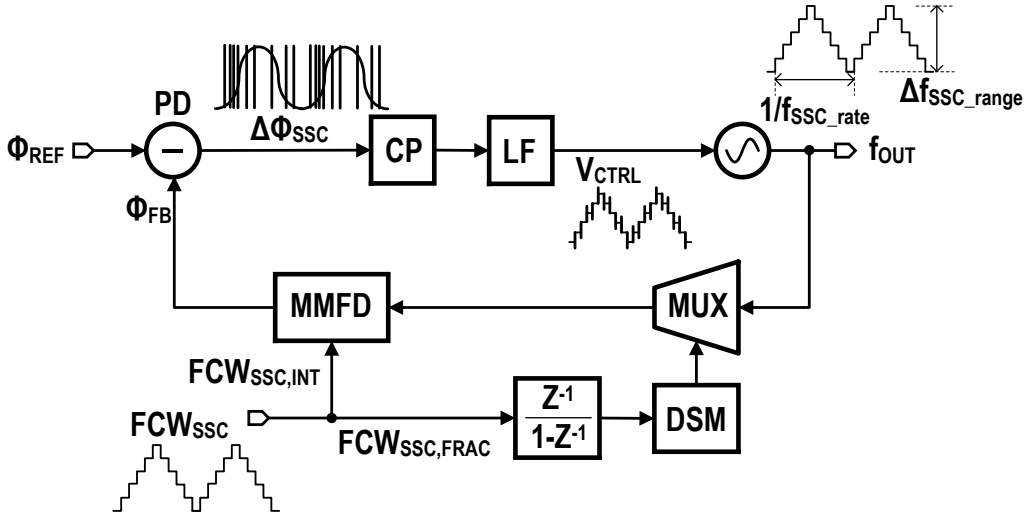


Figure 1-7: Block diagram of an in-loop-BW frequency domain SSC modulation with a phase selector.

One can obtain a smaller dithering step size by using a phase selector or phase interpolator [16] as shown in Fig. 1-7. By either subdividing the output phase into multiple phase levels $\phi_{OUT,0\sim N-1}$ or generating multiple phases from a ring-based VCO, the

dithering step size of the DSM is subdivided. This technique helps to mitigate both the dithering noise and spurs.

Fig. 1-8 shows the phase domain in-loop-BW SSC modulation technique with a time-to-digital converter (TDC) or phase quantizer [18]-[19] in all-digital PLLs. This technique requires a TDC or phase quantizer to quantize the output phase ϕ_{FB} from the VCO. The input frequency control word FCW_{IN} with the additional SSC frequency control word FCW_{SSC} are digitally accumulated and converted to the corresponding phase control word (PCW_{SSC}). The phase control word PCW_{SSC} and the quantized output phase ϕ_{FB} are compared with a digital phase detector, and the residual digital phase difference $\Delta\phi_{SSC}$ is filtered in the digital loop filter. This filtered digital control voltage V_{CTRL} drives the digitally controlled oscillator (DCO). However, there are two quantization errors from a TDC (or phase quantizer) and DCO in this phase domain SSC technique, and these two quantization errors create a undesirable trade-off between accuracy and power.

These in-loop-BW SSC techniques can achieve a robust SSC frequency modulation from PVT variations of K_{VCO}. This is because either the DSM based fractional frequency divider or the digitally controlled phase accumulation guarantees the desired frequency division ratio between the input reference frequency f_{REF} and the output frequency f_{OUT} using a strong loop gain.

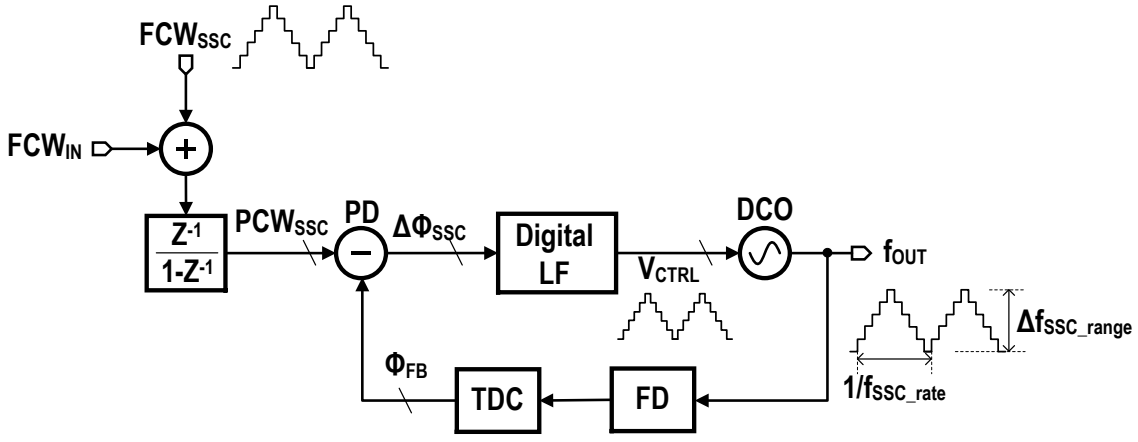


Figure 1-8: Block diagram of an in-loop-BW phase domain SSC modulation.

1.4.3 Two-Points SSC Modulation

The two-point SSC modulation technique is a combination of both the out-of-loop-BW and in-loop-BW SSC modulation schemes [20]-[22]. Two separate modulation signals are injected at the VCO (or DCO in an all-digital PLL) and at the MMFD (or FCW_{SSC} in an all-digital PLL). In this way, this two-point SSC modulation technique allows one to determine the loop BW independently from the SSC modulation pass band. However, matching the SSC modulation gains for two different modulation injection points is not trivial, and the out-of-loop-BW SSC modulation gain is still susceptible to the PVT variations of K_{VCO}.

1.5 Observations and Motivations

A multifunctional print module requires demanding SSC specifications such as more than ±3% modulation range with 10kHz modulation rate on multiple clock phases, which is exceptionally demanding, compared to other conventional SerDes systems, such as the S-ATA, which requires 0~0.5% SSC modulation range with 33kHz SSC modulation rate. For this particular application, a ring-based oscillator is preferred to achieve the multiple clock phases. The out-of-loop-BW direct SSC modulation is not a good candidate because the inevitable narrow loop BW results in a prohibitively large loop filter and significant jitter contribution from a VCO. In the frequency domain in-loop-BW SSC modulation with a DSM, additional spurs and in-band dithering noise from the DSM are inevitable. In the phase domain in-loop-BW SSC modulation technique, this larger SSC modulation range requirement needs demanding acquisition range of the TDC with a sub-pico second time step, which could result in unacceptable power dissipation in a 0.18μm CMOS technology. For example, the work in [19], which was implemented in a 22nm CMOS technology, requires 24bits FCW_{SSC} to support 0~2% SSC modulation range and 25kHz modulation rate by consuming 15.4mA total current. Therefore, to overcome these limitations, a new in-loop-BW SSC modulation architecture is required.

Chapter 2 – Proposed SSC Architecture

Fig. 2-1 shows the block diagram of the proposed phase domain in-loop-BW SSC architecture. This proposed architecture consists of a phase frequency detector (PFD), charge pump (CP), discrete time loop filter (DT-LF), SSC return-to-zero (RZ) current digital-to-analog converter (I-DAC$_{SSC}$), digital integrator, ring VCO, and frequency divider (FD). The CLK GEN block creates three clock phases for the proposed charge-based DT-LF and I-DAC$_{SSC}$ at the rate of f_{REF}. The SSC frequency control word FCW$_{SSC}$ is a triangular spread-spectrum modulation signal, and this FCW$_{SSC}$ is digitally accumulated to convert to a phase domain modulation signal PCW$_{SSC}$. This accumulated PCW$_{SSC}$ drives the I-DAC$_{SSC}$, which injects the phase domain SSC modulation signal into the loop. The charge-based DT-LF combines both the I-DAC$_{SSC}$ modulation current (I_{SSC}) and charge pump current (I_{CP}), and updates V_{CTRL}.

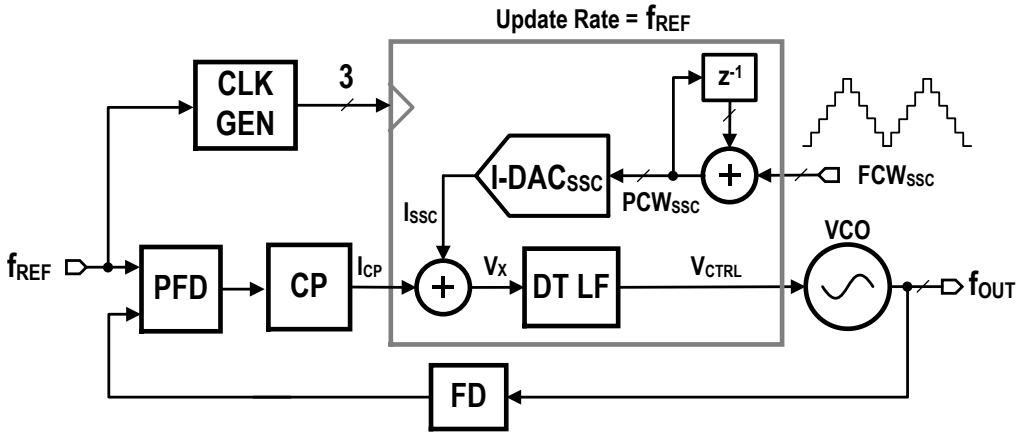


Figure 2-1: Block diagram of the proposed SSC architecture.

Similar to the phase domain in-loop-BW SSC modulation technique in all digital PLLs [18]-[19], this proposed scheme performs the SSC modulation in the phase domain. However, the phase domain operations are performed in the analog domain without the help of a TDC or phase quantizer. In addition, this proposed SSC architecture achieves

significant relaxed PVT sensitivity as other conventional in-loop-BW DSM-based or TDC-based SSC architectures achieve [14]-[19].

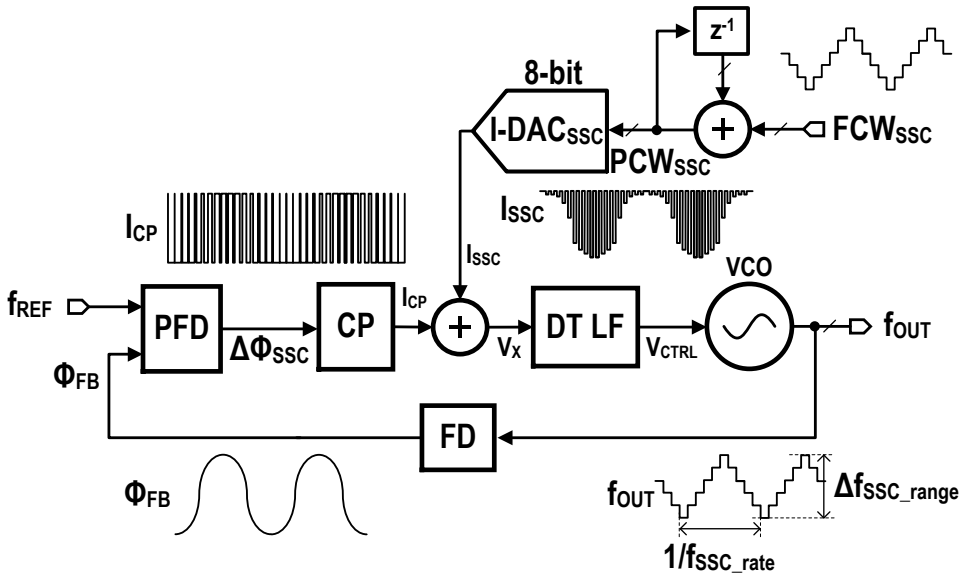


Figure 2-2: Proposed in-loop-BW SSC modulation technique.

2.1 Proposed Phase Domain In-Loop-BW SSC Modulation

Fig. 2-2 shows the proposed in-loop-BW SSC modulation technique. The SSC modulation of the output clock is achieved by providing a triangular ramp on the FCW_{SSC}. The digitally accumulated PCW_{SSC} is converted to the return-to-zero I_{SSC} in I-DAC_{SSC}, whose magnitude is proportional to PCW_{SSC} and the width is fixed to 50% of the reference period T_{REF}. Due to the SSC frequency modulation of the VCO, a SSC phase difference $\Delta\phi_{SSC}$, which is the difference between the divided VCO phase output ϕ_{FB} and the input reference frequency phase ϕ_{REF}, is created. This SSC phase difference $\Delta\phi_{SSC}$ results in the pulse-width modulated I_{CP} at the output of the charge pump. Since this SSC charge pump current I_{SSC} cancels a part of the I-DAC_{SSC} current I_{CP}, the residual current is integrated and converted to a charge signal on a sampling capacitor in the

proposed DT-LF. This sampled charge signal is filtered to generate a triangular SSC signal at V_{CTRL}, which modulates the VCO output frequency f_{OUT}.

In the proposed architecture, the loop filter input is the sum of I_{SSC} and I_{CP}. The I_{SSC} is a return-to-zero current pulse, whereas the I_{CP} is a pulse-width modulated current pulse. Filtering these two different types of current signals with a conventional passive loop filter creates unacceptable spurs at the output, which destroys the shape of the spread spectrum. Therefore, a new charge-based DT-LF is proposed. Before presenting details of the proposed DT-LF, it is useful to examine the limitations of a conventional charge-pump PLL with a passive loop filter in the proposed in-loop-BW SSC modulation technique.

2.2 Limitations of a Conventional Passive Loop Filter

In a charge-pump PLL with a conventional passive loop filter, it is common to model the PFD, CP, and loop filter as s-domain linear transfer functions [10], [23]. However, the PFD operation is discrete-time because the PFD samples phases and updates the difference at a rate of f_{REF}. In addition, the resulting current (I_{CP}) from the charge pump is a pulse-width modulated current, which maintains the information in its width. This charge pump current information is also updated at a rate of f_{REF}. Therefore, the PFD and CP are operating in a discrete-time manner.

When the SSC modulation is disabled, absolute jitter in the PLL creates phase error in the PFD, and results in very narrow current pulses at the output of the CP, whose standard deviation of the width is on the order of tens of pico-second. This very thin pulse-width modulated current pulse can be approximated as a corresponding impulse signal, whose magnitude is weighted by the phase error information. With this approximation, the linear s-domain transfer function for the PFD, CP, and passive LF can be obtained from the weighed impulse response of the passive LF, which is equivalent to convolving the weighted impulse signal with the s-domain transfer function of the passive loop filter.

However, when the SSC modulation is enabled, this continuous-time impulse approximation cannot be valid. Fig. 2-3 shows the one example of the transient response at the control voltage V_{CTRL} due to the SSC modulation with a conventional passive loop filter. First, the width T_W of the pulse-width modulated current pulses I_{CP} is too large (could be 75% of the update period (T_{REF})) to make the approximation. In addition, since the time constant of the loop filter (τ_{LF}) is relatively large with respect to the update period T_{REF}, the significant transient glitches appear at the control voltage V_{CTRL}. Finally, the transient glitches create unacceptable spurs at the output spectrum, and they destroy the shape of the spread-spectrum.

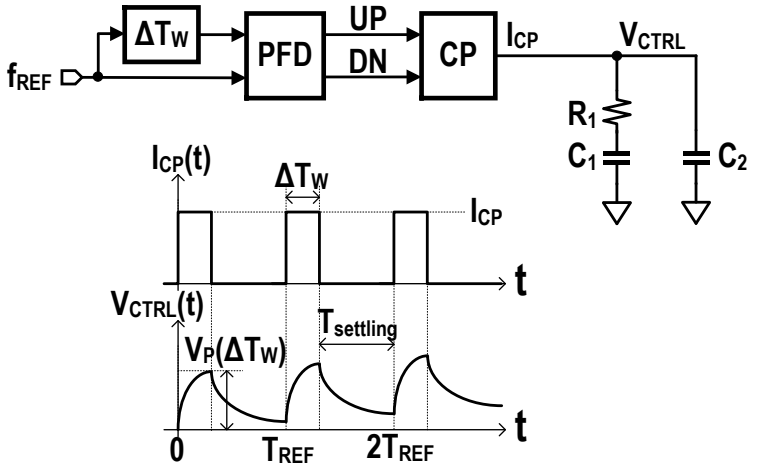


Figure 2-3: Test-bench of a conventional passive loop filter transient response.

To quantitatively elaborate this transient glitch, the peaking voltage (V_P) of the transient response at V_{CTRL} is calculated to:

$$\begin{aligned} V_P(T_W) &= \frac{I_{CP}}{C_1+C_2}\cdot T_W + I_{CP}R_1\cdot\frac{C_1^2}{(C_1+C_2)^2}\cdot(1-e^{-T_W/\tau_{LF}}) \\ &\cong \frac{I_{CP}}{C_1+C_2}\cdot T_W + I_{CP}R_1\cdot(1-e^{-T_W/\tau_{LF}}) \end{aligned} \tag{5}$$

where T_W, I_{CP}, and τ_{LF} are width of the charge pump current due to the SSC phase

difference $\Delta\phi_{SSC}$, the gain of the charge pump, and $R_1 \times C_1C_2/(C_1+C_2)$, respectively. The first term in (5) is the wanted output result at node V_{CTRL}, which is proportional to T_W, whereas the second term in (5) is unwanted transient glitch due to finite time constant τ_{LF}. This second term in (5) roots from the voltage drop across R_1 when the current I_{CP} goes through R_1 during T_W.

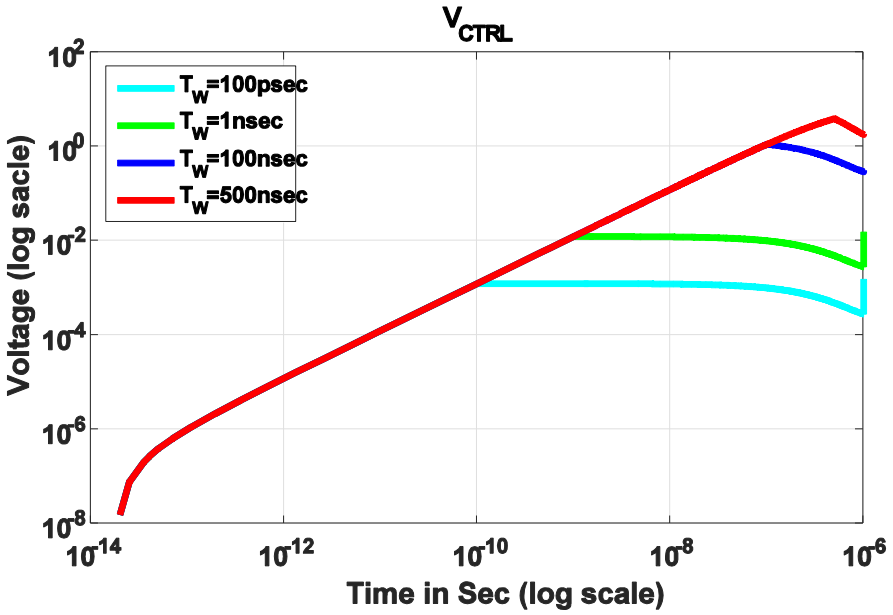


Figure 2-4: Transient simulation results for various T_W in the passive loop filter.

There are three important observations from (5): i) the undesired transient peaking is proportional to the product of I_{CP} and R_1, ii) a larger T_W delivers larger peaking voltage V_P, and iii) a larger T_W results in worse incomplete settling error due to shorter settling time (T_{REF}-T_W). Fig. 2-4 compares the transient simulation results for various T_W values in the conventional passive loop filter, whose design variables are R_1=5.65kohm, C_1=398pF, and C_2=79.6pF. I_{CP}=1mA, T_{REF}=1µsec, phase margin = 60°, and loop BW = $f_{REF}/10$ are used in the simulations. In this example, the loop filter time constant τ_{LF} is 0.375µsec in T_{REF}=1µsec, and this reveals that 100psec or 500nsec (50% of T_{REF}) of T_W gives 1.25mV or 3.93V voltage glitch V_P with 72.89µV or 0.763V incomplete settling

error, respectively. Therefore, these severe glitch and incomplete settling error are not acceptable for the proposed SSC modulation technique since the achievable maximum tuning range of the control voltage V_{CTRL} should be less than 500mV (or even smaller for a better linearity of K_{VCO})

2.3 Proposed Charge-Based Discrete Time Loop Filter (DT-LF)

In a conventional fractional-N synthesizer with a conventional passive loop filter, strong spurs due to the DSM dithering noise are well-known problem. Although the DSM dithering phase error at the PFD is not as large as the SSC modulation phase difference $\Delta\phi_{SSC}$, one can find some valuable insights from loop filter topologies in low spur fractional-N synthesizers.

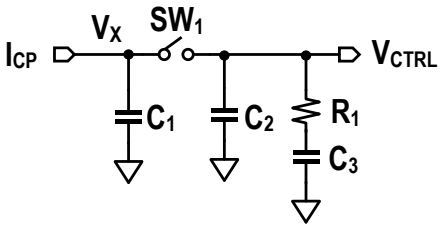


Figure 2-5: Sampled loop filter.

Particularly, the work in [24] presents the sampled loop filter as shown in Fig. 2-5. When SW_1 is open, the pulse-width modulated current pulse I_{CP} is integrated in a capacitor C_1. Then, when SW_1 is closed, the accumulated charge is shared to the conventional passive loop filter. Using this sampled loop filter, the second term of the glitch voltage V_P in (5) is significantly reduced. The glitch V_P is proportional to the voltage difference (V_X - V_{CTRL}), instead of the $I_{CP}\times R_1$ product. It is because when SW_1 is closed, the initial voltage drop across R_1 is V_X - V_{CTRL}. Generally, both I_{CP} and R_1 are important design parameters, and the loop gain K_{LG} (and loop BW) is proportional to the $I_{CP}\times R_1$ product. Therefore, there is a trade-off between the magnitude of the undesired transient glitch V_P and the loop gain K_{LG} (loop BW) in a conventional loop filter.

However, the sampled loop filter breaks this trade-off. In addition, since the voltage difference (V_X - V_{CTRL}) is generally much smaller than the $I_{CP} \times R_1$ product, this sampled loop filter significantly mitigates the spurs in a fractional-N synthesizer. However, similar to the conventional passive loop filter, the large time constant τ_{LF}, of this sampled loop filter is a bottleneck for the proposed DSM-free SSC modulation technique.

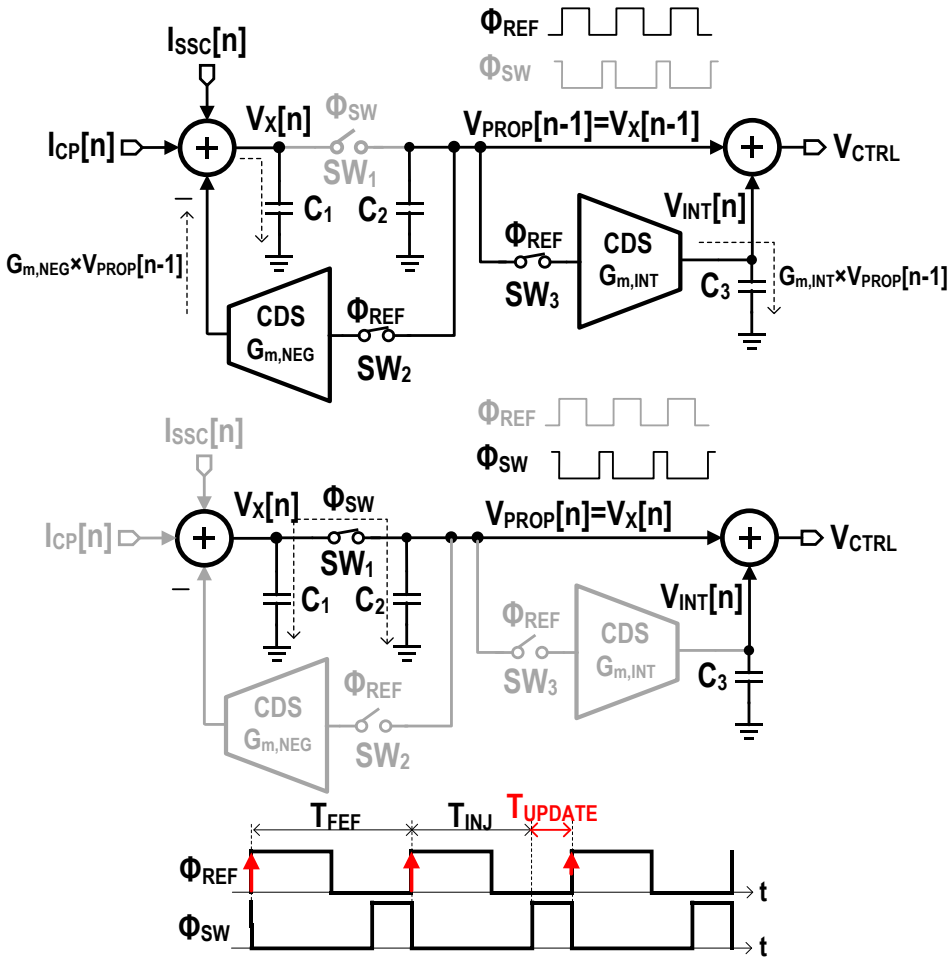


Figure 2-6: Block and timing diagram in the proposed charge-based DT-LF.

Fig. 2-6 shows the block and timing diagrams of the proposed DT-LF. It consists of two transconductors ($G_{m,NEG}$ and $G_{m,INT}$), three capacitors (C_1, C_2, and C_3), and three switches (SW_1, SW_2 and SW_3). The negative feedback $G_{m,NEG}$ is added to synthesize a stabilizing zero in the loop instead of a passive resistor R_1. This negative feedback loop also reduces the swing on the node V_X, improving the linearity of the charge pump and I-DAC_{SSC}. In addition, the G_{m_INT} integral path makes the proposed PLL a Type-II PLL. Any PVT variations from the VCO can be absorbed to the integral path at the node V_{INT}, and the proportional path V_{PROP} is nulled if the SSC modulation is disabled. This relaxes the charge pump, G_{m_NEG}, and I-DAC_{SSC} designs.

The proposed DT-LF operates in two phases: ϕ_{REF} and ϕ_{SW}. During ϕ_{REF}, the currents from $I_{SSC}[n]$, $I_{CP}[n]$, and the negative feedback current ($G_{m\_NEG} \times V_{PROP}[n-1]$) are accumulated on the capacitor C_1. At the same time, the SW_3 is closed and the current from G_{m_INT} ($G_{m\_INT} \times V_{PROP}[n-1]$) is integrated on the capacitor C_3. During ϕ_{SW}, the voltage $V_X[n]$ on capacitor C_1 is transferred to C_2 ($C_1 \approx 10C_2$). This switched mode operation of the proposed DT-LF helps to isolate the node V_{CTRL} from the large transient glitches, which appear at node V_X during ϕ_{REF}. Therefore, with the help of linear charge domain signal filtering, the proposed DT LF achieves in-loop-BW phase domain SSC modulation in analog domain.

2.4 PVT-Tolerant SSC Modulation

The proposed SSC architecture significantly relaxes any PVT variations in the proposed DT-LF and the VCO. This is because any PVT variations in the proposed DT-LF and the VCO are compensated by the loop gain of the PLL. This is key advantage of the proposed SSC modulation technique over the out-of-loop-BW direct SSC and two-point SSC modulations, where any change in K_{VCO} directly appears at the output f_{OUT}. Fig. 2-2 can be further simplified as Fig. 2-7 in order to derive a general form of the SSC modulation transfer function (TF_{SSC}) from the SSC modulation signal FCW_{SSC} to the output frequency f_{OUT}. The SSC modulation transfer function TF_{SSC} can be written as:

$$TF_{SSC} = \frac{K_{SSC} \cdot TF_{LF} \cdot \frac{K_{VCO}}{s}}{1 + TF_{LG}} \cong \frac{K_{SSC} \cdot TF_{LF} \cdot \frac{K_{VCO}}{s}}{K_{PFD+CP} \cdot TF_{LF} \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{M}} = \frac{K_{SSC}}{K_{PFD+CP} \cdot \frac{1}{M}} \quad (6)$$

where K_{SSC}, K_{PFD+CP}, and TF_{LF} are the gain of the SSC block, gain of the PFD and CP, and the transfer function of the loop filter, respectively. When the open-loop gain TF_{LG} is much larger than unity, the denominator of TF_{SSC} can be approximated to the open-loop gain TF_{LG}. Since TF_{LF} and K_{VCO}/s terms are common for both the numerator and denominator in TF_{SSC}, the transfer function TF_{SSC} does not rely on both TF_{LF} and K_{VCO}. In fact, the proposed SSC modulation technique is the in-loop-bandwidth SSC modulation, and the open-loop gain TF_{LG} has to be much larger than unity inside the loop BW. Therefore, one can guarantee that the condition in (6) is satisfied in the proposed SSC architecture.

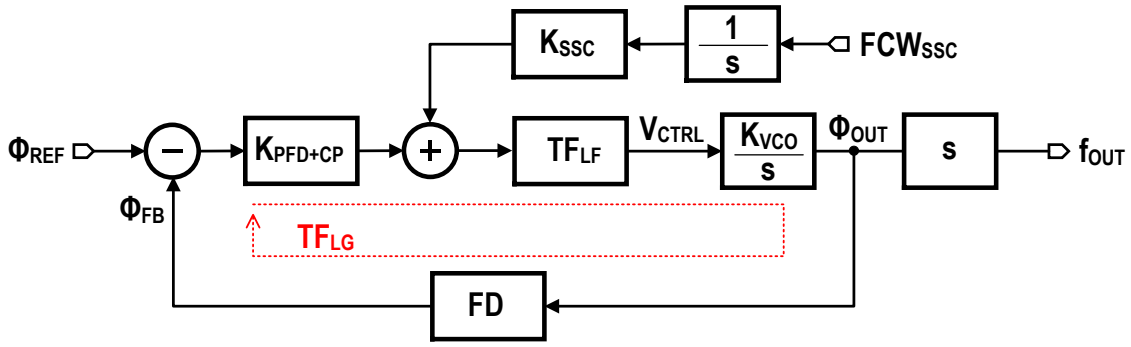


Figure 2-7: Block diagram for the SSC modulation transfer function (TF_{SSC}).

2.5 Correlated Double Sampling (CDS) Transconductor

The use of active elements in the proposed DT-LF results in inevitable DC offset and 1/f noise. Therefore, the correlated double sampling (CDS) scheme in [25] is

implemented in $G_{m,NEG}$ and $G_{m,INT}$ blocks, as shown in Fig. 2-8. The CDS transconductor consists of the main and auxiliary transconductor G_{m1} and G_{m2} with a sampling capacitor C_4. First, the auxiliary G_{m2} forms a negative feedback to sample the DC offset and 1/f noise during ϕ_2. Then the auxiliary G_{m2} loop compensates the sampled DC offset and 1/f noise during ϕ_1. When the CDS scheme is enabled, a significant reduction of 1/f noise is obtained on top of the DC offset cancellation.

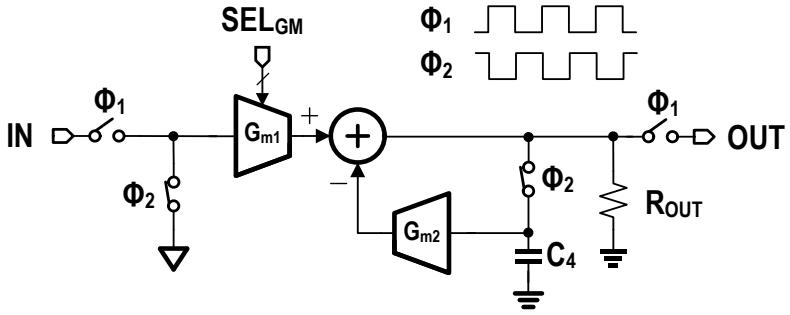


Figure 2-8: Correlated double sampling (CDS) scheme in the transconductors.

2.6 Range Limitation of the SSC Modulation

Fig. 2-9 shows the signal diagram of the proposed SSC modulation technique at the feedback path of a PLL. When the proper SSC modulation is obtained at the VCO, the output frequency $f_{OUT}(t)$ is slowly modulated as a triangular waveform. The corresponding output phase $\phi_{SSC,OUT}(t)$ is an integral of the triangular output frequency $f_{OUT}(t)$. The output phase $\phi_{SSC,OUT}(t)$ is then divided in the frequency divider, and it results in the modulated feedback phase $\phi_{FB}(t)$ or modulated time difference $\Delta t_{FB}(t)$ with respect to the reference input clock ϕ_{REF}.

The modulation phase $\phi_{FB}(t)$ or modulated time difference $\Delta t_{FB}(t)$ are slowly increasing when the modulated output frequency $f_{OUT}(t)$ is ramping. The $\phi_{FB}(t)$ and $\Delta t_{FB}(t)$ will reach at the peak phase or time modulations (ϕ_{FB_peak} and Δt_{FB_peak}) at the half of the SSC modulation period (T_{SSC_rate}). Note that the peak phase modulation value is equivalent to the area ($AREA_{peak}$) in the output frequency f_{OUT} waveform. Therefore, a

simple equation for an achievable maximum SSC modulation range $\Delta f_{SSC\_range(\%)}$ in percent can be written as:

$$\Delta f_{SSC\_range(\%)} \le \frac{4 \times \Delta t_{FB\_peak}}{T_{SSC\_rate}} \times 100 = 400 \times \Delta t_{FB\_peak} \times f_{SSC\_rate} \quad (7)$$

Therefore, for a given f_{SSC_rate}, a larger $\Delta f_{SSC,range(\%)}$ is achieved by increasing the maximum time modulation range Δt_{FB_peak}. Note that larger Δt_{FB_peak} results in larger update period T_{REF}, indicating a slower update frequency f_{REF}. This is because the peak time SSC modulation Δt_{FB_peak} (or ϕ_{FB_peak}) cannot exceed to the update period T_{REF} (or 2π), and this limits the maximum achievable SSC modulation range in (7). Therefore, to achieve wider spread spectrum modulation range $\Delta f_{SSC,range}$, one needs to use a lower f_{REF}. Since the maximum loop BW is typically less than $f_{REF}/10$ due to stability concerns, lowering f_{REF} reduces the maximum achievable loop BW and results in less suppression of the VCO phase noise. Therefore, there is a trade-off between the reference frequency

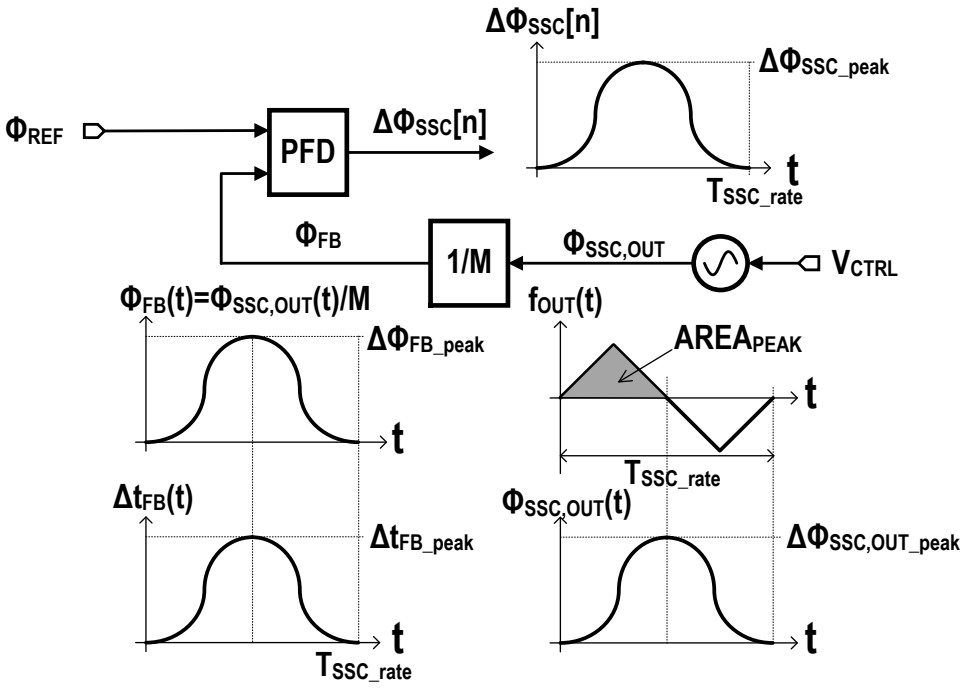


Figure 2-9: Signal diagram of the proposed SSC modulation at the feedback path.

f_{REF} (or jitter suppression of the VCO phase noise) and the SSC modulation range $\Delta f_{SS,range}$.

Chapter 3 – Modeling the Proposed SSC Architecture

In this chapter, two linear equivalent models of the proposed SSC architecture will be derived. These derived linear models (z-domain and hybrid-domain models) will be discussed to inspect limitations of their practice. The z-domain linear model will be exploited to analyze the loop stability, such as the phase margin and root locus analysis. In addition, the hybrid-domain linear model will be used for jitter analysis, and this jitter analysis will be carried on in chapter 4.

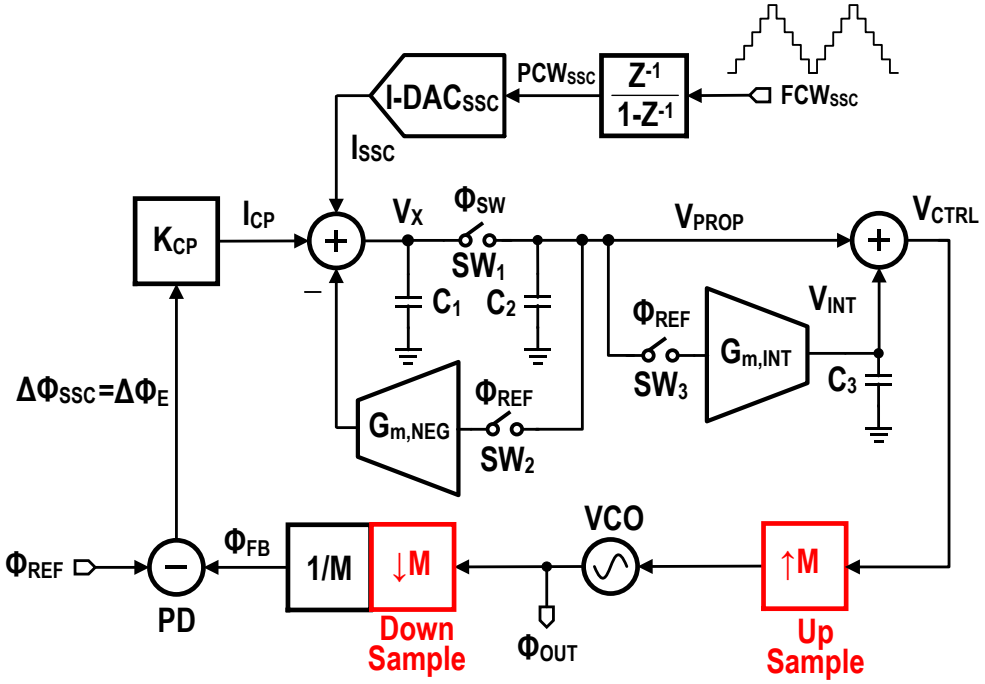


Figure 3-1: Details of the block diagram in the proposed SSC architecture.

Fig. 3-1 shows the details of the block diagram in the proposed SSC modulation architecture. Based on Fig. 2-1, there are up-sampling and down-sampling operations before and after the VCO since the output frequency of the VCO is M-time faster than the update rate f_{REF}.

3.1 z-Domain Model

To derive transfer functions of a linear PLL model in the proposed SSC architecture, one needs to analyze charge domain signal operations at the proposed charge-based DT-LF. First, the amount of charges injected into the capacitor C_1 are

$$\begin{aligned} Q_{CP}[n] &= \frac{I_{CP}}{2\pi} \cdot T_{REF} \cdot \Delta\phi_{SSC}[n-1] \\ Q_{SSC}[n] &= \frac{T_{REF}}{2} \cdot I_{SSC,LSB} \cdot PCW_{SSC}[n-1] \\ Q_{GM\_NEG}[n] &= -\frac{T_{REF}}{2} \cdot G_{m\_NEG} \cdot V_{PROP}[n-1] \end{aligned} \tag{8}$$

where $Q_{CP}[n]$, $Q_{SSC}[n]$, and $Q_{GM\_NET}[n]$ are updated charges from the charge pump, I-DAC_{SSC}, and transconductor G_{m_NEG}, respectively. The $\Delta\phi_{SSC}$ and $I_{SSC,LSB}$ are the phase modulation difference at the PFD and the least-significant bit current in the I-DAC_{SSC}, respectively. There is $T_{REF}/2$ gain factor at $Q_{SSC}[n]$ and $Q_{GM\_NEG}[n]$, since both I-DAC_{SSC} and G_{m_NEG} are enabled during only half of the update period T_{REF}. Therefore, the updated $V_{PROP}(z)$ can be written as:

$$V_{PROP}(z) = \frac{I_{CP}}{2\pi} \cdot \frac{T_{REF}}{C_{12}} \cdot \frac{z^{-1}}{1-\kappa_1 z^{-1}} \cdot \Delta\phi_{SSC}(z) + \frac{T_{REF}}{2} \cdot \frac{I_{SSC,LSB}}{C_{12}} \cdot \frac{z^{-1}}{1-\kappa_1 z^{-1}} \cdot PCW_{SSC}(z) \tag{9}$$

where, $\kappa_1=1-(T_{REF}/2)\times(G_{m\_NEG}/C_{12})$ and $C_{12}=C_1+C_2$, respectively. Due to the local feedback G_{m_NEG}, the position of the pole at DC is modulated to κ_1, and this modulated pole at κ_1 can be cancelled when $(T_{REF}/2)\times(G_{m\_NEG}/C_{12})=1$. Moreover, the pole position κ_1 is a function of the ratio between the G_{m_NEG} and C_{12}, indicating that design scaling for both power and area can be achieved without disturbing the transfer function.

The transfer function of the proportional and integral dual-path loop filter can be written as:

$$V_{CTRL}(z) = \frac{1-\kappa_2 z^{-1}}{1-z^{-1}} \cdot V_{PROP}(z) \tag{10}$$

where, $\kappa_2=1-(T_{REF}/2)\times(G_{m\_INT}/C_3)$. This dual-path loop filter establishes one pole at DC and one zero at κ_2, and a type-II PLL is achieved. Note that the position of the additional

zero κ_2 is also a function of the ratio between the G_{m_INT} and C_3.

As shown in Fig. 3-1, the VCO update rate is M-times faster than the reference frequency f_{REF}. However, since V_{CTRL} is only updated in every f_{REF}, one can derive the linear z-domain transfer function for the VCO as:

$$K_{VCO} \cdot T_{REF} \cdot \frac{z^{-1}}{1-z^{-1}}\Big|_{f=f_{REF}} \tag{11}$$

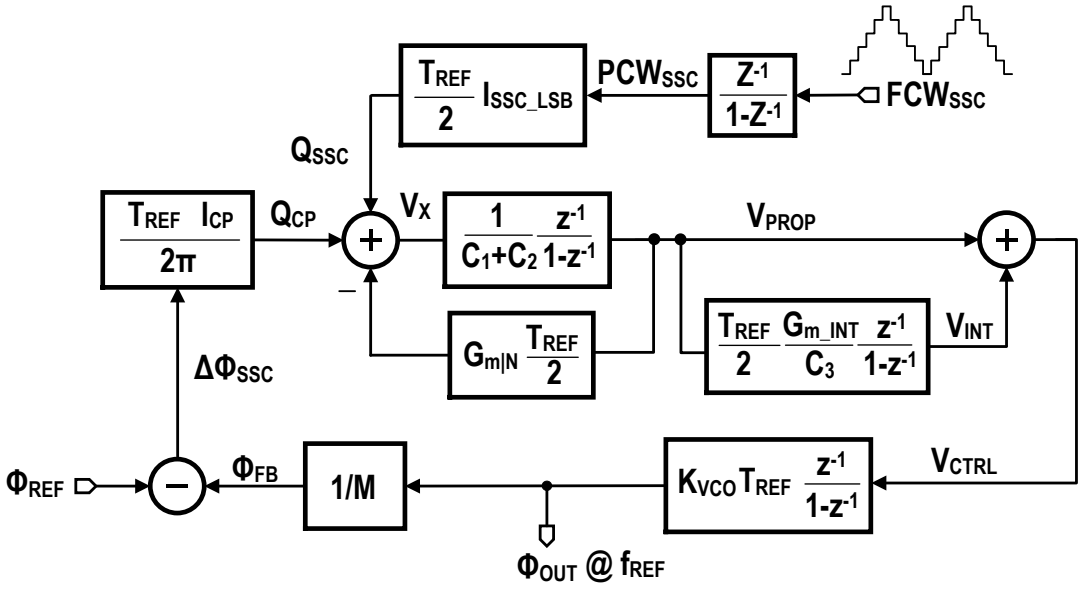


Figure 3-2: z-domain model of the proposed PLL.

Therefore, the block diagram of the z-domain linear PLL model for the proposed SSC architecture can be redrawn as in Fig. 3-2. This simplified discrete-time z-domain PLL model is sufficient to analyze PLL loop dynamics such as the loop gain K_{LG}, phase margin PM, and pole-zero locations. Note that although the Bode analysis originated with continuous-time system which can be described in s-domain, interpretations of the z-domain Bode plot for a PLL are accurate enough to give good estimations [26].

The transfer function for the open-loop gain $TF_{LG}(z)$ and the SSC modulation $TF_{SSC}(z)$ are written as:

$$TF_{LG}(z)=\frac{T_{REF}}{2\pi}\cdot\frac{I_{CP}}{C_{12}}\cdot K_{VCO}\cdot T_{REF}\cdot\left(\frac{z^{-1}}{1-z^{-1}}\right)^{2}\cdot\frac{1-\kappa_2 z^{-1}}{1-\kappa_1 z^{-1}}. \quad (12)$$

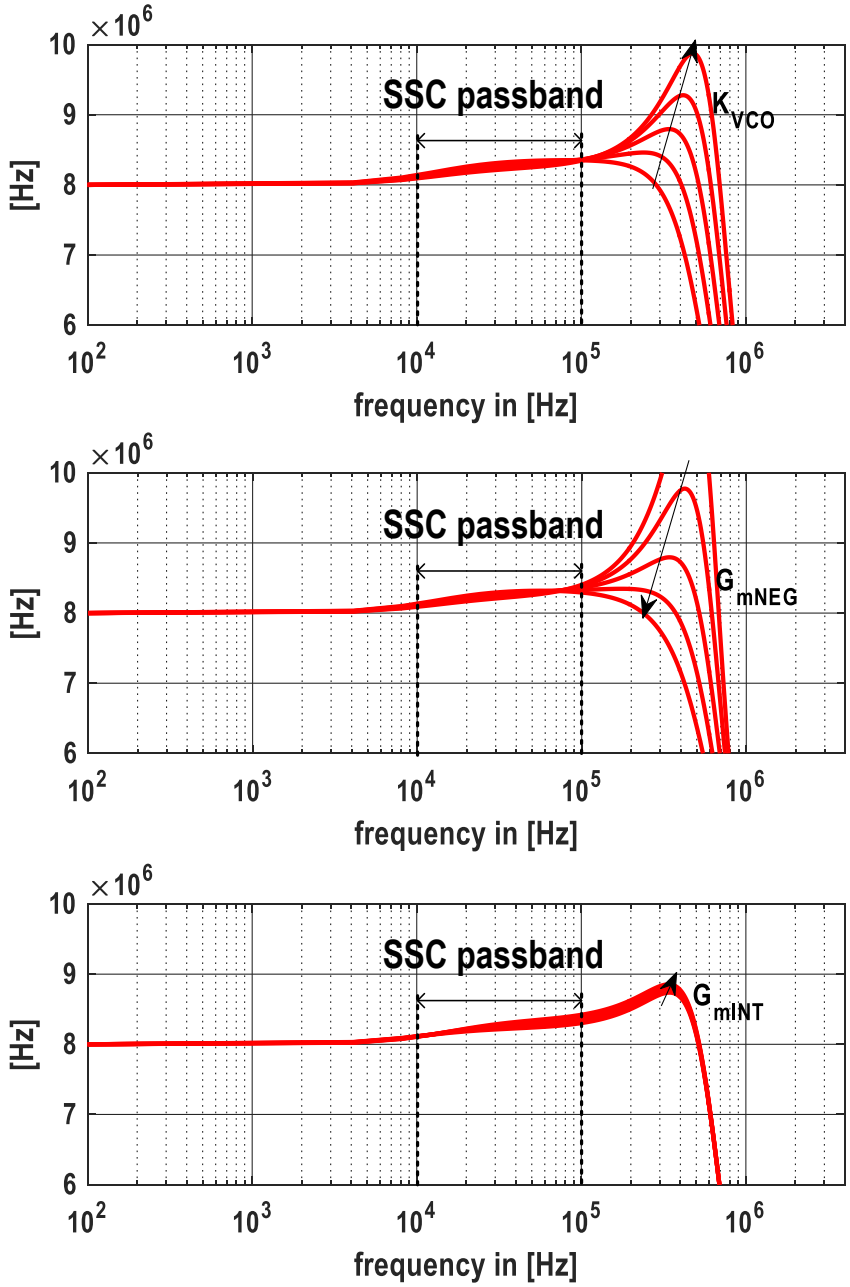


Figure 3-3: PVT sensitivity simulations: K_{VCO}, G_{m_NEG}, and G_{m_INT} for ±20% of the nominal value for f_{REF}=8MHz.

$$TF_{SSC}(z)=\frac{f_{OUT}}{FCW_{SSC}}=\frac{K_{VCO}}{2\pi}\cdot\frac{V_{CTRL}}{FCW_{SSC}}(z)\underset{DC}{\Rightarrow}\frac{I_{SSC,LSB}/2}{I_{CP}/M}\cdot f_{REF} \quad (13)$$

From (13), when the frequency is lower than the loop BW, $TF_{SSC}(z)$ is a function of $I_{SSC,LSB}/I_{CP}$, and the gain of the SSC modulation is proportional to f_{REF}. This indicates that the magnitude frequency response of TF_{SSC} below the loop BW does not depend on either design parameters of the proposed DT-LF or K_{VCO}. Fig. 3-3 shows the PVT sensitivity simulation results due to K_{VCO}, G_{m_NEG}, and G_{m_INT} variations which is ±20% of the nominal value. Because all three variables (K_{VCO}, G_{m_NEG}, and G_{m_INT}) modulate the loop gain K_{LG} and the damping ratio of the loop, the magnitude frequency response of TF_{SSC} around the loop BW is varied due to their changes. However, when a frequency band is relatively smaller than the loop BW (less than 10kHz in Fig. 3-3), a fixed and consistent TF_{SSC} magnitude gain is observed. Therefore, if one can push the loop BW much higher than the SSC modulation pass band, the PVT insensitive modulation gain in TF_{SSC} can be achieved. This limitation is generally true for all conventional in-loop-BW SSC techniques.

3.2 Hybrid-Domain Model

Since the derived z-domain PLL model in Fig. 3-2 is valid up to $f_{REF}/2$, this PLL model should not be sufficient for jitter estimations. It is because the output phase noise is generally integrated up to a few hundred MHz to calculate the integrated phase jitter. There are several advanced modeling techniques [27]-[28] to overcome this limitation. The work in [27] up-samples the control voltage V_{CTRL} from f_{REF} to f_{OUT} at a VCO, and down-samples the output phase ϕ_{OUT} to the feedback phase ϕ_{FB} of the PFD as did in Fig. 3-1, and this modeling technique supports the phase noise transfer function up to $f_{OUT}/2$. In [28], the CT-to-DT and DT-to-CT conversion steps are added before and after a VCO, and the linear model of the VCO is built in s-domain. This hybrid-domain modeling technique provides the unbounded modeling range with the proposed DT-LF. In addition, jitter calculations are generally done in a numerical tool, and evaluating frequency

responses of this hybrid-domain PLL model is easily performed using a numerical tool. Therefore, the simpler z-domain PLL model in (12) is exploited for the stability and root locus analysis, while this extensive hybrid-domain PLL model is necessary for jitter calculations.

Fig. 3-4 shows the DT-to-CT and CT-to-DT conversions around the VCO. The zero-order-hold block is well-known as the DT-to-CT conversion, and its transfer function $H_{DT\text{-}CT}$ can be approximated as:

$$\left|H_{DT-CT}(s)\right| = \left|T_{REF}\cdot e^{-j\omega T_{REF}/2}\cdot \mathrm{sinc}\left(\omega T_{REF}/2\right)\right| \underset{\omega T_{REF}<<1}{\Rightarrow} T_{REF}$$

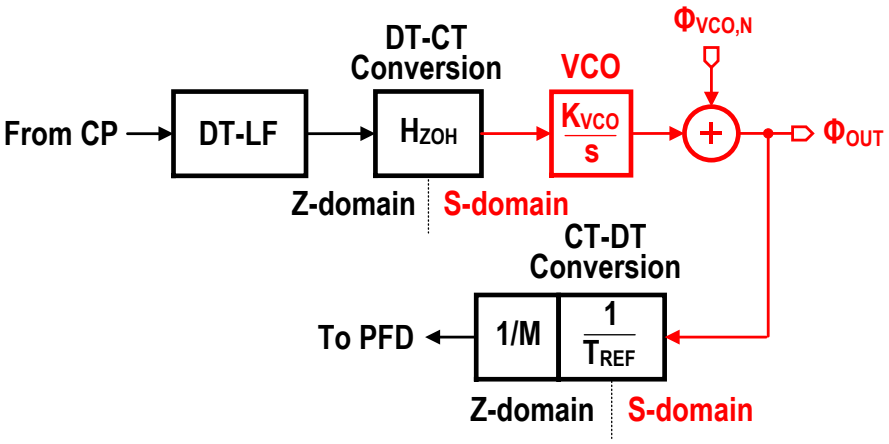


Figure 3-4: DT-to-CT and CT-to-DT conversions around the VCO.

Similarly, the CT-to-DT conversion can be modeled using an impulse train sampling, and its transfer function $H_{CT\text{-}DT}$ can be approximated as:

$$\left|H_{CT-DT}(s)\right| = \left|\frac{1}{T_{REF}}\sum_{n=-\infty}^{\infty}\delta(f-nf_{REF})\right| \underset{\omega T_{REF}<<1}{\Rightarrow} \frac{1}{T_{REF}}$$

Finally, Fig. 3-5 shows the final hybrid-domain PLL model for the proposed SSC architecture. The CT-to-DT conversion block can be moved to in front of the phase detector because the phase detector also samples the input reference clock phase ϕ_{REF} and subtracts it from the sampled feedback phase ϕ_{FB}. Based on this hybrid-domain PLL

model, four major transfer functions are written as:

$$TF_{LG}(z,s)=\frac{T_{REF}}{2\pi}\cdot\frac{I_{CP}}{C_{12}}\cdot\frac{K_{VCO}}{s}\cdot\frac{1}{M}\cdot\left(\frac{z^{-1}}{1-z^{-1}}\right)\cdot\frac{1-\kappa_2 z^{-1}}{1-\kappa_1 z^{-1}} \tag{14}$$

$$TF_1(z,s)=\frac{\phi_{OUT}}{\phi_{REF}}=\frac{\frac{T_{REF}}{2\pi}\cdot\frac{I_{CP}}{C_{12}}\cdot\frac{K_{VCO}}{s}\cdot\left(\frac{z^{-1}}{1-z^{-1}}\right)\cdot\frac{1-\kappa_2 z^{-1}}{1-\kappa_1 z^{-1}}}{1+TF_{LG}(z,s)} \tag{15}$$

$$TF_2(z,s)=\frac{\phi_{OUT}}{\phi_{VCO}}=\frac{1}{1+TF_{LG}(z,s)} \tag{16}$$

$$TF_{SSC}(z,s)\underset{DC}{\Rightarrow}\frac{I_{SSC,LSB}/2}{I_{CP}/M}\cdot f_{REF} \tag{17}$$

For the loop BW (equivalently loop gain K_{LG}) calculation, one can calculate the s-domain counterpart of (14) based on the time-continuous approximation in [29]. Using the first-order approximation of $z=\exp(sT_s)$, when $|sT_s|$ is much smaller than 1, z^{-1} and $1-z^{-1}$ are approximated to 1 and sT_s, respectively. Therefore, the loop gain from from (14) can be

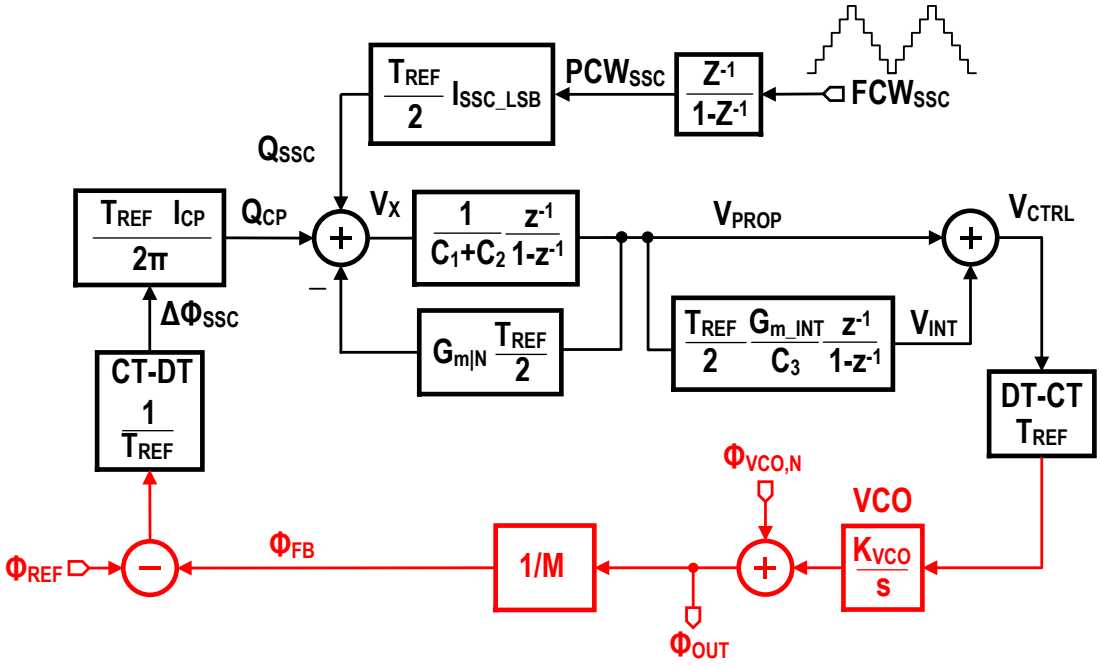


Figure 3-5: Hybrid-domain model of the proposed PLL.

rewritten as:

$$K_{LG} = I_{CP} \cdot \frac{1}{G_{m\_NEG}/2} \cdot \frac{K_{VCO}}{2\pi} \cdot \frac{1}{M} \tag{18}$$

where 2π is added because the unit of the K_{VCO} is rad×Hz/volt. Since the conventional type-II charge-pump PLL with a passive loop filter depicted in Fig. 2-3 gives the loop gain $K_{LG} = I_{CP} \times R_1 \times (K_{VCO}/2\pi)/M$, the negative transconductance G_{m_NEG} in this proposed DT-LF actually replaces the role of R_1. This provides a significant design flexibility because there is no transient glitch problem in (5) and pole-zero perturbations due to G_{m_NEG} can be eliminated if G_{m_NEG}/C_{12} ratio is kept as a constant.

To compare this hybrid-domain PLL model with others, Fig. 3-6 shows the simulated frequency response results for TF_1 and TF_2, where the reference frequency f_{REF}

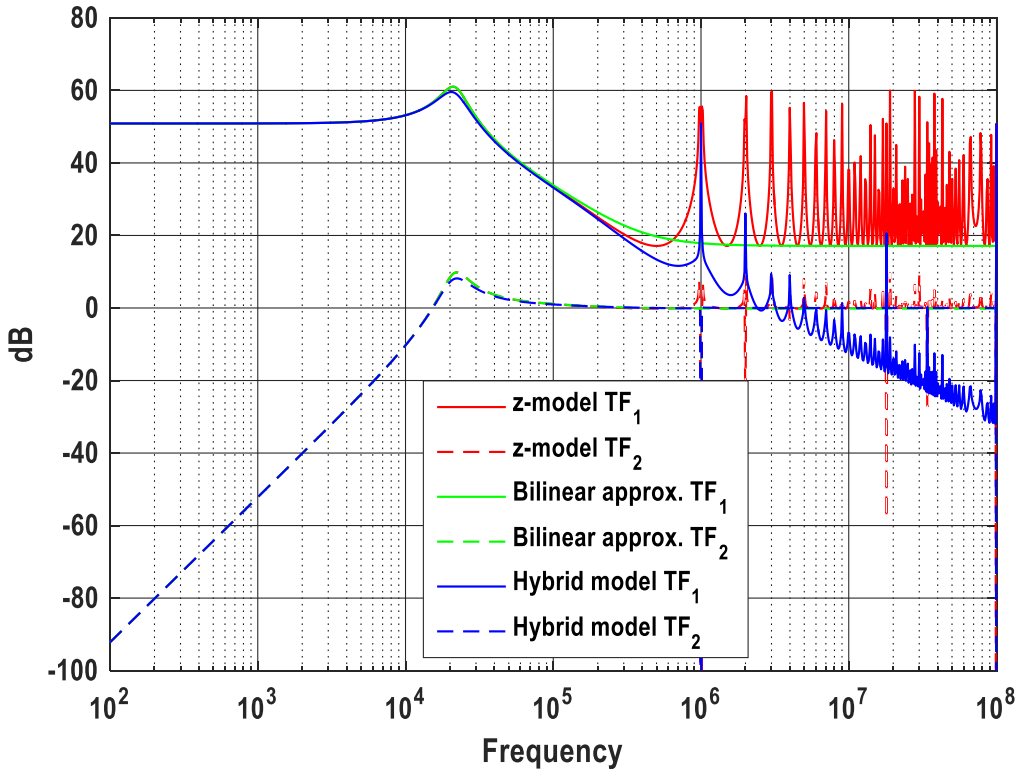


Figure 3-6: Comparisons for different PLL modeling techniques: z-domain, Bilinear approximated, and hybrid model for TF_1 and TF_2.

and output frequency f_{OUT} are 1MHz and 352MHz, respectively. First, the transfer functions for TF_2 are quite similar for all PLL models except the Bilinear PLL model, which gives a little higher peaking at around the loop BW. Second, the magnitude frequency responses of TF_1 begins to deviate when the frequency is greater than 1/10 of f_{REF}. The z-domain PLL model in Fig. 3-1 delivers a good approximation of TF_1 up to $f_{REF}/2$. The magnitude frequency response of TF_1 in the Bilinear PLL model is saturated after the $f_{REF}/2$ and does not roll off. However the hybrid-domain PLL model provides a continuous roll off after the reference frequency f_{REF}. Therefore, the hybrid-domain PLL model is suitable for jitter calculations for the proposed SSC architecture.

Chapter 4 – Circuit Implementations

4.1 Phase Frequency Detector (PFD)

In this work, the tri-state overlap and offset phase frequency detector (PFD) in [30] is implemented as shown in Fig. 4-1. Similar to a conventional tri-state PFD, there are two D-FFs and reset signal (RST_0). The additional two separate delay cells, which establish the overlap delay (Δt_{OV}) and offset delay (Δt_{OS}) at the reset signal path, are added to provide different reset edges (RST_{REF} and RST_{FB}) for two D-FFs.

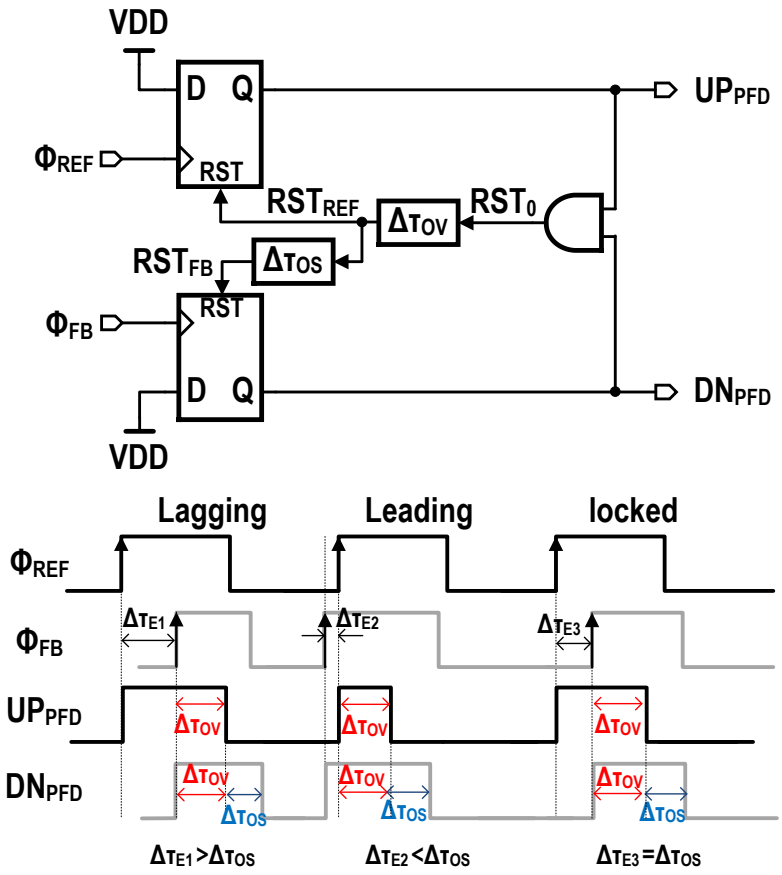


Figure 4-1: Block and timing diagrams of the phase frequency detector (PFD).

The timing diagrams are shown in the bottom of the figure. When the feedback phase ϕ_{FB} is lagged by $\Delta\tau_{E1}$ from the rising edge of the reference phase ϕ_{REF}, the UP_{PFD} and DN_{PFD} have the width of $\Delta\tau_{E1}$ and zero in a conventional PFD. However, due to the overlap and offset delays (Δt_{OV} and Δt_{OS}), the UP_{PFD} has additional fixed overlap delay Δt_{OV} and the DN_{PFD} has additional fixed overlap delay Δt_{OV} and offset delay Δt_{OS}. Since $\Delta\tau_{E1}$ is greater than the offset delay Δt_{OS}, the larger width of the UP_{PFD} triggers a VCO to lead the feedback phase ϕ_{FB}. When the feedback phase ϕ_{FB} is led by $\Delta\tau_{E2}$, the phase error $\Delta\tau_{E2}$ is smaller than the offset delay Δt_{OS}, the larger width of the DN_{PFD} triggers a VCO to lag the feedback phase ϕ_{FB}. Finally, when the loop is locked, the phase error $\Delta\tau_{E2}$ equals to the offset delay Δt_{OS}, and this results in the matched width for both UP_{PFD} and DN_{PFD}. Therefore, the net charge at the charge pump is zero and a VCO holds a same feedback phase position.

The overlapping delay cell gives the constant overlap time Δt_{OV} for both the UP and DN pulses (UP_{PFD} and DN_{PFD}). In a conventional tri-state PFD, when the two phases (ϕ_{REF} and ϕ_{FB}) are locked, it generates very narrow impulse UP_{PFD} and DN_{PFD} signals. The problem is that finite rising/falling transition time of UP/DN currents in the charge pump could be comparable or larger than the width of UP_{PFD} or DN_{PFD} impulse, and this results in the dead-zone at the PFD and charge pump. Therefore, this constant overlapping time Δt_{OV} for both the UP_{PFD} and DN_{PFD} helps to mitigate the dead-zone problem [31]. In addition, this overlap time Δt_{OV} provides longer time for the common-mode feedback amplifier in the charge pump to correct systematic mismatches between top and bottom tail current sources.

The offset delay cell creates the skewed ϕ_{FB} when the loop is locked. The main advantage of this offset delay Δt_{OS} is that one can push the locked position in a PFD away from the inevitable dead-zone as amount of the offset time Δt_{OS}. This offset time Δt_{OS} helps to mitigate spurs from the associated non-linearity in the dead-zone [30]. Therefore, the offset time Δt_{OS} has to be greater than the sum of the dead-zone range and the peak-to-peak absolute jitter.

A TSPC-based PFD from [32] is implemented in this work. This TSPC-based PFD provides approximately 4~8 dB better phase noise compared to other NAND- and NOR-based PFDs [33].

The charge pump rising/falling transition times are simulated, and they are around 150psec to 300psec depending on the corners and temperatures in a 0.18μm technology. In addition, the targeting maximum rms jitter is around $100psec_{rms}$, and the peak-to-peak absolute jitter should be around 14-times. Therefore, the offset and overlap times are set around 1.5nsec to 3.0nsec, which are able to be calibrated using the power supply of the PFD. Note that too large overlap and offset delays exaggerate not only both the PFD and charge pump phase noises, but also random jitter at the delay cells in the reset path.

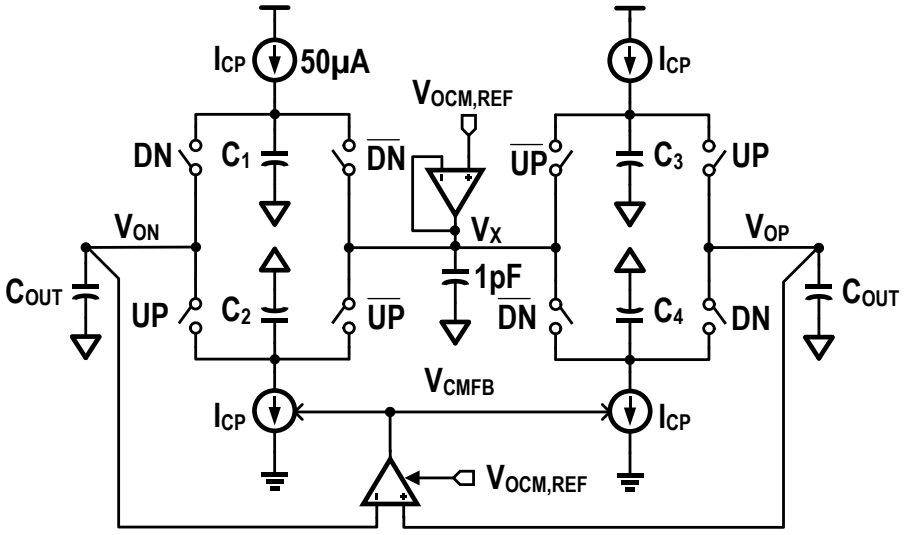


Figure 4-2: Schematic of the charge pump (CP).

4.2 Charge Pump (CP)

In order to eliminate systematic mismatches, a fully differential charge pump (CP) with a servo loop in [34] is implemented as shown in Fig. 4-2. There are top/bottom tail current sources with a fixed charge pump current gain I_{CP} =50μA. The output common-

mode voltage is sensed using source followers following a resistive sensing network, because the outputs (V_{OP} and V_{ON}) have to swing more than $1V_{P-P}$ if the SSC modulation is enabled. This sensed common-mode is compared to the common-mode reference $V_{OCM,REF}$, and fed back to the bottom sink current source. There are UN and DN switches, which route the top source current to either the outputs (V_{OP} and V_{ON}) or the node V_X. When both UP and DN switches are disabled, two top source currents pull the current I_{CP} through V_X and sink to two sink current sources. The dummy switches, which are not shown in the figure, are implemented to absorb the charge sharing non-ideality from the UP/DN switches. The extra capacitors ($C_{1\sim4}$), which are 100fF, prevent the top/bottom tail current sources from falling into a triode region during the UP/DN transitions.

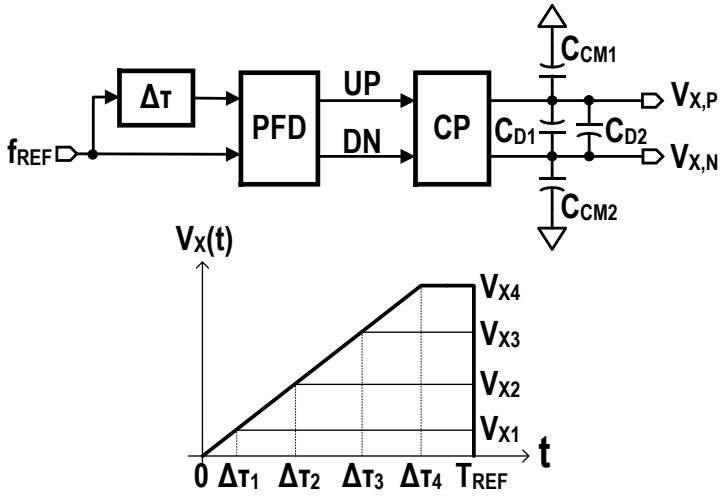


Figure 4-3: Test-bench for PFD+CP linearity simulations.

One unity-gain buffer at the node V_X is implemented, instead of two separated buffers in [35]. In this proposed SSC architecture, PVT variations at a VCO are absorbed into the integral path (V_{INT}), and the output of the CP (V_X and V_{PROP}) is guaranteed to have a zero mean when the SSC modulation is disabled. Therefore, the node V_{OP} and V_{ON} are supposed to be held to equal to $V_{OCM,REF}$, and one unity-gain buffer for the node V_X is

sufficient.

The linearity for PFD+CP in the proposed SSC architecture is examined in transistor level simulations. Fig. 4-3 shows the test-bench for PFD+CP linearity simulations. An arbitrary delay generator is added at one of the inputs in the PFD, and the capacitor C_1 in Fig. 3-1 is decomposed into the differential capacitor pair ($C_{D1\sim2}$) and the common-mode capacitor pair ($C_{CM1\sim2}$). The additional input delay ($\Delta\tau$) at the input creates a finite UP pulse, whose width is equivalent to $\Delta\tau$. This pulse-width modulated UP current dumps charges into the capacitors, and the integrated voltage at the node V_{XP} and V_{XN} are measured to calculate the gain from $\Delta\tau$ to V_X for various input delays ($\Delta\tau_i$).

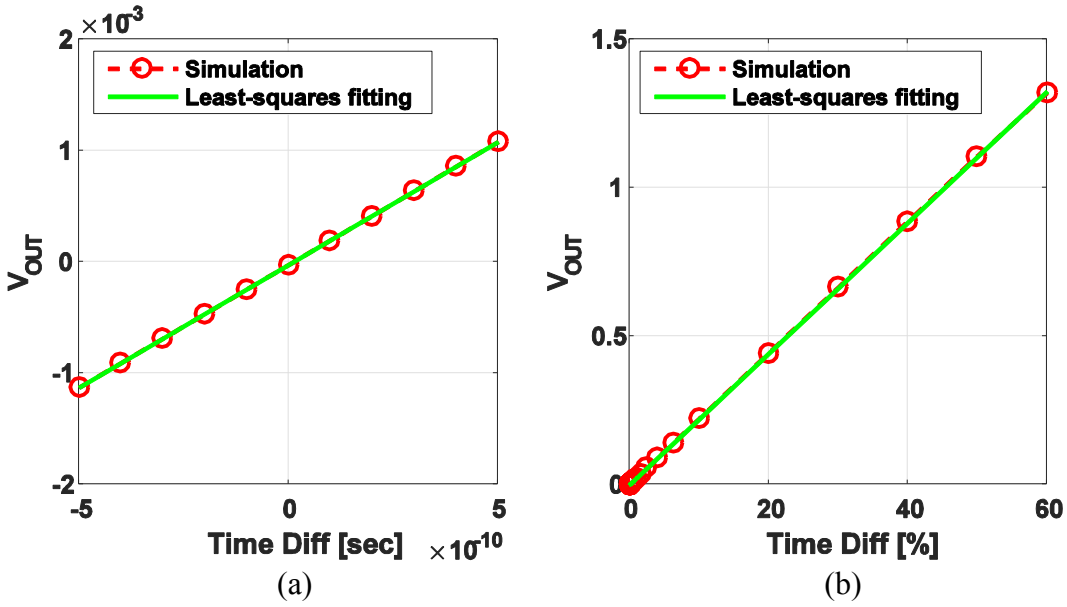


Figure 4-4: Simulated voltage at the node V_X for various delay differences ($\Delta\tau_i$).

Fig. 4-4 plots the voltage at the node V_X for various delay differences (Δt_i). Fig. 4-4(a) shows the zoom-in V_X when the delay $\Delta\tau$ is around zero, revealing that the overlap and offset techniques push the dead-zone away from the normal acquisition range. Fig. 4-4(b) shows the plot of V_X when the delay $\Delta\tau$ is swept from zero to 60% of the reference period T_{REF}. Note that the dead-zone is pushed to negative time delay, and it is not shown

in both figures. Based on the least-squares fitting approximation, the final non-linearity in PFD+CP is simulated and shown in Fig. 4-5. This result shows that the maximum error is 0.458% for $1.3V_{peak}$ maximum swing. A third order nonlinearity due to the channel length modulation of the top/bottom current sources is a dominant distortion source, and the linearity of the PFD+CP strongly relies on the finite output resistance at the output of the charge-pump. In general, for a given fixed intrinsic gain of a transistor, one can obtain a higher output resistance by decreasing the current (or transconductance) of the current source. Therefore, power efficient design in this work can reduce the charge pump current gain I_{CP} down to 10~50μA, and this implicitly results in better linearity.

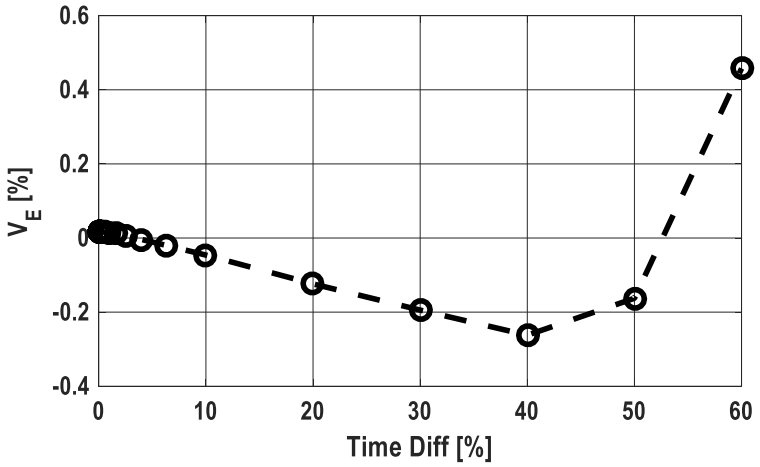


Figure 4-5: Simulated linearity error in the proposed PFD+CP.

4.3 Proposed Charge-Based Discrete Time Loop Filter (DT-LF)

The block diagram of the proposed charge-based DT-LF is found in Fig. 2-6. There are two critical non-idealities in the proposed DT-LF: DC offset and 1/f noise. The DC offset of G_{m_NEG} and G_{m_INT} creates finite leaking current when the two transconductors are disabled, and this leaking current results in a sawtooth waveform at the node V_{PROP} and V_{INT}, respectively. In addition, the 1/f noise of G_{m_NEG} and G_{m_INT}

directly appears at the output phase ϕ_{OUT} with the gain of K_{VCO}. Fig. 4-6 shows the frequency response from the input of G_{m_NEG} and G_{m_INT} to the output phase ϕ_{OUT}. From this figure, although the frequency response from V_{CTRL} to ϕ_{OUT} is a band-pass response, the integral path gain through G_{m_INT} amplifies the low frequency band of both transfer functions (ϕ_{OUT}/G_{m_NEG} and ϕ_{OUT}/G_{m_NEG}). This makes the magnitude response of the transfer fuctions, ϕ_{OUT}/G_{m_NEG} and ϕ_{OUT}/G_{m_NEG}, a low-pass response. The 1/f noise from the two transconductors occurs at the output ϕ_{OUT} without filtering. Therefore, the correlated double sampling (CDS) technique is necessary to eliminate the 1/f noise.

Fig. 4-7 shows the schematic of the transconductor with the CDS scheme, where the transconductor cell is modified from [36]. The top circuitry is working as the main transconductor, and the bottom transistor M_{2P} and M_{2N} are copying the output current of the main transconductor into the output (OUT_P and OUT_N). When ϕ_1 is enabled, the differential input (IN_P-IN_N) directly appears between V_{AP} and V_{AN}, which is across the

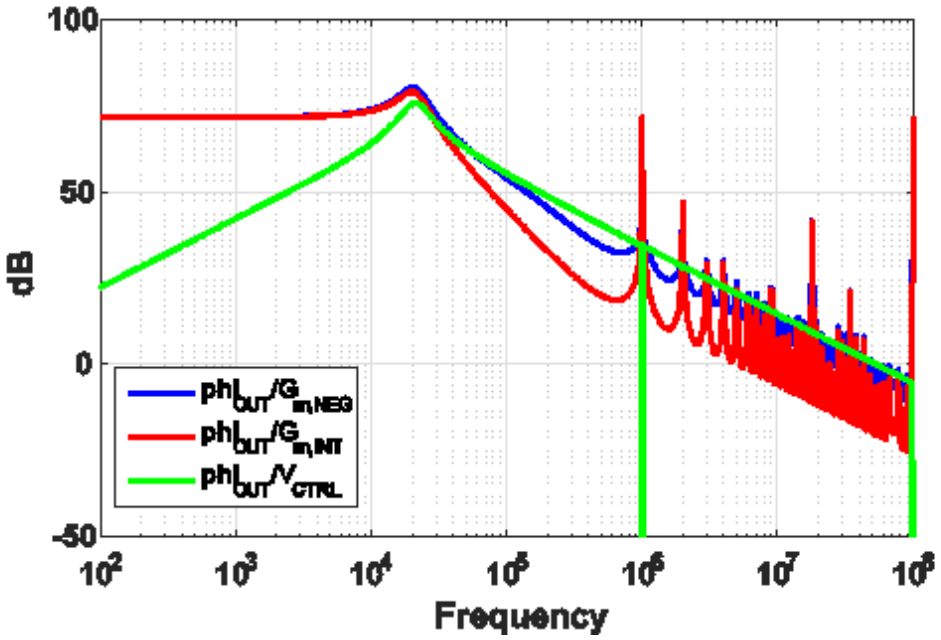


Figure 4-6: Frequency response from 1/f noise of the proposed DT-LF to the output phase.

binary R-bank. This is because the local negative feedback through M_3 to M_1 makes the voltage V_{SG} of M_3 fixed due to the sink constant current I_2 at the bottom. Therefore, the current ($I_{R\text{-}bank}$) through the binary R-bank is the ratio between the differential input to the equivalent resistance of the R-bank. This main transconductor current $I_{R\text{-}bank}$ is amplified and copied to the outputs by M_{2P} and M_{2N}. On the other hand, when ϕ_2 is enabled, the main transconductor current $I_{R\text{-}bank}$ is nulled, and the DC offset and 1/f noise currents are sampled at the capacitors C_{4P} and C_{4N}, through the other local negative feedback, which consists of M_2, C_4, and M_4. This sampled noise is compensated using the secondary transconductor in M_{4P} and M_{4N} during ϕ_1.

Fig. 4-8 shows the block diagram of the CDS technique to analyze the DC offset and 1/f noise cancellation quantitatively. The input of the CDS transconductor is nulled, and there are equivalent input referred noise sources ($V_{1/f,N1}$ and $V_{1/f,N2}$) at each transconductor input. The timing diagram for the CDS operation is shown in the bottom

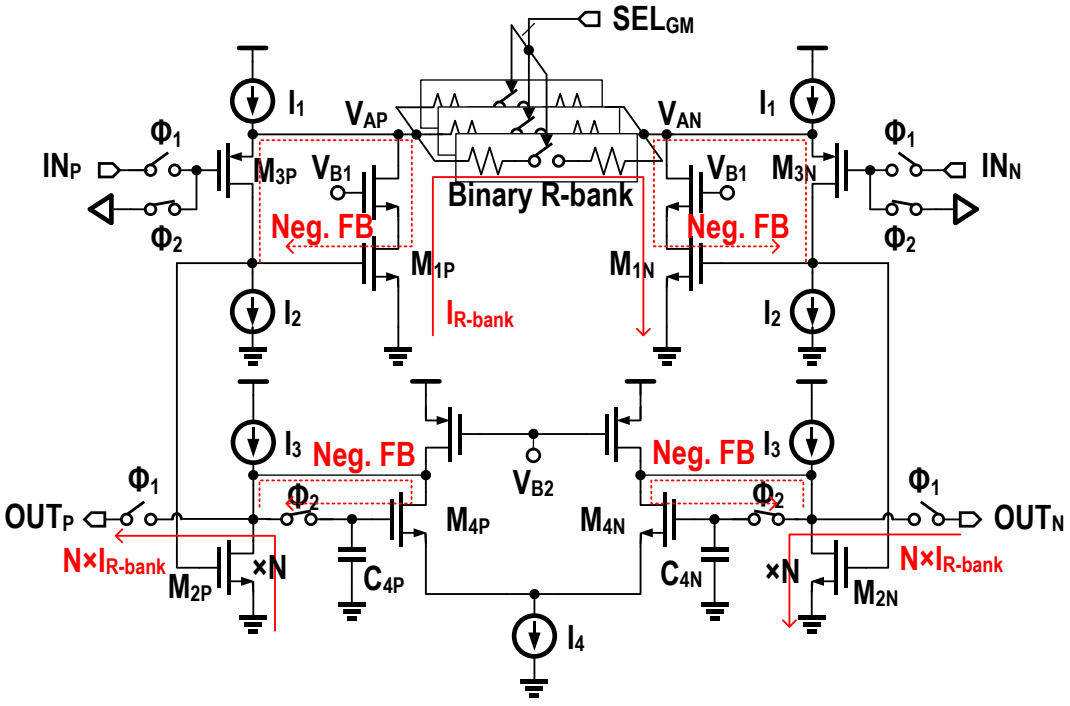


Figure 4-7: Schematic of the proposed CDS transconductor.

of the figure. During ϕ_2, the sampled voltage $V_{OUT}[n]$ is written as:

$$V_{OUT}[n] = \frac{G_{m2} \cdot R_{OUT}}{1 + G_{m4} \cdot R_{OUT}} \cdot V_{1/f,N1}[n] - \frac{G_{m4} \cdot R_{OUT}}{1 + G_{m4} \cdot R_{OUT}} \cdot V_{1/f,N2}[n] \quad (19)$$

During ϕ_1, the sampled output $V_{OUT}[n+1/2]$ is written as:

$$V_{OUT}[n+1/2] = G_{m2} \cdot R_{OUT} \cdot V_{1/f,N1}[n+1/2] - G_{m4} \cdot R_{OUT} \cdot \left(V_{1/f,N2}[n+1/2] + V_{OUT}[n] \right) \quad (20)$$

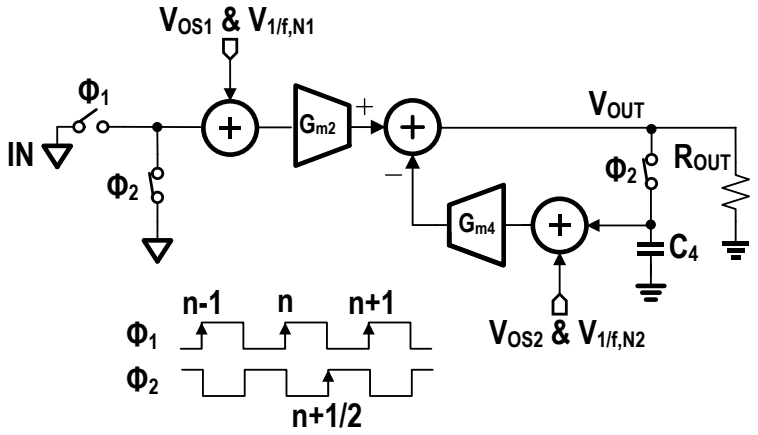


Figure 4-8: Block diagram of a CDS scheme with noise sources.

By plugging (19) into (20), and assuming the auxiliary loop gain is much larger than unity, the total equivalent input referred noise ($V_{IN,noise}(z)$) can be written as:

$$V_{IN,noise}(z) \cong (1 - z^{-1/2}) \cdot V_{1/f,N1}(z) - \frac{G_{m4}}{G_{m2}} \cdot (1 - z^{-1/2}) \cdot V_{1/f,N2}(z) \quad (21)$$

where the 1/f noise for both G_{m2} and G_{m4} are filtered by $(1-z^{-1/2})$. If G_{m2} is relatively larger than G_{m4}, additional 1/f noise contribution from G_{m4} can be negligible. On the other hand, the input referred DC offset due to the CDS scheme can be rewritten as:

$$V_{OS,IN} = \frac{V_{OS,1}}{1 + G_{m4} \cdot R_{OUT}} - \frac{G_{m4}}{G_{m2}} \cdot \frac{V_{OS,2}}{1 + G_{m4} \cdot R_{OUT}} \quad (22)$$

which reveals that both DC offsets are attenuated by the feedback loop gain $(1+G_{m4} \times R_{OUT})$. The further analysis for this CDS scheme can be found in [25].

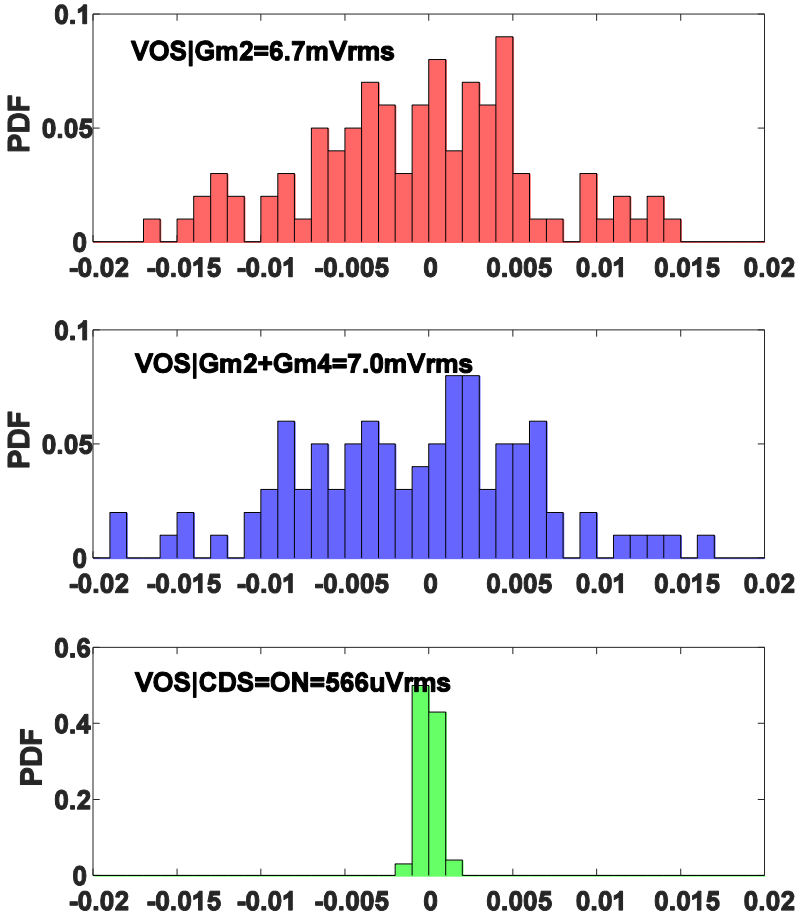


Figure 4-9: Monte-Carlo simulation results for the proposed CDS transconductor.

The input referred DC offset is extracted from 100 Monte-Carlo simulations, and Fig. 4-9 shows the simulation results. The main transconductor G_{m2} gives rise to $6.7mV_{rms}$ input referred DC offset, and the total input referred DC offset is $7.0mV_{rms}$. Due to the CDS scheme, the total input referred DC offset is reduced to $566\mu V_{rms}$, which is 12.4× smaller. In addition, the linearity of the proposed CDS transconductor (G_{m_NEG}) is simulated, and the results are plotted in Fig. 4-10. The second order distortion is dominant, and the maximum error is less than 1% with $0.8V_{P-P}$ input swing. The noise filtering due to the CDS technique are simulated, but will be discussed in chapter 5.

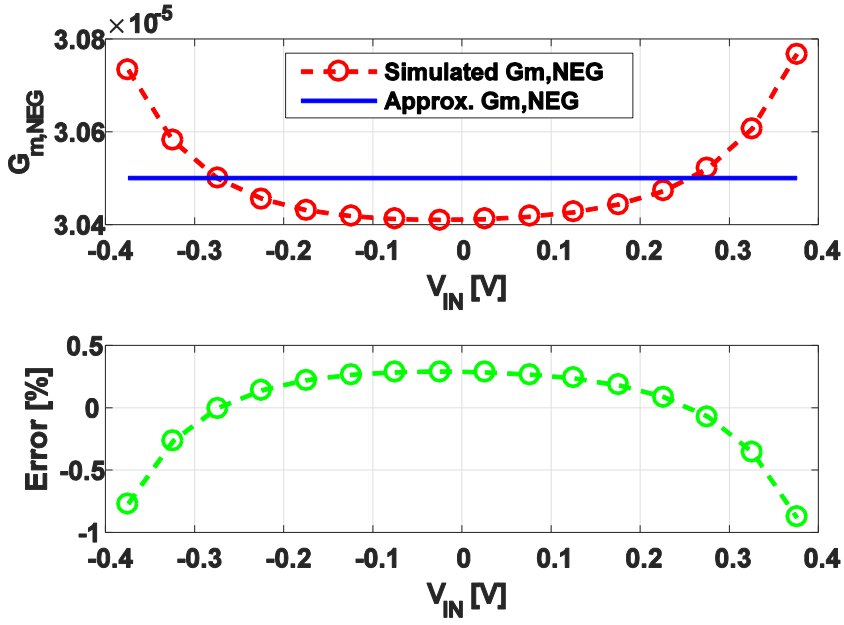


Figure 4-10: Simulated linearity error in the proposed CDS transconductor.

4.4 Voltage-to-Current Converter and VCO

Fig. 4-11 shows the block diagram of the voltage-to-current (V-to-I) converter and schematic of the VCO. The VCO consists of six pseudo-differential delay cells. The pseudo-differential delay cell has the NMOS differential input transistors ($M_{1\sim2}$), regenerative PMOS cross-coupled pair ($M_{3\sim4}$), two frequency control PMOS transistors ($M_{5\sim6}$), and the external frequency tunable PMOS transistor (M_7). There are two separate V-to-I converters for the proportional and integral control voltage (V_{PROP} and V_{INT}), and the implicit signal summation for V_{PROP} and V_{INT} is performed in current domain inside the delay cells. This is because the mirrored currents of M_5 and M_6 from the V-to-I converters are summed at V_{OUT}, and the total mirrored current controls the delay of the delay cell.

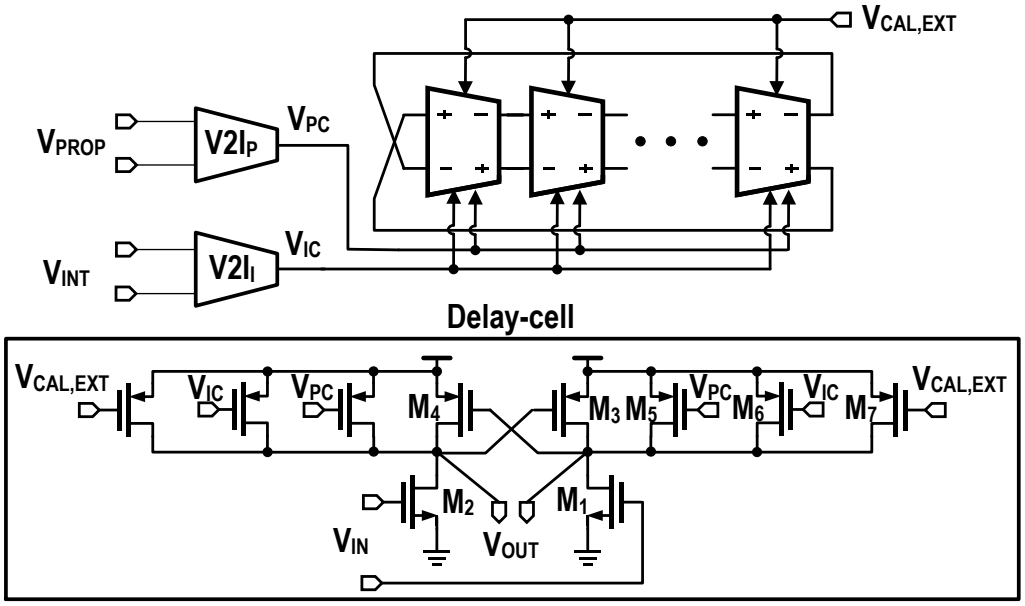


Figure 4-11: Block diagram of the voltage-to-current converter and VCO.

Fig. 4-12 shows the schematic of the V-to-I converter, which converts the differential voltage input to the single-ended output current. The topology of the proposed V-to-I converter is similar to the proposed transconductor in the proposed DT-LF without the CDS scheme. Due to the local negative feedback, the differential input voltage V_{IN} appeares at the binary R-bank, and this current is copied to the mirror PMOS current source M_5 and M_6 of the delay cell as shown in Fig. 4-11. Therefore, one can control the K_{VCO} by adjusting the equivalent resistance at the binary R-bank. Additional differential/common-mode capacitive filter network (C_1~C_4) is implemented to absorb the oscillating kickback noise from the delay cells. It is because the kickback noise from multiple rail-to-rail swing delay cells can be self-modulated and results in additional noise and spurs. This capacitors also helps to balance the differential-to-single-ended V-to-I converter, because any output loading mismatches will create noticeable even order distortions at the gain of the V-to-I converters. Finally, this capacitive filter network (C_1~C_4) pushes the output pole of the V-to-I converter into a lower frequency and provides another high frequency noise filtering.

In general, when the SSC modulation is not required, smaller K_{VCO} is preferred since any noise from the reference clock, PFD, CP, and loop filter will be amplified by K_{VCO}. Although it decreases the loop gain K_{LG}, one can use other design parameters (such as I_{CP} or R_1) to compensate this loop gain K_{LG} reduction. Therefore, K_{VCO} should be minimized to reduce not only the in-band noise gain from reference clock, PFD, CP and loop filter, but also the distortion of K_{VCO}. However, in the SSC modulation mode, the K_{VCO} needs to be large enough to support the required SSC modulation range Δf_{SSC_range}. In particular, the maximum required SSC modulation range Δf_{SSC_range} of this design is ±2.7% (± 27,000 ppm) of the output frequency, and this exceptionally demanding SSC modulation specification requires 380mV_{P-P} swing in the control voltage V_{CTRL} with 2π×50MHz/Volt K_{VCO} in 352MHz output frequency. Therefore, there is a trade-off between the K_{VCO} and SSC modulation range Δf_{SSC_range}.

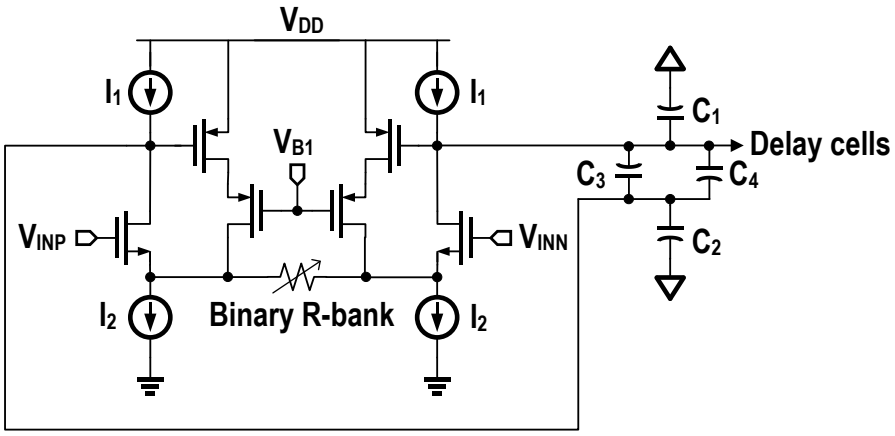


Figure 4-12: Schematic of the voltage-to-current converter.

Fig. 4-13 shows the K_{VCO} linearity simulation for the proposed V-to-I converter and VCO. Because of the demanding SSC modulation requirement, a larger swing at the control voltage (which is V_{IN} in Fig. 4-13) degrades the K_{VCO} linearity (or K_{VCO} error). In other words, for this wide SSC modulation requirement, it is inevitable to have a larger K_{VCO} nonlinearity error and larger in-band noise contribution from the reference, PFD,

charge pump, and loop filter. This indicates that jitter performances of a SSC modulation PLL is generally worse than the ones of a unmodulated PLL due to the K_{VCO} range limiation. Finally, the overall K_{VCO} distortion error is less than 1% from -0.2 to +0.2V input swing at V_{CTRL} from Fig. 4-13. However, the open-loop gain TF_{LG} of a PLL compensates not only PVT variations of the K_{VCO}, but also the distortion of the K_{VCO}. Therefore, the linearity of the K_{VCO} is not critical in the proposed in-loop-BW SSC modulation technique.

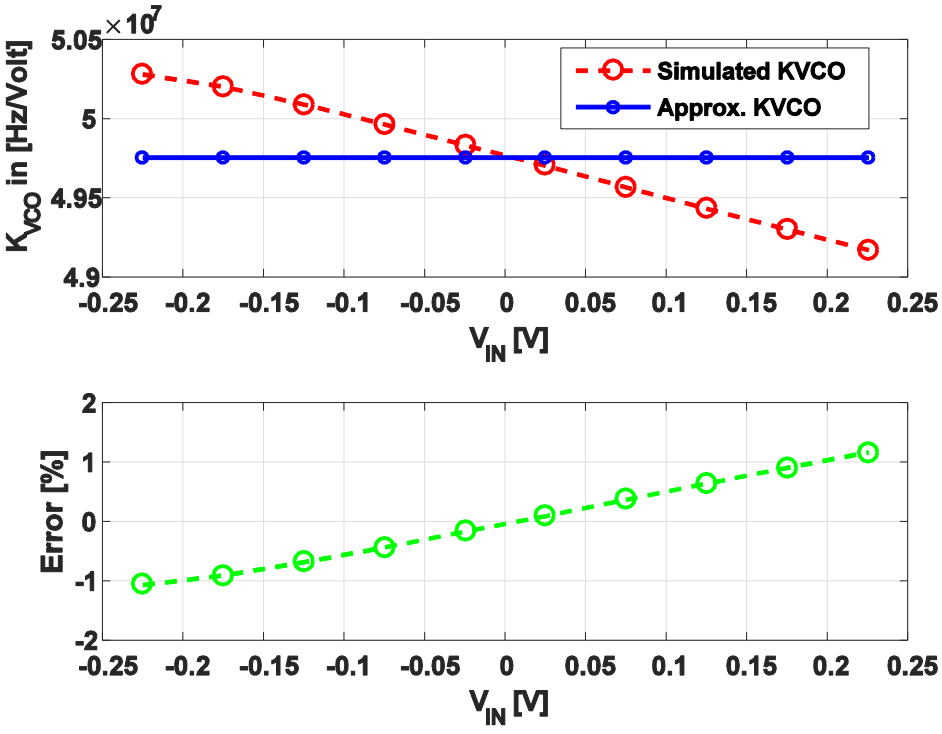


Figure 4-13: Simulated linearity in K_{VCO}.

4.5 SSC Current Digital-to-Analog Converter (I-DAC$_{SSC}$)

4.5.1 LSB of I-DAC$_{SSC}$

Since the design of the I-DAC$_{SSC}$ is strongly related to the SSC modulation gain,

the SSC modulation transfer function in (17) is rewritten here:

$$TF_{SSC}(z,s) \underset{DC}{\Rightarrow} \frac{I_{SSC,LSB}/2}{I_{CP}/M} \cdot f_{REF} \tag{17}$$

Assuming that the gain step of the FCW_{SSC} is f_{REF}, one needs to set $I_{SSC,LSB}/2$ to be equal to I_{CP}/M in (17). Since M is 352, the $I_{SSC,LSB}$ can be calculated as:

$$I_{SSC,LSB} = I_{CP} \cdot \frac{2}{M} = 50\mu A \cdot \frac{2}{352} = 284.1nA \tag{23}$$

4.5.2 FCW_{SSC} Resolution

In this work, maximum Δf_{SSC_range} is ±2.7% of 352MHz output frequency, which is equivalent to ±9.45MHz. In addition, from (17), the gain step for the FCW_{SSC} is f_{REF}, which is 1MHz. Therefore, the maximum $FCW_{SSC}[n]$ is ±9.45, which is smaller than ±10. The corresponding 2's complement of the maximum $FCW_{SSC}[n]$ is 01010_2 ($+10_{10}$) and 10110_2 (-10_{10}), which is 5-bit total including a sign bit. Therefore, 5-bit FCW_{SSC} is implemented in this work.

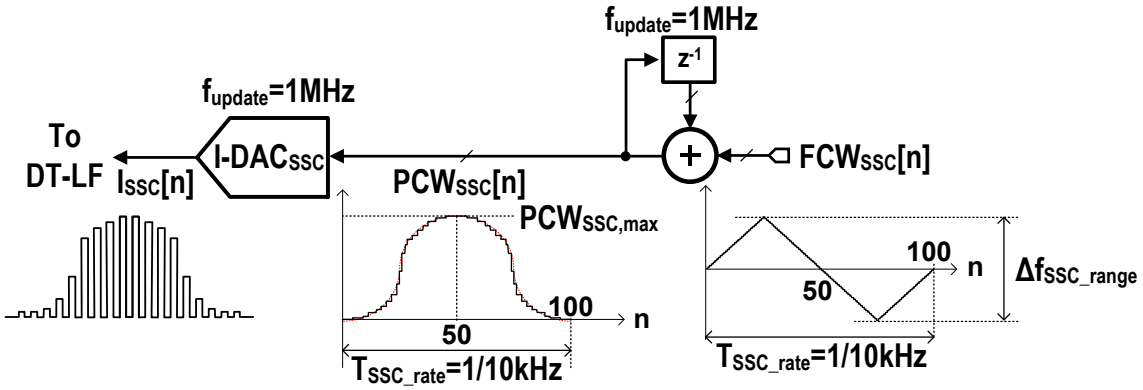


Figure 4-14: Operation diagram of the SSC modulation signal path.

4.5.3 $I\text{-}DAC_{SSC}$ Resolution

The dynamic range (or full scale range) of the $I\text{-}DAC_{SSC}$ is determined from the maximum PCW_{SSC} requirement. Fig. 4-14 shows the detail operations in FCW_{SSC} and

PCW_{SSC} at the SSC modulation signal path. The frequency SSC signal $FCW_{SSC}[n]$ is fed to the digital integrator, and the resulted phase SSC signal $PCW_{SSC}[n]$ drives the I-DAC_{SSC}. The maximum full scale of the I-DAC_{SSC} appears when the minimum SSC modulation rate f_{SSC_rate} (10kHz) and the maximum SSC modulation range Δf_{SSC_range} (±2.7%) are used as depicted in Fig. 4-14. This is because the maximum peak PCW_{SSC} ($PCW_{SSC,max}$) is proportional to both the integrating time duration (T_{SSC_rate}) and the magnitude of FCW_{SSC}, and the slowest modulation rate is 10kHz, and the maximum modulation range is ±2.7% in this work.

Since the update rate (=f_{REF}) is 1MHz, there are 100 sequential samples of the FCW_{SSC} for one period of the SSC modulation. The integrated PCW_{SSC} reaches up to the maximum when half of the samples are accumulated, which is 50th sample in the FCW_{SSC}. Therefore, the resolution for the I-DAC_{SSC} can be obtained by calculating the maximum peak $PCW_{SSC,max}$, which is written as:

$$PCW_{SSC,max} = \sum_{n=1}^{50} FCW_{SSC}[n] = 50 \times \frac{1}{2} \times FCW_{SSC,max} = 250 \Rightarrow 7.97 \text{ bit} \qquad (24)$$

Thus, the calculated maximum $PCW_{SSC,max}$ requires 8-bit of the I-DAC_{SSC}. The resulting full-scale current in the I-DAC_{SSC} is 71μA from (23) and (24).

From Fig. 4-14, since the I-DAC_{SSC} needs to supply only positive currents, it saves power and area in the design of the I-DAC_{SSC}. In addition, when the ratio between the $I_{SSC,LSB}$ and I_{CP} in (17) is kept as a constant, any scaling in I_{CP} results in a following current scaling in the I-DAC_{SSC}. Therefore, the SSC modulation range relies on the ratio of two current ($I_{SSC,LSB}/I_{CP}$), instead of the absolute current of I-DAC_{SSC}. This achieves a very power efficient SSC modulation, and the power penalty of the I-DAC_{SSC} is around 71μA with extra biasing current. This is less than 5% of the total power consumption.

4.5.4 I-DAC_{SSC} Implementation

An 8-bit segmented current steering DAC is implemented, where the thermometer MSBs and binary LSBs is 4-bit, respectively. The 4-bit thermometer DAC decoder design is from [37], and it has eight bias generators distributed around I-DAC_{SSC} current

cells.

Fig. 4-15 shows the schematic of the unit current cell driver, which consists of the R-S latch, and reset switch (M_1). The extra pull down NMOS (M_1) is added to reset the UP signal during a half of the clock period, because this is a 50% duty cycle return-to-zero (RZ) I-DAC_{SSC}. The extra delays with the copied NAND+buffer combination at the clock path makes the UP transition always aligned with respect to the clock edge. This edge alignment between the output UP signal and clock edge minimizes the signal-dependent pulse width modulation error. One can find more sophisticate drivers for higher speed current steering DACs in [38]-[39].

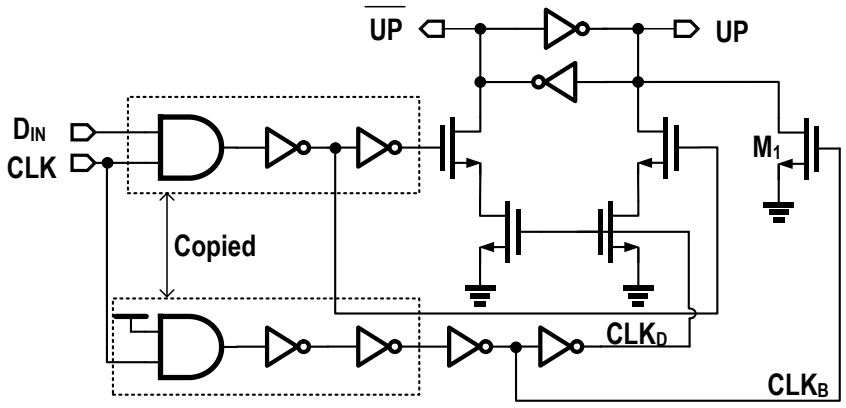


Figure 4-15: Schematic of the unit current cell driver in I-DAC_{SSC}.

The unit current cell is a scaled down version of the charge pump. The only difference is that the unit current cell has only UP current source. This is because the proposed SSC modulation pushes the phase modulation $\Delta\phi_{SSC}$ toward only positive side as shown in Fig. 4-14. Note that this single side SSC modulation scheme helps to get away from the dead-zone in the PFD+CP. This is because if the SSC modulation enables the charge inject for both sides, the offset delay $\Delta\tau_{OS}$ must be larger than the maximum SSC phase modulation range. Otherwise, the SSC modulation phase signal $\Delta\phi_{SSC}$ falls into the dead-zone in the middle of the SSC modulation and creates undesirable SSC modulation discontinuities.

4.5.5 I-DAC$_{SSC}$ Mismatch Analysis

There are multiple design considerations in the current steering I-DAC [40]: finite output resistance, matching errors, noise, slewing and settling errors, glitches, clock feedthrough, and etc. Particularly, the distortion due to the finite output resistance of the I-DAC$_{SSC}$ should be negligible based on the fact that the distortion in the charge pump is less than 0.5% as discussed in Fig. 4-5. Therefore, the static differential non-linearity (DNL) and integral non-linearity (INL) errors due to the unit current cell mismatches are examined to determine the number of bits for the MSB and LSB segments in the proposed I-DAC$_{SSC}$.

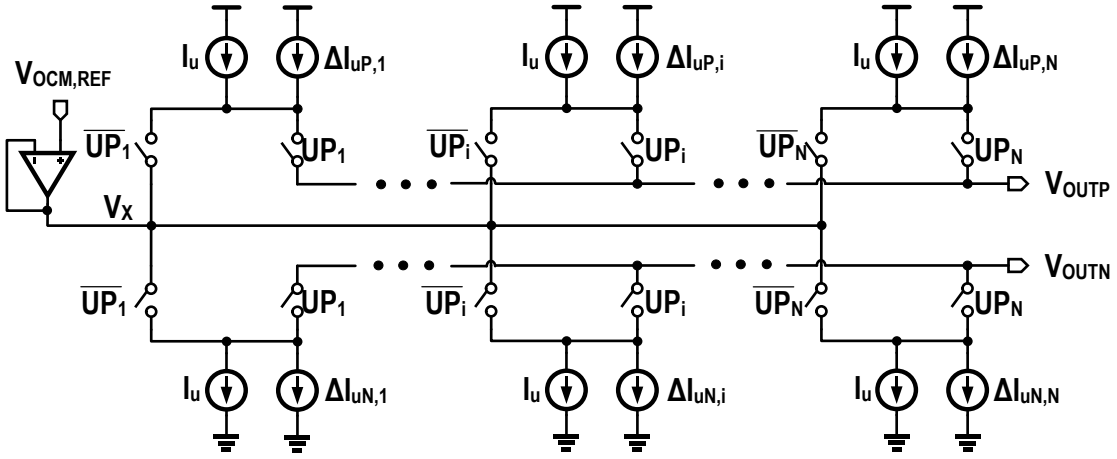


Figure 4-16: I-DACSSC schematic for the mismatch analysis.

As shown in Fig. 4-16, each PMOS-top/NMOS-bottom unit current source has an independently generated mismatch current ($\Delta i_{uP,i}$ and $\Delta i_{uN,i}$), and the standard deviation for net current mismatch of an i-th unit current cell ($\sigma_{\Delta iu,i}$) are equivalent to:

$$\sigma_{\Delta i_{u,i}} = \sqrt{\sigma_{\Delta i_{uN,i}}{}^2 + \sigma_{\Delta i_{uP,i}}{}^2} \tag{25}$$

where $\sigma_{\Delta iu,i}$ and $\sigma_{\Delta iu,i}$ are the standard derivation of $\Delta i_{uP,i}$ and $\Delta i_{uN,i}$, respectively. The DNL and INL in a charge-steering I-DAC due to the mismatches are well-studied in [40]-[41], and the results for a thermometer I-DAC are summarized here:

$$\sigma_{DNL}(k) = \sqrt{1-\frac{1}{N}} \cdot \sigma_{\Delta iu,i}$$
$$\sigma_{INL}(k) = \sqrt{\frac{k(N-k)}{N}} \cdot \sigma_{\Delta iu,i} \quad (26)$$

where N is the number of the total current cells, and k is the number of the enabled current cells.

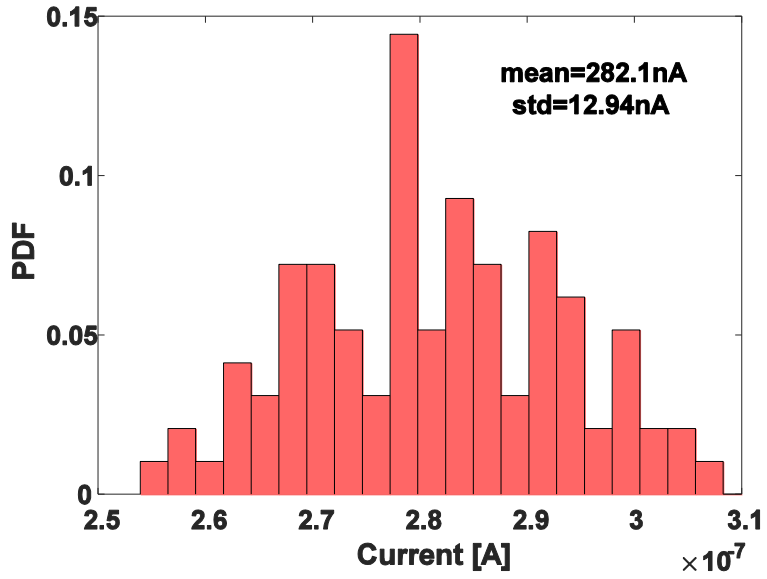


Figure 4-17:Monte-carlo simulation results for the unit current cell in I-DAC$_{SSC}$.

For a conventional thermometer current-steering I-DAC, from (26), the maximum standard deviation for the DNL and INL ($\sigma_{DNL,max}$ and $\sigma_{INL,max}$) is $\sigma_{\Delta iu,i}$ and $(\sqrt{N}/2)\times\sigma_{\Delta iu,I}$, respectively. On the other hand, for a conventional binary current-steering I-DAC, the maximum standard deviation for the DNL and INL ($\sigma_{DNL,max}$ and $\sigma_{INL,max}$) are $\sqrt{N}\times\sigma_{\Delta iu,i}$ and $(\sqrt{N}/2)\times\sigma_{\Delta iu,I}$, respectively. Therefore, the thermometer I-DAC significantly relaxes the DNL due to the mismatches, whereas both current-steering I-DAC topologies results in same INL due to the mismatches.

To determine the number of the LSB binary I-DAC$_{SSC}$, 100 Monte-Carlo

simulations for the unit current $I_{SSC,LSB}$ are performed, and Fig. 4-17 shows that the mean value $I_{SSC,LSB}$ is 282.1nA, and the standard deviation $\Delta i_{u,i}$ is 12.94nA$_{rms}$. In this design, the 4-bit LSB current steering I-DAC is used and this gives the maximum σ_{DNL} is $16\times\sigma_{\Delta iu,I}$, which is 207nA$_{rms}$. This is approximately 73% of the $I_{SSC,LSB}$. The maximum σ_{DNL} is relatively large since only 68.2% of samples are within 73% of the $I_{SSC,LSB}$, and it would be great for the $I_{SSC,LSB}$ to cover the $\pm3\times\sigma_{\Delta iu,I}$ of the maximum σ_{DNL} in the future work. In addition, the maximum σ_{INL} is calculated to 103.52nA$_{rms}$, and this is approximately 40% of the LSB current. Therefore, the number of bits for the binary LSBs in the I-DAC$_{SSC}$ is limited by the maximum σ_{DNL}.

4.6 Programmable Frequency Divider (FD)

The Vaucher's programmable frequency divider from [42] is implemented. An extra retiming D-FF is used to get rid of jitter associated from the frequency divider [43].

4.7 Clock Generator

The clock generator consists of a differential input clock driver, four quadrature phase generator, and non-overlapping phase generator. Since the off-chip ground and the internal clock ground have separated grounds, a fully-differential clock driver is implemented to reject the common-mode noise. Using a frequency divider, four quadrature half-rate phases are obtained, and the non-overlapping phase generator is implemented to generate the phases for the proposed DT-LF.

Chapter 5 – Jitter Analysis and Estimation

5.1 Definition of Random Jitter

In wireline communication systems, jitter performances are primary design specifications, and generally jitter can be categorized into deterministic jitter and random jitter. In this chapter, since we will mainly discuss about random jitter, definitions of this random jitter are necessary to discuss.

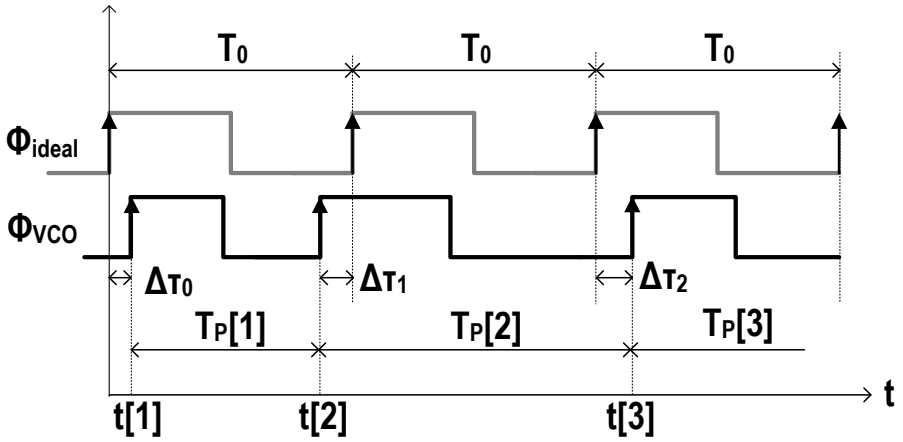


Figure 5-1: Clock edge diagrams to define the random jitter.

Fig. 5-1 shows clock diagrams to define the random jitter. There is the ideal clock (ϕ_{ideal}), which does not have any jitter, and this ideal clock edge is repeated in every T_0. In addition, the jittery clock edges (ϕ_{VCO}) of a VCO, which are notated to t[i], are shown in the bottom. By comparing this jitter clock edges ϕ_{VCO} to the ideal clock edges ϕ_{ideal}, one can define the absolute, period, and cycle-to-cycle jitters from the help of Fig. 5-1.

5.1.1 Absolute Jitter

The definition of the absolute jitter (J_{abs}) is the time difference between the ideal clean clock edge ($i \times T_0$) and the output clock edge t[i], and this can be written as:

$$J_{abs}[i] = i \cdot T_0 - t[i] = \Delta\tau[i] \tag{27}$$

The absolute jitter $J_{abs}[i]$ is equivalent to $\Delta t[i]$ in Fig. 5-1.

5.1.2 Period Jitter

The definition of the period jitter (J_{per}) is the time difference between the measured i-th period $T_P[i]$ and the ideal period T_0, and this can be written as:

$$J_{per}[i] = T_P[i] - T_0 = \Delta\tau[i] - \Delta\tau[i-1] = J_{abs}[i] - J_{abs}[i-1] \tag{28}$$

One can find that the period jitter $J_{per}[i]$ is the first-order difference of adjacent absolute jitters $J_{abs}[i]$. This implies that the accumulation of the period jitters $J_{per}[i]$ from i=0 to N is equivalent to the absolute jitter $J_{abs}[i=N]$. In addition, the average of the measured periods $T_P[i]$ for the jittery clock edges ϕ_{VCO} has to be exactly same to T_0. Otherwise, the absolute jitter J_{abs} becomes unbounded when the running time (t) goes infinite.

The definition of the N-period jitter ($J_{N\text{-}per}$) is the difference between the measured N-period ($T_P[i]+ T_P[i+1]+\ldots +T_P[i+N]$) and the ideal N-period ($N\times T_0$), and this can be written as:

$$J_{N-per}[i] = \Delta\tau[i+N] - \Delta\tau[i] = J_{abs}[i+N] - J_{abs}[i] \tag{29}$$

where the N-period jitter $J_{N\text{-}per}$ is equivalent to the first-order difference of the absolute jitter $J_{abs}[i]$ and $J_{abs}[i+N]$. When N=1, the N-period jitter $J_{N\text{-}per}$ is equivalent to the period jitter J_{per}, and when N goes to infinite, the N-period jitter $J_{N\text{-}per}$ should approach to $\sqrt{2}$ times of the absolute jitter J_{abs}.

5.1.3 Cycle-to-Cycle Jitter

The definition of the cycle-to-cycle jitter ($J_{C\text{-}C}$) is the time difference between two adjacent measured periods ($T_P[i]$ and $T_P[i\text{-}1]$), and this can be written as:

$$J_{CC}[i] = T_P[i] - T_P[i-1] = \Delta\tau[i] - 2\Delta\tau[i-1] + \Delta\tau[i-2] \tag{30}$$

Then, N cycle-to-cycle jitter ($J_{N,C\text{-}C}$) can be defined as the time difference between every N-cycle adjacent measured periods ($T_P[i]$ and $T_P[i\text{-}N]$).

5.1.4 Jitter Relationships

The jitter measurements are performed at every T_0, and they can be expressed in the sampled time error $\Delta t[i]$ (or absolute jitter J_{abs}). Therefore, one can find the relationships among the jitters from (28)-(30), which can be defined as z-domain transfer functions in terms of the absolute jitter $J_{abs}(z)$ [44]. The final relationships are summarized as:

$$\begin{aligned} J_{per}(z) &= (1-z^{-1}) \cdot J_{abs}(z) \\ J_{N-per}(z) &= (1-z^{-N}) \cdot J_{abs}(z) \\ J_{C-C}(z) &= (1-z^{-1})^2 \cdot J_{abs}(z) \end{aligned} \tag{31}$$

These relationships in (31) are very useful when one needs to calculate the jitters based on the phase noise measurements [45].

5.2 Phase Noise vs. Integrated Absolute Phase Jitter

Although jitter specifications are defined and measured in time-domain, it is important to understand their relationships to the phase noise (PN(f)), which is the spectral measurement. It is because transient noise simulation with sub-pico second accuracy is very tedious and time consuming. In addition, quick jitter calculations from the simulated closed-loop phase noise are very efficient and strong in design phases. The details of the derivations can be found in [45], and several valuable observations and conclusions are summarized in this section.

To investigate the relationship between the absolute jitter and the phase noise PN, Fig. 5-2 shows the sinusoid clock generator with a single-tone phase noise $\phi_n(t)$ at ω_n. The output voltage of the VCO is x(t), and it can be written as:

$$x(t) = A\cos(\omega_0 t + \phi_n(t)) \tag{32}$$

where $\phi n(t)=b\times\sin(\omega_n t)$, and ω_0 and ω_n are output oscillating frequency and the single-tone phase noise frequency, respectively. Assuming that the amplitude of $\phi n(t)$ is much smaller than 2π (which satisfies the narrow-band FM approximation condition), (32) can be rewritten as:

$$x(t) \cong A\cos(\omega_0 t) - \frac{Ab}{2}\cos((\omega_0 - \omega_n)t) - \frac{Ab}{2}\cos((\omega_0 + \omega_n)t) \tag{33}$$

This result reveals that there are two side tones at ($\omega_0 \pm \omega_n$) along with the fundamental tone at ω_0. The power spectral density ($S_x(\omega)$) of x(t) is shown in the bottom of the Fig. 5-2, and the phase noise ($PN(\omega_n)$) can be calculated as:

$$PN(\omega_n) = \frac{P_{sideband}}{P_{carrier}} = \frac{S_x(\omega_0 + \omega_n)}{S_x(\omega_0)} = \frac{A^2 b^2/8}{A^2/2} = \frac{b^2}{4} = \frac{1}{2}\cdot S_{\phi n}(\omega_n) \tag{34}$$

where $S_{\phi n}(\omega_n)$ is the phase PSD of $\phi_n(\omega_n)$. From (34), one can find the relationship between the phase noise $PN(\omega_n)$ and the phase PSD $S_{\phi n}(\omega_n)$ of $\phi_n(\omega_n)$. Note that phase noise $PN(\omega_n)$ is a relative magnitude (dBc) with respect to the carrier power $P_{carrier}$, and $S_{\phi n}(\omega_n)$ is also relative magnitude (dB) with respect to 2π since its unit is rad^2/Hz.

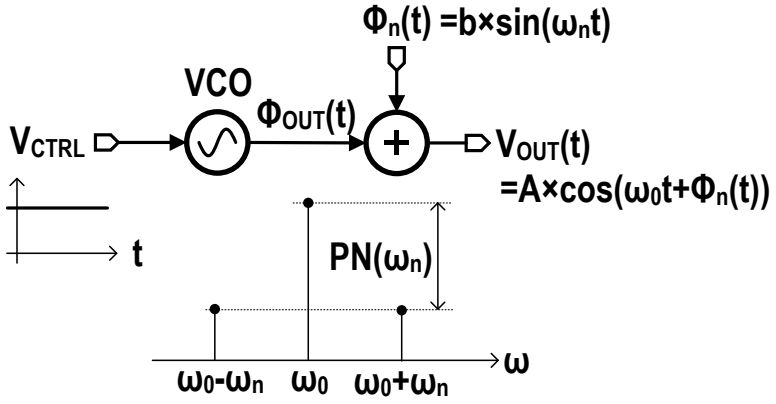


Figure 5-2: clock generator with phase noise.

From the Parseval's theorem, the integrating $S_{\phi n}(f)$ from f=0 to infinite in the spectral domain is equivalent to the variance $\sigma_{\phi n}^2$ of $\phi_n(n)$ in the time domain. Based on this theorem, one can derive the relationship between the rms integrated absolute phase jitter ($J_{\phi,abs}$) and phase noise PN(f), which can be written as:

$$
\begin{aligned}
J_{\phi,abs} &= \left(\frac{T_0}{2\pi}\right)\cdot\sigma_{\phi n} \\
&= \left(\frac{T_0}{2\pi}\right)\cdot\sqrt{\int_{-\infty}^{\infty} S_{\phi n}(f)df} \\
&= \left(\frac{T_0}{2\pi}\right)\cdot\sqrt{\int_{0}^{\infty} 2\times PN(f)df}
\end{aligned}
\tag{35}
$$

For example, if there is a spur at f_0+f_n and the spur phase noise $PN(f_n)$ is -40dBc, then the resulting rms integrating phase standard deviation $\sigma_{\Phi n}$ is $\sqrt{2}\times 0.01\%$ of 2π from (35). Thus, the rms integrated absolute phase jitter results in $\sqrt{2}\times 0.01\%$ of T_0.

5.3 Other Jitter Calculations from Phase Noise

From (35), one can calcualte the absolute phase jitter $J_{\phi,abs}$ from the spectral phase noise PN(f) measurement. What about the other jitters such as period, N-period, and cycle-to-cycle jitters? Interestingly, the z-domain relationships in (31) can be applied into (35), and the period phase jitter ($J_{\phi,per}$) , N-period phase jitter ($J_{\phi,N\text{-}per}$), and cycle-to-cycle phase jitter ($J_{\phi,C\text{-}C}$) can be obtained from the following equations:

$$J_{\phi,per} = \left(\frac{T_0}{2\pi}\right)\cdot\sqrt{\int_{-\infty}^{\infty}\left|1-e^{j2\pi fT_0}\right|^2 S_{\phi n}(f)df} = \left(\frac{T_0}{2\pi}\right)\cdot\sqrt{\int_{0}^{\infty} 2\cdot\left|\sin^2(\pi fT_0)\right|\cdot PN(f)df} \tag{36}$$

$$J_{\phi,N-per} = \left(\frac{T_0}{2\pi}\right)\cdot\sqrt{\int_{-\infty}^{\infty}\left|1-e^{j2\pi fNT_0}\right|^2 S_{\phi n}(f)df} = \left(\frac{T_0}{2\pi}\right)\cdot\sqrt{\int_{0}^{\infty} 2\cdot\left|\sin^2(\pi fNT_0)\right|\cdot PN(f)df} \tag{37}$$

$$J_{\phi,C-C} = \left(\frac{T_0}{2\pi}\right)\cdot\sqrt{\int_{-\infty}^{\infty}\left|1-e^{j2\pi fT_0}\right|^4 S_{\phi n}(f)df} = \left(\frac{T_0}{2\pi}\right)\cdot\sqrt{\int_{0}^{\infty} 2\cdot\left|\sin^4(\pi fT_0)\right|\cdot PN(f)df} \tag{38}$$

In this paper, if absolute, period, N-period, and cycle-to-cycle jitters are calculated from the closed-loop phase noise, we will call them as absolute *phase* jitter ($J_{\phi,abs}$), period *phase* jitter ($J_{\phi,per}$), N-period *phase* jitter ($J_{\phi,N\text{-}per}$), and cycle-to-cycle *phase* jitter ($J_{\phi,C\text{-}C}$) from here.

5.4 Simple Phase Noise Estimation for Targeted Absolute Jitter

At the beginning of PLL design, one needs to guess the target phase noise PN(f) for a VCO, since jitter contribution from a ring-based VCO is dominant in a clock generator. For a given target absolute jitter (J_{abs}), simple phase noise estimation will be discussed in this section.

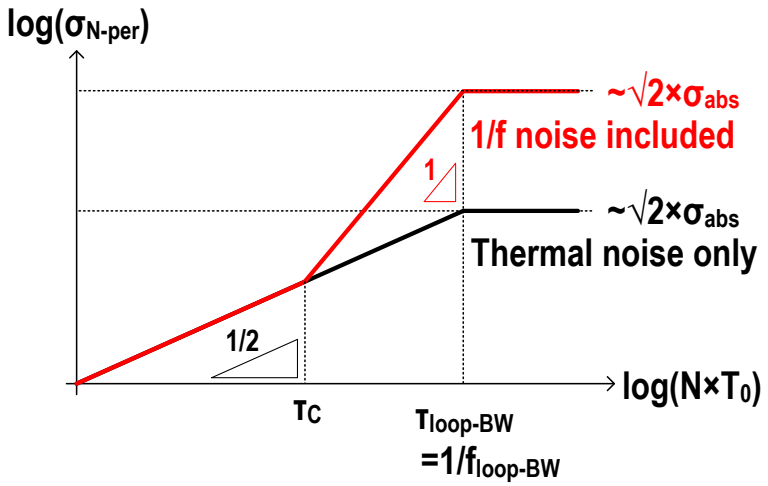


Figure 5-3: N-period jitter versus the number of period (N): simple phase noise model with the thermal noise, and with both the thermal noise and 1/f noise.

From a simplified phase noise model, which only takes into account the thermal noise, one can plug this simplified PN(f) model into (37) to obtain the N-period phase jitter, and this is resulted in:

$$J_{N-per}^{\ 2} = N \cdot \frac{\Delta f_{OS}^{\ 2}}{f_0^3} \cdot PN(\Delta f_{OS}) \qquad (39)$$

where Δf_{OS} is the offset frequency for a phase noise, and f_0 is the VCO output frequency. This result in (39) agrees with the one in [46]-[47]. When N goes to infinite, the N-period jitter $J_{N\text{-per}}$ should be unbounded in an open-loop VCO. However, for a closed-loop PLL, the N-period jitter $J_{N\text{-per}}$ should be bounded as √2-times of the absolute jitter J_{abs} when N goes to infinite as described in Fig. 5-3 [45], [48]. The N-period jitter $J_{N\text{-per}}$ should be

saturated when the time different $N\times T_0$ approaches the time constant of the loop BW ($\tau_{LBW}=1/f_{loop\text{-}BW}$). This is because the negative feedback loop in a PLL corrects the VCO phase noise components, which are slower than the loop BW. In other words, if N increases, slower phase noise gets involved into the N-period jitter, and this results in the increase in the N-period jitter $J_{N\text{-}per}$. However, when the N-period is greater than the time constant of the loop BW τ_{LBW}, there is no increase in N-period jitter $J_{N\text{-}per}$ because the phase noise, which is slower than the loop BW, should be eliminated by the loop and it does not contribute to the N-period jitter $J_{N\text{-}per}$.

Therefore, plugging the equivalent number of N for $N\times T_0=\tau_{LBW}$ into (39), the N-period phase jitter approaches to approximately $\sqrt{2}$ times of the absolute phase jitter, and it can be written as:

$$J_{\phi,N-per}(N=\tau_{LBW}/T_0)=\sqrt{\frac{1}{2\pi f_{LBW}}}\cdot\left(\frac{\Delta f_{OS}}{f_0}\right)\cdot 10^{PN(\Delta f_{OS})_{dBc}/20}\Rightarrow\sqrt{2}\times J_{\phi,abs} \tag{40}$$

This result agrees with the one in [49] except the factor of $\sqrt{2}$, and (40) can be rewritten for $PN(\Delta f_{OS})$ as:

$$PN(\Delta f_{OS})_{dBc}=20\times\log_{10}\left[\sqrt{2}\times J_{\phi,abs}\cdot\left(\frac{f_0}{\Delta f_{OS}}\right)\cdot\sqrt{2\pi f_{LBW}}\right] \tag{41}$$

Note that this is very rough phase noise estimation because it only takes into account the thermal noise of the VCO. More practical and accurate phase noise estimation can be found by including the 1/f noise contribution in the phase noise model in (40)-(41), and the authors in [50]-[51] analyzed or measured the N-period jitter including 1/f noise as shown in Fig. 5-3. Due to the 1/f noise of the VCO, the slope of the $\log(\sigma_{N\text{-}per})$ plot changes from 1/2 to 1 at the corner time constant (τ_C). Therefore, if the time constant of the loop BW τ_{LBW} is larger than the corner time constant τ_C, the absolute jitter J_{abs} increases by twice faster rate. One can find more details about the corner constant in [50]. In this work, -94.14 dBc of the phase noise at 1MHz of the offset frequency for 352MHz of the output frequency is estimated from (41) by achieving $50psec_{rms}$ absolute jitter from a VCO. Although this is very rough estimation, this provides valuable design insights

how to initialize the PLL specifications such as the loop BW and the phase noise PN for a given offset frequency.

5.5 Spectral Phase Jitter Estimations from the Hybrid-Domain Model

The phase jitter can be estimated from the hybrid-domain linear PLL model with proper noise sources obtained from noise simulations, and this phase jitter estimation is a strong and convenient tool for a PLL design. This is because although transient noise time domain jitter simulation should be a good final check, this is not efficient because one needs to run reiterative simulations to optimize jitter. In addition, this transient noise simulation does not provide valuable design insights.

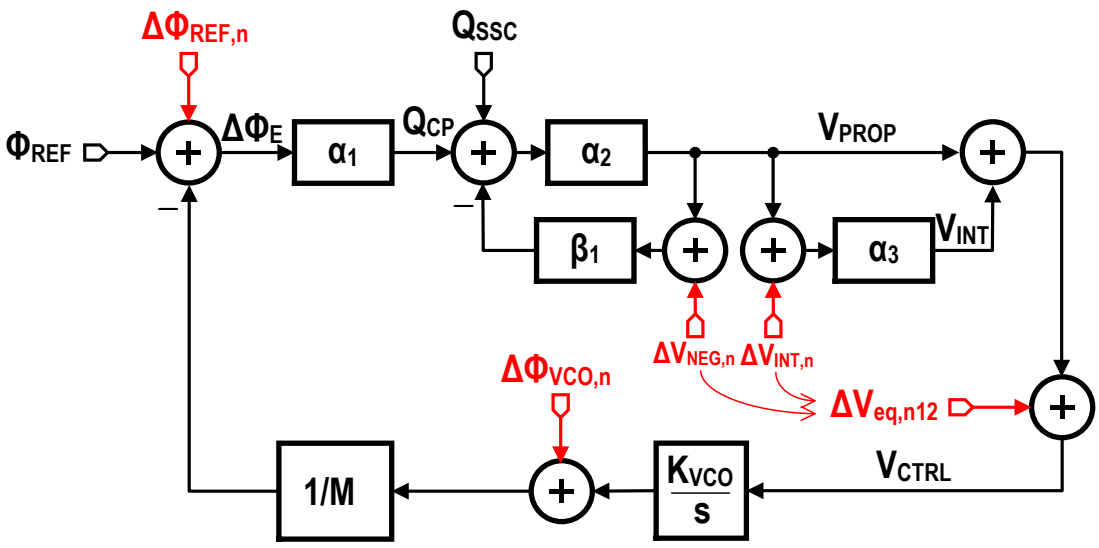


Figure 5-4: Hybrid-domain block diagram of the proposed architecture.

In this section, from the previously derived jitter relationships in (35)-(38) and a simulated closed-loop phase noise PN result, relevant phase jitter estimations will be discussed. The simulated closed-loop phase noise PN can be obtained from a linear PLL model in Fig. 3-5 and simulated source noise PSD results.

The linear transfer functions for the proposed SSC architecture are obtained in

chapter 3, and the results are summarized in (14)-(18). It is ueful to redraw the linear hybrid-domain model of the proposed architecture in Fig. 5-4, and rewrite the transfer functions as:

$$TF_{LG}(z,s)=\frac{T_{REF}}{2\pi}\cdot\frac{I_{CP}}{C_{12}}\cdot\frac{K_{VCO}}{s}\cdot\frac{1}{M}\cdot\left(\frac{z^{-1}}{1-z^{-1}}\right)\cdot\frac{1-\kappa_2 z^{-1}}{1-\kappa_1 z^{-1}} \tag{14}$$

$$TF_{1}(z,s)=\frac{\phi_{OUT}}{\phi_{REF}}=\frac{\frac{T_{REF}}{2\pi}\cdot\frac{I_{CP}}{C_{12}}\cdot\frac{K_{VCO}}{s}\cdot\left(\frac{z^{-1}}{1-z^{-1}}\right)\cdot\frac{1-\kappa_2 z^{-1}}{1-\kappa_1 z^{-1}}}{1+TF_{LG}(z,s)} \tag{15}$$

$$TF_{2}(z,s)=\frac{\phi_{OUT}}{\phi_{VCO}}=\frac{1}{1+TF_{LG}(z,s)} \tag{16}$$

$$TF_{SSC}(z,s)\underset{DC}{\Rightarrow}\frac{I_{SSC,LSB}/2}{I_{CP}/M}\cdot f_{REF} \tag{17}$$

$$K_{LG}=I_{CP}\cdot\frac{1}{G_{m\_NEG}/2}\cdot\frac{K_{VCO}}{2\pi}\cdot\frac{1}{M} \tag{18}$$

We have three major noise sources: VCO phase noise ($\phi_{VCO,N}$), LF noise from G_{m_NEG} ($V_{NEG,N}$) and G_{m_INT} ($V_{INT,N}$), and reference phase noise ($\phi_{REF,N}$). The final PSD of the equivalent closed-loop phase noise ($\phi_{OUT,N}$) can be obtained as:

$$S_{\Delta\phi_{OUT,N}}(f)=\left|TF_1(f)\right|^2 S_{\Delta\phi_{REF,N}}(f)+\left|TF_2(f)\right|^2 S_{\Delta\phi_{VCO,N}}(f)+\left|TF_2(f)\frac{K_{VCO}}{j2\pi f}\right|^2 S_{\Delta V_{CTRL,N}}(f) \tag{42}$$

where $S\phi_{VCO,N}(f)$, $S\phi_{REF,N}(f)$, and $S_{VCTRL,N}(f)$ are the power spectral density for $\phi_{VCO,N}$, $\phi_{REF,N}$, and equivalent $V_{CTRL,N}$ noise due to $V_{NEG,N}$ and $V_{INT,N}$, respectively. From Fig. 5-4, the input referred noise from G_{m_NEG} and G_{m_INT} is continuous noise in s-domain, whereas the V_{CTRL} equivalent noise is the sampled-noise. The linear model in either s- or z-domain cannot support the noise aliasing due to the sampling nature of the proposed DT-LF. Therefore, the equivalent total sampled noise $S_{VCTRL,N}(f)$ at V_{CTRL} is directly simulated from a periodic steady state simulation

5.5.1 Power Spectral Density of the Input Noise Sources

The simulated phase noise of the VCO is shown in Fig. 5-5. In addition, the phase noise spot measurements for a fabricated free-running VCO are plotted for comparisons. Both simulated phase noise and the spot measurements give close agreement with each other up to 2MHz. The spot measurements goes saturated at higher offset frequencies after 3~5MHz due to parasitic wideband noise sources, which could be from clock buffers, power supply noise, ground noise, and so on. The simulated phase noise underestimates the phase noise at higher offset frequencies, and this results in underestimated period and cycle-to-cycle jitter. In other words, wideband noise from clock buffers, power supply, and ground noise could become a critical role to determine the period and cycle-to-cycle jitters. We will revisit this point with real measurements in chapter 6.

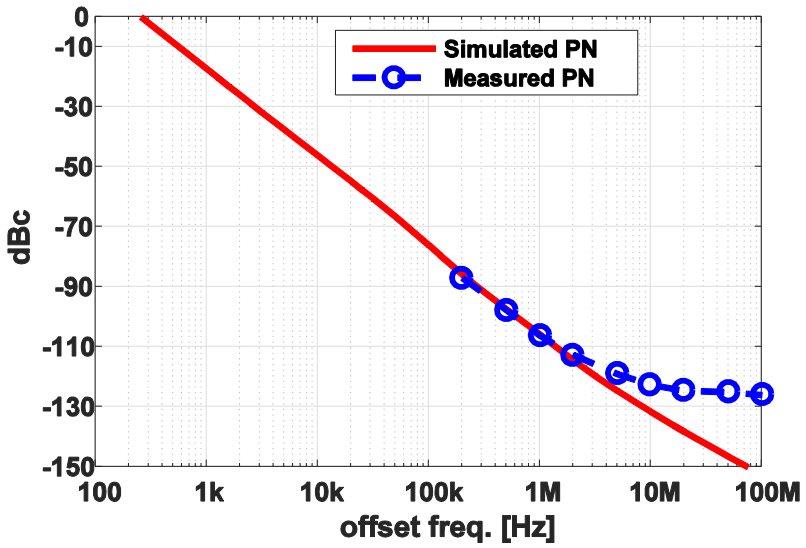


Figure 5-5: Phase noise simulation with open-loop spot measurements.

In this work, the measured and simulated phase noise PN(f_{OS}) is -108dBc at 1MHz of the offset frequency f_{OS}. This phase noise is approximately 14dB better than the estimation obtained from (41), and the calculated absolute phase jitter from (41) is

7.13ps$_{rms}$, whereas the simulated absolute phase jitter of the VCO from (42) is 37.0ps$_{rms}$. Thus, without including the 1/f noise in the phase noise model, the absolute jitter estimation in (41) is very rough and inaccurate.

From the noise analysis in the VCO, the major noise sources are from biasing circuitry for the V-to-I converters. Any 1/f noise from the biasing circuitry is amplified to the six delay cells. Therefore, a low pass noise filter for this 1/f noise is critical. In this design, an extra R-C noise filter is added, which has a triode PMOS transistor as a resistor.

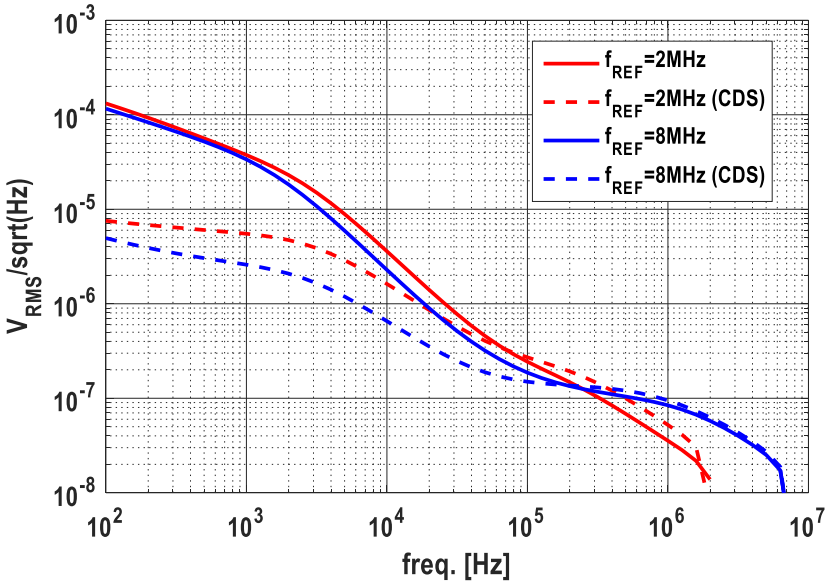
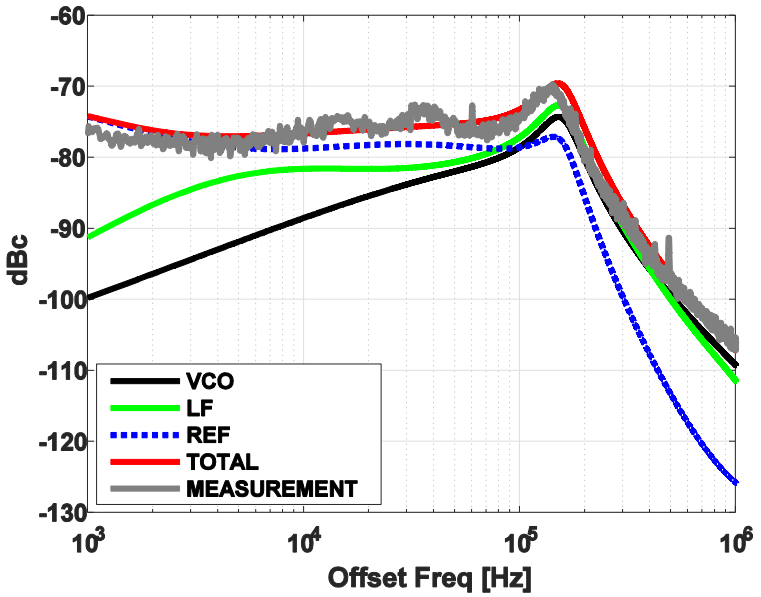


Figure 5-6: Sampled noise simulation of the proposed DT-LF.

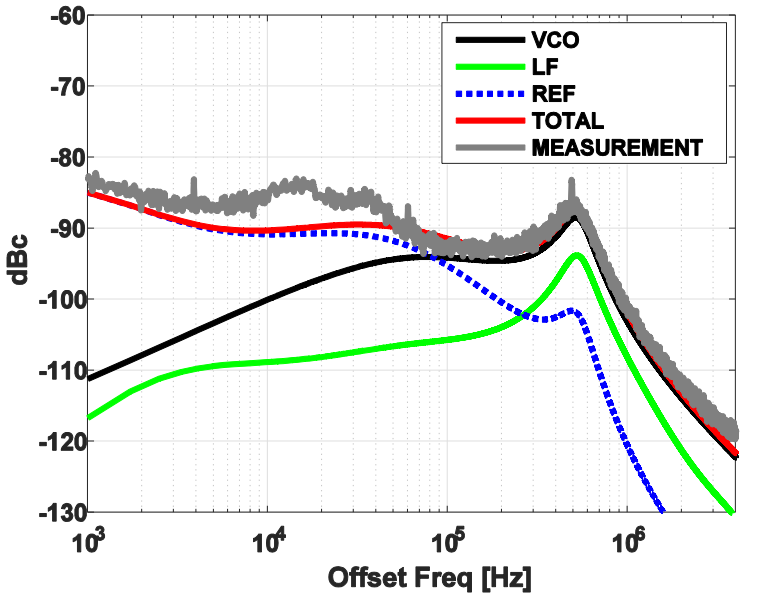
f_{REF}	CDS=OFF	CDS=ON	Unit
2MHz	3.06×10^{-3}	420×10^{-6}	V_{rms}
8MHz	2.05×10^{-3}	237×10^{-6}	V_{rms}

Table. 5-1: Total integrated sampled noise summary for the proposed DT-LF.

Fig. 5-6 shows the simulated sampled noise of the proposed DT-LF at the node V_{CTRL}. The solid lines show the sampled noise of the proposed DT-LF without the CDS scheme, which does not have the 1/f noise filtering. The dot lines show the sampled noise



(a)



(b)

Figure 5-7: Simulated and measured closed-loop phase noise plots for: (a) f_{REF}=2MHz, (b) f_{REF}=8MHz.

with the 1/f noise filtering from the CDS scheme. The update rates for 2MHz and 8MHz are used in the simulations to provide the relationship between the update rate and the 1/f noise filtering of the CDS scheme. The final integrated total rms noise for the proposed DT-LF is summarized in the Table.5-1.

From the CDS scheme, the 1/f noise from the proposed DT-LF is attenuated by more than an order of magnitude as shown in Fig. 5-6. In addition, the integrated total rms noise is improved by 87.3% and 88.4% for both reference frequencies. Therefore, the CDS scheme not only helps to reduce the DC offset, but also the 1/f noise (and total rms sampled noise) in the proposed DT-LF.

However, it is noted that the CDS scheme actually amplifies higher band noise. For example, in f_{REF}=2MHz, the cross over point between CDS=ON and CDS=OFF is around 70kHz, while the cross over point in f_{REF}=8MHz is around 200kHz. This cross over point determines that the CDS scheme is actually attenuating or increasing the noise, and any noise below the cross over point is attenuated, whereas noise above this point is amplified. Therefore, a higher cross over point is desirable to deliver a better noise attenuation in this CDS scheme. In other words, a higher update rate f_{REF}, which is equivalently a higher correlated double sampling rate, provides a superior noise cancellation due to a larger cross over point between CDS=ON and CDS=OFF.

5.5.2 Final Closed-Loop Output Phase Noise Calculation

By plugging the simulated VCO phase noise in Fig. 5-5, the proposed DT-LF sampled noise in Fig. 5-6, and the measured reference clock phase noise into (42), the final simulated closed-loop phase noise is calculated. Fig. 5-7 shows this calculated closed-loop output phase noise for f_{REF}=2MHz and 8MHz, respectively. The measured closed-loop phase noise from the implemented PLL is plotted for comparisons.

Interestingly, the proposed DT-LF phase noise contribution is larger than the one of the VCO in Fig. 5-7(a), whereas the VCO phase noise contribution is dominant in Fig. 5-7(b). This is because the 1/f noise attenuation from the CDS scheme in f_{REF}=2MHz is not sufficient, whereas a higher update rate f_{REF} delivers a better 1/f noise suppression

and the proposed DT-LF sampled noise becomes non-dominant.

Spectral cumulative jitter estimations for the absolute phase jitter $J_{\phi,absr}$ and period phase jitter $J_{\phi,per}$ are useful to inspect jitter characteristics, and the simulated spectral cumulative jitter estimations are shown in Fig. 5-8 and Fig. 5-9, respectively. From these figures, one can sort noise contributions for each noise sources. The jitter contributions from both the VCO and proposed DT-LF reveal the major jump around the loop BW, which is 100kHz in Fig. 5-8 and 800kHz in Fig. 5-9. As expected in Fig. 5-7(a) and confirmed in Fig. 5-8(a), the absolute phase jitter contribution from the proposed DT-LF is 44.5ps,rms, which is greater than 37.0ps,rms of the VCO. On the other hand, the

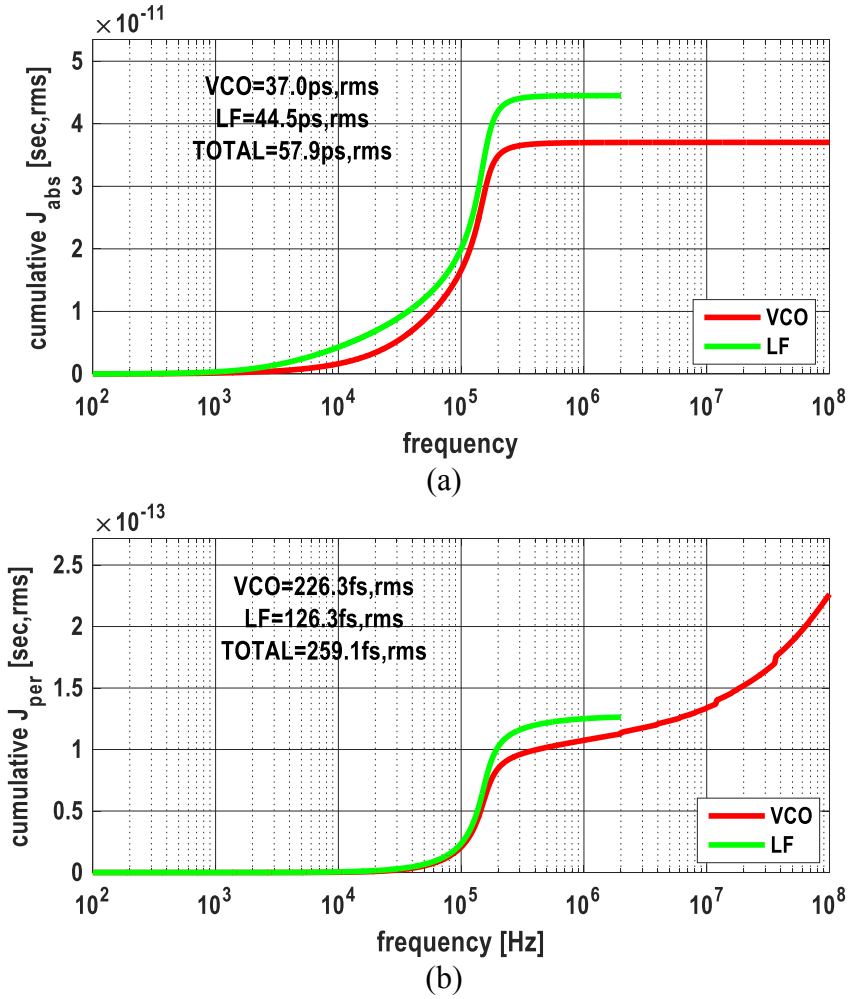


Figure 5-8: Simulated cumulative absolute and period phase jitter for f_{REF}=2MHz.

absolute phase jitter contribution from the proposed DT-LF is 6.34ps,rms in Fig. 5-9(a), which is less than 9.34ps,rms of the VCO.

For period phase jitter estimations, the jitter contribution from the VCO is dominant for both cases. This is because the accumulative period phase jitter reveals the continuous increase up to 100MHz from Fig. 5-8(b) and Fig. 5-9(b), indicating that the phase noise at a higher band becomes a significant factor to determine the period phase jitter.

As mentioned in Fig. 5-5, the simulated phase noise underestimates the higher band phase noise and results in very optimistic period phase jitter. The period phase jitter

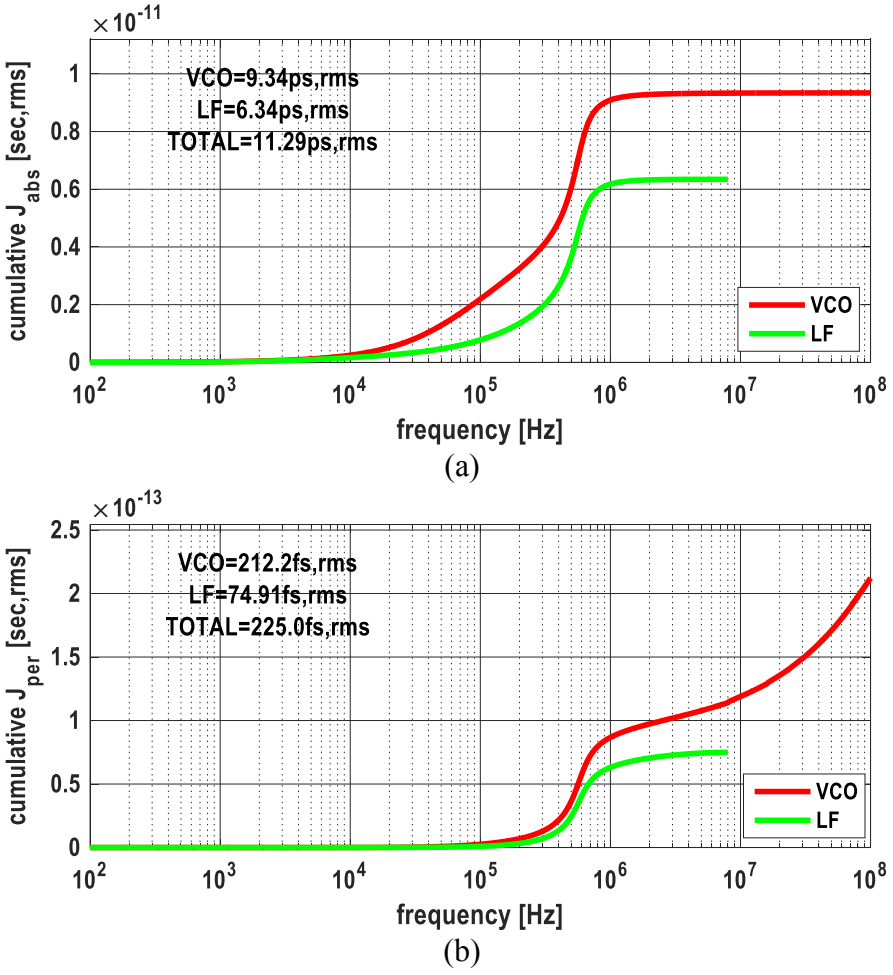


Figure 5-9: Simulated cumulative absolute and period phase jitter for f_{REF}=8MHz.

estimations in Fig. 5-8(b) and Fig. 5-9(b) are around 200~250fs_{rms}, whereas the measured period jitter are around 900fs_{rms}. Therefore, the period phase jitter estimations require an accurate PLL model, which is valid up to at least $f_{OUT}/2$, and accurate phase noise estimation of a VCO in higher offset frequency band. This demands a good model for wideband noise sources such as clock buffers, power and ground noises.

Chapter 6 – Measurement Results and Discussions

The prototype of the proposed SSC PLL is implemented in a 0.18μm CMOS process, and a microphotograph of this PLL is shown in Fig.6-1. The active area of the fabricated chip is 3.01mm^2.

6.1 Measurement Setups

Fig. 6-2 shows the overview of the measurement setups. The 64MHz input clock is fed into the chip from the arbitrary waveform generator, and this single-ended input clock source is converted into the differential clock using the balun. This differential clock source comes into the internal clock generator, and this internal clock generator generates the target update rate phases (1~8MHz). The final locked output clock from the VCO buffer is buffered by a CML differential internal buffer with a 50-ohm matched output loading. This differential output clock is converted into a single-ended through the balun for measurements.

The final output clock is measured in different instruments for different target measurements. The spectrum analyzer is used to measure the spectral characteristics such

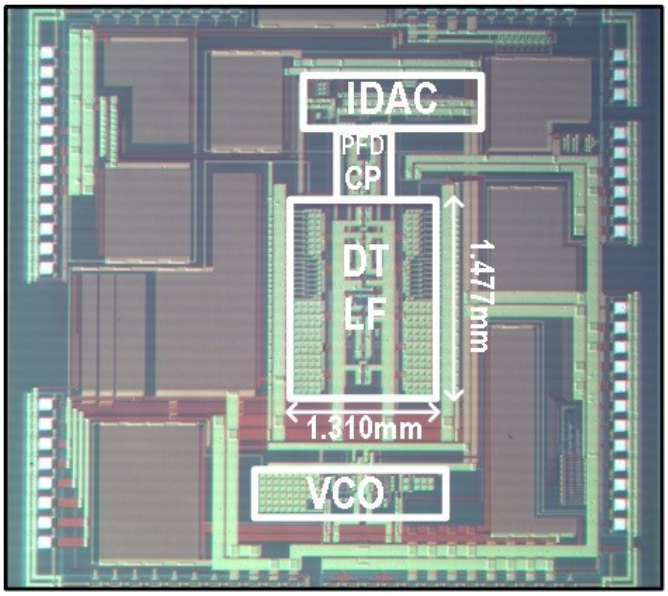


Figure 6-1: Die microphotograph.

as the phase noise and the SSC spectrum. The communication signal analyzer (CSA) and digital series analyzer (DSA) are used to measure the time-domain absolute and period jitter, respectively. The internal reference clock is pulled out to trigger the CSA for the absolute jitter measurements. For the SSC measurements, the pattern generator with the LVCMOS probe combination drives the internal 8-bit register for the I-DAC$_{SSC}$. The internal register bits (PCW$_{SSC}$), which is programmed from the pattern generator, are pulled out to off-chip and can be monitored using the logic analyzer (TLA). In order to synchronize the pattern generator with the update phase ϕ_{REF}, the reference clock signal ϕ_{REF} triggers both the pattern generator and logic analyzer.

6.2 Measurement Results in Spectral Domain

The closed-loop phase noise measurements for different reference frequencies are shown in Fig. 5-7(a) and Fig. 5-7(b), respectively. From (35), by integrating this closed loop phase noise, one can calculate the total rms integrated absolute phase jitter. Since the period and cycle-to-cycle phase jitters are first- and second-order differences of the absolute phase jitter from (36)~(38), the cumulative version of the absolute, period, and

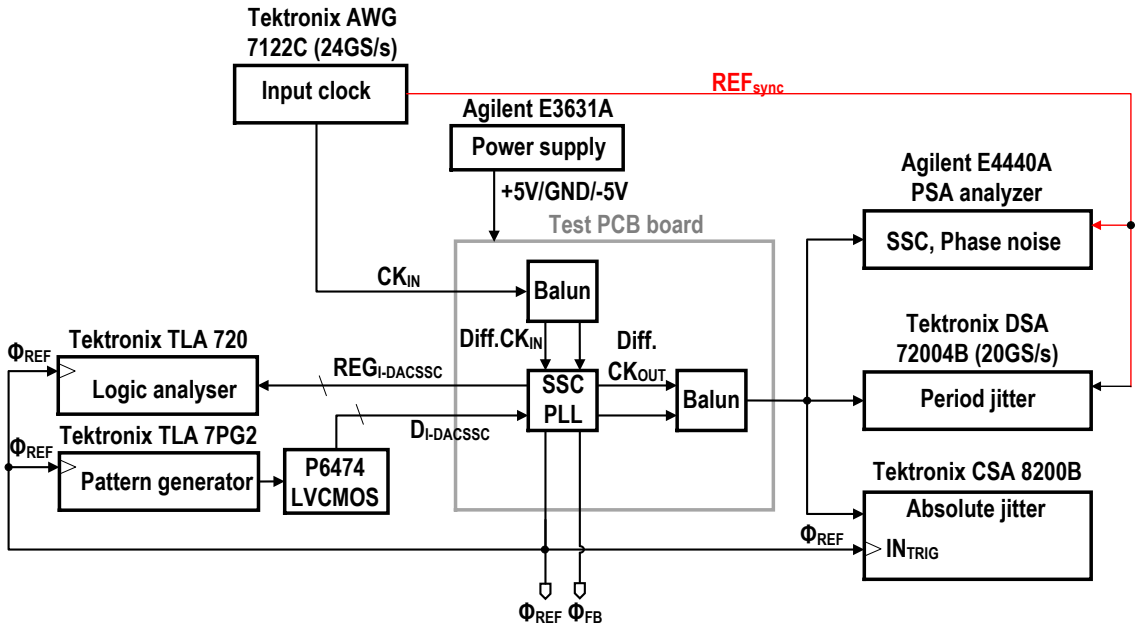


Figure 6-2: Test setups for the proposed SSC architecture.

cycle-to-cycle phase jitters is obtained as well.

The absolute, period, and cycle-to-cycle phase jitters from the closed-loop phase noise measurement are shown in Fig. 6-3. From the cumulative absolute phase jitter plot, the major increase of the cumulative absolute phase jitter indicates the position of the loop BW for two different reference frequencies. The calculated absolute phase jitter for f_{REF}=2MHz and 8MHz is 61.4ps$_{rms}$ and 18.7ps$_{rms}$, respectively, integrated the closed-loop phase noise measurement in Fig. 5-7.

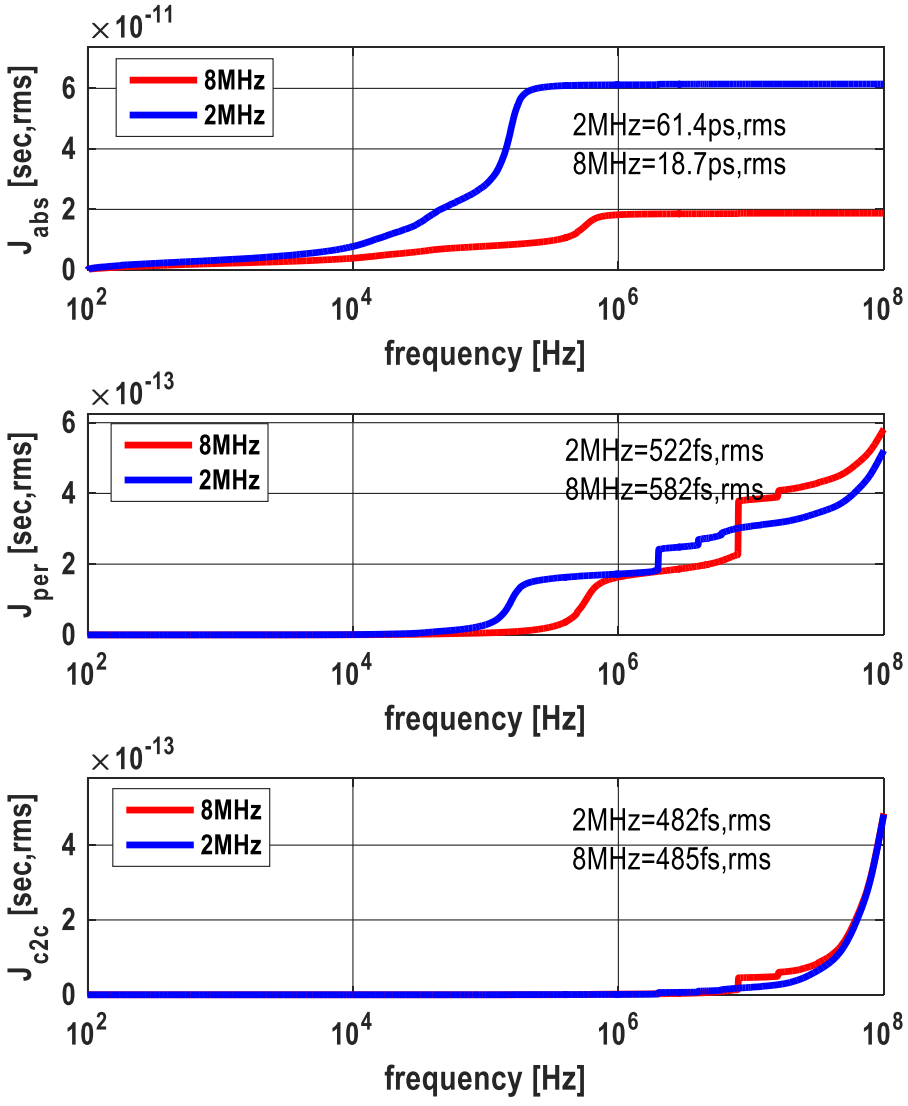


Figure 6-3: Cumulative absolute, period, and cycle-to-cycle phase jitter measurements

From the cumulative period phase jitter plot, the cumulative period phase jitter for 2MHz and 8MHz is $522fs_{rms}$ and $582fs_{rms}$, respectively. Whereas the cumulative absolute phase jitter does not increase when the offset frequency is above the update rate f_{REF}, the cumulative period jitter reveals the continuous ramping up to 100MHz. Therefore, it is critical to achieve both accurate noise sources and relevant PLL noise model in a higher offset frequency. The z-domain PLL model in Fig. 3-2 is not suitable for the period jitter calculation since this model is valid only up to $f_{REF}/2$. The hybrid-domain model in Fig. 3-5 is essential for the period and cycle-to-cycle phase jitter calculations.

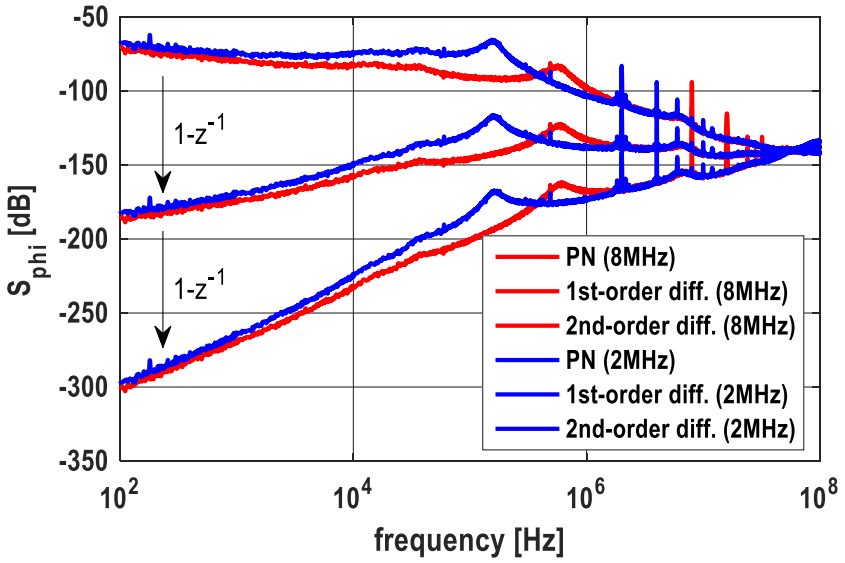


Figure 6-4: Measured closed-loop phase noise with a first- and second-order differences.

The frequency band to contribute major jitter increase in three cumulative phase jitter moves toward to a higher offset frequency in the period phase jitter calculation, and even higher in the cycle-to-cycle phase jitter. This is because low band phase noise is filtered out due to the first- or second-order difference from (31) or (36)-(38). The resulting shaped closed-loop phase noises are shown in Fig. 6-4. From the absolute phase jitter to the period phase jitter, the closed-loop phase noise has to be attenuated from the

first-order difference relationship from (31) and (36). Similarly, from the absolute phase jitter to the cycle-to-cycle phase jitter, the closed-loop phase noise is attenuated from the second-order difference relationship from (31) and (38). Therefore, the major phase noise contribution band in Fig. 6-4 keeps moving higher frequencies from the phase noise to the first-order difference of the phase niose, and from the first-order to the second-order difference of the phase noise. This tendency can be observed in Fig. 6-3.

Fig. 6-3 provides a good guideline for the closed-loop phase noise measurement. This is because if one needs to estimate the absolute jitter, the phase noise measurement up to the reference frequency should be sufficient, whereas one needs to measure the phase noise over 100MHz for the cycle-to-cycle phase jitter measurement. Therefore, the required measurement range for the phase noise (or the integration range for the phase noise) strongly relies on the target jitter type.

There are multiple discontinuities in the cumulative period and cycle-to-cycle phase jitters due to spurs in higher frequencies. Since the difference function $(1-z^{-1})$ pushes majority noise spot (or maximum noise gain spot) into higher and higher frequencies, spurs in higher frequencies, which should not be problematic in the absolute phase jitter, can create big jitter jumps in the period and cycle-to-cycle phase jitter calculations. In addition, the absolute number of the period phase jitter is around sub-pico second, whereas the absolute phase jitter is over $10ps_{rms}$ in this design. Therefore, the spurs in higher frequencies (>20MHz) cannot be negligible in the period and cycle-to-cycle phase jitter if the target period or cycle-to-cycle phase jitter is ranged below sub-pico second.

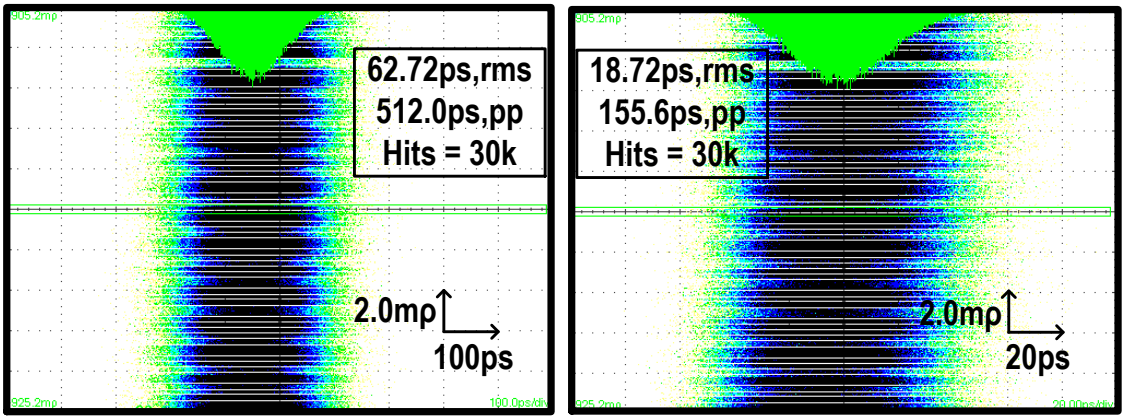
6.3 Measurement Results in Time Domain

The time-domain absolute and period jitters are measured, and the results are plotted in Fig. 6-5 and Fig. 6-6, respectively. The absolute jitter for the reference frequency of 2MHz and 8MHz is $62.72ps_{rms}$ ($512.0ps_{p-p}$) and $18.72ps_{rms}$ ($155.6ps_{p-p}$), respectively. The period jitter is $951.2fs_{rms}$ ($12.58ps_{p-p}$) and $988.1fs_{rms}$ ($8.485ps_{p-p}$),

respectively. The minimum period jitter without a DUT is around 650fs_{rms}. Therefore, the effective period jitters would be 694.5fs_{rms} at 2MHz and 744.2fs_{rms} at 8MHz.

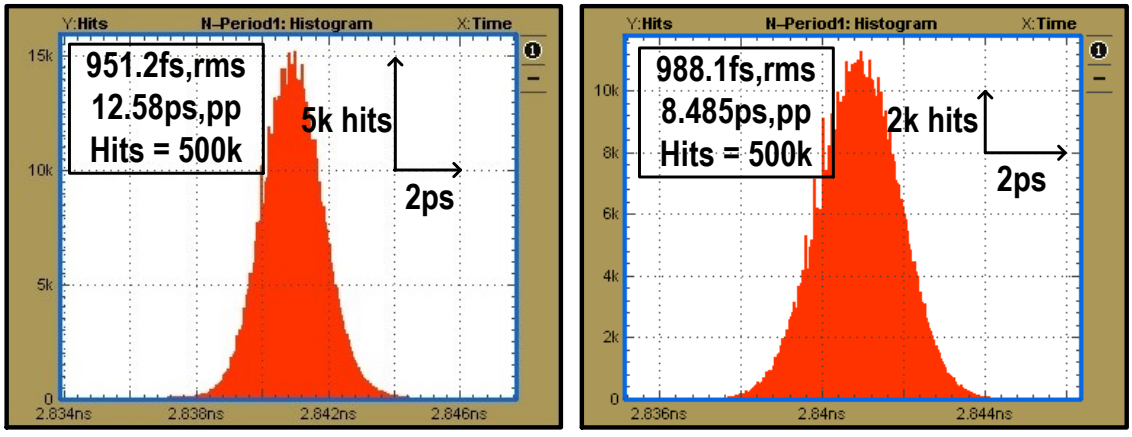
6.4 Comparisons for Spectral and Time Domain Measurements

From the spectral domain calculations in Fig. 6-3 and the time-domain measurements in Fig. 6-5 and Fig. 6-6, the spectral and time domain measurement results are compared and summarized in Table 6-1. The first column is the simulated estimations



(a) (b)

Figure 6-5: Time domain absolute jitter measurements for: (a) f_{REF}=2MHz and (b) f_{REF}=8MHz.



(a) (b)

Figure 6-6: Time domain period jitter measurements for: (a) f_{REF}=2MHz and (b) f_{REF}=8MHz.

from the simulated noise sources in the hybrid-domain PLL model, which was performed in chapter 5. The second column is the spectral phase jitter, which is calculated from the measured closed-loop phase noise, and the relationships from (35)-(38). The last column is the time domain measurements, which are directly measured from the CSA and DSA in Fig. 6-5 and Fig. 6-6.

Jitter type	**Unit**	**Estimation**		**Spectral**		**Time**	
		2MHz	**8MHz**	**2MHz**	**8MHz**	**2MHz**	**8MHz**
$\mathbf{J_{abs}}$	**rms**	57.9ps	11.3ps	61.43ps	18.74ps	62.72ps	18.72ps
	P-P	N/A	N/A	N/A	N/A	512.0ps	155.6ps
$\mathbf{J_{per}}$	**rms**	259.1fs	225.0fs	521.6fs	581.9fs	**694.5fs***	**744.2fs***
	P-P	N/A	N/A	N/A	N/A	12.58ps	8.49ps

*Net period jitter by taking out the baseline of the instrument.

Table 6-1: Summary and comparisons of jitter measurements.

The estimated phase jitters from the simulations are not quite accurate, but this method is sufficient to give quick estimations with 30~50% design margin. In addition, this method provides details of jitter contributions from each noise sources, which is very useful in optimization and debugging steps. The period phase jitter estimation is underestimated since the simulated VCO phase noise does not take into account the wideband noise source appropriately. On the other hand, the spectral phase jitter calculations are very accurate by comparing to the corresponding time domain results, and very convenient because a single closed-loop phase jitter measurement provides all different phase jitters, such as the period, N-period, cycle-to-cycle, and N cycle-to-cycle phase jitters. In addition, the spectral phase jitter calculation provides the cumulative phase jitter estimation as shown in Fig. 6-3, and this could be a good resource for jitter optimization. Particularly, if spurs degrade the period or cycle-to-cycle phase jitters, one can use this method to figure out how much spur attenuations are required to meet a target specification.

Finally, the measurements for the N-period jitter versus the number of N-period are performed in both the spectral and time domains, and the results are shown in Fig. 6-7. First, two different domain results confirm close agreement with each other. Second, the N-period jitter asymptotically approaches to $\sqrt{2}\times J_{abs,RMS}$ when N goes to infinite as mentioned in [45] and [48]. This verifies the assumption in (40). The slope for both cases are in-between ½ and 1, and the simple phase noise calculation in (40) and (41) should not be accurate in this work. In addition, the peaking in $J_{N\text{-}per}$ is observed due to under-damping response in the PLL for f_{REF}=2MHz.

6.5 Spread-Spectrum Measurements

Fig. 6-8 shows the measured spread-spectrum clock spectra with and without the SSC modulation for two different reference frequencies (2MHz and 8MHz). When the reference is 2MHz in Fig. 6-8(a), the maximum SSC modulation range is ±1.6%, and the

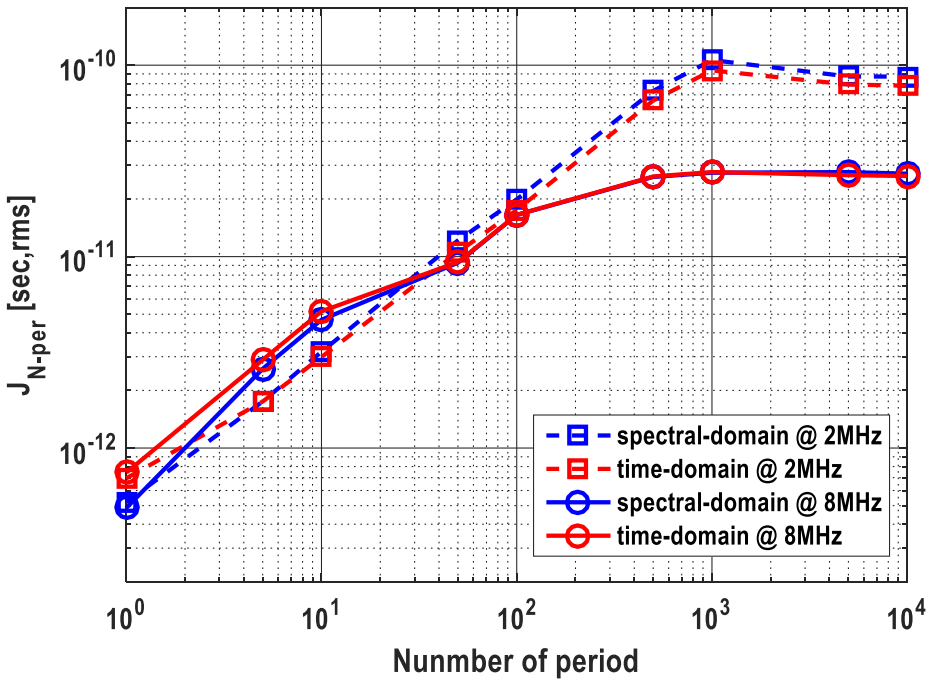
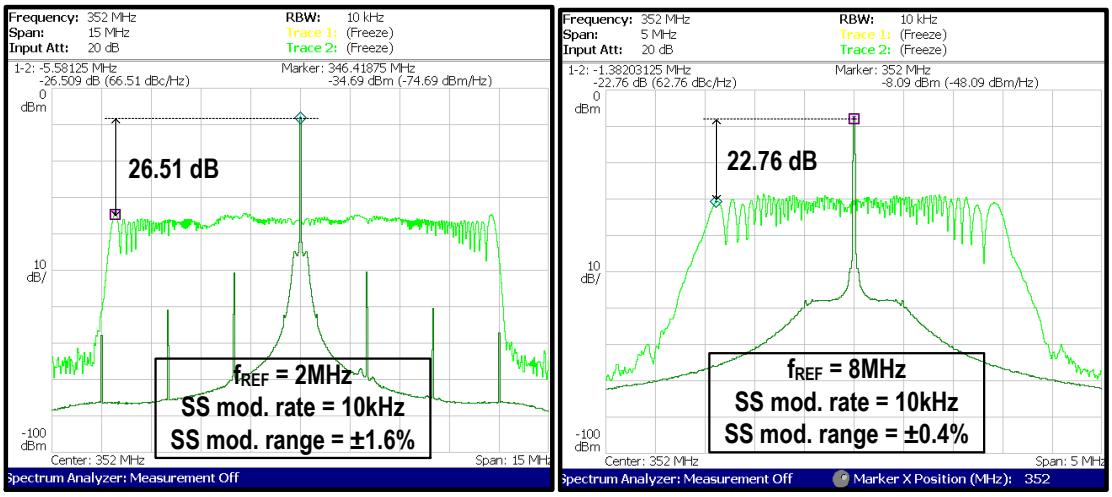


Figure 6-7: N-period jitter versus N from the spectral and time domain measurements for f_{REF}=2MHz and 8MHz.



(a) (b)

Figure 6-8: Measured SSC spectra with and without the SSC modulation.

SSC attenuation is 26.51dB. When the reference is 8MHz in Fig. 6-8(b), the maximum SSC modulation range and attenuation is ±0.4% and 22.76dB, respectively. Note that the SSC modulation rate for both reference frequencies is 10kHz, which is minimum, and the resolution bandwidth (RBW) is 10kHz for the measurements. Fig. 6-8 reveals the trade-off between the reference frequency and the SSC modulation range in (7) because as increasing the reference frequency by 4 times, the SSC modulation rate decreases by 4 times.

Fig. 6-9 demonstrates the PVT sensitivity measurement results for the SSC modulation. In 8MHz reference frequency with the desired ±4000ppm modulation range, a 142% change (from $2\pi\times13.4$ to $2\pi\times90.7$MHz/volt in $2\pi\times50$MHz/volt nominal K_{VCO}) in K_{VCO} results in less than 298ppm perturbations in the SSC modulation range. The K_{VCO} jump from $2\pi\times13.4$MHz/volt to $2\pi\times90.7$MHz/volt is extremely large since this jump results in 6.78× larger triangular waveform swing at the control voltage V_{CTRL} of the VCO. This large amplification at V_{CTRL} easily pushes the VCO into very non-linear region. However, the negative feedback enhances the distortion of K_{VCO} and results in very insensitive PVT variation.

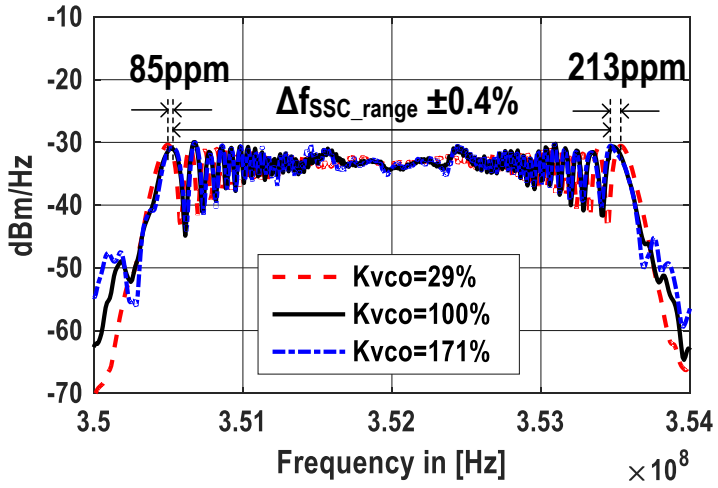


Figure 6-9: PVT sensitivity measurements for various K_{VCO}.

6.6 Summary and Comparisons

The summary of the measurements is shown in Table. 6-2. This proposed SSC architecture is based on an integer-N PLL structure. This SSC architecture establishes the in-loop-BW SSC modulation without a DSM, and the phase domain SSC modulation is built in an analog-domain without a TDC. Therefore, dithering noise from the DSM and quantization noise from the TDC can be avoided.

The jitter measurements are performed for two reference frequencies (2MHz to 8MHz). The higher reference frequency f_{REF} increases the loop BW and gives better jitter performances, whereas it reduces the SSC modulation range from 3.2% to 0.8%. The proposed SSC architecture was fabricated in a 0.18μm CMOS, and this PLL consumes 9.93mW total power, while operating from 1.8V power supply. The proposed charge-based DT-LF dissipates approximately 10% of the total power, and the power penalty due to the I-DAC_{SSC} is less than 5% of the total power.

Table 6-2 compares the results with the state-of-art PLLs which employ a ring-based VCO. The conventional frequency domain in-loop-BW SSC technique in [14] reveals less SSC EMI attenuation with the larger power consumption. This is because the wide SSC modulation requires a larger depth of the SSC modulation control word FCW_{SSC} for the DSM, which results in significant power consumption. In addition, there is a noise trade-off between the VCO phase noise and the in-band DSM dithering noise. The conventional phase domain in-loop-BW SSC technique in [18]-[19] result in worse jitter performances due to the quantization noise from a TDC or phase quantizer. Even for 65nm or 22nm CMOS technology, the wide and high accuracy TDC or phase

	This work		**Kokubo** [14]	**Grollitsch** [18]	**Li** [19]
Architecture	**Integer-N**		Fract.-N	AD-PLL	AD-PLL
Technology	**180nm**		150nm	65nm	22nm
f_{OUT} [GHz]	**0.352**		1.5	0.375~3.0	0.6~3.6
f_{REF} [MHz]	**2**	**8**	20~40	25	25~200
SSC Scheme	**In-LBW (DT LF)**		In-LBW (DSM)	In-LBW	In-LBW
f_{SSC_rate} [kHz]	**≥ 10**		≥ 31.3	≥ 33	≥ 25
Δf_{SSC_range} [%]	**3.2**	**0.8**	0.5	0.5	2
EMI Atten [dB]	**26.5**	**22.76**	20.3	NA	< 20
Jitter type	**Period**		250 cycle	Period	N-cycle
$Psec_{rms}$	**0.951**	**0.988**	8.1	8.16	10.0
$Psec_{p-p}$	**12.6**	**8.49**	NA	75	NA
Supply [V]	**1.8**		1.5	1.1	1.0
Power [mW]	**9.93**		54	2.92 (375MHz)	18.4 (3.6GHz)
Area [mm^2]	**3.01**		0.42	0.38	0.29

Table 6-2: Summary and comparisons of the proposed SSC architecture.

quantizer is not trivial, and it tends to be very power hungry. However, thanks to the proposed DT-LF, operating at an order of magnitude lower f_{REF}, the proposed architecture achieves an order of magnitude lower period jitter performance, without increasing the power consumption. This work achieves a 3.2% SSC modulation range with 26.5dB SSC attenuation using the 8-bit I-DAC_{SSC}, whereas the work in [19] requires a 24-bit FCW_{SSC} to deliver a 2% SSC modulation range with less than 20dB attenuation.

The PVT sensitivity is a critical specification for practical applications. The out-of-loop-BW SSC modulation scheme is very susceptible to the PVT variations of K_{VCO}. This is because the SSC modulation signal directly modulates the VCO. However, the in-loop-BW SSC modulation scheme generally provides a good PVT insensitivity due to the negative feedback in a PLL, and this negative feedback loop gain compensates the PVT variations of a VCO. Therefore, similar to other three state-of-art PLLs in [14],[18], and [19], the proposed SSC architecture confirms excellent PVT insensitivity for the proposed DT-LF and the VCO.

Chapter 7 – Conclusions

In this dissertation, the new phase domain in-loop-BW SSC generation technique was demonstrated. This is because the conventional out-of-loop-BW technique results in prohibitively large loop filter and unacceptable large power consumption in the VCO due to the narrow loop BW. The conventional frequency domain in-loop-BW SSC technique with a DSM does not allow to maximize the loop BW to suppress more phase noise from a ring-based VCO. This is because of the noise trade-off between the VCO phase noise and the in-band DSM noise. The conventional phase domain in-loop-BW SSC technique with a TDC suffers from inevitable quantization noise from the TDC and DCO.

The new charge-domain DT-LF was proposed to achieve the wide and PVT-tolerant SSC modulation. The proposed DT-LF acquires the charge domain signals from the PFD and I-DAC_{SSC}, and filter them into the control voltage V_{CTRL}. This charge-domain acquisition and filtering in the proposed DT-LF provides the excellent linearity to enable wide phase SSC modulation range. In addition, PVT variations from the proposed DT-LF and VCO can be significantly attenuated by the loop gain, which indicates that the nonlinear of K_{VCO} also can be significantly improved from the negative feedback loop gain. The measurement result in this work reveals 3.2% SSC modulation range, 10kHz SSC modulation rate for 2MHz reference frequency. The PVT sensitivity measurements reveal that 298ppm SSC modulation range error due to 142% K_{VCO} variations. It is noted that the out-of-loop-BW and two-point SSC modulation techniques are still susceptible to PVT variations in the VCO, and this proposed SSC modulation technique provides superior PVT insensitivity compared to them. Finally, the CDS scheme is utilized into the proposed DT-LF. The CDS scheme improves more than 14× offset reduction and 11.5× sampled noise reduction.

Two trade-offs are confirmed from the measurement results. The SSC modulation range is inversely proportional to the reference frequency since larger SSC modulation range requires larger phase acquisition range in the PFD, which results in a slower update

rate f_{REF}. This trade-off impacts the jitter performances because a lower f_{REF} indirectly leads to a lower loop BW, and results in larger phase noise from a VCO. In f_{REF}=2MHz, 3.2% SSC modulation range with 62.72ps_{rms} absolute jitter, whereas 0.8% SSC modulation range with 18.72ps_{rms} absolute jitter in f_{REF}=8MHz.

One drawback of this SSC modulation, or any phase-domain in-loop-bandwidth SSC modulation technique, is the finite range of the phase SSC modulation. Therefore, future work must support unlimited phase SSC modulation and decouple the trade-off between the reference frequency and the SSC modulation range. This could maximize the loop BW to save the power consumption of a VCO, and give unbounded SSC modulation range simultaneously. In fact, if one can obtain the infinite SSC modulation based on this proposed SSC modulation architecture, this proposed technique would be utilized as a fractional-N synthesis without a DSM and TDC.

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