

AN ABSTRACT OF THE THESIS OF

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Title VARIABLE-WIDTH PULSE GENERATION USING  
AVALANCHE TRANSISTORS

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The extremely fast ionization process in semiconductors offers a means of generating pulses that have sub-nanosecond rise times and high peak powers. There are several important applications of these pulses which require the duration of the generated pulse to be variable.

This thesis investigates three methods of producing variable-width pulses using transistors operating in the avalanche mode. The first circuit studied is used with a capacitor as the collector load. It produces pulse rise times of less than one nanosecond but has the disadvantage of a relatively slow RC discharge fall time. Distributed and lumped parameter delay lines were used in the second form of circuits studied. With the artificial delay line the pulse width can be controlled by opening the line at different sections whereas with the cable, the length must be altered to change the pulse width. These circuits produced fast rise, flat top, and fast

fall pulses.

In the third method studied, a composite circuit is used in which the fast rise of an avalanche pulse is added to a slower rise, but variable duration pulse, generated by a saturating transistor. This method is shown to produce fast rise, variable-width pulses with overshoot and ringing easily held to less than five percent.

VARIABLE-WIDTH PULSE GENERATION USING  
AVALANCHE TRANSISTORS

by

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# VARIABLE-WIDTH PULSE GENERATION USING AVALANCHE TRANSISTORS

## INTRODUCTION

Many circuit applications require the generation of fast rising variable-width pulses. Such applications include computer circuitry, nuclear instrumentation, sampling oscillography, and the use as test pulses in the evaluation of high speed circuits. Typically, rise times of the order of a few nanoseconds or even fractional nanoseconds are requirements. Pulsed power requirements may vary from milliwatts as in fast low-level computer logic circuits to tens of watts in computer memory applications.

Avalanche multiplication in semiconductor devices offers one method of generating high-current fast rise pulses. The avalanche mode of operation of transistors has been used to generate pulses for use in sampling oscilloscopes<sup>(10, p. 79)</sup>, in a decade ring counter<sup>(6, p. 262)</sup>, and as drivers in computer memories<sup>(7)</sup>.

## AVALANCHE PULSE GENERATORS

The generation of variable-width fast rise pulses may be accomplished in a number of ways. It is the purpose of this thesis to present a limited study of three such ways using normal diffusion transistors operated in the avalanche region. Circuit objectives are fast rise times, flat top pulses, fast fall times, and the convenience of

controlling the width of the pulse.

The pulse width, in the first circuit described, is controlled by the lumped capacitance in the collector load. In the second type of circuit the collector load is a transmission line, either distributed or lumped parameters, and in the third type of variable-width pulse generator, a composite circuit utilizing both a saturating transistor switch and an avalanche transistor is used.

## RESULTS

Of the three general types of circuits studied, each has its advantages and disadvantages in generating rectangular pulses whose width is conveniently controlled. The pulse width of the lumped capacitor circuit is changed merely by varying the value of the capacitor. This circuit produces very fast rise times, but the fall time is regulated by the capacitor controlling the pulse width and the load resistance. Consequently this method is best utilized in applications where the rise time and pulse width are the important design objects and the pulse fall time is of second order interest. A typical example of such an application is in generating trigger or clock pulses.

Fast rise and fall time pulses with flat tops are easily generated using transmission line collector loads. The pulse length is simply twice

the propagation time of the transmission line. This creates the need for changing the length of the line each time a different pulse length is needed. One solution to this disadvantage that was investigated was the use of a lumped constant delay line. Using this method the pulse width could be controlled by adding or taking out sections of the line. This is easily achieved using simple slide switches.

The third method investigated was a composite saturating transistor switch and an avalanche transistor pulse generator. The rise time of the avalanche generator is added to the pulse generated by the saturating transistor. This provides a pulse whose width is easily controlled and yet retains the fast rise time provided by the avalanche transistor.

### AVALANCHE BREAKDOWN

Normal operation of alloy and diffusion transistors rely on the physical processes of drift, diffusion, recombination and generation, and storage. The process of breakdown may occur in various ways. Considering the reverse biased collector-base junction in a transistor, only the reverse saturation current will flow in the absence of signals. This reverse current is very small at normal ambient temperatures.

As the reverse bias voltage is increased the current gradually increases until breakdown is reached. At breakdown the current

becomes independent of the voltage and is normally limited only by the external circuitry. Breakdown may occur either by surface conduction or by conduction within the body of the material. In the majority of present day diffusion transistors, breakdown is a result of ionization and avalanche multiplication as opposed to surface or punch-through breakdown.

Minority carriers which are thermally or otherwise generated, diffuse to the high field region of the reverse biased junction. They are accelerated, and by collision with atoms in the crystal lattice, produce hole-electron pairs. The holes and electrons produced may themselves produce additional pairs, resulting in an avalanche process.

This breakdown due to impact ionization is analogous to field-intensified ionization and breakdown in gas discharges which are called Townsend discharges. In gases, as the electric field is increased, the current follows at first a simple exponential increase. As the field is further increased the current departs from this simple relationship and eventually there is a sudden transition from the Townsend or dark discharge to a self-sustaining discharge or spark breakdown.

In Figure 1 is a schematic diagram indicating the currents in the avalanche process for a n-p-n transistor. The depletion layer is

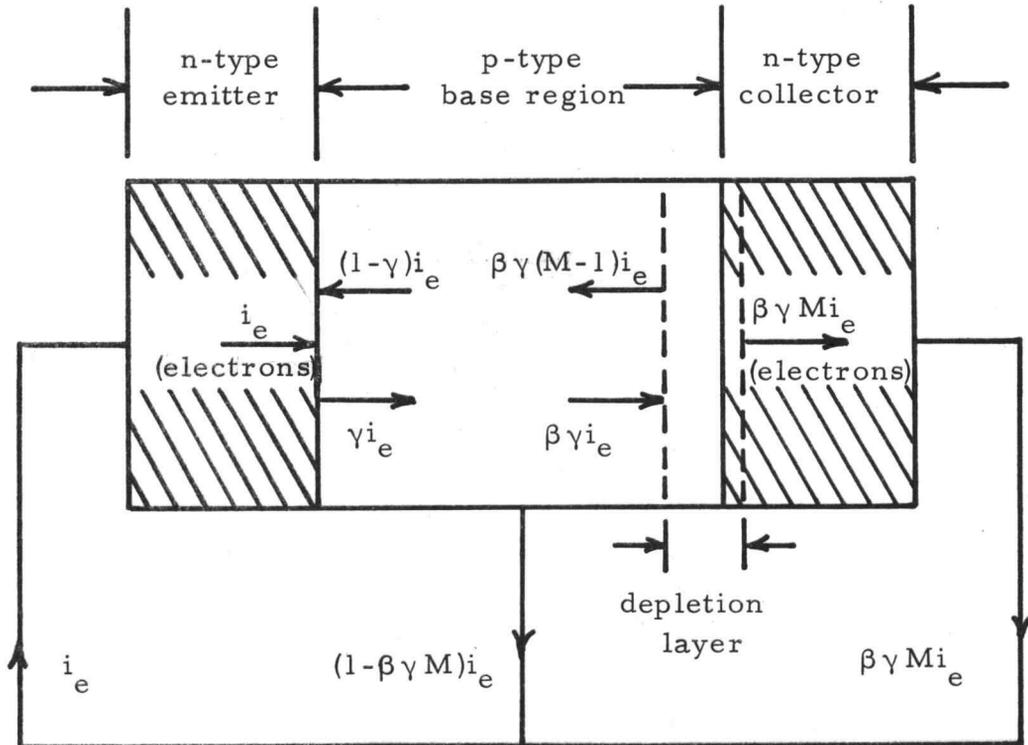


Figure 1

Current-flow Schematic for Avalanche Operation

caused by the reverse biased collector-base junction.

Part of the emitter current  $\gamma I_e$  flowing into the base region is lost by recombination before reaching the collector depletion region. The transport efficiency, designated by  $\beta$ , is the ratio of minority carriers arriving at the collector to the number introduced at the emitter. The fraction lost by recombination then is  $(1 - \beta)$ . Minority carriers thermally generated in the base region also reach the collector and contribute to the total current. Gamma is the emitting efficiency of the emitter.

The rate of multiplication in the depletion region is dependent on the applied voltage and the number of incident electrons. In the depletion layer the incident electrons produce additional hole-electron pairs by impact ionization. Thus the number of carriers reaching the collector junction is a fraction  $M$ , greater than one, of the electrons incident upon the depletion layer. The total current reaching the collector then is  $\beta\gamma M i_e$ .

There will be an associated hole flow returning to the base from the collector. This current may be lost in the base region; through recombination, by reaching the emitter junction, and by leaving through the base lead. The base current must be, to satisfy Kirchoff's law, equal to  $(1 - \beta\gamma M)i_e$  or more simply  $(1 - \alpha)i_e$ .

Lindsay (6, p. 263) has reduced the schematic diagram to an

equivalent circuit for the steady-state avalanche mode of operation. From it he has derived formulas describing the common emitter input and output characteristics.

The expression for  $M$  has been empirically arrived at by Miller (8, p. 1234) and is

$$M(V_{BC}) = 1 / [1 - (V/V_b)^n] \quad (1)$$

where  $M(V_{BC})$  is the multiplication factor,  $V_b$  is the breakdown voltage, and  $n$  is an exponent approximately 2.5 for silicon when the minority particles chiefly responsible for multiplication are either electrons or holes. The value of the multiplication factor controls the rate of build-up of current in avalanche devices. Hamilton (5, p. 1788) has shown that at a given ambient temperature, the optimum bias current which should be used to obtain  $M_{\max}$  varies inversely with the breakdown voltage and that  $M_{\max}$  is proportional to the ratio of optimum bias current to thermally generated current. This current is shown to be:

$$I_{\text{opt}} = (k T_a^2) / (E_g C V_b) \quad (2)$$

where  $k$  is Boltzmann's constant,  $T_a$  is the ambient temperature,  $E_g$  is the energy gap between conduction and valance bands,  $C$  is the junction temperature rise above ambient in degrees centigrade per

watt dissipated, and  $V_b$  is the breakdown voltage.

The response time of the multiplication process should be comparable with the transit time for carriers across the high field region in the reversed biased junction. For high frequency diffusion transistors this time would be a fraction of a nanosecond. The rise to peak current in the avalanche process is then dependent on both the multiplication factor of the transistor and its alpha cutoff frequency. For capacitor loads the maximum value of 10 to 90 percent rise time is (3, p. 35):

$$T_r \text{ max} = \frac{1.6 (V_o - V_p) (W_{bp}^2 / 2D_e) (n + 1)}{V_b (V_o / V_b)^{n + 1}} \quad (3)$$

where  $W_{bp}$  is the base width at peak current,  $D_e$  the effective diffusion constant for minority carriers in the base region,  $V_o$  is the capacitor voltage at the beginning of the pulse, and  $V_p$  is the capacitor voltage at peak current.

In addition to breakdown occurring by avalanche multiplication there is another means by which the transistor may break down. As the reverse bias is applied to a p-n junction, a region of high electric field is formed called the depletion or space-charge region. If the regions are homogeneous as in simple alloy transistors, the electric field intensity will be linear and the depletion region will be

proportional to the applied reverse bias. An increase in reverse bias widens this depletion region and at sufficiently high reverse biases the collector depletion may extend across the base region and make contact with the small electric field associated with the unbiased emitter-base junction.

The voltage required to do this is defined as the punch-through voltage,  $V_p$ . At this voltage, the transistor will suddenly conduct because the direction of the electric field is such that the minority carriers that diffuse across the emitter base junction, against the built-in electric field, experience a high conductive path to the collector.

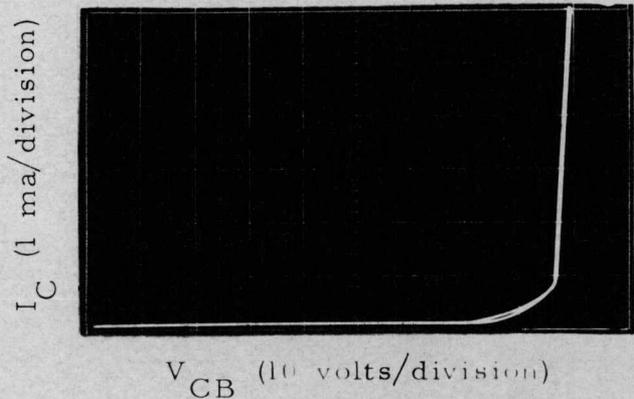
As opposed to alloy junction transistors, diffusion transistors usually have a punch-through voltage higher than the avalanche voltage (11, p. 2). It is desirable, however, to select avalanche transistors so that, although the avalanche voltage is less than  $V_p$ , it is close to it. When thus chosen, the base region at collector voltages near breakdown is only a fraction of the total width of the base material. The transit time of carriers is then greatly reduced resulting in an effective increase in cutoff frequency. The result is, therefore, a faster build up of current when the junction breaks down.

#### TERMINAL BEHAVIOR

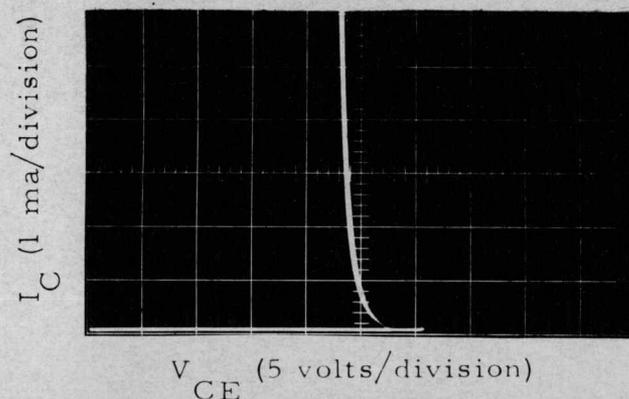
The transistor behaves much like a gas discharge tube in some

respects. Prior to breakdown its characteristics exhibit a high resistance region and after breakdown a low resistance. Figure 2a shows the current-voltage plot with open emitter. Only leakage current flows below the collector-base breakdown voltage  $BV_{CBO}$ . As  $BV_{CBO}$  is approached multiplication of reverse current occurs, eventually resulting in breakdown. When the base is left open the current-voltage plot is as in Figure 2b. The peak voltage  $BV_{CEO}$  is a function of  $BV_{CBO}$  and as the current is increased the voltage drops to  $LV_{CEO}$ . Figure 2c shows the current-voltage plot when the base and emitter are shorted. As the voltage is increased no appreciable current flows until  $BV_{CES}$  (equal to  $BV_{CBO}$ ) is reached. The current then increases due to multiplication until it reaches a value  $I_A$  so that the voltage drop across the internal spreading resistance,  $r_{bb}$ , forward biases the emitter-base diode. The voltage then falls to  $LV_{CES}$  with a current build up due to avalanche multiplication as described above. The voltage remains at  $LV_{CES}$  unless the current is reduced below a holding value,  $I_H$ , where the voltage returns to  $BV_{CES}$ . In general  $I_H$  is below  $I_A$ . The hysteresis is related to the different current flow paths which make  $r_{bb}$  effectively higher approaching from the high current side than from the lower side (2, p. 2).

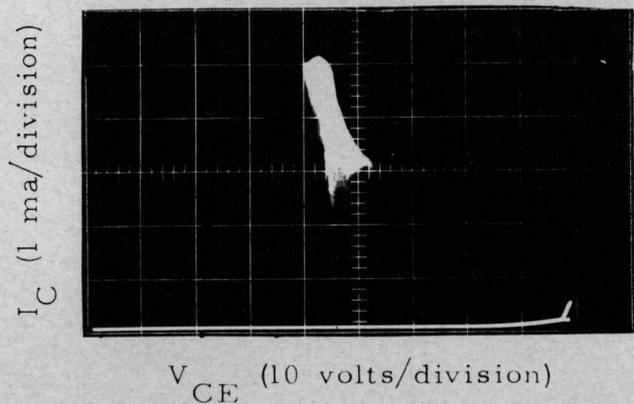
When a resistance,  $R_b$ , is inserted between the base and



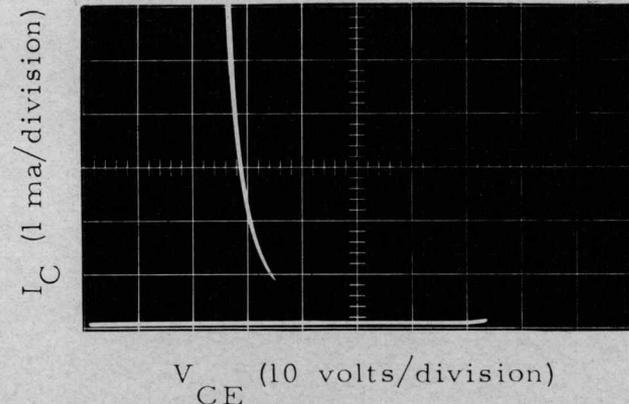
a -  $I_C$  versus  $V_{CB}$  for  $I_E = 0$



b -  $BV_{CEO}$  and  $LV_{CEO}$  for  $I_E = 0$



c -  $BV_{CES}$  and  $LV_{CES}$  with E-B Shorted



d -  $BV_{CER}$  and  $LV_{CER}$  with  $R_b = 10K$  ohms

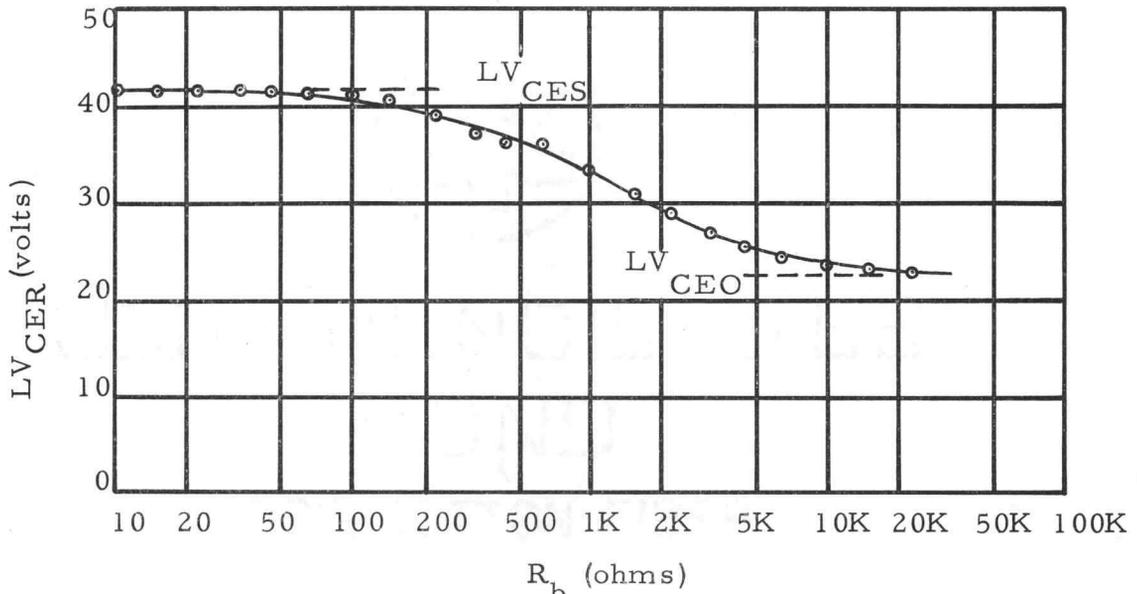
Figure 2

emitter the voltages are changed depending on the value of resistance inserted. The oscillogram in Figure 2d shows  $BV_{CER}$  and  $LV_{CER}$  with 10,000 ohms connecting the base to the emitter. Figure 3a shows the effect of  $LV_{CER}$  as a function of  $R_b$  and Figure 3b exhibits the dependence of  $I_A$  on the value of the external base resistance. All of the above figures were taken from a typical 2N914 transistor.

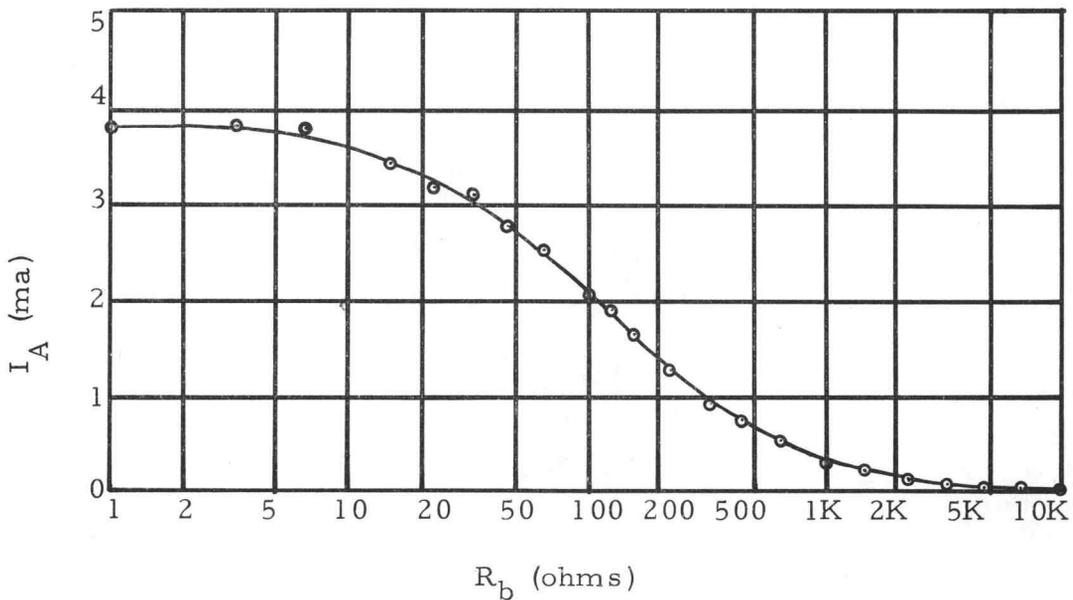
#### AVALANCHE PULSE CIRCUITS WITH LUMPED CAPACITOR LOADS

Perhaps the simplest pulse circuit utilizing avalanche transistors is one using a lumped capacitance on the collector as shown in Figure 4. This circuit may be made to either free-run or be triggered. Considering the free-run situation and the transistor initially off, the voltage at the collector increases exponentially through the  $R_c C_a$  time constant. Eventually the voltage reaches  $BV_{CER}$  and the transistor avalanches to  $LV_{CER}$ , the charge on the capacitor discharges through the transistor until the current reaches  $I_H$  and the transistor returns to the off condition.

For triggered operation the load line intersects the transistor characteristic curve at a point where the collector current is below the avalanche current  $I_A$  as shown in Figure 5. This establishes a stable quiescent operating point,  $Q$ , and capacitor  $C_a$  is charged to just below  $BV_{CER}$ . Applying a  $\Delta I_t$  trigger current at the collector



a - LV<sub>CER</sub> as a Function of External Base Resistance



b - Avalanche Switching Current as a Function of External Base Resistance

Figure 3

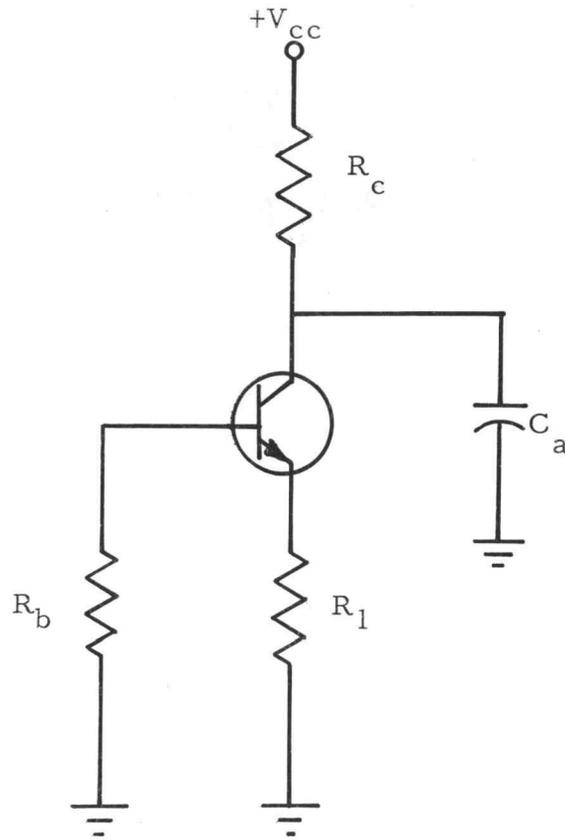


Figure 4. Basic Avalanche Switch with Capacitance Load

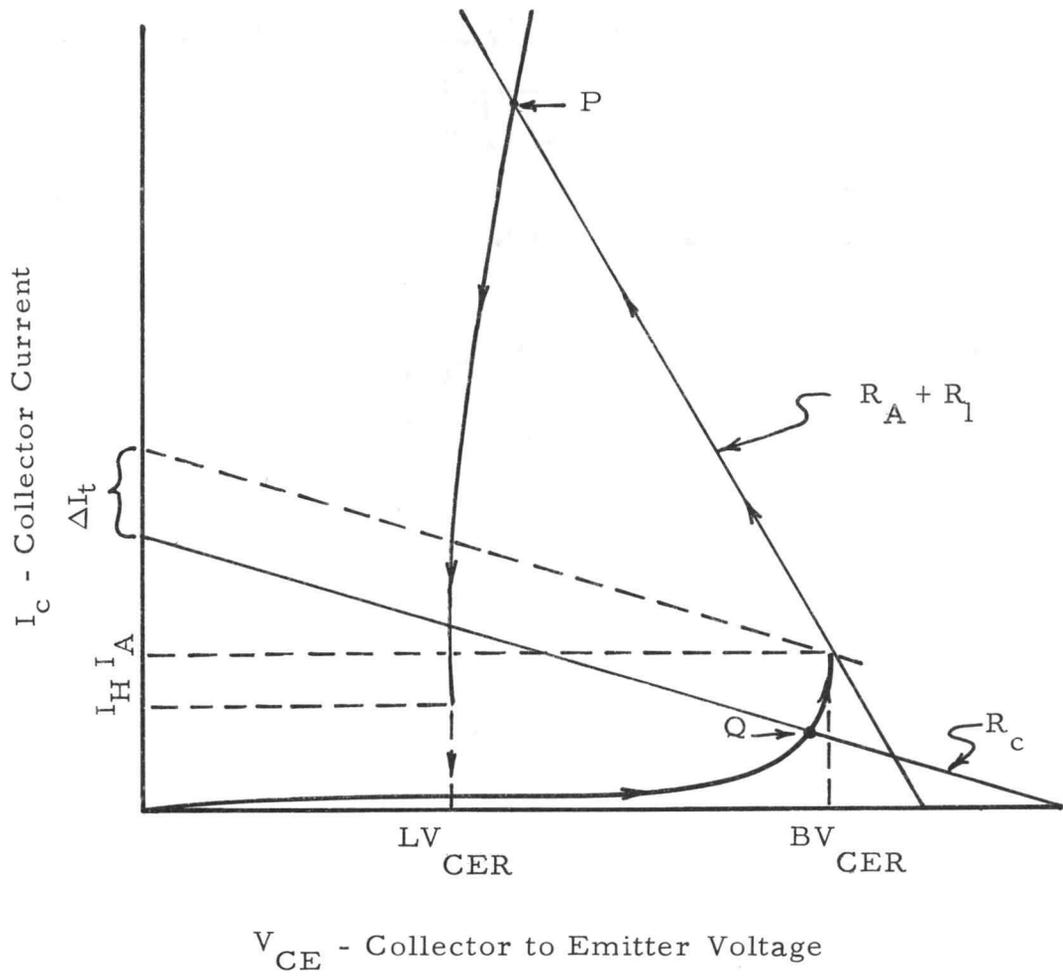


Figure 5. Avalanche Characteristic Curve Showing Switching Load Line

raises the operating point to  $I_A$  on the curve and the transistor avalanches.

The collector current rises abruptly and follows the new load line formed by  $R_A + R_1$  until it intersects  $LV_{CER}$  at P where it remains until the charge on  $C_a$  is insufficient to maintain the discharge current.  $R_A$  is the effective resistance of the transistor in the avalanche condition. The current then decreases following the  $LV_{CER}$  curve until  $I_H$  is reached. Below  $I_H$  the transistor ceases conducting and  $C_a$  recharges towards  $V_{cc}$  with a time constant of  $R_c C_a$ .

The load resistor may be placed either in series with the emitter or in series with the capacitor. For an n-p-n transistor and  $R_1$  in the emitter leg the output pulse will be positive going, and with  $R_1$  on the collector side the pulse out will be negative. If the charge stored in  $C_a$  is insufficient to allow the voltage across  $C_a$  to remain constant as the transistor breaks down, then the amplitude of the output pulse becomes limited. The amplitude of the pulse out depends then on the values of  $C_a$  and  $R_1$  and for large values of either  $C_a$  or  $R_1$  the amplitude of the pulse becomes equal to the voltage difference between  $BV_{CER}$  and  $LV_{CER}$ . The pulse width at the 50 percent points is controlled for the most part by the  $(R_1 + R_A) C_a$  time constant as the initial rise is quite fast compared to the fall time. The resistance  $R_A$  is the resistance of the transistor in the broken-down

condition.

Table I presents the amplitude and pulse-width as a function of the capacitor value for the circuit of Figure 4. The supply voltage was adjusted to 112 volts and the pulse circuit free-ran with a pulse repetition rate controlled by  $R_c$  and  $C_a$ . The maximum pulse recurrence frequency is limited only by the allowable dissipation of the transistor. This circuit may also be triggered as will be described later.

A transient analysis of avalanche transistor circuits with a capacitance load has been carried out through use of a diffusion model described in terms of charge variables by Hamilton (3, p. 25). He later extended the analysis to include the effects of resistance in avalanche transistor pulse circuits on the current rise time (4, p. 456).

The output pulse was monitored across the 50 ohm load by a Tektronix Model 585 oscilloscope with a type 80 plug-in unit having a rise time of 3.5 nanoseconds. Figure 6a shows the shape of the voltage pulse across the load with C equal to 1000 pf and Figure 6b shows the output with C equal to 50 pf as monitored with a Tektronix type N sampling unit having a rise time of 0.6 nanoseconds.

#### AVALANCHE PULSE CIRCUITS WITH RESISTANCE LOADS

Avalanche transistor pulse circuits which use capacitance loads

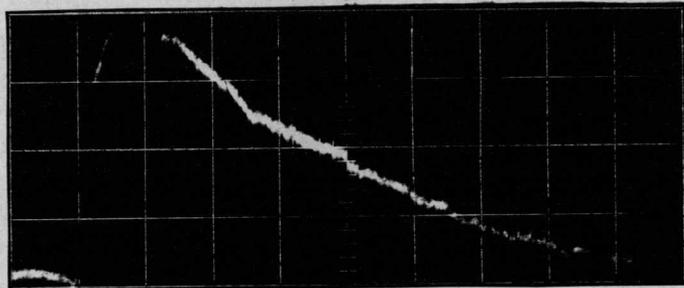
Table 1. Rise Time, Amplitude, and Pulse Width for Different  $R_1$  and  $C_a$  Combinations

$R_1$	$C_a$	$T_r$	AMPL	PW
50 $\Omega$	1500 pf	3.5 ns	37 v	38 ns
50	1000	3.5	36	30
50	500	3.5	31	19
50	200	3.5	28	12
50	100	3.5	26	8
50	50	3.5	21	6
50	stray	3.5	2	2
100	100	2	27.5	11
50	100	1	25	10
20	100	0.6	15.5	7
10	100	0.6	10	6

Circuit Values (See Figure 4):

Transistor	2N914
$V_{cc}$	112 v
$R_c$	220K $\Omega$
$R_b$	10K $\Omega$

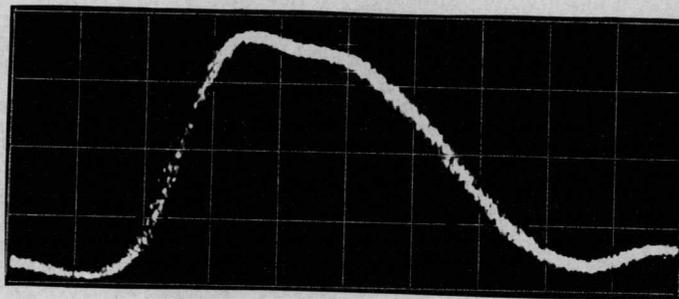
Output Voltage  
(10 volts/division)



Time (10 ns/division)

a - Voltage Across  $R_1$  for  $R_1 = 47$  ohms  
and  $C_a = 1000$  pf

Output Voltage  
(5 volts/division)



Time (1 ns/division)

b - Voltage Across  $R_1$  for  $R_1 = 22$  ohms  
and  $C_a = 50$  pf

Figure 6

produce high-current, short-duration pulses but the pulse shape is not easily controlled. When the load is resistive and takes the form of a transmission line, control of the pulse shape and length may be achieved. The basic circuit using a delay line load is shown in Figure 7.

The operation of the circuit may be described as follows: At time zero the capacity of the line begins to charge through  $R_c$ , when the voltage at the collector reaches  $BV_{CER}$  the emitter junction becomes forward biased and injects carriers into the base. Avalanche regeneration occurs and the collector voltage drops to  $LV_{CER}$  producing a step function of voltage across the open circuited line. This voltage step travels down the line discharging each section as it goes and maintains thus a constant current. When the step reaches the end of the line it is reflected in phase since there is no resistive termination to absorb the energy. The reflected step function continues to discharge the line thus keeping the current constant until it reaches the end of the line. If the pulse sees the characteristic impedance of the line when it arrives at the collector, the impedance of the line suddenly becomes infinite, the current goes to zero and no reflections occur. The line begins again to charge towards  $BV_{CER}$  through  $R_c$ .

When the resistance of the transistor in the avalanche condition

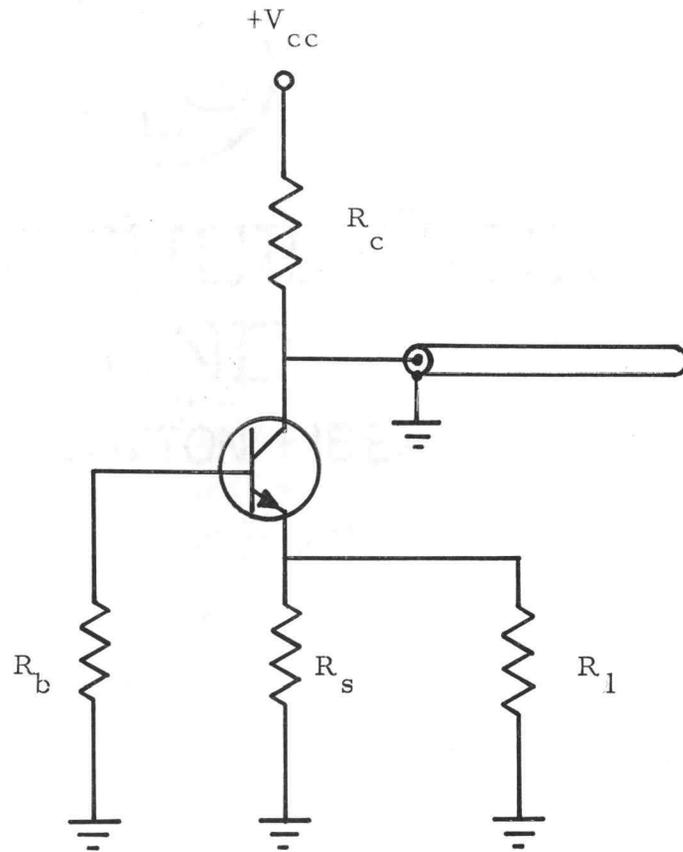
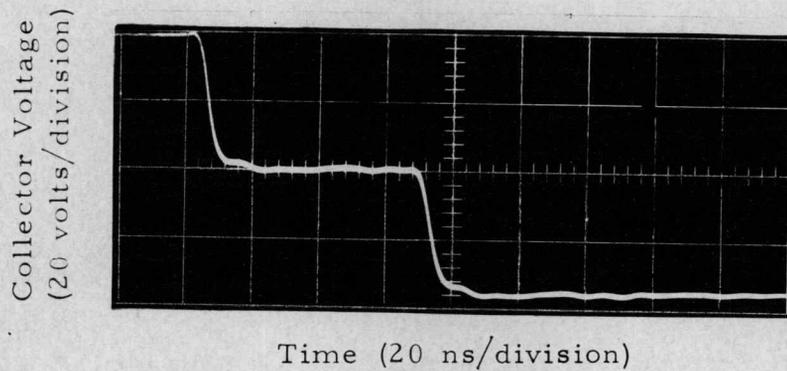


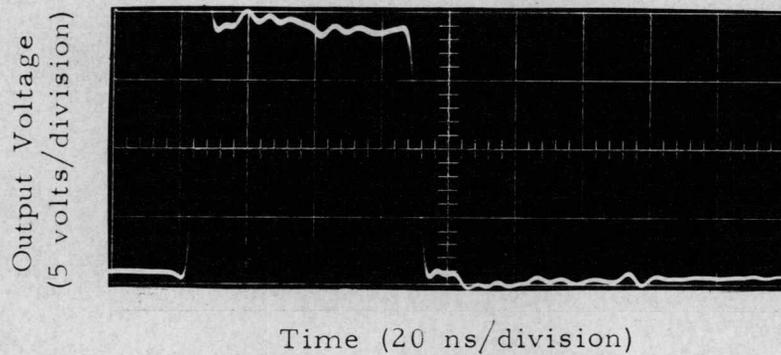
Figure 7. Basic Avalanche Switch with Resistance Load

and the parallel resistance of  $R_s$  and  $R_l$  equal the characteristic impedance of the transmission line no reflections occur and the output across  $R_l$  is a single pulse. The resistance  $R_s$  is used to match the transmission line to the load for different transistor resistances and was equal to 220 ohms for the 2N914 transistor. Generally it was found for 2N914s that  $LV_{CER}$  was nearly one half of  $BV_{CER}$  when  $R_b$  equalled 10,000 ohms and the voltage at the collector went to zero when the pulse returned on the transmission line.

Shown in Figure 8 are the wave forms at the collector and across the load resistor. An open-ended delay line produces a pulse of current equal in duration to twice the length of the line. The pulse across the characteristic impedance in series with the line has one half the amplitude of the step function. The output pulse has a rectangular shape, the duration of which is independent of the transistor. In the avalanching condition the impedance of the transistors used was approximately 40 ohms. The transmission line producing the largest pulse amplitude into a 50 ohm load would be 90 ohms for the line to be terminated correctly. Ninety-three ohm transmission line is available in RG-62/U and by adding shunt resistance to the load it is possible to reduce reflections and obtain relatively clean output pulses. For the transistors used (2N914) a value of  $R_b$  greater than 5,000 ohms proved adequate.



a - Collector Waveform versus Time



b - Corresponding Voltage Across Load versus Time

Figure 8

In place of a distributed parameter transmission line, it is possible to use a delay line constructed of lumped parameters. Such a line provides an easy method of conveniently controlling the duration of the pulse: that is, by simply opening the line at different sections, the pulse duration is altered. Such a line was designed (1, p. 209) and built using slide switches at intervals along the line to provide pulse lengths of 10, 20, 50, and 100 nanoseconds. Slide switches were found suitable for such use having 3 pf capacitance to ground in the closed position and only 1 pf to ground in the open position. The delay line was designed to have a characteristic impedance of 100 ohms and a delay per section of five nanoseconds. To reduce mismatch between sections the capacitors were measured on a precision impedance bridge and arranged in increasing value along the line. The spread in capacitor values from the first section to the tenth section was about six percent and even though placed in sequence to minimize the impedance change between sections there were noticeable reflections in the output pulse. Trimmer capacitors in addition to the fixed capacitors would probably reduce these mismatches considerably. The measured rise time of the line, being proportional to the delay per section, was ten nanoseconds which limited the fall time of the pulse generated until  $I_H$  was reached. The rise time of the pulse, however, is relatively independent of the

delay rise time.

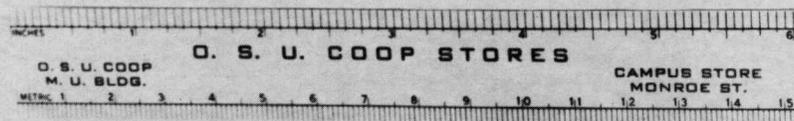
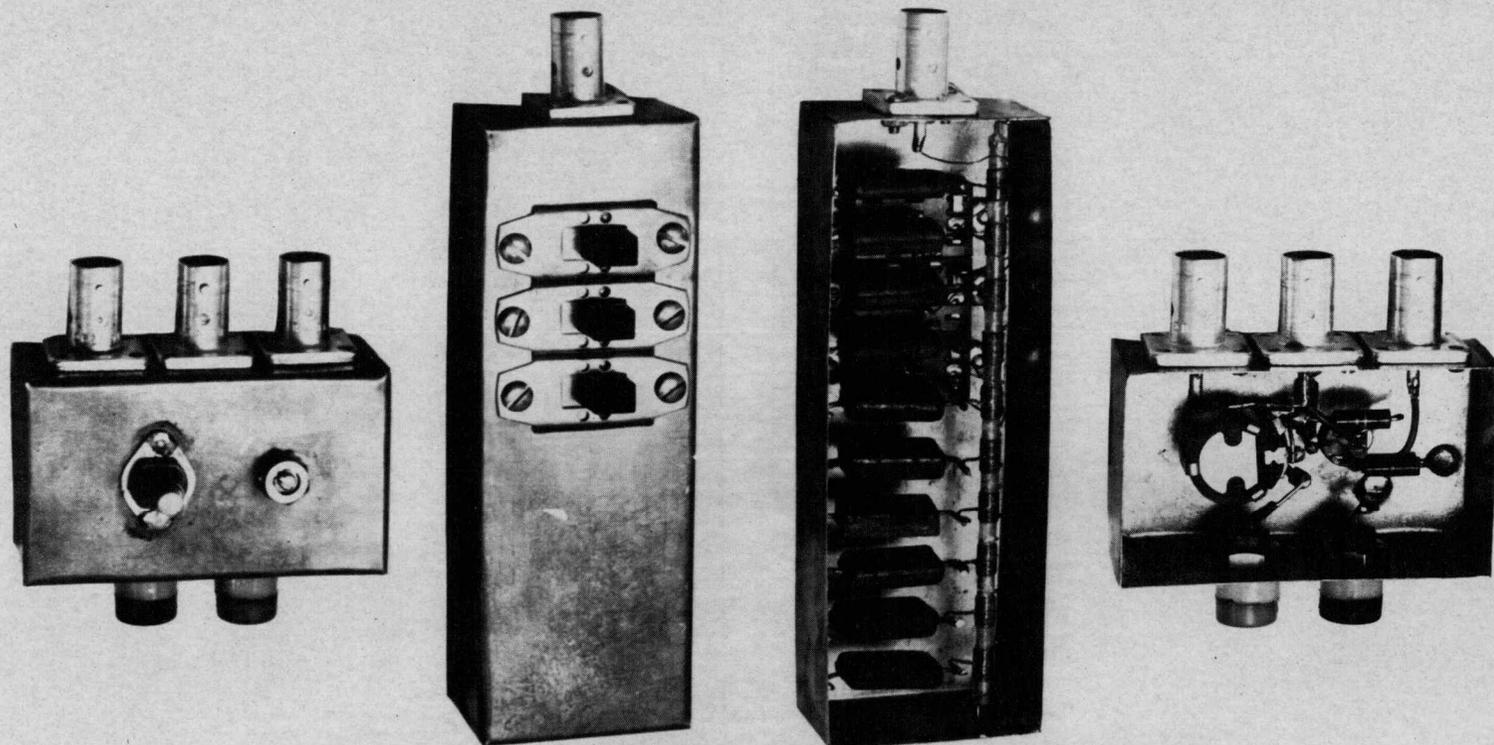
Figure 9 shows photographs of a pulse generator and a delay line that were built. In Figure 10 are their circuit schematics. The collector resistance is composed of two resistors, one fixed and one variable. The 10,000 ohm fixed resistor was chosen so the maximum power dissipation of the transistor would not be exceeded. The variable resistor permits adjusting the pulse repetition frequency which is an exponential function of the total collector load resistance and the total capacity of the charge line. The time interval between pulses is given by:

$$T = R_c C_1 \ln(V_{cc} / BV_{CER}) \quad (4)$$

where  $R_c$  is the sum of the fixed and the variable collector resistance, and  $C_1$  is the capacitance of the delay line. The emitter resistance, 220 ohms, is needed to match to the 50 ohm load.

The trigger from the collector may be used either as a trigger out in the case of free running operation or as a trigger input when  $+V_{cc}$  is adjusted to hold the current below  $I_A$ . Collector triggering produces the shortest delay and requires the least energy for triggering (10, p. 27).

In Figure 11 are depicted the waveforms of the pulses using this pulse generator with first, in part a, pulses produced using



Avalanche Pulse Generator and Delay Line  
Figure 9

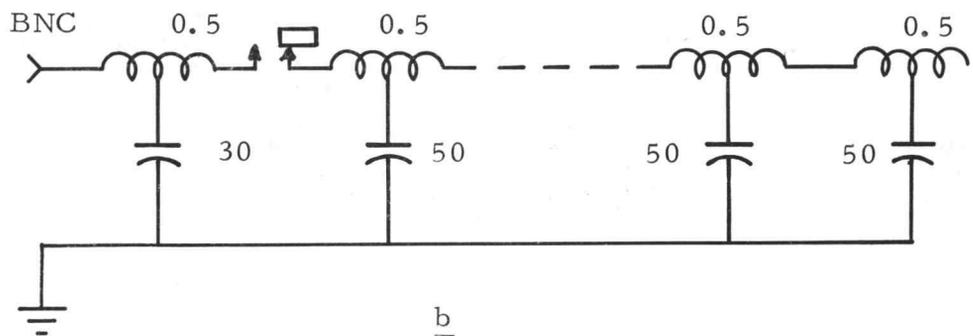
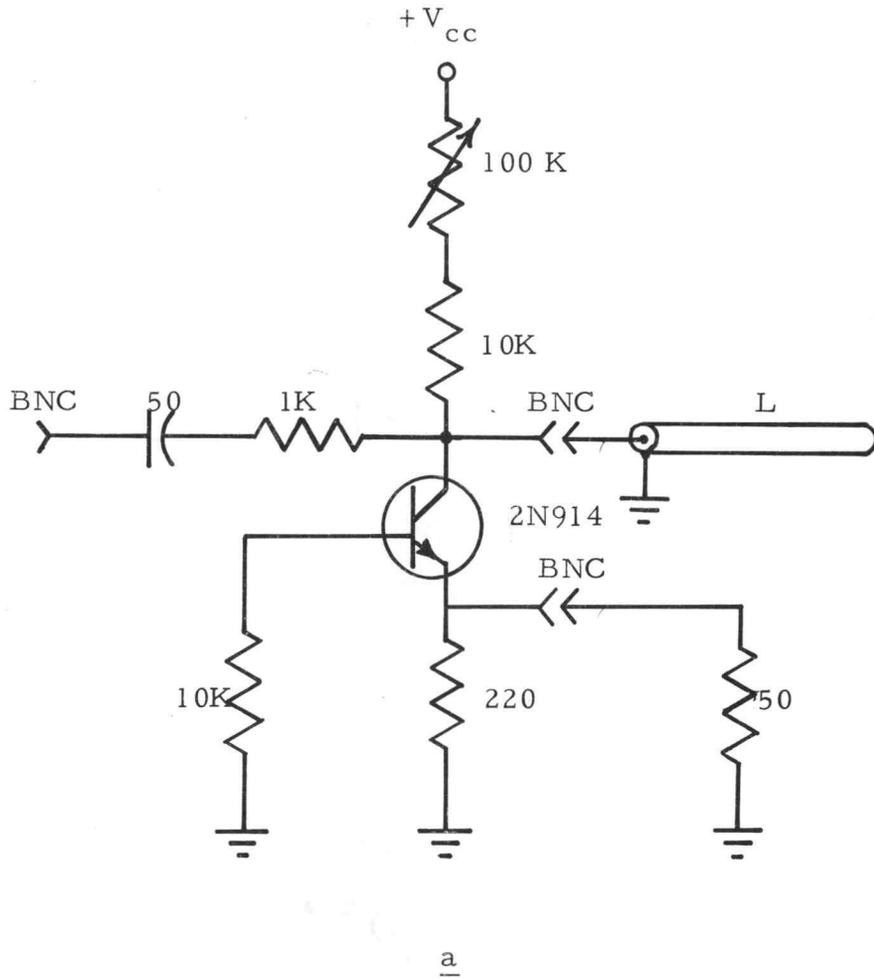
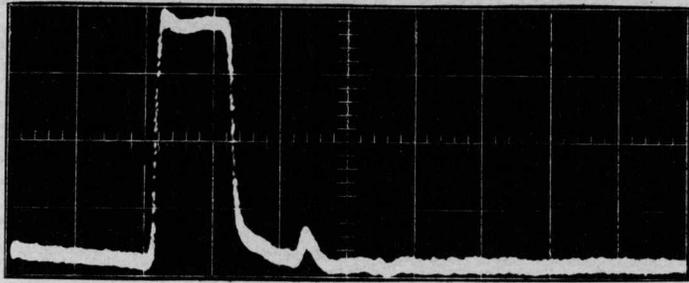


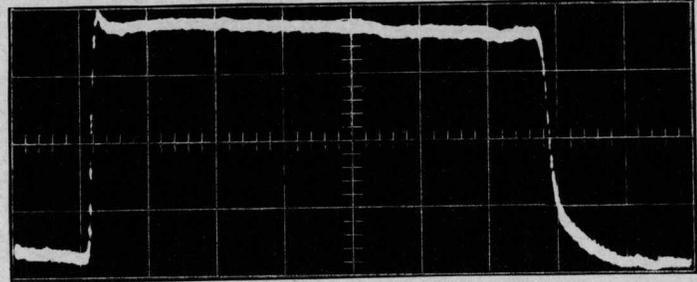
Figure 10. Avalanche Pulse Generator and Lumped Constant Delay Line Circuit Schematics. Resistors in ohms, Capacitors in pf, and inductors in  $\mu$ h.

Output Voltage  
(5.6 volts/division)



Time (10 ns/division)

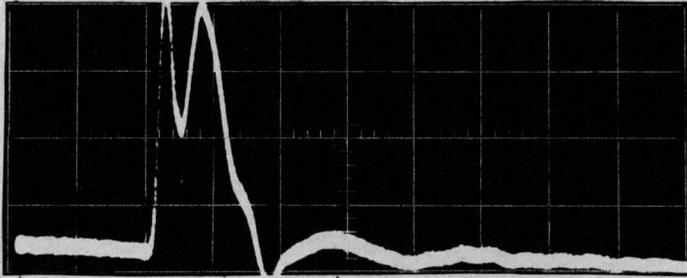
Output Voltage  
(5.6 volts/division)



Time (10 ns/division)

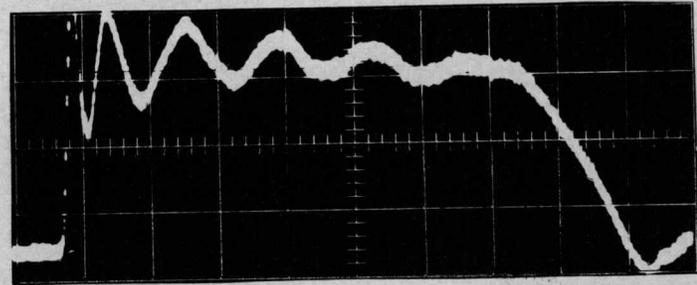
a - Output Waveforms using RG-62/U Cable

Output Voltage  
(6.4 volts/division)



Time (10 ns/division)

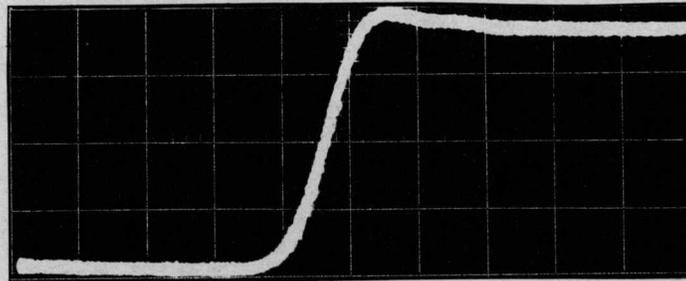
Output Voltage  
(6.4 volts/division)



Time (10 ns/division)

b - Output Waveforms using Lumped Constant Delay Line

Output Voltage  
(5.6 volts/division)



Time (1 ns/division)

c - Part a Expanded

Figure 11

RG-62/U cable of 4 feet and 25 feet in length and in part b, 20 and 100 nanosecond pulses generated using the lumped constant delay line. Figure 11c shows the initial portion of pulse in part a expanded to one nanosecond per centimeter by using a Tektronix type N sampling unit. Using the approximation that the apparent rise time equals the square root of the sum of the squares of the N unit and the pulse generator rise times, the actual rise time of the avalanche pulse generator is 0.8 nanoseconds.

#### COMPOSITE AVALANCHE TRANSISTOR CIRCUITS

Application of transistors in the avalanche mode to generate variable-width pulses may also be accomplished with composite circuits. One way might be to trigger a transistor into avalanche breakdown, and then return the transistor to a normal off condition at some later time. During the time the transistor is at  $V_{CER}$ , current can be delivered to the load.

Another and perhaps easier method to achieve fast rise pulse-width control is by letting an avalanche transistor generate the fast rise time of the pulse and then adding this rise time to the pulse of a saturating transistor. This latter method was studied and will be presented here. Briefly the scheme used was the following: A monostable multivibrator generated a pulse whose width could be adjusted

by controlling the d.c. bias on the base of the first transistor by a variable resistor. The pulse of the multivibrator fed a two-stage common emitter isolation and power amplifier which in turn drove both a saturating common emitter switch and triggered an avalanche transistor into breakdown. The output of these two transistors was summed in the 50 ohm load resistor. Figure 12 presents the block diagram of the pulse generating method.

Assuming the avalanche generates a step voltage followed by a RC exponential discharge through the load resistance, the response will be:

$$I(t) = \frac{BV_{CER} - LV_{CER}}{R_T + R_A} e^{-t/(R_T + R_A) C_a} \quad (5)$$

where  $R_A$  is the equivalent resistance of the transistor in the avalanche condition,  $R_T$  represents  $R_1$  plus any resistance ( $R_v$ ) necessary for voltage amplitude matching, and  $C_a$  is the capacitance at the avalanche transistor collector.

The turn-on response for the transistor switch in the active region is also an exponential and of the form:

$$I_C(t) = \frac{\alpha_0 \Delta V}{(1 - \alpha_0) r_b + r_e} \left[ 1 - e^{-\omega_n \left(1 - \alpha_0 + \frac{r_e}{r_b}\right) t} \right] \quad (6)$$

the necessary conditions for these two responses to add to a flat top voltage pulse across the load are:

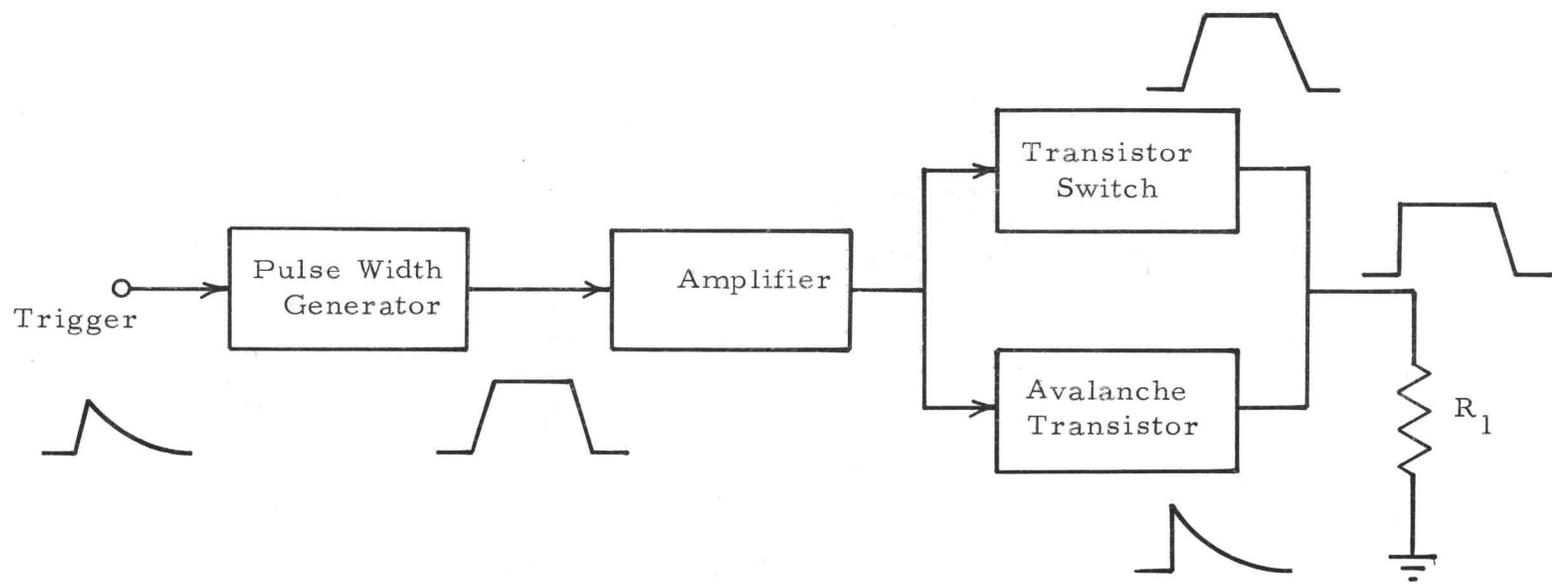


Figure 12. Composite Pulse Generator Block Diagram

$$\frac{\alpha_o \Delta V}{r_e + (1 - \alpha_o)r_b} = \frac{BV_{CER} - LV_{CER}}{R_T + R_A} \quad (7)$$

and

$$\omega_n \left( 1 - \alpha_o + \frac{r_e}{r_b} \right) = \frac{1}{(R_T + R_A) C_a} \quad (8)$$

where  $\alpha_o$  is the value of  $\alpha$  at zero frequency,  $r_e$  and  $r_b$  are small-signal equivalent circuit parameters, and  $\omega_n$  is the radian cutoff frequency of alpha.

In the practical case of satisfying the above conditions it is necessary to adjust the amplitude and pulse width of the avalanche pulse by adjusting  $R_T$  and  $C_a$ . Overshoot and ringing can easily be adjusted to less than 5 percent of the peak amplitude.

The circuit schematic is shown in Figure 13. The monostable multivibrator was designed to be externally triggered but could just as well be free running. Improvement in the rise time is apparent in the pictures of Figure 14. Without the avalanche transistor pulse the rise time of the output pulse is 30 nanoseconds. Adding the pulse from the avalanche transistor reduces the rise time to less than 3.5 nanoseconds. Capacitor  $C_a$  on the collector of the avalanche transistor in conjunction with  $R_v$  and the load resistor determine the width of the pulse from the avalanche transistor. Resistor  $R_v$  was

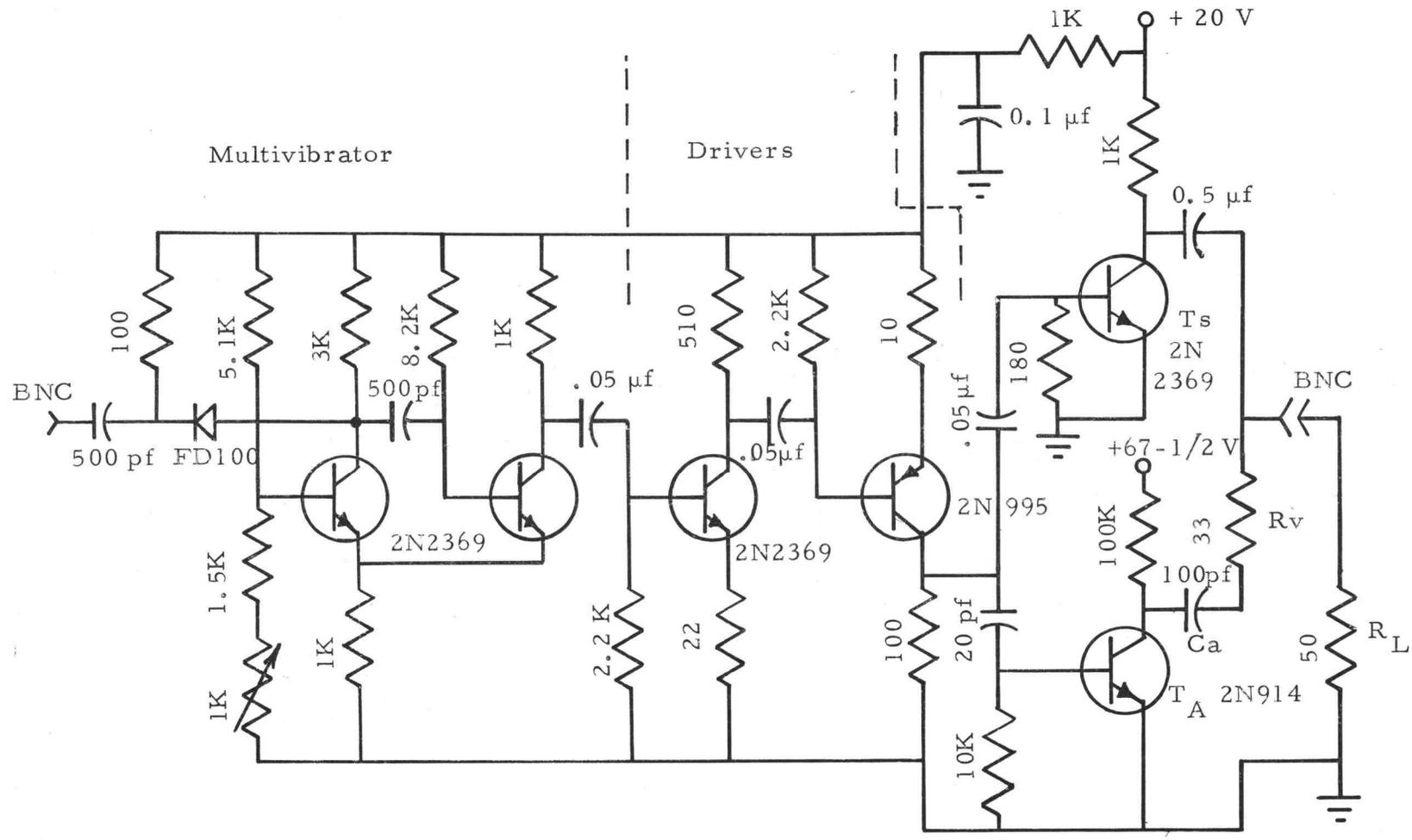
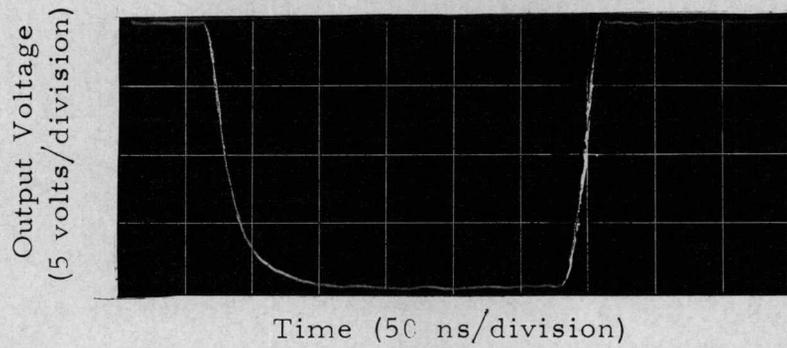
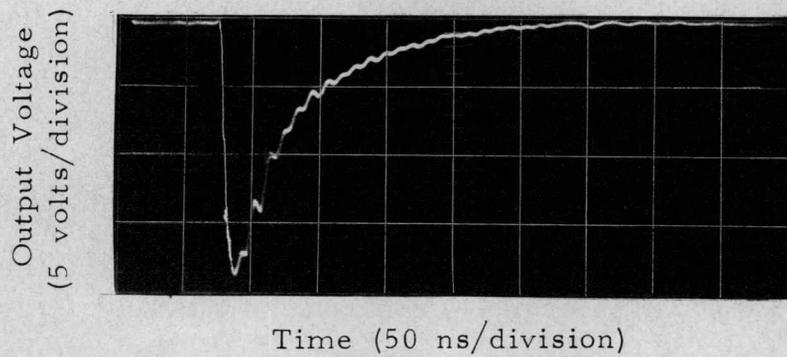


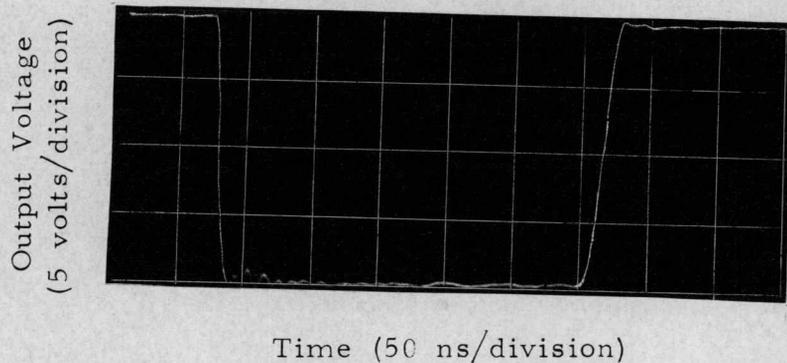
Figure 13. Composite Pulse Generator Circuit Schematic



a - Transistor Switch Pulse



b - Avalanche Pulse



c - Composite Pulse Waveform

Figure 14

necessary so the peak voltage amplitudes from the saturating transistor,  $T_s$ , and the avalanche transistor,  $T_a$ , could be made equal at the load resistor. Satisfaction of Equation (7) can also be achieved by varying the supply voltage of the switching transistor.

To summarize the operation to this method for producing fast rise variable-width pulses, Table II presents measured characteristics of the pulse generator.

Table II. Composite Pulse Generator Specifications

SPECIFICATIONS	
Output Amplitude:	20 volts negative across 50 ohms
Rise Time:	< 3.5 nanoseconds
Pulse Widths:	70 ns (min) to 1.8 $\mu$ s (max)
Pulse Delay:	20 nanoseconds
Repetition Rate:	Externally triggered, Max rate, 1.5 MC
External Drive:	5 volt negative signal required

Turnoff times were, in this circuit, simply the turnoff time of the saturated transistor. However, if it is necessary to have as fast turn off as turn on times this could be achieved also with an avalanche transistor. In one method investigated the positive pulse used to trigger the avalanche transistor and drive the switching transistor was first inverted with a transformer and then

differentiated. The positive going differentiated pulse was used to trigger a transistor into the avalanche mode of operation. A transformer was used to invert the pulse produced across a resistor in series with a capacitor in the collector circuit. This pulse was then added to the fast rise and variable duration pulse produced with the composite circuit described above. The second avalanche pulse being of opposite polarity and occurring at the end of the variable pulse quickly pulls the output to ground. The amplitude of the turn off pulse can be adjusted by varying the turns ratio of the output transformer. Using this method the 40 nanosecond turn on and turn off times of a pulse produced with a 2N914 transistor were improved to five and seven nanoseconds respectively.

If only an improvement in the turn off time is desired then this could be achieved by placing an inductor from the base to ground of the saturating transistor and direct coupling to the driver stage. The energy stored in the inductor during the on portion of the pulse quickly turns the transistor off at the end of the pulse.

#### SUMMARY

This thesis has presented and described techniques which can be used to generate very fast pulses where the width of the pulse generated may be controlled. Rise and fall times on the order of

nanoseconds and sub-nanoseconds with amplitudes of 50 volts across 50 ohms are possible using the switching property based on the avalanche effect of ordinary diffused junction transistors.

Three general methods of producing variable-width pulses have been investigated. Fastest rise times are possible with capacitor loads but the pulse shape has the disadvantage of slow fall times. As has been stated, pulses of this nature would most likely find application in timing pulse generators, trigger pulses, rise time evaluation of fast circuits, and if differentiated could be used as narrow pulse-width sampling pulses in sampling oscilloscopes. Avalanche pulses produced using resistive loads in the form of delay lines have the characteristics of fast rise times, flat tops, and fast fall times. Their disadvantage lies in the necessity of having a different length of cable for each pulse length when using distributed delay lines. This inconvenience is overcome by using lumped parameter delay lines and varying the number of sections in the line. This type of delay line has the further advantage of being physically more compact and may be designed to match the impedance of a particular load and transistor without sacrificing pulse power as is necessary in matching cables to particular load impedances.

Resistive loads produce approximately one-half the amplitude across a given load impedance as capacitive collector loads do.

This is because half of the voltage swing at the collector appears across the resistive line whereas in a capacitor collector load the full voltage appears across the transistor and load resistor.

For generating long duration pulses the composite method of adding an avalanche pulse and a pulse generated by a switching transistor is useful. The power dissipated in both the avalanche and the saturating transistor is low which permits either higher repetition rates or longer pulses without exceeding power limitations. This method would probably be preferable for applications requiring the pulse width to be continuously adjustable.

With the present availability of transistors designed specifically for avalanche operation their application in circuits will undoubtedly increase. The extremely fast ionization process in semiconductors offers a means of producing fast, high power pulses required in such applications as digital computer circuitry with memory cycle time of tens of nanoseconds, fast time-of-flight nuclear spectrometers, power drivers in microminaturized circuitry, and numerous additional applications requiring fast rise, high power pulses.

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APPENDICES

## APPENDIX I

PROOF OF MAXIMUM RISE TIME TO PEAK CURRENT WITH  
CAPACITOR LOAD

This appendix will present the derivation of the maximum rise time for the current in the case where the load is strictly capacitive. It follows the derivation of Hamilton (3, p. 35) very closely and is included not only for completeness but because it is the fast rise time of the avalanche mode of operation that is of the greatest interest.

The current  $I$  at breakdown rises nearly linearly with time and will therefore be approximated by a linear rising current  $i(t)$  as shown in Figure 15. The minimum value that  $dI/dt$  can have during the linearly rising portion of  $I$  is represented by  $di/dt$ .

The total change in charge  $\Delta Q$  in the external circuit during the rise from zero to  $I_p$  is

$$\Delta Q = \int i \, dt = I_p^2 / (2 \, di/dt). \quad (9)$$

This charge must be supplied by the capacitor  $C$  so we can say:

$$\Delta Q = C(V_o - V_p) \quad (10)$$

Combining equations (9) and (10) an estimate of the minimum value

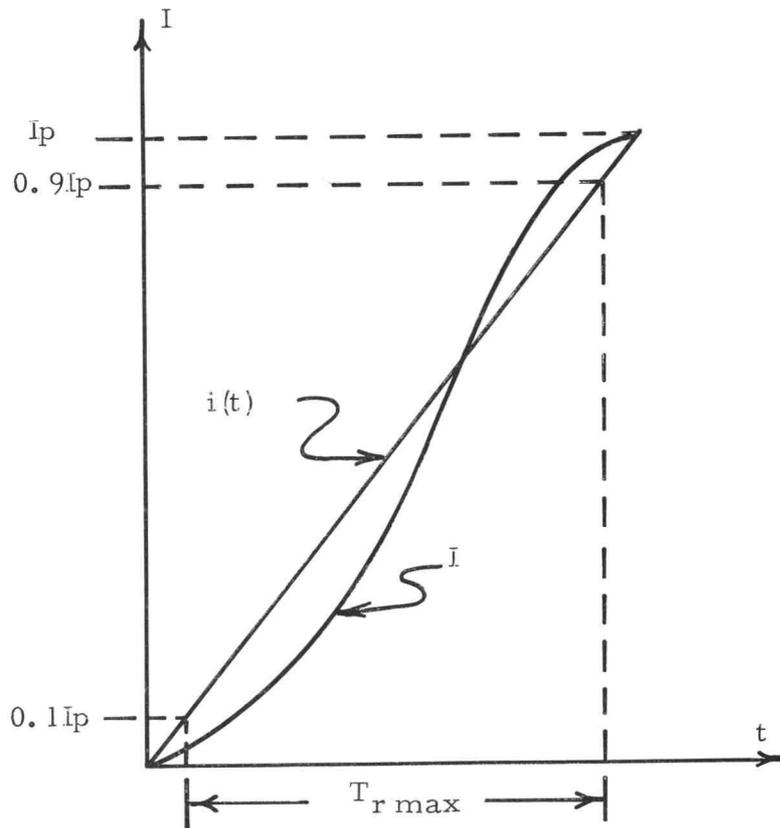


Figure 15. Approximation of  $I$  by Linear  $i(t)$

of the rate of rise is obtained:

$$(dI/dt)_{\min} = di/dt = I_p^2 / 2C(V_o - V_p) \quad (11)$$

which also equals

$$(dI/dt)_{\min} = Q_{sp}^2 / 2\tau^2 C(V_o - V_p) \quad (12)$$

where  $Q_{sp}$  is the stored charge at peak current and is found from a stored charge model for the avalanche transistor to be

$$Q_{sp} = [CV_b / (n + 1)] (V_o / V_b)^{n + 1} \quad (13)$$

and from a linear distribution of charge approximation the peak current is

$$I_p = Q_{sp} 2D_e / W_{bp}^2 = Q_{sp} / \tau. \quad (14)$$

The maximum 10 to 90 percent rise time will be then,

$$\begin{aligned} T_{r \max} &= \frac{1.6 C(V_o - V_p)}{I_p} \\ &= \frac{1.6 (V_o - V_p)\tau(n + 1)}{V_b (V_o / V_b)^{n + 1}} \cdot \end{aligned} \quad (15)$$

## APPENDIX II

## PROOF OF SATURATED TRANSISTOR TURN-ON RESPONSE

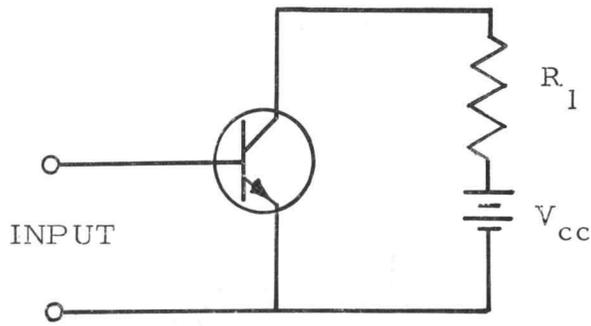
It is the purpose of this appendix to calculate the transient response of a transistor in the active region (9, p. 1774). Figure 16a illustrates the basic circuit for the common emitter switch and Figure 16b its corresponding equivalent circuit. This is a simplified Tee model small signal equivalent circuit, neglecting space-charge widening effects but including  $C_{se}$  the diffusion capacitance associated with the minority carrier density in the base region. This equivalent circuit is sufficiently accurate to describe transient response to a time definition of  $1/\omega_0$  to  $1/10\omega_0$  where  $\omega_0$  is the radian cutoff frequency of alpha.

The assumption that alpha has the form

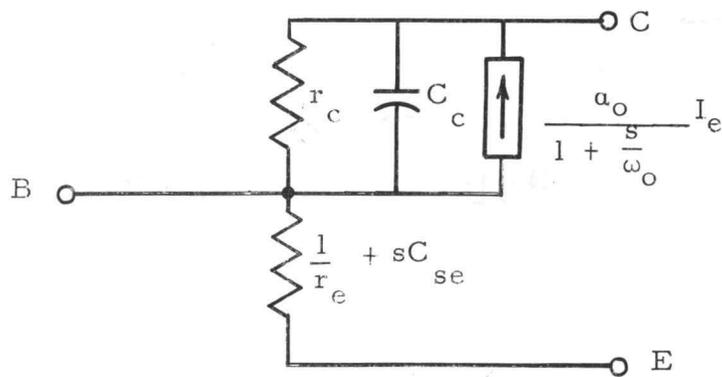
$$\alpha(s) = \frac{\alpha_0}{1 + s/\omega_0} \quad (16)$$

is used where  $\alpha_0$  is the value of alpha at zero frequency and  $s$  is the Laplace transform complex variable.

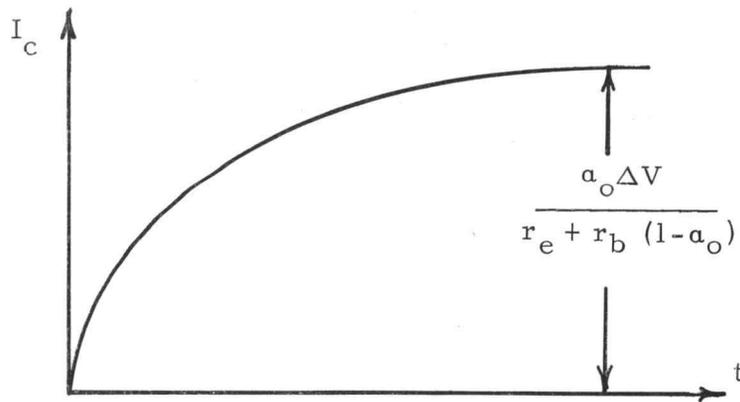
The current gain for the common emitter configuration will be its short circuit value if the following conditions hold:



a - Transistor Switching Circuit



b - Small-signal Equivalent Circuit for Calculating Transient Response



c - Response of Transistor in Common Emitter Circuit to Small  $\Delta V$  in Base Voltage

Figure 16

$$\frac{R_c}{V_c} \ll 1 - a_o \quad (17)$$

$$\omega_o C_c R_c \ll 1 \quad (18)$$

which are valid for the present case. The short circuit current gain is

$$\frac{I_c(s)}{I_b(s)} = \frac{a_o}{1 - a_o + s/\omega_o} \quad (19)$$

and the input impedance is

$$\frac{V_b(s)}{I_b(s)} = r_b + \frac{r_e}{1 - a_o + \frac{s}{\omega_o}} \quad (20)$$

Solving for  $I_c(s)$

$$I_c(s) = \frac{a_o V_b(s)}{r_e + r_b \left(1 - a_o + \frac{s}{\omega_o}\right)} \quad (21)$$

For a step  $\Delta V$  in base voltage the Laplace transform is

$$V_b(s) = \frac{V}{s} \quad (22)$$

then

$$I_c(s) = \frac{a_o \omega_o \Delta V}{r_b s \left[ s + \omega_o \left(1 + \frac{r_e}{r_b} - a_o\right) \right]} \quad (23)$$

Separating Equation (23) by partial fractions yields

$$I_c(s) = \frac{a_o \Delta V}{r_b (1 - a_o + \frac{r_e}{r_b})} \left[ \frac{1}{s} - \frac{1}{s + \omega_o (1 - a_o + \frac{r_e}{r_b})} \right] \quad (24)$$

Taking the inverse gives finally,

$$I_c(t) = \frac{a_o \Delta V}{r_e + r_b (1 - a_o)} \left[ 1 - e^{-\omega_o (1 - a_o + \frac{r_e}{r_b})t} \right] \quad (25)$$

Figure 16 c shows the ideal response of the grounded emitter switch to  $\Delta V$  in base voltage.