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Donn Eugene Bernhardt for the M.S. degree in Elect. Engrg.

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Title A FAST CARRY BINARY ADDER

Abstract approved _____

This thesis describes the adder to be used with the Galaxy computer, which is to be constructed at Oregon State University.

The need for faster, more reliable adders is discussed along with previous adder designs related to the Galaxy Fast Carry Adder.

Both the logical design and circuit design of the Galaxy Fast Carry Adder are discussed. Operating speed measurements for a 3 bit adder are presented and used to predict operating speeds of a 49 bit adder. Reliability considerations are discussed, and a set of worst case resistor value calculations is included as an appendix.

The use of the adder circuit in the Galaxy computer is also discussed.

A FAST CARRY BINARY ADDER

by

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INTRODUCTION

The Need for Speed and Reliability

In modern high speed electronic digital computers there is a need for faster and more accurate computing capabilities. This need is a result of the increasing number and complexity of problems being solved by computers.

One of the more important parts of most modern scientific electronic digital computers is the adder, or accumulator, as it is sometimes called. In machines such as the Galaxy computer, the adder is used in nearly every operation. These include addition, subtraction, multiplication, division, and the determination of storage locations in the magnetic core memory.

Because the adder is used so often, its speed of operation and reliability have a direct effect on the operating speed and reliability of the computer. For this reason, the adder design, both logical and electronic, has stressed operating speed and reliability, rather than a minimum number of components.

The Institute for Advanced Study Adder

In 1955, Gilchrist, Pomerene, and Wong, (2) described an adder carry system for the Institute for Advanced Study computer. This computer was to be a vacuum tube computer with a parallel arithmetic unit and a three step add operation. The carry system described by the authors was used for the second step of the add operation. It used separate lines for one and zero carries.

The system, as described, took advantage of the fact that the average length of the longest carry in the addition of two operands is much shorter than the length of the two operands (1, p. 10)(3)(7). For the 40 bit operand used, the average length of the longest carry encountered is about 5.6 bits. Thus, the average carry propagation time was about 1/7 of the time required to propagate a carry 40 bits.

To determine when the carry step had been completed, a long AND gate, which sampled the carry line at each bit position, was used. When a carry was present at each bit position the carry step was complete and the third step of the add was started.

The Manchester Adder

Kilburn, Edwards, and Aspinal have described the adder system used in the ATLAS computer at Manchester University, Manchester, England (4, p. 573-584). ATLAS is a transistorized computer which uses surface barrier transistors in the arithmetic section.

The adder circuit uses a single carry line which has two operating voltage levels. The carry line is held at the zero level until an operate pulse is received. It then assumes a one or a zero level, as determined by the operands and the incoming carry. The operate signals must last long enough for the adder logic and carry gates to operate, and for the carry to propagate the full length of the adder. The sum is gated into one of the operand registers by a pulse which is long enough to allow the register to receive it, but not long enough to allow the sum to propagate back through the adder, thereby creating a new sum.

An add time of 200 ns for a 20 bit test adder was achieved. No attempt was made to determine exactly when each add had been completed.

The Argonne Adder

Salter has described the adder used in the Argonne National Laboratory FLIP Arithmetic Unit (9). This unit is a transistorized parallel arithmetic unit which is used with their vacuum tube computer, GEORGE.

This adder uses a single 3 level carry line which is activated when the operands are presented to the adder. Since most of the add time is taken by the parallel circuits, (those in each bit which operate simultaneously) and not by the serial carry propagation, no attempt is made to determine when the carries have been completed. The maximum length add time is used for all additions.

The add time for a 68 bit adder was 230 ns.

THE LOGICAL DESIGN OF THE GALAXY FAST CARRY ADDER

Logical Arrangement

The logical design of the Galaxy Fast Carry Adder was described in a paper by Phillips entitled, "A Logical Design for an Asynchronous Parallel Adder" (5, p. 1-13).

The design uses separate transmission lines for ones and zeros at the inputs, for the carry line, and for the

output. This double rail system, as it is called, is necessary in order to achieve completely asynchronous timing. The double-rail system also has other advantages, as will be explained later.

A logical block diagram of one bit of the adder is shown in Fig. 1. The double rail operand inputs, A and B, are made at the two operand comparison circuits, which determine the equality or non-equality of the operands. $\overline{A}$ and $\overline{B}$ represent zero inputs while A and B represent ones. If the operands are equal, a one or a zero carry will be generated and gates 3 and 4 will be turned on. If the operands are unequal, the carry gates, gates 1 and 2, and gates 5 and 6 will be turned on. All of these gates are deactivated when one or both of the operands are removed.

When the carry arrives from the preceding bit position, it will pass through the gates that have been turned on by the operands. In the case where the carry is present before the operands (as in the least significant bit position) it merely waits until the gates are turned on, and then propagates through them.

After the incoming carry has passed through one of

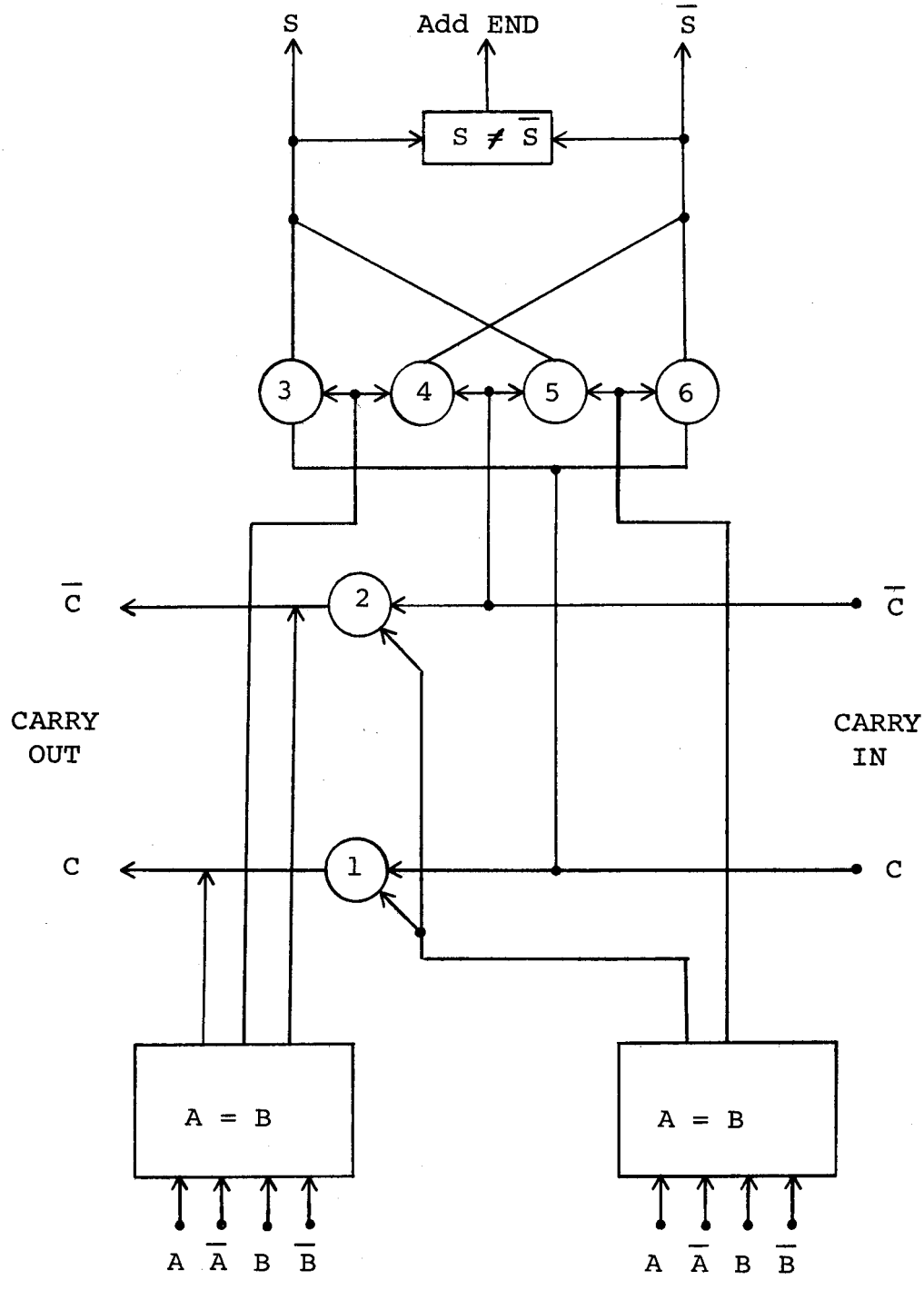


Figure 1. Adder Logical Block Diagram

the gates 3, 4, 5, or 6, it appears as the sum at the output of the adder.

In order to determine when the add has been completed, the output of each bit of the adder is sampled by a large AND gate. In order to improve the noise immunity of the adder, this AND gate is designed to respond only when there is a single output at each bit.

If it is necessary to save the carry out of the most significant bit of the adder, the carry line out of that bit can be included as one of the inputs to the long AND gate. In this case, a circuit similar to the one used at the sum outputs could be used to sample the carry line.

Design Advantages and Disadvantages

This design is different in many respects from each of the designs mentioned earlier. It also has a number of advantages over all of them.

Faster transistors and improved circuit design have reduced the operating times of the portions of each bit of the adder that operate in parallel, so a larger portion of the total addition time is required for the carry propagation. This is true even though the operating

speed of the carry line has been increased. This in effect means that there will be a significant difference between the average add time and the maximum add time. It becomes advantageous, therefore, to make the adder an asynchronous unit and let it time its own completion.

To do this, it is necessary to use a transmission system with three or more states. These states would be a one state, a zero state, and a no operand state. This can be done by using a single transmission line with three stable voltage levels. This system does not work well as tolerances become hard to control. Saturated transistors are basically two state devices, so it becomes necessary to convert from two levels to three levels and then back to two levels in many cases.

In the double rail system, ones and zeros are transmitted on separate two-state transmission lines. The added complexity of this system over the single two-state transmission system is the biggest disadvantage of this transmission system. It more than doubles the number of transistors required. The Galaxy adder requires 35 transistors per bit, while the Argonne adder requires only 12 transistors per bit (9).

Increasing the number of components also increases the probability of component failure. This is the only other significant disadvantage of this system.

The component unreliability is more than offset by the improved operating reliability and noise immunity offered by the double-rail system over the single line system. A close examination of the adder logic will show that almost any stray noise signal in the adder or on the transmission lines into the adder will result in both a one and a zero sum being present at one or more bit positions. Since the add complete signal is generated only when one or the other, but not both of the outputs are present, the computer will wait until the stray signal has disappeared and the proper sum is present before it continues. If the stray signal is due to some component failure, and persists, the computer will remain locked in the add step, and the error will be apparent to the operator. This feature is not present in any of the previously mentioned systems.

THE FAST CARRY LINE

A Comparison with the Half Adder

One of the more commonly used adder systems is the half adder system (6, p. 22). First, a partial sum and a carry are formed from the two operand inputs. Then the partial sum and the carry from the previous bit position are used as inputs to a second half adder which forms the final sum and a carry. The carries from the two half adders are combined, and sent on to the next bit position. This adder is also known as a ripple carry adder.

In the half adder system a carry must travel through several circuits in each bit position. A carry which must propagate through an adder with N bits, each having a delay D, will require a time equal to N times D to reach the end of the carry line.

If such an adder were constructed using circuits similar to those used in the Galaxy Fast Carry Adder, a delay time of 20 ns per bit might be expected. This means that a 49 bit adder of the half adder type would require nearly one microsecond just to propagate the carry.

The principal advantage of the single transistor gate used in each bit position of the fast carry line should now be apparent. Instead of a 20 ns delay in each bit position, there is a delay in the order of 1 ns. This means that a carry can propagate the full length of the 49 bit adder in less than 50 ns, or 20 times faster than in the half adder system.

Operation of the Carry Line

The carry line described by Phillips consists of two separate transmission lines; one for zero carries and the other for one carries. Each line has three separate parts in each bit position. These are, in the order that a carry would encounter them, a carry sampling point, a carry gate, and a carry insertion point. At the carry sampling point, the incoming carry is sampled and amplified for use in forming the sum. The carry gate is either left open or is closed, depending on the operands. The carry insertion point is the point at which a generated carry is placed on the carry line.

If a truth table of all of the combinations of two operands and a carry is constructed, it can be shown that

the outgoing carry can be determined without the aid of the incoming carry. If the operands are unequal (see Table 1, lines 1 through 4), the outgoing carry is not uniquely determined, but is determined to be the same as the carry in. If the two operands are equal (see Table 1, lines 5 through 8), the outgoing carry is uniquely determined, and is, in fact, equal to the operands.

Adder Truth Table

A	B	C in	C out	Sum
1	0	0	0	1
0	1	0	0	1
1	0	1	1	0
0	1	1	1	0
0	0	0	0	0
0	0	1	0	1
1	1	0	1	0
1	1	1	1	1

Table 1

If the operands are unequal, then the carry gate is turned on. Once the gate is on, the propagation delay through it is about 1 ns.

If the operands are equal, a carry is generated and placed on one of the carry lines. Because of the circuits used, this operation is faster than turning on a carry gate.

The Carry Line Amplifier

The fact that the carry gates are not zero impedance conductors when they are turned on presents somewhat of a problem. If enough adder bits are cascaded, the load currents in the first few gates become quite large. When this happens, the voltage drops across the gates soon add up to a voltage comparable to the carry signal voltage.

This problem can be overcome by placing amplifiers in the carry lines. All of the carry systems discussed earlier used periodic current amplification or voltage level restoration. Both of the transistor circuits used emitter-follower current amplifiers which were connected so that they helped offset the voltage drop of the carry gates. These emitter-followers helped reduce the load currents, but failed to compensate completely for the voltage drops.

The saturated carry gate transistors used in the Galaxy carry line have a higher voltage drop than those used in the earlier circuits (4)(9). This is because it was found necessary to compromise voltage drop in order to gain increased operating speed.

Ideally the transistor should display very short operating times, very low saturated voltage drop, reasonably high forward current gain, very low inverted current gain, and a reasonable price.

In general, the first two requirements cannot be met best by any one transistor type. The diffused transistors are faster and the alloyed transistors have lower saturated voltage drops. The third requirement is met by most transistors. The fourth requirement favors the diffused types. It would be possible to have some manufacturer select special transistors from his regular production items that would fulfill the first four of these requirements, but due to the limited quantity of these transistors used, the last requirement would probably not be met.

The transistors chosen for the carry gates are a germanium epitaxial mesa type which have a higher saturated voltage drop than the ones used in the carry lines described earlier. For this reason, periodic voltage amplification as well as current amplification is needed. The circuit used will be described later.

The Average Maximum Carry Length

Hendrickson (3) and Reitwiesner (7) have both shown that the average maximum carry length resulting from the addition of two randomly arranged operands can be approximated by

$$L_{avg} = Log_2 (5N/4)$$

where N is the number of bits in the operands. This approximation holds only for operands longer than about 10 bits. At lower values of N, the value of L_{avg} given by the above relation is slightly lower than the correct value.

For a 49 bit adder, the value of L_{avg} is 5.93. This means that the maximum carry delay time will be 8.3 times as long as the average carry delay time. Comparing this with the values for the 40 bit carry line given earlier indicates that the longer the carry line is, the more time can be saved by making the add operation an asynchronous operation.

THE ADDER CIRCUIT

Circuit Description

A second block diagram of the adder is shown in Fig. 2. This diagram is slanted more to the circuitry than the diagram shown in Fig. 1. Some of the blocks of Fig. 1 have been shown in more detail so that a better representation of the circuit blocks is obtained. The values of the components in Figs. 3, 4, and 5 are shown in Appendix II.

The blocks in Fig. 2 labeled AND #1 and AND #2 are identical circuits, which, when taken together with the OR #1 block, constitute the A = B block of Fig. 1. Similarly, the identical circuits, AND #3 and AND #4, with the OR #2 block form the A = B block of Fig. 1. The carry generators, level shift, inverter, gate drivers, sampling amplifiers, and sum inverters are all circuit elements necessary to obtain proper voltage and current levels and signal polarities, and play no logical role in the adder. The rest of the blocks correspond directly to those in Fig. 1.

The AND #1 block is made up of T_1, T_2, T_3, T_4, R_1,

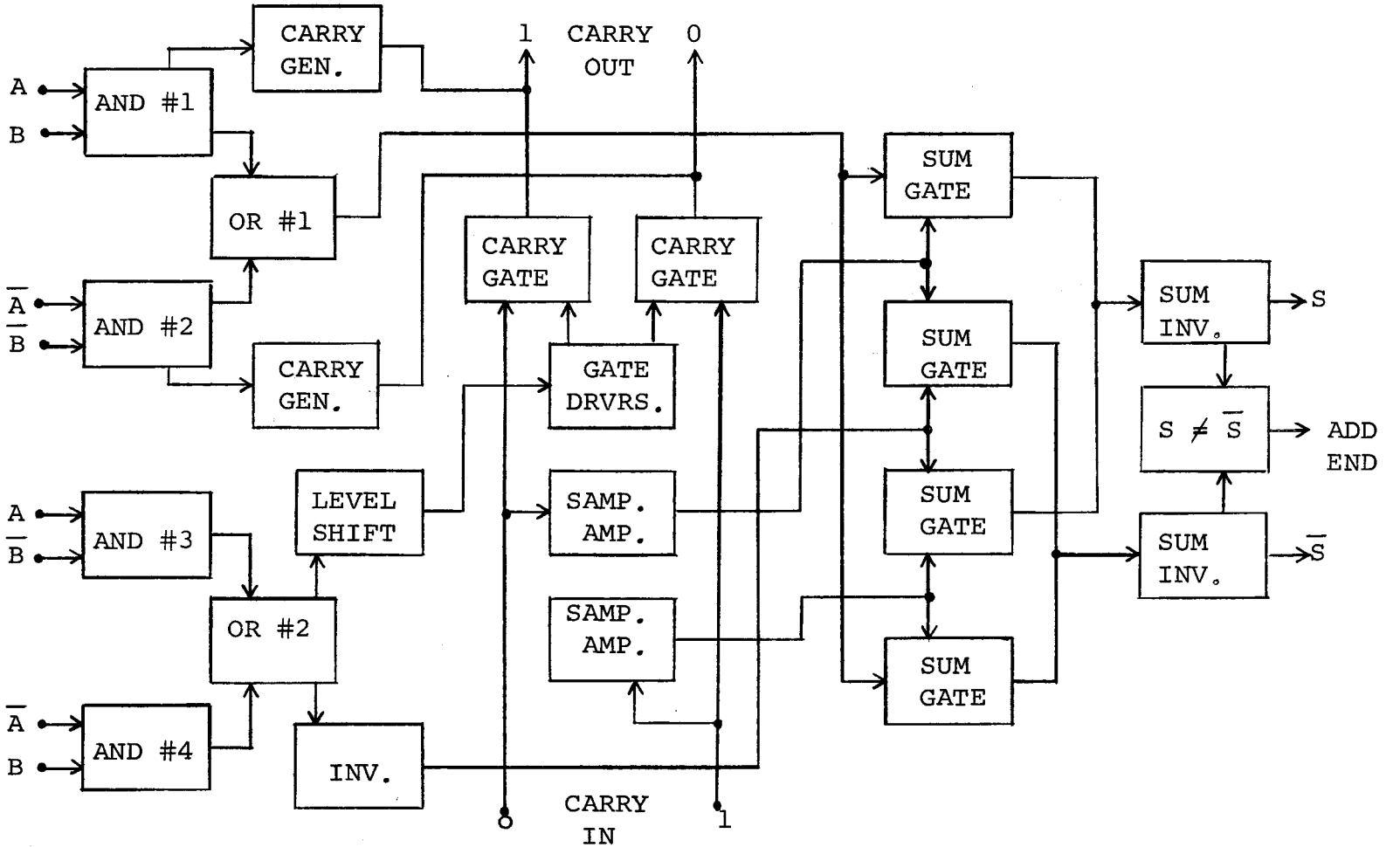


Figure 2. Adder Circuit Block Diagram

R_2, and R_3, as shown in Fig. 3. The circuit consisting of T_1, T_2, T_3, and R_1 is a circuit which was developed by Ruegg and Beeson (8, p. 1-12). The authors have named this circuit Transistor-Transistor Logic, or T^2L.

The features of this circuit are simplicity, very fast operation, and low power dissipation. The gating transistors, T_1 and T_2, are in the saturated condition at all times. The result of this is that most of the delay of this circuit is due to the inverter transistor, T_3. This delay is kept low by providing a low impedance current sink for the inverter reverse base current. Transistor T_4 is a second inverter.

The OR #1 block is made up of D_1, D_2, R_7, and T_{11}. The diodes form the OR function, while the emitter-follower supplies sufficient current to operate the sum gates. R_7 provides a path for any leakage current from T_{11}, and also aids in turning off T_{11}.

The AND #3 block consists of T_{12}, T_{13}, T_{14}, and R_8. The operation of this circuit is identical to the operation of the AND #1 circuit. The OR #2 block is formed by connecting together the collectors of T_{12} and T_{15}.

R_9, R_{10}, D_3, and T_{18} form the level shift circuit.

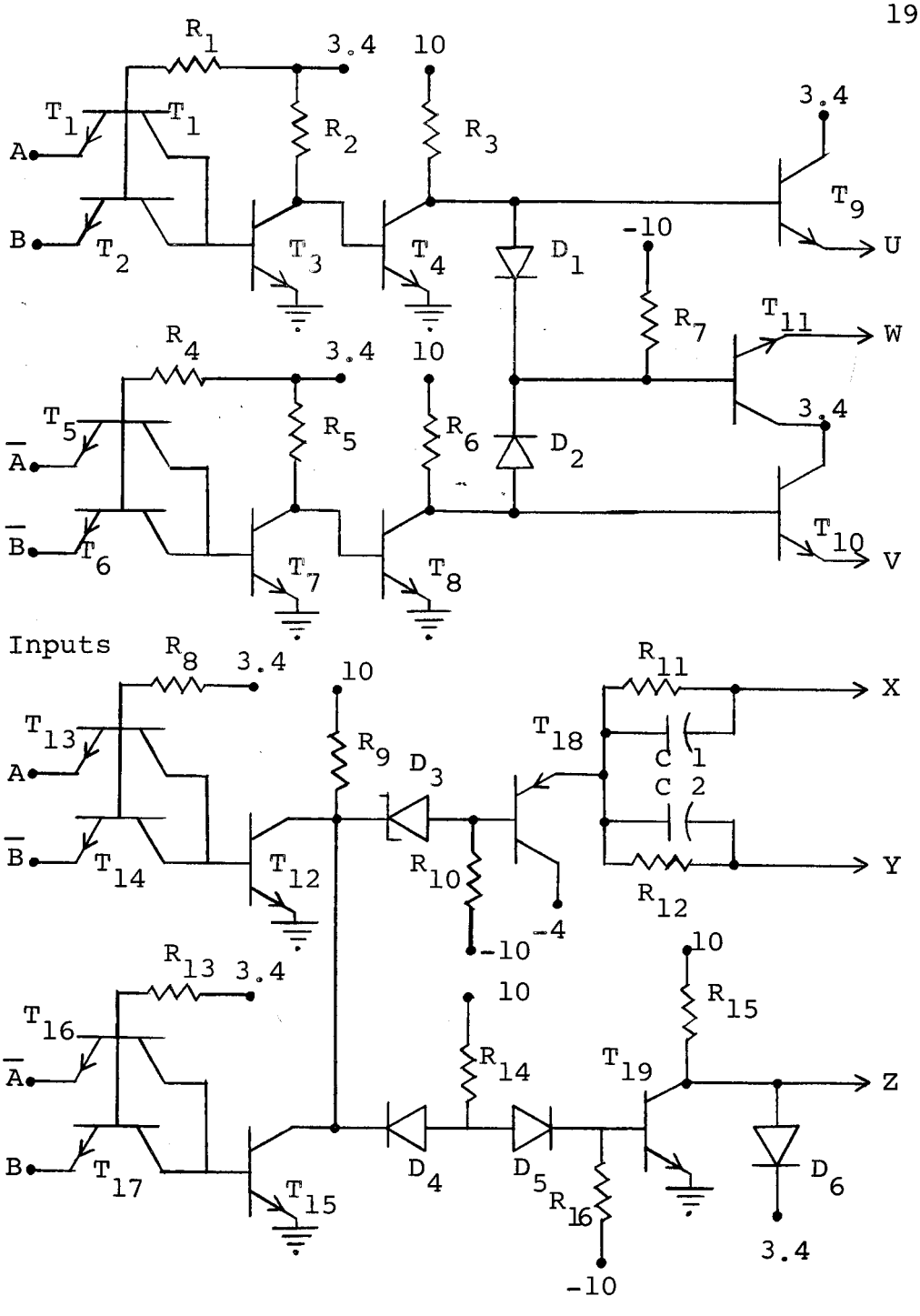


Figure 3. Adder Circuit Diagram, Part 1

A zener diode is used because the level shift required is larger than that which could be easily obtained by a resistor level shift circuit.

In the circuit, T_{18} saturates to provide a stable output voltage. This is necessary to maintain adequate control of the carry gate base current. Resistor R_{10} provides both base current for T_{18} and a small amount of current necessary to maintain a large voltage drop across D_3. R_9 provides enough current to raise the base of T_{18} up to -1 volt when both T_{12} and T_{15} are off.

R_{14}, R_{15}, R_{16}, D_4, D_5, D_6, and T_{19} form the inverter circuit. D_4 is a decoupling diode which allows the collectors of T_{12} and T_{15} to swing as far as required by the level shift circuit. R_{14}, R_{16}, and D_5 constitute a level shift circuit which compensates for the voltage drop of D_4.

Resistor R_{15} provides enough current to drive two sum gates. Diode D_6 clamps the collector of T_{19} to insure that the voltage level does not go too high.

One of the carry line circuits is made up of C_1, R_{11}, R_{17}, R_{19}, D_7, T_{10}, T_{20}, T_{21}, T_{24}, and T_{26}, as shown in Fig. 4. These components form the carry gate, gate

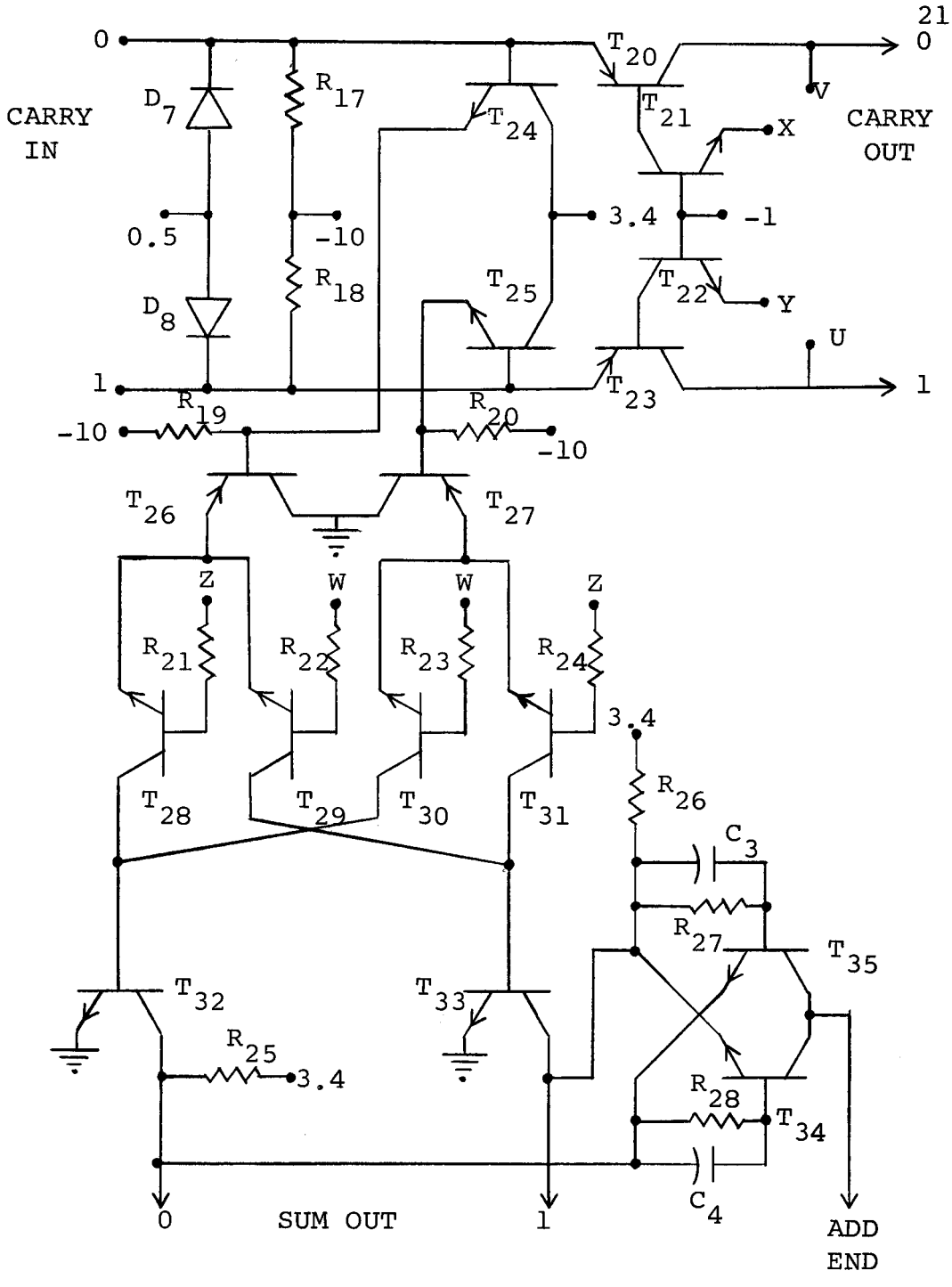


Figure 4. Adder Circuit Diagram, Part 2

driver, sampling amplifier, and carry generator.

The sampling amplifier consists of two emitter-followers and one resistor. The amplifier provides enough current to operate the sum gates without excessively loading the carry line. The carry generator is an emitter-follower which provides enough current to propagate a carry as far as the next carry amplifier. Both of these circuits effectively isolate the carry line from the rest of the adder circuit.

The base current for the carry gate (T_{20}) is supplied by the gate driver, T_{21}. This driver is a non-saturating current sink with a very high collector impedance. This high impedance base current sink provides a constant base current for T_{20} without using a large voltage between the emitter of T_{20} and the emitter of T_{18}.

The capacitor C_1 is used to provide a high initial base current from T_{20}. This causes T_{20} to saturate faster than it would with the steady-state base current.

The heavy initial current would tend to cause T_{21} to saturate if the carry line could reach a low enough voltage level. This condition is undesirable, as it lowers the collector impedance of T_{21} and causes a carry

propagating down the line to be delayed until T_{21} can be pulled out of saturation. Diode D_7 clamps the carry line at some voltage level higher than that required to allow T_{21} to saturate, thus preventing T_{21} from saturating. D_7 also offers a low impedance current path for the initial surge caused by C_1.

Resistor R_{17} provides a current path for the current leaking through T_{20} from collector to emitter. This leakage occurs when T_{21} is not taking current from T_{20}, a carry is being generated by T_{10}, and no carry is being received on the line. These conditions occur if the conditions of line six or line seven of the Adder Truth Table, Table 1, are met. When these conditions are met, the collector of T_{20} may be as much as 3.5 volts more positive than the emitter of T_{20}. With the collector 3.5 volts more positive than the emitter, the collector-base junction is forward biased, and there is some leakage current through the back biased emitter-base junction.

Under these conditions, the transistor is operating in what is called the inverted mode. In this mode, base current flow is from collector to base. A current whose magnitude is equal to the product of the base current and

the inverted transistor beta flows from collector to emitter. The inverted beta is defined by the equation,

$$\text{Beta inverse} = \frac{\Delta I_{\text{emitter}}}{\Delta I_{\text{base}}}$$

Since there is no current flowing through T_{21}, the emitter-base leakage current will be the base current. This leakage current multiplied by one plus beta inverse will flow from the emitter of T_{20}. Without a low impedance path for this reverse conduction current the carry line voltage would rise to levels comparable to those of a carry. R_{17} provides the necessary conduction path.

Transistors T_{28}, T_{29}, T_{30}, and T_{31} and the resistors R_{21}, R_{22}, R_{23}, and R_{24} constitute the sum gates. Transistors T_{32} and T_{33} are the sum inverters. The operand comparison circuit outputs, W and Z, appear at the bases of the sum gates. The incoming carries appear at the emitters.

The sum gates act as current switches and operate in a manner similar to the operation of T_1 and T_2. The gate base current is either used as the sum inverter base

or is shunted to ground by the emitter-followers T_{26} and T_{27}. It is necessary to have both a carry, represented by a positive voltage of 1 or 2 volts on the sum gate emitters, and a signal from the operand comparison circuits, represented by a current to the bases of the sum gates, to turn on the sum inverters.

The sum comparison circuit is shown in Fig. 4 and consists of C_3, C_4, R_{25}, R_{26}, R_{27}, R_{28}, T_{34}, and T_{35}. Under conditions of no sum or of both one and zero sums, the emitters and bases of T_{34} and T_{35} will be at approximately the same voltage level. If one of the emitters is one volt or more below the other, then its base-emitter junction will be forward biased, and the transistor will saturate, thereby pulling down the output.

Base current for T_{34} is provided by R_{25} and R_{28}, and base current for T_{35}, by R_{26} and R_{27}. C_3 and C_4 provide transient current paths to speed up operation of T_{34} and T_{35}. R_{27} and R_{28} provide some isolation between the two sum outputs.

The carry amplifier circuit is shown in Fig. 5. One of these amplifiers is necessary for every 9 carry gates. The amplifier provides both current and voltage gain and

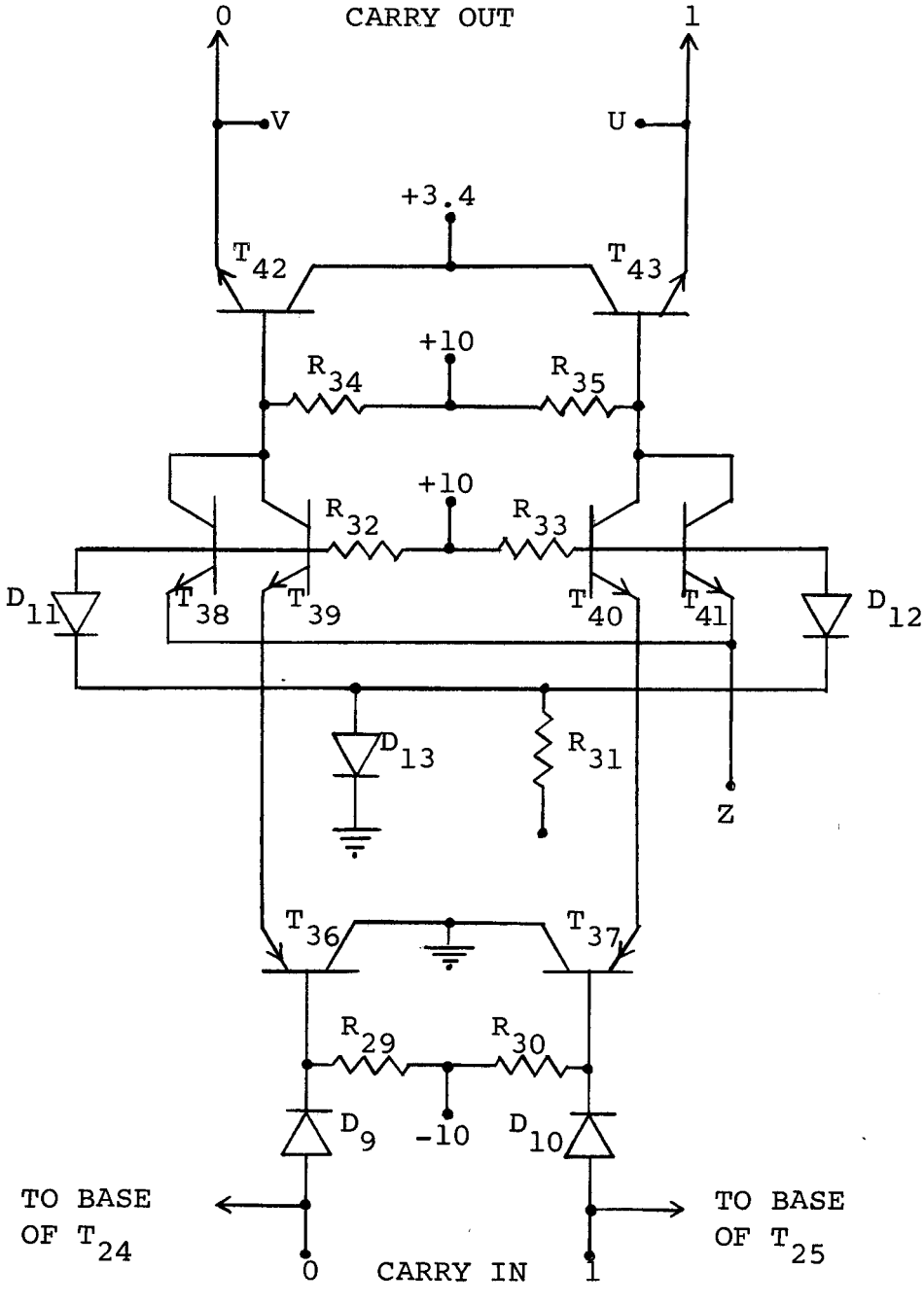


Figure 5. Carry Line Amplifiers

is shown connected as a gated amplifier. This allows one amplifier to be used in every tenth bit position.

Diode D_9 gives a voltage level shift which allows T_{36} to saturate. Base current for T_{36} is provided by R_{29}. T_{36} is a current amplifier, used to establish an input voltage level and to provide sufficient current for operation of the amplifier without heavily loading the carry line.

Transistor T_{39} is a grounded base voltage amplifier. When T_{36} is saturated, T_{39} is also saturated and the emitter voltage of T_{42} is low enough to be clamped by diode D_7 of Fig. 4. When the emitter voltage of T_{36} is raised to about +1 volt, the base current of T_{39} is shifted to the clamp diode D_{11}. When this happens, R_{34} pulls the collector of T_{39} and the base of T_{42} up until T_{42} saturates. The current necessary to drive a carry through nine more gates is then provided by T_{42}. R_{31} and D_{13} establish a clamping voltage for clamp diode D_{11}.

Gating is accomplished by placing the base and collector of T_{38} in parallel with those of T_{39}. It is then necessary to raise the emitters of both T_{38} and T_{39} to about +1 volt to obtain an output from T_{42}. The gating

transistors are controlled by the operand comparison circuits, as were the carry gates.

Worst Case Design

A worst case design procedure was used to assure circuit operation under all forseeable variations of circuit parameters. If circuit component parameters stay within the specified limits, the circuit is guaranteed to work.

Worst case design techniques produce a more conservative circuit design than the statistical design techniques that are sometimes used. Statistical design methods would have been difficult to use in this case because knowledge of the component parameter distributions was unobtainable.

Component tolerances were obtained from two sources, manufacturers literature and component tests. The tolerances are those which were established for use in all of the Galaxy circuit designs. The component tests were performed by members of the Galaxy group.

All of the resistors used in the adder are $\pm$ 5%, 1/4 watt, hot molded carbon. An additional variation of

± 5% must be added to the initial variation to allow for thermal changes and changes due to aging. This results in a resistor tolerance of ± 10%. To stay within this tolerance, the resistors must be operated well within their voltage and power ratings.

The capacitors used in the circuits are ceramic disc types with tolerances of ± 20%. The capacitor values used in the adder are not critical. The values were determined by experimentation rather than calculation.

Transistor and diode parameter variations were obtained from manufacturers specifications and from extensive tests. A minimum current gain of ten was assumed for most of the saturating silicon transistors. Other current gains used were 20 and 40 for non-saturating silicon emitter-followers and 10 and 40 respectively for saturating and non-saturating germanium transistors. The carry gates have a variable minimum current gain depending on how many gates are turned on at one time. Current gains of up to 40 were allowed.

Leakage currents have been ignored in most of the circuits. This is possible because of the silicon transistors used, because of the limited temperature range,

and because most of the current levels are high and impedances are low. The only place that leakage is a problem is in the carry gates, where germanium transistors are used. Adequate compensation is made for this current, however.

Because this adder is part of what amounts to a laboratory instrument, the temperature variations expected are rather small. The effects of temperature are included as part of the component tolerances. Operation is assured over a range of 25^{o} to 50^{o} centigrade.

Operating Speeds

In addition to one bit in breadboard form, three bits of the adder were constructed in the final form used in the Galaxy computer. The following speed tests were run on these three bits.

A number of tests were necessary to determine completely the characteristics of the adder. In all of the following photographs of oscilloscope traces, the horizontal calibration is 5 ns per division. The vertical scale is 1 volt per division. All photos were taken with a Tektronix type C-12 camera from a Tektronix RM43

oscilloscope. A Type N plug in unit with an active probe was used for the measurements. The rise time of the measuring system was less than 1 ns.

Fig. 6 shows the operating time of the operand comparison circuits and the carry generator. The first operand was present before the test started. The lower trace is the output of one carry line. In this test two like operands were used, so a carry was generated and the carry gates remained inactivated.

This test gives two significant results. First, it shows that if a carry is being generated, it will be on the carry line some 12 or 13 ns after the operands enter the adder. Second, this is also the time at which the signal from the operand comparison circuits reaches the sum gates.

Fig. 7 shows the operating time of the sum gates and the sum inverters. The upper trace shows a carry entering one bit. The lower trace is the sum output of the bit. Due to the nature of the sum gates, nearly all of the delay is due to the inverter. The delay in this case was about 5 ns. For this test, the two operands were present before the carry arrived.

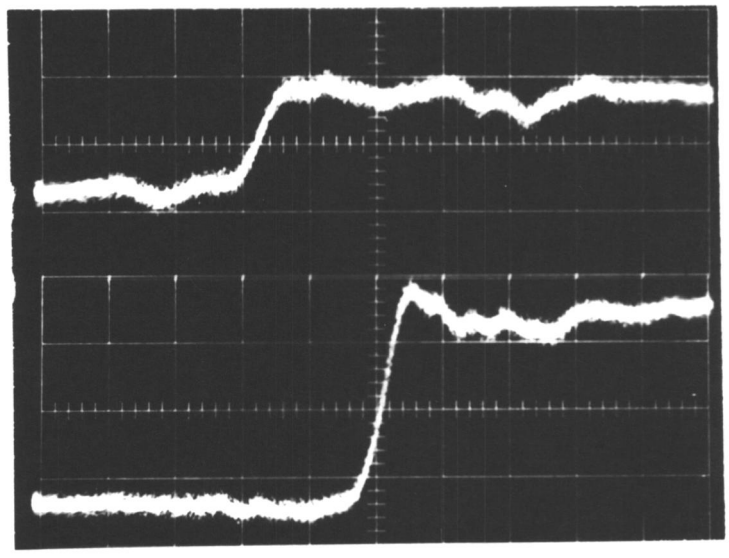


Figure 6. Carry Generation Delay

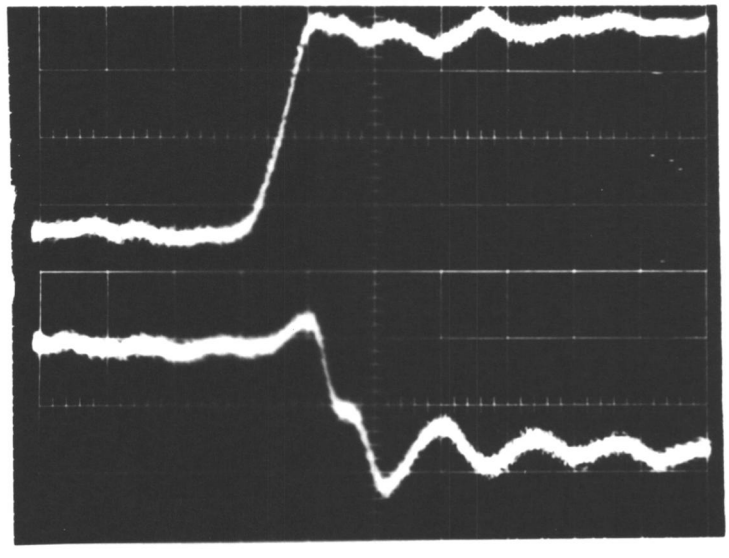


Figure 7. Sum Formation Delay

Because the sum gates do not contribute appreciably to the circuit delay, it makes little difference whether the second signal to reach them is the one that appears on the gate emitters or the one that appears on the bases. The upper trace could just as well have been the signal from the operand comparison circuits. The sum is present at the output of the adder 5 ns after the second of these two signals arrives.

The operating delay time of one bit is therefore the sum of the delays of Figs. 6 and 7. This assumes that the carry is present before the signal from the operand comparison circuits. This delay is 13 to 15 ns.

Another time delay that is of interest is the time required to operate the carry gates. This delay is shown in Fig. 8. In this test the incoming carry and the first operand were present before the second operand. The operands were unequal, so the carry gates were set.

The upper trace shows the second operand entering the adder. The lower trace shows the carry out of the bit. The lengthy delay is caused by the carry gate. It is not so fast a transistor as the NPN types used elsewhere. The delay is between 20 and 25 ns. The small

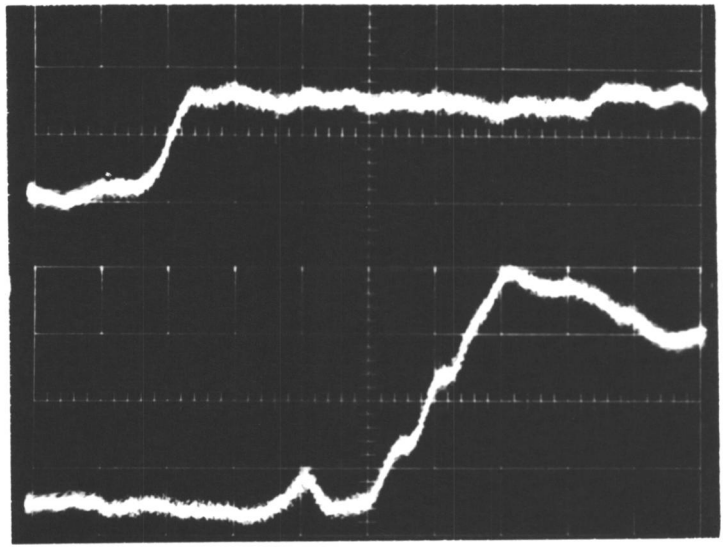


Figure 8. Carry Gate Operating Delay

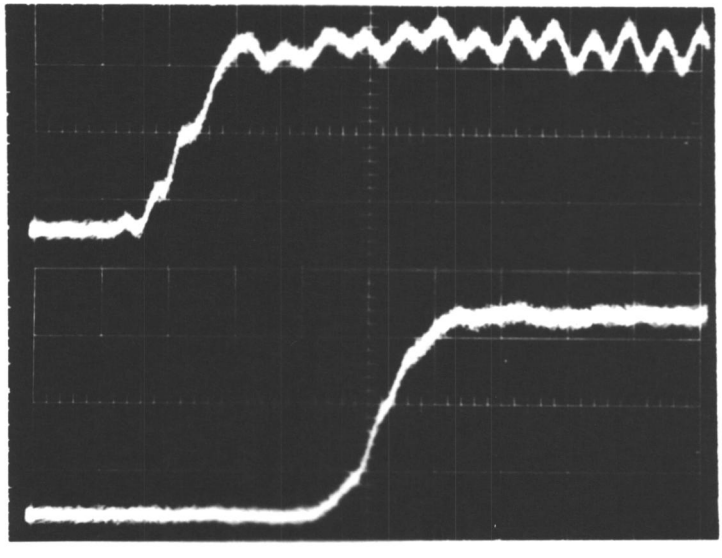


Figure 9. Delay of a 10 Bit Carry Line

peak which occurs 10 ns after the input is due to a carry being generated in the next bit. The generated carry is capacitively coupled through the carry gate of that bit, even though it is not turned on. This signal is not large enough to give a sum output, however.

Because only three bits of the adder were finished, it was impossible to obtain measurements of the carry line delay from them. A ten bit carry line was constructed for this purpose. The line was operated by a pulse generator.

The line consisted of nine carry gates and one gated carry amplifier. Realistic input signals were obtained by placing a second gated amplifier at the front end of the line. The line was built with all of the resistors, diodes, and emitter-followers shown connected to it in Fig. 4. This was done to make this as realistic a test as possible.

The delay time as shown in Fig. 9 is about 15 ns. Of this time, 10 ns is due to the gate delay and 5 ns to the amplifier. The upper trace is the signal into the first of the nine gates. The ripple on the upper part of the trace is due to an oscillating emitter-follower. The emitter-followers used in the adder tend to oscillate

when they are operated with very long leads, as they were in this test. This oscillation can be suppressed by using additional capacitors and shortening lead lengths. The lower trace is the output of the amplifier.

The actual delay time of the amplifier is shown in Fig. 10. The upper trace is the carry at the output of the ninth gate, and the lower trace is the output of the amplifier. The delay is about 5 ns.

As can be seen, the amplifier re-shapes the carry signal. The re-shaping takes place when the amplifier gating transistor T_{39} (Fig. 5) is clamped and turned off. This clamping action makes the shape of the amplifier output signal almost entirely independent of the shape of the input signal.

Using the delay times presented, it is now possible to predict some operating times for the complete adder. Three operating times are pertinent. These are the minimum, average, and maximum add times.

The minimum add time occurs when each bit has operand inputs that are equal to each other. When this condition occurs, no carry gates are operated, and a carry is generated in each bit position.

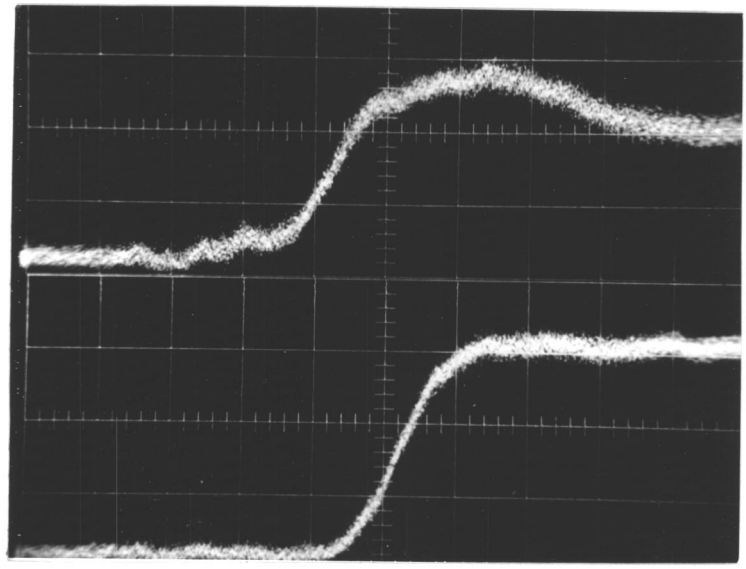


Figure 10. **Carry Amplifier Delay**

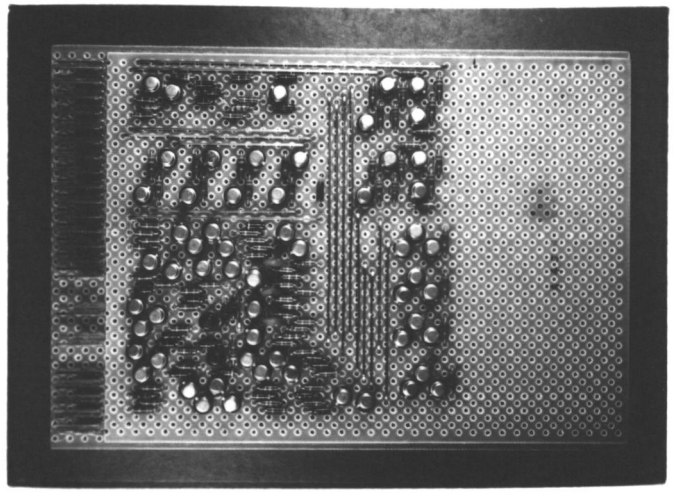


Figure 11. **Adder Circuit Card**

The maximum add time occurs when the operands are unequal in each bit position. This results in a carry propagation as long as the adder.

The average add time is the result of numerous short carries, the longest being the one defined in the section on the average maximum carry length.

The following discussion assumes that the second operand to arrive enters all bits simultaneously, and that a carry is always present at the input to the least significant bit position.

The minimum add time is almost identical to the time shown in Figs. 6 and 7. In this case, the sum gates receive both of their inputs almost simultaneously. The total add time would be about 15 ns.

The maximum add time would include the following delays. The operand comparison circuit and carry gate operating delay shown in Fig. 8, four times the delay for nine gates and one amplifier, shown in Fig. 9, the delay of nine gates obtained from Figs. 9 and 10, and the delay of the sum inverter, shown in Fig. 7. As listed, these delays are 20 ns, 60 ns, 10 ns, and 5 ns, or a total of 95 ns.

The carry gate operating delay is included for only one bit because it is assumed that all of the gates will be turned on simultaneously. Similarly, the sum inverter delay is included only for the bit which receives its carry last.

The average add time also includes the delays required to set carry gates and to form the sum after the carry has arrived, but the carry line propagation delay is different from the delay of the maximum case. Using the formula given earlier for the average maximum length carry, it is found that for a 49 bit adder, the average maximum carry length is about six bits. This gives a carry line delay of about 6 ns.

There is also an amplifier delay, because six of each ten six bit carries will pass through amplifiers. When the longest carry does not pass through an amplifier, there is still the possibility that a shorter carry will pass through an amplifier, so the full 5 ns delay is added to the above time to obtain the average add time. The resulting add time is about 26 ns.

These three add times are the operating times of the adder circuit alone. They do not consider the time

required to get the operands to the adder and to get the sum from the adder to a storage register. These delays must be added to the times given previously to obtain what is known as a hardware add time.

The added delay times for the other circuits involved have been found to total about 40 ns. This results in a minimum add time of 55 ns, a maximum add time of 135 ns, and an average add time of 66 ns.

Comparison of Add Times

By using the operating times given in the last section it is possible to compare the add time of the Galaxy Fast Carry Adder with the add times of the adders presented earlier. To do this, it is necessary to find the add times of Galaxy type adders with as many bit positions as the previous adders.

Kilburn, Edwards, and Aspinal reported an add time of 200 ns for a 20 bit adder (4, p. 573-584). This was a maximum add time, and included the time required to get the operands to the adder and store the sum in a register. A Galaxy type adder would do the same operation in 100 ns.

Salter obtained an add time of 230 ns for a 68 bit

adder (9). This time was for a maximum length carry, but did not include the time required to get the operands to the adder or to store the sum. A similar Galaxy type adder would require 123 ns.

Gilchrist, Pomerene, and Wong reported an average add time for 40 bits of 360 ns (2). This included all of the external circuit delays. The average add time of a 40 bit Galaxy type adder would be about 65 ns.

THE USE OF THE ADDER IN THE GALAXY COMPUTER

Adder Locations

The Fast Carry Adder circuit appears in several places in the Galaxy computer. There are four separate adders in the Galaxy computer.

The arithmetic unit contains a 49 bit adder and a nine bit adder. These adders are used in the arithmetic operations.

The memory address calculation unit also contains two adders. One of these has 15 bits, the other, four. The 15 bit adder is used in the calculation of memory addresses and, in conjunction with certain registers, to

form a counter. The four bit adder is used to modify the address given to the memory control system.

Packaging

The adders used in the Galaxy computer utilize the same construction techniques used for the other parts of the computer. The circuits are constructed on pre-punched glass-epoxy cards, 5 1/2" high and 8" long. The cards have 51 connector pins which are located along one 5 1/2" edge. Twenty seven cards are held upright in a rack which occupies 7 1/2" of space in a standard 19" relay rack.

The components are cemented to one side of the card with epoxy cement. Connections between the components are made by welding interconnecting leads to the component leads, which protrude from the back of the card. Teflon sleeving is used to prevent contact between leads which must cross each other.

There are two adder card layouts. One layout contains one adder bit and two register toggles. The two register toggles are ones which are permanently connected to the adder. The other layout contains two adder bits

on one card. With this layout, it is possible to place the 49 bit adder and all of the external control circuits required in one 27-card card rack.

A photograph of the one bit layout is shown in Fig. 11. This card contains 62 transistors, 21 diodes, and 76 resistors. Notice that much of the rear portion of the card is not used. The second card layout (not pictured) contains 110 transistors, 105 resistors, and 22 diodes.

Compact design such as this reduces lead lengths and lowers wiring capacitance. This contributes significantly to increasing the speed of the circuits.

SUMMARY

The need for a faster more reliable adder is the result of two factors, greater problem volume and greater problem complexity. Although the previous adders discussed were fast, they were neither as fast nor as reliable as the adder presented herein.

The main design concepts (the double rail system, asychronism, the fast carry line) are not new. The way in which these concepts are used is new. The manner in

which the add end signal is generated is unique with this adder, although the circuit used for this purpose was used in another way in one of the adders described earlier.

The circuits used are well adapted to the transistors used. The increase in speed of this adder is due partly to the transistor current switch technique and partly to faster transistors. The inherent reliability of the logical design is enhanced by the use of worst case design techniques.

The packaging technique also plays an important roll in the speed of the adder. Every effort is made to keep leads as short as possible and to minimize stray capacitances.

The circuit described is for one bit position, with or without carry amplifiers. There is no limit to the number of bits that can be used, as long as every tenth one is an amplifier bit.

BIBLIOGRAPHY

1. Burkes, Arthur W., Herman H. Goldstine and John vonNeumann. Preliminary discussion of the logical design of an electronic computing instrument. Washington, Dept. of Commerce, 1946. 53 p. (Report prepared with terms of contract W-26-034-ORD-7481 between the Research and Development Service, Ordinance Dept., U. S. Army and the Institute for Advanced Study)

2. Gilchrist, Bruce, J. H. Pomerene and S. Y. Wong. Fast carry logic for digital computers. Institute of Radio Engineers Transactions on Electronic Computers EC-4:133-136. 1955.

3. Hendrickson, Herbert C. Fast high-accuracy binary parallel addition. Institute of Radio Engineers Transactions on Electronic Computers EC-9:465-468. 1960.

4. Kilburn, T., D. B. G. Edwards and D. Aspinall. A parallel arithmetic unit using a saturated-transistor fast-carry circuit. The Proceedings of the Institution of Electrical Engineers 107:573-584. 1960.

5. Phillips, J. Richard. A logical design for an asynchronous parallel adder. Corvallis, Department of Mathematics, Oregon State University, August 18, 1961. 13 numb. leaves.

6. Pressman, Abraham I. Design of transistorized circuits for digital computers. New York, Rider, 1959. 310 p.

7. Reitwiesner, George W. The determination of carry propagation length for binary addition. Institute of Radio Engineers Transactions on Electronic Computers EC-9:35-38. 1960.

8. Ruegg, H. W. and R. H. Beeson. New forms of all transistor logic. Mt. View, California, Fairchild

Semiconductor, 1961. 12 p. (Technical articles and papers TP-21)

9. Salter, Forrest. High-speed transistorized adder for a digital computer. Institute of Radio Engineers Transactions on Electronic Computers EC-9: 461-464. 1960.

APPENDICES

Worst Case Design Calculations

The part numbers in the following calculations refer to those in the adder circuit diagram, Figs. 4, 5, and 6. The part numbers appear as subscripts to the symbols listed below.

The symbols used and their meanings are as follows:

V_{BE} Transistor base to emitter saturation voltage

V_{CE} Transistor collector to emitter saturation voltage

V_{BC} Transistor base to collector saturation voltage

V_D Diode forward voltage drop

V_R Resistor voltage drop

I_B Transistor base current

I_C Transistor collector current

I_E Transistor emitter current

I_D Diode forward current

I_R Resistor current

E_1 +10V power supply voltage

E_2 +3.4V power supply voltage

E_3 -10V power supply voltage

E_4 -1V power supply voltage

E_5 -4V power supply voltage

A line over a parameter indicates that the value is a maximum. A line under a parameter indicates a minimum.

The following tolerances are used:

Power supply - $\pm$ 5% or $\pm$ 100mv, whichever is larger

Resistors - $\pm$10%

Diodes and transistors - values depend on current levels and type of device. Values given come from test data obtained by the Galaxy group.

In the following calculations, the resistor whose value is being determined will be listed, followed by the figure number in which the resistor is located. Resistors from other identical circuits will be indicated following the figure number.

Figures 3, 4, and 5 form a complete schematic diagram of one adder bit. Although the resistor whose value is being found is located in the indicated figure, the parameters used in the calculations may apply to components in one of the other two figures.

1. R_{21} (Fig. 4) R_{22}, R_{23}, R_{24}

Let $\underline{I_{B32}} = 2ma$

$$\overline{R_{21}} = (\underline{E_2}+\underline{V_{CB9}}-\overline{V_{D1}}-\overline{V_{BE11}}-\overline{V_{CB28}}-\overline{V_{BE32}})/\underline{I_{B32}} \text{ ohms} \quad (1)$$

$= (3.23+0.55-0.33-0.8-0.7-0.85)/2 = 550$ ohms

$R_{21} = 470$ ohms

2. R_{19} (Fig. 4) R_{20}

$$\overline{I_{E28}} = (\overline{E_2}+\overline{V_{BC9}}-\underline{V_{D1}}-\underline{V_{BE11}}-\underline{V_{BC28}}-\underline{V_{BE32}})/\underline{R_{21}}\text{ma} \quad (2)$$

$= (3.57+0.7-0.2-0.65-0.57)/423 = 6.43$ma

$$\overline{I_{E26}} = 2\overline{I_{E28}} = 12.86\text{ma} \quad (3)$$

$$\overline{I_{B26}} = \overline{I_{E26}}/10 = 1.29\text{ma} \quad (4)$$

$$\overline{R_{19}} = (-\overline{E_3} - \overline{V_{BE26}})/\overline{I_{B26}} \text{ ohms} \quad (5)$$

$= (9.5-0.4)/1.29 = 7.05$ k ohms

$R_{19} = 6.2$ k ohms

3. R_{11} = (Fig. 3) R_{12}

Let $I_{E20} = 1$ma

$$\overline{R_{11}} = (-\overline{E_5}-\overline{V_{CE18}}+\underline{E_4}-\overline{V_{BE21}})/\underline{I_{E21}} \text{ ohms} \quad (6)$$

$= (3.8-0.1-1.1-0.75)/1.05 = 1.76$ k ohms

$R_{11} = 1.6$ k ohms

4. R_{10} (Fig. 3)

$$\overline{R_{10}} = (\underline{E_5} - \overline{E_3} - \overline{V_{BC18}})/I_{R10} \text{ ohms} \quad (7)$$

$$= (-4.2+9.5-0.35)/1.33 = 3.72 \text{ k ohms}$$

$$R_{10} = 3.3 \text{ k ohms}$$

5. R_9 (Fig. 3)

$$\overline{R_9} = (\underline{E_1} - \overline{V_{D3}} - \overline{V_{B18}})/\overline{I_{R10}} \text{ ohms} \quad (8)$$

$$= (9.5-5.8+1)/2.86 = 1.65 \text{ k ohms}$$

$$R_9 = 1.5 \text{ k ohms}$$

6. R_{15} (Fig. 3)

R_{15} must supply base current to T_{29} and T_{30}. It was shown (calculation 1) that to do this, the voltage at Z must be at least 2.65 volts. Denote the voltage at Z by E_Z, and the maximum current through R_{22} when E_Z = 2.65 volts by I_{R22}*.

$$R_{15} = (E_1 - E_Z)/2I_{R22}^* \text{ ohms} \quad (9)$$

$$= (9.5-2.65)/7.08 = 970 \text{ ohms}$$

$$R_{15} = 820 \text{ ohms}$$

7. R_{16} (Fig. 3)

$$\underline{R_{16}} = (\underline{-E_3}+\overline{V_{BE19}})/\overline{I_{R16}} \text{ ohms} \quad (10)$$

$$= (10.5+0.9)/1 = 11.4 \text{ k ohms}$$

$$R_{16} = 13 \text{ k ohms}$$

8. R_{14} (Fig. 3)

$$\overline{R_{14}} = (\underline{E_1}-\overline{V_{D5}}-\overline{V_{BE19}})/(\overline{I_{R16}}+\overline{I_{B19}}) \text{ ohms} \quad (11)$$

$$= (9.5-0.78-0.9)/(1+1.41) = 3.2 \text{ k ohms}$$

$$R_{14} = 3 \text{ k ohms}$$

9. R_7 (Fig. 3)

$$\underline{R_7} = (\underline{-E_3}+\overline{E_2}+\overline{V_{BC9}}-\underline{V_{D1}})/\overline{I_{R7}} \text{ ohms} \quad (12)$$

$$= (10.5+3.57+0.7-0.2)/0.3 = 48.6 \text{ k ohms}$$

$$R_7 = 56 \text{ k ohms}$$

10. R_3 (Fig. 3) R_6

$$\overline{R_3} = (\underline{E_1}-\overline{E_2}-\overline{V_{CB9}})/(\underline{I_{B9}}+\underline{I_{D1}}) \text{ ohms} \quad (13)$$

$$= (9.5-3.57-0.7)/(4+0.63) = 1.13 \text{ k ohms}$$

$$R_3 = 1 \text{ k ohms}$$

11. R_2 (Fig. 3) R_5

$$\overline{R_2} = (\underline{E_2} - \overline{V_{BE14}})/I_{B4} \text{ ohms} \quad (14)$$

$$= (3.23-0.85)/1.5 = 1.59 \text{ k ohms}$$

$$R_2 = 1.3 \text{ k ohms}$$

12. R_1 (Fig. 3) R_4, R_8, R_{13}

$$R_1 = (\underline{E_2} - \overline{V_{BE3}} - \overline{V_{BC1}})/\underline{I_{B3}} \text{ ohms} \quad (15)$$

$$= (3.23-0.85-0.65)/1.5 = 1.15 \text{ k ohms}$$

$$R_1 = 1 \text{ k ohms}$$

13. R_{27} (Fig. 4) R_{28}

$$\overline{R_{27}} = (V_{C33} - \overline{V_{BE35}} - \overline{V_{CE32}})/\underline{I_{B35}} \text{ ohms} \quad (15)$$

$$= (2-.85-.2)/2 = 475 \text{ ohms}$$

$$R_{27} = 430 \text{ ohms}$$

14. R_{26} (Fig. 4) R_{25}

$$\overline{R_{26}} = (\underline{E_2} - V_{C33})/\underline{I_{B35}} \text{ ohms} \quad (16)$$

$$= (3.23-2)/2 = 615 \text{ ohms}$$

$$R_{26} = 560 \text{ ohms}$$

15. R_{34} (Fig. 5) R_{35}

$$\overline{R_{34}} = (E_1 - \overline{E_2} - \overline{V_{BE42}})/\underline{I_{B42}} \text{ ohms} \quad (17)$$

$$= (9.5-3.57-0.65)/4.5 = 1.17 \text{ k ohms}$$

R_{34} = 1 k ohms

16. R_{32} (Fig. 5) R_{33}

$$\overline{R_{32}} = (\underline{E_1} - \overline{V_{CE36}} - \overline{V_{BE39}})/\underline{I_{B39}} \text{ ohms} \quad (18)$$

$$= (9.5-0.11-0.86)/1.14 = 7.5 \text{ k ohms}$$

R_{32} = 6.8 k ohms

17. R_{31} (Fig. 5)

$$\underline{R_{31}} = (\underline{E_1} - \overline{V_{D13}})/\underline{I_{R31}} \text{ ohms} \quad (19)$$

$$= (9.5-0.65)/10.5 = 840 \text{ ohms}$$

R_{31} = 750 ohms

18. R_{29} (Fig. 5) R_{30}, R_{17}, R_{18}

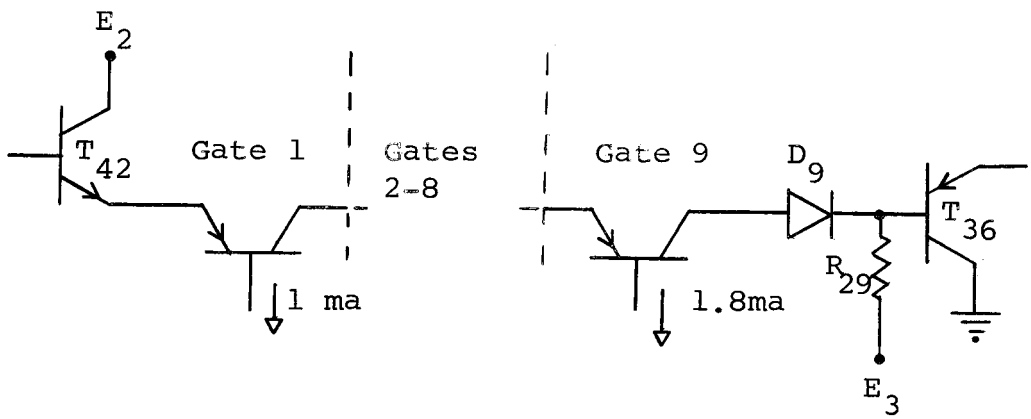
The value of R_{29} was chosen to be as small as could be tolerated from a loading standpoint. This value was chosen to be 7.5 k ohms.

19. The values of C_1, C_2, C_3, and C_4 were determined by

experimentation. See the parts list for values.

After a number of calculations, the following values were found to represent the lowest combination of voltages along a carry line nine gates long. This is the largest number of gates between amplifiers.

Gate #	I_{Cma}	I_{bma}	$V_{CE\ mv}$	V_C volts
1	31.9	1.0	191	2.769
2	28.14	1.0	180	2.589
3	24.92	1.0	168	2.421
4	21.72	1.0	156	2.265
5	17.74	1.8	133	2.132
6	13.78	1.8	115	2.017
7	9.84	1.8	103	1.914
8	5.91	1.8	84	1.830
9	2.00	1.8	57	1.773



V_{E42} = 2.96v

V_{B36} = 1.373v

Fig. 12. Nine Gate Carry Line

Each gate station consists of all of the components shown for one carry line, Fig. 4. I_{42} and D_9 belong to different amplifiers, each as shown in Fig. 5.

APPENDIX II

Parts List for Figures 4, 5, and 6

R_1, R_3, R_4, R_6, R_8, R_{13}, R_{34}, R_{35}	= 1 k ohm
R_2, R_5	= 1.3 k ohm
R_7	= 56 k ohm
R_9	= 1.5 k ohm
R_{10}	= 3.3 k ohm
R_{11}, R_{12}	= 1.6 k ohm
R_{14}	= 3 k ohm
R_{15}	= 820 ohm
R_{16}	= 13 k ohm
R_{17}, R_{18}, R_{29}, R_{30}	= 7.5 k ohm
R_{19}, R_{20}	= 6.2 k ohm
R_{21}, R_{22}, R_{23}, R_{24}	= 470 ohm
R_{25}, R_{26}	= 560 ohm
R_{27}, R_{28}	= 430 ohm
R_{31}	= 750 ohm
R_{32}, R_{33}	= 6.8 k ohm

All resistors are 1/4 watt

C_1, C_2	= 20 pf
C_3, C_4	= 50 pf

T_1, T_2, T_3, T_4, T_5, T_6, T_7, T_8, T_9, T_{10}, T_{11}, T_{12}, T_{13}, T_{14}, T_{15}, T_{16}, T_{17}, T_{19}, T_{28}, T_{29}, T_{30}, T_{31}, T_{33}, T_{34}, T_{35}, T_{42}, T_{43} = Fairchild S5448

T_{18}, T_{20}, T_{26}, T_{27}, T_{36}, T_{37} = Motorola 2N965

T_{21}, T_{22}, T_{24}, T_{25}, T_{38}, T_{39}, T_{40}, T_{41} = Fairchild 2N709

D_1, D_2, D_7, D_8, D_9, D_{10} = Clevite CDG 1030

D_3 = Motorola ¼M5.1AZ10

D_4, D_6, D_{11}, D_{12} = Fairchild FDG 1171A

D_5, D_{13} = Clevite 1N816