AN ABSTRACT OF THE THESIS OF

Sumit A. Talwalkar for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on May 21, 2013.

Title: Modeling and Analysis of Spur Structure of Digital-to-Time Conversion Based Frequency Synthesizers.

Abstract approved:

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S. Lawrence Marple, Jr.

Frequency synthesizers are critical components of all communication systems. This thesis considers the issue of undesirable frequency spurs of a relatively recent type of frequency synthesis architecture called digital-to-time conversion (DTC). The DTC-based frequency synthesis architecture has important performance benefits over older frequency synthesizers, such as fast frequency switching, large frequency range and fine frequency resolution. A DTC-based frequency synthesizer requires less power than a traditional direct synthesis based synthesizer with comparable frequency range, resolution and switching time. The DTC architecture is also easily scalable to newer low-cost digital complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) fabrication technologies. However, the DTC architecture suffers from an important undesirable characteristic: sub-harmonic spurious tones, hereafter, referred to as spurs. Spurs have undesirable effects in both the transmitter and the receiver. In a transmitter, spurs create an out-of-band emission of power that may breach the spectral emission mask set by regulatory agencies to enable co-existence of multiple transmitters in a crowded frequency spectrum. In a receiver, an inopportune-located spur in the local oscillator (LO) signal can mix an out-of-band strong interfering signal into the baseband on top of a mixed-down weak desirable signal. Unlike harmonic spurs that are known to be at multiples of the carrier frequency, sub-harmonic spurs

are especially problematic as they have been difficult to predict as part of the design process. In fact, the spur patterns for most pairs of closely placed desired output frequencies for a DTC-based frequency synthesizer are seemingly unrelated. While one output frequency setting might have an output spectrum with only a few spurs, many other close-by output frequency settings might have output spectra with many weaker spurs.

The primary contribution of this thesis is the development of spur creation models and analysis tools that can predict spur spectrum and spur power levels for a DTC-based frequency synthesizer. This is an important contribution for assuring achievable performance of frequency synthesizer during the design process. The modeling approach has been successful in accounting of more than 99% of spur spectral locations. Predicted power levels for more than 95% are within 10 dB of actual fabricated DTC-based frequency synthesizer ICs. The results developed in this thesis allow for an understanding of the relationship between spur patterns for different selected output frequencies.

In the research reported in this thesis, the spur spectrum for a selected output frequency is shown to be due to periodic occurrences of errors in the locations of rising and falling edges of the output signal. Error sequences for different selected output frequencies are shown to be related in a way that can be exploited by application of the axis-scaling property of the Discrete Fourier Transform (DFT). The axis-scaling property of the DFT relates the transforms of two sets of sequences that are predictably permutated versions of each other. Their respective transforms are also (differently) permutated versions of each other. One key insight made in this thesis is the discovery that the time-domain errors for *all* output frequencies can be classified into a very small number of error sequence classes. All error sequences within a class are shown to be predictable permutations of each other. This insight along with the DFT axis-scaling property permits the respective spur spectra to be classified into error spectra classes. All error spectra within a spur spectra class are predictable permutations of each other. There are two sources of edge errors: quantization error

and buffer delay errors. This classification of spur spectra to a few classes is shown to be possible for both sources of errors. In this thesis, the case of quantization-only error is considered first. The analysis is then extended to the case when both sources of error are present.

As a result of the modeling and analytical techniques developed for spur spectra classification described in this thesis, design tools have been created to predict the spur spectra of DTC-based synthesizer designs for all possible selected output frequencies.

Modeling and Analysis of Spur Structure of Digital-to-Time Conversion Based Frequency Synthesizers

by
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Sumit A. Talwalkar, Author

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CONTRIBUTION OF AUTHORS

My advisor, Dr. S. Lawrence Marple, Jr. co-authored the conference paper that constitutes Chapter2.

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DEDICATION

Lovingly dedicated to the Preceptor of the Universe

Modeling and Analysis of Spur Structure of Digital-to-Time Conversion Based Frequency Synthesizers

1 Introduction and Overview

Frequency synthesizers are critical components of all communication systems. A frequency synthesizer generates the local oscillator (LO) signal used by mixers to up-convert a baseband signal in a transmitter and down-convert the RF signal to baseband in a receiver. Synthesizers also supply the clock signal that runs the digital systems.

There are two types of frequency synthesizer architectures: indirect and direct. The indirect architecture has a feedback loop such as a phase locked loop (PLL). Traditional direct frequency synthesis uses a phase counter, a sine look-up table and a digital-to-analog (DAC) converter. This thesis considers the issue of undesirable frequency spurs of a relatively recent type of direct frequency synthesis architecture called digital-to-time conversion (DTC). The DTC-based frequency synthesis architecture has important performance benefits over older frequency synthesizers, such as fast frequency switching, large frequency range and high frequency resolution. A DTC-based frequency synthesizer requires less power than a traditional direct synthesis based synthesizer with comparable frequency range, resolution and switching time. The DTC architecture is also easily scalable to newer low-cost digital complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) fabrication technologies. However, the DTC architecture suffers from an important undesirable characteristic: sub-harmonic spurious tones hereafter referred as spurs. Spurs have undesirable effects in both the transmitter and the receiver. For a transmitter, spurs create an out-of-band emission of power that may breach the spectral emission mask set by regulatory agencies to enable co-existence of multiple transmitters in a crowded frequency spectrum. In a receiver, an inopportune located spur in the LO signal can mix an out-of-band strong interfering signal into the baseband on top of a mixed-down weak desirable signal. Unlike harmonic spurs that are known to be at multiples of the carrier frequency, sub-harmonic spurs are especially problematic as they have been difficult to predict as part of the design process. In fact, the spur patterns for most pairs of closely placed settings of output frequency for a DTC-based frequency synthesizer are seemingly unrelated. The DTC synthesizer output

frequency selected output frequency is controlled by a digital word. The control words for neighboring output frequencies differ from each other by as little as one least significant bit (LSB). It is quite possible to find a setting of output frequency that has a few spurs in its output spectrum whereas the neighboring setting of output frequency differing by only the LSB has a spectrum with more spurs.

In the research reported in this thesis, the spur spectrum for a selected output frequency is due to periodic occurrences of errors in the locations of rising and falling edges of the output signal. Error sequences for different selected output frequencies are shown to be related in a way that can be exploited by application of the axis-scaling property of the Discrete Fourier Transform (DFT). The axis-scaling property of the DFT relates the transforms of two sets of sequences that are predictable permutations of each other. Their respective transforms are also (differently) systematic permutations of each other. One key insight is that the time-domain errors for *all* output frequencies can be classified into a very small number of error sequence classes. All error sequences within a class are shown to be systematically re-arranged (permutated) versions of each other. This insight along with the DFT axis-scaling property permits the respective spur spectra to be classified into a small number of spur spectra classes. All spur spectra within a class are shown to be systematically re-arranged (permutated) and amplitude-scaled versions of each other. There are two sources of edge errors: quantization error and buffer delay errors. This classification of spur spectra to a few error spectra classes is shown to be possible for both sources of errors. In this thesis, the case of quantization errors is considered first. The analysis is then extended to the case when both sources of errors are present.

One may form a set of ‘principal’ error sequences by choosing one member sequence from each of the error sequence classes. For any output frequency setting, the error sequence is guaranteed to be a permutation of exactly one sequence from the principal error sequence set. The idea of ‘principal’ error sequences can be extended to the frequency domain using the DFT axis-scaling property. One may form a set of ‘principal’ spur spectra by choosing one member spur spectrum from each of the spur spectra

classes. Spur spectra related with all output frequency settings are guaranteed to be amplitude-scaled permutations of exactly one spur spectrum from the principal spur spectrum set. The characterization of spur spectra in terms of worst spurs associated with every output frequency can be completely accomplished by considering only the spur spectra in the principal set.

Consider an example of a DTC synthesizer that uses a 32-bit frequency control word. This means that there are 2^{32}, that is, over 4 billion different possible output frequencies. Each of these over 4 billion output frequency settings has an associated spur pattern of undesirable tones that are present in the spectrum in addition to the desired tone. For this synthesizer there is a principal spur spectrum set with only 32 spur spectra. The spur technique developed in this thesis enables the entire set of spur patterns for *any* frequency setting to be completely characterized by this principal set of 32 spur spectra.

An important tool in this analysis is the axis-scaling property of the Discrete Fourier Transform (DFT). This property of the DFT is the analogue of the time-frequency axis-scaling property of continuous-time Fourier Transform. The main contributions of this thesis are:

i) the modeling of the spurs of DTC-based frequency synthesizers that permits the application of the DFT axis-scaling property; and

ii) the recognition that error sequence for every output frequency setting is a permutation of one of a small set of principal error sequences.

1.1 Overview of Frequency Synthesizer Types

The goal of a frequency synthesizer is to generate a desired output frequency signal given a reference input frequency signal and a frequency control word. Important performance metrics of frequency synthesizers include: frequency range, frequency resolution, settling time (when changing the output frequency), spectral purity (spur mitigation) and stability. Also important, especially for mobile communication systems, is the ease of design integration and battery power drain.

Various frequency synthesis methods can be classified in the broad hierarchy according to references [1.1] and [1.2] as shown in Figure 1.1.

Incoherent frequency synthesis is primarily an analog technique and is therefore not found in digital design literature. An example of incoherent frequency synthesis is described in [1.1]. The incoherent frequency synthesis architecture uses multiple reference frequencies (such as multiple crystal oscillators) to generate the desired output frequency (using combination of frequency division, band pass filtering and mixing to generate a desired output frequency).

Digital design literature (see [1.1] – [1.5] for example) focuses only on the coherent frequency synthesis class. The main difference between incoherent and coherent synthesis is the number of frequency references used in the synthesis process. While multiple references are used in the incoherent synthesis approach, only one reference source is used in the coherent synthesis approach.

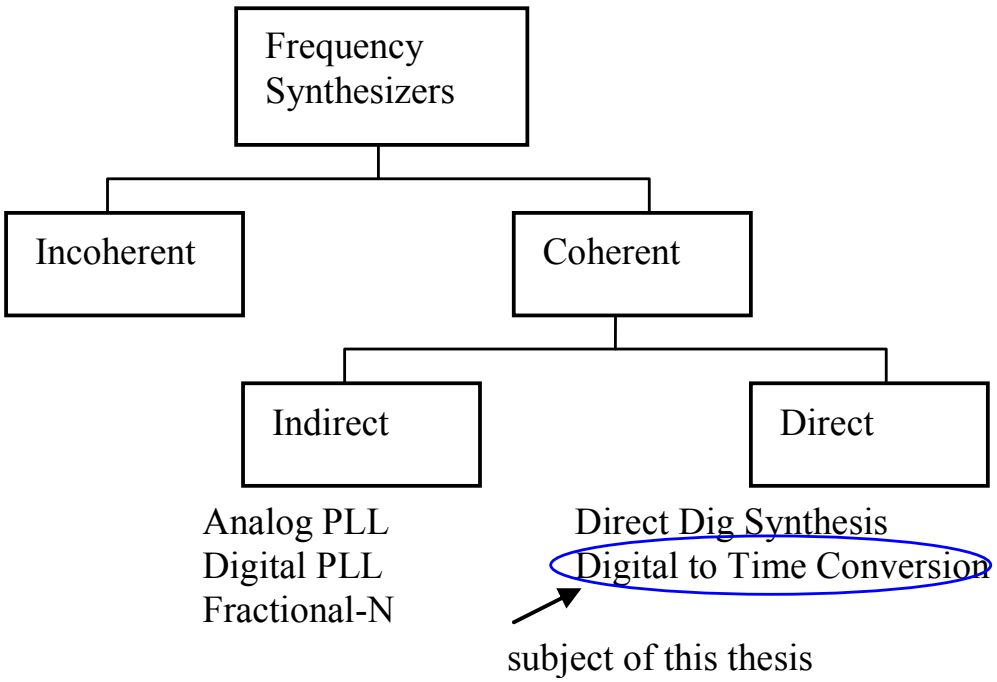

Figure 1.1 Frequency synthesizer types

The class of coherent synthesizers can be further divided into indirect and direct types. Indirect coherent synthesizers typically have a phase locked loop (PLL) architecture. Important components of a PLL include a phase detector, loop filter, a voltage controlled oscillator (VCO) and a frequency divider in the feedback path. The subject of PLL is very mature and has been treated in detail in [1.1], [1.3], and [1.4]. Fractional–*N* synthesizers were designed to overcome the limitation of frequency resolution in an integer-*N* only divider [1.5]. Delta-sigma based fractional–*N* synthesis addresses the noise produced by the switching of the divider values [1.6]. All the components in analog PLLs are implemented in analog circuits. In digital PLLs the phase detector and the loop filter are implemented in digital circuits. A digital VCO (DCO) implements the tuning components of the VCO in discrete values instead of using a continuously variable capacitor (varactor) as used in analog VCOs [1.7]. Recent papers indicate a drive toward all digital PLL (ADPLL) [1.8]. The less expensive and more compact integration available through CMOS technology is the main reason for this drive to all digital implementation. Finally, the class of direct coherent synthesizers includes the basic architecture called direct digital synthesis (DDS) first described in [1.9]. The DDS architecture runs an accumulator that essentially integrates the instantaneous frequency samples to produce the instantaneous phase samples, as shown in Figure 1.2.

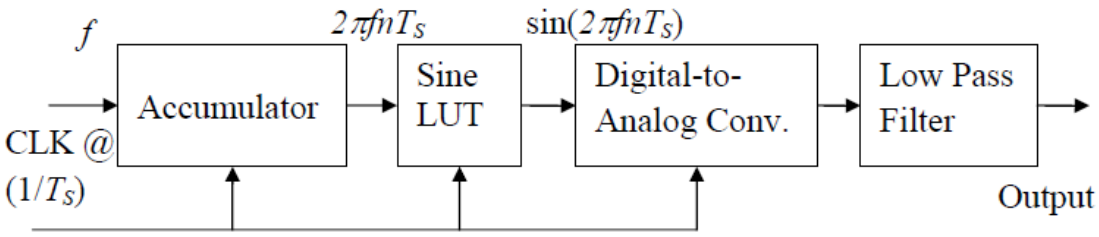

Figure 1.2 Block diagram of a direct digital synthesizer (DDS) as in [1.9]

The phase samples then go through a look up table (LUT) implemented with a read-only memory (ROM) to obtain the sine value of the instantaneous phase. The output

value of the ROM is applied to a digital to analog converter (DAC) to produce the sampled-and-held analog version of the sinusoidal waveform of the desired frequency. The LUT operation generally includes phase truncation (to allow for a practical size LUT). This truncation gives rise to spurious tones in the DDS output. This has been analyzed in [1.10]. Several methods for size reduction, or complete elimination, of the ROM using efficient computation of the sine value have been proposed in [1.11] and [1.12].

1.1.1 Synthesizer Performance Comparison

Table 1.1 provides a subjective performance comparison summarized by the author of this thesis. The comparison is based on the frequency synthesizer architectures from [1.5], [1.15], [1.16], [1.17] and [1.18]. The DDS architecture offers two important advantages over the PLL based methods: fast switching and wide frequency range. The primary drawback of DDS architecture is the higher power consumption by all the digital blocks that operate at a high clock frequency. All PLL based methods allow for a trade-off between signal purity and speed of switching by controlling the bandwidth of the loop filter. Integer-*N* based PLLs have a limited frequency resolution compared to fractional-*N* based PLLs. On the other hand, fractional–*N* based methods suffer from the issue of fractional spurs that are generated due to the modulation of the changing divider ratio. VCOs generally have limited frequency ranges (a maximum of an octave of frequency). This makes all the indirect frequency synthesis approaches limited in their range compared to direct synthesis approaches.

The subject of this thesis, digital-to-time conversion (DTC) architecture, is also a direct synthesis method. The DTC architecture offers the following advantages as that of the DDS architecture: wide frequency range, high precision and extremely fast frequency switching (within few cycles of the output frequency). In addition, it overcomes the important limitation of the higher power drain of a DDS system. DTC architecture also offers simplified integration since most of the design can be easily integrated in a standard digital CMOS process. With newer silicon fabrication technologies, the supply

voltages are reduced as the devices become faster. For analog circuits that use the voltage domain

Table 1.1 Comparison of frequency synthesizer architectures

	PLL Integer – *N*	**PLL Frac – *N***	**DDS**	**DTC**
Range	-	-	+	+
Resolution	-	+	+	+
Settling Time	-	-	+	+
Spectral Purity	+	+	-	-
Direct Modulation	-	+	+	+
Portability across Fabrication Technologies			+	+

for encoding information, decreasing the supply voltages will reduce the signal swing creating an impediment to scalability. The DTC architecture is, however, uniquely qualified for scaling to newer digital technologies. The information in a DTC architecture is encoded by the location of output signal edges rather than by the absolute voltage swing. With the faster devices that become available with newer technologies, the temporal edge location placement resolution increases. This time domain signal processing [1.13] aspect of the DTC makes it very scalable to newer CMOS technologies. DTC, however, suffers from the problem of the presence of spurious frequencies in the output due to the presence of time domain edge placement error or jitter. The main results

of this thesis are to model and analytically predict the structure of the spur spectra of DTC synthesizers.

As the advantages of the DTC architecture become better known, it is evolving from experimental ICs to actual product use. Motorola and Texas Instruments both have products that make use of the DTC architecture. These are reported in [1.14] and [1.15] respectively.

1.1.2 Synthesizer State of Art

Table 1.2 provides illustrative comparison of the various frequency synthesizer architectures from the indicated references. The three synthesizers represented in this comparison are chosen for roughly comparable frequency range specifications.

Table 1.2 Illustrative comparison of some recent synthesizer literature

	Ref. [1.16]	**Ref. [1.17]**	**Ref. [1.14]**
Power (mW)	46.98	4700	120
Freq Range (MHz)	5870-6370	<1 – 2500	100-4000
Resolution (KHz)	Not available	76.2	0.06
Settling time (ms)	8.7	< 0.001	0.1
Technology	CMOS 180 nm	SiGe 130 nm	CMOS 90 nm
Spurious Free Dynamic Range (SFDR) (dB)	-61	-38	-45
Area (mm^2)	3.24	7.5	1.03
Year	2009	2009	2010
Architecture	ΣΔ Frac-*N*	DDS, 24b Acc, 10b DAC	DTC

1.2 DTC Example

We now describe the digital-to-time conversion (DTC) synthesis architecture using a simple example. Figure 1.3 shows a series of four delays, each with a delay d. They are fed with a reference signal with period T_{REF} (= $1/F_{REF}$). The delay d is related to the reference period as $d = T_{REF} / 4$ so that the output of delay 4 coincides with the input of the delay line.

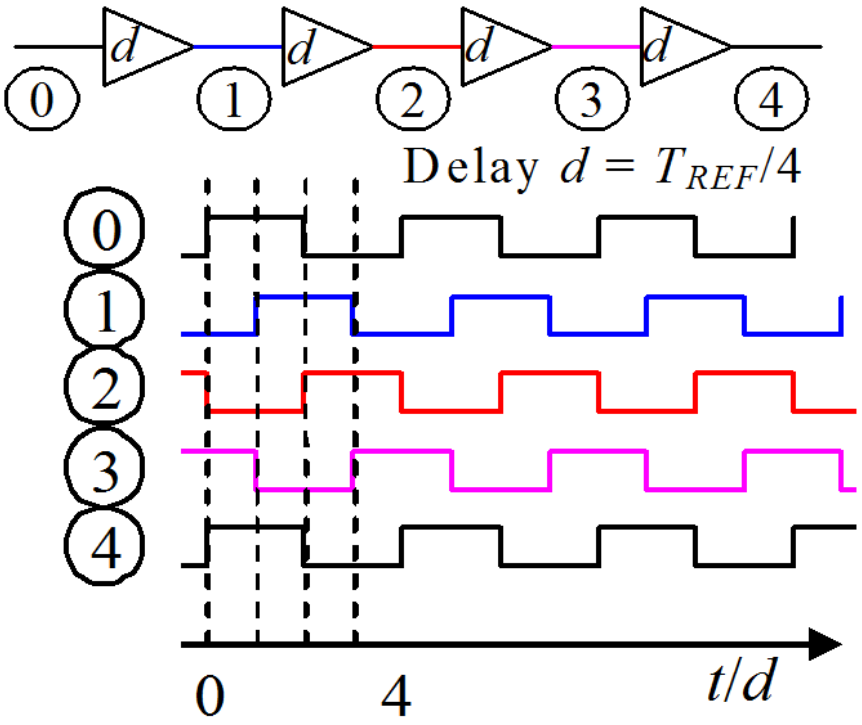

Figure 1.3 Delay line (DL) with four ideal buffers

Within each reference period, there are four rising edges that are available to trigger some event. The delay line can now be combined with a pair of multiplexers (MUXs) with control signals C_S and C_R and a S-R (set-reset) flip flop (FF) shown in Figure 1.4.

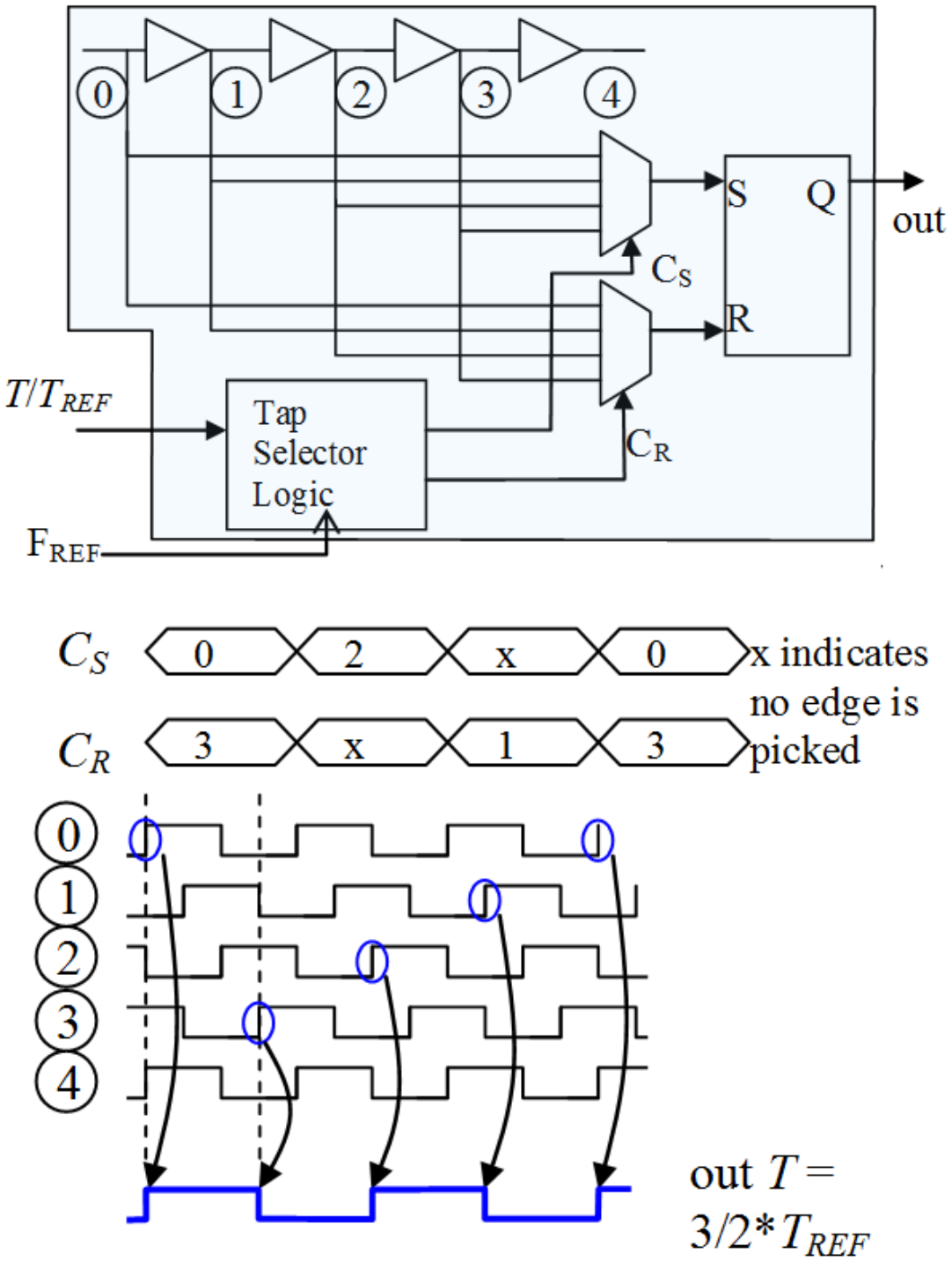

Figure 1.4 Delay line with MUX controls to create output period T=(3/2) x T_{REF}

The multiplexer control signals C_S and C_R are controlled by the tap selector logic. The tap selector block is a digital block having two inputs: the reference frequency signal and a digital frequency control word T/T_{REF}. In this example, the frequency control word is equal to 3/2 so that the desired output period is $T = (3/2) \times T_{REF}$. Based on the frequency control word, the tap selector logic generates the multiplexer control waveforms shown in the figure. The multiplexers route rising edges of the appropriate reference waveform to the set or reset inputs of the S-R FF in order to generate either a rising or a falling edge in the output signal.

1.3 Motivation to Analytically Understand DTC Spurs

Note, in the example above, that, different rising and falling edges in the output are derived from various delay elements in the delay line. An error in the edge location of a delay output signal will show up in the corresponding edge location in the output waveform. It can be shown that the delay choices are made in a periodic fashion (subject of chapters 3 and 4). This periodicity in the choice of multiplexer control signal causes the edge errors to appear periodically in the output waveform. This periodic error in the output causes undesirable spurious tones, or simply spurs, to be present in the output spectrum. The next four figures show actual measured spectra for four different settings of output frequencies generated by an experimental DTC synthesizer for a reference frequency of 1 GHz. The four output frequencies are F_1 = 763 MHz in Figure 1.5, F_2 = 780 MHz in Figure 1.6, F_3 = 790 MHz in Figure 1.7 and F_4 = 800 MHz in Figure 1.8. All four figures have the same settings with an analog spectral analysis span of 1 GHz from 550 MHz to 1550 MHz. It can be observed that the spur patterns for the four output frequencies have no observable relationship to each other in terms of the locations of the spurs and their amplitudes.

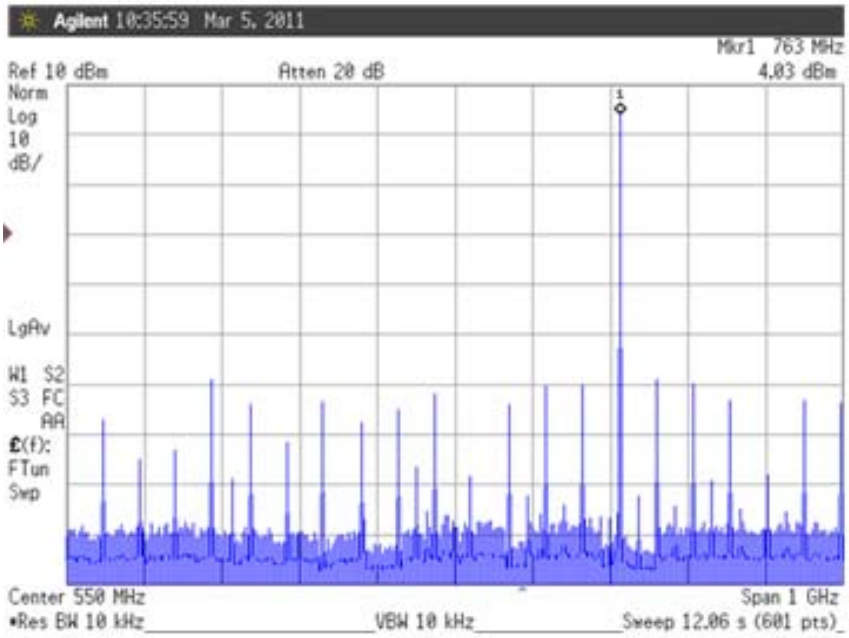

Figure 1.5 DTC spectrum: Output frequency 763 MHz (F_{REF} = 1 GHz)

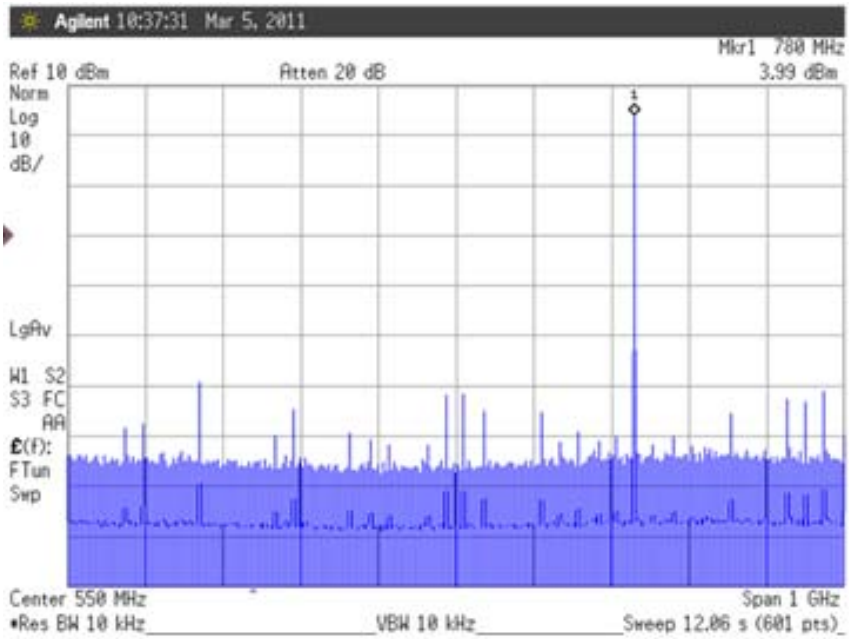

Figure 1.6 DTC spectrum: Output frequency 780 MHz (F_{REF} = 1 GHz)

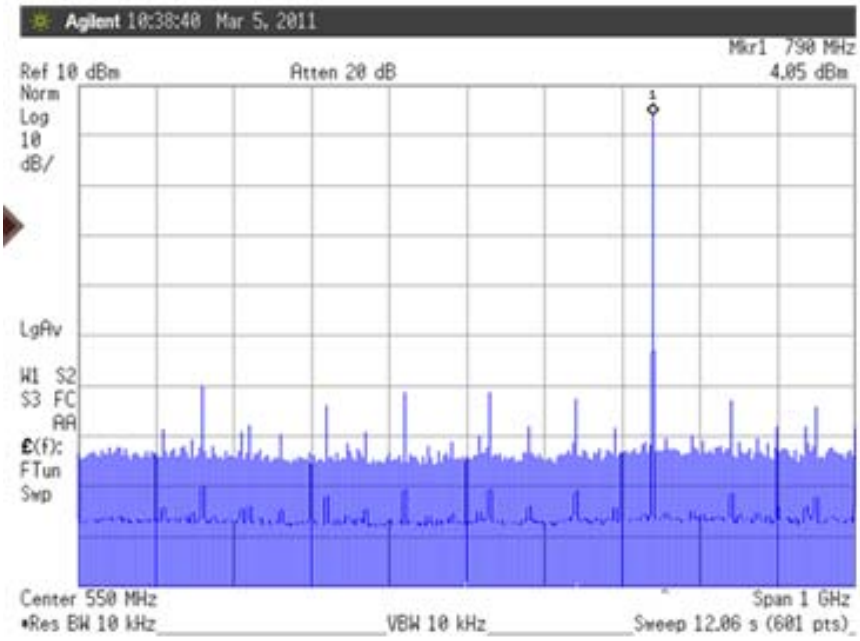

Figure 1.7 DTC spectrum: Output frequency 790 MHz (F_{REF} = 1 GHz)

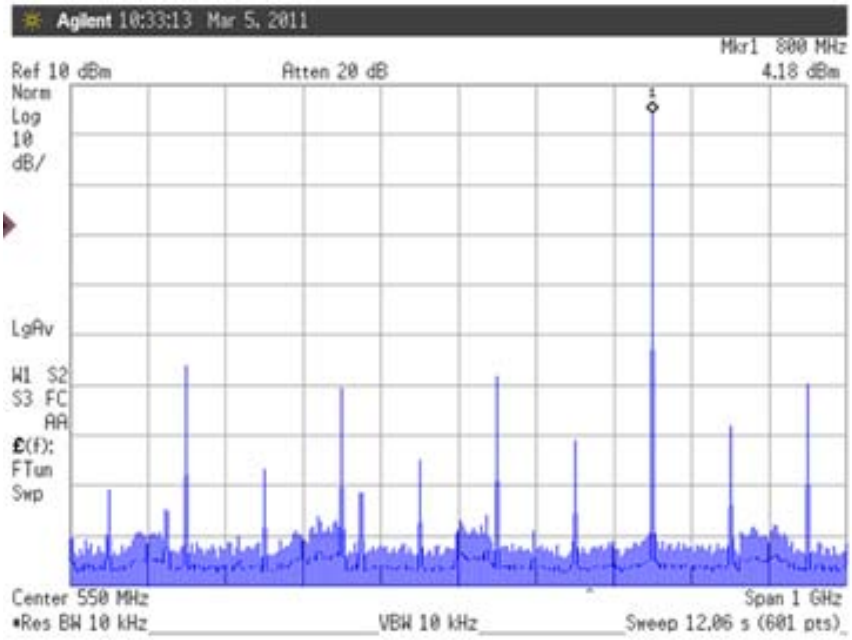

Figure 1.8 DTC spectrum: Output frequency 800 MHz (F_{REF} = 1 GHz)

This thesis answers the following question: do we need to measure the spurs at *every* possible output frequency setting in order to come up with the worst spur magnitude and location for the synthesizer? If the answer to the above question is 'yes', then it will be a prohibitively large task to make such measurements. As a result of the contributions of this thesis, the answer is 'no'. There is a rich structure among the spur patterns for different output frequencies that allows us to determine spur patterns for any output frequency by determining a principal set of spur spectra. Moreover, the determination of a principal set of spur spectra can be done analytically for the spurs due to quantization errors. Results show that more than 99% of the spur locations can be predicted correctly and more than 95% of the spur power levels are within 10 dB of their predicted value.

1.4 Key Property of DFT Axis-Scaling

The key to modeling the structure of the DTC spur spectra and levels is aided by the application of the axis-scaling property of the Discrete Fourier Transform. This property of the DFT is the discrete analogue to the more familiar continuous time/frequency axis-scaling property, namely, if a continuous-time signal is stretched by an arbitrary scaling factor in the time domain, then its Fourier Transform (FT) is compressed by the same factor (or stretched by the reciprocal of the time-axis stretch factor) in the frequency domain. The notion of stretching or compressing the time axis in the case of a continuous-time function translates to a permutation of samples in the case of discrete samples. Unlike the continuous-time case, however, in the case of discrete samples there is a limitation on the stretch factor to be an integer that is relatively prime with the length of the sequence. Two integers a and b are relatively prime if they have no common factors, that is, if $\gcd(a, b) = 1$. It is shown in this thesis that the DTC error sequences satisfy these requirements. Therefore, time domain errors for different desired output frequencies are related to each other via discrete 'stretching' (or 'compressing'). Consequently, the frequency domain spurs can be related to each other by the application of the DFT axis-scaling property.

1.5 Contributions and Organization of This Thesis

Chapter 2 is based on the published conference results [1.18] and it describes the DFT axis-scaling property in detail. This property is analogous to the time/frequency scaling property of the continuous-time (CT) Fourier Transform. The case of continuous time/frequency allows an arbitrary real-valued scaling factor; however, there is a restriction on the scaling factor in the case of discrete time. The restriction requires the scaling factor to be relatively prime with respect to the length of the DFT sequence.

Chapter 3 is derived from the peer-reviewed IEEE Transactions paper [1.19] and it describes the application of the DFT axis-scaling property to the problem of quantization errors that create spurs. In order to limit the sources of errors to only quantization, the delay line (DL) is assumed to be ideal. In an ideal delay line, every delay has its ideal value and hence the delay line mismatch errors are all zero. The quantization error sequences for different selected output frequencies are shown to be related via scaling in the discrete time domain. The spur spectrum for any output frequency is shown to be the Discrete Fourier Transform of the edge location error sequence under a linear approximation. (The validity of this first-order approximation of an exponential is considered in the appendix C).Using the time/ frequency axis-scaling property of the Discrete Fourier Transform (DFT), it is then shown that the quantization spectra associated with *all* possible output frequencies can be divided into a very small number of classes. The spectra within each class are predictably scaled and permutated versions of each other. For a DTC that has a phase accumulator with I integer and M fractional bits, this result simplifies the number of DTC output spectra possibilities from $2^{(I+M)}$ to less than M base classes. Spur spectral locations predictions based on the analysis techniques of this thesis match more than 99% of those measured on a DTC synthesizer fabricated on a 90-nm CMOS IC, while predicted power levels are within 10 dB for more than 95% of these locations. The analysis provided in this thesis also applies to a flying adder (FA) synthesizer, which is an alternative implementation of a DTC-based synthesizer that is slightly different in the design approach than the one used in the modeling of this thesis. The treatment of all possible output spur patterns helps to find an

expression for the location and strength of the i^{th} worst quantization spur. The analysis of this chapter also shows that the choice of the specific method of quantization (truncation or rounding) does not affect the non-DC sub-harmonic spurs.

Chapter 4 is based on the peer-reviewed IEEE Transactions paper [1.20] and it extends the application of the DFT axis-scaling property to the general case of an actual delay line (DL) in which the delay of every buffer is not equal to its ideal value. This delay mismatch error in addition to the previously considered quantization errors can also be analyzed using the DFT axis-scaling property. The spur spectra classification of an ideal DL from chapter 3 is extended in chapter 4 to this case of a non-ideal DL with mismatch error present. The condition that permits the separation of the buffer errors spur locations from the quantization errors spur location is derived. Spurs predicted based on the analysis match closely with actual measurements performed on a 90 nm CMOS DTC synthesizer, with more than 99% spur locations matching and power levels within 10 dB for more than 95% of these locations.

Chapter 5 concludes this thesis with an indication of directions for future research.

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2 Time-Frequency Axis-Scaling Property of Discrete Fourier Transform

The contents of this chapter, by Sumit A. Talwalkar (principal author) and Prof. S. Lawrence Marple, Jr., were published in the International Conference on Acoustics and Speech Signal (ICASSP) 2010, pp 3658 – 3661, March 2010

2.1 Chapter Introduction

This chapter presents the analogue of the time or frequency scaling theorem of continuous-time/frequency Fourier Transform (FT) in appropriate integer terms that apply to the Discrete Fourier Transform (DFT). The scaling property applies to scaling by only integers which are relatively prime to the length of the DFT. The time reversal property of DFT is identified as a special case of this theorem.

The time and frequency scaling property of the Fourier Transform (FT) of continuous-time functions is a fundamental property. It can be found in all the basic textbooks on linear systems and signals, e.g. [2.1] and [2.2]. In qualitative terms, whenever a function is stretched (or compressed) in one domain by a factor; its transform is stretched (or compressed) by the reciprocal of the factor in the other domain. The property does make sense intuitively. For example, if a signal is compressed in time domain by a factor of 2, then the same signal "happens" twice as fast in time. It is not unexpected that the FT of the compressed function has the same content at twice the frequency extent as the original (uncompressed function) frequency extent. Admittedly, this example does not make a mathematically rigorous statement. However, it does make a point.

Many properties of the FT, such as linearity, symmetry, time/frequency shifting and convolution have their direct analogues for the DFT. As for the time-frequency axis-scaling property in discrete time, there are extensive treatments of integer interpolation and decimation operations (see [2.3], for example). Both those operations, however, inherently change the sample values in the discrete time data set. For interpolation, zero

samples are inserted, while for decimation samples are removed. This chapter considers data *permutation* operations only. The data values and its DFT values are both rearranged in a systematic way using integer scaling factors. The scaling factors are limited to integers that are relatively prime with respect to the length of the DFT. A related result is stated in [2.4] without reference to the multiplicative inverse in modulo arithmetic. The main focus of most references (for example, [2.5]) is to use results from *number theory* for efficient transform computation. This chapter explicitly states the time/frequency axis-scaling in terms of the multiplicative inverse of the scaling factor. It also rigorously proves that the underlying condition (that the scaling factor be relatively prime with respect to the length of the sample set) are necessary and sufficient.

The chapter is organized as follows: Section 2.2 defines FT and DFT. It also describes the scaling property of FT. Section 2.3 presents and proves the scaling property of DFT. Section 2.4 shows an example that illustrates the DFT scaling property. In appendix 1 one may find proofs of some basic results from *number theory* that are used in this chapter.

2.2 Definitions

The Fourier Transform (FT), $X(f)$, of a function $x(t)$ and the inverse transform are defined as

$$\mathcal{F}\{x(t)\} = X(f) = \int_{t=-\infty}^{\infty} x(t)\exp(-j2\pi ft)dt \qquad (2.1)$$

and

$$\mathcal{F}^{-1}\{X(f)\} = x(t) = \int_{f=-\infty}^{\infty} X(f)\exp(+j2\pi ft)df \ . \qquad (2.2)$$

This chapter, for convenience, does not consider here the conditions for a function to be Fourier transformable, since they are not directly relevant to the subject of the paper. The important aspects to note is that the function $x(t)$ and its transform $X(f)$ are both defined on continuous variables t and f over $-\infty$ to $+\infty$.

The time/frequency axis-scaling property of FT can be stated for a real number a (negative valued a reverses the function) as

$$\mathcal{F}\{x(t)\} = X(f) \Rightarrow \mathcal{F}\{x(at)\} = \frac{1}{|a|} X\left(\frac{f}{a}\right). \tag{2.3}$$

Note that there is no restriction on the number a other than it being a real number. The special case of $a = -1$ gives rise to time (and frequency) axis reversal.

The Discrete Fourier Transform (DFT) of an N point sequence $x[n]$, $n = 0, 1, \ldots, N-1$ is defined for $k = 0, 1, \ldots, N-1$ with $W_N = \exp(-j2\pi/N)$ as

$$\mathcal{D}\{x[n]\} = X[k] = \frac{1}{\sqrt{N}} \sum_{n=0}^{N-1} x[n] W_N^{-kn} \,. \tag{2.4}$$

The inverse Discrete Fourier Transform is defined as

$$\mathcal{D}^{-1}\{X[k]\} = x[n] = \frac{1}{\sqrt{N}} \sum_{k=0}^{N-1} X[k] W_N^{+kn} \,. \tag{2.5}$$

Note that the integer arguments, n and k, of the finite sequence and its DFT go from 0 to $N-1$. It is not possible to state a time frequency scaling property for any arbitrary real scaling factor. Because sequences are defined over the integer set $\{0, 1, \ldots, N-1\}$, a non-integer general scaling may generate numbers outside this set. However, could it be

possible to say something about a limited set of scaling factors, such as integers? The next section answers this question.

2.3 Time/Frequency Scaling Property of DFT

The time/frequency scaling property for Discrete Fourier Transform (DFT) can be stated for a restricted set of scaling factors. The restrictions come from the fact that the arguments n and k are integers in the set $\{0, 1, \ldots, N-1\}$. Any scaling should be done to ensure that the scaled arguments fall in the same set. This may be guaranteed by restricting the scaling to integer factors and taking the modulo N of the scaled value. Additionally, it is necessary to have the scaling factor be relatively prime to N, the size of the DFT. This second condition is necessary to ensure that the scaled arguments do completely span the set $\{0, 1, \ldots, N-1\}$ as will be seen in the proof. The notation of triangular brackets for modulo from [2.4] is used throughout this thesis, such as

$$\langle x \rangle_N = x \bmod N . \tag{2.6}$$

Theorem 2.1: Time/Frequency Scaling of DFT

For an integer a,

$$\mathcal{D}\{x[n]\} = X[k] \Rightarrow \mathcal{D}\{x[\langle an \rangle_N]\} = X[\langle bk \rangle_N] \tag{2.7}$$

iff (if and only if) a is relatively prime to N. The scaling factor b is given by

$$b = \left\langle a^{\varphi(N)-1} \right\rangle_N \tag{2.8}$$

where $\varphi(N)$ is the Euler's phi function which denotes the number of positive integers less than and relatively prime to N (see appendix A).

Proof of Theorem 2.1: We begin by stating two related known results from basic number theory that follow from the fact that a and N are relatively prime. They are both stated here (appendix A contains a detailed proof for the sake of completeness) as they are used in this proof of the time/scaling property theorem.

For every integer a that is relatively prime with N

i) there exists a unique integer $b = \left\langle a^{\varphi(N)-1} \right\rangle_N$, such that $\langle ab \rangle_N = 1$. Note that b essentially is the "reciprocal" or the multiplicative inverse of a in a modulo integer arithmetic sense.

ii) the sequence $\{\langle an \rangle_N\}$ for $n = 0, 1, \ldots, N-1$ contains every number from the set $\{0, 1, \ldots, N-1\}$ exactly once.

Now consider the definition of DFT (2.4) for the time scaled sequence $x[\langle an \rangle_N]$ for $k = 0, 1, \ldots, N-1$ as

$$\mathcal{D}\{x[\langle an \rangle_N]\} = \frac{1}{\sqrt{N}} \sum_{n=0}^{N-1} x[\langle an \rangle_N] W_N^{-kn} \,. \tag{2.9}$$

Introducing a change of variable $m = \langle an \rangle_N$ then for $n = 0, 1, \ldots, N-1$, the index m also takes every value in $\{0, 1, \ldots, N-1\}$, although not in the same order. Further, n can be expressed in terms of m by multiplying both sides of the equation above by b (the modulo multiplicative inverse of a) and taking modulo N.

$$\langle bm \rangle_N = \left\langle b\left(\langle an \rangle_N\right) \right\rangle_N = \langle ban \rangle_N = \left\langle \langle n \rangle_N \langle ba \rangle_N \right\rangle_N = n \,. \tag{2.10}$$

The last step uses the identity $\langle ab \rangle_N = 1$. Therefore, $\langle bm \rangle_N = n$. With the change of variable, the DFT of the scaled function (2.9) can be written for $k = 0, 1, \ldots, N-1$ as

$$\mathcal{D}\{x[\langle an \rangle_N]\} = \frac{1}{\sqrt{N}} \sum_{m=0}^{N-1} x[m] W_N^{-k\langle bm \rangle_N} . \tag{2.11}$$

The final step follows from the fact that the exponential term is itself periodic so that

$$\begin{aligned} W_N^{-k\langle bm \rangle_N} &= \exp\left(-j \frac{2\pi k \langle bm \rangle_N}{N} \right) = \exp\left(-j \frac{2\pi k b m}{N} \right) \\ &= \exp\left(-j \frac{2\pi m \langle bk \rangle_N}{N} \right) = W_N^{-m\langle bk \rangle_N} . \end{aligned} \tag{2.12}$$

With this substitution, the DFT of the time scaled function can be expressed as

$$\mathcal{D}\{x[\langle an \rangle_N]\} = \frac{1}{\sqrt{N}} \sum_{m=0}^{N-1} x[m] W_N^{-m\langle bk \rangle_N} . \tag{2.13}$$

The right hand side above is simply the DFT $X[\cdot]$ evaluated at $\langle bk \rangle_N$. Therefore, for $n, k = 0, 1, \ldots, N-1$, the time scale property of the DFT is given by

$$\mathcal{D}\{x[\langle an \rangle_N]\} = X[\langle bk \rangle_N] . \tag{2.14}$$

This proves the sufficiency of the condition that the scaling factor a be relatively prime to the length of the DFT N. In order to prove the necessity of this condition, one needs to prove that if a and N do have common factors (other than 1), the scaling property does then not hold. In fact, the multiplicative inverse of a does not exist. Note also that the sequence $\{\langle an\rangle_N\}$ for n = 0, 1, …, $N-1$ does *not* contain every number from the set $\{0, 1, \ldots, N-1\}$. This can be seen by considering $c = \gcd(a,N)$. Since $c > 1$, two numbers n_1 and $n_2 = n_1 + (N/c)$ can be found in $\{0, 1, \ldots, N-1\}$ such that $\langle n_1 c\rangle_N = \langle n_2 c\rangle_N$ (see example 3 in next section). Thus, the scaling operation is now many-to-one and does not map to all N integers. Thus, the scaling operation leads to loss of data samples.

Clearly now, we see that the DFT of a circular time scaled sequence can be expressed with the circular frequency scaled DFT of the original sequence $x[n]$ if and only if the scale factor has no common factors with the DFT length.

2.4 Examples of DFT Time/Frequency Scaling

Example 1: Consider a random sequence of $N = 7$ samples. Use a time stretch factor of $a = 5$. The Euler's phi function of DFT length is $\varphi(7) = 6$ (see appendix A). Then, $b = \langle a^{\varphi(N)-1}\rangle_N = \langle 5^{\varphi(7)-1}\rangle_7 = \langle 5^{6-1}\rangle_7 = \langle 5^5\rangle_7 = 3$. Note that $\langle ab\rangle_N = \langle 5\times 3\rangle_7 = \langle 15\rangle_7 = 1$.

Figure 2.1 shows the sequence $x[n]$ and its time-scaled version $y[n] = x[\langle 5n\rangle_7]$. Figure 2.2 shows the real part of the corresponding DFT. It is apparent that the DFT of the time-scaled version is frequency scaled (by a factor of $b = 3$) version of the DFT of the original sequence, that is $Y[k] = X[\langle 3k\rangle_7]$.

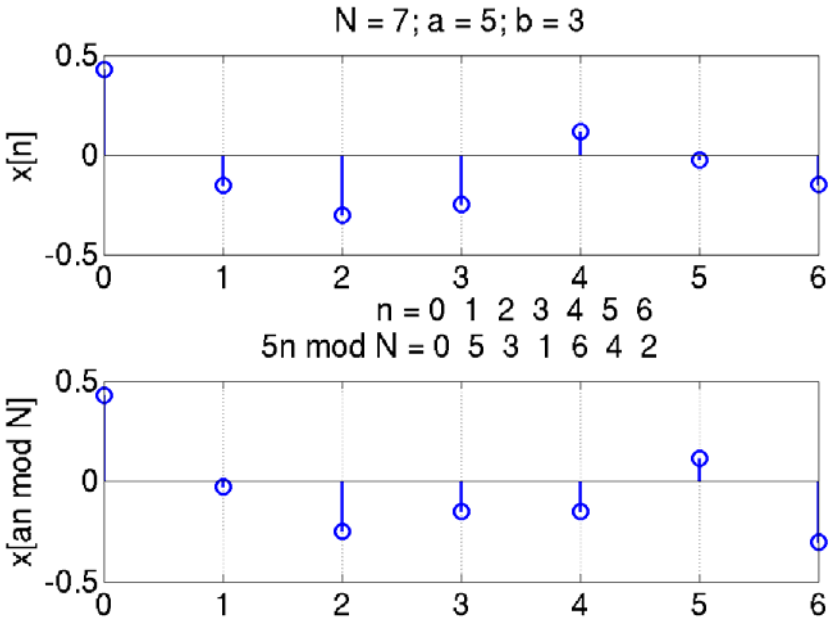

Figure 2.1 Time axis-scaling: $N = 7$, $x[n]$ (top) stretched by $a = 5$ (bottom)

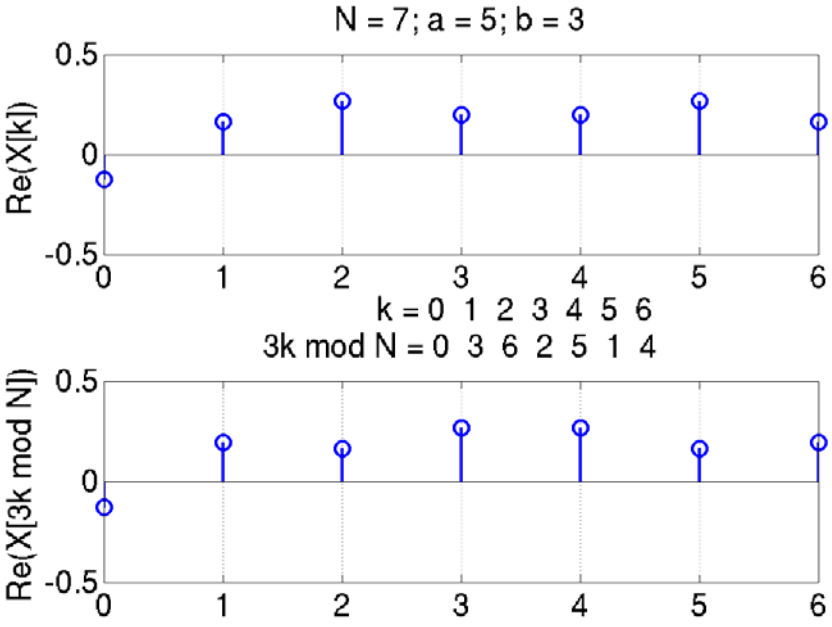

Figure 2.2 Frequency axis-scaling: Re($X[k]$) (top) stretched by $b = 3$ (bottom)

Example 2: Time Reversal: The time reversal property of DFT is found in many texts [2.1]. This can be seen as a special case of the time scaling property for N point DFT with a stretch factor $a = N - 1$. Since $\left\langle (N-1)^2 \right\rangle_N = 1$ the multiplicative inverse of $a = N - 1$ is $b = N - 1$,. Therefore, the DFT of the time reversed sequence is the frequency reversed version of the original DFT.

Example 3: gcd(a,N) > 1: Here is an example in which the time scaling does not work. Let $N = 6$ and $a = 4$ which are not relatively prime (c = gcd(6,4) = 2). Then, $\{\langle an \rangle_N\}$ = $\{0, 4, 2, 0, 4, 2\}$ for $n = 0, 1, \ldots, 5$. Any two integers n_1 and $n_2 = n_1 + N/c = n_1 + 3$ map to the same number. Thus, every alternate sample is dropped in the time scale operation.

2.5 Chapter Summary

The time/frequency axis-scaling property of Discrete Fourier Transforms (DFT) is presented with the necessary and sufficient condition on the scaling integer that it be relatively prime with the length of the DFT. The DFT of the time scaled (permuted) sequence is the DFT of the original sequence scaled (permuted) by the modulo inverse of the scaling factor. Appendix A contains some basic results from number theory that are used in this chapter.

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3 Quantization Error Spectra Structure of a DTC Synthesizer via the DFT Axis-Scaling Property

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3.1 Chapter Introduction

Phase accumulator quantization of a digital-to-time conversion (DTC) direct frequency synthesizer is analyzed for a fixed output frequency. This chapter applies the time/ frequency axis-scaling property of the Discrete Fourier Transform (DFT) from chapter 2 to the analysis of the phase accumulator quantization error of a DTC synthesizer. Using a first-order approximation it is shown that the quantization spectra associated with *all* possible output frequencies can be divided into a very small number of classes. The spectra within each class are predictably scaled and re-arranged versions of each other. For a DTC that has a phase accumulator with I integer and M fractional bits, this result simplifies the number of DTC output spectra from $2^{(I+M)}$ to M classes. Spur values predicted based on the analysis match closely with measurements performed on a 90 nm CMOS DTC synthesizer. It is shown that the choice of the specific method of quantization (truncation or rounding) does not affect the non-DC sub-harmonic spurs. The analysis also applies to a flying adder (FA) synthesizer.

Frequency synthesizers are critical components of all communication systems. They are used to generate the reference signal to up-convert a baseband signal to RF in a transmitter and down-convert an RF signal in a receiver. Synthesizers also generate clock signals to run the baseband processing blocks. Important performance metrics of frequency synthesizers include: frequency range, frequency resolution, settling time (when changing the output frequency), stability and spectral purity. Also important, especially to the mobile communication systems, is the ease of integration and the battery power drain.

Frequency synthesizers can be classified into two main classes: indirect phase locked loop (PLL) based and direct digital frequency synthesis (DDFS) [3.1]. Digital-to-time conversion (DTC) frequency synthesis is a relatively newer type of DDFS. DTC synthesizers attempt to preserve the large frequency range and the fast frequency switching ability of the conventional DDFS (as in [3.2] with a ROM and a precision DAC) while addressing the high power consumption problem. Some of the earliest descriptions of the DTC architecture are found in [3.3] and [3.4]. Further evolution of the DTC architecture (also called digital period synthesis, flying adder, and time-average-frequency) is reported in [3.6] - [3.20]. DTC has some promising unique characteristics. It is capable of generating a wide range of frequencies with very low switching times when changing frequency. DTC is uniquely conducive to integration using the widely used digital CMOS technology. Reference [3.11] reports a DTC-based on-chip synthesizer and [3.12] reports a transceiver IC that has a DTC synthesizer. The time domain signal processing [3.16] aspect of a DTC makes it very scalable to newer CMOS technologies as device voltages keep falling.

The DTC architecture, however, also presents its own unique set of challenges. Important among them is the presence of undesirable spurious tones (spurs), specifically spurs that have a sub-harmonic fundamental component. A small spur frequency fundamental can potentially produce spurs close to the desired output frequency. Sub-harmonic spurs are due to the periodic nature of the edge location errors ([3.15],[3.17] - [3.19], [3.20]) with periods *longer* than the desired output period. There are two main contributors to the periodic edge location errors: the phase accumulator quantization errors and the buffer delay errors (called mismatch errors [3.15]). Only the effect of quantization errors is considered here. The output spur pattern of a DTC synthesizer is dependent on the choice of the desired output frequency. Small changes in the desired output frequency can alter the spur pattern completely. This chapter applies the time-frequency axis-scaling property of the Discrete Fourier Transform (DFT) to the analysis of phase quantization errors. This new insight allows dividing all the output frequencies into a small number of classes. The spur patterns within each class are simply permutated

and scaled versions of each other under a linear first-order approximation. For an *M*-bit phase accumulator, there are only *M* classes of spur patterns. This insight provides direct closed form expressions to determine the strength and location of the i^{th} worst spur for a given output frequency. The worst spur value across all output frequencies is also found easily.

There are two common types of DTC synthesizers. The first type described in [3.4] and named a "flying adder" (FA) in [3.5] is further considered in [3.6], [3.8] - [3.11], [3.13] - [3.15] and [3.17] - [3.19]. Figure 3.1 shows block diagram of a FA based DTC.

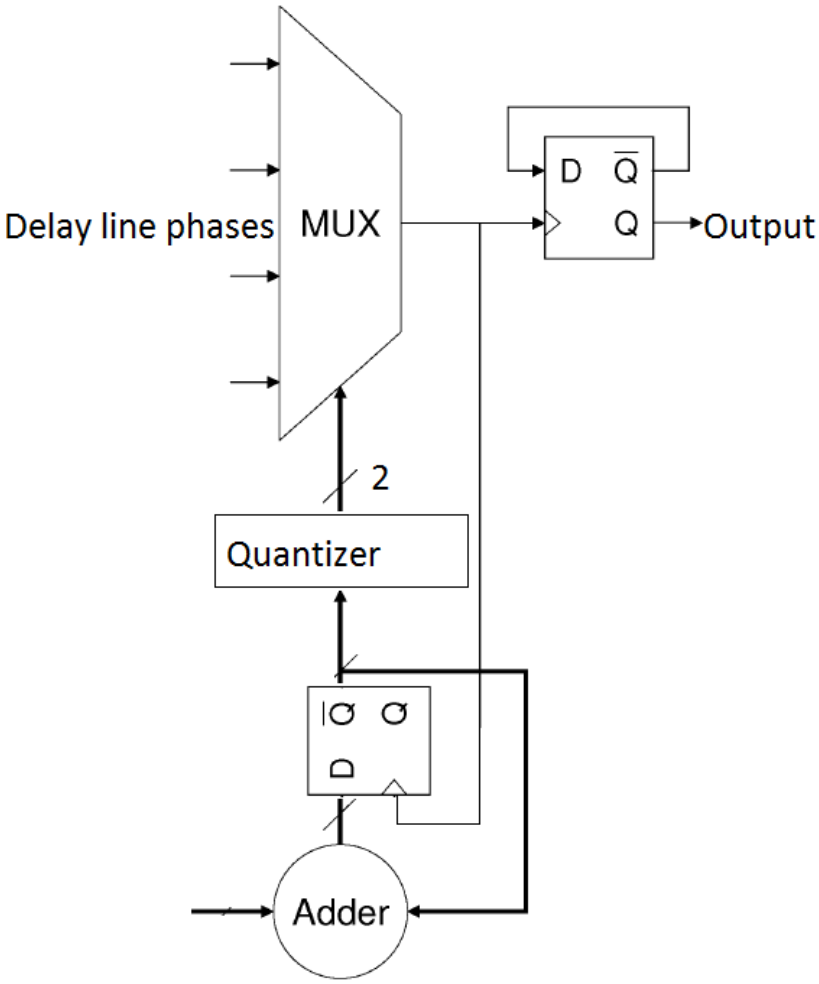

Figure 3.1 Flying adder architecture

The FA architecture uses a signal fed back from the multiplexer (MUX) output to clock the phase accumulator. Thus, the accumulator is clocked at twice the output frequency. The other architecture described in [3.3], [3.7] and [3.20] has a fixed clock accumulator (FCA). An FCA-DTC is analyzed in this chapter. It is shown here that for all output frequencies the phase quantization errors of the FCA-DTC and the FA are identical. This allows the use of either of the two types of architectures to analyze the effect of phase quantization.

Phase quantization spurs for a fixed frequency control word have been analyzed in [3.9], [3.10], [3.15], and [3.17] - [3.19]. The analysis presented here shows how the spurs for all possible frequency control words are related. Previous analyses [3.9], [3.10], [3.15], and [3.17] - [3.19] use truncation as the method of phase quantization. It is shown here that rounding, another common but hardware-intensive method of quantization, does not improve any non-DC spurs. Therefore, it is not necessary to use rounding.

The chapter is organized as follows. The model of the DTC synthesizer used for analysis is explained in section 3.2. The edge error model and output spurs are described in section 3.3. The main result regarding the application of the DFT axis-scaling property to the DTC quantization error spectrum is derived in section 3.4. Throughout the chapter, relevant aspects of the comparison of the FCA-DTC and the FA are included. A 90-nm CMOS transceiver IC with a DTC synthesizer was reported in [3.12]. Quantization spur measurements on this synthesizer validate the theoretical results presented in this chapter. An example is presented in section 3.5 followed by a summary in section 3.6.

3.2 DTC Model

Digital-to-time conversion frequency synthesis architecture uses a series of uniformly spaced digital phases of a reference signal to generate an output binary signal of output frequency specified by the user. Multiple phases may be produced by identical buffers in a delay locked loop (DLL). Depending on the desired frequency the digital tap selector logic selects appropriate phases of the reference signal to create edges in the output signal.

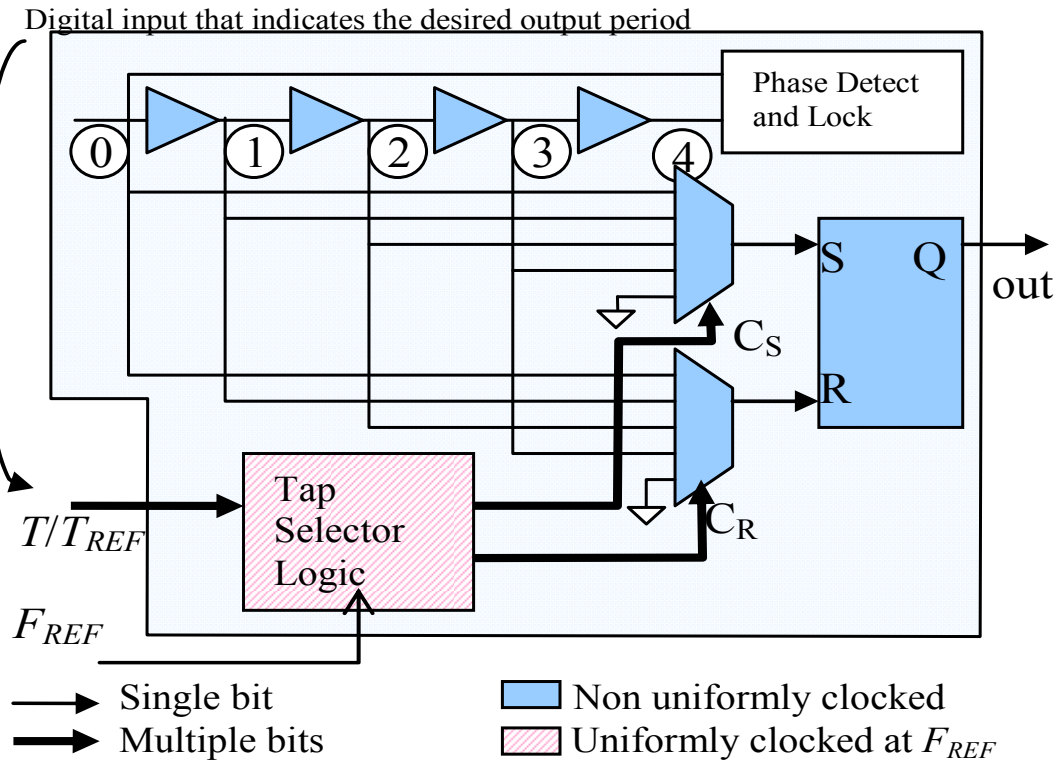

Figure 3.2 Digital-to-time conversion architecture

Figure 3.2 shows an ideal DL with a series of $N = 4$ buffers that carry the reference square wave signal (period T_{REF}). Let $d = (T_{REF}/4)$ denote the delay of each of the buffers. The final buffer output is used to complete the delay loop for locking. The buffer signals 0 through 3 are connected to set and reset inputs of an edge-triggered R-S flip-flop via multiplexers. The R-S flip-flop output is the synthesizer output signal.

The tap selector block is given the desired output frequency (actually, the inverse frequency or period) value as the ratio T/T_{REF} in the form of a binary word. The tap selector logic generates the multiplexer control signals C_S and C_R. Note that the requirement to represent the ratio as a binary number constrains the DTC to produce output periods such that T/T_{REF} is a binary word. The exact dependence of the output period resolution on the number of precision bits of T/T_{REF} is considered later. The other input for the tap-selector block is the clock signal at the reference frequency. The tap

selector block processes signals clocked uniformly at the reference frequency. The fixed clocking of the phase accumulator (tap selector logic) distinguishes this type of DTC from the flying adder type of DTC. All other blocks (labeled non-uniformly clocked) also carry rail-to-rail signals; however, they don't always change at the rising edge of the reference clock signal. Each multiplexer control sends one or none of the buffer outputs (when the MUX input connected to ground is chosen) to the R-S FF to create edges in the synthesizer output. The maximum frequency (minimum period) that can be generated is $F = F_{REF}$.

Figure 3.3 shows an example of C_S and C_R the MUX control signals that synthesize output with period $T = (3/2) \times T_{REF.}$ Each edge in the output signal x(t) is generated by selecting the appropriate rising edge in one of the phases of the reference signal. The reference edge selected to create each of the output edges has been highlighted.

3.2.1 Desired Output Period T/T_{REF}

The period (and frequency) of the DTC output is controlled using a binary digital word representing the ratio T/T_{REF}. Let p/q denote the reduced form ($\gcd(p,q) = 1$) of this ratio. Then,

$$p = \frac{T}{\gcd(T, T_{REF})} \text{ and } q = \frac{T_{REF}}{\gcd(T, T_{REF})} \text{ so that } \frac{p}{q} = \frac{T}{T_{REF}}. \qquad (3.1)$$

Since (T/T_{REF}) is in binary format, q is always a power of 2, and p is always an odd number. This architecture can generate a minimum output period of T_{REF} so that $p \geq q$.

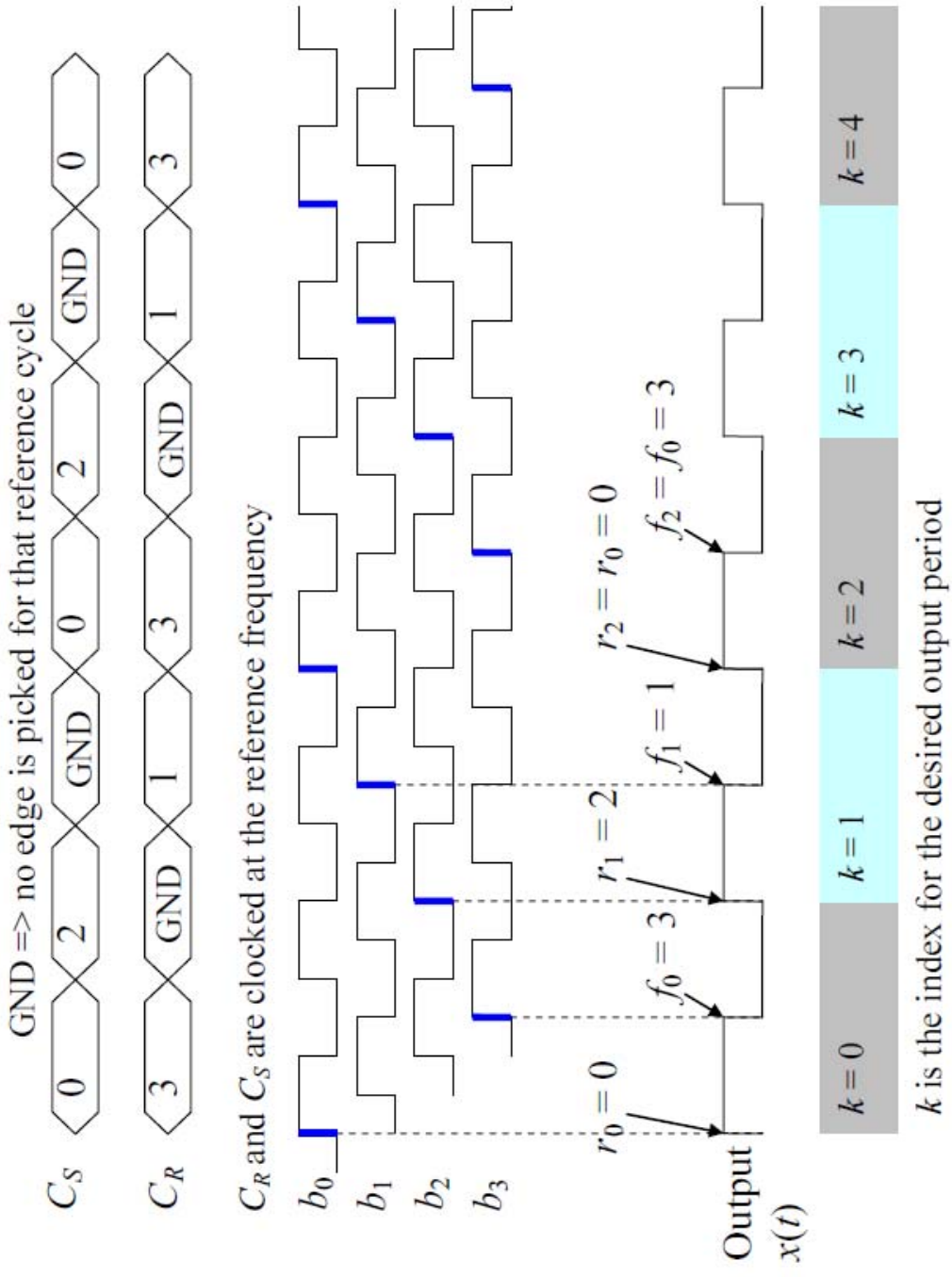

Figure 3.3 Example waveforms to generate period $T = (3/2) \times T_{REF}$.

Suppose the binary input value of T/T_{REF} is represented using $I = 2$ integer bits and $M = 3$ fractional bits. Then, a ratio of $T/T_{REF} = 2.25$ is represented as 10.010_2. In this case $p = 9$ and $q = 4$. It can be seen that the value of q can be found by simply locating the position of the right-most non-zero bit in the fractional part of the binary representation of T/T_{REF}. If l denotes the position of the right-most fractional non-zero bit measured from the binary point, then, $q = 2^l$. In the example above with $T/T_{REF} = 10.0\mathbf{1}0_2$, the second position (shown in bold face) to the right of the binary point has the rightmost non-zero bit. Thus, $l = 2$ and $q = 2^l = 4$. The reason for this is the trailing zeros to the right represent factors of 2 that are common to the ratio. Determination of p and q is crucial to predicting the spectral structure of the output as will be seen in the following sections. The number of integer and fractional bits allowed to represent the input ratio (T/T_{REF}) determine the output period (and frequency) range and resolution. For the range, note the bounds on the input ratio

$$1 \le \frac{T}{T_{REF}} \le 2^I - 2^{-M} \Rightarrow F_{REF} \ge F \ge \frac{F_{REF}}{2^I - 2^{-M}}. \qquad (3.2)$$

The output frequency resolution is the difference between a pair of neighboring output frequencies. For a DTC synthesizer the resolution is uniform for the output *period*, but not uniform across the output *frequency*. Let $T_1 = 1/F_1$ and $T_2 = 1/F_2$ be two neighboring output periods. Then,

$$\frac{T_1 - T_2}{T_{REF}} = 2^{-M} \Rightarrow \Delta F = F_2 - F_1 = 2^{-M} \frac{F_1 F_2}{F_{REF}} \approx \frac{2^{-M} F^2}{F_{REF}}. \qquad (3.3)$$

The equation above shows the dependence of the frequency resolution ΔF on the output frequency. The DTC has better resolution (smaller frequency steps) at the lower value of the output frequency. The worst resolution occurs at $F = F_{REF}$.

$$\Delta F < 2^{-M} F_{REF} \ . \qquad (3.4)$$

Some clarifications are in order. First, the constraint that T/T_{REF} be represented in fixed point binary format with finite number of fractional bits limits the output periods T that can be generated from a DTC synthesizer. In a way this is a form of quantization along the "output period continuum". This quantization of the output period is *not* the subject of this thesis. The focus here is the other quantization that happens in the choice of individual output edge locations *after* an allowed period T (such that T/T_{REF} is represented in binary format) is chosen. Second, N, the number of phases available, is not to be confused with M, the number of fractional bits allowed for the input word controlling the output period. In a practical DTC synthesizer implementation M is much larger than N, thus, allowing for a large choice of output frequency words.

3.2.2 Comparison with Flying Adder

The flying adder (FA) has the advantage of running the accumulator at the minimum possible frequency for a given output frequency, thus consuming the least possible dynamic power. The fixed clock accumulator DTC (FCA-DTC) analyzed here has the advantage of responding quickly to changes in the frequency control word, on the very next reference clock edge and not on the output edge. Such quick response is important in applications that depend on the fast frequency switching. Table 3.1 lists the mapping of some key FA variables used in [3.17] - [3.19] to variables used to analyze FCA-DTC in this thesis.

Table 3.1 Mapping of variables used in [3.17] - [3.19] to that in this thesis

	Ref. phases	Accum. bits	$\frac{T_{OUT}}{T_{REF}}$	Tap Period	Quant Error Seq
Flying Adder (FA) [3.17]	2^m	n	$w/2^{(n-1)}$	K	L
FCA-DTC (analyzed here)	N	M	p/q	$2q$	$2K_Q$

The flying adder can theoretically synthesize a maximum frequency of $F_{REF}\times(N/2)$, the FCA-DTC can generate a maximum frequency of F_{REF}. The FA maximum frequency in practice will be limited by the accumulator speed and the loop delay: clock-to-q delay of the phase register, the multiplexer delay and the clock tree for the phase register clock.

For all possible frequencies of an FCA-DTC (up to F_{REF}), the output of an FCA-DTC is identical to an FA. Thus, the results about quantization error spectra apply to both DTCs. It is explained later that for output frequencies above F_{REF} that only an FA can generate, the error in the approximation of the quantization spur spectrum increases. Therefore, the spur magnitude predictions will be increasingly erroneous as F reaches $F_{REF}\times(N/2)$ (spur locations are still exactly predicted). For brevity, the term DTC is used instead of FCA-DTC.

3.3 DTC Output Spectrum for Ideal DL

The focus of this chapter is the effect of the edge quantization errors. Such errors are present even when the reference edges are spaced uniformly at $d = T_{REF}/N$.

3.3.1 Rising and Falling Edge Tap Sequences

Assume that the first rising edge ($k = 0$) is at $t = 0$. Then, the ideal times of the k^{th} rising and falling edges are:

$$t_{r,Ideal}[k] = kT \text{ and } t_{f,Ideal}[k] = (k + 0.5)T \ . \tag{3.5}$$

The reference rising edges are available at each multiple of d. So the actual times of the k^{th} rising and falling edges are:

$$t_r[k] = d \cdot Q\left(\frac{t_{r,Ideal}[k]}{d}\right) \text{and } t_f[k] = d \cdot Q\left(\frac{t_{f,Ideal}[k]}{d}\right). \tag{3.6}$$

Here $Q(\cdot)$ denotes the quantization operation, for example floor(·), ceil(·) or round(·).

Finally, the buffer (out of the N buffers) for generating the k^{th} rising and falling edges of the output are given by

$$r_k = \left\langle Q\left(\frac{kNp}{q}\right)\right\rangle_N \text{ and } f_k = \left\langle Q\left(\frac{(k+0.5)Np}{q}\right)\right\rangle_N . \quad (3.7)$$

Here $\langle\rangle_N$ denotes the modulo-N operation. The period of each of r_k and f_k is q. An example of a DTC with $N = 4$ taps is shown in Figure 3.4. The desired output period is $T = (9/8)\times T_{REF}$. The figure shows the computation of control signals for rising and falling edges in the output signals. Next the ideal output waveform is shown. Below that all four phases of the reference signals are shown followed by the actual output waveform. The edge of the reference signal that is used to create each of the output signal edges has been highlighted. Finally the error signal is shown. The periodic nature of the error signal gives rise to spurs in the frequency spectrum.

3.3.2 Quantization Error Sequences

The edge quantization error in the k^{th} rising edge is

$$q_r[k] = t_{r,Actual}[k] - t_{r,Ideal}[k] = d\left[Q\left(\frac{kpN}{q}\right) - \frac{kpN}{q}\right]. \quad (3.8)$$

Similarly the k^{th} falling edge quantization error is

$$q_f[k] = d\left[Q\left(\frac{(k+0.5)pN}{q}\right) - \frac{(k+0.5)pN}{q}\right]. \quad (3.9)$$

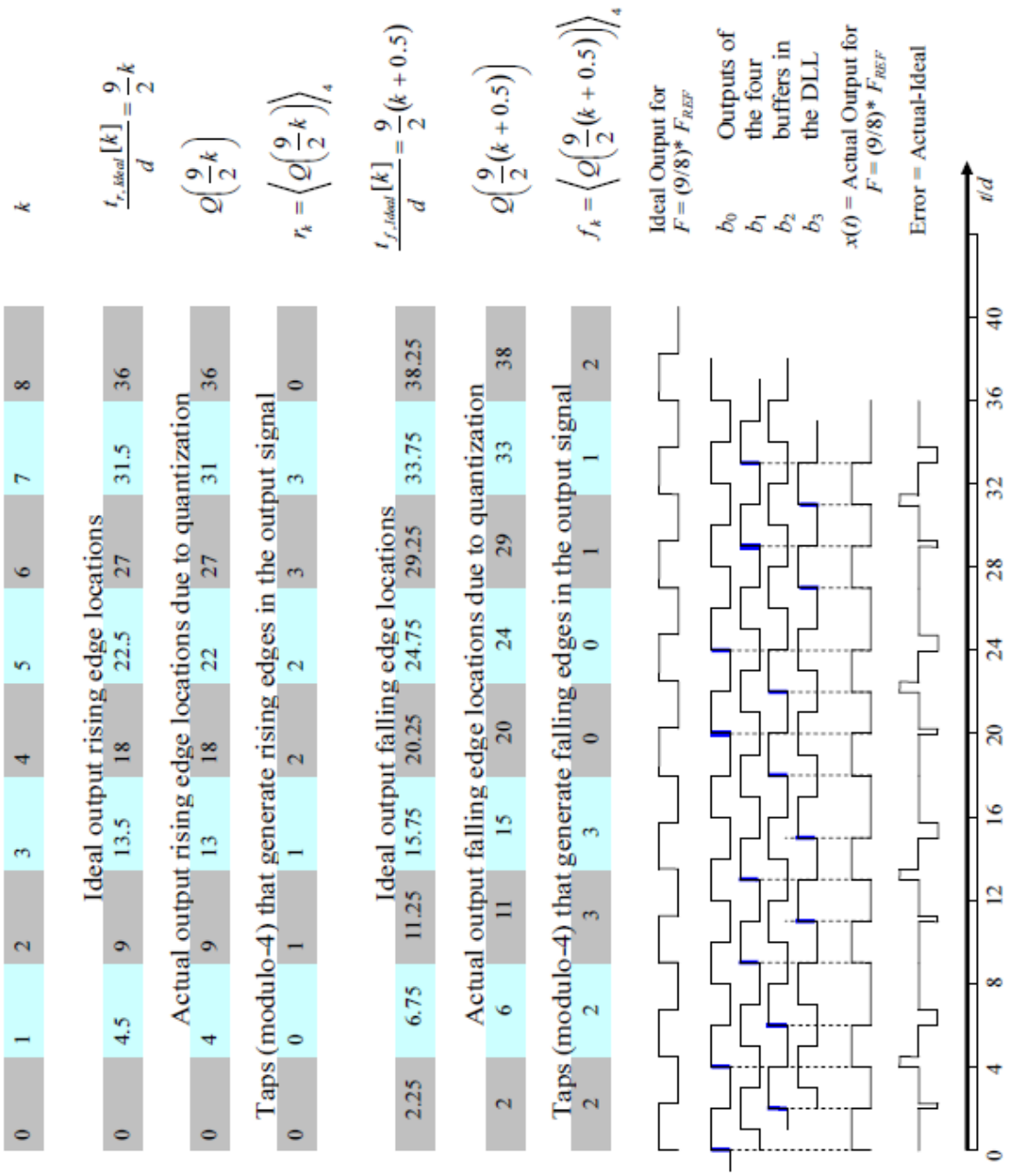

Figure 3.4 Edge quantization for a DTC with $N = 4$ for $T = (9/8)\ T_{REF}$

From (3.8) and (3.9), it can be easily verified that each of the rising and falling edge quantization error sequences have a period of

$$K_Q = q / \gcd(N, q) . \tag{3.10}$$

The last three equations are consistent with the related FA expressions (27)-(32) in [3.18]. For the example shown in Figure 3.4, the rising and falling edge quantization errors are periodic with a period $K_Q = 2$. A period of the rising edge quantization error sequence is {0, -0.5} and the falling edge quantization error sequence is {-0.25, -0.75}.

3.3.3 Output Spectrum

With the identification of the period of the quantization errors, the output waveform $x(t)$ may be written as an infinite sum of periods of quantization errors. Each term in the sum is a pair of unit step functions, added at each rising edge in the output and subtracted at each falling edge in the output.

$$x(t) = A \sum_{i=-\infty}^{\infty} \sum_{k=0}^{K_Q-1} \left\{ u(t - t_{r,Actual}[k + iK_Q]) - u(t - t_{f,Actual}[k + iK_Q]) \right\}. \tag{3.11}$$

Here A is the amplitude of the binary output (goes from 0 to A) and $u(t)$ denotes the unit step function. The inner sum (over k) goes over one period of quantization errors, while the outer sum (over i) goes over all such periods. The Fourier Transform (FT) of the output can be shown to be (see appendix B for details of the derivation)

$$X(f) = \frac{A}{j2\pi f K_Q T} \sum_{m=-\infty}^{\infty} \delta\left(f - \frac{m}{K_Q T} \right) \left(\sum_{k=0}^{K_Q-1} e^{-j2\pi f (kT + q_r[k])} - e^{-j2\pi f ((k+0.5)T + q_f[k])} \right). \tag{3.12}$$

The FT is a series of impulses at the multiples of the fundamental spur frequency of $1/(K_Q T) = F/K_Q$. The notation can be simplified by defining the strength of the m^{th} impulse as

$$J_m = \frac{A}{j2\pi m} \sum_{k=0}^{K_Q - 1} W^{2mk} \left(W^{(2mq_r[k]/T)} - W^m W^{(2mq_f[k]/T)} \right). \qquad (3.13)$$

Here $W = \exp(-j\pi/K_Q)$. Then, the output spectrum of a DTC signal is

$$X(f) = \sum_{m=-\infty}^{\infty} J_m \delta\left(f - \frac{m}{K_Q T} \right). \qquad (3.14)$$

This is consistent with equation (30) in [3.19] with the variable mapping given in Table 3.1. The desired output is at $m_{Desired} = K_Q$ with strength ($m = K_Q$, $q_r[k] = q_f[k] = 0$ in (3.13))

$$J_{K_Q} = \frac{A}{j\pi}. \qquad (3.15)$$

This is same as the amplitude of the first harmonic in an ideal square wave with amplitude A. This confirms that the DTC does synthesize a tone at the desired frequency. For those values of m which are multiples of K_Q, J_m represents the strength of harmonics of the output. For other values of m, J_m represents the strength of non-harmonic spurs. Of these, the sub-harmonic spurs for $m < 2K_Q$ are studied in more detail.

3.4 DTC Quantization Spectra and DFT Axis-Scaling

The expression for J_m, the strength of the m^{th} spur, can be further simplified with the approximation

$$\exp(j\theta) \approx 1 + j\theta \text{ , for } |\theta| << 1 . \tag{3.16}$$

The validity of this first-order approximation of an exponential is considered in appendix C. With this approximation applied to both of the exponentials containing $q_r[k]$ and $q_f[k]$, and observing that the sum of the powers of W^{mk} for $k = 0, 1, \ldots, K_Q - 1$ is zero

$$J_m \approx \frac{-A}{K_Q T} \sum_{k=0}^{K_Q-1} W^{2mk} \left(q_r[k] - W^m q_f[k] \right). \tag{3.17}$$

For $F \leq F_{REF}$ it can be shown that $\theta \leq (\pi/N)$ so that (3.16) is a good approximation for both FCA-DTC and FA. The approximation error rises for $F_{REF} < F \leq F_{REF} \times N/2$ in FA. The spur locations are still predicted by equation (3.14). However, the approximate value of the spur strength given by (3.17) is increasingly erroneous.

It is useful to define a $2K_Q$ - long period of quantization error sequence by interleaving the rising edge error and falling edge error as

$$q_e[l] = \begin{cases} (q_r[l/2]/d) \text{ for even } l \\ -(q_f[(l-1)/2]/d) \text{ for odd } l. \end{cases} \tag{3.18}$$

Hereafter, the combined sequence $q_e[l]$ is referred to as the quantization error sequence. Using (3.8) and (3.9) in (3.18) , the quantization error for $l = 0, 1, \ldots, 2K_Q - 1$ is

$$q_e[l] = (-1)^l \left[Q\left(\frac{lpN}{2q} \right) - \frac{lpN}{2q} \right]. \tag{3.19}$$

The strength of the m^{th} spur is a scaled Discrete Fourier Transform (DFT) of the $2K_Q$ long quantization error sequence is therefore

$$J_m \approx \frac{-A\gcd(N,q)}{pN} Q_e[m], \tag{3.20}$$

where the DFT of the interleaved quantization error sequence is defined for $m = 0, 1, \ldots, 2K_Q - 1$

$$Q_e[m] = \sum_{l=0}^{2K_Q-1} q_e[l] \exp\left(\frac{-j2\pi ml}{2K_Q}\right). \tag{3.21}$$

Since the error sequence is real, by the symmetry property of the DFT, the spurs are symmetric about the desired output tone. That is for $m = 1, \ldots, K_Q - 1$

$$J_m \approx J_{2K_Q - m}. \tag{3.22}$$

Example: Suppose $N = 12$, $p = 9$ and $q = 8$. For this DTC, $K_Q = q/\gcd(q,N) = 2$. Using (3.19), one period of the interleaved quantization error sequence for $l = 0, 1, \ldots, 3$ is

$$q_e[l] = (-1)^l \left[Q\left(\frac{27}{4} l\right) - \frac{27}{4} l \right]. \tag{3.23}$$

Figure 3.5 shows two period-lengths of the quantization sequence (using equation (3.23) for the two common methods of quantization, truncation and rounding).

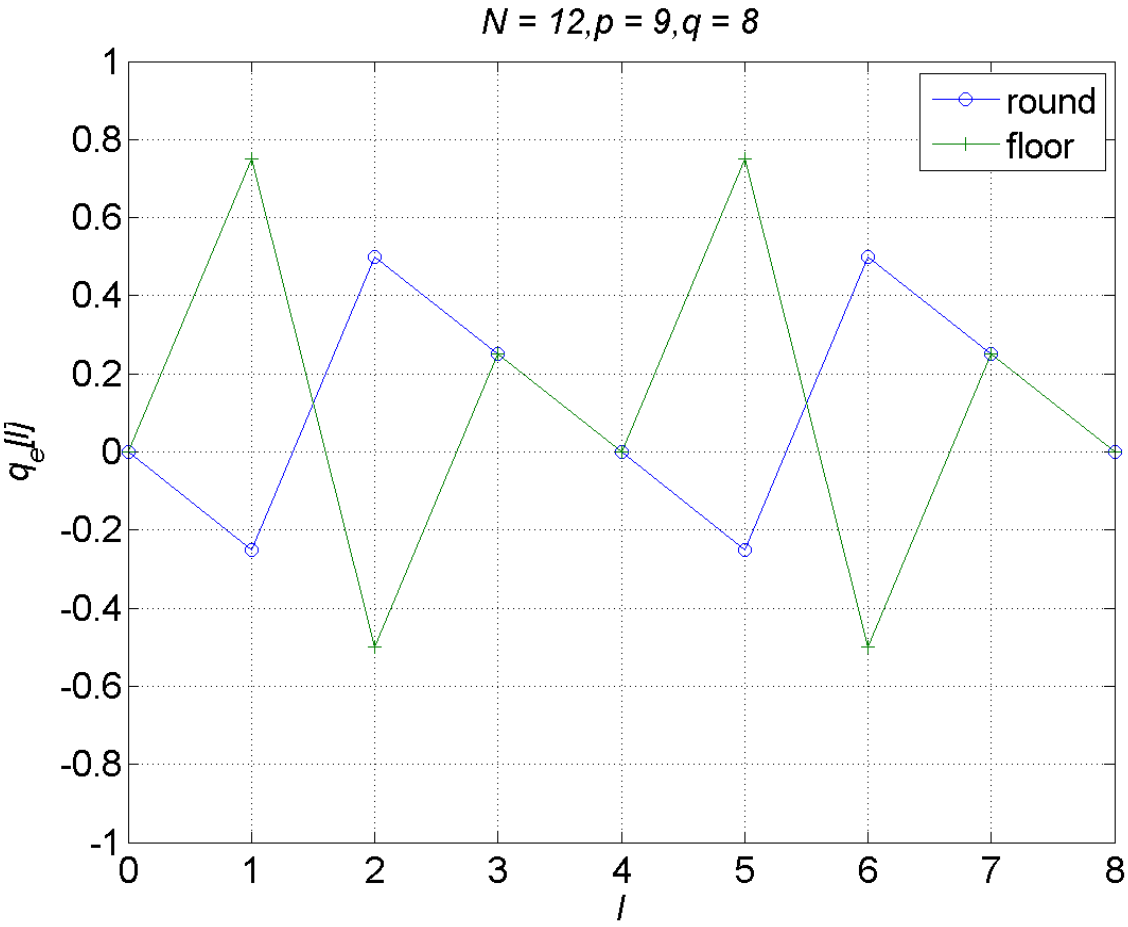

Figure 3.5 Quantization error sequence example for two quantization methods

Next we consider additional useful properties of the quantization error sequences.

3.4.1 Properties of the Quantization Error Sequences

Rewriting the expression for the quantization error sequence while emphasizing its dependence on p, for $l = 0, 1, \ldots, 2K_Q - 1$ yields,

$$q_e[l, p] = (-1)^l \left[Q\left(\frac{lpN}{2q} \right) - \frac{lpN}{2q} \right]. \qquad (3.24)$$

Theorem 3.1. The quantization error sequence is periodic over p with a period $P = 2K_Q$.

Proof of Theorem 3.1: This is easily seen by substituting $(p + P)$ for p in (3.24).

Note that the periodicity of $q_e[l,p]$ over p is separate from the periodicity over l, although the period happens to be the same ($2K_Q$). The periodicity over p implies that, at the most, there are K_Q distinct quantization error sequences (not $2K_Q$ since p can take only odd values) for a given value of N and q. Next consider the structure within a period along the p-axis.

Theorem 3.2. The quantization error sequences for two different values p_1 and p_2 (and same q) are related as time scaled (modulo) versions of each other. That is, for every p_1 and p_2 there exists a unique a such that

$$q_e[l, p_2] = q_e[\langle al \rangle_{2K_Q}, p_1]. \tag{3.25}$$

Proof of Theorem 3.2: First note that the periodicity over p means that

$$q_e[l, p] = q_e[l, \langle p \rangle_P] = (-1)^l \left[Q\left(\frac{l\langle p \rangle_P N}{2q} \right) - \frac{l\langle p \rangle_P N}{2q} \right]. \tag{3.26}$$

The modulo-$2K_Q$ value of p in the right hand side above is simply a mathematically useful substitution. Now consider two odd numbers p_1 and p_2 from $\{1, 3, \ldots, 2K_Q - 1\}$. Since neither of them have any common factors with q, they don't have any common factors with $K_Q = q/\gcd(N,q)$. Therefore,

$$\gcd(p_1, 2K_Q) = \gcd(p_2, 2K_Q) = 1 . \tag{3.27}$$

From basic number theory (see [3.21] for example) there exists a unique odd integer $a < 2K_Q$ such that

$$p_2 = \langle a p_1 \rangle_{2K_Q} \text{ for } a = \langle p_2 \cdot p_1' \rangle_{2K_Q} \tag{3.28}$$

where p_1' is the modulo-$2K_Q$ inverse of p_1. The quantization error for p_2 can be written using (3.28),

$$q_e[l, p_2] = (-1)^l \left[Q\left(\frac{l a p_1 N}{2q} \right) - \frac{l a p_1 N}{2q} \right] . \tag{3.29}$$

As a is odd and $2K_Q$ is even, $(-1)^l = (-1)^{al} = (-1)^{\langle al \rangle_{2K_Q}}$, then

$$q_e[l, p_2] = (-1)^{\langle al \rangle_{2K_Q}} \left[Q\left(\frac{\langle la \rangle_{2K_Q} p_1 N}{2q} \right) - \frac{\langle la \rangle_{2K_Q} p_1 N}{2q} \right] . \tag{3.30}$$

That is, for every l, q, N and p_1, p_2,

$$q_e[l, p_2] = q_e[\langle al \rangle_{2K_Q}, p_1] . \tag{3.31}$$

This is an important relation that shows, in addition to the entire sequence $\{q_e[l,p]\}$, $l = 0, 1, \ldots, 2K_Q - 1$, being periodic over p with a period $2K_Q$, the sequences at any two

values of p are axis-scaled (along the l-axis) versions of each other. The scaling factor is a given by (3.28).

Example: Consider a DTC with $N = 12$ taps. For $q = 16$, the value of $K_Q = q/\gcd(N,q) = 16/4 = 4$. The period of the interleaved quantization error sequence $q_e[l,p]$ over p is $2K_Q = 8$. During each such period, there are $K_Q = 4$ distinct sequences (corresponding to 4 odd values of p). All these 4 sequences can be directly found from each other using modulo-8 scaling along the l-axis. Suppose $p_1 = 19$ and $p_2 = 21$. The multiplicative inverse of p_1 (modulo-8) is 3 (since $3p_1$ is 1 in modulo-8 sense). Then, using (3.28), the scale factor is $a = 7$, so that, (see second (green) and third (blue) plots in Figure 3.6)

$$q_e[l,21] = q_e[\langle 7l \rangle_{2K_Q},19], \text{ for } l = 0, 1, \ldots, 7. \tag{3.32}$$

The final step is to relate the quantization spectra for any two values of p for given N and q. This uses the DFT axis-scaling property from [3.22] (or equation (2.7) from chapter 2). According to the time-frequency scaling property applied to the quantization error sequence $q_e[l]$, the DFT $\mathcal{D}\{q_e[l]\} = Q_e[m]$ of the time-scaled (along the l-axis) sequence is the frequency-scaled (along m-axis, the spur index) version of the DFT of the original sequence. The frequency scaling factor is the "reciprocal" of the time scaling factor (in modulo-$2K_Q$ sense). That is,

$$\begin{aligned} &\mathcal{D}\{q_e[l]\} = Q_e[m] \text{ for } l,m = 0,1,\ldots,2K_Q - 1 \Rightarrow \\ &\mathcal{D}\{q_e[\langle al \rangle_{2K_Q}]\} = Q_e[\langle bm \rangle_{2K_Q}], \text{ where } \langle ab \rangle_{2K_Q} = 1. \end{aligned} \tag{3.33}$$

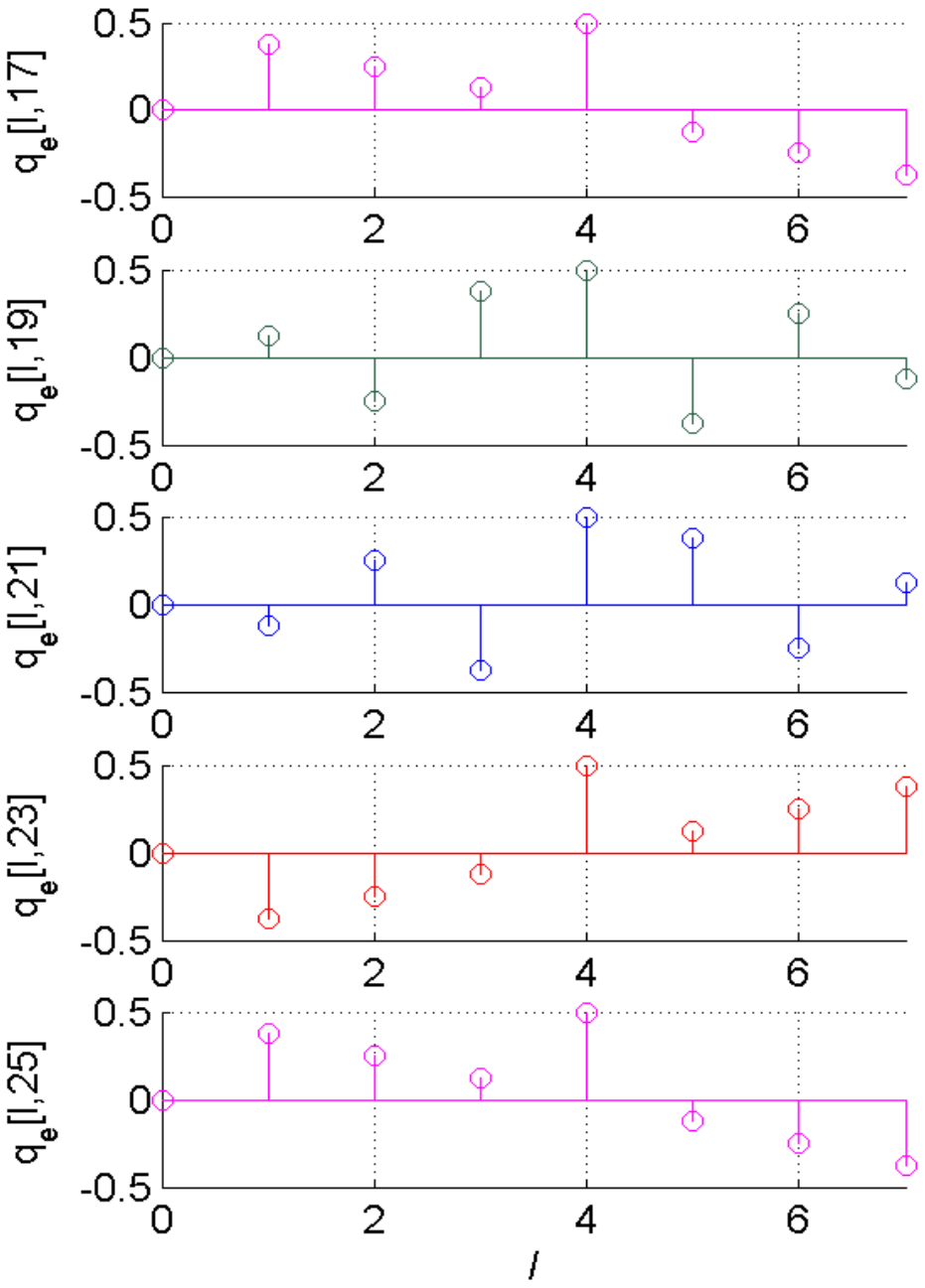

Figure 3.6 Quantization error sequences, $q_e[l,p]$, over one period of p.

Using (3.20), the DFT scaling property and (3.25), the relation for the spur spectra for given values of N and q, and for any two values p_1 and p_2 can be stated as

$$J[m, p_2] \approx \frac{p_1}{p_2} J[\langle bm \rangle_{2K_Q}, p_1], \text{ where } b = \langle p_2' p_1 \rangle_{2K_Q} . \qquad (3.34)$$

Here p_2' denotes the modulo-$2K_Q$ multiplicative inverse of p_2. Since p_2 and q are relatively prime and, so are p_2 and $2K_Q$. This ensures the existence and the uniqueness of b for every p_2. According to (3.34) any two output frequencies that have the same value of q, the quantization spectra are related through an amplitude scale factor and an axis-scaling (modulo-$2K_Q$) along the spur index m-axis.

3.4.2 Example: N = 4 Delays and M = 4 Fractional Bits

Consider a simple example of a DTC synthesizer with $N = 4$ phases to see the spur relation between all output frequencies. Suppose (T/T_{REF}) uses a 5-bit fixed point binary representation with 1 integer bit and 4 fractional bits.

Table 3.2 lists all possible cases of output frequencies. For the group of four frequencies with $K_Q = 1$, the two least significant bits (LSB's) of T/T_{REF} are 2'b00. The notation n'b00 describes a n-bit wide value with 'b' denoting binary representation according the IEEE-1364 standard. There is no quantization error for the rising edge locations. Falling edges may possibly have a constant quantization error depending on the method of quantization. The result is on the duty cycle of the output waveform. Spectrally, there are no sub-harmonic spurs.

For the group of four output frequencies with $K_Q = 2$, the two LSB's of T/T_{REF} are 2'b10. The quantization error sequences $q_e[l,p]$ and spectra $J[m,p]$ are related to $q_e[l,9]$ and $J[m,9]$ respectively for l, m=0, 1, …, 3 as

$$\begin{aligned}
q_e[l,11] &= q_e[\langle 3l \rangle_4, 9] \quad \text{and} \quad J[m,11] \approx \frac{9}{11} J[\langle 3m \rangle_4, 9] \\
q_e[l,13] &= q_e[l,9] \quad \text{and} \quad J[m,13] \approx \frac{9}{13} J[m,9] \\
q_e[l,15] &= q_e[\langle 3l \rangle_4, 9] \quad \text{and} \quad J[m,15] \approx \frac{9}{15} J[\langle 3m \rangle_4, 9]
\end{aligned} \quad . \qquad (3.35)$$

The last group of eight output frequencies with $K_Q = 4$, the two LSB's of T/T_{REF} are 2'b01 or 2'b11. The quantization error sequences $q_e[l,p]$ and spectra $J[m,p]$ are related to $q_e[l,17]$ and $J[m,17]$ respectively for l, m=0, 1, …, 7 as shown in (3.36).

Table 3.2 All possible output frequencies for the example DTC

Binary T/T_{REF}	**Ratio T/T_{REF}**	***p***	***q***	$K_q = \frac{q}{\gcd(q,N)}$
1.0000	16/16	1	1	1
1.0001	17/16	17	16	4
1.0010	18/16	9	8	2
1.0011	19/16	19	16	4
1.0100	20/16	5	4	1
1.0101	21/16	21	16	4
1.0110	22/16	11	8	2
1.0111	23/16	23	16	4
1.1000	24/16	3	2	1
1.1001	25/16	25	16	4
1.1010	26/16	13	8	2
1.1011	27/16	27	16	4
1.1100	28/16	7	4	1
1.1101	29/16	29	16	4
1.1110	30/16	15	8	2
1.1111	31/16	31	16	4

The time scale factors in the first columns of (3.35) and (3.36) are inverses (modulo-4 and modulo-8, respectively) of the frequency scale factors in the second columns.

In conclusion, for this example, *all* 12 non-trivial spectra (of 16 possible output frequencies) can be found from a principal set of two spur spectra, $J[m,9]$ for $m = 0, 1, \ldots, 3$ and $J[m,17]$ for $m = 0, 1, \ldots, 7$ using (3.35) and (3.36).

$$
\begin{aligned}
q_e[l,19] &= q_e[\langle 3l \rangle_8,17] \quad \text{and} \quad J[m,19] \approx \frac{17}{19} J[\langle 3m \rangle_8,17] \\
q_e[l,21] &= q_e[\langle 5l \rangle_8,17] \quad \text{and} \quad J[m,21] \approx \frac{17}{21} J[\langle 5m \rangle_8,17] \\
q_e[l,23] &= q_e[\langle 7l \rangle_8,17] \quad \text{and} \quad J[m,23] \approx \frac{17}{23} J[\langle 7m \rangle_8,17] \\
q_e[l,25] &= q_e[\langle l \rangle_8,17] \quad \text{and} \quad J[m,25] \approx \frac{17}{25} J[\langle m \rangle_8,17] \\
q_e[l,27] &= q_e[\langle 3l \rangle_8,17] \quad \text{and} \quad J[m,27] \approx \frac{17}{27} J[\langle 3m \rangle_8,17] \\
q_e[l,29] &= q_e[\langle 5l \rangle_8,17] \quad \text{and} \quad J[m,29] \approx \frac{17}{29} J[\langle 5m \rangle_8,17] \\
q_e[l,31] &= q_e[\langle 7l \rangle_8,17] \quad \text{and} \quad J[m,31] \approx \frac{17}{31} J[\langle 7m \rangle_8,17].
\end{aligned}
\tag{3.36}
$$

3.4.3 General Spur Pattern Classification

The example above can be generalized to the case of a DTC with N delay elements. Suppose the digital hardware uses M ($> N$) fractional and I integers bits to express T/T_{REF}. Then, there are $2^{(I+M)}$ possible output frequencies. Of these,

- $2^{(I+N)}$ output frequencies with q less than or equal to N have no quantization error. In terms of their frequency settings, the control words have $M - N$ trailing zeros. Then, the period of (with $K_Q = \gcd(q/N) = 1$) have no sub-harmonic quantization spurs.
- For each one of the remaining $2^{I\times(M-N)}$ output frequencies the frequency control word has non-zero bits in the trailing $M - N$ bits and hence there is quantization error. The corresponding spectra have spurs due to quantization. These $2^{I\times(M-N)}$ output frequencies can be classified into $M - N$ classes. For $i = 0, 1, 2, \ldots, M - N - 1$, the i^{th} class has $2^{(I+N+i)}$ output frequencies. The value of K_Q for the i^{th} class is $2^{(i+1)}$. Each of these $2^{I\times(M-N)}$

output frequency settings have quantization error sequences that are permutations of each other. Each of the corresponding spectra are amplitude scaled permutations of each other. Every spur pattern possible can be found from the knowledge of a principal spur spectra set consisting only ($M - N$) spur spectra using (3.34).

3.4.4 Worst Spurs

In order to find the worst spur value, it is convenient to use a value of $p = p_0$ such that

$$\left\langle p_0 \times \frac{N}{\gcd(q, N)} \right\rangle_{2K_Q} = 1 . \tag{3.37}$$

Such a value of p_0 ($> q$) is guaranteed to exist since N/gcd(q,N) and q/gcd(q,N) = K_Q are relatively prime. Since all quantization sequences and spectra for a given q are related, we may choose any convenient value of p to compute the worst spur values. Once the results for the special value of p is found, they can be readily translated for any other value of p using spectral permutation given by equation (3.34). Then, one period of the quantization error sequence, for $l = 0, 1, \ldots, 2K_Q - 1$, is

$$\left[Q\left(\frac{lp_0 N}{2q} \right) - \frac{lp_0 N}{2q} \right] = \left[Q\left(\frac{l}{2K_Q} \right) - \frac{l}{2K_Q} \right]. \tag{3.38}$$

Using (3.24), the error sequence for $l = 0, 1, \ldots, 2K_Q - 1$ is

$$q_e[l, p_0] = (-1)^l \left[Q\left(\frac{l}{2K_Q} \right) - \frac{l}{2K_Q} \right]. \tag{3.39}$$

When truncation is used for quantization, the argument inside the $Q(\ )$ function in (3.39) is less than 1 for all values of l. Thus, the quantized values are all zero. This gives

$$q_e[l, p_0]\big|_{Q=floor} = q_{e,floor}[l, p_0] = (-1)^l \left[-\frac{l}{2K_Q} \right]. \qquad (3.40)$$

The DFT of the quantization error sequence for $m = 1, 2, \ldots, K_Q - 1$ is

$$Q_{e,floor}[m] = \sum_{l=0}^{2K_Q-1} (-1)^l \frac{l}{2K_Q} \exp\left(\frac{-j2\pi ml}{2K_Q} \right) = \frac{1}{2K_Q} \sum_{l=0}^{2K_Q-1} la^l, \qquad (3.41)$$

where $a = -\exp\{-j2\pi[K_Q+m]/(2K_Q)\}$. Using a closed form for the sum in the right hand side above (see appendix D)

$$Q_{e,floor}[m] = \frac{-1}{1-a} = \frac{-1}{1-\exp\left(\frac{-j2\pi(m+K_Q)}{2K_Q} \right)}. \qquad (3.42)$$

Finally, the m^{th} spur can be written using (3.20)

$$J_{m,floor} \approx \frac{-A\gcd(N,q)}{p_0 N} \times \frac{-1}{1-\exp\left(\frac{-j2\pi(m+K_Q)}{2K_Q} \right)}. \qquad (3.43)$$

It has been shown in appendix E that the DFTs of the quantization error sequences obtained using the two different methods of quantization, truncation and rounding, have the same magnitudes. That is, for

$$\left|Q_{e,floor}[m]\right| = \left|Q_{e,floor}[m]\right| \text{ for } m = 0,1,\ldots,2K_Q - 1. \tag{3.44}$$

Therefore, it is not necessary to indicate the quantization method when considering the sub-harmonic non-DC (m = 1, 2, …, K_Q – 1) spur magnitudes. It is clear from (3.43) that the worst (largest) magnitude spur occurs at index m for which the exponential in the denominator is closest to 1, that is, when $m + K_Q$ is closest to zero. It happens when $m = K_Q - 1$ ($m = K_Q$ is the desired signal). The result is,

$$\left|J_{WC}\right| = \left|J_{K_Q-1}\right| \approx \frac{A\,\gcd(N,q)}{p_0 N\left|\left[1-\exp\left(\frac{-j\pi}{K_Q}\right)\right]\right|}. \tag{3.45}$$

The derivation of the worst spur was obtained for a special value of p that satisfied (3.37). For such p, the location of the worst spur $m_{WC} = K_Q - 1$. For any general value of p (within the same class, i.e. same value of q), the magnitude of the worst spur relative to desired output (see (3.15)) is

$$\frac{\left|J_{WC}\right|}{\left|J_{K_Q}\right|} = \frac{\left|J_{m_{WC}}\right|}{(A/\pi)} \approx \frac{\pi\,\gcd(N,q)}{pN\left|\left[1-\exp\left(\frac{-j\pi}{K_Q}\right)\right]\right|}\,(\text{dBc}). \tag{3.46}$$

Here ‘dBc’ refers to the spur magnitude in decibels with respect to the ‘carrier’ or the desired output frequency magnitude. The worst spur index, found using (3.34) and (3.37), is

$$m_{WC} = \left\langle (K_Q - 1)\langle p\rangle_{2K_Q}\,\frac{N}{\gcd(q,N)}\right\rangle_{2K_Q}. \tag{3.47}$$

The general i^{th} worst spur for a given output frequency is found by noting, as m goes away from K_Q in (3.43), that

$$\frac{\left|J_{WC}^{i}\right|}{\left|J_{K_Q}\right|} \approx \frac{\pi \gcd(N, q)}{pN\left\|\left[1 - \exp\left(\frac{-ji\pi}{K_Q}\right)\right]\right\|} \quad \text{(dBc)}. \tag{3.48}$$

The i^{th} worst spur index is found by generalizing (3.47)

$$m_{WC}^{i} = \left\langle \left(K_Q - i\right)\langle p\rangle_{2K_Q} \frac{N}{\gcd(q, N)} \right\rangle_{2K_Q}. \tag{3.49}$$

The worst spur over all possible output frequencies is found by using $q = N$ and $p = q+1$ in (3.48).

3.5 Measurement Results

This section presents a comparison of the measured spurs of a CMOS – DTC synthesizer with the values computed using the analysis presented in this chapter for two related output frequencies. The DTC synthesizer is a part of the transceiver IC in 90-nm CMOS that was described in [3.12]. As part of the IC characterization process, the measurements were made of the actual synthesizer spurs. The IC has a synthesizer output port that allows for direct measurements using an analog spectrum analyzer.

The synthesizer uses F_{REF} = 1000 MHz and N = 32 phases of the reference signal. The synthesizer uses dithering (as described in [3.23] and [3.24]) to mitigate the quantization spurs. For the spur values reported below, the dithering was disabled to allow for the measurement of raw un-dithered spurs. Dithering has been shown to reduce spurs in [3.13] by at least 20 dB (see Figure 25 in [3.13], for example). Similar improvement is also reported in [3.24]. Note that the dither injection mechanisms of [3.13] and [3.24] are

different. While the former adds random noise to the frequency control word, the latter adds it to the phase MUX control.

Synthesizer output spurs were measured for two output frequencies with a common value of $q = 256$ ($K_Q = 8$) with $p_1 = 259$ and $p_2 = 261$. The output frequencies are about 988.416 MHz and 980.843 MHz, respectively. The spur spectra for these two frequencies are predicted to be related by (3.34) as

$$J[m,261] \approx \frac{259}{261} J[\langle 7m \rangle_{16},259]. \tag{3.50}$$

Figure 3.7 and Figure 3.8 show the comparison of the measured and the analytically computed (using (3.20) spurs for $m = 0, 1, \ldots, 7$ (output is at $m = 8$).

The worst quantization spur for the first frequency shown in Figure 3.7) is (using (3.46))

$$\frac{|J_{WC}|}{|J_{K_Q}|} \approx \frac{\pi}{259 \times \left| \left[1 - \exp\left(\frac{-j\pi}{8} \right) \right] \right|} = -30.14 \text{ (dBc)}. \tag{3.51}$$

The worst spur index is found using (3.47) to be $m_{WC} = 5$. The spurs (both predicted by the analysis tools of this thesis and measured) in Figure 3.8 are re-arranged and scaled versions of those in Figure 3.7. Note that the amplitude scaling factor in (3.50) is $10*\log_{10}(259/261) = -0.03$ dB. The spur index scaling factor in (3.50) is 7 (modulo–16). Therefore, the first spur ($m = 1$) in Figure 3.8 is 0.03 dB smaller than the seventh spur ($m = 7$) in Figure 3.7. The second spur in Figure 3.7 is 0.03 dB smaller than the 14th spur in Figure 3.7. Although the 14th spur is not shown in Figure 3.7, there is symmetry around the desired tone since the errors are real valued. Thus, the 14th spur is the same as the 2nd spur ($m = 2$).

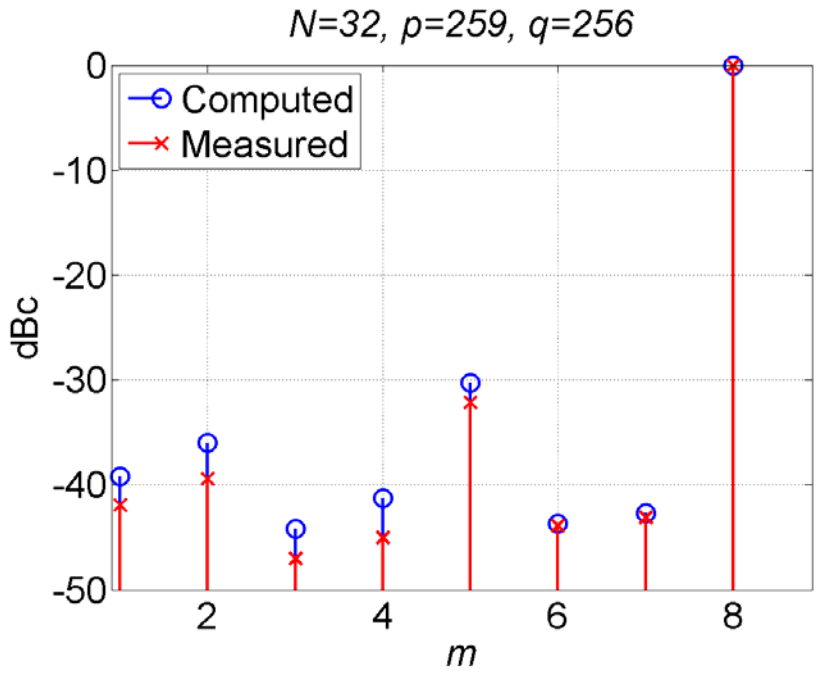

Figure 3.7 Computed (using 3.20) and measured spurs for $F_1=F_{REF}$ x (256/259).

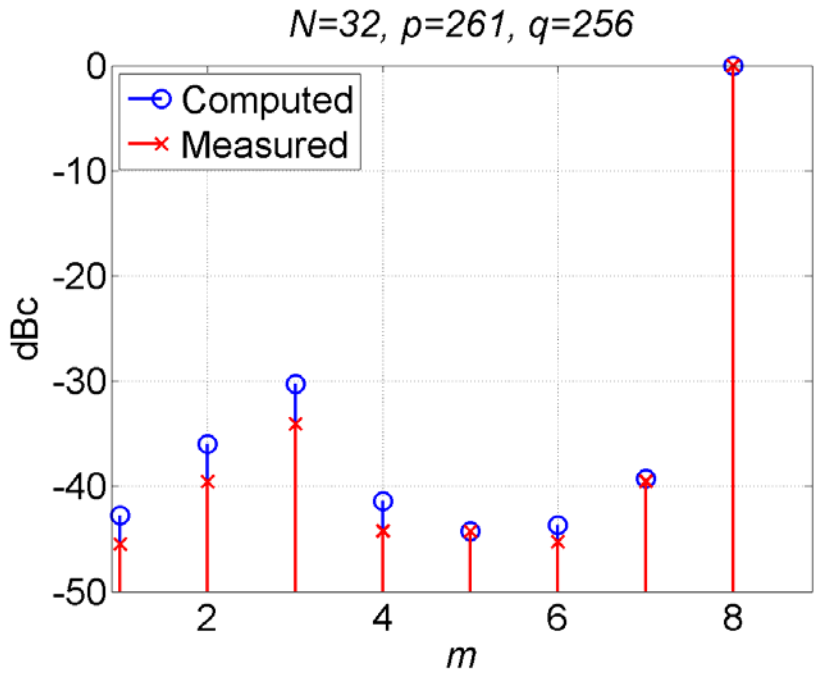

Figure 3.8 Computed (using 3.20) and measured spurs for $F_2 = F_{REF}$ (256/261). The computed spectra for F_1 in Figure 3.7 and F_2 in this figure are related via (3.50).

The measured and analytically predicted spur locations match exactly. The measured amplitudes (shown with the marker ‘x’) for both the frequencies show the frequency-scale relation predicted by (3.50). Each measured spur value is within 3.5 dB of the corresponding predicted value. Discrepancies between the computed and measured values are likely due to phase mismatch errors (see [3.15]) which are considered in the analysis of the next chapter. The mismatch errors also cause additional spurs since the fundamental frequency of mismatch errors is much smaller than the fundamental frequency of quantization errors. However, all of the additional measured spurs are about –53 dBc or smaller.

3.6 Chapter Summary

Sub-harmonic spurs due to the quantization error in a fixed clock accumulator digital-to-time conversion (FCA-DTC) synthesizer have been analyzed for all possible output frequencies. While the spur locations and magnitudes had been computed for a fixed frequency control word before, this chapter reveals an elaborate structure for the quantization error sequences based on different frequency control words. A first-order linear approximation allows the structure to be extended to the frequency domain using the time/frequency axis-scaling property of the Discrete Fourier Transform (DFT). The results derived here also apply to the flying adder (FA) based synthesizer, although the approximation error rises for output frequencies above the reference frequency.

The insight provided in this chapter into the quantization spectra structure allows the quantization spectra for *all* $2^{(I+M)}$ output frequencies to be classified in just M classes. The spectra within each class are systematically rearranged and scaled versions of each other. The location and value of the i^{th} worst spur was analytically derived. It is also shown that the two common methods of quantization, truncation or rounding, lead to the same non-DC sub-harmonic spurs. This justifies the use of much more hardware-friendly truncation as the method of quantization. Finally measurements on a 90-nm CMOS DTC synthesizer validate the theoretical model results.

3.7 Chapter References

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4 Digital-to-Time Synthesizers: Separating Delay Line Error Spurs and Quantization Error Spurs

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4.1 Chapter Introduction

This chapter analyzes the spurs due to delay line (DL) buffer mismatch errors and phase quantization errors in a digital-to-time conversion (DTC) direct frequency synthesizer. Applying the time/frequency axis-scaling property of the Discrete Fourier Transform (DFT) to a linear first-order approximation of the general case for both buffer error and quantization error spurs, it is shown that the spur spectra for all possible output frequencies can be divided into a very small number of classes. All the spectra within a class are scaled and permutated versions of each other. For a DTC with a phase accumulator with I integer and M fractional bits, this result reduces the number of spectra possibilities from $2^{(I+M)}$ to M. The condition that allows separation of the buffer error spur locations from the quantization error spur locations is derived. Spurs predicted based on the analysis of this chapter match closely with actual measurements performed on a 90 nm CMOS DTC synthesizer. The spur analysis also applies to the flying adder (FA) synthesizer.

Frequency synthesizers are critical components of all communication systems. They are used to generate the reference signal to up-convert a baseband signal to RF in a transmitter and down-convert an RF signal to baseband in a receiver. Synthesizers also generate clock signals to run baseband processing. Important performance metrics of frequency synthesizers include: frequency range, frequency resolution, settling time (when changing the output frequency), stability and spectral purity. Also important, especially to the mobile communication systems, is the ease of integration and battery power drain.

Digital-to-time conversion (DTC) frequency synthesis is a newer type of direct digital frequency synthesis (DDFS) architecture. DTC combines the large frequency range and the fast switching of a traditional direct digital synthesizer (as in [4.1] with a ROM and a DAC) while addressing its high power consumption problem. Since early publications found in [4.2]and [4.3], various implementations and analyses of DTC are reported in [4.4]-[4.18]. In addition to its ability for generating a wide range of frequencies with very low switching times, the DTC is also uniquely suitable to integration using the widely used digital CMOS technology ([4.10] and [4.11], for example). The time-domain signal processing [4.15] aspect of DTC makes it especially conducive to scaling to newer nodes of CMOS technologies even as the device voltages keep falling.

The DTC architecture, however, presents its own unique set of challenges. Important among them is the presence of undesirable spurious tones (spurs); specifically spurs that are sub-harmonic, that is, at frequencies *lower* than the output frequency. These sub-harmonic spurs are due to the periodic nature of the edge location errors ([4.8] and [4.9]) with periods *longer* than the desired output period. There are two main contributors to the periodic edge location errors: the phase accumulator output quantization errors and the buffer delay errors. Detailed analysis of the DTC spurs in the case of an ideal delay line (DL) (quantization-only errors, no buffer errors) was considered in chapter 3. This chapter extends the spur analysis to the case of a delay line with buffers that have non-ideal delays. The buffer delays errors are due to mismatches in silicon fabrication and hence are also called mismatch errors. The spur expression for a given output frequency is presented in [4.14]. This chapter shows that by using a linear first-order approximation the spurs can be separated into quantization spurs and mismatch spurs. The output spur pattern of a DTC synthesizer is dependent on the choice of the desired output frequency. This chapter extends the application of the time-frequency axis-scaling property of the Discrete Fourier Transform (DFT) to the analysis of non-ideal delay line DTC. This new insight allows dividing the spur patterns for all possible output frequencies into a small number of classes. The spur patterns within each class are simply permutated and scaled versions of each other under the linear approximation. For a phase accumulator with I

integer and M fractional bit input frequency control word, there are only M classes of spur patterns. This greatly simplifies analytical determination of the average and worst spur values for a given output frequency, as well as the worst spur value across all output frequencies.

This chapter is organized as follows. Section 4.2 describes the model of a DTC synthesizer and develops a spur spectrum expression. The following three sections contain the three key contributions of this chapter. Section 4.4 develops the application of the DFT axis-scaling property to the DTC (mismatch and quantization) spur spectrum. Section 4.5 derives the condition for the separation of quantization error spurs and mismatch error spurs. Measurements on a DTC synthesizer in a 90 nm CMOS transceiver IC [4.11] that confirm the theoretical determination are presented in section 4.6 followed a by chapter summary in section 4.7.

4.2 DTC Synthesizer Model

The Digital-to-time conversion frequency synthesis architecture uses a series of uniformly spaced phases of a reference signal to generate an output binary signal with a desired output frequency specified by the user. Such phases may be produced by a delay line (DL) of identical ideal buffers in a delay locked loop (DLL). The operation is explained with an example in detail in [4.20]. Note that the DL always carries the reference frequency signal. Depending on the desired frequency the digital tap selector logic selects appropriate phases of the reference signal using multiplexers. The multiplexer outputs are used to create edges in the output using an R-S flip flop. An example of a DTC using N=4 buffers is shown in Figure 4.1.

The tap selector block is given the desired output frequency (or rather, the period) control word in the form of the ratio T/T_{REF} expressed as a binary format. It generates multiplexer control signals C_S and C_R. The number of precision bits of T/T_{REF} determines the output period precision. With M fractional bits to represent T/T_{REF}, the frequency resolution ΔF is better than $2^{-M}F_{REF}$.(see chapter 3). The binary frequency control word T/T_{REF} can be expressed as a ratio p/q such that q is a power of 2 and p is an odd number.

Chapter 3 shows the importance of p and q on finding the spur spectra in the case of an ideal delay line. This chapter shows that p and q are important to the analysis of delay lines with non-ideal delays as well.

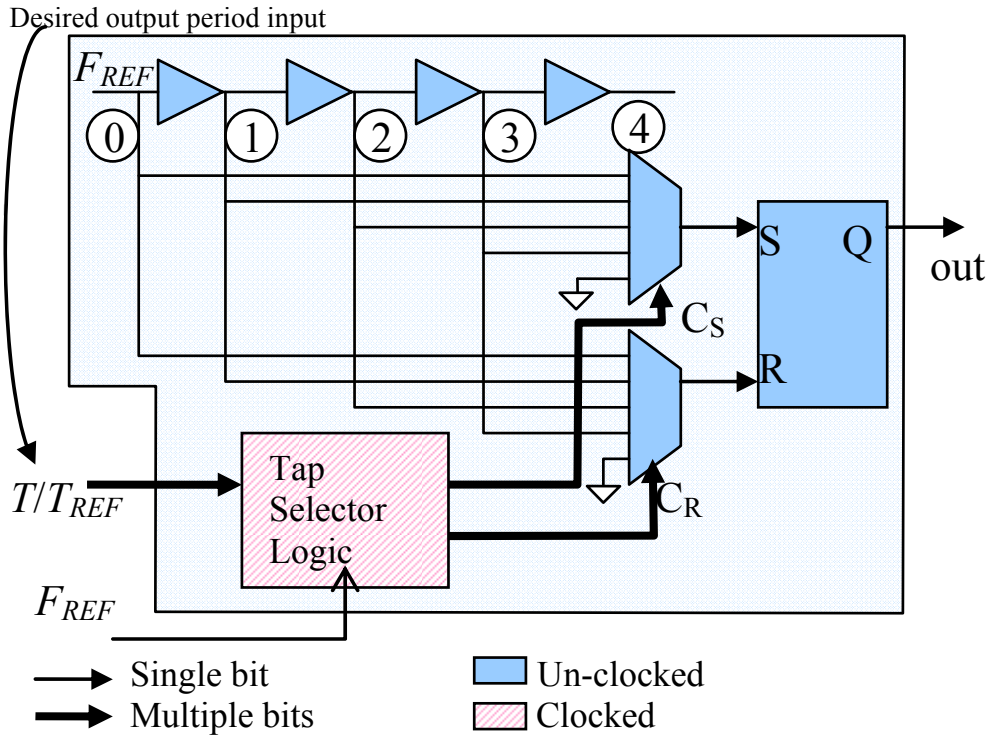

Figure 4.1 Digital-to-time conversion architecture- buffer outputs going through multiplexers to R-S flip flop to cause rising and falling edges

Table 4.1 lists the definitions of some key variables used in the analysis in this chapter. These variables are explained with the help of an example in Figure 4.2. The DTC in this example has $N = 4$ buffers with a buffer edge error in one of the four buffers. The ideal buffer delay is $d = T_{REF}/4$. The frequency control word is $T/T_{REF} = p/q = 9/8$ (1.00100_2 assuming $M = 5$ fractional bits). The first row shows the output cycle count k. The next three rows each show the rising and falling tap selections. Finally there are important waveforms at the bottom. The ideal output signal is shown along with the four available buffer outputs. The buffer signal b_1 has a position error that shows in the actual output (points B, C and D). The choice of buffers selected to create rising (and falling)

edges in the output is periodic with period $K = q = 8$. Using truncation as the method of phase quantization, one period of the rising and falling edge buffer sequences are r_k={0,0,1,1,2,2,3,3} and f_k={2,2,3,3,0,0,1,1}, respectively. The quantization error sequence is periodic with period $K_Q = K/\gcd(q,N) = 2$. One period of rising edge and falling edge quantization errors are $q_r[k]$={0, -d/2} and $q_f[k]$={-d/4,-3d/4}, respectively. Now consider the buffer output edge location errors in shown Figure 4.2. The example assumes that only one of the four buffer output signals is incorrectly delayed. The output of buffer b_1 is delayed by d/4 (shown in continuous red line) compared to its ideal waveform (shown in dashed black line). Thus the error in the position of the output of buffer b_1 is $b[1] = d/4$. Each time buffer b_1 is used to create an output edge, that edge location occurs d/4 *later* than the ideal location of the output edge. The remaining three buffer outputs (b_0,b_2 and b_3) are at their ideal position. Thus, the other three buffer errors are $b[0] = b[2] = b[3] = 0$. The final waveform in Figure 4.2 illustrates the combined effect of quantization and buffer errors. Point A has no quantization error, but only buffer error. Point B has quantization error of d/2 and buffer error of d/4 for a combined error of –d/4. Point C has quantization error of –d/4 cancelled by buffer error of d/4. Finally, point D has quantization error of -3d/4 and buffer error of d/4 for a total error of –d/2.

Table 4.1 Definitions of key variables

Variable	**Definition**
N	Number of buffers in the delay line
d	Nominal delay of each buffer
T_{REF} (= $N \bullet d$)	Reference signal period (= $1/F_{REF}$)
$b[n]$	Error in the position of the output of buffer n
T	Desired output period (= $1/F$)
p/q	Reduced ratio for the control word $p/q = T/T_{REF}$. In binary logic q is always a power of 2 and p is odd
r_k, (f_k)	Buffer chosen to create the k^{th} rising (falling) edge of the output
$q_r[k]$), ($q_f[k]$)	Quantization error incurred in placing the k^{th} rising (falling) edge of the output

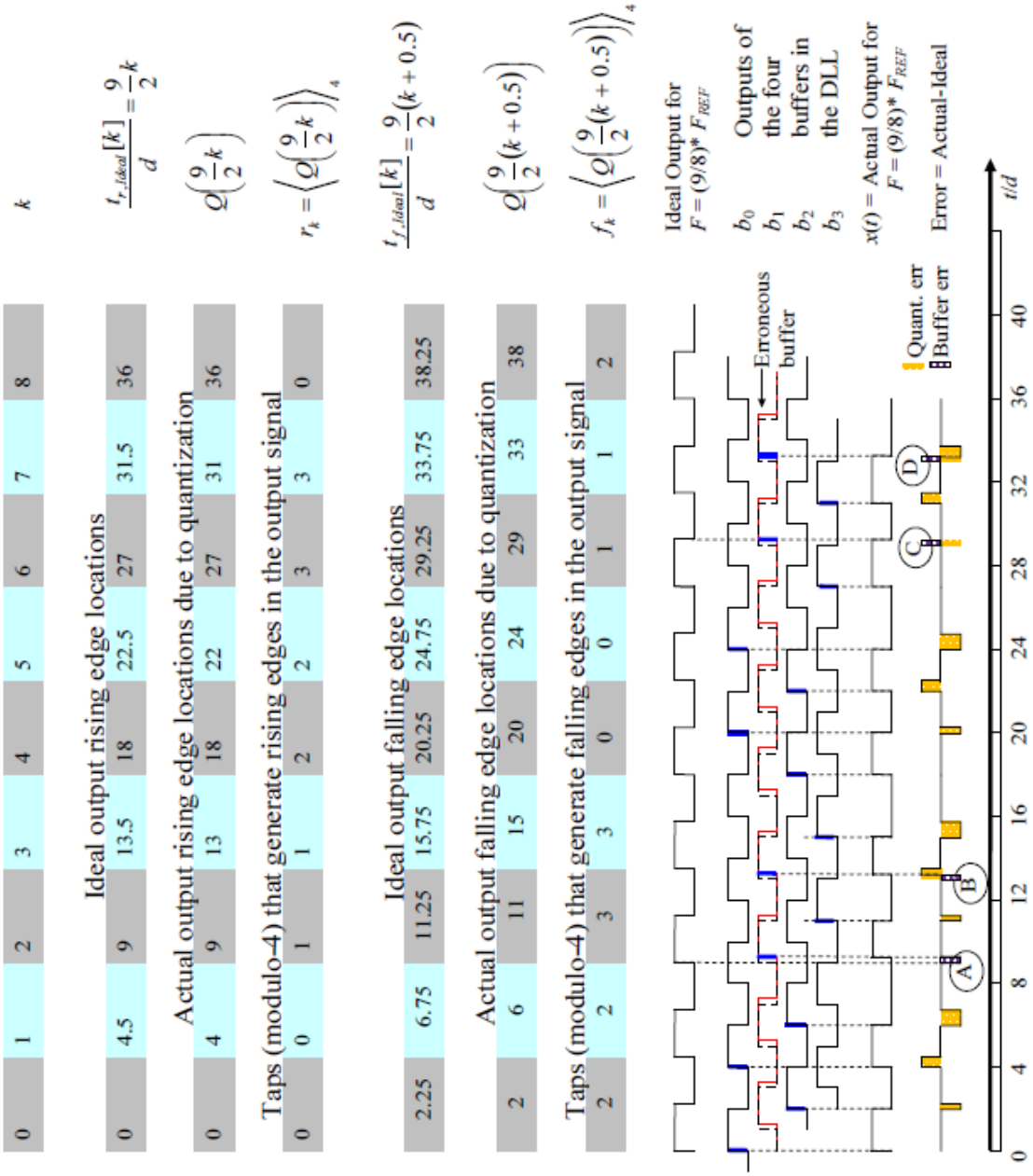

Figure 4.2 Example DTC with buffer error: $N = 4$ delays, $T = (9/8)$

Note that the quantization errors are exactly known for a given desired output frequency. The buffer errors are unknown without some type of measurement of the

delay line. Buffer errors are different for each instance of the DL. A study of sources and features of mismatch errors is found in [4.21]. The terms buffer errors, delay errors and mismatch errors are used interchangeably throughout this chapter.

4.3 Output Spectrum

The total errors $e_r[k]$ and $e_f[k]$ associated with the k^{th} rising and falling edges in the output signal are respectively

$$e_r[k] = q_r[k] + b[r_k] \text{ and } e_f[k] = q_f[k] + b[f_k]. \tag{4.1}$$

In (4.1) above, the quantization error components are given by (see equations (3.8) and (3.9) in chapter 3)

$$q_r[k] = d\left[Q\left(\frac{kpN}{q} \right) - \frac{kpN}{q} \right], \tag{4.2}$$

and

$$q_f[k] = d\left[Q\left(\frac{(k+0.5)pN}{q} \right) - \frac{(k+0.5)pN}{q} \right]. \tag{4.3}$$

Here $< >_N$ denotes the modulo-N operation and $Q(\bullet)$ is a function that represents the quantization operation (truncation or rounding). The rising and falling tap sequences in (4.1) given by (see equation (3.7) in chapter 3) are

$$r_k = \left\langle Q\left(\frac{kNp}{q} \right) \right\rangle_N \text{ and } f_k = \left\langle Q\left(\frac{(k+0.5)Np}{q} \right) \right\rangle_N. \tag{4.4}$$

The rising and falling tap sequences, $\{r_k\}$ and $\{f_k\}$, have period $K = q$ (see appendix E for a proof). Note that the quantization errors, $\{q_r[k]\}$ and $\{q_f[k]\}$, have period $\rho =$

K/gcd(K,N) (see equation (3.10) in chapter 3). Therefore, the total rising and falling edge error sequences $\{e_r[k]\}$ and $\{e_f[k]\}$ are periodic with period K. Using analytical operations like the derivation of the quantization-only spectrum in chapter 3, the output spectrum is found to be

$$X(f) = \sum_{m=-\infty}^{\infty} J_m \delta\left(f - \frac{m}{KT}\right), \tag{4.5}$$

where the m^{th} spur at $f = m\times(F/K)$ is

$$J_m = \frac{A}{j2\pi m} \sum_{k=0}^{K-1} e^{\left(\frac{-j2\pi mk}{K}\right)} \left[\begin{array}{l} \exp\left(-j2\pi m \dfrac{e_r[k]}{KT}\right) - \\ \exp\left(-j2\pi m\left(\dfrac{e_f[k]}{KT} + \dfrac{1}{2K}\right)\right) \end{array} \right]. \tag{4.6}$$

Define a $2K$ - long edge error sequence that interleaves K rising and K falling edge errors for $l = 0, 1, \ldots, 2K - 1$

$$e[l] = q_e[l] + b_e[l] = \begin{cases} \dfrac{q_r[l/2] + b[r_{l/2}]}{d} \text{ for even } l \\ -\dfrac{q_f[(l-1)/2] + b[f_{(l-1)/2}]}{d} \text{ for odd } l \end{cases}. \tag{4.7}$$

Here $q_e[l]$ is the $2K$ – long combined quantization error sequence given by equation (3.18) and $b_e[l]$ is the $2K$ – long combined buffer error sequence given as

$$b_e[l] = \begin{cases} b[r_{l/2}] \text{ for even } l \\ \\ -b[f_{(l-1)/2}] \text{ for odd } l. \end{cases} = (-1)^l b\left[\left\langle Q\left(\frac{lpN}{2q}\right)\right\rangle_N\right] \qquad (4.8)$$

Using the linearization approximation of the exponential function, the m^{th} spur for m = 1, 2, …, $K-1$ is approximately

$$J_m \approx \frac{-A}{pN}\sum_{l=0}^{2K-1} e[l]\exp\left(\frac{-j2\pi ml}{2K}\right) = \frac{-A}{pN}E[m], \qquad (4.9)$$

where $E[m]$ is the DFT of the total interleaved error sequence. The validity of the first-order approximation for quantization-only errors is considered in appendix C. The approximation continues to be valid for combined quantization and mismatch error as long as the average mismatch error is similar to the average quantization error (d/4 for rounding, d/2 for truncation).

4.4 Time-Frequency Scaling Property Application

This section extends the results of chapter 3, which are applicable only to an ideal DL with no buffer errors, to the general case of a DL with buffer errors. Equation (4.7) for the total error sequence may be rewritten with explicit emphasis on its dependence on p, for l = 0, 1, …, $2K-1$ as

$$e[l, p] = (-1)^l\left(Q\left(\frac{lpN}{2q}\right) - \frac{lpN}{2q} + b\left[\left\langle Q\left(\frac{lpN}{2q}\right)\right\rangle_N\right]\right). \qquad (4.10)$$

Now we can state two important properties of the error sequences for two output frequencies with the same q but two different values of p.

Theorem 4.1: The total error sequence $e[l,p]$ is periodic over p with a period $2K$, that is

$$e[l, p] = e[l, p + 2K]. \tag{4.11}$$

Proof of Theorem 4.1: This is seen by substituting $p + 2K$ for p in (4.10).

The periodicity over p implies that, at the most, there are K distinct error sequences. Although the period of the error sequences over p is $2K$, we do not have $2K$ distinct error sequences since p can take only odd values for a given value of N and q. The structure within a period along the p-axis is considered in the next theorem.

Theorem 4.2: The total error sequences for two different values p_1 and p_2 (and same q) are related as time scaled (modulo – $2K$) versions of each other. That is, for every p_1 and p_2, there exists a unique a such that

$$e[l, p_2] = e[\langle al \rangle_{2K}, p_1]. \tag{4.12}$$

Proof of Theorem 4.2: First note that the periodicity over p means that

$$e[l, p] = e[l, \langle p \rangle_{2K}] =$$
$$(-1)^l \left(Q\left(\frac{l\langle p \rangle_{2K} N}{2q} \right) - \frac{l\langle p \rangle_{2K} N}{2q} + b\left[\left\langle Q\left(\frac{l\langle p \rangle_{2K} N}{2q} \right) \right\rangle_N \right] \right). \tag{4.13}$$

The modulo-$2K$ value of p in the right hand side above is simply a mathematically useful substitution. Consider two odd numbers p_1 and p_2

from $\{1, 3,\ldots, 2K - 1\}$. Because neither of them have any common factors with $q = K$, one can conclude

$$\gcd(\, p_1, 2K\,) = \gcd(\, p_2, 2K\,) = 1\,. \tag{4.14}$$

From basic *number theory* (see appendix A lemma A.1) and noting that p_1 and $2K$ are relatively prime, there exists a unique odd integer $a < 2K$ such that

$$p_2 = \langle a p_1 \rangle_{2K} \text{ for } a = \langle p_2 \cdot p_1' \rangle_{2K}\,, \tag{4.15}$$

where p_1' is the modulo – $2K$ inverse of p_1. The quantization error for p_2 can be written using (4.13),

$$e[l, p_2] = (-1)^l \left(Q\left(\frac{l a p_1 N}{2q} \right) - \frac{l a p_1 N}{2q} + b\left[\left\langle Q\left(\frac{l a p_1 N}{2q} \right) \right\rangle_N \right] \right). \tag{4.16}$$

As a is odd and $2K$ is even, $(-1)^l = (-1)^{al} = (-1)^{\langle al \rangle_{2K}}$, then

$$e[l, p_2] = (-1)^{\langle al \rangle_{2K}} \left(\begin{array}{l} Q\left(\dfrac{\langle la \rangle_{2K}\, p_1 N}{2q} \right) - \dfrac{\langle la \rangle_{2K}\, p_1 N}{2q} \\ + b\left[\left\langle Q\left(\dfrac{\langle la \rangle_{2K}\, p_1 N}{2q} \right) \right\rangle_N \right] \end{array} \right). \tag{4.17}$$

That is, for every l, q, N and p_1, p_2,

$$e[l, p_2] = e[\langle al \rangle_{2K}, p_1]\,. \tag{4.18}$$

This is an important relation that shows, in addition to the entire sequence $\{e[l,p]\}$ for $l = 0, 1, \ldots, 2K - 1$ being periodic over p with a period $2K$, the sequence at any two values of p are axis-scaled (along the l-axis) modulo – $2K$ permutated versions of each other. The scaling factor a was defined in equation (4.15).

Example: Consider a DTC with $N = 12$ taps. For $q = 16$, the value of $K = q = 16$. The period of the interleaved total error sequence $e[l,p]$ over p will then be $2K = 32$. During each such period, there are $K = 16$ distinct sequences (corresponding to 16 odd values of p). All these four sequences can be directly found from each other using modulo-32 scaling along the l-axis. Suppose $p_1 = 19$ and $p_2 = 21$. The multiplicative inverse of p_1 (modulo-32) is 27 (since $27 \times p_1$ is 1 in modulo-32 sense). Using equation (4.15), the scaling factor is

$$a = \langle p_2 \cdot p_1' \rangle_{2K} = \langle 21 \times 27 \rangle_{32} = 23\,. \tag{4.19}$$

Using the knowledge that the total error sequences for different values of p are time scaled (in modulo sense) versions of each other given by equation (4.12) and the spurs sequence is the DFT of the error sequence equation (4.9), we can use the DFT scaling property (equation (2.7) in chapter 2) to relate the spurs for different values of p as

$$J[m, p_2] \approx \frac{p_1}{p_2} J[\langle bm \rangle_{2K}, p_1], \text{ where } b = \langle p_2' p_1 \rangle_{2K}\,, \tag{4.20}$$

where p_2' is the modulo-$2K$ inverse of p_2. This result extends the spur classification procedure for an ideal DL with only quantization errors to, the case of DL with buffer

errors. It is consistent with the main result (equation (3.34)) in chapter 3 which considers the special case of an ideal delay line with only the quantization errors.

4.5 Quantization Error Spurs and Buffer Error Spurs

Since the edge error sequence is the sum of the quantization error and buffer errors, the approximated spectrum can be written as a sum of the two spur component spectra,

$$J_m \approx J_m^Q + J_m^B, \tag{4.21}$$

where

$$J_m^Q = \frac{-A}{pN} \sum_{l=0}^{2K-1} q_e[l] \exp\left(\frac{-j2\pi ml}{2K}\right) \tag{4.22}$$

is the quantization error spectrum and the buffer error spectrum is

$$J_m^B = \frac{-A}{pN} \sum_{l=0}^{2K-1} b_e[l] \exp\left(\frac{-j2\pi ml}{2K}\right). \tag{4.23}$$

The sequences $q_e[l]$ and $b_e[l]$ are the interleaved (rising edge and falling edge) quantization and mismatch error components of the total error in equation (4.7) given by equations (3.18) and (4.8).

4.5.1 Quantization Error Spurs

Consider the quantization error spurs from (4.21) using a change of variable $l = \alpha(2K_Q) + \beta$ with the limits $l = 0, 1, \ldots, 2K - 1$ replaced by $\alpha = 0, 1, \ldots, \rho - 1$ and $\beta = 0, 1, \ldots, 2K_Q - 1$. Here $\rho = \gcd(N,q) = K/K_Q$ (see equation (3.10)). We get

$$J_m^Q = \frac{-A}{pN} \sum_{\alpha=0}^{\rho-1} \sum_{\beta=0}^{2K_Q-1} q_e[\alpha(2K_Q) + \beta] \exp\left(\frac{-j2\pi m(\alpha(2K_Q) + \beta)}{2K}\right). \tag{4.24}$$

Recognizing the periodicity of the quantization errors (see section 3.3.2), $q_e(\alpha(2K_Q)+\beta)=q_e(\beta)$. The double summation can then be de-coupled using $\rho = K/K_Q$ as

$$J_m^Q = \frac{-A}{pN}\sum_{\beta=0}^{2K_Q-1} q_e[\beta]\exp\left(\frac{-j2\pi m\beta}{2K}\right)\times\sum_{\alpha=0}^{\rho-1}\exp\left(\frac{-j2\pi m\alpha}{\rho}\right). \quad (4.25)$$

The second summation is zero except when m is a multiple of ρ. In other words, if $m = \mu\rho + \nu$ with an integer μ and a non-negative integer ν less than ρ.

$$\sum_{\alpha=0}^{\rho-1}\exp\left(\frac{-j2\pi m\alpha}{\rho}\right) = \sum_{\alpha=0}^{\rho-1}\exp\left(\frac{-j2\pi(\mu\rho+\nu)\alpha}{\rho}\right) = \begin{cases}\rho \text{ if } \nu = 0\\ 0 \text{ otherwise}\end{cases}. \quad (4.26)$$

Using equation (4.26) the quantization error spectrum can be written as

$$J_m^Q\Big|_{m=\mu\rho+\nu} = \begin{cases}\dfrac{-A\rho}{pN}\displaystyle\sum_{\beta=0}^{2K_Q-1} q_e[\beta]\exp\left(\frac{-j2\pi\mu\beta}{2K_Q}\right) & \text{if } \nu = 0\\ 0 \text{ otherwise}\end{cases} \quad (4.27)$$

In the case of $\nu = 0$, that is when μ is a multiple of ρ, the expression above matches the quantization-only spur expression from equations (3.20) and (3.21). Intuitively, this can be understood by noting that the period of the quantization error K_Q (= K/ρ) is ρ times smaller than the buffer (and the total) error period K. Thus, the fundamental frequency of the quantization spectrum is ρ times higher than that of the buffer (and the total) error.

4.5.2 Buffer Error Spurs

This section considers the buffer error spurs at the location of the quantization error spurs ($m = \mu\rho$). It can be shown that the buffer errors are zero at the quantization error

spur locations when N is a factor of q. On the other hand, if N is not a factor of q, simulations show that the buffer error spurs are greatly smaller than the quantization error spurs at the quantization spur locations. Proving this analytically for any N is still an open problem. Analysis that follows shows that the buffer error spurs are zero at the quantization spur locations when the number of buffers, N, is a factor of q.

The buffer error spurs at the locations of quantization error spurs ($m = \mu\rho$) can be expressed as

$$J_m^B\Big|_{m=\mu\rho} = \frac{-A}{pN}\sum_{l=0}^{2K-1} b_e[l]\exp\left(\frac{-j2\pi\mu\rho l}{2K}\right). \tag{4.28}$$

With a change of variable $l = \alpha(2K_Q) + \beta$ with the limits $l = 0, 1, \ldots, 2K - 1$ replaced by $\alpha = 0, 1, \ldots, \rho - 1$ and $\beta = 0, 1, \ldots, 2K_Q - 1$ in the first sum above,

$$\begin{aligned}&\sum_{l=0}^{2K-1} b_e[l]\exp\left(\frac{-j2\pi\mu\rho l}{2K}\right) = \\ &\sum_{\alpha=0}^{\rho-1}\sum_{\beta=0}^{2K_Q-1} b_e[2\alpha K_Q + \beta]\exp\left(\frac{-j2\pi\mu\rho\left(2\alpha K_Q + \beta\right)}{2K}\right).\end{aligned} \tag{4.29}$$

Using the definition of $b_e[l]$ from equation (4.8), with $p = q+1$, the first term in the right hand side of the summand above is simplified below

$$\begin{aligned}b_e[2\alpha K_Q + \beta] &= (-1)^{(2\alpha K_Q+\beta)} b\left[\left\langle Q\left(\frac{\left(2\alpha K_Q + \beta\right)(q+1)N}{2q}\right)\right\rangle_N\right] \\ &= (-1)^{\beta} b\left[\left\langle Q\left(\frac{2\alpha K_Q qN + \beta qN + 2\alpha K_Q N + \beta N}{2q}\right)\right\rangle_N\right] \\ &= (-1)^{\beta} b\left[\left\langle Q\left(\frac{2\alpha K_Q N}{2q} + \frac{\beta N}{2q}\right)\right\rangle_N\right].\end{aligned} \tag{4.30}$$

Under the condition that N is a factor of q, gcd(N,q) = N so that $K_Q = q/N$,

$$b\left[\left\langle Q\left(\frac{2\alpha K_Q N}{2q}+\frac{\beta N}{2q}\right)\right\rangle_N\right]= \\ b\left[\left\langle Q\left(\alpha+\frac{\beta}{2K_Q}\right)\right\rangle_N\right]=b\left[\left\langle \alpha+Q\left(\frac{\beta}{2K_Q}\right)\right\rangle_N\right]. \tag{4.31}$$

For $Q(\cdot)$ = floor($\cdot$) for quantization and $\beta < 2K_Q$, we have $Q(\beta/(2K_Q))=0$ and

$$b\left[\left\langle \alpha+Q\left(\frac{\beta}{2K_Q}\right)\right\rangle_N\right]\Bigg|_{Q=\text{floor}} = b[\alpha]. \tag{4.32}$$

Thus the first term in the right hand side of the summand in (4.29) is independent of β. Next observe that the exponential term in equation (4.29) depends only on β

$$\exp\left(\frac{-j2\pi\mu\rho\left(2\alpha K_Q+\beta\right)}{2K}\right)=\exp\left(\frac{-j2\pi\mu\beta}{2K_Q}\right). \tag{4.33}$$

Therefore, the buffer error spur double summation can be separated into a product of two sums as

$$J^{B}_{m=\mu\rho}\Big|_{Q=\text{floor}} = \frac{-A}{pN}\left(\sum_{\alpha=0}^{\rho-1} b[\alpha]\right)\left(\sum_{\beta=0}^{2K_Q-1}(-1)^{\beta}\exp\left(\frac{-j2\pi\mu\beta}{2K_Q}\right)\right)=0. \tag{4.34}$$

The second term is zero for $\mu > 0$. Thus, the buffer error spurs (except at DC for $\mu = 0$) at the quantization error spur locations are zero. Note that the derivation of equation (4.34) uses two assumptions. First, the number of buffers N is assumed to be a factor of q (or

equivalently N is a power of 2, q being a power of 2). This is often the case for implementation ease of the tap selection logic. All the published implementations of DTC ([4.3]-[4.5], [4.11]) satisfy this condition. The second assumption concerns the type of phase quantization. The proof above used truncation as the method of quantization. If rounding is used instead of truncation, the same final result can be obtained by redefining the limits in equation (4.23) for $l = -K_Q$ to $2K\text{-}1\text{-}K_Q$, so that a change of variables to α and β yields

$$J_m^B\Big|_{m=\mu\rho} = \frac{-A}{pN}\sum_{l=-K_Q}^{2K-1-K_Q} b_e[l]\exp\left(\frac{-j2\pi\mu\rho l}{2K}\right) = \sum_{\alpha=0}^{\rho-1}\sum_{\beta=-K_Q}^{K_Q-1} b_e[2\alpha K_Q+\beta]\exp\left(\frac{-j2\pi\mu\rho\left(2\alpha K_Q+\beta\right)}{2K}\right). \tag{4.35}$$

For $Q(\cdot) = \text{round}(\cdot)$ and $-K_Q \le \beta < K_Q$, $Q(\beta/(2K_Q)) = 0$, the result is

$$J_m^B\Big|_{m=\mu\rho,Q=\text{round}} = 0\ . \tag{4.36}$$

Example: Consider a DTC with $N = 8$ buffers with desired output period $T = (p/q)\,T_{REF} = (33/32)\times T_{REF}$. Since, the number of buffers is a factor of the denominator q in the output period control word, the spur locations due to buffer errors and quantization errors can be separated. The spur fundamental is at $F/q = F/32$. The spurs for $m = 1, 2, \ldots, 31$ can be divided into buffer error spurs (J_m^B) that are at all m locations except $m = 8$, 16 and 24, at these locations the quantization error spurs are present. Simulated spurs (using a randomly chosen set of buffer errors) are shown in Figure 4.3. Dashed lines show the exact and approximate total spurs for $m = 1,2,\ldots, 31$. Solid lines show the quantization error component (red ×) and buffer error component (cyan □). As expected, the quantization component is non-zero only for $m = 8$, 16, 24, while the buffer is zero at those locations.

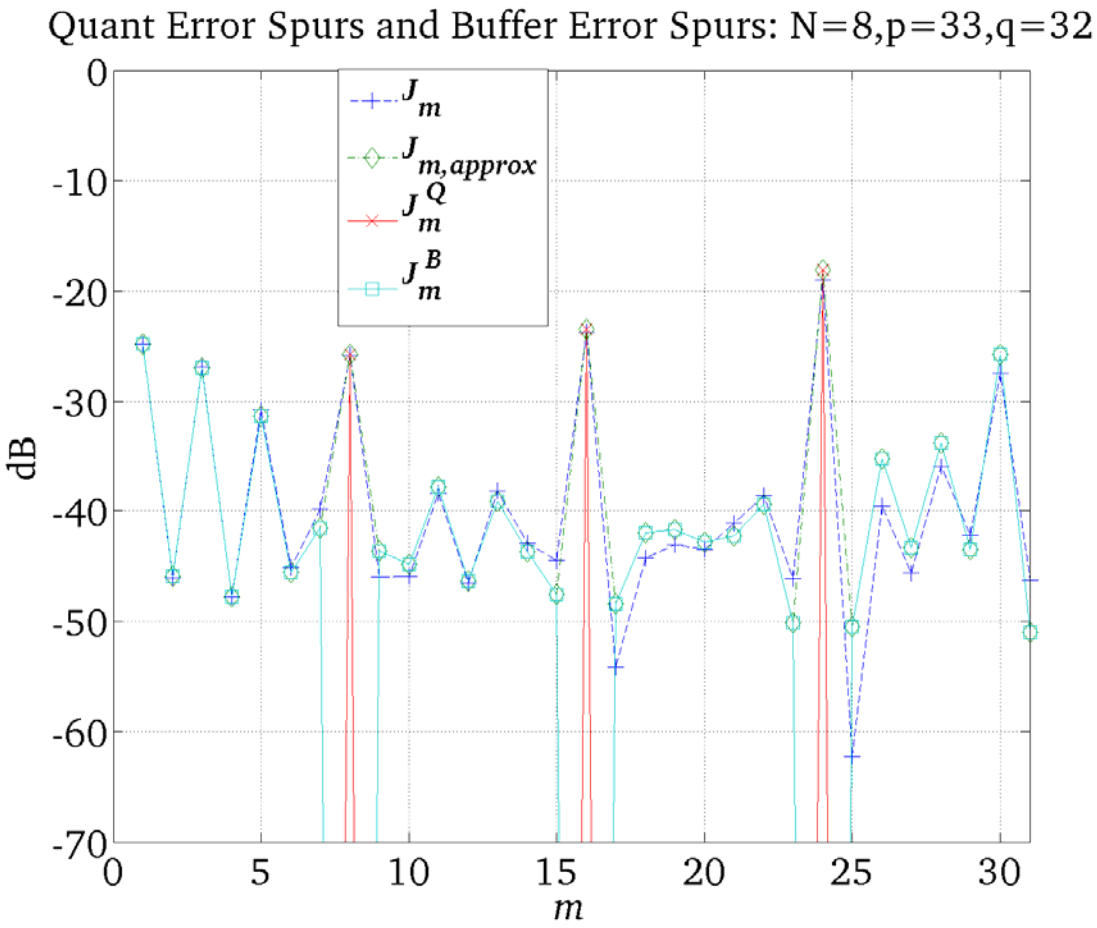

Figure 4.3 Spectrum for $F = (32/33)\text{x}F_{REF}$ using a $N = 8$ buffer DL.

4.6 Measurement Results

In this section measured results from a DTC synthesizer IC synthesized in 90nm CMOS process [4.11] is evaluated relative to theoretical predictions. The DTC uses an $N = 32$ tap delay line running at a reference frequency $F_{REF} = 1000$ MHz. Figure 4.4 and Figure 4.5 show the verification of the spur permutation relation in equation (4.20). The two output frequencies use the same $q = 4$ for two values of p: $p_1 = 5$ and $p_2 = 7$ with output frequencies $F_1 = 800$ MHz and $F_2 = 571.428$ MHz. There are three sub-harmonic ($m = 1$, 2 and 3) spurs in both cases marked by coordinated marker numbers.

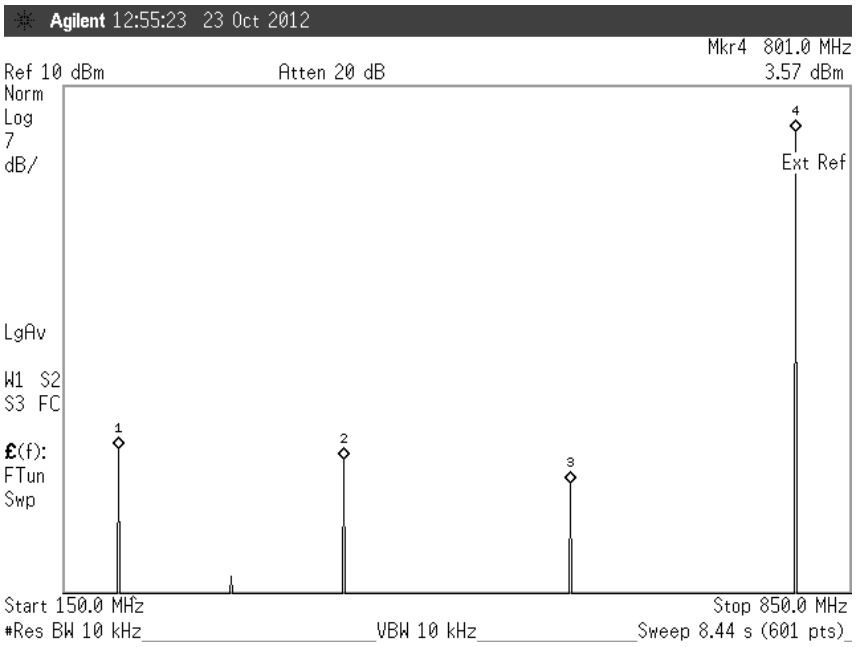

Figure 4.4 $F_1 = (4/5)xF_{REF} = 800$ MHz with three spurs at m $(F_1/4)$ for $m = 1$, 2 and 3 shown by respectively numbered markers.

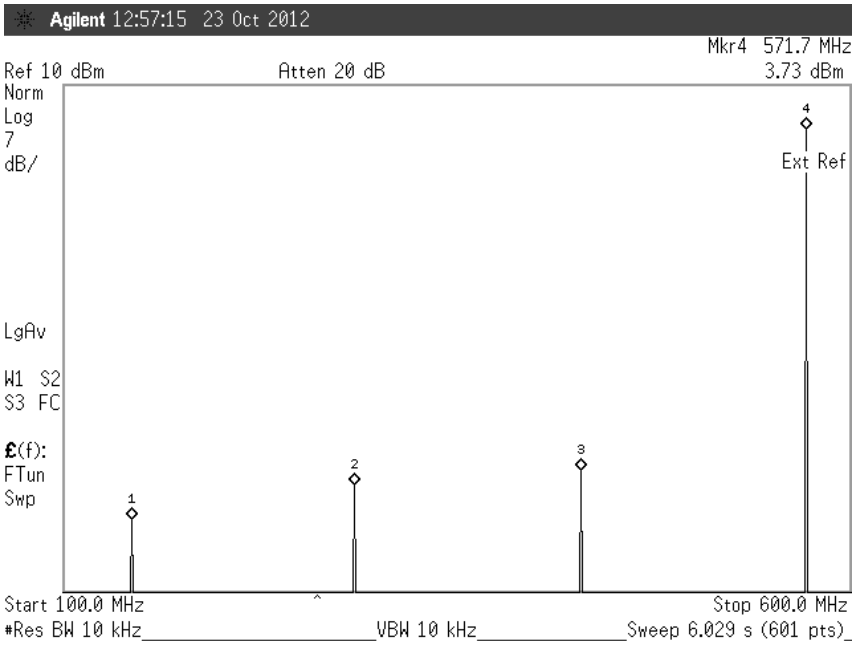

Figure 4.5 $F_2 = (4/7)xF_{REF} = 571.428$ MHz with three spurs at m $(F_2/4)$ for $m = 1$, 2 and 3 shown by respectively numbered markers.

As per equation (4.20) it can be seen that the order of the spurs gets reversed and scaled by a factor of $20\log_{10}(5/7) = 2.92$ dB. Figure 4.4 and Figure 4.5 show this to be the case. In both the figures the top lines correspond to the reference power level of 10 dBm. The vertical scale is identical in both the figures, however, the horizontal scale is different to account for the two different output frequencies. Spurs for one case can be easily predicted (location and magnitude) from the other case.

The validity of equation (4.20) for spur prediction is further evaluated as follows. Figure 4.6 shows the measured spur spectra for the case of $F_2 = (32/35)\ F_{REF}$ together with predicted spur spectra based on the measurement of the spur spectra at another output frequency of $F_1 = (32/33)\text{x}F_{REF}$. The prediction according to equation (4.20) for $p_1 = 33$, $p_2 = 35$ and $q = 32$ gives

$$J[m,35] \approx \frac{33}{35} J[\langle bm \rangle_{64},33], \text{ with } b = \langle 35^{-1} \cdot 33 \rangle_{64} = 43\ . \qquad (4.37)$$

The plots in Figure 4.6 show that the prediction is fairly close (spur locations match 100% while magnitudes are within 10 dB as explained below). The quality of the prediction is measured with the prediction error plotted in Figure 4.7. The prediction error is within ±5 dB in most cases. More precisely, the cumulative distribution function of the absolute prediction error in dB is plotted in Figure 4.8. It shows that 80% prediction errors are within 5 dB. Similar cumulative distribution function of prediction error for another case of $p_1 = 257$, $p_2 = 259$ and $q = 256$ is shown in Figure 4.9. Again, about 80% prediction errors are within 5dB. It is observed that the larger prediction errors occur at places where the predicted spur value itself is smaller than -60 dBc. The final plot in Figure 4.10 shows the prediction error versus the measured spurs that were being predicted. It is seen in Figure 4.10 that most prediction errors of more than 5 dB had a small spur value at -60 dBc or below. Simulations have shown that the errors of the first-order approximation used in equation (4.9) have a similar error profile. This means that the prediction errors are largely due to errors of making the first-order approximation.

Recall, however, that the approximation is key to the entire classification of all the spur patterns.

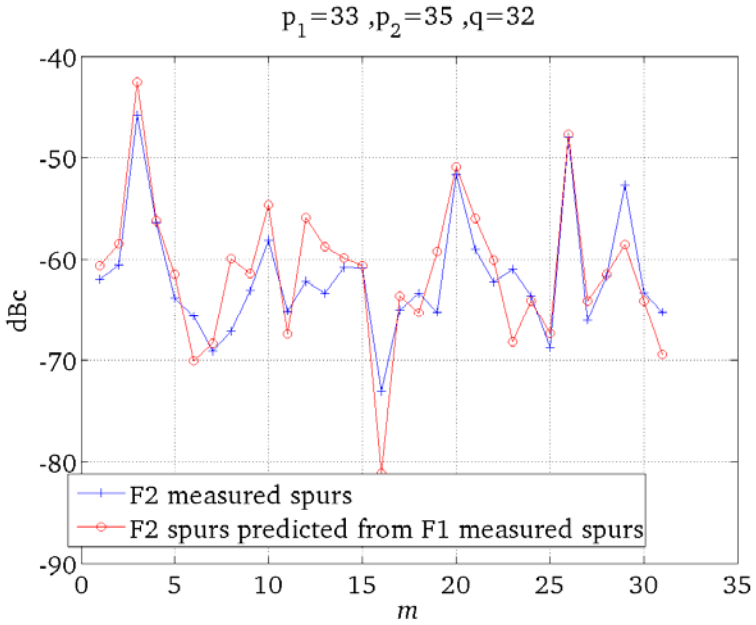

Figure 4.6 Comparison of measured spurs (blue +)for $F_2 = (32/35)xF_{REF}$ and those predicted from the measured spurs (red o) at $F_1 = (32/33)xF_{REF}$

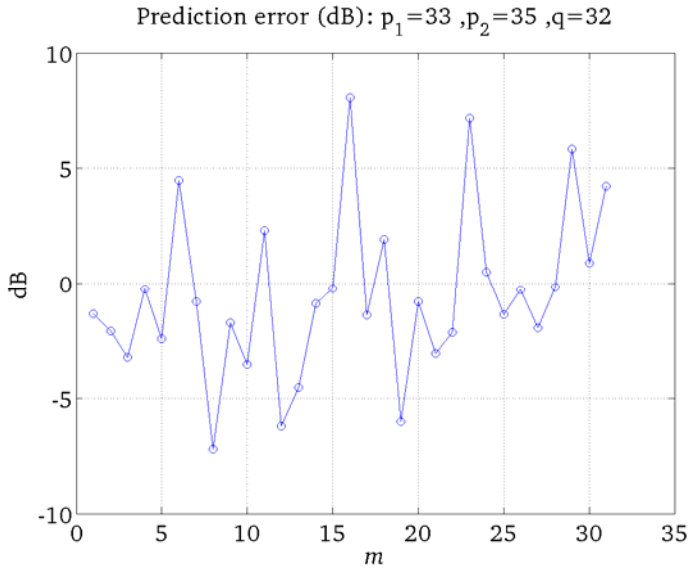

Figure 4.7 Prediction error in Figure 4.6 between the measured spurs for $F_2 = (32/35)xF_{REF}$ and those predicted from the measured spurs at $F_1 = (32/33)xF_{REF}$

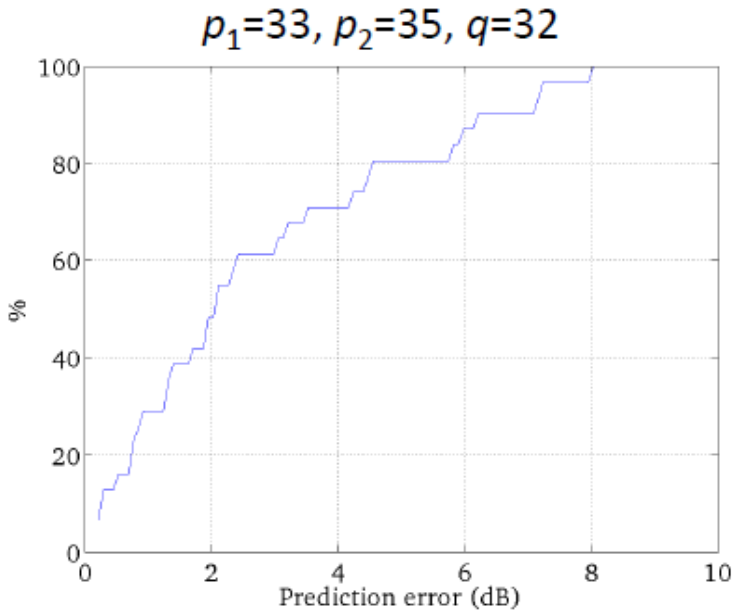

Figure 4.8 Cumulative distribution function of the prediction error between the measured spurs for F_2 = (32/35)xF_{REF} and those predicted from the measured spurs at F_1 = (32/33)xF_{REF}

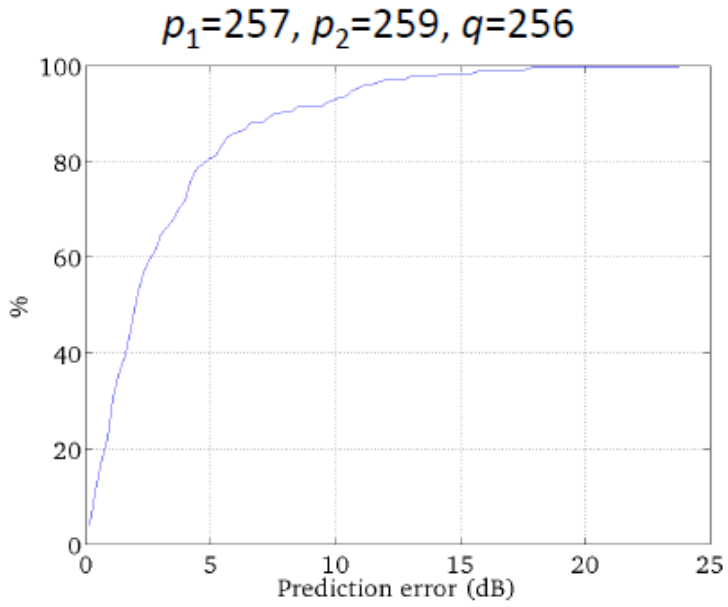

Figure 4.9 Cumulative distribution function of the prediction error between the measured spurs for F_2 = (259/256)xF_{REF} and those predicted from the measured spurs at F_1 = (257/256)xF_{REF}

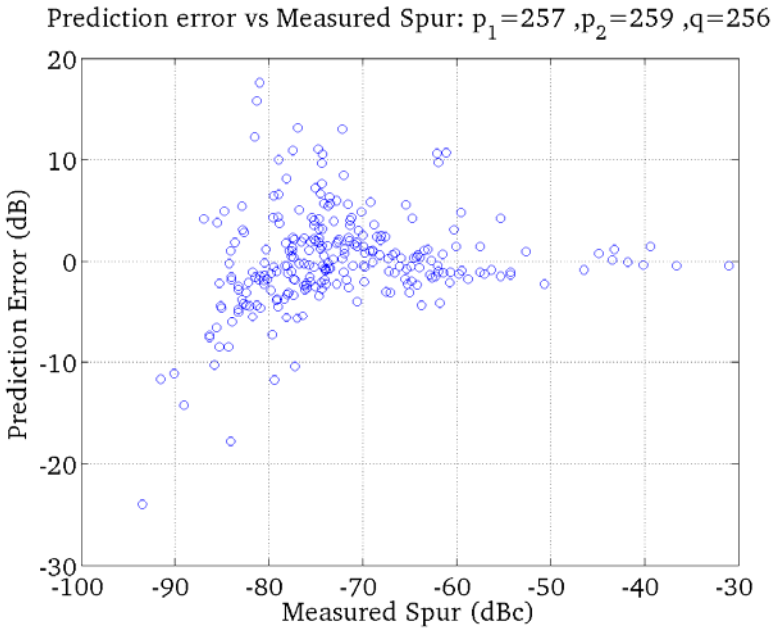

Figure 4.10 Prediction error versus measured spur. Larger prediction errors in dB occur for very weak spurs (< -60 dBc).

4.7 Chapter Summary

Sub-harmonic spurs due to periodic edge errors, buffer delay errors and quantization errors of a digital-to-time conversion (DTC) synthesizer have been analyzed in this chapter for all possible output frequencies. Results here extend an earlier application (see equation (3.34) from chapter 3) of the DFT axis-scaling property to the case of non-ideal delay line. Table 4.2 summarizes the expressions for quantization error spurs from [4.20] and mismatch error spurs developed in this chapter. Further, conditions are derived in this chapter, under which the spurs due to buffer delay errors and those due to quantization errors, can be separated. This condition (number of buffers N be a power of 2 so that it is a factor of q) is naturally satisfied in most practical implementations. The results of this chapter apply to spurs of the flying adder (FA) based DTC as well. The insight into the edge error spectra structure allows the error spectra for *all* $2^{(I+M)}$ output frequencies (for frequency control words with I integer and M fractional bits) to be classified in just M

classes. The spectra within each class are systematically rearranged and scaled versions of each other. Spur measurements on an actual 90nm DTC synthesizer support the theoretical results.

Table 4.2 Summary of results for a N buffer delay line [Assumed here: N is a power of 2 (true in most implementations) and hence, a factor of q and $K_Q = q/\gcd(N,q)$].

Description	Expression
Desired output control word (p/q) in fixed point binary format (p odd, q = power of 2)	$T = \frac{p}{q} T_{REF}\ ,\ F = \frac{q}{p} F_{REF}$
Mismatch spur fundamental frequency	F/q ($=F_{REF}/p$)
Mismatch spur locations for $m = 1, 2, \ldots, q-1$ (except for multiples of N which are the locations of quantization spur)	m x (F/q)
Mismatch spur amplitudes	Needs to be computed using equation (4.23) for a given buffer error profile
Quantization spur fundamental frequency	N x (F/q)
i^{th} worst quantization spur amplitude (w.r.t. the desired tone output) (dBc) (equation (3.48) in chapter 3)	$20 \log_{10}\left(\frac{\pi \gcd(N,q)}{pN\left\lVert 1 - \exp\left(\frac{-ji\pi}{K_Q}\right)\right\rVert} \right)$
Frequency location of the i^{th} worst quantization spur (equation (3.49) in chapter 3)	$\left\langle \left(K_Q - i\right)\langle p\rangle_{2K_Q} \frac{N}{\gcd(q,N)} \right\rangle_{2K_Q} \times \frac{F}{K_Q}$

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5 Thesis Summary and Future Research

The structure of the sub-harmonic spur spectra of a digital-to-time conversion (DTC) based frequency synthesizer has been modeled and analytical expressions derived for spur locations and strength levels. Time-frequency axis-scaling property is shown to apply to the linkage between spur spectra of a DTC synthesizer for different frequency settings. The insight and method of classification of the DTC spur spectra developed in this thesis greatly simplifies the characterization of spurs for all possible output frequencies. In the case of quantization error spurs, all the locations and strengths of spurs are theoretically predicted. Measured spur values match all the spectral locations predicted by the analysis and have strengths within 3-4 dB of the analytically predicted values. For buffer mismatch error spurs, all the spectral locations are completely predicted. The strengths of the mismatch spurs depend on the mismatch errors that cannot be measured directly. However, measurements verify that the validity of the DFT axis-scaling property is capable of predicting to within 5 dB for 80% (and within 10 dB for 95%) of the actually observed spurs. The remaining 20% of spur cases that involve higher prediction error are for spurs that are more than 60 dB weaker than the desired signal.

In chapter 2, the time/frequency axis-scaling property of Discrete Fourier Transforms (DFT) is presented with the necessary and sufficient conditions on the digital scaling integer that require it to be relatively prime with the length of the DFT. The DFT of the time scaled (permuted) sequence is the DFT of the original sequence scaled (permuted) by the modulo inverse of the scaling factor.

In chapter 3, the sub-harmonic spurs due to the quantization errors in a DTC synthesizer have been analyzed for all possible output frequencies. In this analysis, an ideal delay line (DL) is assumed so that the edge errors are entirely due to quantization and not buffer delay. An elaborate structure of the quantization error sequences for different frequency control words is described in the context of the DFT axis-scaling property. A first-order linear approximation allows the structure to be evaluated in the frequency domain by

applying the time/frequency axis-scaling property of the Discrete Fourier Transform (DFT). The results derived in this chapter also apply to the flying adder (FA) based synthesizer, although the approximation error rises for output frequencies above the reference frequency. The insight into the quantization spectra structure provided by the chapter 3 model allows the quantization spectra for *all* $2^{(I+M)}$ output frequencies to be classified with M classes. The spectra within each class are modulo permutations and scaled versions of each other. Analytical expressions providing the location and value of the i^{th} worst spur were developed. It was also shown that the two common methods of quantization, truncation or rounding, lead to identical non-DC sub-harmonic spur magnitudes. This justifies the use of truncation, rather than hardware-intensive rounding, as the method of quantization. Measurements on a DTC synthesizer fabricated on 90-nm CMOS process validate the theoretical results.

In chapter 4, the sub-harmonic spurs due to periodic edge errors for a non-ideal delay line were considered. This means that both buffer delay errors as well as phase quantization errors were present. Extending the methods of chapter 3, the spur spectra of a DTC synthesizer with non-ideal delay line were analyzed for all possible output frequencies. Further, conditions were derived under which the spurs due to buffer delay errors and those due to quantization errors can be separated. This condition (that the number of buffers N be a power of 2) is naturally satisfied in most practical hardware implementations. The results of this chapter also apply to spurs of the flying adder (FA) based DTC architecture. The insight into the edge error spectra structure allows the error spectra for *all* $2^{(I+M)}$ output frequencies (for frequency control words with I integer and M fractional bits) to be classified in just M classes. The spectra within each class are modulo permutations and scaled versions of each other. Spur measurements taken on an actual 90nm DTC synthesizer supported the theoretical results.

Further research can enhance the modeling and analytic fidelity of the characterization of DTC spurs. The next three sections address these research areas.

5.1 Dynamic Edge Errors and Dither Analysis

The entire analysis in this thesis considers only static errors, either stemming from the buffer mismatch or due to quantization. There is no change in these errors over time. A practically important extension, modeling edge errors of a DTC would permit changes dynamically over time. This change over time could be either deterministic or random, such as in the case of dither. Loosely speaking, static errors give rise to discrete spurious tones, while dynamic errors give rise to spread (non-discrete) power spectral density. Deliberate insertion of random dither is used in analog-to-digital converter (ADCs) designs to help mitigate effects of quantization [5.1]. Similar to ADCs, the insertion of dither also mitigates quantization spurs DTC-based synthesizers [5.2]. A rigorous theoretical analysis of how and why dither helps DTC spectrum is an open area for research. Further, determining the effect of shaping of the quantization noise using sigma-delta converters on the DTC spectrum is an additional area for research.

5.2 Use Higher Order Approximation

This future research area was suggested by Prof. Marple, my adviser. Chapters 3 and 4 use the first-order linear approximation of the exponential (see equation (3.16)). This approximation is a contributor to the error between measured spurs and predicted spurs, especially at lower spur levels (see Figure 4.7 in section 4.6). The error in prediction can be mitigated by considering higher order terms in the analysis. For example, a third-order approximation for the exponential term is

$$\exp(j\theta) \approx 1 + (j\theta) + \frac{(j\theta)^2}{2} + \frac{(j\theta)^3}{6} \qquad (3.52)$$

One may start with the consideration of the second-order approximation and extend the technique to the third order approximation.

5.3 Buffer Mismatch Spur Statistics

Another enhancement of the modeling fidelity of this thesis can be done by modeling the statistical properties of the buffer mismatch errors. Based on the error statistical properties, useful insight may be derived about the statistics of the mismatch error spur spectra using equation (4.23). The problem can be briefly stated as follows. The edge delay error for the l^{th} buffer output for $l = 0, 1, 2, \ldots, N-1$ can be written as

$$b_{UNLOCKED}\ [l] = \sum_{k=0}^{l-1} d_{UNLOCKED}\ [k] - l \times d\ . \tag{5.1}$$

The variable $d_{UNLOCKED}[k]$ is the delay of the k^{th} buffer before the delay line is locked and d is the ideal delay of each buffer. When the delay line is locked so that every unlocked delay value gets scaled by a factor α using a tuning mechanism to apply the constraint, the result is

$$b_{LOCKED}\ [N] = \alpha \times \sum_{k=0}^{N-1} d_{UNLOCKED}\ [k] - N \times d\ = 0\ . \tag{5.2}$$

With the locking constraint, the tuning factor can be solved as

$$\alpha\ = \frac{N \times d}{\sum_{k=0}^{N-1} d_{UNLOCKED}\ [k]}\ . \tag{5.3}$$

The buffer errors when the DL is locked are given by

$$b[l] = \alpha \sum_{k=0}^{l-1} d_{UNLOCKED}\ [k] - l \times d\ . \tag{5.4}$$

The unlocked delay may be modeled using a suitable probability density function (PDF). The challenge is to derive the statistics for $b[l]$. This may involve deriving the entire PDF, or just the mean and variance may suffice for $b[l]$.

5.4 Relating Cross-Class Spur Spectra

This future research was suggested by Prof. Faridani of OSU Math department. Chapters 3 and 4 of this thesis suggest a way to relate error spectra for two output frequencies for which the output periods T_1 and T_2 are related to the reference period T_{REF} for the same value of q as

$$\frac{T_1}{T_{REF}} = \frac{p_1}{q} \text{ and } \frac{T_2}{T_{REF}} = \frac{p_2}{q}. \tag{5.5}$$

Here p_1 and p_2 are two different odd numbers and q is a power of 2. There is a possibility to generalize this to the case of two output frequencies with *different* values of q. The first step to doing this would be to relate the spur spectra for two output frequencies with two sequential powers of 2 for the two values of q. Choosing $p_1 = q_1+1$ and $p_2 = q_2+1$,

$$\frac{T_1}{T_{REF}} = \frac{q+1}{q} \text{ and } \frac{T_2}{T_{REF}} = \frac{2q+1}{2q}. \tag{5.6}$$

In this particular case, it can be shown that the buffer error sequences for the two frequencies are related using equations (4.10) as

$$\begin{aligned}&\{b_{e,2}[l]\}_{l=0}^{2(2K)-1} = \\ &\{b_{e,1}[0], b_{e,1}[1], b_{e,1}[0], b_{e,1}[1], \\ &b_{e,1}[2], b_{e,1}[3], b_{e,1}[2], b_{e,1}[3], \\ &\ldots, \\ &b_{e,1}[2K-2], b_{e,1}[2K-1], b_{e,1}[2K-2], b_{e,1}[2K-1]\}.\end{aligned} \tag{5.7}$$

Note that the sequence $b_{e,2}$ is constructed by repeating every two-sample set of the sequence $b_{e,1}$ at a time. Conversely, the sequence $b_{e,1}$ is found by 'bunched' decimation $b_{e,2}$ by a factor of 2. Here bunching refers to taking two samples and skipping two samples. The problem to relate the spectra for the two cases is now transformed to the application of bunched sampling results described in [5.3] and [5.4]. The relationship between the DFTs of $b_{e,1}$ and $b_{e,2}$ may help relate spur spectra of two elements of a principal set of spur spectra described in chapter 3 and 4. The ultimate goal here would be to determine if the principal set can be further reduced to a smaller set of spur spectra.

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Appendices

A. Number Theory Results

The appendix contains proofs of some background number theory results that are used in the proof of the DFT time/frequency scaling theorem. These are included for the sake of completeness. More elaborate treatment can be found in [2.4], [2.5] and [2.6].

We start with a definition of the Euler's phi-function (also known as the totient function) of an integer N

$$\varphi(N) = \left|\{0 \le i < N \mid \gcd(i, N) = 1\}\right| \tag{A.1}$$

The notation denotes the number of positive integers less than and relatively prime to N. The Euler's phi-function of a number N can be computed as follows. First factorize the number as product of powers of prime numbers

$$N = p_1^{n_1} p_2^{n_2} \ldots p_r^{n_r} = \prod_{l=1}^{r} p_l^{n_l} \tag{A.2}$$

Then, the Euler's phi-function is

$$\varphi(N) = \prod_{l=1}^{r} p_l^{n_l} \left(1 - \frac{1}{p_l}\right) \tag{A.3}$$

For example, for the case of $N = 7$ presented in the paper, $\varphi(7) = 7^1(1 - 1/7) = 6$.

Fermat's Little Theorem (due to Euler, stated here without proof):
If integers a and N are relatively prime, then

$$\left\langle a^{\varphi(N)} \right\rangle_N = 1 \tag{A.4}$$

where, $\varphi(N)$ is the Euler's phi-function.

Lemma A.1: Given integers N, for every $a < N$ which is relatively prime with N, there exists a unique integer $b < N$ such that,

$$\left\langle ab \right\rangle_N = 1 \tag{A.5}$$

Such a number b is a (since uniqueness has not yet been proven) multiplicative inverse of the number a in modulo N sense.

Proof of Lemma A.1: First consider the existence of b. This follows from Fermat's Little Theorem since a and N are relatively prime with $b = \left\langle a^{\varphi(N)-1} \right\rangle_N$

$$\left\langle ab \right\rangle_N = \left\langle a.a^{\varphi(N)-1} \right\rangle_N = \left\langle a^{\varphi(N)} \right\rangle_N = 1. \tag{A.6}$$

Now consider the uniqueness of the multiplicative inverse. This is proved using reduction-ad-absurdum. Consider that the converse is instead true, that is, there are two distinct inverses of a, b_1 and b_2, both less than N such that $\left\langle ab_1 \right\rangle_N = 1$ and $\left\langle ab_2 \right\rangle_N = 1$ .Further assume that $b_1 < b_2$. Taking the difference yields

$$\langle a(b_2 - b_1)\rangle_N = 0 \tag{A.7}$$

Since a is relatively prime with N, the difference $(b_2 - b_1)$ must be a multiple of N. In other words, for some positive integer j, $b_2 = b_1 + jN$. Since, they are distinct and both less than N, this is impossible. Hence the assumption about non-uniqueness of multiplicative inverse is not true.

Lemma A.2: For integer N and number a that is relatively prime to N, and $0 \le n_1 < n_2 < N$

$$n_1 \ne n_2 \Rightarrow \langle an_1\rangle_N \ne \langle an_2\rangle_N \tag{A.8}$$

Proof of Lemma A.2: Again assume that the converse is true. That is, $\langle an_1\rangle_N = \langle an_2\rangle_N$. Similar to the proof above it then follows that such distinct numbers n_1 and n_2, both less than N, cannot exist.

The above lemma means that for all numbers in the sequence $\{\langle an\rangle_N\}$ are distinct for $n = 0, 1, \ldots, N-1$. Since the sequence is mapped from $\{0, 1, \ldots, N-1\}$ to itself, this means that all the numbers are mapped to exhaustively.

B. Fourier Transform of Output of DTC with an Ideal DL

Rewriting equation (3.11), the output of a DTC synthesizer with an ideal DL with N buffers, each with a delay d

$$x(t) = A\sum_{i=-\infty}^{\infty}\sum_{k=0}^{K_Q-1}\left\{\begin{matrix} u(t - t_{r,Actual}[k + iK_Q]) \\ -u(t - t_{f,Actual}[k + iK_Q]) \end{matrix}\right\}. \qquad \text{(B.1)}$$

In order to find the frequency domain representation of the output, it is easier to consider the first derivative $x'(t)$ with a change in the order of the double summation

$$x'(t) = A\sum_{k=0}^{K_Q-1}\sum_{i=-\infty}^{\infty}\left\{\begin{matrix} \delta(t - [(iK_Q + k)T + q_r[k]]) - \\ \delta(t - [(iK_Q + k + 0.5)T + q_f[k]]) \end{matrix}\right\}. \qquad \text{(B.2)}$$

Note that for a given value of k, the infinite internal sum (over l) contains uniformly spaced train of impulses. The Fourier Transform (FT) of each of the train of infinite sum of impulses is well-known. Note that the train of impulses (B.2) is separated by K_QT. Adding the time-domain shift property

$$\Im\left\{\sum_{i=-\infty}^{\infty}\delta(t - iK_QT)\right\} = \frac{1}{K_QT}\sum_{m=-\infty}^{\infty}\delta\left(f - \frac{m}{K_QT}\right). \qquad \text{(B.3)}$$

With a time domain shift τ

$$\Im\left\{\sum_{i=-\infty}^{\infty}\delta(t - iK_QT - \tau)\right\} = \frac{e^{(-j2\pi f\tau)}}{K_QT}\sum_{m=-\infty}^{\infty}\delta\left(f - \frac{m}{K_QT}\right). \qquad \text{(B.4)}$$

Note that the time-domain shift in (B.2) is $\tau = kT + q_r[k]$

$$\Im\left\{\sum_{i=-\infty}^{\infty}\delta(t-[(iK_Q+k)T+q_r[k]])\right\}= \frac{e^{(-j2\pi f[kT+q_r[k]])}}{K_QT}\sum_{m=-\infty}^{\infty}\delta\left(f-\frac{m}{K_QT}\right). \tag{B.5}$$

The FT of the derivative of the output can be written as

$$X'(f)=\frac{A}{K_QT}\sum_{m=-\infty}^{\infty}\delta\left(f-\frac{m}{K_QT}\right) \left(\sum_{k=0}^{K_Q-1}e^{(-j2\pi f[kT+q_r[k]])}-e^{(-j2\pi f[(k+0.5)T+q_f[k]])}\right). \tag{B.6}$$

Finally, using the property for FT of a derivative, the FT of the output $x(t)$ is

$$X(f)=\frac{A}{j2\pi fK_QT}\sum_{m=-\infty}^{\infty}\delta\left(f-\frac{m}{K_QT}\right) \left(\sum_{k=0}^{K_Q-1}e^{(-j2\pi f[kT+q_r[k]])}-e^{(-j2\pi f[(k+0.5)T+q_f[k]])}\right). \tag{B.7}$$

C. On the First-order Approximation of the Exponential

The accuracy of the linear approximation (see equation (3.16)) can be studied by considering the maximum absolute value of the term inside the exponential. Since the maximum absolute value of the quantization error is d (for floor(·), and $d/2$ for round(·)), for $m' < K_Q$ (quantization spurs at frequencies less than the output frequency)

$$\left|\frac{j2\pi m'q_r[i]}{K_QT}\right|<\frac{2\pi qd}{pT_{REF}}=\frac{2\pi(q/N)}{2p}\le\frac{2\pi}{2N}. \tag{C.1}$$

The last inequality is true because q is not greater than p. With this bound, the ratio of the approximation error magnitude to the approximated term magnitude can be is shown in the Figure C.1. For example, for a value of $N = 8$, the approximation error is 80 dB below the term being approximated.

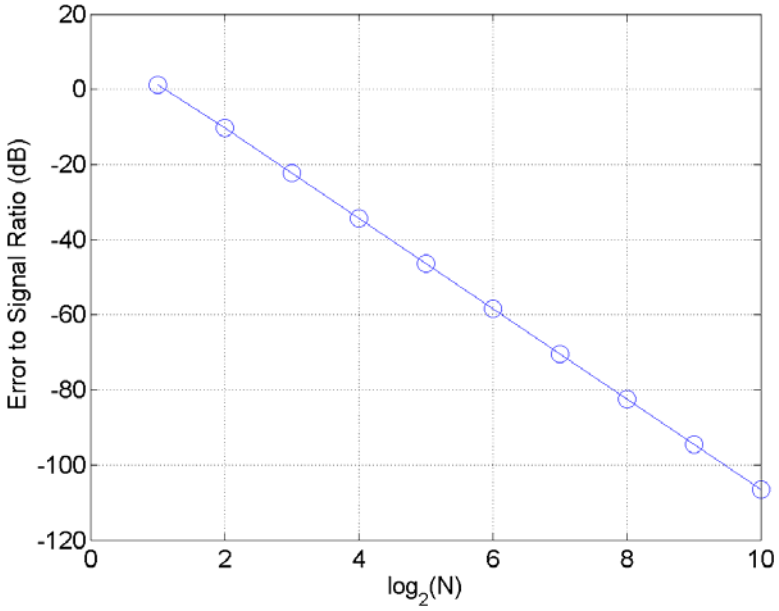

Figure C.1 Error caused by the first-order approximation of the exponential

D. Series Expansion Used for Worst Quantization Spur

Let S denote the series

$$S = \sum_{l=0}^{2K_Q-1} la^l \,. \tag{D.1}$$

Then, a x S is

$$aS = \sum_{l=0}^{2K_Q-1} la^{l+1} = \sum_{l=1}^{2K_Q} (l-1)a^l \,. \tag{D.2}$$

Taking the difference of (D.1) and (D.2)

$$(1-a)S = \sum_{l=1}^{2K_Q-1} a^l - (2K_Q - 1)a^{2K_Q} \,. \tag{D.3}$$

Then,

$$S = \frac{1}{1-a}\left(\frac{a - a^{2K_Q}}{1-a} - (2K_Q - 1)a^{2K_Q} \right). \tag{D.4}$$

In particular if $a = \exp\{-j2\pi[K_Q+m]/(2K_Q)\}$,

$$\begin{aligned} & a^{2K_Q} = 1 \Rightarrow S\big|_{a=\exp\left(-j2\pi[K_Q+m]/2K_Q\right)} \\ & = \frac{1}{1-a}\left(\frac{a-1}{1-a} - (2K_Q - 1) \right) = \frac{2K_Q}{1-a} \,. \end{aligned} \tag{D.5}$$

E. Quantization Spur Magnitudes: Truncation vs Rounding

Recall that for the special value of $p = p_0$ that satisfies (3.37), the quantization error sequence for $l = 0, 1, \ldots, 2K_Q$ can be rewritten from (3.39) as

$$q_e[l, p_0] = (-1)^l \left[Q\left(\frac{l}{2K_Q} \right) - \frac{l}{2K_Q} \right]. \tag{E.1}$$

For $l = 0, 1, \ldots, 2K_Q$ two types of quantization methods yield the output

$$Q_{floor}\left(\frac{l}{2K_Q}\right) = 0 \text{ and } Q_{round}\left(\frac{l}{2K_Q}\right) = \begin{cases} 0 \text{ when } 0 \le \left(l/2K_Q\right) < 0.5 \\ 1 \text{ when } 0.5 \le \left(l/2K_Q\right) < 1 \end{cases}. \quad \text{(E.2)}$$

Using the quantization values from equation (E.2), the quantization error sequences in equation (E.1) for the two methods can written as

$$q_{e,floor}[l, p_0] = (-1)^l\left(-\frac{l}{2K_Q}\right) \text{ for } l = 0,1,\ldots,2K_Q - 1 \text{ and}$$

$$q_{e,round}[l, p_0] = \begin{cases} (-1)^l\left(-\frac{l}{2K_Q}\right) \text{ when } l = 0,1,\ldots, K_Q - 1 \\ (-1)^l\left(1 - \frac{l}{2K_Q}\right) \text{ when } l = K_Q, K_Q + 1,\ldots, 2K_Q - 1. \end{cases} \quad \text{(E.3)}$$

From (E.3), $q_{e,round}[l, p_0]$, the error sequence due to rounding may be expressed in terms of, $q_{e,floor}[l, p_0]$, the error sequence due to truncation, as

$$q_{e,round}[l, p_0] = \begin{cases} q_{e,floor}[l, p_0] & \text{when } l = 0,1,\ldots, K_Q - 1 \\ q_{e,floor}[l, p_0] + (-1)^l & \text{when } l = K_Q, K_Q + 1,\ldots, 2K_Q - 1. \end{cases} \quad \text{(E.4)}$$

The DFT of the error sequences due to rounding is the sum of the DFT due to truncation and the DFT of the sequence of $(-1)^l$ for l from K to $2K_Q - 1$, yielding

$$Q_{e,round}[m] = \sum_{l=0}^{2K_Q-1} q_{e,round}[l] e^{\left(\frac{-j2\pi lm}{2K_Q}\right)} = Q_{e,floor}[m] + \sum_{l=K_Q}^{2K_Q-1} (-1)^l e^{\left(\frac{-j2\pi lm}{2K_Q}\right)}. \quad \text{(E.5)}$$

With the definition $a = \exp\{-j2\pi[K_Q+m]/(2K_Q)\}$ (similar to equation (3.42)),

$$\sum_{l=K_Q}^{2K_Q-1}(-1)^l e^{\left(\frac{-j2\pi lm}{2K_Q}\right)} = \sum_{l=K_Q}^{2K_Q-1} a^l = \frac{a^{2K_Q} - a^{K_Q}}{a-1}. \qquad \text{(E.6)}$$

Recognizing that,

$$a^{2K_Q} = 1 \text{ and } a^{K_Q} = e^{\left(\frac{-j2\pi[K_Q+m]}{2}\right)} = -(-1)^m, \qquad \text{(E.7)}$$

the DFT of the error sequence due to rounding from equation (E.5) becomes

$$Q_{e,round}[m] = Q_{e,floor}[m] + \frac{1+(-1)^m}{1-a}. \qquad \text{(E.8)}$$

Recall from equation (3.42) that $Q_{e.floor}[m] = -1/(1-a)$. Using this in equation (E.8),

$$Q_{e,round}[m] = \frac{-1}{1-a} + \frac{1+(-1)^m}{1-a} = \begin{cases} -Q_{e,floor} & \text{when } m \text{ is even} \\ Q_{e,floor} & \text{when } m \text{ is odd} \end{cases}. \qquad \text{(E.9)}$$

Therefore, the magnitude of the quantization error spectra are the same whether rounding is used or truncation is used.

$$\left|Q_{e,floor}[m]\right| = \left|Q_{e,floor}[m]\right| \text{ for } m = 0,1,\ldots,2K_Q - 1. \qquad \text{(E.10)}$$

F. Period of Rising and Falling Tap Sequences

The k^{th} rising and falling edges in the output are generated from taps

$$r_k = \left\langle Q\left(\frac{kNp}{q} \right) \right\rangle_N \text{ and } f_k = \left\langle Q\left(\frac{(k+0.5)Np}{q} \right) \right\rangle_N . \qquad \text{(F.1)}$$

With a substitution (k+q) in place of k in equation (F.1), it can be verified that q is a period of these sequences. That is, for every k,

$$r_k = r_{k+q} \text{ and } f_k = f_{k+q} . \qquad \text{(F.2)}$$

In order to prove that q is the period, it is necessary to prove that no factor of q is a period of these sequences. In order to do this, it is sufficient to consider only the rising edge tap sequence. Suppose that the period is not q, but the period has factor q/α. For every k, this implies $r_k = r_{k+(q/\alpha)}$. In particular, since $r_0 = 0$, so should $r_{q/\alpha}$, $r_{2q/\alpha}$, … be zero. That is, for every l,

$$r_{l(q/\alpha)} = \left\langle Q\left(\frac{lqNp}{\alpha q} \right) \right\rangle_N = \left\langle Q\left(l\frac{Np}{\alpha} \right) \right\rangle_N = 0 . \qquad \text{(F.3)}$$

Consider the case of l = 1. Suppose truncation is used for quantization (other methods have similar arguments). The result is

$$r_{(q/\alpha)} = \left\langle Q\left(\frac{Np}{\alpha} \right) \right\rangle_N = 0 \Rightarrow \frac{Np}{\alpha} = m_1 N + \delta_1 . \qquad \text{(F.4)}$$

where (m_1N) is the multiple of N closest to and less than Np/α, such that floor(Np/α) = m_1N and δ_1, the truncation error, is in [0, 1). Of course, δ_1 cannot be zero, otherwise, (p/α) = m_1 would mean that α has to be 1 (since p and q are relatively prime and so are p and α). One can show that it is possible to find another value of $l = l'$ for which equation (F.3) requires that tap be zero, but equation (F.4) implies that tap be non-zero. Since δ_1 is not zero, and noting that l' = ceil(1/ δ_1) = (1/ δ_1 + ε_1) where ε_1 is the ceiling error, the result is

$$r_{l'(q/\alpha)} = \left\langle Q\left(\text{ceil}\,(1/\delta_1)(m_1N + \delta_1)\right)\right\rangle_N = Q\left(1 + \delta_1\varepsilon_1\right) = 1\,. \qquad \text{(F.5)}$$

This apparent contradiction is due to the incorrect assumption that δ_1 is not zero. Thus, α has to be equal to 1 and hence q is the period of r_k. Similar arguments can be used to prove that the rising and falling edge tap sequences have period $K = q$ if another quantization method is used.