An Abstract of the the Thesis of

Jieyin Zheng for the degree of Master of Science in Electrical and Computer Engineering presented on August 4, 1993.

Title: A Low Ground Bounce CMOS Off–Chip Driver Design

Redacted for privacy

Abstract approved:

Shih–Lien Lu

With the advancement of technology, sub–micron CMOS–only process is available now for Application Specific Integrated Circuits (ASICs). The high integration leads to the need for high pin counts. However voltage supply and ground bounce due to many output drivers switching at the same time is becoming a major problem. In this thesis, a CMOS off–chip buffer design which generates ECL logic levels with lower ground bounce noise is described and demonstrated. The technique used in designing this buffer to reduce voltage noise differs from conventional design techniques. Traditionally there are two general methods to reduce ground bounce. One approach tries to reduce the instantaneous current change (*di/dt*) by increasing (prolonging) the rise and fall time of the signals. The other approach attempts to reduce the parasitic inductance attributed to packaging by using multiple supply pins. Our technique reduces the voltage noise by controlling the instantaneous current change through the reduction of current difference during switching time. Based on this approach, a novel circuit structure is designed. This circuit has a fully symmetrical configuration and is being self–biased through negative feedback. A current injection technique is also used to increase the stability of the circuit. SPICE simulation of the proposed circuit is performed. Comparison and tradeoffs with other approaches are studied.

A Low Ground Bounce CMOS Off-Chip Driver Design

by

Jieyin Zheng

A THESIS

Submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Completed August 4, 1993

Commencement June 1994

APPROVED:

Redacted for privacy

Professor of Electrical & Computer Engineering in charge of major

Redacted for privacy

Head of department of Electrical & Computer Engineering

Redacted for privacy

Dean of Graduate School

Date thesis is presented August 4, 1993

Typed by Jieyin Zheng

ACKNOWLEDGEMENT

First of all, I would like to thank Professor Shih–Lien Lu, my advisor, for his generosity, patience, encouragement, and valuable help during the preparation of this thesis. Secondary, I would like to thank my wife, Quan Wang, for her support. Third, I want to express my gratitude to the faculties and staffs of ECE Department, and my graduate committee members for their help and encouragement. Without all these people, my time would not have been so enjoyable and memorable. Finally, I would like to thank all my committee members again: professor Donald Amort, professor James Herzog, professor Robert Wilson, professor Shih–Lien Lu, for their time.

Table of Contents

LIST OF FIGURES

LIST OF TABLES

Chapter 1. Introduction

1.1 Motivation

Up until a few years ago, the main technology for high–speed digital systems was emitter–coupled logic (ECL). However, as the gate length in Complementary Metal Oxide silicon (CMOS) technology is scaling down, CMOS circuits are able to attain comparable speed performances on chip. However, one of the bottlenecks which prevents the full utilization of its on chip high speed has been the design and operation of off–chip drivers. There are several constraints which limit the performance of the off–chip output drivers such as electro–static discharge (ESD) protection requirement, power bus noise reduction, and power consumption reduction. Therefore the design of these off–chip drivers must be able to address these problems and at the same time be able to achieve the desired high speed. Moreover, since newly designed CMOS components are used to replace ECL components in high–performance systems, these CMOS chips must be designed to be ECL compatible so that they can communicate with other ECL ports (e.g. ECL memory) in a system environment. This means that extra circuitry is required to convert CMOS–level internal signals into ECL–level output signals and vice verse. Since ECL logic swing is smaller than CMOS logic swing, reduction of power bus noise is even more important. Therefore there is a need to design high speed and low supply/ground noise ECL compatible CMOS buffers for the purpose of off–chip drivers.

1.2 The Buffering Problem

As the gate length in CMOS is scaled down, we are able to pack more devices onto a single chip. This high integration device leads to the need for very high pin counts [1]. Since internal signals are weak compare to the external loads contributed by packaging and printed

circuit board, drivers (or buffers) are usually used to amplify these signals so that they are able to drive off–chip loads. (It is worth noting that on–chip buffering pose a similar problem. In designing complex circuits, it happens very often that a signal has to drive a large fan–outs and hence a large load. Typical examples are buses, clock and controls.) These buffers usually have much larger sized devices so that they may provide the large current necessary to drive the loads. Even though CMOS has little or no static current from supply to ground, however every time a CMOS gate changes its state, either a current flows from the supply to the load or a current flows from the load to the ground (caused by charging or discharging the load). This dynamic current flow causes a spike on the supply or ground voltage due to parasitic inductance and capacitance of the package. This problem is accumulative when several large buffers switch their states at the same time. As a result, the required ECL–line drive capability (75ohm/14mA) and the reduction of supply and ground bounce noise generated by many drivers switching at the same time are the main obstacles for the design of high performance CMOS–ECL interface circuitry.

1.3 The Approach

The *supply* or *ground bounce noise* is known as the simultaneously switching noise (or *di/dt* noise). It is resulted from rapid current change that these drivers conduct which generates a voltage across the parasitic inductance of the package consisting of the bonding and package lead wiring that connects the chip to one of the power supplies (Vdd or Vss). This noise can create a false signal and cause spurious switching. In order to avoid logic errors, a widely used solution to reduce power supply bounce is to have multiple supply and ground pins. With multiple power pins the parasitic inductance attributed by the package pin is reduced. For example, the new Intel i860 XP RISC microprocessor chip has 55 Vcc and 55 Vss pins [1] which amounts to more than 25% of the total available pins. The newly released DEC

ALPHA RISC processor chip has 70 Vdd and 70 Vss pins [2] which amounts to more than 32% of the total available pin counts. The main disadvantage of using this method to reduce supply bounce is that it significantly reduces the number of usable pins for signals. Since the power supply bounce is contributed by the rate current changes in a short period of time, another approach used to reduce the power supply bounce is to prolong the rise time and the fall time of the signal. Gabara and Thompson [3] designed a novel circuit which uses process dependent voltage source to regulate the charge/discharge rate of the buffer. However, due to the high–frequency required by the state–of–art computer chips, there is limit as how much we can prolong the rise time and fall time. Moreover, even with the prolonged rise time and fall time, because of the large current change, the voltage bounce is still significant. Fortunately, there is another way to reduce the power supply noise. To explain this further we consider a particular pin which is to be switched from low to high or high to low. From the Kirchoff's current law we know that

$$I = C_L \frac{dV}{dt} \longrightarrow \Delta I = C_L \frac{\Delta V}{\Delta t} \tag{1}$$

In order to swing a signal from rail to rail given a capacitive load in a given time (either rise or fall time), there will be a current spike from the supply pin. We also know that if a parasitic inductance L is presented at this supply pin, this change of current from (1) will cause a voltage change to the supply voltage since again from Kirchoff's current law:

$$V = L \frac{dI}{dt} \longrightarrow V_{noise} = L_{parasitic} \frac{\Delta I}{\Delta t_{rise\ or\ fall\ time}} \tag{2}$$

Therefore to reduce the supply noise (V_{noise}) we can either reduce the $L_{parasitic}$ or increase Δt. As we have mentioned before these two methods have been used. From (2) we see that a reduction in ΔI will result in a reduction of V_{noise}. That is, by reducing the value of ΔI, we can also reduce the supply noise. Considering some of the problems facing the other two methods, we believe the third method deserve a closer look. Since the current required to

drive the loads can not be reduced (otherwise we will not satisfy the speed requirement), we can only reduce the amount of actual current change in the supply pin due to logic state change. Therefore the solution must be a circuit solution.

1.4 Summary of the Thesis

This thesis describes a new CMOS output buffer which can generate ECL logic levels with lower power supply noise by keeping the total current come from the power and goes to the ground constant at the switching time. This circuit may be realized in any typical digital CMOS/Bulk technology without any extra special processing. There are five chapters in this thesis. In chapter 2 we give a summary of some techniques used currently by the industry to reduce the power supply noise. In chapter 3 we describe the new buffer proposed. In the same chapter we present the detail circuit design and analysis why it is low in supply noise. In Chapter 4 a summery of the simulation results is given. In the same chapter we also present the comparison with other published low noise buffer structures. We conclude this thesis and propose possible future work in the final chapter.

Chapter 2. Noise Reduction

2.1 Introduction

With shrinking physical dimension and increasing circuit speed, communicating with the outside world is one of the toughest task to design. First of all, the number of connections going off chip is approximately proportional to the complexity of circuitry on the chip. This relationship is expressed by the empirical formula – Rent's rule. This rule relates the number of input and output pins required with the complexity of a given integrated circuit as measured by the number of equivalent gates.

$$P = K\,G^{p} \tag{3}$$

where K is the average number of I/O's per equivalent gate, G is the number of gates, p is the Rent exponent and P is the number of I/O pins of a chip. From empirical data, p is normally valued from 0.5 to 1 depending on the circuit organization and the application area. In the current days technology, chips having more than 300 pins are common place. This puts tough requirements on the bonding pad design in terms of noise immunity, since lots of pads will be switching at the same time each driving a large capacitive load causing large transient currents. On the other hand, scaling down of the the technology has reduced the internal capacitance on the chip, while the off–chip load remains roughly the same (20pF to 50pF). At the same time, as on–chip circuit reduces its channel length, the switching speed is increased. As we have mentioned in the previous chapter, the power supply noise is known as the simultaneously switching noise. Currently a typical packaging technology introduces approximately 10nH per pin by the bonding wire and package lead. Assume we would like to switch 50 output pins at the same time with rise or fall time (speed) of 5ns. Assume the logic swing is 1 volt. From equation (1) we derived that the current required to switch one pin (with 50pF load) by the power supply is roughly 10mA. Substituting this

current value of 10mA into (2) gives a voltage variance of 20mV per pin. With 50 pins changing at the same time, power supply will swing as much as 1V which is the same as the logic swing! This voltage fluctuation on the supply lines reduces the noise margin and causes erroneous results. The question then is, how can one reduce the noise introduced by switching several pins at the same time? As we have already mentioned in chapter 1, in order to reduce the supply noise(V_{noise}) we can either reduce the $L_{parasitic}$ or increase Δt or reduce ΔI. This thesis will examine the approach of reducing ΔI. As a comparison to this new approach, let us introduce in more detail the other two methods which are used to reduce the power supply noise.

2.2 Reduce the Parasitic Inductance

The power bus noise which is induced by the parasitic inductance is a build–in noise. This noise source is affected only by both the fabrication process and packaging technology. A number of novel packaging technologies (e.g. multi–chip module) are currently emerging, which help to reduce parasitic inductance and off–chip capacitances as well. However, it is not the purpose of this thesis to investigate the advancement of fabrication nor packaging technology. In reducing parasitic inductance, we can only apply straight forward solution used commonly. The technique describe here is a passive method. According to the elementary electronic theory, the inductance has the same characteristic as the resistance when connecting them in series and in parallel. Using equation to express the equivalent inductance of connecting two identical inductors together in parallel is $L//L = 1/2L$. This is the main reason why modern chips have so many ground and power pins. For instance, let's assume the maximum power noise that the system can tolerate is 0.025 volt. If only one power pin is used. Because of the current change due to signal switching causes this pin to have a noise of 0.1 volt. Adding 3 extra power pins to the chip will reduce the effective inductance to be 1/4 of the inductance of the one power pin setup. This will, then, satisfy the noise require-

ment imposed by the system. The advantage of this technology is very simple and easy to apply. The disadvantage of this technology is also very obvious that by adding more supply pins the number of useful pins is drastically reduced (both power and ground).

2.3 Prolong the Rise and Fall Time

The second common solution used to reduce noise is to prolong the rise and fall time of the signal. This method requires a more complex design to achieve the desired effect. A circuit diagram is shown in Figure 2.3.1(a) which depicts the model of an output pin. The output impedance of the off–chip driver is $1/g_m$, the device width is chosen to match the output impedance to the transmission–line impedance. A positive signal on the input gate initially produces half as much signal on the output node connected to the near end of the transmission line, with the voltage dividing equally across the off–chip driver device and the transmission line. A 1.2–V input swing in a time t produces a 0.6V output swing in the same time period. This output signal traverses the transmission line in a time period t_L and at the unterminated far end, according to the electric magnetic theory, the reflect coefficient $c=(Z_0–Z)/(Z_0+Z)=1$, causes a reflected wave which doubles the far–end signal swing to 1.2V, which also rises in a period t (following the delay of t_L). This reflected wave begins to arrive at the driver output after a total delay of $2t_L$ and adds to the original signal swing. As the reflected wave is absorbed in the matched driver impedance, the signal at the driver output rises to the full 1.2V input signal swing. This is because that when the output impedence is the same as the impedence of the transmission line, the reflection coefficient c equals zero can be derived. The driver current wave–form is shown in figure 2.3.1(b). In the initial period t the current rises up to a value of 0.6V/R and is reduced back to zero when the far–end reflected wave arrives at the driver. (The transmission line is then fully charged and the current is zero everywhere on the line.) The inductive ringing of the power supply is

closely connected to the rise time t, namely,

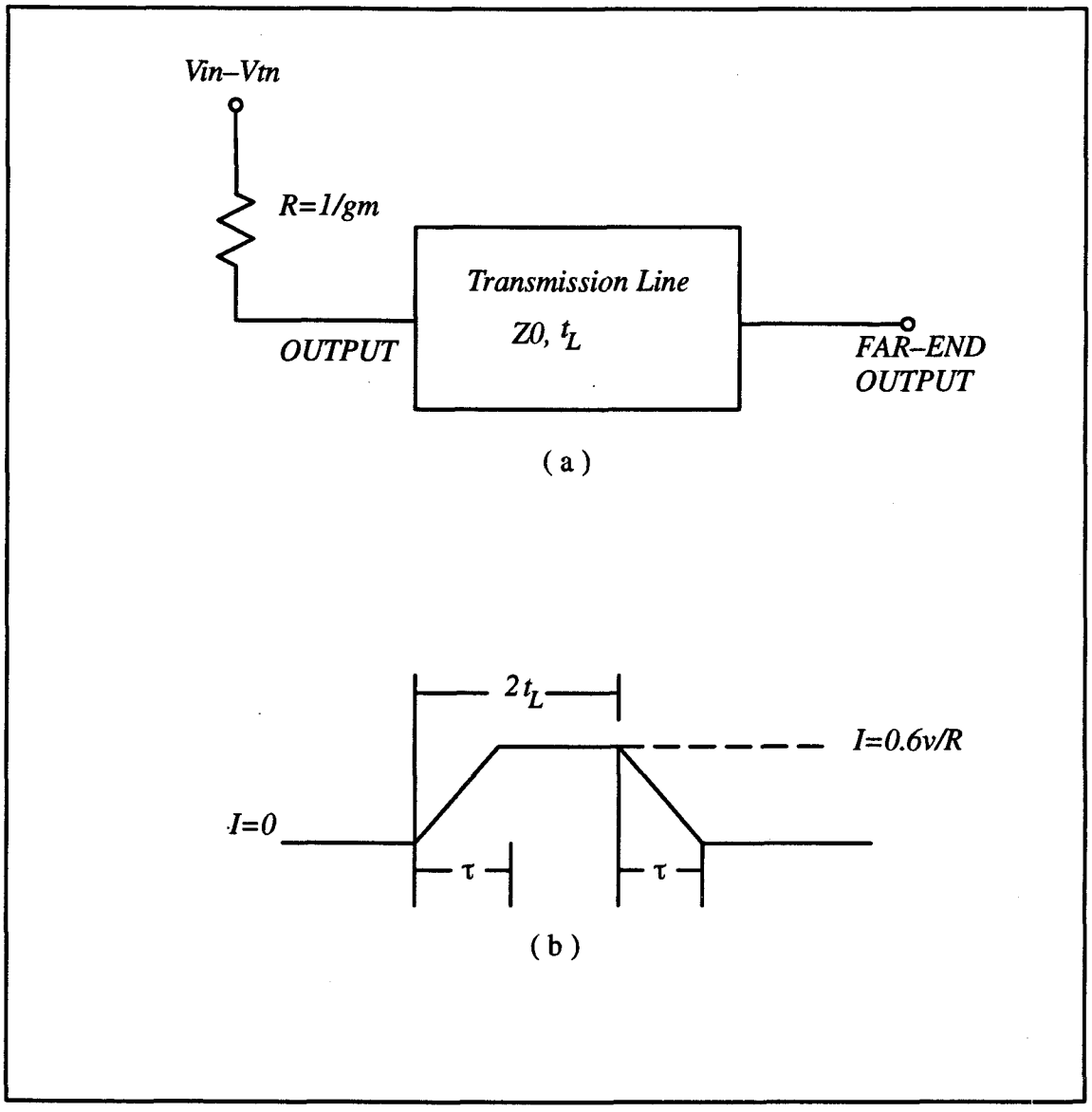

Figure 2.3.1 A circuit diagram which reduces the ground bounce by prolong the rise/fall time (a) Output equivalent circuit (b) timing diagram

L di/dt =0.6 L / Rt per driver switching. It is advantageous to make t longer to reduce this inductive ringing. The disadvantage of this technology is that you have to sacrifice the signal delay time to satisfy the low power supply noise requirement.

According to the analysis above, we feel that these two technology all have some disadvantages and limitations. A new circuit which can overcome these problem by keeping the total current from the power supply to ground constant is, therefore, proposed and described in the next chapter.

Chapter 3. Proposed Circuit Design

3.1 Introduction

As discussed, there is a limit as to how much we can prolong the rise time and the fall time of a circuit because of the system speed requirement. Moreover, there is a price to how many more extra supply and ground pins we can add to a chip. There is an incentive to investigate the third method of noise reduction which is to reduce the rate of current change. However, the amount of current used to charge and discharge external capacitive load determines the speed of the CMOS circuit. Reducing the absolute current itself is not an acceptable solution. With less current to charge and discharge the capacitive load, we need more time to bring the node to the desired output voltage. It reduces the overall speed of the circuit, thus the speed of the system. A possible remedy is to reduce the rate of current change instead of decreasing the absolute amount of current flow from the supply and to the ground. That is, we would like to find circuit structures which instead of having a dynamic current change every time the circuit change its state, it will have a constant current flow from the supply and to the ground. By maintaining a desired constant current which flows from the supply we can satisfy the overall system speed requirement. Since the current is steered from one branch to another charging or discharging the node to the desired voltage, the rate of current change may be maintained to be constant also causing very little noise on the supply and the ground line. This current switching (steering) can be achieved by using a common analog circuit structure – the *differential amplifier*. The differential amplifier is a voltage controlled voltage source with infinite voltage gain and with zero input admittance as well as output impedance. It is free of frequency and temperature dependence, distortion, and noise. It has become a very useful circuit because of its compatibility with integrated circuit technology. To overcome the problem of noise in the supply and ground lines, a new tech-

nique which uses a modification of differential amplifier is proposed. This technique of using current steering to reduce the power and ground noise is the main contribution of this thesis.

3.2 The First Approach

The first approach is based on a modified cascode differential amplifier design. As mentioned we would like to maintain a constant current flow. This is achieved by steering the current from one branch to the other branch. As a result the total dynamic current variation for both supplies is kept constant. As we know from equation (2) that the voltage noise is proportional to $L\ di/dt$. If di is very close to zero, the voltage variance is then eliminated. The circuit proposed is fully symmetrical, but it is not self–biased. A total 16 transistors are needed for each signal. There is some other circuit needed to generate the voltage bias. The basic operation of this circuit is perhaps most readily understood by following its derivation from well–known conventional cascode CMOS amplifier configurations. However, we are interested in its large signal (DC voltages) behavior instead of the small signal behavior (AC). We will describe the operation in the following section.

3.2.1 Circuit Description

Figure 3.2.1 illustrates the circuit diagram of this novel circuit. There are two similar differential amplifiers. One of the differential amplifiers is of the N–type and the other is of the P–type. The N–type differential amplifier has an N–channel current bias, a differential pair of N–channel devices (M1 and M2) as input stage and two P–channel transistors (M9 and M10) as its loads. Similarly the P–type differential amplifier has a P–channel current bias, a differential pair of P–channel devices (M3 and M4) as input stage and two N–channel transistors (M11 and M12) as its loads.

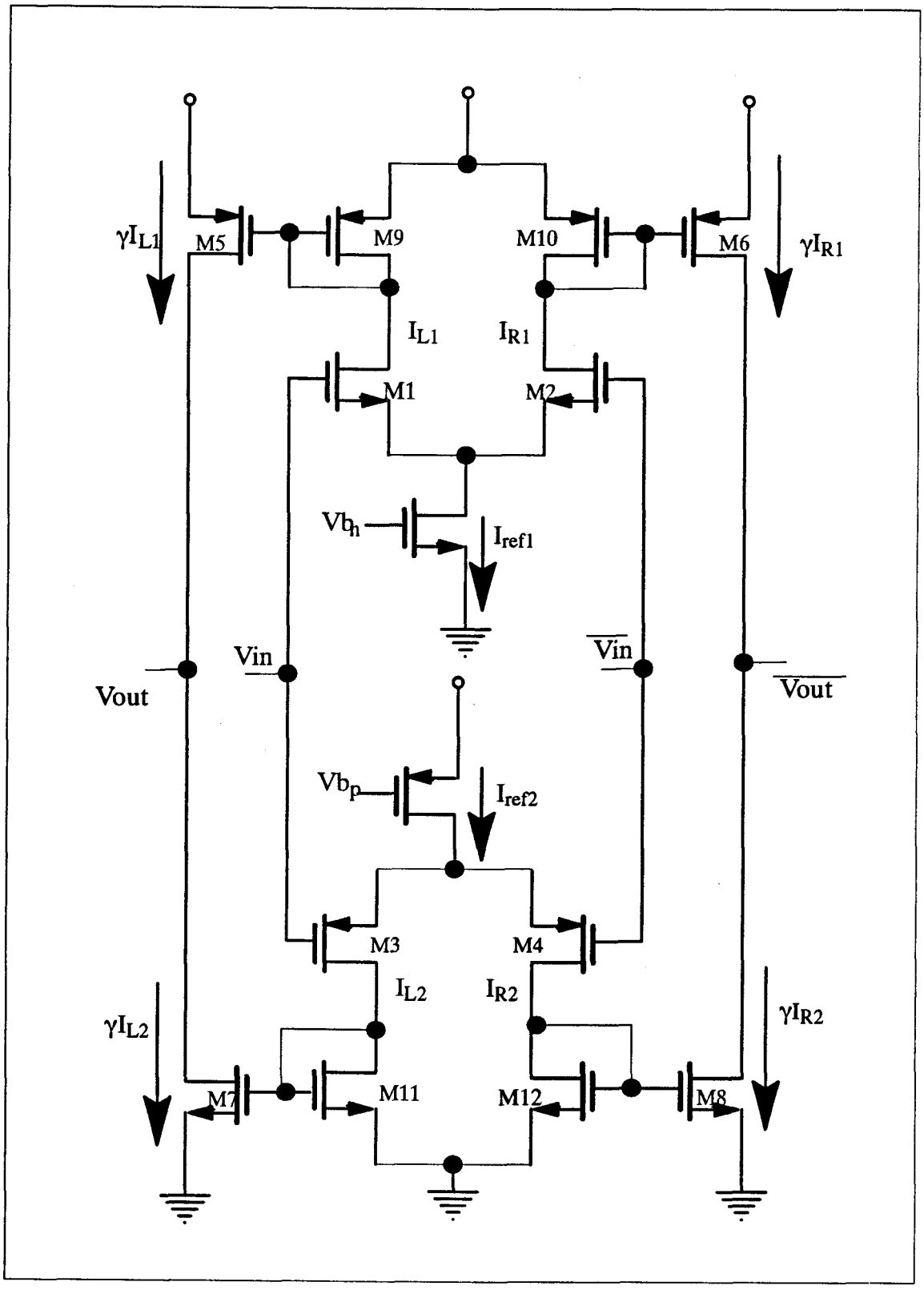

Figure 3.2.1 CMOS OCD Buffer circuit (Approach#1)

There are two output stages one for the true and the other for the complement output. Each output stage consists of one P–channel device and one N–channel device. P–channel devices of the two output stages are connected to the N–type differential pair while the N devices are connected to the P–type. When the input voltage is at logic 0 (low voltage), the complement of input is at logic 1. Therefore, transistors M1 (N–channel) and M4 (P–channel) are OFF, while M2 (N–channel) and M3 (P–channel) are ON. There will be more current flowing through the right branch of the N–type differential pair, while there will be more current flowing through the left branch of the P–type differential pair. Thus, transistors M6 and M7 are ON, while transistors M5 and M8 are OFF. Therefore the output is discharged to logic low (0), while its complement is charged to logic high (1). Visversa, if the input signal is at logic high (1), the opposite will happen. M2 and M3 are OFF while M1 and M3 are ON. Thus, transistors M6 and M7 are OFF, while transistors M5 and M8 are ON. Therefore the output is charged to logic high, while its complement is discharged to logic low. In the following section we will derive the current flow in this circuit structure and show that the current flowing from the supply and to the ground is indeed constant.

3.2.2 Current Derivation

As we mentioned, there are two differential amplifiers of the opposite types. Refer to the notation in Figure 3.2.1. We know each of the differential amplifiers must satisfy the following current equations:

$$I_{ref1} = I_{L1} + I_{R1} \tag{4}$$

$$I_{ref2} = I_{L2} + I_{R2} \tag{5}$$

Moreover, in the circuit depicted, M1, M2, M3 and M4 are current mirrors of M5, M6, M7 and M8 respectively, except that M1–M4 are sized appropriately by γ to give enough current for charging and discharging the external load capacitance . Therefore, the total current flowing throughout the power supply is:

$$I_{total\,P} = I_{L1} + I_{R1} + \gamma (I_{L1} + I_{R1})$$

$$+ I_{ref2} = (1 + \gamma) I_{ref1} + I_{ref2} \qquad (6)$$

Also, the total current flowing through all N–channel devices to ground is:

$$I_{total\,N} = I_{L2} + I_{R2} + \gamma (I_{L2} + I_{R2})$$

$$+ I_{ref1} = (1 + \gamma) I_{ref2} + I_{ref1} \qquad (7)$$

Since reference currents are constant, from the above two current equations, we conclude that the circuit will have constant supply and ground current independent of the input (output) swings. As mentioned above, the advantages of this circuit are lower power supply noise and simple configuration. However, this circuit also has several important disadvantages. One potential problem is their static power consumption. Another critical problem is their large area occupied by the output transistor. From the voltage–current equation of MOSFET,

$$I_d = K/2(W/L)[2(V_{gs} - V_T)V_{ds} - V_{ds}^2 \qquad (Linear) \qquad (8)$$

and

$$I_d = K/2(W/L)(V_{gs} - V_T)^2 \qquad (\ Saturation\ ) \qquad (9)$$

We know that I_d is directly proportional to the W/L. Since the output current required by the ECL circuit is around 16mA, the size of transistors M1, M2, M3, and M4 are all very large. Achieving this large size on a chip is practically impossible, so that the circuit configuration of Fig.3.2.1 is impractical.

3.3 A Modified Design

A modification to the circuit of Figure 3.2.1, however, results in a less transistor number, completely complementary self–biased through negative feedback, fully symmetry circuit.

3.3.1 Circuit Description

This modification is illustrated in Figure 3.3.1. In this circuit, the transistors M9, M10, M11, and M12 in the previous design are eliminated. These transistors were used as the current mirrors. Instead the drain of the transistor M1 is directly connected to the gate of the transistor M5. Similarly the drain of M2 is connected to the gate of M6, the drain of M3 to the gate of M7, the drain of M4 to the gate of M8. Previously current mirrors achieved by transistor pairs – M9/M5, M10/M6, M11/M7, and M12/M8 reflecting the signal current from the drains of M1, M2, M3, and M4, respectively. By connecting the drain directly to the respective gates, we would inject these currents directly instead. This results in a circuit more stable and faster than the design proposed in Figure 3.2.1.

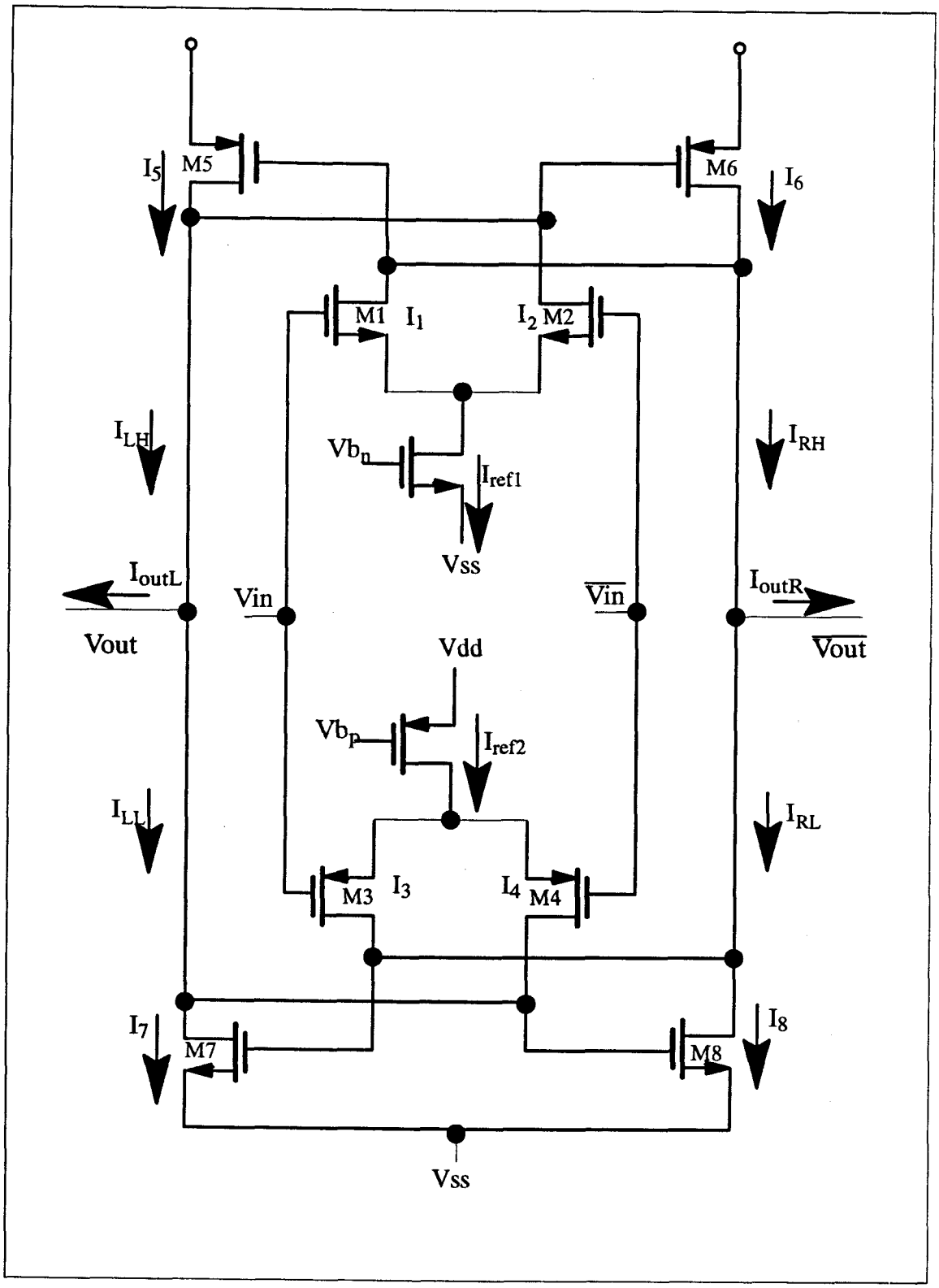

Figure 3.3.1 CMOS OCD Buffer circuit (Approach#2)

Also, since the output node is connected to the gate of the transistors M5, M6, M7, and M8, due to the negative feedback, a number of circuit performances are improved, such as reduced sensitivity of gain to active–device parameter changes, and the reduction of distortion because of circuit nonlinearities, etc. Moreover, because all the output transistors are self–biased through feedback, there is no effect on the output voltage gain by the frequency change. Furthermore, even though the negative feedback reduces the system gain, this disadvantage in the conventional system is a great advantage in this CMOS–ECL interface. As the magnitude of the voltage swing is reduced, the desired compatibility with ECL standard voltage levels is achieved. By reducing the gain, output voltage swing is reduced. This helps the interfacing problem also.

3.3.2 Current Derivation

Finally, and most importantly, we would like to verify that the total current coming from the power supply and going to the ground is constant even during the circuit's logic switching phase. From Fig. 3.3.1 we can derive the following current equations (10)–(15) due to Kirchoff's Law:

$$I_2 + I_{LH} = I_5 \tag{10}$$

$$I_1 + I_{RH} = I_6 \tag{11}$$

$$I_1 + I_2 = I_{ref1} \tag{12}$$

$$I_3 + I_4 = I_{ref2} \tag{13}$$

$$I_3 + I_{RL} = I_8 \tag{14}$$

$$I_4 + I_{LL} = I_7 \tag{15}$$

In order to meet ECL specifications, a voltage of –0.9525v and a voltage of –1.715v, which correspond to a logic "0" and a logic "1" in ECL, respectively, are supposed be showing at both buffer output nodes. Because the ECL input impedance is 75 ohms, to match –0.9525v and –1.715v when Vss=–2v, the output current I_{OUTL} and I_{OUTR} must be 14mA and 3.8mA respectively. When Vin is high, due to Vdd=3v, Vss=–2v, transistor M_3 and M_7 are off. So I_3=0, I_7=0. From Fig.4 we find out that $I_{OUTL} = I_{LH} + I_4$ =0.014 due to M_7 being off; and $I_{OUTR} = I_{RH} - I_8$ =0.0038 due to M_3 being off. So the derivation concludes that I_{LH} =0.014 – I_4 =0.014 – I_{ref2} and I_{RH} =0.0038 + I_8. Moreover, from equation (10) to (15), we obtain:

$$\begin{aligned}(I_5 + I_6)_H &= I_1 + I_2 + I_{LH} + I_{RH} \\ &= I_{ref1} + I_{LH} + I_{RH}\end{aligned} \tag{16}$$

Replace I_{LH} and I_{RH} in the equation (16) with the above derivation conclusions, we obtain:

$$(I_5 + I_6)_H = I_{ref1} + I_{LH} + I_{RH}$$

$$= I_{ref1} + 0.014 - I_{ref2} + 0.0038 + I_8$$

$$= 0.0178 + I_8 \qquad (17)$$

if we let $I_{ref1}=I_{ref2}$.

Similarly, when Vin is low, transistors M_4 and M_8 are off and we will obtain:

$$(I_5 + I_6)_L = 0.0178 + I_7 \qquad (18)$$

Since both of the output voltage Vout and $\overline{\text{Vout}}$ are fixed at ECL circuit logic level, from Fig.4 we can figure out that the voltage condition of transistor M_8 are $V_{source}=\overline{Vout_H}$, $V_{gate}=Vout_H$, $V_{drain}=Vss$, when Vin is high and the voltage condition of transistor M_7 are $V_{source}=Vout_L$, $V_{gate}=\overline{Vout_L}$, $V_{drain}=Vss$, when Vin is low. Because of the fact that $\overline{Vout_H}=Vout_L$, $Vout_H=\overline{Vout_L}$ and size (*W/L*) of M_7 and M_8 are exactly the same, I_7 and I_8 are the same and is equal to a constant, regardless of the state of the input Vin. This means that equation (8) and (9) are also equal to a constant. The noise induced on the power supplies by the *di/dt* is then eliminated due to $I_{total}=(I_5+I_6+I_{ref2})_H=\text{constant}=(I_5+I_6+I_{ref2})_L$. Also from the above analysis, since I_7 and I_8 are constant, we can say that all the currents going to the ground are constant too.

3.4 Comparison of the Proposed two Designs

In summary, the circuit configuration of the second approach differs from the original approach in two important ways:

(1) the second approach is self–biased through negative feed–back;

(2) the second approach uses the current injection technique rather than the current mirror technique.

These two differences in the amplifier configuration result in several performance enhancements:

(1) less sensitivity of active–region biasing to variations in processing, temperature, and power supply;

(2) capability of supplying switching currents that are significantly greater than the quiescent bias current;

(3) reduction of the transistor numbers and area.

Table 3.4.1 tabulates some physical differences between these two approaches. The first column summarizes the total number of transistors required to implement these two designs. The second column indicates the transistor sizes for the output stages. The third column lists the required power supply voltage. The first design has one advantage over the second design. It requires the typical CMOS power supply (0 and 5 V) only while the second design needs extra supply voltages. However, we see that the second design definitely has a better performance cost ratio.

Table 3.4.1

Comparison of Approach #1 and Approach #2

	# of transistor	driving transistor size (W/L) in microns	power supply voltage required
Approach #1	16	PMOS 900/1 NMOS 300/1	5/0 V
Approach #2	8	NMOS 90/1 PMOS 20/1	3/–2 V

Chapter 4. Simulation and Implementation

4.1 Introduction

It is a common practice for the circuit designers to simulate a particular design using a circuit simulator first. A widely used program is SPICE. SPICE is a general–purpose circuit simulation program for circuit analysis. In this thesis a commercial verson of the original SPICE, namely HSPICE is used exclusively. Models used to describe the MOSFET devices are acquired from MOSIS (Metal–Oxide Silicon Implementation System) Service. They are listed in the Appendix.

4.2 SPICE simulation

The circuit has been extensively simulated using HSPICE. The output buffer is loaded by a 75 ohms lossy transmission line with 1 ns propagation delay and 1 pf distributed capacitance. All the simulations were performed under typical conditions of Vdd=3V, Vss=–2V, and temperature of 25 degree with 1 um CMOS process parameters. The simulation results of the different frequencies are listed in Table 4.2.1 and the waveforms at the ends of the line are shown in Fig.4.2.1, Fig.4.2.2 and Fig4.2.3 respectively. The maximum simulated speed performance of the proposed buffer for input signals between 0V~3V is 400 MHz, which is comparable and better to the recently published structures of the similar design [3] [4] [5]. The rise and fall times reaching the minimum ECL levels are 0.31ns and 0.38ns respectively. This is a factor of 1.75 faster than the references provided above. A summary of comparison is listed in Table 4.2.2. The measured output levels of this buffer are –1.73V and –0.94V for the ECL low level and high level, respectively. Even with input voltages of less then 500mV, the circuit was able to distinguish the difference and produced the correct logic as required.

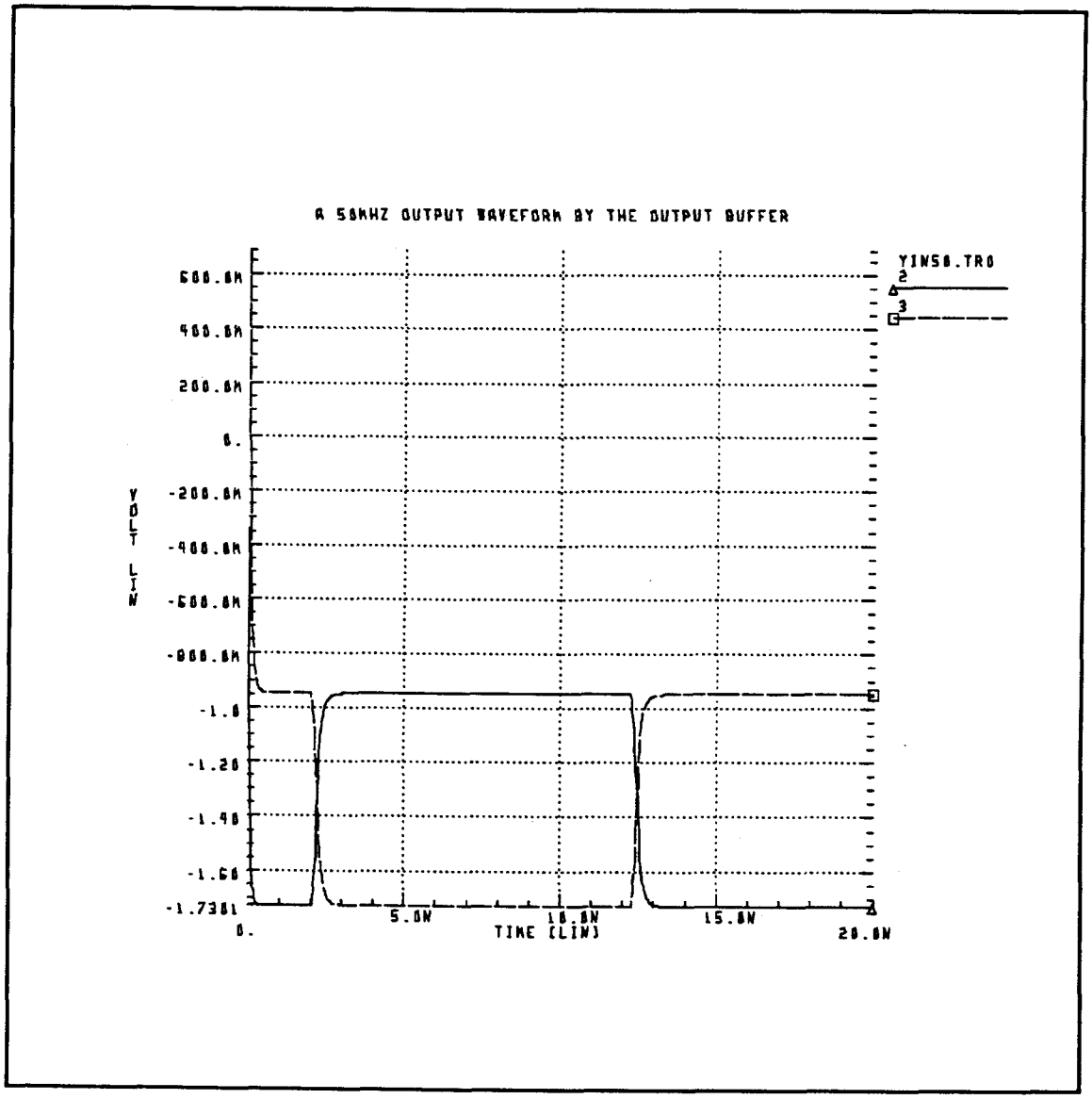

Figure 4.2.1 Output Voltage Waveform at 50MHz

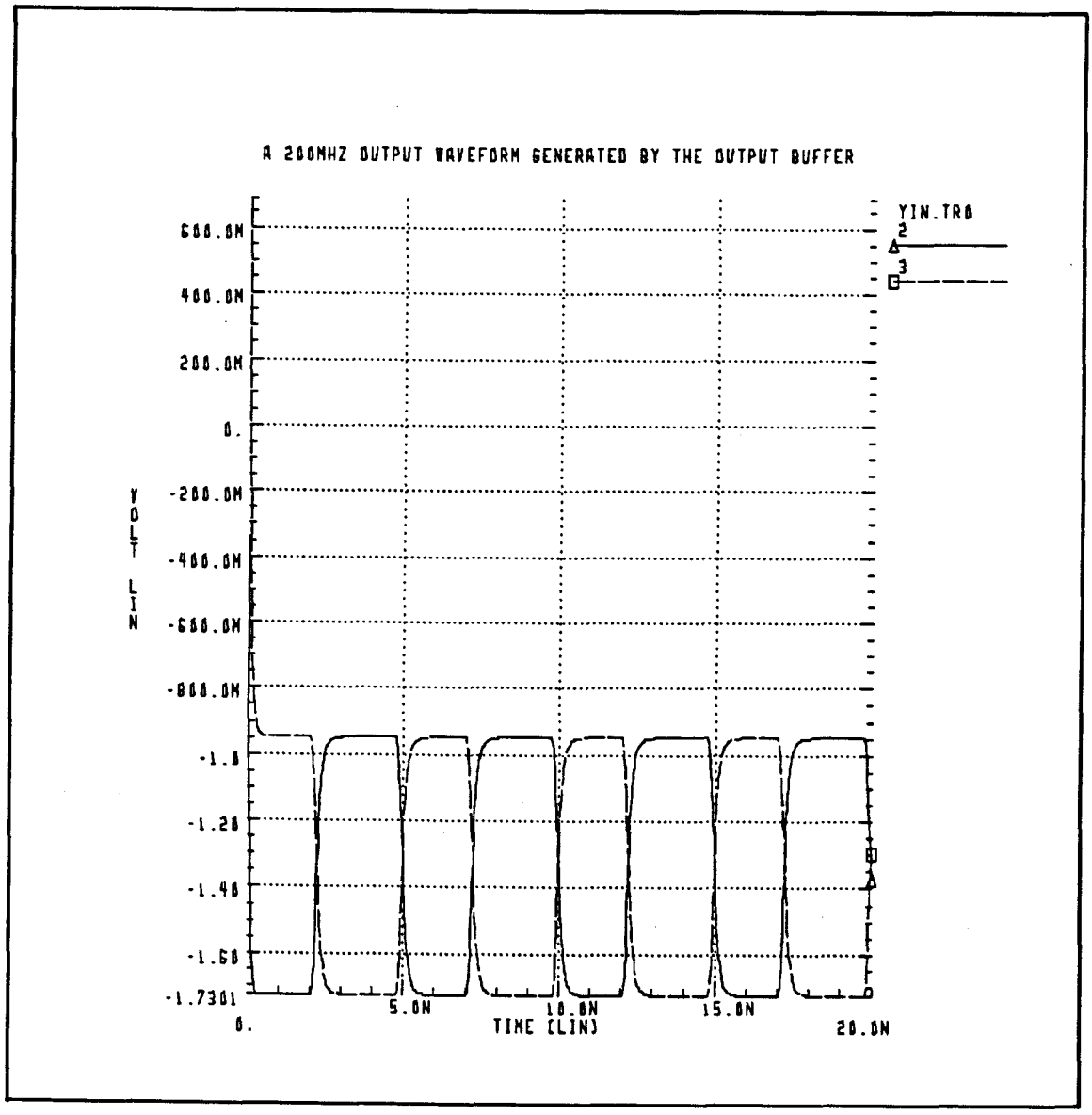

Figure 4.2.2 Output Voltage Waveform at 200MHz

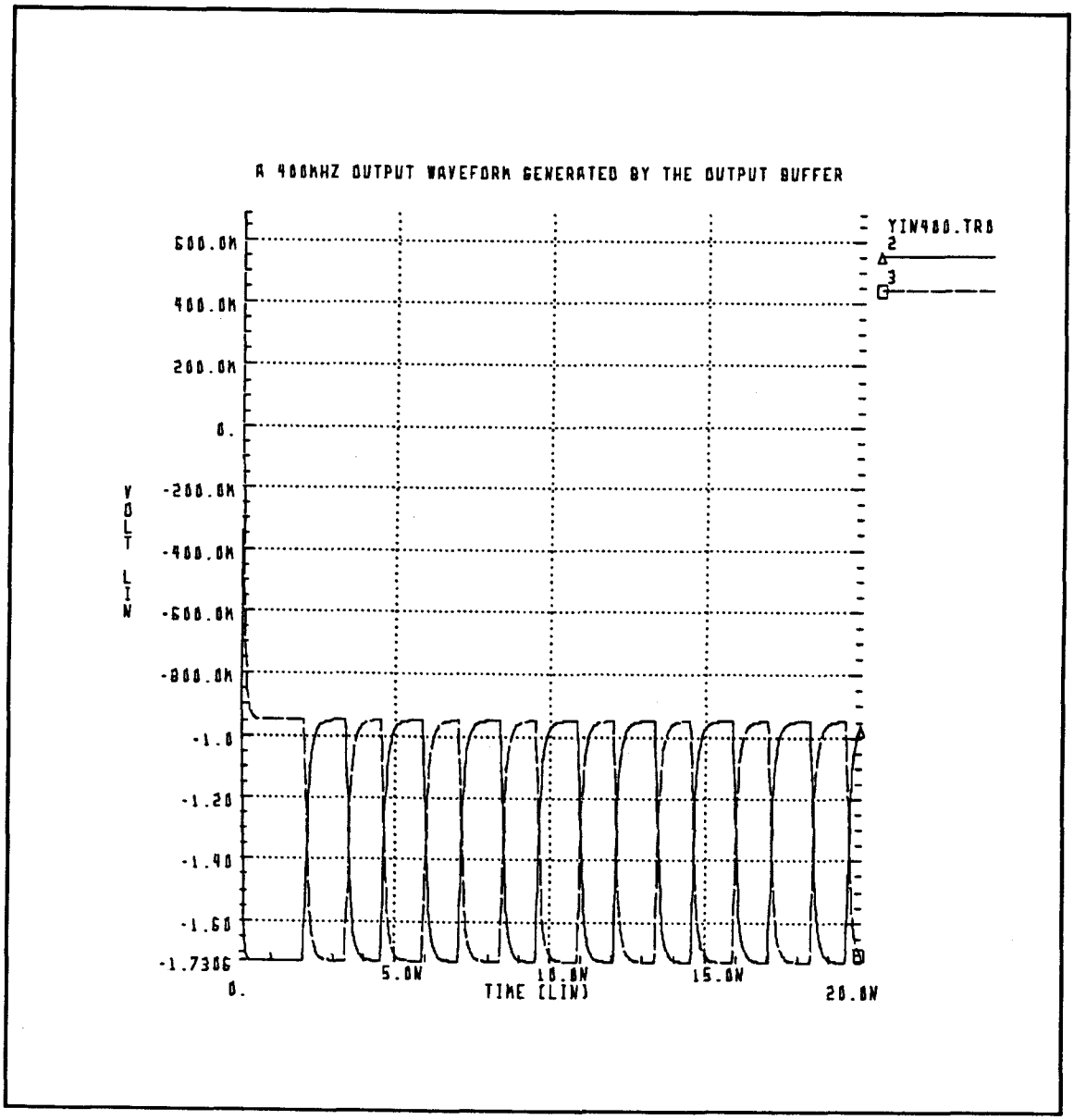

Figure 4.2.3 Output Voltage Waveform at 400MHz

Table 4.2.1

Simulated Performance of the OCD Buffer

	Circuit performance	Units
CMOS–ECL		
OUTPUT signal levels		
HSPICE	–0.94/–1.73	V
RISE Time		
HSPICE	0.31	ns
FALL Time		
HSPICE	0.38	ns

Table 4.2.2

Comparison to Other Recently Published
CMOS–ECL Structures

	Circuit Performance	ref [3]	ref [4]	ref [5]	Units
Process	1	0.9	1.2	0.25	um
Power supply	–2/3	–2/3	0/5	0/2.5	V
Performances					
Rise time	0.31	1.23	0.54	2.0	ns
Fall time	0.38	1.14	0.49	1.9	ns

4.3 Comparison

The simulations of the novel buffer current waveform from 50MHz to 400MHz are shown in Fig.4.3.1, Fig.4.3.2 and Fig.4.3.3. The calculated maximum *di/dt* noise is 0 mA/ns. This is about a factor of 10 smaller than the conventional full swing driver of [6]. In comparison, a conventional driver made out of a chain of inverters induces much more voltage variance on the power bus. Fig.4.3.4 shows the power supply noises as predicted by HSPICE between the new driver and the conventional one. This new circuit offers a solution to the off–chip driver noise problem, incurred with the conventional full–swing design as the number of I/O drivers that switch simultaneously increase, without sacrificing signal delay.
Standby power dissipation of the reduced power supply noise driver is 32mW using the newest 1μm technology available from MOSIS. Even though this is a known disadvantage of this circuit, we felt it is a trade–off we have to make to reduce the power supply noise.

4.4 Layout

The layout of this output buffer is designed. The output of the buffer is attached to a bond pad with glass openning to which a bond wire can be attached. This bond pad is usually of the order of 100μm by 100μm. As large transistors are typically used and I/O currents are high, the susceptibility to latch–up is highest also in I/O structures. To prevent this problem a guard rings tied to the supply rails to separate N– and P–transistors is applied. A main technique used in laying out this circuit is that we design the differential pair fully symmetry. All the input devices and their loads were placed side by side, with identical geometries including connecting lines. Because of the heat source(high current output), the matched elements were located symmetrically with respect to it, to make sure matched temperatures. This strategy helps reducing the sensitivity of the circuit to variations in processing and supply. Figure 4.4.1 shows the circuit layout.

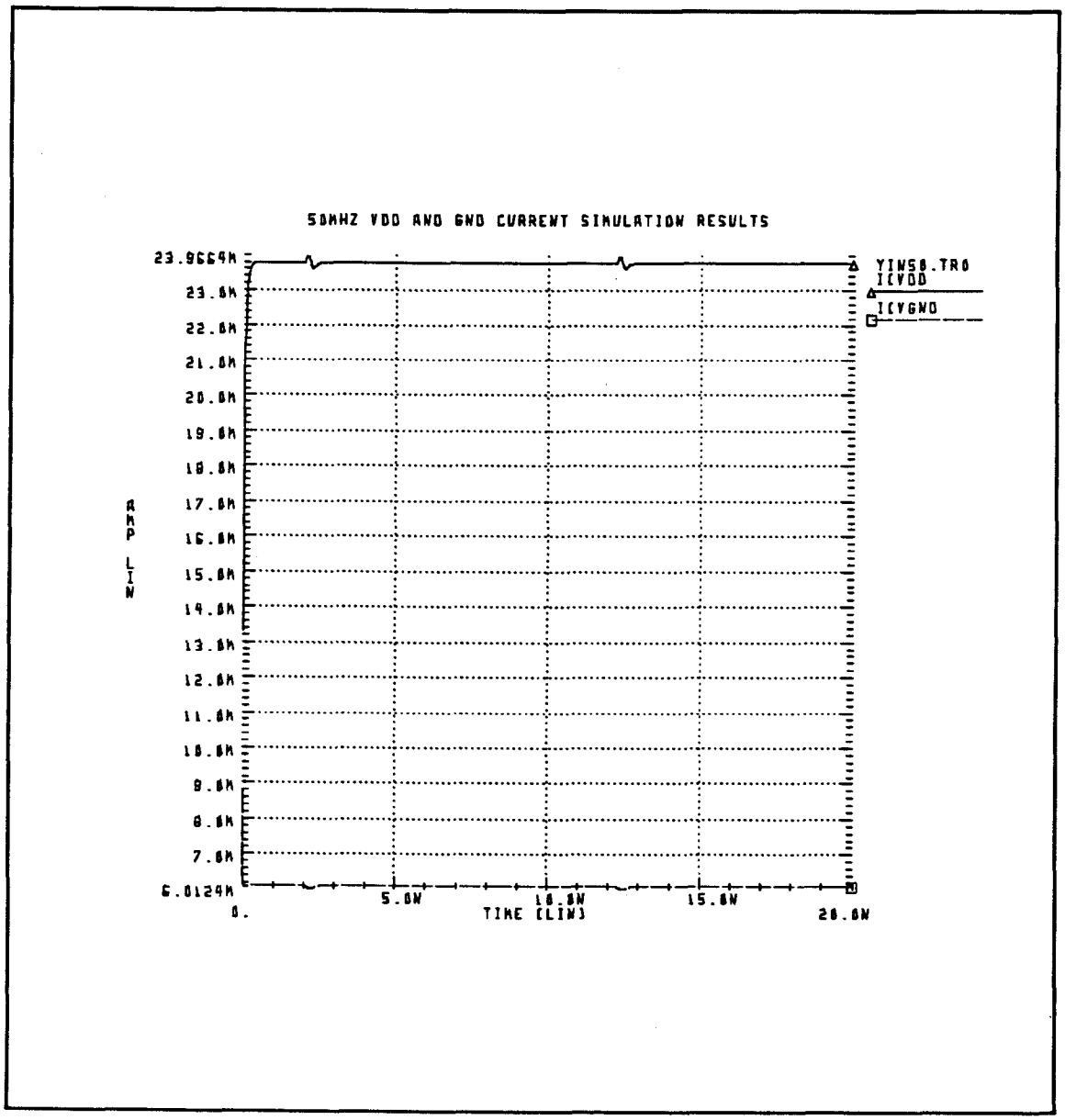

Figure 4.3.1 Total ground current waveform at 50MHz

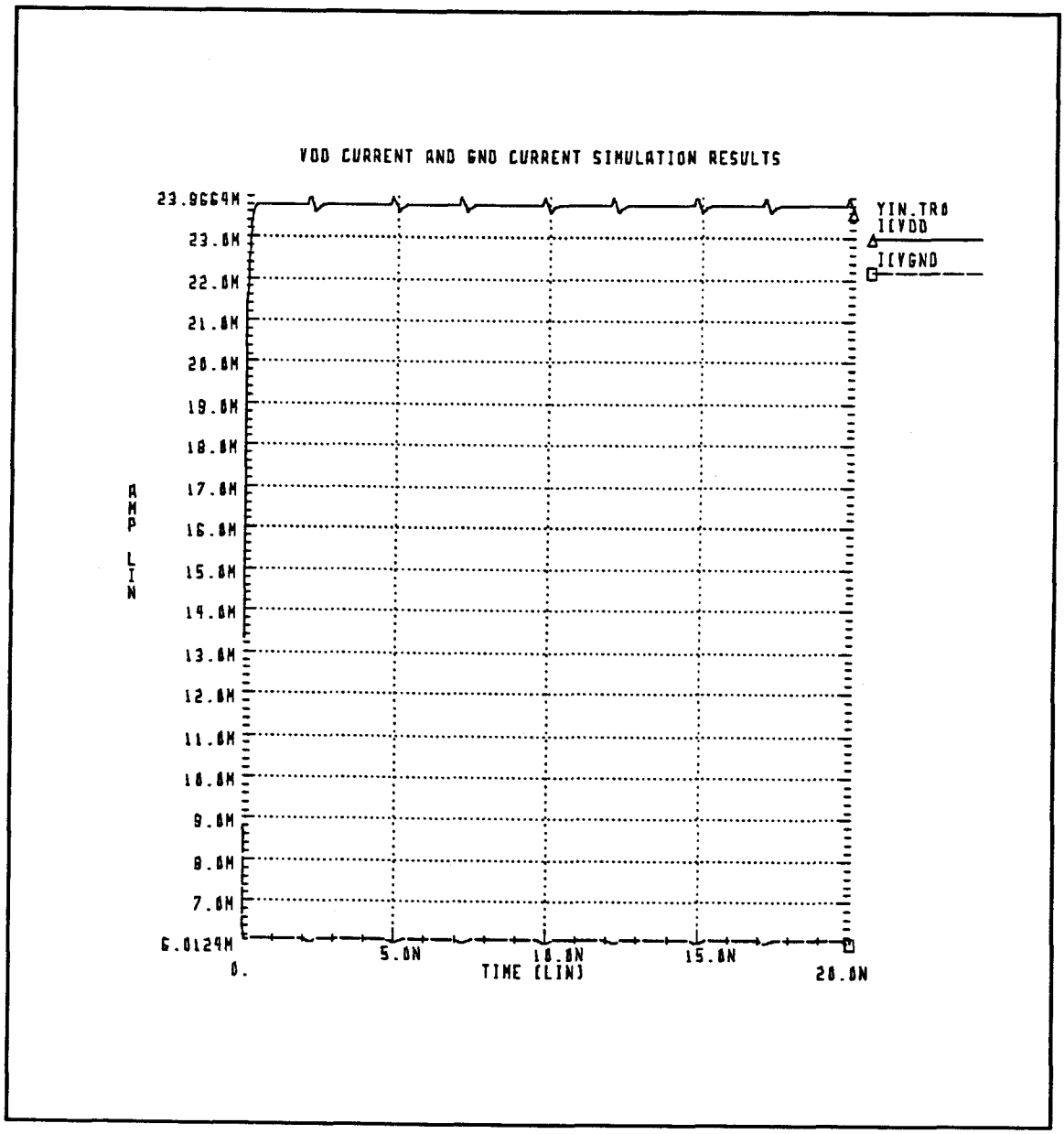

Figure 4.3.2 Total ground current waveform at 200MHz

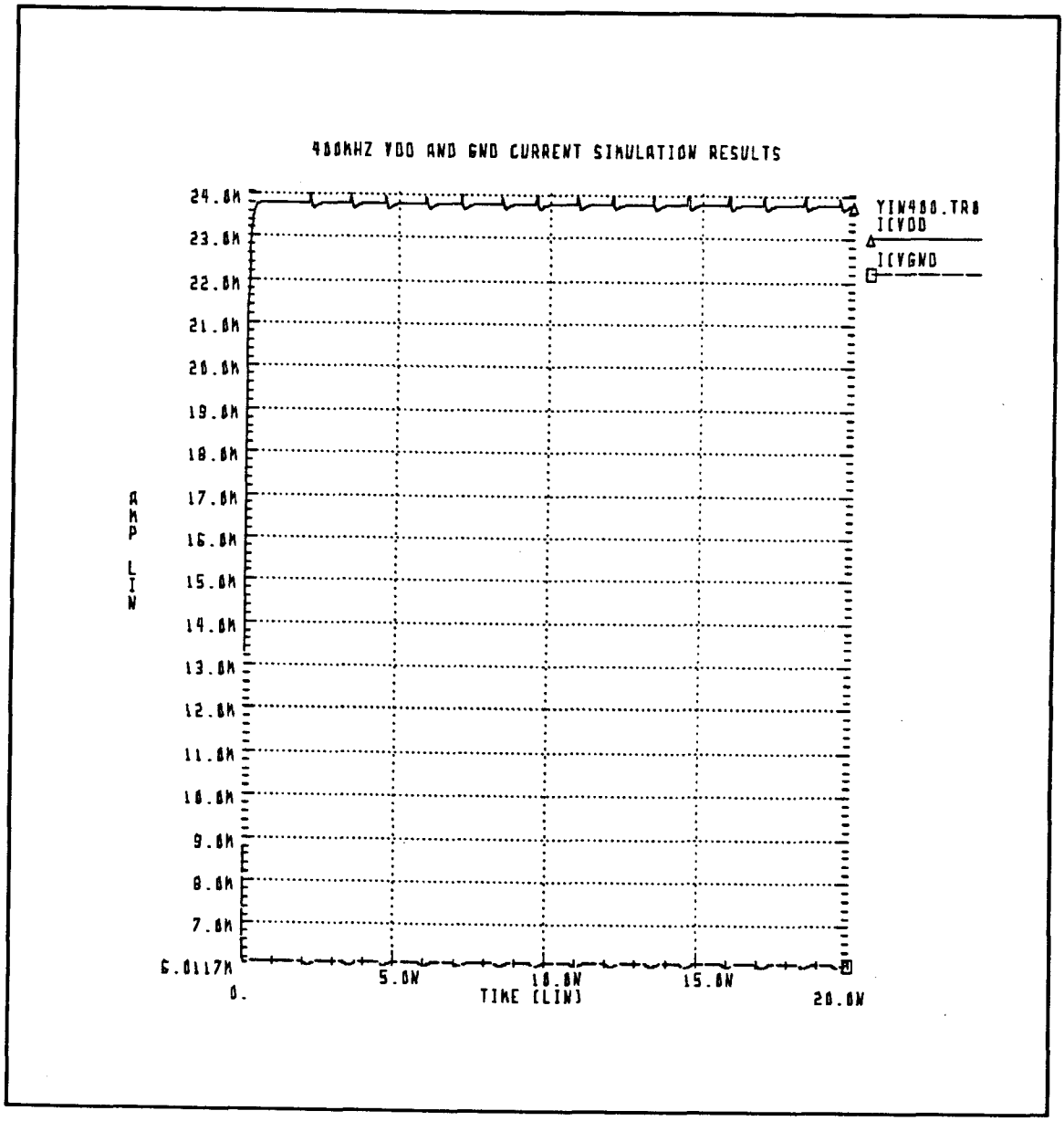

Figure 4.3.3 Total ground current waveform at 400MHz

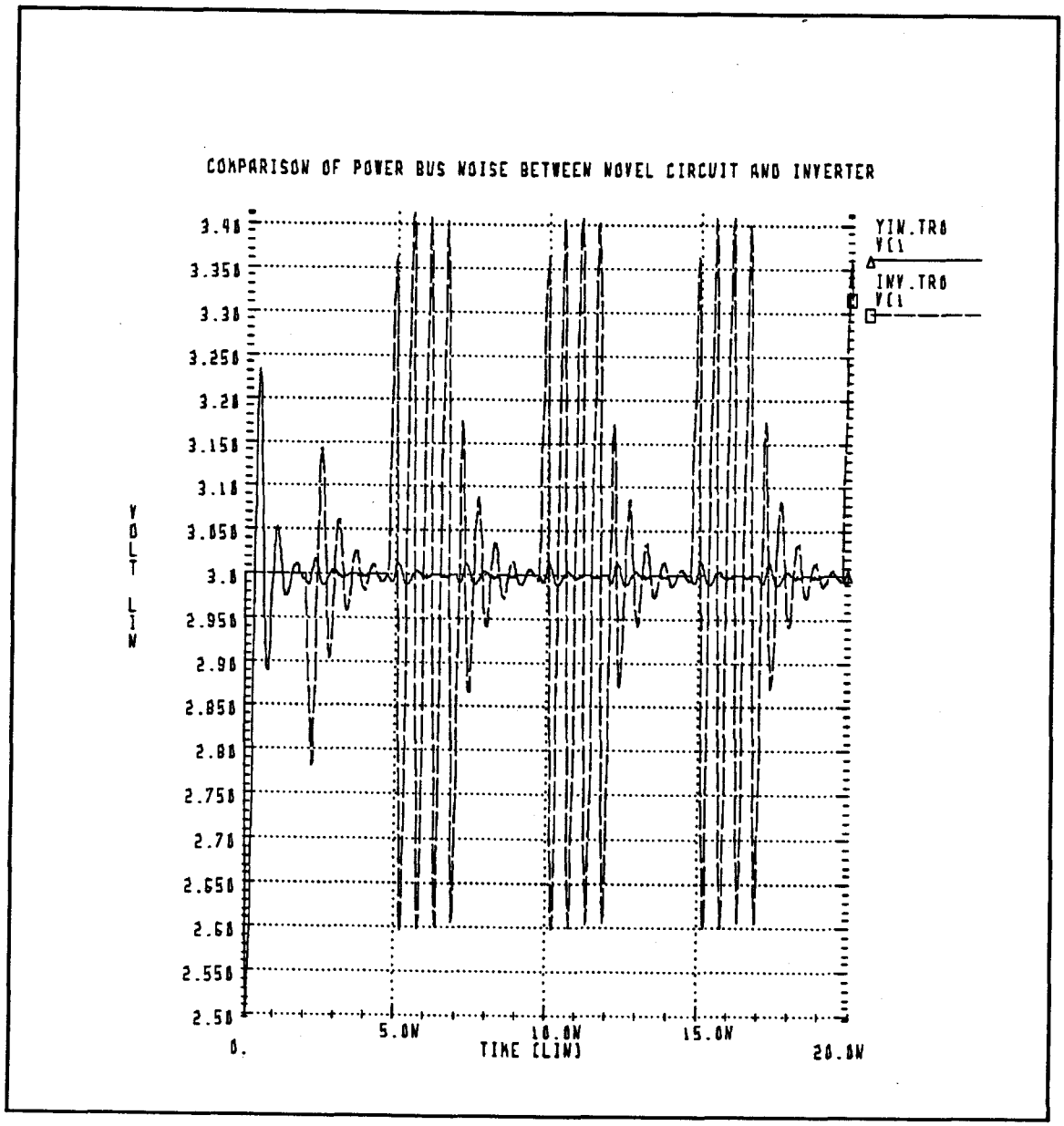

Figure 4.3.4 The ground bounce comparison between new circuit & conventional one

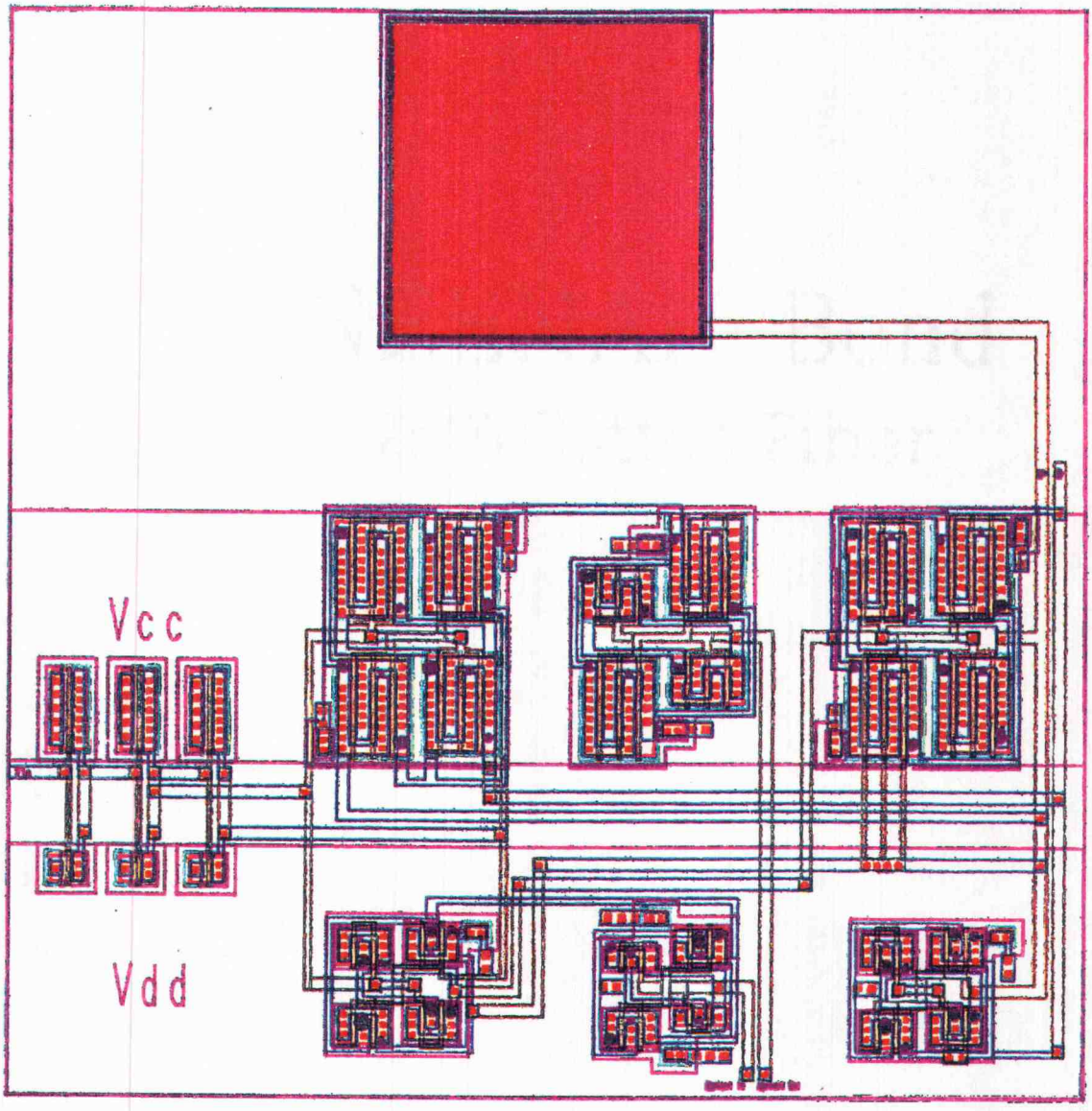

Figure 4.4.1 The layout of new circuit

4.5 Summary

Our second approach achieves the main purpose of this circuit design. The simulation results show that the circuit works very well. Inspite of power consumption, the lowest power noise displayed by this circuit is very attractive for the future high precision circuit designs.

Chapter 5. Conclusion

5.1 Summary

The original goal of this research was to design a CMOS output buffer which is capable of driving ECL compatible parts with low supply noise. The first step we took was to examine the cause of supply noise by the buffers in a chip. From equations (1) and (2) we found three parameters – the parasitic inductance, the transient time, and the rate of current change, which contribute to the supply noise. Literature search suggested that reducing the first parameter and the careful controlling of the second have been reported and commonly used. We believe there is no known design utilizing the reduction of the third parameter. Therefore, instead of investigating more on the known methods we looked into reducing noise by reducing the third contributing parameter, namely the rate of current change. Since the amount of current determines the speed of the circuit, we would like to maintain the absolute amount of current while minimizing only the rate of current change. With this requirement we found that the differential structure used in analog circuit design to be useful. Our first attempt utilize two opposite type modified differential amplifiers. We utilized the large signal property of these two amplifiers to balance the current flow. The end result is a design which has very little current rate change. However, the cost of this design is quite large. Not only it needs quite a few number of transistors, the sizes of the last stages are large also. This makes the design impractical in a chip which demands area. Further modification, therefore, was done to the first design to yield our second circuit structure. This structure uses self–biasing techniques as well as feedback to reduce the overall hardware cost. Again this design is shown to have a very low supply noise. However, one possible draw back is that the power supply voltages needed for this design is different from a typical CMOS digital circuit power supply voltage. Extra pins are necessary for these different voltages.

5.2 Possible Future Work

Our second design achieves the main purpose of the original goal of this research. Simulation results show that the circuit works well and it introduces very little noise to the supply line. But since the circuit performance depends on the accuracy of the current source and the match of the symmetry transistors, the fabrication technology will be the critical point of this design. More effort could be put into the investigation reducing the circuit's sensitivity to fabricating process parameters. Also, because the skew between IN and $\overline{\text{IN}}$ is critical to this off–chip driver for high frequency operation, specially crafted circuits which matched the delay and skew of input signal and its complement are needed to generate IN and $\overline{\text{IN}}$. Moreover, research should be performed to see if there is a possible circuit structure which does not require extra supply voltages.

Bibliography

[1] Intel Microprocessor Data Book Vol.I & II, Intel, 1992.

[2] ALPHA Data Book, DEC, 1993.

[3] Thaddeus Gabara and David Thompson, "Ground Bounce Control In CMOS Integrated Circuits", ISSCC88, pp.88–89, February 17, 1988.

[4] Michel S.J.Steyaert, Wout Bijker, Pieter Vorenkamp and Jan Sevenhans, " ECL–CMOS and CMOS–ECL Interface in 1.2–um CMOS for 150–MHz Digital ECL Data Transmission Systems " IEEE J. Solid–State Circuits, vol.26, no.1, pp.18–23, 1991.

[5] Hussein I.Hanafi, Robert H.Dennard, Chih–Liang Chen, Russell J.Weiss and David S.Zicherman " Design and Characterization of a CMOS Off–Chip Driver/Receiver with Reduced Power–Supply Disturbance " IEEE J. Solid–State Circuits, vol.27, no.5, pp.783–791, 1992.

[6] C.J.Bartlett et al., " Multichip packaging design for VLSI–based systems, " IEEE Trans. Components, Hybrids, Manuf. Technol. , vol. CHMT–10, no.4, pp.647–653, 1987.

[7] E.E.Davidson, " Electrical design of a high speed computer package, " IBM J. Res.Develop. vol.26, no.3, pp.349–361, 1982.

[8] T.Yoneda, M.Tomaki, S.Sugatani, and Y.Ezaki, " An ECL compatible full CMOS 210 Mbps crosspoint switch, " IEEE CICC Proc., pp.10.7.1–10.7.4, 1989.

[9] K. Toh et al., " Wide–band low–noise matched impedance amplifiers in submicrometer MOS technology, " IEEE J. Solid–State Circuits, vol. SC–22, no.12, pp.1031–1040, 1987.

[10] Itoh,Y., et al., " Noise–Generation Analysis and Noise–Suppression Design Techniques in Megabit DRAMS, " IEEE J. Solid–State Circuits, vol. SC–22, no.8, pp.619–621, 1987.

[11] Shoji,M., " Reliable Chip Design Method in High Performance CMOS VLSI, " ICCD 86 Digest, no. 10, pp.389–392, 1986.

APPENDIX

APPENDIX : SPICE Deck Used for Simulation

```
* New version motified from version3, current inject directly
* N-diff amp
V1p1 1 25 0
V1p2 1 26 0
M5 3 2 25 25 P L=1 W=90 PD=100 PS=100 AS=450 AD=450
M6 2 3 26 26 P L=1 W=90 PD=100 PS=100 AS=450 AD=450
M1 2 4 6 6 N L=1 W=20 PD=30 PS=30 AS=100 AD=100
M2 3 5 6 6 N L=1 W=20 PD=30 PS=30 AS=100 AD=100
* current source
Iref1 6 100 6ma
*M9 12 12 100 100 N L=1 W=10 PD=20 PS=20 AS=50 AD=50
*M10 60 12 100 100 N L=1 W=20 PD=30 PS=30 AS=100 AD=100
Vcsn 60 6 0
*P-diff amp
* current source
Vcsp 17 7 0
*M11 13 13 1 1 P L=1 W=22 PS=32 PD=32 AS=110 AD=110
*M12 17 13 1 1 P L=1 W=90 PD=258 PS=100 AS=450 AD=450
Iref2 1 17 6ma
*
M3 2 4 7 7 P L=1 W=90 PD=100 PS=100 AS=450 AD=450
M4 3 5 7 7 P L=1 W=90 PD=100 PS=100 AS=450 AD=450
*
M7 3 2 100 100 N L=1 W=20 PD=30 PS=30 AS=100 AD=100
M8 2 3 100 100 N L=1 W=20 PD=30 PS=30 AS=100 AD=100
*Input inverter
*M14 5 4 1 1 P L=1 W=32 PD=42 PS=42 AS=160 AD=160
*M15 5 4 100 100 N L=1 W=8 PD=18 PS=18 AS=40 AD=40
*M16 4 21 1 1 P L=1 W=32 PD=42 PS=42 AS=160 AD=160
*M17 4 21 100 100 N L=1 W=8 PD=18 PS=18 AS=40 AD=40
*M18 21 20 1 1 P L=1 W=96 PD=106 PS=106 AS=480 AD=480
*M19 21 20 100 100 N L=1 W=24 PD=34 PS=34 AS=120 AD=120
*Cext1 2 105 1pf
Cext2 3 105 1pf
*L1 2 14 5nh
*l2 3 16 5nh
T1 2 105 15 105 Z0=75 TD=1ns
T2 3 105 18 105 Z0=75 TD=1ns
R1 15 105 75
R2 18 105 75
*Input
vin1 4 0 pulse (3 0 2ns 0.25ns 0.25ns 2.5ns 5ns)
vin2 5 0 pulse (0 3 2ns 0.25ns 0.25ns 2.5ns 5ns)
```

```
*vgnd 100 0 −2
vegnd 105 0 −2
vdd 101 1 0
vdc 101 0 3
.inc hdr
.tran 0.01ns 20ns
.print tran v(3) v(2) v(6) v(7) v(4) v(5)
.print tran i(vdd) i(vgnd) i(M1) i(M2) i(M3) i(M4) i(M5) i(M6)
+ i(M7) i(M6) i(M9) i(M10) i(M11) i(M12)
.options post
.end
```