AN ABSTRACT OF THE THESIS OF

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Title: Physical Mechanisms, Device Models, and Lifetime Projections of Hot-Carrier Effects in CMOS Transistors

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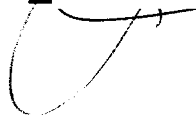
Abstract approved: 

Leonard Forbes

The purpose of this work is to investigate the theoretical and practical aspects of reliability analysis including physical mechanisms, parameter mismatches, lifetime projections, circuit analysis, and reliability improvement techniques. A spectral analysis of oxide trap energy distributions after hot-electron injection in LDD n-MOSFET's at room temperature and above has been performed by using both electric field stimulated (or tunneling) and thermal emission methods. It has been found that the trapping mechanisms of both deep levels (2.4eV) at room temperature and shallow levels (0.9eV) below room temperature are similar. Two new reliability models for analog IC designs and reliability projections have been proposed by applying channel mobility reduction due to hot carrier induced interface states. One of the proposed reliability models is a drain conductance (gd) degradation model which is a function of the transconductance (gm) degradation in the linear region which is then used to determine parameter mismatches in analog IC designs. This is then applicable to lifetime predictions of analog circuits. It has been found that the gd degradation lifetime (i.e., τ gd) is less dependent on Leff than τgm, and is shorter than τgm when Leff is longer than 1.2μm. The other model is the hot-carrier induced series (drain) resistance (ΔRd)

enhancement model for reliability projections of analog IC designs. The proposed ΔRd model, based on the increase of the hot-carrier induced interface trapped charge (ΔNit), shows a good agreement between the increase of the series resistance in the drain region and the degradation of device characteristics. A specific example of a reliability projection has been given to show that the ΔRd model (one parameter) is much simpler and more applicable in analog IC designs rather than the commercial reliability simulator (i.e., BERT) which requires a set of stressed device parameter files (6 parameters). In order to demonstrate reliability projections using the proposed reliability models, a conventional CMOS differential amplifier has been employed as an example of analog and mixed-mode IC designs.

Physical Mechanisms, Device Models, and Lifetime Projections of Hot-Carrier Effects in CMOS Transistors

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PHYSICAL MECHANISMS, DEVICE MODELS, AND LIFETIME PROJECTIONS OF HOT-CARRIER EFFECTS IN CMOS TRANSISTORS

1. INTRODUCTION

The technical advances in the semiconductor industry have been accompanied by the development of the physics for device operation. The metal oxide semiconductor field effect transistor (MOSFET) has been chosen as a representative type of silicon device and is commonly used in contemporary very large scale integrated circuits (VLSI). In addition, the complimentary MOSFET technology (CMOS) has high-speed and allows low-power operation, the integration scale achievable with CMOS is the greatest strength of leading semiconductor technologies. As a consequence, this MOSFET technology has been the most challenging and active area in the IC industry over the last three decades [1]-[3].

As the size of silicon devices is reduced into the range of sub-micron dimensions, the injection of hot electrons from the silicon into the gate silicon dioxide layer generates electron oxide traps and surface state damage. This is one of the main physical mechanisms that determines the reliability of MOS structure-based device performance. The hot-carrier effects in CMOS devices can be summarized by an increase of threshold voltage (surface trapping and recombination) and a decrease of transconductance (channel mobility degradation) resulting in decreased drain current. Substrate current has become a major parameter to monitor hot-carrier effects under

operating conditions and in determining the lifetime projection of CMOS devices and IC's.

Much of the applicability of the study of hot-carrier effects in the field of semiconductor devices rests upon the progress made in physical analysis and model of hot-carrier effects. Moreover, reliability considerations due to hot-carrier effects of size-constrained devices (i.e., deep sub-micron devices) in VLSI circuits provide design guidelines and alternatives to maintain reliability assurance during device operation.

1.1 Literature Review

The hot-carrier is defined under the influence of the high electric field as the effective carrier (both electrons and holes) temperature based on the carrier energy becomes much greater than ambient temperature in equilibrium with the lattice. The concept of the hot-electron is very important in modeling device characteristics under the high electric fields, where the electron drift velocity becomes saturated and comparable to the thermal velocity ($\sim 10^7$cm/sec). As the size of the device decreases with a constant power supply voltage (i.e., 5V), the increase of the internal electric field becomes unavoidable. Thus, hot-carrier effects including both the hot-electron and the hot-hole become the main cause of CMOS device degradation. Consequently, lifetime projections and reliability models of hot-carrier induced MOSFET degradation have been developed under operating conditions (i.e., AC/DC operation conditions) including the worst case of operation and/or power supply [4]-[49]. The recent studies of hot-carrier effects on device degradation can be summarized as follows;

Region	Location	Organization	References
U. S. A.	CA	U. C. Berkeley	[4]-[5]
		Hewlett-Packard	[8]-[10]
		Intel	[11]-[13]
	TX	U. T. Austin	[14]-[17]
		Texas Instrument	[18]-[19]
		Motorola	[20]-[21]
	NJ	AT&T Bell Lab.	[22]-[25]
	NY/VT:	IBM	[26]-[27]
	MA	Digital Equip. Co.	[28]-[29]
Europe	German	Siemens AG	[30]-[33]
	France	BULL Co.	[34]-[36]
	Belgium	IMEC	[37]-[38]
Japan		Hitachi Ltd.	[39]-[43]
		Toshiba Corp.	[44]-[45]

This summary was based on literature from IEEE Trans. Electron Devices, IEEE Electron Device Lett., IEDM Tech. Dig., and Proc. of Int. Reliability Phys. Symp..

Among these research groups, U. C. Berkeley, Siemens, and Hitachi have been most active in reliability modeling and studying the device structure and the process induced hot-carrier effects. The detailed works of these three groups can be summarized as follows;

U. C. Berkeley	Physical and empirical modeling of MOSFET's degradation under DC [7], and AC [5], [6], stress conditions.
Siemens	Degradation modeling under various AC stress waveforms [30], [33].
Hitachi	Degradation modeling [43], and structure [39], and process induced hot-carrier effects [40]-[42].

The device physics and reliability modeling of the hot-carrier induced device degradation have been developed under DC operating conditions [7], [43], and are still being developed under AC conditions with various waveforms, [5], [6], [8], [9], [28], [30]-[33], [38], including the temperature dependence of hot-electron effects [10], [37], [45]. The complete physical and empirical AC modeling of the hot-electron-induced device degradation under various waveforms and stress conditions is expected to be achieved.

The conventional technologies to suppress the hot-carrier effects are summarized in Table 1-1. The primary guidelines to reduce the hot-carrier effects are, then, summarized as follows;

1) reduce the high electric field near the drain region (low hot-carrier injection),
2) reduce the damage sites (i.e., less trapping centers in either oxide or interface),
3) improve hot-carrier immunity (i.e.; high binding energy).

The MOSFET device structure [29], [39], [44], [46], which induces the hot-electron effect has been well summarized by J. J. Sanchez et al., [46], and this issue will be continuously discussed as new technologies which result in the scaling of devices are developed. Recently, various processing technologies have been generating new insight into the hot-electron effect (i.e., oxidation growth conditions [14], [16], [17], [40],

Table 1-1 Comparison of technology developments for hot-carrier effects.

Level	Method	Technology	Highs	Lows
Device	**Structure**	DDD (1.5μm)	Simple	Bigger Lateral Diffusion
		LDD (0.8 μm)	Controllability of n- Region	Sidewall Effects
		GOLD (0.5 μm)	Reduced Emax	Complicated Proc. Increased C
	Process	Ge, F, C, etc.	Enhanced Hot-Carrier Immunity	Low μ_{eff} (Ge & C) Δt_{ox} (F)
		Gate Oxide Formation		High Temp. Proc.
Circuit	**Extra Device**	Digital	Conventional . Process Tech.	Extra Transistors
	Shield Device	Mixed-Mode		

radiation [47] or irradiation [48] treatments, and doping methods [23], [41], [43], [49].) The results have been quite promising and may be useful in future applications.

1.2 Technology Trends

As shown in Figure 1-1, the IC industry has been doubling the circuit density every two years based on the reduction of the channel length and gate oxide thickness. Recently, Micro Tech 2000, recommended by the National Advisory Committee on Semiconductors (NACS), has been proposed providing the US industry with 0.12μm IC technology by the 21st century [50]. Also, IBM Thomas J. Watson Research Center, Yorktown Heights, N.Y., has announced 0.1μm design rules, whose minimum active area MOSFET is 0.7μm×0.15μm, for 4G-bit DRAM's [51]. Furthermore, in some research laboratories the channel length of MOSFET has been already scaled down to beyond 0.1 μm which is a limit of the classical scaling of MOSFETs. However, the circuit properties were seriously affected by poor subthreshold characteristics, causing the logic swing to decrease with short-channel devices due to the increase of subthreshold current in short channel devices.

The electric field of the oxide breakdown and the typical maximum allowable gate leakage current specification (~1μA/cm^2) lowers the maximum allowable electric field of a gate oxide to 7MV/cm [52] which is less than the physical breakdown electric field of 10MV/cm. However, the future trends cannot follow a simple mathematical reduction in channel length and oxide thickness without supporting processing technology such as oxidation and fine pattern lithography which are approaching, or may have already reached their tolerance limits. Also, effects of statistical fluctuation on device edge definition in fabrication and dopant distribution on minimum size

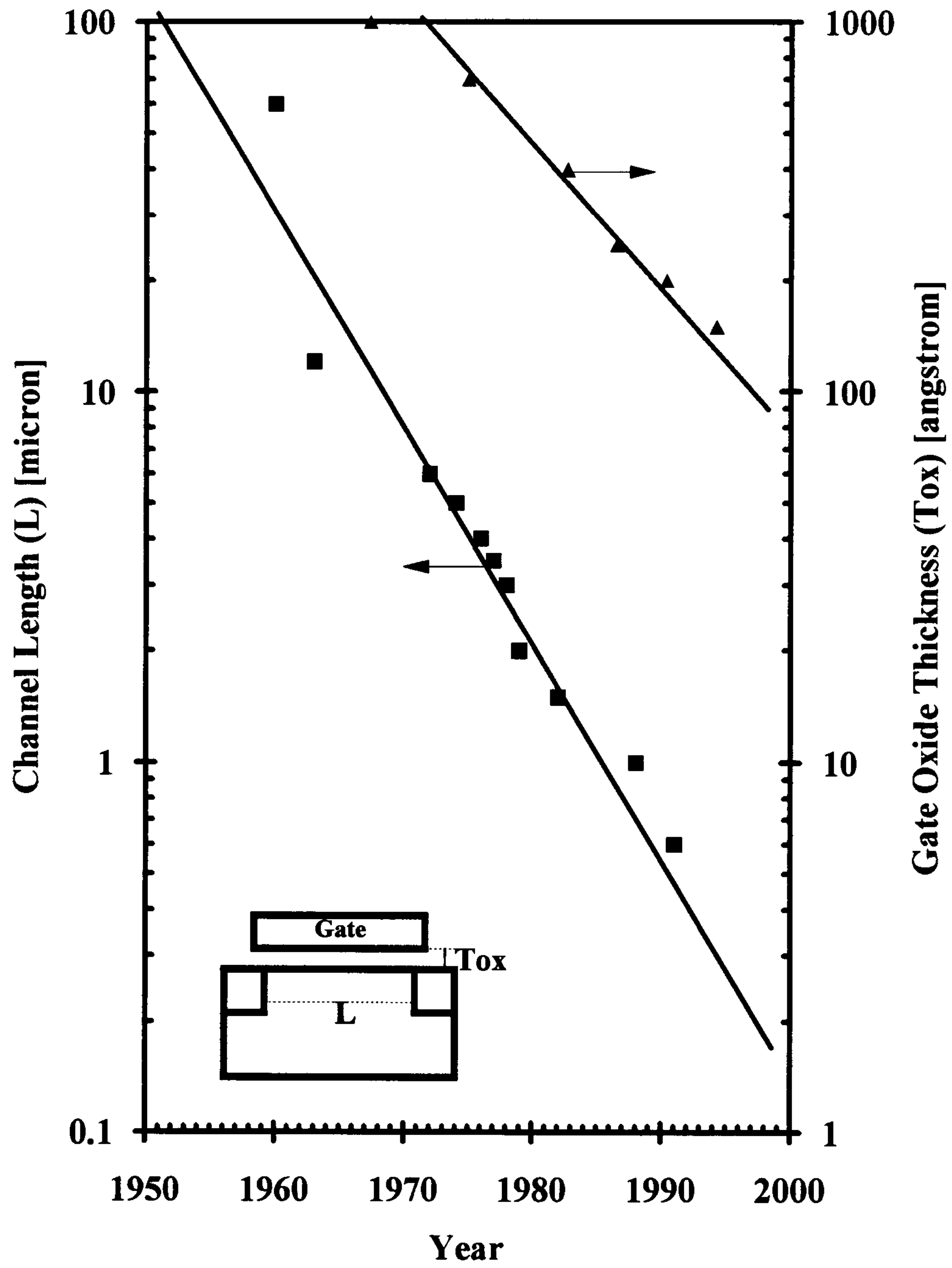


Figure 1-1 CMOS technology trend.

devices has become problematic; for instance, a technical breakthrough for precisely controlling dopant distribution must be achieved.

Power dissipation in a compact chip is well known to limit the maximum density of devices integrated on the chip [53]. As channel length decreases, an increasing electric field with the unscaled power supply (i.e., Vdd=5V) has been a primary cause of hot-carrier effects in past. However, the electric field in the devices can be kept constant by scaling down the power supply to 3.3V or below while reducing the threshold voltage and the logic swing in proportion to the decreasing power supply. In spite of technical difficulties in maintaining the same performance while lowering the IC power supply, the concept of the low power supply has two major commercial advantages in the IC industry. One is the further miniaturization of micro-computers such as battery-operated laptops and palm-sized computers with light-weight and extended operating time. The second advantage is the improvement in reliable operation of the internal circuitry which cannot sustain normal operation with a 5V power supply. Kakumu et. al., Toshiba, Japan, [54] has reported the optimum power supply voltage of CMOS devices for each set of design rules based on hot-carrier induced degradation as shown in Table 1-2. From an engineering and physical perspective, the importance of a lower power supply is to reduce the internal electric field, thus, improving IC reliability by reducing the hot-carrier effects.

Therefore, the future trend of CMOS technology is strongly affected by the state-of-the-art technology in the IC industry as well as the design rules and an optimum choice of the power supply voltage. In the digital IC industry, a 128M DRAM at 100MHz with 3.3V will be available in micro-computer chips no later than the year 2000, possibly sooner, as projected in Figure 1-2.

Table 1-2 CMOS device design rules and device parameters [53].

Design Rule [μm]		2	1.2	0.8	0.6	0.5	0.3
V_{DD} [V]	Conv.	5	-		3.3	3	2.3
	LDD		5	5	4.5	4	-
Tox [nm]	Conv.	48	-	-	11	10	8
	LDD	-	26	15	13	13	-
Ids [mA/μm] Vth [V]	NMOS	0.12 0.78	0.21 0.76	0.40 0.58	0.40 (Conv.) 0.58	0.44 (Conv.) 0.56	0.52 (Conv.) 0.55
					0.48 (LDD) 0.68	0.51 (LDD) 0.68	
	PMOS	0.06 -0.79	0.13 -0.77	0.24 -0.71	0.22 @ 3.2V -0.59	0.24 @ 3.0V -0.56	0.28 -0.55
					0.28 @ 4.5V -0.68	0.26 @ 4.0V -0.68	

Optimum power supply voltage of CMOS devices can be empirically determined as follows where L is the channel length [μm] in the design rule.

Conventional MOSFET $V_{DD}\,[\mathrm{V}] = 6.1 \times \sqrt{\frac{L}{2}}$

LDD MOSFET $V_{DD}\,[\mathrm{V}] = 8.4 \times \sqrt{\frac{L}{2}}$

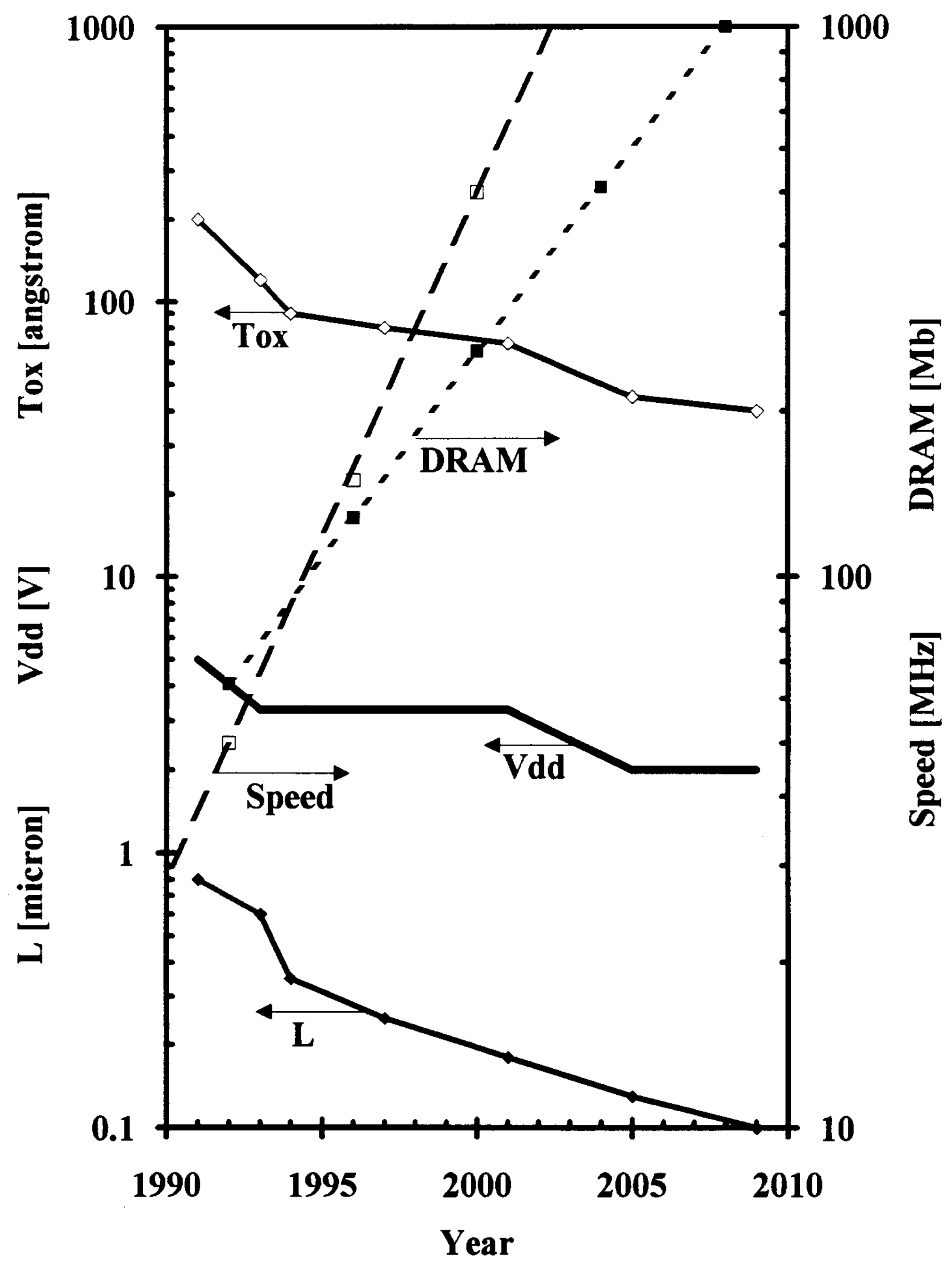


Figure 1-2 Projection of CMOS technology.

1.3. Overview of Reliability Analysis

In the early stages of the semiconductor industry, the initial value of yield was used as a measure of reliability since the statistical variations of device characteristics induced by operation conditions such as hot-carrier effects were negligible and infinitesimal as a result of the relaxed design rules and wide tolerance levels. However, the scaling of feature size has progressed more rapidly than the scaling of process tolerance resulting in the degradation of device characteristics under operating conditions which can no longer be neglected any more ($L \ll 2\mu m$). Parameter mismatches and consequent IC functional failures have become a consequence of process fluctuations during fabrication and the operating conditions of the IC's [55].

Therefore, the definition of reliability [56] has become different than that of yield which is a measure of the fraction of manufactured units that are functional at the time of manufacture. For instance, even if the semiconductor devices or IC's may still pass the yield test (i.e., burn-in) conducted at the manufacturing plant, they can malfunction in real-world operations with a shorter operational lifetime than the customary lifetime. The definition for reliability is then the probability that an initially functional device or circuit will perform as designated, under predetermined conditions, for a projected lifetime. From this definition, any time dependent aspect that degrades the effective functioning of a device is a legitimate issue of reliability analysis for today's custom-oriented IC industry.

Reliability models can be classified into two general categories: empirical models and physical models. Empirical models attempt to determine, through mathematical tests, the probability distribution underlying observed life test data. For example, an empirical reliability model can be obtained from monitoring the amount of device parameter shifts as a function of the stress time (i.e., [29], [43]). However,

physical models attempt to describe the degradation, with time, of the same physical parameters which is used as a measure of reliability. Such device parameters are related to physical attributes such as dimensions and material properties of the device, and operating or environmental conditions. The discrepancy between empirical and physical reliability models is due to the fact that there is an underlying probability distribution which governs the values of the physical parameters which enter into fundamental properties of the device. As a consequence of the difficulty of physical models, semi-empirical models are commonly adopted by measuring the change with time of a particular parameter.

One of the most important reliability analysis techniques is the accelerated lifetime test in which the reliability data within a reasonable time can be obtained by acceleration of the degradation or aging process. The validity of the results of accelerated lifetime tests strongly depends upon the assumption that the degradation process is only accelerated and not altered. Therefore, reliability analysis in the IC industry is a concurrent field of semiconductor devices and IC design as shown in Figure 1-3.

1.4 Motivation and Objectives

The main scheme and impact of this research in the field of semiconductor devices and IC design is illustrated in Figure 1-3. The purpose of this research consists of developing a physical reliability model which can assure simple and versatile applicability in the IC industry, and proposing reliability projection techniques based on the physical analysis of hot-carrier induced degradation mechanisms in CMOS transistors.

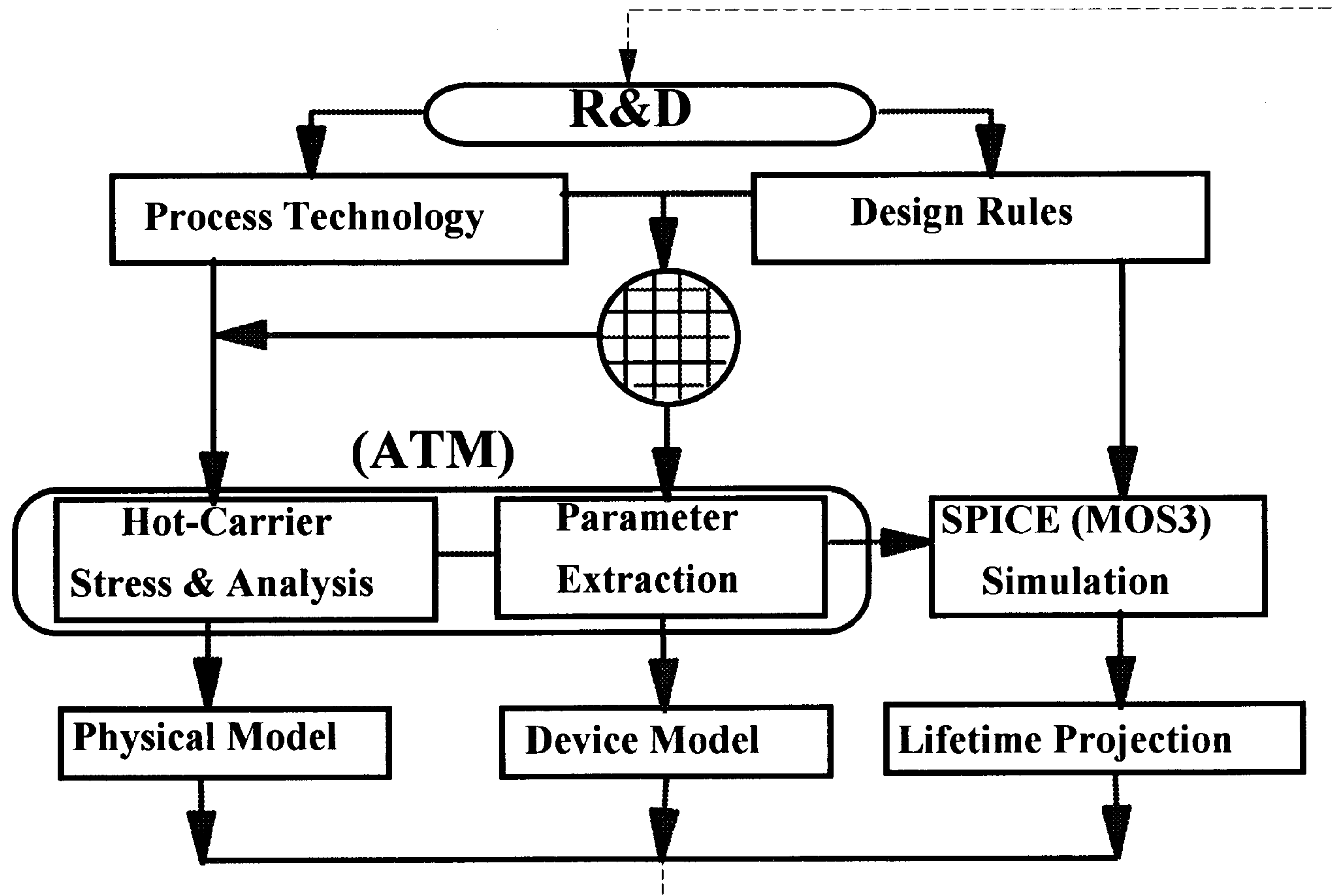


Figure 1-3 Structure of reliability analysis of hot-carrier effects.

In chapter 2, the fundamental physical mechanisms of degradation have been reviewed including substrate current models. Comparisons have been made between p- and n-channel devices of different drawn channel lengths in terms of hot-carrier induced degradation based on substrate current models for reliability projections.

In chapter 3, the device part of this work has been to analyze the effects of using drain avalanche hot carrier injection (DAHI) and electric field stimulated re-emission (EFSE) techniques on CMOS sub-micron devices. The physical mechanisms of hot-carrier induced device degradation have been studied by investigating the electron trapping energy levels in CMOS gate oxides. Also, hot-carrier induced interface trap charge has been investigated by using the charge pumping method.

In chapter 4, the lifetime projections for current foundry service technologies have been investigated by accelerated lifetime tests, and comparisons have been made between HP34-CMOS and HP26B-CMOS processes. Also, empirical models of hot-carrier induced device characteristics and the device model parameters of SPICE MOS level 3 have been developed for reliability simulations.

In chapter 5, a physical model of drain conductance degradation due to hot-carrier injection is proposed for lifetime projections in analog IC's. The proposed drain conductance (gd) degradation model has been found to be a function of the gm degradation in the linear region. This results in parameter mismatches in analog IC designs, which are then applicable to the lifetime prediction for analog IC design. Also, design guidelines based on the gd degradation model have been described for analog IC's.

In chapter 6, a hot-carrier induced series resistance enhancement (ΔRd) model of nMOSFET's is proposed for reliability projections in analog IC design. The proposed ΔRd model is based on the increase of the hot-carrier induced interface trap charge (ΔNit). Furthermore the reliability projection is demonstrated to show the ΔRd

model (one parameter) is much simpler and more applicable in analog IC design rather than the commercial reliability simulator which requires to extract a set of stressed process files (6 parameters in the BERT).

In chapter 7, concluding remarks on this study have been summarized and future work has been suggested.

In appendix A, a new design technique using a composite nMOSFET is introduced to reduce the effects of substrate current and hot electron injection; thus, improving circuit reliability. Comparisons have been made between the performance of this design technique and other alternatives.

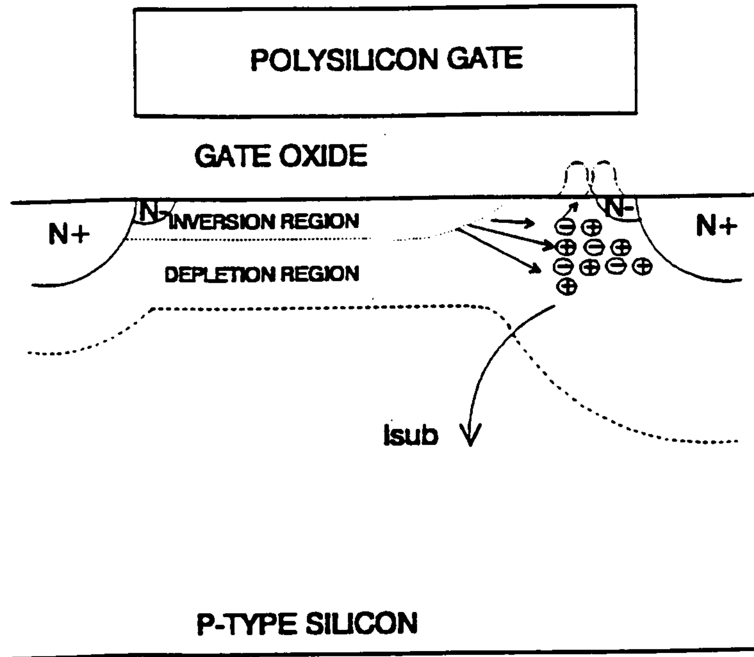
In the device models and the reliability projections (Chapt. 4, 5, and 6), a CMOS single-ended output differential amplifier has been adopted as representative analog IC designs. Although digital IC design is more concerned with speed and performance in circuit simulations, analog IC design requires more accuracy. The performance of an analog IC is strongly related to its DC bias condition, at which parameter mismatches can affect every aspect of the circuit performance. Hence, the concentration of this work is to analyze the performance and investigate the effect of hot electron injection on devices in both types of circuits.

2. HOT-CARRIER EFFECTS ON DEVICES

2.1 Introduction

The down scaling of integrated circuit device dimensions and layouts has been driven by the desire to reduce die costs, increase chip performance, and to increase the number of functions available on a single chip (chip complexity). The threshold electric field for the hot-carrier injection is around 100 kV/cm [54] in silicon devices, which limits the device shrinking process. Above the threshold electric field, the effective carrier temperature increases much higher than the ambient temperature, that is, the energy gain rate of electrons and holes from the field is greater than the energy loss rate to the optical phonons. During device operation, hot-carrier effects result in several reliability problems as previously described. Fig. 2-1 illustrates a schematic diagram of the hot-carrier mechanisms showing the impact ionization and the avalanche multiplication processes [58]-[60]. Impact ionization is a collision process by which carriers gain sufficient energy from an electric field to create electron-hole pairs upon colliding with atoms in the lattice as shown in Fig. 2-1. The channel carriers (electrons in nMOSFET's or holes in pMOSFET's) gain energy as they travel through the high-field region. Some of the carriers gain sufficient energy (at least the bandgap energy) to ionize the atoms upon collision resulting in carrier multiplication. This excess carrier generation is called avalanche multiplication. In nMOSFET's, the electrons created are swept by the field toward the drain, while the holes become the substrate current.

Hot-carrier injection can be divided into two categories [21]: channel hot-carrier injection (CHI) and drain-avalanche hot-carrier injection (DAHI). Once the surface of a transistor is inverted, the applied drain voltage accelerates channel carriers



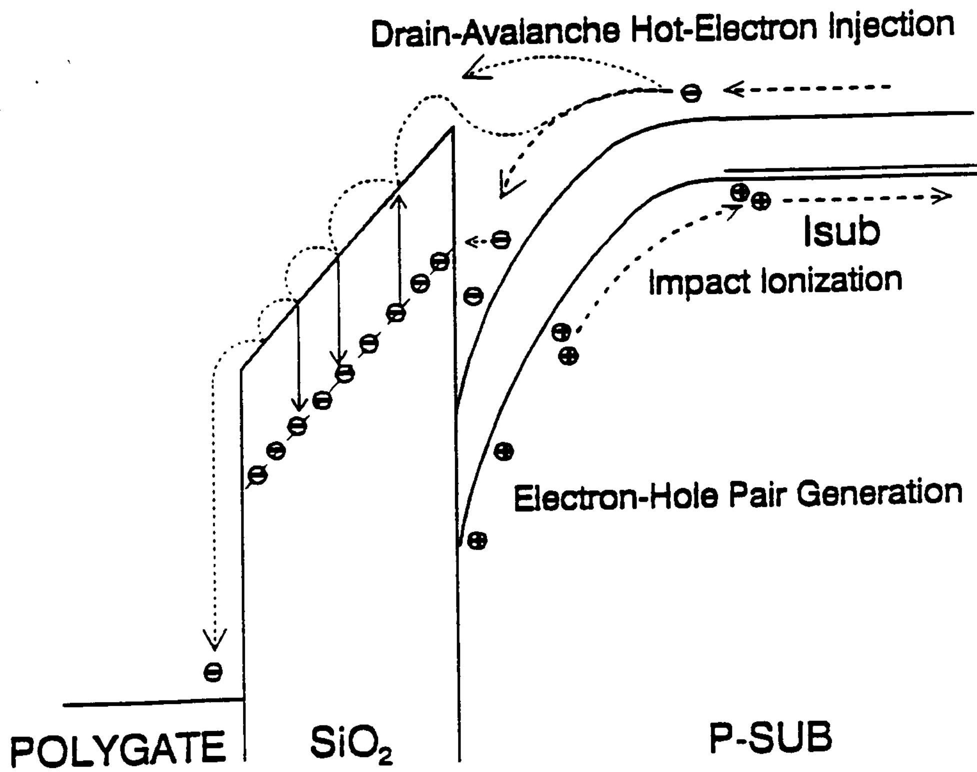


Figure 2-1 Schematic diagram of hot-carrier mechanisms.

from the source to the drain. Before reaching the drain edge, some of the channel carriers gain enough energy to surmount the $Si\text{-}SiO_2$ interface potential barrier. Thus, this mechanism is called CHI. Some of channel hot-carriers collide with atoms of the lattice in the pinch-off region during saturation operation and excite electron-hole pairs by impact ionization. Some of the impact ionization induced carriers will have a high enough energy to overcome the $Si\text{-}SiO_2$ interface potential barrier. This mechanism is then called DAHI. Both CHI and DAHI generate carriers traversing the gate oxide in which the injected carriers are accelerated and monitored as gate current. The hot carriers injected into gate oxide can lead to the formation of interface states and trapped oxide charge. The resulting degradation which is referred to hot-carrier effects can lead to device failure. Additionally, the substrate current produced by impact ionization can produce 4 terminal latch-up in CMOS structures [62]-[63].

Due to the inherent differences of the majority carriers in CMOS devices; in nMOSFET's, electrons and in pMOSFET, holes; and the potential barrier of electrons (3.1eV) and holes (4.8eV) [59]-[60]; the transistors in a CMOS circuit experience different amounts of hot-carrier induced degradation as shown in Table 2-1. Although both CHI and DAHI occur in both p- and n-MOSFET's, hot-carrier induced degradation of pMOSFET's in terms of threshold voltage shifts, transconductance shifts, and drain current shifts is much less than that of nMOSFET's [64]-[65]. For the nMOSFET case, electron injection into the oxide near the drain is responsible for interface state generation and negatively charged traps, and that the positive charge is due to trapped holes being injected into the same region. In order to improve process optimization and assess device reliability in CMOS technology, hot-carrier effects in nMOSFET's only have been investigated in this study.

Another limitation to the device shrinking process has been imposed by equipment and processes (i.e., fine pattern lithography) which the IC industry is using.

Table 2-1 CMOS device characteristics after hot-carrier injection.

MOSFET (W=50μm, Tox=20nm)	Type	N	P	P
	L [μm]	1	1	0.6
Stress Condition (DAHI)	Vds	7.0V	-7.0V	-7.0V
	Vgs	2.5V	-2.0V	-2.0V
	Isub(max)	-490μA	7μA	22μA
	Stress time	1441 min	1441 min	961 min
Threshold Voltage	Vth_O	0.746V	-0.873V	-0.864V
	Δ|Vth|	+74.4%	-2.3%	-15.4%
Max. Transconductance	gm_O(max)	592μS	154μS	227μS
	Δgm(max)	-23.2%	+18.3%	+36.2%
Sat. Drain Current |Vds|=6.5V, |Vgs|=5.5V	$Idss_O$	18.17mA	-8.51mA	-11.8mA
	Δ|Idss|	-11.4%	+5.0%	+13.0%

The trade-off issues are largely those of performance and density versus manufacturability. Thus, technical progress is necessary in understanding the role of key physical parameters on these degradation mechanisms and ultimately on their control within safe limits [66]-[68].

The purpose of this chapter is, hence, to offer an introductory review of hot-carrier effects on devices. Some basic concepts and measurement techniques will be explained and discussed.

2.2 Hot-Carrier Induced Device Degradation

Figure 2-2 shows a schematic representation of the hot-carrier induced currents which have been monitored as gate, drain, and substrate currents. The most important feature of the hot-carrier induced currents is that the currents are composed of both electrons and holes and vary as functions of gate voltage. The drain voltage (Vds) represented here is high and in the order of 7V which is the typical stress condition for hot-carrier injection.

The gate current in Fig. 2-2 is a good example of the both electron and hole injection. Hot-carrier injection starts even with low gate voltages. The carriers can turn around inside the oxide and come back to the interface again, and then go back into the channel, at least a major portion of them because of the orientation of the electric field inside the oxide. The electric field is in this instance determined by a high drain voltage and a low gate voltage. On the other hand, since the barrier height of holes for injection into the oxide is higher than that of electrons, hole injection will require a higher field. Hence, as the electric field becomes higher with the increase of gate voltage, holes can be still injected into the oxide, but not as readily as electrons. Hole injection

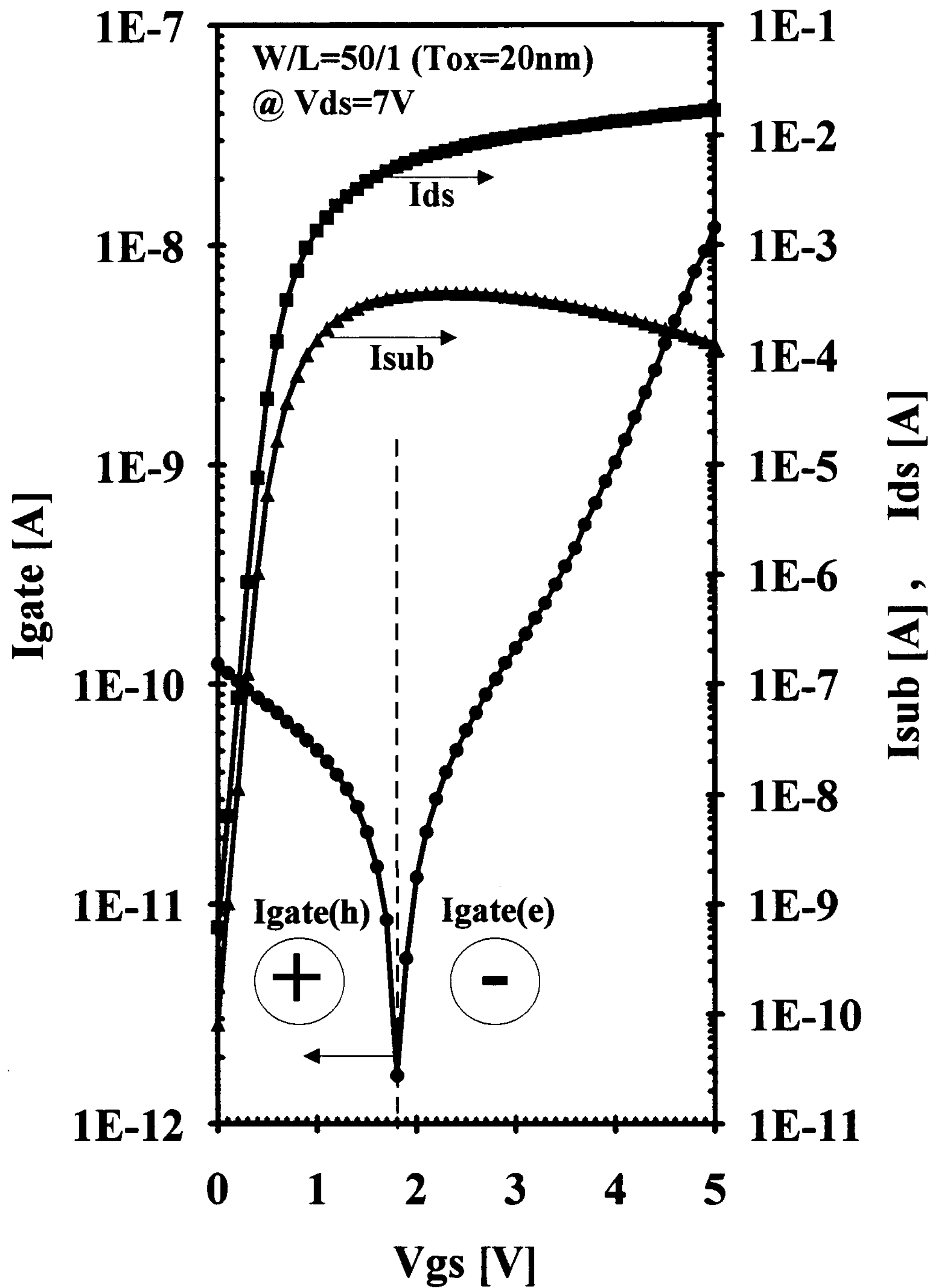


Figure 2-2 Hot-carrier induced currents of an nMOSFET in terms of drain, substrate, and gate currents.

predominantly occurs at low gate voltage while electron injection becomes dominant at high gate voltage. It should be noted that, even at very low gate voltages ($Vgs<1.5V$), electron injection already exists. Hence, in the MOSFET due to the inhomogeneous field distribution, it is impossible to achieve and analyze a situation where either hole or electron injection exists exclusively. Thus, there is no way to measure experimentally the maximum injected current of either electrons or holes.

The number of carriers in the channel increases with increasing gate voltage but there is no step at the threshold voltage but rather a gradual increase. For higher gate voltages, since the gate and drain voltages become comparable, this increase of the gate voltage reduces the net electric field inside the oxide near the drain. Hence, the substrate current and the gate current decrease for higher gate voltage, $Vgs>6V$, as the electric field goes down as shown in Fig. 2-2. This combination of applied electric fields and carrier generations causes a maximum condition of hot-carrier injection. Fig. 2-3 shows the hot-carrier induced threshold voltage shifts of nMOSFET"s as a function of channel length with W=50μm. It should be pointed out that the hot-carrier induced threshold voltage shifts become most noticeable at channel lengths below 2μm. Hence, the hot-carrier effects are mainly as result of small geometry devices. Also, as shown in Fig. 2-3, the threshold voltage shifts are very closely related to the substrate currents induced by hot-carrier generation. For that reason, in the study of hot-carrier effects (mainly in nMOSFET's), the maximum in the substrate current, which is around $Vgs\leq 0.5\cdot Vds$, has been the primary parameter used for monitoring the hot-carrier effects and correlating with lifetime projections.

Figure 2-4 shows a comparison of the Ids-Vgs characteristic curves for pre- and post-stress. After hot-carrier injection, the I-V characteristic curves are not totally symmetrical with respect to the source-drain terminals because the damage caused by hot-carrier injection is localized at the drain region. The device parameter shifts are

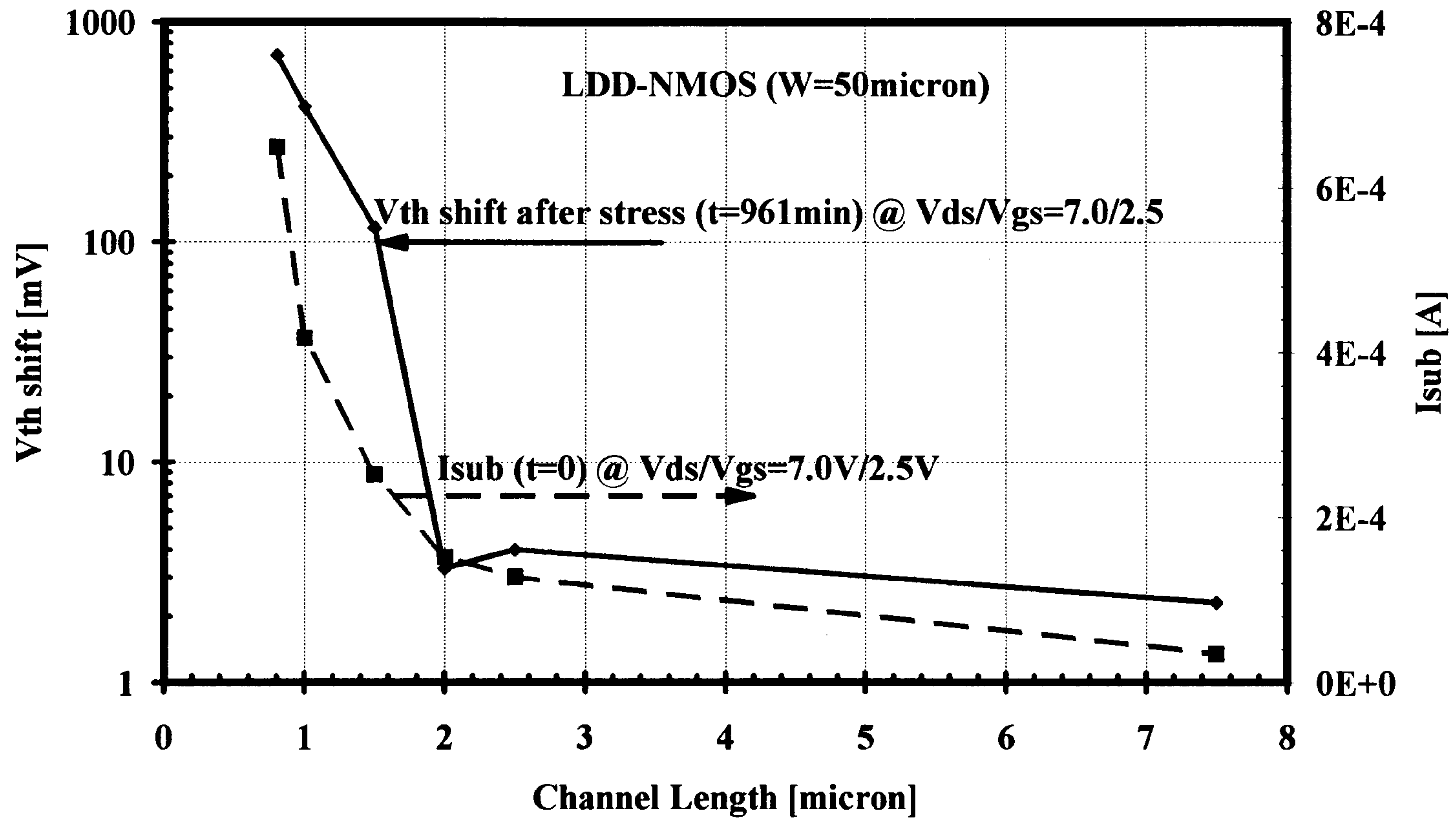


Figure 2-3 Substrate currents and threshold voltage shifts under hot-carrier injection as a function of channel lengths.

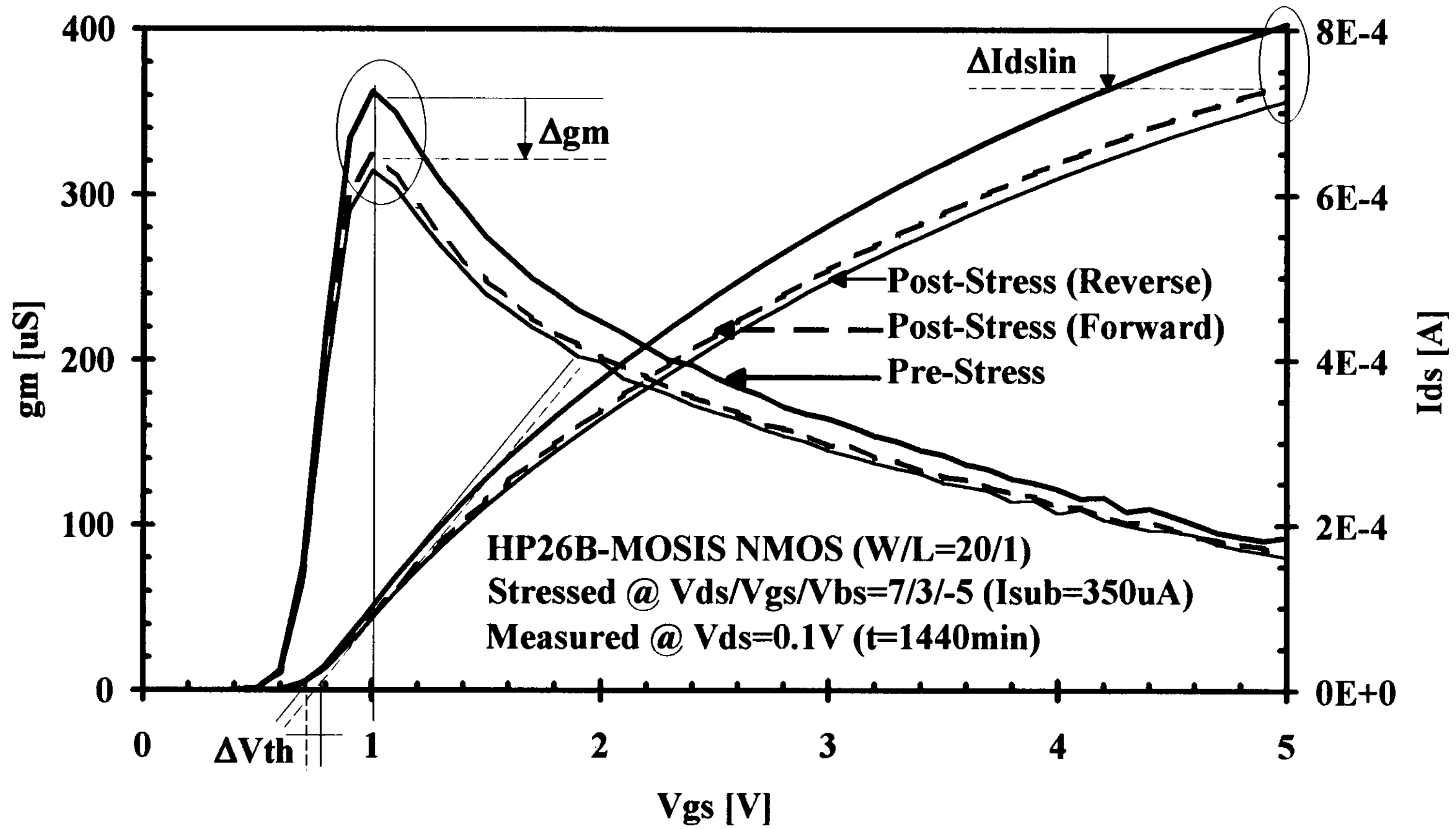


Figure 2-4 Ids-Vgs characteristic curves of an nMOSFET device under hot-carrier injection.

slightly larger in the reverse mode than forward mode, where reverse mode means that the source and drain terminals are reversed during measurement and the forward mode means that the source and drain terminals are the same during hot-carrier stress and measurement. Also, Ids-Vds characteristic curves of pre- and post-stress are shown in Fig. 2-5. For simplicity, mainly the forward mode device characteristics have been studied. The device parameters of interest in the linear region are the threshold voltage (ΔVt), the maximum transconductance in linear region (Δgm at Vds=0.1V), and the linear drain current (ΔIdslin at Vgs/Vds=5.0V/0.1V) as illustrated in Fig. 2-4. In the saturation region the device parameters of interest are the minimum drain conductance in the saturation region (Δgd at Vds=5.0V), the saturation drain current (ΔIdssat at Vds/Vgs=Vdsat/5.0V), and the maximum saturation current (ΔIdsmax at Vds/Vgs= 5.0V/5.0V) as illustrated in Fig. 2-5. These device parameters have been chosen for lifetime projections of hot-carrier induced degradation which will be discussed in Chapter 4 in more detail.

2.3 Substrate Current Model

In nMOSFET's, the hot-carrier (or electron) induced substrate current is the hole current generated by impact ionization in the drain high-field region where electron-hole pairs are generated by the high energy channel electrons. This can cause long-term device degradation. Hence, the more severe the impact ionization, the higher the substrate current which is produced, and the more hot-carrier induced damage. The purpose of this session is then to investigate and establish a substrate current model which will correlate with hot-carrier induced device degradation and then develop lifetime projections in this study.

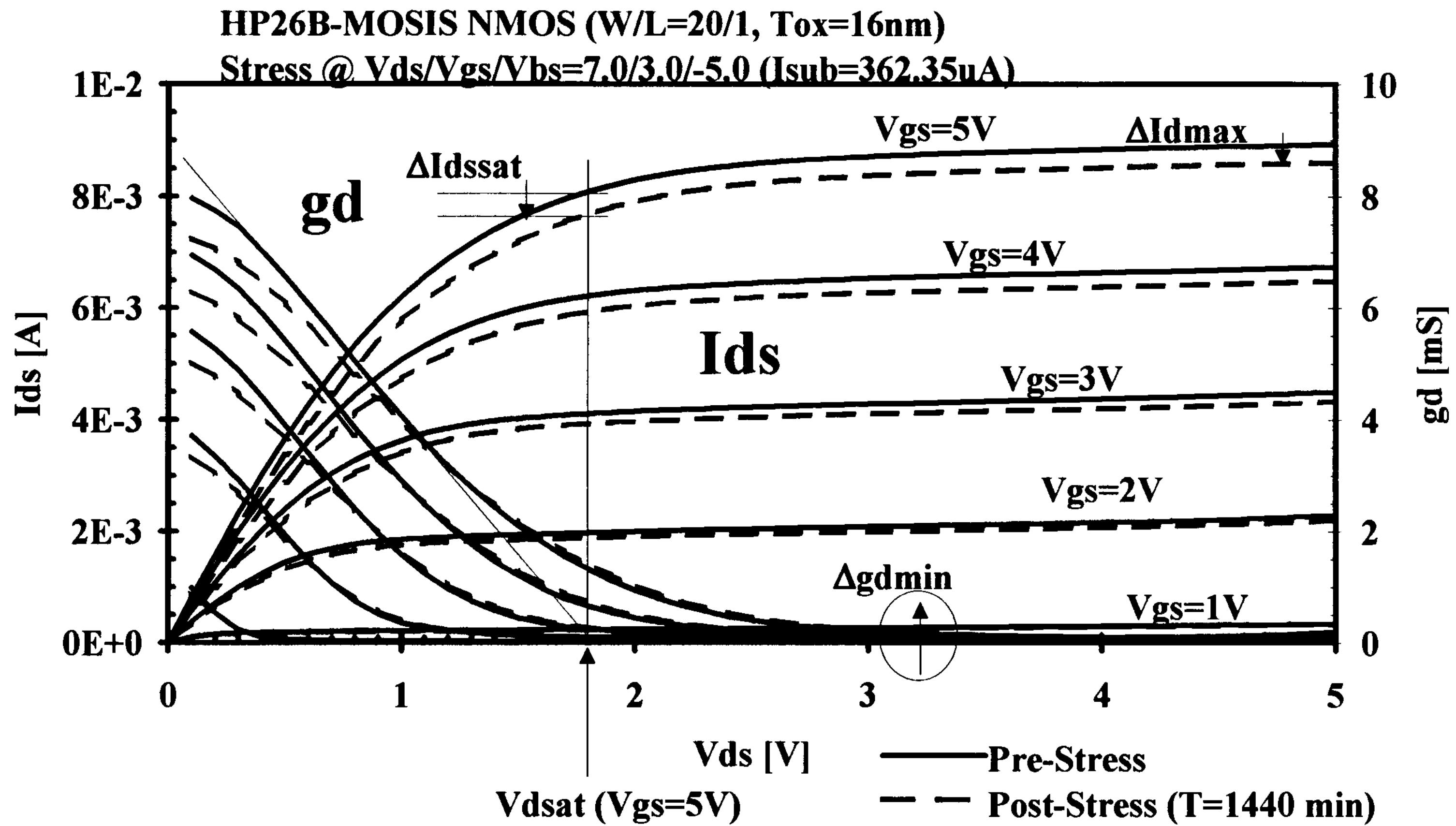


Figure 2-5 Ids-Vds characteristic curves of an nMOSFET device under hot-carrier injection.

There have been a number of substrate current models [69]-[77]. Since these models employ various types (at least a couple) of process dependent parameters (i.e., ionization constants and saturation region parameters), some of the substrate current models are too unnecessarily complicated to allow a fitting between measured and the simulated data. For the purpose of lifetime projections, then a simple and reasonably accurate substrate current model is more suitable for correlations between hot-carrier induced device degradation and circuit simulations. Hence, in this work, the substrate current model has been selected based on the physical phenomena in association with a minimum number of empirical parameters.

A simple but efficient expression accepted for the substrate current (Isub) model which is a function of DC biases is given by [64];

$$Isub = \frac{Ids \cdot Ai \cdot Em \cdot l_d}{Bi} \cdot \exp(-\frac{Bi}{Em}) \qquad (2\text{-}1),$$

where Ids is the drain-to-source current, Em is the maximum channel electric field, l_d is an effective ionization length [cm], and Ai and Bi are the pre- and post- exponential ionization coefficients, respectively. There have been quite numbers of studies of these ionization coefficients as shown below;

MOS	Ai [10^6/cm]	Bi [10^6V/cm]	Ref.
N	2.45	1.92	[69]
N	2	1.7	[71]
N	9	1.3	[74]
N	2	1.76	[77]
P	2.25	3.26	[59]
P	8	3.7	[71]

The large variations in the ionization coefficients indicate that these coefficients are the most process and geometrical dependent constants. Hence these coefficients should be determined in order to construct the Isub model.

Also, l_d and Em in Eq. (2-1) can be physically modeled as;

$$l_d = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} \cdot Tox \cdot Xj} \qquad (2\text{-}2),$$

where ε_{si} and ε_{ox} are the dielectric permitivities of SiO_2 and Si ,respectively, Tox is the gate oxide thickness, and Xj is the junction depth. And,

$$Em = \frac{Vds - Vdsat}{l_d} \qquad (2\text{-}3),$$

where Vds is the drain voltage and Vdsat is the saturation drain voltage. Although Ai and Bi are the major empirical parameters which are process dependent constants, Vdsat must be precisely defined to obtain Ai and Bi. As shown in Fig. 2-6, Vdsat has been determined by using the method developed by Jang et al. [78]. In this method the peak position of the function G [64] as defined in Fig. 2-6 corresponds to Vdsat. This Vdsat can be modeled as,

$$Vdsat = Leff \cdot Esat \cdot [\sqrt{1 + \frac{2 \cdot (Vgs - Vth)}{\alpha \cdot Leff \cdot Esat}} - 1] \qquad (2\text{-}4),$$

where Leff is the effective channel length, Esat is the channel field at which the carriers reach velocity saturation, Vth is the threshold voltage, and α is the body factor in the saturation region (i.e., Vdsat=Vgs-α·Vth(Vds)). The experimental methods used to obtain α and Esat are shown in Fig. 2-6. Since Vdsat is a circuit parameter which is important during device operation, once Vdsat is known, then a Isub model which is suitable for lifetime projections in circuit simulations can be easily determined from Eq. (2-1) by using the following empirical expression of the Isub model;

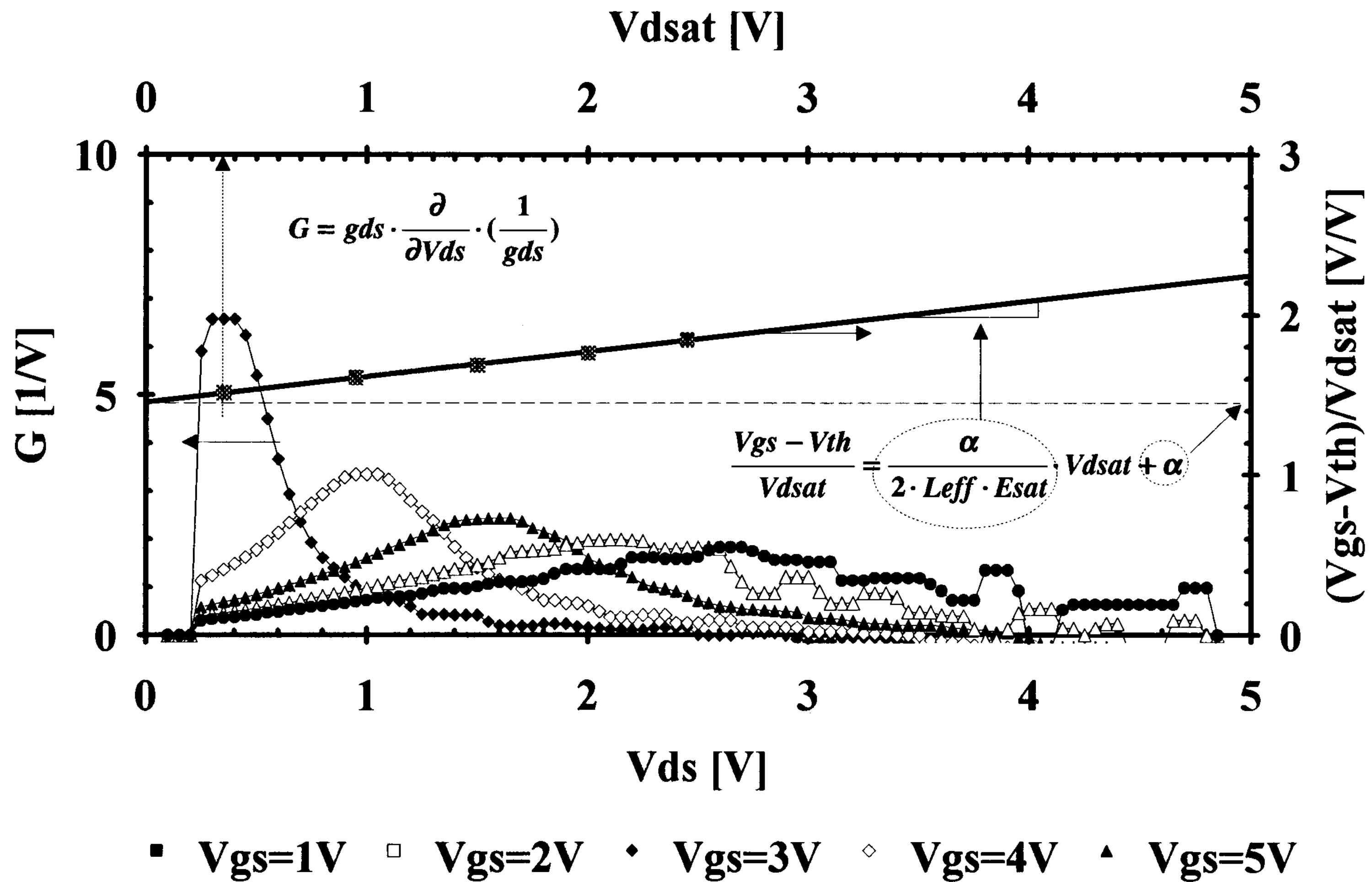


Figure 2-6 Saturation drain voltage (Vdsat) measurements.

$$Isub = C_1 \cdot Ids \cdot (Vds - Vdsat) \cdot \exp\left(-\frac{C_2}{Vds - Vdsat}\right) \qquad (2\text{-}5),$$

where C_1=Ai/Bi and C_2=Bi$\cdot l_d$. Table 2-2 shows a summary of measured values of C_1 and C_2 on various channel length devices and with different bulk-biases. Although, the Vdsat model parameters (α and Esat in Eq. (2-4)) are included in Table 2-2, Vdsat is pre-determined by the given operating conditions prior to Ids simulations during device simulations. Hence, C_1 and C_2 are the main parameters used to simulate substrate currents. It should be pointed out that Table 2-2 has been obtained for two different processes which will be described in chapter 4. By using the Vdsat and Isub model parameters, the simulation results of the Isub model have been obtained as shown in Fig. 2-7. The measured data is in marks and the simulation results are in lines. The simulated substrate currents match well the measured data over a wide range of drain and gate voltages. This is the substrate current model will be used in this study to calculate degradation and provide lifetime projections from circuit simulations due to hot-carrier injection.

2.4 Summary

Hot carrier injection mechanisms have been reviewed. Hot-carrier induced device degradation has been caused by the increase of trap charge and surface states induced by hot-carrier injection during device operation. Substrate current due to hot-carrier injection has been shown to be the best lifetime monitor of hot-carrier induced degradation in submicron devices. For lifetime projections in circuit simulations, an Isub model has been obtained by employing two empirical model parameters. Although the Isub model presented in this study has been limited to nMOS devices, it can be also

Table 2-2 Summary on substrate current model parameters of nMOSFET's.

W [μm] =50	(HP34- CMOS)		Tox [nm] =20		
Leff [μm] =0.7					
Vsb [V]	Vth [V]	α	Esat [V/cm]	C_1 [1/V]	C_2 [V]
0	0.468802	1.553007	142544.40	0.690978	25.50692
1	0.783112	1.378801	113798.70	1.027110	28.20998
2	0.950668	1.318937	90196.66	1.113107	29.16711
3	1.037171	1.295385	79933.51	1.156754	29.69413
4	1.068467	1.221862	57316.74	1.470327	30.27213
5	1.091894	1.155907	42076.29	1.167915	29.59434
Leff [μm] =0.9					
Vsb [V]	Vth [V]	α	Esat [V/cm]	C_1 [1/V]	C_2 [V]
0	0.4959	1.394703	69389.16	0.712541	25.51048
1	0.8261	1.263337	61448.16	0.921148	27.89681
2	1.0196	1.203302	51603.53	1.036313	29.14562
3	1.1359	1.123705	40760.93	1.037790	29.48735
4	1.1875	1.037262	31731.72	1.152489	32.97653
5	1.2131	1.014073	21951.20	1.708095	31.79782
Leff [μm] =1.7					
Vsb [V]	Vth [V]	α	Esat [V/cm]	C_1 [1/V]	C_2 [V]
0	0.6327	1.273663	107798.00	0.817625	25.96492
1	0.9914	1.166476	89522.28	1.546527	30.29492
2	1.2181	1.085157	74530.30	2.343795	32.94198
3	1.3839	0.985214	60856.79	3.495428	34.94418
4	1.5023	0.957824	44999.50	4.243279	36.53851
5	1.5803	0.890766	23862.96	4.733346	37.34192

W [μm] =20	(HP26B- CMOS)		Tox [nm] =16		
Leff [μm] =0.44					
Vsb [V]	Vth [V]	α	Esat [V/cm]	C_1 [1/V]	C_2 [V]
0	0.627759	1.580099	30239.15	0.736713	24.21416
1	0.794410	1.468854	27075.46	1.004180	25.52987
2	0.864985	1.405008	24882.74	1.103829	25.98674
3	0.894910	1.334591	19186.11	1.124120	26.17007
4	0.907839	1.273453	16781.63	1.124002	26.14533
5	0.918526	1.207371	13561.92	1.106147	26.12332
Leff [μm] =0.64					
Vsb [V]	Vth [V]	α	Esat [V/cm]	C_1 [1/V]	C_2 [V]
0	0.682390	1.391658	35643.20	1.088489	26.00688
1	0.964753	1.334323	33918.83	1.558872	28.22865
2	1.122386	1.293616	29633.66	1.802634	29.34054
3	1.218545	1.263101	27978.82	2.026591	30.11887
4	1.261872	1.241450	25137.18	2.113124	30.45892
5	1.276403	1.225144	23256.70	1.998561	30.26946
Leff [μm] =0.84					
Vsb [V]	Vth [V]	α	Esat [V/cm]	C_1 [1/V]	C_2 [V]
0	0.693172	1.288127	38504.26	0.982391	25.72086
1	1.009039	1.229441	34600.92	1.398005	28.18276
2	1.209604	1.203092	32548.94	1.544260	29.33704
3	1.350822	1.161338	31108.99	2.315544	31.53143
4	1.449231	1.142610	30025.51	2.837087	32.80015
5	1.487988	1.091908	25024.04	2.879591	32.92197

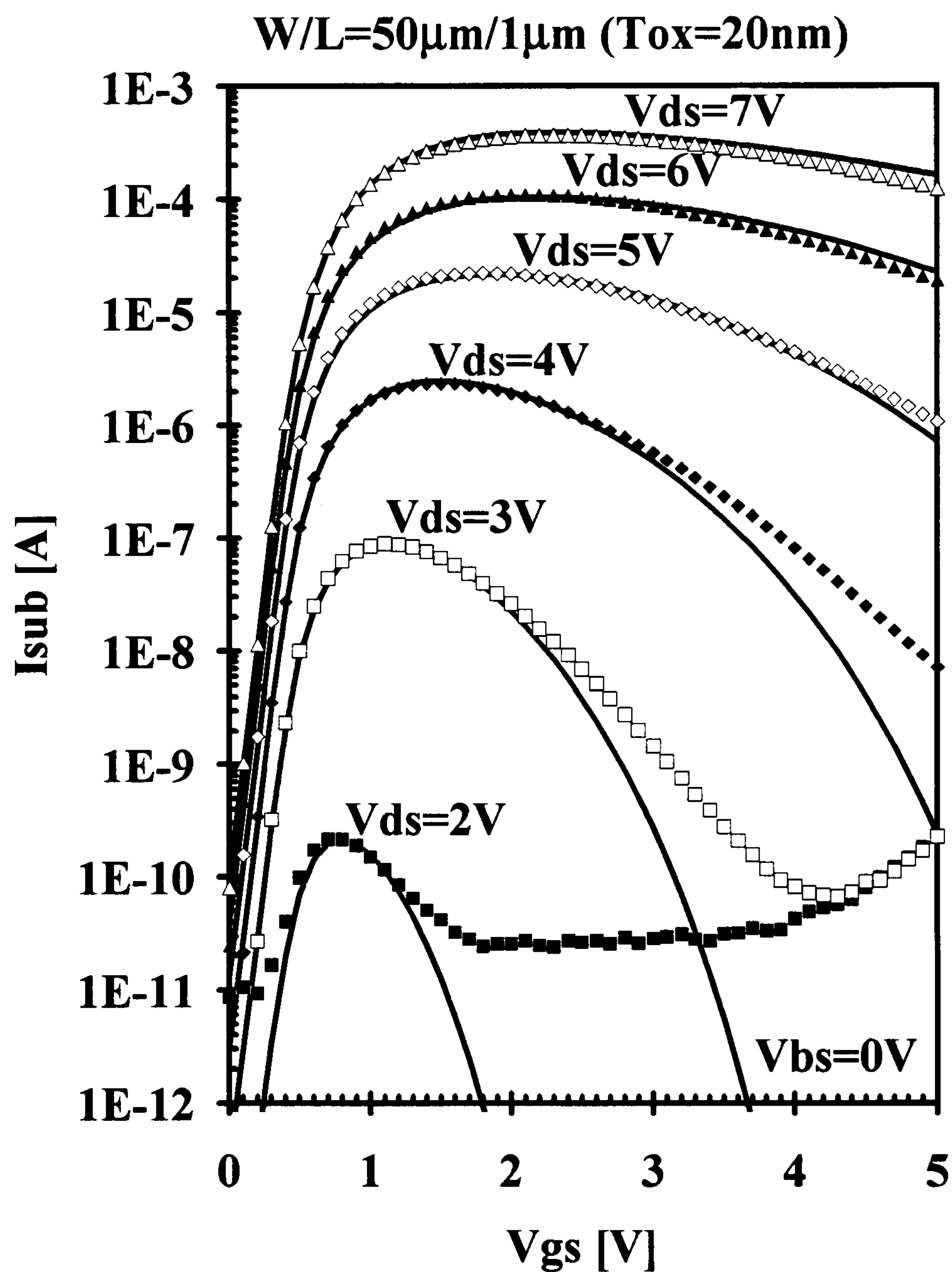


Figure 2-7 Measured (marks) and simulated (lines) substrate currents.

easily adopted for pMOS devices [70]. Using such parameters, this Isub model can then be used to calculate the degree of hot-carrier induced device degradation of MOSFET's under operating conditions.

3. PHYSICAL MECHANISMS OF TRAPS AND SURFACE STATES

3.1 Introduction

As the dimensions of devices become smaller, hot-carrier induced device degradation has become a major concern in the long-term reliability of sub-micron CMOS technology and applications. Hot electron trapping in gate oxides and surface (or interface) states due to hot-carrier injection cause a threshold voltage shift [79] and reduction of drain to source current, and consequently an increase in the switching time in VLSI/ULSI circuits [80]. Recently, the electric field stimulated emission (EFSE) method [81] was introduced to characterize the shallow level traps (0.9eV) at low temperature (77°K~200°K). In this chapter, a simple model of injection and thermal re-emission is shown to be adequate for predicting the hot-carrier injection induced degradation on sub-micron nMOSFET technology.

The ability to analyze charge trapping and surface states in semiconductor devices is critical to the accurate simulation of devices such as deep sub-micron devices. As the quality of gate oxide increases, the generation of interface states has been another main cause of MOSFET degradation in devices [82]-[89]. The interface states are electronic states in the forbidden gap of the semiconductor energy bands on the boundary between the gate oxide and the semiconductor. The origin of the interface states may be stretched Si-O bond, stretched Si-Si bond, oxygen vacancy, or silicon dangling bond [90]. Hot-carrier effects become severe as internal electric field increases. The increased possibilities of Si-SiO2 interfacial damage lead to create interface trap charge (electrons and/or holes). These trap charge strongly effect the electrical performance of devices by trapping carriers and reducing the mobility. As an

example, the subthreshold region (subthreshold swing; S=∂log(Ids)/∂Vgs) is greatly extended ($\Delta S>0$), since the interface trap states within the energy band must be filled with electrons before the channel can form.

The purpose of this chapter has been to determine the deep oxide trap level distribution (2.4eV) in our devices and the tunneling emission of the trapped electrons at room temperature by employing the EFSE method, and then investigate surface states by using a charge pumping method during hot-carrier stress.

3.2 Thermal Re-Emission

To obtain the energy spectrum of oxide traps the oxide electron traps were created at room temperature by applying a gate voltage of 2.5V and drain voltage of 7.0V at which maximum substrate current was obtained for long time periods (typically two or three days), and then, devices have been tested under various temperatures for recovery to show the thermal re-emission mechanism. The time constant (τ) of the thermal re-emission of electrons from oxide traps with zero gate voltage, [91]-[92], was determined as a function of temperature. From the Arrhenius plot of the recovery phase in Fig. 3-1, a 1.5eV activation energy of the trapped electrons in SiO_2 has been obtained. Also, Fig. 3-1 shows that the time constant of recovery (re-emission of oxide trapped electrons) at room temperature is around 10^5 minutes, while it is around 600 minutes at 70°C.

The mechanism for the self-limiting or saturation [93] in drain current degradation appears to be the thermal re-emission of the trapped electrons in the gate oxide. In fact, self-heating during AC stress causes a detrapping of electrons that leads to the self-limiting or saturation in the drain current.

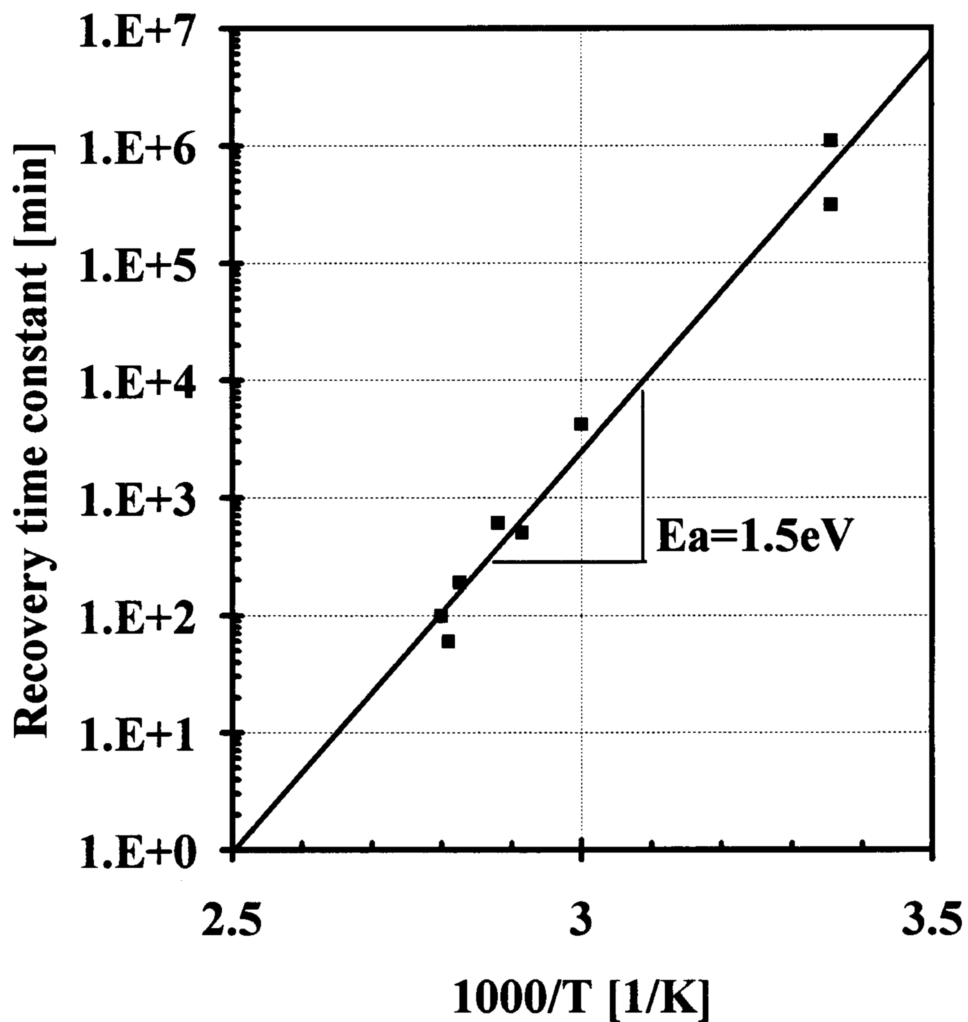


Figure 3-1 The Arrhenius plot of the drain-to-source current recovery mechanism; thermal emission of trapped electrons.

3.3 Tunneling Emission

Figure 3-2 (a) and (b) show the energy band diagrams in order to visualize the internal mechanism of the thermal recovery of trapped electrons under different bias conditions. We have been able to determine that the trap level (thermal activation energy) is 1.5eV below the conduction band in the oxide and its photoionization energy is greater than 2eV by optical stimulation by using a laser light source (HeNe) as shown in Fig. 3-2 (a). It is clear that the trapped electron first makes a transition to the excited state and then tunnels out to the semiconductor. This tunneling mechanism involves some lattice relaxation (Jahn-Teller Effect [94]-[95]). The dynamic Jahn-Teller effects is thought to be the origin of the differences in the thermal activation energy and the photoionization and photoemission energy of an electron bound to a trap. It has also been observed that the devices do not recover with positive gate voltage as shown in Fig. 3-2 (b). Therefore, the recovery and self-limiting mechanism can only be observed under AC stress conditions (Fig. 3-2 (c)) but never under DC stress conditions.

3.4 Electric Field Stimulated Emission

The density of oxide trap (Not(t)) after a time t at an oxide field Eox is known as [81];

$$Not(t) = \int_{Ev}^{Ec} (1 - e^{-\omega \cdot t}) \cdot Dot(Et)\, \partial Et \qquad (3\text{-}1),$$

where Ec and Ev are the conduction and valence energy, respectively. Using the Price-Sah tunneling emission model [81], [91]-[92], the tunneling rate, ω, out of a group of traps located below the conduction band in the oxide is given as

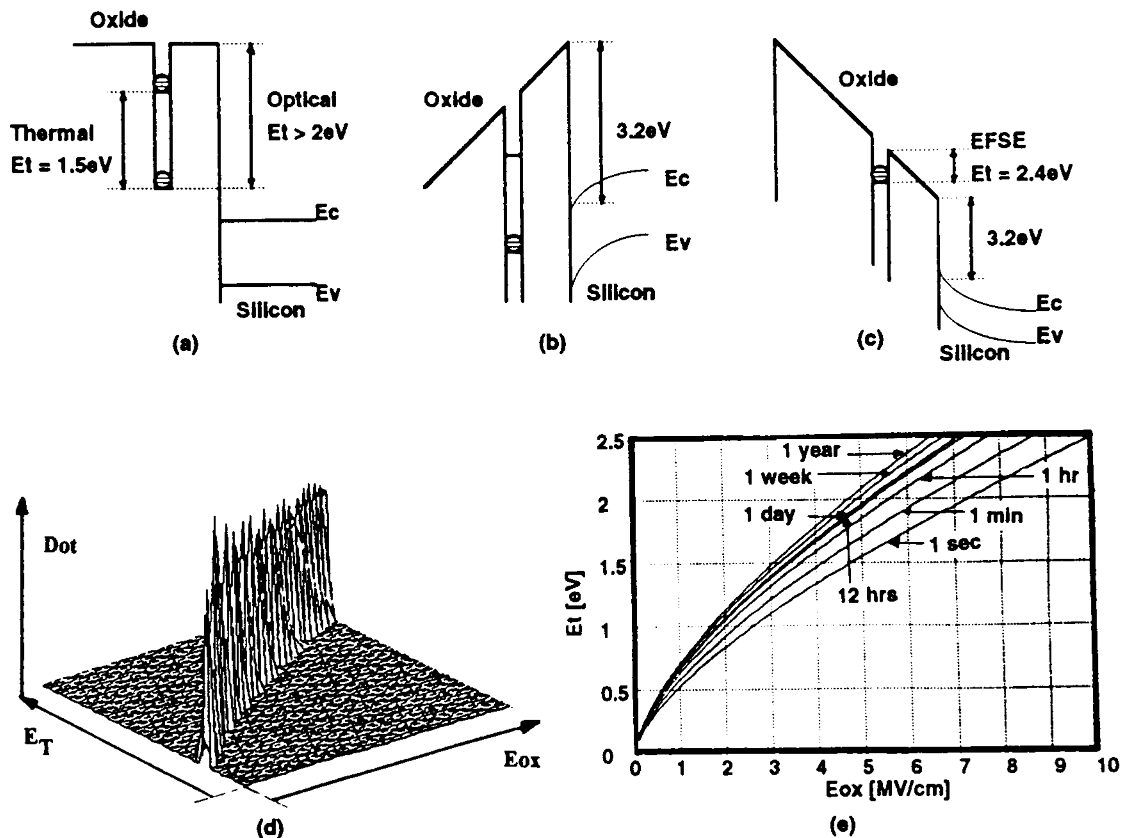


Figure 3-2 Tunneling model for re-emission of trapped electrons at different gate bias conditions: (a) thermal recovery with zero or negative gate voltages, (b) the trapped electrons will not recover with positive gate voltages, (c) tunneling (EFSE) from ground state at large negative gate voltages at room temperature, (d) trap energy distribution from Price-Sah emission equations (not to scale), and (e) the projection of oxide trap density as a function of applied oxide electric field and trap energy level.

$$w = \frac{8 \cdot \pi^5}{h^3} \cdot q \cdot m^* \cdot \frac{Eox}{Et} \cdot W^2 \cdot \exp(-2 \cdot \theta) \qquad (3\text{-}2),$$

where
$$\theta = \frac{4 \cdot \pi}{3} \cdot \sqrt{2 \cdot m^*} \cdot \frac{Et^{1.5}}{q \cdot h \cdot Eox} \qquad (3\text{-}3),$$

Eox is the maximum electric field in the gate oxide, Et is the energy level of the oxide electron trap measured from the oxide conduction band, W^2 is the matrix element of the trap potential energy [91], and m* is the effective mass of carriers in the oxide [81], [96].

$$w = 7.93 \times 10^{10} \cdot \frac{Eox}{Et} \cdot \exp(-68.31 \cdot \frac{Et^{1.5}}{Eox}) \qquad (3\text{-}4).$$

The density of oxide electron traps at energy, Dot(Et), is then

$$Dot(Et) = \frac{Cox}{q} \cdot \frac{\Delta Vot}{\Delta Et} \qquad (3\text{-}5),$$

and the density of state (Dot) of oxide electron traps at energy, Eti, is then determined experimentally;

$$Dot(Et_i) = \frac{Cox}{q} \cdot \frac{\Delta Vg_{i-1} - \Delta Vg_i}{Et_i - Et_{i-1}} \qquad (3\text{-}6),$$

where Cox is the gate oxide capacitance per unit area [F/cm^2], Vot is the voltage shift due to the oxide traps, and Et_i at each applied electric field (Eox=Vg/Tox) is calculated from Eq. (3-4) at $\omega t \approx 1$ [81].

Fig. 3-2 (d) shows the trap energy distribution of trapped electrons in the oxide indicating the tunneling rate is a strong function of applied oxide electric field. The relationship between applied oxide electric field and monitored time are shown in Fig. 3-2 (e). It should be pointed out that the limitations of the maximum trap energy spectrum obtained by field-induced re-emission consists of not only the applied electric field but also the monitoring time.

The EFSE method consists of the following steps;

(1) Hot-carrier stress: the oxide electron traps in the n-channel device are first created at room temperature.

(2) Field induced re-emission: a negative gate voltage is increased in uniform steps and maintained constant for preset period at each step.

(3) Measurement: at the end of each step, the thresh-old voltage and gate voltage at constant drain current are monitored.

Fig. 3-3 shows the threshold voltage shifts versus detrapping oxide electric field upon increasing the negative gate voltage in 0.2V steps. As the oxide electric field steps up, the threshold voltage recovers gradually. It is clear that the large numbers of electrons are detrapped at an oxide field of approximately 5.8 MV/cm. Fig. 3-4 shows the energy spectrum for the oxide traps or the density of states of electron traps versus energy that is given by Eq. (3-4). The maximum oxide electron trap density appears at an energy of 2.4eV. However, this trap depth from tunneling is larger than the thermal activation energy of 1.5eV, and the difference is due to the lattice relaxation during thermal activation.

3.5 Charge Pumping Current Measurements

Figure 3-5 shows a basic charge pumping measurement set-up. When the transistor is pulled into inversion, the surface becomes deeply depleted and electrons will flow from both the source and drain regions into the channel, where some of electrons will be captured by the interface states. As the gate pulse drives the surface

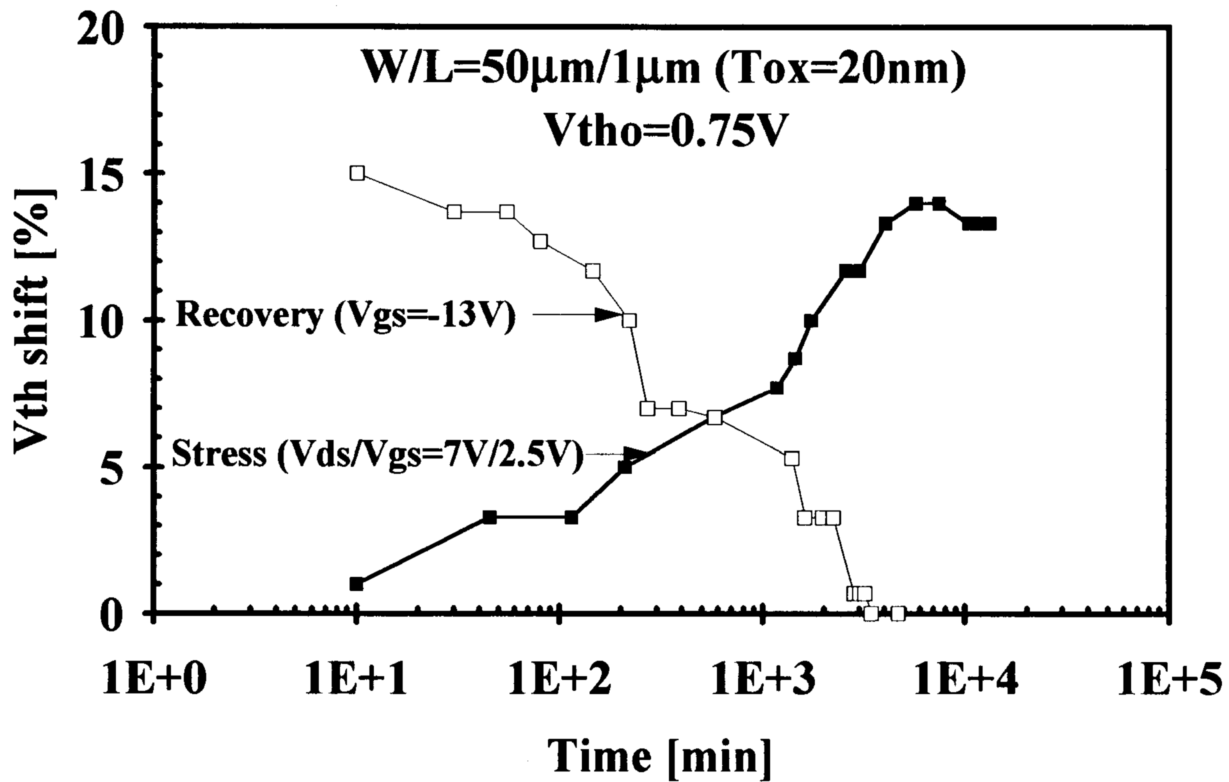


Figure 3-3 Recovery of the threshold volatge under negative gate voltage.

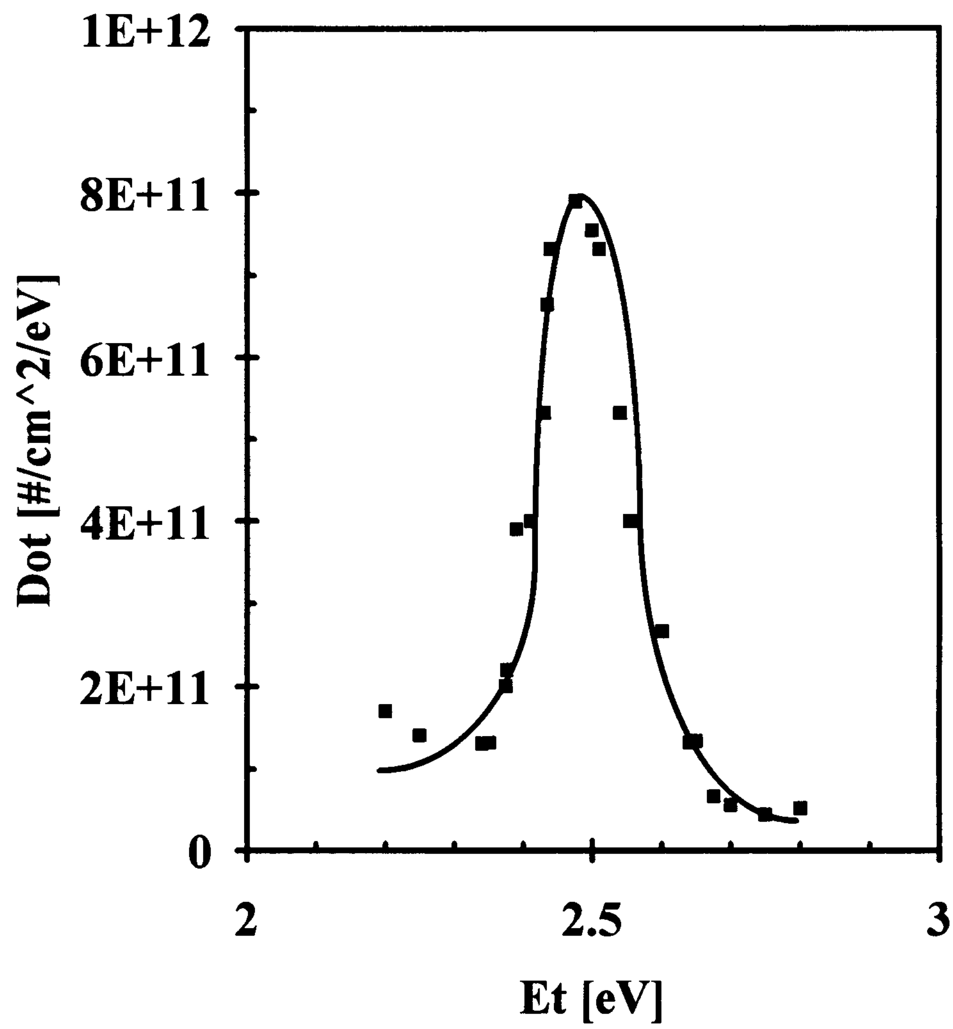


Figure 3-4 The density of charged oxide electron traps versus trap energy.

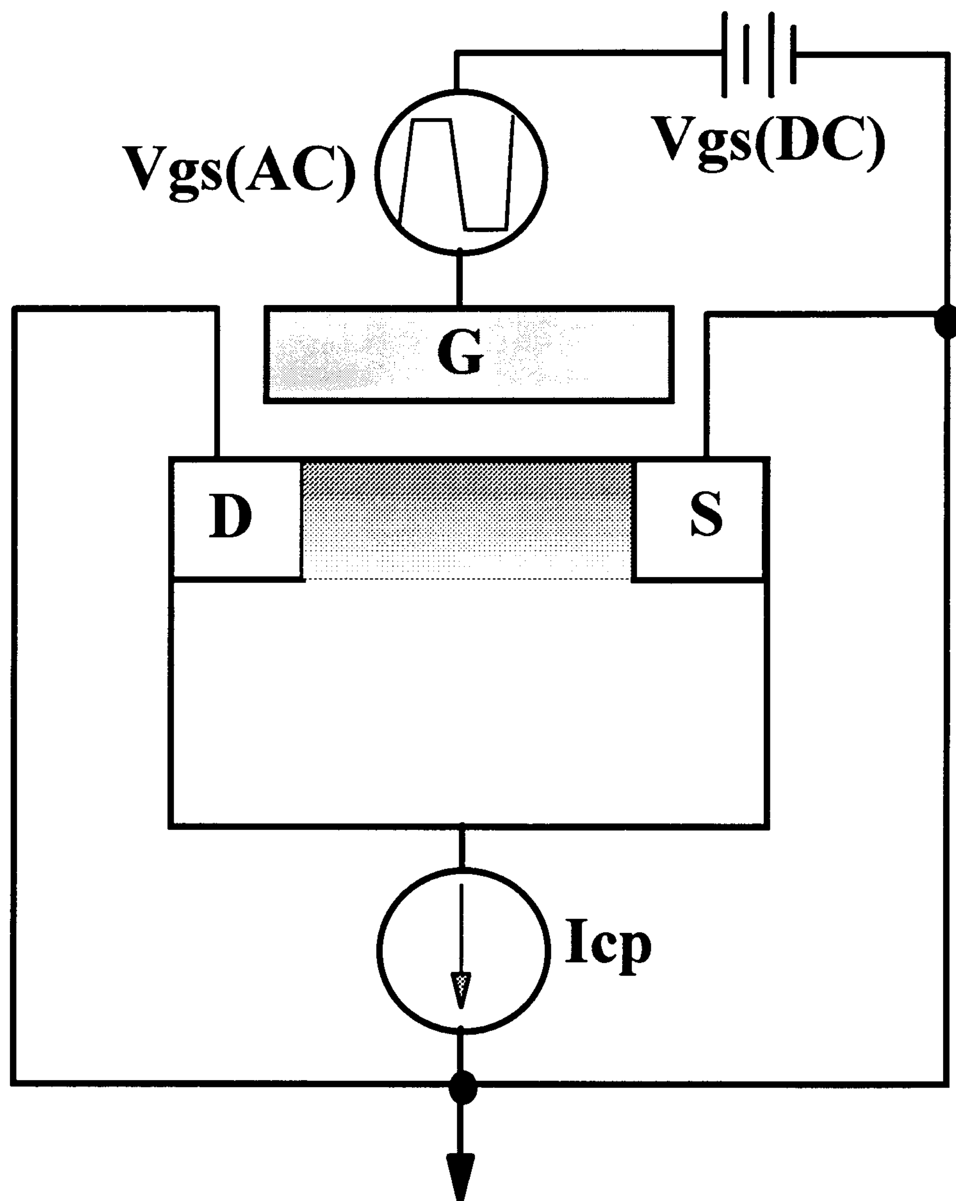


Figure 3-5 Schematic diagram of charge-pumping current measurement set-up.

back into accumulation, the mobile charge drifts back to the source and drain under the influence of the reverse bias, but the charges trapped in the interface states will recombine with the majority carriers from the substrate and give rise to a net flow of negative charge into the substrate. The negative charge (Qss) is given by [89]

$$Qss = A \cdot q \int Dit(E)\, \partial E \qquad (3\text{-}7\ (a)),$$

or

$$Qss = A \cdot q^2 \cdot Dit \cdot \Delta\psi_S \qquad (3\text{-}7\ (b)),$$

where A is the gate area of the transistor [cm^2], q is the electron charge (1.6×10^{-19} C), Dit(E) is the interface state density at the energy, E, [#/cm^2/eV], and $\Delta\psi s$ is the total sweep of the surface potential [V]. The interface states can be described by Dit which is the average interface state density over the range of energy levels swept [#/cm^2].When applying repetitive pulses to the gate with frequency (f), this charge (Qss) will give rise to a current in the substrate given by,

$$Icp = f \cdot Qss = f \cdot A \cdot q^2 \cdot Dit \cdot \Delta\psi_S \qquad (3\text{-}8),$$

where Icp is the charge pumping current. Since Dit is an approximation over the energy range in the bandgap swept by the charge pumping waveform, then,

$$Nit = q \cdot Dit \cdot \Delta\psi_S \qquad (3\text{-}9),$$

where $q \cdot \Delta\psi_S = Eg_{(Si)}$. Thus, the interface state shift (ΔNit) is described by;

$$\Delta Icp = q \cdot f \cdot A \cdot \Delta Nit \qquad (3\text{-}10).$$

This simple experimental derivation is quite suitable for the studies of the hot-carrier induced degradation since interface state generation becomes a dominant degradation mechanism due to hot-carrier injection as the gate engineering becomes more sophisticated. Moreover, charge pumping current information on the interface state distribution is important since the interface states consist of both donor-like states (below mid-gap) and acceptor-like states (above mid-gap). In order to determine the distribution of the interface states, the rise time (t_r) and the fall time (t_f) of the pulses has to be changed. The interface states at energy level E, Dit(E) are given by [89]

$$Dit(E) = -\frac{t_f}{q \cdot A \cdot k \cdot T} \cdot \frac{\Delta Icp}{\Delta t_f} \tag{3-11}$$

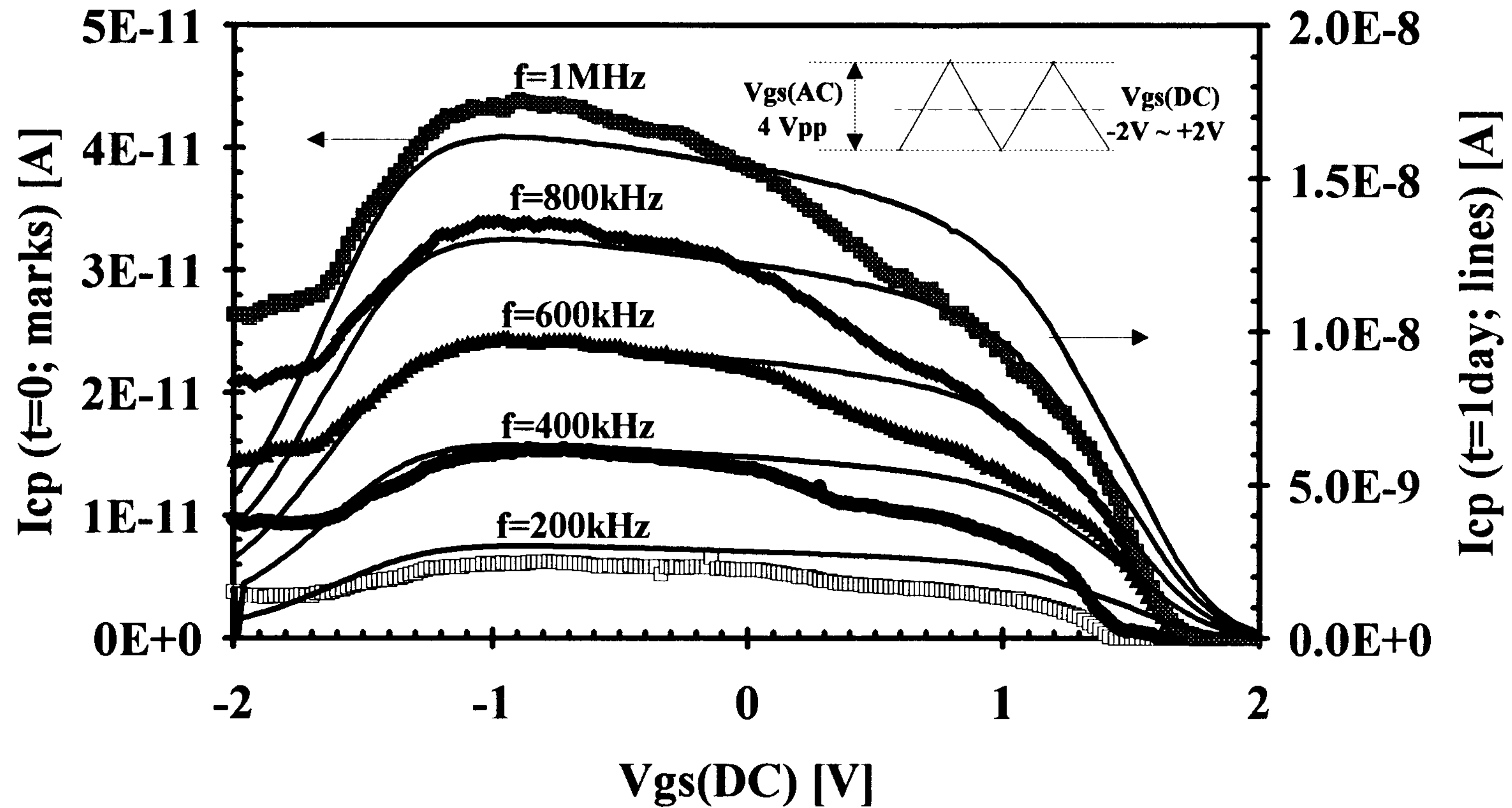
for a constant rise time with varying falling time, and

$$Dit(E) = -\frac{t_r}{q \cdot A \cdot k \cdot T} \cdot \frac{\Delta Icp}{\Delta t_r} \tag{3-12}$$

for a constant fall time with varying rising time, where k is the Boltzmann constant (1.38×10^{-23} [J/K]) and T is the ambient temperature [K]. By changing t_f and t_r, the distribution of the interface states can be obtained. The charge pumping current measurement has been adopted in the studies of interface state generation due to hot-carrier injection.

Figure 3-6 shows Icp measurements from an nMOSFET device with W=50μm and L=1μm by using a triangular gate voltage waveform with frequencies from 200kHz to 1MHz. It can be seen that the Icp increases as the frequency increases as expected in Eq. (3-10). After one-day hot-carrier stress, the maximum Icp's have increased approximately 400 times more than the fresh Icp(max)'s. Also, it should be noted that the positive shift of the gate voltage in Icp measurements is due to negative charge trapping in the gate oxide resulting in the positive shifts of flat band voltage and threshold voltage. However, the oxide trapping mechanism is not a main consideration in Icp measurements since the positive gate voltage shifts in Icp measurements are highly ambiguous (depending on the definition of the threshold voltage level) and difficult to monitor in the experimental data unless one is equipped with a precisely controlled voltage source and a high-accuracy current meter [84]. Thus, the Icp measurement in MOSFET's is one of the interface state evaluation methods rather than being used to determine trapped oxide charge.

Fig. 3-7 shows the increase of the maximum value of Icp measured at a frequency of 1MHz under hot-carrier stress with Vds=7V and Vgs=3V for one day.



W/L=50/1 (Leff=0.88μm), Tox=20nm Stress; Vds/Vgs=7V/3V (Isub=382μA)

Figure 3-6 Charge pumping current measurements as a function of gate voltages with different frequencies.

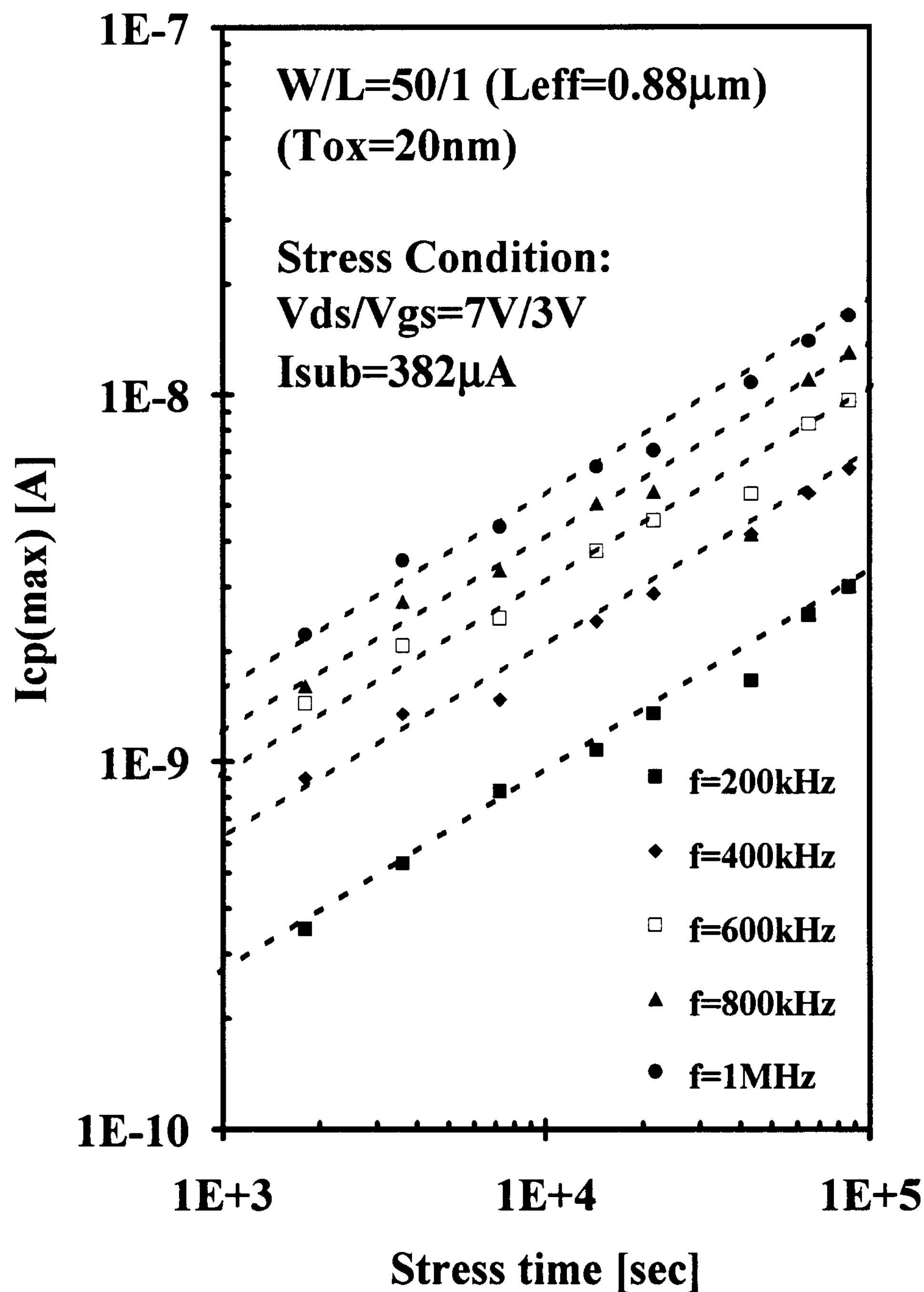


Figure 3-7 The increase of Icp(max) under hot-carrier stress.

The increase of Icp(max) indicates the increase of interface states during hot-carrier injection. Also, the linear increase of Icp(max) with increasing frequency shows that the interface traps are emitting carriers at a rate faster than the frequency of gate voltage waveform.

Also, Fig. 3-8 shows the validity of Eq. (3-10) which is simple and efficient to determine the interface states shifts due to hot-carrier injection, rather than the full-physical description of Icp such as [89];

$$Icp = 2 \cdot q \cdot Dit \cdot f \cdot A \cdot k \cdot T \cdot \ln[\upsilon_{th} \cdot n_i \cdot \sqrt{\sigma_n \cdot \sigma_p \cdot \alpha \cdot (1-\alpha)} \cdot \frac{|V_{FB} - V_T|}{|\Delta Vg|} \cdot \frac{1}{f}] \quad (3\text{-}13)$$

where υ_{th} is the thermal velocity of carriers, n_i is the surface concentration of minority carriers, V_{FB} is the flat band voltage, V_T is the threshold voltage, ΔVg is the amplitude of the gate voltage waveform, α is the duty cycle factor (i.e., α=0.5 for a triangular waveform), and σ_n and σ_p are the capture cross sections of electrons and holes, respectively. In Fig. 3-8, the calculations of Nit's from Eqs. (3-10) and (3-13) are shown as marks and a line, respectively. The calculated Nit from Eq. (3-10) at f=1MHz is comparable with the Nit calculated from Eq. (3-13). Hence, for measurement convenience, a triangular waveform at the frequency of 1MHz was used in the charge pumping current measurements in this study.

3.6 Summary

Thermal emission of electrons from deep traps in the gate oxides on LDD n-MOS devices (W/L=50μm/1μm and Tox=20nm) has been observed and characterized over long time periods at room temperature and above following hot-carrier stress. The tunneling and thermal re-emission processes and the distribution of oxide trapped

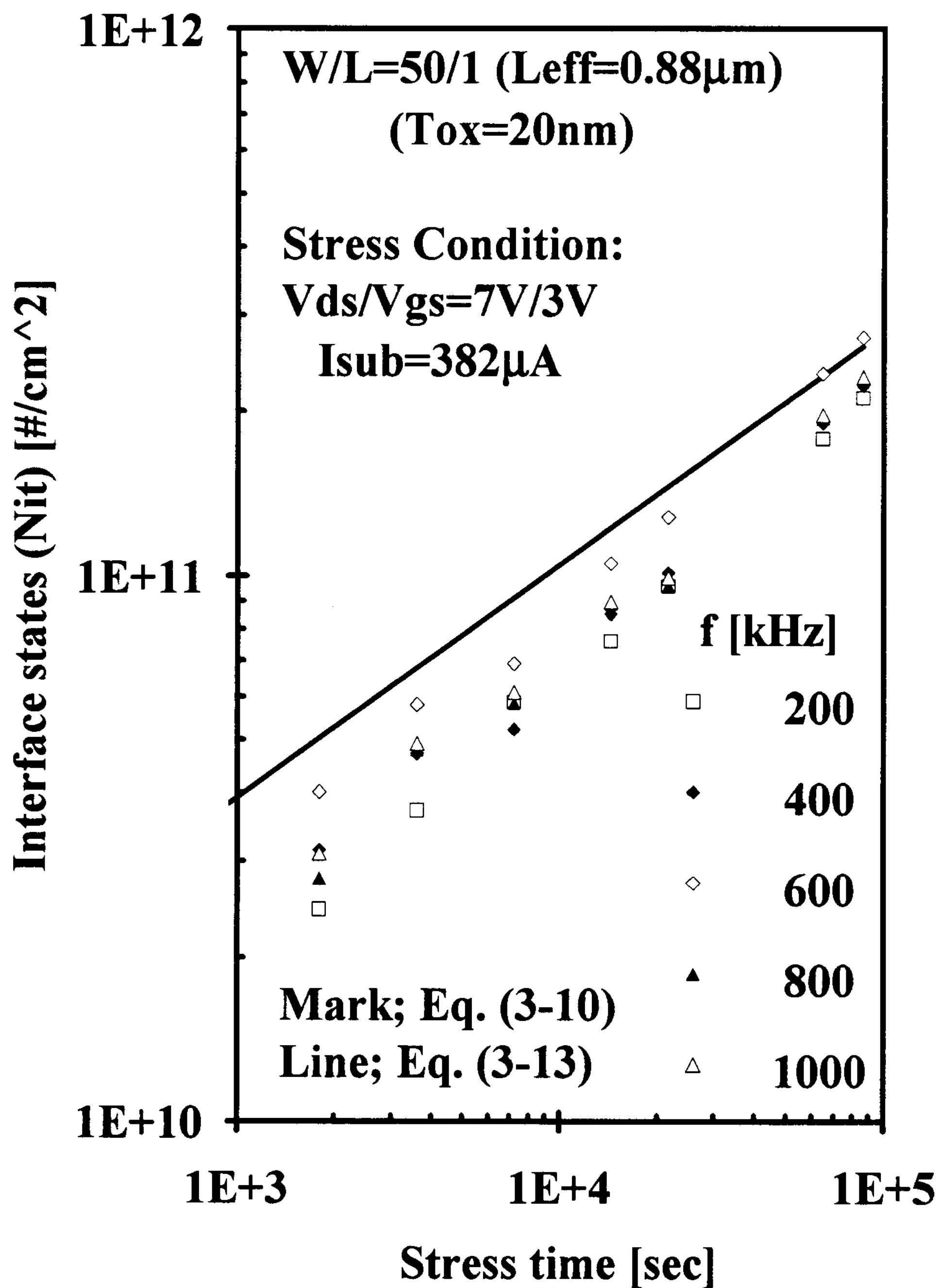


Figure 3-8 The increase of interface states with stress time.

electrons have been studied to develop a long-term reliability model for AC hot-carrier stress and use conditions which is different from DC stress results alone. The difference between the thermal activation energy (1.5eV) and the field induced tunneling energy (2.4eV) from deep traps is found to be due to a lattice relaxation of the trapped electrons.

In order to analyze surface state generation during hot-carrier injection, charge pumping current measurements were employed to determine the interface state density under hot-carrier stress. Some basic relationship in the increases of Icp and Nit will be observed later for lifetime projections and in device characterization. The Icp measurements have been shown here to be a simple and efficient to study the hot-carrier induced interface state generation.

4. LIFETIME PROJECTIONS

4.1 Introduction

Circuit reliability issues are becoming more of a problem due to the shrinking of device dimensions without a corresponding reduction in the power supply voltage. The hot-carriers generated in the MOSFET high field region will result in degradation of transistor characteristics and will eventually affect the circuit performance. One of the main concerns in the reliability of CMOS IC designs is device parameter mismatches [97]-[108] which reduce overall circuit performance such as a gain reduction of a CMOS amplifier [98] and a frequency shift in a ring oscillator [108]. However, given the increased IC complexity and difficulties in process control, and IC designs can no longer support relaxed design rules. Instead a more careful and thoughtful IC design has become mandatory from reliability considerations. For example, a composite nMOSFET for deep submicron IC designs has been introduced and is given in appendix A.

The design of CMOS IC's depends on the ability to accurately predict and simulate device and circuit performance under operating conditions [105]-[108]. However, the accuracy of this reliability simulation is very much dependent upon the extensive stress parameter files to update the degraded model parameters for each specific aging level (or degree of hot-carrier effects) of each device under operating conditions. In order to obtain accurate degraded model parameters, an aging evaluation is required in the pre-processor of a reliability simulation such as BERT (Berkeley Reliability Tools) [109]. During this pre-processing evaluation, each device under operating condition produces substrate current and/or gate current which will be

converted into an equivalent age of the device per operating cycle, then the total age is determined by integrating over the whole operating time. The total age is then used to obtain the proper degraded model parameters. Thus the device parameters as degraded by operating time are used in the circuit simulation.

The main schemes for reliability projections rely highly on the device age under each operating condition and the degraded model parameters. Hot-carrier induced device degradation has been studied extensively [108]-[110] and is still a topic in IC design-for-reliability due to the various operating conditions [111]. Ironically, the importance of the degraded model parameters has been underestimated since the reliability projections have been adopted from the process-oriented lifetime criteria [7], [29], [49], [112] which is quite different than those from IC design considerations. Also the model parameters are dependent upon the particular foundry process. Therefore, without enough information on or a physical understanding of hot-carrier effects on device parameters and operating conditions, the reliability simulations can be overly simplified and no longer be valid.

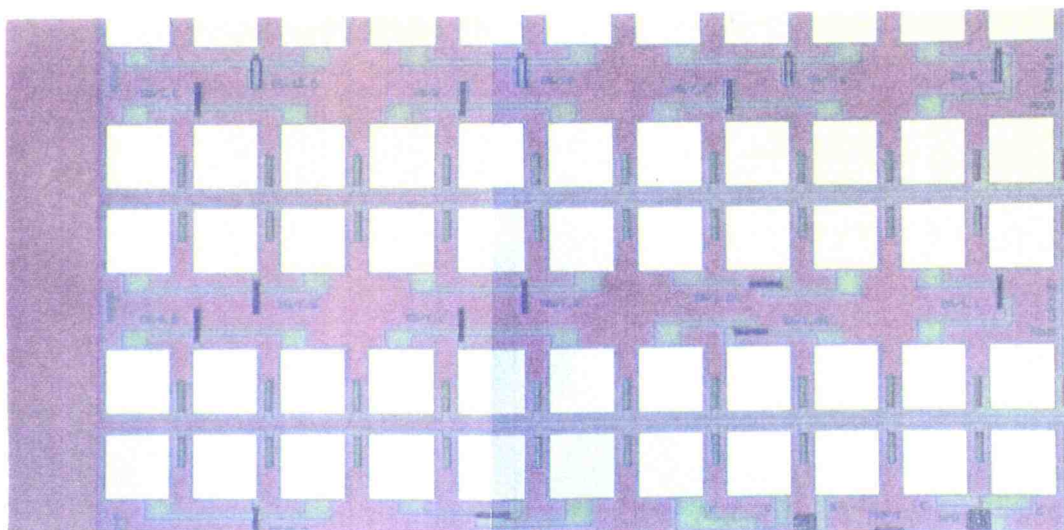
The purpose of this chapter is to analyze and project a general trend in the degradation of device parameters and SPICE MOS3 parameters through lifetime projections. Unlike the process induced device parameter mismatches which are commonly considered individually, the hot-carrier induced degradation of device parameters is considered to occur simultaneously. Since the main cause of device parameter shifts is hot carrier injection resulting in trapped charges and the surface states, the device parameters shifts under operating conditions are affected simultaneously. The physical and process oriented parameters of the SPICE MOS3 (i.e., W, L, Tox, NSUB, etc.) will remain constant under operating conditions. The SPICE MOS3 parameters such as VTO, GAMMA (γ), UO, THETA (θ), VMAX, and KAPPA (κ) [113] will be investigated under hot-carrier stress conditions in this

chapter. The main emphasis on these parameters is to propose a degradation model of these parameters for CMOS devices. This model of hot-carrier effects on these model parameters is then used for lifetime projections and reliability projections in circuit simulations. Design guidelines for a CMOS sense amplifier have also been demonstrated based on reliability projections.

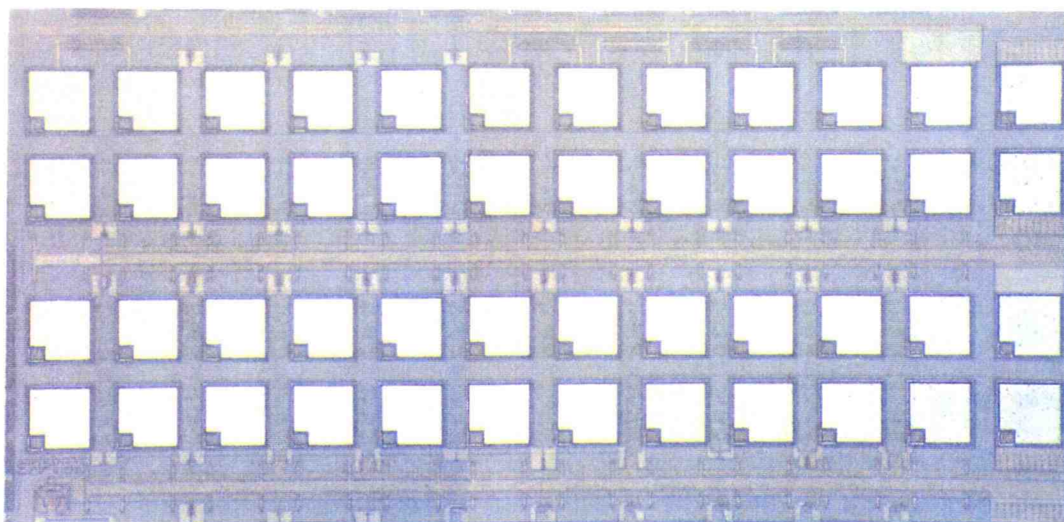
4.2 Accelerated Lifetime Test

The MOSFET's used in this experiment were fabricated by two different foundry processes: MOSIS-HP-CMOS34 (1.2-micron, N-Well) with W/L=50/1 (Tox=20nm) and MOSIS-HP-CMOS26B (0.8-micron, N-Well) with W/L=20/1 (Tox=16nm). Fig. 4-1 shows a photomicrograph of the test device patterns used in this experimental study. Fig. 4-1 (a) and (b) are taken from the MOSIS-HP-CMOS 34 and 26B, respectively. They have different gate interconnections in which the HP-CMOS26B has been prepared with the common gate structure shown over the entire row. The common gate interconnection increases the number of test devices. For instance, HP-CMOS26B (20 devices) has 3 times more devices than HP-CMOS34 (7 devices). However, the unavoidable gate potential in neighboring devices produces a larger gate leakage current and also induces some parasitic capacitance and resistance. Hence, some of reliability analysis (i.e., the charge pumping current measurement) could not be performed on the HP-CMOS26B.

In order to accelerate lifetime projections, drain avalanche hot-carrier injection (DAHI) at the maximum substrate current condition was used to monitor the maximum transconductance (gmx) shift at Vds=100mV, the saturation drain voltage current (Idsat) shift at Vds/Vgs=Vdsat/5V, and the drain conductance (gd) shift at



(a)



(b)

Figure 4-1 Photomicrograph of the test device patterns for (a) MOSIS-HP-CMOS34 and (b) MOSIS-HP-CMOS26B.

Vds/Vgs=5V/5V as well as the SPICE MOS3 parameters. The data was automatically taken by a PC-controlled automated measurement system employing a custom program which is developed for hot-carrier stress and SPICE MOS3 parameter extraction (HOTPEX shown in appendix B). During hot-carrier stress, the stress program is interrupted at each pre-determined time, and then all of the device physical parameters and SPICE model parameters were obtained.

Figure 4-2 shows threshold voltage shifts and gmx degradation under the DAHI accelerated lifetime test. In this typical example the lifetime as defined by ΔVth=10mV and Δgmx=10% are found in both cases to be around 700min. While ΔVth is caused mainly by the oxide trapped charge as shown in Fig. 2-5, the transconductance degradation involves both aspects of the hot-carrier induced device degradation. In the early stage of this reliability analysis where lifetime projections were carried out on long channel devices (L>2μm) with considerable oxide trapped charge, the lifetime projections were rather simpler than the contemporary approach which is composed of both surface states and oxide trapped charge in short channel devices (L<2μm). Also, as shown in Fig. 4-2, ΔVth is no longer linear with stress time. Hence lifetime projections based on ΔVth become less attractive in circuit simulations and Δgmx has become most commonly adopted in lifetime projections [112], [114]-[115]. Also, the good linearity of Δgmx with stress time is the prime factor in Δgmx being correlated with Isub.

Figure 4-3 shows drain current degradation (ΔIds) under hot-carrier stress where the lifetime definitions of ΔIds(lin)=10%, ΔIds(sat)=2.5% and ΔIds(max)=2.5% are found to be 1500min, 450min, and 2500min, respectively. In other words, the parameter mismatches corresponding to ΔIds(lin)=10% are ΔIds(sat)=4.5% and ΔIds(max)=2%, respectively. However, as shown in Fig. 4-4, Δgmx obtained under various stress conditions shows a good linear relationships with ΔIds under most of

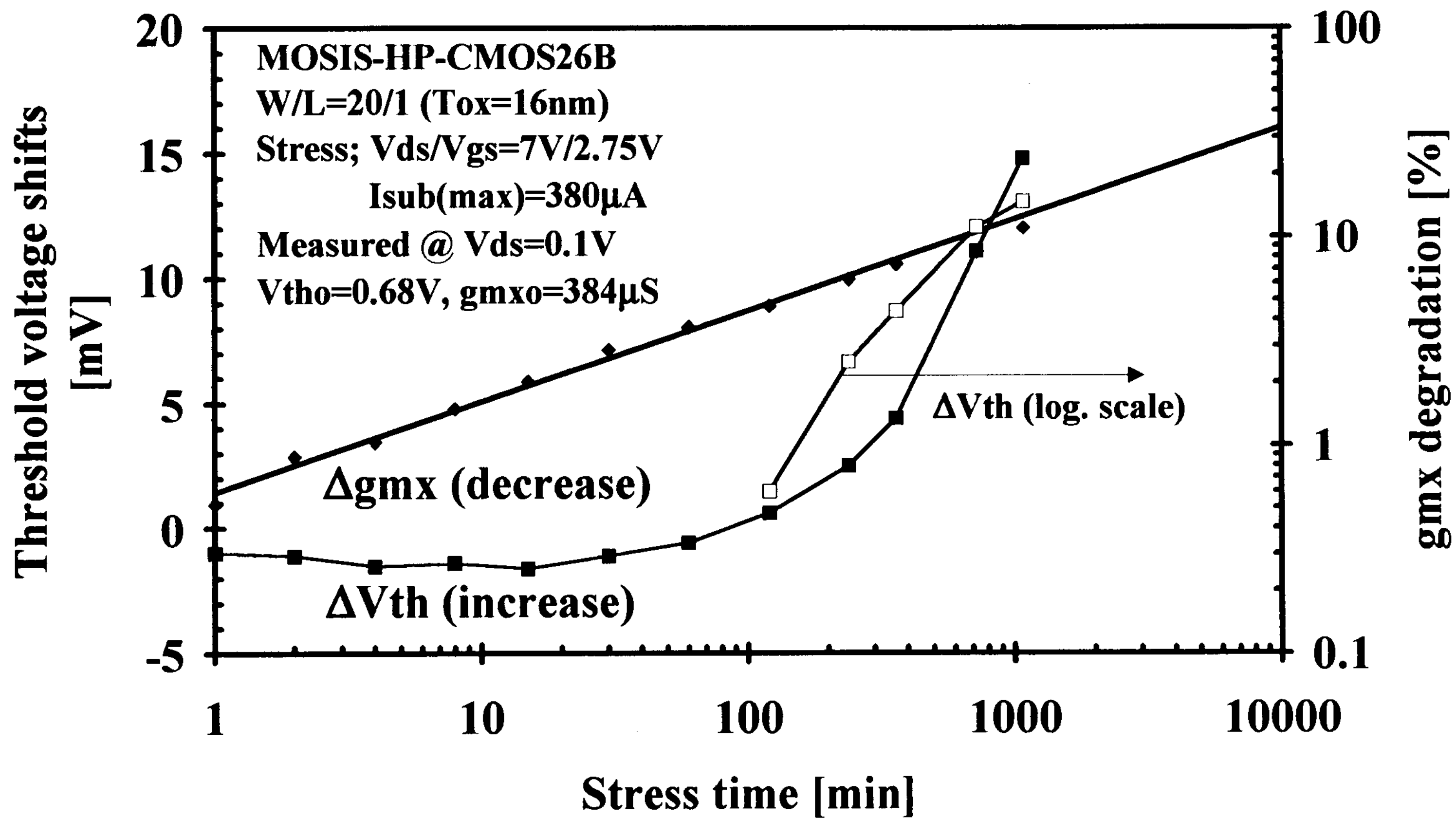


Figure 4-2 ΔVth and Δgmx under hot-carrier stress.

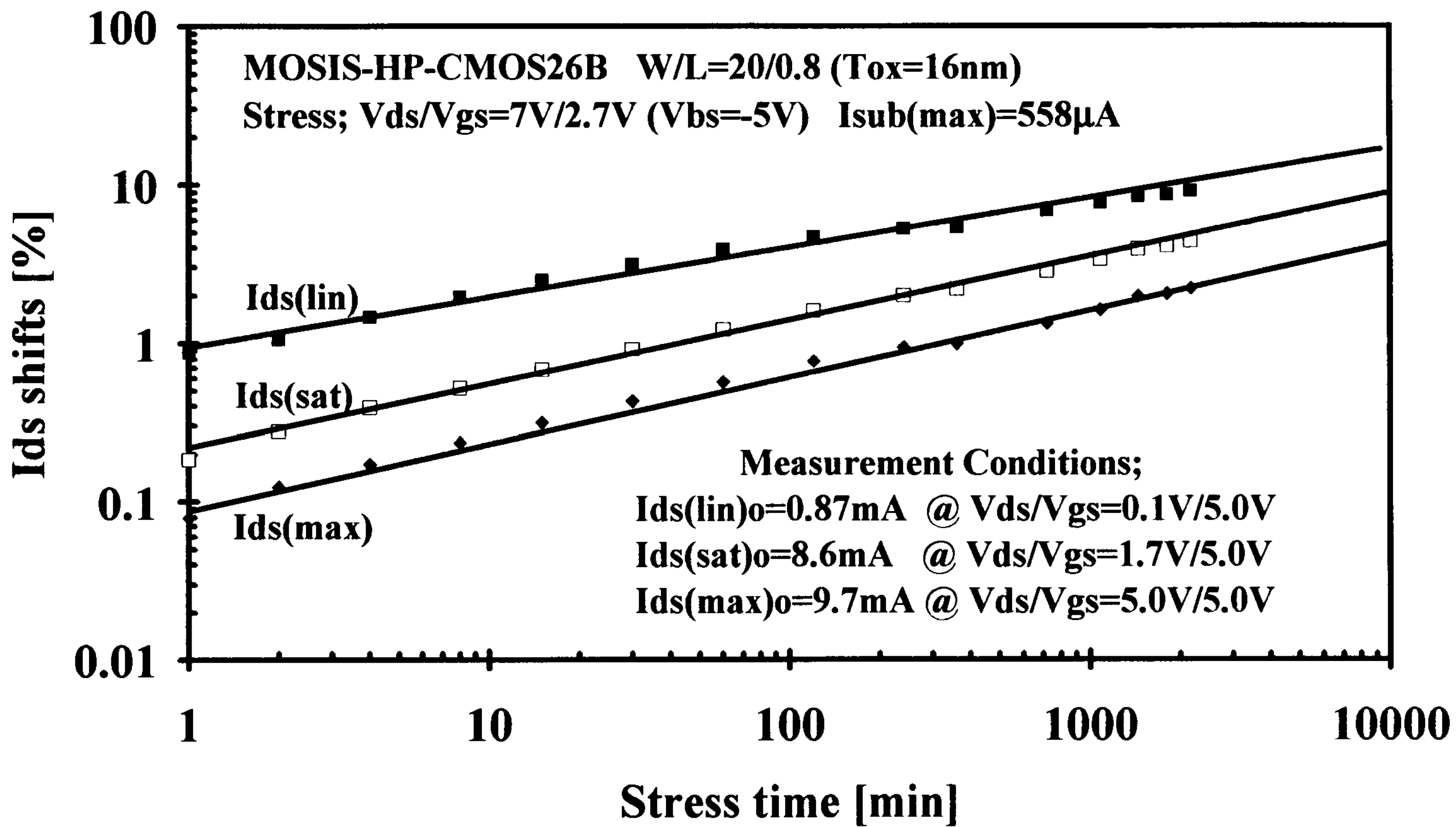


Figure 4-3 Ids degradation under hot-carrier stress.

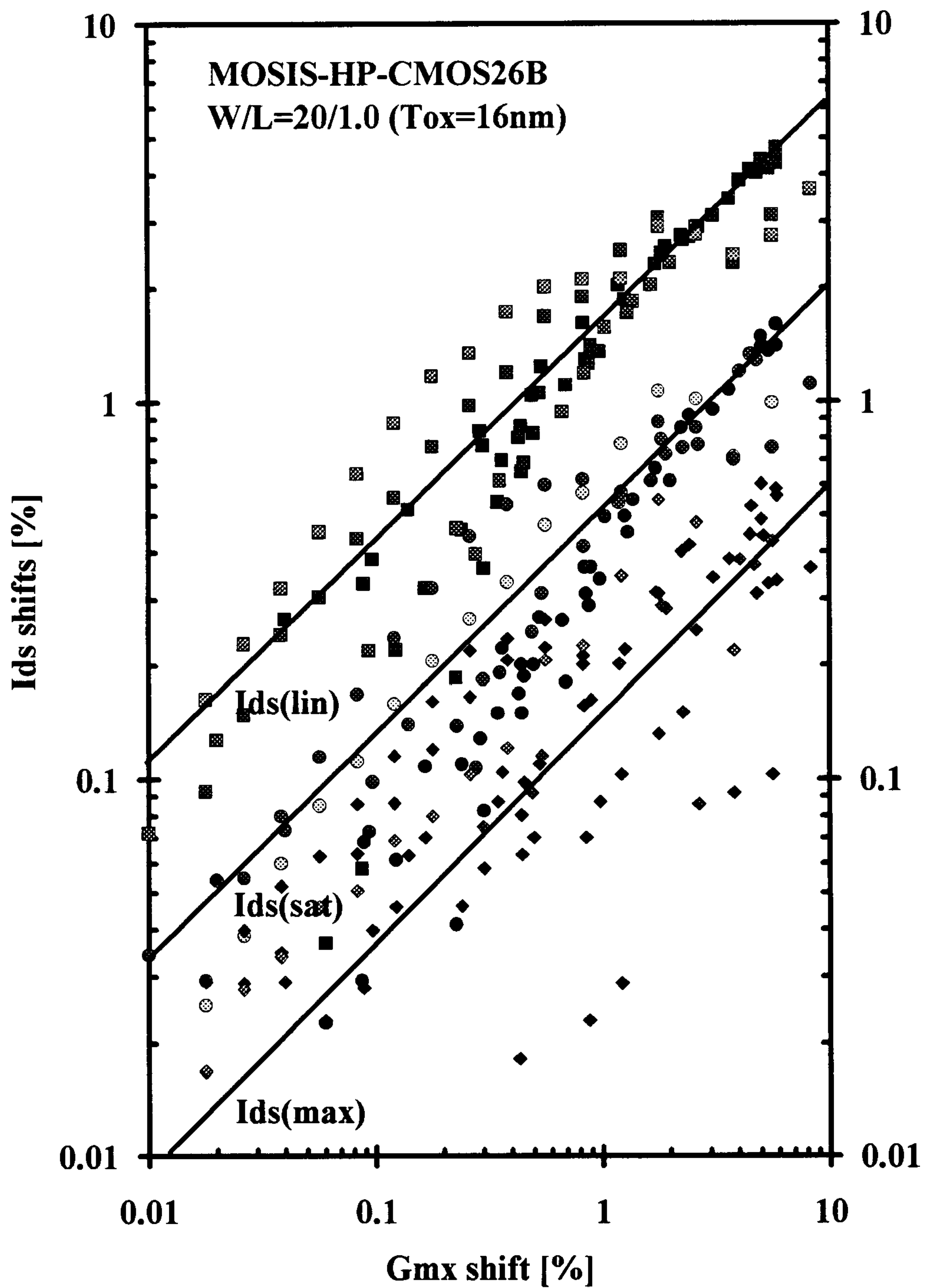


Figure 4-4 Ids degradation in terms of gmx degradation.

operating conditions. Hence Δgmx is more suitable for lifetime projections and reliability projections in circuit simulations.

Figure 4-5 shows an accelerated lifetime test and the maximum condition of the hot-carrier degradation with a constant Vds=7V. The maximum Δgmx change occurs around the maximum substrate current condition induced by the DAHI. Hence the accelerated lifetime test for lifetime projections is normally set to the DAHI condition at Vgs<Vds/2.

4.3 Lifetime Projections

Since all the hot-carrier effects are caused by a common force (i.e., the channel electric field near the drain region), the hot-carrier induced device degradation can be monitored by the substrate current which is an easily measurable quantity as shown in Fig. 4-6. Also, this substrate current can be easily modeled by using Eq. (2-5).

Table 4-1 shows some of previously reported lifetime models and definitions which were primarily based on process-oriented device parameters. In general, the power law relationship of lifetime projections on Isub(max) has been found to be in the range of 2~5 as shown in Table 4-1 where the common lifetime definition was made as ΔVt=10mV and Δgmx=10%. Due to the development in the reliability analysis which had been introduced into memory devices (i.e., DRAM) in digital IC's, the gm degradation is conceptually related to circuit performance such as an increase of the delay time in inverters and frequency shifts in a ring oscillator. In Table 4-1, notice that the lifetime model has developed into a more general form by inserting Ids into the empirical model of Takeda et al [43].

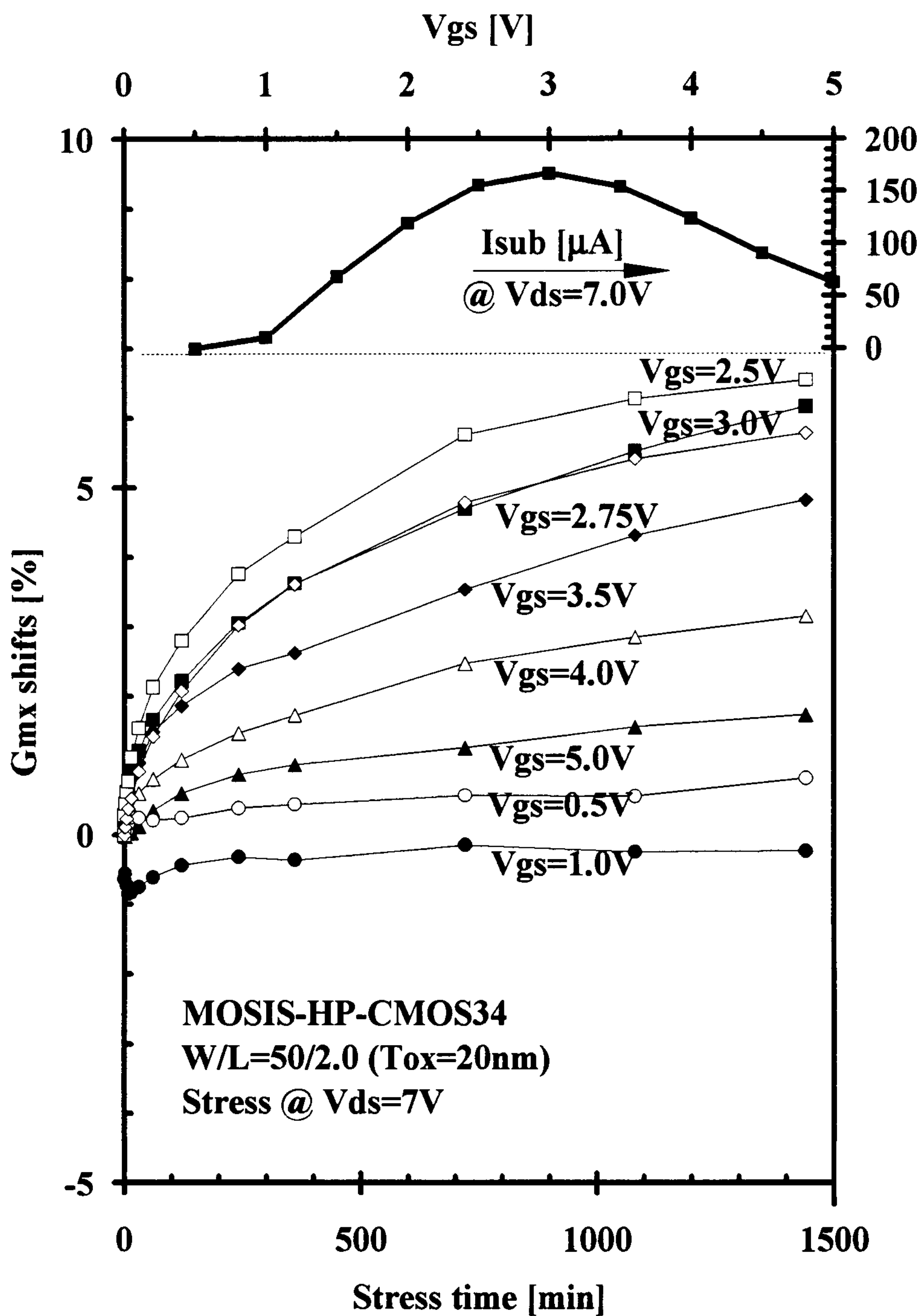


Figure 4-5 gmx degradation trend during accelerated lifetime tests.

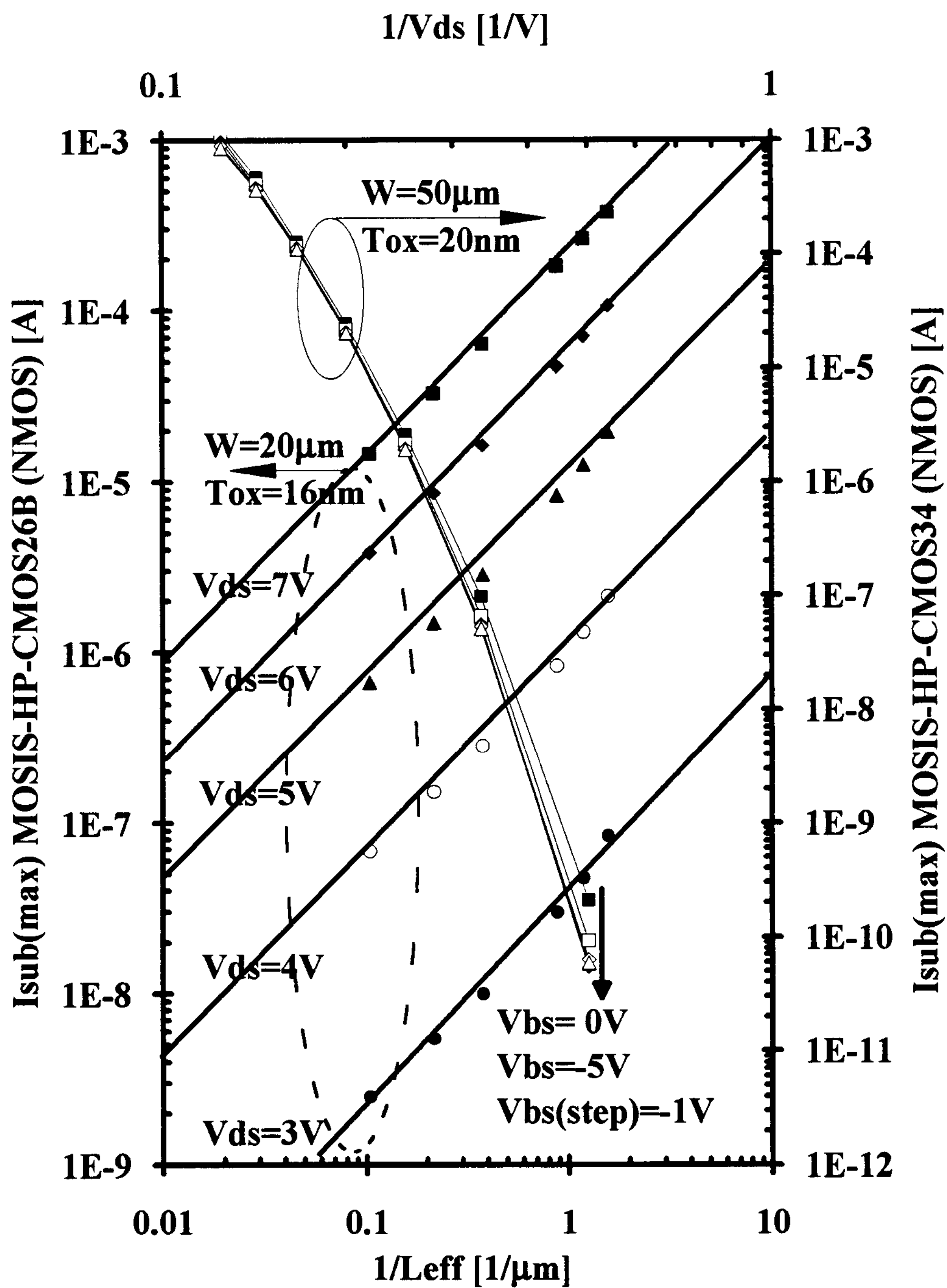


Figure 4-6 Isub(max) as a function of 1/Leff, 1/Vds, and Vbs.

Table 4-1 Lifetime models and power law of nMOSFET.

Group	Lifetime Model	Comment
Hitachi	$\tau = A \cdot Isub^{-m}$	Empirical
UC Berkeley	$\tau = B \cdot [Ids^{(m-1)}/Isub^{m}]$*	Semi-Emp.
Dig. Equip. Co.	$B = C \cdot (1/Leff)^{n}$	Leff
IMEC	$\tau \cdot Ids/W = A \cdot (Isub/Ids)^{-m}$	ΔIcp

* $m = \varphi_{it}/\varphi_{i} = 2.85$ ($\varphi_{it} = 3.7eV$ and $\varphi_{i} = 1.3eV$)

Group	Tox [nm]	W [μm]	L [μm]	Stress	Lifetime Definition	Power Law (m)	Measurement Condition
Hitachi [43]	7~ 10	10	0.35 ~2	DAHI	ΔVt (10mV)	3.4	Vg @ Id=1μA with Vd=5.0V
UC Berkeley [7]	11~ 82	50~ 100	1.2 ~2	DAHI & CHI	ΔVt (10mV)	2.9	Vg @ Id=.1μA/μm with Vd=50mV
Dig. Equip. Co. [29]	15	12.5	0.75 ~3	DAHI	Δgm (10%)	4~5	Vg @ Id=5μA with Vd=5.0V
IMEC [112]	30	25	2 ~10	DAHI	ΔIcp (50pA)	2~3	f=100kHz Vpp(pulse)=5V

In our work here, the lifetime projections for the IC design parameters were defined at the stress time for Δgmx=10%, ΔIdsat=2.5%, and Δgd=50%. These parameter shifts are directly related to the performance degradation of both digital and analog or mixed-mode circuits.

The design guidelines for reliability projections on MOSIS-HP-CMOS34 and -CMOS26B are shown in Figs. 4-7 and 4-8, respectively. It is hard to compare these two since their processes are different. For example, the CMOS34 and CMOS26B used LOCOS [116] and SWAMI [117] isolations, respectively. Hence they have different process-oriented hot-carrier effects. However, in design aspects and matching considerations, the circuit performance should remain constant given the same power supply. Hence, in this work, as long as the hot-carrier induced degradation of device parameters are measured under the same conditions, the lifetimes can be compared. In Figs. 4-7 and 4-8, the power law of the lifetime projections is about 3 for both devices which is close to the theoretical value of 2.85 [7].

For instance, as shown by the voltage scales at the top of Fig. 4-7 (CMOS34) the normalized substrate currents are about two times lower on 2μm devices as opposed to 1μm devices, this results in about eight times longer lifetimes (i.e., $(Isub[1\mu m]/ Isub[2\mu m])^{-3}$). However, longer drawn gate lengths result in smaller bandwidths and lower f_T values for the devices. While analog circuits normally use longer drawn gate lengths, up to 5μm, in reality the better engineering choice is to limit the voltages across analog devices rather than using longer gate lengths.

In the same manner, Fig. 4-8 shows the lifetime projections on the CMOS26B 1μm devices. By comparing two processes at Vdd=5.5V (the worst case), the normalized substrate current per unit channel width (Isub/W) of the CMOS34 and CMOS26B are 1μA/1μm and 3μA/μm, respectively. Hence the relative lifetime of CMOS26B is roughly longer by $\sim 3^3$. However, a careful examination of Idsat with

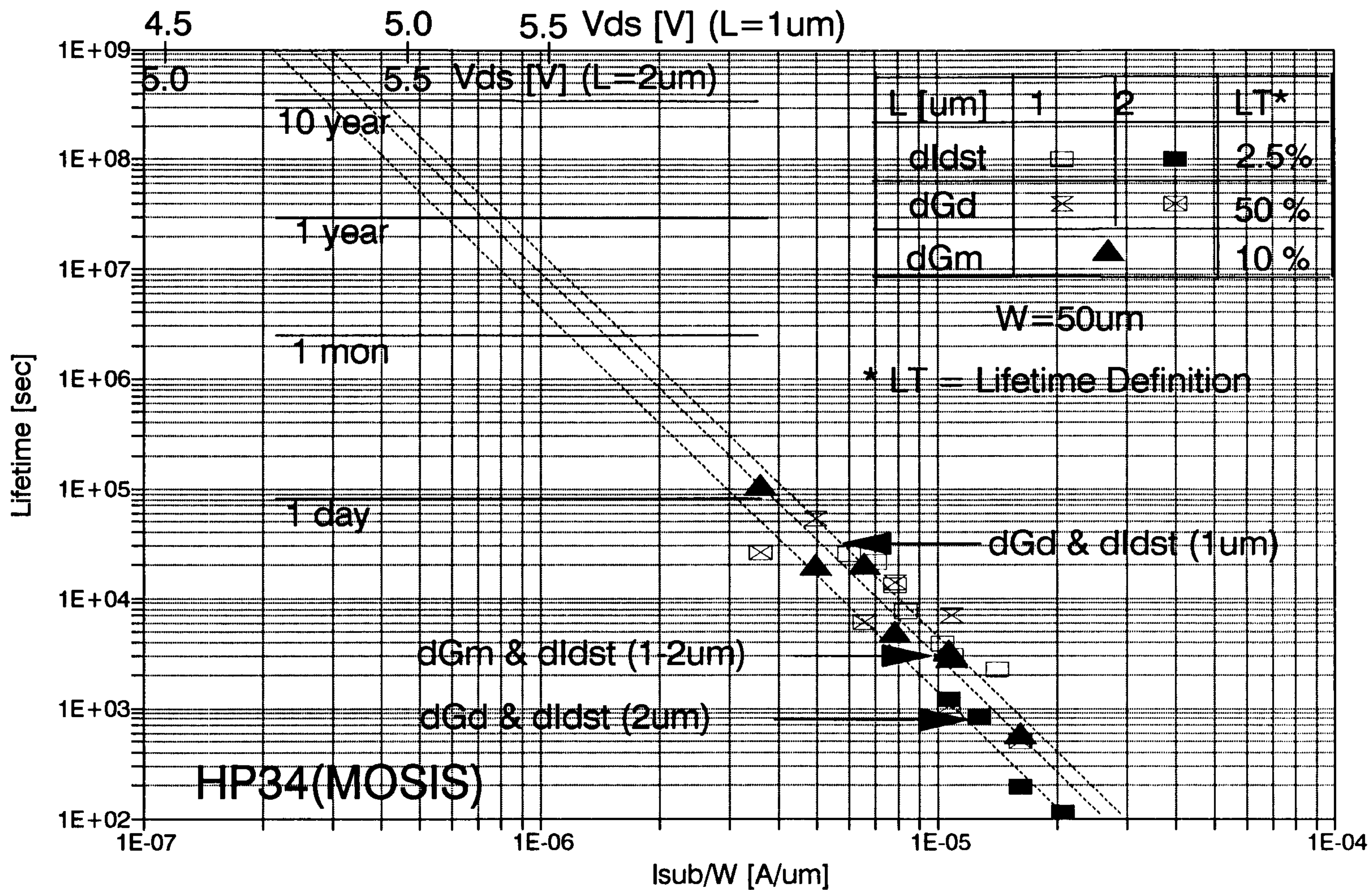


Figure 4-7 Lifetime projections on MOSIS-HP-CMOS34.

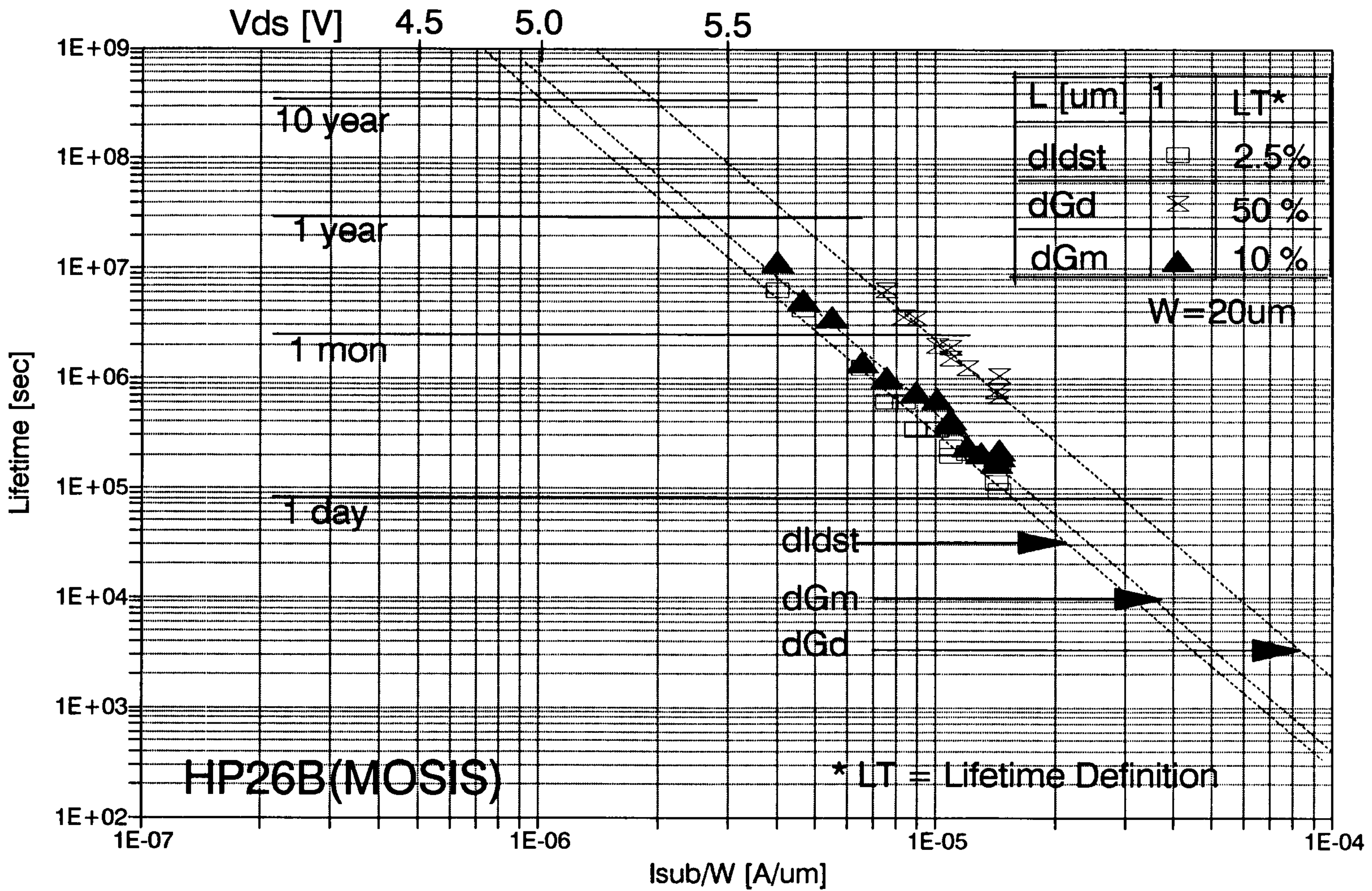


Figure 4-8 Lifetime projections on MOSIS-HP-CMOS26B.

L=1μm shows that the lifetime projections of CMOS 26B is shorter than that given by gm. This is due to the severe mobility degradation induced by the larger interface charge of the CMOS26B in comparison to CMOS34. Also, the enhanced gd degradation which occurs under hot-carrier stress shows that the main mechanism of hot-carrier effects in the CMOS26B is due to the mobility reduction. An increase of oxide trapped charge results in an increase of the threshold voltage rather than a degradation.

To demonstrate an importance of parameter mismatches, the hot-electron induced device parameter mismatches were simulated with a sense amplifier [118]. A sense amplifier is a very important circuit for a DRAM, the parametric mismatches due to hot-carrier injection can cause it to sense an incorrect logic level (either by '0' for a '1' or vice versa) in the memory cell. As shown in Fig. 4-9, our SPICE simulation results on a sense amplifier show that the sensitivity degradation (ΔS) of the sense amplifier is more influenced by the Idsat degradation (ΔS =65mV) rather than the degradation of the Gmx (ΔS=30mV) and the Gd (ΔS=3mV). Hence the reliability concerns in a sense amplifier should emphasize the current mismatch under user operating conditions.

During circuit operations, the degree of hot-carrier induced degradation (or age) of devices can be determined by Isub due to hot-carrier injection. In this study, an empirical model of the gm degradation under hot-carrier stress has been developed which is also to be used in reliability simulations in chapter 6. Assuming that the Isub of a fresh device is correlated with the gmx degradation during hot-carrier stress such as;

$$\Delta gmx(t)=C\cdot(F\cdot t)^{m} \qquad (4\text{-}1),$$

where

$$m=A\cdot(Isub/W)^{-n} \qquad (4\text{-}2).$$

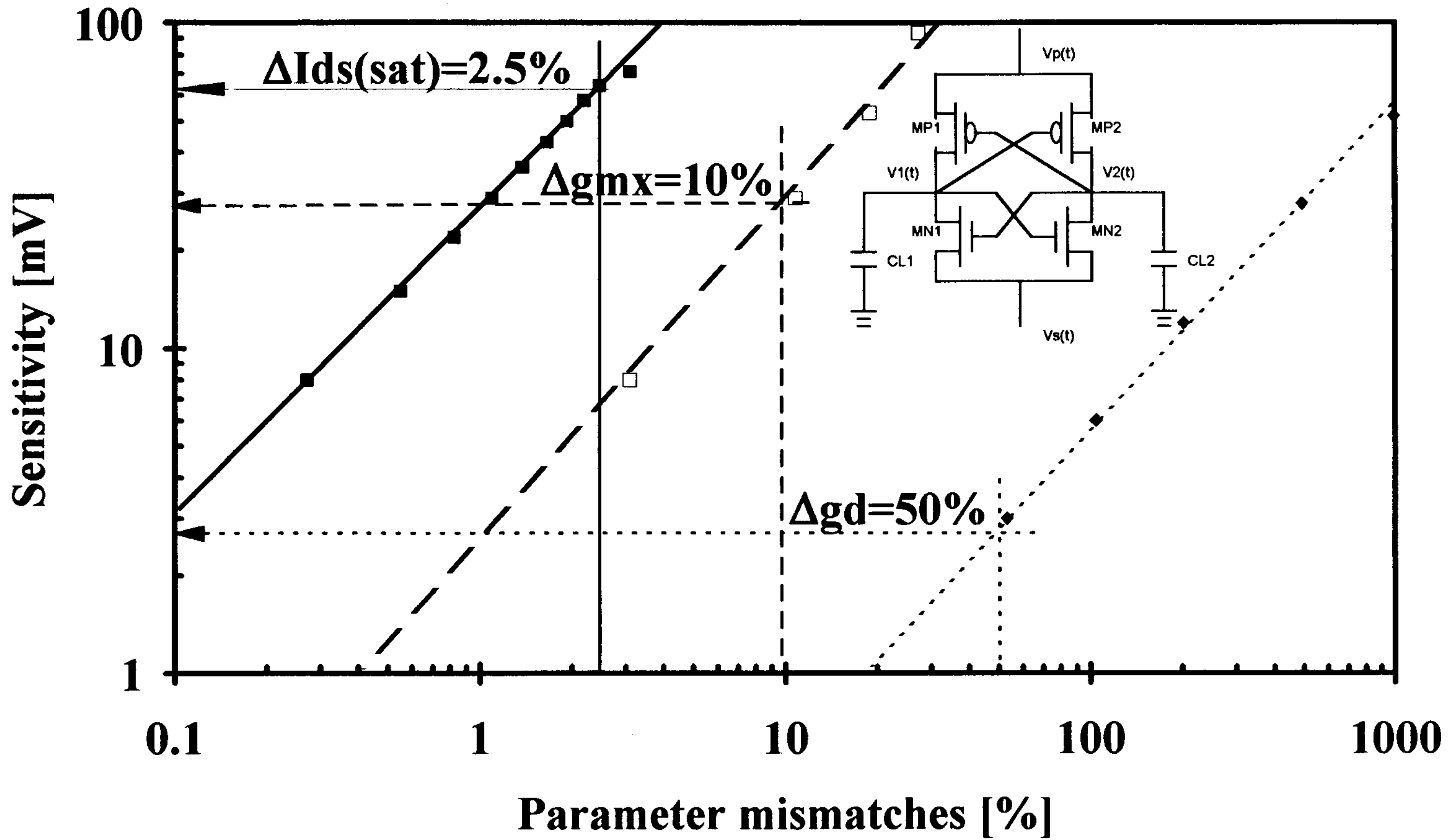


Figure 4-9 Parameter mismatches of a CMOS sense amplifier for reliability projections.

Hence, the plot of the lifetime projections can be easily converted into the model of the hot-carrier induced gm degradation by determining the empirical fitting parameters (C and F) of Eq. (4-1). The empirical parameters for MOSIS-HP-CMOS26B in Eqs. (4-1) and (4-2) have been found to be;

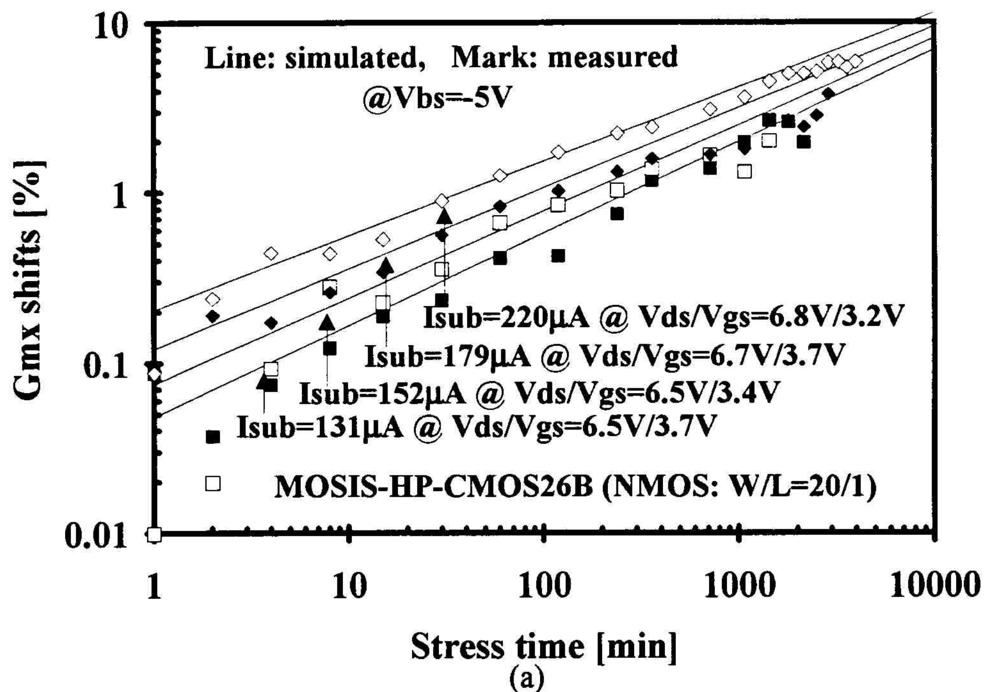
	C	F	A	n
nMOS	93.081	8.11×10^{-7}	4.04×10^{-3}	0.41
pMOS	47.612	1.40×10^{-7}	9.20×10^{-4}	0.37

with Isub/W in [A/μm] and t in [min].

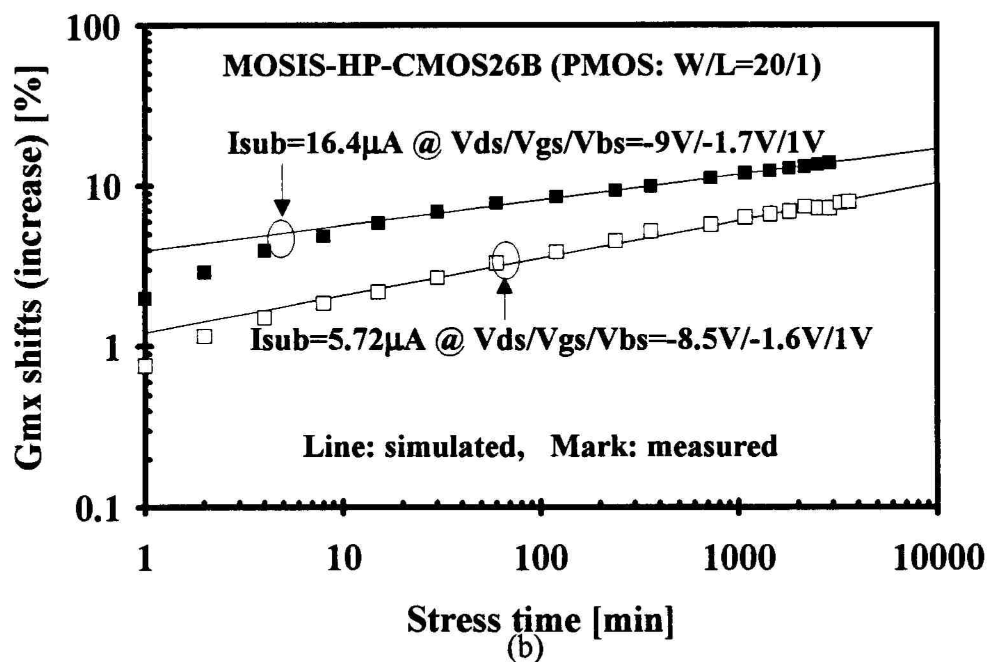
In Fig. 4-10, the simulation results of the gm degradation with hot-carrier stress are shown by lines and the measured data is in marks. Good results have been obtained in both n- and p-MOS devices. Hence, this gmx degradation model can be adopted to project the corresponding hot-carrier induced circuit parameters in reliability simulations.

4.4 Hot-Carrier Induced Degradation of SPICE MOS3 Parameters

In order to develop a model which correlates the lifetime projections with SPICE model parameters for MOSFET level 3 (MOS3), the maximum transconductance (gmx) in linear region was employed as a lifetime correlator of the SPICE MOS3. Gmx is not only sensitive to the interface and oxide trapped charges, but is also one of the major device parameters for circuit analysis and design. Also, gmx has been widely used for lifetime projections as discussed in the previous session. Therefore, hot-carrier induced degradation of SPICE MOS3 parameters can be



(a)



(b)

Figure 4-10 Empirical Δgmx model for MOSIS-HP-CMOS26B: (a) NMOS and (b) PMOS.

correlated with the gmx degradation for reliability projections in circuit simulations [99]-[100].

A full set of SPICE MOS3 parameters for the drain current model for DC conditions is shown Table 4-2 which includes about 10 parameters. Among the 10 parameters, 5 parameters are mainly used for the threshold voltage. Hence, once Vth is known (or measured), the rest of the Vth parameters become trivial. For that reason, the main emphasis on SPICE MOS3 parameter extraction during hot-carrier stress has been on VTO, GAMMA, THETA, UO, VMAX, and KAPPA which are also commonly adopted into reliability simulators such as BERT [108]-[109].

Figure 4-11 shows a flow chart of SPICE MOS3 parameter extraction which has been imbedded into HOTPEX. The linear region parameters (VTO and GAMMA) were first determined and then iterated until the linear region parameters converged. Secondly, the triode region parameters (UO, THETA, and VMAX) were then extracted. The saturation region parameter (KAPPA) was then finally obtained using the previously determined parameters. It should be noted that all of the SPICE model parameters are sensitive to bias points (both Vgs and Vds) for each region [119]-[121]. The best bias points for these parameter extractions should be initially optimized by comparing the I-V characteristic curves of SPICE simulation results and experimental measurements. The parameters extracted during hot-carrier stress can not be statistically optimized since the hot-carrier induced degradation of an individual device is destructive. However, the parameter shifts are not dependent upon the parameter extraction techniques but rather depend upon the stress conditions. To insure the accuracy of hot-carrier effects on the SPICE MOS3 parameters, the experimental data was tested under various stress conditions.

Table 4-2 SPICE MOSFET level 3 (MOS3) drain current equation [113].

Device Parameters	$Leff = L - 2 \times LD \qquad Weff = W - 2 \times WD$ $Vth = VTO + GAMMA \times (\sqrt{(Vbs + PHI)} - \sqrt{PHI}) + FN \times Vbs - DELTA \times Vds$ $\mu_s = \frac{UO}{1 + THETA \times (Vgs - Vth)}$ $Vdsat = \frac{Vgs - Vth}{1 + FB} + \frac{VMAX \times Leff}{\mu_s} - \sqrt{(\frac{Vgs - Vth}{1 + FB})^2 + (\frac{VMAX \times Leff}{\mu_s})^2}$
Vdsat≥Vds (Linear)	$Ids = Cox \times \frac{Weff}{Leff} \times \frac{UO}{\{1 + THETA \times (Vgs - Vth)\} \times \{1 + \frac{Vds}{VMAX \times Leff} \times \frac{UO}{1 + THETA \times (Vgs - Vth)}\}} \times (Vgs - Vth - \frac{1 + FB}{2} \times Vds) \times Vds$
Vdsat≤Vds (Saturation)	$Ep = \frac{(Vgs - Vth - \frac{1 + FB}{2} \times Vdsat) \times Vdsat}{[\{Vgs - Vth - (1 + FB) \times Vdsat\} \times Vdsat - \frac{(Vgs - Vth - \frac{1 + FB}{2} \times Vdsat) \times Vdsat}{\frac{VMAX \times Leff}{\mu_s} + Vdsat}] \times Leff}$ $\Delta L = \sqrt{(\frac{Ep \times Xd^2}{2}) + KAPPA \times Xd^2 \times (Vds - Vdsat)} - \frac{Ep \times Xd^2}{2}$ $Ids = Cox \times \frac{Weff}{Leff - \Delta L} \times \frac{UO}{\{1 + THETA \times (Vgs - Vth)\} \times \{1 + \frac{Vdsat}{VMAX \times Leff} \times \frac{UO}{1 + THETA \times (Vgs - Vth)}\}} \times (Vgs - Vth - \frac{1 + FB}{2} \times Vdsat) \times Vdsat$

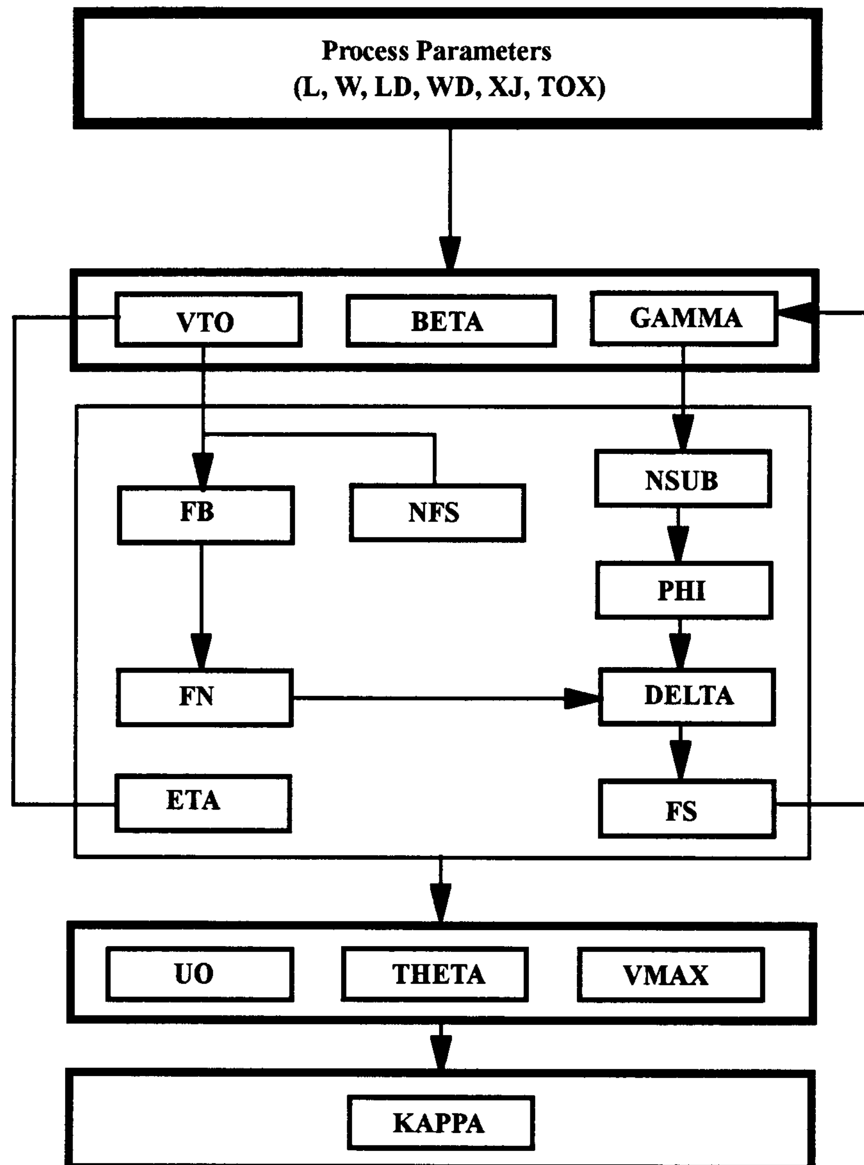


Figure 4-11 Schematic diagram of SPICE MOS3 parameter extraction.

While the gmx degradation is mainly related to the effective mobility reduction, the gate voltage shift in gmx degradation is determined by the threshold voltage shifts (Vth). In the SPICE MOS3 model, Vth and gm are defined as [113];

$$V_{th} = V_{FB} + PHI - DELTA \cdot V_{ds} + GAMMA \cdot F_S \sqrt{PHI - V_{BS}} + F_N \cdot (PHI - V_{BS}) \quad (4\text{-}3),$$

$$\beta = \frac{Weff}{Leff} \cdot \mu_{eff} \cdot Cox \quad (4\text{-}4),$$

$$gm = \frac{\partial Ids}{\partial Vgs} = \beta \cdot \frac{Vds}{1 + \theta \cdot (Vgs - Vth)^2} \quad (4\text{-}5).$$

Thus, the major contribution to the threshold voltage shift is due to the flatband voltage (V_{FB}) shift caused by the charge trapping in the CMOS gate oxide while the gm shift is induced by the interfacial charge trapping which reduces the effective channel mobility resulting in the gmx degradation. However due to the measurement limitations in the gate voltage shift at gmx (±100mV), the gmx degradation is most appropriate to use in making a correlation to lifetime projection and SPICE parameters.

Figure 4-12 shows the threshold voltage shifts as a function of the hot-carrier induced gmx degradation. Notice that the threshold voltage shifts are on a linear scale with the units of [mV] rather than the typical unit of [%] in logarithmic scales since Vth has been controlled to 0.7V during device processing. In order to reach the same amount of the gmx degradation of the nMOS device, the pMOS device needs either more stress time or higher field injection than the nMOS device due to the different degree of hot-carrier effects between n- and p-MOS devices. On the other hand, at an increase of 10mV in threshold voltage, the gmx degradation of the nMOS device is about 3 times larger than that of the pMOS device. The nMOS degradation dominates the threshold voltage shifts in CMOS devices, and is mainly caused by the increase of .the oxide trapped charge.

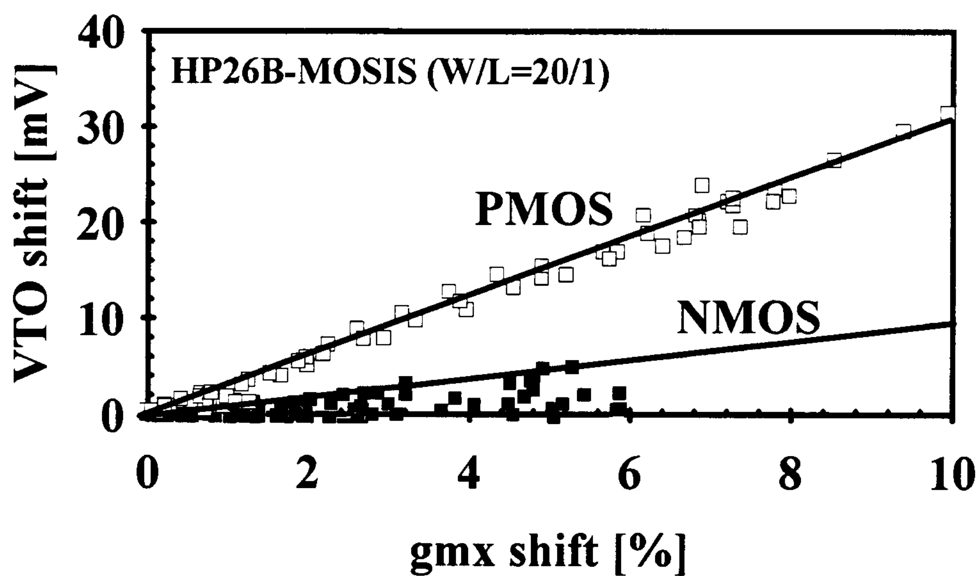


Figure 4-12 VTO shifts as a function of gmx degradation.

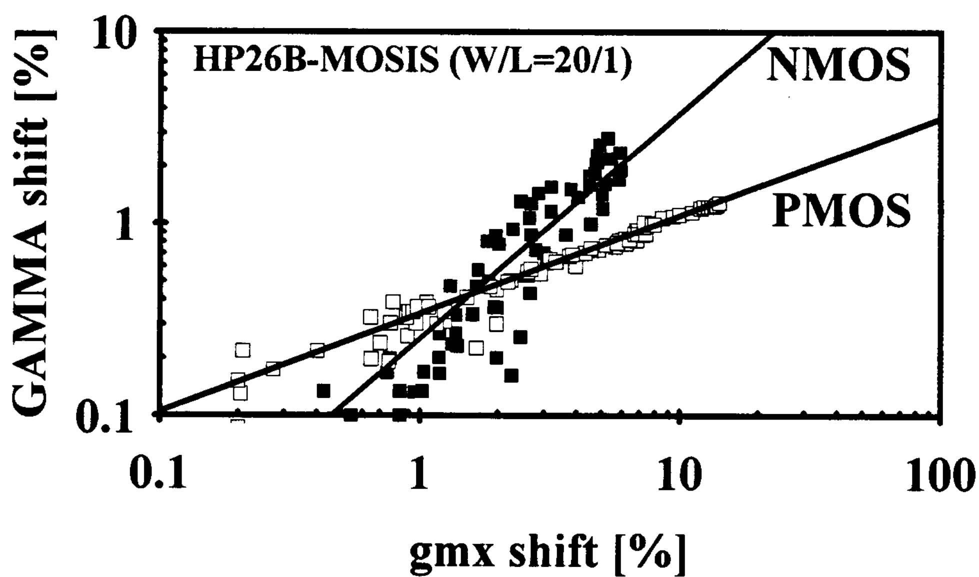


Figure 4-13 GAMMA shifts as a function of gmx degradation.

The GAMMA shifts due to hot-carrier injection are shown in Fig. 4-13 where the GAMMA of the nMOS devices decreases while that of the pMOS devices increases. Since GAMMA ($\gamma = \frac{\sqrt{2 \cdot q \cdot \varepsilon_{Si} \cdot NSUB}}{Cox}$) increases with increasing substrate doping, this phenomenon explains that the trapped charge in the gate oxides and/or surface states is negative. For instance, this trap charge can be modeled with NSUB (i.e., by changing NSUB(nMOS)↓ or NSUB(pMOS)↑). However, since NSUB is also related to VTO ($VTO = V_{FB} + PHI + \gamma \cdot \sqrt{PHI}$) in terms of PHI ($2 \cdot \varphi_F = 2 \cdot \frac{k \cdot T}{q} \cdot \ln(\frac{NSUB}{n_i})$), the experimental relationship has been empirically modeled by the hot-carrier induced gmx degradation.

Figure 4-14 shows the mobility shifts as a function of the gmx degradation which decreases in the nMOS case and increases in the pMOS case. The slope of degradation rate is about 1 implying that the hot-carrier induced gmx degradation is mainly due to the mobility degradation in both p- and n-MOS devices.

Figure 4-15 shows the hot-carrier induced degradation of the mobility modulation parameter which is used to simulate mobility degradation as a function of the applied gate voltage. It should be pointed out that the UO and THETA shifts match the gmx degradation and these relationship can simplify the parameter extraction for reliability simulations.

VMAX shifts as a function of the gmx degradation are shown in Fig. 4-16. The increase of VMAX after hot-carrier stress implies that the channel electric field increases with the hot-carrier induced trapped charge. Hence the increased VMAX can be interpreted as the channel length reduction due to the trapped charge which is located near the drain region.

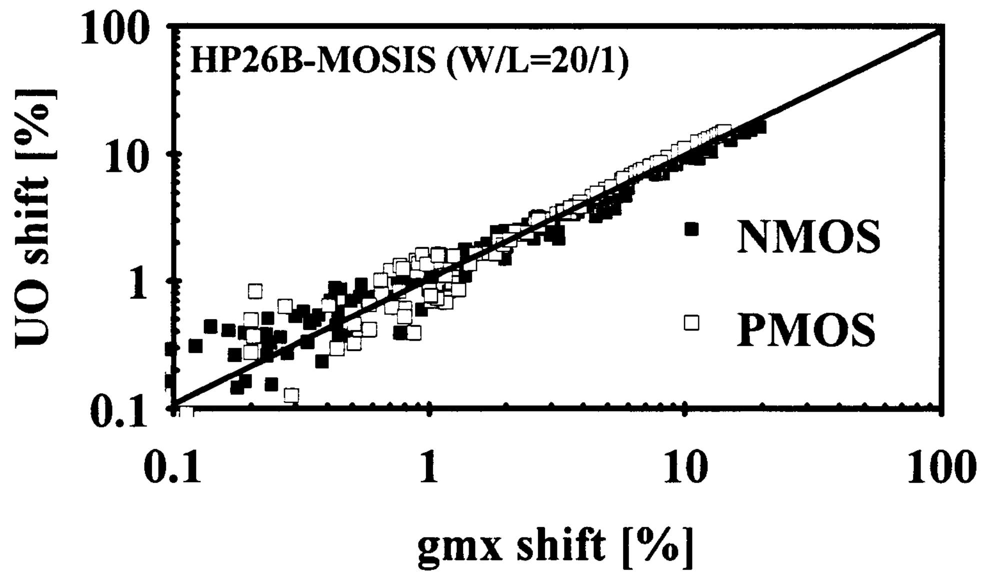


Figure 4-14 UO shifts as a function of gmx degradation.

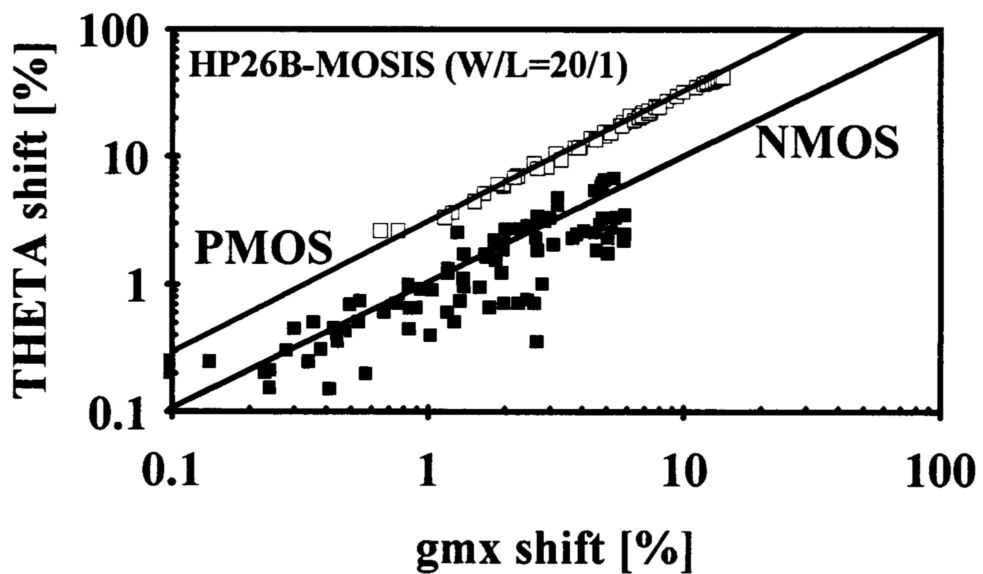


Figure 4-15 THETA shifts as a function of gmx degradation.

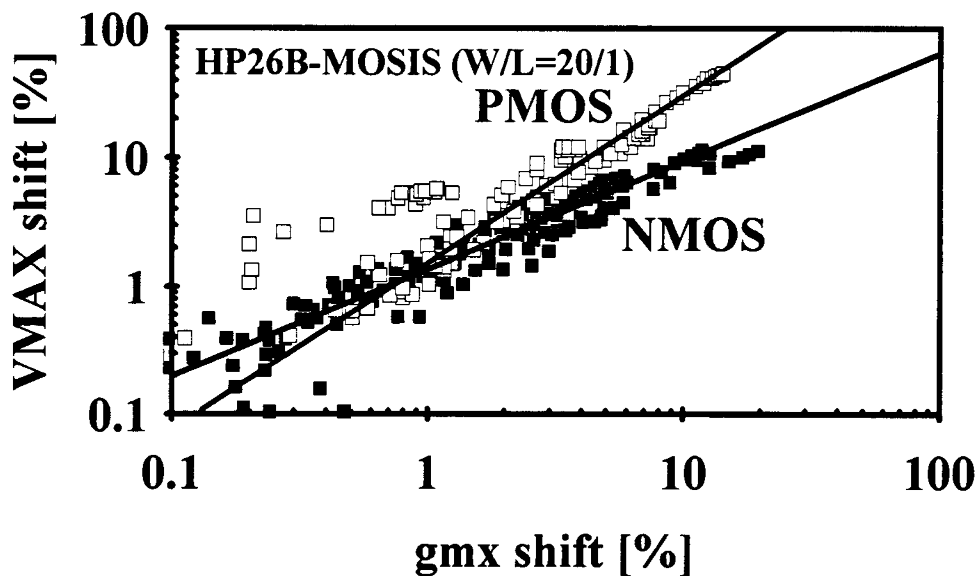


Figure 4-16 VMAX shifts as a function of gmx degradation.

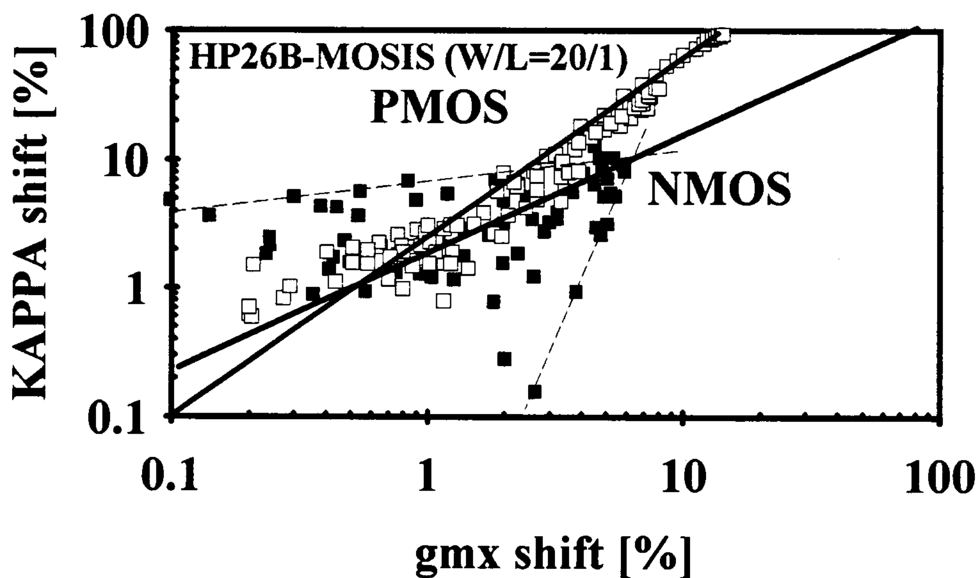


Figure 4-17 KAPPA shifts as a function of gmx degradation.

KAPPA is the saturation field correlation factor, and the increase of KAPPA is shown in Fig. 4-17. KAPPA is determined from the calculated saturation drain voltage and current and then the adjusted the saturation region electric field ($\propto$Vdsat/$Leff_{sat}$) which increases with decreasing $Leff_{sat}$ (i.e., channel length reduction). Hence KAPPA increases after hot-carrier stress. The large scatter in KAPPA shifts suggests that the hot-carrier induced trap charge is non-uniformly localized near the drain region.

In order to obtain the degraded circuit parameters for reliability simulations, the hot-carrier induced degradation of SPICE MOS3 parameters has been summarized as shown in Table 4-3. Also, the empirical model of the degraded circuit parameter shifts in terms of the gmx degradation is presented in Table 4-3. Hence, by using Eqs. (4-1) and (4-2), the circuit parameters for the hot-carrier induced degradation of circuit simulations can be obtained as follows;

1) Calculate Isub/W under operating conditions from Eq. (2-5) and Table 2-2.
2) Calculate the Δgmx from Eqs. (4-1) and (4-2).
3) Calculate Δ from Table 4-3, and then, find the degraded SPICE MOS3 parameters.

The results of these parameter shifts for an nMOS device are shown in Fig. 4-18 where the simulated results are in lines and the extracted parameter shifts are in marks. As a rule of thumb, the 10% gmx degradation (which is the same as a 10% Ids reduction in the linear region) due to hot-carrier induced trapped charge can be simulated as 10% shifts of the SPICE MOS3 parameters in general, in which case projected lifetime will not be overestimated.

Table 4-3 Empirical model parameters of hot-carrier induced SPICE MOS3 parameter shifts as a function of gmx degradation.

$$\Delta = A \cdot |\Delta Gm \max[\%]|^{m}$$

T= @ 10% Gmmax shift

MOS3	TYPE	N		P			N	P	N	P
Δ	UNIT	A	m	A	m	UNIT	t=0	t=0	t=T	t=T
VTO	[mV]	+1.00	1.00	+3.00	1.00	V	0.46	-0.43	0.47	-0.40
GAMMA	[%]	-0.26	1.21	+0.34	0.53	$V^{1/2}$	0.30	0.36	0.29	0.36
UO	[%]	-1.00	1.00	+1.00	1.00	$cm^2/V/s$	510	104	459	114
THETA	[%]	+1.00	1.00	+3.16	1.00	1/V	0.2	0.1	0.22	0.13
VMAX	[%]	+1.33	0.83	+1.53	1.29	$10^5 m/s$	1.33	2.00	1.45	2.60
KAPPA	[%]	+1.90	0.91	+2.40	1.39		0.24	6.00	0.28	9.53

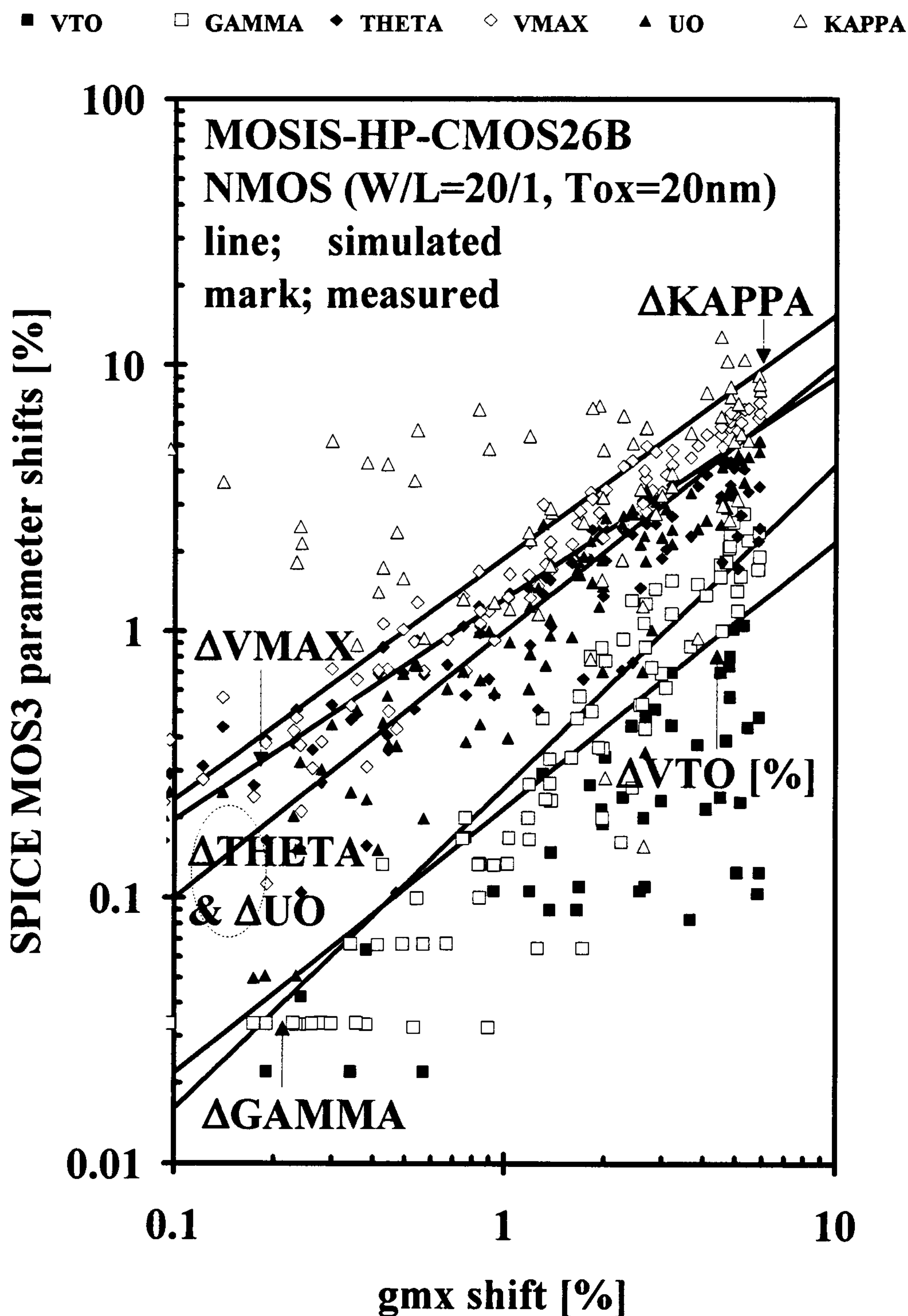


Figure 4-18 Hot-carrier induced degradation of SPICE MOS3 (NMOS) parameters as a function of gmx shifts.

4.5 Summary

In order to improve process optimization and assess device reliability in CMOS technology, hot-carrier effects in CMOS device parameters have been investigated. In this study two different processes have been compared by means of lifetime projections on design-specific device parameters such as gmx (maximum value in the linear region) = 10% , gd (minimum value in the saturation region) = 50%, and Idsat (measured at Vdsat with Vgs=5V) = 2.5%. The MOSIS-HP-CMOS26B process whose Isub/W value is 3 times less than that of MOSIS-HP-CMOS34 has been shown to be more reliable in device operation than MOSIS-HP-CMOS34. Also, the power law of the conventional lifetime model has been found to be around 3 which is close to the theoretical values of 2.85. By using the gmx degradation, the hot-carrier induced degradation of the SPICE MOS3 parameters has been examined, and a model for reliability projections in circuit simulations has been proposed and shown to be acceptable.

5. PHYSICAL MODEL OF DRAIN CONDUCTANCE DEGRADATION

5.1 Introduction

MOSFET instability due to hot carrier injection into gate oxides is a potential problem for sub-micron ultra large scaled integrated circuits (ULSI) and a reliability issue. Many studies have been made of this problem and it has been reported that the degradation of nMOSFET's is caused by the interface state generation and electron trapping in the gate oxide due to hot carrier injection [7], [122]-[124]. Lifetime predictions of the devices based on mobility reduction due to interface state generation have been also proposed [82]. Although there have been some publications on lifetime predictions in digital circuits by using parameters in saturation region [80], [125]-[126], in general, degradation of the transconductance or the drain current in linear region is considered for lifetime predictions in these simulations because of the standard practices which have developed in the industry in defining test conditions.

Recently, it has been reported that an important analog circuit parameter, drain conductance, gd, in the saturation region is also degraded by hot carrier injection [98], [127]-[128]. In predicting the lifetime of analog circuits, it is important that the phenomenon of gd degradation is clearly explained and modeled. However, the mechanism of gd degradation is not well understood. The difficulty of gd degradation modeling is due to the distribution of the damaged region such as the interface states and electron trapping in the gate oxide along the direction of the channel. Here, a gd degradation model is proposed by using the gradual channel approximation. In this modeling, a simple distribution of interface states which has a step function along the length of the channel has been considered because the depletion region near the drain

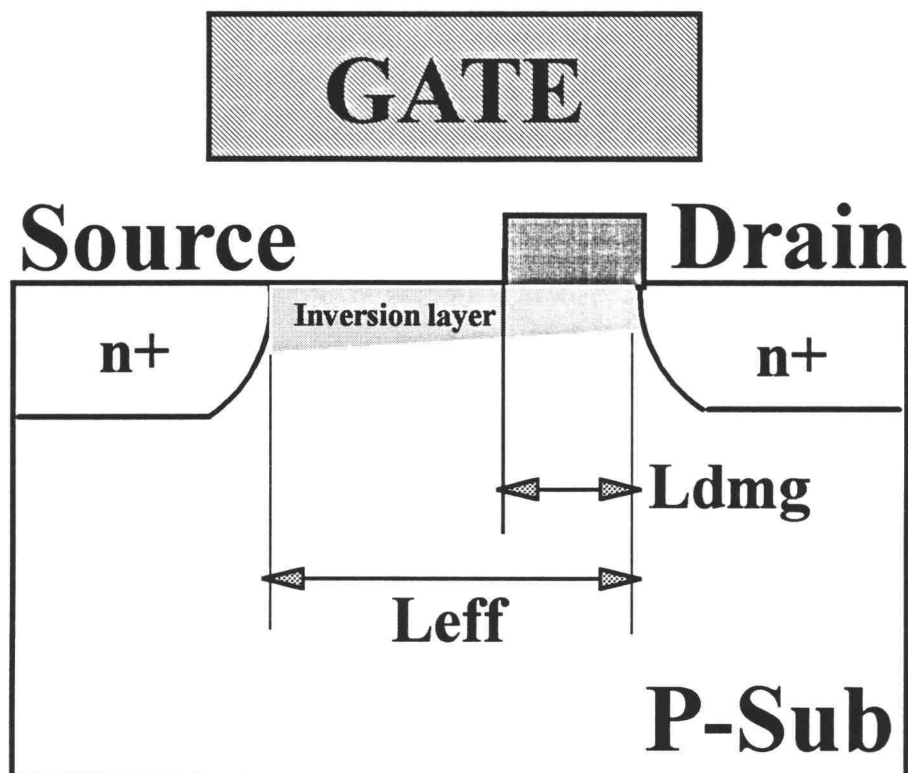
can shield the charge of the interface states and trapped electrons and the contribution of these charges can be neglected in the saturation region. It is assumed that only the mobility reduction due to interface states generated by hot carrier injection affects the gd degradation.

In section 5.2, the model which has been proposed is described. By using this model, gd degradation can be related to gm degradation in the linear region which is usually monitored in the hot carrier degradation of MOSFET's. In section 5.3, the fitting of the model to data is also demonstrated which includes the Leff dependence.

5.2 Model Derivations

Figure 5-1 shows a schematic cross-section of a degraded nMOSFET due to hot carrier injection. The interface states were generated in the channel region near the drain edge or drain end. The distribution of interface states along the length of the channel was assumed to be a step function which has value Nits in the damaged region (Ldmg); $Nit(y) = 0$ at $0 \le y \le Leff - Ldmg$ and $Nit(y) = Nits \cdot (\frac{y - Leff}{Ldmg} + 1)$ at $Leff - Ldmg \le y \le Leff$ where Leff is the effective channel length between metallurgical junctions of the source and the drain. These interface states are acceptor like traps and negatively charged when gate voltage is higher than the threshold voltage and electrons are present in an inversion layer.

When the MOSFET is in linear region assuming that the net charge in interface traps is negative-fixed charges for an nMOSFET operating in strong inversion (Vgs> Vto), then from the gradual channel approximation, the potential rise along the channel can be given by



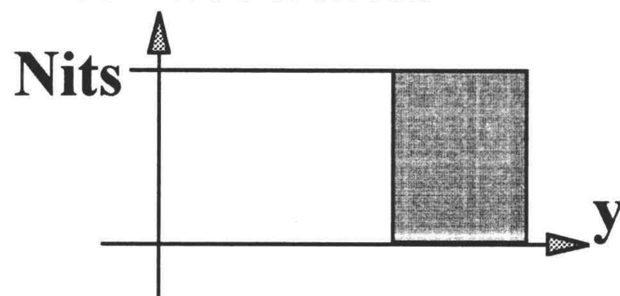


Figure 5-1 Schematic cross-section of the damaged MOSFET in linear region.

$$\partial V = -\frac{Ids}{Weff \cdot \mu \cdot Qn(y)} \cdot \partial y \quad (5\text{-}1)$$

where Ids is the drain current, W is the width of channel, Qn(y) is the charge of electrons in the inversion layer, and μ is effective mobility of electrons at the surface [59]. If this negative charge is reduced by interface states, Qn(y) is then expressed by [129]

$$Qn(y) = -Cox \cdot (Vgs - Vto - V(y)) + q \cdot Nit(y) \quad (5\text{-}2)$$

where Cox is the capacitance of the gate oxide, Vto is the threshold voltage, and q is the unit electron charge. Substituting Eq. (5-2) into Eq. (5-1) and integrating from source to drain yields

$$\int_0^{Leff} (\mu_o \cdot Ids)/(\mu \cdot Leff) \cdot \partial y = (\mu_o \cdot Weff/Leff) \int_0^{Vds} \{Cox \cdot (Vgs\text{-}Vto\text{-}V(y))\text{-}q \cdot Nit(y)\} \cdot \partial V \quad (5\text{-}3)$$

where μ_O is the mobility in the non-damaged region and μ is the mobility in the damaged region. Using an empirical mobility degradation model [130], the mobility, μ, can be expressed by

$$\mu = \frac{\mu_O}{1 + \alpha \cdot Nits} \quad (5\text{-}4)$$

where α=(-0.104+0.0193·log(Na))·1×10^{-11} [cm^2], μ_0=3490-164·log(Na) [cm^2/V/s], and Na is substrate doping concentration. In our modeling, Na=2.8×10^{16} [1/cm^3], α=2.13×10^{-12} [cm^2] and μ_O =792 [cm^2/V/sec] have been used. By using Eq. (5-4), the left-hand-side of Eq. (5-3) then becomes

$$\int_0^{Leff} (\mu_o/\mu) \cdot (Ids/Leff) \cdot \partial y = Ids \cdot \{1 + \alpha \cdot Nits \cdot (Ldmg/Leff)\} \quad (5\text{-}5)$$

The first term of the right-hand-side in Eq. (5-3) is identical to the drain current of a non-degraded MOSFET and becomes

$$(\mu_o \cdot Weff/Leff) \cdot \int_0^{Vds} Cox \cdot (Vgs\text{-}Vto\text{-}V(y)) \cdot \partial V = (\mu_o \cdot Weff/Leff) \cdot Cox \cdot (Vgs\text{-}Vto\text{-}Vds/2) \cdot Vds \tag{5-6}$$

In the second term of the right-hand-side in Eq. (5-3), it is assumed that $\partial V=(\partial V/\partial y)\cdot\partial y \cong (Vds/Leff)\cdot\partial y$ for the channel region of a MOSFET in the linear region with a small Vds. Therefore,

$$-(\mu_o Weff/Leff) \int_0^{Vds} q \cdot Nit(y) \cdot \partial V = -(\mu_o \cdot Weff/Leff) \cdot q \cdot Nits \cdot (Ldmg/Leff) \cdot Vds \tag{5-7}$$

Substituting Eqs. (5-5), (5-6), and (5-7) into Eq. (5-3) yields

$$Ids \cdot (1 + \alpha \cdot Nits \cdot \frac{Ldmg}{Leff})$$

$$= \frac{\mu_o \cdot Weff}{Leff} \cdot Cox \cdot (Vgs - Vto - \frac{Vds}{2}) \cdot Vds - \frac{\mu_o \cdot Weff \cdot Ldmg \cdot q \cdot Nits \cdot Vds}{Leff^2} \tag{5-8}$$

Differentiating Eq. (5-8) with respect to Vgs yields

$$(1 + \alpha \cdot Nits \cdot \frac{Ldmg}{Leff}) \cdot \frac{\partial Ids}{\partial Vgs} = \frac{\mu_o \cdot Weff}{Leff} \cdot Cox \cdot Vds$$

$$(1 + \alpha \cdot Nits \cdot \frac{Ldmg}{Leff}) \cdot gm = \frac{\mu_o \cdot Weff}{Leff} \cdot gm_o$$

$$Nits = \frac{1}{\alpha} \cdot \frac{Leff}{Ldmg} \cdot \frac{gm_o - gm}{gm} \tag{5-9}$$

where gm is the degraded transconductance $(\partial Ids/\partial Vgs)$, and gm_o is the transconductance of a fresh device. From Eq. (5-9), then the interface states generated

by hot carrier injection can be calculated from the transconductance change, $(gm_o-gm)/gm$.

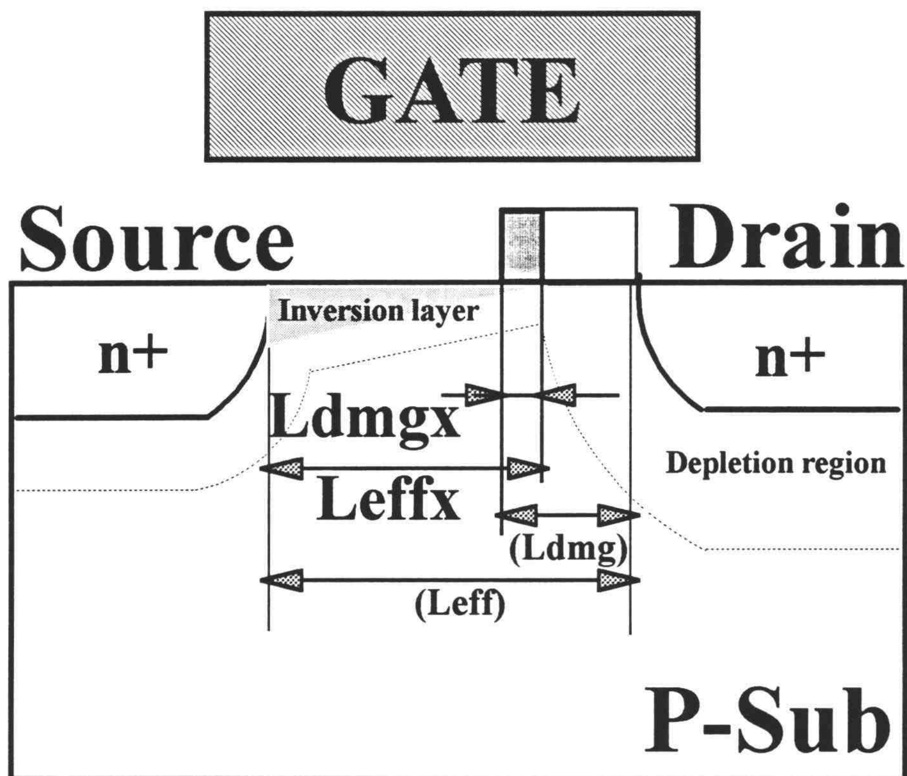
In the saturation region (Vds>Vgs-Vto), a depletion region is formed between the pinch-off point and the drain edge as shown in Fig. 5-2. The conducting electrons which flow through the inversion layer by drift are injected into the depletion region and then accelerated by the high electric field in this depletion region. Therefore, the drain current in saturation region is limited by the drift current of electrons from the source to the pinch-off point. Consequently, Eq. (5-3) is also valid for the drain current in saturation region when Leff is changed to Leffx and Vds to Vdsat. Leffx is effective gate length which is the length between source edge and pinch-off point and Vdsat is the voltage at the pinch-off point. The drain current equation in saturation region is given by

$$\int_0^{Leffx} (\mu_o/\mu)\cdot(Ids/Leff)\cdot\partial y = (\mu_o\cdot Weff/Leff)\int_0^{Vdsat}\{Cox\cdot(Vgs\text{-}Vto\text{-}V(y))\text{-}q\cdot Nit(y)\}\cdot\partial V \quad (5\text{-}10)$$

In this integration, the contribution of interface states must also be taken into account. The interface states in the depletion region near the drain are almost all neutral and make no contribution to the integration because the interface states are acceptor like traps and the surface potential in this region is lower than $2\phi_f$. Upon considering this interface state contribution, then Eq. (5-10) becomes

$$Ids = \frac{Leffx}{Leffx + Ldmgx\cdot\alpha\cdot Nits}\cdot Ids_o - \frac{\mu_o\cdot Weff\cdot Ldmgx\cdot q\cdot Nits\cdot Vdsat}{Leffx\cdot(Leffx + Ldmgx\cdot\alpha\cdot Nits)} \quad (5\text{-}11),$$

where $$Ids_o = \mu_o\cdot Cox\cdot\frac{Weff}{Leffx}\cdot\frac{Vdsat^2}{2} \quad (5\text{-}12),$$



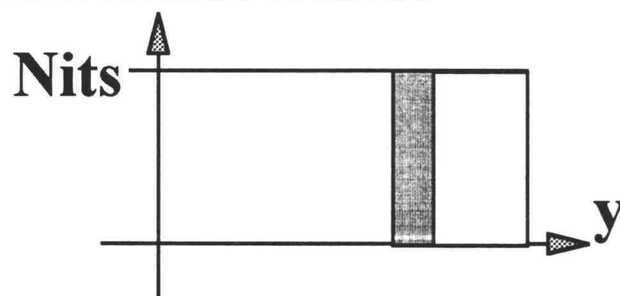


Figure 5-2 Schematic cross-section of the damaged MOSFET in saturation region.

where Ldmgx is the length between the damaged region edge and pinch-off point as shown in Fig. 5-2. If Leffx, Ldmgx, and Vdsat are known, the drain current, Ids, can be calculated from Nits which is calculated from $(gm_o-gm)/gm$ by using Eq (5-9).

In Eq.(5-11), the first term on the left-hand-side is the drain current degradation due to the mobility reduction in the damaged region. The second term is the contribution of interface charge to inversion layer formation. This term can also include the electron trapping in the gate oxide above the damaged region when q·Nits in the numerator is replaced by q·{Nits+q·Nots·(tox-X)/tox} where Nots is the electron trap density in the oxide, tox is the gate oxide thickness, and X is centroid of the trapped electron from the surface of Si. In comparing the first term and the second term of Eq. (5-11), the second term can be neglected when Ldmgx is small because the depletion region near the drain shields the charge of the interface states and the trapped electrons in the oxide. For instance, with values of W=50μm and L=1.0μm for a conventional LDD-nMOSFET in the saturation region (at Vds=5.0V and Vgs=5.0V), the first term is around 15mA and the second term is less than 1μA. Therefore, the drain current in saturation region after stress is given by

$$Ids = \frac{Leffx}{Leffx + Ldmgx \cdot \alpha \cdot Nits} \cdot Ids_O \qquad (5\text{-}13)$$

From this equation, the degradation of the drain current in the saturation region is mainly caused by mobility reduction due to interface states generated by hot carrier injection and it is expected from Eqs. (5-8) and (5-13) that the drain current degradation rate in the saturation region is smaller than that in the linear region.

Drain conductance (gd) is given by differentiating Ids with respect to Vds. Using Eq.(5-13), gd then becomes

$$gd = \frac{\partial Ids}{\partial Vds} = -\frac{(Leffx - Ldmgx)\cdot\alpha\cdot Nits}{(Leffx + Ldmgx\cdot\alpha\cdot Nits)^2}\cdot\frac{\partial Leffx}{\partial Vds}\cdot Ids_o + \frac{Leffx}{Leffx + Ldmgx\cdot\alpha\cdot Nits}\cdot gd_o$$

(5-14)

where gdo is drain conductance of a fresh device. From Eq. (5-12), drain conductance of a fresh device is given by

$$gd_o = \frac{\partial Ids_o}{\partial Vds} = -\mu_o\cdot Cox\cdot\frac{Weff}{Leffx^2}\cdot\frac{Vdsat^2}{2}\cdot\frac{\partial Leffx}{\partial Vds} = -\frac{Ids_o}{Leffx}\cdot\frac{\partial Leffx}{\partial Vds} \quad (5\text{-}15)$$

Substituting Eq. (5-15) into Eq. (5-14) yields

$$gd = \frac{(Leffx - Ldmgx)\cdot\alpha\cdot Nits}{(Leffx + Ldmgx\cdot\alpha\cdot Nits)^2}\cdot Leffx\cdot gd_o + \frac{Leffx}{Leffx + Ldmgx\cdot\alpha\cdot Nits}\cdot gd_o$$

$$= \frac{Leffx^2\cdot(1+\cdot\alpha\cdot Nits)}{(Leffx + Ldmgx\cdot\alpha\cdot Nits)^2}\cdot gd_o \quad (5\text{-}16)$$

When Ldmgx<<Leffx, Eq.(5-16) can be approximated as $gd \cong (1+\alpha\cdot Nits)\cdot gd_o$. Thus, by using Eq. (5-9), Eq. (5-16) becomes

$$\frac{gd - gd_o}{gd_o} = \alpha\cdot Nits = \frac{Leff}{Ldmg}\cdot\frac{gm_o - gm}{gm} \quad (5\text{-}17)$$

By using Eq. (5-17), drain conductance degradation can then be predicted from the transconductance (gm) degradation. This equation is then the basic equation of our gd degradation model.

5.3 Experimental and Simulation Results

The nMOSFETs used in this study were fabricated by a 1.0μm N-well CMOS process. LOCOS isolation and conventional LDD structures (MOSIS-HP34CMOS) were employed. The gate oxide thickness is 20nm and the channel width and length of the nMOSFETs are 50μm and 0.8-2.0μm, respectively.

The transconductance in linear region (gm) and the drain conductance in saturation region (gd) were monitored with stress time. The transconductance (gm) was measured at Vds=0.1V and displays the usual maximum upon varying Vgs. The drain conductance (gd) was measured at Vgs=5.0V and displays a minimum value upon varying Vds. The lifetime of the MOSFETs was defined as a 10% gm degradation or a 50% gd degradation [125], [131]. The stress conditions of the nMOSFETs were set with a value of Vgs to give a maximum substrate current for a given Vds value. The MOSFETs were usually stressed at this condition for at least one day.

The gain of a single transistor amplifier was also measured under DC stress as a function of time. The amplifier consisted of an nMOSFET and a constant current source as show in Fig. 5-3. In the measurements, the channel width and length of the nMOSFET are 50μm and 1.0μm respectively. The constant current source was set at Ibias=5mA and the gate voltage was set to give the maximum gain for a fresh device (Vgs=2.56V for this case). The input signal was 50mVp-p. The transconductance (gm) and the drain conductance (gd) were also measured at the same condition as the operating point of the amplifier. The stress condition for this measurement was Vds=7.0V and Vgs=2.5V which gave the maximum substrate current.

Gain degradation of a single nMOSFET amplifier with DC stress time is shown in Fig. 5-4. The initial gain was about 30. However, the gain degraded to about 10 after 1×10^4sec of stressing. The gain of amplifier is given by Gain=gm/gd where gm and gd

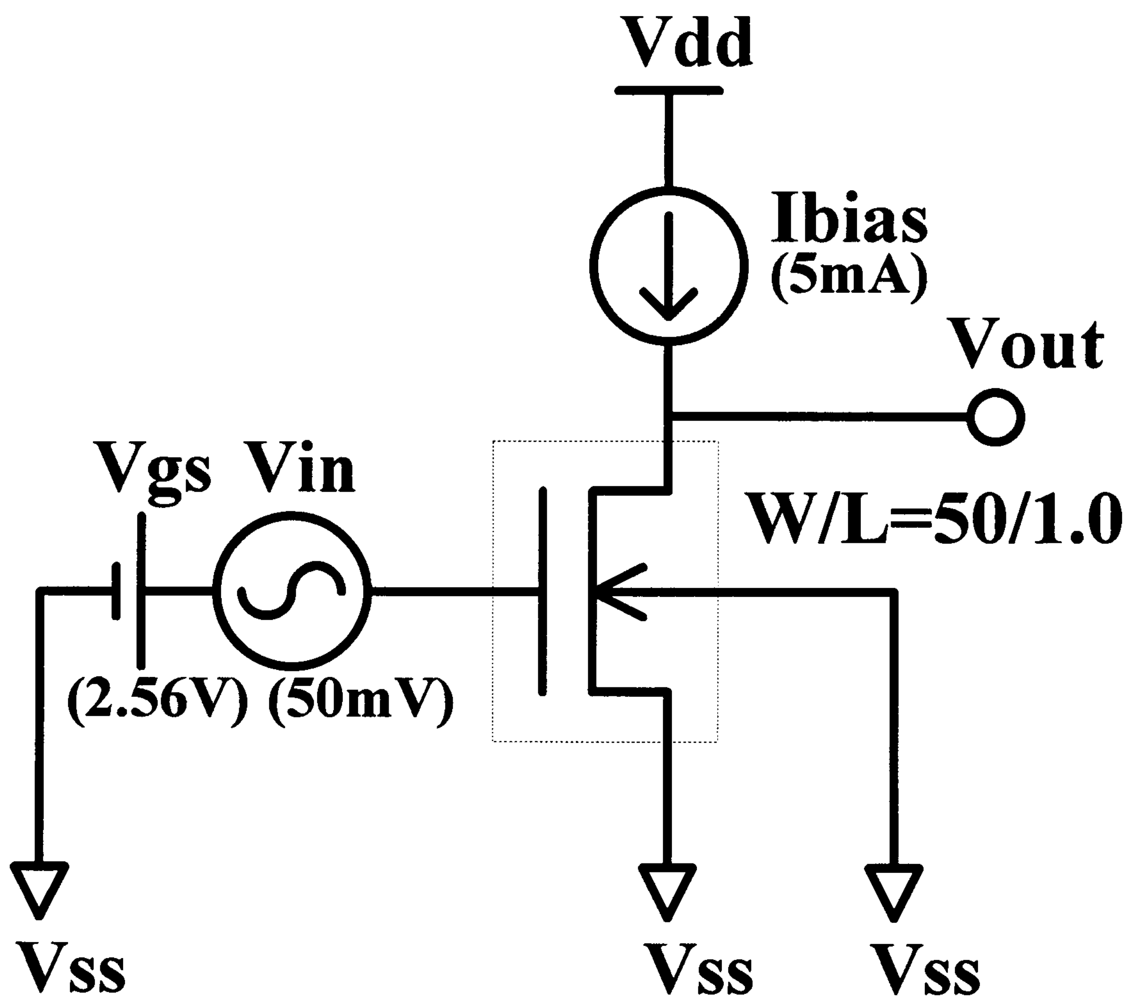


Figure 5-3 Circuit diagram of a single nMOSFET amplifier.

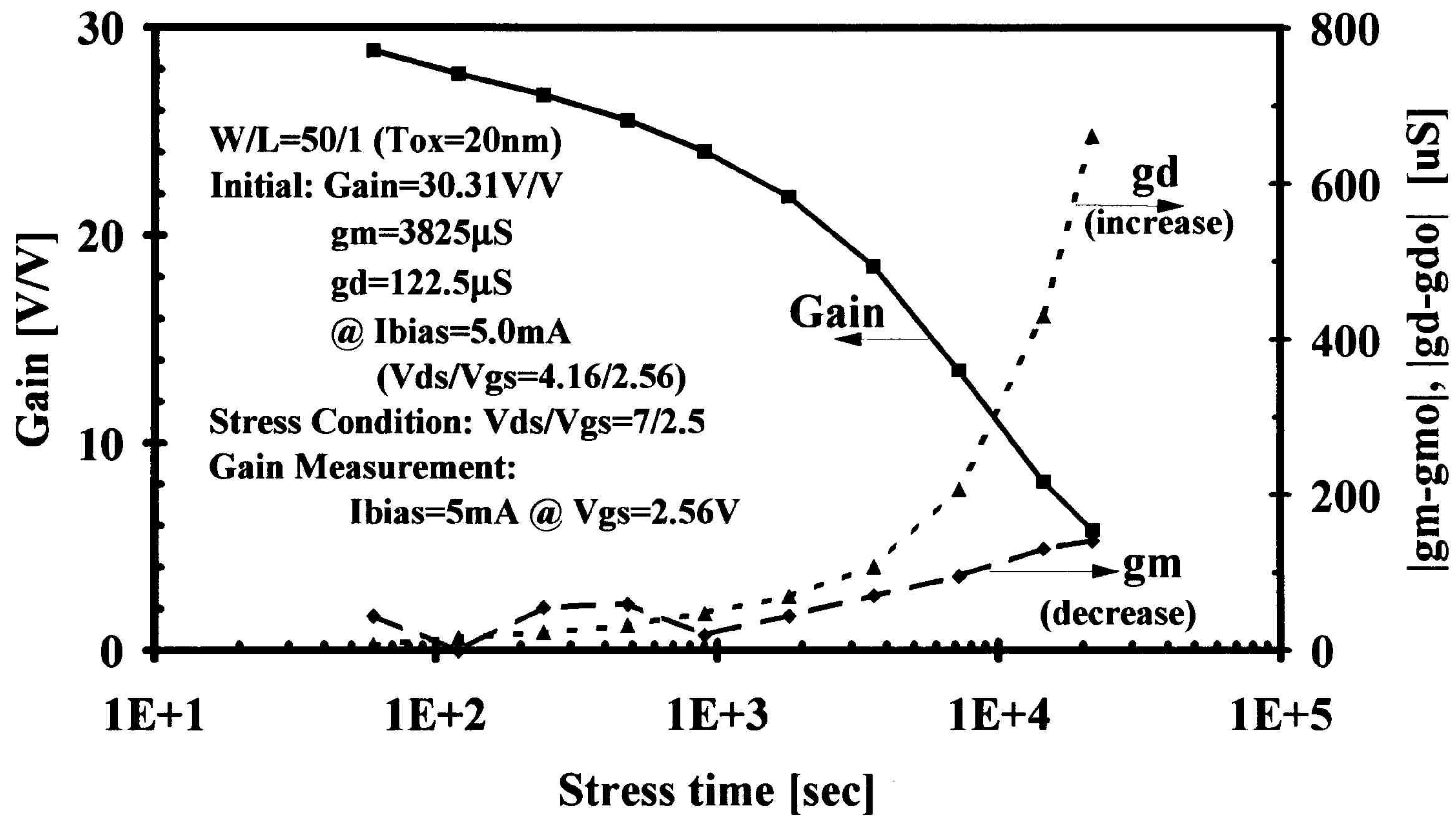


Figure 5-4 Gain degradation of a single nMOSFET amplifier as a function of stress time.

are measured at the operating point in saturation region. To investigate the degradation of the gain, gm and gd at the operating point (Ibias=5mA with Vgs=2.56V) were also measured, and the shifts of gm and gd were also plotted in Fig. 5-4. The shift of gm in saturation region was very small (a few %). On the other hand, gd increased with stress time and gd after 10^4 sec stressing was about twice the initial value of gd. Therefore, the main cause of gain degradation was the gd increase due to hot carrier injection. In conventional amplifiers, the MOSFET is operated in the saturation region, in the saturation region, gm degradation is less than that in the linear region because the depletion layer at the drain shields the region damaged by hot carrier injection and the effective mobility reduction by the damaged region is smaller than that in the linear region. However, gd in the saturation region is sensitive to hot carrier degradation because the pinch-off point is swept across the damaged region and the effective mobility is changed by the pinch-off point. To predict the lifetime of an amplifier, it is obvious that the gd degradation model is more important than the gm degradation model.

In section 5.2, the relationship between gd in the saturation region and gm in the linear region was given by Eq. (5-17). To confirm this equation, the relationships between (gd-gdo)/gd and (gmo-gm)/gm have been plotted for Ldrawn=1.0μm and 2.0μm nMOSFET's as shown in Fig. 5-5. In Fig. 5-5, a good linear relationship is obtained between (gd-gdo)/gd and (gmo-gm)/gm. The slope for the 2.0μm nMOSFET is larger than that of the 1.0μm nMOSFET. This Leff dependence is also expected by Eq. (5-17). The gd degradation of the longer channel length device is larger for a given gm degradation. This channel length dependence is discussed in the following section.

Figure 5-6 shows the gd change of a Ldrawn=1.0μm nMOSFET with stress time and also the gd change calculated from gm degradation data. It is well known that (gmo-gm)/gmo shows a power law relationship [131], that is

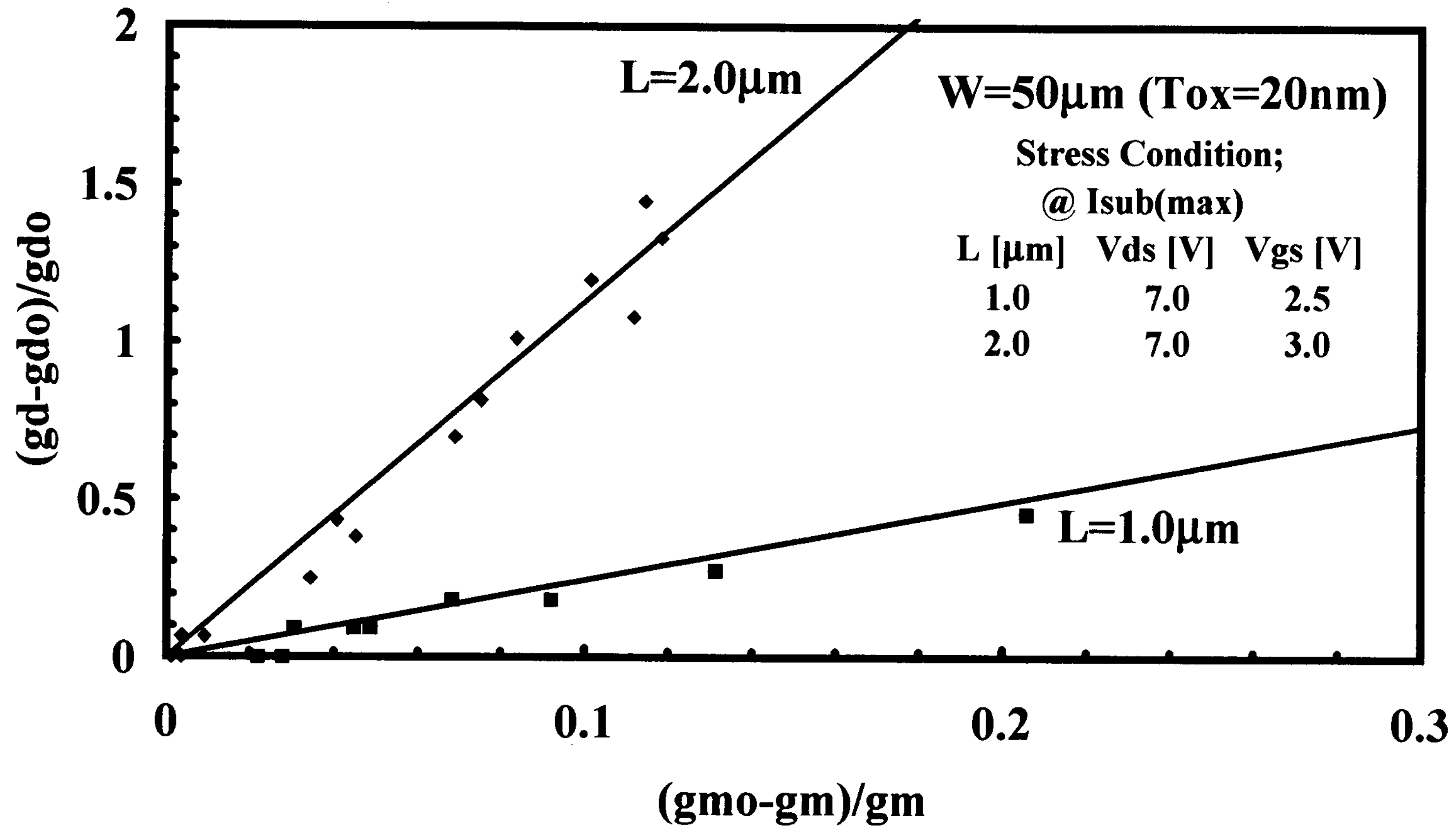


Figure 5-5 Relationship between Δgm/gm and Δgd/gdo for L=1.0μm and 2.0μm.

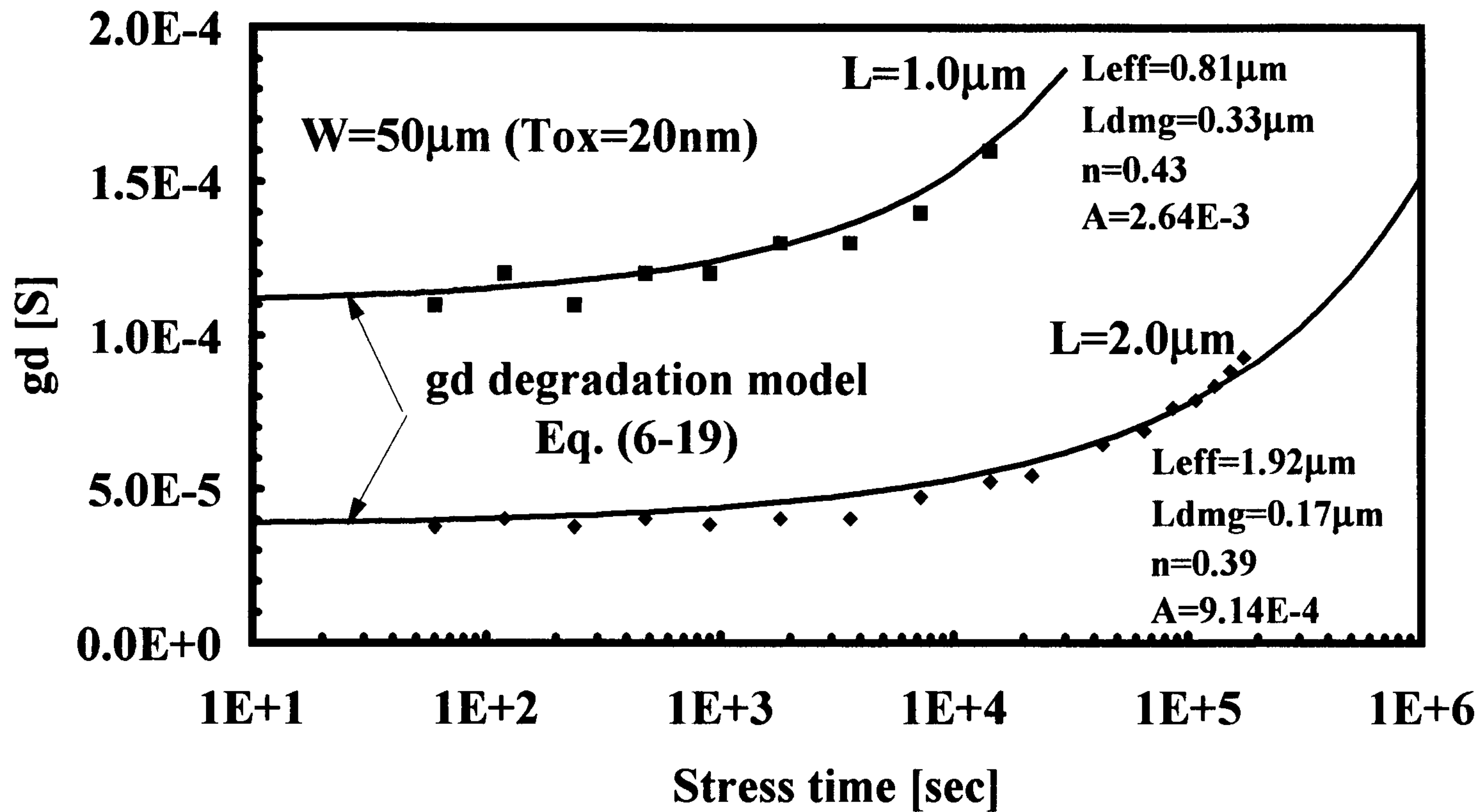


Figure 5-6 Comparison between drain conductance model and experimental data as a function of stress time.

$$\frac{gm_o - gm}{gm_o} = A \cdot t^n \tag{5-18}$$

Substituting Eq. (5-18) into Eq. (5-17) yields

$$gd = gd_o \cdot (1 + \frac{Leff}{Ldmg} \cdot \frac{A \cdot t^n}{1 - A \cdot t^n}) \tag{5-19}$$

If A, n and Ldmg are known, gd can be calculated by using Eq. (5-19). In Fig. 5-6, the measured and calculated gd values are also shown for a Ldrawn=2.0μm nMOSFET as a function of stress time. For the both Ldrawn=1.0μm and 2.0μm, the calculated value of gd matches the measured value of gd.

Figure 5-7 shows the Vds dependence of the 10% gm degradation lifetime (τ gm) and the 50% gd degradation lifetime (τgd) for both Ldrawn=1.0μm and Ldrawn=2.0μm nMOSFET's. When Ldrawn=1.0μm, τgd is longer than τgm. On the other hand, τgd is shorter than τgm when Ldrawn=1.0μm. This phenomenon can be explained by Eq. (5-17). The Leff dependence of τgm is expressed by [131]

$$\log(\tau gm) = C_1/Leff + C_2 \tag{5-20}$$

where C_1 and C_2 are constants. Using Eq. (5-18), τgm can also be written as

$$A \cdot \tau gm^n = \frac{gm_o - gm}{gm_o} = 0.1 \tag{5-21}$$

By substituting (gd-gdo)/gdo=0.5 into Eq. (5-19), τgd is then expressed by

$$\tau gd = (\frac{Ldmg}{A \cdot (2 \cdot Leff + Ldmg)})^{1/n} \tag{5-22}$$

Using Eqs. (5-20)-(5-22), finally τgd becomes

$$\log(\tau gd) = \frac{C_1}{Leff} + C_2 + \frac{1}{n} \cdot \{\log(\frac{Ldmg}{2 \cdot Leff + Ldmg}) + 1\} \tag{5-23}$$

In Eq. (5-23), if C_1, C_2, n, and Ldmg are known, τgd can be calculated. Fig. 5-8 shows the Leff dependence of τgm and τgd. In this figure, the regression line of τgm and

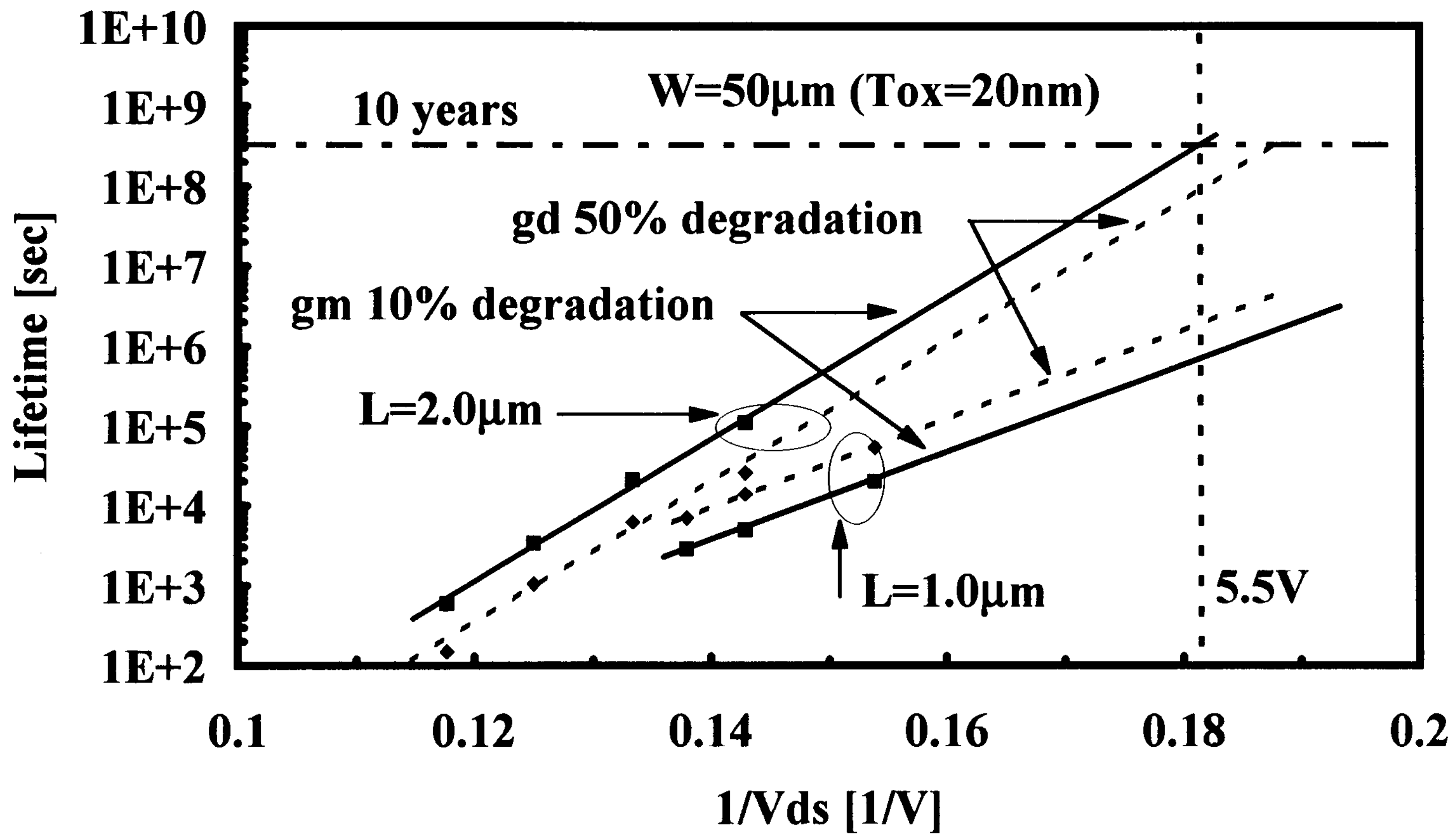


Figure 5-7 Lifetime dependence on 1/Vds.

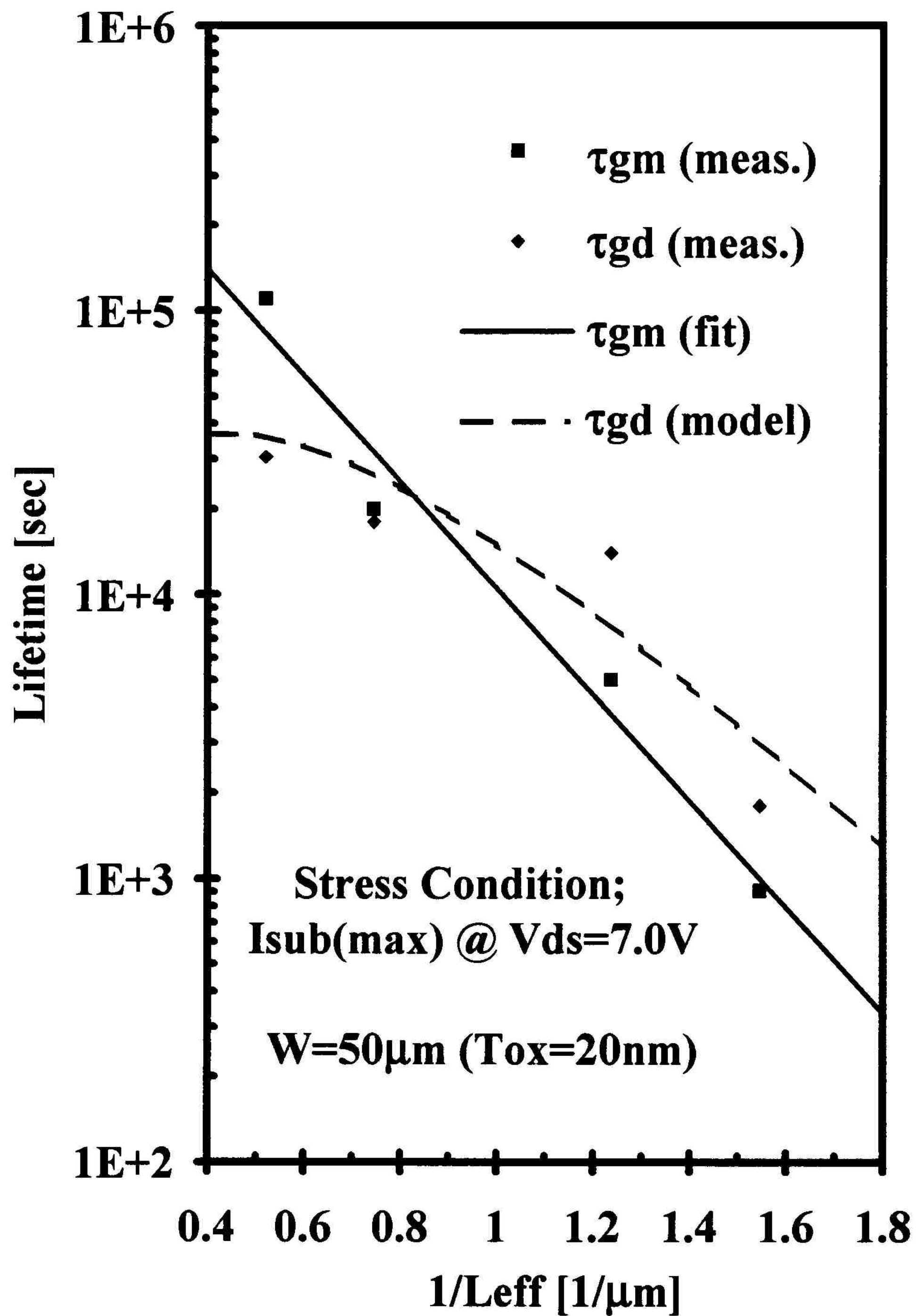


Figure 5-8 Channel length dependence of τgm and τgd.

calculated τgd are also shown. In the calculation of τgd, C_1 and C_2 were extracted from the log(τgm) versus 1/Leff relationship and n≅0.5 [131]. Ldmg was also assumed to be 0.27μm. It was found that the Leff dependence of τgd is smaller than that of τgm and τgd is shorter than τgm when Leff is longer than 1.2μm. This means that we should pay particular attention to the device reliability when longer gate length MOSFET's are used in analog circuits. Usually τgm is used as the lifetime of the devices, which is not correct.

Substrate current is the best monitor of MOSFET degradation due to hot carrier injection because log(τgm) has a good linear relationship to log(Isub) as shown in Fig. 5-9 [131]. The gm degradation lifetime, τgm, of devices can be predicted when Isub of the devices is known. From this point of view, the relationship between Isub and the gd degradation lifetime, τgd, must be clarified.

Upon considering the relationship between log(τgm) and log(Isub), it was found that

$$\log(\tau gm) = C_3 . \log(Isub) + C_4 \qquad (5\text{-}24)$$

where C_3 and C_4 are constants. From Eqs. (5-21), (5-22) and (5-24), the relationship for τgd becomes

$$\log(\tau gd) = C_3 \cdot \log(Isub) + C_4 + \frac{1}{n} \cdot \{\log(\frac{Ldmg}{2 \cdot Leff + Ldmg}) + 1\} \qquad (5\text{-}25)$$

Therefore, the slope of log(τgd) and log(Isub) is the same as that of log(τgm) and log(Isub). Only the y-intersect of log(τgd) and log(Isub) is different than that of log(τ gm) and log(Isub). The intersect depends on Leff and Ldmg. The measured data of Isub versus τgd is shown in Fig. 5-10 including the calculated curve which uses n=0.5, Ldmg=0.27μm, this calculated curve fits the measurement data well.

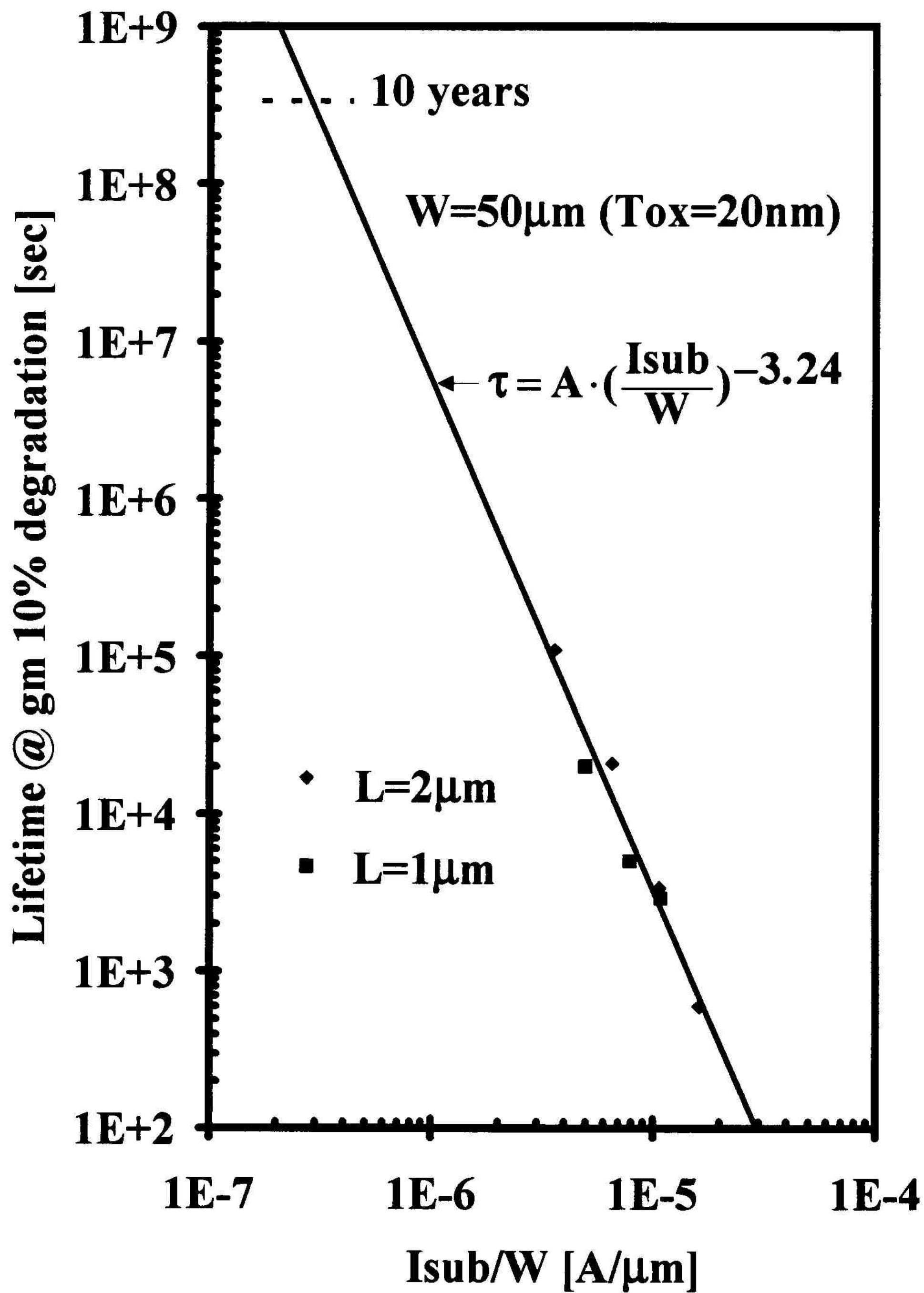


Figure 5-9 Lifetime projection of gm degradation.

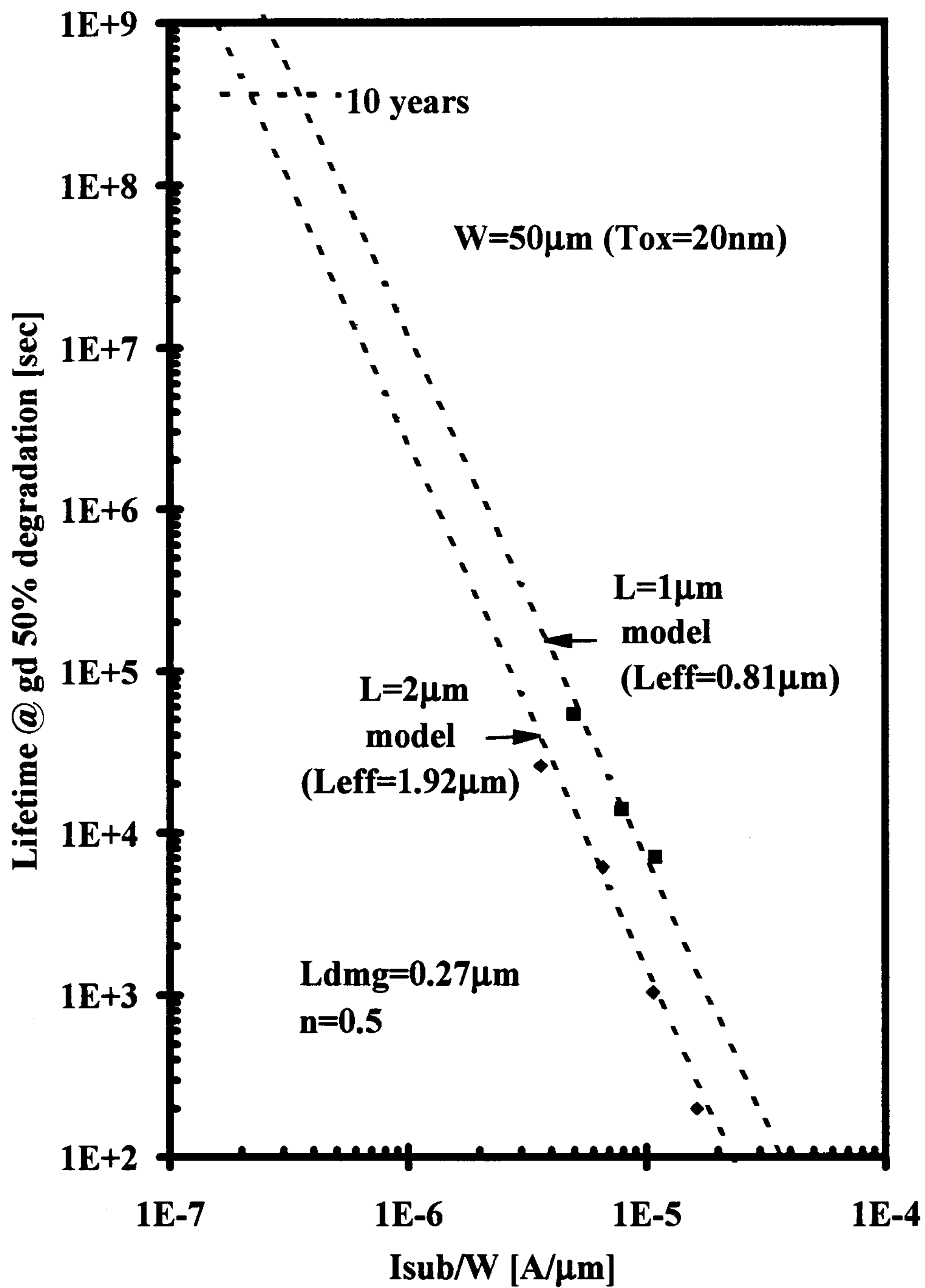


Figure 5-10 Lifetime projection of gd degradation.

5.4 Summary

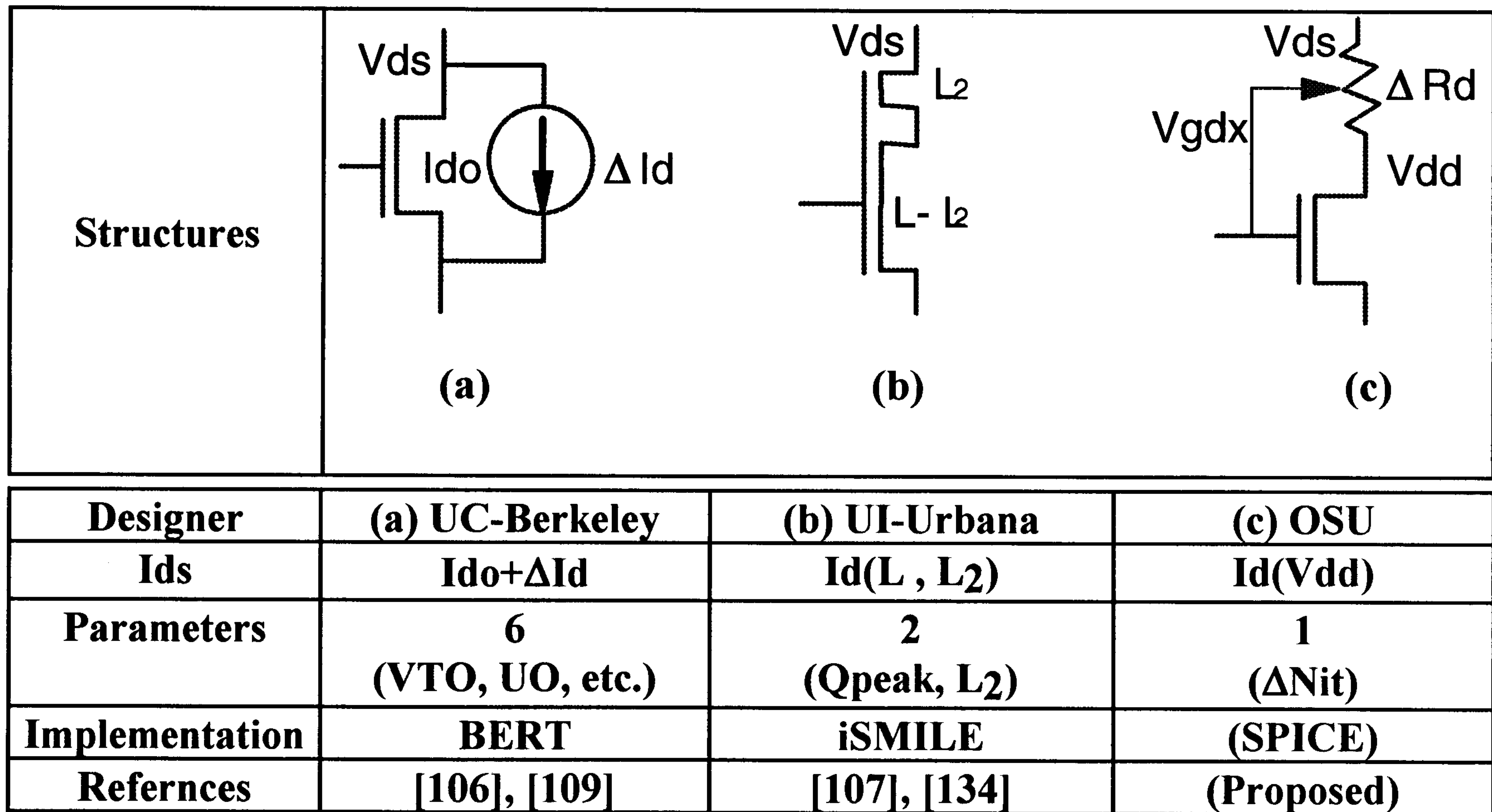
A drain conductance (gd) degradation model based on a gradual channel approximation is proposed. The gd degradation can be calculated from the linear region transconductance (gm) degradation data by using Eq. (5-17). Usually the degradation of MOSFET's due to hot carrier injection is evaluated by gm degradation. Therefore, using this model, gd degradation can also be predicted from the evaluation of conventional gm degradation data. The Leff dependence of the gd degradation lifetime has been also demonstrated by comparing measurement data and this model. The results of this gd degradation model predict that the gd degradation lifetime changes slowly with Leff and is shorter than the gm degradation lifetime when the channel length is longer than 1.2μm. This model then is particularly applicable to longer channel length devices normally used in analog circuits.

6. SERIES RESISTANCE ENHANCEMENT MODEL

6.1 Introduction

Hot-carrier induced device degradation has been known to be one of the main mechanisms affecting the lifetime and performance projections under operating conditions [7], [32], [43], [53], [127], [132]-[133]. As VLSI chip density and complexity increase, design for reliability becomes more important, scaled down devices in the sub-micron regime suffer more hot-carrier effects resulting in parameter mismatches and IC functional failures [53]. Hot-carrier induced device degradation consists of an increase of threshold voltage and decrease of channel mobility resulting in a decrease of drain current. Also, the series resistance enhancement of an nMOSFET induced by hot-carrier effects has been known to be one of possible causes of the self-limiting effects of hot-carrier degradation [32]. The increase of series resistance results in a longer access time in digital memories. Furthermore, in analog IC's, the increase of series (drain) resistance of nMOSFET's has become a major consideration in reliability projections since the increase of series resistance directly effects the output resistance of transistors [127]. However, very little consideration has been given to physical or experimental results on series resistance enhancement under hot-carrier stress [132]-[133].

Although, there have been several reliability models [106]-[107], [109], [134] as shown in Fig. 6-1 and simulators introduced (HOTRON, RELIC, BERT, RELY, CREST, RELIANT) [105], the conventional hot-carrier reliability models and simulators require a set of agetable parameters for each lifetime-window in reliability projections in order to update the input file with the stressed parameters. For instance,



Designer	(a) UC-Berkeley	(b) UI-Urbana	(c) OSU
Ids	Ido+ΔId	Id(L , L_2)	Id(Vdd)
Parameters	6 (VTO, UO, etc.)	2 (Qpeak, L_2)	1 (ΔNit)
Implementation	BERT	iSMILE	(SPICE)
Refernces	[106], [109]	[107], [134]	(Proposed)

Figure 6-1 Structures of reliability models and the proposed hot-carrier induced series (drain) resistance (ΔRd) enhancement model.

Figs. 6-1 (a) and (b) show the structures of conventional reliability models of the MOSFET. As shown in Fig. 6-1 (a), the UC-Berkeley model (implemented in BERT) [106], [109] requires a set of agetable parameters and a bi-directional voltage controlled current source (ΔId) obtained by correlating statistical forward and reverse ΔId data with stress conditions. Consequently, the parameter extraction becomes very critical to increase or manage the simulation accuracy and efficiency. Since the hot-carrier stressed device model parameters must be extracted from the individually stressed transistor, the parameter extraction is mainly limited to several device model parameters (i.e., 6 parameters in BERT) to maximize the efficiency of the reliability simulation. On the other hand, as shown in Fig. 6-1 (b), the UI-Urbana model (implemented in iSMILE) [107], [134] uses a more physically described method and requires only two process parameters (Qpeak, L_2) which must be evaluated during circuit simulations. Thus, it is rather complicated and requires some iterations with more sophisticated techniques to improve computational efficiency.

The purpose of this paper is to develop and propose a simple reliability model that minimizes the use of the process parameters to simulate the hot-carrier induced degradation of device characteristics of nMOSFET's. By adopting the fact that the increase of hot-carrier induced series resistance is due to hot-carrier injection near the drain region, the series (drain) resistance (ΔRd) can be attributed to the increase of hot-carrier induced interface trap charge (ΔNit) and emulates the mobility reduction and threshold voltage shifts. It should be pointed out that the ΔRd model is used to replicate the mobility degradation and threshold voltage shifts in circuit simulations of hot-carrier induced degradation. It does not utilize any parameter extraction scheme nor represent the physical aspects of the series and/or contact resistance such as the n^- region resistance (Rn^-) of LDD devices [132]. Once the relationship of ΔNit on hot-carrier effects is known, we are able to construct a realizable reliability model which is

simple to implement into any circuit simulator such as SPICE. Moreover, this simple technique of the series connected resistance is found to be very applicable to analog IC design since the ΔRd can be realized with a simple resistor under the normal DC biased operating conditions.

In order to show the validity of the ΔRd model for reliability projections, a conventional CMOS amplifier has been employed for reliability projections, and then, the reliability projection of the ΔRd model is compared with the aged parameter model such as in BERT. The simulation results of the CMOS Op-Amp using the ΔRd model are quite compatible with the present reliability simulator (BERT).

6.2 Derivation of the ΔRd Model

Figure 6-2 shows a schematic diagram of an nMOSFET with hot-carrier induced interface trap charge. The derivation of the ΔRd reliability model will be carried out under the assumption that mobility degradation is predominantly caused by interface generation (ΔNit) as observed by Sun et al. [130]:

$$\mu = \frac{\mu_o}{1 + \alpha \cdot \Delta Nit} \qquad (6\text{-}1)$$

where μ_o is the mobility and α is a process dependent constant (~2.4×10^{-12} cm^2, [82]). Also, all fast interface states (traps) are considered to be acceptor-like interface states occupied by electrons as in [82], [83]; namely, the net charge in interface traps is a fixed negative charge for an nMOSFET operating in strong inversion (Vgs>Vto), then the charge in the conducting channel, *Qch(y)*, is described as:

$$Qch(y) = -Cox \cdot (Vgs - Vto - \frac{q \cdot \Delta Nit}{Cox} - Vch(y)) \qquad (6\text{-}2)$$

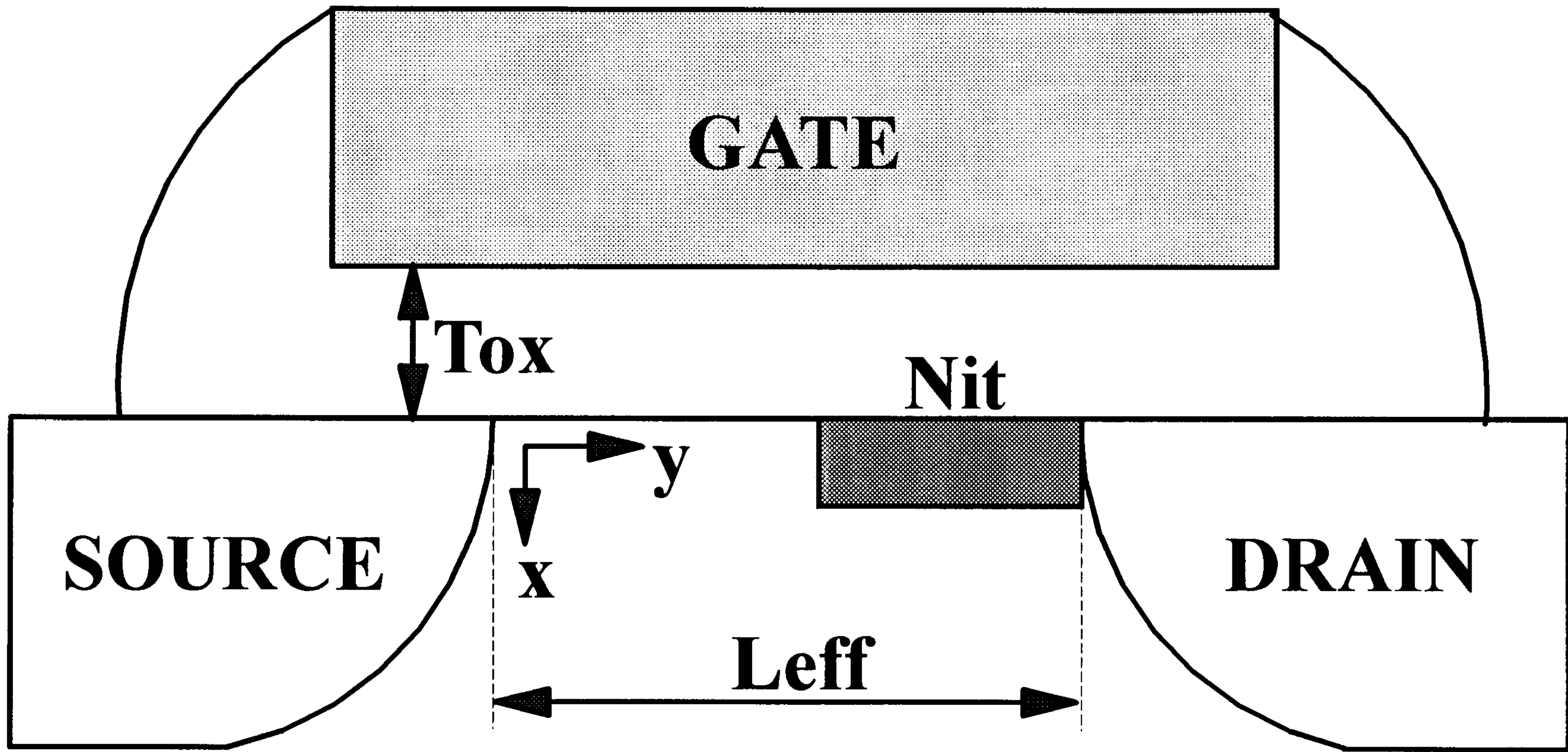


Figure 6-2 Schematic illustration of the device structure for the ΔRd model derivation and the hot-carrier induced interface trap charge.

where Cox is the gate oxide capacitance per unit area, Vgs is the gate-to-source voltage, Vto is the threshold voltage, Vch(y) is the potential along the channel, and q is the electron charge (1.6×10^{-19}C). Notice that, as the hot-carrier induced interface trap charge increases, the channel becomes more negatively charged resulting in an increase of the threshold voltage.

By applying the gradual channel approximation (GCA) and accounting for the mobility degradation from the hot-carrier induced interface trap charge, the hot-carrier induced degradation of the drain current, Ids(ΔNit), is obtained as [129]:

$$Ids(\Delta Nit) = \frac{\mu_o}{1+\alpha\cdot\Delta Nit}\cdot Cox\cdot\frac{Weff}{Leff}\cdot\left(Vgs - Vto - \frac{q\cdot\Delta Nit}{Cox} - \frac{Vds}{2}\right)\cdot Vds \quad (6\text{-}3)$$

where Weff is the effective channel width, Leff is the effective channel length, and Vds is the drain-to-source voltage. The hot-carrier induced drain current reduction (ΔIds) is then given by

$$\Delta Ids = Ids_O - Ids(\Delta Nit) = \frac{\alpha\cdot\Delta Nit}{1+\alpha\cdot\Delta Nit}\cdot Ids_O + \frac{\mu_O}{1+\alpha\cdot\Delta Nit}\cdot\frac{Weff}{Leff}\cdot Vds\cdot q\cdot\Delta Nit$$

$$= \frac{\alpha\cdot\Delta Nit}{1+\alpha\cdot\Delta Nit}\cdot Ids_o + \frac{q\cdot\Delta Nit}{1+\alpha\cdot\Delta Nit}\cdot\frac{Ids_o}{Cox\cdot(Vgs - Vto - \frac{Vds}{2})} \quad (6\text{-}4)$$

where Ids_O is the unstressed drain current (ΔNit=0 @ t=0) which is:

$$Ids_O = \mu_O\cdot Cox\cdot\frac{Weff}{Leff}\cdot(Vgs - Vto - \frac{Vds}{2})\cdot Vds \quad (6\text{-}5).$$

Consequently, Eq. (6-4) is described by [F14]

$$\Delta Ids \approx \frac{\alpha\cdot\Delta Nit}{1+\alpha\cdot\Delta Nit}\cdot Ids_o \quad (6\text{-}6\text{ (a)}),$$

$$Ids(\Delta Nit) = Ids_O - \Delta Ids = \frac{Ids_O}{1+\alpha\cdot\Delta Nit} \quad (6\text{-}6\text{ (b)})$$

Although Eqs. (6-6 (a)) and (6-6 (b)) has been empirically derived by using the linear region drain current degradation, we have found and confirmed that Eqs. (6-6 (a)) and (6-6 (b)) are still valid in saturation region as long as α can be modified with operating conditions [82].

Using the ΔRd connected in series with the unstressed device as shown in Fig. 6-1 (c), the drain current of the ΔRd reliability model, *Ids(ΔRd)*, is given by

$$Ids(\Delta Rd) = \mu_o \cdot Cox \cdot \frac{Weff}{Leff} \cdot (Vgs - Vto - \frac{Vds - V_{Rd}}{2}) \cdot (Vds - V_{Rd}), \quad (6\text{-}7)$$

where $V_{Rd} = \Delta Rd \cdot Ids(\Delta Rd)$.

Combining Eqs. (6-3) and (6-7), and then solving for V_{Rd} (= Ids·ΔRd) yields:

$$V_{Rd}^2 + 2 \cdot (Vgs - Vto - Vds) \cdot V_{Rd} - 2 \cdot Vds \cdot [\frac{q \cdot \Delta Nit}{Cox} + \frac{\alpha \cdot \Delta Nit}{1 + \alpha \cdot \Delta Nit} \cdot (Vgs - Vto - \frac{Vds}{2})] = 0 \quad (6\text{-}8),$$

and then, the V_{Rd} is obtained as

$$V_{Rd} = -Vgdx + \sqrt{Vgdx^2 + 2 \cdot Vds \cdot \{\frac{\alpha \cdot \Delta Nit}{1 + \alpha \cdot \Delta Nit} \cdot (Vgdx + \frac{Vds}{2}) + \frac{q \cdot \Delta Nit}{Cox}\}} \quad (6\text{-}9),$$

where $Vgdx = Vgs - Vto - Vds$, and in saturation region ($Vds \geq Vgs - Vto$), $Vgdx = 0$.

Using Eq. (6-6 (b)) for Ids(ΔRd), then ΔRd is given by:

$$\Delta Rd = \frac{1 + \alpha \cdot \Delta Nit}{Ids_o} \cdot [-Vgdx + \sqrt{Vgdx^2 + 2 \cdot Vds \cdot \{\frac{\alpha \cdot \Delta Nit}{1 + \alpha \cdot \Delta Nit} \cdot (Vgdx + \frac{Vds}{2}) + \frac{q \cdot \Delta Nit}{Cox}\}}] \quad (6\text{-}10).$$

As shown in Eq. (6-10), the ΔRd reliability model is represented by the ΔRd connected in series with a fresh n-MOSFET which is easily realizable. Hence, the operation of the degraded nMOSFET is emulated by the fresh device with a variable voltage source (Vdd) which is controlled by ΔRd which is a function of the applied voltages (Vgs and Vds) and the hot-carrier induced interface trap charge (or operation time). With this simple realization technique, the proposed ΔRd reliability model is

capable of representing the hot-carrier induced degradation of nMOSFET's and reliability projections in IC design. The main advantage of the ΔRd reliability model is that the ΔRd requires only one parameter (ΔNit) to simulate hot-carrier induced device degradation, and these ΔNit projections have been developed by several research groups [29], [85]-[87]. Therefore, the proposed ΔRd reliability model can be easily adopted into VLSI/ULSI circuit design since the implementation of the new ΔRd model is much simpler and more efficient. This ΔRd reliability model is most applicable for reliability projections in analog IC design where the device under the most severe hot-carrier effects can be represented by ΔRd under operating conditions, and then the ΔRd can be used to determine the maximum hot-carrier induced interface trap charge (density) allowed and/or the corresponding maximum operating time (lifetime).

6.3 Experimental and Simulation Results

The nMOSFET's used in this work were fabricated by two different foundry processes: MOSIS-HP-CMOS34 (W/L=50/1, Tox=20nm) and MOSIS-HP-CMOS26B (W/L=20/1, Tox=16nm). The experimental setup for the hot-carrier stress and analysis is illustrated in Fig. 6-3 which includes the charge-pumping current (Icp) measurements. The data on device characteristics was monitored by a HP-IB controllable PC with a custom program for hot-carrier stress and device characterization which included SPICE parameter extraction. Fig. 6-4 shows the hot-carrier induced device degradation of the drain current (Vds/Vgs=0.1V/3.0V) and the charge pumping current. The charge pumping currents were measured at each pre-determined time period using a triangular gate voltage waveform with a frequency of 1MHz while the source and drain were grounded. The gate bias was shifted from -2 to

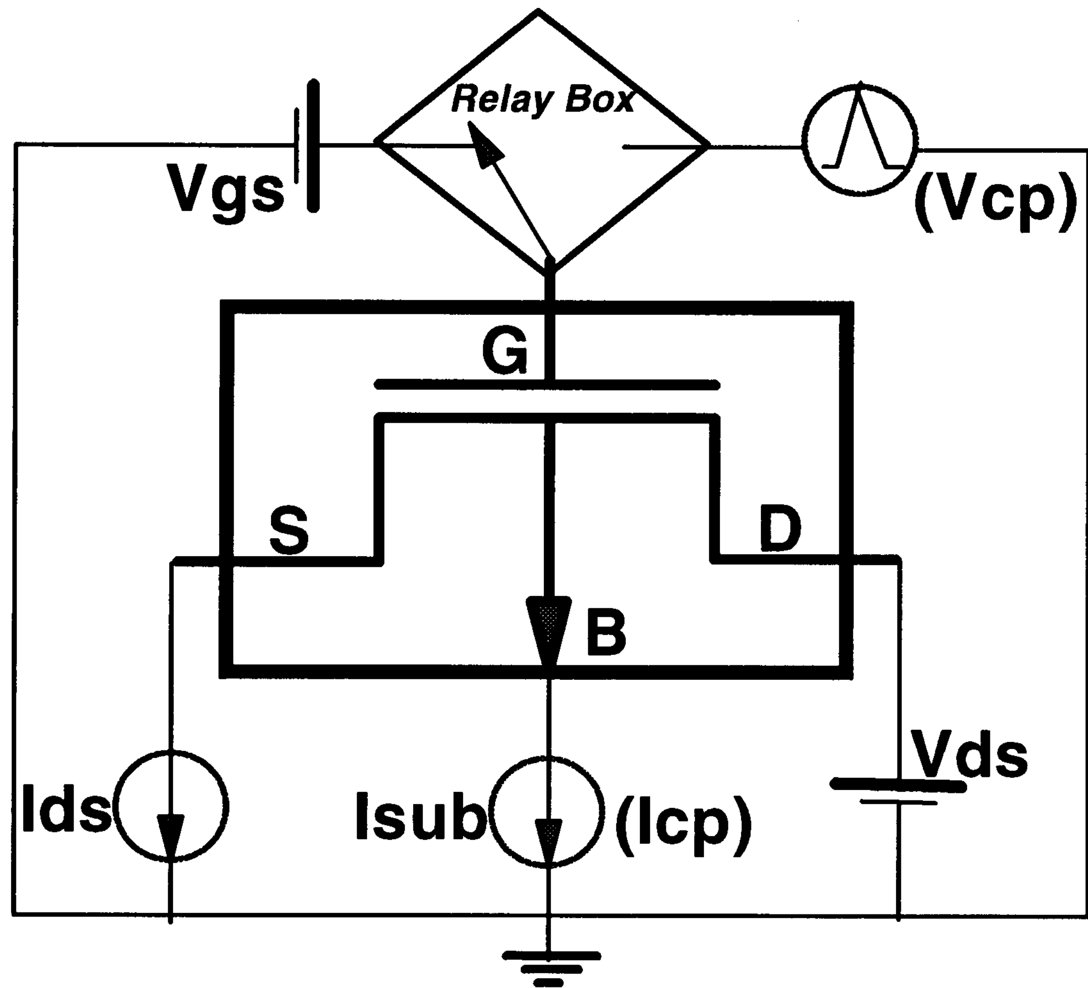


Figure 6-3 Experimenat setup for the hot-carrier stress and device characterization which includes charge pumping current measurements.

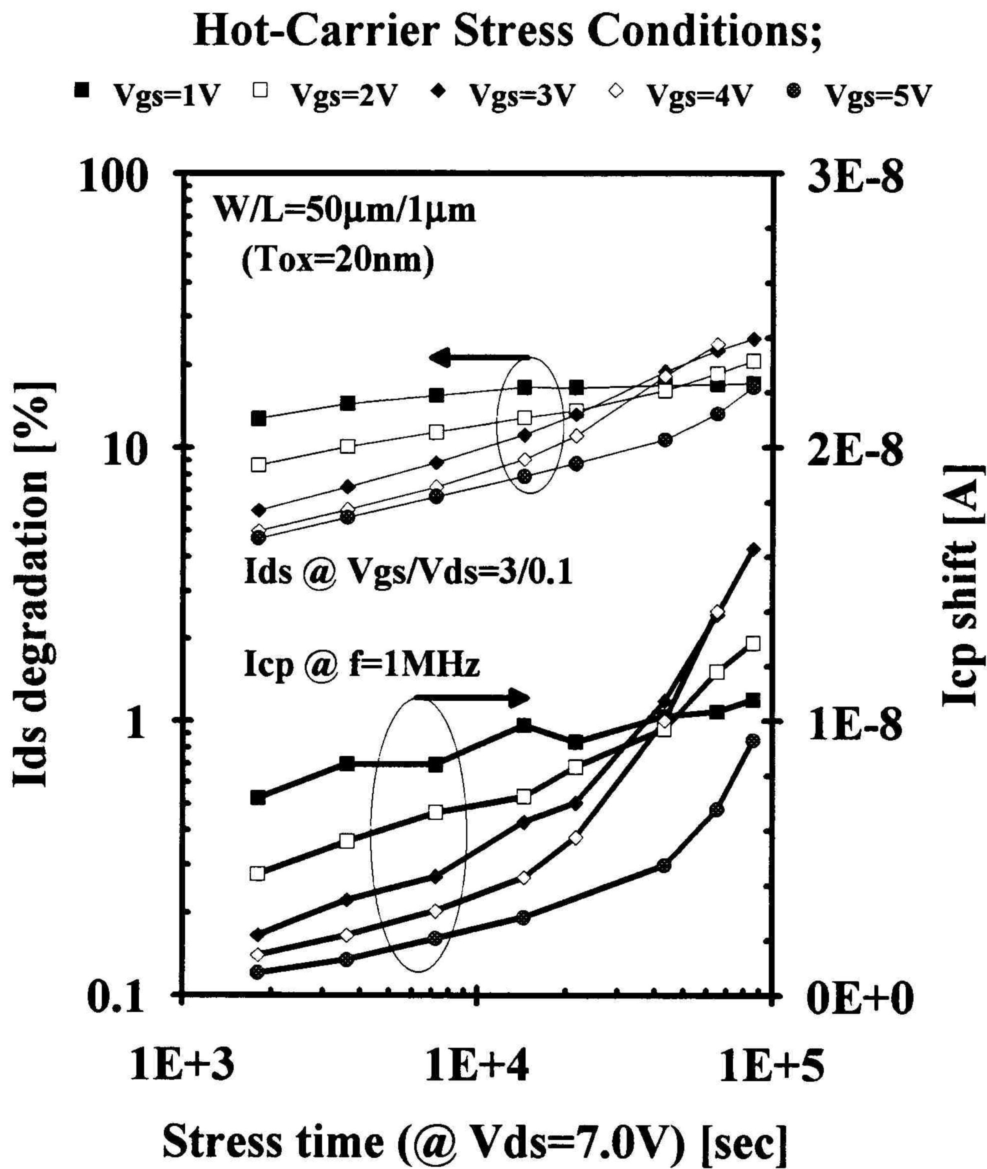


Figure 6-4 Linear region drain current degradation and charge pumping current shifts as a function of stress time.

2V during which the channel was swept from accumulation to inversion without any measurement induced degradation. The increase of the hot-carrier induced interface trap charge (ΔNit) with stress time under the stress conditions was measured by monitoring the increase of Icp which is given by [88]-[89],

$$\Delta Icp = q \cdot f \cdot A \cdot \Delta Nit \tag{6-11}$$

where f is the frequency of the gate voltage waveform, and A is the channel area (i.e., $A = Weff \times Leff$). Hence the ΔNit is directly proportional to ΔIcp. By monitoring the ΔIcp and ΔIds, then α was determined from the slope of ΔNit versus ΔIds/Ids(ΔNit) as described by Eq. (6-6 (b)) and as illustrated in Fig. 6-5 where α is about 1.44×10^{-12} [cm^2]. This is close to the empirical value of K by Chung et. al. [82] which is 2.4×10^{-12} [cm^2]. Also, it should be noted that the value of α found in Fig. 6-5 is valid over a wide range of stress gate voltages (Vgs=1V~5V), so that the proposed ΔRd reliability model is capable of circuit simulations of hot-carrier induced degradation in terms of ΔNit along with stress (operation) time.

Figure 6-6 shows experimental data of the linear region drain current characteristics and the SPICE simulation results of the ΔRd model. The linear region characteristics were obtained at Vds=0.1V and Vds=0.05V after hot-carrier stress at Vds/Vgs=7.0V/2.0V for t=1080 min. The experimental data which is in marks and the simulation results which are the solid lines correspond to ΔRd described by Eq. (6-10). The value of ΔRd obtained varies from 38Ω to 12Ω as the gate voltage increases from 0V to 5V, respectively. Also, Fig. 6-7 (a) shows the Id-Vd characteristics of the hot-carrier induced degradation of the nMOSFET and the simulated characteristics obtained by using the ΔRd reliability model. The simulated values of ΔRd over the various gate voltages is shown in Fig. 6-7 (b). The simulation results from the ΔRd

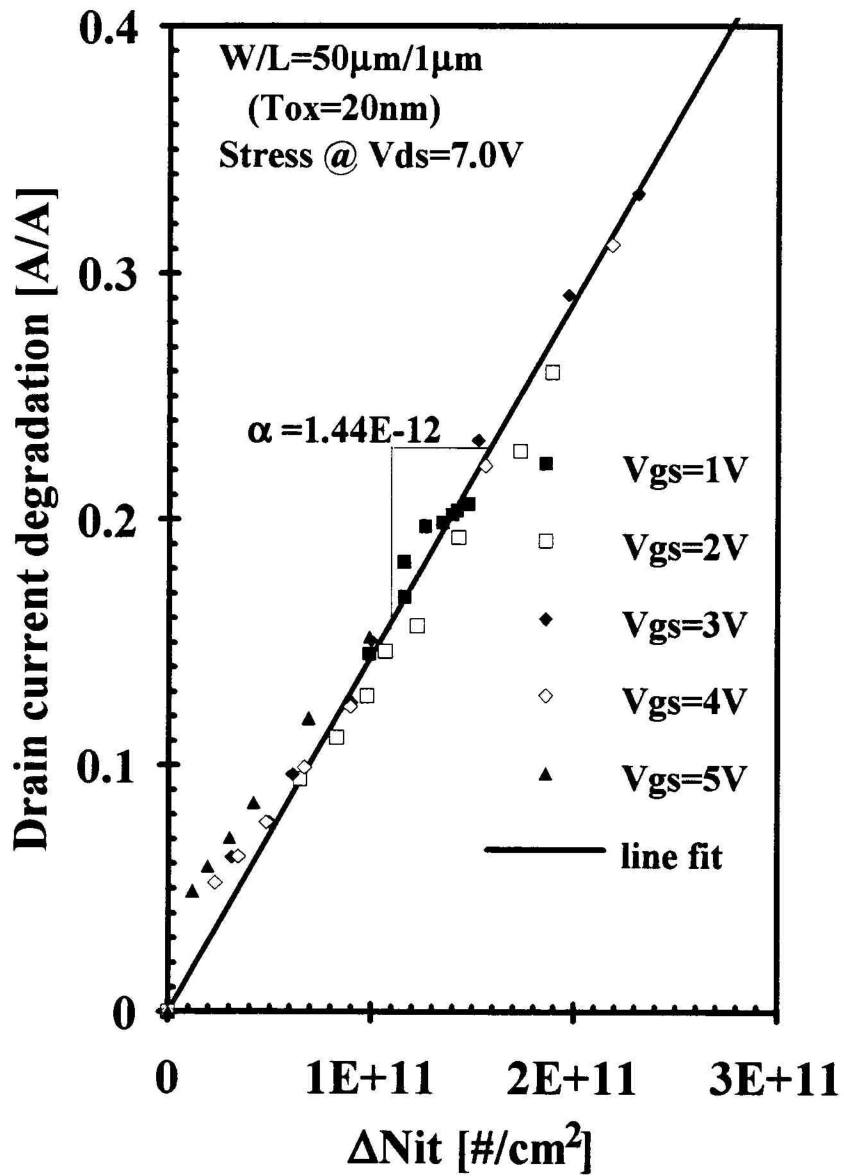


Figure 6-5 Correlation between the hot-carrier induced interface trap density and the linear region drain current degradation.

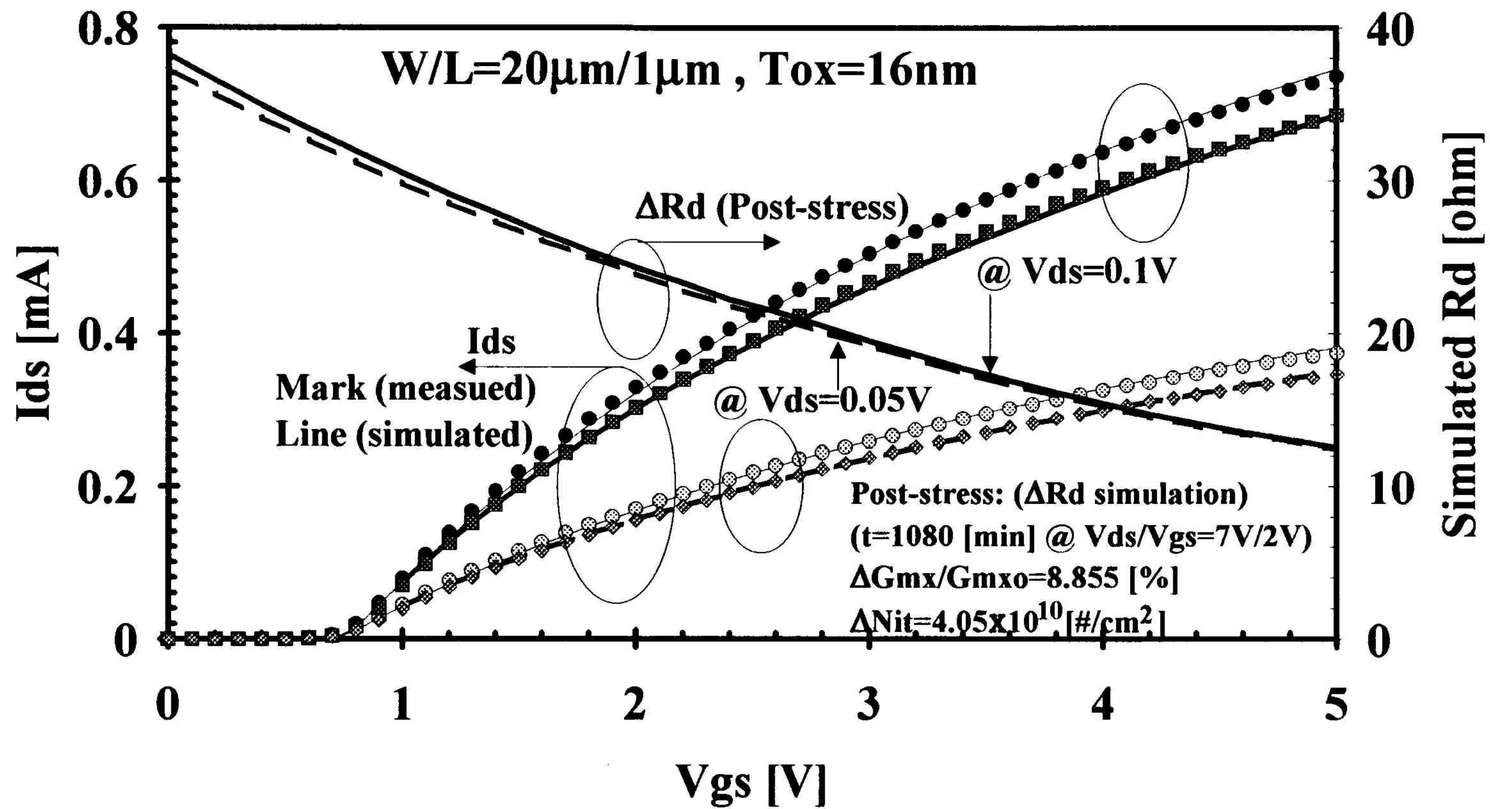


Figure 6-6 Id-Vg characteristics of the hot-carrier induced drain current degradation and the simulation results of the ΔRd model.

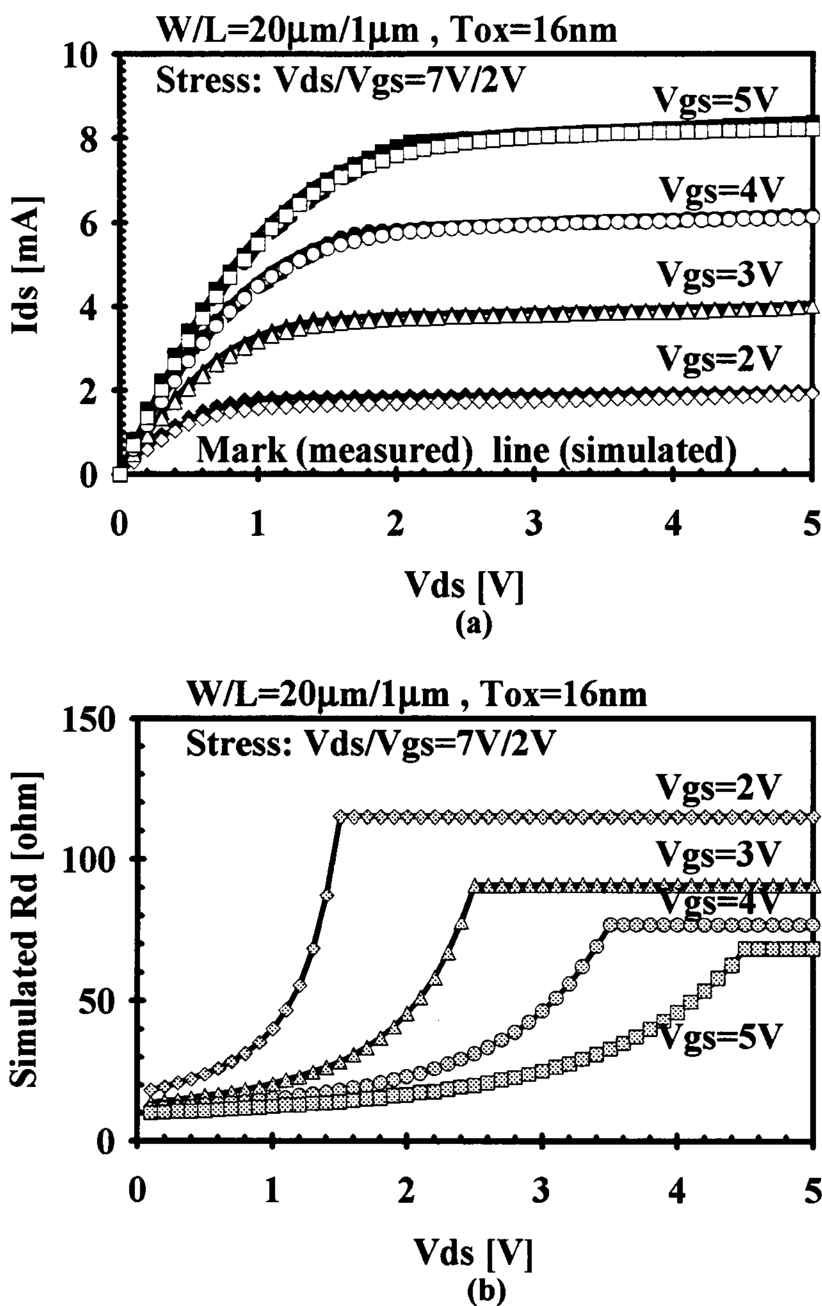
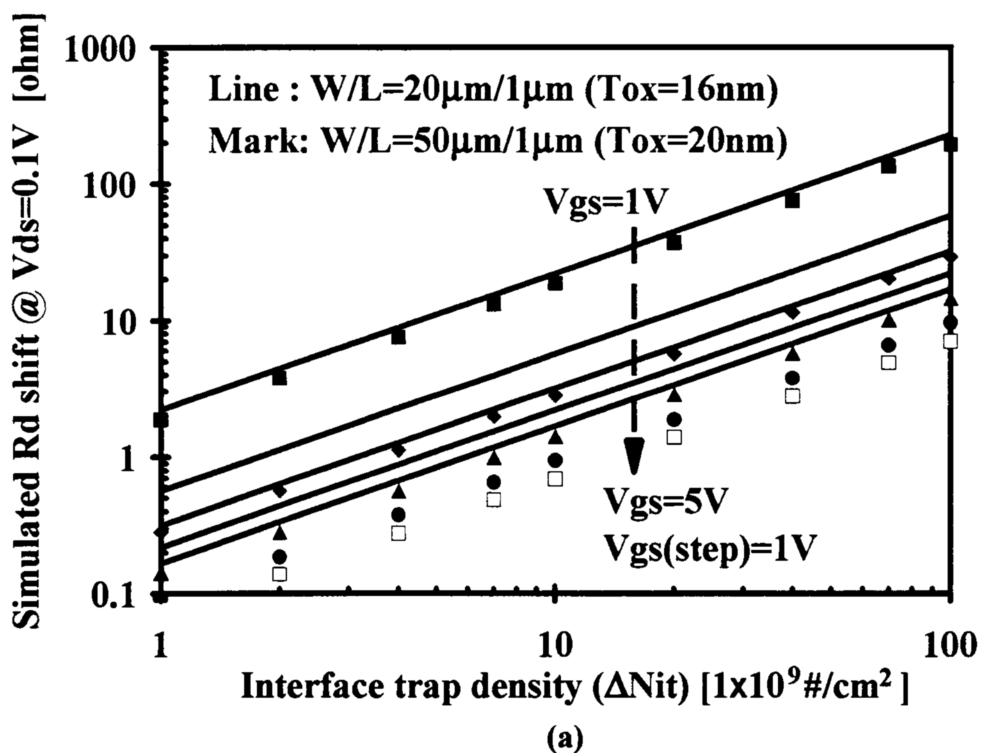


Figure 6-7 Hot-carrier induced drain current degradation and the simulation results of the ΔRd model; (a) Id-Vd characteristics and (b) the simulation results of ΔRd.

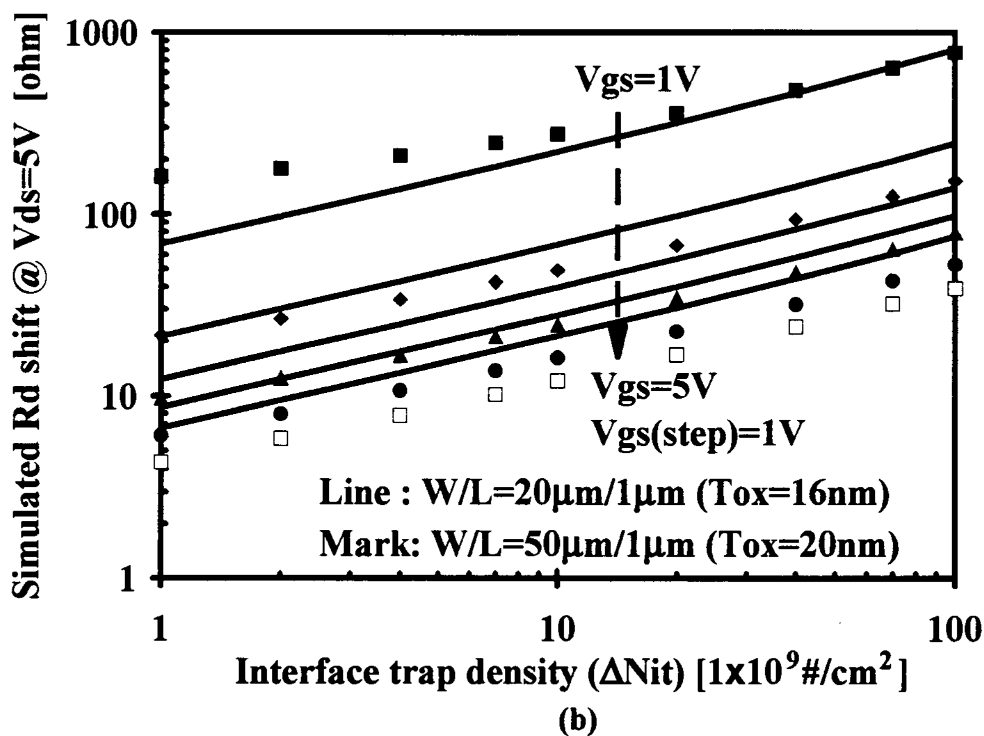
reliability model are in a good agreement with the experimental data on the hot-carrier induced degradation of the nMOSFET regardless of the drain voltages.

Figure 6-8 shows the simulation results of the projected ΔRd from two different processes as a function of the ΔNit which increases with stress time. Fig. 6-8 (a) represents ΔRd in the linear region ΔRd while ΔRd in the saturation region is in Fig. 6-8 (b). The ΔRd model is, thus, quite suitable for reliability projections in IC design since the hot-carrier induced degradation can be specified by setting only one parameter (ΔNit) in the ΔRd reliability model. Furthermore, as shown in Fig. 6-8, the main feature of the ΔRd model is the simplicity in application in IC design. More specifically, the concept of the series connection of a constant resistance can easily represent the hot-carrier induced degradation of the nMOSFET in analog IC design where we can identify the degree of hot-carrier effects under the DC biased operating conditions.

In order to show validity of the ΔRd model for reliability projections, the performance of a conventional CMOS Op-Amp [135] has been simulated and compared to the simulations of an aged parameter method such as in BERT. A schematic diagram of the Op-Amp (L=1μm) is shown in Fig. 6-9. It consists of two gain stages whose total gain was adjusted to 40dB by optimizing Vbias, the corner frequency is about 70 MHz. A buffer stage (MP8 and MP9) is added for the feedback compensation (Cfb). In this circuit configuration, MN7 of the Op-Amp is the main concern in hot-carrier effects as shown in Fig. 6-9. Therefore, it is most appropriate to include ΔRd in this MN7 model which operates under DC conditions. The appropriate values of ΔRd have been projected as shown in Fig. 6-10. The increase of ΔRd has been plotted as well as the increase of interface trap charge as a function of the operation time under the hot-carrier effects of the operating condition. In the ΔRd reliability model the only change is a series resistance added to MN7, the BERT model requires a set of degraded SPICE parameters (Vto, γ, μ_o, θ, V_{max}, κ) for MN7, MP2,

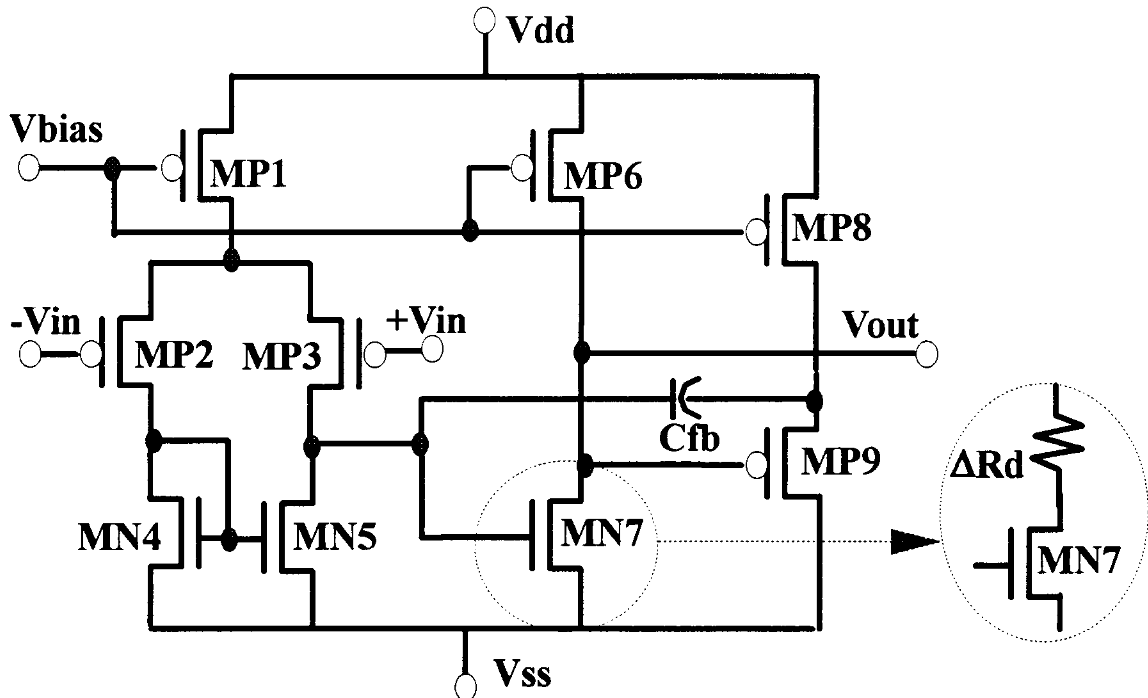


(a)



(b)

Figure 6-8 The ΔRd simulations as a function of hot-carrier induced interface trap density (a) in the linear region and (b) in the saturation region.



L=1μm	W [μm]	Vgs [V]	Vds [V]
MP1	15	4.10	2.52
MP2 *	15	2.48	5.82
MP3 *	15	2.48	5.82
MN4	15	1.66	1.66
MN5	15	1.66	1.66
MP6	30	4.10	4.96
MN7 ***	60	1.66	5.04
MP8	15	4.10	3.09
MP9 **	80	1.87	6.91

The * mark indicates a degree of hot-carrier effects under the operating condition. (i.e., * is for "HOT", ** for "HOTTER", and *** for "HOTTEST.")

Figure 6-9 Circuit diagram of a conventional CMOS Op-Amp and the application of the ΔRd model.

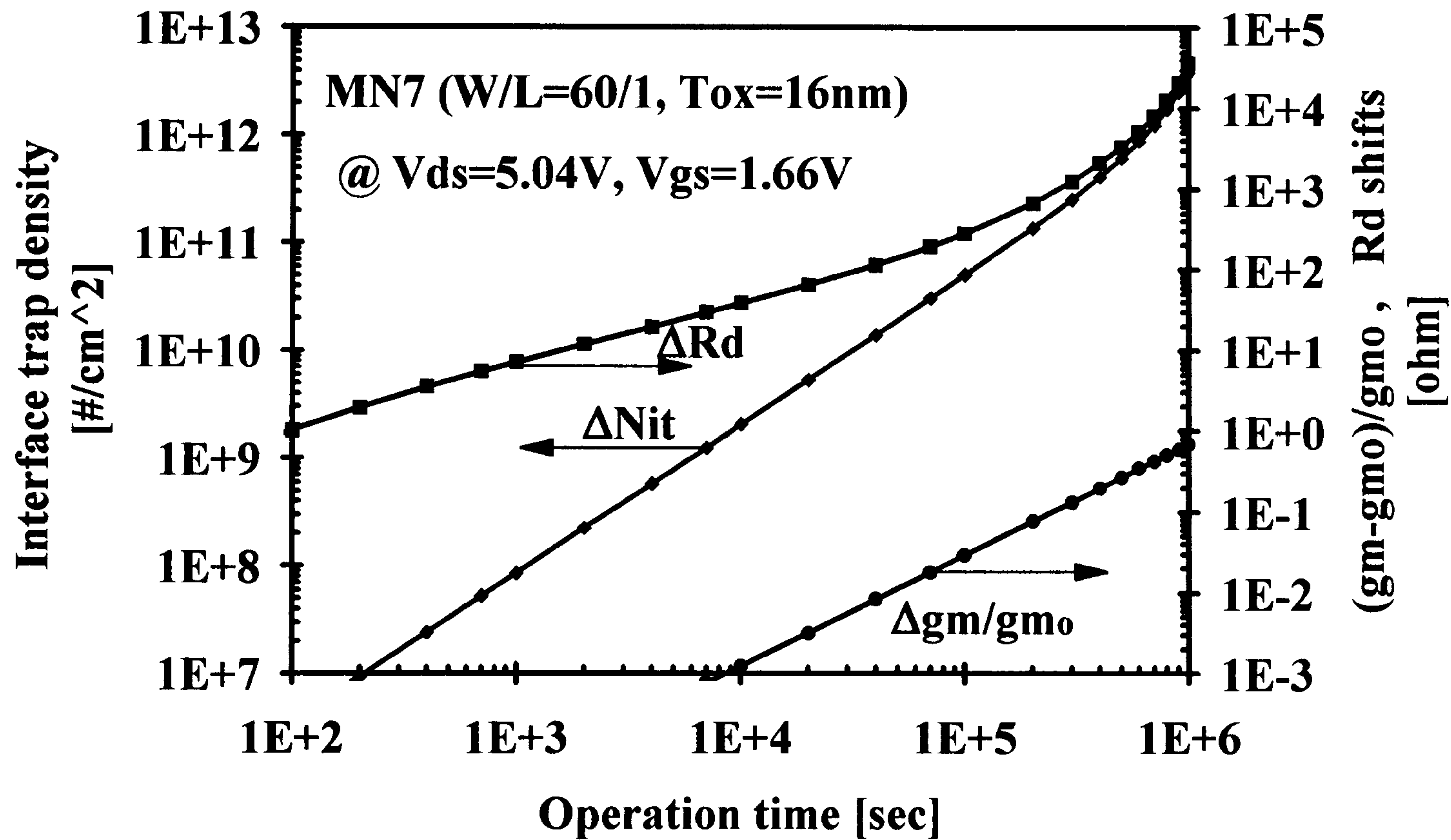


Figure 6-10 Simulation results of ΔRd for MN7 in Fig. 6-9 from Eq. (6-10) under the operating condition.

MP3, and MP9. Fig. 6-11 shows the comparison of the reliability projections by the ΔRd model (mark) and the BERT model (line) obtained by repeated simulations of circuit performance. The ΔRd model projection of the gain and the output resistance changes corresponds well with the BERT model. Thus, it is quite clear that the ΔRd model is much simpler and a more efficient technique of reliability projections in analog IC design.

6.4 Summary

We have proposed an easily realizable reliability model of hot-carrier induced degradation of nMOSFET's for circuit simulations and reliability projections in IC design. Hot-carrier induced interface trap charge is represented by a series connected resistance (ΔRd). The proposed ΔRd reliability model requires only one parameter (ΔNit) for reliability projections in circuit simulations without extensive parameter extraction from the characterization of hot-carrier induced degradation. The ΔRd reliability model can be implemented in any circuit simulator such as SPICE. The proposed ΔRd reliability model is found to be much simpler and is suitable for reliability projections in IC design, most specifically in analog IC design. Unlike conventional reliability simulators which require stressed parameter files for each lifetime time period, the proposed ΔRd reliability model can be used in IC design-for-reliability, reliability projections of any IC design can be predetermined by a pre-selected ΔRd without stressed parameter files. In addition, one of the potential applications of the ΔRd model is that this model can be easily used for a sensitivity analysis. A process-oriented lifetime criteria (i.e., Δgm/gmo=10%, [7], [43]) may not be appropriate in nor

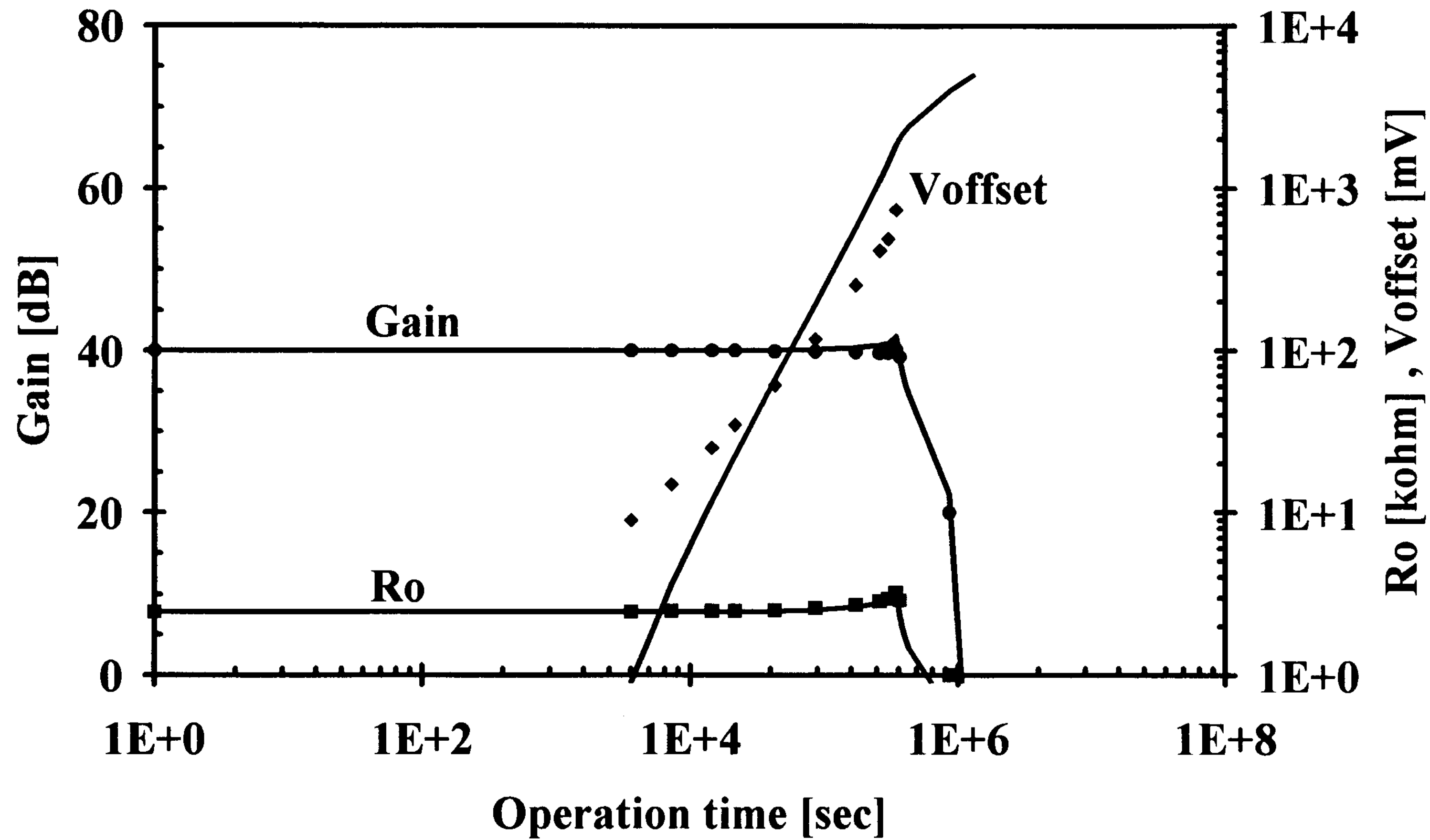


Figure 6-11 Comparison of the ΔRd model (mark) and the BERT model (line) reliability projections of the CMOS Op-Amp.

suitable for design-for-reliability. In general, the proposed ΔRd model is a powerful and versatile reliability model which can be used in IC design.

7. CONCLUSIONS

This research has been divided into three parts which are related with hot-carrier effects in CMOS transistors:

1) an investigation of physical mechanisms which can explain the hot-carrier induced degradation on CMOS transistors;
2) development of device models for hot-carrier induced device degradation and reliability simulations;
3) lifetime projections which can provide IC design guidelines based on allowable parameter mismatches.

Particular attention has been given to hot-carrier induced trapped charge in the gate oxides and/or surface states and the physical effects of these on device degradation. Models of the devices and circuit simulations have then been given resulting in reliability projections for the circuits. Several conclusions may be drawn concerning the results and analysis of the hot-carrier effects in CMOS transistors presented in this thesis. The major accomplishments achieved during this study can be summarized as follows;

1) several device characteristic models for MOSIS-HP-CMOS34 and MOSIS-HP-CMOS26B foundry service processes have been developed such as saturation drain voltage model and substrate current model which are vital for lifetime projections and reliability simulations. Both p- and n-MOS devices have been characterized for the applications in the CMOS IC design and the reliability simulations.

2) the hot-electron trapping level in the gate oxides has been investigated by applying the tunneling model of the electric field stimulated emission technique. This is the result of hot-carrier stress at room temperature, and we have found that a 2.5eV trap level below the oxide conduction band is responsible for the hot-carrier induced device degradation. This will not recover under normal DC operating conditions. In order to examine the increase of the surface states under hot-carrier stress, the charge pumping current technique was employed on HP-CMOS34 devices.

3) for current foundry service technologies; the MOSIS-HP-CMOS34 and MOSIS-HP-CMOS26B processes, lifetime projections have been obtained by accelerated lifetime tests, and comparisons have been made between both processes. Design guidelines based on allowable parameter mismatches have been demonstrated in a CMOS sense amplifier. It can be concluded that one of the most important transistor parameters to be monitored under stress is the maximum transconductance (gmx) degradation in the linear region since it can provide basic information on the hot-carrier induced device degradation. Empirical models of hot-carrier induced device degradation and device model parameters for SPICE MOS level 3 have been developed for reliability simulations as a function of the gmx degradation which occurs with time.

4) since analog circuit parameters are more susceptible to the hot-carrier induced degradation than the commonly monitored digital circuit parameters, a physical model of drain conductance degradation due to hot-carrier injection has been derived for lifetime projections in analog IC's. The proposed drain conductance (gd) degradation model, which is simple and practical, is a function of the gmx

degradation in the linear region. The parameter mismatches which develop in analog IC designs are then utilized for lifetime predictions for these analog IC designs. Also, design guidelines based on this gd degradation model have been given for analog IC's in which longer channel length devices have shown larger saturation gd degradation than shorter channel length devices.

5) a hot-carrier induced series resistance enhancement (ΔRd) model of nMOSFET's has been devised for reliability projections in analog IC designs. The proposed ΔRd model is based on the increase of the hot-carrier induced interface trapped charge (ΔNit). A reliability projection has been demonstrated using a conventional CMOS amplifier. Comparison has been made between conventional reliability simulation techniques and the ΔRd model. The ΔRd model has been shown to be much simpler and more applicable in analog IC designs. In the ΔRd model, the only degradation parameter is the increase of the hot-carrier induced trapped charge near the drain region. The most obvious application area of the ΔRd model is in IC design-for-reliability. The ΔRd model where degradation is represented by a simple additional resistor is however not limited only to analog circuits.

In general, the analytical models presented in this thesis are in good agreement with the measured results. The advantage of the analytical approach is that it provides a guide based on physical mechanisms and will enable the design of improved reliability VLSI circuits.

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APPENDICES

APPENDIX A

COMPOSITE nMOSFET

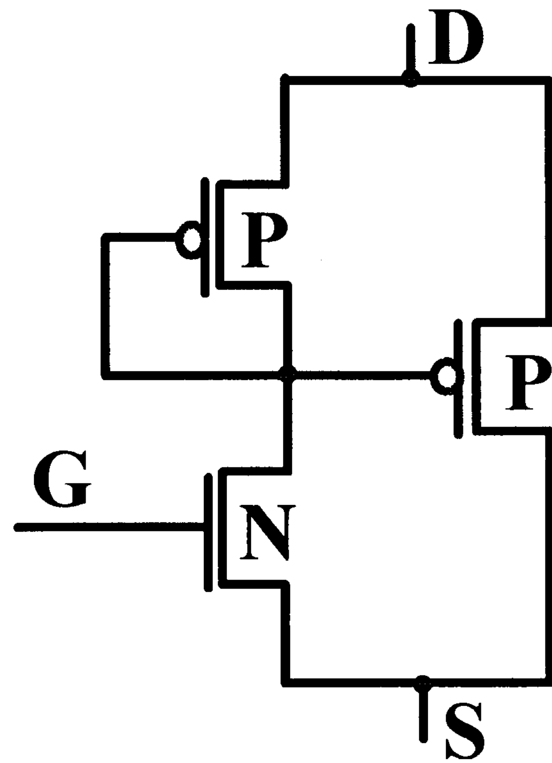
A.1 Introduction

The dimensions and the switching and the switching speeds of MOSFET VLSI circuits have been reduced dramatically during the last decade. However, problems emerge as channel length and gate oxide thickness decrease. Some of the MOSFET parameters change over time under operating conditions due to hot-carrier induced degradation. This degradation of the MOSFET devices directly affects the performance of circuits, especially analog and mixed-mode digital circuits [A1]. Substrate current is usually employed as the primary indicator of hot-carrier degradation [A2]. By measuring the substrate current of the device under operation conditions, the lifetime of the circuit can be predicted. Hot-carrier effects will cause the degradation of the transconductance, drain conductance, and threshold voltage shifts, thus leading to changes in DC bias condition, gain and circuit delays [A3]-[A5].

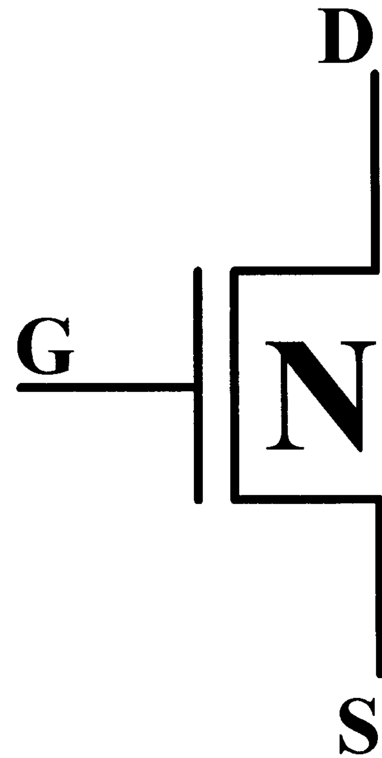
The purpose of this chapter is to examine a new composite nMOSFET circuit replacing a single n-channel MOSFET in the output stage where high drain-to-source voltage exists, and to also explore the possibility of employing devices with larger channel length as an alternative when hot-carrier induced degradation is critical.

A.2 Design Configuration

A composite nMOSFET has been designed to replace a conventional n-channel MOSFET device, the schematic diagram being presented in Fig. A-1. This composite device consists of one n-channel transistor and two p-channel transistors. The voltage and/or current across the nMOSFET is kept low by using a voltage and current divider technique. Most of the current and/or voltage is absorbed by the output p-MOSFET.



Composite nMOSFET



Conventional nMOSFET

Figure A-1 Schematic comparison between composite and conventional nMOSFET implementation.

The I-V characteristic curve of this composite device is very similar to that of a conventional nMOSFET, as shown in Fig. A-2.

A good example of employing a composite nMOSFET is an output buffer stage of conventional analog and mixed-mode IC's where the normal nMOSFET is in the saturation region with a high DC biasing condition. In order to demonstrate, the composite nMOSFET design schemes, the saturation drain current in the composite nMOSFET is assumed to be driven mainly by the parallel connected pMOS (P3) as shown in Fig. A-3 where the gate voltage (Vx) is determined by equating the saturation drain currents of the series-connected pMOS (P2) and nMOS (N1);

$$Vx = \frac{Vgs + (\sqrt{(W1/W2)\cdot(\mu_n/\mu_p)} - 1)\cdot Vtn + Vtp}{1 + \sqrt{(W1/W2)\cdot(\mu_n/\mu_p)}} \qquad \text{(A-1)},$$

where the channel lengths are assumed as L0=L1=L2=L3 and Vds=Vgs-Vth in the saturation region. The channel widths of the devices in the composite nMOSFET are then determined as follows;

$$\frac{Vgs - 2\cdot Vtn + Vtp}{Vgs - Vtn} = \sqrt{\frac{W3 - W1}{W0}}\cdot(\sqrt{\frac{W2}{W1}} + \sqrt{\frac{\mu_n}{\mu_p}}) \qquad \text{(A-2)}$$

Fig. A-3 shows a design chart of the composite nMOSFET for the applications in analog IC's by letting $\mu_n / \mu_p \approx 3$, Vth=Vtn=Vtp, and W1=W2;

$$\frac{Kv - 3}{Kv - 1} = \sqrt{\frac{1 - W1/W0}{W3/W0}}(1 + \sqrt{3}) \qquad \text{(A-3)}$$

where Kv=Vgs/Vth. Eq. (A-3) shows that as gate voltage increases, the total size of a composite nMOSFET (W1+W2+W3) can be comparable with that of a normal nMOSFET (W0). Hence this composite nMOSFET is suitable for high DC biasing operating conditions.

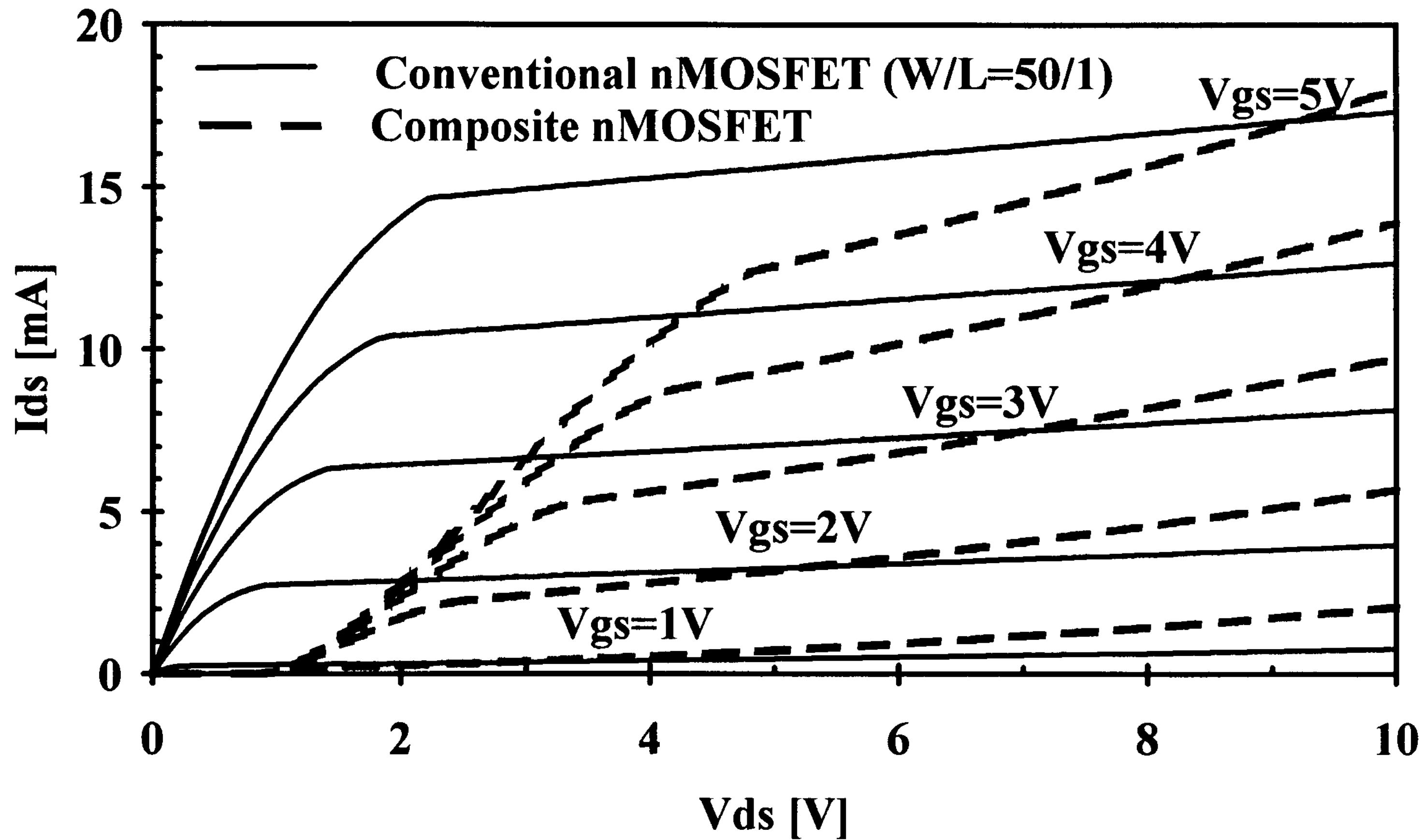


Figure A-2 I-V characteristic curves of conventional and composite nMOSFET's.

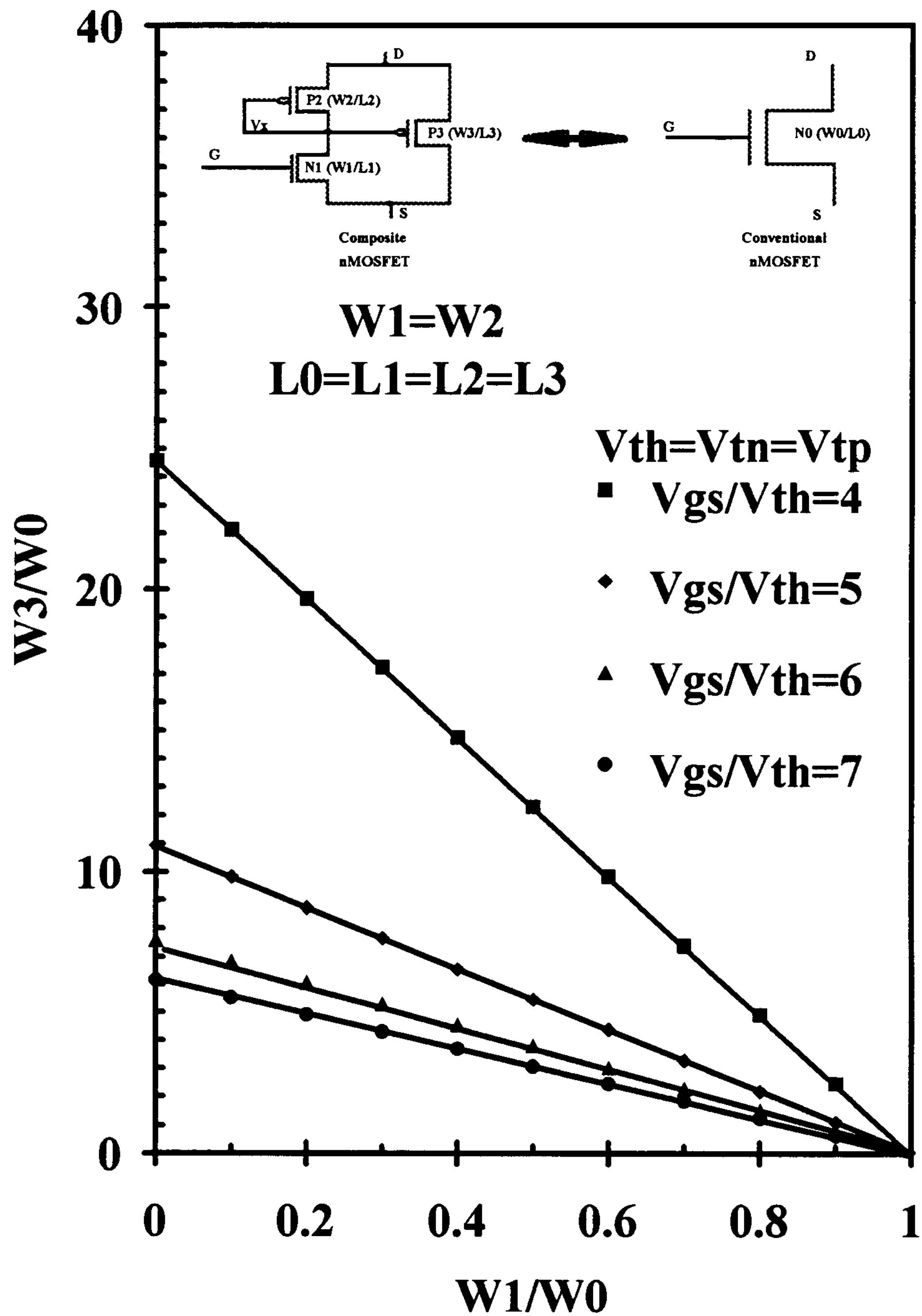


Figure A-3 Design chart of a composite nMOSFET in analog IC's.

A.3 Small-Signal Model of the Composite nMOSFET

A small signal model of the composite nMOSFET is shown in Fig. A-4 to derive the output resistance (r_O). Since P2 is in the saturation region as N1 turns on, by summing the current at the drain then;

$$i_{ds} = v_{ds} \cdot \frac{gm2 \cdot gd1}{gm2 + gd1} - (v_{ds} \cdot \frac{gm2 \cdot gd1}{gm2 + gd1} \cdot \frac{1}{gd1} - v_{ds}) \cdot gm3 + v_{ds} \cdot gd3 \quad \text{(A-4 (a))}.$$

and

$$i_{ds} = v_{ds} \cdot \frac{(gm2 + gm3) \cdot gd1}{gm2 + gd1} + v_{ds} \cdot gd3 \quad \text{(A-4 (b))},$$

The output resistance becomes

$$r_o = \frac{v_{ds}}{i_{ds}} = \frac{gd1 + gm2}{gd1 \cdot (gm2 + gd3) + (gd1 + gm2) \cdot gd3} \quad \text{(A-5)}.$$

Figure A-5 shows a good agreement between the results of Eq. (A-5) and the SPICE simulations which are in marks and lines, respectively. It should be noted that the output resistance becomes 1/gd3 if the composite nMOSFET is in the saturation region where gm3>>gm2>>gd1 and gd3·gm2>>gd1·gm3, since W3 is generally much larger than W1 and W2.

By the same approach, transconductance (gm) of a composite nMOSFET can then be derived as;

$$gm = \frac{gm1}{gd1 + gm2} \cdot (gm2 + gm3) \quad \text{(A-6)}.$$

Since gm3>>gm2>>gd1, Eq. (A-6) becomes;

$$gm = \frac{gm1}{gm2} \cdot gm3 \quad \text{(A-7)}.$$

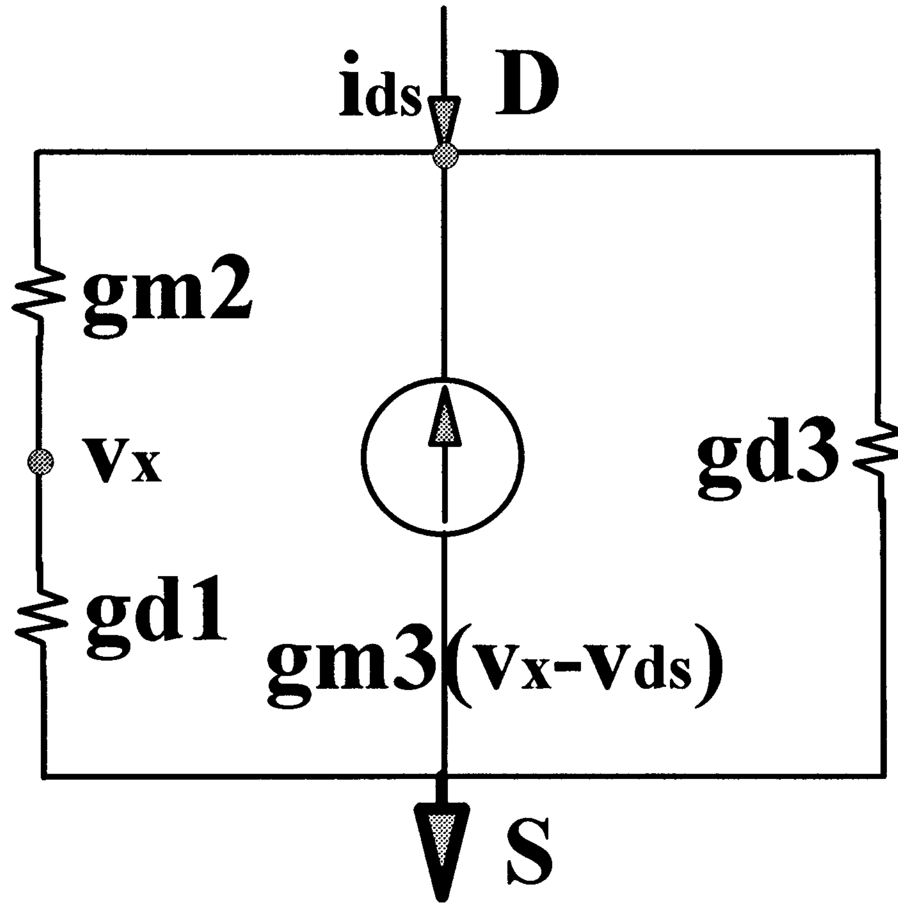


Figure A-4 Small-signal model of a composite nMOSFET for the output resistance calculation.

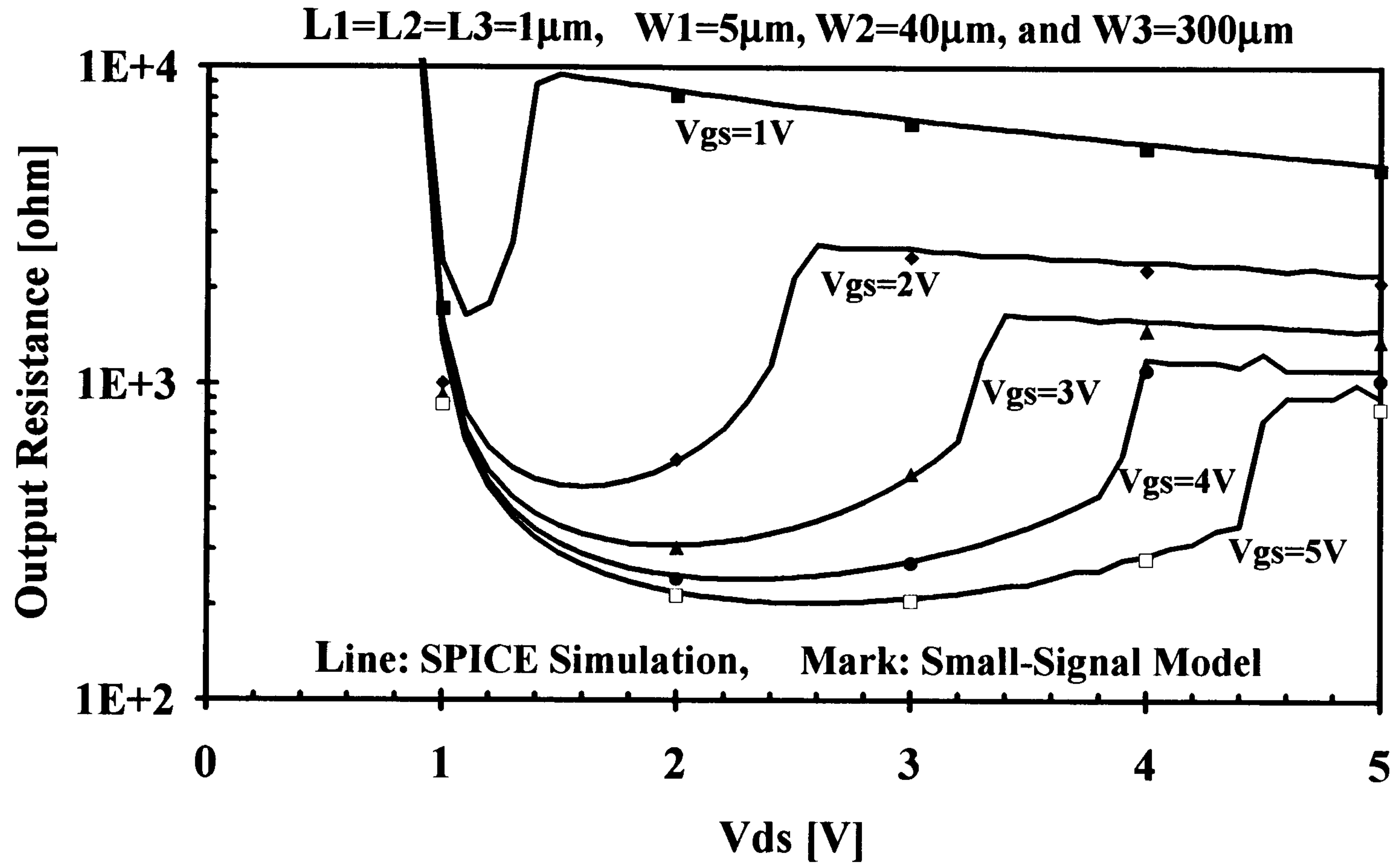


Figure A-5 Output resistance of a composite nMOSFET.

Figure A-6 shows a good agreement between the results of Eq. (A-6) and the SPICE simulations which are in marks and lines, respectively.

A.4 Circuit Simulations and Results

In order to determine the performance of the composite device, a simple differential amplifier with an output stage has been used. Fig. A-7 shows the schematic diagram of the amplifier in which the three-terminal characteristic of the composite device enables it to be used as a direct replacement of a conventional nMOSFET. Transistor M9 in Fig. A-7 which is connected to the output is problematic in that a large voltage can appear across the drain and source. A high drain-to-source voltage implies a large substrate current due to hot-carrier effects, if one micron devices are employed, and large amounts of degradation. An alternative might be to use a device with larger channel length which is much less affected by hot-carrier degradation; 2μm devices in general have smaller substrate currents thus providing longer lifetimes compared to 1μm devices.

Figure A-8 shows the SPICE simulation results using various devices for M9 in the differential amplifier. As the device channel length is reduced, the performance gap between the conventional and composite devices also reduces. For example, with 1μm devices, DC gain, cutoff frequency and unity gain frequency are roughly factors of 2 different, whereas with 0.8μm devices, there is very little difference in circuit performance between using conventional and composite nMOSFET's, while the substrate current is reduced substantially.

This substrate current reduction translates into an improvement of device or circuit lifetime, especially for submicron devices. The lifetime is a strong function of

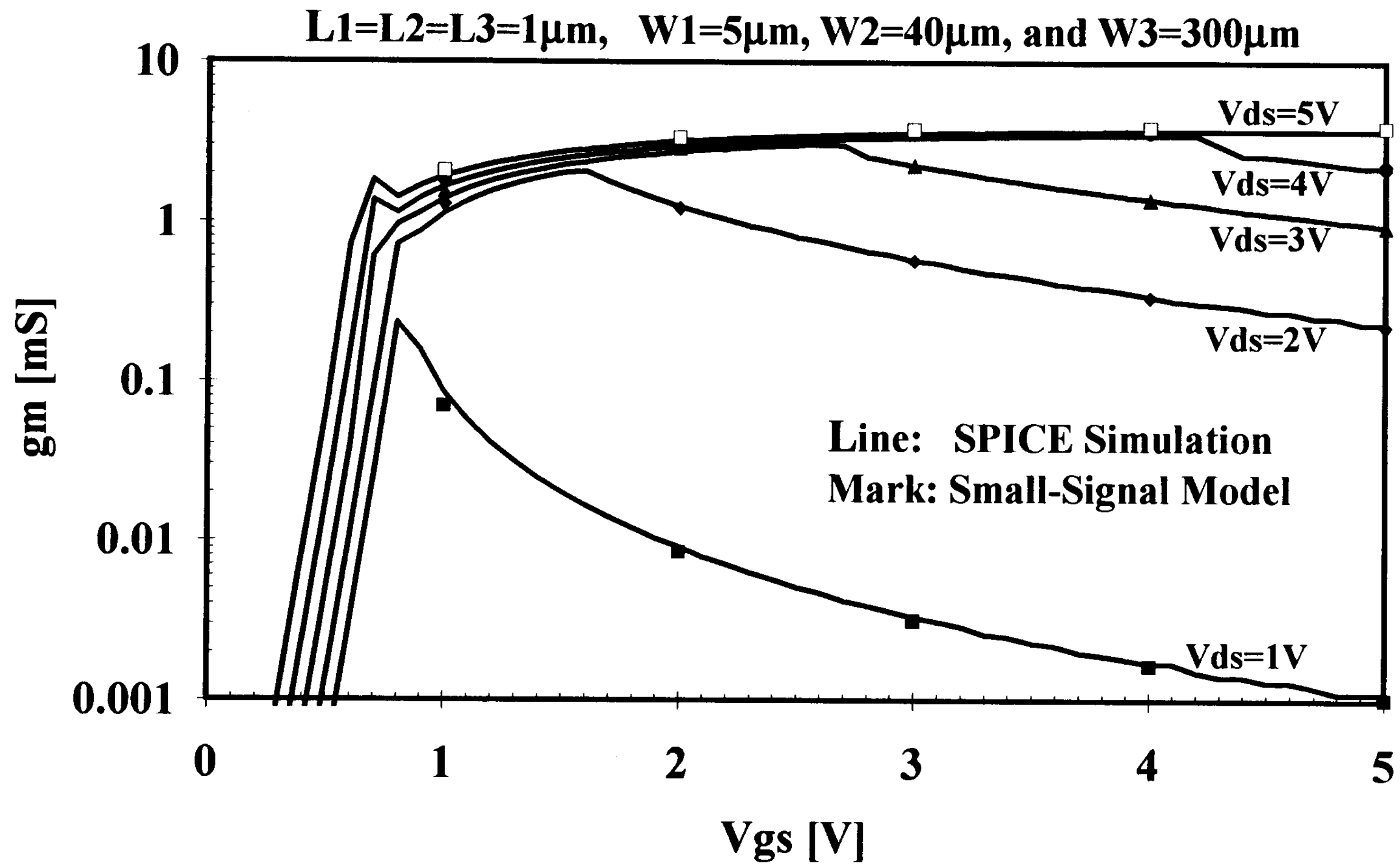


Figure A-6 Transconductance (gm) of a composite nMOSFET.

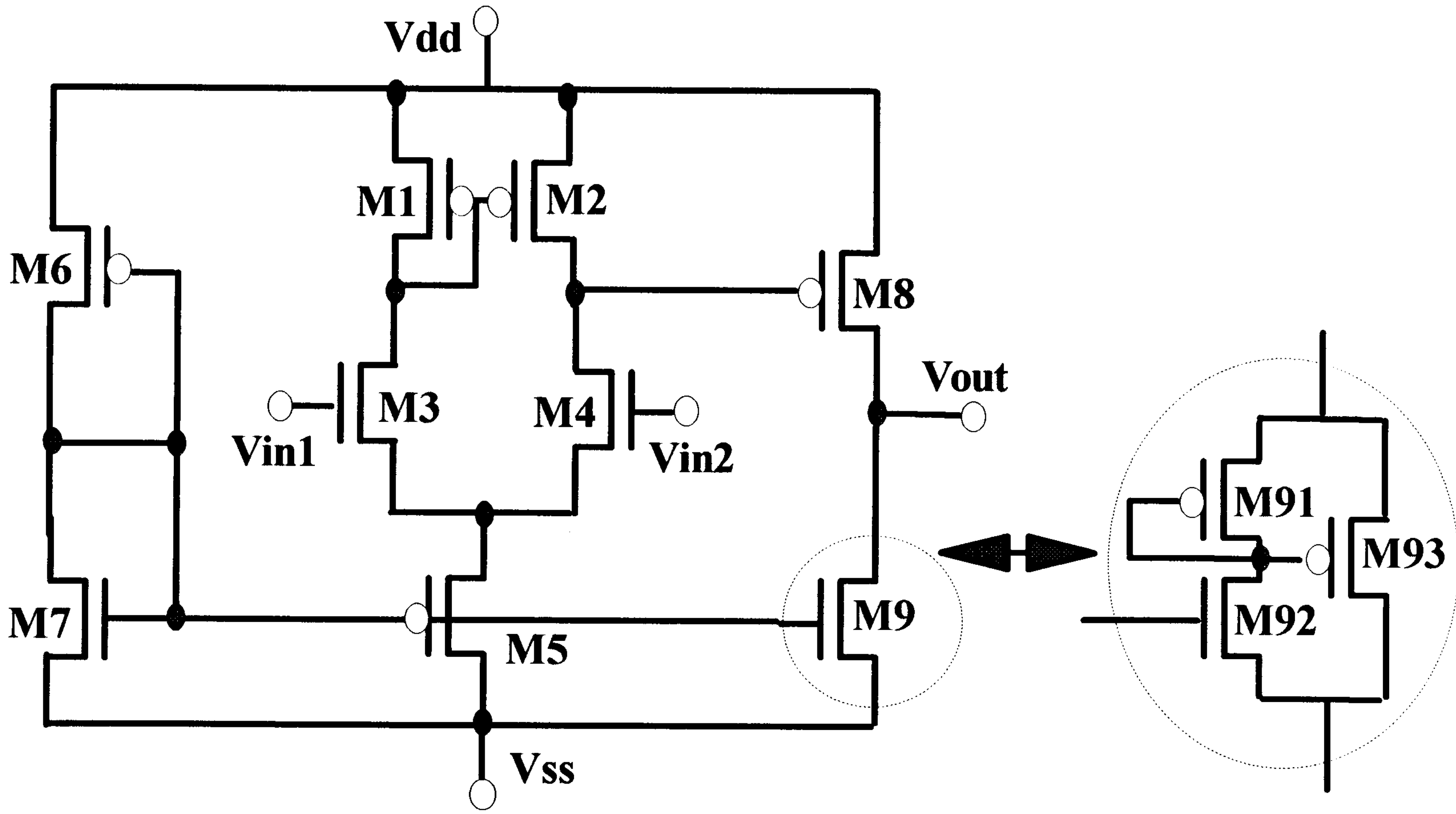


Figure A-7 CMOS single-ended output differential amplifier.

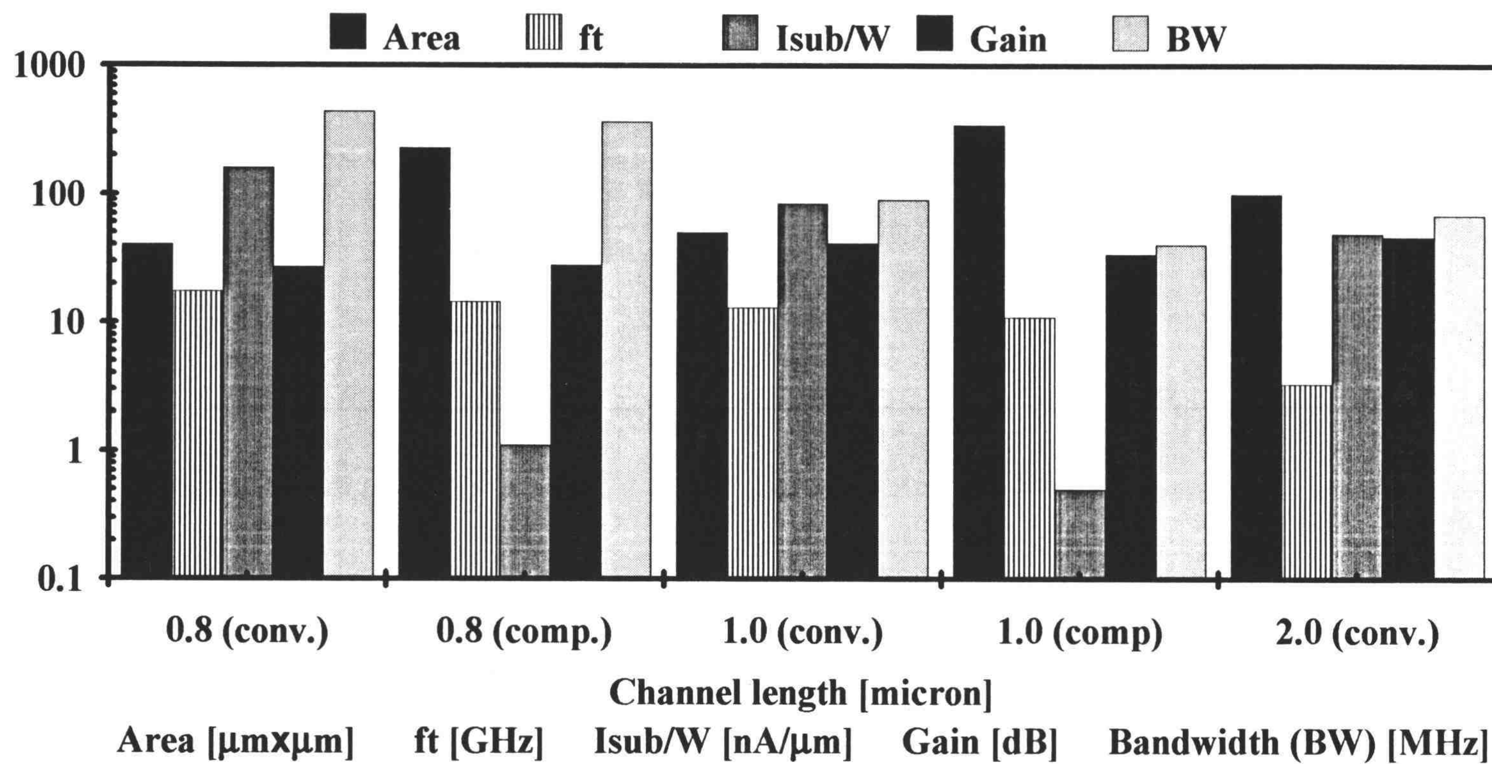


Figure A-8 Device characteristics and circuit performance of composite and conventional nMOSFET's.

substrate current [A2] as shown in Fig. A-9. In the circuit simulations, we have numerically calculated the average substrate current from device characteristics.

Figure A-9 presents the relative lifetime with different devices in the output circuit for both composite and conventional nMOSFET's. The device channel length ranges from 0.8 to 2μm. Assuming a 1μm technology, the simple amplifier with 1μm devices throughout has a gain of 41 dB and bandwidth of 90 MHz, two of the primary circuit performance parameters. Two other designs have comparable circuit performance characteristics: the conventional nMOSFET design with a 2μm channel length used for M9 and the composite nMOSFET design with a 1μm channel length used for M9. Gains are 46 and 34 dB, and bandwidths are 68 and 40 MHz, respectively.

The conventional nMOSFET with a 2μm channel length for M9 appears to be one of the better choices based on the circuit performance parameters. However, the relative lifetime improvement of the 2μm conventional nMOSFET design is less than a factor of 10, whereas the 1μm composite nMOSFET design provides eight orders of magnitude improvement. A lifetime improvement of this order of magnitude is needed as the device dimensions (channel length) reduce further and 5V power supplies are used.

A.5 Summary

The composite nMOSFET is a good design choice for a device in a circuit that often has large drain-to-source voltage and needs a longer operating lifetime. The SPICE simulations have shown that by using composite nMOSFET design techniques, the lifetime can be improved by 8 orders of magnitude in contrast to just a minor

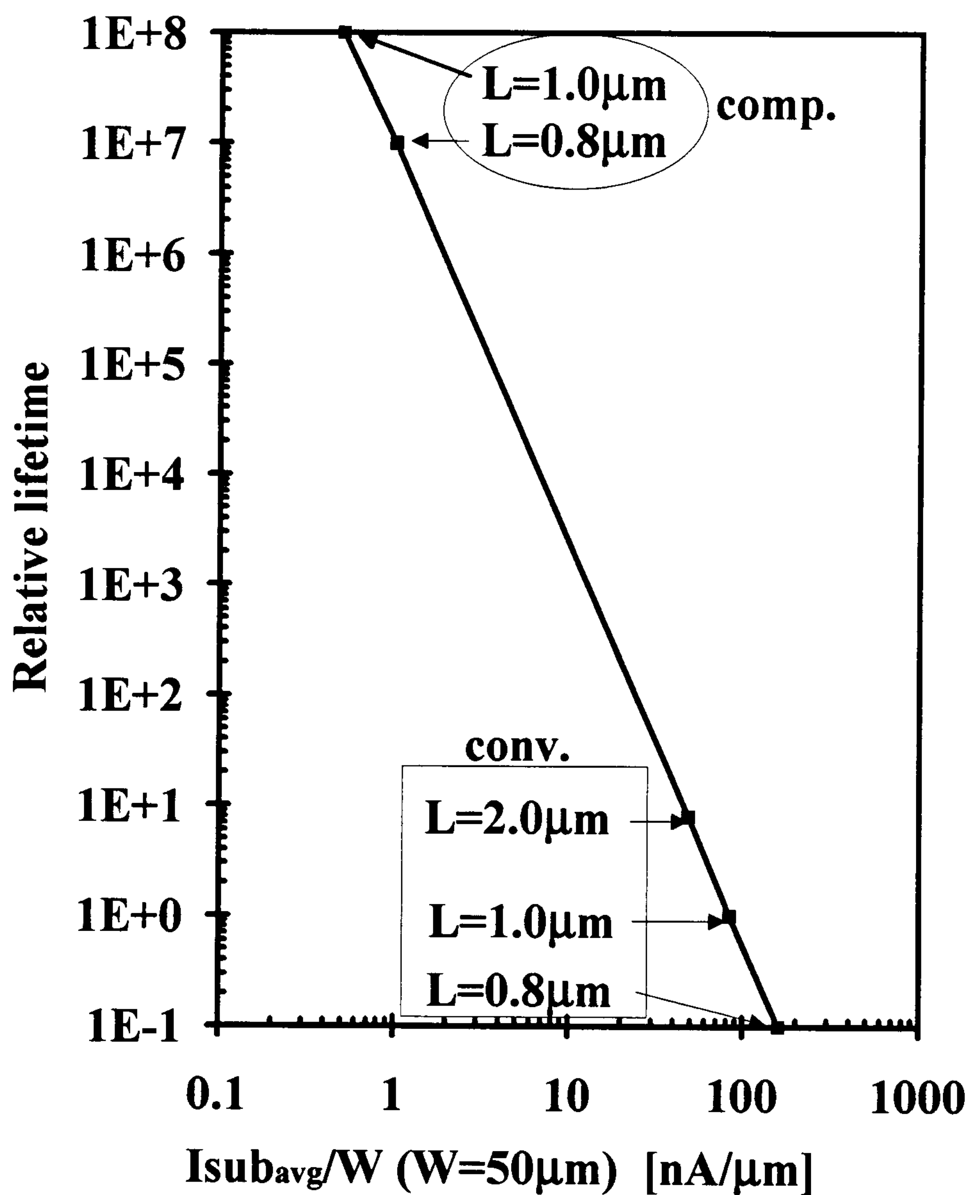


Figure A-9 Relative lifetime projection of composite and conventional nMOSFET's.

improvement by using larger channel lengths. The composite nMOSFET design technique could find applications in submicron circuits where the lifetime is unacceptably short, with only minor circuit performance reduction.

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APPENDIX B

HOTPEX:

HOT-CARRIER ANALYSIS

AND

PARAMETER EXTRACTION PROGRAM

```
1000 '****************************** HOTPEX.BAS ********************************
1010 '$$$$$$$$$$$$$$$$$$$$$$$$ HOT-CARRIER ANALYSIS PROGRAM $$$$$$$$$$$$$$$$$$$$
1020 '****************** SPICE MOS3 PARAMETER EXTRACTION PROGRAM ***********
1030 '*********************** NAM HWANG (Jan. 19, 1993) ***********************
1040 'UPGRADED VERSION OF HESAP & PEX (HPEX1, HPEX2, HPEX3, HPEX4, HPEX5,
    HPEX6)
1050 'REVISED UO, VMAX, THETA EXTRACTION WITH ADAPTIVE TEST (1/22/93)NH
1060 'REVISED TO CREATE FILES ON STRESS TIME (1/24/93)NH
1070 'REARRANGED FOR MAXIMUM EFFICIENT CYCLE TIME (1/28/93)NH
1080 'EMPHASIZED DBCS MEAS. AND LIMITED HAMER METHOD (2/02/93)NH
1090 'REVISED FOR HP CMOS 26B PROCESS AND INPUT CORRECTION (2/12/93)NH
1100 PROG$="HOTPEX" : BKPF$="C:"+PROG$+".BKP" : SAVE BKPF$ 'BACK-UP FILE
1110 TSTART$=TIME$ : DSTART$=DATE$ : COLOR 14,1,2
1120 '--------------------------------------------------------------------
1130 DIM DR(0),SUBPT(10),X(20),Y(20),Z(20)
1140 DIM VT(13),VB(5),VU(6),VK(5),T(100),VXTF(15),VXTR(15),VGJPN(15),IDJPN(15)
1150 DIM GDNF(5),VGDNF(5),GDNR(5),VGDNR(5),SXTF(15),SXTR(15),VXXF(15),VXXR(15)
1160 DIM IDF(5,50),IDR(5,50),IBF(50),IBR(50),IMF(50),IMR(50),IP(5,50),VS(5)
1170 '--------------------------------------------------------------------
1180 CMD$=SPACE$(20)   : CMDVSS$=SPACE$(20) : CMDVBB$=SPACE$(20)
1190 CMDVDD$=SPACE$(20) : CMDVGG$=SPACE$(20) : CMDIDS$=SPACE$(20)
1200 'DEVICE CONSTANTS [cm] ------------------------------------------------
1210 L=.0001 : W=.002 : VDSTR=7 : VGSTR=2.5 : VBSTR=-1
1220 SSS=0 '<-------------------------- <Show Spice Sim> 1=STOP AFTER PLOTTING
1230 DUTID$="H1-54-7HG"
1240 CLS : GOSUB 2150 : X=0
1250 PRINT "    1 ------> DUT-ID : ";DUTID$
1260 PRINT "    2 ------> DEVICE : W [um]=";W*10000!
1270 PRINT "    3 ------>        : L [um]=";L*10000!
1280 PRINT "    4 ------> STRESS : VDS[V]=";VDSTR
1290 PRINT "    5 ------>        : VGS[V]=";VGSTR
1300 PRINT "    6 ------>        : VBS[V]=";VBSTR
1310 PRINT "    7 ------> SPICE SIM. MODE:";SSS;"<--- 1=STOP WITH SPICE SIM."
1320 PRINT "    0 ------> NO CHANGE & START ! "
1330 INPUT "            ENTER A CODE # ----->";X
1340 PRINT : PRINT : IF X=0 THEN GOTO 1430
1350 IF X=1 THEN INPUT "        ENTER NEW DUT-ID";DUTID$ : GOTO 1240
1360 IF X=2 THEN INPUT "        ENTER NEW W[um]";W : W=W*.0001 : GOTO 1240
1370 IF X=3 THEN INPUT "        ENTER NEW L[um]";L : L=L*.0001 : GOTO 1240
1380 IF X=4 THEN INPUT "        ENTER NEW VDS[V]";VDSTR : GOTO 1240
1390 IF X=5 THEN INPUT "        ENTER NEW VGS[V]";VGSTR : GOTO 1240
1400 IF X=6 THEN INPUT "        ENTER NEW VBS[V]";VBSTR : GOTO 1240
1410 IF X=7 THEN INPUT "        ENTER A SPICE SIM. MODE : 0(AUTO) OR 1(SEMI-
    AUTO)";SSS : GOTO 1240
1420 PRINT "     UNDEFINED CODE (";X;") ......!" : GOTO 1240
1430 '+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
1440 FILES "C:\DATA\*" : PRINT : FFF=0
1450 INPUT "     ENTER 1 <--- TO CREATE A FILE(DIR)";FFF
1460 IF FFF=0 THEN FINA$="TEST" : GOTO 1480
1470 INPUT "     ENTER A DIR\FILE NAME";FINA$
1480 DINA$="C:\DATA\"+FINA$
1490 'PHYSICAL CONSTANTS ---------------------------------------------------
```

```
1500  KO=3.9 : KSI=11.8 : EO=8.854E-14 : Q=1.6E-19 : PI=3.141592
1510  AI=1.2 : NI=1.18E+10
1520  LD2=.000036 : WD2=.00002 : TOX=.0000016 : DD=.00935 : DELSL=9.440699E-06
1530  XJ=.00001 : COX=KO*EO/TOX : LEFF=L-LD2 : WEFF=W-WD2
1540  OHM=8.15E-20 : ETA=DD/OHM*COX*LEFF^3
1550 'INITIAL VALUES (DEFAULT VALUES) <-------------------------- TO BE ALTERED
1560  VTO=.75 : PHI=.7 : FB=.02 : FM=.02 : FS=1 : DELTA=0 : THETA=.2 : XD=.00001
1570  KAPPA=.1 : GAMMA=.5 : UO=487 : VMAX=1E+07 : NSUB=2E+16 : NFS=1E+12
1580  DF=0 : PF=0        '<---------------------------------------- SET ERROR FREE
1590  FK1=0 : FK2=0      '!!!!!!! DO NOT TOUCH THE Function Keys !!!!!!
1600 '-----------------------------------------------------------------------
1610 ISC=7 'INTERFACE!
1620 SPA=717 'HP4145B!    1-SOURCE, 2-DRAIN, 3-GATE, 4-SUBSTRATE
1630 TIME=5 : MAX=2 : ACTUAL=0 : ZT=1
1640 FOR I=1 TO 10 : SUBPT(I)=1 : NEXT I  '<-------------- FULL FUNCTION OF HOTPEX
1650 '-----------------------------------------------------------------------
1660 VGSMAX=5 : VDSMAX=5 : VSS=0 : VDM=.1
1670 INFS=1E-09 : IGG=1E-08 : NT=12 : DNTF=1 : DNTR=3
1680 VT(1)=.06 : VT(2)=.25 : VT(3)=.56 : VT(4)=1 : VT(5)=1.56 : VT(6)=2.25
1690 VT(7)=3.06 : VT(8)=4 : VT(9)=5.06 : VT(10)=6.25 : VT(11)=7.56 : VT(12)=8
1700 NB=3 : VB(1)=0 : VB(2)=-2 : VB(3)=-5 '<---------------- [VTO, BETA, THETA]
1710 VJPN=.4 : DVG1=.4 : DVG2=.9 : ITH=.0000005 '<----------- [VTO, BETA, GAMMA]
1720 '<---------------------------------------------------- [UO, THETA, VMAX]
1730 NU=3 : VU(1)=3! : VU(2)=3! : VU(3)=5! : VBU=0   ' VGS-VTO
1740       VU(4)=.8 : VU(5)=1.8 : VU(6)=2.5        ' VDS-VTO
1750 '<----------------------------------------------------- VGS-VTO [KAPPA]
1760 NK=2 : VK(1)=4! : VK(2)=5! : VBK=0!
1770 '-----------------------------------------------------------------------
1780 TTOTAL=0 : TK=0 '<-------------------------------- STRESS TIME INTERVALS
1790 T(0)=1 : T(1)=1 : T(2)=1 : T(3)=2 : T(4)=4 : T(5)=7
1800 T(6)=15 : T(7)=30 : T(8)=60 : T(9)=120 : T(10)=120
1810 FOR I=11 TO 100  : T(I)=360 : NEXT I
1820 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
1830 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
1840 '
1850 '
1860 '************************************************************************
1870 '$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ MAIN PROGRAM $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
1880 '************************************************************************
1890 GOSUB 2150 '<---------------------------------------------------- HEADER!
1900 PRINT : PRINT "          GPIB INSTALLATION....  Please wait ..."
1910 GOSUB 2260 '<------------------------------------------ HANDSHAKES & RESET
1920 GOSUB 2410 '<---------------------------------------------------- ZEROV!
1930 '>>>>>>>>>>>>>>>>>>>>> HOT CARRIER STRESS - MAIN LOOP <<<<<<<<<<<<<<<<<<
1940 KEY(1) ON : ON KEY(1) GOSUB 2550
1950 IF TK=0 THEN STRD=1 : GOTO 1980
1960 GOSUB 3200 '<----------------------------------------- HOT-CARRIER STRESS
1970 GOSUB 2410 '<---------------------------------------------------- ZEROV!
1980 IF SUBPT(1)=1 THEN GOSUB 3730   '<---------------- HOT-CARRIER STRESS CHARACTE.
1990 IF SUBPT(2)=1 THEN GOSUB 3920   '<---------------- INFORMAL DEVICE DATA.
2000 IF SUBPT(3)=1 THEN GOSUB 4760   '<---------------- DRAIN-BIASED CHARACT.
2010 IF SUBPT(4)=1 THEN GOSUB 5020   '<---------------- SUBTHRESHOLD SLOPE S.
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2020 IF SUBPT(5)=1 THEN GOSUB 5190  '<------------------- PEX -  VTO,B,G.
2030 IF SUBPT(6)=1 THEN GOSUB 5600  '<------------------- PEX -  UO,H,VM.
2040 IF SUBPT(7)=1 THEN GOSUB 5940  '<------------------- PEX -  KAPPA...
2050 IF SUBPT(8)=1 THEN GOSUB 6350  '<------------------- LPRINT PEX RESULTS...
2060 IF SUBPT(9)=1 THEN GOSUB 6900  '<------------------- SPICE (MOS3) SIMULAT.
2070 IF SUBPT(10)=1 THEN GOSUB 7620  '<------------------- FILE SAVER...........
2080 TK=TK+1 : IF TK<=100 AND FK1=0 THEN GOTO 1960
2090 KEY(1) OFF : GOSUB 3520 : END
2100 '+++++++++++++++++++++++++++++ END OF LOOP +++++++++++++++++++++++++
2110 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
2120 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
2130 '
2140 '
2150 'SUBROUTINE : HEADER *********************************************************
2160 FIDE$="HOT-CARRIER STRESS & SPICE MOS3 - LDD NMOS :
     W[um]/L[um]="+STR$(W*10000!)+"/"+STR$(L*10000!)
2170 CLS : PRINT : PRINT
2180 PRINT "      ***************************************************************"
2190 PRINT "      $$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ";PROG$;" $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$"
2200 PRINT "      ***************************************************************"
2210 PRINT "      ";FIDE$
2220 PRINT "      Vds [V] / Vgs [V] =";VDSTR;"/";VGSTR;"     @ Vbs [V] =";VBSTR
2230 PRINT : RETURN '<------------------------------------------- END OF HEADER
2240 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
2250 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
2260 'SUBROUTINE : HANDSHAKE & RESET ********************************* *********
2270 '<--------------------------------------------------------------- HANDSHAKE
2280 CALL IORESET(ISC)
2290 IF PCIB.ERR <> NOERR THEN ERROR PCIB.BASERR
2300 CALL IOTIMEOUT(ISC,TIME)
2310 CALL IOCLEAR(ISC)
2320 CALL IOCLEAR(SPA)
2330 CALL IOFASTOUT(ISC, TRUE)
2340 '<----------------------------------------------------------- RESET HP4145B
2350 CMD$="US;IT2 CA1 BC" : CL=LEN(CMD$)
2360 CALL IOOUTPUTS(SPA,CMD$,CL)
2370 IF PCIB.ERR <> NOERR THEN ERROR PCIB.BASERR
2380 RETURN '<++++++++++++++++++++++++++++++++++++++++ END OF SUB-HAND
2390 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
2400 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
2410 'SUBROUTINE : ZEROV *********************************************************
2420 CMD$="DV1,DV2,DV3,DV4" : CL=LEN(CMD$)
2430 CALL IOOUTPUTS(SPA,CMD$,CL)
2440 TIMEOFF=0
2450 IF PCIB.ERR <> NOERR THEN ERROR PCIB.BASERR
2460 ON TIMER(ZT) GOSUB 2510  'WAIT ZT SEC
2470 TIMER ON
2480 IF TIMEOFF=1 THEN RETURN
2490 GOTO 2480
2500 RETURN
2510 'SUB-TIMER
2520 TIMEOFF=1 : TIMER OFF : RETURN  '<+++++++++++++++++++++ END OF SUB-ZEROV
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```
2530 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
2540 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
2550 'SUBROUTINE : INTERRUPTION (FK1) ******************************************
2560 FK1=1 : DUMBO=0
2570 IF STRD=1 THEN FOR K=1 TO 10 : SUBPT(K)=9 : NEXT K : RETURN '<----- END NOW
2580 FOR K=1 TO 5 : PRINT : NEXT K : COLOR 14,1,2
2590 PRINT "   ENTER 0 FOR FINAL MEASUREMENT UPDATED AT INTERRUPTION"
2600 INPUT "         1 FOR IMMEDIATE TERMINATION WITHOUT ANY
    MEASUREMENT";DUMBO
2610 IF DUMBO=1 THEN FOR K=1 TO 10 : SUBPT(K)=9 : NEXT K : RETURN '<---- END NOW
2620 PRINT "              INTERRUPTION @ CYCLE #";TK
2630 PRINT "         ENTER THE ELAPSED TIME OF T(";TK;") in [min] ----->";T(TK)
2640 INPUT T(TK)
2650 STRD=1 : RETURN '<++++++++++++++++++++++++++++++++++++ END OF SUB-FK1
2660 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
2670 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
2680 'SUBROUTINE : PLOT REVIEW (FK2)
2690 FK2=1 : SSSX=SSS : SSS=1
2700 GOSUB 6900 : SSS=SSSX : FK2=0
2710 GOSUB 2150 '<--------------------------------------------------- HEADER!
2720 PRINT "STRESSING ..... CYCLE #:";TK;"(";T(TK);"min)";"-- START TIME:";TSET$
2730 PRINT "DON'T TOUCH !!!!               PRESENT TIME:"
2740 PRINT "              DON'T TOUCH !!!!"
2750 PRINT "                            DON'T TOUCH !!!!"
2760 PRINT "                                          DON'T TOUCH !!!!"
2770 RETURN '<++++++++++++++++++++++++++++++++++++++++++++++++ END OF
    SUB-FK2
2780 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
2790 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
2800 'SUBROUTINE : HP4145B MEASUREMENT ****************************************
2810 '         TI=1 (FORWARD  IDS) : TI=2 (REVERSE  IDS)
2820 '         TI=3 (FORWARD ISUB) : TI=4 (REVERSE ISUB)
2830 IF ABS(VDD)<10 AND ABS(VGG)<10 THEN GOTO 2850
2840 DF=999999! : PRINT "        DEVICE FAULT #999999" : GOSUB 3400
2850 CMDVSS$="DV1,1,"+STR$(VSS)+",.1"
2860 CMDVDD$="DV2,1,"+STR$(VDD)+",.1"
2870 IF TI=2 OR TI=4 THEN CMDVSS$="DV1,1,"+STR$(VDD)+",.1"
2880 IF TI=2 OR TI=4 THEN CMDVDD$="DV2,1,"+STR$(VSS)+",.1"
2890 CLVSS=LEN(CMDVSS$) : CLVDD=LEN(CMDVDD$)
2900 CMDVBB$="DV4,1,"+STR$(VBB)+",.1" : CLVBB=LEN(CMDVBB$)
2910 CMDVGG$="DV3,1,"+STR$(VGG)+",.1" : CLVGG=LEN(CMDVGG$)
2920 IF TI=1 THEN CMDIDS$="TI2"
2930 IF TI=2 THEN CMDIDS$="TI1"
2940 IF TI=3 OR TI=4 THEN CMDIDS$="TI4"
2950 CLIDS=LEN(CMDIDS$)
2960 CALL IOOUTPUTS(SPA,CMDVSS$,CLVSS)
2970 CALL IOOUTPUTS(SPA,CMDVBB$,CLVBB)
2980 CALL IOOUTPUTS(SPA,CMDVGG$,CLVGG)
2990 CALL IOOUTPUTS(SPA,CMDVDD$,CLVDD)
3000 CALL IOOUTPUTS(SPA,CMDIDS$,CLIDS)
3010 IF PCIB.ERR <> NOERR THEN ERROR PCIB.BASERR
3020 CALL IOENTERA(SPA,DR(0),MAX,ACTUAL)
```

```
3030 IDS=DR(0)
3040 RETURN '<+++++++++++++++++++++++++++++++++++++++++++++ END OF SUB-DATA
3050 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
3060 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
3070 'SUBROUTINE : VGS @ IDSconst. MEASUREMENTS**********************************
3080 'SP : IXX, VDD, VSS, VBB, TI    ------> OP : VGSXX, IDXX(~IXX)
3090 VGG=0 : DVGS=1 : P=1 : NTH=14
3100 FOR K=0 TO NTH
3110 VGG=VGG+DVGS/(2^K)*P : GOSUB 2800
3120 P=SGN(IXX-ABS(IDS))
3130 IF P=0 THEN VGXX=VGS : K=NTH : GOTO 3150
3140 IF P=1 THEN GOTO 3110
3150 NEXT K
3160 VGXX=VGG : IDXX=ABS(IDS)
3170 RETURN '<+++++++++++++++++++++++++++++++++++++++++++++ END 0F SUB-VGXX
3180 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
3190 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
3200 'SUBROUTINE : HOT-CARRIER STRESS**********************************************
3210 KEY(1) ON : ON KEY(1) GOSUB 2550
3220 KEY(2) ON : ON KEY(2) GOSUB 2680
3230 GOSUB 2150 '<--------------------------------------------------------- HEADER!
3240 TSTR=60*T(TK) : STRD=0 : TSET$=TIME$ : DSET$=DATE$
3250 VDD=VDSTR : VGG=VGSTR : VBB=VBSTR : VSS=0 : TI=1
3260 GOSUB 2800 '<--------------------------------- HOT-CARRIER STRESS ON
3270 PRINT "STRESSING ..... CYCLE #:";TK;"(";T(TK);"min)";"-- START TIME:";TSET$
3280 PRINT "DON'T TOUCH !!!!                PRESENT TIME:"
3290 PRINT "                DON'T TOUCH !!!!"
3300 PRINT "                                DON'T TOUCH !!!!"
3310 PRINT "                                                DON'T TOUCH !!!!"
3320 ON TIMER(TSTR) GOSUB 3370
3330 TIMER ON
3340 IF STRD=1 OR FK1=1 THEN TTOTAL=TTOTAL+T(TK) : RETURN
3350 LOCATE 10,50 : IF FK1=0 THEN PRINT TIME$
3360 GOTO 3340
3370 STRD=1 : RETURN '<+++++++++++++++++++++++++++++++++++++ END OF SUB-STRESS
3380 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
3390 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
3400 'SUBROUTINE FOR ERROR HANDLING *******************************************
3410 '
3420 '
3430 '
3440 '
3450 '
3460 '
3470 '
3480 '
3490 RETURN '<++++++++++++++++++++++++++++++++++++++++++++ END OF SUB-ERROR
3500 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
3510 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
3520 'SUBROUTINE FOR EXIT **********************************************************
3530 GOSUB 2410 '<------------------------------------------------- GOOD-BYE ZEROV!
3540 CALL IOCLEAR(SPA)
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3550 CALL IOLOCAL(SPA)
3560 CALL IOCLEAR(ISC)
3570 IF PCIB.ERR<>NOERR THEN ERROR PCIB.BASERR
3580 CLS : PRINT : PRINT
3590 GOSUB 2150 '<---------------------------------------------------- HEADER!
3600 PRINT "    -----------> END OF HOT PARAMETER EXTRACTION  <---------------"
3610 PRINT "              START TIME : ";TSTART$,,DSTART$
3620 PRINT "               END  TIME : ";TIME$,,DATE$
3630 RETURN '<++++++++++++++++++++++++++++++++++++++++++++++++++ END OF SUB-EXIT
3640 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
3650 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
3660 '
3670 '
3680 '||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||
3690 '|MAIN SUBROUTINES FOR SPICE MOS3 PARAMETER EXTRACTION|
3700 '||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||
3710 '
3720 '
3730 'SUB-PT1 : HOT-STRESS CHARACTERISTICS****************************************
3740 GOSUB 2150 '<---------------------------------------------------- HEADER!
3750 PRINT "             ********** ANALYSIS & SPICE MOS3 **********" : PRINT
3760 VGG=VGSTR : VBB=VBSTR
3770 VDD=VDSTR : VSS=0 : TI=3 '<--------------------- ISUB(FORWARD) MEASUREMENT
3780 PRINT "MEASURING ISUB(forward)....   ";
3790 GOSUB 2800 : IBSTRF=-IDS : PRINT IBSTRF*1000000!;"[uA]"
3800 VSS=VDSTR : VDD=0 : TI=4 '<--------------------- ISUB(REVERSE) MEASUREMENT
3810 PRINT "MEASURING ISUB(reverse)....   ";
3820 GOSUB 2800 : IBSTRR=-IDS : PRINT IBSTRR*1000000!;"[uA]"
3830 VDD=VDSTR : VSS=0 : TI=1 '<---------------------- IDS(FORWARD) MEASUREMENT
3840 PRINT "       IDS (forward)....    ";
3850 GOSUB 2800 : IDSTRF=IDS : PRINT IDSTRF*1000!;"[mA]"
3860 VDD=VDSTR : VSS=0 : TI=2 '<---------------------- IDS(REVERSE) MEASUREMENT
3870 PRINT "       IDS (reverse)....    ";
3880 GOSUB 2800 : IDSTRR=IDS : PRINT IDSTRR*1000!;"[mA]"
3890 RETURN '<++++++++++++++++++++++++++++++++++++++++++++++++++ END OF SUB-PT1
3900 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
3910 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
3920 'SUB-PT2 : DATA ACQUISITION (ID-VD & ID-VG)*********************************
3930 VBB=0 : VSS=0 '<--------------------------------------- ID_VD MEASUREMENTS
3940 FOR TI=1 TO 2
3950 PRINT "              MEASURING ID-VD (Gdmin) ......";
3960 IF TI=1 THEN I1=1 : I2=5 : PRINT "(forward)"
3970 IF TI=2 THEN I1=5 : I2=5 : PRINT "(reverse)"
3980 FOR I=I1 TO I2
3990 VGG=I
4000 IF TI=1 THEN GDNF(I)=1E+10  ELSE GDNR(I)=1E+10
4010 FOR J=0 TO 50
4020 VDD=J*.1
4030 GOSUB 2800 : IF TI=1 THEN IDF(I,J)=IDS  ELSE IDR(I,J)=IDS
4040 IF I=5 THEN TI=TI+2 : GOSUB 2800  '<------------------------- MEASURE ISUB
4050 IF TI=3 THEN IBF(J)=-IDS : TI=1  '                          FORWARD
4060 IF TI=4 THEN IBR(J)=-IDS : TI=2  '                          REVERSE
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```
4070 IF J=0 THEN GOTO 4110
4080 IF TI=1 THEN GD=(IDF(I,J)-IDF(I,J-1))/.1 ELSE GD=(IDR(I,J)-IDR(I,J-1))/.1
4090 IF GD>0 AND TI=1 AND GD<GDNF(I) THEN GDNF(I)=GD : VGDNF(I)=VDD
4100 IF GD>0 AND TI=2 AND GD<GDNR(I) THEN GDNR(I)=GD : VGDNR(I)=VDD
4110 NEXT J
4120 GOSUB 2410 '<------------------------------------------------------ ZEROV!
4130 NEXT I
4140 GOSUB 2410 '<------------------------------------------------------ ZEROV!
4150 NEXT TI
4160 '------------------------- VDSAT CALCULATION ------------------------
4170 PRINT "       CALCULATING VDSAT(KAIST)......forward";
4180 TI=1 : VGG=5 : VBB=0 : VSS=0 : VKIST=2 : I1=35 : I2=45
4190 FOR J=1 TO 10
4200 X=0 : XX=0 : XY=0 : Y=0 : K=0
4210 FOR I=I1 TO I2
4220 IF I/10<=VKIST OR IBF(I)<=0 OR IDF(5,I)<=0 THEN GOTO 4250
4230 EE=1/(LOG(AI*(I/10-VKIST))-LOG(IBF(I))+LOG(IDF(5,I)))
4240 X=X+I/10 : XX=XX+(I/10)^2 : XY=XY+I/10*EE : Y=Y+EE : K=K+1
4250 NEXT I
4260 IF K<=2 THEN  GOTO 4280
4270 SLOPE=(K*XY-X*Y)/(K*XX-X^2) : YINT=(Y/K)-SLOPE*X/K : VKIST=-YINT/SLOPE
4280 NEXT J
4290 VDD=VKIST : GOSUB 2800 : VKKF=VDD : IKKF=IDS : GOSUB 2410
4300 PRINT VKKF;"[V]   ";IKKF*1000;"[mA]"
4310 PRINT "       CALCULATING VDSAT(KAIST)......reverse";
4320 TI=2 : VGG=5 : VBB=0 : VSS=0 : VKIST=2
4330 FOR J=1 TO 10
4340 X=0 : XX=0 : XY=0 : Y=0 : K=0
4350 FOR I=I1 TO I2
4360 IF I/10<=VKIST OR IBR(I)<=0 OR IDR(5,I)<=0 THEN GOTO 4390
4370 EE=1/(LOG(AI*(I/10-VKIST))-LOG(IBR(I))+LOG(IDR(5,I)))
4380 X=X+I/10 : XX=XX+(I/10)^2 : XY=XY+I/10*EE : Y=Y+EE : K=K+1
4390 NEXT I
4400 IF K<=2 THEN  GOTO 4420
4410 SLOPE=(K*XY-X*Y)/(K*XX-X^2) : YINT=(Y/K)-SLOPE*X/K : VKIST=-YINT/SLOPE
4420 NEXT J
4430 VDD=VKIST : GOSUB 2800 : VKKR=VDD : IKKR=IDS : GOSUB 2410
4440 PRINT VKKR;"[V]   ";IKKR*1000;"[mA]"
4450 '- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
4460 VDD=VDM : VSS=0 : VBB=0 '<------------------------------ ID_VG MEASUREMENTS
4470 FOR TI=1 TO 2
4480 PRINT "             MEASURING ID-VG (Gmmax) ......";
4490 IF TI=1 THEN PRINT "(forward)" ELSE PRINT "(reverse)"
4500 IF TI=1 THEN GMXF=0 ELSE GMXR=0
4510 FOR J=0 TO 50
4520 VGG=J*.1 : GOSUB 2800
4530 IF TI=1 THEN IMF(J)=IDS ELSE IMR(J)=IDS
4540 IF J=0 THEN GOTO 4580
4550 IF TI=1 THEN GM=(IMF(J)-IMF(J-1))/.1 ELSE GM=(IMR(J)-IMR(J-1))/.1
4560 IF GM>GMXF AND TI=1 THEN GMXF=GM : VGMXF=VGG
4570 IF GM>GMXR AND TI=2 THEN GMXR=GM : VGMXR=VGG
4580 NEXT J
```

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4590 GOSUB 2410 '<---------------------------------------------------------- ZEROV!
4600 NEXT TI
4610 KTH=INT(VGMXF*10) : X=0 : XX=0 : XY=0 : Y=0 : N=0
4620 FOR I=KTH-1 TO KTH+3
4630 X=X+I/10 : XX=XX+(I/10)^2 : XY=XY+(I/10)*IMF(I) : Y=Y+IMF(I) : N=N+1
4640 NEXT I
4650 SLOPE=(N*XY-X*Y)/(N*XX-X^2) : YINT=(Y/N)-SLOPE*X/N
4660 VTHFZ=(-YINT/SLOPE-VDD/2)
4670 KTH=INT(VGMXR*10) : X=0 : XX=0 : XY=0 : Y=0 : N=0
4680 FOR I=KTH-1 TO KTH+3
4690 X=X+I/10 : XX=XX+(I/10)^2 : XY=XY+(I/10)*IMR(I) : Y=Y+IMR(I) : N=N+1
4700 NEXT I
4710 SLOPE=(N*XY-X*Y)/(N*XX-X^2) : YINT=(Y/N)-SLOPE*X/N
4720 VTHRZ=(-YINT/SLOPE-VDD/2)
4730 RETURN '<+++++++++++++++++++++++++++++++++++++++++++++++++ END OF SUB-PT2
4740 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
4750 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
4760 'SUB-PT3 : DRAIN-DEPLETION CHARACTERISTICS*********************************
4770 PRINT "        ????????????????????????????-ANALYSIS......"
4780 VBB=0 : TI=1
4790 FOR I=1 TO NT STEP DNTF
4800 VDD=VT(I) : VSS=0
4810 IXX=IGG : GOSUB 3070 : VXTF(I)=VGXX
4820 VGG=VGXX : GOSUB 2800 : VGFF1=VGG : IDFF1=IDS
4830 IXX=INFS : GOSUB 3070 : VXXF(I)=VGXX
4840 VGG=VGXX : GOSUB 2800 : VGFF2=VGG : IDFF2=IDS
4850 IF IDFF2<=0 OR IDFF1<=0 OR IDFF2=IDFF1 THEN SXTF(I)=4444 : GOTO 4870
4860 SXTF(I)=(VGFF2-VGFF1)*1000/(LOG(IDFF2/IDFF1)/LOG(10)) '<---------- [mV/dec]
4870 NEXT I
4880 TI=2 : NDF=INT((NT-1)/DNTF+1) : NDR=INT((NT-1)/DNTR+1)
4890 FOR I=1 TO NT STEP DNTR
4900 VDD=VT(I) : VSS=0
4910 IXX=IGG : GOSUB 3070 : VXTR(I)=VGXX
4920 VGG=VGXX : GOSUB 2800 : VGFF1=VGG : IDFF1=IDS
4930 IXX=INFS : GOSUB 3070 : VXXR(I)=VGXX
4940 VGG=VGXX : GOSUB 2800 : VGFF2=VGG : IDFF2=IDS
4950 IF IDFF2<=0 OR IDFF1<=0 OR IDFF2=IDFF1 THEN SXTR(I)=4444 : GOTO 4970
4960 SXTR(I)=(VGFF2-VGFF1)*1000/(LOG(IDFF2/IDFF1)/LOG(10)) '<---------- [mV/dec]
4970 NEXT I
4980 GOSUB 2410 '<---------------------------------------------------------- ZEROV
4990 RETURN '<+++++++++++++++++++++++++++++++++++++++++++++++++ END OF SUB-PT3
5000 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
5010 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
5020 'SUB-PT4 : SUBTHRESHOLD SLOPE CHARACTERISTICS***************************
5030 PRINT "    SUBTHRESHOLD SLOPE MEASUREMENTS...."
5040 VDD=VDM : VSS=0 : VBB=0 : IXX=INFS
5050 TI=1 : GOSUB 3070 : VFSF=VGXX
5060 VGG=VFSF : GOSUB 2800 : VGFF1=VGG : IDFF1=IDS
5070 VGG=VFSF+.05 : GOSUB 2800 : VGFF2=VGG : IDFF2=IDS
5080 IF IDFF2<=0 OR IDFF1<=0 THEN VAF=4444 : GOTO 5100
5090 VAF=(VGFF2-VGFF1)/(LOG(IDFF2/IDFF1)/LOG(10))
5100 TI=2 : GOSUB 3070 : VFSR=VGXX
```

```
5110 VGG=VFSR : GOSUB 2800 : VGFR1=VGG : IDFR1=IDS
5120 VGG=VFSR+.05 : GOSUB 2800 : VGFR2=VGG : IDFR2=IDS
5130 GOSUB 2410 '<-------------------------------------------------------- ZEROV
5140 IF IDFR2<=0 OR IDFR1<=0 THEN VAR=4444 : GOTO 5160
5150 VAR=(VGFR2-VGFR1)/(LOG(IDFR2/IDFR1)/LOG(10))
5160 RETURN '<+++++++++++++++++++++++++++++++++++++++++++++ END OF SUB-PT4
5170 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
5180 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
5190 'SUB-PT6 : PEX (VTO, BETA, GAMMA)************************************
5200 PRINT "   PEX - PART 1 : (VTO, BETA, GAMMA)"
5210 TI=1 : NITFD=10
5220 VDD=VJPN : VSS=0 : IXX=ITH
5230 FOR I=1 TO NB
5240 VBB=VB(I) : GOSUB 3070
5250 VGG=VGXX+DVG1 : GOSUB 2800 : VGJPN(2*I-1)=VGG : IDJPN(2*I-1)=IDS
5260 VGG=VGXX+DVG2 : GOSUB 2800 : VGJPN(2*I)=VGG : IDJPN(2*I)=IDS
5270 NEXT I
5280 GOSUB 2410 '<-------------------------------------------------------- ZEROV
5290 APT=1+FB : PHIX=PHI : IT=0 : FD=7
5300 X=0 : XX=0 : XY=0 : YY=0 : Y=0 : P1=0 : P2=0 : P3=0 : N=0
5310 FOR I=1 TO 2*NB
5320 IF IDJPN(I)<=0 THEN GOTO 5380
5330 VBS=ABS(VB(INT((I+1)/2)))
5340 X(I)=VGJPN(I)-APT/2*VJPN : Z(I)=IDJPN(I)/VJPN
5350 Y(I)=SQR(VBS+PHIX)-SQR(PHIX)+VDD/8/SQR(VBS+PHIX)
5360 X=X+X(I) : Y=Y+Y(I) : XX=XX+X(I)^2 : YY=YY+Y(I)^2 : XY=XY+X(I)*Y(I)
5370 P1=P1+Z(I) : P2=P2+Z(I)*X(I) : P3=P3+Z(I)*Y(I) : N=N+1
5380 NEXT I
5390 A=X/N-XX/X : B=Y/N-XY/X : C=X/N-XY/Y : D=Y/N-YY/Y : E=B*C-A*D
5400 R11=(N*E-X*(B-D)-Y*(C-A))/(E*N^2)*P1
5410 R12=(Y/X*C-D)*P2+(X/Y*B-A)*P3 : R1=R11+R12/N/E
5420 R2=((B-D)*P1+N/X*D*P2-N/Y*B*P3)/N/E
5430 R3=((C-A)*P1-N/X*C*P2+N/Y*A*P3)/N/E
5440 VTO=-R1/R2 : BETA=R2 : GAMMA=-R3/R2 : VBS=0
5450 NSUB=(COX*GAMMA)^2/(2*KSI*EO*Q) : PHI=2*.0259*LOG(NSUB/NI)
5460 IF PHI<0 THEN PF=4 : PRINT "      PEX FAULT #";PF : GOSUB 3400
5470 XD=SQR(2*KSI*EO/Q/NSUB) : WD=XD*SQR(PHI+VBS+VJPN) : WS=XD*SQR(PHI+VBS)
5480 AWD=XJ/2/LEFF*(SQR(1+2*WD/XJ)-1) : AWS=XJ/2/LEFF*(SQR(1+2*WS/XJ)-1)
5490 FS=1-AWD-AWS : FM=DELSL/(PHI+VBS)/WEFF : FB=GAMMA/4/SQR(PHI+VBS)+FM
5500 IF LEFT$(STR$(PHI),FD)=LEFT$(STR$(PHIX),FD) THEN GOTO 5530
5510 PHIX=PHI : FD=FD-INT(IT/NITFD) : IT=IT+1
5520 IF FD>=3 THEN GOTO 5290 ELSE PF=1 : PRINT "      PEX FAULT #";PF
5530 IF PF>=1 THEN GOSUB 3400
5540 DELTA=DELSL*(2*COX)/(PI*KSI*EO)/PHI
5550 NFS=COX/Q*(VAF/.0259-1-GAMMA*(SQR(PHI+VBS)-SQR(PHI))/2/(PHI+VBS))
5560 PRINT "    : VTO[V]=";VTO;" BETA[A/V^2]=";BETA;" GAMMA =";GAMMA
5570 RETURN '<+++++++++++++++++++++++++++++++++++++++++++++ END OF SUB-PT6
5580 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
5590 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
5600 'SUB-PT7 : PEX (UO, THETA, VMAX)*************************************
5610 PRINT "   PEX - PART 2 : (UO, THETA, VMAX)"
5620 TI=1 : VBB=VBU : VSS=0 : VBX=ABS(VBB) : IT=1 : FD=6 : NITFD=10
```

```
5630 VTU=VTO+GAMMA*(SQR(VBX+PHI)-SQR(PHI))+FM*VBX
5640 FBU=GAMMA/(4*SQR(VBX+PHI))+FM : APU=1+FBU : UOX=UO
5650 X=0 : XX=0 : XY=0 : YY=0 : Y=0 : P1=0 : P2=0 : P3=0 : N=0
5660 FOR I=1 TO NU
5670 VGG=VU(I) : VDD=VU(I+NU)
5680 GOSUB 2800
5690 X(I)=VGG-VTU : Y(I)=VDD : N=N+1
5700 Z(I)=COX*WEFF/LEFF*(VGG-VTU-APU/2*VDD)*VDD/IDS
5710 X=X+X(I) : Y=Y+Y(I) : XX=XX+X(I)^2 : YY=YY+Y(I)^2 : XY=XY+X(I)*Y(I)
5720 P1=P1+Z(I) : P2=P2+Z(I)*X(I) : P3=P3+Z(I)*Y(I)
5730 NEXT I
5740 GOSUB 2410 '<------------------------------------------------------- ZEROV
5750 IF N<=2 THEN DF=10 : PRINT "    DEVICE FAULT #10" : GOSUB 3400
5760 A=X/N-XX/X : B=Y/N-XY/X : C=X/N-XY/Y : D=Y/N-YY/Y : E=B*C-A*D
5770 R11=(N*E-X*(B-D)-Y*(C-A))/(E*N^2)*P1
5780 R12=(Y/X*C-D)*P2+(X/Y*B-A)*P3 : R1=R11+R12/N/E
5790 R2=((B-D)*P1+N/X*D*P2-N/Y*B*P3)/N/E
5800 R3=((C-A)*P1-N/X*C*P2+N/Y*A*P3)/N/E
5810 UO=1/R1 : THETA=R2/R1 : VMAX=1/R3/LEFF  '<--------!!!!!!!!!! VMAX IN [cm/s]
5820 IF UO<0 THEN PF=100 : PRINT "    PEX FAULT #100"
5830 IF THETA<0 THEN PF=200 : PRINT "    PEX FAULT #200"
5840 IF VMAX<0 THEN PF=300 : PRINT "    PEX FAULT #300"
5850 IF PF<100 THEN GOTO 5900
5860 IF R1<0 THEN UO=BETA/COX/(WEFF/LEFF)
5870 IF R1<0 AND R2>0 THEN THETA=R2*UO
5880 IF R1>0 AND R2<0 THEN THETA=1.111E-05
5890 IF R3<0 THEN VMAX=BETA/DD/COX/WEFF
5900 PRINT "    UO[cm^2/V/s]=";UO;"  THETA[1/V]=";THETA;"  VMAX[m/s]=";VMAX/100
5910 RETURN  '<++++++++++++++++++++++++++++++++++++++++++++++ END OF SUB-PT7
5920 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
5930 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
5940 'SUB-PT8 : PEX (KAPPA)**************************************************
5950 PRINT "    PEX - PART 3 : (KAPPA)"
5960 TI=1 : KAPPA=0 : TKAP=0 : VBB=VBK : SATM=0 : VBK=ABS(VBB)
5970 VTK=VTO+GAMMA*(SQR(VBK+PHI)-SQR(PHI))+FM*VBK
5980 FOR I=1 TO NK
5990 VGK=VK(I)
6000 FBK=GAMMA/(4*SQR(VBK+PHI))+FM : APK=1+FBK
6010 US=UO/(1+THETA*(VGK-VTK))
6020 VAP=(VGK-VTK)/APK : VUS=VMAX*LEFF/US
6030 VDSAT=VAP+VUS-SQR(VAP^2+VUS^2)
6040 IF VGK<>5 OR SATM=1 THEN GOTO 6070
6050 VDSAT5=VDSAT : VDD=VDSAT : VGG=VGK : VBB=0 : VSS=0
6060 GOSUB 2800 : IDSAT5=IDS : SATM=1
6070 IF VDSAT>=VAP THEN VUS=100000! : VMAX=VUS/LEFF*US : VDSAT=VAP+VUS-
     SQR(VAP^2+VUS^2)
6080 IF VDSAT>0 AND VDSAT<VDSMAX THEN
     VDT2=(VGDNF(INT(VGK+.5))+VGDNF(INT(VGK-.5)))/2 : VDT1=(VDSAT+VDT2)*2/3 :
     GOTO 6120
6090 IF VDSAT<=0 THEN PRINT " ?!@#$%& OUT OF VDSAT (";VDSAT;")"
6100 IF VGDNF(5)>0 THEN VDT1=VGDNF(5)-1 : VDT2=VGDNF(5)
6110 IF VGDNF(5)<=0 THEN VDT1=VDSMAX-1 : VDT2=VDSMAX
```

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6120 '- - - - - - - - - - - - - - - - - - - - - - - - - - - - - VDSAT PASS LINE
6130 UEFF=US/(1+VDSAT/VUS)
6140 IDSATC=UEFF*COX*WEFF/LEFF*(VGK-VTK-APK/2*VDSAT)*VDSAT
6150 VBB=VBK : VGG=VGK : VDD=VDSAT : VSS=0
6160 GOSUB 2800 : IDSATM=IDS
6170 VDD=VDT1 : GOSUB 2800 : ISAT1=IDS
6180 VDD=VDT2 : GOSUB 2800 : ISAT2=IDS
6190 GOSUB 2410 '<----------------------------------------------------- ZEROV
6200 DIDS=IDSATC-IDSATM
6210 ISR1=ISAT1+DIDS : ISR2=ISAT2+DIDS
6220 DL1=LEFF*(1-IDSATC/ISR1) : DL2=LEFF*(1-IDSATC/ISR2)
6230 EPX=(VGK-VTK-APK/2*VDSAT)*VDSAT
6240 EP1=EPX/(VGK-VTK-APK*VDSAT-EPX/(VUS+VDSAT))/(LEFF-DL1)
6250 EP2=EPX/(VGK-VTK-APK*VDSAT-EPX/(VUS+VDSAT))/(LEFF-DL2)
6260 KAP1=DL1*(DL1+XD^2*EP1)/XD^2/(VDT1-VDSAT)
6270 KAP2=DL2*(DL2+XD^2*EP2)/XD^2/(VDT2-VDSAT)
6280 KAPPA=KAPPA+KAP1+KAP2 : TKAP=TKAP+2
6290 NEXT I
6300 KAPPA=KAPPA/TKAP
6310 PRINT "     KAPPA=";KAPPA;"          --- END OF PEX ---"
6320 RETURN '<++++++++++++++++++++++++++++++++++++++++++++++ END OF SUB-PT8
6330 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
6340 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
6350 'SUB-PT9 : PRINT-OUT ******************************************************
6360 PRINT "     PRINTING ......"
6370 LPRINT
6380 LPRINT "          >>>>>>>>>>>>>>>>>> HOT-CARRIER STRESS <<<<<<<<<<<<<<<<"
6390 LPRINT FIDE$
6400 LPRINT DUTID$,"Vds [V] / Vgs [V] =";VDSTR;"/";VGSTR;"   @ Vbs [V] =";VBSTR
6410 LPRINT "CYCLE #:";TK," (STRESS TIME [MIN]=";T(TK);")","File_Name:";DINA$
6420 LPRINT "TOTAL STRESS TIME [MIN] =";TTOTAL,TIME$,DATE$ : LPRINT
6430 LPRINT "FORWARD:  Isub [uA] =";IBSTRF*1000000!;"  Ids [mA] =";IDSTRF*1000
6440 LPRINT "REVERSE:  Isub [uA] =";IBSTRR*1000000!;"  Ids [mA] =";IDSTRR*1000
6450 LPRINT "Forward: Vdsat(KAIST) [V] =";VKKF;"  Idsat [mA] =";IKKF*1000!; " @ Vgs[V]=5"
6460 LPRINT "Reverse: Vdsat(KAIST) [V] =";VKKR;"  Idsat [mA] =";IKKR*1000!;"  @ Vgs[V]=5"
6470 LPRINT "IDSMAX (forward) [mA] =";IDF(5,50)*1000;"  IDSMAX (reverse) [mA]
    =";IDR(5,50)*1000!;"  @ Vds/Vgs=5/5"
6480 LPRINT "IDSLIN (forward) [mA] =";IMF(50)*1000;"  IDSLIN (reverse) [mA]
    =";IMR(50)*1000!;"  @ Vds/Vgs=0.1/5"
6490 LPRINT "VTH (forward) [V] =";VTHFZ,"VTH (reverse) [V] =";VTHRZ
6500 LPRINT "FORWARD : VA [mV/dec] =";VAF*1000;"  Vgs (@Ids=";INFS*1E+09;"[nA]) [V]
    =";VFSF
6510 LPRINT "REVERSE : VA [mV/dec] =";VAR*1000;"  Vgs (@Ids=";INFS*1E+09;"[nA]) [V]
    =";VFSR : LPRINT
6520 LPRINT "Gmmax(forward)[uS]=";GMXF*1000000!;"
    Gmmax(reverse)[uS]=";GMXR*1000000!;" @ Vds [V] =";VDM : LPRINT
6530 FOR I=1 TO 5
6540 LPRINT "Forward :  Gdmin(Vgs[V]=";I;")[uS]=";GDNF(I)*1000000!;" @Vds[V]=";VGDNF(I)
6550 NEXT I
6560 LPRINT "Reverse :  Gdmin(Vgs[V]=5)[uS]=";GDNR(5)*1000000!;" @Vds[V]=";VGDNR(5)
6570 LPRINT : LPRINT "DBCS(FORWARD) @ Ids1=";IGG*1E+09;"[nA],
    Ids2=";INFS*1E+09;"[nA]"
```

```
6580 LPRINT "Vds[V]","Vgs1[V]","Vgs2[V]","S[mV/dec]"
6590 FOR I=1 TO NT STEP DNTF
6600 LPRINT VT(I),VXTF(I),VXXF(I),SXTF(I)
6610 NEXT I
6620 LPRINT : LPRINT "DBCS(REVERSE) @ Ids1=";IGG*1E+09;"[nA],
     Ids2=";INFS*1E+09;"[nA]"
6630 LPRINT "Vds[V]","Vgs1[V]","Vgs2[V]","S[mV/dec]"
6640 FOR I=1 TO NT STEP DNTR
6650 LPRINT VT(I),VXTR(I),VXXR(I),SXTR(I)
6660 NEXT I
6670 LPRINT
6680 LPRINT "    ************> SPICE MOS3 PARAMETER EXTRACTION <**************"
6690 LPRINT "L [um] =";L*10000!,"W [um] =";W*10000!,
6700 LPRINT "LD [um] =";LD2/2*10000!,"WD [um] =";WD2/2*10000!
6710 LPRINT "TOX [nm] =";TOX*1E+07,"XJ [um] =";XJ*10000!
6720 LPRINT "VTO [V] =";VTO,
6730 LPRINT "PHI [V] =";PHI
6740 LPRINT "NSUB [#/cm^2] =";NSUB,
6750 LPRINT "NFS [#/cm^2] =";NFS
6760 LPRINT "DELTA  =";DELTA,
6770 LPRINT "GAMMA [1/V] =";GAMMA
6780 LPRINT "THETA [1/V] =";THETA,
6790 LPRINT "UO [cm^2/V/s] =";UO,"VMAX [m/s] =";VMAX/100
6800 LPRINT "KAPPA =";KAPPA,,"ETA =";ETA
6810 LPRINT "*******************************************************************"
6820 LPRINT "XD [um] =";XD*10000!
6830 LPRINT "VDSAT @ Vgs=5 [V] =";VDSAT5,"IDSAT [mA] =";IDSAT5*1000
6840 LPRINT "  : FB=";FB,"FS=";FS,,"FN [1/V] =";FM
6850 LPRINT "###################################################################"
6860 LPRINT : LPRINT : LPRINT
6870 RETURN '<++++++++++++++++++++++++++++++++++++++++++++++ END OF SUB-PT9
6880 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
6890 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
6900 'SUB-PT10 : SPICE SIMULATION ********************************************
6910 PRINT "          --------------- SPICE SIMULATION --------------"
6920 VBS=0 : FBP=GAMMA/(4*SQR(VBS+PHI))+FM : APP=1+FBP
6930 FOR I=1 TO 5
6940 VGS=I : PRINT "        SPICE SIM. ON PART:";I;"/5"
6950 FOR J=0 TO 50 STEP 2
6960 VDS=J*.1
6970 VTH=VTO+GAMMA*(SQR(VBS+PHI)-SQR(PHI))+FM*VBS-DD*VDS
6980 VGP=VGS-VTH : US=UO/(1+THETA*VGP)
6990 VUP=VMAX*LEFF/US : VSP=VGP/APP
7000 VDSATP=VSP+VUP-SQR(VSP^2+VUP^2)
7010 IF VGS<=VTH THEN IP(I,J)=0   : GOTO 7090
7020 IF VDSATP>=VDS THEN LEFFX=LEFF : GOTO 7070
7030 EPX=(VGP-APP*VDSATP/2)*VDSATP
7040 EPP=EPX/(VGP-APP*VDSATP-EPX/(VUP+VDSATP))/LEFF
7050 DLP=SQR((EPP*XD^2/2)^2+KAPPA*XD^2*(VDS-VDSATP))-(EPP*XD^2)/2
7060 VDS=VDSATP : LEFFX=LEFF-DLP
7070 UEFFP=US/(1+VDS/VUP)
7080 IP(I,J)=COX*WEFF/LEFFX*UEFFP*(VGP-APP*VDS/2)*VDS
```

```
7090 NEXT J
7100 NEXT I
7110 '- - - - - - - - - - - - - - - - - PLOT - - - - - - - - - - - - - - - - - -
7120 SCREEN 8
7130 KEY OFF : COLOR 7,1 : CLS
7140 YMAX=(INT(INT(IDF(5,50)*1000)/5)+1)/200
7150 XMAX=VDSMAX : XMIN=0 : YMIN=0
7160 FOR K=1 TO 5
7170 YG=150-(K-1)*25
7180 LINE (100,YG)-(600,YG)
7190 NEXT K
7200 FOR K=1 TO 6
7210 XG=100*K
7220 LINE (XG,150)-(XG,50)
7230 NEXT K
7240 XS=500/(XMAX-XMIN) : YS=100/(YMAX-YMIN)
7250 LOCATE 22,41 : PRINT "Vds [V]"
7260 LOCATE 21,60 : PRINT "dVds [V]=.1"
7270 FOR K=1 TO 6
7280 LOCATE 20,12*K+(K-2) : PRINT XMAX/5*(K-1)
7290 NEXT K
7300 LOCATE 6,13 : PRINT "Ids [A]"
7310 LOCATE 4,60 : PRINT "VgsH [V]=5"
7320 LOCATE 5,60 : PRINT "VgsL [V]=1"
7330 LOCATE 6,60 : PRINT "dVgs [V]=1"
7340 FOR K=1 TO 5
7350 LOCATE 4+3*K,7
7360 IF K<5 THEN PRINT (YMAX-YMIN)/4*(5-K) ELSE PRINT YMIN
7370 NEXT K
7380 LOCATE 3,20 : PRINT "SPICE MOS3 SIMULATION VS. MEASUREMENT"
7390 LOCATE 4,13 : COLOR 12,1 : PRINT " + measured"
7400 LOCATE 5,13 : COLOR 14,1 : PRINT " - SPICE sim."
7410 FOR I=1 TO 5
7420 FOR J=0 TO 50 STEP 2
7430 X2=100+XS*.1*J
7440 IF J<>2*INT(J/2) THEN GOTO 7500
7450 IF IP(I,J)<=0 THEN Y2=150 : GOTO 7470
7460 IF IP(I,J)>YMAX THEN Y2=50 ELSE Y2=150-YS*(IP(I,J)-YMIN)
7470 IF J=0 THEN X1=100 : Y1=150
7480 COLOR 14,1 : LINE (X1,Y1)-(X2,Y2)
7490 X1=X2 : Y1=Y2
7500 IF IDF(I,J)<=0 THEN YM=150 : GOTO 7520
7510 YM=150-YS*(IDF(I,J)-YMIN)
7520 COLOR 12,1
7530 LINE (X2-2,YM)-(X2+2,YM)
7540 LINE (X2,YM-1)-(X2,YM+1)
7550 NEXT J
7560 NEXT I
7570 IF SSS=1 OR FK1=1 THEN LOCATE 22,30 : INPUT JEFF
7580 KEY ON : SCREEN 0 : COLOR 14,1,2 : CLS
7590 RETURN '<++++++++++++++++++++++++++++++++++++++++++++++++ END OF SUB-PT10
7600 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
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7610 'XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
7620 'SUB-PT11 : FILE-SAVER
7630 GOSUB 2150 '<------------------------------------------------------- HEADER!
7640 PRINT "                    SAVING FILES ....."
7650 IF TK=0 AND FFF=1 THEN MKDIR DINA$
7660 LTK=LEN(STR$(TK))-1
7670 SC$="VDS="+STR$(VDSTR)+"[V], "+"VGS="+STR$(VGSTR)+"[V],
     "+"VBS="+STR$(VBSTR)+"[V]"
7680 FDD$="C:\DATA\"+FINA$+"\DD"+RIGHT$(STR$(TK),LTK)+".DAT"
7690 FMM$="C:\DATA\"+FINA$+"\MM"+RIGHT$(STR$(TK),LTK)+".DAT"
7700 FSP$="C:\DATA\"+FINA$+"\SP"+RIGHT$(STR$(TK),LTK)+".DAT"
7710 OPEN FDD$ FOR OUTPUT AS #1
7720 OPEN FMM$ FOR OUTPUT AS #2
7730 OPEN FSP$ FOR OUTPUT AS #3
7740 PRINT #1,FDD$,DUTID$,TIME$,DATE$
7750 PRINT #1,SC$
7760 PRINT #1,FIDE$;"    ID-VD CHARACTERISTICS"
7770 PRINT #1,"          ************************ FORWARD IDS [A]
     **********************",":REVERSE IDS [A]"
7780 PRINT #1,"VDS [V], ";"  VGS[V]=1,";"  VGS[V]=2,";"  VGS[V]=3,";"  VGS[V]=4,","
     VGS[V]=5,";" : VGS[V]=5(rev)"
7790 PRINT #2,FMM$,DUTID$,TIME$,DATE$
7800 PRINT #2,SC$
7810 PRINT #2,FIDE$;"    ID-VG CHARACTERISTICS"
7820 PRINT #2,"      FORWARD      REVERSE"
7830 PRINT #2,"VGS [V],";" IDSF [A],";" IDSR [A]"
7840 PRINT #3,FSP$,DUTID$,TIME$,DATE$
7850 PRINT #3,SC$
7860 PRINT #3,FIDE$;"    SPICE (MOS3) SIMULATION"
7870 PRINT #3,"        ********************* FORWARD IDS [A] **********************"
7880 PRINT #3,"VDS [V],","VGS[V]=1,","VGS[V]=2,","VGS[V]=3,","VGS[V]=4,","VGS[V]=5"
7890 FOR J=0 TO 50
7900 V=J*.1
7910 PRINT #1, USING "##.##, ";V;
7920 PRINT #2, USING "##.##, ";V;
7930 IF J=2*INT(J/2) THEN PRINT #3, USING "##.##, ";V;
7940 FOR I=1 TO 5
7950 PRINT #1,USING "##.####^^^^, ";IDF(I,J);
7960 IF I=1 THEN PRINT #2,USING "##.####^^^^, ";IMF(I);
7970 IF I=2 THEN PRINT #2,USING "##.####^^^^, ";IMR(I)
7980 IF J=2*INT(J/2) AND I<=4 THEN PRINT #3,USING "##.####^^^^, ";IP(I,J);
7990 IF J=2*INT(J/2) AND I=5 THEN PRINT #3,USING "##.####^^^^, ";IP(I,J)
8000 NEXT I
8010 PRINT #1,USING "##.####^^^^, ";IDR(5,J)
8020 PRINT #2, : PRINT #3,
8030 NEXT J
8040 CLOSE #1 : CLOSE #2 : CLOSE #3
8050 '- - - - - - - - - - - - - - - - - - - - - - - - -(PARAMETER EXTRACTION DATA FILE)
8060 IF TK>=1 THEN GOTO 9410
8070 FA1$="C:\DATA\"+FINA$+"\"+FINA$+".A1"
8080 FA2$="C:\DATA\"+FINA$+"\"+FINA$+".A2"
8090 FA3$="C:\DATA\"+FINA$+"\"+FINA$+".A3"
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```
8100 FA4$="C:\DATA\"+FINA$+"\"+FINA$+".A4"
8110 FA5$="C:\DATA\"+FINA$+"\"+FINA$+".A5"
8120 FD1$="C:\DATA\"+FINA$+"\"+FINA$+".D1"
8130 FD2$="C:\DATA\"+FINA$+"\"+FINA$+".D2"
8140 FD3$="C:\DATA\"+FINA$+"\"+FINA$+".D3"
8150 FD4$="C:\DATA\"+FINA$+"\"+FINA$+".D4"
8160 FD5$="C:\DATA\"+FINA$+"\"+FINA$+".D5"
8170 FD6$="C:\DATA\"+FINA$+"\"+FINA$+".D6"
8180 FS1$="C:\DATA\"+FINA$+"\"+FINA$+".S1"
8190 FS2$="C:\DATA\"+FINA$+"\"+FINA$+".S2"
8200 FS3$="C:\DATA\"+FINA$+"\"+FINA$+".S3"
8210 OPEN FA1$ FOR OUTPUT AS #1
8220 OPEN FA2$ FOR OUTPUT AS #2
8230 OPEN FA3$ FOR OUTPUT AS #3
8240 OPEN FA4$ FOR OUTPUT AS #4
8250 OPEN FA5$ FOR OUTPUT AS #5
8260 '------------- FILE #1 (.A1) : STRESS CONDITION --------------------------
8270 PRINT #1, DINA$, FA1$, DUTID$, TIME$, DATE$
8280 PRINT #1,SC$,"W/L=";W*10000!;"/";L*10000!
8290 PRINT #1,"    IDSMAX MEASUREMENT CONDITION : VDS[V]=5, VGS[V]=5, VBS[V]=0"
8300 PRINT #1,"Cycle #, ";"T[min], ";"ISBF[A], ";"IDSF[A], ";"ISBR[A], ";"IDSR[A],
     ";"IDSMAXF[A], ";"IDSMAXR[A]"
8310 '------------- FILE #2 (.A2) : GDMIN -------------------------------------
8320 PRINT #2, DINA$, FA2$, DUTID$, TIME$, DATE$
8330 PRINT #2,SC$,"W/L=";W*10000!;"/";L*10000!
8340 PRINT #2,"FORWARD MINIMUM DRAINCONDUCTANCE (Gdmin) WITH dVds=0.1V,
     VBS=0 : REVERSE"
8350 PRINT #2,"VGS[V]=1, ";"VGS[V]=2, ";"VGS[V]=3, ";"VGS[V]=4, ";"VGS[V]=5,
     ";":VGS[V]=5(rev)"
8360 '------------- FILE #3 (.A3) : VDS(GDMIN) --------------------------------
8370 PRINT #3, DINA$, FA3$, DUTID$, TIME$, DATE$
8380 PRINT #3,SC$,"W/L=";W*10000!;"/";L*10000!
8390 PRINT #3,"IDS(LIN)@VDS/VGS=0.1/5 : FORWARD VDS @ Gdmin ---- dVds=0.1V, VBS=0
     : REVERSE"
8400 PRINT #3,"IDSLIN(F)[A], ";"IDSLIN(R)[A], ";"VGS[V]=1, ";"VGS[V]=2, ";"VGS[V]=3,
     ";"VGS[V]=4, ";"VGS[V]=5, ";":VGS[V]=5(rev)"
8410 '------------- FILE #4 (.A4) : VDSAT/IDSAT & GMMAX -----------------------
8420 PRINT #4, DINA$, FA4$, DUTID$, TIME$, DATE$
8430 PRINT #4,SC$,"W/L=";W*10000!;"/";L*10000!
8440 PRINT #4,"VDSAT @ VGS=5V & VBS=0V   :   GMMAX @ VDS=0.1V & VBS=0V"
8450 PRINT #4,"VDSATF[V], ";"IDSATF[A], ";"VDSATR[V], ";"IDSATR[A], ";"GMMAXF[S],
     ";"VGMXF[V], ";"GMMAXR[S], ";"VGMXR[V]"
8460 '------------- FILE #5 (.A5) : SUBTHRESHOLD SLOPE -----------------------
8470 PRINT #5, DINA$, FA5$, DUTID$, TIME$, DATE$
8480 PRINT #5,SC$,"W/L=";W*10000!;"/";L*10000!
8490 PRINT #5,"INFS[nA]=";INFS*1E+09,"    MEASURED @ VDS=0.1V, VBS=0V"
8500 PRINT #5,"SUBTHRESHOLD CHARACTERISTICS"
8510 PRINT #5,"S(fwd)[mV/D], ";"VGS(fwd)[V], ";"S(rev)[mV/D], ";"VGS(rev)[V],
     ";"VTH(fwd)[V], ";"VTH(rev)[V]"
8520 '
8530 CLOSE #1 : CLOSE #2 : CLOSE #3 : CLOSE #4 : CLOSE #5
8540 OPEN FD1$ FOR OUTPUT AS #1
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8550 OPEN FD2$ FOR OUTPUT AS #2
8560 OPEN FD3$ FOR OUTPUT AS #3
8570 OPEN FD4$ FOR OUTPUT AS #4
8580 OPEN FD5$ FOR OUTPUT AS #5
8590 OPEN FD6$ FOR OUTPUT AS #6
8600 '------------- FILE #1 (.D1) : FORWARD DBCS : VGG1 ------------------------
8610 PRINT #1, DINA$, FD1$, DUTID$, TIME$, DATE$
8620 PRINT #1,SC$,"W/L=";W*10000!;"/";L*10000!
8630 PRINT #1,"IGG1[nA]=";IGG*1E+09,"   MEASURED @ VBS=0V"
8640 PRINT #1,"VGG1(fwd) : FORWARD DRAIN-BIASED CHANNEL SCANNING - DBCS(fwd)"
8650 N=0
8660 FOR I=1 TO NT
8670 PRINT #1,"VDS[V]=";VT(I);
8680 N=N+1 : IF N=NDF THEN PRINT #1, ELSE PRINT #1,", ";
8690 NEXT I
8700 '------------- FILE #2 (.D2) : REVERSE DBCS : VGG1 ------------------------
8710 PRINT #2, DINA$, FD2$, DUTID$, TIME$, DATE$
8720 PRINT #2,SC$,"W/L=";W*10000!;"/";L*10000!
8730 PRINT #2,"IGG1[nA]=";IGG*1E+09,"   MEASURED @ VBS=0V"
8740 PRINT #2,"VGG1(rev) : REVERSE DRAIN-BIASED CHANNEL SCANNING - DBCS(rev)"
8750 N=0
8760 FOR I=1 TO NT STEP DNTR
8770 PRINT #2,"VDS[V]=";VT(I);
8780 N=N+1 : IF N=NDR THEN PRINT #2, ELSE PRINT #2,", ";
8790 NEXT I
8800 '------------- FILE #3 (.D3) : FORWARD DBCS : VGG2 ------------------------
8810 PRINT #3, DINA$, FD3$, DUTID$, TIME$, DATE$
8820 PRINT #3,SC$,"W/L=";W*10000!;"/";L*10000!
8830 PRINT #3,"IGG2[nA]=";INFS*1E+09,"   MEASURED @ VBS=0V"
8840 PRINT #3,"VGG2(fwd) : FORWARD DRAIN-BIASED CHANNEL SCANNING - DBCS(fwd)"
8850 N=0
8860 FOR I=1 TO NT STEP DNTF
8870 PRINT #3,"VDS[V]=";VT(I);
8880 N=N+1 : IF N=NDF THEN PRINT #3, ELSE PRINT #3,", ";
8890 NEXT I
8900 '------------- FILE #4 (.D4) : REVERSE DBCS : VGG2 ------------------------
8910 PRINT #4, DINA$, FD4$, DUTID$, TIME$, DATE$
8920 PRINT #4,SC$,"W/L=";W*10000!;"/";L*10000!
8930 PRINT #4,"IGG2[nA]=";INFS*1E+09,"   MEASURED @ VBS=0V"
8940 PRINT #4,"VGG2(rev) : REVERSE DRAIN-BIASED CHANNEL SCANNING - DBCS(rev)"
8950 N=0
8960 FOR I=1 TO NT STEP DNTR
8970 PRINT #4,"VDS[V]=";VT(I);
8980 N=N+1 : IF N=NDR THEN PRINT #4, ELSE PRINT #4,", ";
8990 NEXT I
9000 '------------- FILE #5 (.D5) : FORWARD DBCS : Sub-SLOPE ------------------
9010 PRINT #5, DINA$, FD5$, DUTID$, TIME$, DATE$
9020 PRINT #5,SC$,"W/L=";W*10000!;"/";L*10000!
9030 PRINT #5,
9040 PRINT #5,"S[mV/dec] : FORWARD DRAIN-BIASED CHANNEL SCANNING - DBCS(fwd)"
9050 N=0
9060 FOR I=1 TO NT STEP DNTF
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9070 PRINT #5,"VDS[V]=";VT(I);
9080 N=N+1 : IF N=NDF THEN PRINT #5, ELSE PRINT #5,", ";
9090 NEXT I
9100 '------------- FILE #6 (.D6) : REVERSE DBCS : Sub-SLOPE ------------------
9110 PRINT #6, DINA$, FD6$, DUTID$, TIME$, DATE$
9120 PRINT #6,SC$,"W/L=";W*10000!;"/";L*10000!
9130 PRINT #6,
9140 PRINT #6,"S[mV/dec] : REVERSE DRAIN-BIASED CHANNEL SCANNING - DBCS(rev)"
9150 N=0
9160 FOR I=1 TO NT STEP DNTR
9170 PRINT #6,"VDS[V]=";VT(I);
9180 N=N+1 : IF N=NDR THEN PRINT #6, ELSE PRINT #6,", ";
9190 NEXT I
9200 CLOSE #1 : CLOSE #2 : CLOSE #3 : CLOSE #4 : CLOSE #5 : CLOSE #6
9210 'XXXXXXXXXXXXXXXX END OF FILE-.A# OPENNIG XXXXXXXXXXXXXXXXXXXXXX
9220 OPEN FS1$ FOR OUTPUT AS #1
9230 OPEN FS2$ FOR OUTPUT AS #2
9240 OPEN FS3$ FOR OUTPUT AS #3
9250 '------------- FILE #1 (.S1) : VTO,PHI,NSUB,NFS----------------------------
9260 PRINT #1, DINA$, FS1$, DUTID$, SC$, DATE$, TIME$
9270 PRINT #1,"SPICE MOS3 PARAMETERS ON HOT-CARRIER STRESS @
     VDS/VGS=";VDSTR;"/";VGSTR
9280 PRINT #1,"W[um]/L[um]=";W*10000!;"/";L*10000!;"
     LD[um]=";LD2/2*10000!,"WD[um]=";WD2/2*10000!
9290 PRINT #1,"TOX[nm]=";TOX*1E+07,"XJ[um]=";XJ*10000!
9300 PRINT #1," #, ";"T[min], ";"VTO[V], ";" PHI[V], ";" NSUB,       ";" NFS"
9310 '------------- FILE #2 (.S2) : DELTA,GAMMA,THETA,VMAX,UO------------------
9320 PRINT #2, DINA$, FS2$, DUTID$, SC$, DATE$, TIME$
9330 PRINT #2,"SPICE MOS3 PARAMETERS ON HOT-CARRIER STRESS @
     VDS/VGS=";VDSTR;"/";VGSTR
9340 PRINT #2," #, ";" DELTA, ";"  GAMMA, ";"  THETA, ";"  VMAX[m/s], ";"  UO[cm^2/V/s]"
9350 '------------- FILE #3 (.S3) : KAPPA,ETA,FB,FS,FN,XD ----------------------
9360 PRINT #3, DINA$, FS3$, DUTID$, SC$, DATE$, TIME$
9370 PRINT #3,"SPICE MOS3 PARAMETERS ON HOT-CARRIER STRESS @
     VDS/VGS=";VDSTR;"/";VGSTR
9380 PRINT #3,"KAPPA, ";"   ETA, ";"      FB, ";"       FS, ";"      FN[1/V], ";"      XD[um]"
9390 '
9400 CLOSE #1 : CLOSE #2 : CLOSE #3
9410 'XXXXXXXXXXXXXXXXXXXXXX END OF FILE OPENNING XXXXXXXXXXXXXXXXXXXX
9420 OPEN FA1$ FOR APPEND AS #1
9430 OPEN FA2$ FOR APPEND AS #2
9440 OPEN FA3$ FOR APPEND AS #3
9450 OPEN FA4$ FOR APPEND AS #4
9460 OPEN FA5$ FOR APPEND AS #5
9470 PRINT #1,USING"##., ######., ##.####^^^^, ##.####^^^^, ##.####^^^^, ##.####^^^^,
     ##.####^^^^, ##.####^^^^";TK,TTOTAL,IBSTRF,IDSTRF,IBSTRR,IDSTRR,IDF(5,50),
     IDR(5,50)
9480 PRINT #2,USING"##.####^^^^, ##.####^^^^, ##.####^^^^, ##.####^^^^, ##.####^^^^,
     ##.####^^^^";GDNF(1),GDNF(2),GDNF(3),GDNF(4),GDNF(5),GDNR(5)
9490 PRINT #3,USING"##.####^^^^, ##.####^^^^, ##.####, ##.####, ##.####, ##.####, ##.####,
     ##.####";IMF(50),IMR(50),VGDNF(1),VGDNF(2),VGDNF(3),VGDNF(4),VGDNF(5),VGDNR
     (5)
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9500 PRINT #4,USING"##.####, ##.####^^^^, ##.####, ##.####^^^^, ##.####^^^^, ##.####,
     ##.####^^^^, ##.####";VKKF,IKKF,VKKR,IKKR,GMXF,VGMXF,GMXR,VGMXR
9510 PRINT #5,USING"###.####, ##.####, ###.####, ##.####, ##.####,
     ##.####";VAF*1000!,VFSF,VAR*1000!,VFSR,VTHFZ,VTHRZ
9520 CLOSE #1 : CLOSE #2 : CLOSE #3 : CLOSE #4 : CLOSE #5
9530 OPEN FD1$ FOR APPEND AS #1
9540 OPEN FD2$ FOR APPEND AS #2
9550 OPEN FD3$ FOR APPEND AS #3
9560 OPEN FD4$ FOR APPEND AS #4
9570 OPEN FD5$ FOR APPEND AS #5
9580 OPEN FD6$ FOR APPEND AS #6
9590 N=0
9600 FOR I=1 TO NT STEP DNTF
9610 N=N+1
9620 IF N<NDF THEN PRINT #1,USING"##.####, ";VXTF(I);
9630 IF N<NDF THEN PRINT #3,USING"##.####, ";VXXF(I);
9640 IF N<NDF THEN PRINT #5,USING"###.####, ";SXTF(I);
9650 IF N=NDF THEN PRINT #1,USING"##.####";VXTF(I)
9660 IF N=NDF THEN PRINT #3,USING"##.####";VXXF(I)
9670 IF N=NDF THEN PRINT #5,USING"###.####";SXTF(I)
9680 NEXT I
9690 N=0
9700 FOR I=1 TO NT STEP DNTR
9710 N=N+1
9720 IF N<NDR THEN PRINT #2,USING"##.####, ";VXTR(I);
9730 IF N<NDR THEN PRINT #4,USING"##.####, ";VXXR(I);
9740 IF N<NDR THEN PRINT #6,USING"###.####, ";SXTR(I);
9750 IF N=NDR THEN PRINT #2,USING"##.####";VXTR(I)
9760 IF N=NDR THEN PRINT #4,USING"##.####";VXXR(I)
9770 IF N=NDR THEN PRINT #6,USING"###.####";SXTR(I)
9780 NEXT I
9790 CLOSE #1 : CLOSE #2 : CLOSE #3 : CLOSE #4 : CLOSE #5 : CLOSE #6
9800 OPEN FS1$ FOR APPEND AS #1
9810 OPEN FS2$ FOR APPEND AS #2
9820 OPEN FS3$ FOR APPEND AS #3
9830 PRINT #1,USING"##.#, #####.#, ##.####, ##.####, ##.####^^^^,
     ##.####^^^^";TK,TTOTAL,VTO,PHI,NSUB,NFS
9840 PRINT #2,USING"##.#, ##.####, ##.####, ##.####, ##.####^^^^,
     ####.####";TK,DELTA,GAMMA,THETA,VMAX/100,UO
9850 PRINT #3,USING"##.####, ##.####^^^^, ##.####^^^^, ##.####, ##.####^^^^,
     ##.####";KAPPA,ETA,FB,FS,FM,XD*10000!
9860 CLOSE #1 : CLOSE #2 : CLOSE #3
9870 RETURN '<++++++++++++++++++++++++++++++++++++++++++++END OF SUB-PT11
9880 '***************************** END OF PROGRAM ******************************
9890 '$$$$$$$$$$$$$$$$$$$$$$$$ NO MORE BEYOND THIS LINE $$$$$$$$$$$$$$$$$$$$$$$$$$$$
9900 '*******************************************************************************
□
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