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David J. Allstot

In recent years, there has been an extensive effort to develop low-cost implementations of radio frequency integrated circuits for consumer applications. This thesis is a research effort in the design and implementation of integrated RF CMOS Power Amplifiers (PAs). A significant challenge in the implementation of RF CMOS ICs is the impact of device, package and passive element parasitics on circuit performance. Passive components are a critical part of any RF IC design, and a process optimized for digital circuits results in inductors and capacitors with very high parasitics. In this work, we have developed a compact model for inductors fabricated in a digital CMOS process. Measured results have been used to further refine the accuracy of the inductor model. This model has been used to predict the impact of inductor parasitics on the performance of RFICs, and is also simple enough to be included in a CAD tool for circuit optimization. We have also studied the operation of Class A, B and C power amplifiers and highlighted design issues which are specific to the implementation of *integrated* PAs. It is shown that inductor loss has the most critical impact on the performance of integrated PAs. A custom CAD tool, based on the simulated annealing algorithm, has been developed to optimize the performance of power amplifiers for maximum efficiency in the presence of package, device and passive element parasitics. This CAD tool

simulates the process of load-pull to determine the optimum *large-signal* load impedance for the PA, and optimizes the matching network design based on *the trade-off between the loss in the matching network and its impedance transformation properties.* This trade-off is relevant in the case of high-loss matching networks only, as is the case in integrated RF CMOS ICs. This CAD tool has been used to optimize the efficiency of balanced 100mW CMOS PAs operating at 900MHz. Measured results validate the design and optimization process outlined in this work.

It is demonstrated that in the design of RF CMOS ICs, significant benefits can be gained by incorporating parasitics into the design process by means of CAD optimization. The CAD tool developed is an effort towards achieving this goal. It is further proposed that CAD optimization is an essential part of the design of RF CMOS ICs in general, and with the development of improved package, device and passive element models, CAD optimization will replace the "tuning" of RF circuits and result in robust, fully-integrated implementations of RF circuits.

Design and Computer-Aided Optimization of RF CMOS Power Amplifiers

by

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DESIGN AND COMPUTER-AIDED OPTIMIZATION OF RF CMOS POWER AMPLIFIERS

1. INTRODUCTION

The recent explosion in consumer applications for radio frequency and wireless systems has resulted in an extensive research and design effort to develop low-cost implementations of RF integrated circuits. Cellular and cordless phones, pagers, wireless local-area networks and wireless modems, wireless computer peripherals, and RF ID tags are just a few examples of devices which are becoming a part of everyday life. With this market projected to exceed several tens of billions of dollars annually [1], the economics is driving an intense effort to develop improved architectures for transmitters/receivers, as well as reduce implementation costs by utilizing low cost technology. Higher degree of integration in transceiver architectures, with the aim of realizing a single chip radio, is also a sought after goal of this research effort. A wide variety of system standards have been adopted in different parts of the world to support various applications. These standards differ in the modulation schemes they employ, in the frequency band they assign for transmitting and receiving wireless signals, in the multiplexing techniques employed, in the pulse-shaping filters used, etc. (see, for example, [2]). Operating frequency bands exist in the 800MHz-900MHz range, in the 1.8GHz range, and in the 2.4GHz frequency range. Modulation schemes employed include analog FM (in the relatively older, analog AMPS standard) as well as a variety of digital schemes like $\pi/4$-DQPSK, GMSK, FSK, etc. Multiple access may be either time domain (time-division multiplexing) or frequency domain (frequency-division multiplexing). The various standards impose varying operating specifications on the circuits employed in transceivers, especially at the RF front end. The transceiver architectures further impose additional functional or performance requirements in the building blocks

of modern-day RF transceivers. Due to the multiplicity of standards prevailing today, there is an effort to develop universal phones and other products, with the functionality to work with a variety of standards all over the world. As a consequence of these factors, todays wireless transceivers generally tend to be relatively complex systems, and require circuits performing a variety of functions.

1.1 Common RF Front-End Circuits

Some of the building blocks constituting the RF front-end of most of the modern day transceivers include power amplifiers (PAs), band-pass filters, low-noise amplifiers (LNAs), down-conversion and up-conversion mixers, frequency synthesizers, and transmit/receive switches. Power amplifiers are part of the transmitter front-end, and are used to amplify the signal being transmitted in order that the signal can be received and decoded by the receiver within a fixed geographical area. Output power levels range from a few milliwatts to several watts, depending upon the application. These amplifiers tend to be a major source of power dissipation in transmitters, and their power efficiency is critical to the battery-life of mobile units. Some modulation schemes allow using non-linear power amplifiers since the signal to be amplified has a constant envelope. An example of such a modulation scheme is GMSK modulation, which uses a gaussian pulse shaping filter to reduce the bandwidth of the transmitted signal. However, other modulation schemes require linear amplification of the transmitted signal. π-4 DQPSK modulation, used with a raised-cosine pulse-shaping filter to reduce signal bandwidth without causing inter-symbol interference, results in a non-constant envelope modulation signal, and requires linear power amplifiers. Linear power amplifiers tend to have much lower efficiency than non-linear amplifiers. Limiting the bandwidth of the transmitted signal is essential to avoid interference with signals in adjacent channels. FCC imposed masks are used to determine the requirements for the spectrum of the transmit

signal. Figure 1.1 shows a π-4 QPSK modulated signal, generated using MATLAB. A raised-cosine filter, with an α value of 0.5, is used for pulse shaping. As can be observed, the amplitude of the signal is not constant. These variations in the envelope result due to the band-limiting of this signal, performed by the raised-cosine filter. These variations in the envelope need to be preserved in the transmitted signal in order for it to retain its band-limited spectrum.

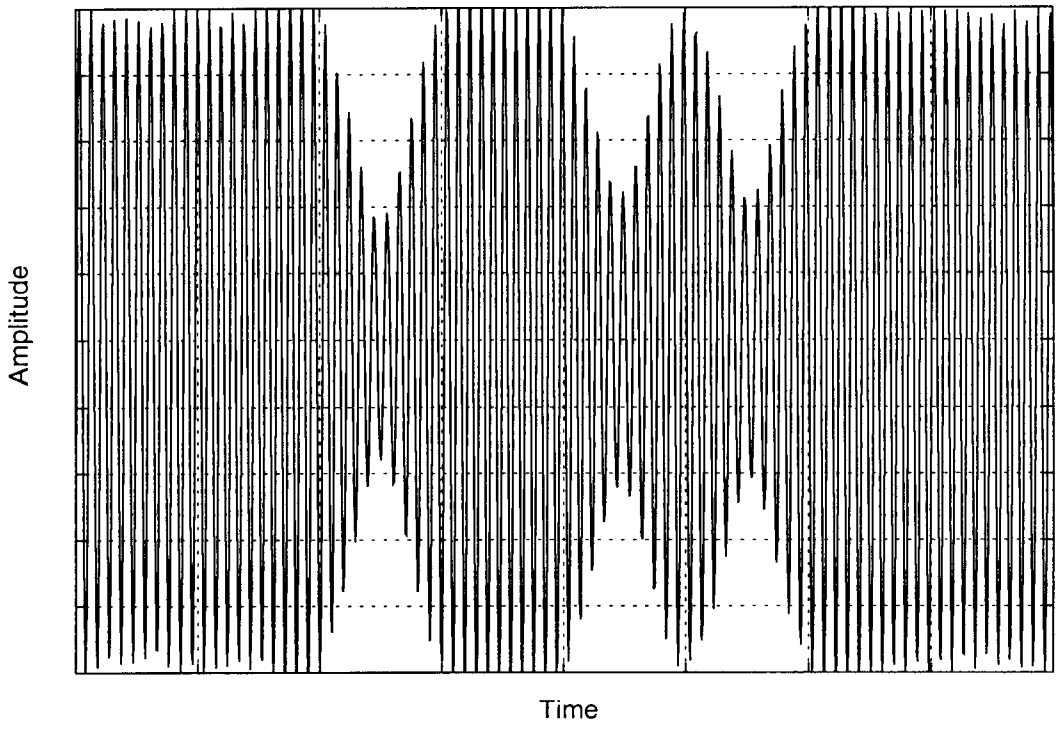

Figure 1.1 A π-4 QPSK modulated signal with raised-cosine pulse shaping, in the time domain.

Figure 1.2 illustrates the impact of a non-linear power amplifier on the spectrum of this signal. It shows the spectrum of a transmitted signal in two cases - using a linear power amplifier and using a non-linear power amplifier. Spectral regrowth in the transmit signal spectrum is evident in the case of the non-linear power amplifier. The increased

energy in the transmit signal, outside of its transmit channel, degrades signal quality in the other transmit/receive channels (hence the requirement for an FCC regulated mask). In contrast, Figure 1.3 is a plot of the transmit signal waveform for a GMSK modulated signal, using a gaussian pulse-shaping filter. Due to the nearly constant envelope of this signal, non-linearities in the power amplifier have negligible impact on the spectrum of this signal. Since non-linear power amplifiers consume less battery power compared to linear power amplifiers for a given RF power output, their use in transmitters is highly desirable. For a power amplifier, its efficiency, power output, power gain and linearity are important design specifications. Appendix I includes the code used to generate these plots.

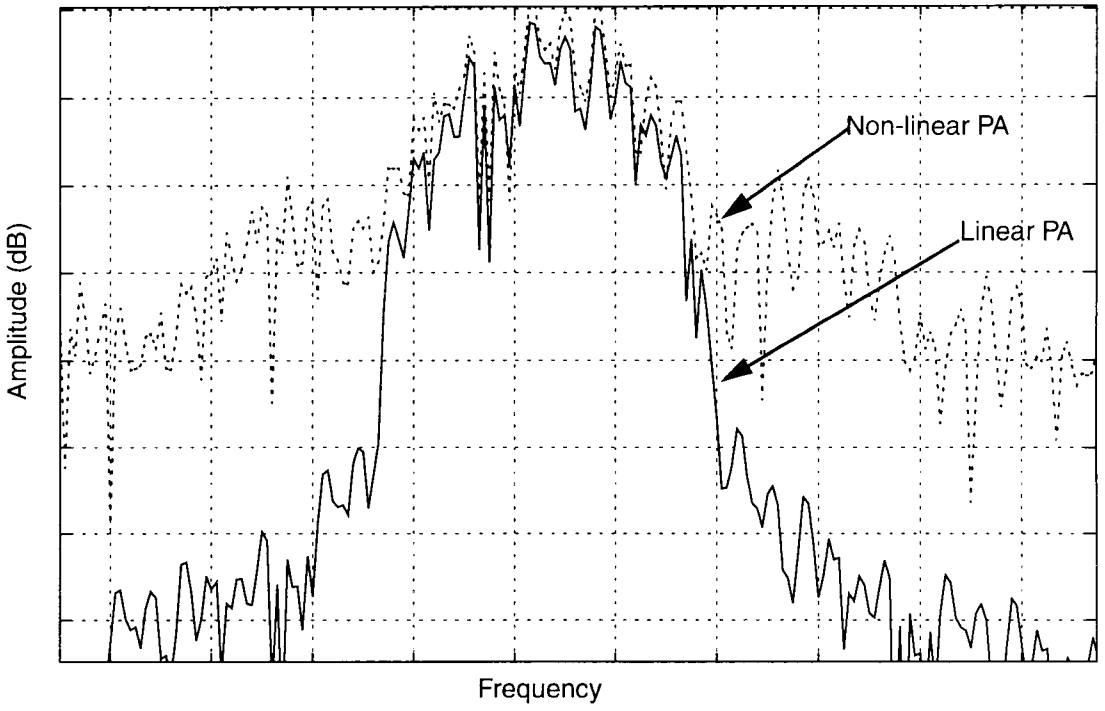

Figure 1.2 Effect of a non-linear power amplifier on the spectrum of a non-constant envelope transmit signal.

Bandpass filters are employed in the RF front end for a variety of purposes. They are used to limit the spectrum of the transmitted signal, and in this case are placed between the power amplifier and the antenna. They are also used as image-reject filters in, for example, a super-heterodyne receiver. In such a receiver, a mixer is used to down-convert the RF frequency signal to an IF, or intermediate frequency. However, there are *two* frequencies which the mixer will multiply down to the IF frequency - the signal frequency and another frequency, related to the signal frequency and the LO frequency, referred to as the image frequency. Since the image frequency signal is an interferer, an image-reject filter is used *prior* to mixing (usually immediately following the receiver antenna) to attenuate the amplitude of the received signal at the image frequency. The passband of the image-reject filter is set to allow the transmit signal to pass, and its Q-factor is high enough so as not to allow the image frequency to fall in its passband.

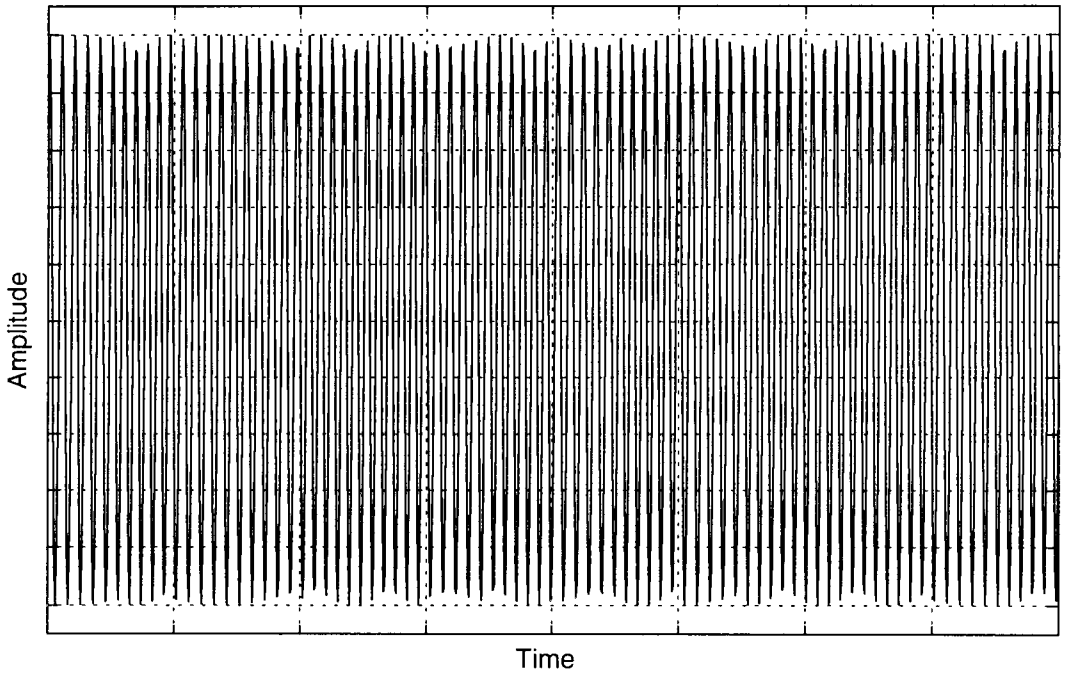

Figure 1.3 A GMSK modulated signal in the time domain with gaussian filter pulse shaping.

Another requirement for filtering is immediately following the mixing, to eliminate one of the two signals which, in general, result at the output of the mixer (the sum and difference of the RF and LO frequencies).

Low-noise amplifiers are critical to the receiver RF front end, and serve to extract the extremely low power RF signal from the noise prevalent in the atmosphere. They are used to amplify the RF signal level, without causing significant degradation in the signal-to-noise ratio, or SNR, of the received signal. A measure of the noise these amplifiers add to the signal, in addition to the noise which is already part of the received signal, is the noise-figure (NF) of the amplifier. The NF, along with the *power* gain of the low-noise amplifier, primarily determine the NF of the entire receiver, and therefore are critical to the sensitivity of the receiver. The sensitivity of a receiver is a measure of minimum signal level that the receiver can detect which results in an acceptable SNR. Some of the key specifications for low-noise amplifiers are noise figure, power gain, reverse isolation and linearity.

Mixers are used in both transmitters and receivers. In the transmitter, they are used to up-convert a low-frequency signal to higher frequency. Again, depending upon the receiver architecture being employed, this involves converting either a baseband signal to IF, or an IF signal to a higher IF or to RF for transmission. In the receiver, mixers perform the reverse operation of down-converting a high frequency signal to a lower frequency. An exception is the sub-sampling receiver, where no mixing is required to recover the baseband signal from the received RF signal. Isolation between various ports of the mixer, its conversion gain, linearity and power dissipation are critical in the design of mixers. Note that minimizing the power dissipation is a significant goal not just in mixer design but in the design of all RF building blocks using active components.

Frequency synthesizers are used to provide the LO signal for up-conversion or down-conversion. Frequency synthesizers for transceivers are one of the most challenging blocks to design due to the stringent performance requirements imposed on them in

terms of spectral purity, frequency accuracy, and the small step size by which the output frequency is required to vary in order to select different channels. They are implemented either as a phase-locked loop or use direct digital synthesis (DDS). PLLs use phase-locking to generate an output frequency from a reference frequency. DDS involves generating a digitally sampled version of the desired frequency signal, followed by a D/A converter to obtain the corresponding analog waveform. Depending upon the transceiver architecture, sometimes two signals at a given frequency are required, with a relative phase shift of 90^{o} between them. Referred to as I and Q signals, they are often generated from the given frequency synthesizer by using quad-generator circuits. Examples of quad-generators are polyphase filters, and an RC-CR network. A differential ring oscillator in a PLL has also been used to provide both I and Q signals.

A transmit switch, or duplexer, is used to switch between the transmit and receive functions of the transceiver. The loss in the switch, as well as the isolation it provides between the transmit and receive path are important specifications for transmit switch design. Figure 1.4 shows the block diagram of a heterodyne transceiver with the various building blocks discussed above.

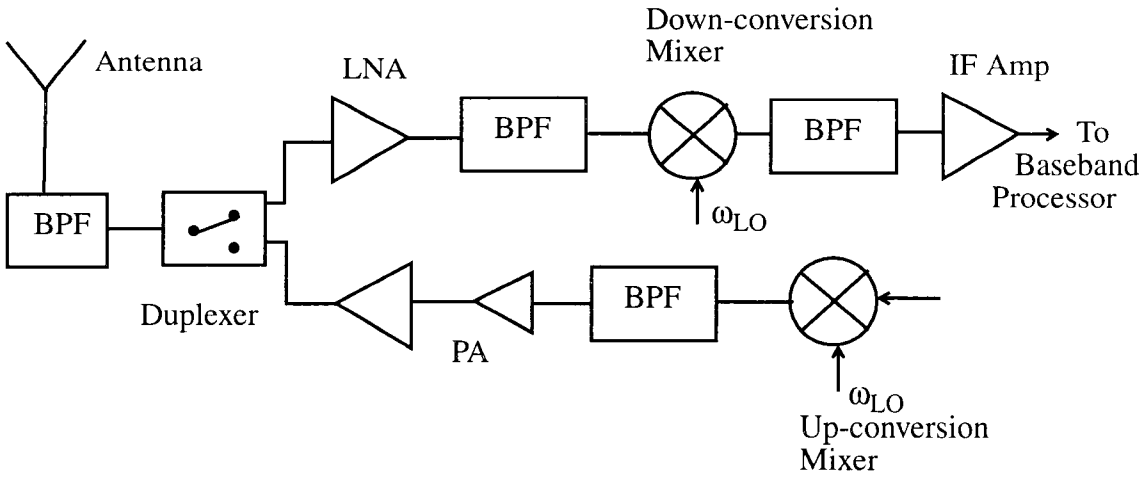

Figure 1.4 A block diagram of the RF part of a heterodyne transceiver.

1.2 Typical Implementations of Power Amplifiers

As is evident from the above section, a typical RF front-end requires a wide variety of circuits with stringent performance specifications. It is the purpose of this work to study the design and implementation of power amplifiers for RF transmitters. In this section, we will review some of the existing implementations of PAs. TQ9142 and TQ9143 are three-stage and two-stage PA ICs from TriQuint Semiconductor [3]. They are designed to supply 1.4W into a 50Ω load in the frequency band of 824MHz - 849MHz. TQ9142 is specified to operate from a nominal 5.8V supply and TQ9143 from a nominal 4.6V supply. Both these designs utilize an off-chip output matching network and require several external bias voltages for various stages of the power amplifier. They have a rated PAE of 60%, and a power gain of 30dB. These amplifiers exhibit impressive performance, but are also relatively high-cost since they are fabricated in GaAs technology. Thus, the availability of low-loss passives as well as GaAs transistors with high gain at RF frequencies results in an implementation with a high degree of integration and impressive performance, at the expense of higher cost of implementation and reduced ability for the integration of the entire system onto a single chip.

LDMOS devices have also been extensively used in RF power amplifier applications [4]-[5]. A wide variety of LDMOS power amplifier transistors, as well as power amplifier modules based on LDMOS transistors are available from Motorola Inc. MRF9745T1 is a LDMOS power FET available from Motorola [6] in a surface mount package which is capable of supplying greater than 1W at 900MHz with 55% drain efficiency from a 5.8V power supply. It has a power gain of 10dB. Similarly, MXR9745T1 and MXR9745RT1 are LDMOS power transistors capable of supplying 1.4W power at 900MHz with a 60% drain efficiency and with 8.5dB power gain, from a 6V power supply. By using a suitable driver amplifier cascaded to a power LDMOS FET, it is possible to realize power amplifier modules with high efficiency. A 4.8V, 2.7W, 440MHz power

amplifier module with a gain of 32dB, using LDMOS transistors, has demonstrated a power-added efficiency (PAE) of 55% [7]. However, the degree of integration for this three-stage amplifier is not as high as the GaAs implementations outlined earlier, with both the bias as well as interstage and output matching networks being off-chip. Also, it is worth noting that LDMOS is not among the general purpose, low cost digital silicon technologies.

A GaAs MESFET implementation of a Class-E PA, with a Class-F driver, is described in [8]. This non-linear power amplifier outputs 250mW at 835MHz with a power-added efficiency of 50%, and operates from a 2.5V power supply. Bias voltages are provided externally. However, this amplifier has a high degree of integration, with all the matching networks being implemented on-chip also. The integrated output matching network reduces the efficiency from 75% (for an off-chip matching network) to 50%. The availability of low-loss passives in GaAs technology suggests that the reduction in efficiency may not be entirely due to loss in the output matching network, but also due to a sub-optimal design of the output matching network, in the presence of both the transistor as well as inductor and capacitor parasitics.

A 1W BiCMOS power amplifier is reported in [9]. This 830MHz PA has a measured PAE of 30%, and operates from a 5V power supply. While biasing for the different stages is provided on-chip, the matching networks are not completely integrated. External inductors are used as part of inter-stage matching networks, with the output matching network being completely off-chip. Measurement results are reported for a chip-on-board die. The process used for this PA is a high-speed BiCMOS process from Philips Semiconductor. While BiCMOS is capable of supporting other RF transceiver functions and is a strong candidate for a low-cost technology for realizing a single-chip radio, the reduction in performance of a BiCMOS PA compared to a GaAs implementation is clearly evident.

Due to the high volume of digital ICs using CMOS technology, digital CMOS is an extremely attractive candidate for realizing low-cost RF circuits. However, this process is geared towards optimizing digital circuit performance which imposes severe restrictions upon realizing high-performance RF circuits in this technology. Any process modifications aimed at improving RF circuit performance tends to increase cost, thereby reducing the primary advantage of digital CMOS over other RF technologies. However, CMOS power amplifiers have been reported recently [10]-[11]. A balanced 20μW-20mW, 900MHz CMOS power amplifier is described in [10]. It works from a 3V power supply, and has a measured drain efficiency of 25%. No input matching is used (an input matching network is not required if the PA is integrated with the remaining transmitter circuitry), and the output matching network is off-chip. Process modifications are used to obtain a high Q inductor for realizing a tuned amplifier to drive the PA output stage. This PA is realized in a 1μm CMOS technology. A 2.5V, 1W CMOS PA for operation in the 800-900MHz band is described in [11]. The final stage of this multistage amplifier is implemented as a Class-D stage, with the transistor used as a switch. This amplifier has a measured drain efficiency of 62%, and a PAE of 42%, but does not have a high degree of integration, with the input and output matching network being off-chip. Bond wires are also used as part of the interstage matching networks. This PA, however, does indicate that even though the inductors and capacitors that may be realized in CMOS technology are not suitable for RF circuits requiring high performance, CMOS transistors do have adequate gain at 1GHz to allow the design of low-cost hybrid (not monolithic) 1W amplifiers. Of course, the performance is still not comparable to GaAs or LDMOS but the advantage is in the cost of implementation.

1.3 Future Trends: System on a chip

"Compared to other types of integrated circuits, the level of integration in the RF sections of such transceivers is still relatively low. Considerations of power dissipation, form factor, and cost dictate that the RF/IF portions of these devices evolve to higher levels of integration than is true at present." - P.R. Gray and R.G. Meyer [12].

"Let us say the goal of industry is to lower the cost, power dissipation, weight, and size of the portable cellular phone so that it eventually reduces to the size of a credit card. This translates to a minimum number of (off-chip) components; low-power dissipation, especially in the PA and baseband DSP(s); and fewer batteries." - B. Razavi [13].

As is evident from above, highly integrated RF transceivers in a low-cost, mainstream technology are very attractive for a number of reasons - the small size and weight of the resulting wireless product is attractive for consumers, the absence of the need to match the input and output of RF circuits to 50Ω eliminates the power-hungry buffers required to drive this load impedance [14], long-term reliability will improve as the number of components is reduced, and it is possible the integrated transceiver implementation will result in a lower cost than a discrete implementation. At this time, however, there are still several hurdles which need to be overcome before a single-chip radio becomes a reality. Before the integration of transceivers becomes practical, it is required to fully integrate the various building blocks that constitute an RF transceiver. Circuit design techniques need to be developed, and are being researched, which result in fully-integrated RF circuits with acceptable performance for, at the very least, applications at the low-end of the wireless spectrum, i.e., maybe not cellular telephones but cordless phones or wireless computer peripherals, etc. Apart from integration of individual building blocks, a fully integrated transceiver requires other design considerations involving interaction of the various RF circuits in an integrated environment.

CAD tools need to be developed to aid the designer in evaluating and predicting substrate interactions, minimize the impact of parasitics on RF circuits, evaluate cross-talk, etc. Other than circuit techniques, integrated transceivers can also become a reality with the development of modulation schemes, transceiver architectures, etc., which may relax the performance requirements from the RF front end. An example of this is the possibility of realizing a fully integrated power amplifier in a low-cost technology like digital CMOS if the required power output were in the range of few tens of milliwatts [13]. This would require a smaller cell-size for the wireless system, and is referred to as the microcell or picocell approach.

1.4 Integrated CMOS RF Power Amplifiers

It is clear that realizing highly integrated transceivers is desirable for a number of reasons. It is equally obvious from section 1.2 that power amplifier implementations are either in an RF specific (and consequently high cost) technology with a reasonably high degree of integration, or in a low-cost technology with not only poor performance compared to LDMOS or GaAs, but also significantly reduced level of integration. It is also worth noting that fully integrated PAs for cellular applications have not been realized in any technology, either due to the limitations imposed by the technology in terms of losses in inductors and capacitors, or due perhaps to the lack of CAD tools which would allow the design of integrated power amplifiers. It is the goal of this work to explore the design of fully-integrated RF power amplifiers in a digital CMOS technology. Due to the high loss in the inductors and capacitors available in such a process, an attempt has been made to integrate a PA with an output power of 100mW. It is proposed that while digital CMOS does not offer the same high performance as GaAs or LDMOS, lower-cost and completely integrated implementations can be realized using this technology. While the output power level is not adequate for cellular applications,

numerous other applications exist which require output power in this range. It should be feasible to realize fully integrated transceivers, including power amplifiers, for such applications by utilizing the design approach followed in this work.

An inductor is a very significant element in the design of RF circuits. Integrated RF circuits have been reported which make extensive use of integrated inductors [15]-[19] as well as integrated transformers [20]-[21]. A realistic inductor model can greatly enhance the capability of a circuit designer to optimize RF circuits. Chapter 2 deals with the modeling of planar spiral inductors on a high-loss substrate such as found in a digital CMOS technology. While some models exist in the open literature for inductors fabricated on silicon [22]-[24], the emphasis in this work has been to develop an inductor model which is simple enough, but reasonably accurate, to be included in a CAD tool for optimization of circuit performance. Measurement results have been used to validate the modeling approach and to refine the predictions of the model. Chapter 3 discusses the operation and design of Class A, B, AB and C power amplifiers. Issues relevant in an integrated environment are discussed, and the impact of various parasitics on a fully integrated implementation of the above class of power amplifiers is highlighted by means of a design example. This chapter further motivates the need for CAD optimization of fully integrated RF power amplifiers. Chapter 4 describes a CAD tool which has been developed to aid in the design of integrated CMOS RF power amplifiers. The simulated annealing algorithm, upon which this CAD tool is based, is also described in this chapter. This CAD tool is used to optimize the design of two integrated, 100mW, balanced, 900MHz CMOS RF power amplifiers working from a 3V power supply. The details of these designs are also included in this chapter. This CAD tool is an effort towards realizing design aids which would make possible replacing the manually tuned RF circuits that dominate today with robust, fully integrated implementations. Chapter 5 gives details of the layout of the power amplifiers and inductors fabricated as part of this work, as well as measurement results for a pair of integrated inductors and one of

the designed power amplifiers. These results validate the design technique outlined in this work. Finally, chapter 6 includes some conclusions which were inferred from the results of this work, and outlines possibilities for the continuance of this effort in realizing other power amplifiers.

2. INDUCTOR MODELING AND CHARACTERIZATION

The losses associated with inductors fabricated on a high loss silicon substrate are significant, and any successful circuit design utilizing such monolithic inductors should, by necessity, incorporate a realistic inductor model as part of the design process. A good circuit model for inductors on silicon greatly benefits the circuit designer in predicting the performance of the circuit, as well as in optimizing it. The common approaches to developing an inductor model have been either the fabrication of inductors and subsequent fitting of the measured response to an equivalent circuit [25], or the performance of time-consuming electromagnetic simulations. However, in either case, the designer does not have the freedom to optimize the design for a different inductance value, without repeating the above process. In this chapter, we present a simple method for obtaining the impedance of an inductor at different frequencies, taking into account various parasitics associated with it. Our approach is similar to the approaches followed in [26]-[28]. Next, an equivalent model for the inductor is presented which closely approximates its impedance behavior in the frequency range of interest (900MHz to, say, 2.7GHz). This model is specific to the geometry of the inductor (width of the metal trace, spacing between adjacent turns, and the length of the smallest two segments). The parasitic elements in this model are expressed in terms of inductance of the family of inductors corresponding to the selected geometry, allowing the circuit designer to optimize his design for any inductance value. This inductor equivalent circuit is suitable for use in the simulated annealing based CAD tool developed as part of this work for optimizing the PA performance. The results from this modeling approach are compared to one-port measurements of two inductor structures fabricated in a digital CMOS process. Based on measurement results of these two inductors, the estimation of substrate resistance in the inductor model is refined to obtain improved accuracy over a wider range of frequencies. This improved model is used to study the trade-offs between various

aspects of the inductor geometry, as well as illustrate the improvement in self-resonance frequency of a floating inductor over an inductor with one port grounded.

2.1 Frequency Response of Inductor

Inductors fabricated on silicon suffer resistive losses due to the substrate and the metal layer(s) used to form the inductor. Substrate losses are caused by both inductive and capacitive coupling between the inductor metal layer(s) and the substrate. The flux generated in the coil links the substrate and induces eddy currents in it. These eddy currents flow in opposition to the inductor current and give rise to a negative coefficient of mutual inductance between the inductor and the substrate. Even in the case of a heavily-doped substrate, however, the substrate resistivity is usually much larger than that of the metal(s) forming the inductor. Thus, the effects of substrate eddy currents on the inductance are negligible, but their effects on inductor losses are significant and must be considered. Capacitive coupling occurs due to the SiO_2 between the inductor metal layer(s) and the substrate. Various techniques have been used to improve the inductor Q including etching the substrate under it [29], ganging multiple metal layers together using vias [30], and using negative resistance to cancel out the inductor resistance [31], [32]. Our goal is to be able to predict the inductor behavior from its geometry. In order to be able to predict the impedance v/s frequency behavior (referred to in the remainder of the chapter as the frequency response) of an inductor fabricated in a CMOS process, the effects of the series resistance, the capacitance from the conductor to the silicon substrate, as well as the substrate resistance, should be considered. Also, the capacitance between the adjacent turns of the metal forming the inductor, or inter-turn capacitance,

should be taken into account though sometimes it has been ignored in equivalent circuits for inductors [25]. In this work, we have modeled the inductor by modeling each segment of each turn of the inductor by the equivalent circuit shown in Figure 2.1.

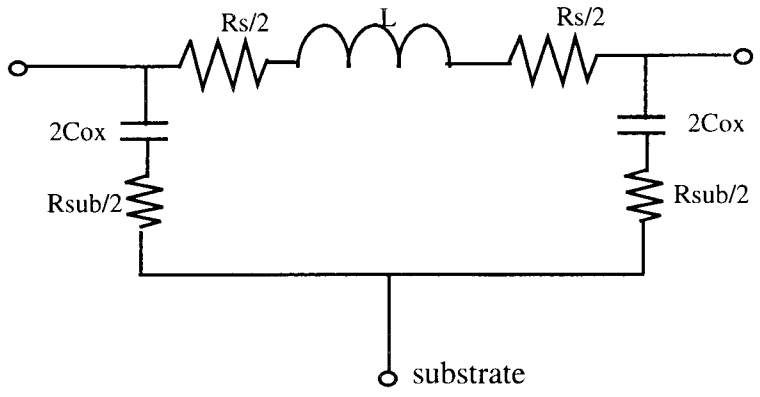

Figure 2.1 Equivalent circuit model for one segment of the inductor.

Here, R_s represents the total series resistance of the metal forming one segment, C_{ox} represents the capacitance between that metal segment and the substrate and R_{sub} represents the effective substrate loss resistance, *due to both inductive and capacitive coupling*, corresponding to the segment of the inductor being modeled. Note that it is not the goal of this research to develop a theory to accurately predict the interaction between the inductor and the substrate. Rather, a simplified approach is taken to compute R_{sub}, and experimental data is relied upon to improve the accuracy of this approach. Thus, a five segment square turn inductor, shown in Figure 2.2(a), is modeled with five equivalent circuits similar to the circuit shown in Figure 2.1 connected in cascade. An additional capacitance between the first and fifth equivalent circuit represents the inter-turn capacitance between segments 1 and 5. This is shown in Figure 2.2(b). R_s for each segment can be calculated as

$$R_s = R_{sheet} \times N \tag{2.1}$$

where R_{sheet} is the sheet resistance of the metal forming the inductor, and N is the number of squares in the segment being modeled. C_{ox} can be calculated by

$$C_{ox}/2 = C_u \times A/2 \tag{2.2}$$

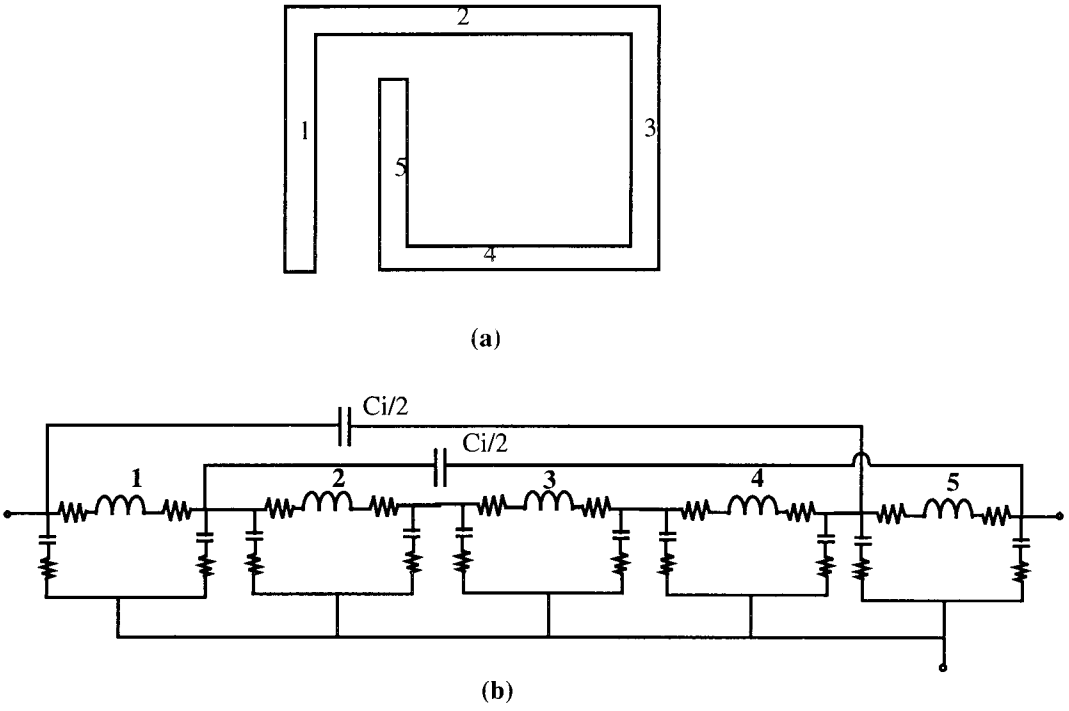

Figure 2.2 (a) A five segment inductor and (b) the circuit used to model it.

where C_u represents the metal-substrate capacitance (per unit area) for the metal used for the inductor, and A is the surface area of the inductor segment being modeled. C_u and R_{sheet} for the metal layer can be determined from the process data available through MOSIS. C_i represents the inter-turn capacitance between segments one and five. This capacitance is calculated assuming that the two sidewalls of these segments form a parallel-plate capacitor, and fringing capacitance is ignored. Substrate resistance is calcu-

lated using the single node substrate model [33]. It is assumed that the CMOS process utilizes a 10μm thick P- epitaxial layer on top of a P+ bulk. The bulk is assumed to be a single node (ground), and an effective epitaxial layer resistance is computed between the inductor metal segments and the bulk, or ground, nodes. As shown in Figure 2.3, the epitaxial layer resistance is computed assuming an active area corresponding to the geometry of the metal segment. It is computed as the parallel combination of two resistances - an area component and a perimeter component, and is given by

$$R_{sub} = \left(\frac{\rho T}{WL}\right) \| \left(\frac{\rho}{2(W+L)}\right) \tag{2.3}$$

where ρ is the resistivity of the epitaxial layer, T is its thickness, and W and L are the width and length of the surface area for which the epitaxial resistance is being computed.

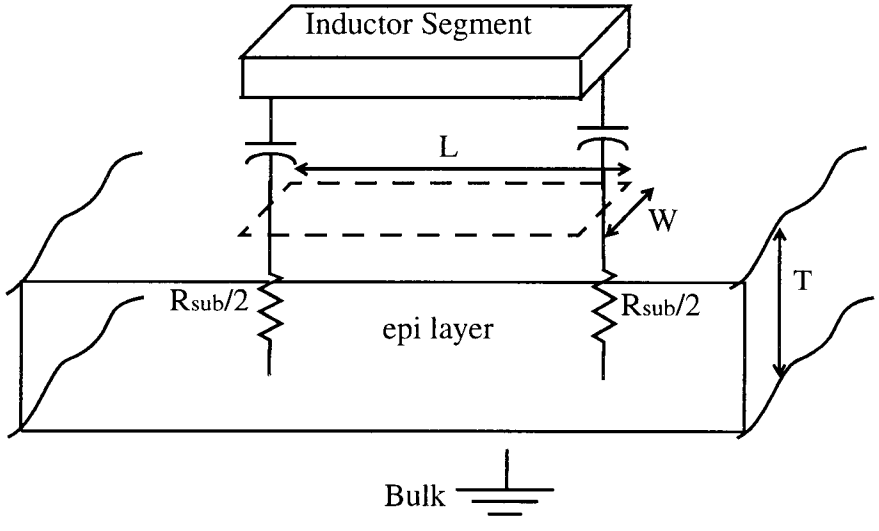

Figure 2.3 Computing the substrate resistance using the single-node substrate model.

The inductance L for each segment includes self and mutual inductance terms, and is determined using the procedure outlined in [26]. Thus, all the elements of the inductor circuit can be calculated once the geometry of the inductor is decided. The frequency response of the inductor can then be obtained from this circuit. Note that the procedure outlined above to determine the values of the various elements of this circuit involves many approximations in order to simplify analysis. A significant limitation of the above approach is that in computing the substrate loss resistance using the single-node substrate model, the loss in the substrate due to inductive coupling is not being accounted for. Experimental results will be used to further refine the prediction for the substrate loss resistance associated with planar inductors.

2.2 Inductor Equivalent Circuit

While the circuit presented in section 2.1 above may be used to model the inductor, it is not a suitable model for inclusion in any CAD tool designed for parasitic-aware optimization of RF circuits. The simulated annealing algorithm, which is used in a CAD tool developed as part of this work, generally requires several thousands of iterations before it reaches an optimum solution, and including the circuit model of Figure 2.2(b) for every inductor in the circuit will substantially increase the computation time required to optimize a design. In this section, we present an equivalent circuit for the inductor which is more suited for inclusion in a CAD tool, and develop equations for the various elements of the equivalent circuit in terms of the inductance. As a first step, the frequency response of the inductor is approximated by an equivalent circuit with the

same ω_{max} (the frequency at which the impedance of the inductor is maximum) and Q (the ratio of ω_{max} and the 3-dB bandwidth of the inductor frequency response) as the inductor circuit. This process is carried out for inductor values ranging from slightly greater than 1nH to 17nH. Next, each element in the equivalent circuit is plotted as a function of the inductance. Finally, in order to obtain an expression relating the value of each unknown circuit parameter to the inductance, polynomials are used to fit the curves generated above.

The equivalent circuit used to model the *complete* inductor is the same as the circuit used to model each segment of the inductor in the distributed model of Figure 2.1, and is represented in Figure 2.4. Since this model utilizes only five distinct elements to model the complete inductor, it is not computationally intensive and may be incorporated into a CAD tool for circuit optimization. In this model, L represents the inductance of the inductor calculated using a program based on [26], and R_1 is the resistance of the metal(s) forming the inductor, calculated using equation (2.1), with N being the total number of squares in the metal(s) used to implement the inductor. The parameters C_2 and R_2 do not necessarily have direct physical significance, and their values are chosen such that the frequency response of Figure 2.4 approximates the inductor response obtained in section 2.1. For the circuit of Figure 2.4, the impedance between nodes a and b can be easily derived to be

$$Z_{ab}(s) = R_2 \frac{s^2 + s\left[1/(R_2C_2) + R_1/L\right] + R_1/(R_2LC_2)}{s^2 + s\left[(R_1 + R_2)/L\right] + 1/(LC_2)} \tag{2.4}$$

By comparing the denominator of equation (2.4) with the canonical transfer function for a bandpass filter [34], the values of Q and ω_{max} are

$$Q = \frac{1}{R_1 + R_2}\sqrt{\frac{L}{C_2}} \tag{2.5}$$

$$\omega_{max} \approx \omega_n = \frac{1}{\sqrt{LC_2}} \tag{2.6}$$

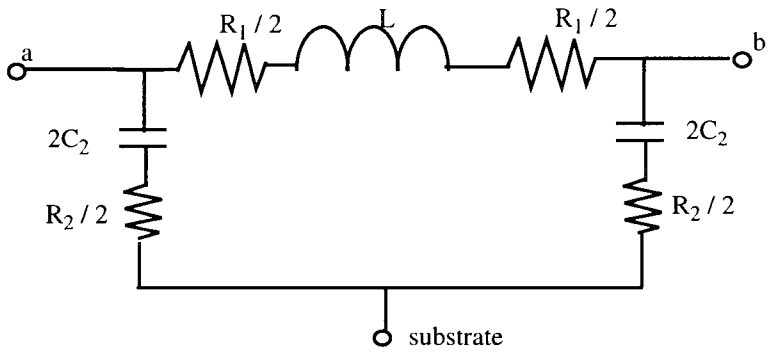

Figure 2.4 Equivalent circuit for the inductor.

The values of the two unknown elements in Figure 2.4, namely R_2 and C_2, are determined by solving equations (2.5) and (2.6) using Q and ω_{max} obtained from the inductor's simulated frequency response. Thus, the circuit of Figure 2.4 will have the same Q and ω_{max} as the original inductor. We have approximated the value of ω_{max} as given by equation (2.6) to the natural frequency ω_n. Thus, there may be some error in the value of ω_{max} obtained from the inductor equivalent circuit. However, it is found that this error is negligible for the Q values typical of integrated inductors and equation (2.6) is a good approximation to ω_{max}.

2.3 Determination of Inductor Circuit Parameters

In this section, equations relating various components of the inductor equivalent circuit of Figure 2.4 to the inductance value will be determined using the process data for a HP 0.6μm n-well CMOS process. This data was obtained from MOSIS. It is assumed that the inductor is a planar inductor fabricated entirely in metal 3. As an example, the steps involved in obtaining the lumped model for a seven segment inductor (1.75 turns) will be shown. Figure 2.5 shows the inductor from the top and the side.

2.3.1 Computing Inductance

The inductance is calculated using the procedure outlined in [26] for planar inductors. This method is summarized below. The total inductance of the seven segment inductor shown in Figure 2.5 has three components:

(i) The self-inductance of all seven segments.

(ii) The positive mutual inductance. This includes components due to mutual inductance between segments 1 and 5, 2 and 6, and 3 and 7 (all segments which have current flowing in the same direction).

(iii) The negative mutual inductance terms between the segments 1 and 3, 2 and 4, 3 and 5, 4 and 6, 5 and 7, and 1 and 7.

The total inductance is the algebraic sum of the three components mentioned above. The formulae used to calculate the self and mutual inductance terms are given in [26] and restated here for convenience. The self inductance is given by

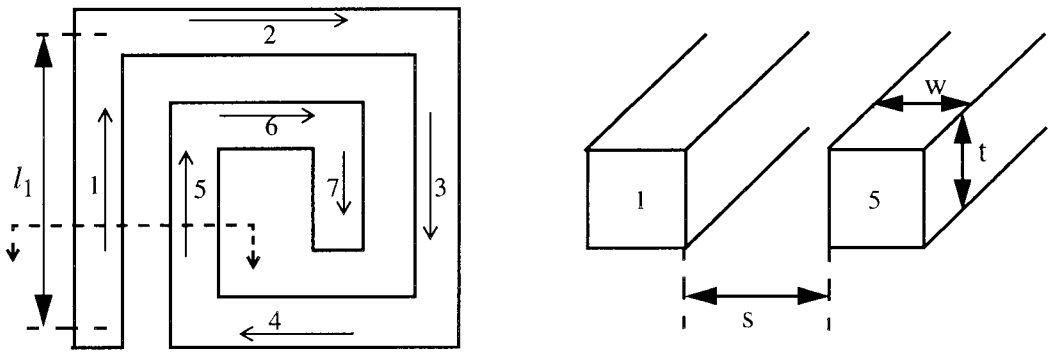

Figure 2.5 Top and front view of a seven segment inductor.

$$L_{self} = 200l\{\ln((2l)/(t+w)) + 0.50049 + (t+w)/(3l)\} \tag{2.7}$$

where l is the length, t the thickness and w the width of the segment. If l, t and w are in meters, L_{self} will be in nH as given by the above equation. The mutual inductance, in nH, between two segments, each of length l meters, is given by

$$M_l = 200l[\ln(l/gmd + \sqrt{1 + l^2/gmd^2}) - \sqrt{1 + gmd^2/l^2} + (gmd)/l] \tag{2.8}$$

where *gmd* is the geometric mean distance between the two conductors. GMD between two conductors is the distance between two imaginary, infinitely thin filaments having the same mutual inductance as the two original conductors and it may be approximated by the distance between the centers of the two actual conductors. This approximation is used in our design. The mutual inductance between two conductors of different length can be calculated, as given in [26], by (see Figure 2.6)

$$2M_{j,m} = M_{m+p} + M_{m+q} - (M_p + M_q) \tag{2.9}$$

The subscripts in the mutual inductance terms on the right side of the above equation indicate the lengths of the conductor segments. For example, M_{m+p} is the mutual inductance between two inductors of length $l = m+p$, and is given by equation (2.8). Thus,

from equations (2.7)-(2.9), and from a knowledge of the geometry of the inductor, the total inductance of an inductor with any number of segments can be calculated. In this work, the following dimensions were chosen for the inductor geometry (see Figure 2.5),

$l_6 = l_7 = 240\mu m$ (length of segments 6 and 7)

$w = 15\mu m$

$s = 1.2\mu m$

The thickness of the metal layer, t, is approximately $1\mu m$ for the given technology. The value for the metal width was chosen based on skin effect considerations, and the dimensions for the inner hole for the inductor, which determined the size of the inductor segments, was chosen as explained later in section 2.5.

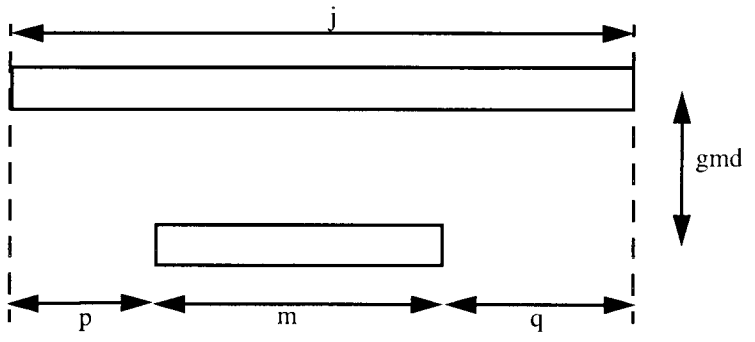

Figure 2.6 Calculating mutual inductance between segments of unequal length (from [26]).

2.3.2 Calculation of Parasitics

Equation (2.1) is used to calculate the series resistance of the inductor, with the value of R_{sheet} for metal3 being 50mohms/sq for the given technology (as per data avail-

able from MOSIS). Substrate resistance is calculated using equation (2.3). The resistivity of the epi-layer is assumed to be 2 Ω-cm (estimated from the NSUB parameter of the Level 3 model for an NMOS transistor). The capacitance of metal3 over substrate is 20aF/μm^2 (from MOSIS). Thus, the capacitance between the metal segments and substrate is easily calculated. Capacitance between turns is calculated by assuming that the two adjacent turns form a parallel-plate capacitor separated by oxide, and therefore its capacitance is given by

$$C = \varepsilon_0 \varepsilon_r lt/s \tag{2.10}$$

Fringing capacitance is ignored. The length l is taken as the average of the length of the two adjacent segments forming the parallel-plate capacitor. In the equivalent circuit, half the capacitance calculated above is associated with each end of the two segments. Note that equation (2.10) will only give an approximate value for the inter-turn capacitance, since the parallel-plate capacitor is a poor approximation of the inter-turn capacitance (for equation (2.10) to be valid, the surface dimensions of the parallel plates must be much larger than the separation between them). However, this equation gives an estimation of the order of magnitude of the inter-turn capacitance.

2.3.3 Simulation Results

A MATLAB program has been written to calculate the inductance, and the values of the inductor parasitics, based on the procedure outlined above. The code for this program is included in Appendix II. This program computes the total inductance, and the total series resistance, of the inductor given its geometry. It also generates SPICE

compatible files which can be used to obtain the frequency response of the inductor. Figure 2.7 shows the frequency response of a 29 segment inductor, obtained by simulating the SPICE files generated by this MATLAB program. In order to obtain this response, a current source of 1A is connected across the two ends of the inductor circuit and the voltage across it is plotted as a function of frequency. The voltage across the current source is equal to the impedance of the inductor. This inductor had center frequency f_{max} of 3.31GHz and Q of 5.1 (calculated based on the half-power points and the center frequency). Equations (2.4) and (2.5) are now solved to obtain the values of elements C_2 and R_2, for the equivalent circuit. The value of R_2 was found to be 31ohm and that of C_2 to be 0.183pF.

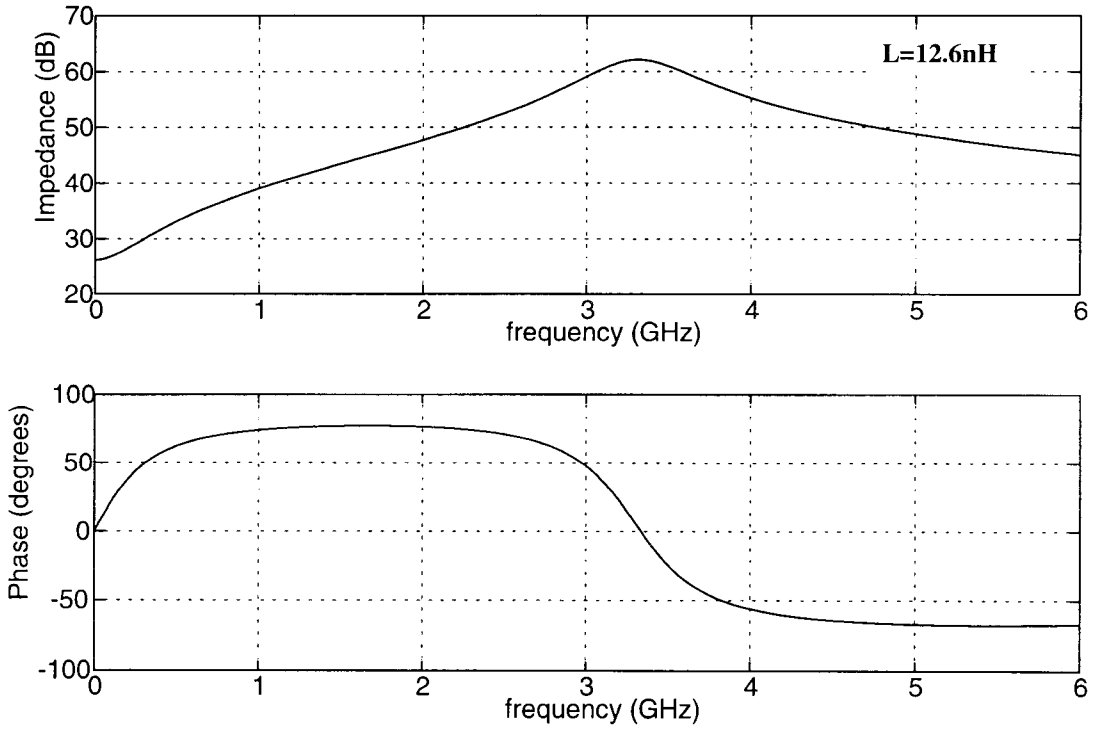

Figure 2.7 Frequency Response of the 29 segment inductor.

Figure 2.8 shows the frequency response of the inductor circuit (same as Figure 2.7) and the frequency response of the equivalent circuit. As can be seen, the equivalent circuit does approximate the frequency response of the inductor structure very well, and is a good model for use in the CAD tool being developed. The same process was repeated for inductors with more number of turns, but with the same metal width and inter-turn spacing as the seven segment inductor considered above. Table 2.1 summarizes the results obtained. As can be seen from this table, inductors from 1nH to 17nH are simulated. The values of R_2 and C_2, to be used in the equivalent circuit, are listed in this Table 2.2, along with the value of the series resistance obtained from the MATLAB program.

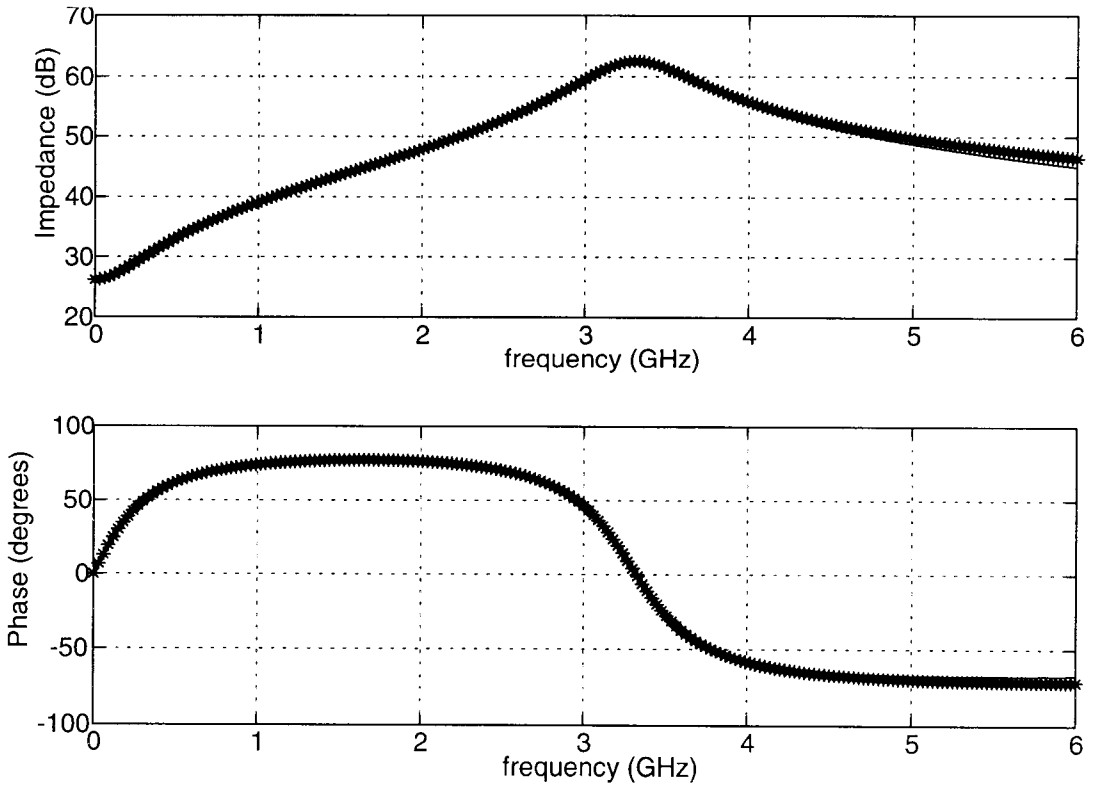

Figure 2.8 Frequency response of the inductor (-) and the equivalent circuit (*).

2.3.4 Equations for Circuit Parameters

The next step in this modeling process is to obtain equations relating the various elements of the inductor equivalent circuit, namely R_1, R_2 and C_2, to the value of the inductance L. This is achieved by using polynomials to fit the data obtained in Table 2.2.

Table 2.1: Summary of Simulated Inductor Frequency Response

Number of segments	l_1 (μm)	L (nH)	R_1 (ohm)	f_{max} (GHz)	Q
9	166	1.08	3.91	23.92	4.27
13	198	2.22	6.34	13.55	4.805
17	231	3.87	9.2	8.72	5.07
21	263	6.1	12.5	6.03	5.198
25	296	8.98	16.23	4.38	5.214
29	328	12.6	20.4	3.31	5.1
33	360	17	25	2.58	4.96

The MATLAB function *polyfit*, is used to perform this polynomial fitting. It provides the best fit in the least-square sense. The following equations are obtained

$$R_1 = -0.0296L^2 + 1.8307L + 2.2875 \quad (2.11)$$

$$2C_2 = -0.0005L^2 + 0.0312L + 0.0543 \quad (2.12)$$

$$R_2 = -0.0789L + 31.7071 + 3.4892/L \quad (2.13)$$

In these equations, L is in nH, R_1 and R_2 are in ohms, and C_2 is in pF. Figure 2.9 show the polynomial fit and the original data.

Table 2.2: Parameters of Inductor Equivalent Circuit

L (nH)	R_1 (ohm)	$2*C_2$ (pF)	R_2 (ohm)
1.08	3.91	0.082	34.12
2.22	6.34	0.1242	33.01
3.87	9.2	0.172	32.64
6.1	12.5	0.228	31.98
8.98	16.23	0.294	31.19
12.6	20.4	0.367	31.0
17	25	0.447	30.583

In order to verify that the equivalent circuit does indeed provide a good approximation to the inductor frequency response, the equivalent circuit of a 23 segment inductor was derived from equations (2.11)-(2.13) and its frequency response compared with that obtained from the circuit similar to Figure 2.2(b) for 23 segments. Figure 2.10 shows the frequency responses for both circuits. As can be seen from this figure, the two circuits have identical behavior in the frequency range for which the simulation was performed. Thus, the equations derived for the inductor equivalent circuit are accurate enough to be included in the CAD tool.

2.4 Experimental Results

As was mentioned in section 2.1, the interaction between the inductor and the substrate is dealt with in a very simplistic manner in the modeling approach presented above. In this section, measured results for monolithic inductors are presented and these results are used to refine the prediction of loss associated with the substrate. Two test inductor structures were fabricated in the HP 0.6μm CMOS process offered through the

MOSIS service. The geometry of the inductors was identical to that described in section 2.3.1. The two inductors consisted of 5.25 and 7.25 turns, respectively. The inside port of both the inductors was grounded. One-port S-parameter (S_{11}) of the two inductors was measured over a frequency range of 30KHz - 6GHz.

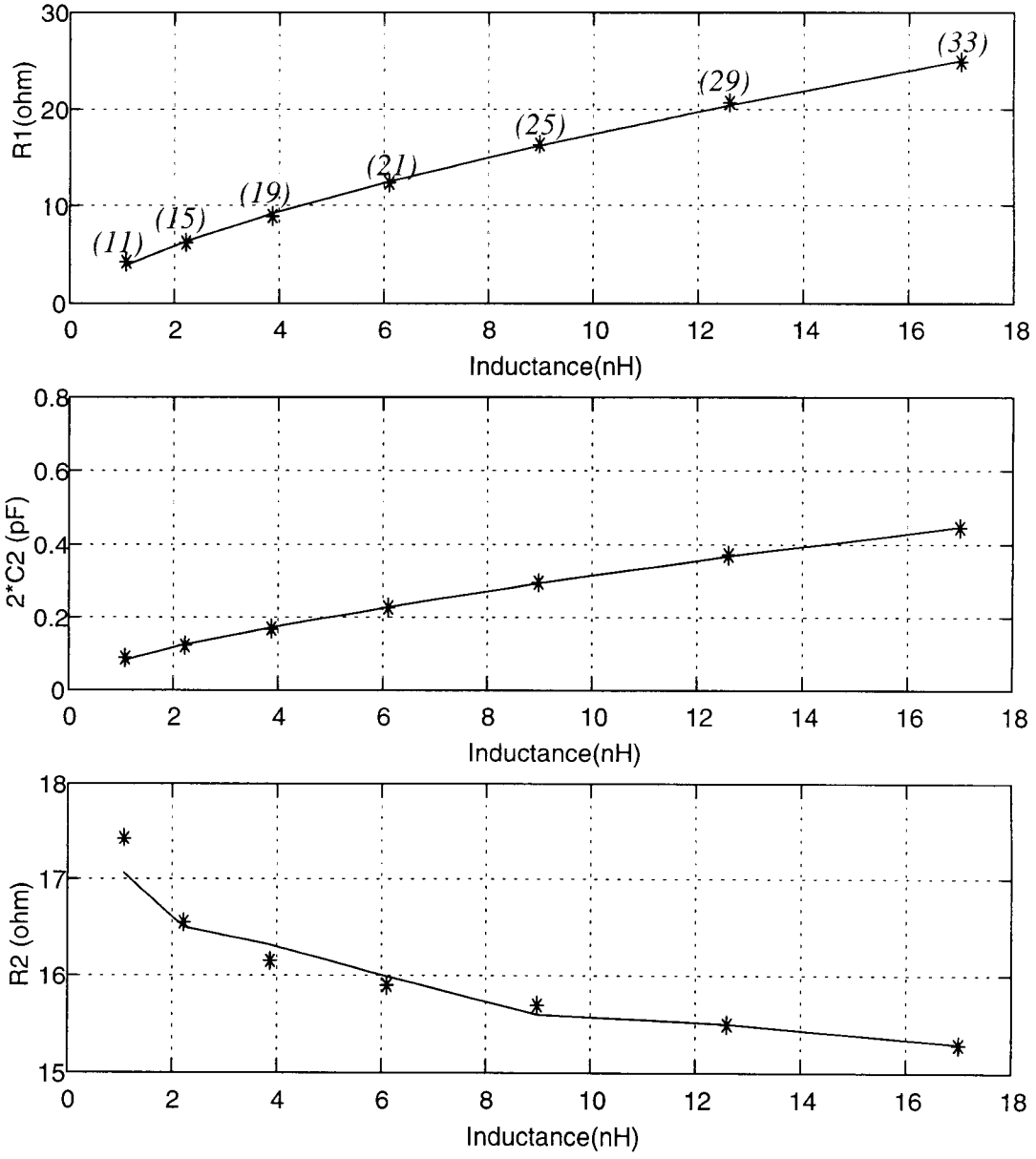

Figure 2.9 Data (-) and polynomial fit (*) for R1, 2C2 and R2 of the inductor equivalent circuit. The number of inductor segments corresponding to each data point are indicated in parentheses.

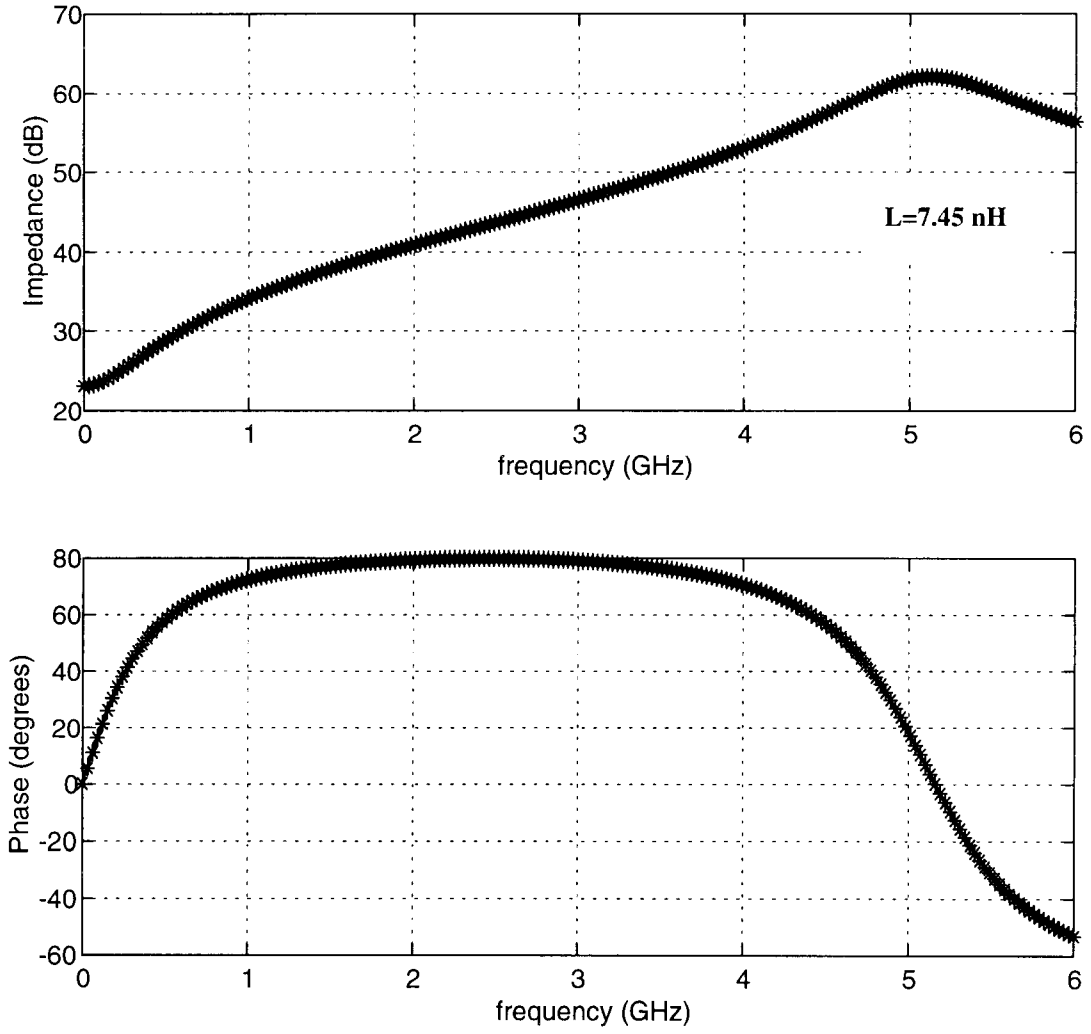

Figure 2.10 Impedance of a 23 segment inductor (-) and its equivalent circuit (*) v/s frequency.

In addition, S_{11} for a set of open probe pads was also measured. This latter measurement was performed in order to calibrate out the effect of the probe-pads and de-embed the S-parameter of the inductor by itself. Figure 2.11 shows the layout of the chip with the two test inductors and the open probe pads.The impedance of the inductor was extracted from the de-embedded S-parameter data. Figure 2.12 shows the real and imaginary components of the measured inductor impedance compared with the predictions

of the distributed model, for the 5.25 turn inductor. The measured low-frequency inductance and resistance agree very well with the model.

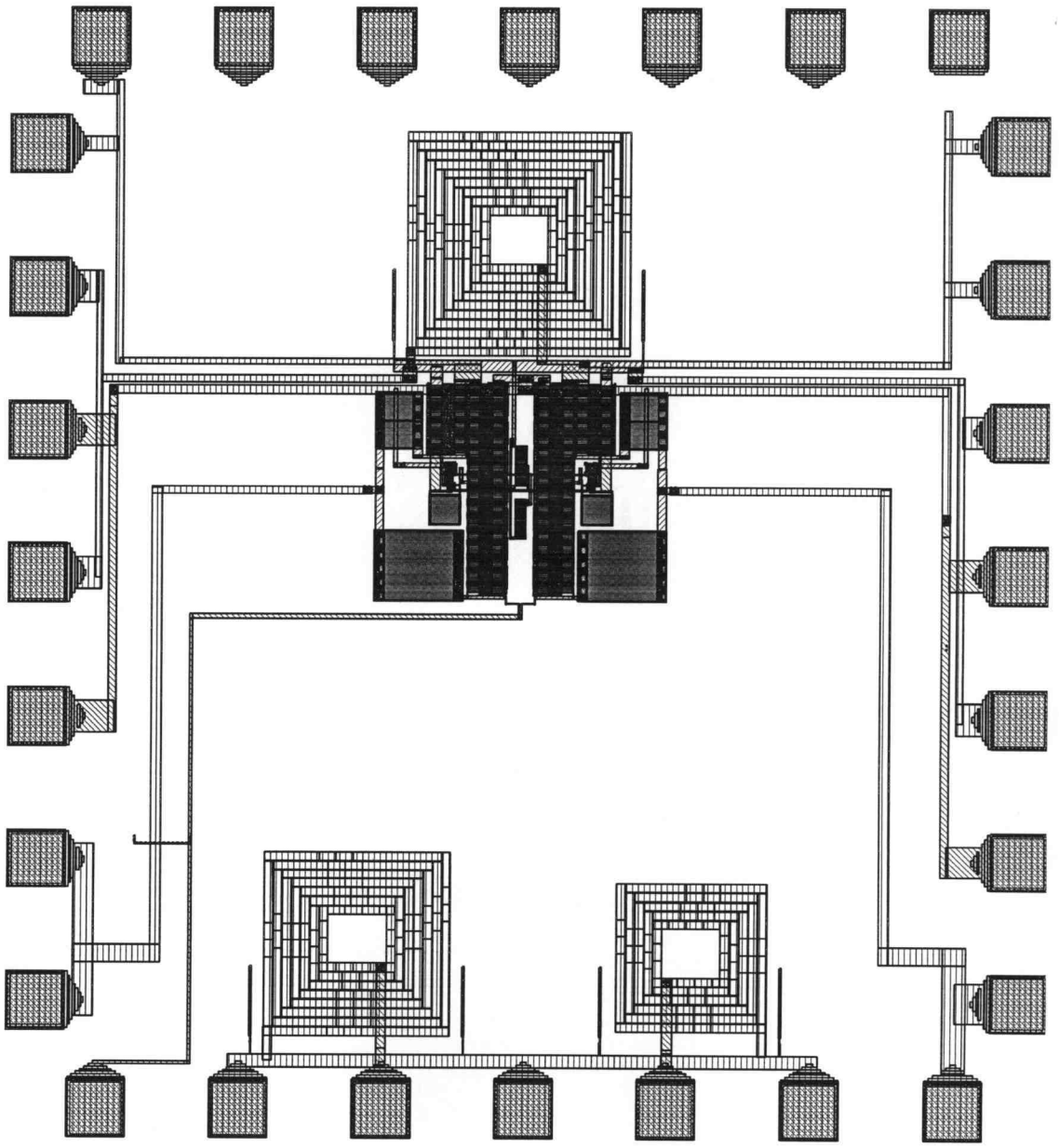

Figure 2.11 Layout of the chip showing the test inductors and the open probe pads.

As can be seen from this figure, the model predicts the self-resonant frequency with reasonable accuracy also, but does not accurately predict the impedance over the entire useful frequency range of the inductor (i.e. from dc to the self-resonant frequency of the inductor). The significant error in the estimation of impedance, near the self-resonant frequency of the inductor, may be attributed to the overly simplistic technique adopted for computing the substrate loss. More specifically, the loss due to inductive coupling to the substrate has a very significant impact on the inductor response.

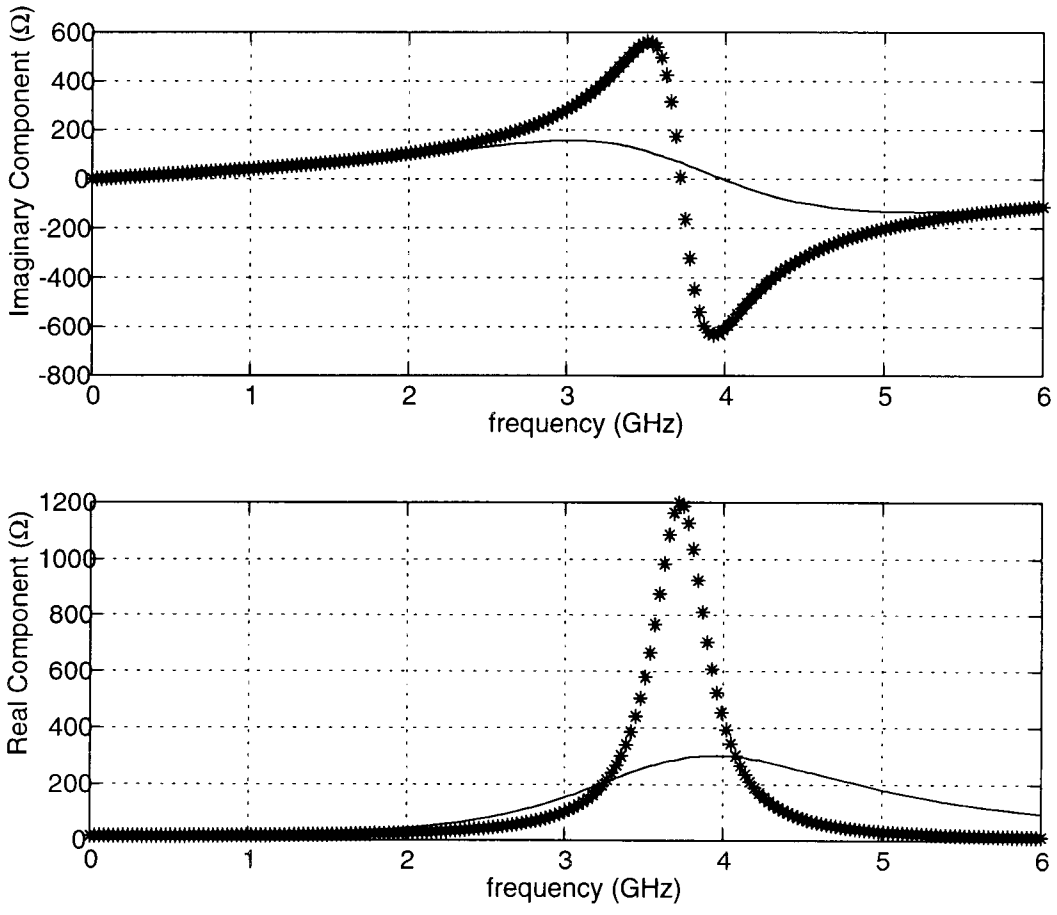

Figure 2.12 Comparison of the measured (-) and predicted (*) impedance of the inductor v/s frequency.

2.4.1 Estimation of Substrate Loss

A common technique to compute the measured Q of an inductor structure is to approximate it as the ratio of the measured reactance to the measured resistance for the inductor. This is essentially the definition of the Q-factor for a series RL circuit. Figure 2.13 compares the measured Q value with the predicted Q value using this definition. As can be seen, while the model predicts a peak Q-factor of 4, the measured value of the peak Q-factor is only 2.35. The significant difference between the two values may be attributed primarily to the substrate loss due to inductive coupling.

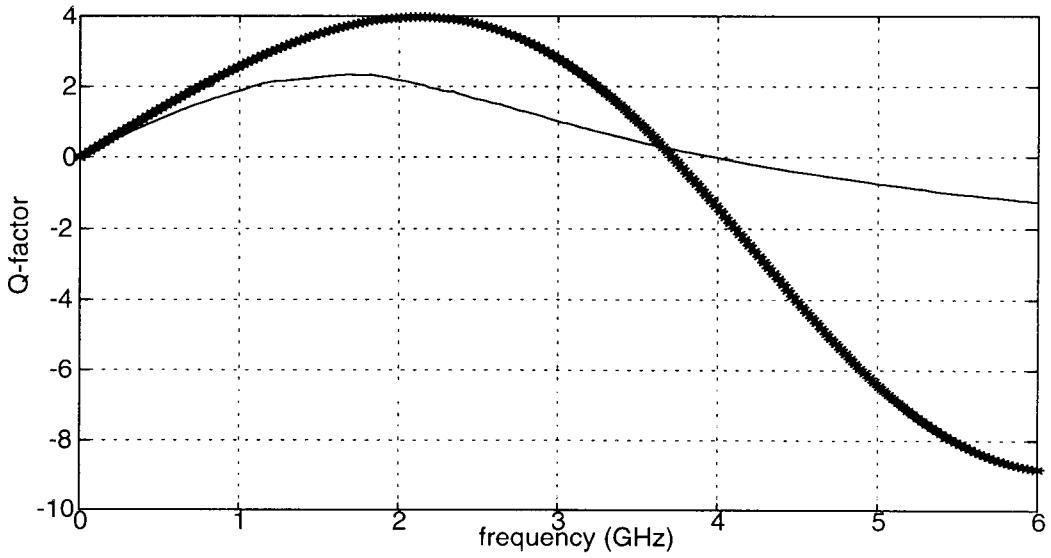

Figure 2.13 Comparison of the measured (-) and predicted (*) Q-factor of the inductor v/s frequency.

Inductive coupling to the substrate may be modeled by a parasitic inductor coupled to the metal inductor structure, and substrate loss due to this inductive coupling may be represented by a resistance across the ports of the parasitic inductor [35], as shown in Figure 2.14. However, in order to avoid introducing additional elements into

the inductor model, we have decided to represent both the inductive and capacitive substrate loss into a single effective substrate resistance (another alternative being to model it as a series loss).

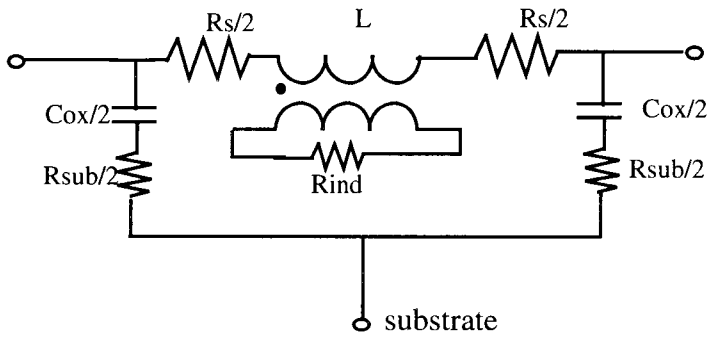

Figure 2.14 An equivalent inductor circuit including inductive substrate loss resistance (Rind).

An effective substrate loss resistance may be defined as the resistance value which would produce the same loss in the inductor structure due to capacitive coupling alone as the total substrate loss caused by both inductive and capacitive coupling to the substrate. Its value is computed by introducing an empirical constant, K, into the computation of substrate loss resistance.The substrate resistance value given by equation (2.3) is multiplied by K to obtain the effective substrate loss resistance. The value of K is determined by fitting the results of the distributed model to the measured inductor frequency response.

Figure 2.15 shows the measured inductor response compared with the distributed model modified to include the effect of substrate loss as described above. Note that the value of the empirical constant, K, is the only parameter which has been varied in the model, and this has resulted in significantly improved agreement between the measured inductor impedance and the inductor model. Further, the self-resonant frequency

of the inductor, as obtained from the model, also agrees more closely with the measured data. Figure 2.16 shows the measured and predicted inductor frequency response for the 7.25 turn inductor. Good agreement between the two sets of results lends credence to the substrate modeling approach adopted in this work. The modeled and measured results for the two inductors, as well as some process parameters, are summarized in Table 2.3.

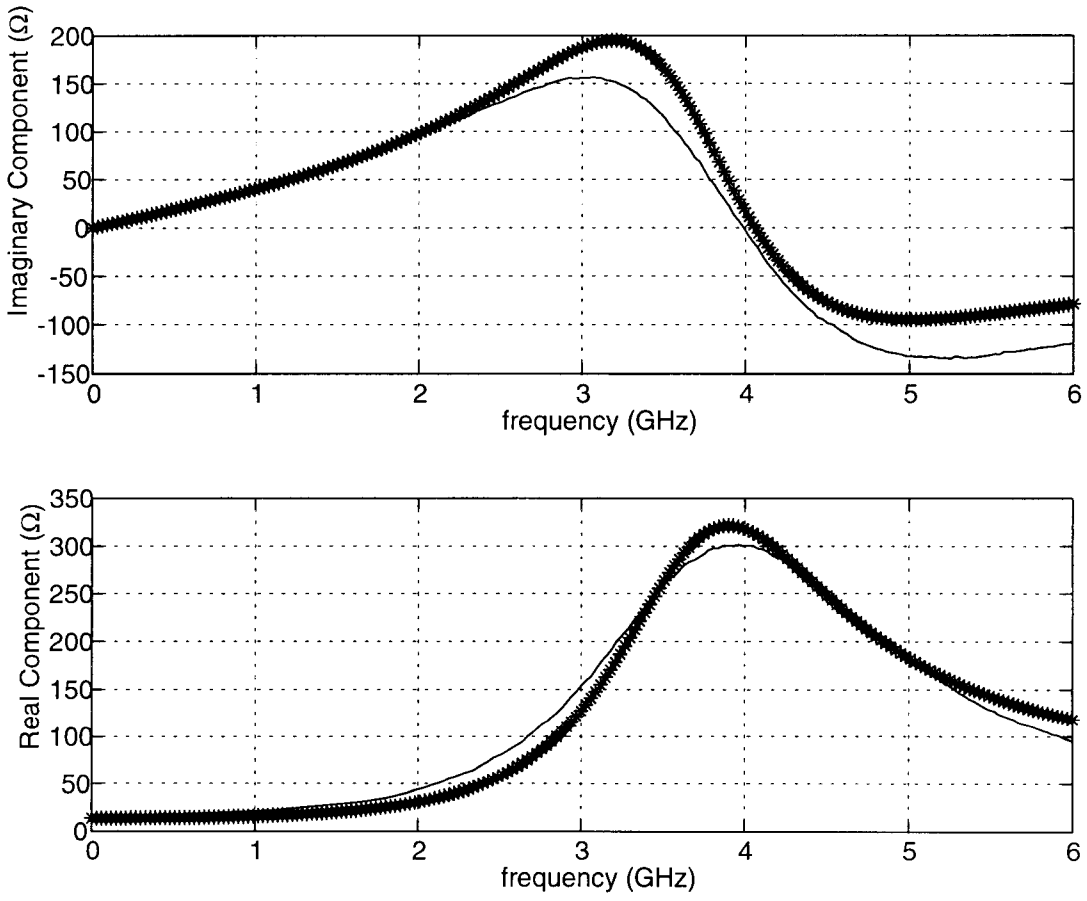

Figure 2.15 Comparison of the measured (-) and predicted (*) impedance of the5.25 turn inductor v/s frequency using a more accurate estimation of substrate loss.

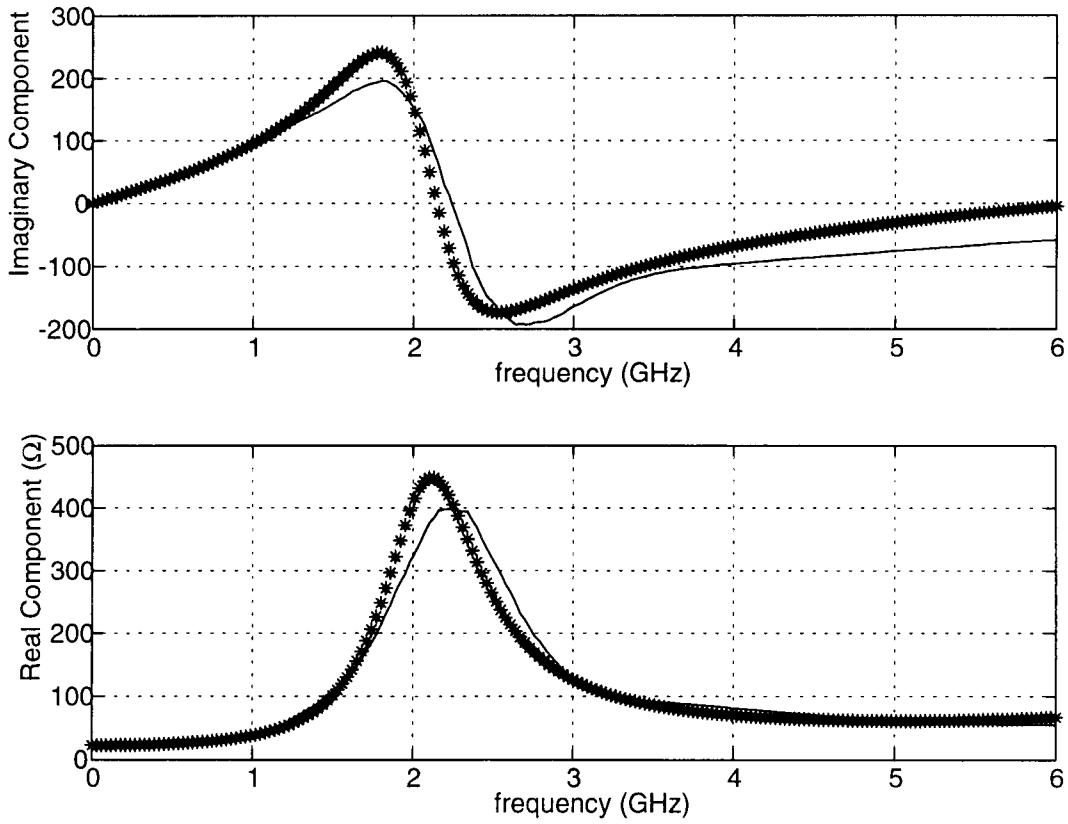

Figure 2.16 Comparison of the measured (-) and predicted (*) impedance of the7.25 turn inductor v/s frequency using a more accurate estimation of substrate loss.

Table 2.3: Comparison of measured and modeled results for two inductors

Parameter	5.25 Turn Inductor		7.25 Turn Inductor	
	Measured	Modeled	Measured	Modeled
Inductance (nH)	6.18	6.09	12.4	12.6
Resonant Frequency (GHz)	3.99	4.06	2.24	2.15
Peak Q-factor	2.35	3.3	2.17	2.52
Series Resistance (Ω)	14	12.5	20	20.4
Empirical Constant K	-	70	-	70
Metal sheet resistance (mΩ/sq)	58	50	50	50
Metal-substrate capacitance (af/μm^2)	10-14	12	10-14	12

2.4.2 Comparison with Compact Model

Figure 2.17 shows the compact model for the 5.25 turn inductor, obtained by fitting the measured response of the inductor to the circuit of Figure 2.4. Equations (2.5)-(2.6) are used to estimate the values of C_2 and R_2. Note that since one port of the inductor is grounded, the equivalent circuit for the inductor is also derived with one port grounded, and therefore R_2 is replaced with $R_2/2$and C_2 is replaced with $2C_2$ in equations (2.5)-(2.6), resulting in the compact model configuration shown in Figure 2.17.

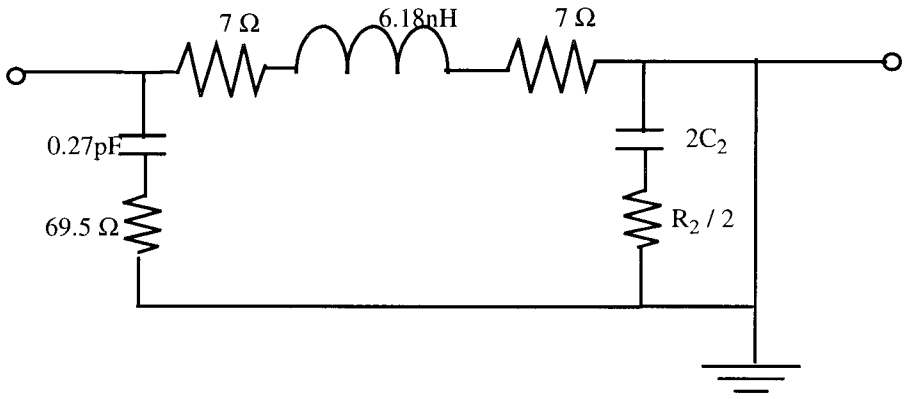

Figure 2.17 Compact inductor model for the5.25 turn inductor.

In Figure 2.18, the magnitude and phase of the impedance obtained from the compact inductor model are compared with the measured inductor response. It can be seen that the compact model also provides a reasonable approximation to the measured inductor response.

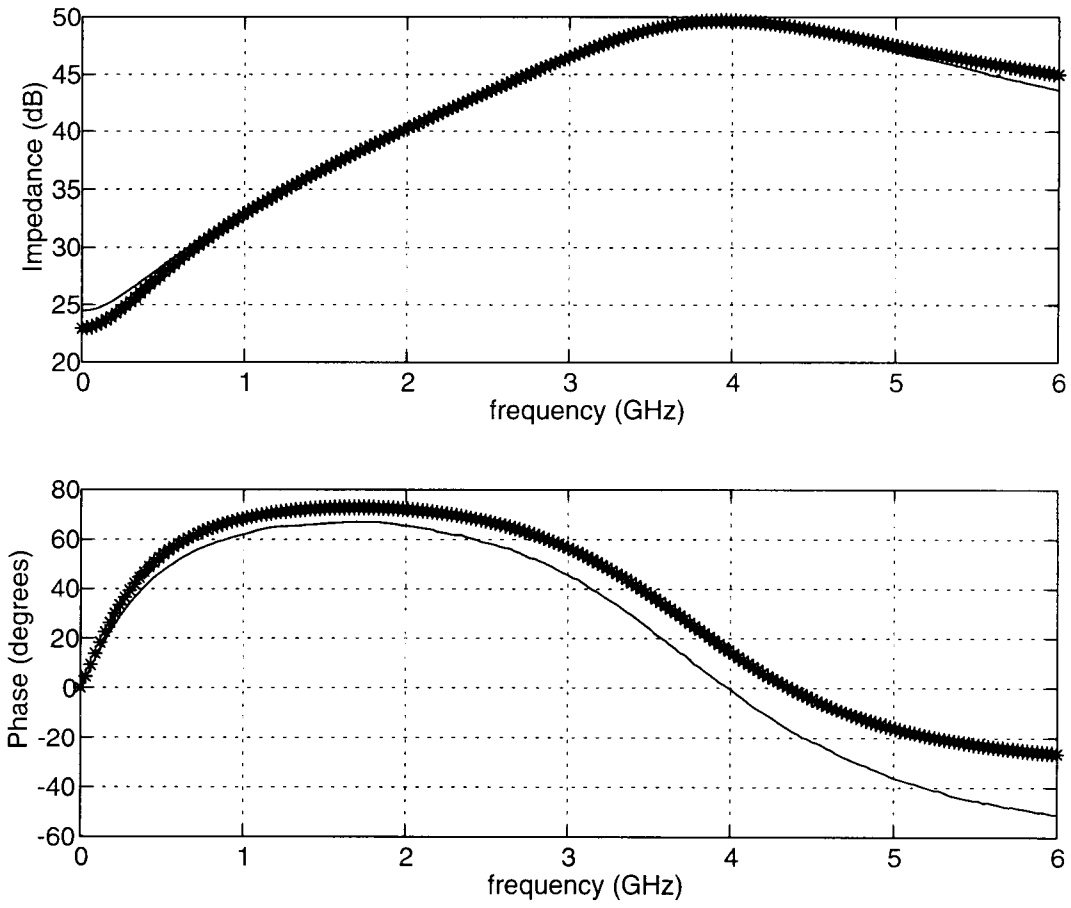

Figure 2.18 Comparison of the measured inductor impedance (-) with the compact model(*) response.

2.5 Floating and Mutually Coupled Inductors

In the previous section, measurements on two inductor structures were used to refine the distributed inductor modeling approach, and it was shown that the compact inductor model, extracted from the distributed model, was a fair approximation of the measured inductor response. Next, we make use of the distributed model to contrast the inductor response with one port grounded to that with both inductor ports floating. Also, simulation results for mutually coupled inductors are presented, and the various possible geometries of implementing such inductors are compared.

In general, an inductor with both of its ports floating has different parasitics than if one of its ports is grounded. As a result, the self-resonant frequency and the peak Q-factor for the two cases are different. Figure 2.19 shows the modeled response of the 5.25-turn inductor with both ports floating. It can be observed that the self-resonant frequency of the floating inductor has increased to 6.82 GHz, compared to 4.06GHz for the case with one port of the inductor grounded. Also, the peak Q-factor has improved to 5 from the modeled value of 3.3.

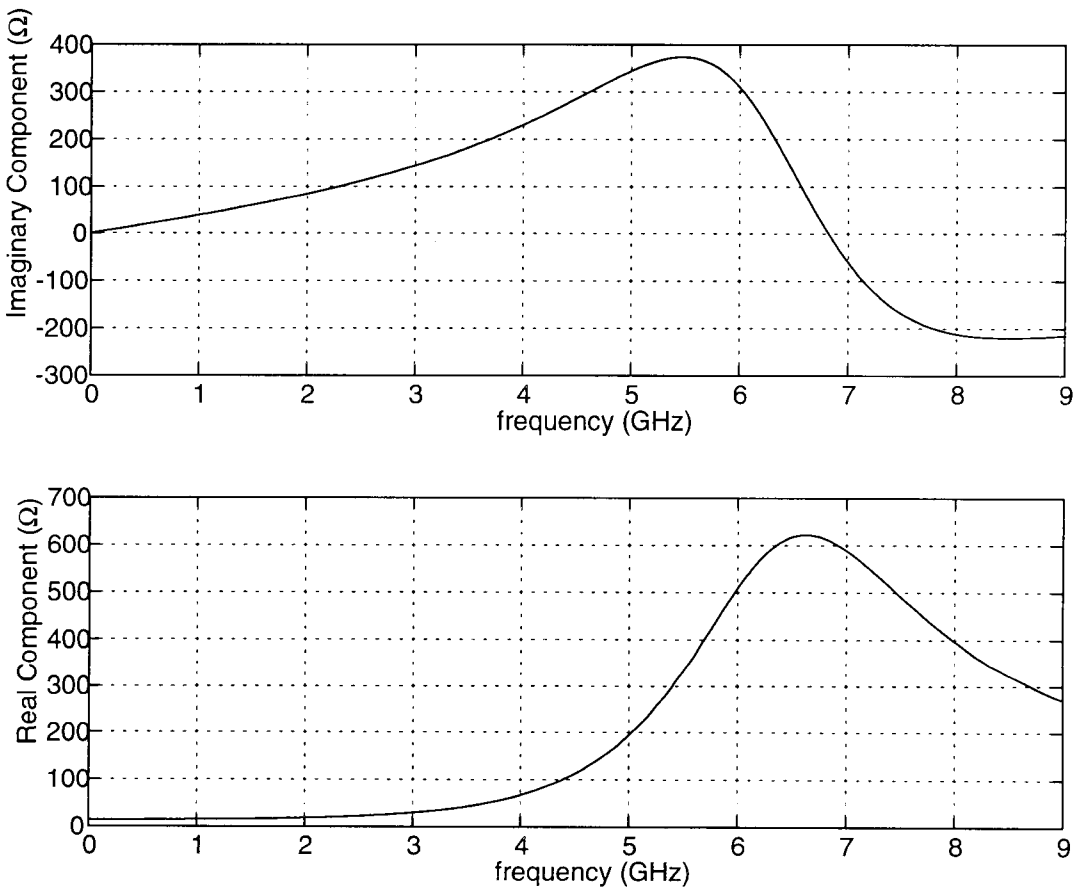

Figure 2.19 Estimated impedance of the 5.25 turn inductor with both ports floating.

Similarly, Figure 2.20 shows the modeled response of the floating 7.25 turn inductor. In this case, the resonant frequency has increased from 2.15GHz to 3.84GHz, and the peak

Q-factor improved from 2.52 to 4.1. Thus, for the same inductance value, floating inductors exhibit an increase in self-resonant frequency and peak Q by factors of 1.7 and 1.5, respectively. Therefore, it is desirable to use inductors with neither port grounded, whenever possible.

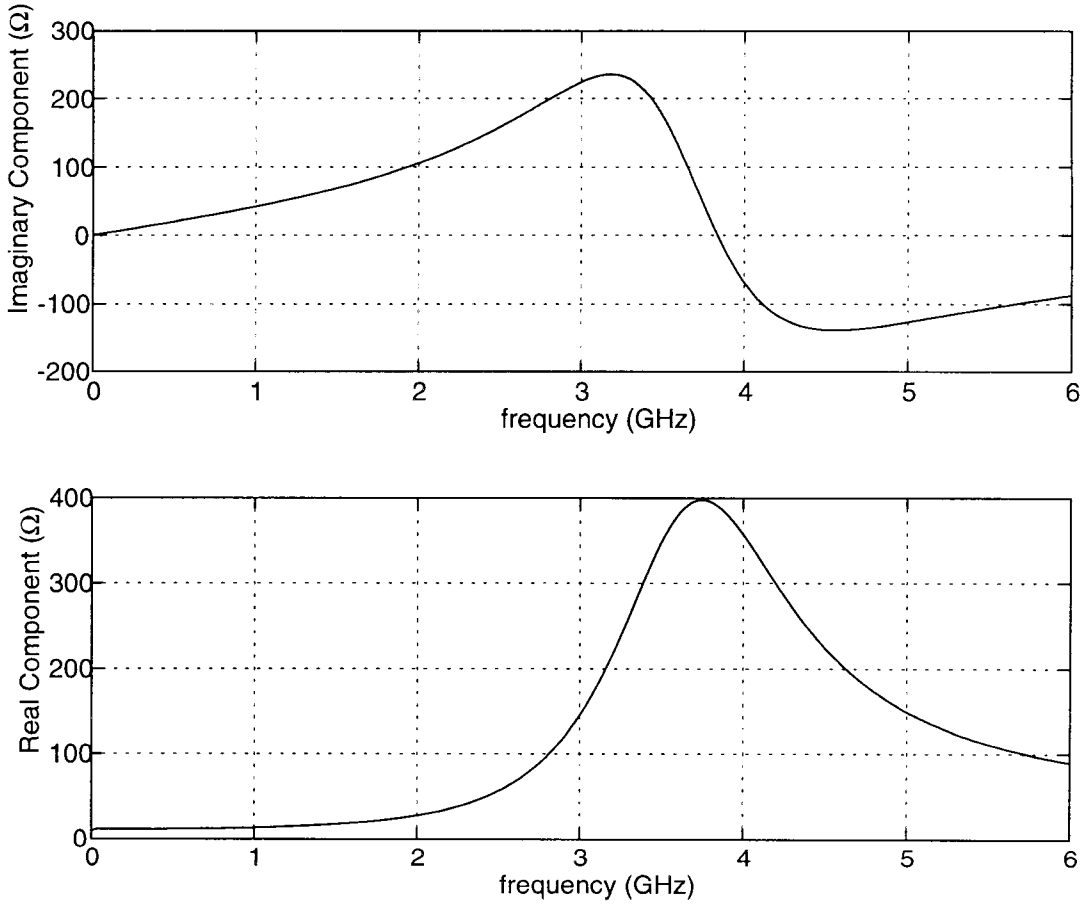

Figure 2.20 Estimated impedance of the 7.25 turn inductor with both its ports floating.

The modeling approach of section 2.3.1 may also be used to design mutually coupled inductors. Since the self and mutual inductance terms are calculated separately in the inductance calculation, this method can be used to compute the mutual coupling between a pair of inductors. Any point in a planar inductor may be tapped out as an

additional port and modeled by a set of two mutually coupled inductors. For example, the 7.25 turn inductor may be considered as a pair of two coupled inductors - one inductor consisting of the inner 4.5 turns, and the other inductor consisting of the outer 2.75 turns. The inductance of these two inductors is 4.39nH and 4.49nH respectively, whereas the inductance of the 7.25 turn inductor is 12.6 nH. The 7.25 turn inductor exhibits an inductance higher than the sum of the two constituent inductors due to the mutual inductance between the segments of the two 4.5 turn and 2.75 turn inductors. In this case, the mutual inductance is given by

$$M = 12.6nH - 4.39nH - 4.49nH = 3.72nH \tag{2.14}$$

which corresponds to a coupling coefficient of

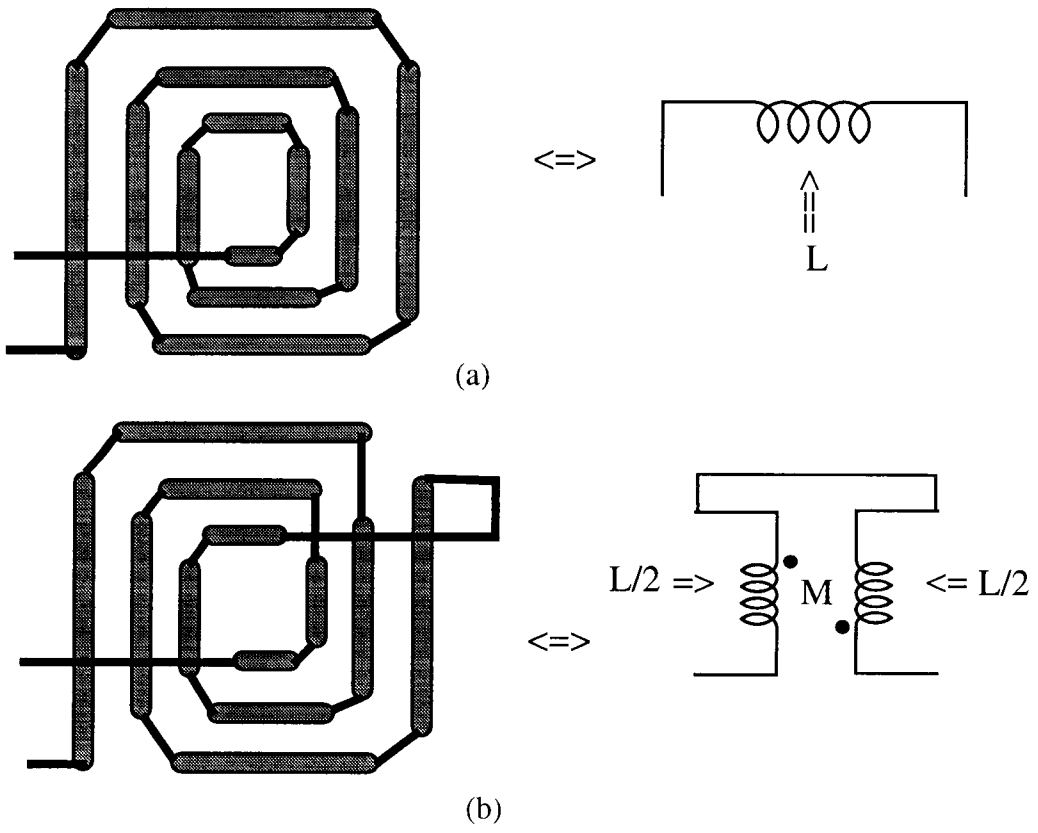

Figure 2.21 (a) A traditional spiral structure and (b) spiral inductor implemented as a centre-tapped spiral structure [27].

$$k = \frac{3.72}{\sqrt{4.39 \cdot 4.49}} = 0.84 \qquad (2.15)$$

Thus, in this manner, coupled inductors corresponding to almost any arbitrary value of self and mutual inductance may be realized.

Figure 2.21 above shows the interconnection of the segments of a given planar inductor to form either a single inductor or two separate, mutually coupled inductors. The geometry shown in Figure 2.21(b) is referred to as a centre-tapped spiral [27]. As can be seen from this figure, the essential difference between a centre-tapped spiral and a traditional spiral inductor is the manner in which the segments are connected together. Therefore, a pair of mutually coupled inductors implemented as a centre-tapped spiral structure will have the same parasitics as a conventional spiral. Thus, a traditional spiral structure may be used to implement any of the following:

(i) A single inductor.

(ii) A pair of mutually coupled inductors.

(iii) A centre-tapped geometry resulting in two separate, equal-valued, mutually coupled inductors (as may be required, for example, in differential circuits).

Other than a centre-tapped spiral, a pair of equal-valued inductors may also be implemented using two separate, uncoupled spirals. Figure 2.22 shows the two implementations for such a pair of inductors.

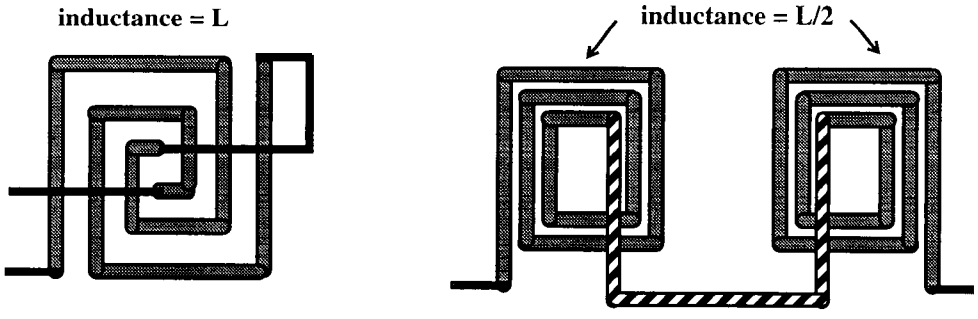

Figure 2.22 A pair of inductors implemented as centre-tapped spiral and as two separate coils.

The primary advantage in using a centre-tapped spiral v/s two separate coils is the saving in die area, and an improvement in the Q-factor. Figure 2.23 is a plot of the Q-factor for two cases - a single 12.4nH inductor with segments interconnected as shown in Figure 2.21(a) (equivalent to a centre-tapped spiral), and two separate coils of inductance 6.2nH each connected in series. As mentioned earlier, the parasitics for the 12.6nH spiral are identical to that for the two mutually coupled 6.2nH centre-tapped spiral inductors.

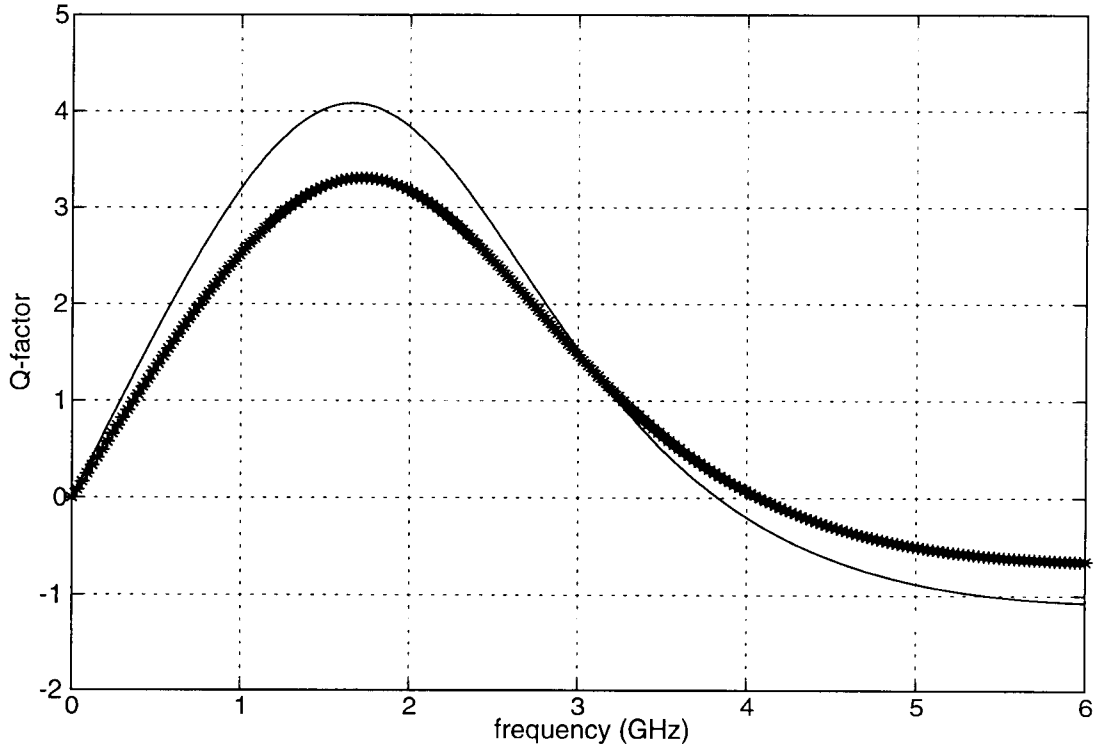

Figure 2.23 Q-factor for a centre-tapped spiral (-) and two series connected inductors (*).

The modeled peak Q-factor for the centre-tapped spiral is 4.05, and that of the two series connected inductors is 3.35. The self-resonance frequency of the centre-tapped spiral is 3.83GHz, compared to 4.07GHz for the two series connected inductors. How-

ever, the centre-tapped spiral occupies 0.1076mm^2, whereas the two 6.2nH inductors occupy, at the very least, an area of 0.1388mm^2. Thus, a centre-tapped spiral occupies 77% of the area of two series connected spiral inductor and exhibits a peak Q-factor value improvement by 21%. Further, its self-resonant frequency reduces by 6% compared to that for the two series connected inductors. Further, for the two implementations to have the same Q, the centre-tapped spiral occupies 63% of the area of two separate coils as reported in [27].

In the above sections, we have outlined a method for obtaining the impedance of an inductor for different frequencies. The inductor impedance is approximated by a simple circuit which is included in the simulated annealing based CAD tool described in chapter 4 for performing load-pull on the PA design, as well as optimizing the PA efficiency in the presence of various parasitics. Equations are derived which predict the values of the three unknown elements of the inductor equivalent circuit from the value of the inductance. Note that these equations will change if the width, thickness or spacing between the turns of the inductor changes. Thus, in order to use this model, first these dimensions of the inductor circuit should be decided, and then the procedure outlined above can be carried out to obtain the equations corresponding to the given inductor geometry. Equations (2.11)-(2.13) are valid for a planar inductor formed by using metal3, with the metal width being 15μm and the spacing between adjacent turns being 1.2μm, and with the innermost segments having a length of 101.4μm. The size of the hollow center was chosen such that the contribution of the inner turns which were removed was less than 10% of the inductance of an inductor greater than 10nH. It has also been suggested that the centre-hole dimension should be greater than five times the

width of the metal segments forming the inductor [28], a criterion which is met by the above choice for the dimension of the centre hole.

3. POWER AMPLIFIER DESIGN AND INTEGRATION ISSUES

The transmitted signal in wireless systems should have sufficient energy to reach the receiver, overcoming losses in the transmission medium between the receiver and transmitter. In order to achieve this, power amplifiers (PAs) are used in wireless systems to amplify the power of the transmitted signal. Linear PAs include Class A and Class B amplifiers, whereas Class C power amplifiers tend to be relatively non-linear and are referred to as tuned PAs [36]. Class D and Class E PAs are examples of high-efficiency switching amplifiers. Class F amplifiers also exhibit high efficiency and in this case the active device is used as a current source (similar to Class A, B and C PAs) rather than as a switch. The output power level of the PA is determined by the distance between the transmitter and the receiver, or the cell size. Depending upon the application, power output for these amplifiers can vary from milliwatts (wireless LAN, RF ID tags, cordless phones) to watts (cellular phones, two-way radios, base stations). Power amplifiers are a major source of power consumption in transmitters. Implementation of high efficiency PAs in standard CMOS is required to achieve low overall cost and to realize a single-chip CMOS transceiver. Current CMOS implementations of PAs exhibit low efficiency (30-45%) [10],[21] compared to around 50-60% [3],[8] for GaAs implementations. In this chapter, we discuss the operation of Class A, B and C amplifiers and determine some of the trade-offs involved in designing these PAs for operation in the higher efficiency region (i.e., the Class C mode). Current implementations of PAs make use of off-chip inductors as the load for the output stage devices [10],[11], as well as off-chip output matching networks. A significant amount of effort and resources are devoted to

"tuning" the PA for optimum performance (output power or efficiency) by changing the output matching network. This can be eliminated by integrating the output matching network (provided the load impedance required by the power device(s) can be predicted from available device models). In this chapter, a PA is presented which uses an active load and achieves efficiency close to that obtained using inductive loads. The various factors affecting the performance of a fully integrated (*i.e., with the output stage matching network also realized on silicon*) CMOS PA are enumerated, and their impact on the PA performance is illustrated by means of a design example.

3.1 Class A, B and C Power Amplifiers

Figure 3.1 shows the basic topology of what could be any of the above PAs. The transistor M1 acts as a current source in these power amps. The inductor in the drain of the common source amplifier makes it possible to achieve a peak signal swing equal to the supply voltage.

In addition, the drain inductor together with the load network acts to provide a tuned load to the amplifier in order to achieve frequency selectivity. It also serves as an impedance transforming network. An input driver circuit (labelled pre-amp in Figure 3.1) is used to provide a suitable signal for driving this amplifier. The dc level of this signal determines the efficiency at which the output stage operates for the given ac signal amplitude. Control over the output power of the PA can be obtained by controlling the ac signal amplitude of the pre-amp output.

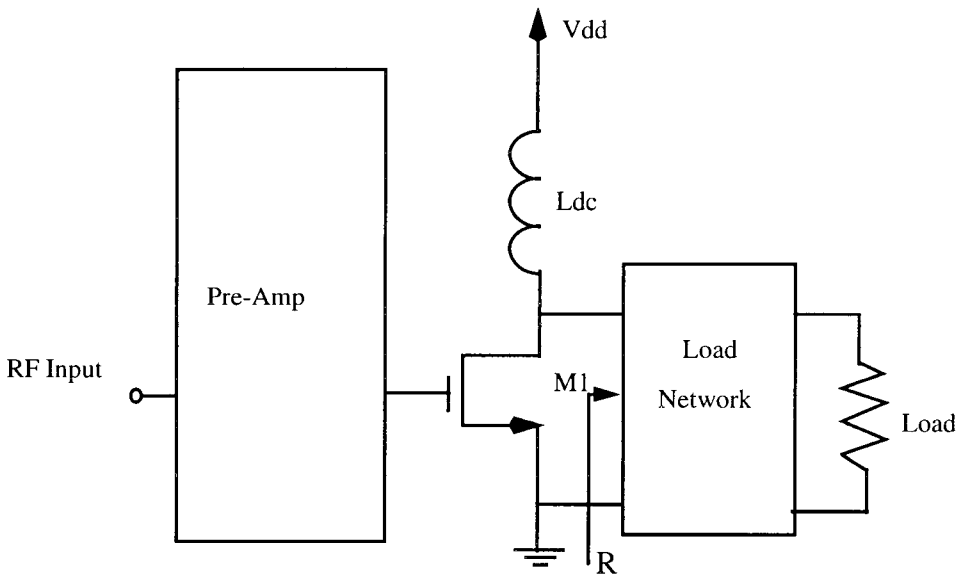

Figure 3.1 A Basic Power Amplifier.

3.1.1 Class A Power Amplifiers

The fraction of the RF cycle for which the transistor M1 conducts may be used to classify whether the PA is Class A, B or C. If the transistor is biased to be on for the entire RF cycle, then it operates as a Class A amplifier. If it is on for half the RF cycle, then the PA is classified as a Class B amplifier and for Class C operation, the transistor is on for any fraction less than half of the RF cycle. The drain (or collector) efficiency of a power amplifier is defined as

$$\eta = (rfpower_{out})/(dcpower) \tag{3.1}$$

Here, the dc power refers to the power drawn from the power supply only. The Power Added Efficiency (PAE) is used as a measure of how much output RF power is contributed by the input to the power amplifier and is defined as

$$PAE = (rfpower_{out} - rfpower_{in})/(dcpower) \quad (3.2)$$

For Class A operation, when the transistor is on for the entire RF cycle, the ideal drain current and voltage waveforms are as shown in Figure 3.2.

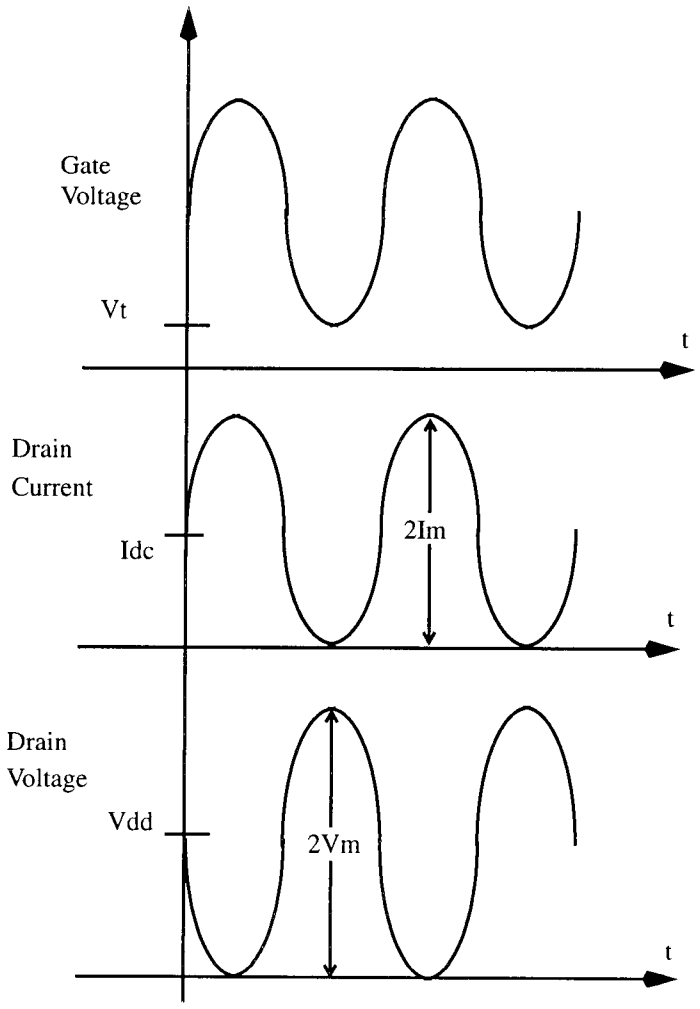

Figure 3.2 Ideal Signal waveforms for a Class A Power Amplifier.

The drain voltage ideally has a peak signal swing equal to the supply voltage (V_{dd}). In reality though, the drain signal swing (V_m) will be less than V_{dd}, since the drain-source voltage of the transistor should not go below V_{dsat}. For an ideal optimum design, the

drain current swing will equal the dc bias current and will be slightly less for a real design since the drain current should not reduce to zero. The RF power output for the Class A PA is then given by

$$P_{out} = V_m^2/2R \tag{3.3}$$

where $V_m \sim V_{dd}$ and $I_{dc} \sim I_m = V_m/R$, R being the load resistance seen by the transistor. The dc power drawn from the supply is

$$P_{dc} = V_{dd}I_{dc} = V_{dd}^2/R \tag{3.4}$$

and the efficiency of a Class A amplifier is

$$\eta = P_{out}/P_{dc} = V_m^2/2V_{dd}^2 \leq 1/2 \tag{3.5}$$

The maximum efficiency of an inductively-loaded Class A amplifier is thus limited to 50%. Further, in reality it will never achieve this efficiency since the signal voltage and current swings will always be less than the supply voltage and the dc bias current, respectively, for any practical transistor.

3.1.2 Class B Power Amplifiers

In Class B power amplifiers, the transistor is on for only half the period of the RF cycle. As will be shown, this type of operation is more efficient than the above described Class A operation. Sometimes, two transistors are used in Class B amplifiers, with one of them being on at any given time. Figure 3.3 shows the voltage and current waveforms for an ideal Class B PA using one transistor. The dc current drawn from the supply is the dc component of the drain current waveform shown. The fundamental component of this current waveform contributes to the RF power delivered to the load.

The load network attenuates the harmonic components of the signal current and allows the fundamental component to flow through, thereby generating a sinusoidal output voltage.

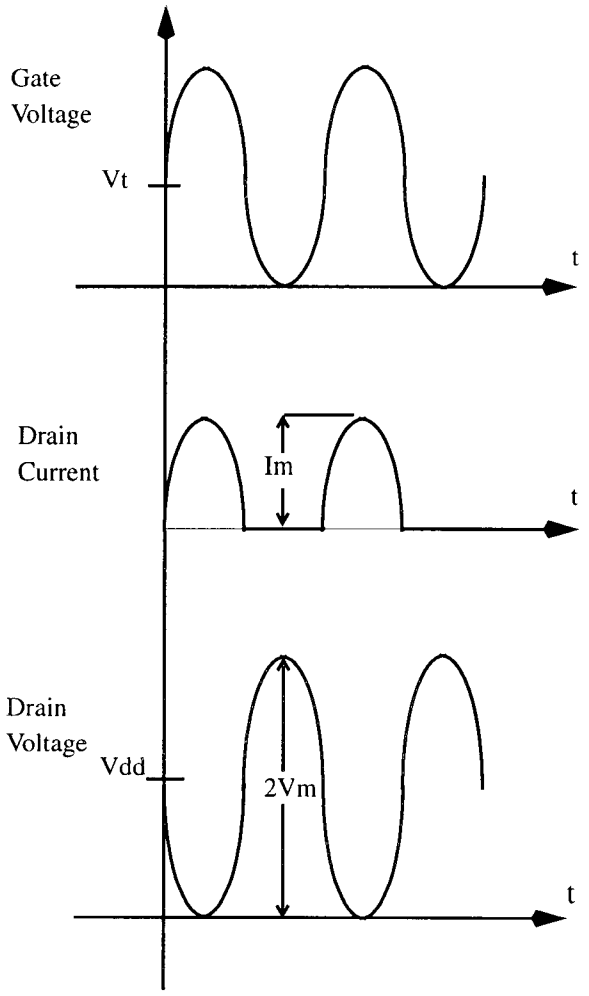

Figure 3.3 Ideal Signal waveforms in a Class B PA.

Assuming that the drain current waveform shown in Figure 3.3 is a half sine wave, it can be shown using Fourier Series analysis that its dc and fundamental components are

$$i_{dc} = I_m/\pi \tag{3.6}$$

$$i_{f1} = I_m/2 \tag{3.7}$$

For the case that $I_mR \sim V_{dd}$, the efficiency of the Class B power amplifier is

$$\eta = (i_{f1}^2 R)/(V_{dd} i_{dc}) \approx \pi/4 \tag{3.8}$$

Thus, the maximum possible efficiency of a Class B amplifier is 78.5%. Note that in order for the amplifiers discussed above to achieve their maximum efficiency, the signal voltage swing at the drain has to be the maximum possible and, in the case of Class A amplifiers, the bias current should be appropriately chosen such that, for the given value of load, the drain voltage swing corresponds to a drain current swing equal in magnitude to the bias current i.e. $V_m \sim V_{dd}$ and $I_m = V_m/R \sim I_{dc}$.

3.1.3 Class C Power Amplifiers

Class B amplifiers were shown to be more efficient than Class A amplifiers. The primary distinguishing feature between Class A and Class B power amplifiers is that for Class B amplifiers, the conduction angle of the transistor is 180°, or only half the RF cycle. Power Amplifiers for which the conduction angle can be any value up to or less than 180° are classified as Class C amplifiers. As is suggested by comparing Class A and Class B amplifiers, reducing the conduction angle results in further improvement in the efficiency of the power amplifier. However, reducing the conduction angle also decreases the maximum power output delivered by the PA. In this section, we derive the performance of a PA, in terms of efficiency, maximum output power, distortion, etc., as the conduction angle is made to vary over the range from 0 to 360°. Figure 3.4 shows the desired signal waveforms for a case where the transistor is on for a fraction *y* of the

RF cycle. Using Fourier series analysis, the drain current waveform can be expressed in terms of a dc component and sinusoidal components of fundamental and harmonic frequencies. The drain current may be modeled as a sine wave of amplitude I_m and having a dc component I_{dq} [36]. Note that I_{dq} will be negative for Class C, zero for Class B and positive for Class AB or A operation. The drain current may be written as

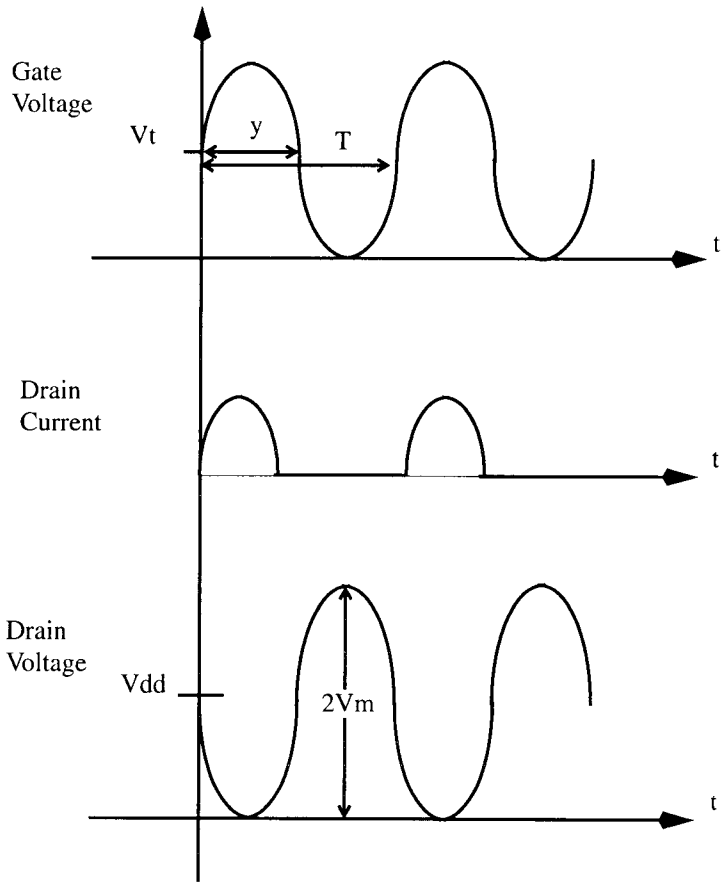

Figure 3.4 Ideal Signal waveforms for a Class C Power Amplifier.

$$i(\theta) = \begin{pmatrix} I_m \cos\theta + I_{dq} \ldots\ldots -y/2 \le \theta \le y/2 \\ 0 \ldots\ldots\ldots otherwise \end{pmatrix} \tag{3.9}$$

The Fourier series expansion of this waveform is given by

$$i(\theta) = i_{dc} + \sum_n i_n \cos n\theta \tag{3.10}$$

where

$$i_{dc} = \left(\left(2I_m \sin\frac{y}{2} + yI_{dq}\right)/(2\pi)\right) \tag{3.11}$$

and

$$i_n = \frac{I_m}{2\pi}\left(\frac{2}{n+1}\sin(n+1)\frac{y}{2} + \frac{2}{n-1}\sin(n-1)\frac{y}{2}\right) + \frac{2I_{dq}}{n\pi}\sin n\frac{y}{2} \tag{3.12}$$

The dc component of this drain current can be used to calculate the average power drawn from the power supply. With an appropriately designed load network, only the fundamental component of the drain current will flow through the load resistor. The load network will provide an alternate path for the harmonic components of current to flow. Similarly, the inductor connected to the drain of the transistor provides a path for the dc component of the drain current, and offers high impedance to the signal current. Thus, with a sinusoidal fundamental frequency current flowing through the load resistor, a sinusoidal voltage is obtained at the output.

In order to obtain a peak voltage swing equal to the power supply voltage, a suitable value of load resistance has to be presented to the device. For a given conduction angle y, the product of the load resistance (R_{opt}, say), and the peak instantaneous value of the fundamental component of drain current (which flows through R_{opt} to generate the output voltage), should equal the desired voltage swing. For each value of the conduction angle, the value of R_{opt} will be different and can be obtained from the following constraint (assuming the voltage swing is V_{dd})

$$V_{dd} = i_1(y) \times R_{opt} \tag{3.13}$$

where i_1 is the amplitude of the fundamental frequency current given by equation (3.12) for n=1. Given the above, the efficiency of a Class C power amplifier is given by

$$\eta = \frac{v_o \times i_1/2}{V_{dd} \times i_{dc}} \tag{3.14}$$

Noting that v_o, the output voltage, has a peak value equal to V_{dd}, and that

$$\cos\frac{y}{2} = \frac{-I_{dq}}{I_m} \tag{3.15}$$

the expression for the efficiency of a Class C PA reduces to

$$\eta = \frac{y - \sin y}{4\left(\sin\frac{y}{2} - \frac{y}{2}\cos\frac{y}{2}\right)} \tag{3.16}$$

Figure 3.5 shows a plot of the efficiency of a Class C amplifier as a function of conduction angle. As can be seen from this figure, the efficiency of the PA operating in Class C mode increases as the conduction angle decreases. Also evident is the Class A efficiency of 50% and Class B efficiency of 78.5% corresponding to a conduction angle of 360^o and 180^o, respectively.

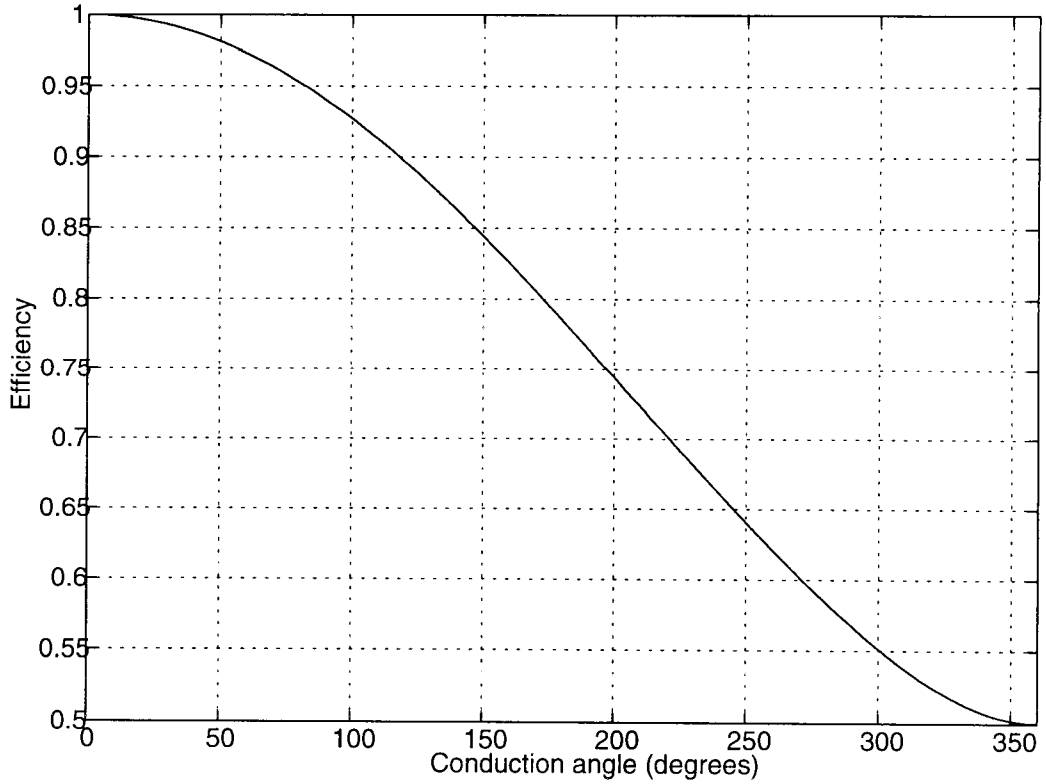

Figure 3.5 Efficiency v/s conduction angle for a Class C PA.

This figure is somewhat misleading, though. It is not correct to assume that, for a PA with a *fixed* load and matching network, reducing the conduction angle will result in higher efficiency. Implicit in the above analysis is the assumption that the output voltage swing is equal to V_{dd} for all values of conduction angle y. In order to meet this criterion, the load resistance value has to be different for each value of the conduction angle, as stated previously. Thus, this curve does *not* correspond to how a PA, with a fixed load resistor, would behave if the conduction angle of the driver transistor were varied. It does, however, give an upper limit for the efficiency achievable for a fixed, optimum, load resistance value. This efficiency is achieved only for a particular conduction angle value, corresponding to that for which the output voltage swing is maximum (and can be found from equation (3.16) or from Figure 3.5).

In order to illustrate how the efficiency of a PA, with a fixed load resistance, varies with conduction angle, an expression for the efficiency can be derived without the constraint that the voltage swing at the output is equal to V_{dd}. In this case, the efficiency is given by

$$\eta = \frac{i_1^2 \times R_{opt}}{2V_{dd} \times i_{dc}} = \frac{I_m R_{opt} \times (y - \sin y)^2}{4\pi V_{dd} \times \left(2\sin\frac{y}{2} - y\cos\frac{y}{2}\right)} \tag{3.17}$$

Figure 3.6 shows the variation of efficiency of a given amplifier as a function of conduction angle for an optimum value of load resistance. The efficiency has a maximum value at a conduction angle of 260^{o}, which corresponds to the maxima of equation (3.17). When designing for a particular efficiency, Figure 3.5 should be used to determine the value of conduction angle required at which the PA will meet the efficiency specification. Using equation (3.13), the optimum load resistance value should be determined

and impedance transforming networks designed to transform the standard 50 ohm load resistance to this value. Once the PA is designed, varying its conduction angle will change its efficiency as per Figure 3.6, except that an efficiency greater than that for which it is designed will not be achieved even though there is a maxima in the efficiency curve of Figure 3.6 To achieve the efficiency corresponding to this maxima requires a voltage swing *greater* than the supply voltage, which is not physically realizable. In fact all the points in Figure 3.6 which correspond to an efficiency greater than that given by Figure 3.5 are not physically feasible due to the fact that the drain voltage swing cannot exceed V_{dd}.

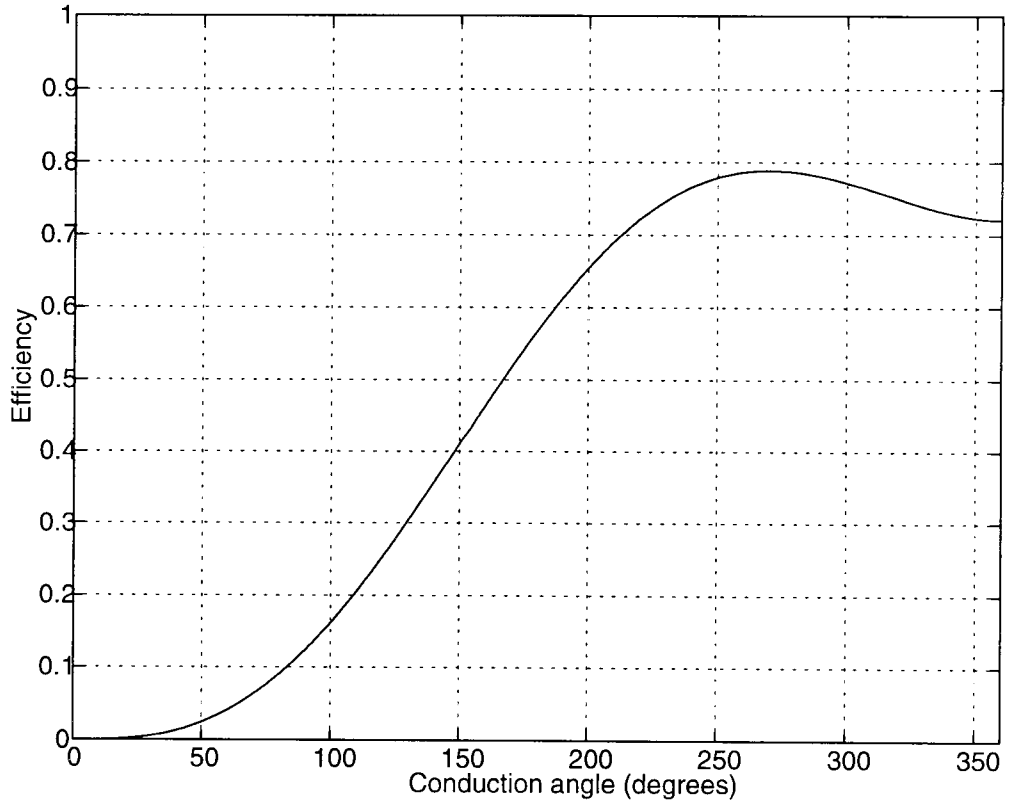

Figure 3.6 Efficiency v/s conduction angle for a Class C PA with a fixed load.

Thus, as Figure 3.6 suggests, changing the conduction angle from its designed value will *reduce* the PA efficiency. Since the conduction angle is determined by both the bias as well as the input signal level, reducing the input signal (i.e. when the PA is working at lower power output than its maximum value) will increase the conduction angle and result in lower efficiency of the PA.

To summarize, Figure 3.5 gives the maximum value of efficiency for a Class C (or, for that matter, a Class AB) PA and this value is achieved only for a fixed value of load resistance (the value that causes a drain voltage swing equal to the power supply voltage). Once a PA matching network is designed for this value of load resistance, its efficiency will, in general, tend to *decrease* from this designed value as the conduction angle is changed. Implicit in the plot of Figure 3.5 is the assumption that the load resistance varies with the conduction angle.

The improvement in efficiency of a Class C PA is achieved at the expense of reduced power output from the PA. In fact, even though one can design a Class C PA to achieve an efficiency approaching 100% (as Figure 3.5 suggests), the output power obtainable at this level of efficiency will approach zero. The output power obtainable from the PA may be written as

$$P_o = \frac{1}{2} v_o i_1 = \frac{1}{2} V_{dd} \times \frac{I_m}{2\pi}(y - \sin y) \tag{3.18}$$

Figure 3.7 shows a plot of the output power (divided by the power output from a Class A PA) as a function of conduction angle. It is assumed that the voltage swing at the output is equal to V_{dd}. As can be seen from this figure, the increase in efficiency (which results by reducing the conduction angle) is achieved at the expense of reduced output

power from the PA. Thus, there is a direct trade-off between the efficiency and power output in the design of this class of PAs.

The distortion in the amplifier output also increases as the conduction angle is reduced. Thus, a tuned output circuit is an essential part of Class C amplifiers whereas it may or may not be used in Class A or two transistor Class B power amplifiers. The total harmonic distortion in the absence of a tuned circuit (i.e. assuming a resistive load) may be computed using the Fourier series analysis results for the drain current. It is given by

$$THD = \frac{\sum\sqrt{v_n^2}}{v_1}100 = \frac{\sum\sqrt{i_n^2}}{i_1}100\% \tag{3.19}$$

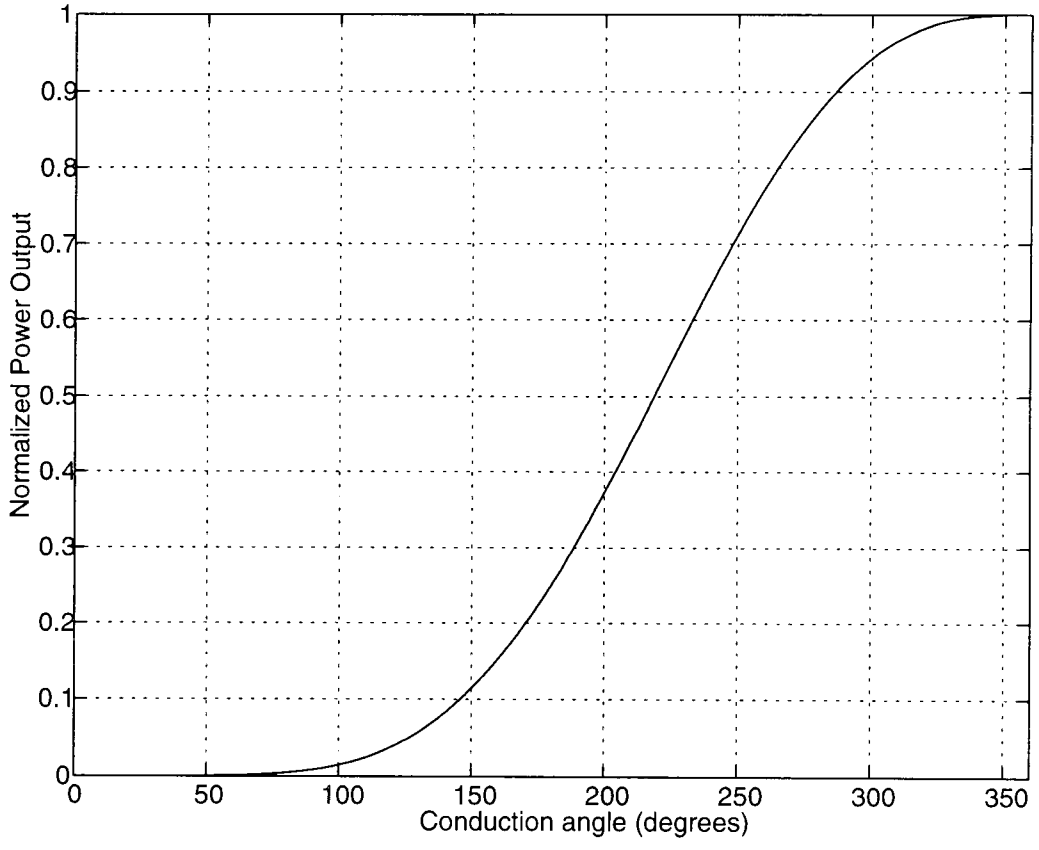

Figure 3.7 Output Power, normalized to Class A power output, v/s conduction angle.

Figure 3.8 shows the variation of the THD as a function of conduction angle. In a practical Class C PA however, the load network and an external filter will reduce the harmonics and the frequency response of this output circuit will determine the THD v/s conduction angle performance of the PA. In order to estimate the gain of the above class of power amplifiers, a slight modification of the above analysis is required. Notice that the above method assumes a waveform for the drain current, but does not relate it to the input signal which results in such a waveform. The input voltage waveform and the large signal characteristics of the transistor together determine the drain current waveform. If the input gate voltage is given by

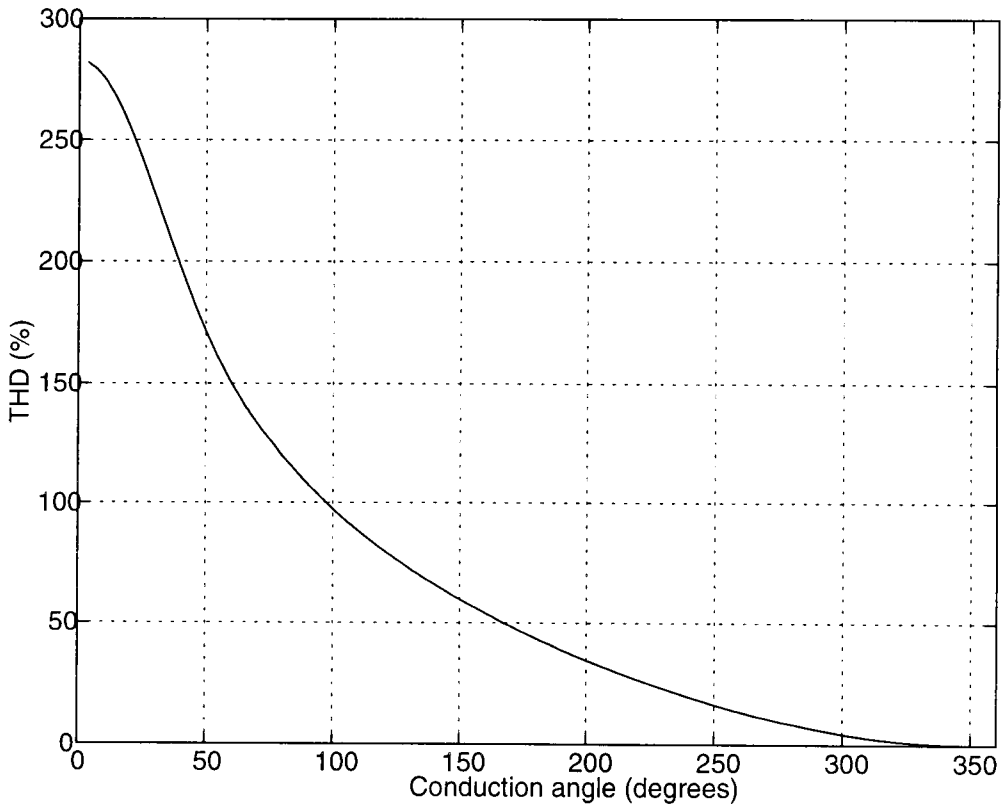

Figure 3.8 THD v/s conduction angle for a resistive load.

$$V_{in} = V_{dc} + v_m \cos\theta \tag{3.20}$$

then, neglecting the subthreshold region of operation, the conduction angle is related to the input voltage by

$$\cos\left(\frac{y}{2}\right) = \frac{V_t - V_{dc}}{v_m} \tag{3.21}$$

where V_t is the threshold voltage of the transistor. This input voltage results in a drain current waveform given by (neglecting the knee voltage and the associated linear region of operation)

$$i(\theta) = \begin{pmatrix} i_0 + i_1\cos\theta + i_2\cos 2\theta \ldots\ldots -\frac{y}{2} \le \theta \le \frac{y}{2} \\ 0 \ldots\ldots otherwise \end{pmatrix} \tag{3.22}$$

where

$$i_0 = \beta\left[(V_{dc} - V_t)^2 + \frac{v_m^2}{2}\right] \tag{3.23}$$

$$i_1 = 2\beta(V_{dc} - V_t)v_m \tag{3.24}$$

$$i_2 = \beta\frac{v_m^2}{2} \tag{3.25}$$

and

$$\beta = \frac{\mu_n C_{ox}}{2}\frac{W}{L} \tag{3.26}$$

For small values of the input voltage, the above expressions reduce to that given by equation 3.9. Using fourier series analysis, the fundamental component of the drain current waveform given by the above equation is

$$i_{f1}(y) = \frac{1}{2\pi}\left[i_0 4\sin y + i_1(2y + \sin 2y) + i_2\left(2\sin y + \frac{2}{3}\sin 3y\right)\right] \tag{3.27}$$

Thus, for a given input power, the conduction angle may be changed by changing the gate bias voltage, and the output power (or gain) will vary as either proportional to i_{f1} (for the optimum load) or as proportional to the square of i_{f1} (for a fixed load). Figure 3.9 shows the qualitative variation of power gain as a function of conduction angle for the former case. A variation of the output power of the amplifier as the input power is changed is also of extreme interest in determining the gain compression characteristics of the power amplifier. Various non-linearities result in the generation of harmonics in the output waveform as well as gain compression. Defining a large-signal transconductance, G_m, as

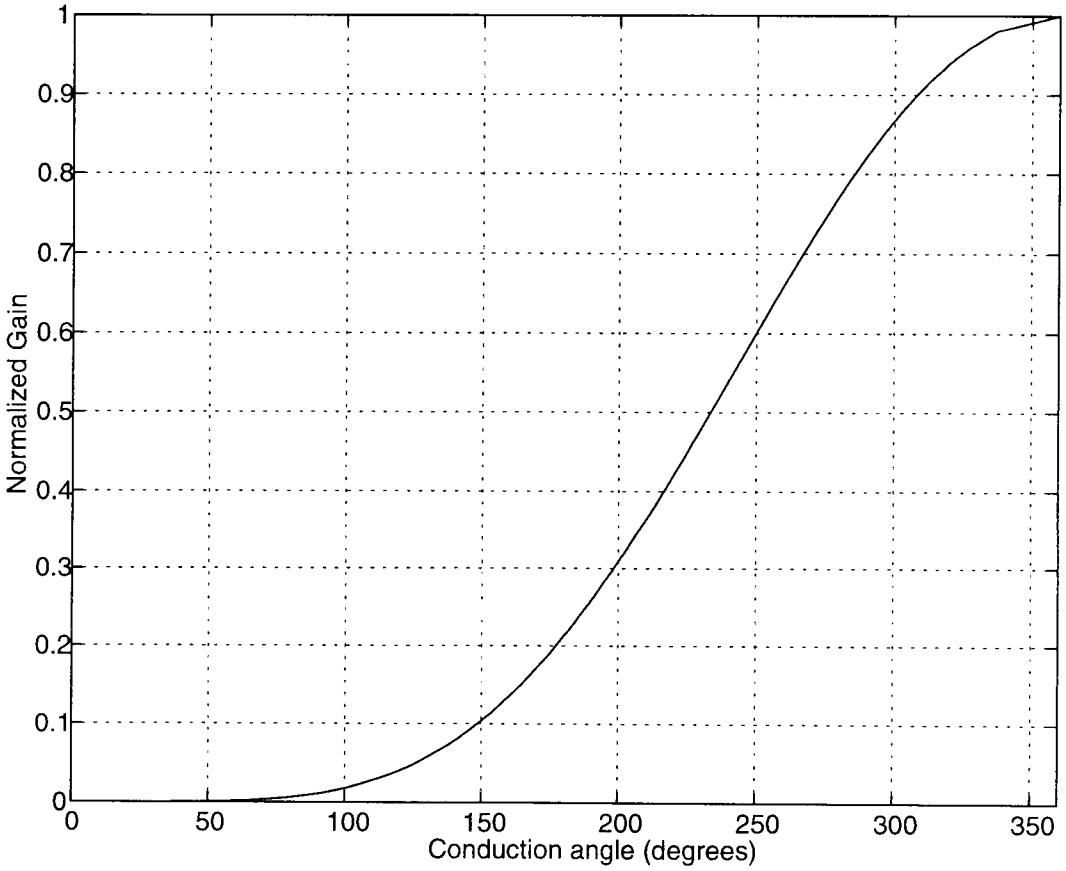

Figure 3.9 Variation of Power Gain with conduction angle for the optimum load resistances.

$$G_m = \frac{i_{f1}}{v_m} \tag{3.28}$$

an expression for the gain of the power amplifier may be derived as

$$PowerGain = \frac{\frac{1}{2} i_{f1}^{\ 2} R}{\frac{1}{2} C_{in} v_m^{\ 2} f} = \frac{G_m}{C_{in} f} G_m R \tag{3.29}$$

which simplifies to

$$PowerGain = k \frac{f_T}{f} G_m R \tag{3.30}$$

where k is the ratio of the large signal G_m to the small-signal g_m. Note that the first term in the above expression is a current gain term, and the second term is a voltage gain term. For a given input bias voltage, changing the input signal amplitude will change the conduction angle and i_{f1}, thereby changing G_m and the power gain. For lower conduction angle, the fundamental frequency drain current component reduces, thereby reducing the gain for reduced conduction angle.

3.2 Design Example

Let us design a CMOS PA for the following specifications:

Power Output = 50mW

Efficiency = 60%

Power Supply voltage = 3V

Load Resistance = 50ohm

Frequency of operation = 900MHz

3.2.1 Ideal Power Amplifier Design

From Figure 3.5, an efficiency of 60% requires a conduction angle of less than 270^{o} (i.e. the PA may be classified as a Class AB amplifier). Note that there is a direct trade-off between the efficiency and power output requirement. Designing for a higher efficiency, for a given power output, will require a larger transistor with higher maximum drain current rating. In order to deliver 50mW with a voltage swing of 3V (peak), the value of load resistance to be presented to the transistor can be calculated from the following equation

$$P_{out} = \frac{v_o^2}{2R} \tag{3.31}$$

or

$$R = \frac{3^2}{2 \times 50mW} = 90ohm$$

With this value of load resistance, and for a conduction angle y of 270^{o} (4.71 radians), the peak value of drain current can be calculated from equation (3.18) as

$$I_m = \frac{v_o \times 2\pi}{R \times (y - \sin y)} = \frac{6\pi}{90 \times (4.71 - \sin 270)} = 36.7mA$$

and

$$I_{dq} = -I_m \cos\frac{y}{2} = -36.7 \times \cos 135\text{mA} = 25.9mA$$

The maximum value of drain current that will flow through the transistor is given by the sum of I_m and I_{dq}, which in this case equals 62.6mA. Thus, a suitable transistor size can be selected knowing the amplitude of the ac signal at its input as well as its dc voltage level. The signal amplitude and dc level should be such that the transistor is on for 270^{o}

of every cycle. The transistor size should be such that the peak current in the transistor corresponds to the sum of I_{dq} and I_m and the dc (Fourier) component of the drain current is I_{dq}. The pre-amp must provide a suitable gate signal to the output stage transistor, which, in this example, is operating in the Class AB mode. The load network must be designed such that it transforms the 50 ohm load resistance to the desired value of 90 ohm at 900 MHz. If possible, the impedance transforming network should also act as a tuning network and serve to filter out the harmonic components of the current waveform.

Figure 3.10 shows the output stage of the PA with one such matching/tuning network which may be designed to transform the 50 ohm load resistance to 90 ohm at 900 MHz as well as filter out the harmonics. Here, the transistor M1 is biased to have a conduction angle of less than 270^o.

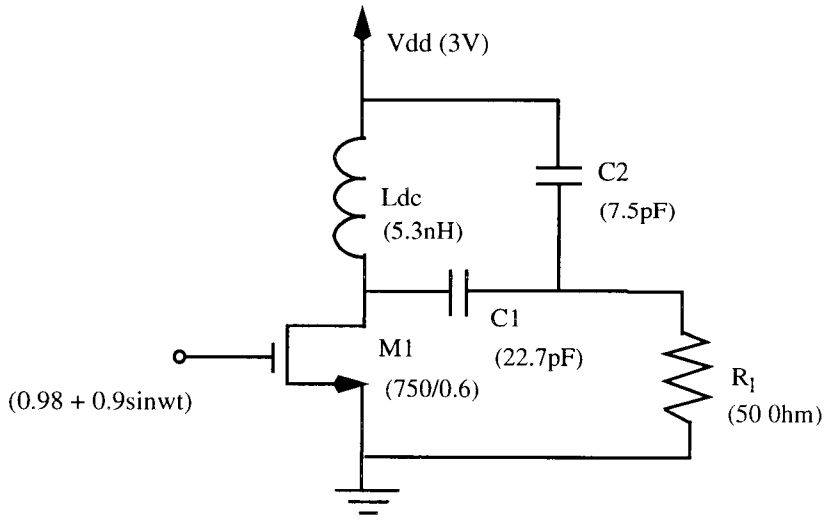

Figure 3.10 Output stage and matching network of the PA.

The inductor L_{dc} is part of the tapped-capacitor matching/tuning network and also makes it possible to obtain a high voltage swing at the drain. L_{dc}, C_1 and C_2 constitute the matching and tuning network. This network transforms the load resistance R_l to a value R at a particular frequency ω_o. Defining R_{eq} and C_{eq} as below

$$R_{eq} = \frac{R_l}{1 + \omega^2 C_2^2 R_l^2} \tag{3.32}$$

$$C_{eq} = \frac{C_1 C_{eq2}}{C_1 + C_{eq2}} \tag{3.33}$$

where

$$\frac{1}{\omega C_{eq2}} = \frac{\omega C_2 R_l^2}{1 + \omega^2 C_2^2 R_l^2} \tag{3.34}$$

the transformed value of the resistance, R, as well as the frequency at which R_l is transformed to this value, ω_o, is given by

$$R = \frac{L_{dc}}{R_{eq} C_{eq}} \tag{3.35}$$

and

$$\omega_o = \sqrt{\frac{1}{L_{dc} C_{eq} - R_{eq}^2 C_{eq}^2}} \tag{3.36}$$

The Q of this network is [36]

$$Q = \frac{R}{\omega_o L_{dc}} \tag{3.37}$$

Using the above design equations, the following results are obtained for the matching network of Figure 3.10 (designed for R_l=50ohm, R=90ohm and resonant frequency of 900MHz)

C_1=22.7pf

C_2=7.5pf

L_{dc}=5.3nH

From equation (3.37), the above network should have a Q of 3.

The above design procedure, however, ignores several effects that have a significant impact on the performance of a real power amp, namely

a) The package and device parasitics.

b) The inductance of the ground plane.

c) An ideal inductor is used in the design, whereas inductors available in standard silicon CMOS processes typically have a Q of about 4.

d) The effect of a non-zero substrate resistance is not considered.

The performance of the output stage, ignoring the above effects, is first studied and subsequently, the effect of the above non-idealities on the performance of the PA is investigated. HSPICE simulations are used to verify the performance of the above output stage design. BSIM (i.e., LEVEL=13) models, available from the MOSIS service, are used for the transistors. In order to obtain the required current level, the device size chosen was 750/0.6 and the input applied had a dc voltage level of 0.98 volt and an ac signal amplitude of 0.9 volts. The areas and perimeters of the drain and source of the transistor were ignored in order to minimize the device parasitic capacitance. Thus, as a first step, the PA output stage being simulated is nearly ideal. The parasitics will be subsequently added and their effect on the performance of this output stage will be studied. Simulation results are listed in Table 3.1. The performance achieved agrees very closely to the design. The dc value of the drain current is 25.9mA. Figure 3.11 shows the frequency response of this circuit and its drain current waveform. The Q of this circuit is 2.25. The threshold voltage of the NMOS device is about 0.5volts. Assuming that the device turns

off when V_{gs} goes below V_t, and is on when V_{gs} is above V_t, the conduction angle for the applied bias is

$$\text{conduction angle} = 180 + 2\,\text{asin}\left(\frac{0.98-0.5}{0.9}\right) = 245^{o}$$

In reality, though, the transistor does not turn off cleanly, as can be seen from the drain current waveform of Figure 3.11. The drain current does not go to zero as the gate voltage goes below threshold (the transistor enters the sub-threshold region). Thus, the conduction angle is actually greater than 245°. The dip in the drain current, seen at the peak of the drain current waveform, is due to the transistor entering the non-saturation region of operation due to the large-signal RF input applied to the gate.

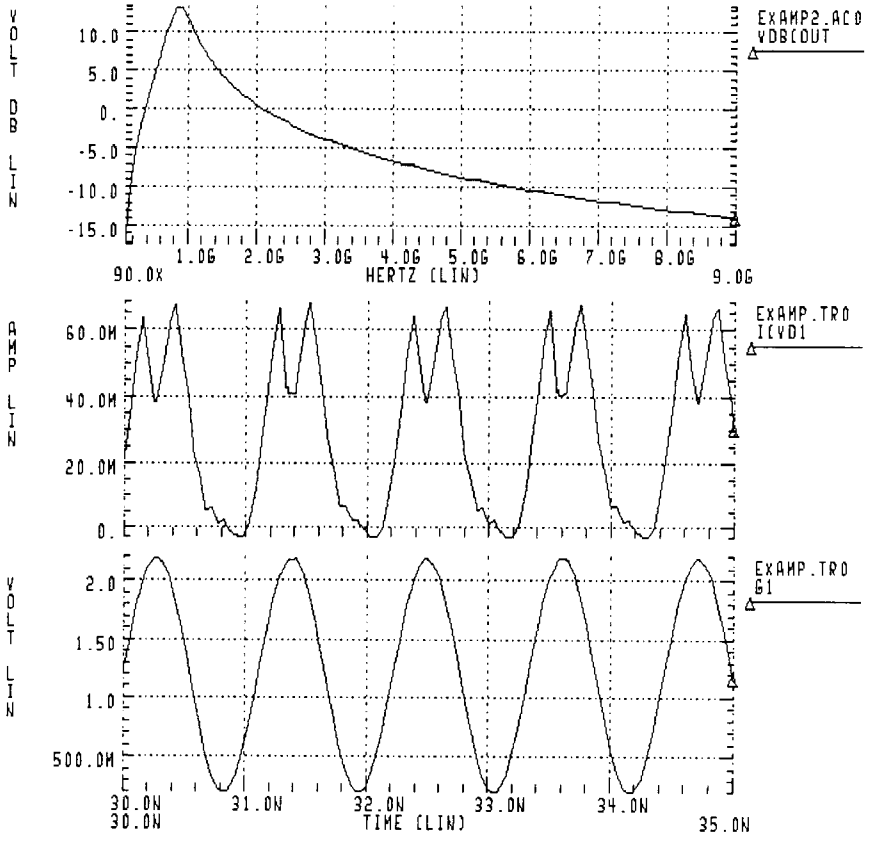

Figure 3.11 Plot of the frequency response, the drain current waveform and the gate voltage for the ideal output stage.

3.2.2 Effect of non-idealities on the output stage performance.

In an integrated power amplifier fabricated in silicon, the device as well as package parasitics have a significant impact on the performance of the power amplifier. Further, the inductance of the ground plane limits the maximum swing possible at the output and, therefore, reduces the efficiency of the power amplifier. The inductors available in silicon have low Q and losses in these inductors also reduce the efficiency of the PA. Figure 3.12 shows the output stage of the PA with package parasitics (at output, ground and V_{dd}). The inductor is still assumed to be ideal.

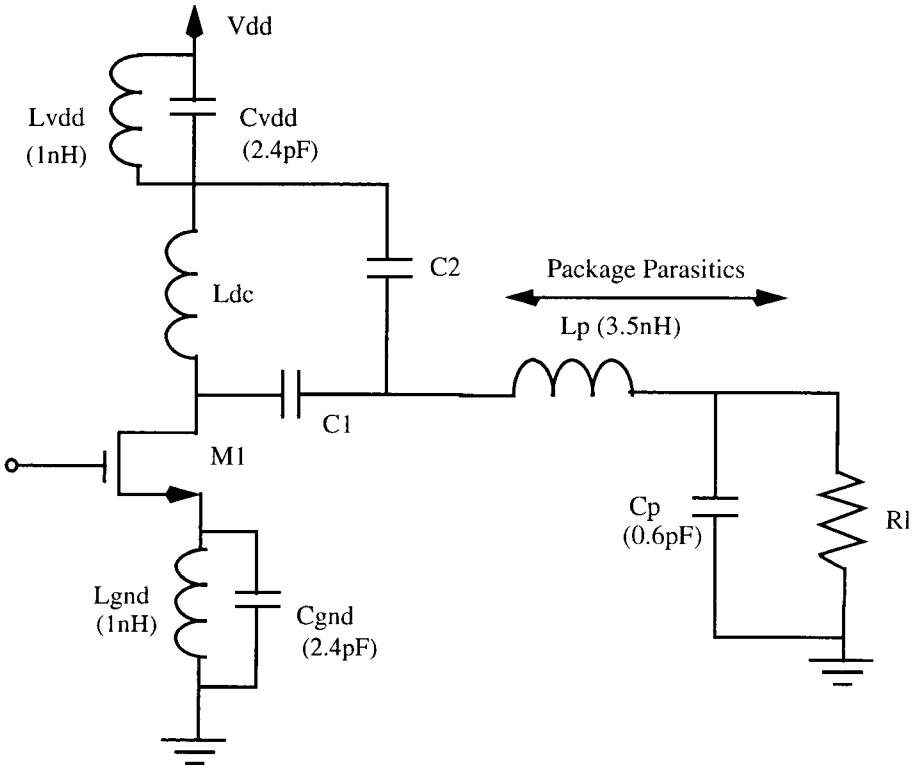

Figure 3.12 Output stage with package parasitics.

The package parasitics assumed correspond to the pins with the lowest parasitics (based on data available from MOSIS for a standard 28 pin package), and it is assumed that the

ground inductance can be reduced to 1nH (by connecting several pins in parallel, for example). The simulations results are listed in Table 3.1. The efficiency reduces to 54%. The device and package parasitics, in this example, have only a small impact on the matching/tuning network.

So far, the inductor in the drain has been assumed to be ideal. Inductors available in standard silicon processes have a Q of about 4 [25] (they achieve a higher Q if special processing steps are used [29]). Shown in Figure 3.13 is an inductor model with parasitic element values for a 5.3nH inductor obtained from the one-port version of the inductor model developed in sections 2.3 and 2.4. Figure 3.14 shows the frequency response of this inductor circuit, driven by an ideal current source. The self-resonating frequency and the Q may be obtained directly from this plot. The PA output stage performance results listed in the last column of Table 3.1 correspond to the case when the drain inductor in the output stage is replaced with an inductor modeled by the circuit of Figure 3.13

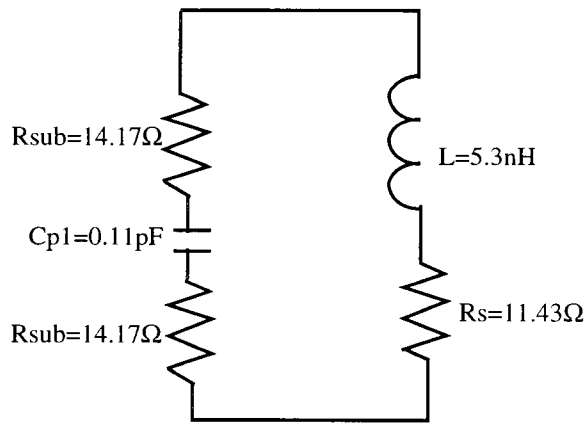

Figure 3.13 Model for an inductor fabricated in silicon.

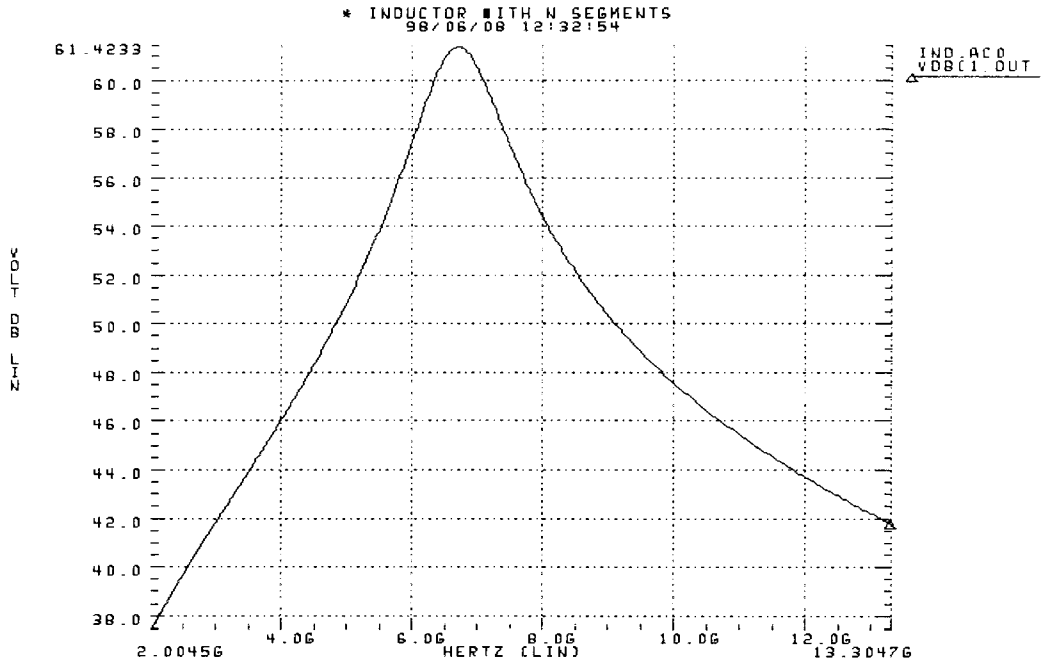

Figure 3.14 The magnitude response of the inductor circuit of Figure 3.12.

From these results, it is obvious that the poor Q inductors available in silicon have a very negative impact on the PA output stage of Figure 3.10. The efficiency drops to almost one-third of the designed value, and there is a significant reduction in the RF power output from the PA. The high loss inductor destroys the accuracy of the impedance transforming network, so that the impedance at the drain, instead of being close to 90 ohm, is 46 ohm. Losses in the inductor also contribute directly to the observed degradation in drain efficiency.

Table 3.1: Simulation results for the PA output stage (with and without parasitics)

Performance Parameter	Ideal o/p stage	O/p stage with device and package parasitics	O/p stage including all parasitics
Frequency of operation (MHz)	900	900	900
Efficiency (%)	59.9	54	20.4
PAE (%)	59.4	52.5	19.1
Output Power (mW)	53	50	24.5
Total Harmonic Distortion (dB)	-23.5	-34.2	-27.7
Fundamental frequency peak swing at drain (V)	3	2.97	2.1
Fundamental frequency peak current through drain (mA)	34.9	36.17	45.8
Impedance at drain, at 900MHz (ohm)	86	82	46

3.3 Output Stage with a PMOS Load

Based on the design example presented in section 3.2 the following conclusions may be drawn:

a) Designing an amplifier for higher efficiency, for a given power output, will require increasingly larger devices. Alternately, for a given transistor size, reducing the conduction angle will improve the efficiency of the output stage of the PA but reduce its power output.

b) The inductors available in a standard silicon CMOS process do not have performance good enough to be included in a PA stage in a conventional manner between the drain and the power supply. For the matching network shown, at least, this is not possible. Some of the possible strategies to deal with the poor Q inductors available in silicon are briefly discussed next.

The most obvious, and perhaps least attractive, solution for minimizing the impact of lossy inductors is not to use the on-chip inductor in the drain. Rather, the inductor and the matching network can be off chip. However, this defeats the goal of a fully monolithic PA. Another alternative is to compensate for the losses in the inductor by using active circuits. This requires adding a negative resistance in series [31], or parallel [32], with the inductor to compensate for its series resistance. The drawback of this approach is that the negative resistance active circuit will draw power, and therefore will also reduce the efficiency of the PA. Thus, while high quality on-chip inductors can be obtained in this manner [37], PAs are not the right application for such inductors due to the power used by the active compensation circuit. As is the case with any circuit using positive feedback, careful circuit design is required in order to ensure stability of the compensation circuit.

The other alternative is to decouple the drain inductor from the matching network (by using a large valued inductor which acts as an RF choke) and explore different topologies of matching networks which may be used, along with the drain inductor, to provide the required impedance transformation. However, the inductor suffers from high loss, and the higher is the net inductance used in the matching network, etc., the higher are the losses associated with the inductor(s) and the lower is the efficiency of the

matching network, and therefore of the power amplifier. In the example in the previous section, with a realistic model for an inductor, the output power delivered to the load is 24.5mW. However, if one computes the total RF power at the drain of the power amplifier, it is 2.1 X 45.8/2 mW or 48.09mW. The difference between this and the output power is dissipated primarily in the lossy inductor. The poor Q inductor does not allow proper impedance transformation to take place and as a result the power transfer from the drain to the load is not the most efficient possible. Thus, the goal should be to minimize the total inductance used in the circuit (to avoid excessive loss in the matching network) as well as minimize the sensitivity of the matching network to inductor parasitics.

One possibility is to remove the inductor from the drain. An inductor in the drain of the PA output stage serves one purpose - to allow a large voltage swing (ideally a peak swing equal to V_{dd}) at the drain. This, in turn, makes it possible to deliver higher RF power, for a given current, than if the signal swing were $0.5V_{dd}$ (which would be the case if any other kind of load, like a pmos transistor, were used). Thus, if the inductor is replaced by some other load, the RF power output would reduce by 2x (assuming the signal current is the same). Therefore, the efficiency of the output stage would reduce by 2x too. Replacing the inductor load with a PMOS transistor load will result in improved performance only if some way could be found to maintain the same level of RF power, while consuming the same amount of dc current. This can be achieved by applying the RF signal to the gate of both the nmos and pmos transistors [38]. Therefore, both the pmos and nmos devices will contribute to signal current, and if the impedance at the drain of the output stage transistors is low enough, this 2x current will not result in a signal swing greater than $0.5V_{dd}$. Further, the 2x increase in signal current will not

require any additional dc bias current, so that the efficiency of the PA output stage will approach that of a stage with an ideal inductor load. The pre-amp now has to be able to drive both a pmos and an nmos transistor (i.e. a higher capacitance). Further, the device parasitics are much increased (due to the presence of a pmos transistor) and their impact on the matching network may be more significant than observed in the earlier example. Also, an additional circuit needs to be included to define the dc voltage at the output node. This approach is further explored in the next section where a PA output stage design is presented without a drain inductor. Only one on-chip inductor is used as part of the matching network.

3.3.1 PA Output Stage Without Drain Inductor

In this section, the output stage of a power amplifier is designed to deliver 50mW into a 25 ohm load. This stage will be part of a fully balanced PA, supplying a total of 100mW into a 50 ohm load. *Thus, the single ended load is taken as 25 ohm.* Figure 3.15 shows the output stage circuit. The drain inductor has been replaced by a pmos transistor. The matching network is a simple LC branch. Again, the starting point is an ideal circuit, and the first step is to demonstrate that the efficiency of this circuit approaches that with an ideal inductor in the drain. Since the only inductor required in this PA output stage design is in the matching network, the topology of the matching network should be such that the inductance required is minimized. Also, the network should be designed taking into consideration the inductor parasitics.

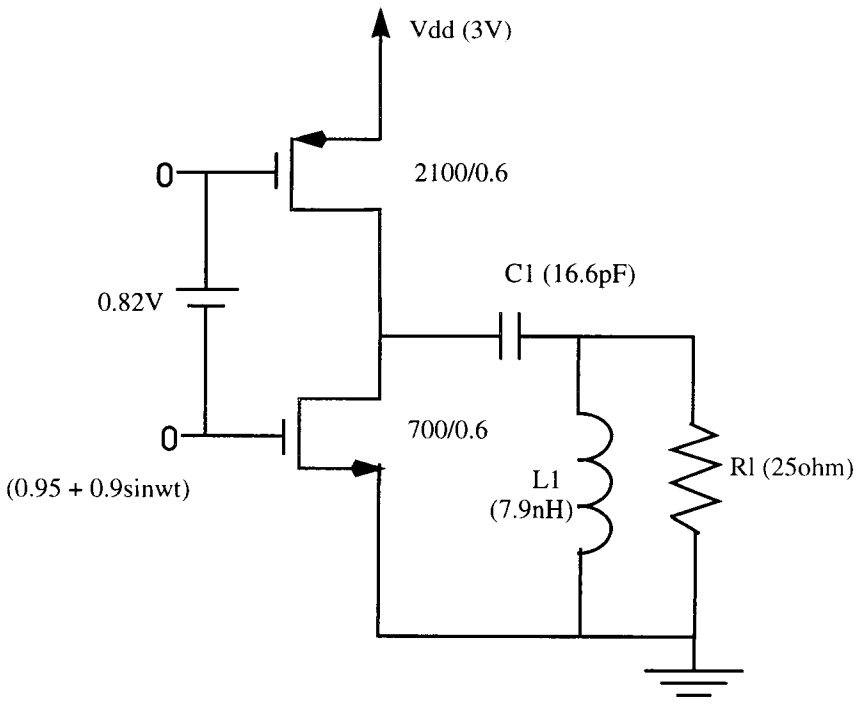

Figure 3.15 The output stage and impedance matching network

In order to get 50mW output power with a 1.3volt swing (assuming a value of 200mV for V_{dsat}), the signal current required is

$$i_1 = \frac{2 \times 50mW}{1.3} = 77\text{mA}$$

and therefore, the impedance at the drain of the transistors should be

$$R = \frac{1.3}{77\text{mA}} = 16.9\text{ohm}$$

The matching network being used transforms the load resistance R_l to a value, R, given by

$$R = \frac{L_1}{C_1 R_l} \tag{3.38}$$

at a frequency

$$\omega_o = \sqrt{\frac{1}{L_1 C_1 - R^2 C_1^2}} \tag{3.39}$$

For R = 16.9ohm and R_1 = 25ohm, and for a frequency of 900MHz, the above two equations yield

L_1 = 6.4nH

C_1 = 15.11pF

This circuit is simulated in HSPICE, again by ignoring the areas of the transistors, with input1 being 0.95 + 0.9sin(wt) and input2 being offset from input1 by a dc voltage of 0.82volt. The results are listed in Table 3.2.

The THD of this circuit is substantially higher than the design with an ideal inductor. The swing at the drains of the transistors is 1.4volts, and they are biased at a V_{dsat} of about 200mV. Thus, the transistors are entering the non-saturation region, which is causing the higher distortion seen at the output. In order to reduce the distortion, the transistors should be biased at a lower V_{dsat}, which in turn means having wider devices (so that the same drain current waveform can be obtained for a smaller input signal). However, it can be seen that the same performance in terms of efficiency and power output can be obtained without the use of an inductor in the drain.

Table 3.2: Simulation results for PA output stage with PMOS load

Performance Parameter	Ideal o/p stage	O/p stage with parasitics
Frequency of operation (MHz)	900	900
Efficiency (%)	62	37
PAE (%)	60.9	35.8
Output Power (mW)	50.5	33.9
Total Harmonic Distortion (dB)	-14.75	-13.8
Fundamental frequency peak swing at drain (V)	1.39	1.1
Fundamental frequency peak current through drain (mA)	72.8	82.66
Impedance at drain, at 900MHz (ohm)	19.2	13.3

3.3.2 Effect of Parasitics on the PA Output Stage

As was done in the previous case, various parasitic effects significant at RF frequencies are included next. The output stage was simulated again with the area of the transistors included and with package parasitics corresponding to those used in the previous case for the output, ground and V_{dd} nodes, and including the parasitics associated with the inductor. The last column of Table 3.2 lists the results obtained. The efficiency of the PA output stage, in the presence of all the parasitics, reduces to 37% and the power output to 34mW. The impedance at the drain of the transistors, instead of being 16.9ohm, is only 13.3ohm. The device, inductor and package parasitics, are significant and impact the matching network. In order to achieve better performance, these parasitics must be included in the design of the matching network. The primary reason for the

loss in efficiency is the mismatch in the impedance transformation. Instead of transforming 25ohm to 19ohm, the impedance at the drain of the transistors is 13.3ohm. The RF power at the drain of the output stage is 43.45 X 2.37 Cos(23.36) = 43.45mW (the angle between the current and voltage is 23.36^{o} since the impedance matching network is *not* transforming the real 25ohm load to a purely real impedance at the drain output). The output stage is producing 43.45mW (*with an efficiency of 57%*) but only 34mW is being delivered to the load.

Thus, even in this case, the parasitics adversely impact the output stage performance. Notice however that in both the designs presented, the transistor stage is operating at high efficiency and generating the desired RF output power at its drain. *In both cases, the poor overall efficiency results due to the inability of the matching network to efficiently transfer the power being developed at the drain of the transistor(s) to the load.* However, in the second case, the impedance transforming network can be designed to improve the power transfer from the drain to the load. For example, by increasing the capacitance to 30pF and the inductance to 20nH, the efficiency goes up to 53.7%. However, the values of the inductor and capacitor have been arrived at in an arbitrary manner. Further, there is no guarantee that these matching network element values give the best result and that further improvement in efficiency is not possible for a different matching network. Therefore, we can conclude that one critical issue which needs to be addressed in order to implement high efficiency PAs is the ability to design on-chip matching networks including package as well as active and passive element (i.e. transistor, inductor and capacitor) parasitics. This issue is addressed in the next chapter.

4. COMPUTER-AIDED DESIGN AND OPTIMIZATION

The design of a discrete/hybrid power amplifier involves selecting an appropriate device which meets the output power requirements at the given supply voltage and operating frequency, determining the optimum input and output impedance for the device using tuners (or load pull), and implementing matching networks using discrete inductors and capacitors to transform the 50Ω or 75Ω load (corresponding to the impedance of standard coaxial cables, antennae, RF measuring equipment, etc.) to the desired impedance values. On the RF board used for implementing the complete PA, a transmission line having a characteristic impedance of 50Ω is used to transfer RF power into, and out of, the active device. Assuming the input and output of the power device are matched to 50Ω, this transmission line will perform no impedance transformation, and its length will not effect the PA performance other than due to the (insignificant) loss associated with it. Substantial resources and effort, however, are spent on tuning the values of the various elements of the matching network to obtain the correct impedance transformation. Since the input or output of the power device are not matched to 50Ω by itself, the segment of the transmission line on the RF board between the device output (or input) and the first element of the matching network acts as an impedance transforming network. Very often, one aspect of tuning the PA involves sliding the various shunt elements of the matching network along the length of this transmission line in order to determine their optimum location. Indeed, it would not be an exaggeration to state that the most significant part of the design of a discrete/hybrid power amplifier is performed on the test bench. A monolithic PA implementation eliminates the need for tuning the

PA on the test bench, but requires that the optimum load impedance be determined, and corresponding integrated matching networks designed, *before* fabrication of the amplifier. This may be accomplished by utilizing the available device models to predict the optimum input and output impedances for the power amplifier, and the models for the passive element may be used to design integrated matching networks. This chapter discusses a CAD tool which has been developed to optimize PA efficiency by determining the optimum load impedance for the device and design input and output monolithic matching networks for the PA. It is based on the well known simulated annealing heuristic [39]-[41], and uses BSIM II (LEVEL 39) models for the active devices and the compact inductor model developed in chapter 2 for inductors. Bottom- plate parasitics of floating capacitors are estimated from available process data.

4.1 Simulated Annealing based CAD tool

As has been observed from the design examples in the previous chapter, while the PA output stage can generate RF power with high efficiency, it is critical to have the required tools to design the matching network to transfer power efficiently from the output stage to the load. While simple matching networks can be designed using lumped elements with the aid of Smith chart [42], such an approach is not accurate enough for this case, as can be seen from the two design examples presented in chapter 3. The inductor and its associated parasitics can not be treated as distinct lumped elements as their values depend upon each other. Thus, if a given impedance value is required to be implemented by an inductor, an iterative approach needs to be taken to determine what inductance value, together with its associated parasitics, provide an impedance closest to the desired value. This process is too cumbersome for design by hand and requires a

CAD tool. Transmission line matching is also not feasible since, at 900MHz, the length of the transmission line would be of the order of several centimeters, which is impractical for integration on silicon. While the efficiency of the matching network directly effects the efficiency of the power amplifier, the ability of the matching network to transform the 50Ω load impedance to an impedance value appropriate for the power device(s) is also critical to the performance of the PA. In general, load pull is used to determine the optimum input and output impedance values for the amplifier [43], and matching networks are designed to transform 50Ω to these impedance values. A poorly designed matching network results in sub-optimal power generation in the active device. *In such a case, even a low loss matching network will result in poor efficiency PAs.*

There are, consequently, two criteria to be considered in designing optimal *integrated* matching networks for power amplifiers (in contrast, off-chip matching networks tend to use low loss inductors and capacitors, and the primary concern there is to present the correct load impedance to the device). Firstly, the matching network should be able to transform the load impedance into the impedance value that the power devices require. This will allow the device to generate RF power in the most efficient manner. Secondly, the power loss in the matching network should be minimized as it directly impacts the overall efficiency of the PA. Since planar inductors fabricated in a digital CMOS process suffer from very high loss, a trade-off exists between the total inductance value used in the matching network and its functionality of impedance transformation. *It is conceivable that an integrated matching network may not perform optimum load impedance transformation, but still result in higher overall efficiency due to lower loss in it, compared to an optimal (with respect to impedance transformation) integrated matching network!* A CAD tool, based on simulated annealing, has been developed to explore this trade-off and design integrated matching networks which optimize the effi-

ciency of PAs. Note that this trade-off does not exist for designs using off-chip matching networks since the loss in these matching networks is very low.

4.1.1 The Simulated Annealing Algorithm

Simulated annealing is a heuristic which can be used to iteratively arrive at a solution to a problem while minimizing some error function. Simulated annealing is not guaranteed to arrive at the best solution every time (hence it is a heuristic and not an algorithm). However, as the number of iterations increases, the probability of arriving at the best solution approaches unity [40]. This algorithm is based on the metallurgical process of annealing. Annealing involves first heating a metal to a high temperature, and then allowing it to cool slowly at a controlled rate. Heating of the metal allows the atoms to rearrange into any one of numerous possible arrangements, and slow cooling allows these atoms to settle into a highly ordered structure. In simulated annealing, the attainment of the global optimum for an optimization problem is analogous to the formation of a highly ordered metal structure in the case of conventional annealing. Similar to its metallurgical counterpart, in this case too the "temperature" of the solution to the problem is gradually reduced and at lower temperatures, the system approaches the optimum solution (analogous to a highly ordered state in the metallurgical annealing of solids). This algorithm has the advantage that the probability of getting trapped in a local minima is low since at higher temperatures, the solution has enough energy to jump out of the local minimum. As the temperature is reduced, and if enough iterations are carried out at each temperature, the simulated annealing algorithm should settle down in the global minima, rather than being trapped in a local minima. However, since it is not certain that the final solution corresponds to the global minima, simulated annealing is not certain to converge to the best possible solution. Figure 4.1 illustrates the concept of global and local minima using a two-dimensional plot. The cost, plotted

on the y-axis, is an indicator of the extent of optimization of a problem. The configuration, or state, which may be defined as a set of values for variables of the problem which impact the cost function, is shown on the x-axis. In general, there may exist a solution set corresponding to a global minimum in the cost function as well as for several local minima. A gradient algorithm like the steepest descent algorithm only accepts solutions which result in improved cost, and therefore will find the global minimum only if the initial solution set, or configuration, lies between the two dotted lines shown in Figure 1. In contrast, simulated annealing is likely to find the global minima irrespective of the starting solution as it conditionally accepts solutions of higher cost from one iteration to the next.

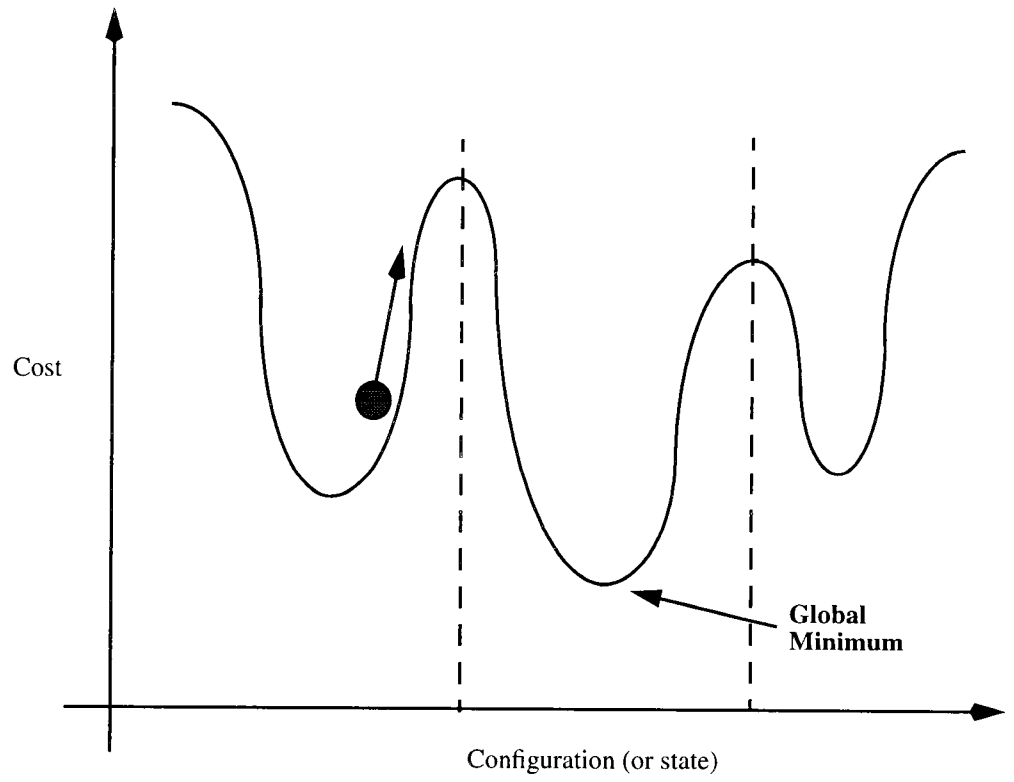

Figure 4.1 Global and local minima for a given cost function.

The Metropolis algorithm is commonly employed to simulate the process of annealing. Figure 4.2 shows the simulated annealing algorithm, as well as the metropolis algorithm (based on [40]).

```
Algorithm Simulated Annealing

begin
    T = initial temperature;
    S = initial solution;
    M = number of iterations to be carried out at initial temperature;
    maxtime = total number of iterations;
    time = 0;
    α = cooling rate;
    β = constant;

        repeat
            Call Metropolis(S,T,M)
            time = time + M;
            M = β x M;
            T = α x T;
        until (time > maxtime);
        Output best solution
end

Algorithm Metropolis(S,T,M)

begin
        repeat
            New_S = S + ΔS
            Δc = Cost(New_S) - Cost(S);
            If (Δc < 0) or (random < exp(-Δc/T)) then S = New_S
            M = M-1;
        until (M=0)
end
```

Figure 4.2 The Simulated annealing and Metropolis algorithms.

In the Metropolis algorithm, a certain number of iterations are performed at a given temperature. For each iteration, a new solution set is generated by randomly varying the

solution in the previous iteration, and the cost function for this new solution set is evaluated. If this solution results in a lower cost, it is accepted. However, it is *conditionally accepted* even if it results in a higher cost. The probability of conditional acceptance is determined by comparing a random number against a threshold. Only if the random number is lower than the threshold is the higher cost solution accepted. The threshold value is a function of the increase in cost as well as the current temperature. At higher temperatures, there is an increased probability of accepting a higher cost solution. Simulated annealing begins by selecting an initial temperature and number of iterations to be performed at this temperature, and carrying out the Metropolis algorithm for this temperature. Subsequently, the temperature is lowered, the number of iterations is increased, and Metropolis is called again. This process is repeated until the terminating criterion for simulated annealing is met. Alternatively, the algorithm may be terminated after a certain number of iterations.

4.1.2 Simulated Annealing and PA Optimization

Practical design experience indicates that there is more than one set of values for the elements of a matching network being used to tune an RF circuit which results in acceptable performance. Simulated annealing is ideally suited to find the global minimum in the presence of such local minima. A CAD tool has been developed, based on simulated annealing, to optimize the performance of CMOS RF circuits by minimizing the impact of device, inductor and package parasitics on circuit performance. This tool may be used in the design and optimization process in a variety of ways. For example, it may be used only to design matching networks with high loss inductors (it took 10mS system time on a HP712/80MHz machine to design an L-section to transform 50ohm to

19.86 + j6.04 ohm with the goal being 20 + j6 ohm). It may also be used to directly optimize the circuit/package being designed. In such case, it would be used to determine the optimum pin configuration for a given package, as well as the design of any integrated passive networks. However, maximum benefits are realized if it is used to determine the optimum *large-signal* load impedance required by the PA in the presence of various parasitics, as well as design integrated matching networks. As noted earlier, in the design of monolithic PAs using lossy matching networks, there is an important trade-off between the loss in the matching network and its impedance transformation property. Note that the goal is to maximize the efficiency of the PA, not necessarily to present the correct load impedance to the active device. Using a matching network that presents the right load impedance to the PA results in the active device generating RF power most efficiently. *However, if the resulting matching network has very high loss, this may not translate into the most efficient PA since the power available at the load is reduced by the losses in the matching network.* There will also exist matching networks which may not present the optimum load to the device, but may also have lower losses than the matching network required for optimum load impedance. In this case, the effect of reduced efficiency due to improper impedance transformation may be offset by the reduced loss in one of these matching networks, and the overall PA efficiency may actually improve by using one of the latter matching networks. This CAD tool may be used to explore this trade-off in monolithic PA design. Therefore, while this tool may be used in a variety of ways to improve the performance of integrated RF circuits, the benefits realizable by using this CAD approach increase significantly in the design of fully integrated circuits using high loss matching networks.

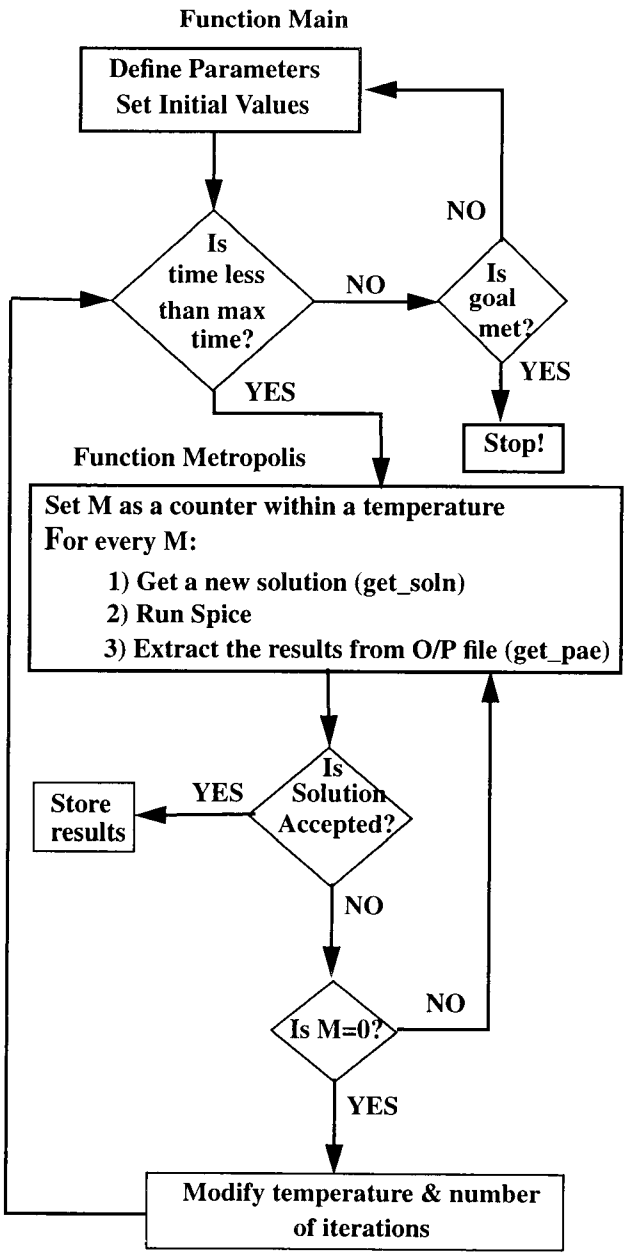

Figure 4.3 Flow of the simulated annealing CAD tool.

Figure 4.3 shows the flow chart for this CAD tool. As is the case in simulated annealing, a certain number of iterations are carried out at each temperature. Each iteration involves selecting a solution set (which may consist of values for the various pas-

sive elements, as well as package parasitic values corresponding to specific pins of the package) and evaluating the cost, or error, function. This function is the efficiency in this case. The solution is accepted if it is better than the previously accepted solution, and conditionally accepted otherwise. This process is repeated for different temperature values until either a certain number of iterations are performed or the goal is met. The initial temperature, the cooling rate, and the number of iterations to be carried out at each temperature were determined by trying several values for these parameters. This tool was initially implemented using C code for use in the design of lossy matching networks only. However, this implementation is not suitable for directly optimizing the PA efficiency as discussed above. Consequently, the code was converted into Perl [44], and modified such that it used HSPICE to evaluate the efficiency of the PA when delivering full output power. The algorithm is set-up to run a certain number of iterations, and stops once that number is reached.

Figure 4.4 illustrates the working configuration of this tool. The simulated annealing algorithm, implemented in Perl, involves running transient analysis on the circuit to be optimized, reading the efficiency from the HSPICE output file, deciding if or not the solution is to be accepted, generating a new solution set, modifying the HSPICE netlist, and repeating the above process. The accepted solutions, as well as the power output, efficiency and harmonic distortion, are documented in a separate output file. The parametric inductor model equations, developed in chapter 2, were also incorporated into the CAD tool.

4.2 Optimized PA Output Stage Designs

In this section, two PA design stages are presented. Both the stages are designed to supply 100mW into a 50Ω load at 900MHz, and operate from a single 3V power supply. While the first design does not have an integrated input matching network, the second stage includes such a network. For the first design, it is argued that for a fully integrated PA implemented as part of a single-chip transceiver (or for which the RF circuits are implemented on a a single chip), matching the input impedance of the PA to a fixed, known impedance value is not critical, and such PAs do not require input impedance matching networks.

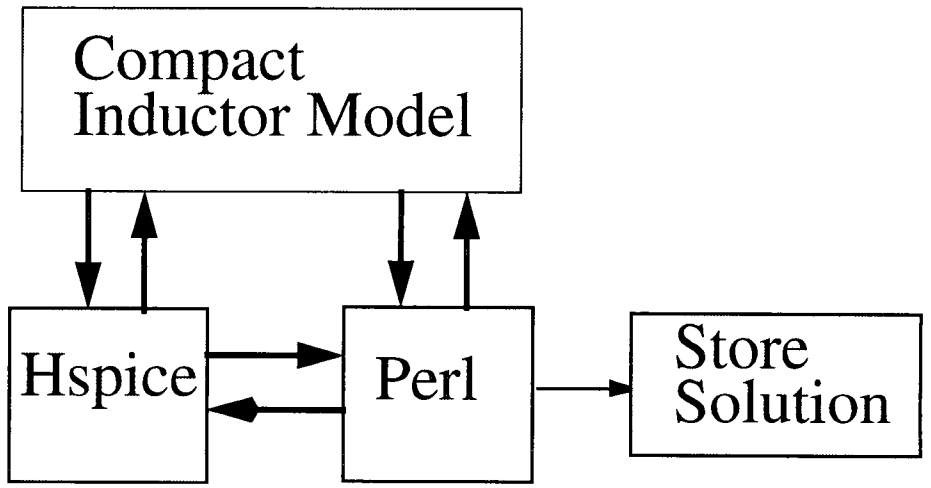

Figure 4.4 Working flow-diagram of the CAD tool.

4.2.1 PA Stage with Integrated Output Matching Network Only

Figure 4.5 shows the PA stage of Figure 3.14 implemented as a Class AB amplifier. The conduction angle of the PMOS transistor is determined by its threshold voltage

and the dc voltage applied to its gate. A feedback amplifier is used to set the NMOS gate voltage such that the output dc voltage is $V_{dd}/2$. The RF output signal is low-pass filtered and compared with $V_{dd}/2$ at the input of the feedback amplifier. The output of this feedback amplifier is used to provide gate bias to the NMOS power device. The RF input signal is capacitively coupled to the PMOS and NMOS gates, as shown in the figure.

This simulated annealing based CAD tool was used to optimize the PA output stage of Figure 4.5 for maximum drain efficiency. The goal was to design an integrated PA stage which would output 100mW into a 50Ω load, at 900MHz, and work from a single 3V supply. In order to realize the maximum degree of optimization, the determination of the appropriate load impedance and the design of a corresponding matching network were combined into a single step.

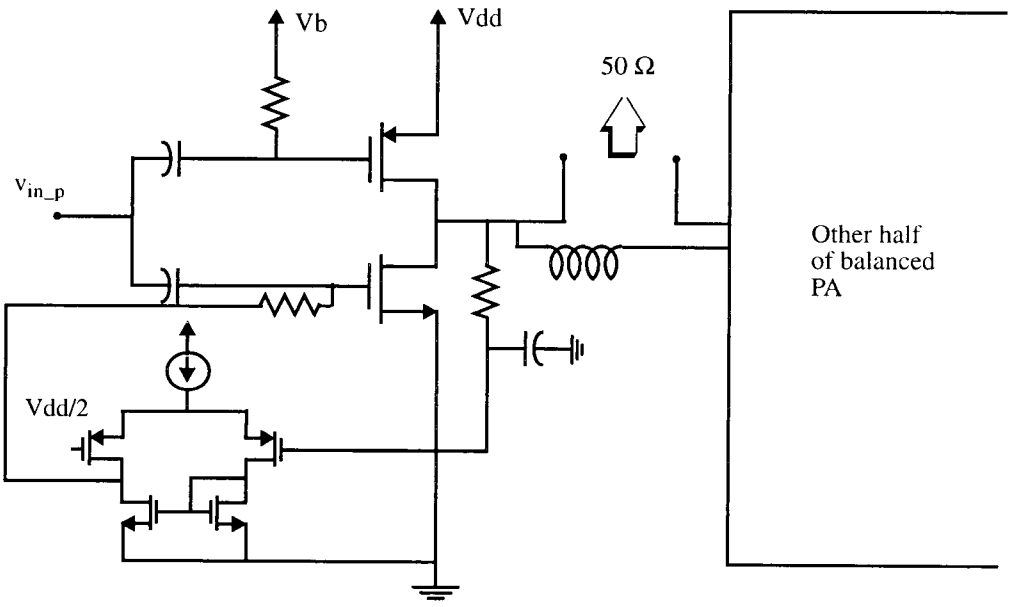

Figure 4.5.Balanced PA with a PMOS load.

Optimizing for the PA efficiency with a high loss matching network at the output allowed the design to reach an optimum between the impedance transformation and the loss in the matching network. During the optimization process, the topology as well as the value of the elements forming the matching network were changed. Various matching network topologies were used in order to present a wide spectrum of possible load impedance values to the active devices. This ensured transformation of the 50Ω load resistance to the optimum load impedance that the power devices required in order to generate RF power efficiently. Figure 4.6 shows the various matching networks considered and simulated for this PA stage.

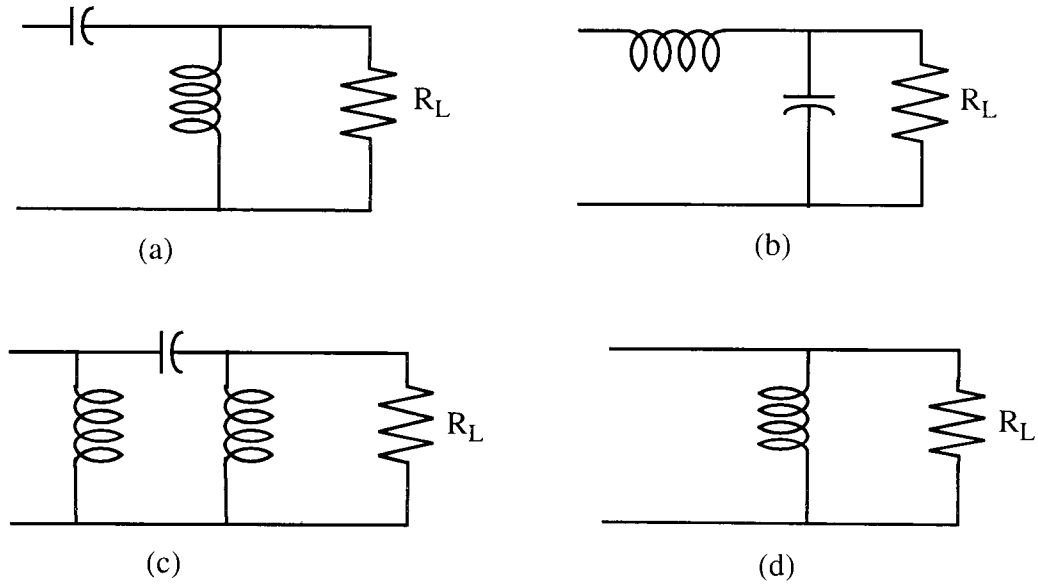

Figure 4.6 Topologies considered for output matching network of PA (a) High-pass L-section (b) low-pass L-section (c) π-network (d) shunt inductor.

Topologies include two L-sections, a pi section, and a simple inductor. Before optimization the PA exhibited a drain efficiency of 36% using an L-section as an output match.

After 4 days of optimization, an high-pass L-section was found for which the PA had an efficiency of 49%, while a simple shunt inductor (Figure 4.6(d)) used as the matching network achieved an efficiency of 57%. The pi-section resulted in a maximum efficiency of about 40% only. It is noteworthy that the best efficiency result was obtained when using just a simple inductor as the output matching network. The inductor transforms the 50Ω load into a complex impedance but results in better efficiency than the more complex matching networks due to reduced loss in it. This is a specific case where the impact of loss in the matching network dominates the impact of sub-optimal load impedance presented to the PA.

Figures 4.7 and 4.8 show the post-layout simulated performance of this PA stage using the matching network of Figure 4.6(d). Details of the layout, as well as the die photo, are included in chapter 5. The inductance value for each half of the balanced PA was 11nH. In order to save die area, and to obtain an improvement in the Q-factor of this pair of inductors, the two inductors were implemented as a single spiral rather than as two separate coils. The advantages of this approach were outlined in chapter 2. The distributed model for inductors, developed in chapter 2, was used to verify the final design and to obtain the post-layout simulation results shown in Figures 4.7 and 4.8.

4.2.2 PA Stage with Integrated Input and Output Matches

The PA stage presented above can be easily integrated with the other building blocks of a transceiver on to a single chip. *In such a case, its input is not required to be matched to 50Ω.* Presenting a fixed, known input impedance (50Ω or 75Ω) is critical in

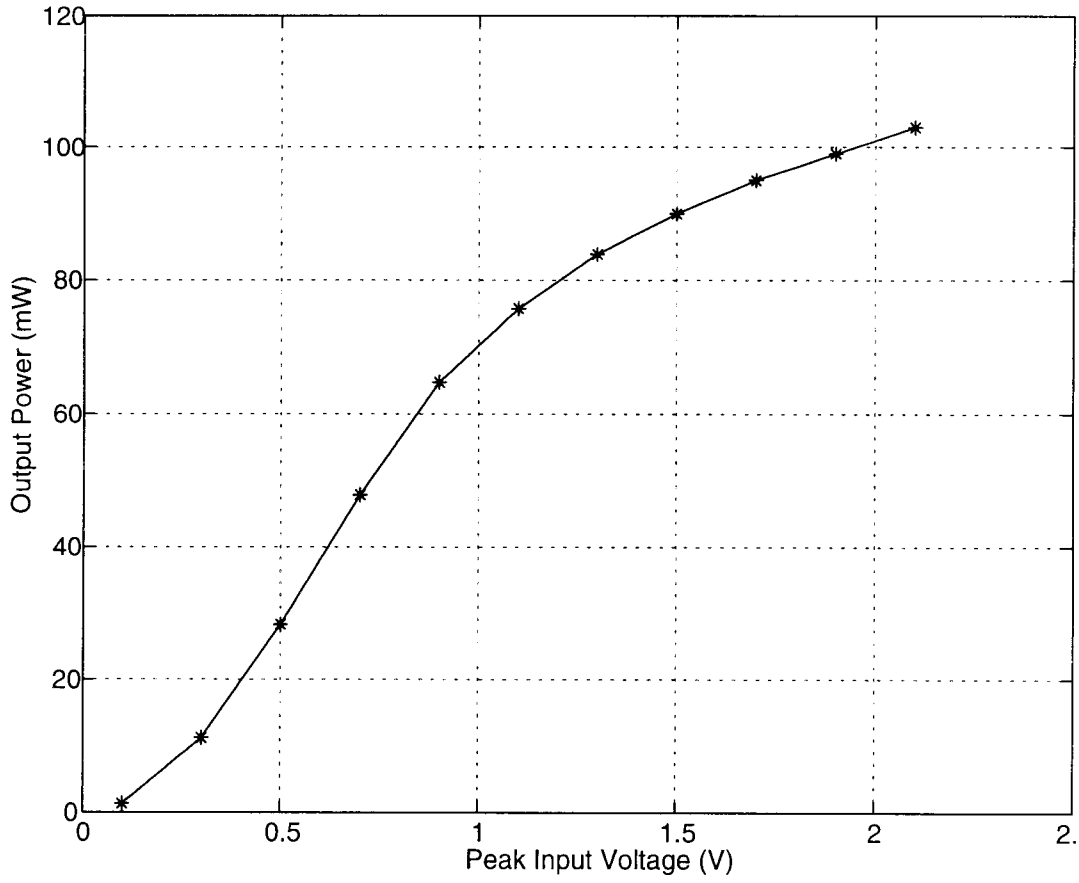

Figure 4.7 Post-layout simulation of output power v/s input voltage for PA at 900MHz.

the case when the interface to the power amplifier input is off-chip. In order to facilitate easy interface between the various building blocks found in RF transceivers, all the external input and output ports of RF circuits are matched to 50Ω (or 75Ω), and the performance of these circuits is rated for operation under these conditions. Since traditionally many of the RF building blocks have consisted of discrete implementations, ease of interfacing these circuits has been very critical. Presenting an arbitrary load impedance may result in significant degradation in the performance of these building blocks [1], and complicate the operation of these circuits in a transceiver. For example, if the PA

input impedance is not fixed, *and the PA is a discrete implementation*, the matching network following the driver to the PA will have to be redesigned every time any changes are made in the RF board, or the bias of the amplifier etc. Therefore, while there is no requirement for matching the ports of circuits which are fully integrated, *the interface with the outside world does need to be matched to a fixed impedance*. Consequently, since the PA stage presented above can be integrated with the other RF circuits, its input matching to 50Ω is not essential. However, the output does need to be matched to 50Ω since it drives an external band-pass filter or antenna.

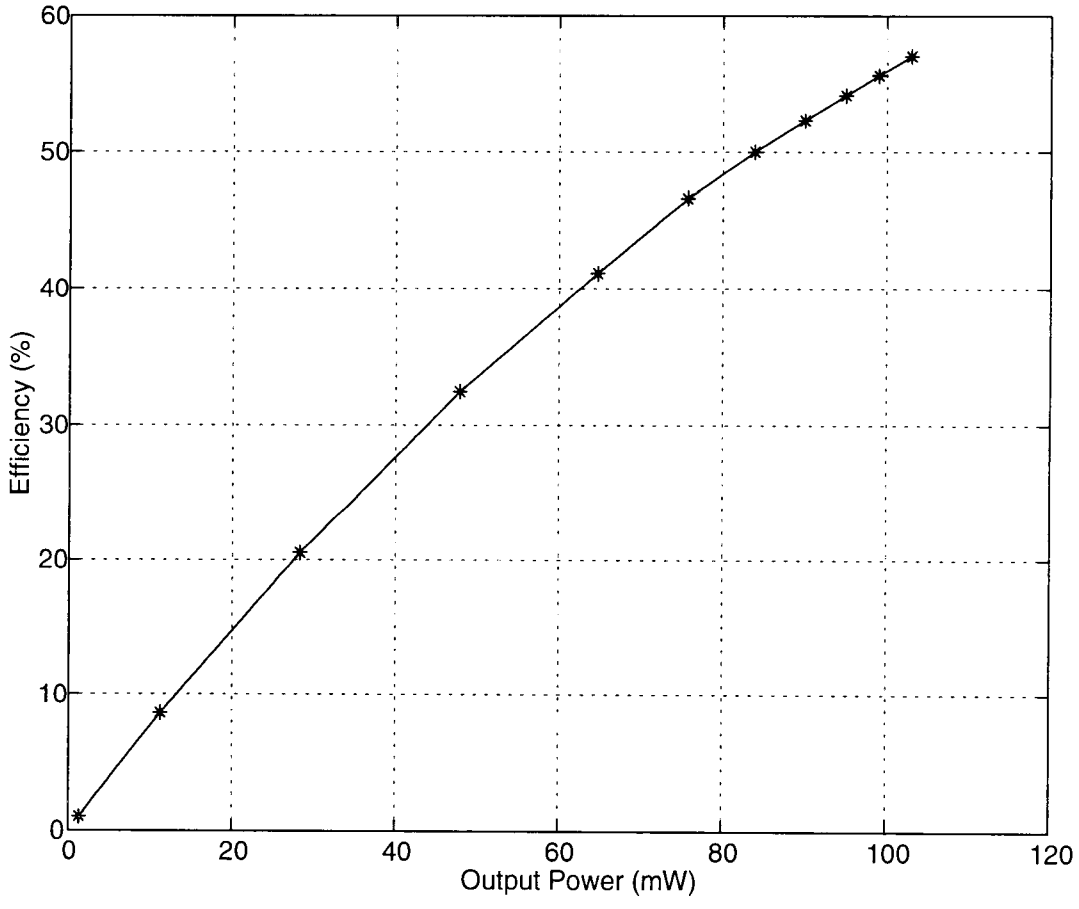

Figure 4.8 Simulated output power v/s efficiency for PA at 900MHz.

Another issue which dictates input/output port matching is the requirement of measurement and characterization equipment for RF circuits. At UHF or higher frequencies, the performance of circuits is characterized by measuring signal power, instead of the conventional low frequency quantities of signal voltages and currents. Thus, instead of quantifying voltage gain, the performance is specified in terms of *power* gain of the amplifier. Linearity is specified by the input third-order intercept (IIP3) and the 1-dB compression point (where the *power* gain compresses by 1-dB). Network analyzers are used to measure the two port S-parameters of an amplifier circuit, and obtain information about power gain (S_{21}), as well as input (S_{11}) and output matching (S_{22}) and reverse isolation (S_{21}). For large signal characterization, bi-directional couplers and power meters are used to obtain the power gain and matching characteristics of large-signal amplifiers (e.g. power amplifiers). The S-parameters of any real amplifier are a function of the terminating load impedances, which are 50Ω (or 75Ω) in the case of commercial network analyzers. For example, S_{11} for port 1 of a two-port network depends upon the impedance which terminates port 2, and in the case of commercial network analyzers, this impedance will be either 50Ω or 75Ω. Further, the mismatch between the characteristic impedance of the measurement system (50Ω in most cases) and the input and output impedances to which the amplifier is matched, will alter the S-parameters of the amplifier. As an example, the (transducer) power gain of an amplifier can be derived to be (see, for example, [45])

$$PowerGain = \frac{|S_{21}|^2(1-|\Gamma_s|^2)(1-|\Gamma_l|^2)}{|1-\Gamma_{out}\Gamma_l|^2|1-\Gamma_s S_{11}|^2} \tag{4.1}$$

where S_{21} is the power gain of the transistor amplifier, and the various reflection coefficients - Γ_s, Γ_l and Γ_{in}, are defined at the reference planes as shown in Figure 4.9.

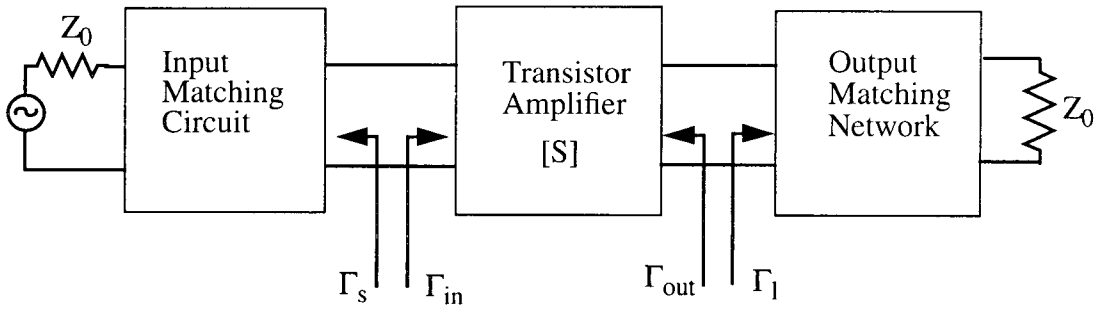

Figure 4.9 A transistor amplifier with input and output matching networks.

The S-parameters are defined for a system characteristic impedance of Z_o. It can be seen that the input/output matching networks impact the measured transistor amplifier power gain due to their effect on the reflection coefficient values. Therefore, the power gain for the amplifier may be defined as the product of three gain terms - the gain in the input matching network (actually a loss term), the gain in the transistor amplifier, and the gain (loss) in the output matching network. The loss terms due to the matching networks depend upon the losses in the non-ideal components used in the matching network, as well as upon any impedance mismatch and the corresponding reflection of power back from the load towards the source. Thus, in order to be able to characterize a CMOS power amplifier in the conventional manner requires an input matching network to minimize reflections. This is also important from the point of view of stability of the amplifier, as well as allows the driving signal source to work effectively. A two-port network

can result in oscillations if either the input or the output port exhibits a negative resistance [46]. A necessary and sufficient condition for stability of a two-port network is given by[46]-[47]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|}{2 \cdot |S_{12}S_{21}|} > 1 \tag{4.2}$$

and

$$|\Delta| < 1 \tag{4.3}$$

where

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{4.4}$$

As is evident from these equations, a lower value of S_{11} is desirable in meeting the above criterion for stability.

Due to the above reasons a second power amplifier was also designed in which an integrated input matching network was implemented. In this design, the CAD tool was used to optimize the amplifier for maximum power added efficiency. In general, a purely capacitive impedance cannot be transformed to a real impedance by any L-section. Since the input impedance of a MOS device is primarily capacitive, it is very difficult to realize a practical L-section input matching network. Consequently, a bridged T-coil was used as the input matching network [48]. The bridged T-coil can be designed to match an arbitrary impedance value to 50Ω, for example. Figure 4.10 shows the bridged T-coil circuit. In this circuit, the impedance Z_{load} is being transformed to a value of R at the input to the bridged T-coil network. Assuming that Z_{load} is given by

$$Z_{load} = R_{load} + j\omega L_{load} + 1/j\omega C_{load} \tag{4.5}$$

the values of L_1, L_2, M and C_B can be chosen such that Z_{in} is equal to R for an arbi-

trarily high frequency, resulting in a broadband match. Equating the input impedance expression to R at arbitrary frequencies results in the following design equations for the elements of the bridged T-coil network [48]

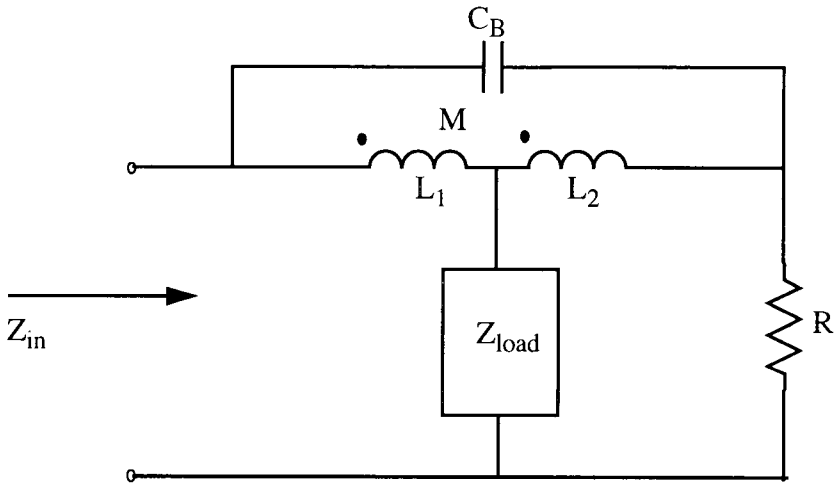

Figure 4.10 A bridged T-coil circuit used to transform an impedance Zload to R.

$$L_1 = \frac{C_{load}}{4}\left[1 + \frac{1}{4\delta^2}\right][R + R_{load}]^2 - RR_{load}C_{load} - L_{load} \tag{4.6}$$

$$L_2 = L_1 + RR_{load}C_{load} \tag{4.7}$$

$$M = \frac{C_{load}}{4}\left[R^2 + R_{load}{}^2 - \frac{1}{4\delta^2}(R + R_{load})^2\right] + L_{load} \tag{4.8}$$

$$C_B = \frac{C_{load}}{16\delta^2}\left[1 + \frac{R_{load}}{R}\right]^2 \tag{4.9}$$

where $\delta = 0.707$, and is a parameter that sets the bandwidth of the transimpedance transfer function between the voltage across Z_{load} and the input current. The above value of δ

results in a maximally flat response for this transfer function. Figure 4.11 shows one stage of the balanced, 100mW, 900MHz power amplifier with a bridge t-coil input matching network. Figure 4.12 and Figure 4.13 show the simulation results for the PA with the bridged T-coil input matching network. The CAD tool was used to optimize this circuit for maximum PAE (and not for minimum input return loss), and this resulted in a circuit with an input return loss of 10.7dB. The next chapter discusses the details of the layout, as well as some measurement results.

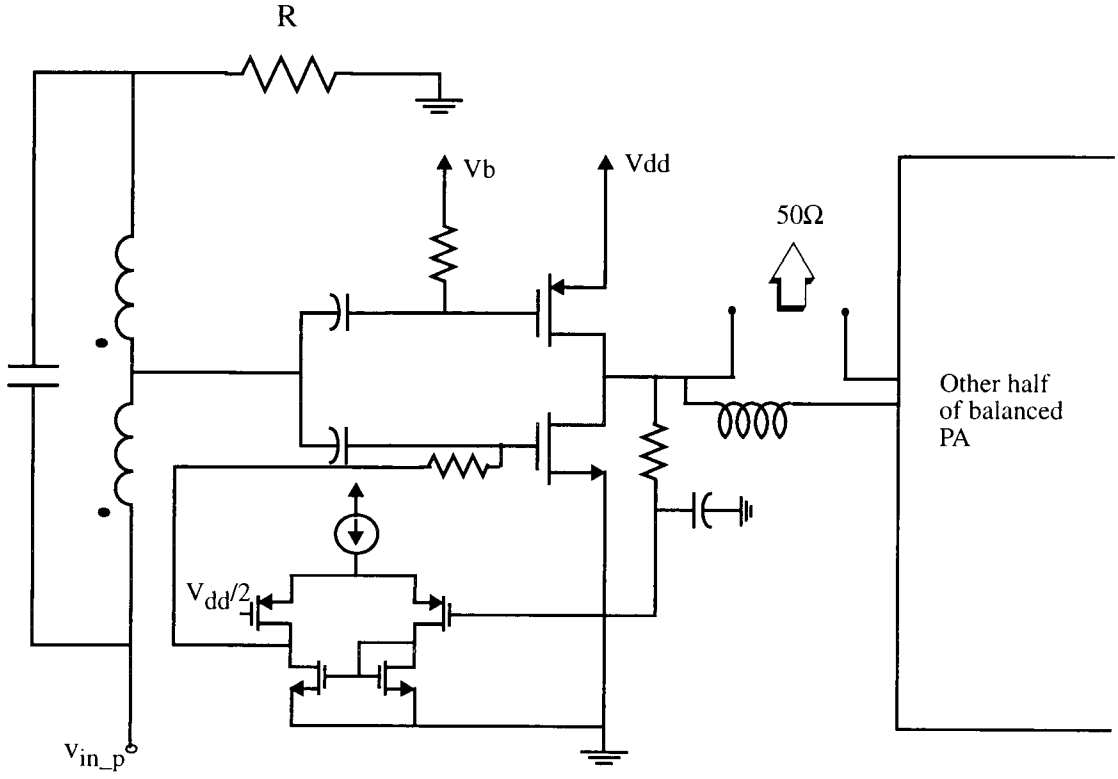

Figure 4.11 A 900MHz, 100mW, balanced PA with integrated input and output matching networks.

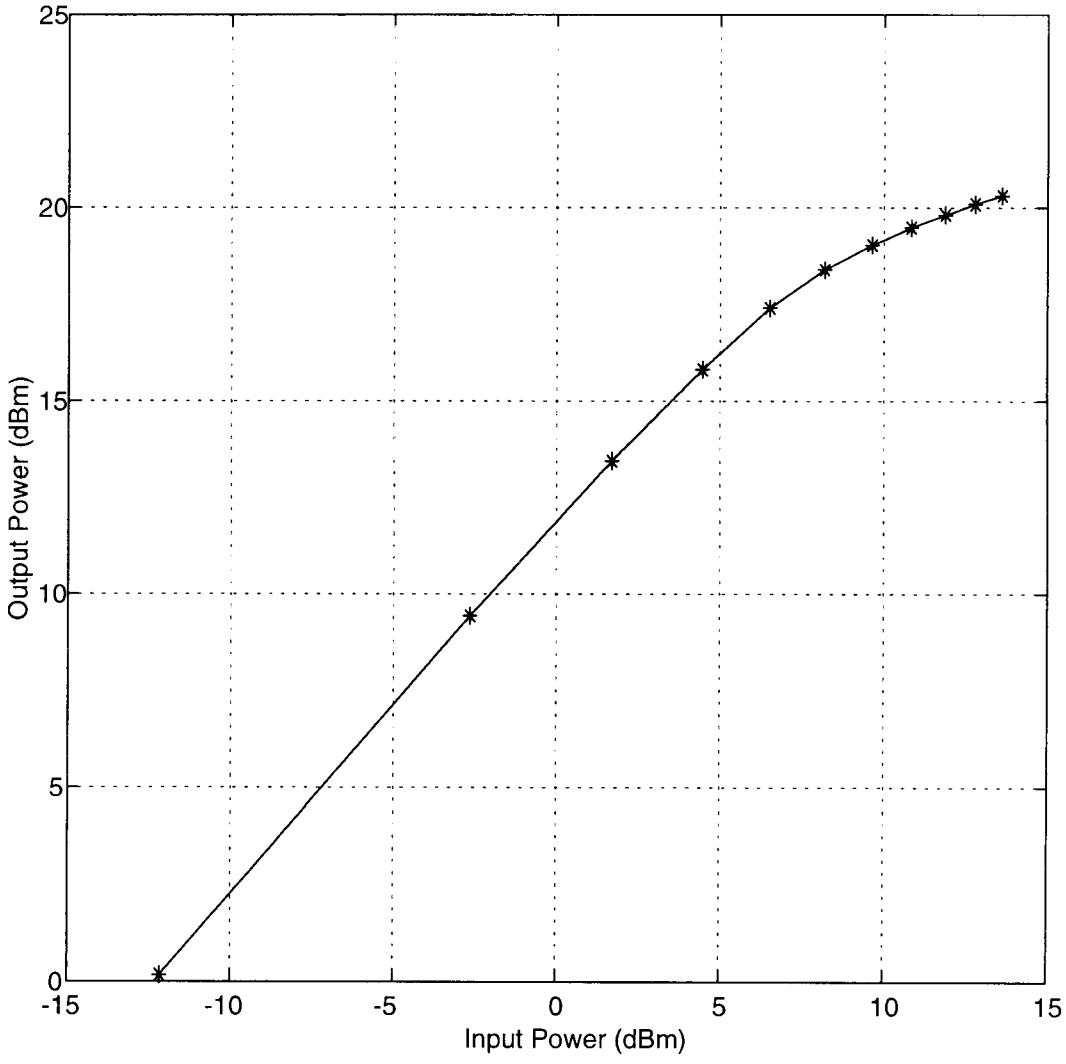

Figure 4.12 Simulated output power v/s input power for the PA with input match, at 900MHz.

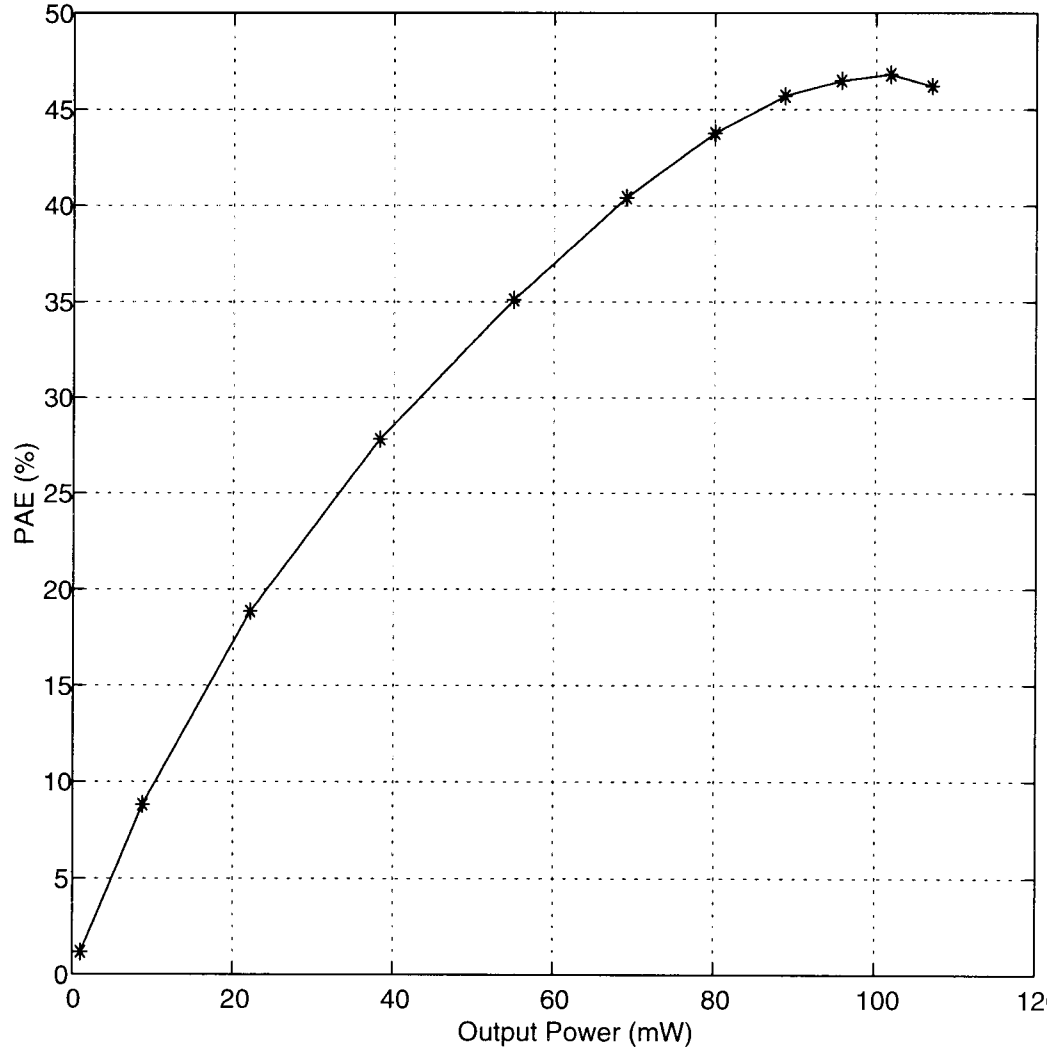

Figure 4.13 Simulated output power v/s PAE for the PA with input match, at 900MHz.

5. LAYOUT AND MEASUREMENT RESULTS

This chapter describes the layout of the two power-amplifier stages and some test inductors fabricated in the HP 0.6μm triple metal, n-well CMOS process, offered through the MOSIS service. In addition, results obtained from measurements are also described. While the results obtained from inductor measurements have been included in section 2.4, the calibration and measurement is described in more detail in this chapter, and some plots obtained from the network analyzer for S_{11} of test inductors are also included here. In addition, the measurement results from the two PA circuits described in chapter 4 are also included in this chapter.

5.1 Details of Layout of PA and Inductors

Figure 5.1 shows the die photo of the first PA described in chapter 4. The transistors are made up of stacked, 20μm wide fingers. The gate poly is contacted on both sides of the transistor in order to reduce the gate resistance [49]. The width of the stacked transistor strip was chosen in order to achieve a compromise between the gate resistance value and the area and perimeter parasitics of the transistors, and the total height of the transistor structure. If the distance between the first and the last gate fingers of the transistor is too large, there can be a significant phase shift in the gate signal as it travels along the stacked transistor's poly gate fingers, which is undesirable. Consequently, the transistor height should be chosen taking this effect into consideration. Linear capacitors, formed by polysilicon (top plate) and active (bottom plate) are used as coupling capacitors, and in the low-pass filter used in the feedback loop [50]. Resistors are implemented by using non-silicided poly. As is commonly done, the layout of resistors is in the form of long, snaking lines of poly. These resistors are used to couple the dc bias to the gate of transistors, in the low-pass filter used in the feedback loop, as well

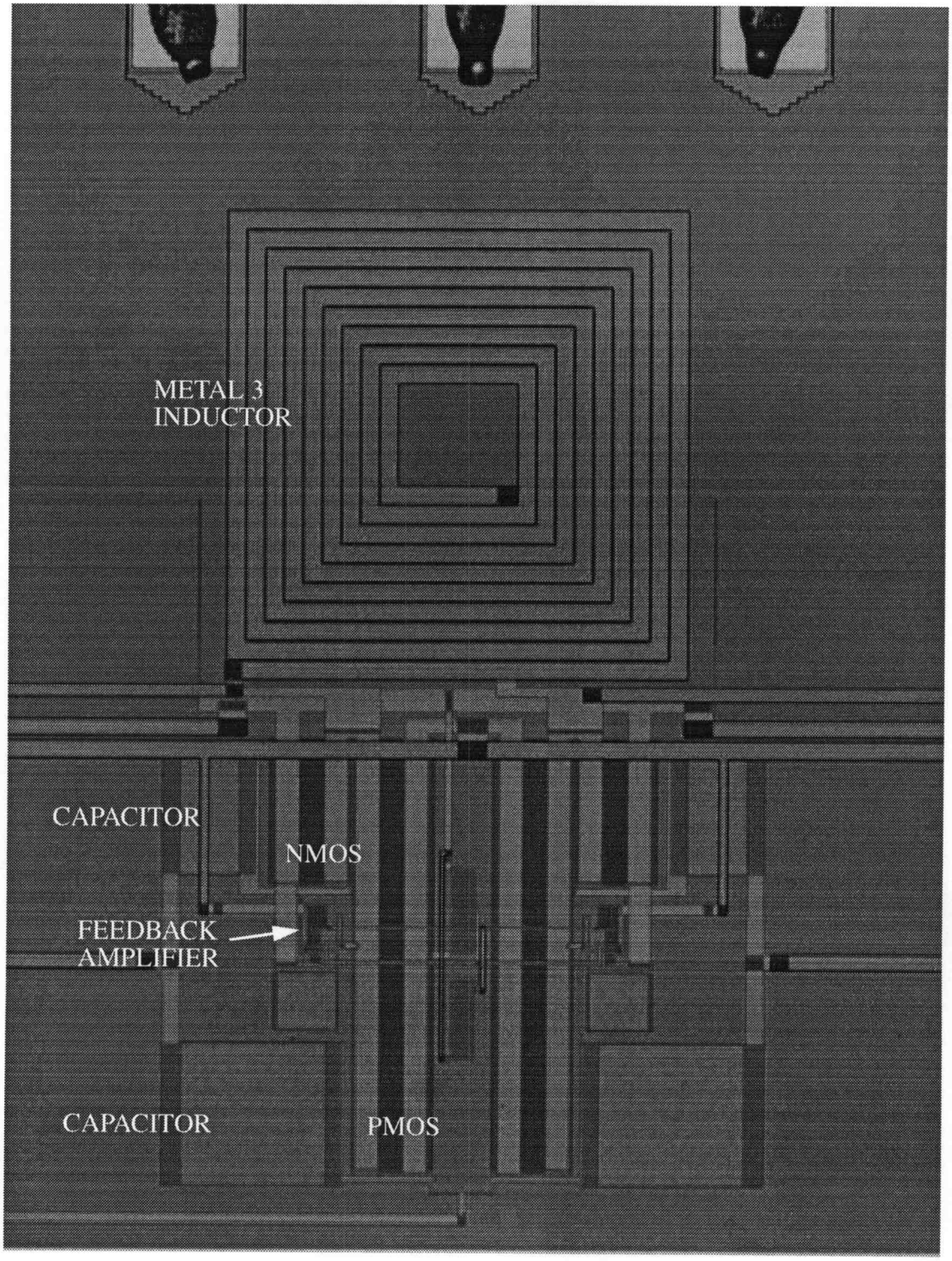

Figure 5.1 Die photo of part of the first chip showing the PA stage.

as to generate a reference voltage of one-half the supply voltage. The inductor used in the matching network has a geometry identical to that described in chapter 2, and is formed using the top metal layer of this triple-metal process. The pair of inductors for the two halves of the balanced PA are implemented as a single coil and not as two separate coils. As mentioned in chapter 2, this results in savings in the die area, as well as some reduction in the losses of this matching network. The bonding pads are 100μm by 100μm, and consist of metal3-metal2 structures with a ring of vias at the periphery, and outside the glass cut. This structure is a requirement for fabrication by MOSIS, and is chosen in order to prevent any metal lifting problems during the wire-bonding process. The complete layout of this chip is included in chapter 2. In the first chip that has been fabricated, the same bonding pads are also used as probe pads for two test inductors. The inductors are 5.25 turns and 7.25 turns, respectively, and also implemented using metal3. The inside port of the inductors is brought out by using a metal2 underpass, and connected to the ground probe pads. The probe pads are set up for ground-signal-ground probes with 250μm pitch. A set of open probe pads have also been included for calibration purposes. An effort has been made to have ground and power supply lines run close to each other, with the intent that the negative mutual coupling between them will reduce the net ground and power supply inductance. Multiple ground and power supply pads are provided in the layout.

The second PA described in chapter 4 is part of the second chip which has been fabricated. Figure 5.2 shows a plot of the layout of this PA. Some modifications have been made to the layout of the first PA stage, and an input matching network has been included in the design. The gate poly for the transistors is not contacted on both sides. Non-silicided poly resistors have been replaced by silicided poly resistors. In addition, the transistors and the other blocks have been rearranged. The probe pads used are distinct from bonding pads, in that they are formed by using metal3 only. The layout allows the use of ground-signal-ground pads with any pitch from 6mil to 10mil. A set of

four inductors are included in this chip, as well as an NMOS and PMOS transistor which may be used to obtain measurement based S-parameter models for the devices. Figure 5.3 shows a close-up of the transistor layout, Figure 5.4 shows a linear capacitor, Figure 5.5 shows a resistor, and Figure 5.6 shows the layout of an inductor.

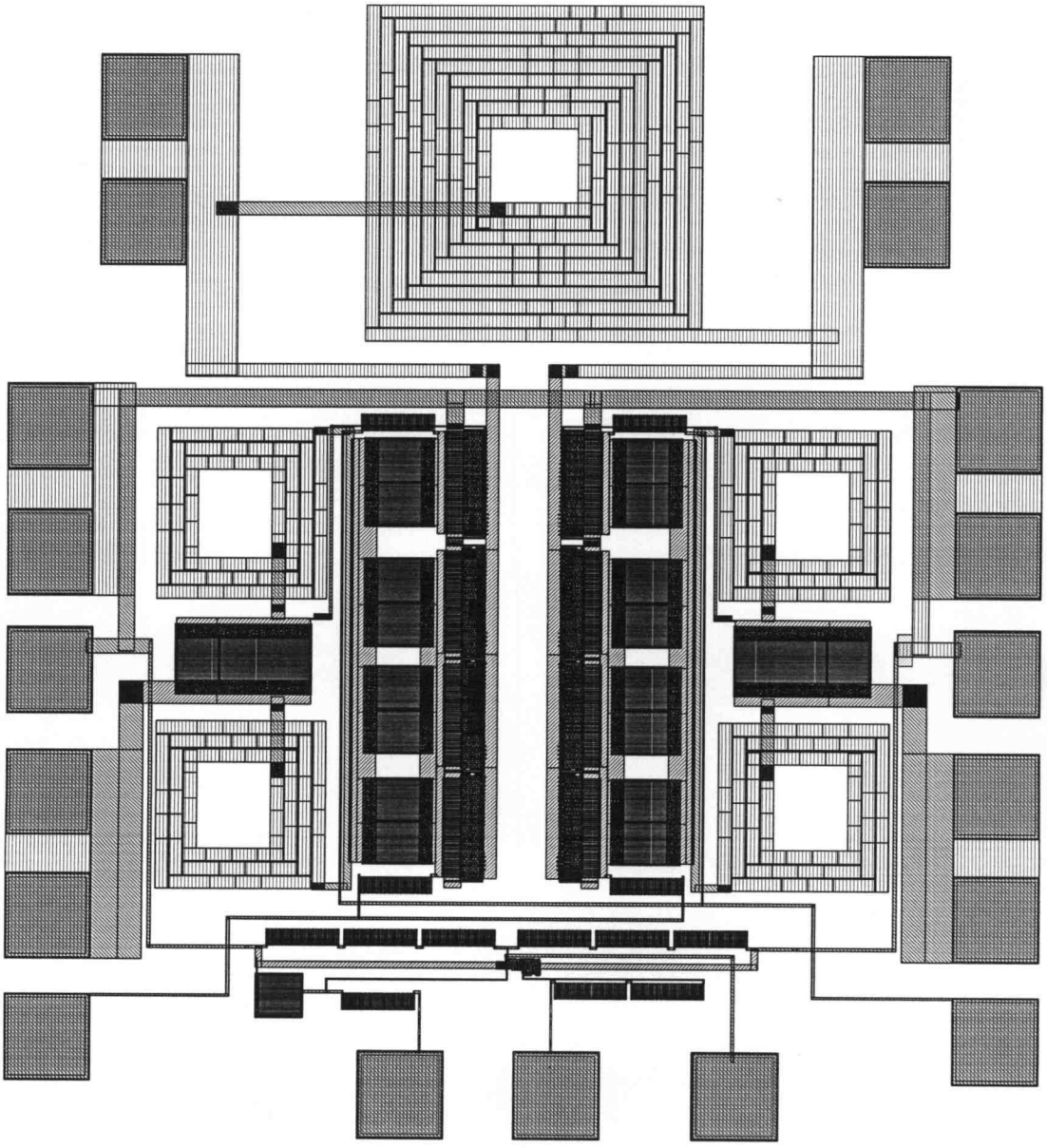

Figure 5.2 Layout of part of the second chip showing the PA stage.

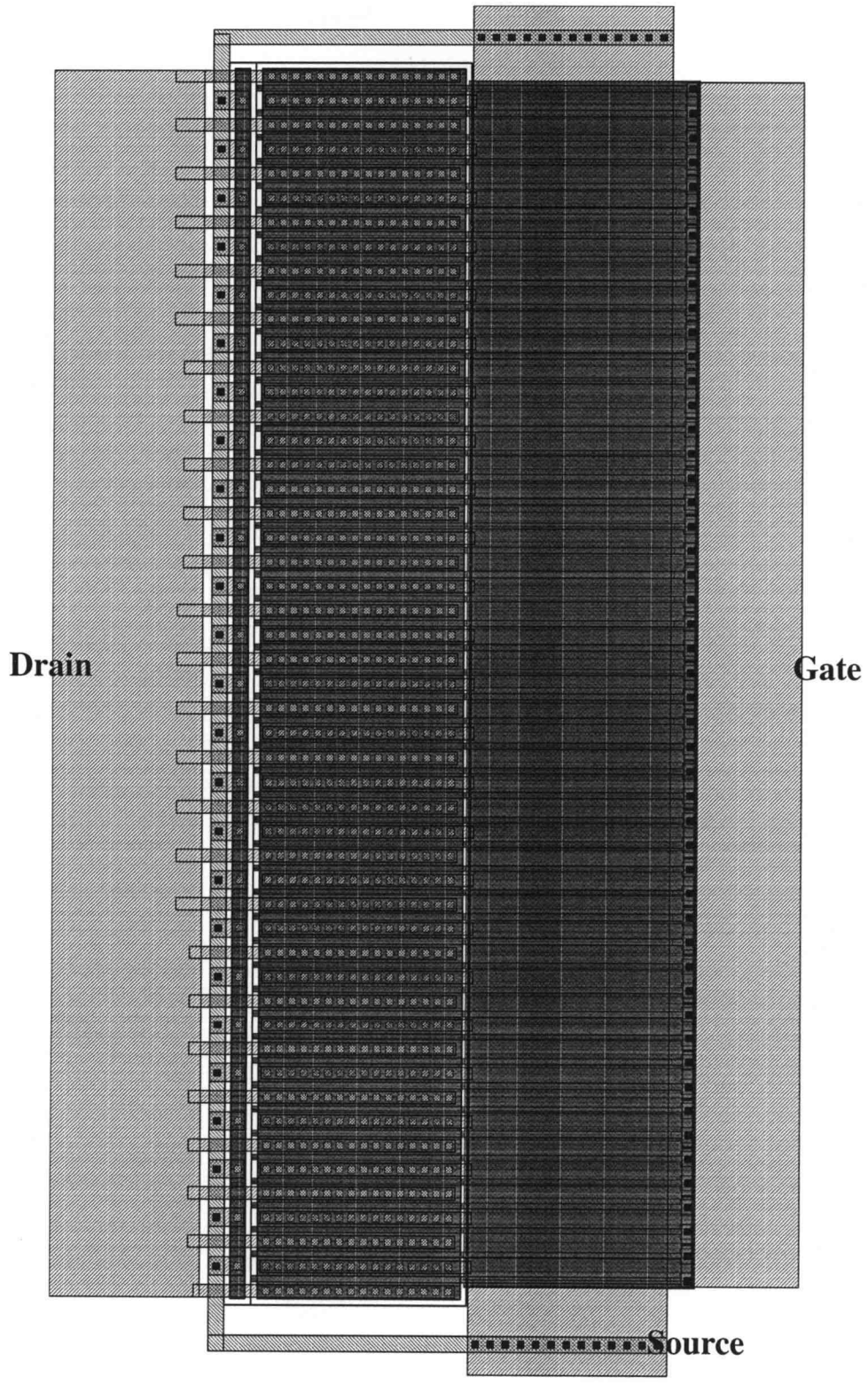

Figure 5.3 Layout of an NMOS power transistor used in the PA stage.

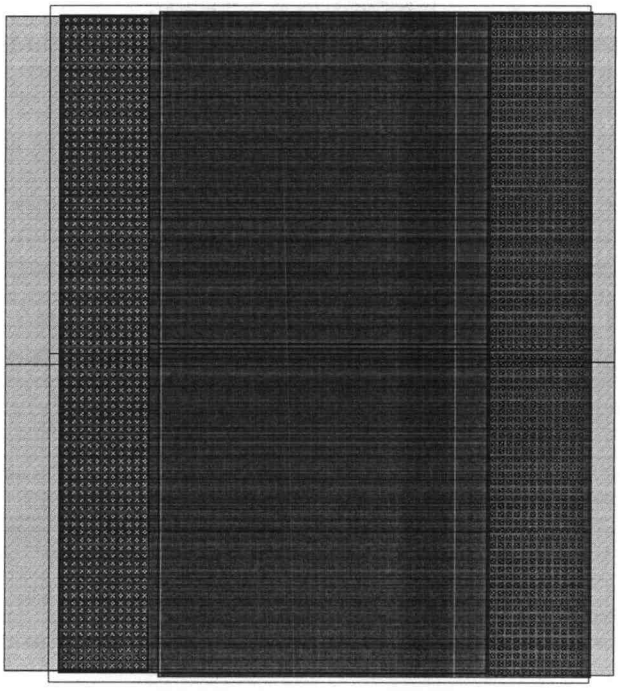

Figure 5.4 Layout of the linear capacitor used in the PA.

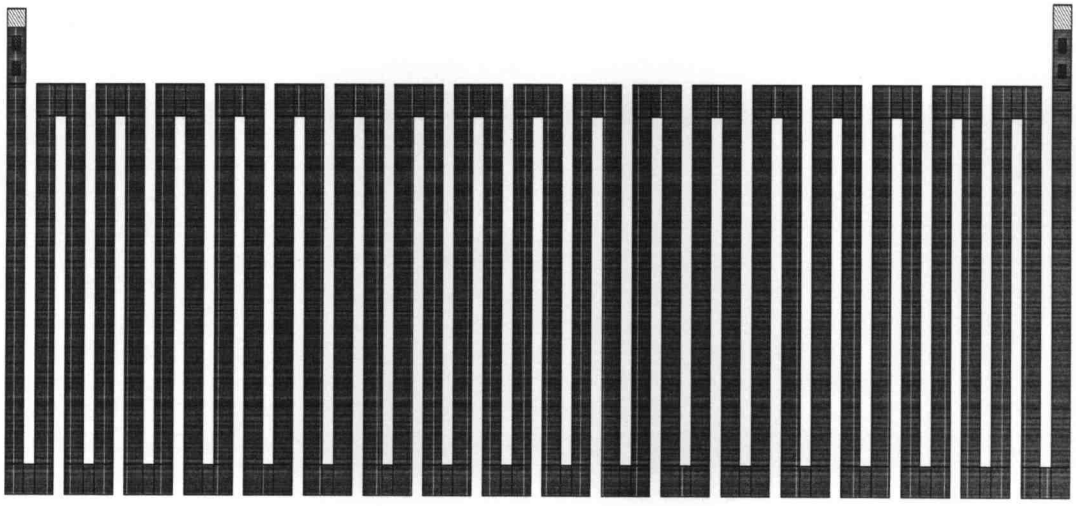

Figure 5.5 Layout of a 1KΩ polysilicon resistor.

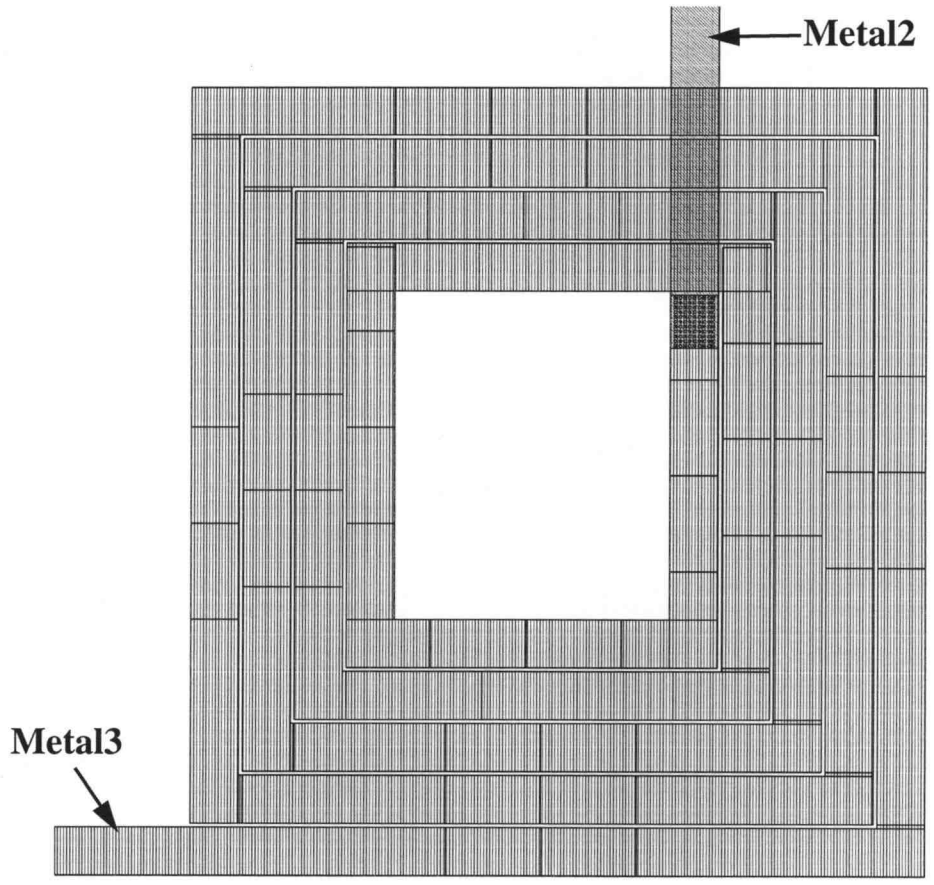

Figure 5.6 Layout of an inductor used in the matching network for the PA.

5.2 Measurement Results

The first chip that has been fabricated, including a PA and two test inductors, and has been completely characterized at this stage. As described in chapter 2, a set of one-port S-parameter measurements were performed for two integrated inductors. The measured S_{11} was converted to the impedance of the inductor structures, for the frequency range from 30KHz to 6GHz. S_{11} is related to the impedance for a one-port network, Z_{in}, according to the following equation

$$S_{11} = \frac{Z_{in} - Z_o}{Z_{in} + Z_o} \tag{5.1}$$

where Z_0 equals 50Ω for the measurement system used. In addition, S_{11} was also measured for a set of open probe pads. Cascade Microtech probes were used to perform these measurements. These probes were calibrated using the available impedance substrate standard for a 10mil pitch probe. Therefore, while the probes were calibrated upto the tip of the probes, the probe pads were still part of the measurement. The S_{11} data for the set of open probe pads was used to calibrate out the effect of probe pads on the inductor structures as outlined in [51], and summarized here. The S-parameter data for the open probe pads is converted to Y-parameter data and stored. The S-parameter of the inductor and the probe pads is also converted to Y-parameter, and the probe pad Y-parameter subtracted from this data to obtain the Y-parameter of the inductor by itself. Figures 5.7 and 5.8 show the measured S-parameter plots for the two inductor structures, as available from the network analyzer, respectively. As is a common practice, the Smith chart is used to represent the inductor measurement data. Note that the effect of the probe-pads has not been calibrated out from these plots. This data was stored on a computer disk as a text file and the probe-pad calibration was performed as part of the post-processing of the measured data, using the procedure outlined above.

A test board was fabricated using gold-plated FR4 for testing the PA. The die was directly mounted and wire-bonded to the test board. Four bond wires were used for the ground and power supply, and two for all the other RF signals. Figure 5.9 shows the schematic of the test setup used for the PA. RF input power was fed to the PA stage through a transformer used to convert single-ended signal from the RF signal generator (HP8657B) to a differential signal required by the PA. The transformer was mounted on the test board. Minicircuits TC 1-15 transformer, with an insertion loss of 1dB, was used as the balun, or a balanced-unbalanced transformer. Similarly, at the output also,

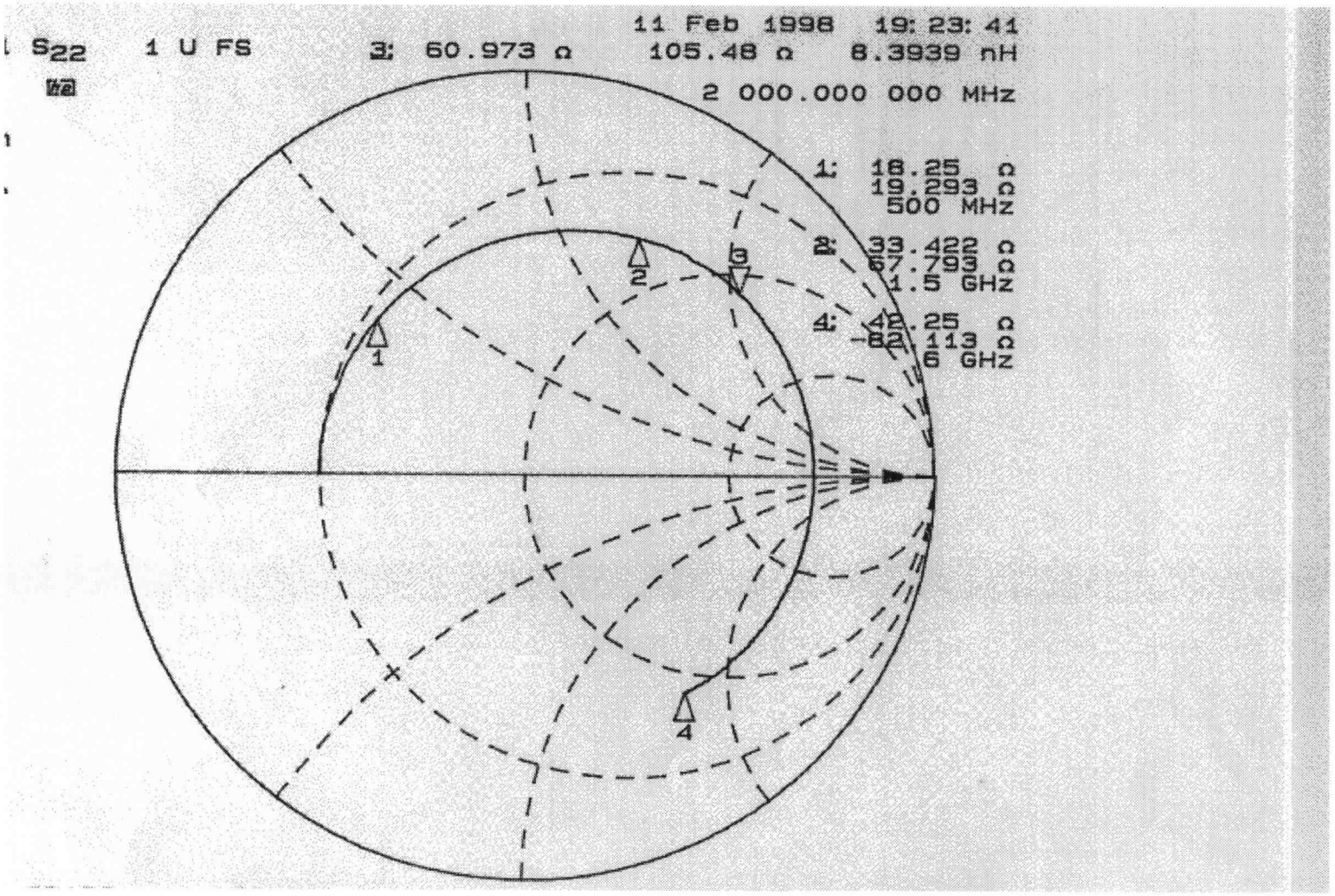

Figure 5.7 Measured S11 for the 5.25 turn inductor, shown on a Smith chart.

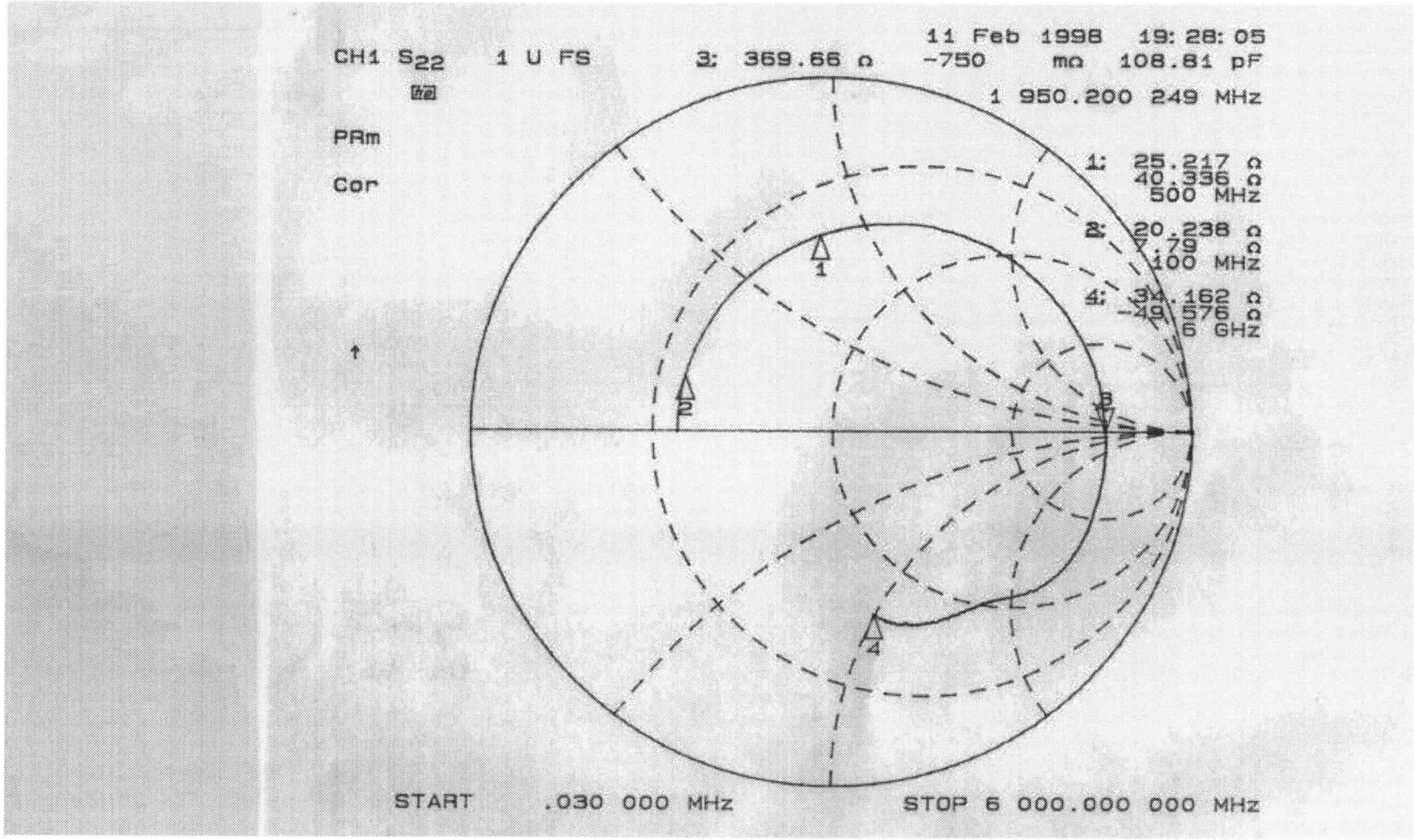

Figure 5.8 Measured S11 for the 7.25 turn inductor, shown on a Smith chart.

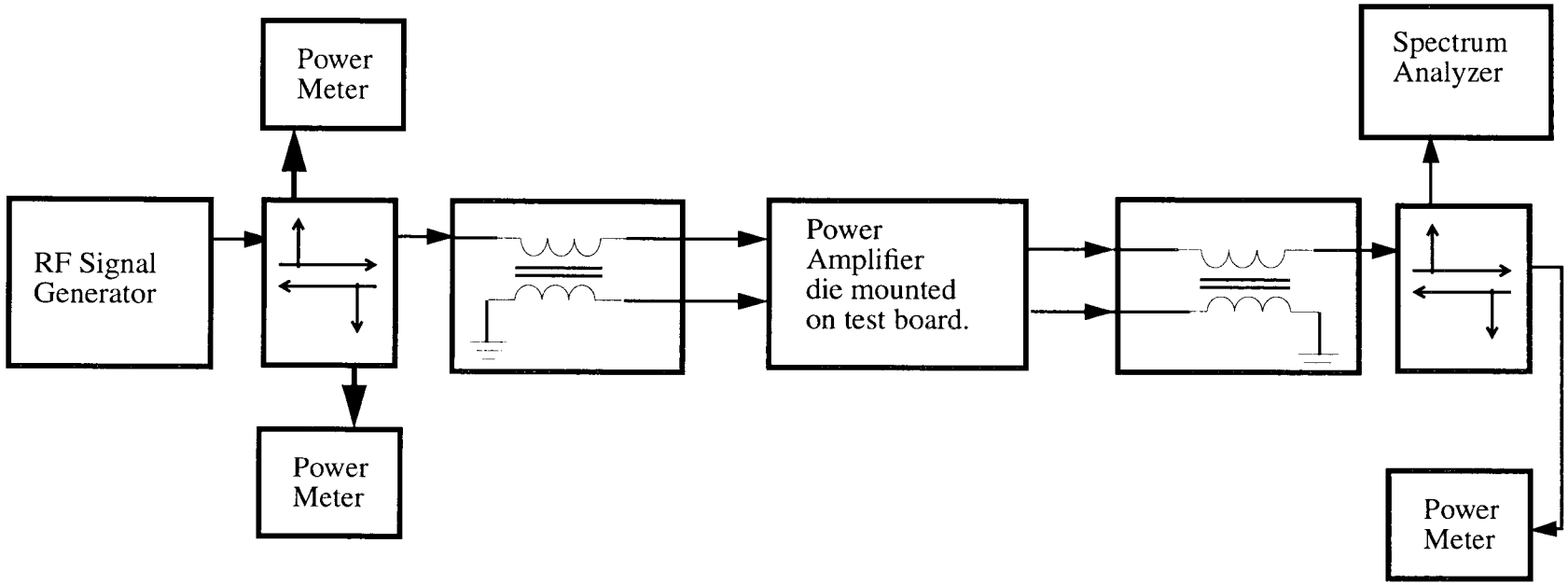

Figure 5.9 Schematic of the test setup for the Power Amplifier.

another one of these transformers was used as a balun to convert the differential output signal into a single-ended signal which was measured using a Boonton power meter. A pair of bi-directional couplers were used at the input and output. The coupler at the input allowed an estimate of the input power required by the PA, and that at the output allowed the output signal to be connected to a Tektronix spectrum analyzer. The spectrum analyzer was used to obtain data on harmonics, as well as to ensure that the PA was stable. The entire setup was calibrated for a representative set of frequencies over the frequency range of 800MHz to 990MHz. In testing this PA, it was found that the feedback loop, used to bias the NMOS power transistor, was not functioning. It is estimated that this was due to improper fabrication of some of the non-silicided poly resistors, especially the resistor which is part of the low pass filter in the feedback loop, due to the absence of silicide blocking in the fabrication of these resistors (it is for this reason that the second PA which has been fabricated does not use silicide blocking over poly to form resistors). As a result, measurements were performed on the PMOS half of the PA, along with the integrated matching network. The results were then extrapolated assuming the NMOS power device has the same transconductance as the PMOS device. Figure 5.10 shows the output power and efficiency as a function of frequency for this case. Measurements were performed on three different PAs, and the results obtained were similar. The change in efficiency among the three different PAs was less than 2%, and that in output power less than 5%. The results shown in Figure 5.9 represent the best case results of the three sets of measurements. The PA was also found to be stable into an open circuit.

The second PA, with integrated input and output matching networks, has also been characterized. As with the first PA test chip, in this case also the PA die was directly mounted on to a gold-plated FR4 test board, and a test setup identical to that represented in Figure 5.9 was used to obtain data regarding the efficiency, power gain, and bandwidth of the amplifier. From two-port S-parameter measurements, at 900MHz,

the input return loss of the amplifier is 6.15dB, the output return loss is -17.9dB, and reverse isolation is -25.6dB. While this indicates that the output is well matched to 50Ω, the input matching is not as accurate (even though the PA was optimized for maximum efficiency and not the best input match, the simulated input return loss was 9.8dB at 900MHz). This is attributed primarily to the inaccuracy of the available device models in predicting the input impedances of the PMOS and NMOS transistors.

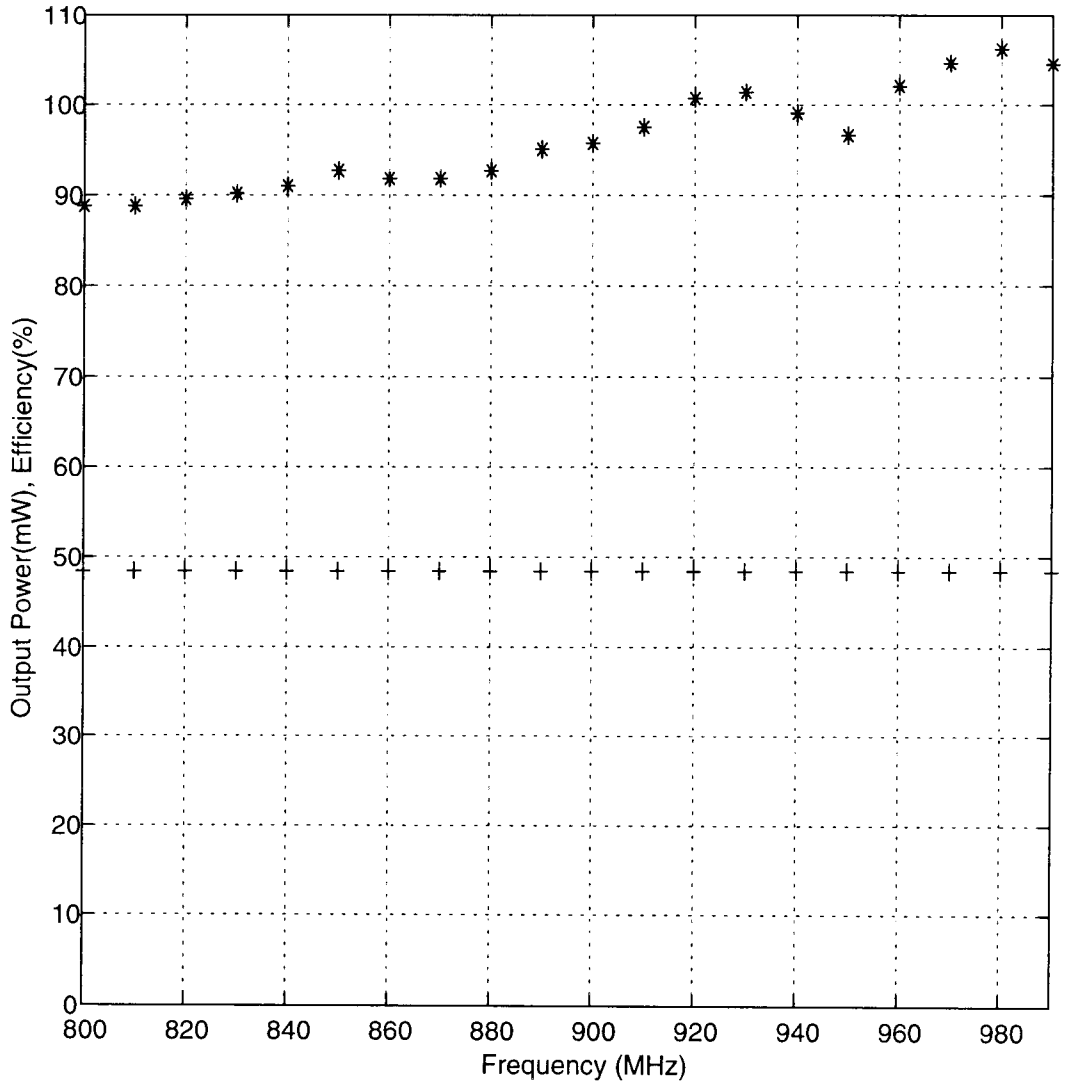

Figure 5.10 Measured output power (*) and efficiency(+) for the first power amplifier.

Figure 5.11 shows the output power v/s the input power for the PA, at 900MHz. As can be seen from the plot, the power gain is only 5dB, whereas the simulations indicate a power gain of 10dB. This discrepancy is attributed primarily due to the inaccuracy of device models. The models used in this work have been generated from ring-oscillator data, and are not verified for accuracy at RF frequencies. It is estimated that the results for power gain and input impedance, as obtained from these models, are not accurate. Note that the input matching network has a significant impact on the power gain also, as mentioned in section 4.3.2.

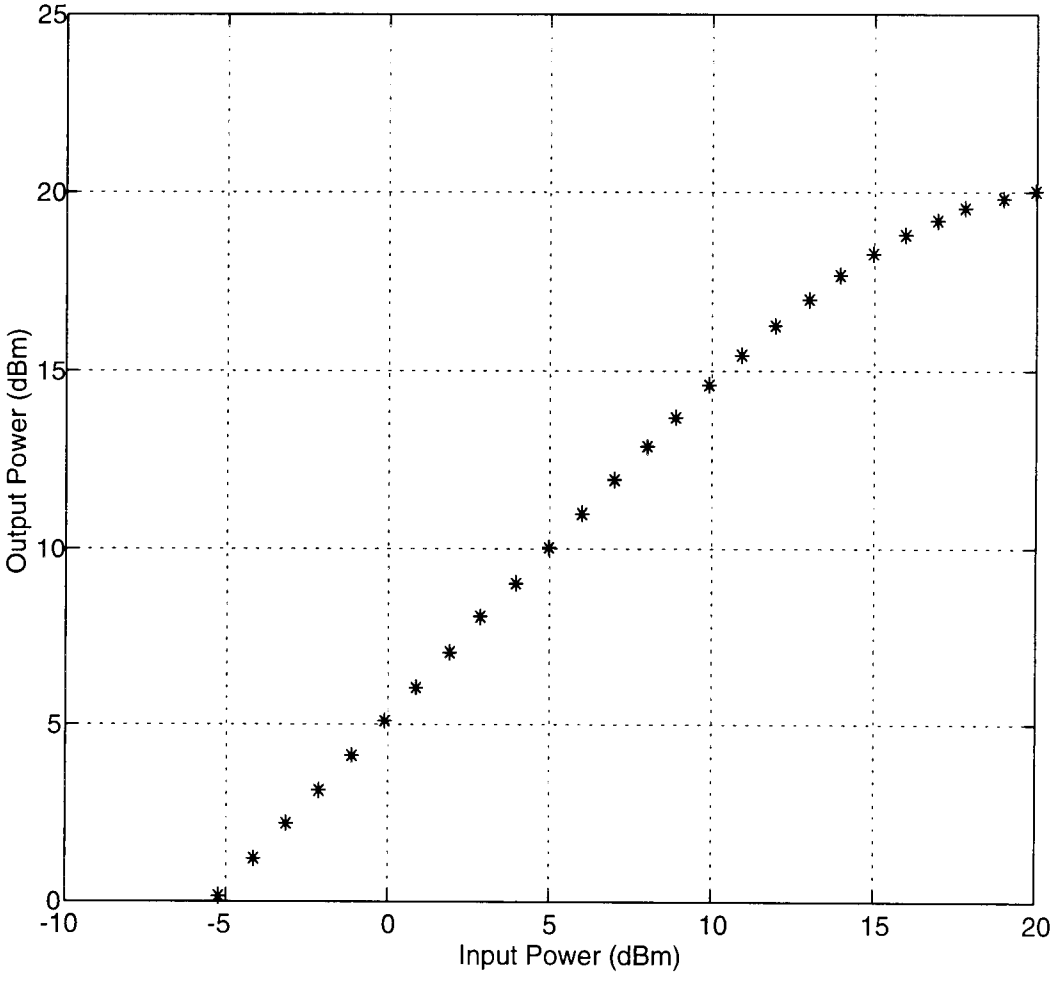

Figure 5.11 Measured input power v/s output power characteristic for the amplifier, at 900MHz.

Figure 5.12 is a plot of the PAE of this amplifier. The low gain adversely impacts the PAE also.

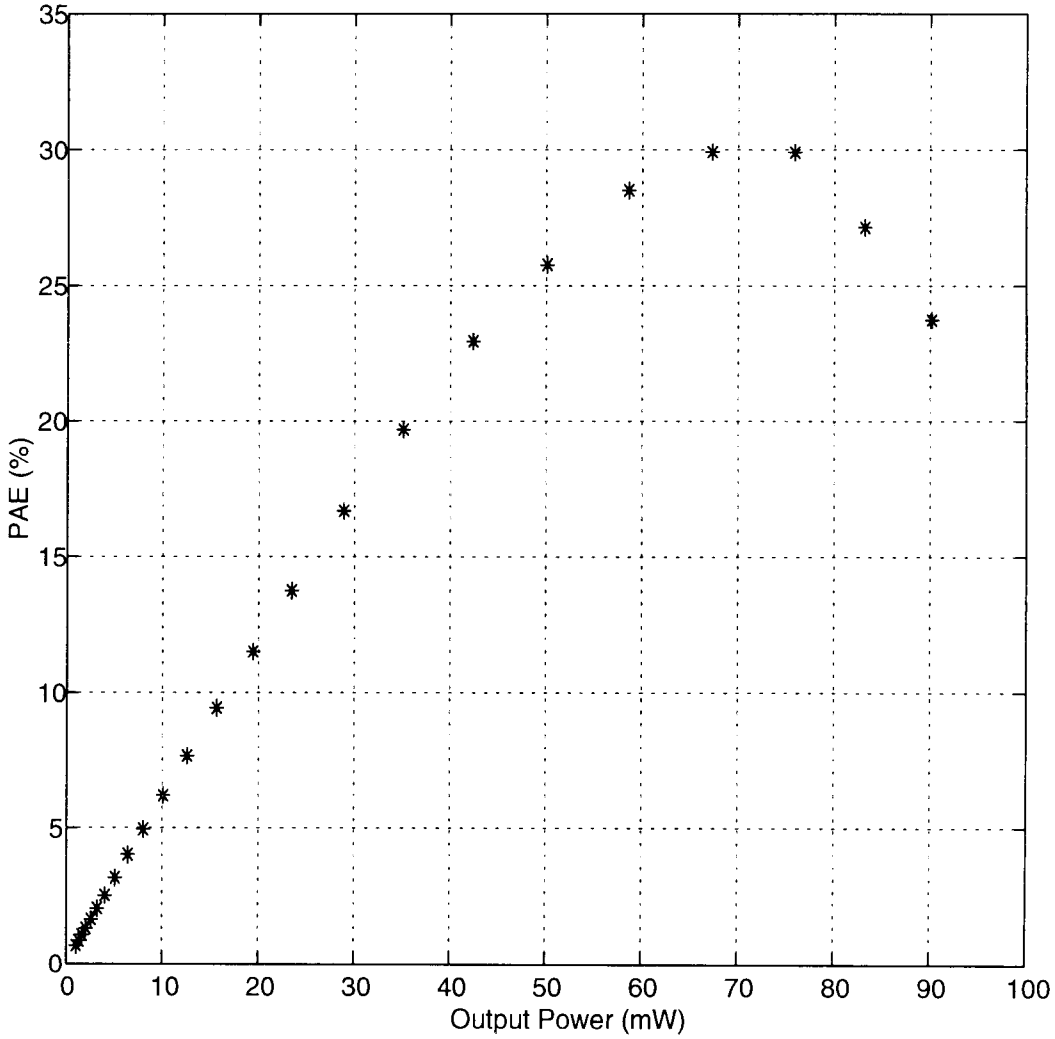

Figure 5.12 Measured PAE v/s output power for the amplifier, at 900MHz.

Figure 5.13 shows the drain efficiency of the amplifier over a frequency range of 800MHz to 1GHz. As can be seen from this figure, the amplifier has a drain efficiency of 55% at 900MHz. This efficiency is obtained while supplying 85mW output power, and the PAE at this power level is 27%.

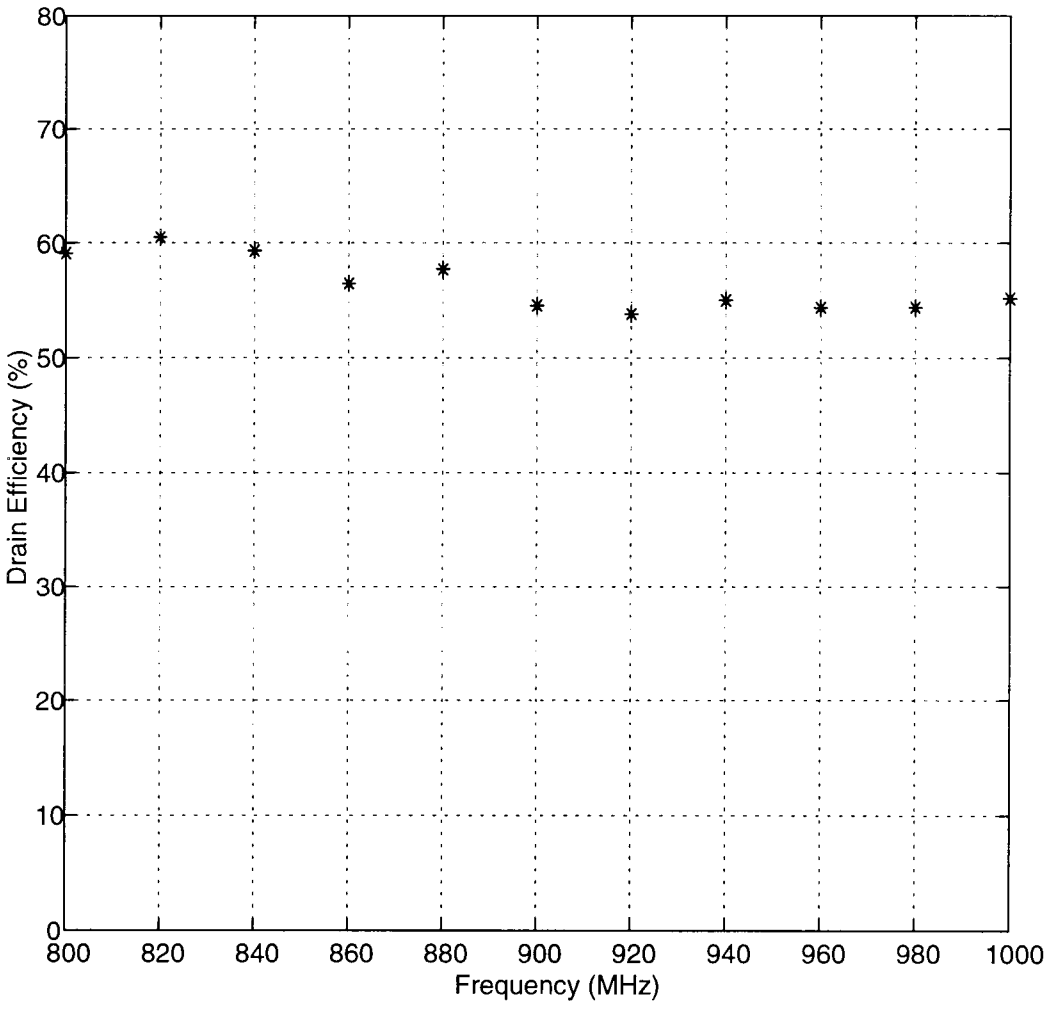

Figure 5.13 Measured drain efficiency v/s frequency for the amplifier.

Figure 5.14 shows the output power available from the amplifier over a frequency range of 800MHz to 1GHz. The low-Q nature of the response of the amplifier is evident from this plot. Note that even though the amplifier is able to supply upto 100mW, the PAE at this output power level is very low. As a result, operation at this output power level is not very useful. Consequently, the amplifier has been characterized for efficiency at an output power level of 85mW, which corresponds to a PAE of 27% and a drain efficiency of 55% at 900MHz.

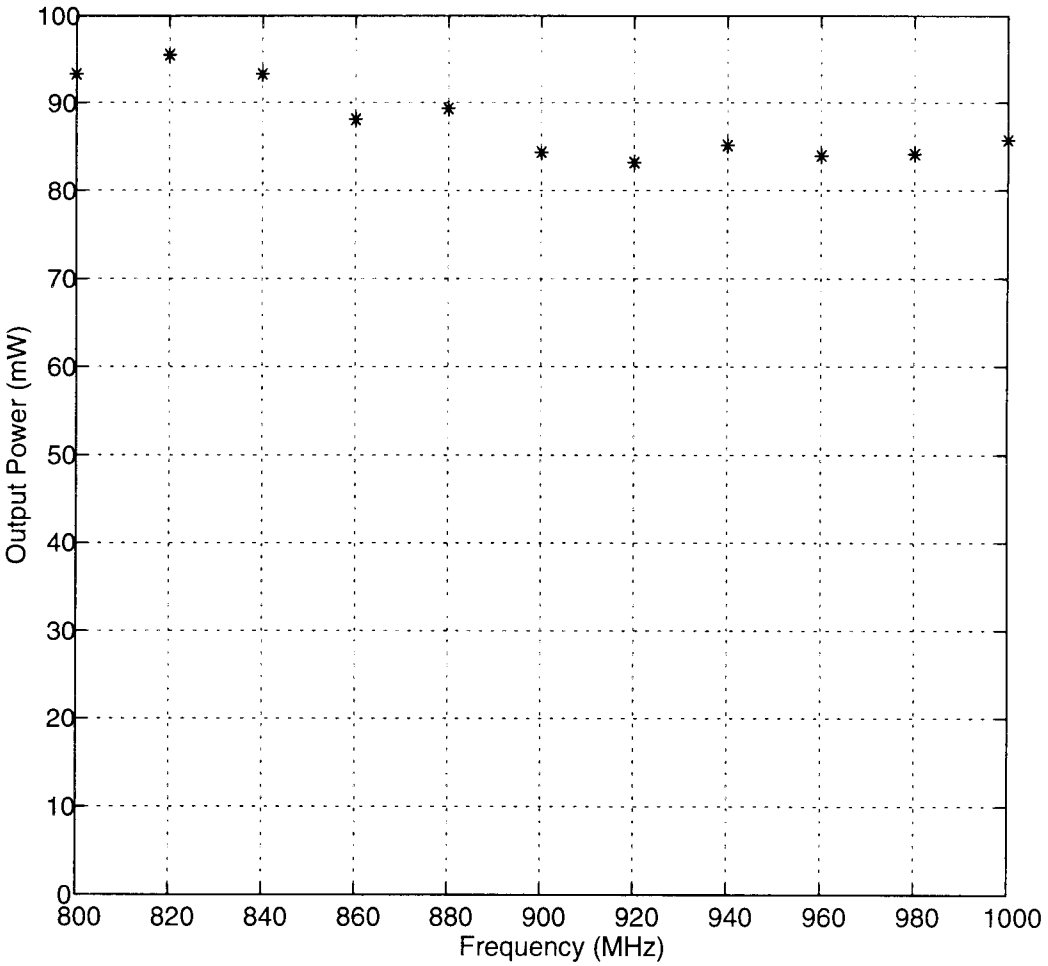

Figure 5.14 Measured output power v/s frequency for the amplifier.

6. CONCLUSIONS AND FUTURE WORK

This chapter lists some of the conclusions which have been inferred from the various parts of this work for the design of CMOS RF integrated circuits, as well as discusses some of the possibilities which this work opens up regarding implementation of CMOS RF PAs for wireless applications.

6.1 Conclusions

Based on the inductor model outlined in chapter 2, it can be inferred that the geometry of the inductor plays a significant role in determining its electrical characteristics, and significant benefits may be gained by using an optimum geometry. For example, reducing the spacing between the turns of the inductor results in higher mutual inductive coupling, but it also increases the capacitive coupling between turns. However, the effect of capacitive coupling is insignificant upto a few GHz, and the increased mutual inductance results in higher inductance for a given die area. For example, a 9.25 turn, 6.2nH inductor in a digital CMOS process is reported in [52]. It is formed by stacking metal1-metal2-metal3 layers of 5.2μm width and with 2μm spacing between turns. It occupies 145 x 145 μm^2, and, *based on two-port measurements*, has a self-resonant frequency of 3.8GHz and a peak Q-factor of 2.5 In contrast, the 5.25 turn, 6.2nH inductor reported in this work has a a measured peak Q-factor of 2.35, and a self-resonant frequency of 3.99GHz with one port grounded, and of 6.82 GHz with both ports floating. It occupies 264 x 264 μm^2. The increase in self-resonance frequency is due to the metal3 capacitive coupling to substrate being much smaller than metal1 coupling.

However, it can be observed that by optimizing the geometry of the inductor, a peak Q-factor is obtained which is only 6% smaller than a stacked inductor structure.

While skin effect results in an increase in the ac resistance of metal segments, the increase is even more pronounced for the inner turns of the inductor [53]. The magnetic flux density linking the inner coils of a spiral inductor is higher than that linking the outer coils. As a result, the eddy current induced magnetic field, which opposes the magnetic flux of the inductor, is strongest for the inner turns of the inductor. The reduced net flux results in reduced inductance for the inner turns. Further, eddy currents distort the current distribution in the metal segments, resulting in a non-uniform flow of current. This effect is most severe for the inner turns of the inductor, where eddy currents are strongest. As a result, the increase in ac resistance, caused by non-uniform current density in the inductor segments, is most severe in the inner segments. The reduced contribution to the total inductance of the coil combined with the increased contribution to the ac resistance of the inductor make the use of innermost turns in an inductor coil counterproductive.

The modeling approach adopted here can also be used to design mutually coupled inductors. For example, bridge T-coil networks can be implemented using coupled inductors. This network may be used for input impedance matching networks [48] for MOS devices. However, an accurate CAD model for mutually coupled inductors requires modeling of the coupling between such inductors which occurs through the substrate as well. The parasitic coupling between mutually-coupled inductors has not been addressed as part of this work. It is likely that coupling parasitics have a major impact on the performance of integrated coupled inductors, and a true measure of the

benefits gained by using coupled inductors can be obtained only by taking into account parasitic coupling effects.

In chapter 3, a procedure was outlined for designing a Class A, B or C power amplifier. The trade-offs between efficiency, output power and distortion for these amplifiers were explained by means of simple equations derived for these power amplifiers. While Class C amplifiers have higher efficiency than Class A or B PAs, they also exhibit higher harmonic distortion and reduced output power for a given device size. It was demonstrated by means of a design example that package, device and inductor parasitics have a significant impact on the overall performance of integrated PAs. In order to realize efficient fully integrated power amplifiers in a low-cost technology like standard CMOS, it is essential to incorporate the effects of parasitics into the design process. It was shown that significant improvement in RF circuit performance results by optimization of the design in the presence of parasitics associated with the active and passive elements. The design equations given in this chapter for PAs only serve as a starting point in the design, with the final design being arrived at by optimizing the initial design to include the effects of both active and passive element parasitics.

In chapter 4, a CAD tool was described which has been developed to aid in the design of RF circuits in the presence of high loss passives. It was shown that the simulated annealing heuristic is well-suited for the optimization of RF circuits. The Perl code for this CAD tool is included in Appendix III. This CAD tool enables incorporation of device, passive element (inductors, capacitors) and package parasitics into the design and optimization process of fully-integrated power amplifiers. Two power amplifiers were designed and optimized using this CAD tool. Measurement results from the first of these circuits validates the design and optimization procedure outlined in this work.

While the CAD tool developed here has been used to directly optimize PA efficiency, the same approach can be used in the design of fully-integrated linear power amplifiers, low-noise amplifiers, mixers and other RF building blocks. The availability of simple models for the various circuit elements is critical to the advancement of CAD for RF circuit design. Towards that end, a simple inductor model is developed and included in the CAD optimization process. It is proposed that with the availability of improved package and device models, it is possible to eliminate the tuning of RF circuits completely. Rather, tuned RF circuits may be replaced by robust, fully-integrated implementations which have been optimized for performance in the presence of parasitics significant at RF frequencies [54]-[55]. The power amplifier designs included in chapter 4 highlight this design approach. The CAD tool presented in that chapter is an effort towards realizing successful package-chip co-synthesis techniques. This work has demonstrated the feasibility of implementing *fully integrated* CMOS RF PAs with output power in the range of 100mW, which may be incorporated into a single-chip transceiver for certain wireless applications.

6.2 Future Work

During the course of this work, several possible approaches presented themselves which would complement the design approach of this work. These options were not necessarily vigorously pursued due to various reasons. Some of these possibilities are outlined in this section as possible future work. The approach for modeling of inductors has been limited to planar spiral structures. It would be interesting to extend this approach to the modeling of monolithic transformers, as discussed in chapter 2, in

order to obtain an accurate estimate of the benefits that can be realized in differential RF circuits by replacing inductors with transformers. The inductor modeling approach followed here does predict the coupling between the transformer turns. However, the estimate of substrate loss for transformers is an issue which has not been addressed. Further, analytical estimation of substrate loss for inductors and transformers fabricated on silicon is also desirous. A first step in this direction may be to estimate the inductive coupling between the inductor and the substrate, and use this to predict a value for the inductive substrate loss resistance. The technique of active compensation of inductors, which involves the use of a negative resistance to compensate for the inductor series resistance and allows realization of high-Q inductors without any process modifications, has not been pursued in this work. However, this may perhaps be a worthwhile approach to the design of integrated CMOS power amplifiers with power output in the range of 1W or higher.

This work has dealt with the implementation of saturated power amplifiers which have been optimized for efficiency. The design of linear power amplifiers has not been performed using this approach. The CAD tool developed here may be used to design and implement power amplifiers optimized for linearity, rather than efficiency. Alternatively, several approaches have recently appeared in literature which allow the use of non-linear power amplifiers in applications requiring linear power amplifiers [56]-[58]. Design of matching networks is even more critical in some of the non-linear power amplifiers like Class-E and Class-F power amplifiers. The transistor in these power amplifiers acts as a switch. It would be interesting to estimate the switching capabilities of transistors fabricated in state-of the-art CMOS processes of today, and to examine the viability of implementing *integrated* Class-E and Class-F power amplifiers for operation at 900MHz, 1.8GHz, or 2.4GHz. Further, the CAD tool developed here could be used to design the matching networks which are critical to the working of this class of power amplifiers.

While this work has addressed the design of power amplifiers only, the design of matching networks is critical to the performance of other RF circuits. An example is the design of low-noise amplifiers. The noise figure of LNAs is critically affected by the design of the input matching network, which is designed in order to achieve a compromise between the input return loss and the noise figure and sensitivity of the receiver. It is likely that the same CAD approach outlined here would be very effective in the realization of fully-integrated CMOS RF low-noise amplifiers. While several integrated versions of LNAs have appeared in literature, it is not apparent that the designs using inductors have been optimized for noise and input matching performance. If the improvement in performance obtained for the power amplifiers designed in this work is any indication, there is significant room for improvement in the design of other integrated RF circuits as well. As an example, the simulated-annealing based CAD tool has been modified and used in the design and optimization of a fully-integrated CMOS distributed amplifier also with great success [59].

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APPENDICES

APPENDIX I. CODE FOR GENERATING π-4 QPSK AND GMSK WAVEFORMS

Note: This code has been succesfully executed on MATLAB 5.1, running on a HP Model 712/80 workstation.

```
% simulating the pi/4-qpsk signal/channel
n=100;      % no of input samples
p=1;        % power in input signal
fb=960;     % bit rate
fc=5e3;     % carrier frequency
alpha=0.4*fb/2;  % alpha for raised cos roll-off filter
gain=1.0; %20/fb;  % factor in the raised cos filter
fs=48.001e3;    % sampling frequency
fs1=fs;     % baseband sampling frequency
%generating the even and odd bit stream
rand('seed',0);
for k=1:n,
 b(k)=rand;
 if b(k) >= 0.5
   b(k)=10.0;
 else
   b(k)=-10.0;
 end;
end;
k=1;
theta(1)=0;
for m=1:2:n,
```

```
k=k+1;
if b(m)==10.0
 if b(m+1)==10.0
  phi(k)=pi/4;   % symbol sequence 1 1
 else
  phi(k)=-pi/4;  % symbol sequence 1 -1
 end;
else
 if b(m+1)==10.0;
  phi(k)=3*pi/4;   % symbol sequence -1 1
 else
  phi(k)=-3*pi/4;  % symbol sequence -1 -1
 end;
end;
theta(k)=theta(k-1)+phi(k);
be2(k-1)=10.0*cos(theta(k));
bo2(k-1)=10.0*sin(theta(k));
end;
for j=1:n/2,
be(2*j-1)=be2(j);
be(2*j)=be2(j);
bo(2*j-1)=bo2(j);
bo(2*j)=bo2(j);
end;
m=round(fs1/fb);
%passing it thru a pulse shaping filter - first sample it at frequency of fs1
bo_s1(1:50)=zeros(1,50);
```

```
for k=1:n
 for l=1:m,
   aind=m*(k-1)+l;
   bo_s2(aind)=bo(k);
   be_s2(aind)=be(k);
 end;
end;
bo_s1=zeros(size(1:max(size(bo_s2))));
be_s1=zeros(size(1:max(size(be_s2))));
for k=1:n/2,
 bo_s1(1+100*(k-1))=bo_s2(1+100*(k-1));
 be_s1(1+100*(k-1))=be_s2(1+100*(k-1));
end;
 %now convolve the input with the impulse response
imp(1)=1;
for j=2:600,
 k=j-1;
 h1(j)=cos(2*pi*alpha*k/fs)/(1-(4*alpha*k/fs)^2);
 h2(j)=sin(pi*fb*k/fs/2)/(pi*fb*k/fs/2);
 imp(j) = h1(j)*h2(j);
end;
h(600)=gain*imp(1);
for k=1:599,
 h(600+k) = gain*imp(k);
 h(600-k)=h(600+k);
end;
bolpf=filter(h,1,bo_s1);
```

```
belpf=filter(h,1,be_s1);
% output is bolpf and belpf-upconvert it
for k=1:max(size(belpf)),
 so(k)=-sqrt(p)*bolpf(k)*sin(2*pi*fc*k/fs);
 se(k)=sqrt(p)*belpf(k)*cos(2*pi*fc*k/fs);
 st(k)=se(k)+so(k);
end;
%adding the PA
pa_gain=3.1623; % 10dB voltage gain
for j=1:max(size(st)),
 paop(j)=pa_gain*st(j);
 if paop(j)>10.0
  paop(j)=10.0;
 end;
 if paop(j)<-10.0
  paop(j)=-10.0;
 end;
end;
blak=hanning(4096);
vb=blak'.*st(1:4096);
V=fft(vb,4096);
Pvv = V.*conj(V)/(4096^2);
Pdb=10.0*log10(Pvv);
af=(0:4095);
% Simulating the msk modulated channel
n=100;       % no of input samples
p=1;         % power in input signal
```

```
fb=960;      % bit rate
fc=5e3;      % carrier frequency
alpha=0.01;    % for Gaussian filter
gain=1;
fs=48.001e3;     % sampling frequency
fs1=fs; %4*fb;   % baseband sampling frequency
m=round(fs1/fb);
%generating the even and odd bit stream
rand('seed',0);
for k=1:n,
 b(k)=rand;
 if b(k) >= 0.5
   b(k)=10.0;
 else
   b(k)=-10.0;
 end;
 if rem(k,2)==1,
  bo(k)=b(k);
  bo(k+1)=bo(k);
 else
  be(k)=b(k);
  be(k-1)=be(k);
 end;
end;
for k=1:50,
 bo_s1(k)=0;
end;
```

```
for k=1:n
 for l=1:m,
   bo_s(50+m*(k-1)+l)=bo(k);
   be_s(m*(k-1)+l)=be(k);
 end;
end;
 %%%now pass thru a gaussian filter
 imp(1)=sqrt(pi)/alpha;
for j=2:600,
 k=j-1;
 imp(j) = sqrt(pi)*exp(-1*(pi*k*fb/fs/alpha)^2)/alpha;
end;
h(600)=gain*imp(1);
for k=1:599,
 h(600+k) = gain*imp(k);
 h(600-k)=h(600+k);
end;
bo_s1=filter(h,1,bo_s);
be_s1=filter(h,1,be_s);
%%%now generating x and y
for k=1:n*fs/fb
  x2(k)=cos(2*pi*k*(fc+fb/4)/fs);
  y2(k)=cos(2*pi*k*(fc-fb/4)/fs);
end;
x=0.5*(x2+y2);
y=0.5*(x2-y2);
%%now generating modulated signal
```

```
si=x.*bo_s1(1:5000);
sq=y.*be_s1;
st2=si+sq;
st=10*st2/max(st2);
%adding the PA
pa_gain=3.1623; % 10dB voltage gain
for j=1:max(size(st)),
 paop(j)=pa_gain*st(j);
 if paop(j)>10.0
   paop(j)=10.0;
 end;
 if paop(j)<-10.0
   paop(j)=-10.0;
 end;
end;

blak=hanning(4096);
vb=blak'.*st(1:4096);
V=fft(vb,4096);
Pvv = V.*conj(V)/(4096^2);
Pdb=10.0*log10(Pvv);
af=(0:2047);
plot(af,Pdb(1:2048));
```

APPENDIX II. CALCULATION OF THE INDUCTANCE OF A PLANAR SPIRAL COIL

Note: This code has been succesfully executed on MATLAB 5.1, running on a HP Model 712/80 workstation.

```
% calculating the nominal inductance of a square spiral
clear;
z=21; % # of segments
l=zeros(1,z);   % vector for lengths of all the segments
ind=l;   % vector for self inductance of all segments
total = 0;   % total self inductance, in nH, of all the segments
k=1;   % used as a flag while determining segment lengths
n=(z-9)/4;
w=15e-6;   % width of the conductor
t=1e-6;   % thickness of conductor
s=1.2e-6;   % edge to edge spacing between conductors
not=fix(z/4);   % # of complete turns
mpos=zeros(1,2*not*(not-1)+not*(z-4*not));   %vector of +ve mutual inductance
index=1;   %index for the above vector
totalmp=0;   %total value of positive mutual inductance
mneg=zeros(1,2*not^2+not*(z-4*not)+(z-4*not-2)*(z-4*not-1)*(z-4*not)/6 );
indexn=1;      %index for the above vector
totalmn=0;     %total value of negative mutual inductance
% determining the segment lengths
l(z)=101.4e-06;   % lengths of smallest two segments
l(z-1)=101.4e-6;
```

```
for n=2:z-1
 if k==1,
   l(z-n) = l(z-n+2) + (w+s);
   k=2;
 else
   l(z-n) = l(z-n+2) + (w+s);
   k=1;
 end;
end;
% determining self inductance, in nH, of all segments (and total)
for n=1:z,
 ind(n) = 2*l(n)*100*(0.50049 + (w+t)/(3*l(n)) + log((2*l(n))/(w+t)));
 total = total + ind(n);
end;
% determining +ve mutual inductance terms
for n=1:not,            % no of turns
  for y=1:z-4*n,        % y+4n has to be l.t. z
    if (y+4*n) <= z,    % this if loop is a redundant check
       if ( (y>4));
         if ( rem(y,4) ~=0),
          k=rem(y,4) + 4*(n-1);
             alpha=fix(y/4);
         else
          k=4 + 4*(n-1);
          alpha=fix(y/4)-1;
            end;
         gmd(n)=(1+alpha)*(s+w);
```

```
          p(n)=(1+alpha)*(s+w);
          lpk=l(k)-p(n);
        else
         k=y+4*(n-1);
         gmd(n)=(s+w);
         if k==1
           p(n) = (s+w);
           lpk=l(k)-p(n);
         else
           p(n) = (s+w);
           lpk=l(k)-p(n);
         end;
       end;

        q(1)= log(lpk/gmd(n)+sqrt(1+(lpk/gmd(n))^2)) + gmd(n)/lpk - sqrt(1+ (gmd(n)/
lpk)^2);
      q(2)= log(p(n)/gmd(n)+sqrt(1+(p(n)/gmd(n))^2)) + gmd(n)/p(n) - sqrt(1+ (gmd(n)/
p(n))^2);

       mpos(index)= (2*lpk*q(1) - 2*p(n)*q(2))*1e2;
       totalmp = totalmp + mpos(index);
       index;
       index=index+1;

    end;
  end
end;
```

```
totalmp = 2*totalmp;
 % determining the negative mutual inductance terms
for n=1:not,              % no of turns
 for y=1:z-2-4*(n-1),
   if (y+4*n-2) <= z      % again, this if loop is a redundant check
     if (y>4)
       if (rem(y,4) ~= 0),
         k=rem(y,4)+4*(n-1);
         alpha2=fix(y/4);
       else
         k=4+4*(n-1);
         alpha2=fix(y/4)-1;
       end;
         gmd2 = l(k+1) - alpha2*(s+w);
         p2 = alpha2*(s+w);
         p2b = (alpha2+1)*(s+w);
         lpk3=l(k+2+4*alpha2)+p2;
         lpk5=l(k+2+4*alpha2)+p2b;
          q(3)= log(lpk3/gmd2+sqrt(1+(lpk3/gmd2)^2)) + gmd2/lpk3 - sqrt(1+ (gmd2/
lpk3)^2);
           q(5)= log(lpk5/gmd2+sqrt(1+(lpk5/gmd2)^2)) + gmd2/lpk5 - sqrt(1+ (gmd2/
lpk5)^2);
       q(4)= log(p2/gmd2+sqrt(1+(p2/gmd2)^2)) + gmd2/p2 - sqrt(1+ (gmd2/p2)^2);
          q(6)= log(p2b/gmd2+sqrt(1+(p2b/gmd2)^2)) + gmd2/p2b - sqrt(1+ (gmd2/
p2b)^2);
       mneg(indexn) = 0.5*(2*lpk3*q(3)+2*lpk5*q(5) - 2*p2*q(4)-2*p2b*q(6))*1e2;
     else
```

```
        k=y+4*(n-1);
        gmd2 = l(k+1);
        p2 = l(k)-l(k+2);

          if p2==0
          q(4)=0;
        else
          q(4)= log(p2/gmd2+sqrt(1+(p2/gmd2)^2)) + gmd2/p2 - sqrt(1+ (gmd2/p2)^2);
        end;
            q(3)= log(l(k)/gmd2+sqrt(1+(l(k)/gmd2)^2)) + gmd2/l(k) - sqrt(1+ (gmd2/
l(k))^2);
        q(5)= log(l(k+2)/gmd2+sqrt(1+(l(k+2)/gmd2)^2)) + gmd2/l(k+2) - sqrt(1+
(gmd2/l(k+2))^2);
        mneg(indexn) = 0.5*(2*l(k)*q(3)+2*l(k+2)*q(5) - 2*p2*q(4))*1e2;
      end;
      totalmn = totalmn + mneg(indexn);
     indexn=indexn+1;
   end;
 end;
end;
if rem(z,4)==3
 k=z-2;
 gmd2 = l(k+1);
 p2 = l(k)-l(k+2);
 q(3)= log(l(k)/gmd2+sqrt(1+(l(k)/gmd2)^2)) + gmd2/l(k) - sqrt(1+ (gmd2/l(k))^2);
 q(5)= log(l(k+2)/gmd2+sqrt(1+(l(k+2)/gmd2)^2)) + gmd2/l(k+2) - sqrt(1+ (gmd2/
l(k+2))^2);
```

```
 if p2==0
   q(4)=0;
 else
   q(4)= log(p2/gmd2+sqrt(1+(p2/gmd2)^2)) + gmd2/p2 - sqrt(1+ (gmd2/p2)^2);
 end;
 mneg(indexn) = 0.5*(2*l(k)*q(3) + 2*l(k+2)*q(5) - 2*p2*q(4))*1e2;
 totalmn = totalmn + mneg(indexn);
end;
totalmn = 2*totalmn;
inductor= total + totalmp - totalmn
Rsquare=0.05;
Rsubsq=20;
Coxsq=20e-6; %12.2e-6; % F/m^2
eoxer=35.1742e-12;   % F/m
%series resistance
res=0.0;
for k=1:z,
 res=res+l(k);
end;
rs_tot=res*Rsquare/w

%%%%%%calculating the parasitics for the spice ckt
k1=1; %0.96;
k2=1; %0.71;
delta=0; %5e-6;
tepi=10e-6;
rhoepi=1.4;
```

```
for j=1:z
 res(j)=l(j)*Rsquare/(2*w);  %one half the total series resistance per segment
 rarea=k1*rhoepi*tepi/(l(j)+delta)/(w+delta);
 rperi=k2*rhoepi/2/(w+l(j)+2*delta);
 rsub(j)=rarea*rperi/(rarea+rperi)/2;  %one half the total substrate resistance
% rsub2(j)=l(j)*Rsubsq/(2*w);
 cox(j)=l(j)*w*Coxsq/2;      %oxide cap per side (one half of total)
end;

fid=fopen('subck.in','w');
endlp=fix(z/2);
for k=1:z
 j=z-k+1;
 fprintf(fid,'.SUBCKT ind%d',j);
 fprintf(fid,' in out a b grnd \n');
 fprintf(fid,'Rser1 in a %e \n', res(k));
 fprintf(fid,'Rser2 b out %e \n', res(k));
 fprintf(fid,'Cox1 in c %e \n',  cox(k));
 fprintf(fid,'Rsub1 c grnd %e \n', rsub(k));
 fprintf(fid,'Cox2 out d %e \n', cox(k));
 fprintf(fid,'Rsub2 d grnd %e \n', rsub(k));
 %fprintf(fid,'Rsublat d c %e \n', rsub2);
 fprintf(fid,'Rspice1 in grnd 100meg \nRspice2 out grnd 100meg \n.ENDS \n\n');

end;
%%%%%calculating the coeff's of mutual ind%%%
fid2=fopen('mutcoeff.in','w');
```

```
fprintf(fid2,'\n *the positive coefficients \n');
% the positive one's
m=1;
for a=z:-4:z-4*(not-1),
 b=a;
  for l2=1:fix(a/4),
    for k=1:4,
      if (b-4*l2 >0)
        mp(b, b-4*l2)=mpos(m);
        kp(m)=mp(b,b-4*l2)/sqrt(ind(z-b+1)*ind(z-b+4*l2+1));
%%%%%%%%%%write the o/p to a spice file
        fprintf(fid2,'KP%d',m);
        fprintf(fid2,' L%d',b);
        fprintf(fid2,' L%d %f \n',b-4*l2,kp(m));
        b=b-1;
        m=m+1;
      end;
    end;
    b=a;
  end;
  j=j+1;
end;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
fprintf(fid2,'\n *the negative coefficients \n');
% the negative one's
m=1;
for a=z:-4:z-4*(not),
```

```
  b=a;
   for l3=1:fix(a/4)+1,
     for k=1:4,
        if (b-4*l3+2 >0)
          mn(b,b-4*l3+2)=mneg(m);
          kn(m)=mn(b,b-4*l3+2)/sqrt(ind(z-b+1)*ind(z-b+4*l3-2+1));
%%%%%%%%%%write the o/p to a spice file
          fprintf(fid2,'KN%d',m);
          fprintf(fid2,' L%d',b);
          fprintf(fid2,' L%d %f \n',b-4*l3+2,-kn(m));
          b=b-1;
          m=m+1;
        end;
      end;
      b=a;
   end;
   j=j+1;
end;
%%%%calculating the inter-turn capacitance
correctn=2;   %correction factor for the simple formula being used
for j=1:z-4,
 lave=(l(z-j+1) + l(z-j+1-4))/2.0;
 cfr(j) = correctn*eoxer*t*lave/s;
end;
fid3=fopen('induct.in','w');
capfr(1)=0.5*cfr(1);
capfr(z-4+1)=0.5*cfr(z-4);
```

```
for j=2:z-4,
 capfr(j)=0.5*(cfr(j) + cfr(j-1));
end;
for j=1:z-4+1,  %z-4+1 are the # of inter-turn caps
 fprintf(fid3,'Cf%d %d %d %e \n',j,j,j+4,capfr(j));
end;
fprintf(fid3,'\n');
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%fid4=fopen('induct.in','w');
for m=1:z
 fprintf(fid3,'X%d %d %d a%d b%d grnd ind%d \n',m,m,m+1,m,m,m);
 fprintf(fid3,'L%d',m);
 fprintf(fid3,' a%d b%d',m,m);
 fprintf(fid3,' %fn \n\n',ind(z-m+1));
end;
```

APPENDIX III. SIMULATED ANNEALING BASED CAD TOOL

Note: This code has been succesfully executed on Perl version %, running on a HP Model 712/80 workstation.

```
#! /usr/local/bin/perl -w
sub output_header {   # The header subroutine
 system("clear");
 print"\n\n\n\Unote:  makesure that your screen size is maximized for full display!\n\n";
 print"\n\n\t\t\t\Uversion 1.1\E";

print"\n\n*****************************************************************
***\n\n";
 print"This is an iterative approach process to obtain a best\n";
 print"possible circuit component values to achieve high efficiency and\n";
 print"and high output power at the load antenna of 50-Ohm.\n";
 print"The process is done using simulated Annealing algorithm, in which\n";
 print"aids us to achieve this goal.\n";

print"\n*****************************************************************
**\n\n\n\n";
}

sub user_input {
 START1:print "Enter the SPICE (file.sp) filename: ";
   $spice_name = <STDIN>;
   chomp($spice_name);
```

```
 if (! -e $spice_name) {
  print"File $spice_name does not exist!!\n";
  goto START1;
 }
 chmod(0500,'$spice_name');

print"Enter the data (file.m) filename to store data: ";
 $data_name = <STDIN>;
 chomp($data_name);
 chmod(0500,'$data_name');

print "Would you like to generate a MATLAB file (y/n)? ";
$matlab=<STDIN>;
chomp($matlab);
if ($matlab eq 'y') {
 print"Enter the name of the MATLAB filename to be generated: ";
 $matlab_name=<STDIN>;
 chomp($matlab_name);
 print "Would you like to plot the results in MATLAB and print plots to printer when
done simulating (y/n)? ";
 $plot_results=<STDIN>;
 chomp($plot_results);
 if ($plot_results eq 'y') {
  print"Enter the name of the printer: ";
  $print_name=<STDIN>;
  chop($print_name);
 }
```

```
}
print"Would like E-Mail to be generated about the status of the iteration (y/n)? ";
$email=<STDIN>;
chomp($email);
if ($email eq 'y') {
  print"At every how many iterations would you like an e-mail (e.g. 5000=12Hrs.)? ";
  $limit=<STDIN>;
  chomp($limit);
}
if ($email eq 'y') {
  print"Enter the login names followed by a space: ";
  $login_name=<STDIN>;
  print"Enter the subject heading of the mail: ";
  $amp_name=<STDIN>;
 }

 print"\n";
 print"\n";
 print"\t\t\U Process Start Here!\n";
 print"\n";
 print"\n";

}

sub nominals {
        # INITIAL CONDITIONS (STARTING POINT)
```

```
$n=4;# Number of elements
$L1=1e-9;
$L3=10.0e-9;
$Cmatch1=1.0e-12;
$Rmatch1=50.0e-12;

@soln=($L1, $L3, $Cmatch1, $Rmatch1);
 @soln_name=("Best PAE", "Best RL(p)", "Best THD (%)", "L1 (H)", "L3 (H)",
"Cmatch1 (F)", "Rmatch1");
#foreach (@soln) {print"$_ \n";}
$size=@soln_name;
$size2=@soln;
}

sub main {
 if (-e $data_name){
  unlink $data_name;
 }
 open(DATA,">$data_name") || die "Can't open $data_name!! $!";
   $stamp2=localtime();
   print DATA "% $stamp2 \n\n";
       print DATA "%\t B(PAE)\t\t B(RL)\t\t B(HD)\t\t L1\t\t L3\t\t Cmatch1\t\t
Rmatch1\t\n\n";
   print DATA "x=[ \n";
 close(DATA);
 $bestpae=0;
 $Goal=60;# Goal to reach efficiency
```

```
$Max_time=50000;# Total number of iterations
$beta=1.1;# Constant
$alpha=.9;# Cooling Rate
$percentage=100;
$th_pae=30;
$th_dist=20;
$ind_limit=20e-9;
$cap_limit=50e-12;
while($bestpae<=$Goal) {
 $time=0;
 $m=500;# Number of iterations at each T
 $T=10;
 $iterations=0;
 $M=0;# Write to data file if pae>=th
 $accepted=0;# Accepted P.A.E.'s
 $index=1;
 do {
  if ($time==0) {
   print"\UEntering Metropolis Subroutine!\n\n";
  }
  if ($time>0) {
   print "\UEntering Metropolis Subroutine Again!!\n\n";
  }
  @hold=&metropolis();
  print"\UThe Metropolis subroutine is now done! \n\n";
  $time=$time+$m;
  $T=$alpha*$T;
```

```
    $m=$beta*$m;
    $m=int($m+.5);
    if ($time < $Max_time) {
      my($run)=$time+$m;
      my($diff)=$Max_time-$time;
      if ($run>$Max_time) {
        $m=$diff-1;
      }
      print"\UStill time available (time=$time), back to Metropolis subroutine\n";
      print"\UAnnealing parameters (T, M, alpha) are modified\n\n";
    }
  }
  until $time>=$Max_time;
  if ($email eq 'y') {
    &mail_manager(@soln);
     print "NOTE:  GENERATED STATUS REPORT BY E-MAIL TO: $login_name
\n";
  }
  print"\n\n\t\t\UThe Annealer Algorithm is now done!!\n\n";
  print"The best solutions obtained were: \n\n";
  print"\t P.A.E. = $hold[0]%\n";
  print"\t RI(P)  = $hold[1] Watts\n";
  print"\t Distorion = $hold[2]%\n";
  print"\n";
  if ($bestpae<=$Goal) {
    print"Since $bestpae is less than $Goal (The goal), testing again with\n";
    print"best solution in hand at this time and reseting the control parameters\n\n";
```

```
    open(DATA,">>$data_name") || die "Can't open $data_name!! $!";
      print DATA "\n\n %  A set of Iterations are done!\n";
      print DATA "% Goal has not been reached so going back to algorithm\n\n";
      print DATA "%  Total # of Iterations were: $hold[3] \n";
      print DATA "%  Total # of P.A.E.s accepted: $hold[4] \n";
      printf DATA "%%  Percentage of New P.A.E. accepted: %7.4f %%\n", $hold[5];
      $stamp3=localtime();
      print DATA "% $stamp3 \n";
    close(DATA);
   }
 }
 open(DATA,">>$data_name") || die "Can't open $data_name!! $!";
    print DATA "]; \n\n";
    print DATA "%  Total # of Iterations were: $hold[3] \n";
    print DATA "%  Total # of P.A.E.s accepted: $hold[4] \n";
    printf DATA "%%  Percentage of New P.A.E. accepted: %7.4f %%\n", $hold[5];
    $stamp3=localtime();
    print DATA "% $stamp3 \n";
 close(DATA);
}

sub metropolis {
  @newsoln=@soln;
  if ($time==0) {
    print"\UModifying the Initial spice.sp file Values to New values & Run SPICE (@
Metropolis)\n\n";
    @best=&get_pae(@soln);
```

```
  $bestpae=$best[0];
  $bestrlp=$best[1];
  $bestdist=$best[2];
  print"The accepted Annealing solution is: \n\n";
  print"\t\tPAE = $bestpae% \n";
  print"\t\tRL(p) = $bestrlp Watts\n";
  print"\t\tDistortion = $bestdist% \n\n";
  unshift(@soln,$bestdist);
  unshift(@soln,$bestrlp);
  unshift(@soln,$bestpae);
  &write_file(@soln);
  shift(@soln);
  shift(@soln);
  shift(@soln);
 }
 $M=$m;
 do {
  print"\Uinside Metropolis Subroutine loop with M=$M\n\n";
  @newsoln=&getsoln(@newsoln);
  $iterations++;
   print"\UModifying the Old spice.sp file values to new values & run spice (@ Get-
soln)\n\n";
  @new=&get_pae(@newsoln);
  $newpae=$new[0];
  $newrlp=$new[1];
  $newdist=$new[2];
  $x=rand();
```

```
$delta_h=$newpae-$bestpae;
    if ($delta_h>0 || ($x<exp($delta_h/$T) && $newpae>$th_pae && $newd-
ist<$th_dist)) {
  for ($j=0; $j<$n; $j++) {
    $soln[$j]=$newsoln[$j];
  }
  $bestpae=$newpae;
  $bestrlp=$newrlp;
  $bestdist=$newdist;
  print "\t\UNew Annealing solution has been found!!!!!!!!\n\n";
  $accepted++;
  unshift(@newsoln,$bestdist);
  unshift(@newsoln,$bestrlp);
  unshift(@newsoln,$bestpae);
  &write_file(@newsoln);
  shift(@newsoln);
  shift(@newsoln);
  shift(@newsoln);
 }
 if ($email eq 'y') {
  $dum=$index*$limit;
  if ($iterations==$dum) {
    unshift(@newsoln,$bestdist);
    unshift(@newsoln,$bestrlp);
    unshift(@newsoln,$bestpae);
    &mail_manager(@newsoln);
```

```
        print "NOTE:  GENERATED STATUS REPORT BY E-MAIL TO: $login_name
\n";
        $index++;
        shift(@newsoln);
        shift(@newsoln);
        shift(@newsoln);
       }
     }
     $M=$M-1;
     print"The accepted Annealing solution so far is: \n\n";
     print"\t\tPAE = $bestpae% \n";
     print"\t\tRL(p) = $bestrlp Watts\n";
     print"\t\tDistortion = $bestdist% \n\n";
     if (! $iterations==0){
      $percentage=($accepted/$iterations)*100;
      print"\t\tNumber of Iterations so far: $iterations \n";
      print"\t\tNumber of New PAEs Accepted: $accepted  \n";
      printf"\t\tPercentage of new P.A.E. Accepted: %7.4f %%\n\n", $percentage;

     }
    }
   until ($M<0);
   @dummy=($bestpae,$bestrlp,$bestdist,$iterations,$accepted,$percentage);
   return @dummy;
}

sub write_file {
```

```
  open(DATA,">>$data_name") || die "Can't open $data_name!! $!";
   foreach (@_) {printf DATA "\t %8.4e", $_;}
   print DATA "\n";
  close(DATA);
}

sub getsoln{
 @_=@newsoln;
 $l_val=1;
 for ($j=0; $j<=$l_val; $j++){# Inductor Loop
  $delta1=$T*(rand()-.5)/10000000000;# For Inductors
  if (($newsoln[$j]+$delta1>0) && ($newsoln[$j]+$delta1<=$ind_limit)) {
   $newsoln[$j]=$newsoln[$j]+$delta1;
  }
  else{
   $newsoln[$j]=$newsoln[$j];
  }
 }
 for ($j=$l_val+1; $j<$n; $j++){# Capacitor Loop
  $delta2=$T*(rand()-.5)/10000000000000;# For Capacitors
  if (($newsoln[$j]+$delta2>0) && ($newsoln[$j]+$delta2<=$cap_limit)) {
   $newsoln[$j]=$newsoln[$j]+$delta2;
  }
  else{
   $newsoln[$j]=$newsoln[$j];
  }
 }
```

```
return @newsoln;
}

sub get_pae {
  @input=@_;
  open(SPICE_SP,"$spice_name") || die "Can't Open $spice_name File: $!";
  $i=0;
  @place=0;
  while(<SPICE_SP>) {
   s/^\s+//;
   $place[$i] = $_;
   if (/^l1\s/i) {
    $line=$_;
    chomp($line);
    print"Line Read for Replacement:\t $line\n";
    @hold=split(' ',$line);
    print "Line Replaced By:\t\t $place[$i] \n" if $place[$i]=~s/$hold[3]/$input[0]/i;
    $Rxrser=-0.0139*(($input[0]/1e-9)**2)+0.8705*($input[0]/1e-9)+1.1701;
    $Rxrsub=-0.0447*($input[0]/1e-9)+16.0755+3.5064/($input[0]/1e-9);
    $Cxcox=(-0.0005*(($input[0]/1e-9)**2)+0.0307*($input[0]/1e-9)+0.0468)*1e-12;
   }
       # L1 Parasitics

   if ((/^rser1\s/i) || (/^rser2\s/i)) {
    $line=$_;
    chomp($line);
```

```
 print"Line Read for Replacement:\t $line\n";
 @hold=split(' ',$line);
 print "Line Replaced By:\t\t $place[$i] \n" if $place[$i]=~s/$hold[3]/$Rxrser/i;
}
if ((/^Cox1\s/i) || (/^Cox2\s/i)) {
 $line=$_;
 chomp($line);
 print"Line Read for Replacement:\t $line\n";
 @hold=split(' ',$line);
 print "Line Replaced By:\t\t $place[$i] \n" if $place[$i]=~s/$hold[3]/$Cxcox/i;
}
if ((/Rsub1\s/i) || (/^Rsub2\s/i)) {
 $line=$_;
 chomp($line);
 print"Line Read for Replacement:\t $line\n";
 @hold=split(' ',$line);
 print "Line Replaced By:\t\t $place[$i] \n" if $place[$i]=~s/$hold[3]/$Rxrsub/i;
}

if (/^I3\s/i) {
 $line=$_;
 chomp($line);
 print"Line Read for Replacement:\t $line\n";
 @hold=split(' ',$line);
 print "Line Replaced By:\t\t $place[$i] \n" if $place[$i]=~s/$hold[3]/$input[1]/i;
 $Rxrser2=-0.0139*(($input[1]/1e-9)**2)+0.8705*($input[1]/1e-9)+1.1701;
 $Rxrsub2=-0.0447*($input[1]/1e-9)+16.0755+3.5064/($input[1]/1e-9);
```

```
    $Cxcox2=(-0.0005*(($input[1]/1e-9)**2)+0.0307*($input[1]/1e-9)+0.0468)*1e-
12;
  }
        # L2 Parasitics

  if ((/^rser3\s/i) || (/^rser4\s/i)) {
   $line=$_;
   chomp($line);
   print"Line Read for Replacement:\t $line\n";
   @hold=split(' ',$line);
   print "Line Replaced By:\t\t $place[$i] \n" if $place[$i]=~s/$hold[3]/$Rxrser2/i;
  }
  if ((/^Cox3\s/i) || (/^Cox4\s/i)) {
   $line=$_;
   chomp($line);
   print"Line Read for Replacement:\t $line\n";
   @hold=split(' ',$line);
   print "Line Replaced By:\t\t $place[$i] \n" if $place[$i]=~s/$hold[3]/$Cxcox2/i;
  }
  if ((/Rsub3\s/i) || (/^Rsub4\s/i)) {
   $line=$_;
   chomp($line);
   print"Line Read for Replacement:\t $line\n";
   @hold=split(' ',$line);
   print "Line Replaced By:\t\t $place[$i] \n" if $place[$i]=~s/$hold[3]/$Rxrsub2/i;
  }
```

```
 if (/^Cmatch1\s/i) {
  $line=$_;
  chomp($line);
  print"Line Read for Replacement:\t $line\n";
  @hold=split(' ',$line);
  print "Line Replaced By:\t\t $place[$i]\n" if $place[$i]=~s/$hold[3]/$input[2]/i;
 }

 $Rinmatch = $input[3]*1000000000000;
 if (/^Rmatch1\s/i) {
  $line=$_;
  chomp($line);
  print"Line Read for Replacement:\t $line\n";
  @hold=split(' ',$line);
  print "Line Replaced By:\t\t $place[$i]\n" if $place[$i]=~s/$hold[3]/$Rinmatch/i;
 }


$i++;
}
 close(SPICE_SP);
 open(SPICE_SP,">$spice_name");
    print SPICE_SP "@place\n";
    #print "The contents of the new SPICE file is:\n\n @place\n";
 close(SPICE_SP);
```

```
$spice_output="spice1.lis";
print"Running HSPICE on $spice_name file.  Please wait ....\n";
print"\nThe output of the HSPICE will be: $spice_output \n\n";
open(FILE,"|hspice $spice_name > $spice_output");
close(FILE);
print"\nDone with HSPICE!!\n\n";

print"**  Reading the contents of the $spice_output output file!!\n\n";
open(SPICE_LIS,"$spice_output");
while(<SPICE_LIS>) {
 s/^\s+//;
 if (/^eff\s+/i) {
   $line=$_;
   chomp($line);
   print"Line Read from $spice_output:\t\t\t$line\n";
   @hold_pae=split(' ',$line);
   $pae=$hold_pae[2];
 }
 if (/^pow_out\s+/i) {
   $line=$_;
   chomp($line);
   print"Line Read from $spice_output:\t\t\t$line\n";
   @hold_rl_power=split(' ',$line);
   $rlp=$hold_rl_power[2];
 }
 if (/^total\sharmonic\sdistortion\s+/i) {
   $line=$_;
```

```
    chomp($line);
    print"Line Read from $spice_output:\t\t$line\n";
    @hold_distortion=split(' ',$line);
    $disto=$hold_distortion[4];
   }
  }
  print"\n\n\t\t**************************************************\n";
  print"\t\t*\t P.A.E.\t=\t $pae % \t\t *\n";
  print"\t\t*\t RL(P)\t=\t $rlp Watts \t *\n";
  print"\t\t*\t HD\t=\t $disto % \t\t *\n";
  print"\t\t**************************************************\n\n";
  @dummy2=($pae,$rlp,$disto);
  return @dummy2;
}

sub mail_manager {
 if ($email eq 'y') {
   @get=@_;
   $my_login='guptara@ece.orst.edu';
   open(MAIL,"|/usr/sbin/sendmail -t -fguptara\n");
    print MAIL "From: $my_login \n";
    print MAIL "To: $login_name \n";
    print MAIL "Subject: $amp_name \n\n";
    print MAIL "\n";
    print MAIL "\nNOTE:  This e-mail is generated automatically\n\n";
    print MAIL "\t\t\UStatus Report on the Annealer Program\n";
    print MAIL "\t\t**********************************\n";
```

```
print MAIL "\n\tTotal number of iterations up to now: $iterations\n";
print MAIL "\tTotal number of PAEs accepted (data file: $data_name): $accepted
\n";
printf MAIL "\tPercentage of new PAE Accepted: %7.4f %%\n\n", $percentage;
print MAIL "The current Annealing solution accepted is: \n\n";
print MAIL "\t\tPAE = $get[0]% \n";
print MAIL "\t\tRL(p) = $get[1] Watts\n";
print MAIL "\t\tTHD = $get[2]% \n\n";
print MAIL "\t\t\t\UOther stats:\n";
print MAIL "\t\t\t**********\n\n";
print MAIL "Number of iterations allowed at each temperature: m = $m \n";
printf MAIL "Current Temperature: T = %11.8f \n", $T;
print MAIL "Cooling Rate at: Alpha = $alpha\n";
print MAIL "Increase iterations at each temperature coefficient: Beta = $beta\n";
print MAIL "Anealling Parameter M inside Metropolis Subroutine is currently at:
M = $M\n";
print MAIL "Number of elements in circuit under test: $size2\n";
print MAIL "Number of elements in circuit & obtained from SPICE: $size\n";
my($times)=$time+($m-$M);
$left=$Max_time-($times);
if ($left<0) {
 print MAIL "Done already with time; waiting for inner loop to finish\n";}
else {print MAIL "Current time: $times out of $Max_time\n";}
print MAIL "Number of iterations to go yet: $left\n";
print MAIL "The maximum inductor limit: $ind_limit\n";
print MAIL "The maximum capacitor limit: $cap_limit\n\n";
print MAIL "The MATLAB filename to plot data is $matlab_name\n\n\n";
```

```
    print MAIL "Ravi Gupta \n\n";
    print MAIL"*********************************************\n";
    print MAIL"Oregon State University\n";
    print MAIL"Department of Electrical and Computer Engineering\n";
    print MAIL"*********************************************\n\n";
    print MAIL"Tel   : (541) 758-9003\n";
    print MAIL"Office: (541) 737-4069\n";
    print MAIL"E-Mail: $my_login\n\n";
    print MAIL"*********************************************\n";
   close(MAIL)
  }
}
&output_header();
&user_input();
&nominals();
&gen_matlab_file();
&main();
&do_matlab();
```