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René Spée

The awareness of electric power quality has increased over the past decade as electronic equipment has become more susceptible to power disturbances. The most disruptive power disturbances are voltage sags and momentary interruptions and their effect on adjustable speed drives (ASDs) is studied in this thesis.

Several solutions have been suggested to provide only voltage sag ride-through to ASDs, but most solutions focus on ASDs with passive rectifiers since they hold the largest share of the market. This thesis focuses on ASDs with active rectifiers, which is an emerging and growing market due to the advantages of four quadrant operation and reduced harmonics offered. A solution is presented which provides an ASD with an active rectifier with the capability to ride through the most common sags in order to reduce the frequency at which the ASD trips and thereby increase its reliability.

In order to provide ASDs with the capability to ride through momentary interruptions, it is necessary to interface an energy storage system to the ASD. Flywheels, ultra-capacitors and batteries are evaluated for use in an energy storage system to provide voltage sag and momentary interruption ride-through and a detailed comparison of six systems based on these technologies is presented. The interface circuit between the energy storage system and ASD has a significant influence on the performance of the energy storage system and therefore interface circuits to ASDs with passive and active rectifiers are studied.

The addition of an ultra-capacitor energy storage system to an ASD with an active rectifier in order to provide ride-through of deeper sags and momentary interruptions is studied and a fuzzy logic controller is designed to enhance system performance. Initially, no communication between the ASD and the ultra-capacitor system is assumed and the ultra-capacitor system can therefore be added as a retro-fit to an existing ASD. It is, however, foreseen that the market for ASDs with ride-through capability of voltage sags and momentary interruptions will grow and the concepts for an integrated design of an ASD and an energy storage system are presented.

Voltage Sag and Momentary Interruption Ride-through for Adjustable Speed Drives

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LIST OF SYMBOLS

C_{dc}	capacitance of the dc bus capacitor [F]
C_{es}	equivalent capacitance of the ultra-capacitor bank [F]
E_{dc}	energy stored in the dc bus capacitor [J]
E_{del}	energy delivered by the ultra-capacitor bank to the dc bus of the ASD [J]
E_{st}	ultra-capacitor bank [J]
E_{fw}	energy stored in the flywheel [J]
i_{Cdc}	instantaneous current in dc bus capacitor [A]
I_{Cdc}	average current in dc bus capacitor [A]
I_{es}	average ultra-capacitor current [A]
$I_{es,dc}$	average boost converter output current [A]
$i_{inv,dc}$	instantaneous inverter input current [A]
$I_{inv,dc}$	average inverter input current [A]
I_{inv}	rms inverter output current [A]
$I_{inv,rated}$	rated continuous inverter output current [A]
I_{rec}	rms rectifier input current [A]
$i_{rec,dc}$	instantaneous rectifier output current [A]
$I_{rec,dc}$	average rectifier output current [A]
$I_{rec,sag}$	rms rectifier input current during sag [A]
I_{rec0}	rms rectifier input current before onset of sag [A]
$P_{inv,out}$	inverter output power [W]
$P_{rec,in}$	rectifier input power [W]
P_{Cdc}	average power delivered by the dc bus capacitor [W]
R_{es}	equivalent series resistance of the ultra-capacitor bank [Ω]
sag	sag magnitude, $0 \leq sag \leq 1$
$S_{inv,rated}$	rated inverter apparent output power [VA]
v_{dc}	instantaneous dc bus voltage [V]
V_{dc}	average dc bus voltage [V]
$V_{dc,rec}^{*}$	reference average dc bus voltage for rectifier [V]
$V_{dc,bst}^{*}$	reference average dc bus voltage for boost converter [V]
V_{es}	voltage across ultra-capacitor bank [V]
V_{ll}	rms rectifier input line-to-line voltage [V]
$V_{ll,nom}$	nominal rms rectifier input line-to-line voltage [V]
$V_{ll0,sag}$	rms rectifier input line-to-line voltage during sag [V]
V_{ll0}	rms rectifier input line-to-line voltage before onset of sag [V]
V_o	rms fundamental line-to-line inverter output voltage [V]

LIST OF SYMBOLS (Continued)

V_{uc}	voltage across equivalent capacitance of ultra-capacitor bank [V]
η_{inv}	inverter efficiency, $0 \leq \eta_{inv} \leq 1$
η_{rec}	rectifier efficiency, $0 \leq \eta_{rec} \leq 1$

Subscripts

$_{max}$	maximum
$_{min}$	minimum

Superscripts

*	reference value

DEDICATION

The fear of the Lord is the beginning of knowledge.
Proverbs 1:7a

VOLTAGE SAG AND MOMENTARY INTERRUPTION RIDE-THROUGH FOR ADJUSTABLE SPEED DRIVES

1. INTRODUCTION

1.1 POWER QUALITY

Power quality has become an active research field over the past decade as a result of the increase in non-linear loads in the power system, causing a deterioration in power quality, as well as the increased sensitivity of modern electric and electronic equipment to power system disturbances. Power line disturbances can adversely affect the operation of sensitive equipment such as computers, communication equipment and process control systems, leading to valuable data loss, interruption to communication services and long production downtimes. The increased sensitivity of electronic devices and equipment that provide automation in process industries is redefining the reliability of the power system to cycle-to-cycle continuity of power [2].

There are also concerns that the deregulation of the electric utilities will cause a deterioration in reliability and power quality as utilities will try to cut operating costs in order to competitively price their power. This may include a decrease in preventative maintenance such as tree trimming which will increase the risk of faults on the power system.

The two kinds of disturbances which present the most problems with these types of equipment are voltage sags and momentary interruptions [22]. A voltage sag is defined as a decrease in rms voltage of between 10% and 90% of nominal voltage, for periods from a half cycle up to a minute long, whereas a momentary interruption is a decrease in rms voltage of greater than 90% [2]. The severity of the effect of a voltage sag on equipment depends on both its magnitude and its duration [22]. Adjustable speed drives (ASDs), automated data processors and programmable logic controllers have been found to be the three kinds of equipment most susceptible to voltage sags and momentary interruptions. Industrial facilities which rely heavily on electronics-based controls such as adjustable speed drives (ASDs) can therefore experience heavy losses due to voltage sags or momentary interruptions [3]. The textile, plastics and paper industries are particularly sensitive because of the high degree of continuity required in their processes to produce high quality products. In order to minimize the impact of a power disturbance on a manufacturing plant, it is therefore of importance to provide ASDs with immunity to, or at least a certain level of robustness to power disturbances. There is an abundance of Adjustable Speed Drives (ASDs) on the market and different types of ASDs and even different models present important differences with respect to their susceptibility to voltage sags.

1.2 Causes and Properties of Sags and Interruptions

A voltage sag or momentary interruption is caused by fault conditions within the manufacturing facility or power system and lasts until the fault is cleared by a fuse or breaker. The process of a voltage sag created by remote fault clearing is explained in [28] and simple equations for calculating voltage sag magnitude are given. The voltage sag magnitude at any particular location depends on fault current and impedance. Each voltage sag lasts as long as the protection equipment allows fault current to flow. On the utility side the fault condition may be a result of lightning, wind, contamination of insulators, animals or accidents [8]. Similarly, failures in the manufacturing facility or the starting of large motors can lead to a voltage sag, although the magnitudes of sags due to motor starting are usually not severe enough to cause equipment malfunction [27].

Momentary interruptions occur when the fault is electrically very close to the customer, but voltage sags are much more common since they are the result of faults electrically further away. For a specific type of fault, the sag magnitude depends on the distance from the customer to the fault location, with a fault close to the customer resulting in a deeper sag than a remote fault. Single line-to ground faults are the most common and result in a much less severe voltage sag than three phase faults.

Transmission-related voltage sags are generally much more consistent in duration than distribution voltage sags. Because of the large amounts of energy associated with transmission faults, they are cleared as soon as possible. This normally corresponds to 3-6 cycles, which is the total time for fault detection and breaker operation. Normally, customers do not experience an interruption for a transmission system fault since transmission systems are looped or networked, as opposed to distribution systems which are often radial [27].

It is impossible to eliminate voltage sags due to remote fault clearing and predicting the voltage sag frequency, or how often voltage sags occur, requires an accurate network impedance model and reliability data for all equipment in the electrical neighborhood. The impact of a particular remote fault-clearing voltage sag depends on the design of the drive. Performance improves when drives are modified to decrease their sensitivity to remote fault-clearing voltage sags. Uninterruptible power supplies and other power conditioning equipment are traditional solutions for low-power loads, but these cannot readily be applied to sensitive high power loads like adjustable speed drives.

Several ways of achieving ASD ride-through have been suggested in the literature [38][54] and/or implemented commercially. A first step in deciding which ride-through scheme to apply is to specify what events the ASD is required to ride through. Then it is necessary to consider the functional operation of the ASD in order to determine the requirements for a ride-through scheme.

1.3 Power Quality Surveys

Several major power quality surveys have been conducted in the last decade in an attempt to describe the electrical environment in which electrical and electronic equipment typically has to operate. With this information, it is possible to define reasonable requirements for an ASD to meet in order to ride through the most common sags and momentary interruptions. Only results of power quality surveys in North America are considered.

It was found that most sags have a magnitude of less than 40% [21], i.e. the minimum rms voltage during the sag does not drop below 60% of nominal, with the highest density of sag magnitudes between 10% and 20% [10]. Furthermore, most sags have a duration of less than 60 cycles [21][28] and tend to cluster around durations of 4, 30 and 120 cycles, which are typical circuit breaker reclosing times. Most momentary interruptions last between one and three seconds [22]. It was also found that continuous processes are prone to be interrupted for sags deeper than 15% to 20% [28][8][9] and with a duration of more than 12 cycles [8].

When combining data from different surveys it has to be kept in mind that the data may have been collected at different points within the electrical system – some at the building service entrance, others at substations at the distribution voltage level, still others at the electrical outlet in the building [10]. This is important because it has been found that sags are more frequent, deeper and of longer duration on the industrial (secondary) side than on the utility (primary) side [11]. Although the surveys present valuable information with regards to what an average or typical site may expect, it is important to note the uniqueness of each site in terms of power disturbances experienced [11].

Therefore, in order to make the drive immune to the most common sags, ride-through for sags with a magnitude of up to 40% and duration of up to 60 cycles should be provided. If immunity from the most common momentary interruptions is also desired, ride-through should be provided for at least 3 seconds with a complete loss of input power, but more effective protection can be gained if ride-through is provided for up to 5 seconds. It is important to note that there are two distinct categories of providing ride-through of power disturbances to equipment:

1. enable the equipment to ride through the most common power disturbances (~5 sec.)
2. enable the equipment to ride through power disturbances until a backup generator is brought on line (~10-45 sec.)

Only the first category, of providing ride-through only through the most common power disturbances, is addressed in this thesis.

1.4 Adjustable Speed Drives

An adjustable speed drive is an electronic interface between the utility grid and an electrical motor which provides speed and torque control of the motor. It has been found that most drives in industry are

in the fractional to 300kVA range, with the majority rated around 100kVA [38], therefore ride-through requirements for drives in the 100kVA to 300kVA range with a constant power load and 480V three phase input voltage are considered in this study. The type of ASD considered for this work consists of a rectifier and inverter, connected through a common dc bus, as shown in Figure 1. The inverter controls the magnitude and frequency of the motor current I_{inv} in order to control the speed and torque of the motor and it consists of three half bridge arrangements of transistors with anti-parallel diodes, as shown in Figure 2. The rectifier may have the same configuration as the inverter, known as an active rectifier, shown in Figure 2. An active rectifier regulates the dc bus voltage V_{dc} by controlling the rectifier input current I_{rec}. The rectifier may also consist of a three phase diode bridge, known as a passive rectifier, shown in Figure 3.

1.5 Voltage Sags and ASDs

For an ASD with a common dc bus between the inverter and rectifier, the available inverter output voltage and current is dependent upon the dc bus voltage. As the dc bus voltage drops, the maximum voltage and current the inverter can deliver drops. The result of a significant drop in dc bus voltage is that the inverter is no longer able to deliver the required voltage and current to the machine load, resulting in a loss of speed and/or torque control. Methods for achieving ride-through therefore focus on maintaining the dc bus voltage within an acceptable margin from nominal.

The drop in dc bus voltage which can be tolerated is determined by the individual application requirements of the ASD, but will generally be in the order of 10% to 15%. It is also important to maintain sufficient voltage for the control electronics. This can be achieved by either using power supplies with the capability of operating reliably under voltage sag conditions, or by drawing the power for the control electronics from the dc bus, assuming that the dc bus voltage is regulated during the sag or interruption condition.

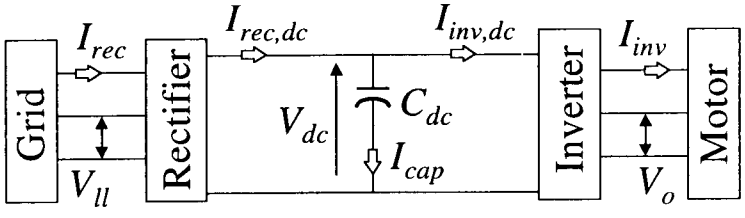


Figure 1 ASD with a common dc bus

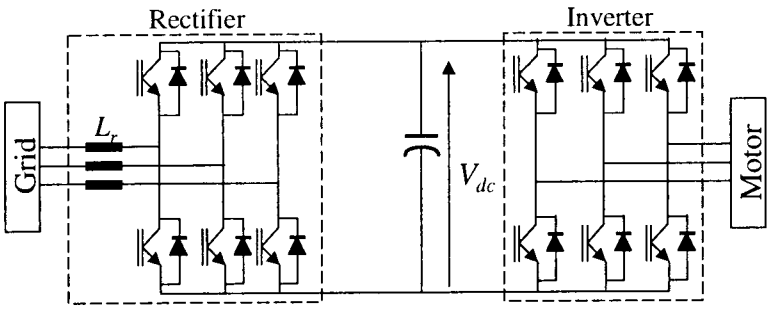


Figure 2 ASD with an active rectifier

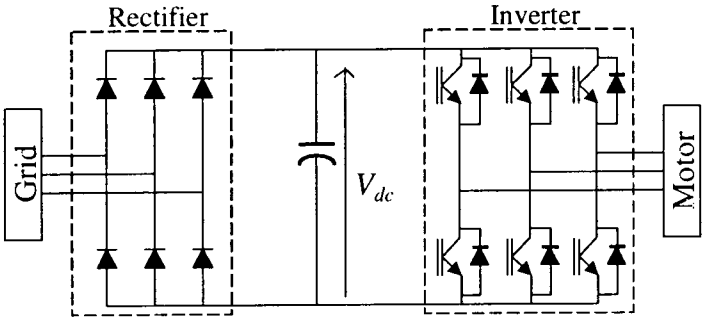


Figure 3 ASD with a passive rectifier

The second reason is that some processes, referred to as critical loads, cannot tolerate the loss of precise speed or torque control even for a few seconds. For inverters under current regulation, the current regulator can saturate if the dc bus voltage drops too low. For a motor under a standard V/Hz control, if the dc bus voltage drops too low, the drive may not be able to deliver the required voltage to the motor at a certain speed. The dc bus voltage therefore needs to be kept within reasonable bounds from the nominal dc bus voltage during a sag.

1.6 Objectives and Thesis Outline

The susceptibility of ASDs to voltage sags and momentary interruptions and methods of increasing their robustness to these disturbances are investigated because of the financial losses which could be incurred by manufacturers, especially those with continuous processes, as a results of the sensitivity of ASDs. The objective of this study is to propose a methodology for increasing the ride-through capability of ASDs to voltage sags and momentary interruptions. The ride-through requirements have already been set forth based on results from several major power quality surveys. Since an energy storage system is

needed to provide ride-through of deep sags and momentary interruptions, Chapter 2 discusses and compares three viable energy storage technologies for this application. The requirements on energy storage technologies to be used for ASD ride-through are presented as well as different ways of interfacing an ASD and an energy storage system.

Chapter 3 gives an overview of ride-through methodologies for ASDs which have been published and/or implemented commercially. This study focuses on ASDs with active rectifiers and in Chapter 4 a sag ride-through methodology for an ASD with an active rectifier is presented and in Chapter 5 this is extended to ride-through of sags *and* interruptions, which can only be achieved by the interfacing of an energy storage system to the ASD. An ultra-capacitor system is selected for this purpose. A global control philosophy is presented which enhances system performance by coordinating the rectifier and the boost converter.

Chapter 6 concludes the study and offers recommendations for future work.

2. ENERGY STORAGE

2.1. INTRODUCTION

It is necessary to interface an energy storage system with an ASD in order to provide it with the capability to ride through deep sags and momentary interruptions. In this chapter the requirements on an energy storage system for voltage sag and momentary interruption ride-through are presented and viable energy storage technologies for this application are discussed and compared. Methods of interfacing the energy storage system to an ASD are discussed and a novel interface circuit by which the active rectifier of the ASD is used for AC/DC as well as DC/DC conversion is introduced. Results from an experimental evaluation of two ultra-capacitor technologies are presented.

Due to the nature of the application, the energy storage system has some unique requirements. The most important of these is the high power to energy ratio which is required. For example, if 3 seconds of momentary interruption ride-through is required for a 250kW load, the energy storage system is required to deliver 250kW and 750kJ, resulting in a ratio of 0.33W/J. Many energy storage technologies have advanced in terms of ever higher energy densities, as opposed to power densities needed in this application. Some other requirements on an energy storage system for ASD ride-through are listed below.

- cost-effective
- high specific power
- high power density
- high efficiency, during discharge and while on standby
- fast response
- low maintenance
- reliability

An evaluation of currently available energy storage technologies which can meet the above mentioned requirements was made and three viable energy storage technologies were found: flywheels, advanced lead-acid batteries and ultra-capacitors. Since the interface circuit between the energy storage elements and the ASD has a significant influence on the performance of the system, energy storage systems which include the interface circuit are compared for application to ASD ride-through.

2.2. SPECIFICATIONS

The specifications for the energy storage system may differ depending on whether a passive or active rectifier is used. In either case, a suitable energy storage technology needs to be decided upon

which is connected to the ASD through an appropriate interface circuit. An energy storage system connected to the dc bus of the ASD is shown in Figure 4.

2.2.1. ASD with Passive Rectifier

In an ASD with a passive (diode bridge) rectifier, the dc bus voltage is directly proportional to the line voltage, with a nominal dc bus voltage of approximately 650V for a 480V three phase input. The dc bus voltage will drop as the line voltage drops during a sag or interruption condition. The dc bus capacitance can provide some hold-up time, but this is in the order of milliseconds rather than seconds.

Once the dc bus voltage drops to the minimum voltage at which satisfactory operation of the ASD can be achieved, the energy storage system is engaged to supply power to the load and to regulate the dc bus voltage. Since the energy storage system is regulating the bus voltage to a voltage higher than what the diode bridge can maintain it at, the diodes in the rectifier are reverse biased and therefore the energy storage system has to supply all the power to the load.

2.2.2. ASD with Active Rectifier

For a 480V input to an ASD with an active rectifier, the nominal dc bus voltage is typically around 800V. Ride-through of shallow sags can be provided by increasing the input current to the rectifier as the input voltage drops in order to provide constant power to the load [12]. By doing this, the rectifier is able to regulate the dc bus voltage as long as the current limit of the rectifier is not exceeded. Beyond that point, an energy storage system is needed to regulate the bus voltage. For a constant power load, which is assumed here, the energy storage system has to supply the power which cannot be supplied by the rectifier under power system disturbance conditions.

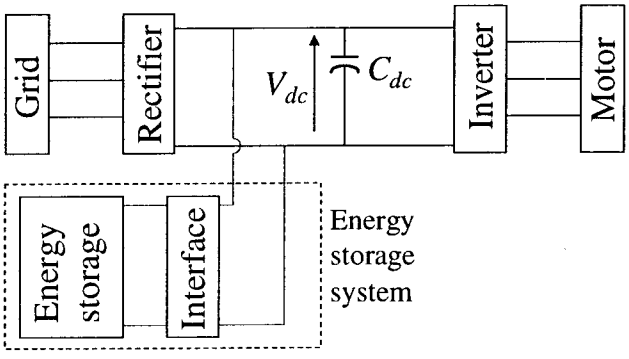


Figure 4 ASD under consideration

When only voltage sag ride-through is required, an ASD with an active rectifier has a distinct advantage over a drive with a passive rectifier since, for a passive rectifier, the energy storage system has to supply *all* of the load power once the dc bus voltage drops below the specified minimum voltage, i.e. even if the sag is only 30%, the energy storage system has to supply 100% of the load power.

However, for voltage sag *and* momentary interruption ride-through the energy storage system is required to deliver the full load power regardless of whether the ASD has an active or passive rectifier.

2.3. Comparison of Energy Storage Technologies for ASD Ride-through

ASD ride-through applications require the energy storage system to have a high power density, but in contrast to traditional energy storage applications, the energy density required is fairly low. Due to the nature of the application, the energy storage system will spend most of its life on standby and therefore its efficiency on standby is of importance. Other important parameters include the efficiency, output voltage regulation, reliability and level of maintenance required. In evaluating how cost-effective a specific energy storage system is, it is important to consider both the initial capital investment required and the cost of ownership which is influenced by the level and frequency of maintenance required as well as the life time of the energy storage elements. A comparison of three energy storage technologies, flywheels, ultra-capacitors and batteries, based on criteria specifically developed for ASD ride-through applications, is presented. An overview of the three energy storage technologies and a comparison of specific products are presented.

2.3.1. Flywheels

To store energy, a flywheel energy storage system converts electrical energy to kinetic energy through an electrical motor, increasing the rotational speed of the flywheel coupled to the rotor. The amount of energy stored in a rotating flywheel E_{fw} is

$$E_{fw} = \frac{mr^2\omega^2}{2} \tag{2.1}$$

with m the mass, r the mean radius of the flywheel and ω the angular velocity in radians per second. During discharge, kinetic energy is converted to electrical energy through a generator. Two possible configurations of flywheel energy storage systems which can be connected to the dc bus of an ASD are shown in Figure 5, where an AC motor and generator are assumed. A separate motor and generator can be used as shown in Figure 5(a) or the same machine can be used as a generator and motor along with a bi-directional AC/DC converter interface, as shown in Figure 5(b). The latter is the preferred arrangement since it requires less space than a system with a separate motor and generator and it provides a simple two terminal interface to the ASD.

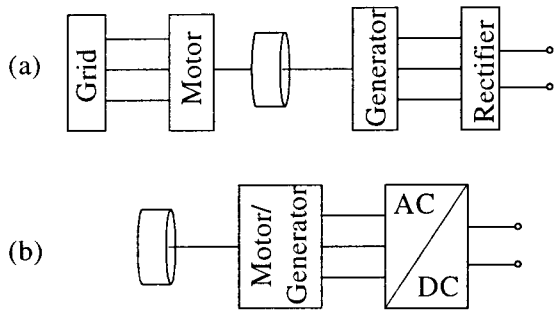


Figure 5 Flywheel energy storage systems with (a) a separate motor and generator and (b) a single motor/generator with a bi-directional AC/DC converter

This system is charged from the dc bus of the ASD as well as being discharged into the dc bus.

Regardless of the configuration used, the system has to be able to supply a regulated dc output voltage to the ASD, which can be achieved by using

1. a passive (diode bridge) rectifier and regulating the generator output voltage
2. a passive three phase rectifier and a DC/DC converter
3. an active rectifier
4. a dc generator

Extracting the energy from the flywheel in the form of dc energy has the advantage that, since the generator output voltage is rectified, the output frequency of the ac generator is of less concern and it becomes possible to extract energy from the flywheel to a lower rotor speed, increasing the deliverable energy compared to when the energy is used in an ac form.

There is still a concern about the safety of flywheels because of the expending of their energy in an uncontrolled manner when the enclosure of the flywheel is damaged. Some systems use flywheels made of composite materials, with high tensile strength and low density, while others still use low speed steel flywheels, because of the lower associated cost and safety concerns.

Most commercial flywheel systems are geared towards providing power till a backup generator can be started, therefore they are designed for 15 seconds of ride-through at full load. When applied to ASD ride-through of the most common sags, an investment is necessarily made in stored energy which will seldom be used.

2.3.2. Ultra-capacitors

Ultra-capacitors store electrical energy by accumulating and separating unlike charges. Extremely high capacitance and thereby energy density differentiates ultra-capacitors from standard capacitor technologies. For a simple plate capacitor with plate area A_p and distance d_p between the plates, the capacitance is

$$C = \frac{\varepsilon A_p}{d_p} \tag{2.2}$$

with ε the dielectric constant. High capacitance can therefore be achieved by using a plate material which has a very high surface area, such as carbon. Different material combinations are under development, e.g. a carbon composite electrode using an organic electrolyte and carbon/metal fiber composite electrodes with aqueous electrolyte.

Ultra-capacitor technologies can also be classified based on their internal structure. The cells of prismatic ultra-capacitors each have two plates and these cells are externally connected. Bipolar ultra-capacitor cells share plates between them, therefore a bipolar ultra-capacitor with n cells will have $(n+1)$ plates in total.

Because the square of the capacitor voltage is proportional to the energy stored, the voltage drops as the capacitor discharges, necessitating a DC/DC converter interface to the dc bus to regulate the bus voltage. The capacitor output current increases as the capacitor discharges, therefore a trade-off exists between the current rating of the DC/DC converter and the percentage of stored energy deliverable to the dc bus of the ASD.

2.3.3. Batteries

Batteries store and deliver electrical energy through reversible chemical reactions and many different kinds of batteries have been developed, e.g. lead-acid, Nickel-Cadmium, Nickel-metal hydride and lithium-ion, to list but a few. The newer battery technologies such as the Nickel-metal hydride and Lithium-based batteries are very expensive and since it is important to find a cost-effective energy storage system for this application, only two well established technologies, lead-acid and Nickel-Cadmium batteries, are considered. For the lead-acid batteries, both sealed lead-acid (SLA) and two advanced lead-acid battery technologies are considered. The aim for battery operation under voltage sag and momentary interruption ride-through operation is to maximize instantaneous power output while maintaining an acceptable voltage. However, advancement in battery technology has generally been in the direction of increased energy density rather than power density, as dictated by the electric vehicle industry. The requirements on batteries for ASD ride-through applications can be listed as :

- High discharge rate capability
- High power density
- Good float operation
- Low internal resistance
- Reliability
- Low maintenance

Battery discharge rates are given as a factor of C, , where C is the maximum constant current which can be delivered by the battery for one hour [13]. It is therefore equal to the capacity, in Ah, of the battery, although the battery may be rated for a duration of discharge different from one hour.

The characteristics of sealed lead-acid and vented sintered-plated Ni-Cd batteries are discussed in more detail and are summarized in Table 1.

2.3.3.1. Lead-Acid Batteries

Lead-acid batteries have traditionally been used for uninterruptible power supply (UPS) applications, currently holding two thirds of the world market for UPS and standby power applications [13]. The main advantages of sealed lead-acid batteries are their relatively low cost and their suitability to float operation. The expected float life of sealed lead-acid batteries is eight years at room temperature, decreasing as operating temperature increases [13]. They have low internal resistance which allows for high power delivery for short periods [14], therefore they can be used in engine starting applications.

Table 1 Summary of battery characteristics

Sealed Lead-Acid	**Vented Sintered-Plated Nickel-Cadmium**
Low cost	Expensive
Suited to float operation with expected float life of 8 years at room temperature	Expected cycle life of 500-2000, dependent upon depth of discharge
Low internal resistance	Low internal resistance
Moderately high power density Maximum discharge rate of 16C	High power density Maximum discharge rate of 40C
Flat discharge profile at low discharge rates, but flatness decreases as discharge rate increases; Coup de fouet transient phenomenon at high discharge rates	Very flat discharge profile at low discharge rates; flat at high discharge rates
No 'memory effect'	Exhibits 'memory effect'; reversible by a full discharge and overcharge, but requires taking battery out of service
Advisable to temperature compensate charging voltage for constant voltage charging	Require a temperature controlled charger for constant voltage charging
Can be fast charged	Can be fast charged
Used for engine starting	Used for aircraft turbine and diesel engine starting

However, as the discharge rate increases, the plateau of the voltage discharge profile is lowered, shortened and its slope is increased, i.e. the flatness of the voltage discharge profile is decreased. At high discharge rates the voltage also exhibits the *coup de fouet* (whipcrack) transient phenomenon whereby the voltage dips below the plateau shortly after the load is applied [14]. It would therefore necessitate a converter to interface with the dc bus in order to regulate the dc bus voltage. The charging voltage should be temperature compensated to prevent thermal runaway and to ensure adequate charging at low temperature [13].

2.3.3.2. Nickel-Cadmium Batteries

Nickel-Cadmium batteries are more expensive than lead-acid batteries, but offer very high discharge rate capabilities and a flat voltage discharge profile even at high discharge rates. Vented sintered-plated Nickel-Cadmium batteries are used for aircraft turbine and diesel engine starting [13], which are very demanding applications. They are capable of delivering very high currents because of low internal resistance. They can also be fast charged if necessary and have a cycle life of 500 – 2000, depending on the depth of discharge.

Their major disadvantage is cost, since they are considerably more expensive than sealed lead-acid batteries. They also require a temperature controlled charging system, to minimize water usage and therefore maintenance. The objective under constant potential charging is to supply the overcharge current to the battery that it would have required at room temperature. Without temperature compensation, the overcharge current will typically increase by approximately 60% for a 10°C rise in cell temperature [13].

Ni-Cd batteries also exhibit a 'memory effect' which manifests itself as an output voltage depression upon discharge. It is a result of charging after repetitive shallow discharges, but is completely reversible by a complete discharge and overcharge of the battery [13]. This however requires the battery to be taken out of service, i.e. increased maintenance.

2.3.3.3. Advanced Lead-Acid Batteries

Standard sealed lead-acid and Nickel-Cadmium batteries have the advantage of being mature energy storage technologies, but they require a high level of maintenance and have a limited lifetime. ASD ride-through requires very high discharge rates and although Ni-Cd batteries exhibit a more flat voltage profile at high discharge rates, their high cost puts them at a disadvantage for this application which demands a cost-effective solution.

The performance of sealed lead-acid batteries can be improved by using pure lead-tin rather than lead alloys for the electrodes. The pure lead electrodes resist corrosion, even under severe conditions such

as high temperature, resulting in a significantly longer lifetime than standard lead-acid batteries. A higher power density and specific power under high discharge rates can also be achieved as a result. The discharge voltage profile of these batteries are similar to Nickel-Cadmium batteries because of their low internal resistance [50].

A recent development in lead-acid battery technology, Thin Metal Foil (TMF) batteries, holds promise for ride-through applications [47]. Standard lead-acid chemistry is utilized, but by using extremely thin metal foil plates, a very low internal resistance is achieved, which is important at high discharge rates. This produces batteries capable of delivering flat voltage profiles at very high discharge rates, up to 60*C*, thereby achieving very high power densities. The power density of this battery technology is about twice that of the pure lead-tin batteries, but these batteries are not yet in full production and face some quality control challenges in the manufacturing process.

2.3.4. Comparison

Due to the fast changing nature of energy storage technologies, specific products are compared in Table 2 at their current state of development. Table 2 is not meant to be an exhaustive list of available ride-through systems, but rather details products which are representative of different energy storage technologies. The information was gathered from manufacturers' data sheets and through personal communication with manufacturers.

In some cases, a ride-through system, incorporating the energy storage element(s) and interface circuit to provide a regulated dc output voltage, is available and known parameters are presented. Under this category, two commercially available flywheel systems, one using a low speed steel flywheel [39][40] and one a high speed composite flywheel [41][42], and a system based on prismatic ultra-capacitors [43][44] are included. Other technologies show promise for this application, but have not yet been commercially packaged. For these technologies, a reasonable projection is made of what the parameters of a ride-through system incorporating the technology would be. In this category projections of systems using bipolar ultra-capacitors [45][46], Thin Metal Foil lead-acid batteries [47][48] and pure lead-acid batteries [50] are included. Both the prismatic and bipolar ultra-capacitors use a carbon composite electrode and an organic electrolyte.

It is important to note that the characteristics listed in Table 2 are for the integrated systems, not only the energy storage components. The maximum constant power output is the maximum power which can be output continuously for the maximum duration of discharge. Systems with ratings ranging from 100kW to 240kW are considered. The maximum duration of discharge is defined as the time it takes the energy storage element to discharge to its minimum voltage or rotational speed while delivering maximum constant output power.

Table 2 Comparison of available and conceptual energy storage systems for ASD ride-through

System qualities	Units	Low speed flywheel	High speed flywheel	Prismatic ultra-capacitors	Bipolar ultra-capacitors†	TMF Pb-acid batteries†	Pure lead-acid batteries†
Maximum constant power output	kW	240	200	100	100	100	100
Maximum duration of discharge	sec.	13.5	7.7	5	5	15	15
Current system retail cost (compare $/kW)		Low	High	High	Very high	Low	Very low
Cost trend		Decreasing slowly	Decreasing fast	Decreasing fast	Decreasing fast	Decreasing	Stable
Nominal output voltage	V	550	800	585	585	585	585
Output voltage regulation during discharge	%	1	5	1	1	1	1
Initial stored energy	MJ	4.25	2.3	1.2	4.8	5.9	18
Energy delivered to ASD (% of stored energy)	%	76	67	42	11	25	8
Standby losses (% of rated output power)	%	1	0.5	0.2	0.5	0.5	0.1+
Discharge losses (% of rated output power)	%	7	12	25	96	12	10+
Weight	kg	1,275	200	475	445	345	445
Volume	m^3	1.9	0.3	0.8	1.1	0.8	0.8
Footprint	m^2	1	0.5	0.5	1	0.5	0.5
Specific power	W/kg	188	1,000	211	225	290	225
Power density	kW/m^3	126	740	125	100	125	125
Response time	ms	<4	3	<4	<4	<4	<4
Minimum recharge time (interface limit)	min.	15 - 20	1	20	20	20	20
Expected life	years	20	10 – 20	10	10 – 15	3 - 5	8 – 10
Expected life	cycles	>150,000	>100,000	100,000	10,000 – 50,000	>300	>300
Operating temperature range	°C	-20 / 40	-20 / 50	0 / 40	0 / 40	0 / 40	0 / 40
Level of maintenance		Low	Low	Minimal	Minimal	High	High
Maintenance intervals		3 months	6 months	5 years	5 years	3 to 5 years	5 years

† System specifications estimated

At lower output power, the duration of discharge will be longer. The high speed flywheel and ultra-capacitor systems can provide ride-through for the most common sags and interruptions, which have been shown to mostly last less than 3 seconds. Ride-through until a motor-generator set can be started is provided by the low speed flywheel and battery systems.

The current and projected system retail cost in the near future refer to the initial capital investment required by the customer and is compared on a $/kW basis. Currently the least expensive systems are the advanced lead-acid battery and low speed flywheel systems. The pure lead-acid battery system cost is stable, with only a marginal decrease in cost expected in the future, a slow decrease in cost is expected for the low speed flywheel system and a further decrease in cost is also predicted for the TMF battery system. The ultra-capacitor and high speed flywheel technologies are more expensive at present, with the bipolar ultra-capacitor system the most expensive, although a fast decrease in retail cost is predicted for all three of these systems as production volume increases.

The output voltage is user adjustable for all the systems, but in general it is desirable to have the output voltage no more than 10% lower than 650V for use with a passive rectifier or 800V for use with an active rectifier. The output voltage is a function of the design of the interface circuit and is not limited by the energy storage technology. Currently only the high speed flywheel system has an interface circuit with the capability to output a high enough voltage for use with an active rectifier. For the low speed flywheel system, the current nominal output voltage is 15% lower than 650V and there are applications which will not operate satisfactorily at such a low dc bus voltage. Output voltage regulation during discharge is given as a percentage of the nominal dc bus voltage.

Figure 6 is a graphical representation of the distribution of stored energy during discharge. Only a part of the initial stored energy can be delivered to the dc bus of the ASD, because not all the stored energy can be extracted and there are also losses associated with the discharge process.

The initial stored energy is listed in Table 2 for the system at its fully charged state. The energy delivered to the dc bus of the ASD is listed for the condition where maximum output power is supplied for the rated duration of discharge at that power level and is listed as a percentage of the initial stored energy.

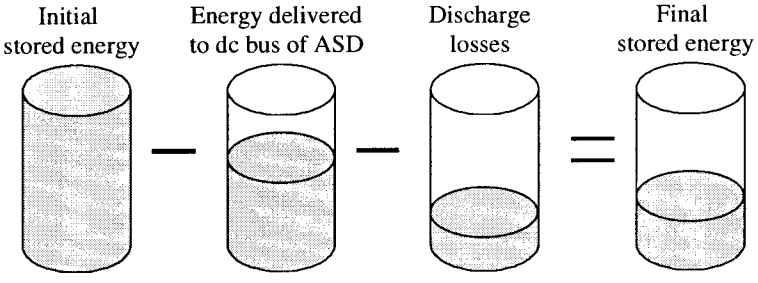


Figure 6 Distribution of stored energy during discharge

The flywheel systems are able to deliver the highest percentage of stored energy, followed by the prismatic ultra-capacitor and then the TMF battery system. The bipolar ultra-capacitor system and the pure lead-acid battery system deliver the lowest percentage of stored energy at maximum output power.

Standby losses are expressed as a percentage of the maximum constant power output of the system. All systems under consideration have low standby losses, which is of great importance in ride-through applications where the energy storage system will spend most of its life in a standby mode, since the standby losses contribute to the cost of ownership of the system. For example, a system which dissipates 1kW on standby will dissipate 24kWh per day. At a cost of $0.15/kWhr, the standby power to the system will cost $13,140 over a period of ten years.

Average discharge loss is calculated by dividing the energy lost during the discharge, i.e. the difference between the initial stored energy and the sum of the final stored energy and energy delivered to the ASD, by the duration of the discharge. It is listed as a percentage of the maximum constant output power of the system. Discharge losses are highest for the bipolar ultra-capacitor system due to high internal resistance and significantly lower for the prismatic ultra-capacitor system. The flywheel and battery systems have the lowest discharge losses, i.e. highest discharge efficiency.

The weight and volume entries refer to the entire system, not only the energy storage elements, and are used to calculate the specific power and power density of the system. These are important parameters for ASD ride-through since it is desirable to have a system capable of delivering the desired output power when needed while taking up the minimum amount of space and weighing as little as possible. The packaging for both the flywheel systems are able to house one or two rotors and the data listed here is for a single rotor system. For a double rotor system the specific energy and power density will be higher.

The high speed flywheel system has very high specific power and power density. The system exhibiting the next highest specific power, the TMF battery system, has a specific power three times less and a power density six times less than the high speed flywheel. The pure lead-acid battery, low speed flywheel and ultra-capacitor systems have the same power density as the TMF battery system.

Response time refers to a step response from standby mode to maximum power output and all of the systems respond fast enough for application to ASD ride-through. Minimum recharge time is the shortest time in which the energy storage elements can be recharged from its minimum voltage or rotational speed to the nominal. The minimum recharge time for the system ultimately depends on the design of the charger in the interface circuit and does not necessarily reflect limits of the energy storage technologies themselves.

Only one system, the high speed flywheel system, has opted for a short recharge time, but it may not be possible to take advantage of this in an ASD ride-through application because the flywheel system is recharged from the dc bus. The rectifier of the ASD therefore has to supply both the load power to the inverter and recharge power to the flywheel system and fast recharge will only be possible as long as the rectifier rating is not exceeded. Due to the nature of the application, with the system spending most of its

time in standby mode with only occasional discharges, fast recharge is not a requirement for this application.

The expected life at room temperature is listed in years as well as number of discharge cycles and the operating temperature range refers to the ambient temperatures the system can operate in. Both ultra-capacitor and flywheel systems have a long expected life, in years and cycles, while the battery systems have a relatively short lifetime, after which the batteries will need to be replaced. The lifetime of the system depends on its operating temperature, with the system lifetime decreasing as the operating temperature increases.

The TMF lead-acid battery systems need battery replacements every three to five years and a periodic discharge of the batteries is required, which translates to the highest maintenance needs of these systems. The pure lead-acid battery system also requires replacement of batteries, but the lifetime of the batteries is significantly higher than the TMF lead-acid batteries. The low speed flywheel system needs minor maintenance, such as replacement of air filters every few months and replacement of mechanical bearings every 7 to 12 years. The high speed flywheel system has an auto-lubricator which needs to be checked every 6 months and magnetic bearings will be available in the future. The ultra-capacitor systems have minimal maintenance needs.

2.3.5. Conclusions

Three viable energy storage technologies were investigated. Some of these technologies have commercially available, or soon to be available, ride-through systems and for other technologies, estimates were made of what the specifications for such a ride-through system would be. An analysis of how these systems perform relative to the requirements set forth for application to ASD ride-through has been presented.

Short term energy storage is an emerging market with many technologies and systems being introduced and there are opportunities for retrofit of existing drives as well as inclusion in new drives. The bipolar ultra-capacitor and TMF lead-acid battery systems were found to not be suitable for this application because of the very high cost of the bipolar ultra-capacitor system and the high maintenance requirements and short lifetime of the TMF lead-acid battery system.

A qualitative summary of the qualities of the remaining four systems, the two flywheel systems, the pure lead-acid battery and prismatic ultra-capacitor energy storage systems are presented in Table 3.

The pure lead-acid battery system requires extensive maintenance compared to the other systems which translates to high cost of ownership despite the low retail cost for the system. The main disadvantage of the flywheels systems is the safety concern, especially in an industrial setting.

The prismatic ultra-capacitor system has the advantages of minimal maintenance requirements and long lifetime. The costs are still high, but the operating cost will be lower than battery or flywheel systems because of the low maintenance requirements and retail costs are expected to drop in the future.

Table 3 Qualitative summary of attributes of ASD ride-through systems

System qualities	Low speed flywheel	High speed flywheel	Pure lead-acid batteries	Ultra-capacitors
Availability	Commercial	Prototype / Commercial	Conceptual	Commercial
Cost (compare $/kW)	Low, decreasing slowly	High, decreasing fast	Very low, stable	High, decreasing fast
Power level/unit	Systems ranging from 160kW / 15 sec to 800kW / 5 sec	Systems ranging from 50kW / 20 sec to 200kW / 7.5 sec	100kW modules, can be paralleled	100kW modules, can be paralleled
Duration of discharge			15 sec	5 sec
Advantages	Long lifetime Low cost	Very high power density & specific power Long lifetime	Very low cost High specific power	Long lifetime Minimal maintenance
Concerns	Low specific power Safety concerns Maintenance	High cost Safety concerns Maintenance	Limited lifetime Cost of ownership Maintenance	High cost Low power density

2.4. Interfacing an ASD and an Energy Storage System

2.4.1. Introduction

Regardless of the energy storage technology decided on, it remains to choose an appropriate interface circuit between the ASD and the energy storage elements. A matrix of the possible interface configurations between energy storage elements and an ASD is shown in Table 4. The three energy storage technologies considered are batteries, ultra-capacitors and flywheels.

The *source type* refers to whether the energy storage elements output power in AC or DC form. Batteries and ultra-capacitors have a DC output voltage and where a flywheel system is referred to, it is assumed that an ac generator is integrated with the flywheel, therefore it is classified as an AC type source. The *interface* to the ASD can either be a direct connection (no interface circuit) or some type of power electronic converter. The interface circuit can be connected to either the dc bus or rectifier input of the ASD, as long as a transfer switch is provided, with the input line reactor of the rectifier considered a part of the rectifier.

In some cases the connection to the rectifier input can only be made if the ASD has an active rectifier and/or a transfer switch between the grid and the energy storage system is provided. From Table 4 it can be seen that batteries can be connected through a diode to the dc bus if they exhibit a very flat voltage profile during discharge, but this is an unrealistic requirement on most available battery technologies under the high power discharge conditions required by this application and no control over the charging current of the batteries is possible with a diode connection.

Table 4 Matrix of possible interface circuits between the energy storage elements and ASD

Source type	Source	Connected to	Interface	Rectifier	Transfer switch
DC	batteries	dc bus	diode	either	no
DC	batteries	dc bus	DC/DC	either	no
DC	batteries	rectifier input	direct	active	yes
DC	batteries	rectifier input	DC/AC	either	yes
DC	ultra-capacitors	dc bus	DC/DC	either	no
DC	ultra-capacitors	rectifier input	direct	active	yes
AC	flywheel	dc bus	AC/DC	either	no
AC	flywheel	rectifier input	direct	passive	yes
AC	flywheel	rectifier input	direct	active	yes
AC	flywheel	rectifier input	AC/AC	either	yes

Usually a DC/DC converter interface is employed to regulate the dc bus voltage and control the charging current and it allows for the inclusion of protection features in the converter.

Batteries can also be connected to the rectifier input in several different ways. If the ASD has an active rectifier and a transfer switch is provided, the batteries can be connected directly to the rectifier and the three inherent boost converters in the active rectifier can then be used to boost the battery voltage to the reference dc bus voltage. This configuration is discussed in more detail later. If a DC/AC converter interface is used, batteries can also be connected to the rectifier input with an ASD with a passive rectifier, as long as a transfer switch is provided.

The state of charge of an ultra-capacitor bank is proportional to the square of the ultra-capacitor bank voltage and therefore a DC/DC interface is required to connect it to the dc bus. For an ASD with an active rectifier and a transfer switch, the ultra-capacitors can be connected directly to the rectifier input.

A flywheel can be connected to the dc bus through an AC/DC converter. It can also be directly connected to the rectifier input or through an AC/AC converter, as long as a transfer switch is provided. For a direct connection, if the ASD has an active rectifier, the frequency and voltage magnitude at the output of the flywheel are allowed to vary, but with a passive rectifier, only the output frequency is allowed to vary.

Since batteries are the traditional energy storage elements used for dc bus voltage regulation in UPS applications, an overview of battery interface circuits will be given in section 2.4.2. The same basic interface circuits can be used for ultra-capacitors as for batteries, since they are both DC type energy storage technologies, although the charging requirements may vary and generally the boost factor required for ultra-capacitors will be higher than that required for batteries. A bi-directional DC/DC converter which can be used to interface an ultra-capacitor or battery bank to the dc bus of the ASD is

discussed in section 2.4.3. The direct connection of a battery or ultra-capacitor bank to the rectifier input of an ASD with an active rectifier and a transfer switch between the grid and the energy storage system is discussed in more detail and simulation results of this interface are presented in section 2.4.4.

2.4.2. Battery Interface Circuits

It is standard practice to interface the battery bank to the dc bus of the ASD and there are several ways of doing this. If the battery bank is a high voltage bank, i.e. the batteries are stacked in series until the desired dc bus voltage is reached, it can be connected directly or through a diode to the dc bus. A direct connection to the dc bus has the disadvantage that the battery bank is subjected to the ripple that appears on the dc bus voltage and with a diode connection, the battery bank voltage has to be lower than the dc bus voltage in order to ensure that the battery is connected electrically to the bus only when the rectifier cannot supply enough power to regulate the bus voltage to the desired value. For ASD applications this voltage level may be unacceptably low and therefore it is standard practice to provide a power electronic interface between the battery bank and dc bus to regulate the dc bus voltage. The power electronic interface needs to include a circuit to recharge the battery bank after a discharge during a sag or momentary interruption condition and the charging circuit can be connected to either the AC grid or the dc bus of the ASD. The charge and discharge circuits can be combined in a bi-directional DC/DC converter, as will be discussed in section 2.4.3.

In the case of a low voltage battery bank where the battery bank voltage is significantly lower than the dc bus voltage, a boost converter is needed to interconnect the battery bank and dc bus. A separate charger can be connected to the battery bank, as in the case for a high voltage battery bank, but it is often more convenient to use a bi-directional DC/DC converter to perform the charging and discharging functions. A trade off exists between the complexity of the interface to the dc bus, the factor by which the output current of the battery bank is increased as a result of a boost converter, and the number of batteries required.

Charge equalization among the batteries is a problem and the series connection of batteries also has an inherent reduced reliability [18], because if one battery fails, the whole string of batteries it is located in, has to be taken out of use. When batteries are connected in series in order to achieve a higher battery bank output voltage, the charge and hence voltage may be unequally distributed because of mismatches in the batteries due to manufacturing tolerances and/or ageing and differences in the operating temperature of the batteries [19]. This unbalance increases with time as low voltage batteries charge less effectively, resulting in the bank being charged at less than its nominal capacity. The charge on the low voltage batteries can be increased by charging the bank at a higher voltage, but this will overcharge the high voltage batteries and decrease their expected life.

The traditional way of equalizing the battery charges is by an extended overcharging of the battery bank. This is referred to as a *passive* equalization technique, since the bank has to be taken off line.

Recently attention has been given to *active* equalization procedures which can be implemented with the bank online. It has been proposed to use power converters to either divert charge from high voltage batteries [20] or to send charge selectively to low voltage batteries. Some problems with these procedures are that they need precise control and they can only be employed once at least one battery is fully charged. Recently an active procedure was proposed which does not suffer from these two disadvantages and operates at very low loss [19]. The concept is illustrated in Figure 7 for four batteries.

For n batteries connected in series, $n-1$ capacitors are needed. By connecting the capacitors alternately between two adjacent batteries, charge is exchanged between these two batteries. This eventually leads to balanced charge on all the batteries, independent of the battery technology used, number of batteries and other design parameters, although the speed with which the charge is equalized depends on design parameters such as the capacitance and switching frequency. MOSFETs are used to realize the single pole double throw switches, since the losses are low and a high switching frequency is needed.

The manufacturer of the pure lead-tin lead-acid batteries, as discussed in paragraph 2.3.3.3, claims that no charge equalization will be necessary with their batteries due to tight manufacturing tolerances as well as the batteries' ability to withstand corrosion at high operating temperatures.

2.4.3. Bi-Directional DC/DC Converter

As discussed for battery interface circuits, where a boost converter is used to interface the energy storage to the dc bus, the charging circuit can be incorporated with the boost converter, resulting in a bi-directional DC/DC converter. This circuit can be used for a battery or ultra-capacitor energy storage system. One possible implementation of this bi-directional converter is shown in Figure 8 [18][17] with an ultra-capacitor bank modelled as an ideal capacitor C_{es} and a series resistance R_{es}.

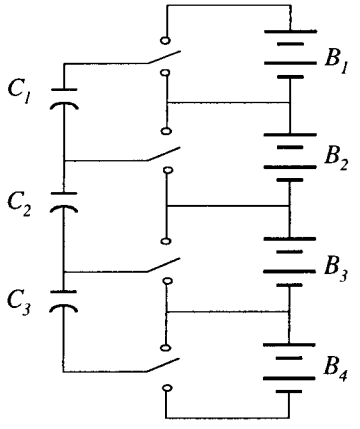


Figure 7 Diagram of switched capacitor equalizer

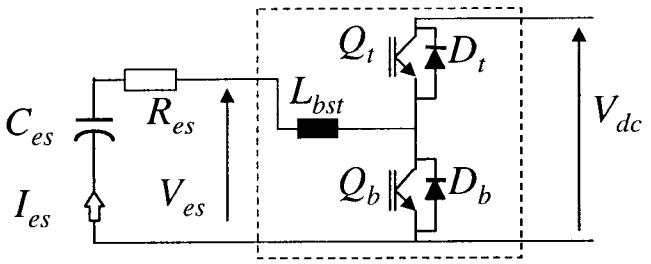


Figure 8 Operation of bi-directional DC/DC converter

During battery bank discharge, D_t and Q_b, together with inductor L_{bst} and the bus capacitance C_{dc}, form a boost converter. For battery bank charging, Q_t is switched and D_b operates in conjunction with it to form a buck converter. This implementation requires a minimum of passive elements, although neither the buck nor boost converter can be optimized, since the passive components are shared.

The boost converter components D_t and Q_b must be rated to carry the full discharge current, but since power is drawn from the dc bus for charging, the charging current is limited by the rectifier and therefore Q_t and D_b can be of a much lower current rating. This circuit is very simple and effective and because of the intermittent use of the discharge circuit, resulting in low average discharge losses, and the low charging power required, the circuit need not be complicated by snubbers or soft switching circuits.

2.4.4. Rectifier as AC/DC and DC/DC Converter

Ultra-capacitors and batteries can also be connected directly to the rectifier input of an ASD with an active rectifier when a transfer switch between the energy storage system and the grid is provided, as shown in Figure 9 for an ultra-capacitor bank. During normal operation, the rectifier is used as an AC/DC converter, but when a deep voltage sag or momentary interruption occurs, which the active rectifier by itself cannot provide ride-through for, the rectifier input is transferred from the grid to the energy storage system and the rectifier is controlled to operate as a DC/DC converter, using the three inherent boost converters in the rectifier.

This interface circuit was simulated in *EMTDC*, an electromagnetic transients program with a graphical user interface, with a constant power load and an ultra-capacitor bank for energy storage. The *EMTDC* schematics are included in Appendix A. The active rectifier regulates the dc bus voltage to a reference value by controlling the rectifier input current. For a constant power load on the inverter, the rectifier will increase the rectifier input current as the grid voltage drops in order to deliver constant power to the inverter. An active rectifier can therefore regulate the dc bus voltage under voltage sag conditions as long as the required rectifier input current does not exceed the current rating of the rectifier [12]. The inverter and rectifier are current controlled using simple hysteresis current controllers.

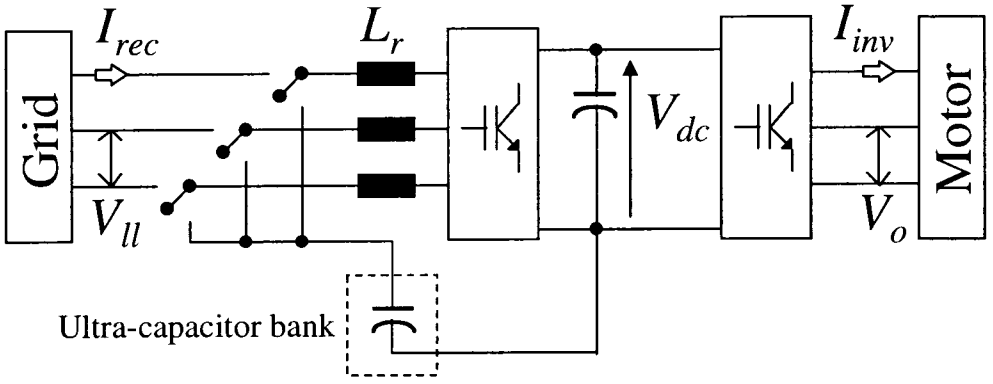


Figure 9 Rectifier used as AC/DC or DC/DC converter

For the simulations, the nominal grid voltage is 480V line-to-line, the reference dc bus voltage is 800V, the inverter load is 100kW, the dc link capacitance is 10mF and the rectifier input line reactor is 3.4mH. The rectifier input current is limited to 230A, which will allow the rectifier to provide ride-through of sags up to 42% with a 100kW load, assuming that the efficiency of the rectifier and the inverter is 95%. The ultra-capacitor bank is made up of nine 56V ultra-capacitor modules connected in series and the sizing of the ultra-capacitor bank is discussed in section 2.4.5.

The transfer switch is transferred from the grid to the ultra-capacitor bank when the dc bus voltage drops below 85% of nominal, i.e. 680V, and the rectifier regulates the dc bus voltage to 95% of nominal, i.e. 760V, with the ultra-capacitors connected to the rectifier input. The rectifier input is reconnected to the grid when the grid voltage returns to a value higher than 90% of nominal, i.e. 432V.

Simulation results are presented in Figure 10 with a 50% sag introduced at t = 0.05sec, which is removed at t = 0.35sec, and another sag of 30% introduced at t = 0.63sec. The rectifier is able to provide ride-through for the 30% sag, but not the 50% sag and the transfer switch connects the ultra-capacitors to the rectifier input during the 50% sag. Trace (a) shows the dc bus voltage response and trace (b) shows the rectifier input current.

As the dc bus voltage drops below 680V, the transfer switch connects the rectifier input to the ultra-capacitors and the rectifier changes from AC/DC conversion mode to DC/DC conversion mode. The results in Figure 10 show the successful transition of the rectifier between the two conversion modes. The drop in the ultra-capacitor bank voltage, shown in trace (c), is not significant due to the short time (0.25 sec) during which it delivers power to the ASD and therefore the simulation result of a 50% sag of a longer duration is shown in Figure 11 in which the ultra-capacitor bank voltage response shows a more substantial drop. Trace (d) in Figure 10 and Figure 11 shows the inverter output power and rectifier input power.

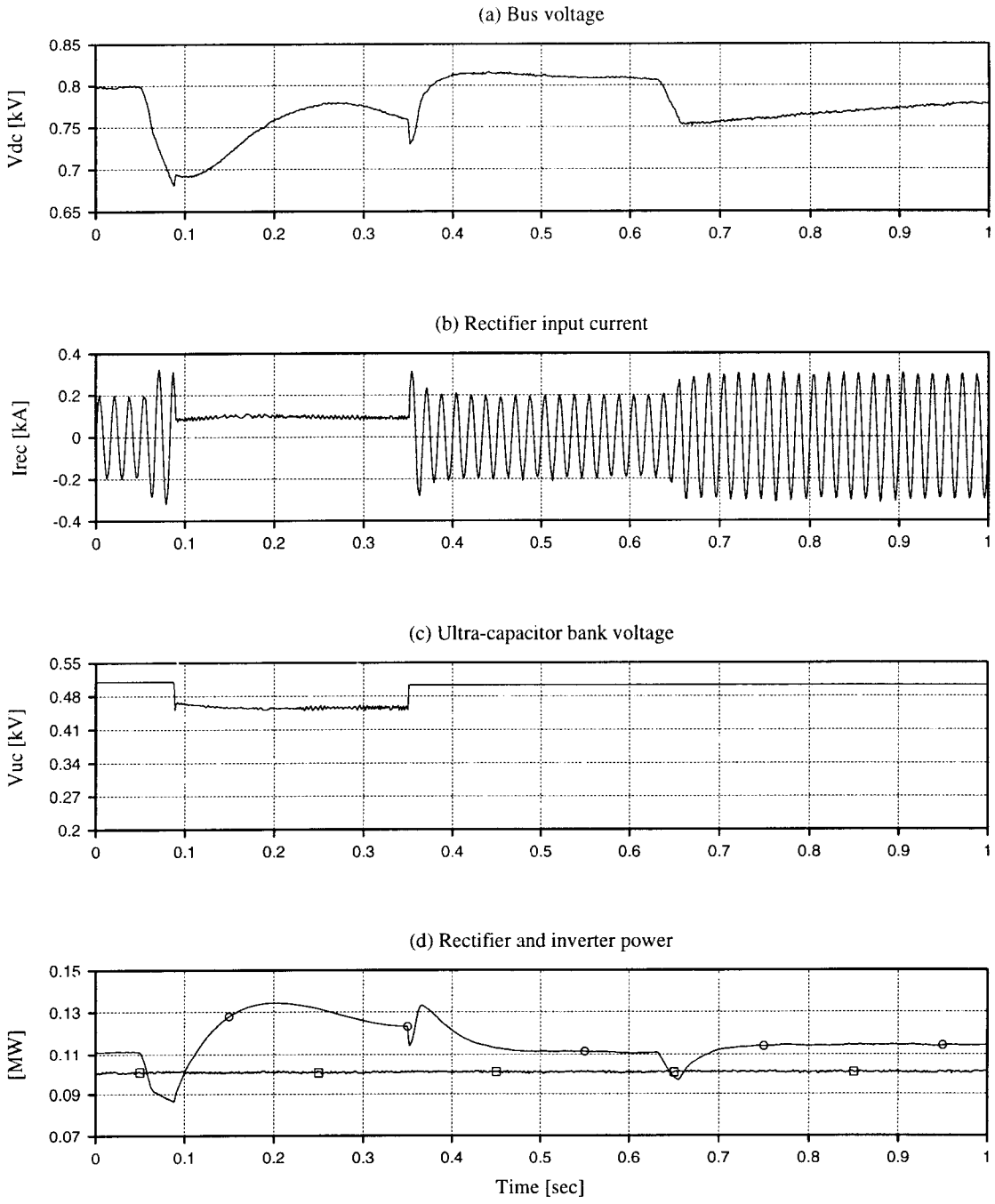


Figure 10 Simulation results of rectifier performing AC/DC and DC/DC conversion

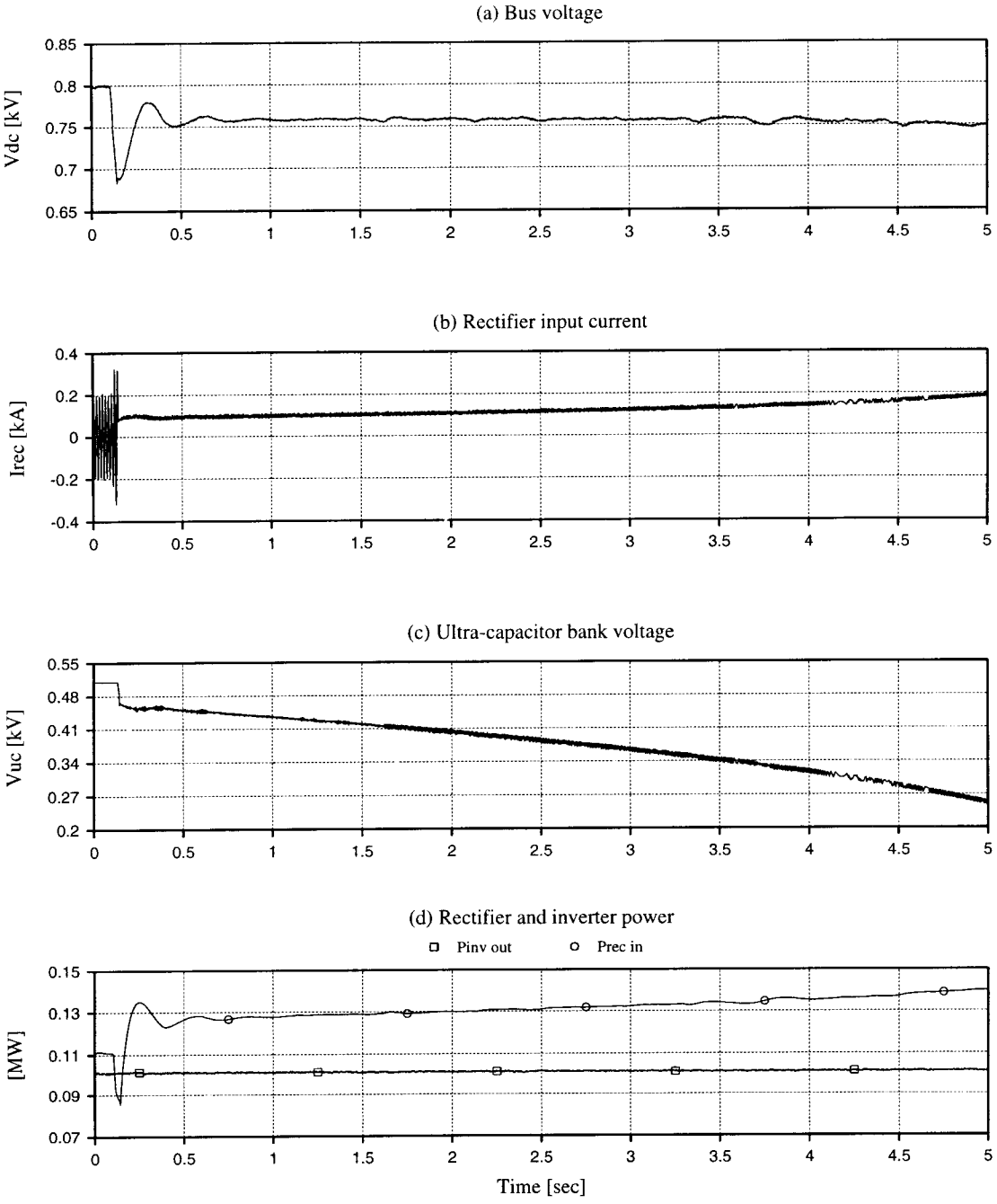


Figure 11 Simulation results of rectifier performing AC/DC and DC/DC conversion

The rectifier input power is higher during DC/DC conversion than AC/DC conversion, although the inverter output power stays constant. This is because of the differences in the two conversion processes and this is expanded upon in Appendix B where the rectifier losses are calculated in detail for a rectifier with 1200V/200A IGBT devices [34] with the rectifier input power equal to 111kW.

It was found that for AC/DC conversion under normal conditions, i.e. with the rectifier input voltage equal to 480V, the total losses in all three of the rectifier modules are approximately 1.3% of the input power, i.e. 1.4kW, and when the maximum current of 230A is drawn, the total losses are approximately 1.9%. The total losses for DC/DC conversion increase from 1.5% to 1.8% as the duty ratio and input current increase. This rise in rectifier losses can be seen in Figure 11(d) as the ultra-capacitor bank current increases. With the rectifier derated to provide ride-through for sags of up to 42%, the total losses in the rectifier in the worst case condition for DC/DC conversion are less than the total losses under the worst case condition for AC/DC conversion. However, all the losses for DC/DC conversion have to be absorbed by three IGBTs and diodes of the rectifier, whereas the total losses for AC/DC conversion are absorbed by all six IGBTs and diodes. The junction temperatures of the diodes and IGBTs in the modules were calculated in Appendix B and it was found that the diode junction temperatures under the worst case conditions for AC/DC conversion are 8°C higher than for the worst case DC/DC conversion conditions. The IGBT junction temperatures under the worst case conditions is 6 °C higher for DC/DC conversion than for AC/DC.

Therefore an active rectifier designed for AC/DC conversion which would provide ride-through for sags of up to 42% with a 100kW load, i.e. the maximum rectifier input current is 230A, can be used for DC/DC conversion with a maximum boost factor of 3 if the IGBT junction temperatures can be allowed to rise another 6 °C.

The *EMTDC* simulations show a greater increase in losses for DC/DC conversion and the reason for this may be that the current regulator implemented in *EMTDC* is a hysteresis regulator with varying switching frequency, which increases the switching losses in the rectifier.

2.4.5. Ultra-capacitor Sizing

In this section the sizing of an ultra-capacitor bank to provide ride-through for an ASD with a 100kW load is discussed for a bi-directional DC/DC converter interface to the dc bus, for a passive and active rectifier, as well as for an ultra-capacitor bank connected to the rectifier input of an ASD with an active rectifier.

It is assumed that 56V ultra-capacitor packs from Maxwell Technologies [44] with a rated capacitance of 95F and rated equivalent series resistance of 25mΩ are used, and it is necessary to determine how many of the 56V ultra-capacitor packs are required to provide the load power of 100kW for 5 seconds for the different interface circuits. Assuming an efficiency of 95% for the rectifier, inverter

and boost converter i.e. $\eta_{rec} = \eta_{inv} = \eta_{bst} = 0.95$, the load step applied to the fully charged capacitor bank with an inverter load of 100kW, is

$$P_{es} = \frac{P_{inv,out}}{\eta_{rec}\eta_{inv}} = \frac{P_{inv,out}}{\eta_{bst}\eta_{inv}} = \frac{100kW}{0.95\times0.95} \approx 111kW \ . \qquad \textbf{(2.3)}$$

It is assumed that the dc bus voltage is regulated to 95% of nominal, i.e. 760V for an ASD with an active rectifier and 585V for an ASD with a passive rectifier, by the ultra-capacitor interface circuit. The minimum voltage across the ultra-capacitor bank is determined by the maximum boost factor of the rectifier or boost converter and if the boost factor is limited to three, the minimum terminal ultra-capacitor bank voltage is 253V for an active rectifier and 195V for a passive rectifier. It should also be ensured that the maximum current the capacitor bank needs to supply does not exceed the rated current of 600A. In order to calculate how many 56V ultra-capacitor packs are needed to deliver 111kW for 5 seconds at the prescribed voltage, a program was written in MATLAB and the program listing is included in Appendix C. The ultra-capacitor bank voltage, capacitor discharge current and percentage of stored energy delivered at the output of the ultra-capacitor bank are shown in Figure 12 for eight and nine packs respectively.

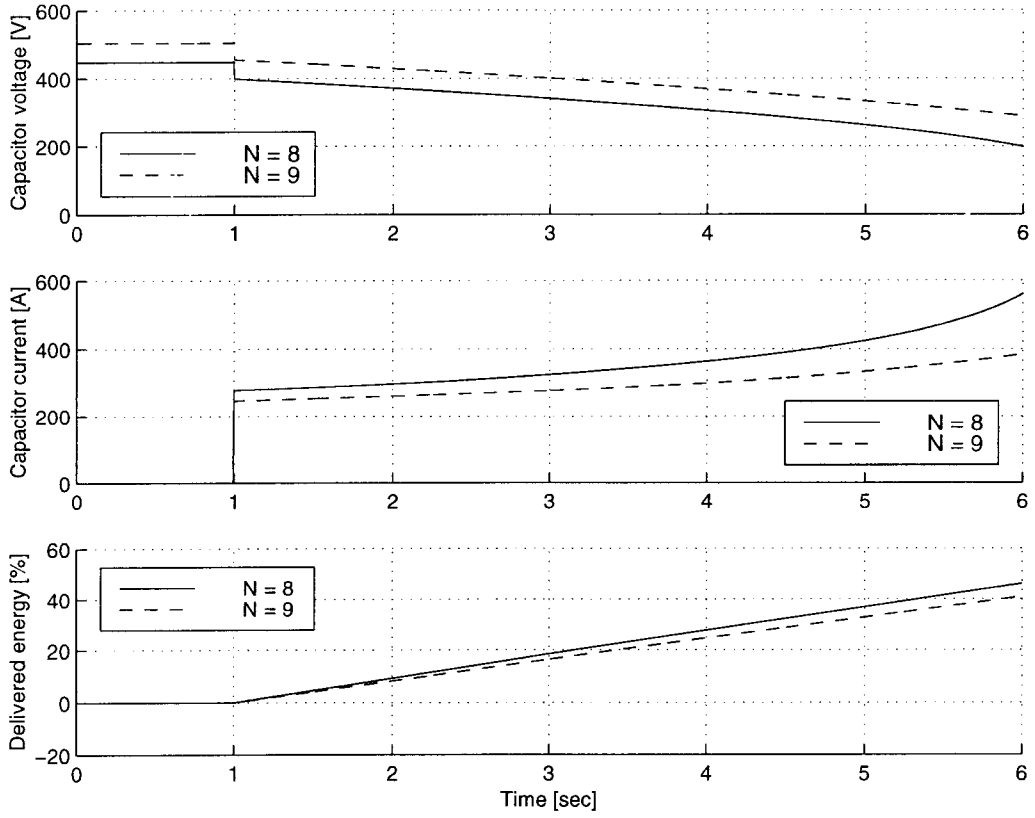


Figure 12 Simulated discharge curves of bank of ultra-capacitors with constant power load

The ultra-capacitors packs are modelled as an ideal capacitor with a capacitance of 96F in series with a 22mΩ resistor in MATLAB. It was found that eight 56V ultra-capacitor packs connected in series discharge to 198.5V in 5 seconds and therefore it would be suitable for an ASD with a passive rectifier, but nine 56V packs which discharge to 289V in 5 seconds are required for an ASD with an active rectifier.

2.4.6. Conclusions

Regardless of the energy storage technology chosen, a suitable interface circuit between the ASD and the energy storage system has to be decided upon. The possible interface configurations for flywheel, battery and ultra-capacitor energy storage systems were presented and interface circuits for batteries and ultra-capacitors were discussed in more detail.

A novel interface circuit was presented which allows for the direct connection of batteries or ultra-capacitors to the rectifier input if an active rectifier and transfer switch between the grid and energy storage system are provided. The rectifier is used for both AC/DC conversion during normal operation and for DC/DC conversion during a deep sag or momentary interruption. The advantage of this configuration is that it eliminates the need for additional power electronics when interfacing the ultra-capacitors with the ASD. It was also shown that the losses during DC/DC conversion are higher than during AC/DC conversion with nominal input voltage. The rectifier will therefore have to be derated in order to allow for DC/DC conversion. If the rectifier is already derated in order to allow for ride-through of sags up to 40%, it was shown that the total losses for DC/DC conversion are less than the total losses for AC/DC conversion at the maximum rectifier current.

This configuration requires a transfer switch and enhanced control features for the rectifier to be able to operate in two modes and therefore it does not lend itself to retro-fit applications. It is a very promising topology, but will require a completely new design of the rectifier as well as the design of a suitable transfer switch. This falls outside the scope of this thesis and the design was therefore not pursued any further.

2.5. Experimental Evaluation of Ultra-capacitors

The two ultra-capacitor technologies considered for application to ASD ride-through, prismatic and bipolar ultra-capacitors, were evaluated experimentally. The cells of prismatic ultra-capacitors each have two plates and these cells are externally connected, while bipolar ultra-capacitor cells share plates between them, therefore a bipolar ultra-capacitor with n cells will have $(n+1)$ plates in total. The equivalent series resistance of bipolar ultra-capacitors are higher than that of prismatic ultra-capacitors because of their differences in structure and therefore bipolar ultra-capacitors have much higher internal losses than prismatic ultra-capacitors. Cell balancing is done for the prismatic ultra-capacitor, but not for

the bipolar ultra-capacitor, which puts the bipolar ultra-capacitor at a disadvantage since cell balancing can prolong the life of the ultra-capacitor and the balancing circuit can also give an early warning of impending cell failure. The ratings and dimensions of the two ultra-capacitors which were evaluated are listed in Table 5.

The first step in the experimental evaluation was to verify the rated capacitance of the ultra-capacitors and to determine their equivalent series resistance. Ultra-capacitors can be modelled as *RC* ladder networks, as shown in Figure 13, but for the purpose of these experiments, the ultra-capacitors are modelled with a single ideal capacitance C_{es} in series with a single resistance R_{es}.

The parameters of the bipolar ultra-capacitor were verified through constant load and constant current discharge tests, while only constant current discharge tests were performed on the prismatic ultra-capacitor. The experimental setup for the constant load test is described in Appendix D. The thermal performance and efficiency of the ultra-capacitors are also investigated.

Table 5 Rated parameters and dimensions of bipolar and prismatic ultra-capacitors

	Units	**Bipolar**	**Prismatic**
Rated voltage	V	135	56
Rated capacitance	F	18.6	95
Rated maximum constant power output	kW	3	15.5
Peak current	A	75	600
Dimensions		12.25"×12.25"×2.75"	19", 5U rack
Volume	litre	6.8	18
Weight	kg	8	37
Stored energy	kJ	170	149

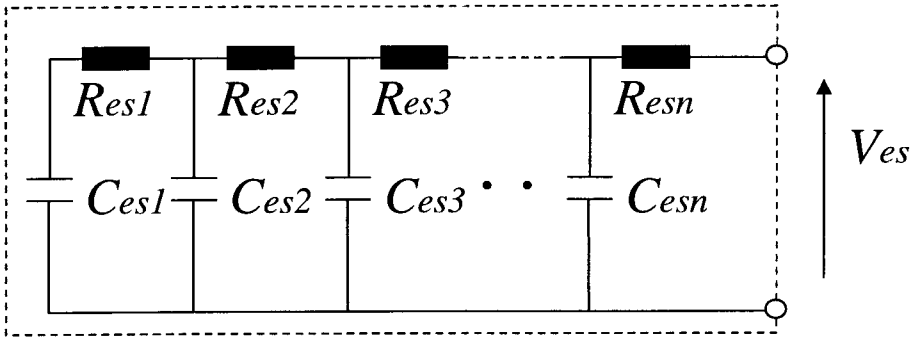


Figure 13 *RC* ladder network model of ultra-capacitor

2.5.1. Constant Load Discharge Test

It was attempted to estimate the parameters C_{es} and R_{es} of the bipolar ultra-capacitor through a constant (resistive) load discharge test, the equivalent circuit of which is shown in Figure 14.

It is assumed that the ultra-capacitor is initially charged to $V_{es}(0)$ and the circuit breaker S is open. Since there is no current flowing in the circuit, $V_{uc}(0) = V_{es}(0)$. At $t = 0$, the circuit breaker is closed which results in a discharge current flowing

$$I_{dis}(0^+) = \frac{V_{es}(0)}{R_{es} + R_d} \tag{2.4}$$

and therefore, at $t = 0^+$, the terminal voltage of the ultra-capacitor drops to

$$V_{es}(0^+) = V_{es}(0) - I_{dis}(0^+) \times R_{es} \tag{2.5}$$

The series resistance of the ultra-capacitor can therefore be determined as follows

$$R_{es} = \frac{V_{es}(0) - V_{es}(0^+)}{I_{dis}(0^+)} \tag{2.6}$$

Similarly, when the discharge is interrupted by opening the circuit breaker during discharge, the current drops to zero and the terminal voltage correspondingly rises to reflect the voltage across the ideal capacitor C_{es}. The average calculated series resistance R_{es} for the bipolar capacitor from measurements of several discharges is approximately 0.6Ω. The series resistance can be verified by measurement of the interruption in discharge. Since this resistance is determined from data during transient behavior, it will only accurately describe the ultra-capacitor response during transients, but it is assumed that the equivalent resistance describing steady state behavior is equal to this 'transient' or 'high frequency' resistance value.

The ideal capacitance C_{es} can be calculated by determining the RC constant from a discharge curve. The voltage V_{uc} across the ideal capacitor can be described as

$$V_{uc}(t) = V_{uc}(0) \exp\left(\frac{-t}{(R_d + R_{es})C_{es}} \right). \tag{2.7}$$

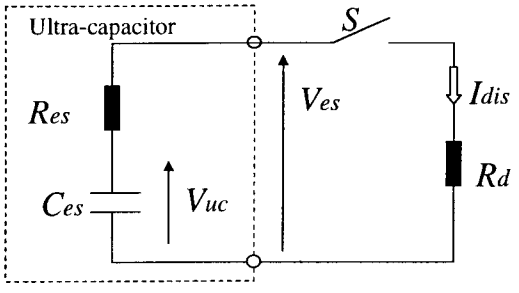


Figure 14 Equivalent circuit of ultra-capacitor discharging into resistive load

The RC constant can therefore be calculated from $V_{uc}(t)$ at $t = 0$ and $t = t_1$ as follows

$$(R_d + R_{es})C_{es} = -t_1 \times \left[\ln\left(\frac{V_{uc}(t_1)}{V_{uc}(0)} \right) \right]^{-1} \tag{2.8}$$

with

$$V_{uc}(0) = V_{es}(0) \tag{2.9}$$

and

$$V_{uc}(t_1) = V_{es}(t_1) + I_{dis}(t_1) \times R_{es} . \tag{2.10}$$

Substituting (2.9) and (2.10) in (2.8), we have

$$(R_d + R_{es})C_{es} = -t_1 \times \left[\ln\left(\frac{V_{es}(t_1) + I_{dis}(t_1) \times R_{es}}{V_{es}(0)} \right) \right]^{-1} . \tag{2.11}$$

The ideal capacitance C_{es} can now be determined since R_d and R_{es} are known. Graphs generated from a particular discharge of the bipolar capacitor lasting 45 seconds are shown in Figure 15.

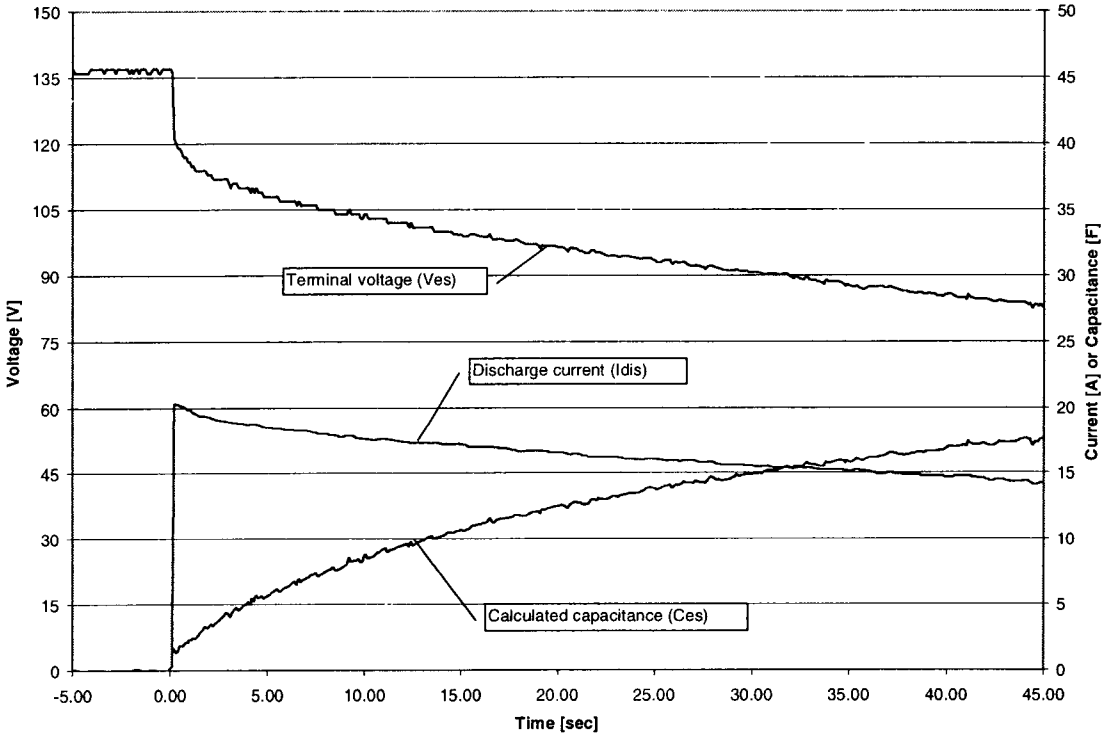


Figure 15 Calculation of capacitance from discharge curves of bipolar ultra-capacitor into resistive load

The ultra-capacitor is charged to its nominal voltage of 135V and then discharged into a resistive load of 5.8Ω. The terminal voltage of the ultra-capacitor V_{es} and the discharge current I_{dis} were measured with an HP 54542A oscilloscope and imported into an Excel spreadsheet and the ideal capacitance was calculated using (2.11). It can be seen that the calculated capacitance varies as t_1 is varied and therefore this method was found to be unreliable for determining the ultra-capacitor parameters. A constant current test was performed on both ultra-capacitors in order to determine their parameters.

2.5.2. Constant Current Discharge Test

The parameters of the bipolar and prismatic ultra-capacitors were calculated from discharge curves measured under constant current discharge. Under constant current discharge $V_{uc}(t)$ will change linearly with time, since

$$I_{dis}(t) = I = C_{es}\frac{dV_{uc}(t)}{dt} \tag{2.12}$$

therefore

$$\frac{dV_{uc}(t)}{dt} = \frac{I}{C_{es}} = \text{constant} \tag{2.13}$$

The capacitance can be estimated from a discharge lasting t_1 seconds as

$$C_{es} = I \times \left[\frac{dV_{uc}(t)}{dt}\right]^{-1} \approx I \times \frac{\Delta t}{\Delta V_{uc}} = \frac{I \times t_1}{V_{uc}(t_1) - V_{uc}(0)} = \frac{I \times t_1}{V_{es}(t_1^+) - V_{es}(0)} \tag{2.14}$$

where $V_{es}(0)$ is the open circuit voltage of the ultra-capacitor before the discharge and $V_{es}(t_1^+)$ is equal to the open circuit voltage of the ultra-capacitor after the discharge current was interrupted at $t = t_1$. The constant current discharge tests were performed at Maxwell Technologies and the discharge curves for the bipolar ultra-capacitor are shown in Figure 16 and for the prismatic ultra-capacitor in Figure 17.

The capacitance of the bipolar capacitor was estimated at 17.2F using (2.14) and the equivalent 'transient' series resistance is estimated at 0.88Ω from measurements of the interruption of the discharge, similar to measurements made with discharge into a resistive load, i.e.

$$R_{es} = \frac{V_{es}(t_1^+) - V_{es}(t_1)}{I} \tag{2.15}$$

It can be seen that the terminal voltage of the ultra-capacitor continues to rise after the current is interrupted and this is a result of voltage equalization across the internal equivalent capacitors in the more detailed ladder network model of the ultra-capacitor shown in Figure 13. The series resistance describing the steady state behavior of the ultra-capacitor is determined by allowing the ultra-capacitor voltage to stabilize before the open circuit voltage is measured, i.e.

$$R_{es} = \frac{V_{es}(t_1 + 10) - V_{es}(t_1)}{I} \tag{2.16}$$

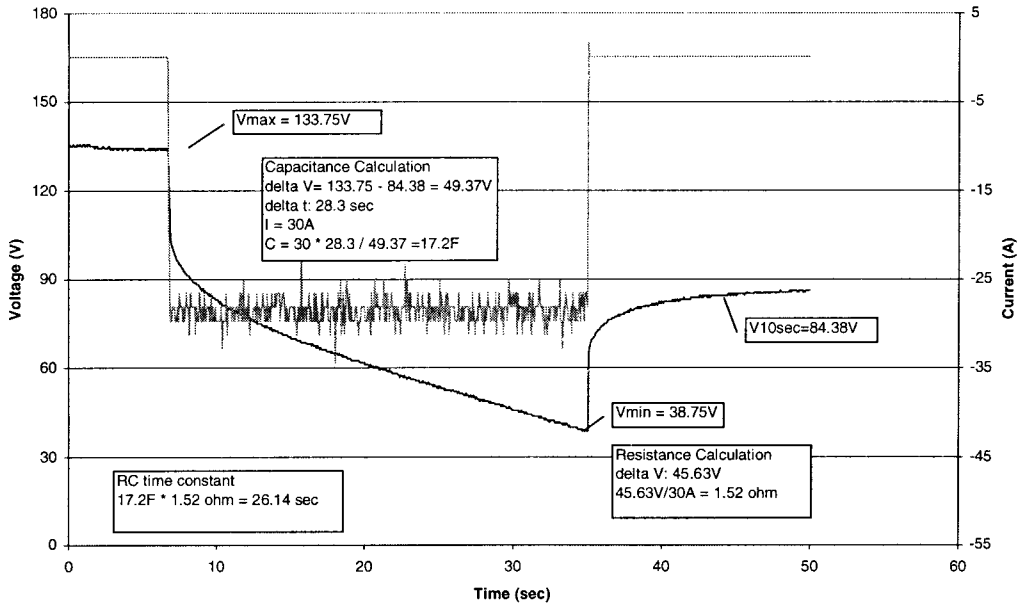


Figure 16 Verification of parameters of bipolar ultra-capacitor from constant current discharge curves

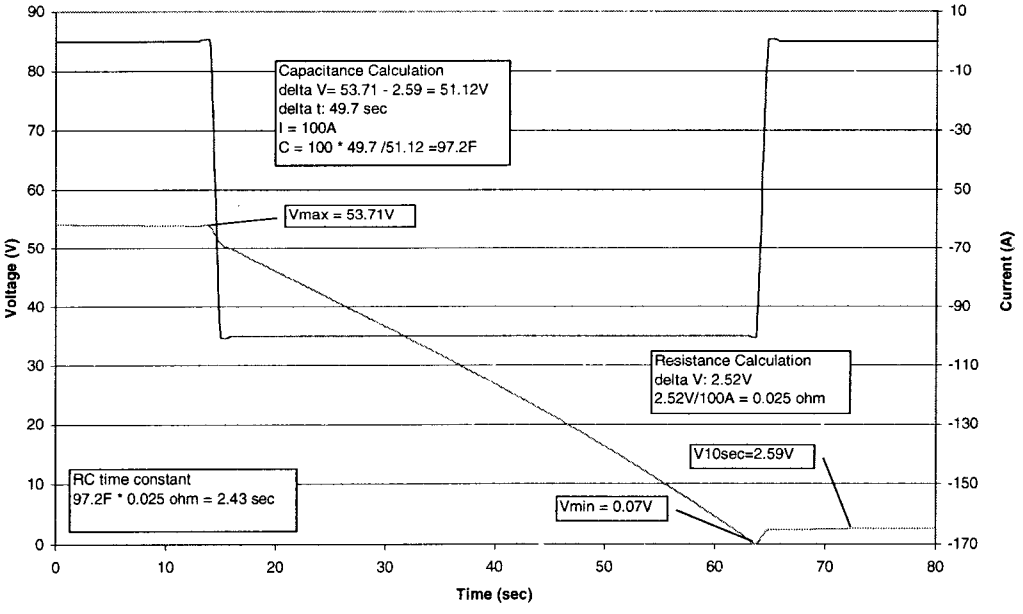


Figure 17 Verification of parameters of prismatic ultra-capacitor from constant current discharge curves

The series resistance of the prismatic ultra-capacitor is estimated at 0.025Ω using (2.16) and the capacitance was estimated at 97.2F using (2.14).

The equivalent parallel resistance R_p of the bipolar ultra-capacitor can be determined by charging the ultra-capacitor and then leaving it open circuited for a number of hours. R_p can be calculated using equation (2.8) with $V_{uc}(0)$ the voltage the ultra-capacitor is charged to and $V_{uc}(t_1)$ the voltage at the end of the self-discharge and $(R_{es} + R_d)$ replaced by R_p.

The parallel resistance of the bipolar ultra-capacitor was calculated to be 38kΩ from self-discharge data collected over 18 hours and the prismatic ultra-capacitor's parallel resistance was found to be 8kΩ from self-discharge data collected over 16 hours.

2.5.3. Temperature Performance

The ultra-capacitors were subjected to a series of consecutive charge and discharge cycles with the purpose of monitoring the temperature performance of the ultra-capacitor. A K-type thermo-couple was adhered to the skin of the bipolar ultra-capacitor in order to enable monitoring of the temperature inside the ultra-capacitor unit while the case temperature of the individual cells of the prismatic ultra-capacitor was monitored.

The bipolar ultra-capacitor was discharged ten times into a resistive load with a peak current of 20A, a rest of 10 seconds between each discharge and charge and no air flow over the ultra-capacitor. A constant current charge and discharge at 100A was performed on the prismatic ultra-capacitor with a 15 second rest and no air flow. The cycling test on the bipolar ultra-capacitor was stopped when the temperature rose above 38°C, since the specification on the capacitor is to not operate it when the temperature is above 40°C. The rise in temperature is shown in Figure 18. The capacitor was fully discharged immediately following this test and the temperature rose to 38.8°C during the final discharge. It can be seen that the temperature continued to rise during the cycling test with no indication of stabilizing at a temperature below the maximum temperature of 40°C.

The prismatic ultra-capacitor consists of individual cells and the case temperature of each of these was monitored. In Figure 19 the maximum and minimum case temperatures are shown and, as for the bipolar ultra-capacitor, the temperature fails to stabilize during the cycling test and the maximum case temperature approaches 40°C after 40 minutes, although the prismatic ultra-capacitor can be operated at much higher temperatures than the bipolar ultra-capacitor and the test could therefore be conducted over a longer period of time. However, in an ASD ride-through application, the ultra-capacitor will not be subjected to this many consecutive cycles in such a short time.

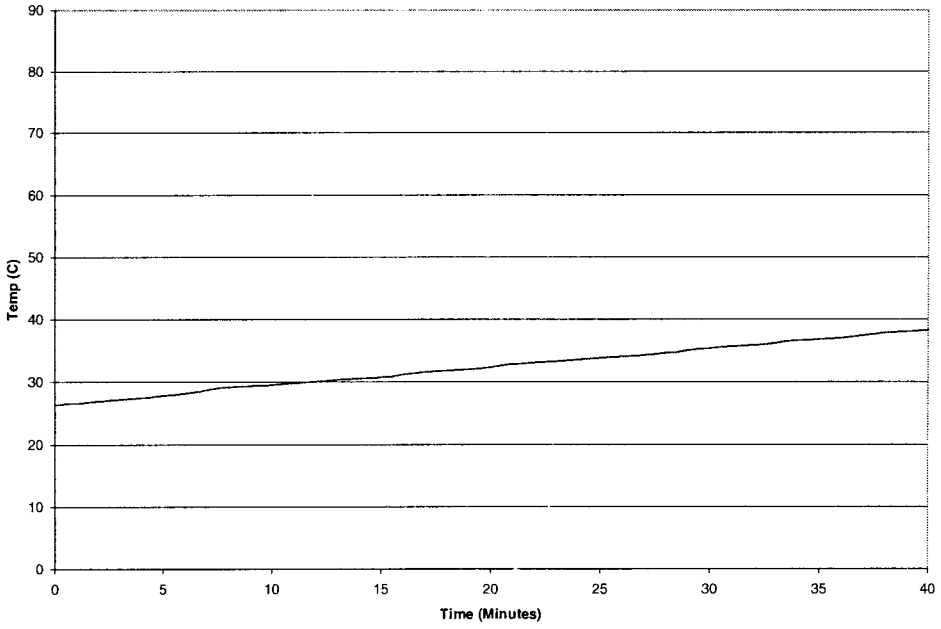


Figure 18 Temperature performance of bipolar ultra-capacitor during cycling test

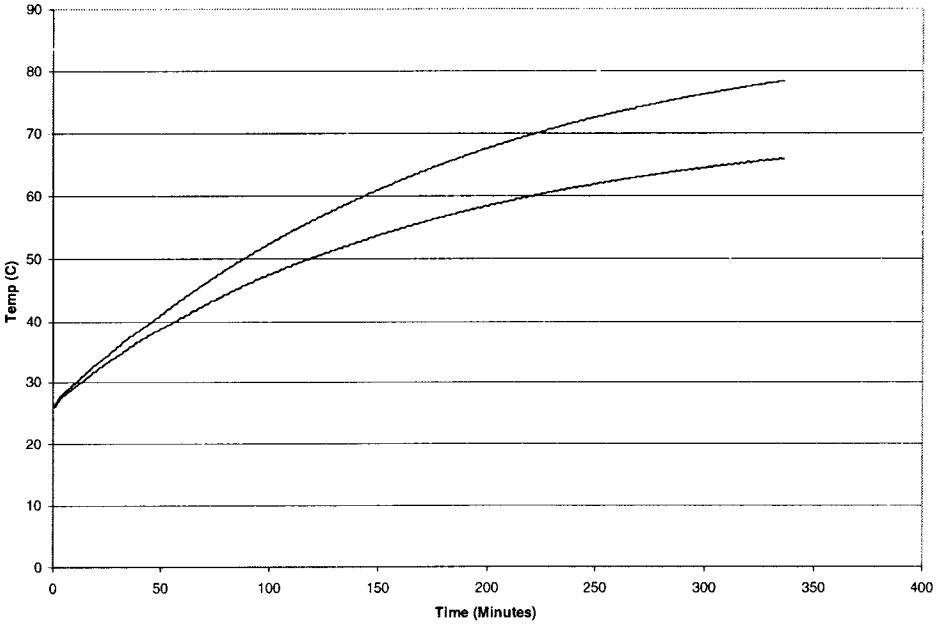


Figure 19 Minimum and maximum temperatures of prismatic ultra-capacitors during cycling test

2.5.4. Efficiency

It is also of interest to determine how efficiently the energy stored in the ultra-capacitor can be transferred to the load during a discharge. The efficiency is expressed as follows

$$\eta(t) = \frac{E_{del}(t)}{E_{del}(t) + E_{loss}(t)} \times 100\% \tag{2.17}$$

with $E_{del}(t)$ the energy delivered to the load and $E_{loss}(t)$ the losses within the ultra-capacitor. The sum of the energy delivered to the load and the losses within the ultra-capacitor is equal to the total loss in stored energy of the ultra-capacitor as a result of the discharge. The energy delivered to the load is calculated as

$$E_{del}(t) = \int_0^t V_{es}(\tau) I_{dis}(\tau) d\tau \tag{2.18}$$

and the losses in the ultra-capacitor is calculated as

$$E_{loss}(t) = \int_0^t I_{dis}^2(\tau) R_{es} d\tau \tag{2.19}$$

The integral is approximated by rectangular numerical integration for the discharge period and the data of the same discharges as shown in Figure 16 and Figure 17 are used to calculate the efficiency. The calculated delivered energy, losses and efficiency, using data after the switching transient, are shown in Figure 20 for the bipolar ultra-capacitor and in Figure 21 for the prismatic ultra-capacitor.

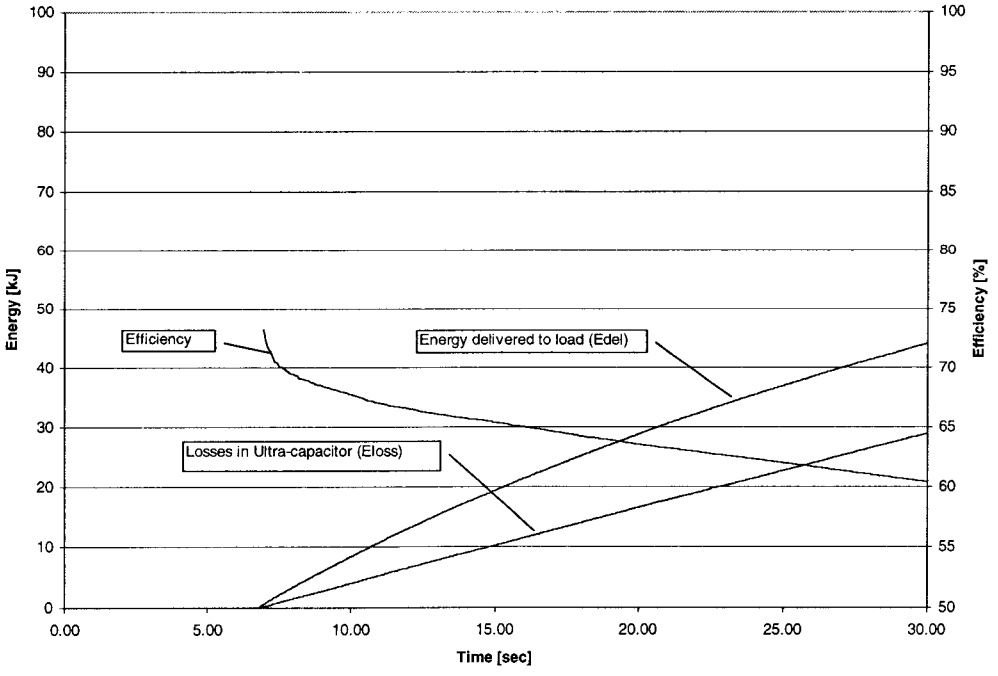


Figure 20 Calculation of efficiency of bipolar ultra-capacitor from constant current discharge

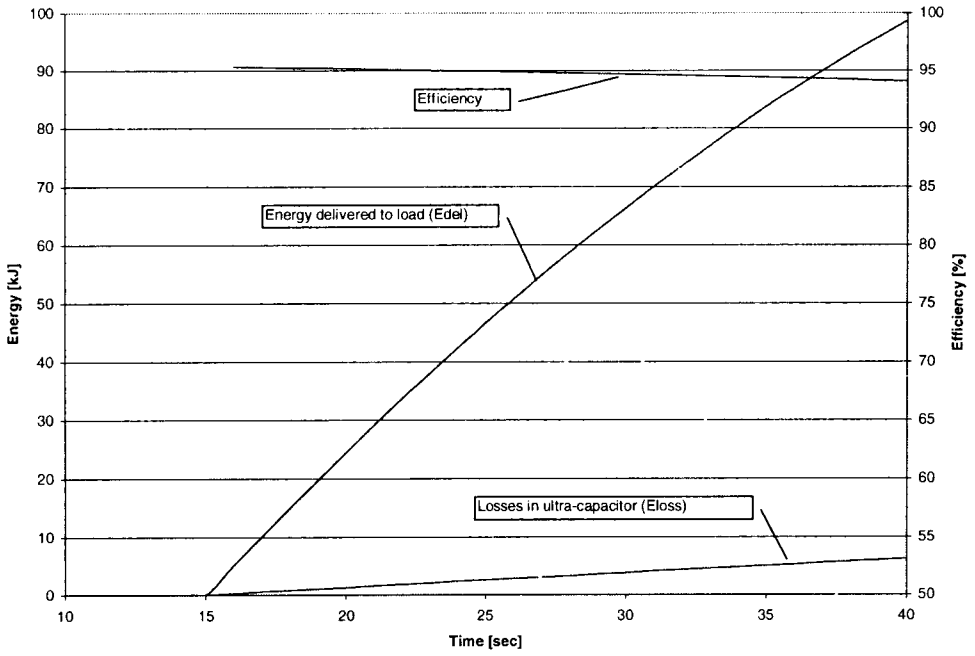


Figure 21 Calculation of efficiency of prismatic ultra-capacitor from constant current discharge

The bipolar ultra-capacitor has a significantly lower efficiency as a result of its higher internal resistance R_{es} and the efficiency for both ultra-capacitors decrease with time as the ultra-capacitor voltage, and therefore the power delivered to the load, drops and the losses stay constant for a constant current discharge.

A lower discharge efficiency translates into the need for more ultra-capacitors. This is illustrated by considering an application where it is required to deliver X kJ over 15 seconds, i.e.

$$E_{del}(15) = \mathrm{X} \tag{2.20}$$

For an ultra-capacitor which has an efficiency of λ over 15 seconds, i.e. $\eta(15) = \lambda$, the energy which has to be extracted from the ultra-capacitor to deliver the required energy to the load equals

$$E_{del}(15) + E_{loss}(15) = \frac{E_{del}(15)}{\eta(15)} = \frac{\mathrm{X}}{\lambda} \tag{2.21}$$

If 60% of the initial stored energy $E_{st}(0)$ in the ultra-capacitor bank can be extracted, then the sum of the delivered energy and losses in the ultra-capacitors may total up to 60% of $E_{st}(0)$, i.e.

$$E_{del}(15) + E_{loss}(15) = \frac{\mathrm{X}}{\lambda} \le 0.6E_{st}(0) \tag{2.22}$$

therefore

$$E_{st}(0) \ge \frac{1}{0.6 \times \lambda}\mathrm{X} \tag{2.23}$$

For an ultra-capacitor with an efficiency of 63%, i.e. λ=0.63, as calculated for the bipolar ultra-capacitor for the discharge in Figure 16, the initial stored energy $E_{st}(0)$ has to be 2.65 times the amount of energy delivered to the load $E_{del}(15)$ and for an ultra-capacitor bank with an efficiency of 95%, as calculated for the prismatic ultra-capacitor for the discharge in Figure 17, only 1.75 times the amount of energy delivered to the load needs to be stored.

2.6. CONCLUSIONS

In order to provide an ASD with momentary interruption ride-through, an energy storage system with high specific power and power density needs to be interfaced to the ASD. Flywheels, ultra-capacitors and advanced batteries were found to be viable technologies and were evaluated for use in such an energy storage system. Since the interface circuit between the energy storage elements and the ASD has a significant influence on the performance of the system, energy storage systems which include the interface circuit were compared based on criteria developed specifically for this application. Because of the safety concerns with flywheels and the high maintenance required for batteries, it was determined that ultra-capacitors are the best suited to this application.

Possible interface circuits between the energy storage elements and the ASD were presented. The bi-directional DC/DC converter and a novel interface circuit in which an active rectifier can be used for both AC/DC and DC/DC conversion were discussed in more detail. The use of the rectifier for AC/DC and DC/DC conversion is a promising topology, but further evaluation of this circuit falls outside the scope of this thesis.

Two ultra-capacitor technologies, prismatic and bipolar, were experimentally evaluated in order to verify their rated parameters and to investigate their suitability to this application. Their equivalent series and parallel resistances, temperature performance and discharge efficiencies were determined. The bipolar ultra-capacitor has a higher internal resistance due to its internal structure which results in a lower discharge efficiency. It was shown how a lower discharge efficiency translates into the need for more ultra-capacitors, which would make the bipolar ultra-capacitors a less cost-effective solution. Overall the prismatic ultra-capacitors exhibit superior performance for application to ASD ride-through and they are also less expensive than the bipolar ultra-capacitors.

3. VOLTAGE SAG RIDE-THROUGH STRATEGIES FOR ASDS

3.1. INTRODUCTION

The reliable operation of electrical equipment under power system disturbance conditions can be ensured in a number of different ways [1]. A number of solutions have been suggested in the literature and/or implemented commercially for ASD ride-through and a classification of these solutions is shown in Figure 22.

The first distinction is between solutions implemented on the utility side and those implemented on the customer side. Solutions on the utility side ensure the quality of the ac input voltage to an entire manufacturing facility during power system disturbances. This can be achieved by supplying power to the facility through a separate feeder so as to not be influenced by other customers on the same feeder or by installing an alternative tie with a fast solid state transfer switch between the feeders [21]. These are very costly solutions however and in some cases it is more economical to install compensating equipment, such as a Static Compensator (Statcom) or Dynamic Voltage Restorer (DVR) at the service entry to a customer's premises. Compensating equipment installed on the utility side conditions all of the power supplied to the customer, even power supplied to loads which are not sensitive to power system disturbances or non-critical loads. The rating of compensating equipment can be reduced by installing it on the customer side and loading it with sensitive and/or critical equipment only.

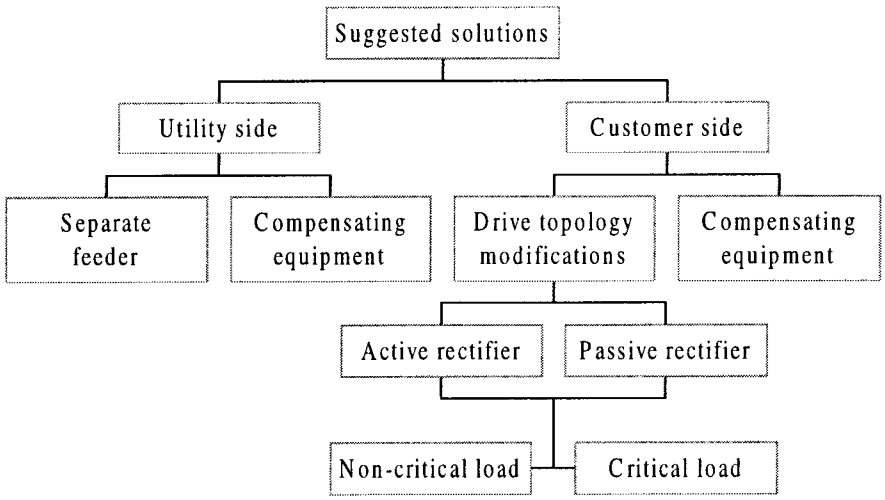


Figure 22 Suggested solutions

Within the customer's facility, sensitive equipment can be isolated from the main supply through an in-line uninterruptible power supply (UPS). Disadvantages related to the use of an in-line UPS include the cost of the UPS, especially at high power levels, and the losses associated with the UPS which reduce the efficiency of the system, since all of the load power is continuously processed. In order to increase the efficiency, an off-line UPS can be used which is only used when the utility supply experiences a disturbance. Usually batteries are used for energy storage in the UPS which require regular maintenance and can take up a significant amount of floor space, depending on the amount of ride-through which is provided. The number of discharge cycles the batteries can stand is also limited.

Instead of using additional equipment to protect sensitive loads from power system disturbances, it may prove much simpler to design electrical equipment with the inherent ability to ride through these disturbances. Several different modifications of the topology and/or control strategy of the ASD to achieve ride-through have been proposed. When choosing which of the proposed drive topology modifications to use it is important to keep in mind that some of the topologies are only for a passive or active rectifier and some address only non-critical loads, as opposed to critical loads.

It should always be kept in mind that power quality and reliability can be enhanced by tree trimming, adding line arresters, insulator washing and adding animal guards, improvement of fault clearing practices by adding line reclosers, eliminating fast tripping, adding loop schemes, modifying feeder design and good grounding practices. The solutions presented here are to be reserved for use where these general preventative measures prove insufficient.

3.2. Compensating Equipment

Most disruptive voltage sags and momentary interruptions are caused by remote fault clearing and therefore series and shunt compensation techniques for voltage sags caused by remote fault clearing were investigated. Traditional compensating equipment include motor-generator sets, uninterruptible power supplies, ferroresonant, constant voltage transformers and magnetic synthesizers. Recent advances in power electronics have led to the development of several compensating devices such as the Dynamic Voltage Restorer, Statcom and Unified Power Flow Controller [2][21]. These devices are operated at high switching frequencies and therefore exhibit very fast response. These devices can regulate the voltage during a sag by either injecting a controlled current (shunt compensation) or voltage (series compensation) into the system. In order to explain the occurrence of voltage sags as a result of remote fault clearing, consider the system in Figure 23. When a three phase short circuit fault occurs at **A**, the voltage V_b at the distribution bus can be approximately expressed as

$$V_b = \frac{Z_{line2}}{Z_{line2} + Z_{tf} + Z_{bus}} \times V_{tr} \qquad (3.1)$$

with V_{tr} the transmission system voltage referred to the low voltage side of the transformer.

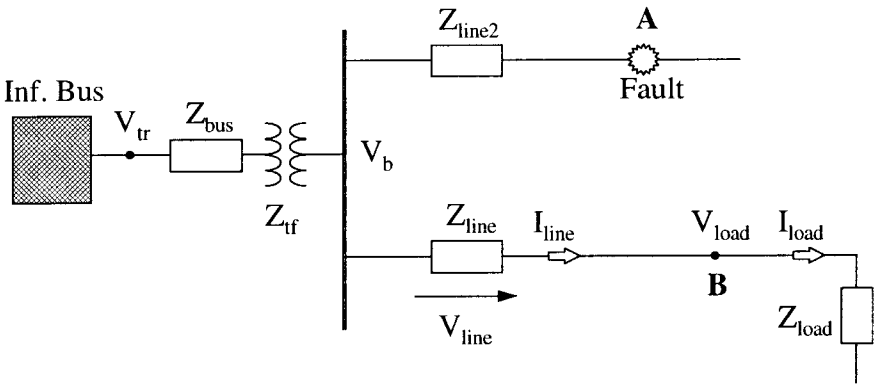


Figure 23 Line diagram of a simple distribution system

It is assumed that an infinite bus establishes a constant transmission voltage. The closer the fault occurs to the bus, the lower the bus voltage V_b will be, because a larger impedance is shorted out of the line. The voltage V_{load} at **B** on a distribution line fed from the same bus will be

$$V_{load} = \frac{Z_{load}}{Z_{load} + Z_{line}} \times V_b \tag{3.2}$$

Three phase short circuit faults are the most severe, but also the least common. Single line-to-ground and line-to-line faults are more common, but cause less severe faults. Fault clearing procedures involve opening of circuit breakers upstream of the faults, which restores the upstream voltages to nominal, followed by usually two to three reclosing attempts which returns the voltages to sag levels as long as the fault persists.

Steady state conditions during the sag are assumed, therefore the study could be conducted using phasor diagrams. The MATLAB programs used to determine the compensating current and/or voltage and the power rating of the compensator are listed in Appendix E. The objective is to regulate the voltage V_{load} across a critical load Z_{load} to a prescribed level of 0.99pu. The phase angle of this voltage relative to the bus voltage can be arbitrarily chosen, but will usually not be phase shifted too much from the bus voltage V_b. The bus voltage is assumed to be 12kV nominal and the critical load is assumed to be a constant power load drawing 3MVA/2.7MW. The load current is approximately 275A. It is also assumed that the critical load is small in comparison with the short circuit rating of the distribution bus and therefore the compensators do not influence the bus voltage.

3.2.1. Shunt Compensation

A shunt compensator, as shown in Figure 24, is installed in parallel with the critical load for which voltage sag ride-through needs to be provided and is modelled as a controllable current source I_c.

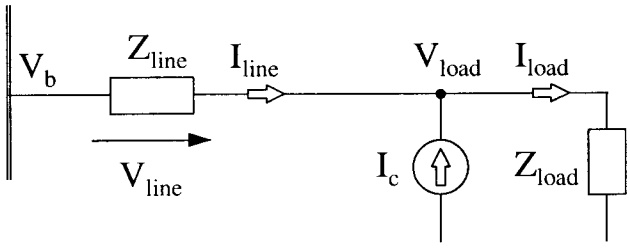


Figure 24 Line diagram of shunt compensator

In Figure 25 the phasor diagram for shunt compensation is drawn with the load voltage angle lagging the bus voltage. The load current I_{load} is related to the load voltage by the load impedance, which is assumed to be inductive. The voltage drop across the line V_{line} leads to a certain line current I_{line} flowing. The compensation current needed to establish the desired load voltage is equal to the difference between the line and load currents, i.e.

$$I_c = I_{load} - I_{line} \tag{3.3}$$

Results from the MATLAB simulations are shown in Figure 26 for a 0%, 20% and 40% sag in bus voltage respectively. The active P_c and reactive power Q_c delivered by the compensator and the compensator current as a function of the phase difference ψ between the load and bus voltages are shown. The magnitude of the injected current and delivered power increases as the sag magnitude increases. The active power rating has a zero crossing at some finite phase difference ψ, depending on the sag magnitude. This means that sag compensation can be achieved by only providing reactive power to the system. This has the advantage of not requiring an energy storage system to be interfaced to the converter of the compensator.

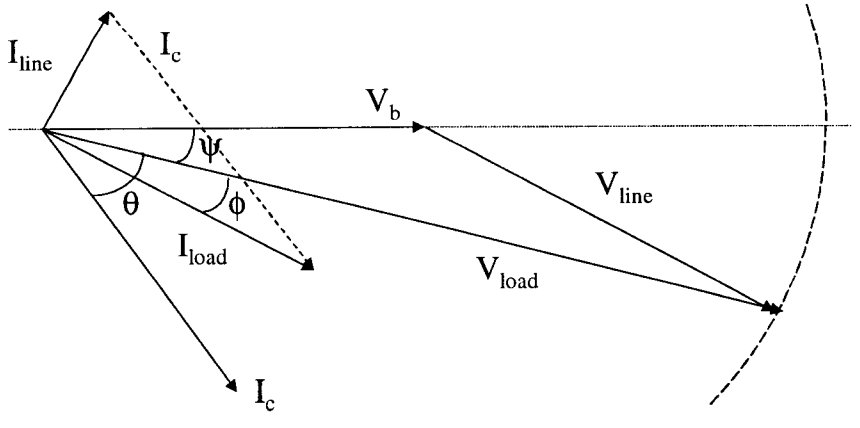


Figure 25 Phasor diagram for shunt compensation

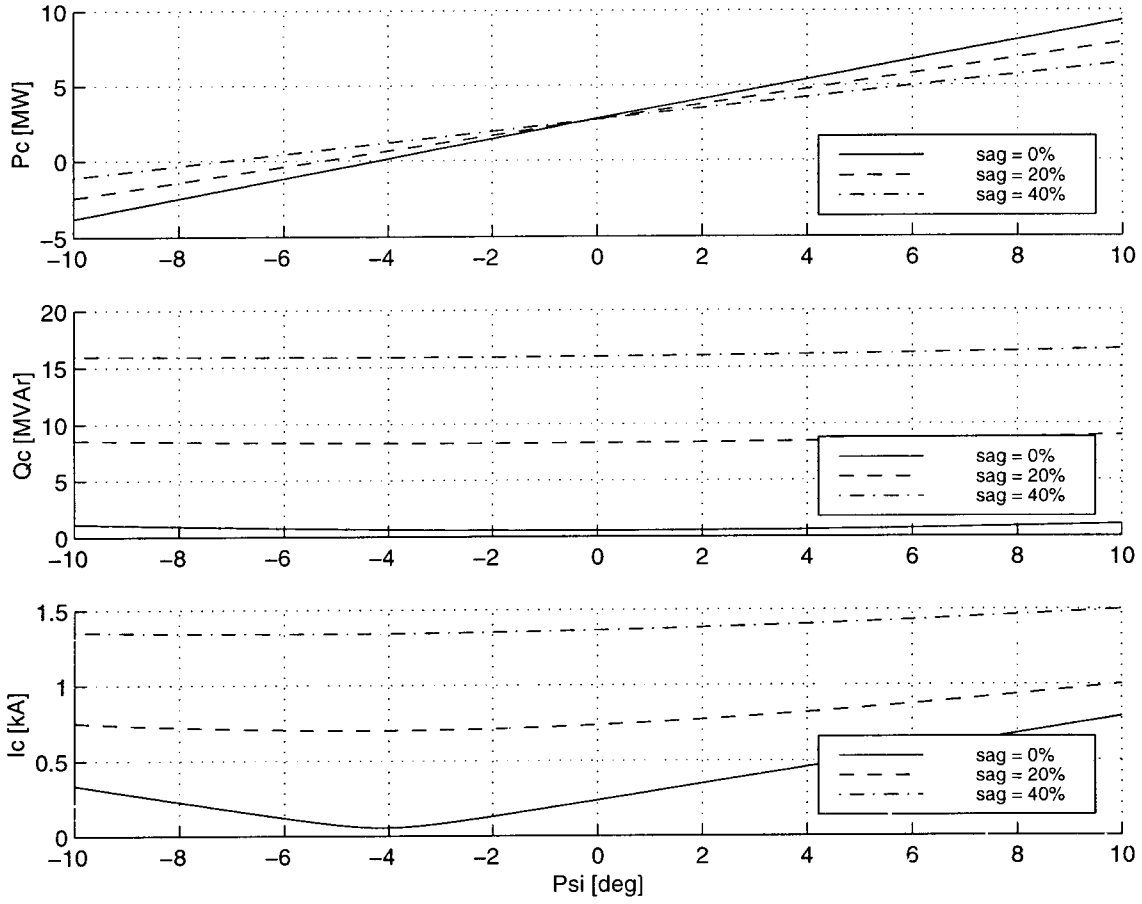


Figure 26 Compensating current and delivered power for shunt compensator

However, the apparent power required from the compensator to regulate the load voltage for a 40% sag is higher by an order of magnitude than the load power rating. This is because the compensator not only supplies reactive power to the load, but also to the line because of the voltage drop between the load and the bus.

In order to reduce the power rating of the shunt compensator to the same order as the load, it is necessary to add an isolation switch between the compensator and the grid which will prevent the compensator from feeding the fault. This will however require the compensator to provide the load power during the sag which will make the addition of an energy storage system necessary. Figure 27 shows the increase in line current with increased sag magnitude. For deep sags the line current is much higher than the load current of 275A and it may exceed the thermal limit of the line.

The commercial implementation of a converter based shunt compensator is known as a Static Compensator (Statcom). A 100MVAr installation has been implemented in the Tennessee Valley Authority transmission system to provide day to day voltage regulation and to damp power system oscillations.

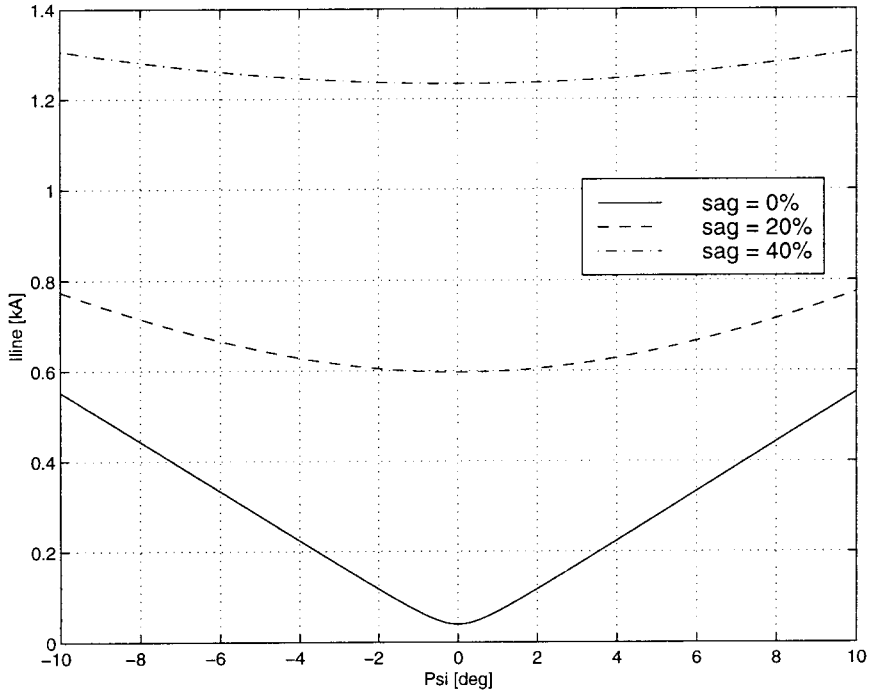


Figure 27 Line current for a shunt compensator

A thyristor inverter in the Statcom rectifies a portion of the ac power from the line to dc power to charge a large capacitor and then inverts this dc power to ac for re-injection to the line as needed. The capacitor both acts as a source of constant voltage and provides enough energy to supply real power to the line for a few cycles during voltage sags or interruptions [22], although only reactive power is exchanged with the system on a steady state basis [29]. The topology can also be used in conjunction with an energy storage device which will enable it to exchange real power with the system [30].

3.2.2. Series Compensation

A series compensator is placed in series with the line and is modelled as a controllable voltage source V_c. The injected voltage V_c establishes the desired voltage across the critical load. The line diagram of a series compensator is shown in Figure 28 and the phasor diagram for series compensation is shown in Figure 29.

In this configuration the load and line currents are the same, i.e. $I_{load} = I_{line}$, and the relationship for the compensating voltage is

$$V_c = V_b + V_{line} - V_{load}. \tag{3.4}$$

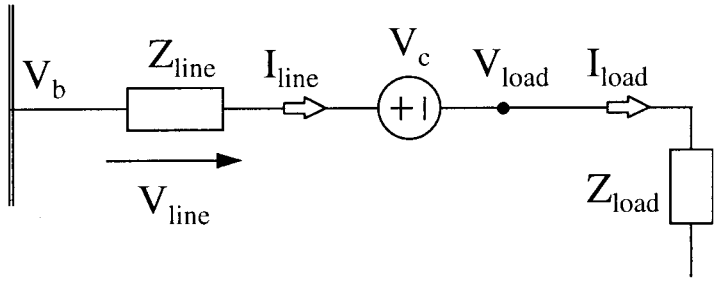


Figure 28 Line diagram for series compensation

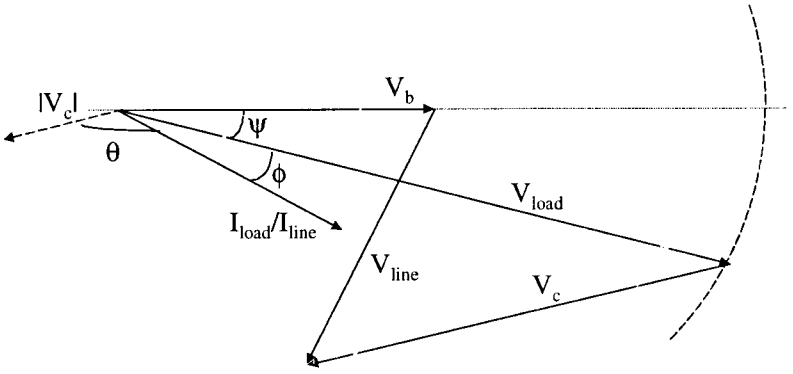


Figure 29 Phasor diagram for series compensation

From simulation results for a 0%, 20% and 40% sag respectively shown in Figure 30 it can be seen that the required power rating for series compensation is an order of magnitude lower than for shunt compensation and for all cases lower than the load power. This is because the series compensator only supplies power to the load and no power is delivered to the line. However, active power and hence an energy storage system is always required for series compensation and the series transformer required to inject the compensating voltage in series with the line also poses significant technical challenges. The injected voltage, active and reactive power delivered to the system increase as the sag magnitude increases.

A commercially available series compensator is known as a the Dynamic Voltage Restorer and there are several installations worldwide at the 2MVA to 4MVA power level. It consists of a DC/AC converter interfaced through a series injection transformer to the power system. The dc bus voltage is supported by a capacitor, but is also connected to an energy storage system which delivers the required active power during voltage sag conditions. Any of the energy storage technologies discussed in Chapter 2 can be used for this purpose.

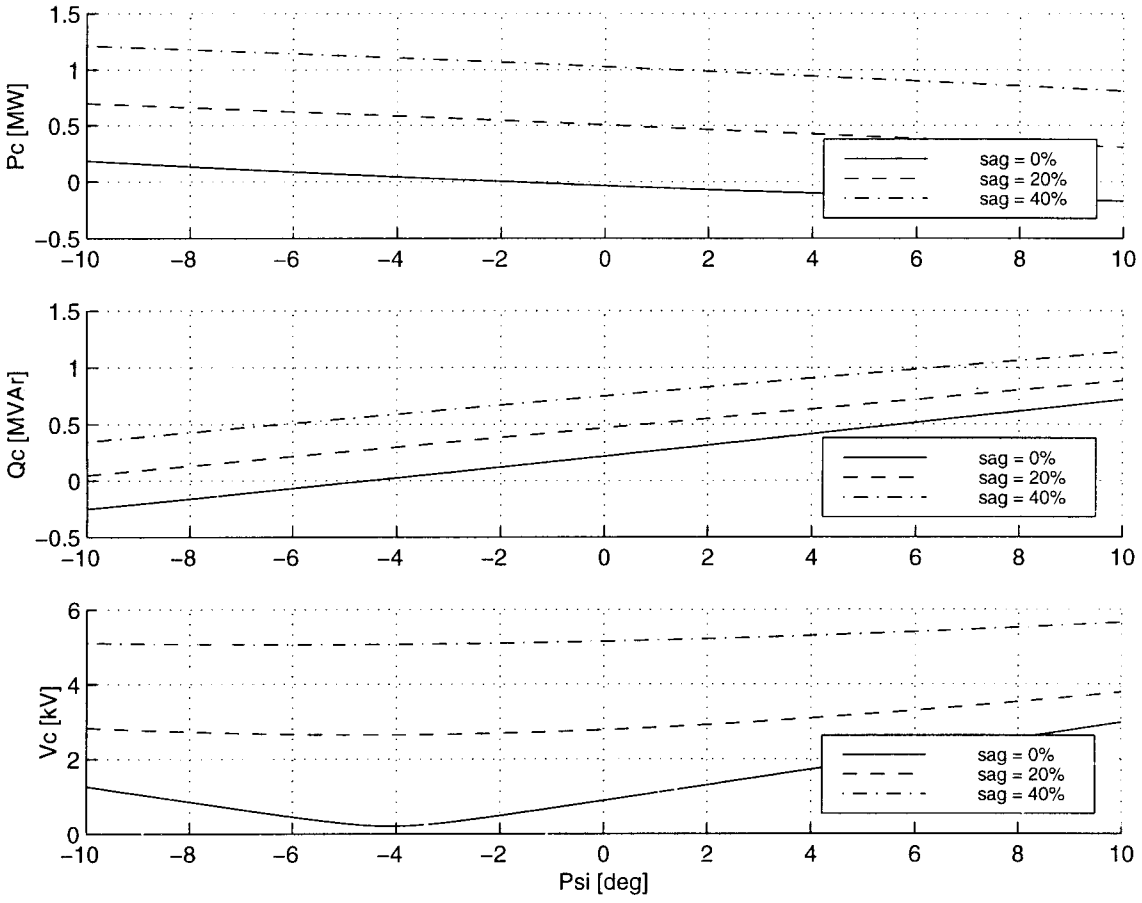


Figure 30 Compensating voltage and power delivered for a series compensator

The need for an energy storage system can be eliminated by connecting the dc bus to another converter which is connected to the power system through a shunt transformer. The shunt converter can be controlled to draw the real power needed by the series converter from the system [33]. The single line diagram is shown in Figure 31, with the shunt converter modelled as a current source.

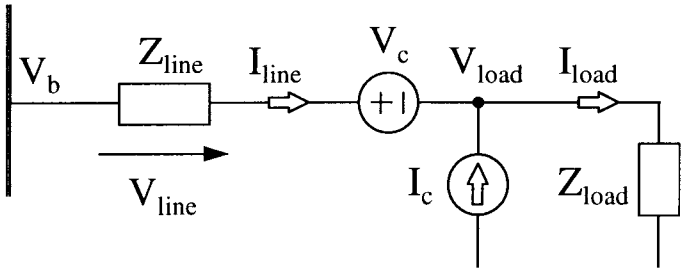


Figure 31 Line diagram for series and shunt compensation

A commercial implementation of this type of compensator is known as a Unified Power Flow Controller, which has other features besides voltage regulation. A UPFC rated at 100MVA has been operational in Inez, KY since 1998.

3.2.3. Conclusions

Compensating equipment for voltage sags and momentary interruptions can be classified as either shunt or series devices and the operating characteristics of these two types of compensators have been presented. The power rating of the shunt compensator is an order of magnitude higher than the load power and this can only be reduced by inserting an isolation switch between the compensator and the load which will prevent the compensator from feeding the fault during a sag. This will however require an energy storage system to be interfaced to the compensator to supply the load power during the sag.

The series compensator has more desirable power rating characteristics than the shunt compensator, although it poses considerable difficulties in construction and protection of the series injection transformer. The series compensator has to deliver real power to the power system in order to provide voltage sag ride-through, but the need for an energy storage system can be eliminated by connecting the dc bus of the series converter to a shunt converter which can draw the required real power from the power system.

3.2.4. Compensating Equipment

Developments in power electronics devices over the past decade have made it possible to implement power electronics converter based solutions to voltage sags and momentary interruptions such as the Statcom, Dynamic Voltage Restorer and Unified Power Flow Controller. These devices can also be used to address other power quality problems such as harmonics, voltage regulation and flicker.

A brief discussion of some converter based power quality compensators which have been developed to address voltage sag and/or other power quality problems is presented. All of these compensators are commercially available or in a pre-commercial stage of development with results from field tests available. They are categorized by topology and their capabilities and compensation strategies are summarized in Table 7. They are compared in the context of a very simple system with a single power source and single load, for ease of comparison, although they can be used in much more complex systems. Some compensating functions can be achieved with more than one topology, hence the choice of a particular compensator depends on the specific problem in terms of the functions required and the associated cost limit. All the converters are voltage source inverters (VSI) which are connected to the power system through a transformer. They are depicted as controllable current or voltage sources, as shown in Figure 32, where a current source implementation is achieved through a current control loop. The symbols used in the discussion of each compensator are listed in Table 6.

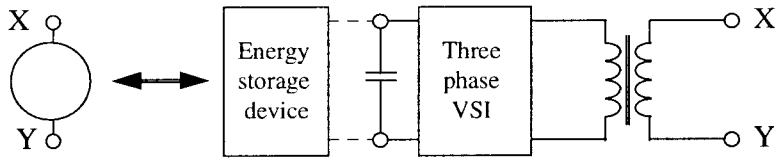


Figure 32 Definition of symbols used in Table 6.

Table 6 Description of symbols used in discussion of power quality compensators

Symbol	Description
i_s	Line current
i_u	Load current
i_c	Compensator current
Z_F	Impedance of the passive filter
Z_S	Line Impedance
K	Active impedance
v_s	Supply voltage
v_t	Line voltage
v_c	Converter output voltage

Some converter topologies need to supply active power to the load in order to provide compensation and the capabilities of other compensators can be expanded by the addition of an energy storage system. Where an energy storage system is required to implement a certain function, it is denoted by an asterisk (*) in Table 7.

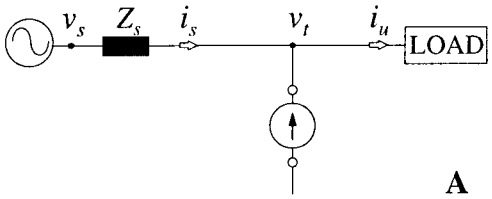
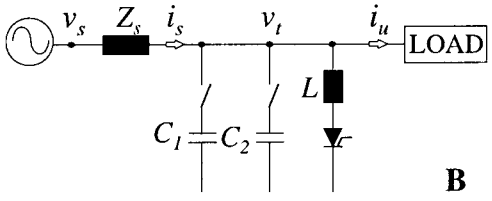
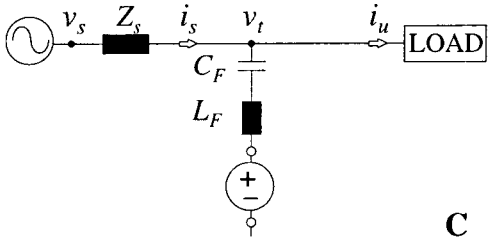
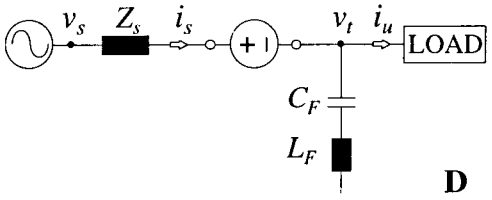
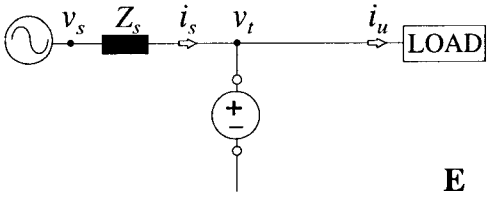
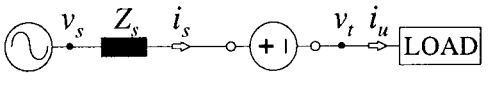
3.2.4.1. Active Filter

An Active Filter [63] consists of a current source in shunt with the line and compensates for load harmonics by injecting the harmonics of the load side current into the system, i.e.

$$i_c = i_{uh} \tag{3.5}$$

In this way, the power system does not have to supply the harmonics which reduces line voltage harmonics by eliminating the harmonic voltage drop across the line impedance. The main advantage of the active filter over passive tuned filters which are still extensively used is that the filtering characteristics of the active filter do not depend on system impedances. However, active filters are inferior in initial cost and efficiency to passive filters.

Table 7 Comparison of Converter Based Power Quality Compensators

Topology	Name and Capabilities	Strategy
 A	**Active Filter** Harmonic compensation **Multi-Functional Active Filter** Harmonic compensation, voltage regulation, power factor improvement, imbalance compensation	Converter injects load current harmonics Converter injects the sum of the load current harmonics and a fundamental component current calculated from voltage and power factor requirements
 B	**Static Var Compensator** Voltage regulation, flicker compensation, power factor improvement	Amount of reactance switched in parallel to the load is controlled via the capacitor bank switches and the thyristor switched reactors
 C	**Harmonic Isolator** Harmonic isolation **Hybrid active filter** Harmonic compensation	Converter improves filtering characteristics of passive filter Injects load current harmonics
 D	**Hybrid Series Active Filter** Harmonic isolation*	Converter improves filtering characteristics of passive filter
 E	**Statcom** Voltage regulation, flicker compensation, voltage sag compensation*	Sources or sinks the necessary amount of reactive power to regulate line voltage
 F	**Dynamic Voltage Restorer** Harmonic, flicker and impedance compensation, voltage regulation, voltage sag compensation*	Injects difference between desired line voltage and measured line voltage

*Energy storage system needed to deliver active power in order to perform this function

3.2.4.2. Multi-Function Active Filter (MFAF)

By adding a fundamental component current to the harmonic current the active filter injects into the system, it is possible to achieve voltage regulation, power factor improvement and imbalance compensation along with harmonic compensation. Meidensha Corporation is marketing units with a rating of up to 1MVA [78].

The fundamental current component is out of phase with the line voltage, therefore reactive power is sourced or sunk by the MFAF. It is possible to control the line voltage by controlling this "source" of reactive power in shunt with the load. And in the same way power factor improvement and imbalance compensation can be achieved.

3.2.4.3. Static Var Compensator (SVC)

The Static Var Compensator (SVC) is able to regulate the line voltage under changing load conditions up to flicker frequencies (<12Hz). It replaced the synchronous condenser as a line voltage regulator in transmission systems, since it has a faster response time and requires less maintenance due to the absence of moving parts.

The SVC is a shunt compensating device based on thyristor technology. It consists of a bank of capacitors with a certain fixed capacity as well as capacitors which can be switched in and out of the system to regulate the capacitive contribution of the SVC. The capacitors are switched in or out for the full cycle by thyristor switches. However, the bank of reactors is switched into the distribution system for part of a cycle in order to continuously control the reactive contribution. Line voltage regulation is achieved by controlling the reactance of the SVC so as to source or sink the required amount of reactive power.

Developed for transmission system applications, it has shown itself to be a robust and reliable technology, to the extent that in 1994 about 500 SVCs were in active duty around the globe [74]. Where voltage regulation and/or flicker problems exist in a distribution system, the usefulness of the SVC should not be forgotten in the wake of newer converter based compensators.

3.2.4.4. Harmonic Isolator / Hybrid Active Filter

This topology is a series combination of a passive filter and a converter which appears in shunt with the line. Two distinctive compensators have this topology: the Harmonic Isolator and Hybrid Active Filter. For the Harmonic Isolator [65] the converter is used to improve the filtering characteristics of the passive filter. For a passive filter alone, the ratio of line harmonic current to load harmonic current is given by

$$\frac{i_{sh}}{i_{uh}} = \frac{Z_F}{Z_S + Z_F} \qquad \textbf{(3.6)}$$

By injecting a converter voltage which is proportional to the line harmonic current, $v_c = K \times i_{sh}$, this ratio is changed to

$$\frac{i_{sh}}{i_{uh}} = \frac{Z_F}{Z_S + Z_F + K} \tag{3.7}$$

It can be seen that by increasing K, the line current harmonics can be reduced significantly compared to the case where only a passive filter is used. The advantage of this topology is that the converter power rating is greatly reduced in comparison to the Active Filter and therefore higher switching frequencies can be used which makes the response time faster.

The Hybrid Active Filter [66] has the same control strategy as the Active Filter, i.e. the injection of load harmonics into the system. The passive filter is used along with the converter to reduce the converter power rating.

3.2.4.5. Hybrid Series Active Filter

The control strategy of the Hybrid Series Active Filter [67] is the same as for the Harmonic Isolator and the filtering characteristics of the Hybrid Series Active Filter are described by equation (3.7). In this topology the converter injects a voltage proportional to the load harmonic current in series with the line. The converter power rating, as with the Harmonic Isolator, is small in comparison to the load power. Disadvantages of this configuration are that a converter failure will interrupt load power supply and an energy storage system is required since the load current, with changing load power factor, flows through the converter. This topology can also be used to simultaneously compensate for voltage unbalance [68].

3.2.4.6. Statcom

The Statcom or "Static Condenser" [64] was developed for transmission systems to regulate the line voltage under changing load conditions and to compensate for voltage flicker. It acts like a controllable reactance which can source or sink the required amount of reactive power for line voltage regulation. It consists of a voltage controlled converter connected in shunt with the line through a transformer. The output voltage of the converter is controlled to be in phase with the line voltage. When the amplitude is greater than the line voltage, a leading current with respect to the line voltage flows through the transformer impedance and the line voltage is boosted. In the same way the line voltage can be bucked by injecting a voltage with smaller amplitude than the line voltage.

The Statcom has the advantage of being able to deliver rated reactive current under reduced voltage conditions. For transmission system applications GTOs have to be used as switches because of the high converter power rating which limits the switching frequency. For distribution system applications IGBTs can be used, making higher switching frequency and therefore higher control bandwidth possible. With an IGBT based Statcom it is possible to achieve active filtering along with voltage regulation and flicker

compensation. An IGBT based 2 MVA Statcom has been built by Westinghouse under contract to EPRI for installation in a distribution system [21].

3.2.4.7. Dynamic Voltage Restorer

The Dynamic Voltage Restorer [21] compensates for any deviation of the line voltage from the reference waveform, including voltage sags, surges and harmonics, by injecting the difference between the reference and the measured line voltage in series with the line, i.e.

$$v_c = v_t - v_{t,desired} \tag{3.8}$$

The power rating of the converter for this device depends on the magnitude of disturbances experienced, but will be less than the load power rating. The response time of the compensator is less than one fundamental cycle. As a series compensator it has the disadvantage of having to carry the full load current with the appropriate short circuit rating and it also needs an energy storage system for operation, but it is still a promising topology for voltage sag compensation. It has also been proposed to use this topology to compensate for voltage unbalance [70] and voltage flicker [71].

3.2.4.8. Compensators Under Development

Many innovative compensators have been proposed, but to date only laboratory scale experiments have been reported. Only a few will be mentioned here. The Power Quality Manager has the same topology as the Hybrid Active Filter but is also able to regulate line voltage and do flicker compensation [75]. The Active Power Quality Conditioner consists of a six-pulse converter for voltage regulation and a PWM converter for active filtering [76]. The Unified Power Flow Controller was proposed as a device to control power flow in transmission systems, but because of its flexibility it also shows promise as a power quality compensator [77].

3.3. Drive Topology Modifications for Voltage Sag Ride-through

Instead of adding additional equipment in order to protect the ASD, it is possible to modify the topology and/or the control strategy of the ASD in order to provide it with voltage sag ride-through. Some manufacturers already have ASD models on the market with the capability to resynchronize the ASD output into a spinning motor [27]. In order to provide momentary interruption ride-through it is necessary to interface the ASD to an energy storage system and this will be discussed separately in section 3.4.

An ASD can have either a passive (diode bridge) or active (transistor) rectifier, but the vast majority of ASDs have a passive rectifier, because active rectifier ASDs are more expensive and more complex.

Active rectifiers are used when a bi-directional (four quadrant) drive is needed and/or where the harmonics generated by the drive need to be limited.

For an ASD with a passive (diode bridge) rectifier, the dc bus voltage is directly proportional to the line voltage. As the ac line voltage drops during a sag condition, the nominal dc bus voltage is still imposed on the dc bus capacitance and the diodes in the rectifier become reverse biased. The load power is then drawn from the dc bus capacitance, which discharges the capacitance and the dc bus voltage drops. This drop in dc bus voltage continues until the ASD trips or the rectifier diodes are once more forward biased and the rectifier is able to supply the load power to the inverter. The dc bus voltage will remain at this lower voltage, until the input ac voltage is restored to its nominal value.

For an ASD with an active (transistor) rectifier, the dc bus voltage is regulated by controlling the input current to the rectifier. When the input voltage suddenly drops during a voltage sag condition, the input power to the rectifier becomes less than the load power required by the inverter and the inverter draws power from the dc bus capacitance, which results in a drop in dc bus voltage. The dc bus voltage continues to drop until the dc bus voltage regulator has increased the rectifier input current to where the rectifier is again supplying all of the load power to the inverter. If the required rectifier input current exceeds the current rating of the rectifier, the rectifier is not able to regulate the dc bus voltage and the drive trips.

3.3.1. Drive Topology Modifications for ASD with Passive or Active Rectifier

For both a passive and active rectifier ASD therefore, the dc bus voltage drops due to the dc bus capacitor being discharged when power is drawn from it. From this observation several ways of extending the ride-through time of an ASD can be arrived at. The first is increasing the dc bus capacitance, although it has been shown [53] that the number of capacitors needed to provide ride-through for a few seconds is exorbitant. It is not a viable solution due to the cost and space which would be required by the capacitors.

Another option is to derate the ASD in order to provide a margin for operation under sag conditions. The ASD can be derated by using an ASD rated at a higher voltage, output power or output frequency than the motor. When a higher voltage ASD is used, the dc bus voltage is much higher than the minimum voltage required to deliver rated voltage and current to the motor load, so there is a greater margin for change in the dc bus voltage. The disadvantage to this approach is that the motor has to be equipped with sufficient insulation to handle the higher peak voltages imposed on it [53][54].

Ride-through time can also be extended by using an ASD with a higher power rating than the load. Drives are designed to provide ride-through of a voltage sags for a short time, in the order of milli-seconds, at rated output power. At lower power levels, ride-through can be provided for a longer time. The same result can be achieved by operating the ASD at a lower output frequency than what it is rated for. Non-critical fan and pump loads are good candidates for this scheme [53][54], but cost/benefit

characteristics of these methods need to be critically evaluated. The above mentioned ride-through strategies, the addition of capacitors or derating of the ASD, can provide ride-through for a short duration only, and the ride-through time is determined by the depth of the sag. More advanced topology modifications will be necessary to meet the specification to ride through the most common voltage sags with magnitudes of up to 40% and duration of up to 60 cycles.

3.3.2. Use of Load Inertia for Ride-through for Non-critical Loads

ASDs with an active or passive rectifier can drive either critical or non-critical loads. Critical loads are defined as those which cannot tolerate any decrease in speed whereas non-critical loads experience no significant loss of performance due to a loss in speed, as long as the speed returns to nominal after the disturbance. Critical loads are mostly found in continuous processes such as in paper mills and the textile industry.

Where a loss in speed can be tolerated, the inverter can be operated at a slightly lower frequency than synchronous, thereby achieving generator action supporting the dc bus voltage. Load energy is used to support the dc bus voltage which keeps the ASD from tripping and enables the ASD to continue operation once the sag condition is cleared. However, the load is not supported through this action resulting in a loss of speed and limiting this ride-through scheme to use with non-critical loads. Still, this is an effective method for keeping the ASD from tripping and is available in some commercial drives [53]. The duration of sags for which this method provides ride-through depends on the load inertia, but in general the applicability is restricted to short duration power quality problems.

3.3.3. Addition of Boost Converter to ASD with Passive Rrectifier

For an ASD with a passive rectifier, the dc bus voltage is proportional to the input line voltage. By adding a boost converter between the rectifier and inverter, as shown in Figure 33, the dc bus voltage as seen by the inverter can be regulated.

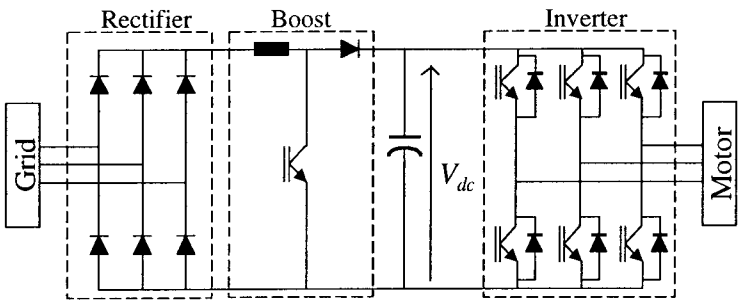


Figure 33 Adjustable speed drive with passive rectifier

In order to deliver the required power to the inverter at a reduced input voltage, the input current to the rectifier will have to be increased and the rectifier and boost converter have to be derated to handle the increased current. As long as the devices are rated for continuous operation at the increased current, ride-through for sags of any duration can be provided.

A standard ASD can also be retro-fitted with a boost converter, as shown in Figure 34. The rectifier which is part of the standard drive will become reverse biased with the boost converter regulating the dc bus voltage and the load power will be delivered to the inverter through the retrofit rectifier and boost converter. Another variation is to modify the rectifier so that it has two positive outputs and a boost converter is provided at the output of one of the rectifiers, as shown in Figure 35.

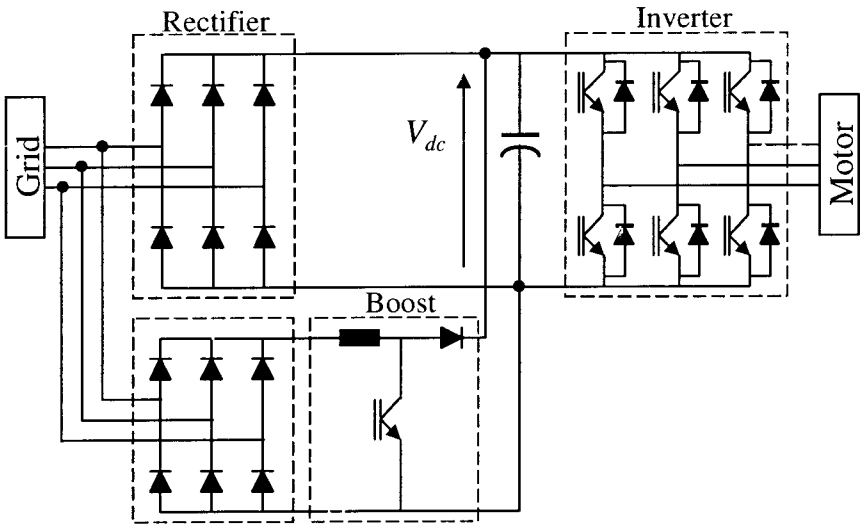


Figure 34 Retrofit addition of boost converter to ASD with passive rectifier

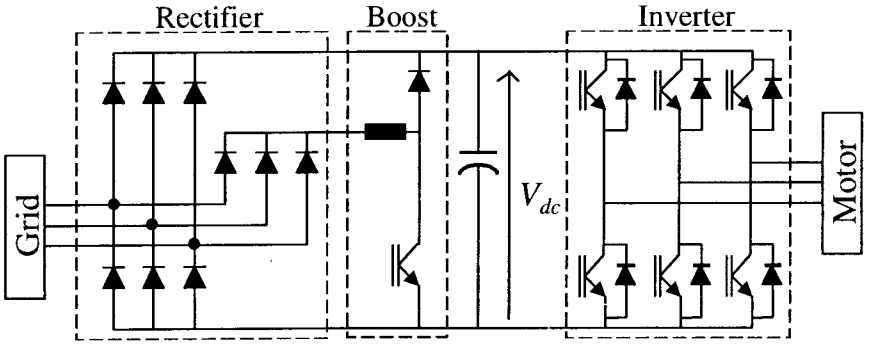


Figure 35 Variation of addition of boost converter to ASD for ride-through using brake resistor

The advantage of this method is that the load current only flows through the inductor and diode of the boost converter during power disturbances, and only half of a three phase diode bridge has to be added. It has been suggested to use the transistor provided for the brake resistor of the ASD in the boost converter [55] in order to save on cost.

The ASD with a passive rectifier/boost converter combination is able to provide ride-through of voltage sags of unlimited duration, assuming appropriate rating of devices, but the magnitude of sags for which ride-through can be provided is limited by the current rating of the rectifier and boost converter devices. The limit on the magnitude of sags for which ride-through can be provided by these methods can also be viewed as a limit on the ratio of dc bus voltage to input voltage for the boost converter [56].

The different drive topology modifications for voltage sag ride-through for ASDs discussed in this section are summarized in Table 8.

3.4. Energy Storage System for Momentary Interruption Ride-through

Several different drive topology modifications which can provide ASDs with voltage sag ride-through have been presented, but these are only able to provide ride-through for sags of limited magnitude. In order to provide an ASD with ride-through of deep sags and momentary interruptions, it is necessary to interface the ASD to an energy storage system, as discussed in Chapter 2. The interfacing of an energy storage system to an ASD with no modifications will be discussed here, although it can be used in addition to implementing any of the drive topology modifications presented in the previous section to extend their ride-through capabilities. Although several different interface circuits between an ASD and energy storage system were presented in Chapter 2, the simplest way to support the dc bus voltage of an ASD is to connect the energy storage system to the dc bus, as shown in Figure 36.

The comparison of different energy storage technologies in Chapter 2 showed that ultra-capacitors are very well suited to this application and results from a commercial ultra-capacitor energy storage system [44] designed for an ASD with a passive rectifier and a nominal dc bus voltage of 650V, are presented here. The ultra-capacitor system is rated for 100kW maximum output power and consists of an ultra-capacitor bank with a nominal capacitance of 12F, a charger and a boost converter, as shown in Figure 37.

Table 8 Methods of providing voltage sag ride-through for ASDs

Rectifier type	**Critical or non-critical load**	**Only non-critical load**
Passive or active	Additional capacitors on dc bus	Load inertia
	Derate ASD to obtain margin for ride-through	
Only passive	Add boost converter on dc bus	

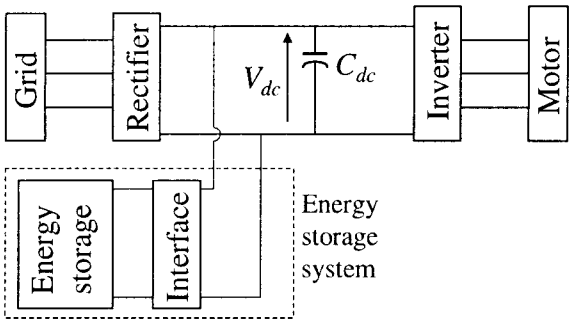


Figure 36 Energy storage system interfaced to dc bus of ASD

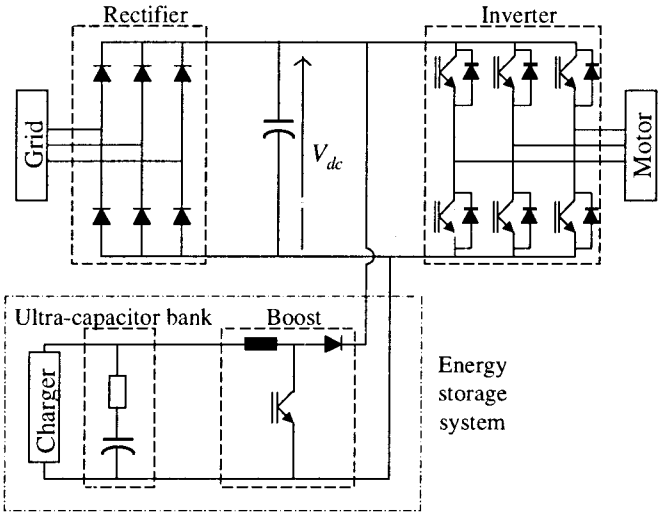


Figure 37 Ultra-capacitor energy storage syste interfaced to an ASD with a passive rectifier

The charger is connected to the dc bus and the ultra-capacitor bank is charged to 448V. The reference dc bus voltage for the boost converter is set to 90% of nominal, i.e. 585V and the ultra-capacitor system is engaged if the dc bus voltage drops below 585V. The system response to a momentary interruption lasting 3 seconds with a 100kW load is shown in Figure 38 [44]. As the dc bus voltage drops below 585V as a result of the momentary interruption, the ultra-capacitor system is engaged and regulates the dc bus voltage to 585V for the duration of the outage. The minimum dc bus voltage is less than 585V because the voltage continues to drop until the output power of the boost converter equals or exceeds the inverter input power. This drop in dc bus voltage is shown in more detail in Figure 39 [44]. The ultra-capacitor system is able to deliver 100kW for 5 seconds and at lower output power it is able to provide ride-through for a longer period of time [44]. In Chapter 5 it is investigated if this ultra-capacitor system can be interfaced to an ASD with an active rectifier to provide momentary interruption ride-through.

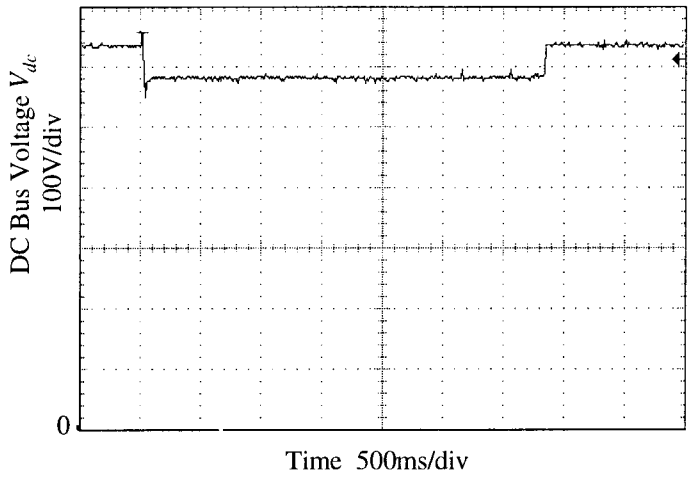


Figure 38 System response to a momentary interruptions with 100kW load.

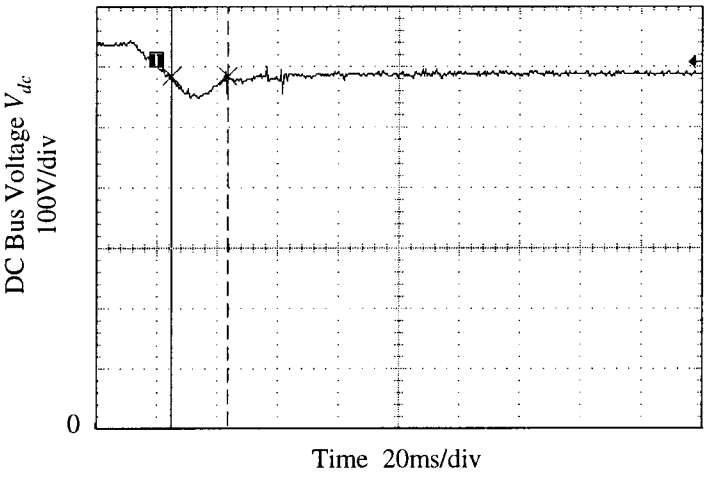


Figure 39 Dc bus voltage response at onset of momentary interruption

3.5. CONCLUSIONS

Several solutions for voltage sag ride-through of ASDs have been suggested in the literature and/or implemented commercially and a classification of the different strategies were presented. Several compensators are available and a discussion of the two generalized compensation techniques, series and shunt compensation, was given as well as a qualitative comparison of a number of different power quality compensators. Compensators can be implemented on either the utility or customer side, but if it is implemented at a substation on the utility side, it will have to be rated to protect the total substation load, which will include critical and non-critical loads.

If a compensator is added on the customer side and the critical loads are supplied on a different distribution system than the non-critical loads, the compensator can be added to the critical distribution system which would reduce the rating of the compensator required. It is however seldom the case that critical loads are supplied on a separate system and therefore it is proposed that it is better to enhance the voltage sag ride-through ability of ASDs than to add compensators in the distribution system.

The ride-through ability of ASDs can be enhanced by appropriate drive topology and/or control system modifications. Possible drive topology modifications include the derating of the ASD and the addition of a boost converter to the dc bus of an ASD with a passive rectifier. These modifications can only provide ride-through for sags of limited magnitude and the addition of an energy storage system is required for momentary interruption ride-through. Experimental results from a commercial ultra-capacitor system which can be interfaced to an ASD with a passive rectifier was presented.

Most strategies for ASD drive topology modifications focus on ASDs with passive (diode bridge) rectifiers because they hold the largest share of the market. However, ASDs with active rectifiers offer additional features of regeneration and a cleaner harmonic interface to the power system and it is expected that their market share will increase as harmonic regulations are more strictly enforced and a greater awareness of the adverse effects of harmonics on electrical equipment comes about. It was therefore decided that a study on the voltage sag ride-through ability of ASDs with active rectifiers would be a valid research contribution in light of the lack of work in this area and the expected growth in the market for ASDs with active rectifiers in the future.

4. SAG RIDE-THROUGH FOR ASD WITH ACTIVE RECTIFIER

4.1. INTRODUCTION

For an ASD with an active rectifier, the rectifier only has to process the active power delivered to the load in order to regulate the dc bus voltage. The rectifier is therefore often operated at unity displacement power factor and for the purposes of this discussion it is assumed that this is the case. For a typical motor load operating at a lagging power factor, the rectifier therefore processes less current than the inverter. For equivalent inverter and rectifier ratings, it follows that some percentage of the current capacity of the rectifier can be used to provide voltage sag ride-through to the ASD. In the following derivation and discussion, it is assumed that all quantities are rms, unless otherwise quantified. A simple line diagram of an ASD with an active rectifier is shown in Figure 40.

The dc bus voltage drops during a sag condition due to an active power imbalance between the rectifier and inverter which results in energy being extracted from the dc link capacitor. To regulate the dc bus voltage of the ASD during sags it is therefore necessary to ensure that the same active power is supplied by the rectifier during the sag as before the sag, i.e.

$$\sqrt{3}V_{ll0}I_{rec0} = \sqrt{3}V_{ll,sag}I_{rec,sag} \tag{4.1}$$

with V_{ll0} and I_{rec0} the input line voltage and current respectively before the onset of the sag and $V_{ll,sag}$ and $I_{rec,sag}$ the voltage and current during the sag. It is assumed that balanced three phase sags are experienced and the input line voltage during the sag can therefore be expressed as $V_{ll0}(1-sag)$, where sag is the sag magnitude in per unit.

$$\sqrt{3}V_{ll0}I_{rec0} = \sqrt{3}V_{ll0}(1-sag)I_{rec,sag} \tag{4.2}$$

This means that the rectifier input current will have to increase by the factor κ where

$$\kappa = \frac{I_{rec,sag}}{I_{rec0}} = \frac{1}{1-sag} \tag{4.3}$$

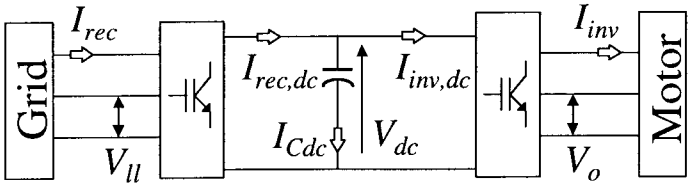


Figure 40 Line diagram of ASD with active rectifier

The ASD can regulate the dc bus voltage under sag conditions as long as the rectifier input current during the sag $I_{rec,sag}$ does not exceed the current rating of the rectifier devices, i.e.

$$I_{rec,sag} = \frac{1}{1-sag} I_{rec0} \leq I_{rec,\max} \tag{4.4}$$

therefore the sag magnitude for which ride-through can be provided is limited to

$$sag \leq 1 - \frac{I_{rec0}}{I_{rec,\max}}. \tag{4.5}$$

Although the previous discussion assumes balanced three phase sags, this concept can be extended to unbalanced sags by recognizing that (4.1) can be re-written as

$$\sqrt{3} V_{ll0} I_{rec0} = (V_{a,sag} + V_{b,sag} + V_{c,sag}) I_{rec,sag} \tag{4.6}$$

where it is assumed that the rectifier input currents are controlled to be balanced in magnitude and each phase current is in phase with one of the phase voltages, and that balanced conditions exist before the onset of the sag. This leads to a sag limit for unbalanced sags of

$$\frac{sag_a + sag_b + sag_c}{3} \leq 1 - \frac{I_{rec0}}{I_{rec,\max}} \tag{4.7}$$

where $sag_{a,b,c}$ are the sag magnitudes for the individual phases.

The rectifier input current before the sag, which reflects the load condition of the ASD, determines the factor by which the current can be increased before it reaches the device rating. The maximum sag magnitude for which ride-through can be provided with nominal input line voltage V_{ll0} at 480V and a constant power load of 100kW, i.e. nominal input current of 133A if an efficiency of 95% is assumed for both the inverter and rectifier, is shown as the current rating of the rectifier is varied in Figure 41. In Figure 42, the maximum sag magnitude for which ride-through can be provided with a constant current rating for the rectifier of 200A is shown as the load power is varied. These results are with efficiencies of 95% assumed for both the rectifier and inverter.

In order to further quantify the maximum sag for which ride-through can be provided by drawing more current through the rectifier, it is assumed that the inverter and rectifier have similar ratings and that the rectifier is operated at unity input power factor. The inverter devices are rated at the maximum dc bus voltage V_{dc} and the current rating is determined by the worst case condition of supplying rated apparent power $S_{inv,rated}$ to the load at the minimum fundamental output voltage $V_{o,min}$, i.e.

$$I_{inv,rated} = \frac{S_{inv,rated}}{\sqrt{3} V_{o,\min}} \tag{4.8}$$

Assuming the same device rating for the rectifier, the rms rectifier current needs to be limited to less than $I_{inv,rated}$. Sinusoidal ac current is assumed for both the inverter and rectifier. Since the rectifier is controlled to operate at unity power factor, it only supplies the active power $P_{inv,out}$ to the load.

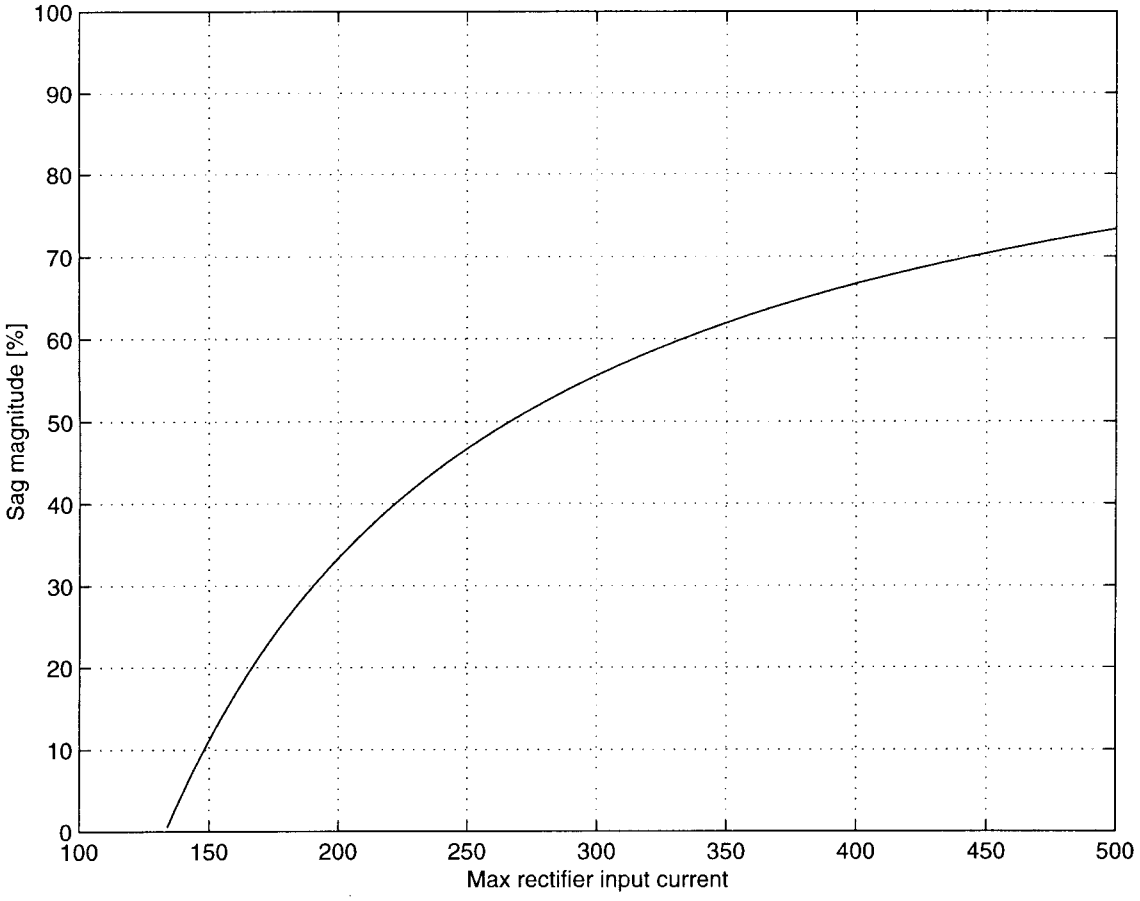


Figure 41 Maximum sag ride-through which can be provided as a function of rectifier current rating

Based on this discussion, the resulting rms rectifier input current during the sag is limited to:

$$I_{rec,sag} = \frac{P_{inv,out}}{\sqrt{3}V_{ll0}(1-sag)\eta_{inv}\eta_{rec}} \leq \frac{S_{inv,rated}}{\sqrt{3}V_{o,\min}} \tag{4.9}$$

Consequently, for similar rectifier and inverter ratings, the sag magnitudes for which ride-through can be provided are limited to:

$$sag_0 \leq 1 - \frac{P_{inv,out}V_{o,\min}}{S_{inv,rated}V_{ll0}\eta_{inv}\eta_{rec}} \tag{4.10}$$

The sag magnitude sag_d for which ride-through can be provided by derating the rectifier depends on the factor K_d by which the rating of the rectifier is increased and on the sag ride-through capability sag_0 of the drive before derating, i.e.

$$sag_d = 1 - \frac{1-sag_0}{K_d} \tag{4.11}$$

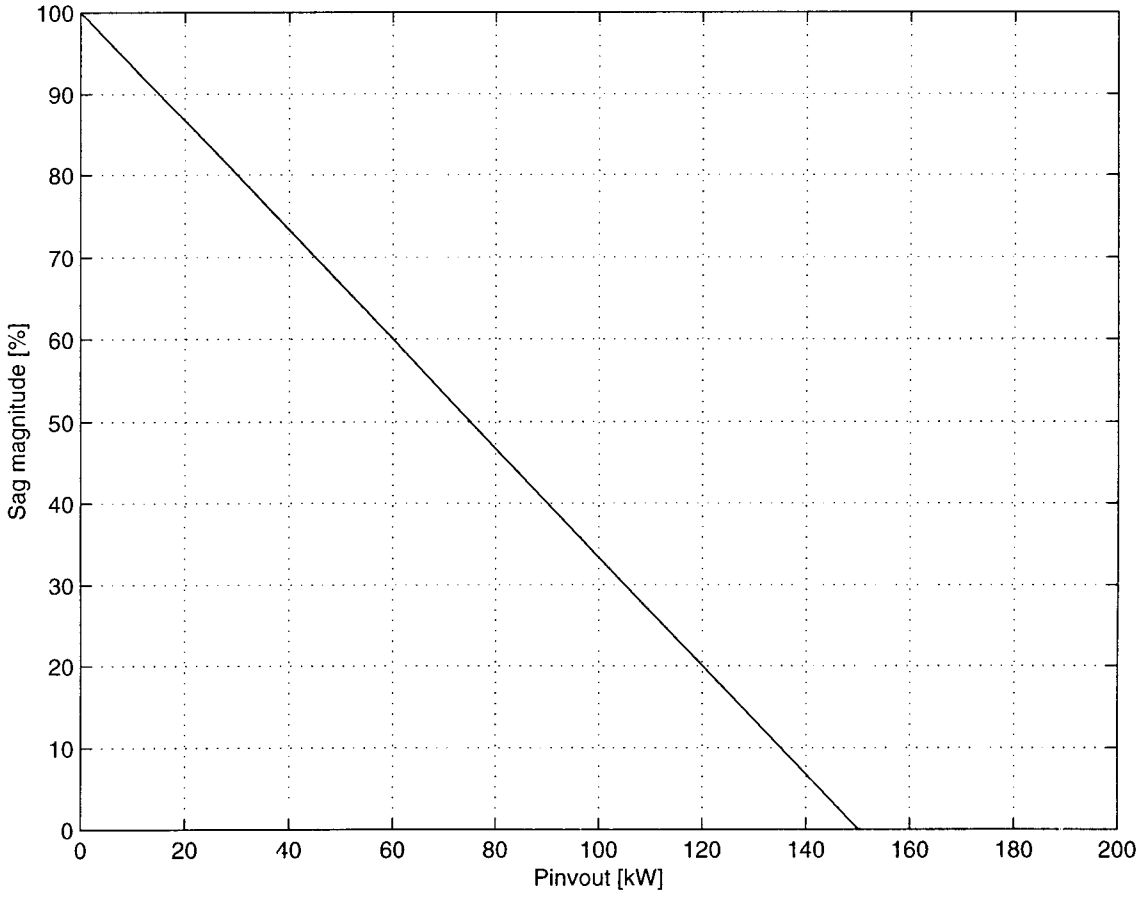


Figure 42 Maximum sag ride-through which can be provided as a function of load power

For example, for an induction motor load operating at 85% load with rectifier and inverter efficiencies of 95% and $V_{o,min}$= $0.9V_{ll0}$, voltage sag ride-through for sags of up to 15% and of any duration can be provided without derating of the rectifier, i.e. sag_0 = 0.15. By derating the rectifier by a factor of 1.5, ride-through for sags of up to 43% can be provided at full load. Since the majority of sags are of a magnitude of less than 40%, the derating of the rectifier will prevent tripping of the drive under the majority of sag conditions, improving the process reliability.

In order to design a controller for an ASD with an active rectifier to regulate the dc bus voltage, a mathematical model describing the behavior of the average value of the dc bus voltage is developed which assumes a constant load, i.e. constant inverter output power. The derivation of the state variable description, controller design, simulation results, implementation and experimental results are presented.

4.2. State Variable Description

The dc bus voltage controller objective is to keep the dc bus voltage fairly constant, which can also be expressed as the objective to keep the energy stored in the dc link capacitor fairly constant, since

$$E_{dc}(t) = \frac{C_{dc} v_{dc}^2(t)}{2}. \tag{4.12}$$

The energy stored in the dc link capacitor is determined by the active power flow through the capacitor, which in turn is determined by the flow of active power through the inverter and rectifier. For example, if the active power processed by the inverter is increased, the average value of the inverter input current $i_{inv,dc}$ will increase which will tend to decrease the average value of v_{dc}. The reactive power processed by the inverter and rectifier determines the high frequency ripple component of $i_{inv,dc}$ and $i_{rec,dc}$ respectively which in turn determines the high frequency ripple component of v_{dc}. It is the average value of the dc bus voltage, V_{dc}, which needs to be regulated, therefore consider the average active power balance for the inverter and the rectifier, which yields

$$V_{dc} I_{inv,dc} \eta_{inv} = P_{inv,out} \tag{4.13}$$

$$\sqrt{3} V_{ll} I_{rec} \eta_{rec} = V_{dc} I_{rec,dc}. \tag{4.14}$$

where it is assumed that the rectifier is operated at unity input power factor and that the inverter output power $P_{inv,out}$ is constant. In order to investigate the performance of the dc bus voltage controller by simulation, a mathematical model describing the behavior of the average dc bus voltage is derived by considering the simplified diagram of the drive shown in Figure 40. The instantaneous dc bus voltage v_{dc} is determined by the instantaneous current i_{Cdc} through the link capacitor C_{dc}, i.e.

$$C_{dc} \frac{dv_{dc}}{dt} = i_{Cdc} = i_{rec,dc} - i_{inv,dc}. \tag{4.15}$$

The current contributions to the dc link capacitor from the rectifier $i_{rec,dc}$ and inverter $i_{inv,dc}$ consist of a dc component and a high frequency component. The active rectifier needs to regulate the average value, or dc component, of the bus voltage V_{dc}, which is determined by the dc component of the above mentioned currents, denoted by $I_{rec,dc}$ and $I_{inv,dc}$. Therefore we can write

$$C_{dc} \frac{dV_{dc}}{dt} = I_{Cdc} = I_{rec,dc} - I_{inv,dc}. \tag{4.16}$$

From (4.13) we know that

$$I_{inv,dc} = \frac{P_{inv,out}}{\eta_{inv} V_{dc}} \tag{4.17}$$

and from (4.14) we have

$$I_{rec,dc} = \frac{\sqrt{3} V_{ll} I_{rec} \eta_{rec}}{V_{dc}}. \tag{4.18}$$

By substituting (4.17) and (4.18) in (4.16), the following non-linear differential equation describing the behavior of the average dc bus voltage is obtained

$$\frac{dV_{dc}}{dt} = \frac{\sqrt{3}V_{ll}I_{rec}\eta_{rec}}{C_{dc}V_{dc}} - \frac{P_{inv,out}}{C_{dc}V_{dc}\eta_{inv}}. \tag{4.19}$$

A sudden change in either V_{ll} or $P_{inv,out}$ causes a power imbalance between the inverter and rectifier with a resulting change in V_{dc}. The dc bus voltage regulator has to regulate the dc bus voltage under sag and load change conditions. The control problem is to determine a suitable I_{rec} which will regulate the dc bus voltage V_{dc} to the reference V_{dc}^*. We can write (4.19) in standard control system notation

$$px_1 = \frac{u_1u_c - u_2}{x_1} \tag{4.20}$$

by defining quantities as listed in Table 9. The independent inputs u_1 and u_2 are not known, in fact, only the dc bus voltage, i.e. state variable x_1, is measured. Also, it is the average value of the dc bus voltage which needs to be regulated and the dc bus voltage controller should therefore only react to fluctuations in the average value of the dc bus voltage. This requires filtering of the measured dc bus voltage and the selection of an optimal speed of response for the control system. If the control system responds too fast, it will respond to high frequency fluctuations in the dc bus voltage and if its response is too slow, the dc bus voltage regulation will be poor during sag conditions.

4.3. System Stability

The system described in (4.20) is non-linear because of the division of the inputs by the state and system stability is investigated by using the tests for non-linear systems introduced by Liapunov [37]. Liapunov's first method provides information about the stability of an equilibrium state and the stability of the system in (4.20) is examined at the equilibrium state $x_1 = V_{dc}^*$. To employ Liapunov's first method, it is necessary to examine the autonomous system, i.e. $px_1 = f(x_1,\boldsymbol{u})$ with $\boldsymbol{u} = \boldsymbol{0}$.

Table 9 Definition of symbols used in control system notation

Symbol	Definition	Type	Description
p	d/dt	operator	derivative
x_1	V_{dc}	state variable	dc bus voltage
u_1	$\sqrt{3}V_{ll}\,\eta_{rec}/C_{dc}$	independent input	rectifier input voltage $\times\sqrt{3}\times\eta_{rec}/C_{dc}$
u_2	$P_{Inv,out}/\eta_{inv}/C_{dc}$	independent input	inverter output power $/\eta_{inv}/C_{dc}$
u_c	I_{rec}	controlled input	rectifier input current

The autonomous system in this case is described by

$$px_1 = \frac{0}{x_1} = 0, \tag{4.21}$$

therefore Liapunov's first method cannot be used. Liapunov's direct method is not limited to local stability and can provide information about system stability in a neighborhood around an equilibrium state. If the neighborhood is unlimited, the system is globally stable. In order to use Liapunov's direct method to examine the stability of the system, the following energy function is chosen.

$$V(x_1) = \frac{x_1^2}{2} \tag{4.22}$$

The derivative of the energy function is

$$pV(x_1) = \frac{\partial V}{\partial x_1} \times px_1 = x_1 \left(\frac{u_1 u_c - u_2}{x_1} \right) = u_1 u_c - u_2 \tag{4.23}$$

The system is stable for $pV(x_1) \leq 0$, therefore it can be determined that the system is stable for $u_1 u_c - u_2 \leq 0$, written in expanded form as

$$\sqrt{3} V_{ll} I_{rec} \eta_{rec} \leq \frac{P_{inv,out}}{\eta_{inv}}. \tag{4.24}$$

The system is therefore stable as long as the input power of the inverter equals or exceeds the output power of the rectifier, i.e. when energy is being extracted from the dc link capacitor. No conclusion can be reached through this method using the energy function in (4.22) as to the stability of the system when energy is being added to the dc link capacitor.

It was investigated if another energy function could be found which would provide information about the stability of the system over a wider range of operating conditions. This proved to be impossible because the derivative of the energy function $pV(x_1)$ in (4.23) contains the term $(u_1 u_c - u_2)$ which depends on the operating point. In order to negate the effect of this term in the derivative of the energy function, the energy function should contain this term, but this makes the energy function dependent upon the operating point and it is therefore impossible to find an energy function which is positive or zero for all values of x_1.

Although the stability of the system could not be ascertained under all operating conditions, it is known that a proportional-integral (PI) controller can be employed to regulate the dc bus voltage of an ASD with an active rectifier and therefore two non-linear controllers, a Liapunov and adaptive PI controller, are designed under the assumption that the system will behave in a stable manner.

4.4. CONTROLLER DESIGN

4.4.1. Liapunov

A Liapunov controller is designed for the non-linear system described in (4.20). The first step is to move the equilibrium state to the origin, therefore define $x = V_{dc}^{*} - x_1$. We then have $px = -px_1$ and the system described in terms of the new state variable x, is

$$px = \frac{u_2 - u_1 u_c}{V_{dc}^{*} - x} \tag{4.25}$$

Choose as a Liapunov energy function

$$V(x) = \frac{x^2}{2} \tag{4.26}$$

and calculate $-pV(x,\boldsymbol{u})$

$$-pV(x,\bar{u}) = -\frac{\partial V}{\partial x} px = -x\left(\frac{u_2 - u_1 u_c}{V_{dc}^{*} - x}\right). \tag{4.27}$$

A maximum $-pV(x,\boldsymbol{u})$ will minimize system response time to the origin. It follows from (4.27) that, for a positive (negative) error, i.e. $x>0$, the maximum (minimum) value of u_c, i.e. input rectifier current, will yield the fastest system response. The Liapunov design therefore yields a bang-bang controller which oscillates between the maximum and minimum values of rectifier input current. The rectifier input current will therefore have the maximum rated magnitude with phase changes of 180° as the polarity of the dc bus voltage error changes, as shown in Figure 43 with $I_{rec,max(peak)}$ = 350A.

The distorted current waveform which results from this type of controller will distort the rectifier input voltage waveform which will make it impossible to connect equipment sensitive to voltage distortions to the same line and the bang-bang Liapunov controller can therefore not be used for this application.

4.4.2. Adaptive PI Control

Only the state variable V_{dc} is measured and therefore the presence of a voltage sag condition has to be determined from the response of the dc bus voltage. Usually a PI controller is employed to regulate the dc bus voltage, with acceptable steady state performance.

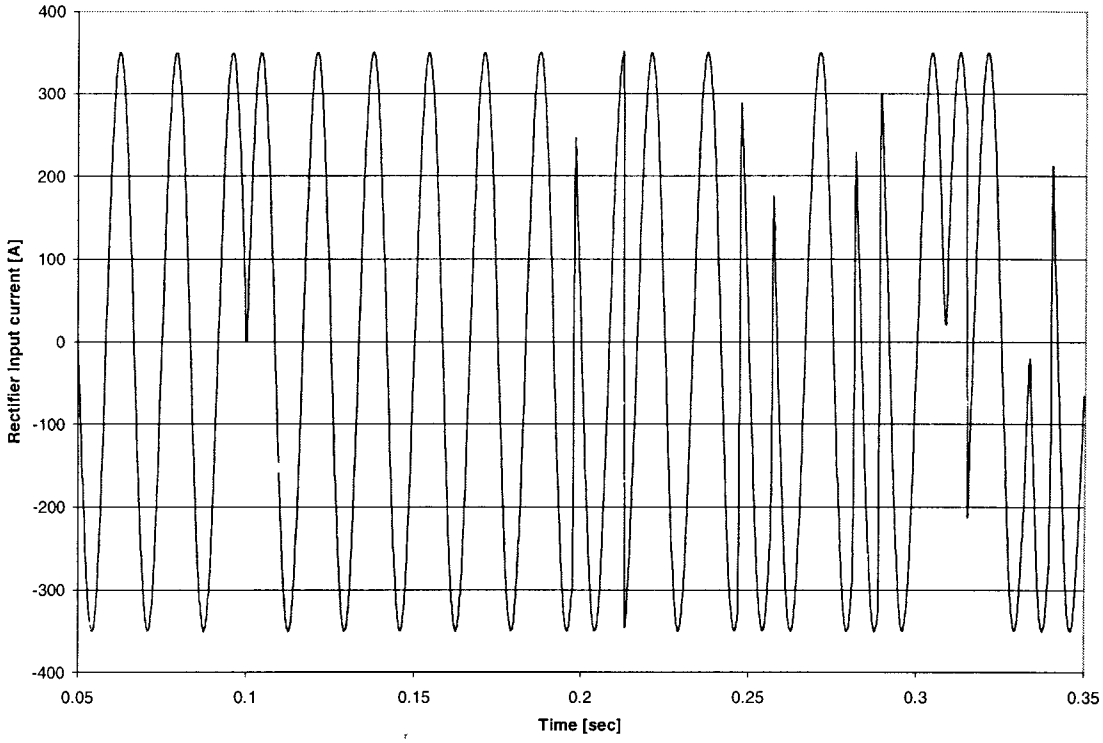


Figure 43 System response with Liapunov controller

For the system in (4.20) under PI control and choosing state variables $x_1 = V_{dc}$ and $x_2 = u_c = I_{rec}$, the state equations for the dc bus voltage regulator become

$$px_1 = \frac{u_1 x_2 - u_2}{x_1}$$
$$px_2 = K_{ir}\left(V_{dc}^* - x_1\right) - K_{pr}\left(\frac{u_1 x_2 - u_2}{x_1}\right) \qquad \textbf{(4.28)}$$

The structure of the closed loop system is shown in Figure 44.

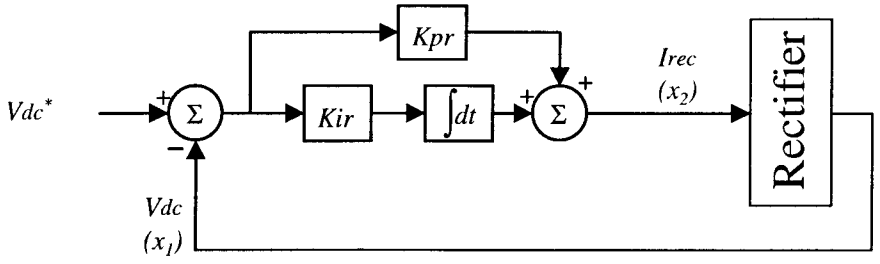


Figure 44 Structure of PI controller

When a voltage sag sets in, very fast controller response is required and therefore it was decided to enhance the performance of the PI controller by adaptively controlling the PI gains. It is not desirable to have too large gains when the error is small, since the controller will then react to the ripple in the dc bus voltage. Hence the PI gains are only adapted once the error $\varepsilon = V_{dc}^{*} - V_{dc}$ exceeds a certain critical error ε_{crit}. The adaptive control rule is the following:

$$\begin{aligned} &if \quad |\varepsilon| > \varepsilon_{crit}, \quad \begin{cases} K_{pr} = K_{pr0} + \alpha_p \times \left\| |\varepsilon| - \varepsilon_{crit} \right\| \\ K_{ir} = K_{ir0} + \alpha_i \times \left\| |\varepsilon| - \varepsilon_{crit} \right\| \end{cases} \\ &else \qquad \begin{cases} K_{pr} = K_{pr0} \\ K_{ir} = K_{ir0} \end{cases} \end{aligned} \tag{4.29}$$

where $\varepsilon = V_{dc}^{*} - x_1 = V_{dc}^{*} - V_{dc}$ and K_{pr0}, K_{ir0}, α_i, α_p and ε_{crit} are constants to be determined.

4.5. Simulation Study of Adaptive PI Controller

The state variable description of the ASD in (4.28) and (4.29) was simulated using *MATLAB*, a high level programming language with built-in ability to solve non-linear differential equations. This state variable description describes the average behavior of the dc bus voltage with an idealized model of the rectifier behavior which models the rms values of the AC voltages and currents and not their instantaneous values. The inaccuracy introduced by modeling the rms values is illustrated by considering the rectifier input current shown in Figure 45.

The output of the adaptive PI controller is a variable DC quantity which is equal to the reference peak value of the AC rectifier input current $I_{rec,pk}$. The reference for the actual AC rectifier input current waveform is generated by multiplying the reference magnitude $I_{rec,pk}$ by a unity sinewave and it is assumed that the rectifier input current I_{rec} is equal to this reference. The absolute value of the rectifier input current is shown in Figure 45. The assumption in the average model of the ASD is that the rms value of the rectifier input current is equal to the reference peak value divided by the square root of two $I_{rec,pk}/\sqrt{2}$ which is different from the rms value calculated over one fundamental period of the rectifier input current $I_{rec,rms}$. The rms value calculated from the rectifier input current waveform lags the assumed rms rectifier current value by an average of half a fundamental period. The rms rectifier current will therefore respond slower than assumed in this model.

The system was also simulated in a power systems electromagnetic transients simulation program, *EMTDC,* which is equipped with a graphical user interface, *PSCAD* [51]. *EMTDC* models each component of the system, including the switching devices, and therefore yields more detailed results than the average model simulated in *MATLAB*. For both simulations, the nominal line to line voltage V_{ll0} is 480V, the reference dc bus voltage V_{dc}^{*} is 800V, the dc link capacitance C_{dc} is 10mF and the inverter is loaded with a constant power load with a nominal value of 100kW. The rectifier is assumed to have a peak current rating of 325A, i.e. rms current rating of 230A.

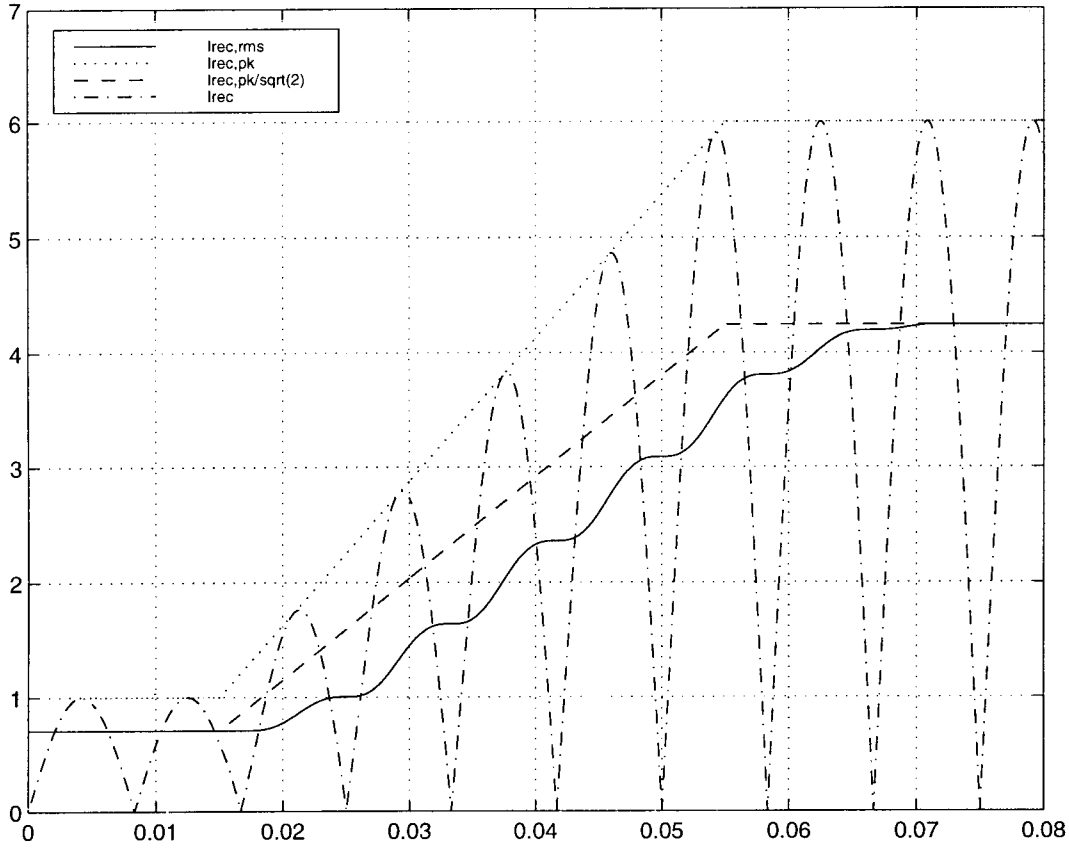


Figure 45 Inaccuracies introduced by modeling of rms values of rectifier input current

Equations (4.28) and (4.29), which describe the average behavior of the ASD, were programmed in *MATLAB* and the program listing is included in Appendix F. The inverter output power $P_{inv,out}$ is constant and equal to 100kW and the rectifier and inverter efficiencies, η_{rec} and η_{inv} respectively, are assumed to be 95%.

The step responses of the dc bus voltage and rms value of the rectifier input current to a sag of 40% are shown in Figure 46 for constant PI gains and adaptively controlled PI gains and the phase trajectories are shown in Figure 47. The PI constants which yielded a good response were iteratively determined as K_{pr0}=0.5 and K_{ir0}=2.5. From the *MATLAB* simulations it was determined that the integral gain K_{ir} determines the speed of approach to the steady state input rectifier current and the proportional gain K_{pr} determines the slope of the phase trajectory. For the adaptively controlled PI gains, the critical error was chosen as 5% of the nominal dc bus voltage, i.e. $\varepsilon_{crit}=0.05\times V_{dc}^{*}$ = 40V, and it was iteratively determined that good results are achieved with α_i= 0.1 and α_p=0.05. The adaptively controlled system shows improved performance by limiting the drop in dc bus voltage to 10%, as compared to 18% for the case with constant PI gains.

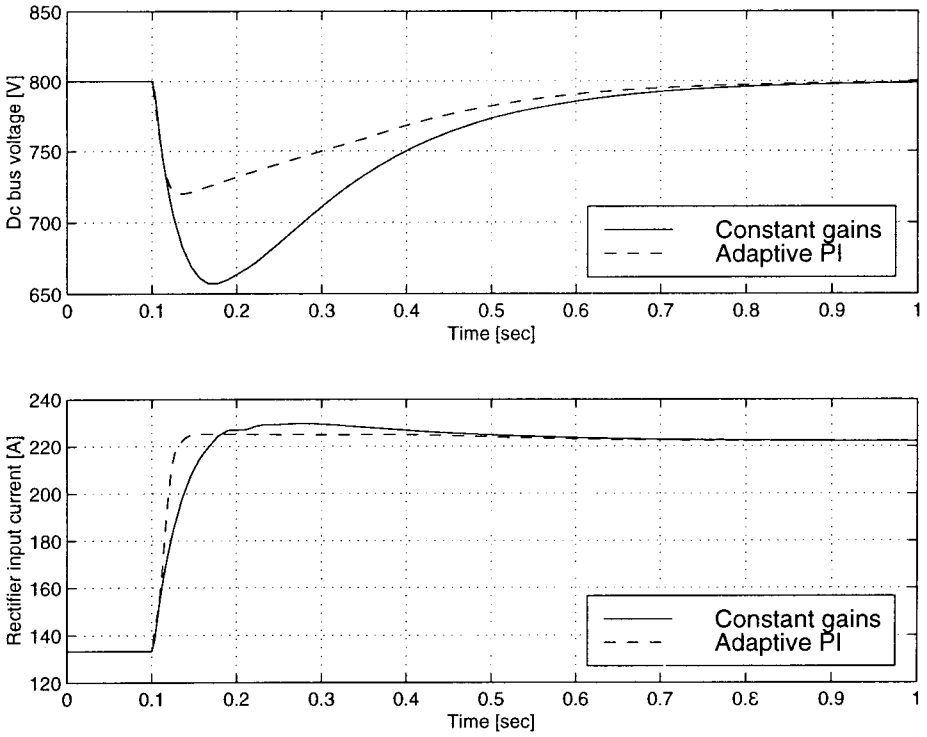


Figure 46 Simulated *(MATLAB)* step response to a 40% sag with $P_{inv,out}$ = 100kW for constant and adaptively controlled gains

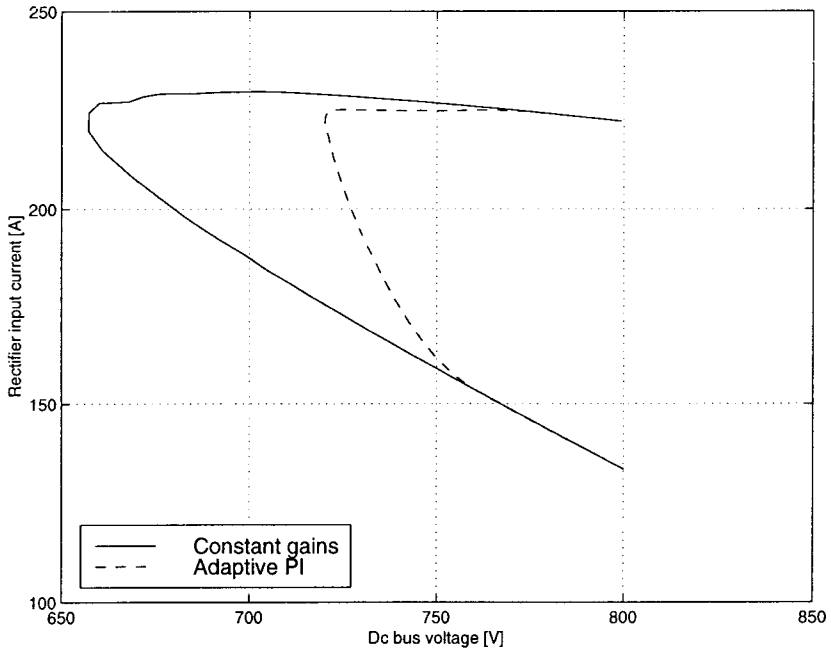


Figure 47 Simulated *(MATLAB)* phase trajectory of step response to 40% sag with constant and adaptively controlled PI gains

To illustrate the effect of the rectifier current limit, the current limit is decreased to 310A peak, and the step responses to a 40% sag with this current limit and adaptively controlled gains are shown in Figure 48. The rectifier is unable to regulate the dc bus voltage because it is not able to deliver the required current.

The system, with similar parameters as used in *MATLAB*, including a rectifier line reactor of 2mH, was also simulated in *EMTDC* to further validate the control scheme. The *EMTDC* simulation is different from the *MATLAB* simulation since it simulates the instantaneous currents and voltages of the ASD and also the reactive power flow through the ASD. Therefore different PI gain constants from those in the *MATLAB* simulations were used. It was found through iteration that gain constants K_{ir} = 5 and K_{pr}=1, with $\alpha_i=\alpha_p=0.02$, yield good results and the adaptive control could be simplified to the following form.

$$\begin{aligned} &if \quad |\varepsilon| > \varepsilon_{crit}, \quad \begin{cases} K_{pr} = K_{pr0} + \alpha_p \times |\varepsilon| \\ K_{ir} = K_{ir0} + \alpha_i \times |\varepsilon| \end{cases} \\ &else \qquad\quad \begin{cases} K_{pr} = K_{pr0} \\ K_{ir} = K_{ir0} \end{cases} \end{aligned} \tag{4.30}$$

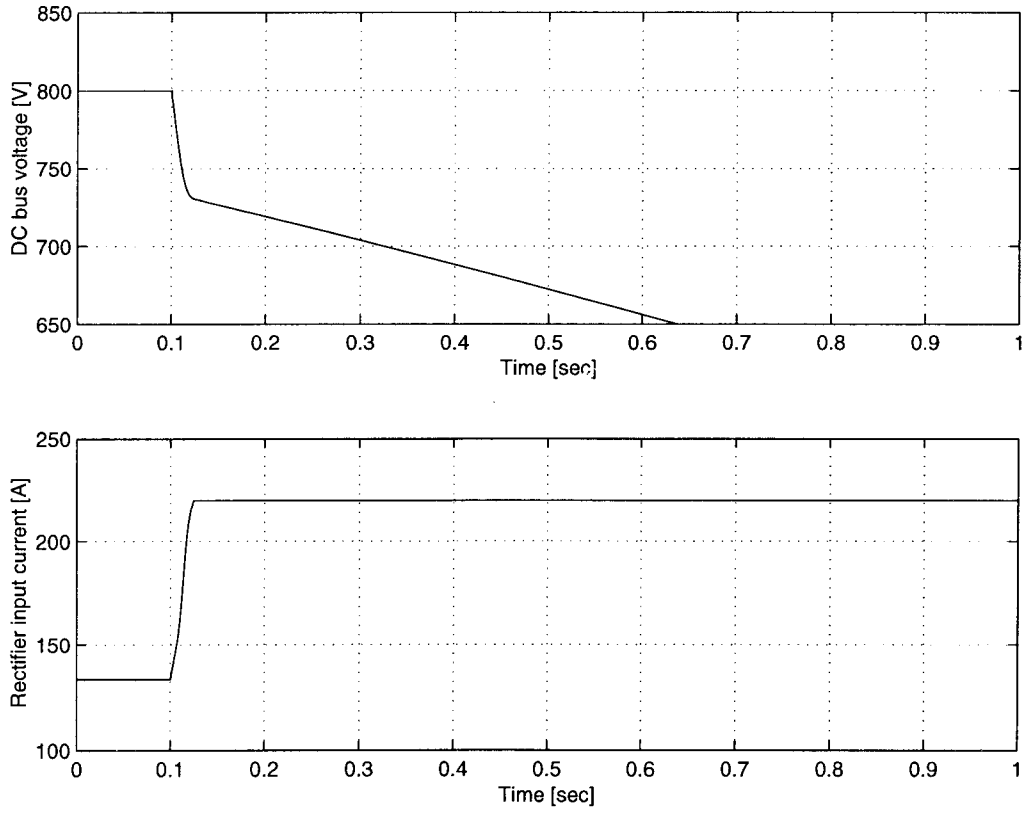


Figure 48 Simulated *(MATLAB)* step response to a 40% sag with adaptively controlled PI gains, and a peak current limit of 310A, i.e. rms current limit of 220A, imposed

The step responses of the dc bus voltage and rectifier input current to a 40% sag with the inverter output power equal to 100kW are compared for constant PI gains in Figure 49, and adaptively controlled PI gains in Figure 50.

A hysteresis band was implemented for the adaptation of the PI gains, keeping the adaptive rule operational until the dc bus voltage error has decreased to less than 10V. The switching action in the rectifier and inverter is simulated by a hysteresis current regulation scheme.

The calculated reference magnitude of the rectifier input current is shown as a dotted line, together with the actual rectifier current. By adaptively controlling the PI gains, the drop in the dc bus voltage is reduced from 17% to 9%. This is the result of the rectifier input current approaching the steady state value for the sag condition faster with the adaptively controlled PI gains. These results support the *MATLAB* results despite the simplifications used in the model simulated in *MATLAB*.

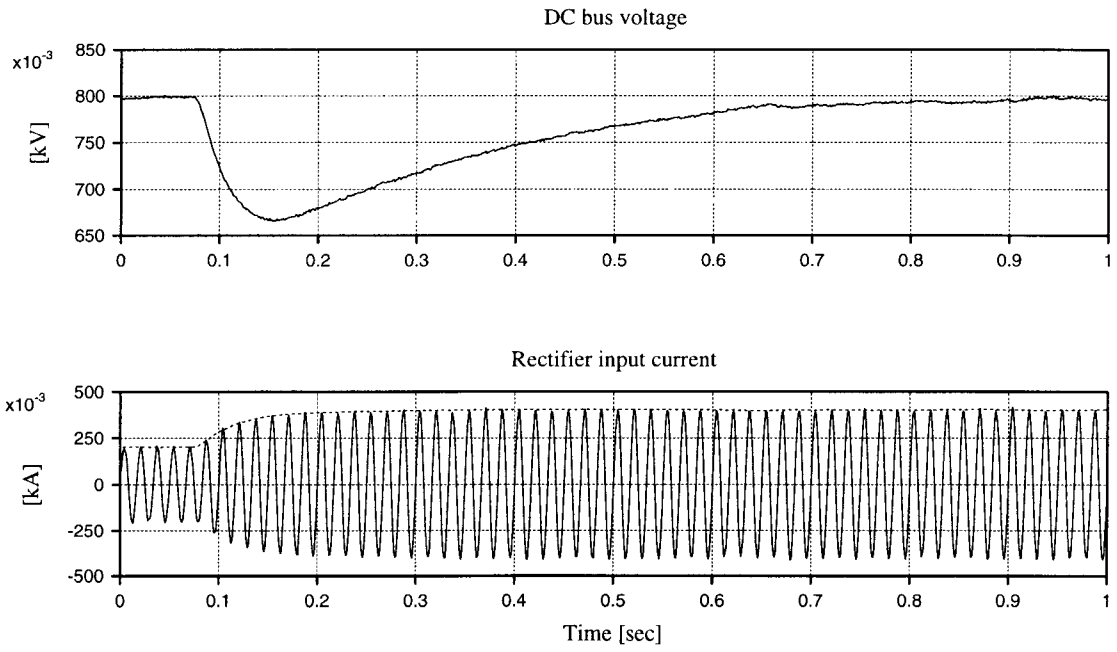


Figure 49 Simulated *(EMTDC)* step response to a 40% sag with constant PI gains

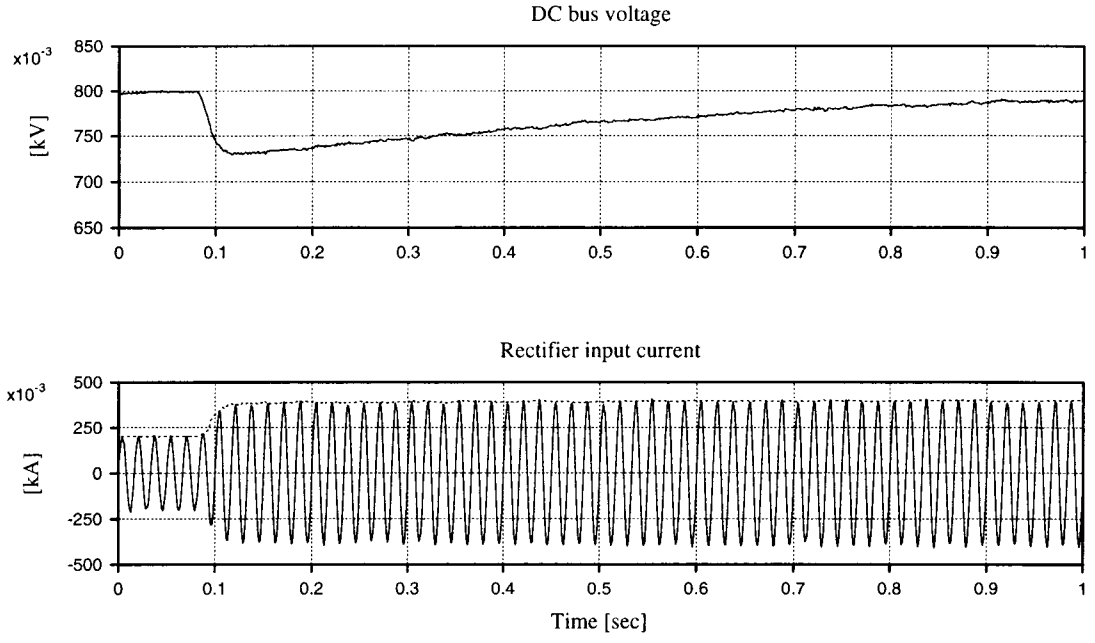


Figure 50 Simulated *(EMTDC)* step response to a 40% sag with adaptively controlled PI gains

4.6. IMPLEMENTATION

The adaptive PI controller was implemented on a 3kVA, IGBT-based laboratory prototype, as shown in Figure 51, with nominal dc bus voltage of 380V, nominal input line-to-line voltage of 230V, rectifier line reactor of 7.5mH and dc link capacitance of 2.48mF [5][7]. The load is an 8 pole induction machine coupled to a regenerative dc drive which can be controlled to act as a fan or pump load. The power supply for the control electronics is connected to a dedicated power supply at nominal input line to line voltage of 230V.

The drive is controlled by two Intel 80196 microcontrollers, dedicated to the rectifier and inverter respectively. The reference rms rectifier input current is calculated at each switching state using a discrete PI controller:

$$I_{rec}^{*}[n] = I_{rec}^{*}[n-1] + K_{ir}T\varepsilon[n] + K_{pr}\left(\varepsilon[n] - \varepsilon[n-1]\right) \qquad \textbf{(4.31)}$$

with T the sampling period

n the sample number index

and $\varepsilon = V_{dc}^{*} - V_{dc}$

Discrete pulse modulation (DPM) is used for the current regulated inverter and rectifier [7]. On the experimental system, different gains from the simulation had to be implemented in order to attain satisfactory operation.

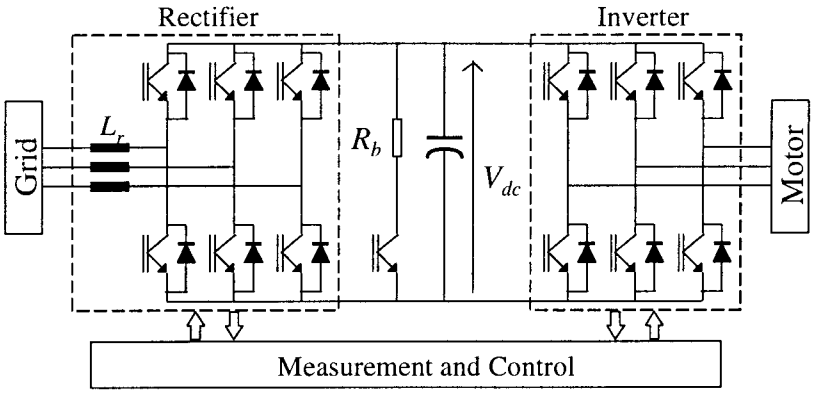


Figure 51 Schematic of experimental ASD

The control rule in (4.29) was implemented, but it was found that a simple gain scheduling control rule yields comparable results and therefore the simpler gain scheduling controller is implemented. The gains are increased by a factor of 5 when the error exceeds 5% of nominal dc bus voltage (19V), i.e.

$$\begin{aligned} &if \quad |\varepsilon| > 19V, \quad \begin{cases} K_{pr} = 3.1 \\ K_{ir} = 0.5 \end{cases} \\ &else \qquad\quad \begin{cases} K_{pr} = 0.6 \\ K_{ir} = 0.1 \end{cases} \end{aligned} \tag{4.32}$$

4.7. Experimental Study

In order to evaluate the drive, the response of the dc bus voltage for sags of different magnitudes with different rectifiers, i.e. a diode bridge rectifier, an active rectifier with constant PI gains and an active rectifier with gain scheduled PI gains, were recorded. A summary of the step responses of the dc bus voltage with a 2kVA load at a 0.5 lagging power factor is presented in Table 10. The minimum dc bus voltage recorded during the sag is given in % of nominal dc bus voltage in Table 10, with nominal dc bus voltage 290V for the diode bridge and 380V for the active rectifier. With scheduled PI gains, the response is faster and, as shown in Table 10, the dc bus voltage does not drop below 95% of nominal.

The measured ratio between the steady state current while the sag persists $I_{rec,sag}$ and the current before the sag I_{rec0} is listed for the active rectifier. This compares well with the theoretical value calculated from (4.3). This factor is also used to determine the allowable sag duration if transient thermal ratings are employed.

The dc bus voltage responses of a diode bridge rectifier, active rectifier with constant PI gains and active rectifier with gain scheduling are compared in Figure 52 for a 40% sag.

Table 10 Responses to Different Sag Conditions

Sag [%]	Minimum V_{dc} [%]			$I_{rec,sag} / I_{rec0}$	
	Passive rectifier	Active rectifier			
	Diode	Constant PI gains	Gain scheduled PI gains	Measured	Theoretical
20	80	93	95	1.3	1.25
40	60	90	95	1.7	1.67
50		87	95	2.1	2

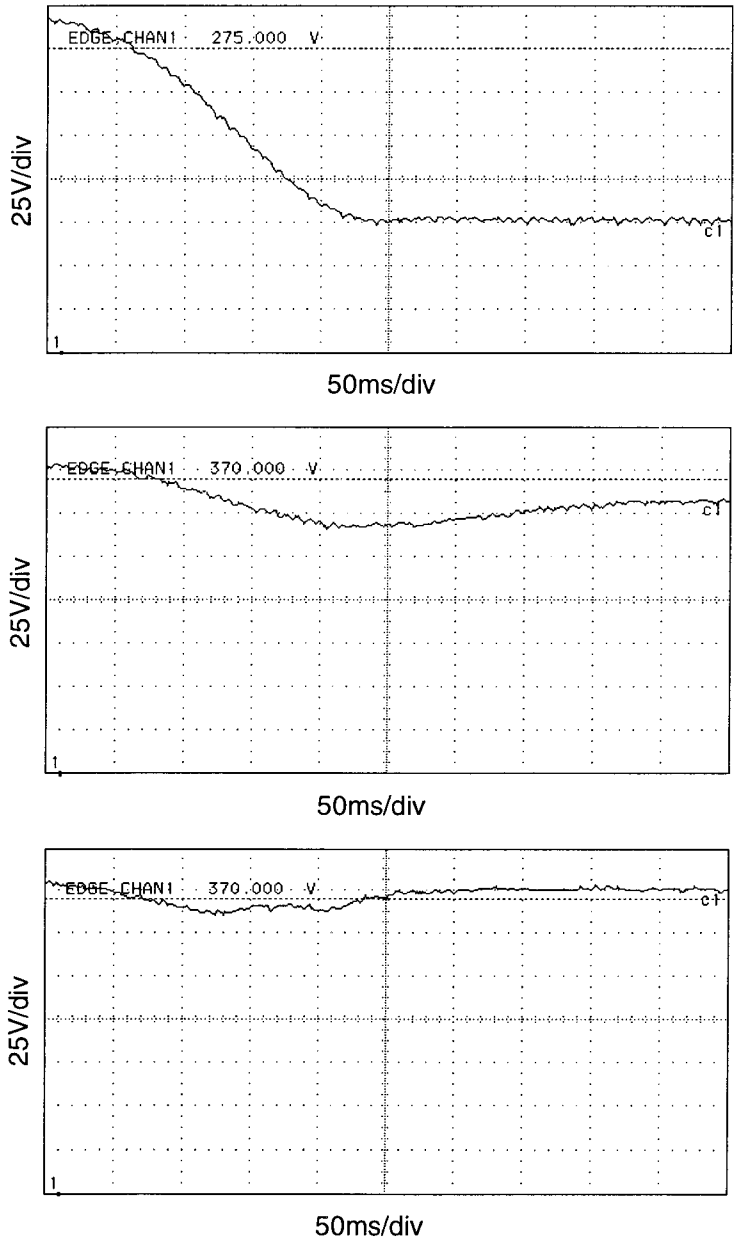


Figure 52 Comparison of experimental dc bus voltage response to a 40% sag of (top) diode bridge, (middle) active rectifier with constant PI gains and (bottom) active rectifier with gain scheduling

With a diode rectifier, the dc bus voltage drops at the onset of the sag and is only restored once the sag condition is removed. Deep sags or sags occurring during heavy loading conditions can cause the dc bus voltage to drop so low that the drive trips. The active rectifier, with and without gain scheduling, regulates the dc bus voltage to the nominal voltage. However, with constant PI gains, the voltage can drop significantly before this is achieved. The drop in dc bus voltage is a function of the load on the ASD, with a larger drop in voltage at higher load conditions due to the higher rate of energy transfer. The active rectifier with scheduled PI gains is able to regulate the dc bus voltage faster because the input rectifier current increases at a faster rate.

The step responses of the dc bus voltage and rms value of the rectifier input current are compared for a 30% sag in Figure 53 and a 50% sag in Figure 54 with constant and scheduled PI gains. As the dc bus voltage drops below 95% of nominal, i.e. 361V, the rms rectifier input current start to increase at a more rapid rate with scheduled PI gains than with constant gains. This results in a decrease in the rate at which the dc bus voltage drops and therefore in an increase in the minimum dc bus voltage. In the case of a 50% sag, the drive trips with constant PI gains whereas the dc bus voltage does not drop below 90% of nominal with scheduled PI gains.

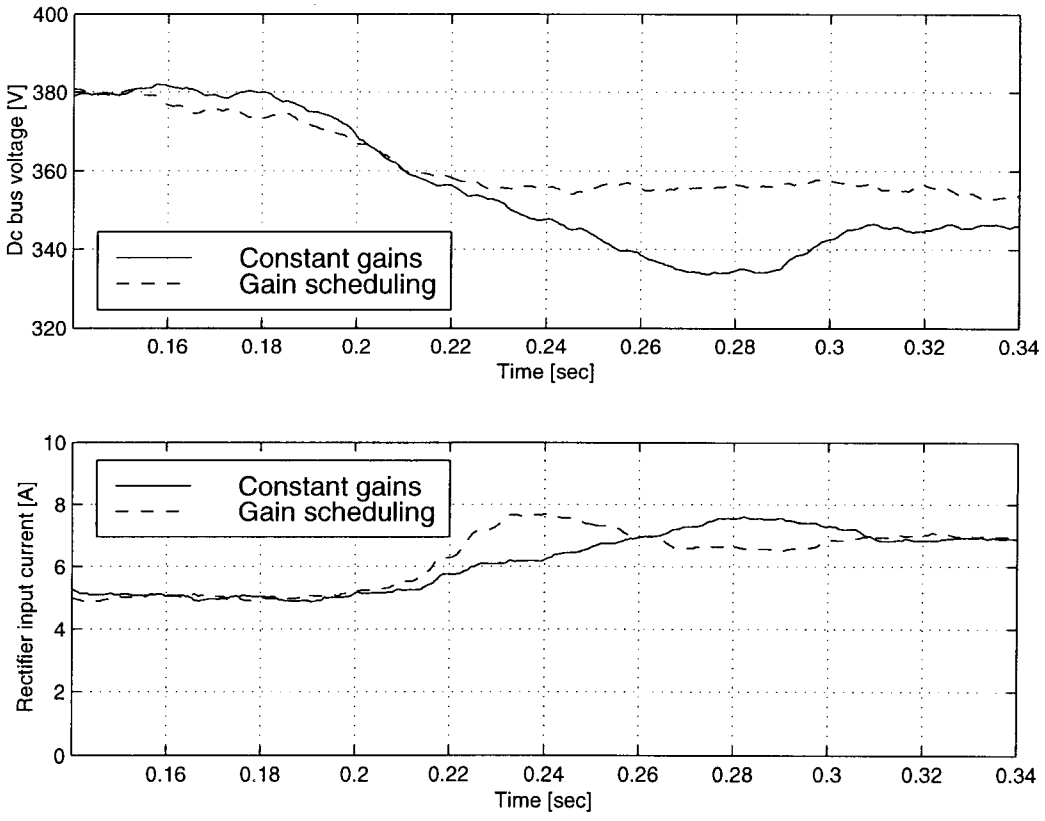


Figure 53 Step responses of dc bus voltage and rms rectifier input current to 30% sag with constant and gain scheduled PI gains

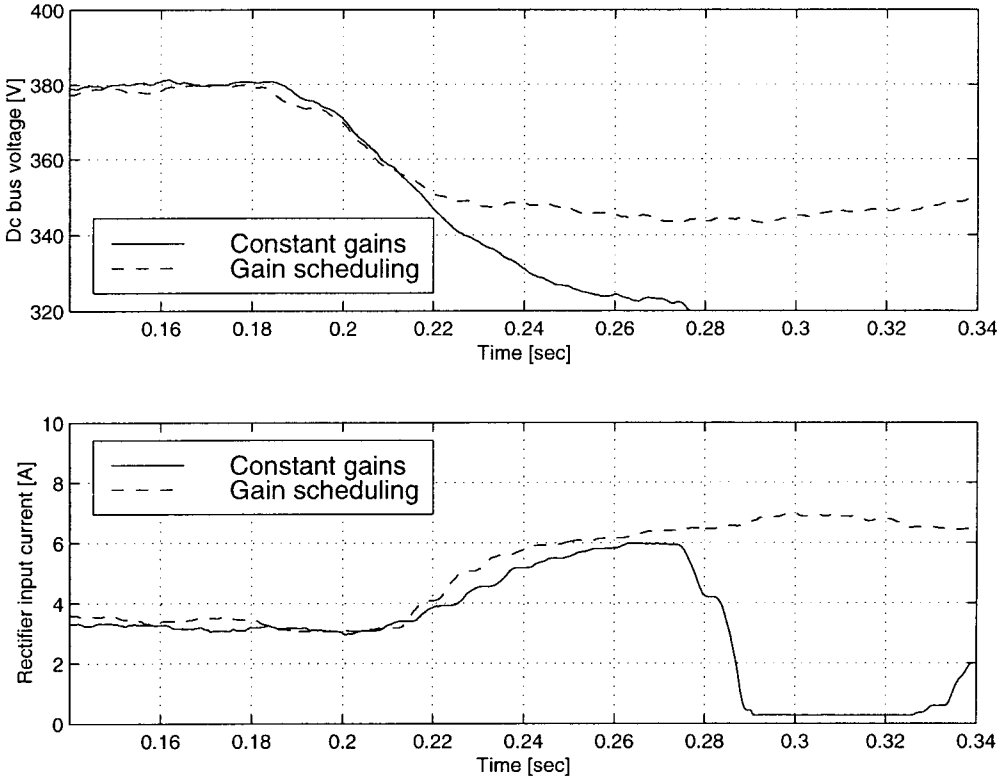


Figure 54 Step responses of dc bus voltage and rms rectifier input current to 50% sag with constant and gain scheduled PI gains

The response of the ASD with an active rectifier front end to the removal of a 40% sag condition is shown in Figure 55. Once the sag is removed, the dc bus voltage increases rapidly due to the power imbalance between rectifier and inverter. In the case of constant PI gains, the brake resistor on the dc bus is used to limit the voltage, resulting in a chopped waveform. In this particular case regulation of the dc bus voltage could not be achieved and the drive was tripped due to sustained overvoltage.

With gain scheduling, the brake does not have to be used to limit the bus voltage since the voltage does not exceed 105% of nominal. This is a result of the more rapid rate at which the rectifier input current is decreased when the dc bus voltage exceeds the nominal dc bus voltage by more than 5%.

4.8. Conclusions

A methodology has been presented for the design of Adjustable Speed Drives (ASDs) with active rectifiers and voltage sag ride-through capability for a range of voltage sags, supported by simulation and experimental results from a 3kVA laboratory prototype drive.

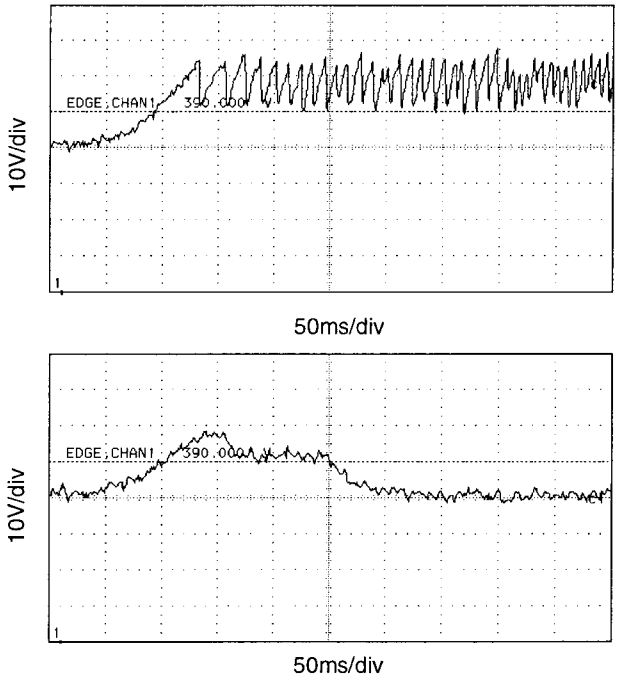


Figure 55 Experimental sag recovery from 50% sag for (top) constant PI and (bottom) gain scheduling

The design is based on the principle of using the full current capacity of the rectifier in order to prevent the drive from tripping as a result of voltage sags. The magnitude of the sag which can be compensated for is determined by the current rating of the rectifier and the load condition of the ASD, while a sag of any duration can be compensated. More ride-through can be provided to the ASD at lighter load conditions.

An active rectifier has the added advantages of reducing harmonic pollution of the power system and providing regenerative capabilities. Fast response by the dc bus voltage regulator is best achieved by employing non-linear control techniques and a non-linear controller was designed using the state variable description developed for the average behavior of the ASD.

The state variable description is idealized since it assumes that the actual rectifier currents are equal to their references and it only models the rms values of the voltages and currents and not their instantaneous values. It has however been shown that it can provide useful information about the average behavior of the system and that it can be used successfully to investigate the performance of the system under different control strategies.

For retrofit applications, the active rectifier can be added in parallel to the existing rectifier. The rectifier can also be derated if it is required to ride through deeper sags and, as discussed in Chapter 2, an energy storage system can be interfaced to the ASD in order to provide ride-through of momentary interruptions. For critical processes where it is required to operate the ASD through outages, the energy storage system can be used to operate the system until a motor-generator set can be started.

5. INTERRUPTION RIDE-THROUGH FOR ASD WITH ACTIVE RECTIFIER

5.1. INTRODUCTION

A methodology for providing Adjustable Speed Drives (ASDs) with active rectifiers with the capability to ride through voltage sags was presented in Chapter 4. The depth of sags for which ride-through can be provided is limited by the current rating of the rectifier, although ride-through can be provided for a sag of any duration. In order to provide ride-through of deep voltage sags and momentary interruptions, it is necessary to interface the ASD with an energy storage system and an overview of energy storage technologies which can be used for this application was presented in Chapter 2. In this chapter the control philosophy for an ultra-capacitor energy storage system which can be interfaced to an ASD with an active rectifier, in order to provide momentary interruption ride-through, is presented. The need for an ultra-capacitor system designed specifically to operate with an active rectifier is demonstrated by simulation and experimental results. A commercially available ultra-capacitor system [43] designed as a retro-fit to ASDs with passive rectifiers is shown in Figure 56. The ultra-capacitor system includes a boost converter which interfaces the ultra-capacitors to the dc bus of the ASD, as well as a charging circuit which can be interfaced to either the grid or the dc bus of the ASD. The specification on the ultra-capacitor system is to regulate the dc bus voltage to 90% of the nominal dc bus voltage, i.e. 585V for an ASD with a passive rectifier with a 480V nominal input.

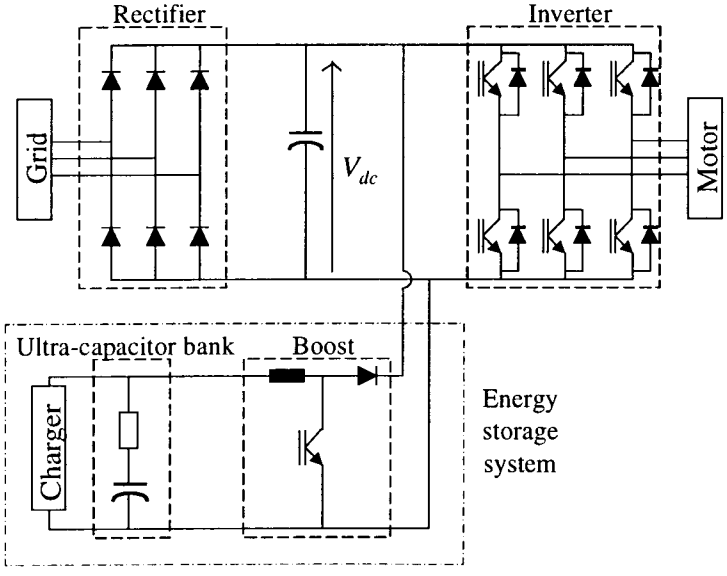


Figure 56 Retro-fit ultra-capacitor energy storage system connected to ASD with passive rectifier

There is no communication between the ASD and the ultra-capacitor system and the only interface between them is the connection of the output of the boost converter to the dc bus of the ASD. Results of this system operating with an ASD with a passive rectifier are presented in Chapter 3. The feasibility of connecting this ultra-capacitor system to an ASD with an active rectifier, as shown in Figure 57, to provide momentary interruption ride-through was investigated through simulation and experimentally.

It was found that this is only feasible if the ultra-capacitor system controller is designed specifically to operate with an ASD with an active rectifier, but no hardware changes are required in order to operate with an ASD with an active rectifier. The combination of an active rectifier and a boost converter connected to the dc bus leads to the problem of two converters trying to regulate the dc bus voltage and the control philosophy of the ultra-capacitor system needs to take this into account. When two regulators are connected to the same dc bus and equal current sharing is required, droop control can be employed. In the case under consideration however, it is desired that the rectifier should carry maximum current and that the ultra-capacitors system should carry the minimum required current and droop control is therefore not an option.

A simple control methodology for an ultra-capacitor system which will operate successfully with an ASD with an active rectifier and which requires minimal changes from the original controller, is presented, supported by simulation and experimental results. The performance of this ultra-capacitor system controller can, however, be enhanced by the addition of advanced control features and by providing communication with the ASD. The development of the enhanced ultra-capacitor system controller and supporting simulation results are presented.

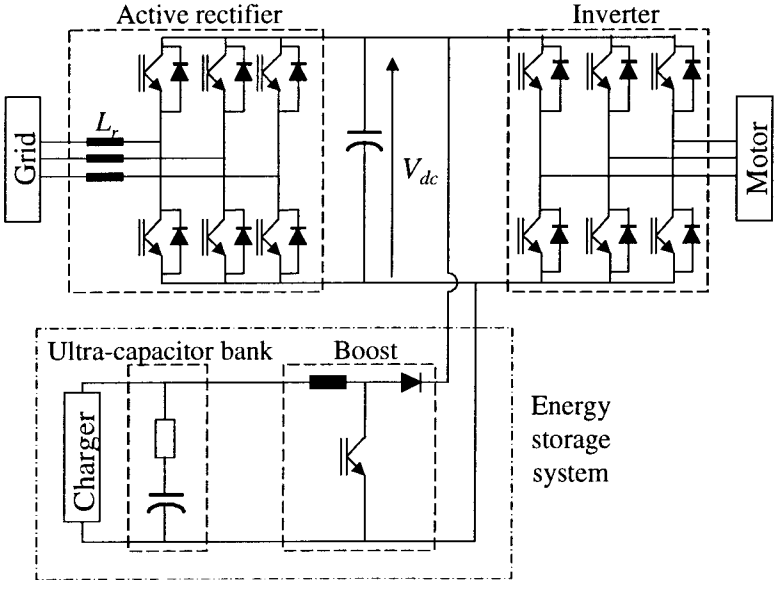


Figure 57 Retro-fit ultra-capacitor energy storage system connected to an ASD with an active rectifier

5.2. State Variable Description of an Ultra-capacitor System Connected to an ASD

In order to simulate the operation of the ultra-capacitor system with an ASD with an active rectifier, the state variable description as developed for an ASD with an active rectifier and a constant power load in Chapter 4 is expanded to include the ultra-capacitor energy storage system, as shown in Figure 58. The charger is ignored in this analysis without any loss of generality and the ultra-capacitor bank is modelled as an ideal capacitance in series with an equivalent series resistance. The ultra-capacitor system is added as a retro-fit to provide momentary interruption ride-through and the only interface to the ASD is the dc bus connection. There is no communication between the controllers of the ultra-capacitor system and the ASD. The average value, or dc component, of the dc bus voltage V_{dc} is determined by the average currents flowing in the dc bus, i.e.

$$C_{dc}\frac{dV_{dc}}{dt} = I_{Cdc} = I_{rec,dc} - I_{inv,dc} + I_{es,dc} \tag{5.1}$$

with $I_{es,dc}$ the current contribution from the ultra-capacitor system. It was shown in Chapter 4 that

$$I_{inv,dc} = \frac{P_{inv,out}}{\eta_{inv}V_{dc}} \tag{5.2}$$

and

$$I_{rec,dc} = \frac{\sqrt{3}V_{ll}I_{rec}\eta_{rec}}{V_{dc}} \tag{5.3}$$

where it is assumed that the rectifier is operated at unity input power factor. For the boost converter the following average power balance exists:

$$I_{es}V_{es}\eta_{bst} = I_{es,dc}V_{dc} \tag{5.4}$$

with V_{es} the ultra-capacitor bank voltage, I_{es} the ultra-capacitor bank current and η_{bst} the efficiency of the boost converter.

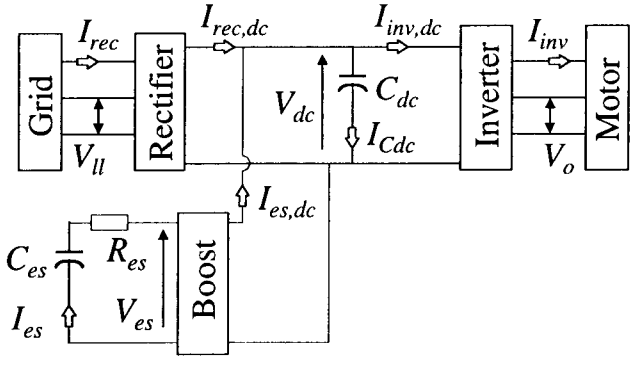


Figure 58 Line diagram of an ultra-capacitor system connected to an ASD with an active rectifier

From this the output current of the boost converter can be determined as

$$I_{es,dc} = \frac{I_{es} V_{es} \eta_{bst}}{V_{dc}} \tag{5.5}$$

By substituting (5.2), (5.3) and (5.5) in (5.1), the following non-linear differential equation describing the behavior of the average dc bus voltage is obtained

$$\frac{dV_{dc}}{dt} = \frac{\sqrt{3} V_{ll} I_{rec} \eta_{rec}}{C_{dc} V_{dc}} - \frac{P_{inv,out}}{C_{dc} V_{dc} \eta_{inv}} + \frac{V_{es} I_{es} \eta_{bst}}{C_{dc} V_{dc}} \tag{5.6}$$

The ultra-capacitor bank voltage V_{es} can be described by modelling the ultra-capacitor bank as an ideal capacitance C_{es} with a voltage V_{uc} across it, in series with an equivalent series resistance R_{es} and a current I_{es} flowing through it. From this model it follows that

$$\frac{dV_{uc}}{dt} = \frac{I_{es}}{C_{es}} \tag{5.7}$$

and

$$V_{es} = V_{uc} - R_{es} I_{es} \tag{5.8}$$

By taking the derivative of (5.8) and substituting into (5.7), we have that

$$\frac{dV_{es}}{dt} = \frac{dV_{uc}}{dt} - R_{es} \frac{dI_{es}}{dt} = \frac{I_{es}}{C_{es}} - R_{es} \frac{dI_{es}}{dt} \tag{5.9}$$

The two quantities which are controlled in this system are I_{rec}, the rectifier input current and I_{es}, the ultra-capacitor bank current, i.e. the boost converter input current. The reference values of these two quantities are determined by PI controllers and it is assumed that the boost converter PI controller aims to regulate the dc bus voltage to a reference voltage $V_{dc,bst}^{*}$ which is different from the reference voltage $V_{dc,rec}^{*}$ which the rectifier aims to regulate the dc bus voltage to. The structure of the controllers is shown in Figure 59.

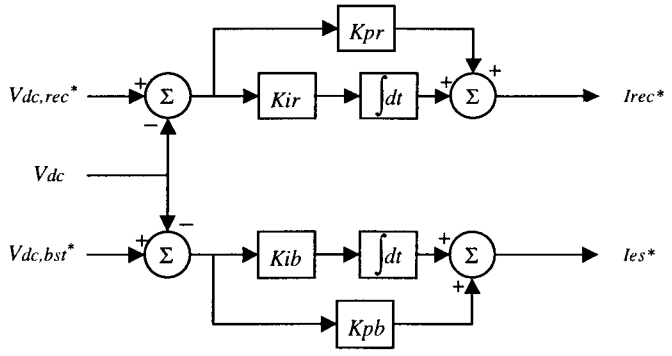


Figure 59 Structure of PI controllers for active rectifier and ultra-capacitor energy storage system

The independent inputs to this system are the rectifier input voltage V_{ll} and the load power $P_{inv,out}$. By defining quantities as listed in Table 11, we can write the state variable description of the ASD with an active rectifier and an ultra-capacitor energy storage system in standard control systems notation, as shown in (5.10).

$$
\begin{aligned}
px_1 &= \frac{1}{x_1}\left(u_1 x_2 - u_2 + c_1 x_3 x_4\right) \\
px_2 &= K_{ir}\left(V^*_{dc,rec} - x_1\right) - \frac{K_{pr}}{x_1}\left(u_1 x_2 - u_2 + c_1 x_3 x_4\right) \\
px_3 &= K_{ib}\left(V^*_{dc,bst} - x_1\right) - \frac{K_{pb}}{x_1}\left(u_1 x_2 - u_2 + c_1 x_3 x_4\right) \\
px_4 &= c_2 x_3 - c_3 K_{ib}\left(V^*_{dc,bst} - x_1\right) + c_3 \frac{K_{pb}}{x_1}\left(u_1 x_2 - u_2 + c_1 x_3 x_4\right)
\end{aligned}
\tag{5.10}
$$

Non-linearities in this state variable description arise from the multiplication of and division by state variables. Adaptive control of the rectifier PI gains as introduced in Chapter 4 is also included in this model.

$$
\begin{aligned}
&\textit{if} \quad |\varepsilon| > \varepsilon_{crit}, \quad \begin{cases} K_{pr} = K_{pr0} + \alpha_p \times \left\| |\varepsilon| - \varepsilon_{crit} \right\| \\ K_{ir} = K_{ir0} + \alpha_i \times \left\| |\varepsilon| - \varepsilon_{crit} \right\| \end{cases} \\
&\textit{else} \qquad \begin{cases} K_{pr} = K_{pr0} \\ K_{ir} = K_{ir0} \end{cases}
\end{aligned}
\tag{5.11}
$$

Table 11 Definition of symbols used in control system notation

Symbol	Definition	Type	Description
p	d/dt	operator	derivative
x_1	V_{dc}	state variable	dc bus voltage
x_2	I_{rec}	state variable	rectifier input current
x_3	I_{es}	state variable	boost converter input current
x_4	V_{es}	state variable	ultra-capacitor bank voltage, i.e. boost converter input voltage
u_1	$\sqrt{3}V_{ll}\,\eta_{rec}/C_{dc}$	input	rectifier input voltage $\times\sqrt{3}\times\eta_{rec}/C_{dc}$
u_2	$P_{inv,out}/\eta_{inv}/C_{dc}$	input	inverter output power $/\eta_{inv}/C_{dc}$
c_1	η_{bst}/C_{dc}	constant	
c_2	$1/C_{es}$	constant	
c_3	R_{es}	constant	

This state variable description is a model of the average behavior of the dc bus voltage and it models the rms values of the currents and voltages and not their instantaneous values. The inaccuracy introduced by modeling only the rms values was explained in more detail in Chapter 4. It also assumes that the actual rectifier and boost converter currents are equal to their respective references. It is therefore an idealized model, but it can provide valuable information about the average behavior of the system, as shown in Chapter 4.

5.3. Performance Evaluation of Ultra-capacitor System

The performance of an ultra-capacitor system connected to the dc bus of an ASD with an active rectifier to provide momentary interruption ride-through was evaluated through simulation and through experimental work.

5.3.1. Simulation Study

The *MATLAB* program used to simulate an ASD with an active rectifier in Chapter 4 was updated to simulate the state variable description in (5.10) with adaptive control for the rectifier gains described in (5.11). The program listing is included in Appendix G.

The nominal input line voltage V_{ll0} is 480V, the inverter output power $P_{inv,out}$ is 100kW, the rectifier reference voltage $V_{dc,rec}^*$ is 800V and the boost converter reference voltage $V_{dc,bst}^*$ is 760V, i.e. 95% of nominal. The rms current rating of the rectifier is 200A, which will provide ride-through for sags of up to 33% at the nominal load of 100kW with efficiencies of 95% assumed for the inverter and rectifier. No communication between the ultra-capacitor system and the ASD controllers is assumed.

By choosing $V_{dc,bst}^*$ to be less than $V_{dc,rec}^*$, it is ensured that, while the sag persists, the maximum possible current will be drawn from the rectifier in order to regulate the dc bus voltage and therefore only the necessary current will be extracted from the ultra-capacitor system. The PI gains in the rectifier controller are $K_{pr} = 0.5$, $K_{ir} = 2.5$, and the gain scheduling factors are $\alpha_p = 0.05$ and $\alpha_i = 0.1$, the same as was used in Chapter 4. The PI gains for the boost converter controller were found by an iterative method to have good performance when set to $K_{pb} = 10$ and $K_{ib} = 50$.

The commercial ultra-capacitor system which was introduced in Chapter 3, is designed as a retro-fit to an ASD with a passive rectifier and is engaged when $V_{dc} < V_{dc,bst}^*$. This control strategy works well for an ASD with a passive rectifier where the dc bus voltage is proportional to the input voltage. When the ASD experiences a voltage sag or momentary interruption, the dc bus voltage decreases until the diodes in the rectifier are once more forward biased and the dc bus voltage does not increase again until the input voltage is restored. The dc bus voltage of an ASD with an active rectifier however exhibits a transient behavior due to the PI controller of the rectifier. For such an ASD the dc bus voltage decreases until the power drawn by the rectifier equals or exceeds the power drawn by the inverter. If the current limit of the

rectifier is exceeded before such a point is reached, the dc bus voltage will continue to drop since the rectifier is not able to regulate it. If the rectifier current limit is not exceeded, the dc bus voltage will drop to a minimum voltage and after that it will increase and approach the reference voltage $V_{dc,rec}^{*}$.

The minimum dc bus voltage may be lower than $V_{dc,bst}^{*}$ even if the rectifier is able to regulate the dc bus voltage during the sag, which would engage the ultra-capacitor system unnecessarily. This is illustrated by a simulation result of a 30% sag in Figure 60. The top trace shows the dc bus voltage response V_{dc}, the middle trace shows the rms rectifier input current $I_{rec,rms}$ and the bottom trace shows the output current of the boost converter $I_{es,dc}$.

5.3.2. Experimental Evaluation

In order to experimentally evaluate the feasibility of connecting an ultra-capacitor energy storage system developed as a retro-fit for ASDs with passive rectifiers [43] to an ASD with an active rectifier, the commercial ultra-capacitor system described in section 5.1 was connected to the 3kVA/230V bi-directional ASD used for experimental evaluation in Chapter 4.

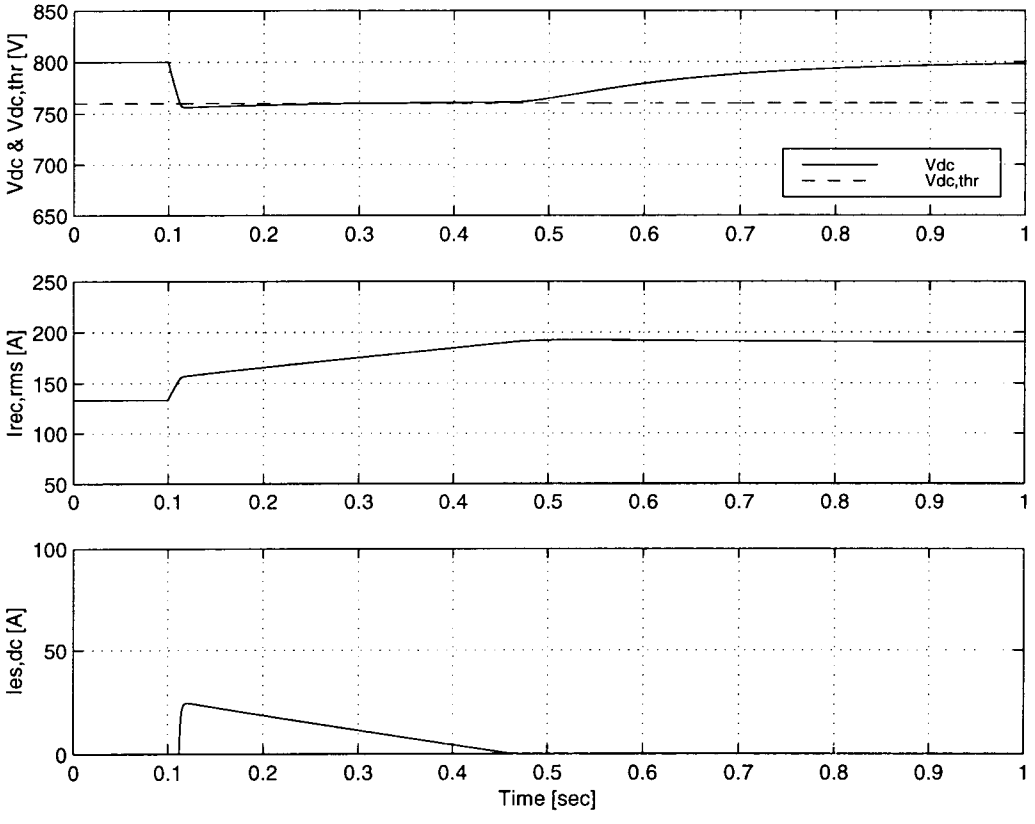


Figure 60 Simulation results for a 30% sag with $P_{inv,out}$ = 100kW and the ultra-capacitor system set to engage if $V_{dc} < V_{dc,bst}^{*}$ = 760V

The ultra-capacitor system is rated for 100kW maximum output power and is designed to be connected to an ASD with a passive rectifier and a nominal dc bus voltage of 650V. Results of the ultra-capacitor system operating with an ASD with a passive rectifier were presented in Chapter 3.

The nominal dc bus voltage of the 3kVA ASD is 380V, the maximum rectifier input current is 8A rms and gain scheduling is implemented in the rectifier PI controller as described in Chapter 4. To enable the ultra-capacitor system to operate with the 3kVA ASD, the ultra-capacitor bank was charged to only 200V and the reference dc bus voltage for the boost converter $V_{dc,bst}^{*}$ was set to 95% of 380V, i.e. 361V.

Figure 61 shows experimental results for a 27% sag at 30% load for which the active rectifier is able to provide ride-through, but the ultra-capacitor system is engaged since the dc bus voltage drops below $V_{dc,bst}^{*}$=361V and it regulates the dc bus voltage to the boost converter reference voltage of 361V for the duration of the sag. The top trace shows the dc bus voltage V_{dc}, the middle trace shows the rms value of the rectifier input current $I_{rec,rms}$ and the bottom trace shows the output current of the boost converter $I_{es,dc}$.

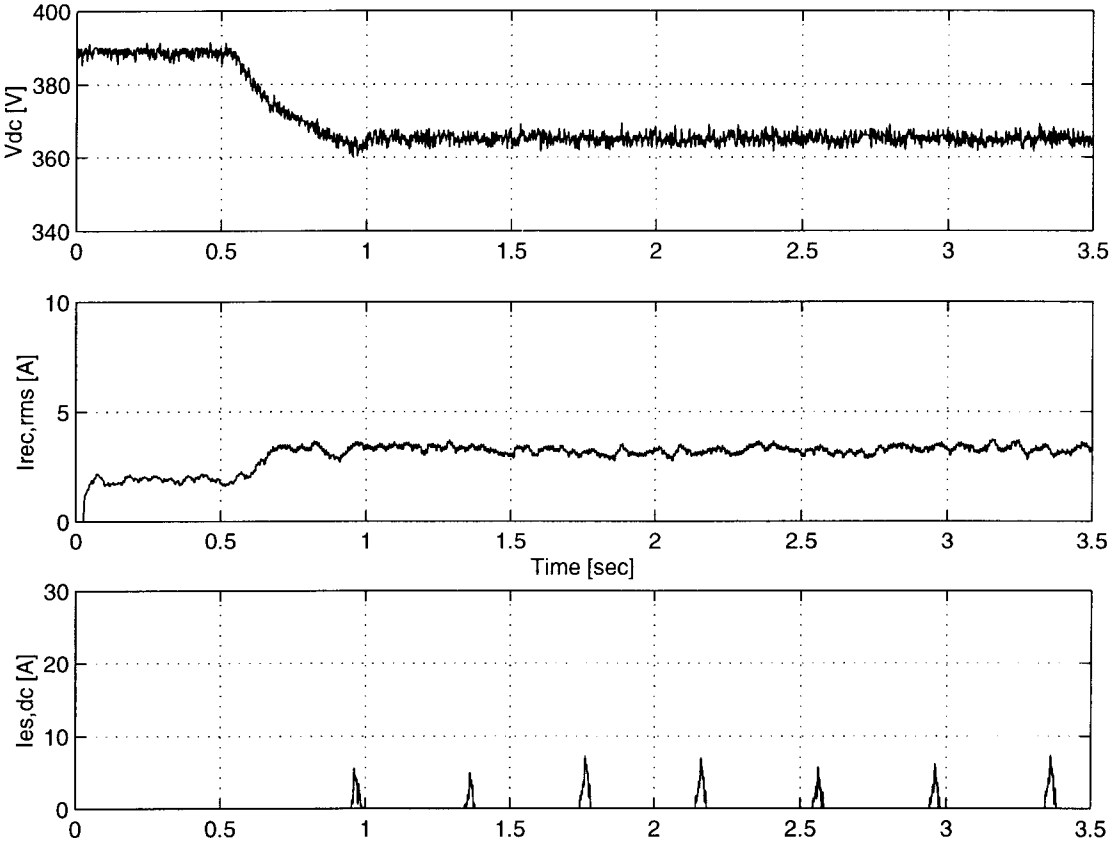


Figure 61 Experimental results of ultra-capacitor system connected to ASD with an active rectifier for a 27% sag at 30% load

The boost converter output current $I_{es,dc}$ consists of short current bursts since the boost converter controller gains were set for an ASD with 10mF of capacitance on the dc bus and the bus capacitance of the 3kVA ASD is only 1.2mF. The response of the PI controller of the boost converter is therefore much faster than with the ASD with a passive rectifier. The output capacitance of the boost converter is 5mF and therefore the total bus capacitance is five times higher than for the ASD alone and this slows down the response of the rectifier.

The experimental results proved the basic premise that an ultra-capacitor system can be used to provide ride-through to an ASD with an active rectifier. However, the ultra-capacitor system is engaged when the active rectifier could have provided ride-through. An ASD with an active rectifier has the capability to regulate the dc bus voltage to the nominal voltage during a sag condition as long as its current rating is not exceeded and it is investigated how the ultra-capacitor system controller can be enhanced to take this into account. This is done by using the *MATLAB* simulation program which models the average behavior of the ASD and it has been shown in Chapter 4 that it provides accurate enough results of the ASD response to be used for controller development.

5.3.3. Retro-fit Ultra-capacitor System for ASD with an Active Rectifier

It has been shown that ultra-capacitor system can be used with an ASD with an active rectifier to regulate the dc bus voltage. However, since the active rectifier has the capability to ride through sags as discussed in Chapter 4, the ultra-capacitor system may be engaged when the active rectifier would have been able to provide ride-through as shown by simulation in Figure 60 and experimentally in Figure 61. This problem can be circumvented by engaging the ultra-capacitor system when the dc bus voltage drops below a threshold dc bus voltage $V_{dc,thr}$ which is set lower than $V_{dc,bst}^*$. The effectiveness of this solution is illustrated in Figure 62 for a 30% sag with $P_{inv,out}$ = 100kW and $V_{dc,thr}$ = 720V. The rectifier is able to regulate the dc bus voltage during this sag and the ultra-capacitor system is not engaged.

Figure 63 shows the response of the system to a 50% sag for which the rectifier cannot provide ride-through and the ultra-capacitors system is engaged. The rectifier draws maximum rated current and the ultra-capacitor system supplies the difference in power between the inverter input and rectifier output power.

The simulations showed that minor changes should be made to the control strategy of the commercial ultra-capacitor system to allow for the transient behavior of the dc bus voltage, but that no hardware changes to the ultra-capacitor system are necessary in order to interface it to an ASD with an active rectifier. In order to ensure that the rectifier will draw maximum current during the sag and that only the minimum required power is drawn from the ultra-capacitor system, it is necessary to set the reference voltage for the boost converter $V_{dc,bst}^*$ lower than the reference voltage for the rectifier $V_{dc,rec}^*$, i.e. $V_{dc,bst}^* < V_{dc,rec}^*$.

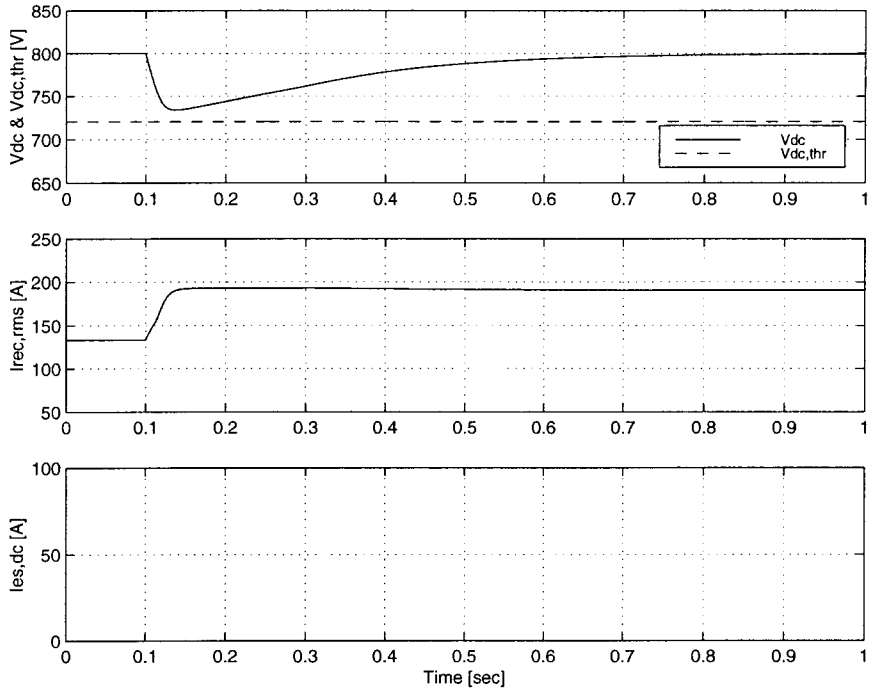


Figure 62 Simulation results for a 30% sag with $P_{inv,out}$ = 100kW and the ultra-capacitor system set to engage if $V_{dc} < V_{dc,thr}$ = 720V

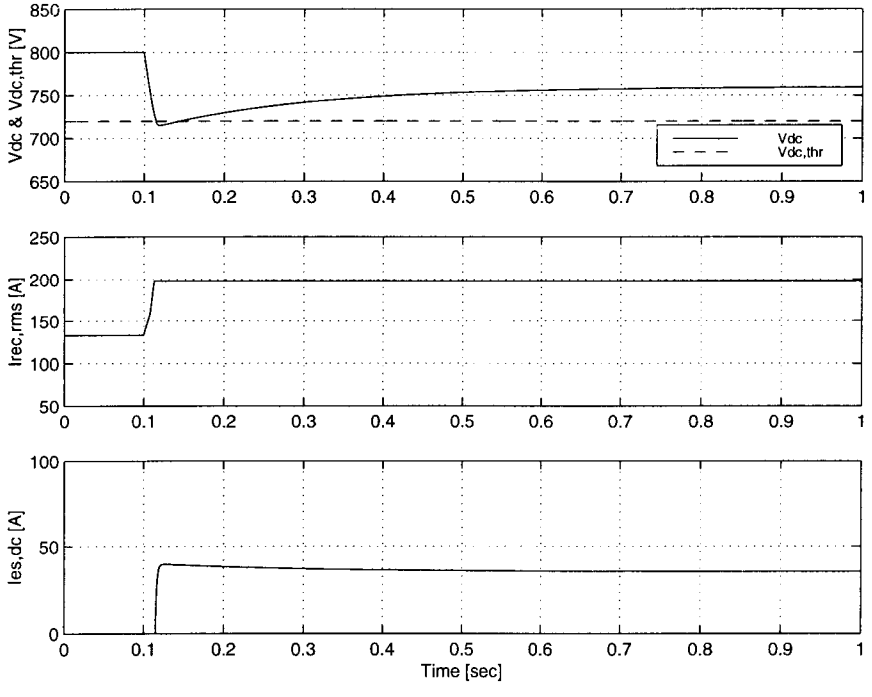


Figure 63 Simulation results for a 50% sag with $P_{inv,out}$ = 100kW and the ultra-capacitor system set to engage if $V_{dc} < V_{dc,thr}$ = 720V

Because of the PI controller in the rectifier which regulates the dc bus voltage, the minimum dc bus voltage may be less than $V_{dc,bst}^*$ even if the rectifier is able to provide ride-through. The performance of the ultra-capacitor system can be greatly improved by introducing a threshold voltage $V_{dc,thr}$ at which the ultra-capacitor system is engaged, with $V_{dc,thr} < V_{dc,bst}^*$.

It remains to choose a threshold voltage $V_{dc,thr}$ which would yield optimum performance. The threshold voltage was introduced to prevent the ultra-capacitor system from being engaged unnecessarily when the rectifier can provide ride-through. In order to prevent any unnecessary engagement of the ultra-capacitor system, the threshold voltage should be set lower than the minimum dc bus voltage which will be achieved under any combination of sag magnitude and ASD load condition for which the rectifier is able to provide ride-through. However, the threshold voltage defines the minimum dc bus voltage, since the ultra-capacitor system will be engaged once the dc bus voltage reaches the threshold voltage. The minimum dc bus voltage is actually less than the threshold voltage, since the dc bus voltage continues to decrease beyond the threshold voltage until the sum of the output power of the boost converter and rectifier equals or exceeds the inverter input power. It is therefore recommended that the threshold voltage $V_{dc,thr}$ be set equal to 87.5% of the nominal dc bus voltage, i.e. 700V, which is slightly higher than the minimum allowable dc bus voltage, which is assumed to be 85% of nominal for this thesis.

If the rectifier has a slow response, the dc bus voltage may drop to the threshold voltage even if the rectifier can provide ride-through. The ultra-capacitor system would then be engaged despite the fact that the rectifier can provide ride-through, but the ultra-capacitor system will improve the dc bus voltage regulation.

A disadvantage of choosing $V_{dc,thr}$ to be just higher than the specified minimum dc bus voltage is that the dc bus voltage will always drop to 87.5% of nominal when a sag or momentary interruption occurs for which the rectifier cannot provide ride-through. There will therefore always be at least a 12.5% drop in dc bus voltage before the ultra-capacitor system is engaged and regulates the voltage to 95% of nominal.

The drop in dc bus voltage at the onset of the sag can be limited, thereby improving the dc bus voltage regulation, if $V_{dc,thr}$ is set to a higher value if it is known that the ultra-capacitor system will be required to provide ride-through of the sag or interruption.

This can be seen by comparing the system response for a 90% sag with $V_{dc,thr}$ set to 87.5% of nominal, i.e. 700V, in Figure 64 with $V_{dc,thr}$ set to 95% of nominal, i.e. $V_{dc,thr} = V_{dc,bst}^* = 760$V, in Figure 65. With $V_{dc,thr} = 700$V, the minimum dc bus voltage is 681V, i.e. 85.1% of nominal and with $V_{dc,thr} = 760$V, the minimum dc bus voltage is 739V, i.e. 92% of nominal.

The dc bus voltage regulation can therefore be improved significantly by implementing a variable threshold voltage $V_{dc,thr}$ and the rest of this chapter will deal with how this can be achieved.

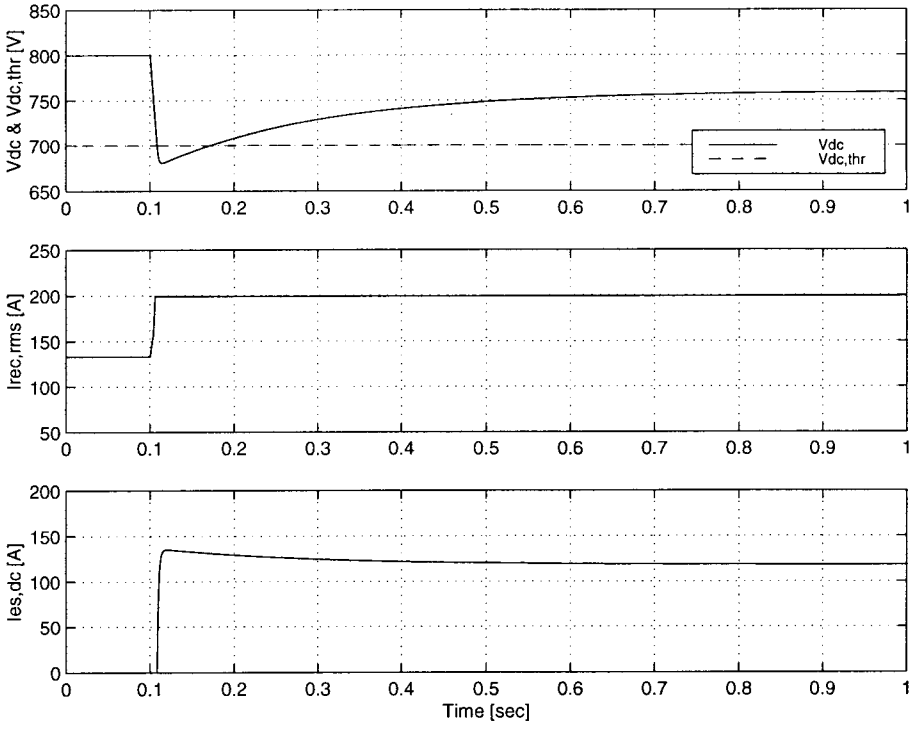


Figure 64 Simulation results for a 90% sag with $P_{inv,out}$ = 100kW $V_{dc,thr}$ = 700V

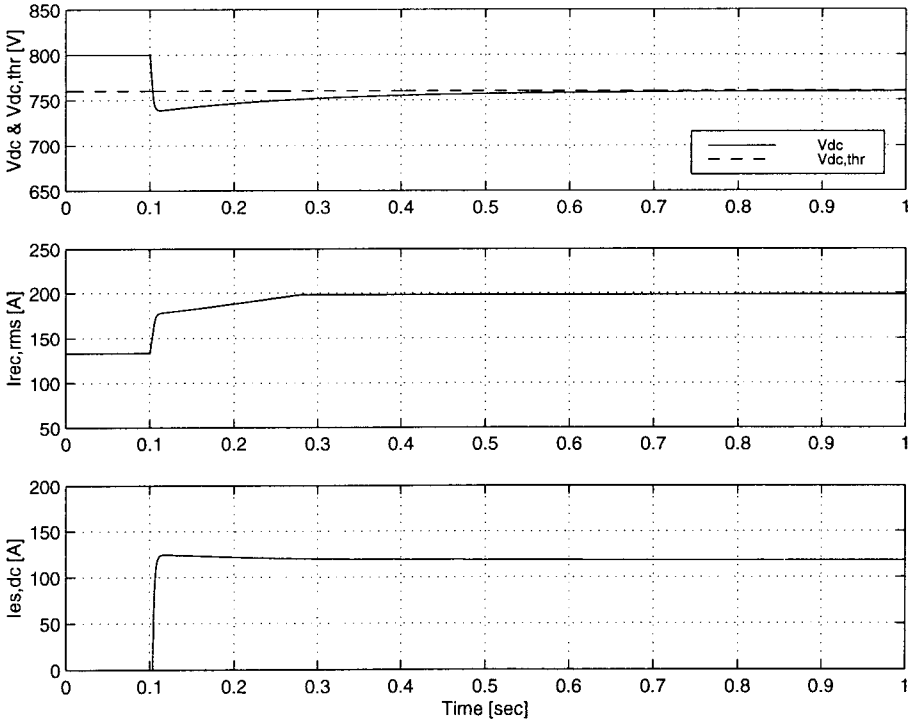


Figure 65 Simulation results for a 90% sag with $P_{inv,out}$ = 100kW and $V_{dc,thr}$ = 760V

5.4. Development of Enhanced Controller for Ultra-capacitor System

It has been shown that the implementation of a variable threshold voltage $V_{dc,thr}$ will improve system performance. If the rectifier can provide ride-through, the threshold voltage should be set to a low value in order to prevent unnecessary engagement of the ultra-capacitor system, whereas the threshold voltage should be set to a high value if the rectifier cannot provide ride-through in order to limit the drop in dc bus voltage. This will improve the dc bus voltage regulation. It remains to investigate how the ride-through capability of the rectifier for a particular sag can be determined and what additional information is required by the ultra-capacitor system controller, since only the dc bus voltage is currently measured.

Whether or not the rectifier can provide ride-through of a particular sag depends on whether the rectifier input current required to provide sag ride-through $I_{rec,sag}$ exceeds the current rating of the rectifier $I_{rec,max}$. This cannot be determined from a dc bus voltage measurement alone, since the dc bus voltage only reflects the amount of power extracted from the dc link capacitor P_{Cdc} and for a given P_{Cdc}, $I_{rec,sag}$ varies as a function of the sag magnitude. In order to achieve superior system performance by implementing a variable threshold voltage, it is therefore necessary to supply the ultra-capacitor system controller with measurements of additional system variables. This will increase the system complexity because of the additional sensors and analog to digital converters required and because more computational power is required from the system controller. The enhanced performance of the ultra-capacitor system will however allow the full ride-through capability of the active rectifier to be used. There is still no communication with the rectifier controller and therefore the ultra-capacitor system can be connected to an existing ASD with an active rectifier as a retro-fit to provide momentary interruption ride-through.

5.4.1. Implementation of Variable Threshold Voltage

The required current during the sag $I_{rec,sag}$ can be calculated from the active power balance in (4.6)

$$I_{rec,sag} = \frac{\sqrt{3}V_{ll0}}{V_{a,sag} + V_{b,sag} + V_{c,sag}} I_{rec0}, \tag{5.12}$$

with V_{ll0} and I_{rec0} the rectifier input line voltage and current respectively before the onset of the sag and $V_{a,sag}$, $V_{b,sag}$ and $V_{c,sag}$ the rectifier input phase voltages during the sag. It is assumed that the rectifier input currents are balanced in magnitude and in phase with the input phase voltages and that balanced conditions exist before the onset of the sag. The required current $I_{rec,sag}$ therefore depends on the sag magnitude and the rectifier input current before the sag, which reflects the load condition of the ASD. Both the input voltages and currents to the rectifier therefore have to be measured in order to calculate $I_{rec,sag}$.

If $I_{rec,sag} > I_{rec,max}$, the threshold voltage $V_{dc,thr}$ should be high. However, if $I_{rec,sag} < I_{rec,max}$, $V_{dc,thr}$ should be low.

In order to verify the validity of the proposed controller with a variable threshold voltage, the following control rule was implemented in the *MATLAB* program created to simulate the ultra-capacitor system connected to an ASD with an active rectifier.

$$\begin{aligned} &if \quad I_{rec,sag} > I_{rec,\max} \quad then \quad V_{dc,thr} = 0.95 \times V^{*}_{dc,rec} = 760V \\ &if \quad I_{rec,sag} < I_{rec,\max} \quad then \quad V_{dc,thr} = 0.875 \times V^{*}_{dc,rec} = 700V \end{aligned} \tag{5.13}$$

The program listing is in Appendix H. The system response for a 30% sag with $P_{inv,out}$ = 100kW is shown in Figure 66. The top trace shows the dc bus voltage V_{dc}, as well as the value determined for $V_{dc,thr}$. When the dc bus voltage drops below $V_{dc,thr}$, the controller engages the ultra-capacitor energy storage system. The middle trace shows the rms value of the rectifier input current $I_{rec,rms}$ and the bottom trace shows the output current of the boost converter $I_{es,dc}$. The rectifier current required to provide ride-through $I_{rec,sag}$ is calculated to be less than $I_{rec,max}$ using (5.12) and $V_{dc,thr}$ is therefore set equal to 87.5% of nominal, i.e. 700V. The minimum dc bus voltage is 734V, i.e. 92% of nominal.

Simulation results showed that the controller has good performance over a wide range of voltage sags and load conditions. However, when $I_{rec,sag}$ is only marginally greater than $I_{rec,max}$, the controller still sets $V_{dc,thr}$ to a high value and the boost converter engages before the rectifier reaches its maximum current and more energy is extracted from the ultra-capacitors than needed. This is illustrated in Figure 67 for a 40% sag with a 100kW load for which the peak boost converter output current is 40A, compared to the required steady state value of 13A.

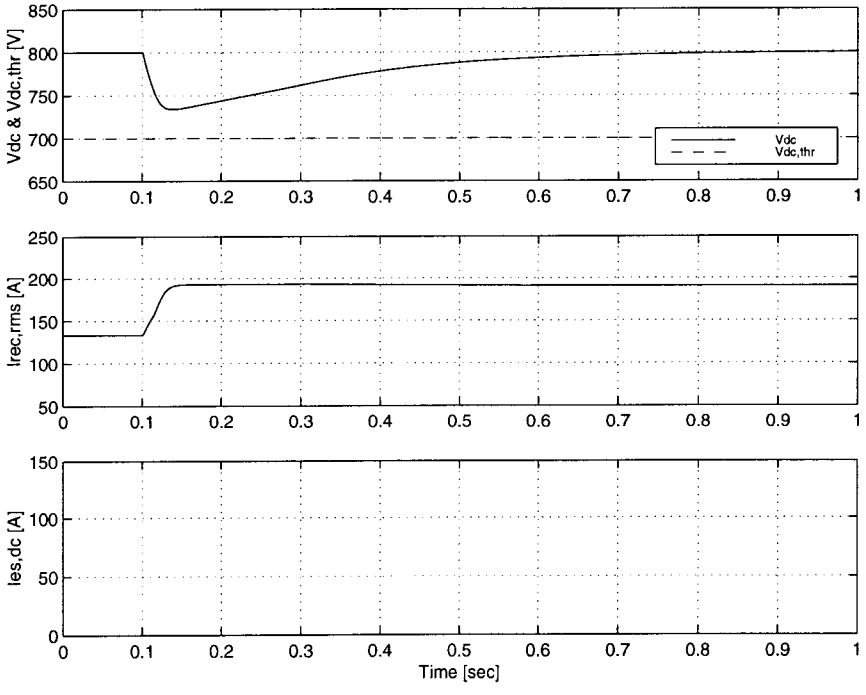


Figure 66 Simulation results for a 30% sag with $P_{inv,out}$ = 100kW and a variable threshold voltage

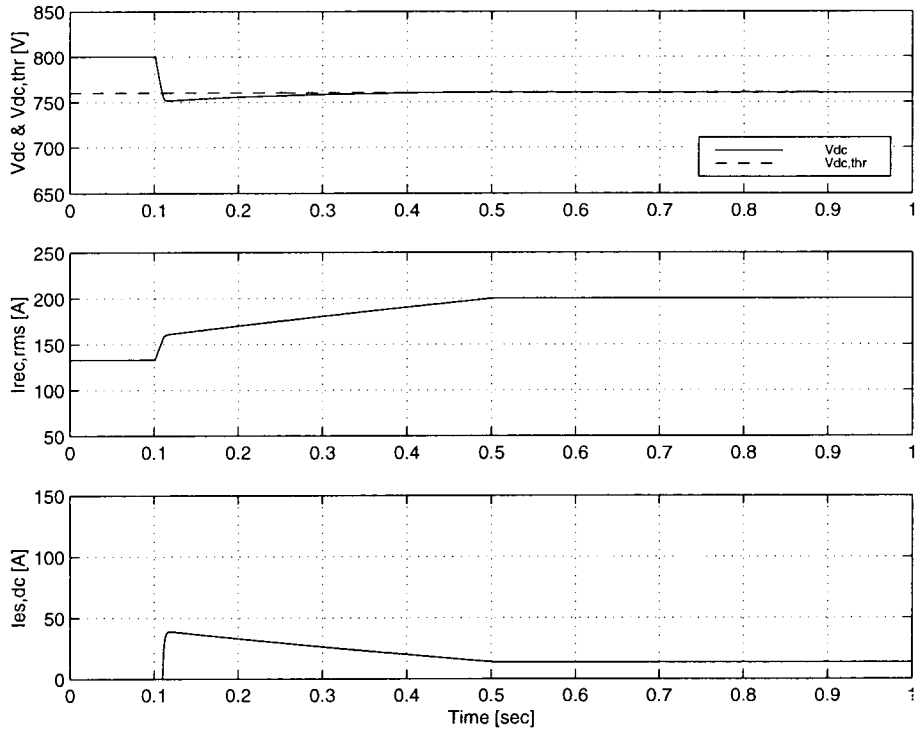


Figure 67 Simulation results *(MATLAB)* for a 40% sag with a variable threshold voltage

It would therefore be desirable to have a gradient for $V_{dc,thr}$ to change along during the transition from a low to a high value of $I_{rec,sag}$. The control philosophy lends itself well to fuzzy logic because of its 'if ... then' structure as can be seen in (5.13) and it was decided to implement a fuzzy logic controller [80][81] to determine the appropriate threshold voltage $V_{dc,thr}$.

5.4.2. Fuzzy Logic Control

The concept of fuzzy or multi-valued logic was developed in the 1920's independently by Bertrand Russell and Jan Zukasiewicz [80]. In a 1937 article in *Philosophy of Science*, Max Blanck applied multi-valued logic to lists or sets. Almost thirty years later, Lofti Zadeh published "Fuzzy Sets", a landmark paper that gave the field its name. He worked out a complete algebra for fuzzy sets [82], but, even so, fuzzy sets were not put to use until the mid-1970's when Ebrahim Mamdani designed a fuzzy controller for a steam engine [80].

Fuzzy control systems are currently used in many Asian products, e.g. to automate subways, control the focus of cameras and camcorders, tune televisions, control air conditioners, adjust the wash cycle of washing machines, etc. The most famous application of a Fuzzy Logic Controller (FLC) is the subway car controller used in Sendai, which has outperformed both human operators and conventional automated

controllers. It has been found that systems with fuzzy controllers are often more energy efficient than conventional controllers [80].

5.4.2.1. Principle of Operation

Fuzzy logic is based on rules of the form "if...then..." which convert inputs to outputs [80]. The inputs are defined with words or phrases, such as "low", "high" or "moderately high", and not values. When provided with a set of inputs, the outputs are determined by the fuzzy rules. In order to produce a control system based on fuzzy logic, the fuzzy membership functions and fuzzy rules must be defined. A fuzzy membership function assigns real values between 0 and 1 to every possible input and output value, thereby indicating the degree to which a specific value belongs to the fuzzy set, as illustrated in Figure 68. Consider two hypothetical inference rules which has the error of a controlled variable *e* and the rate of change in the error *de/dt* as inputs and a control variable *c* as output. The two fuzzy rules are:

If *e* is positive medium (PM) and *de/dt* is positive big (PB) then *c* is positive medium (PM)

If *e* is positive big (PB) and *de/dt* is positive big (PB) then *c* is positive small (PS)

Where two or more inputs are combined in one rule to determine the degree of membership of the output, as in this example, the product of the degrees of membership of the inputs, or their minimum, can be used to clip the output membership function at the degree of membership. In this example the minimum of the two inputs is used. The fuzzy system's output fuzzy set has to be defuzzified and a method called centroid defuzzification can be used in which the defuzzified output value is equal to the center of gravity of the shaded area. Almost all fuzzy systems rely on a preliminary set of rules supplied by an expert or drawn up from the input-output data of an existing controller [82]. A lengthy process of tuning these rules then follows. To automate this process, adaptive fuzzy systems that use neural networks [80], genetic algorithms [83] or another fuzzy system [84] to refine or even form the rules have been developed. Adaptive fuzzy systems are used to refine the fuzzy rules in order to optimize performance, and to change the rules as the system's structure changes over time.

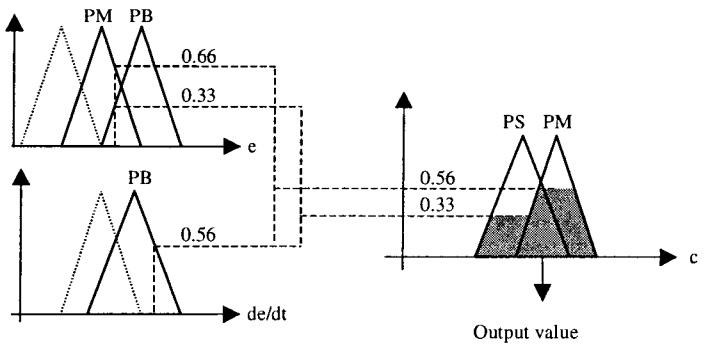


Figure 68 Example of fuzzy controller

5.4.2.2. Fuzzy Logic Applied to Power Electronics

The possibility of applying fuzzy algorithms to control systems in power electronics, which require faster and more accurate response compared to other industrial processes for which fuzzy control is normally used, has been investigated. Switching power converters need accurate control at very high frequencies (2-40kHz). Fuzzy controllers have been proposed for one-phase buck/boost DC/DC converters [79], a one phase full-bridge VSI PWM inverter with non-linear loads [90], three phase converters and inverters, a phase controlled converter DC machine drive [91] and an inverter fed induction machines in conjunction with direct self control [92]. It has been reported that fuzzy controllers outperformed conventional PI controllers.

Fuzzy products use both microprocessors that run fuzzy inference algorithms and sensors that measure changing input conditions. Fuzzy chips are microprocessors designed to store and process fuzzy rules. Fuzzy chips capable of processing two million Fuzzy Logic Inferences Per Second (FLIPS) are available. A hardware implementation of fuzzy controllers on Field Programmable Gate Arrays (FPGAs) has been investigated [93]. Alternatively the algorithms are pre-calculated and stored in a look-up table.

5.4.3. Fuzzy Logic Control for Ultra-capacitor System

A fuzzy logic controller was designed to determine the threshold voltage $V_{dc,thr}$ for the ultra-capacitor system. The inputs to the ultra-capacitor system controller are the dc bus voltage and the rectifier input phase voltages and currents. The fuzzy logic controller has two inputs R and S with

$$R = \frac{I_{rec,sag}}{I_{rec,\max}} \tag{5.14}$$

$$S = \frac{I_{rec0}}{I_{rec,\max}} \tag{5.15}$$

and the output is the threshold voltage $V_{dc,thr}$. The rules for the fuzzy controller are the following

1. if R is small and S is small, then $V_{dc,thr}$ is low
2. if R is large and S is large, then $V_{dc,thr}$ is high

The product inference method is used to determine the degree of membership of the output, i.e. the degrees of membership of small R and small S are multiplied to obtain the degree of membership of low $V_{dc,thr}$ and the degrees of membership of large R and large S are multiplied to obtain the degree of membership of high $V_{dc,thr}$. Several membership functions were tried and the one which yielded the best results is shown in Figure 69, and the input-output relationship for these membership functions is shown in Figure 70.

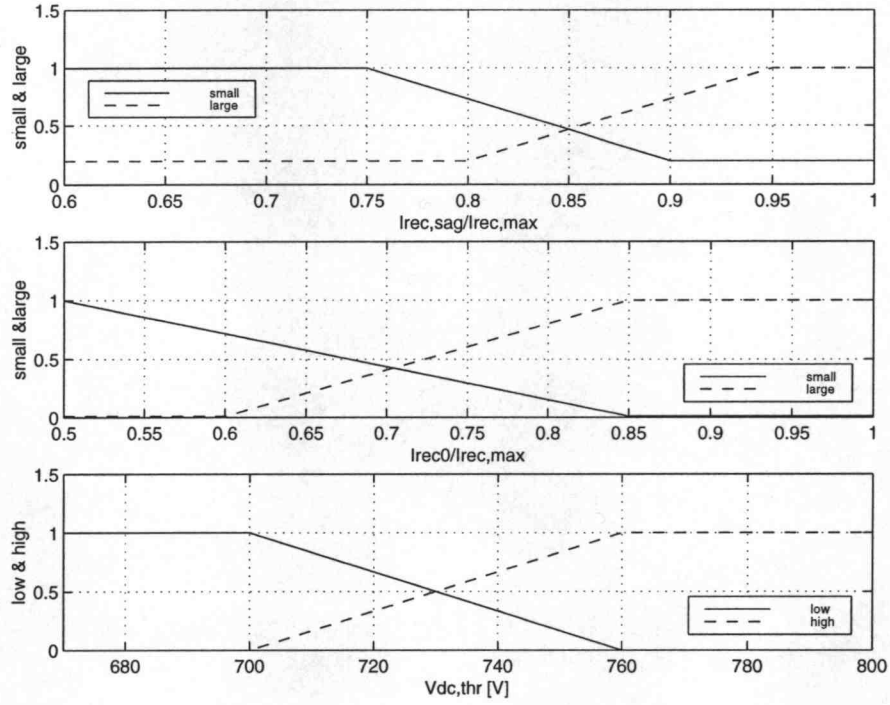


Figure 69 Membership functions for fuzzy logic controller

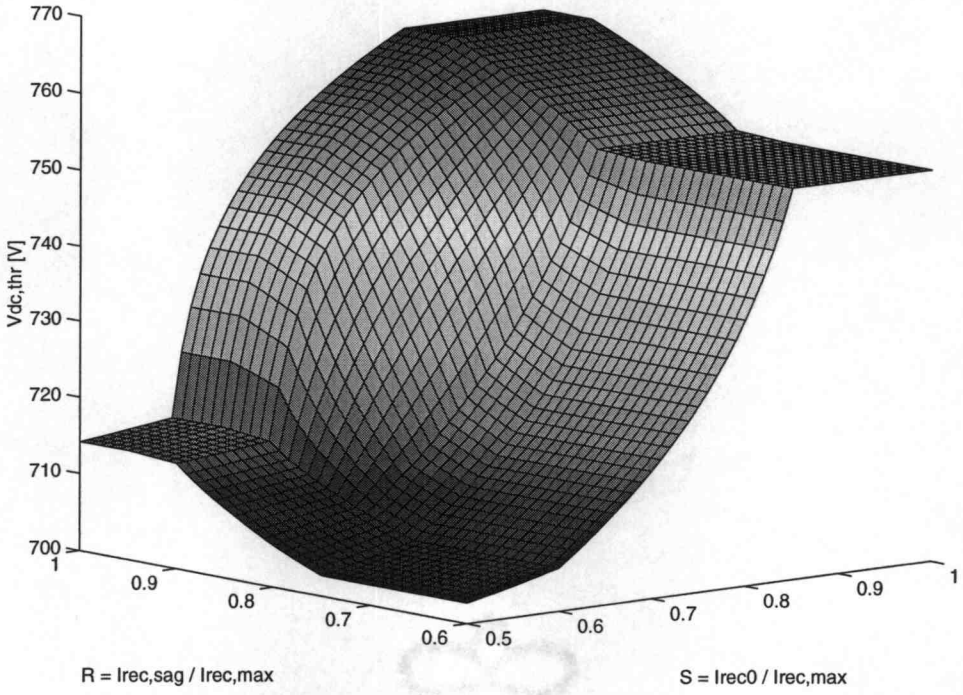


Figure 70 Input-output relationship for fuzzy logic controller

5.5. VERIFICATION OF THE ENHANCED ULTRA-CAPACITOR SYSTEM CONTROLLER

The improvement gained in system performance through the implementation of a variable threshold voltage $V_{dc,thr}$ determined by a fuzzy logic controller is verified through simulation of the system response in *MATLAB* as well as an off-line experimental evaluation.

5.5.1. Simulation

The *MATLAB* program used to simulate the ASD with an active rectifier and an ultra-capacitor system was expanded to include the fuzzy logic controller and the program listing appears in Appendix I.

The system response for a 20% sag with a 100kW load is shown in Figure 71. The top trace shows the dc bus voltage V_{dc} and the calculated threshold voltage $V_{dc,thr}$. The middle trace shows the rms rectifier input current $I_{rec,rms}$ and the bottom trace shown the output current of the boost converter $I_{es,dc}$. The rectifier is able to provide ride-through of this sag and $V_{dc,thr}$ is set to 91% of nominal, i.e. 724V. The minimum dc bus voltage is 750V, i.e. 94% of nominal. As shown in Figure 72, $V_{dc,thr}$ is set to a low value of 93% of nominal, i.e. 745V, in response to a 40% sag with a 100kW load. This allows the rectifier to reach maximum current before the ultra-capacitor system is engaged. The minimum dc bus voltage is limited to 93% of nominal.

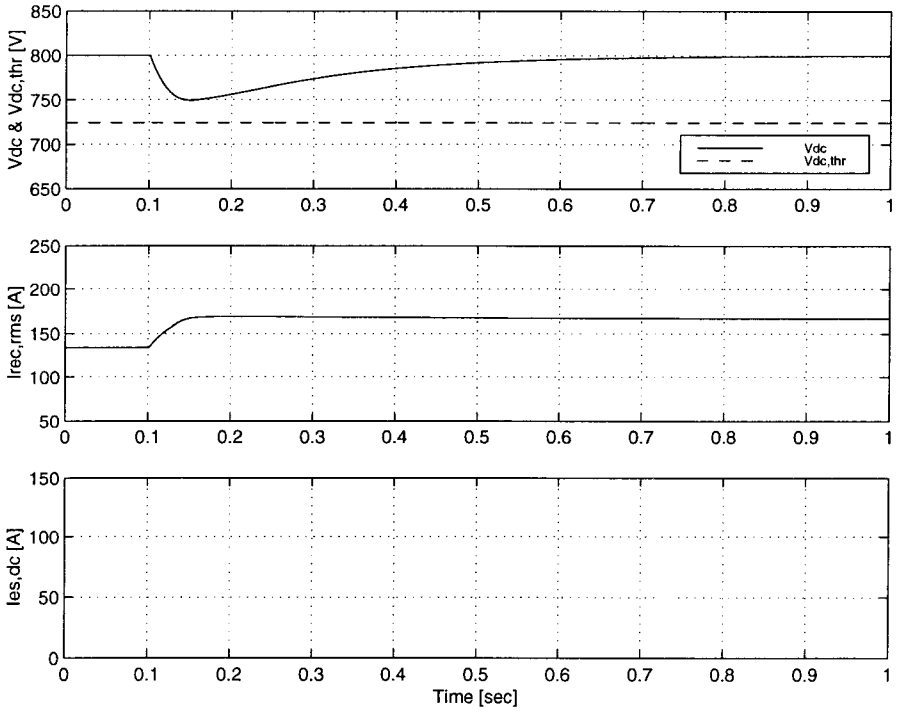


Figure 71 Simulation results for a 20% sag with a 100kW load and a fuzzy logic controller

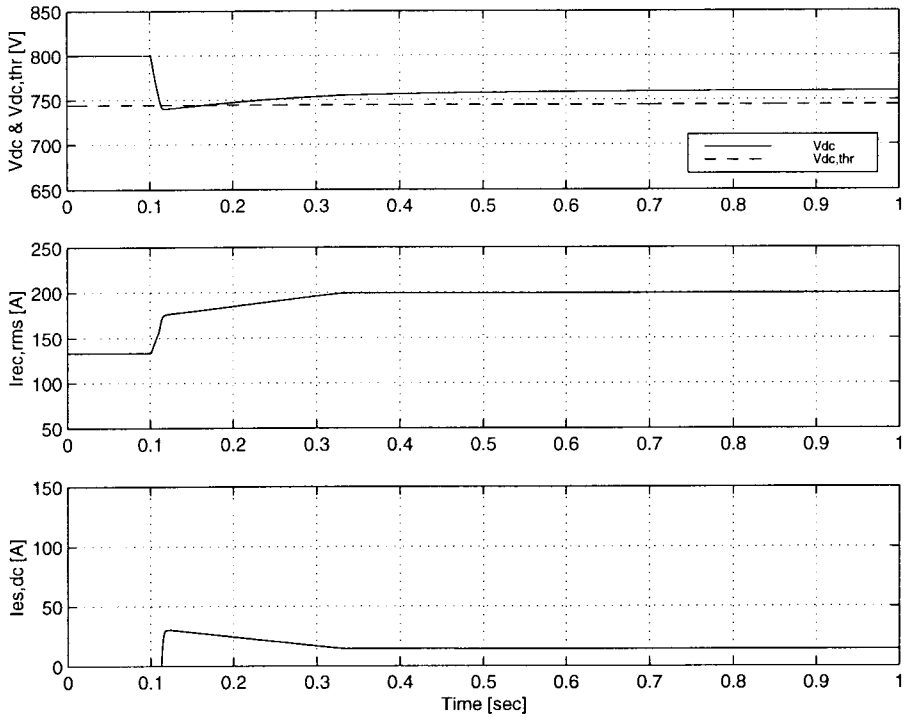


Figure 72 Simulation results for a 40% sag with a 100kW load and a fuzzy logic controller

For a nominal load of 100kW, the rectifier input current before the onset of the sag I_{rec0} is 133A and with the maximum rectifier input current set to 200A, the input R to the fuzzy logic controller is equal to 0.67. Even for a very large input S, the maximum value the threshold voltage will be set to by the fuzzy controller is 745V, i.e. 93% of nominal, as can be seen in Figure 70. In order to show the response of the system to a high input value R, the maximum rectifier current is decreased to 170A in the simulation. The response to a 50% sag with a 100kW load is shown in Figure 73 with $I_{rec,max}$ = 170A.

$V_{dc,thr}$ is determined to be 758V, i.e. 95% of nominal, since both inputs to the fuzzy controller, R and S, are large. The ultra-capacitor system is therefore engaged soon after the onset of the sag, and the minimum dc bus voltage is limited to 94% of nominal, i.e. 748V.

The *MATLAB* simulation study shows good performance of the enhanced ultra-capacitor system controller which measures the rectifier input currents and voltages and uses a fuzzy logic controller to determine an optimum threshold voltage at which to engage the ultra-capacitor system. The *MATLAB* simulation uses an idealized model of the system which simulates only rms values of the voltages and currents and does not take into account the effects of switching in the rectifier and inverter. It has, however, been shown that it provides useful results on the average behavior of the system.

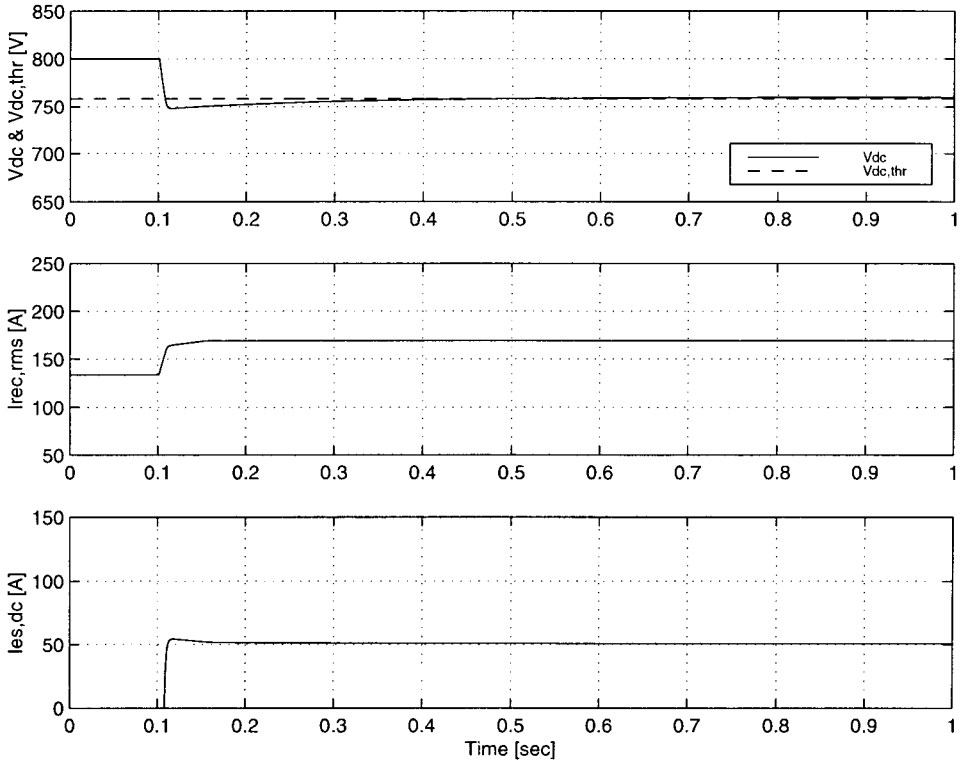


Figure 73 Simulation results for a 50% sag with a 100kW load and $I_{rec,max}$ = 170A

5.5.2. Estimation of Rectifier Input Current

The implementation of the enhanced controller requires additional sensors to measure the rectifier input voltages and currents. It is possible to eliminate the current sensors, which would reduce the cost and complexity of the system, by estimating the rectifier input current from the dc bus voltage and rectifier input voltages. The estimation is based on the active power balance on the dc bus and the power flow in the ASD circuit as shown in Figure 74. The equations for the estimates of the rectifier input current before and during the sag are determined by considering the onset of a voltage sag as illustrated in Figure 75.

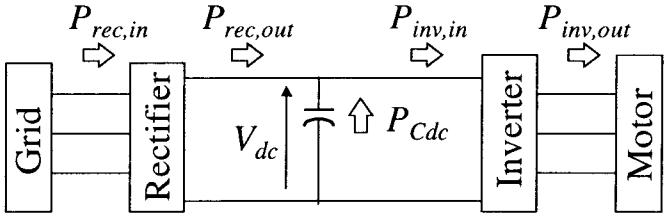


Figure 74 Diagram of ASD with an active rectifier showing power flow in circuit

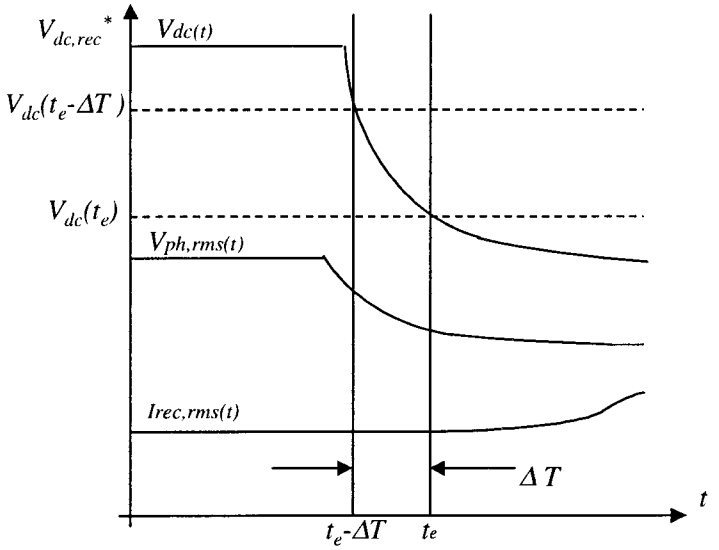


Figure 75 Dc bus voltage transient under sag condition

The time t_e is chosen to be soon after the onset of the sag and it is assumed that the rectifier input current I_{rec} stays constant over the time period $t\in[t_e-\Delta T,t_e]$, which has proven to be a reasonable assumption based on experimental data. The rms values of the currents and phase voltages are determined over a period of ΔT seconds, i.e.

$$X_{rms}(t)=\sqrt{\frac{1}{\Delta T}\int_{t-\Delta T}^{t}x^2(t)dt} \tag{5.16}$$

From the active power balance at the dc link capacitor during $t\in[t_e-\Delta T,t_e]$, we have

$$P_{inv,in}=P_{rec,out}+P_{Cdc} \tag{5.17}$$

with $P_{inv,in}$ the inverter input power, $P_{rec,out}$ the rectifier output power and P_{Cdc} the average power delivered by the dc link capacitor during $t\in[t_e-\Delta T,t_e]$. This balance can be rewritten as

$$\frac{P_{inv,out}}{\eta_{inv}}=\eta_{rec}P_{rec,in}+P_{Cdc} \tag{5.18}$$

with $P_{inv,out}$ the inverter output power, i.e. load power, which is assumed to be constant and $P_{rec,in}$ the average input power to the rectifier during $t\in[t_e-\Delta T,t_e]$. It is possible to estimate the average active power delivered by the dc link capacitor P_{Cdc} by considering the dc bus voltage transient shown in Figure 75.

The average power extracted from the dc link capacitor is calculated as

$$P_{Cdc}=\frac{1}{\Delta T}\frac{C_{dc}}{2}\left(V_{dc}^2(t_e-\Delta T)-V_{dc}^2(t_e)\right) \tag{5.19}$$

The rms values of one phase voltage and input current are shown in Figure 75, but these can differ from phase to phase and therefore all three phase voltages are measured. The average input power to the rectifier can be estimated as

$$P_{rec,in} = I_{rec0}\left(V_{a,rms}(t_e)+V_{b,rms}(t_e)+V_{c,rms}(t_e)\right)= I_{rec0}\sum_{a,b,c} V_{ph,rms}(t_e) \tag{5.20}$$

where it is assumed that the rms value of the rectifier input current I_{rec0} stays constant during $t\in[t_e-\Delta T,t_e]$ and that the rectifier input current magnitudes are balanced. Substituting (5.19) and (5.20) in (5.18), we have that

$$\frac{P_{inv,out}}{\eta_{inv}} = \eta_{rec} I_{rec0}\sum_{a,b,c} V_{ph,rms}(t_e)+\frac{1}{\Delta T}\frac{C}{2}\left(V_{dc}^2(t_e-\Delta T)-V_{dc}^2(t_e)\right) \tag{5.21}$$

and prior to the onset of the sag, there exist a power balance such that

$$P_{inv,out} = \eta_{rec}\eta_{inv}P_{rec,in} \tag{5.22}$$

and substituting (5.20), we have that

$$P_{inv,out} = \eta_{rec}\eta_{inv} I_{rec0}\sum_{a,b,c} V_{ph,rms0} \tag{5.23}$$

with $V_{ph,rms0}$ the rms phase voltage before the onset of the sag. Substituting (5.23) in (5.21) and rearranging terms, we find an expression for the estimated current before the onset of the sag

$$I_{rec0} = \frac{1}{\Delta T}\frac{C_{dc}}{2}\frac{1}{\eta_{rec}}\frac{\left(V_{dc}^2(t_e-\Delta T)-V_{dc}^2(t_e)\right)}{\sum_{a,b,c}\left(V_{ph,rms0}-V_{ph,rms}(t_e)\right)} \tag{5.24}$$

The estimated rectifier input current required for the rectifier to ride through the sag without engaging the ultra-capacitor system is

$$I_{rec,sag}(t) = \sum_{a,b,c}\frac{V_{ph,rms0}}{V_{ph,rms}(t)}\times I_{rec0} \tag{5.25}$$

and it is assumed that the rectifier is controlled to draw currents which are balanced in magnitude. The estimate of $I_{rec,sag}(t)$ has to be updated as the input voltage continues to drop. If the estimated current during the sag is greater than the rated rectifier current $I_{rec,max}$, the ultra-capacitor system will need to be engaged to provide voltage sag ride-through. It is therefore possible to estimate shortly after the onset of the sag whether the ultra-capacitor system will be required or not and the threshold voltage $V_{dc,thr}$ can then be set accordingly.

5.5.3. Off-line Experimental Evaluation

An off-line experimental evaluation of the enhanced controller was performed using experimental data collected from the 3kVA ASD under many different sag and load conditions. This experimental data

was used as input to the fuzzy logic controller and the validity of the calculated threshold voltage was qualitatively evaluated.

The *MATLAB* program used for the simulation study in section 5.5.1 was adapted to use the data files with experimental results as inputs to the fuzzy logic controller rather than the simulated system values. The estimation of the rectifier input current was also added to the program and the program listing is included in Appendix J. The off-line experimental verification of the enhanced controller was performed using a 3kVA/230V ASD with a nominal dc bus voltage of 380V as opposed to the simulated 100kW/480V ASD with a nominal dc bus voltage of 800V, and all variables in the enhanced controller are therefore appropriately scaled. Experimental data was collected with an HP oscilloscope sampling at 10kHz in order to replicate the sampling of the A/D converters which are available in the commercial ultra-capacitor system.

The dc bus voltage and all three rectifier input phase voltages are inputs to the enhanced controller. Although only balanced three phase sags were generated experimentally, most sags on the power system are unbalanced in both magnitude and phase and therefore all three input phase voltages are used as inputs. The rms values of the rectifier input current before the sag I_{rec0} and during the sag $I_{rec,sag}$ are estimated from the dc bus voltage and rectifier input voltage measurements. Experimental data of the rectifier input current of one phase was collected in order to determine the accuracy of the estimator. Currently the rectifier input currents are controlled to be balanced in magnitude and phase by generating one reference in phase with one of the phase voltages and shifting the current reference by ±120 degrees to generate the references for the other two phases. A more effective way to control the rectifier under unbalanced sag conditions would be to generate three current references which are balanced in magnitude, but with each current reference being in phase with one of the phase voltages.

The current and proposed current control schemes are illustrated in Figure 76. In this way the active rectifier would draw the maximum active power from the grid that its current rating allows.

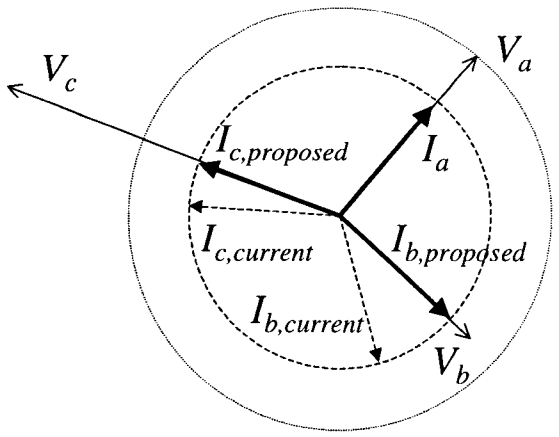


Figure 76 Proposed rectifier current control for unbalanced sags

A flow chart for the program used for the off-line experimental evaluation of the enhanced ultra-capacitor system controller is shown in Figure 77. At each sampling instant the measured current and voltages are filtered using a digital first order Butterworth low pass filter and the rms values of each of the rectifier input voltages $V_{ph,rms}$[k] and the measured rectifier input current $I_{rec,rms}$[k] are determined using (5.16). The time period over which the rms value is calculated ΔT was chosen as 150% of a fundamental period, i.e. 25.1ms. When the dc bus voltage drops below 94.5% of the nominal dc bus voltage, i.e. 359V, the rectifier input current before the onset of the sag I_{rec0} is estimated using (5.24) with $V_{dc}(t_e)$ = 359V. The estimate of the current during the sag $I_{rec,sag}$[k] is updated using (5.25) as the input voltages continue to drop until they reach their minimum levels. The fuzzy logic controller determines $V_{dc,thr}$[k] using I_{rec0} and $I_{rec,sag}$[k] as inputs and if an ultra-capacitor is connected to the ASD, it would be engaged if V_{dc}[k] drops below $V_{dc,thr}$[k].

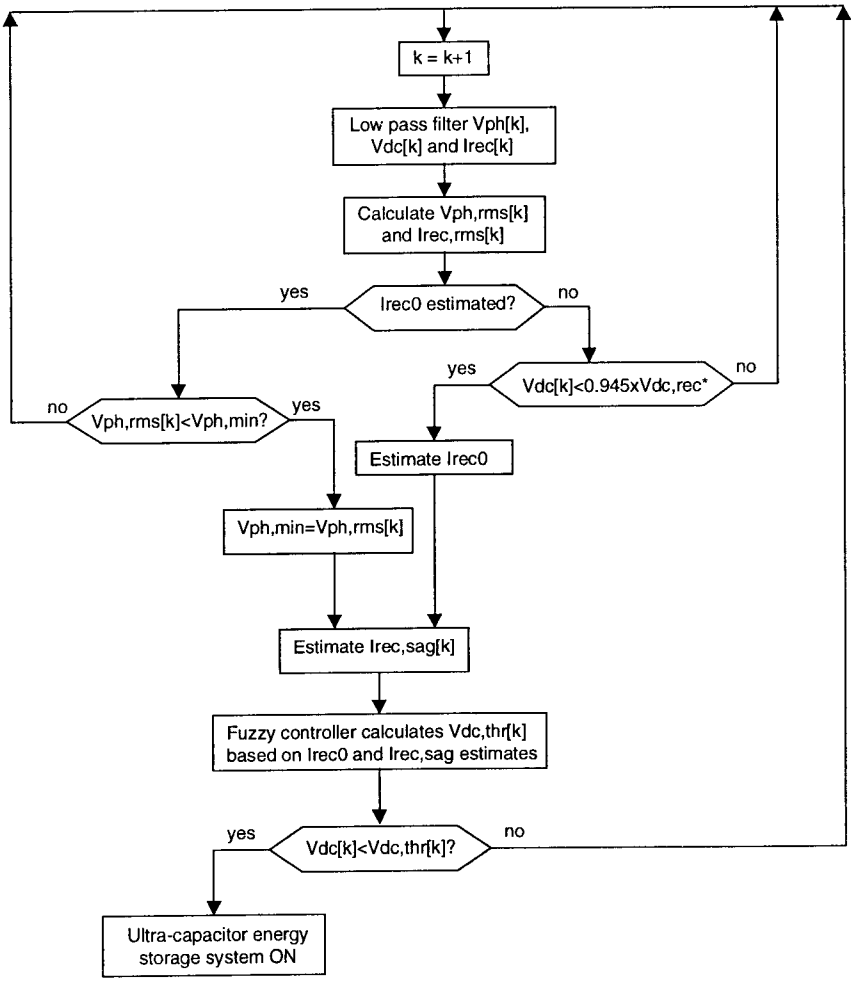


Figure 77 Flowchart for enhanced ultra-capacitor system controller

Experimental data was collected for forty cases with different sag depths and load conditions. The results of all of these cases are presented in detailed table form in Appendix K. The performance of the controller was evaluated by considering the calculated value of $V_{dc,thr}$ and rating it as *good* or *poor*. The waveforms of some cases follow with the top trace showing the rms values of the measured rectifier input phase voltages and the middle trace showing the dc bus voltage V_{dc} as well as the calculated value of $V_{dc,thr}$. If the dc bus voltage drops below $V_{dc,thr}$, the ultra-capacitor system controller would be engaged. The bottom trace shows the rms value of the measured rectifier input current as well as the estimate of the rectifier input current. The initial threshold voltage $V_{dc,thr}$ is set to 87.5% of the nominal dc bus voltage, i.e. 332.5V.

Experimental data from a case where the ASD is subjected to a 70% load and a shallow sag of 18% is shown in Figure 78. The dc bus voltage in this case does not drop below 94.5% of nominal and the fuzzy logic controller is not activated and the threshold voltage therefore remains set at 87.5% of nominal.

The cases shown in Figure 79 and Figure 80 are for sags of 30% and 43% respectively with the ASD at 45% load. In both cases an accurate estimate of the rectifier input current is made and $V_{dc,thr}$ is set to a low value of 334V, i.e. 88% of nominal, since the rectifier can provide ride-through of this sag. The controller therefore made *good* decisions.

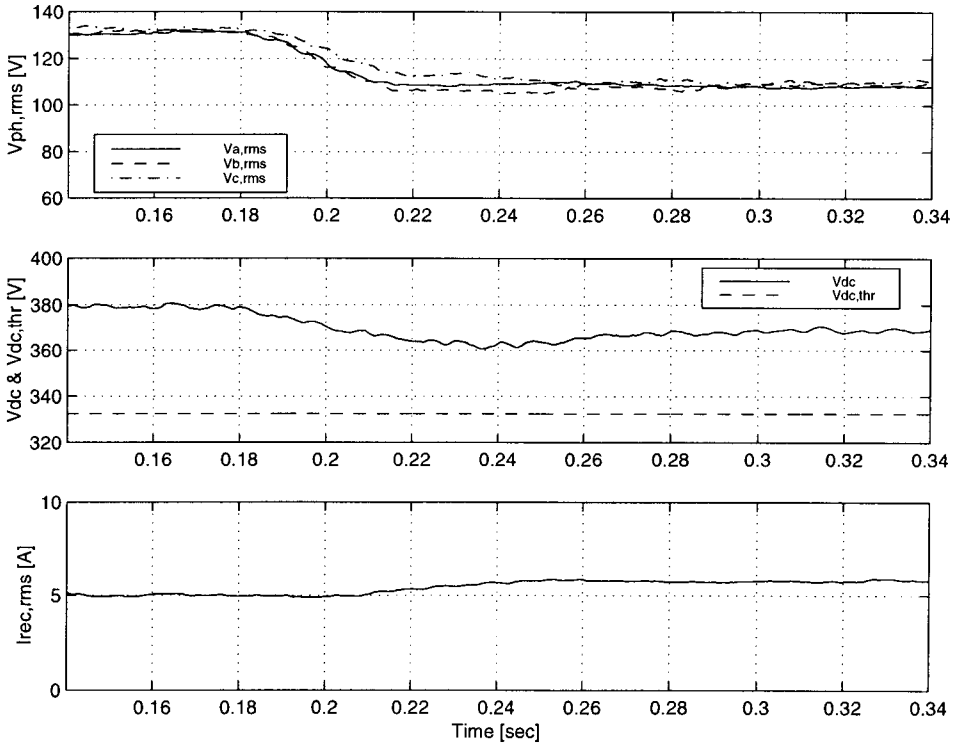


Figure 78 Experimental results and controller response for 18% sag at 70% load

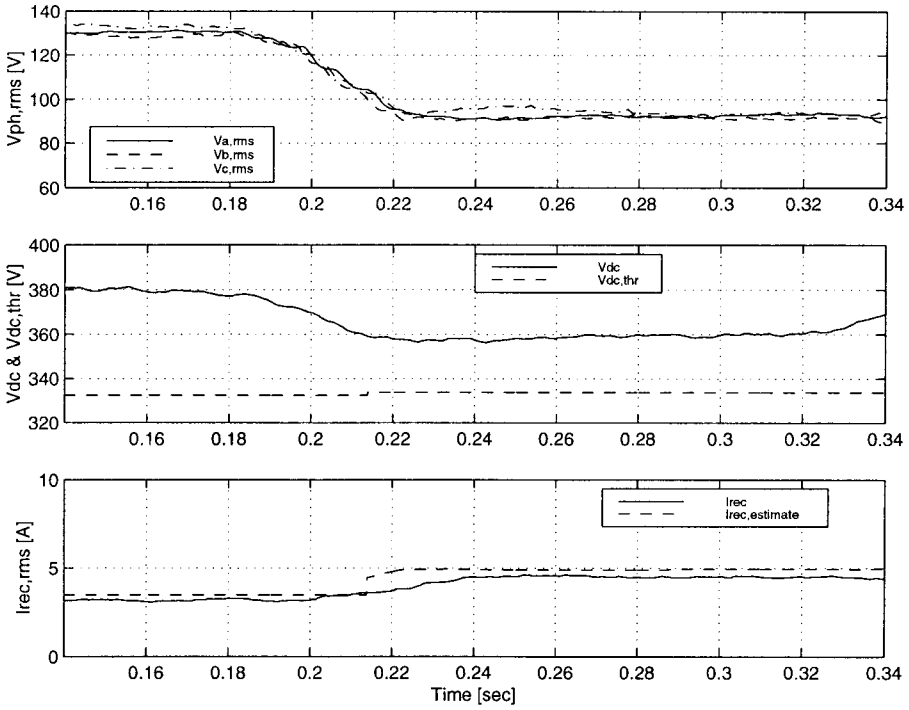


Figure 79 Experimental results and controller response for 30% sag at 45% load

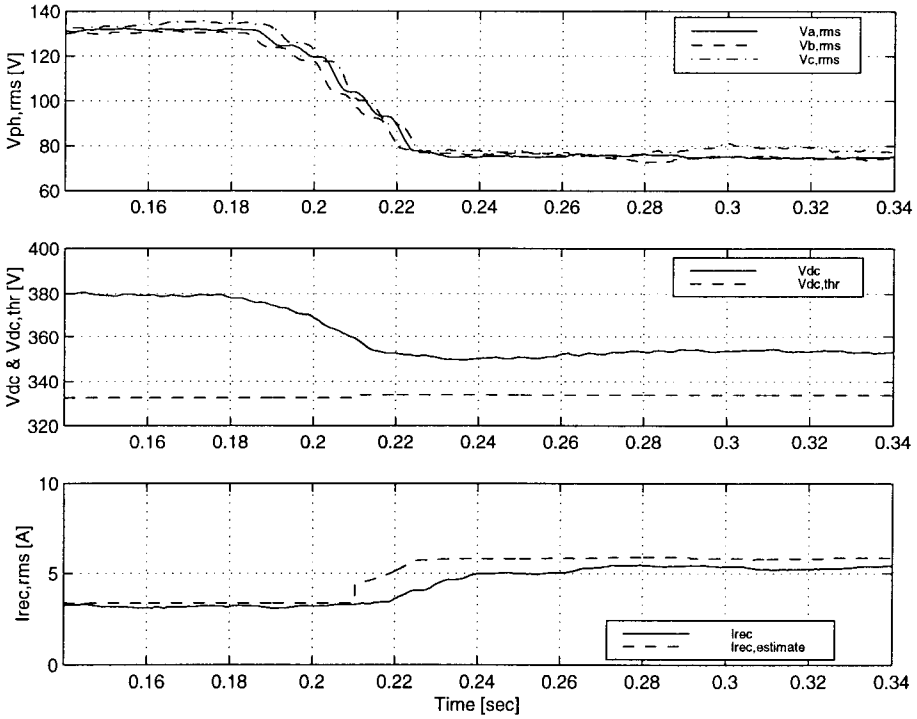


Figure 80 Experimental results and controller response for 43% sag at 45% load

The case shown in Figure 81 is for a sag of 30% with the ASD at 70% load. The controller sets $V_{dc,thr}$ to a value of 340V, i.e. 89% of nominal, and the minimum dc bus voltage is 354V, i.e. 93% of nominal, therefore the ultra-capacitor system would not have been engaged which is a *good* decision since the active rectifier can provide ride-through. An accurate estimation of the rectifier input current is made.

The accuracy of the estimates of the rectifier input current deteriorates as the load on the ASD is increased, as illustrated in Figure 82 for a 30% sag at 75% load. This is a result of poor dc bus voltage regulation at high loads which leads to fluctuations in the dc bus voltage which are not a result of average active power variations as assumed in the derivation of the formula for the estimate of the rectifier input current. Since the measured dc bus voltage is squared, the estimate is very sensitive to dc bus voltage fluctuations. The poorly regulated dc bus voltage also leads to fluctuations in the rectifier input current and therefore the current estimation error cannot be accurately known. In Figure 82 a case is shown where an inaccurate estimate of the rectifier input current is made as a result of poor dc bus voltage regulation. The ultra-capacitor system controller still makes a *good* decision in setting $V_{dc,thr}$ to a low value of 88% of nominal, i.e. 333.7V, since the active rectifier can provide ride-through and is able to limit the minimum dc bus voltage to 356V, i.e. 94% of nominal.

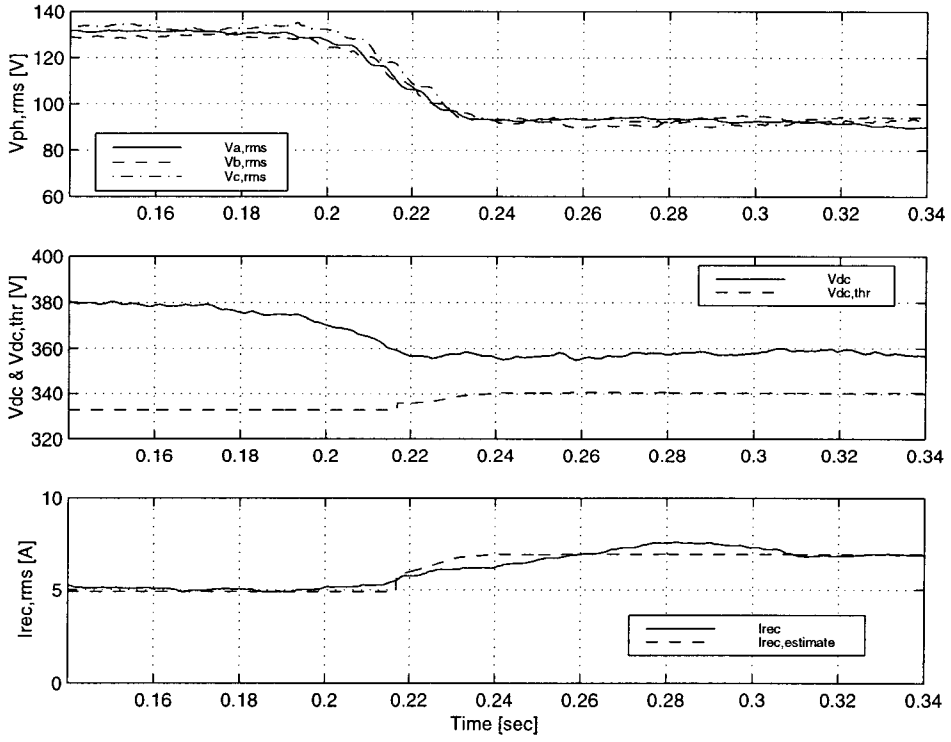


Figure 81 Experimental results and controller response for 30% sag at 70% load

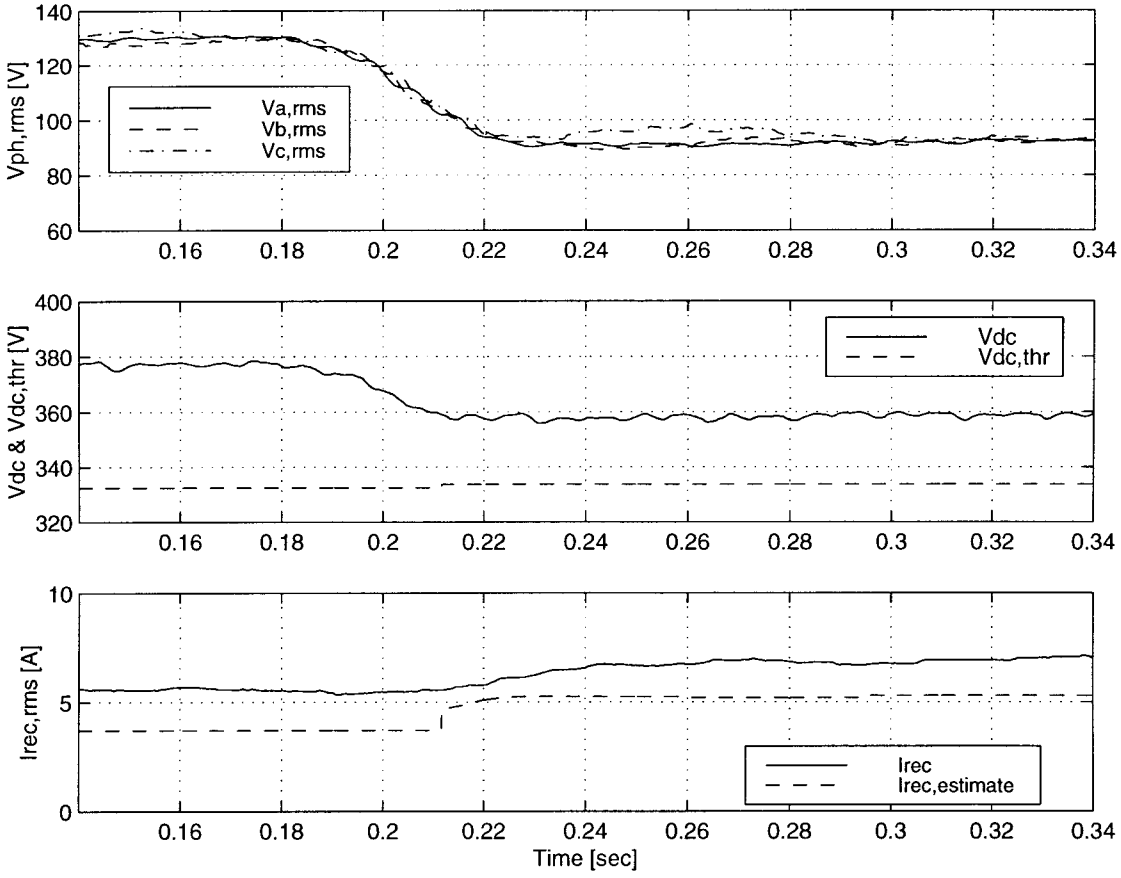


Figure 82 Experimental results and controller response for 30% sag at 75% load

The fluctuations seen by the controller can be addressed by reducing the cut-off frequency of the low pass filter for the dc bus voltage. This, however, introduces more of a time delay between the measured and filtered voltage which can result in a discrepancy between the time periods over which the average power delivered by the dc bus capacitor and the average power delivered by the rectifier are calculated. The dc bus voltage regulation can be improved by decreasing the PI gains in the rectifier, but this would also slow down the response of the rectifier. Although both these remedies were implemented to some degree, the estimation error continued to be higher at higher loads.

Of the forty cases for which controller performance was evaluated, a *poor* decision was made in only one case. The estimate of the rectifier input current is too low because of poor dc bus voltage regulation, as shown in Figure 83, which leads the ultra-capacitor system controller to determine that the rectifier would be able to provide ride-through and it therefore sets $V_{dc,thr}$ to a low value of 88% of nominal . This is a *poor* decision since the ASD cannot provide ride-through of this sag and there would be a significant drop in dc bus voltage before the ultra-capacitor system is engaged.

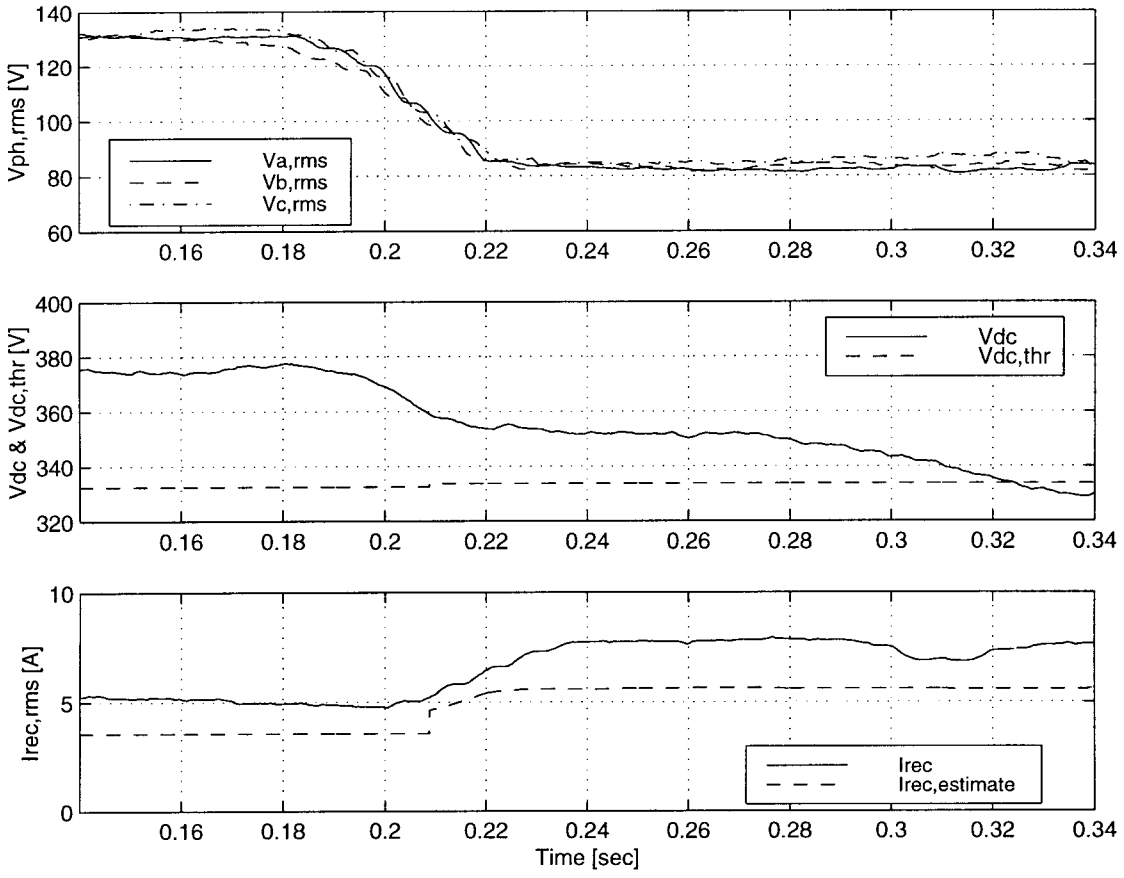


Figure 83 Experimental results and controller response for 35% sag at 75% load

5.5.4. Discussion

The performance of the proposed enhanced controller for an ultra-capacitor system to be interfaced to an ASD with an active rectifier to provide momentary interruption ride-through has been evaluated by simulation and an off-line experimental study. The enhanced controller can be used for an ultra-capacitor system which is added to an existing ASD as a retro-fit since there is no communication between the ultra-capacitor system and ASD controllers. The simulation study showed good performance over a wide range of sags and load conditions and although the *MATLAB* simulations are for an idealized system, it has been shown that it provides useful information on the average behavior of the system.

The off-line evaluation involved using experimental data collected from a 3kVA ASD with an active rectifier. The data was used as input to the fuzzy logic controller which determines the threshold voltage and then the calculated threshold voltage was rated as a *good* or *poor* result. Detailed results of the off-line experimental evaluation are presented in Appendix K. Out of forty cases considered in the

off-line experimental evaluation with a wide range of sags and load conditions, only one *poor* decision was made by the controller. In one other case an undervoltage trip was experienced for a sag of 55% at 45% load and the controller made a *good* decision based on the data available to it, but it would not have been able to prevent the ASD from tripping. There were also two cases in which the controller results were *fair* rather than *good.* Inaccurate estimates of the rectifier input current were made at higher loads as a result of poor dc bus voltage regulation and methods of improving the dc bus voltage regulation have been proposed.

5.6. CONCLUSIONS

A methodology for providing an ASD with an active rectifier with ride-through capability for sags of limited magnitude was presented in Chapter 4. In order to extend its ride-through capability to include deep sags and momentary interruptions, it is necessary to interface the ASD with an energy storage system. The suitability of ultra-capacitors as energy storage elements for this application was demonstrated in Chapter 2 and in Chapter 3 an ultra-capacitor energy storage system designed to be interfaced to an ASD with a passive rectifier to provide voltage sag and momentary interruption ride-through was presented. In this chapter it was investigated if this ultra-capacitor system could also be used as a retro-fit for ASDs with active rectifiers through a simulation and experimental study. Since both the rectifier and the boost converter of the ultra-capacitor system will attempt to regulate the dc bus voltage, it was found that the introduction of a threshold voltage $V_{dc,thr}$ at which the ultra-capacitor system is engaged, is required.

This minor change in the control algorithm of the ultra-capacitor system provides an effective way of adapting the existing system to operate with an ASD with an active rectifier. No hardware changes need to be made to the existing system and no sensors need to be added, making this a cost-effective way of extending the operating range of the existing ultra-capacitor system to include ASDs with active rectifiers.

In search of an optimum value for the threshold voltage, it was determined that system performance can be enhanced by introducing a variable threshold voltage which is set to a low value if the rectifier can provide ride-through and is set to a high value if the ultra-capacitor system would be required to provide ride-through. This will allow the ride-through capability of the active rectifier to be used before the ultra-capacitor system is engaged to regulate the dc bus voltage and will limit the minimum dc bus voltage when the active rectifier is not able to provide ride-through. A fuzzy controller was designed which takes into account both the depth of the sag and the load condition of the ASD to determine the threshold voltage.

The implementation of a variable threshold voltage would require the addition of more sensors since both the rectifier input voltages and currents are necessary to determine if the rectifier will be able to provide ride-through. This would add cost and complexity to the system, but it would improve system

performance by minimizing the unnecessary engagement of the ultra-capacitor system for shallow sags and by improving the dc bus voltage regulation for deep sags and interruptions. In order to limit the number of sensors required to implement the enhanced controller, the rectifier input current is estimated from the dc bus voltage and rectifier input phase voltage measurements. The performance of the enhanced controller was evaluated through simulation and off-line experimental work with very good results.

The addition of an ultra-capacitor energy storage system as a retro-fit to an existing ASD has been presented. The performance of the ASD can be improved by an integrated design of the ASD and the ultra-capacitor system which would allow for communication between the active rectifier and ultra-capacitor system controllers. This would eliminate the need for two separate dc bus voltage and rectifier input voltage measurement circuits and since the rectifier measures its input currents to provide current control, this information can be shared with the ultra-capacitor system controller which would remove the uncertainties introduced into the system by the estimation of the rectifier input currents. It has also been shown that the rectifier current [7] or voltage [35] sensors can be eliminated if the rectifier input voltages (currents) are measured, which would further reduce the cost and complexity of the system. The instantaneous rectifier input currents (voltages) are calculated from the rectifier input voltages (currents), dc bus voltage and switching state of the rectifier.

An integrated design of an ASD with an active rectifier and an ultra-capacitor system can therefore allow for the addition of an ultra-capacitor system to a standard design of an ASD with no additional sensors required, as long as communication between the rectifier and ultra-capacitor system controllers are provided.

6. CONCLUSIONS AND RECOMMENDATIONS

6.1. SUMMARY OF RESULTS

The awareness of electric power quality has increased over the past decade as electronic equipment has become more susceptible to power disturbances and more non-linear loads such as power electronic converters are found in the power system. The most disruptive power disturbances are voltage sags and momentary interruptions which have the potential of halting production, causing loss of data and tripping vital infrastructure equipment. Many important loads are influenced and the focus of this work is on adjustable speed drives (ASDs) which are prolific in the manufacturing industry. Industries with continuous processes, such as the textile, paper and rubber industries, are very dependent upon the reliable operation of ASDs during power disturbances for good quality products.

The focus of this work is on solutions which would provide an ASD with the capability to ride through the most common momentary interruptions and/or voltage sags in order to reduce the frequency at which the ASD trips and thereby increase its reliability. Power quality surveys conducted on the North American continent have revealed that most sags have a magnitude of less than 40% and last less than 60 cycles while most momentary interruptions last less than 3 seconds. In order to provide ASDs with the capability to ride through momentary interruptions, it is necessary to interface an energy storage system to the ASD. There are unique requirements on an energy storage system for voltage sag and momentary interruption ride-through, since a high output power capability is required, but not a very high energy density. Flywheels, ultra-capacitors and batteries were evaluated for use in an energy storage system to provide voltage sag and momentary interruption ride-through and a detailed comparison of six systems based on these technologies was presented. These technologies are developing at a fast pace, but at its current state of development it was found that the prismatic ultra-capacitor and pure lead-acid battery technologies are the best suited for use in an energy storage system for ASD ride-through.

The interface circuit between the energy storage system and ASD has a significant influence on the performance of the energy storage system and therefore interface circuits to ASDs with passive and active rectifiers were studied. A novel interface circuit by which an ultra-capacitor or battery bank can be connected directly to the input of an ASD with an active rectifier was proposed. This configuration requires a transfer switch between the grid and ultra-capacitor or battery bank and the active rectifier is used for AC/DC conversion when it is connected to the grid and for DC/DC conversion when it is connected to the ultra-capacitor or battery bank. Simulation results and a detailed thermal design of this topology were presented, but further study of this circuit fell outside the scope of this work.

Several solutions which have been suggested to provide only voltage sag ride-through to ASDs and which can be implemented by either the utility or the customer, were discussed. Compensating equipment

can be added on either the utility or the customer side and the operating characteristics of the two basic types of compensators, shunt and series, were presented as well as a summary of available compensating equipment. The interfacing of an energy storage system to a compensator or an ASD with a passive rectifier to provide ride-through of deep voltage sags and momentary interruptions was also discussed. Rather than adding compensators, the robustness of the equipment can be increased in order to provide voltage sag ride-through by appropriate drive topology or control modifications. Most of the drive topology modifications suggested for providing voltage sag ride-through focus on ASDs with passive rectifiers since they hold the largest share of the market. The thesis focused on ASDs with active rectifiers which is an emerging and growing market because of the advantages of four quadrant operation and reduced harmonics which are offered by active rectifiers.

A methodology for providing an ASD with an active rectifier with voltage sag ride-through was proposed. The depth of sag for which ride-through can be provided is a function of the load condition of the ASD and is limited by the current rating of the rectifier. The state variable description of the average behavior of the dc bus voltage, which uses only the rms values of the AC voltages and currents, was derived and this model was simulated in *MATLAB*. An adaptive PI controller which provides fast response to voltage sags was designed with the use of this simulation program. Although this model is idealized, it provides useful information on the average behavior of the dc bus voltage and the controller design was verified by a more detailed simulation using *EMTDC* and experimentally using a 3kVA prototype ASD with an active rectifier.

The addition of an ultra-capacitor energy storage system to an ASD with an active rectifier in order to provide ride-through of deeper sags and momentary interruptions was studied. At first the feasibility of using a commercial ultra-capacitor system designed to be interfaced to an ASD with a passive rectifier was investigated. Since the active rectifier and the boost converter which interfaces the ultra-capacitors to the dc bus of the ASD will try to regulate the dc bus voltage, it was found that the control algorithm of the commercial ultra-capacitor system has to be adapted in order to achieve good system response. It was shown through simulation that the introduction of a threshold voltage at which the ultra-capacitor system is engaged, is a simple and effective solution which requires no hardware changes to the existing ultra-capacitor system.

The performance of the ultra-capacitor system can however be enhanced by introducing a variable threshold voltage which is set to a low value if the rectifier can provide ride-through and to a high value if the ultra-capacitor system is needed to provide ride-through. In order to implement this variable threshold voltage, the ultra-capacitor system controller needs the rectifier input phase voltages and currents as additional inputs which adds to the cost and complexity of the system. The number of sensors required can be reduced by estimating the rectifier input current. A fuzzy logic controller was designed to determine the threshold voltage and its performance was evaluated through simulations and off-line experimental evaluation.

No communication between the ASD and the ultra-capacitor system was assumed in this design and the ultra-capacitor system can therefore be added as a retro-fit to an existing ASD. If communication is provided, the number of sensors needed can be reduced and the uncertainty introduced in the ultra-capacitor system controller through the estimation of the rectifier input current can be eliminated. This can only be done through an integrated design of the ASD and ultra-capacitor system. It is foreseen that the market for ASDs with ride-through capability of voltage sags and momentary interruptions will grow and the concepts for an integrated design of an ASD and an energy storage system presented in this thesis is a timely contribution.

6.2. Future Work and Recommendations

Currently the active rectifier is controlled to draw currents which are balanced in magnitude and phase from the grid. In order for the rectifier to draw maximum active power from the grid, the rectifier input currents and voltages need to be in phase so that all of the current processed by the rectifier will add to the active power delivered to the dc bus. The rectifier should therefore be controlled such that it can draw currents which are unbalanced in phase, but it is best to keep the magnitude of the rectifier input currents balanced so that the rectifier devices are not stressed unequally which could result in early failure of the more stressed devices. The estimation of the rectifier input current in the ultra-capacitor system controller therefore assumes that the rectifier inputs are balanced in magnitude, although it allows for unbalance in the rectifier input phase voltages and the phase of the rectifier input currents.

All the equipment, including circuit breakers, transformers and fuses, which are located upstream from the ASD will have to be derated to handle the maximum current which the ASD will draw under sag conditions. If the ASD is small in comparison to the capacity of system, the increased current drawn to provide sag ride-through will not increase the depth of the sag significantly by drawing more current across the faulted line.

The controllers for the ASD with an active rectifier and the ultra-capacitor system were developed independently from one another, with the assumption that no communication is provided between the two controllers. This allows for the addition of the ultra-capacitor system to an existing ASD, but if communication between the ultra-capacitor system and ASD is provided, the number of sensors required can be reduced and the estimation of the rectifier input currents can be eliminated. The number of sensors required can be further reduced by calculating the rectifier input currents (voltages) using the measured rectifier input phase voltage (current), dc bus voltage and switching state information of the rectifier.

Since the performance of the enhanced ultra-capacitor system controller could not be experimentally verified, it would be desirable to design and construct a low power ultra-capacitor system which could be used for further experimental work.

6.3. CONTRIBUTION

The thesis has made a contribution to the collection of solutions available to provide adjustable speed drives (ASDs) with voltage sag and momentary interruption ride-through. By making ASDs more robust to disruptive power system disturbances such as sags and interruptions, the reliability and productivity of the processes in which the ASDs are used, will be increased. ASDs are prolific in the manufacturing industry and industries which depend on continuous processes such as the paper, textile and rubber industries, can experience heavy financial losses due to the tripping of ASDs.

Most strategies for ASD drive topology modifications focus on ASDs with passive (diode bridge) rectifiers because they hold the largest share of the market. However, ASDs with active rectifiers offer additional features of regeneration and a cleaner harmonic interface to the power system and it is expected that their market share will increase as harmonic regulations are more strictly enforced and a greater awareness of the adverse effects of harmonics on electrical equipment comes about. This study on the voltage sag ride-through ability of ASDs with active rectifiers is therefore a valid research contribution in light of the lack of work in this area and the expected growth in the market for ASDs with active rectifiers in the future.

In order to provide momentary interruption ride-through, the addition of an energy storage system is required and a detailed comparison of viable energy storage technologies for this application was presented. Comparisons of energy storage technologies for other applications, such as the electric vehicle market, is not useful for application to ASD ride-through, since there are some special requirements on the energy storage system for this application. For example, the development of energy storage technologies for the electric vehicle market focus on increasing the energy density of the energy storage elements and for ASD ride-through the power density is of much more importance than the energy density due to the short time periods over which the energy storage system will be used. Due to the fast pace at which progress is made in the development of energy storage technologies, comparisons become outdated very quickly and the comparison presented here is current and includes the latest developments in the different technologies.

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APPENDICES

APPENDIX A EMTDC SCHEMATICS OF RECTIFIER AS ENERGY STORAGE SYSTEM INTERFACE

The *EMTDC* schematics are divided into different subsystems

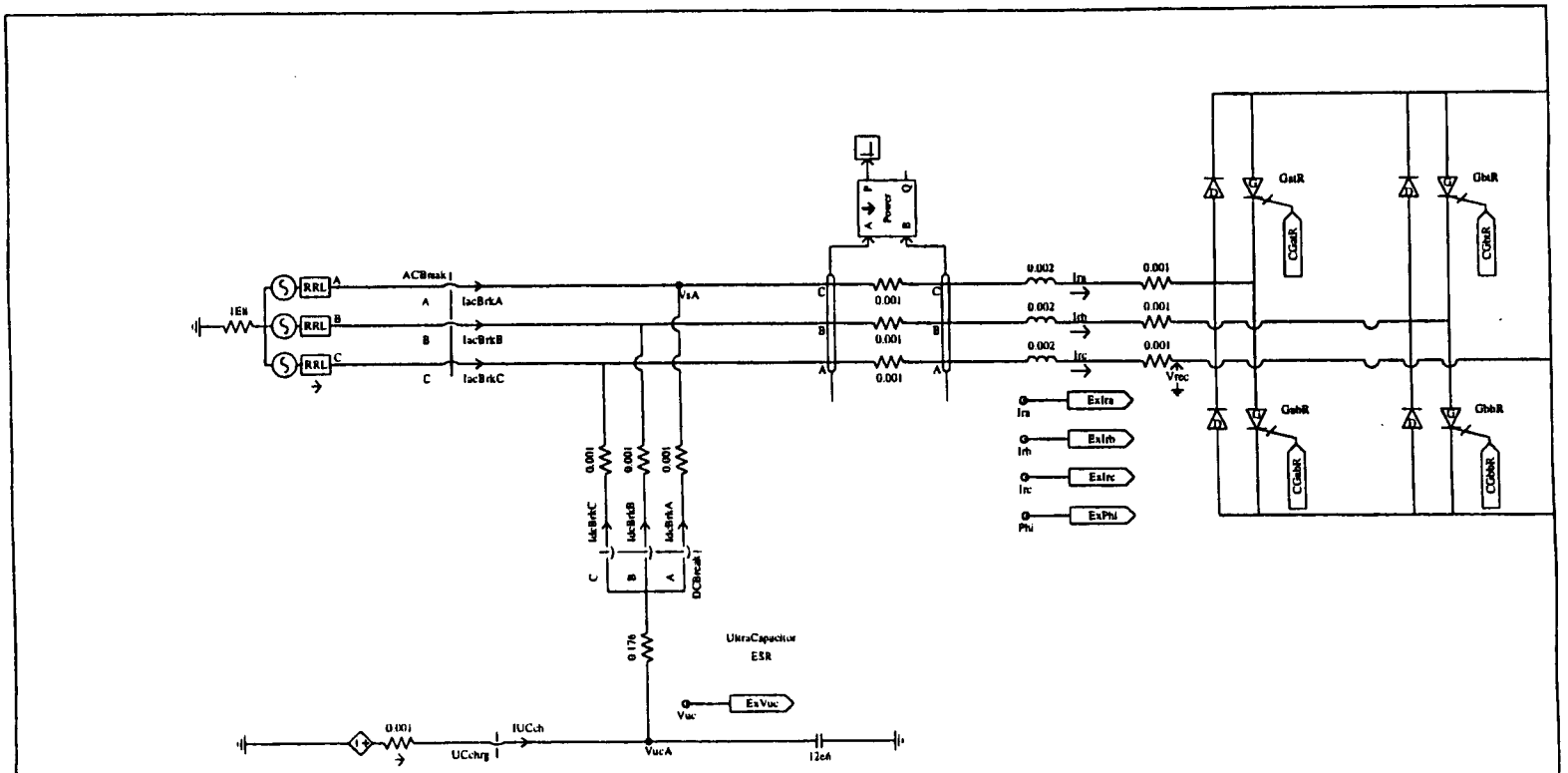
Subsystem # 1

Pages 1 – 2	:	Power electronic circuit
Page 3	:	Logic for transfer switch between the grid and the ultra-capacitors

Subsystem # 2 — Inverter current controller

Subsystem # 3

Page 1	:	PI and current controller for rectifier for DC/DC conversion
Page 2	:	Switching logic for rectifier
Page 3	:	PI and current controller for rectifier for AC/DC conversion



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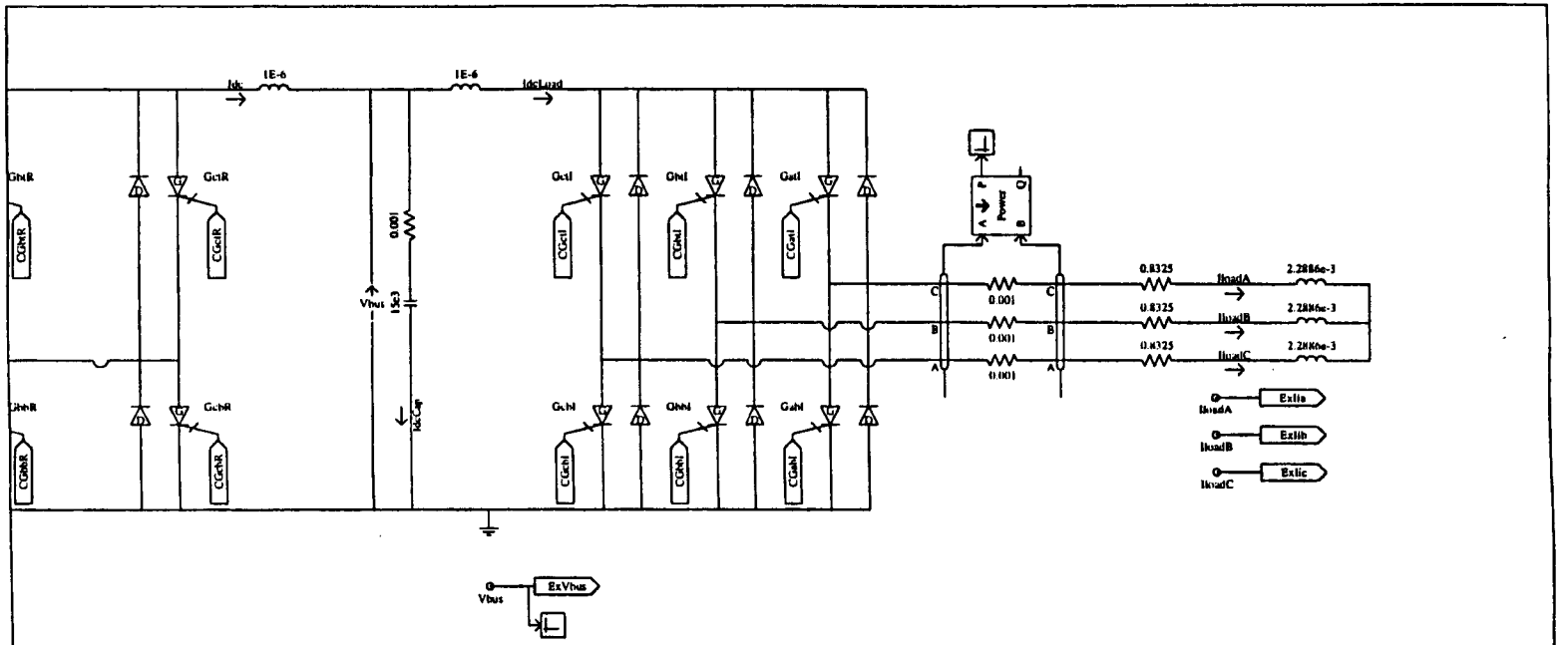

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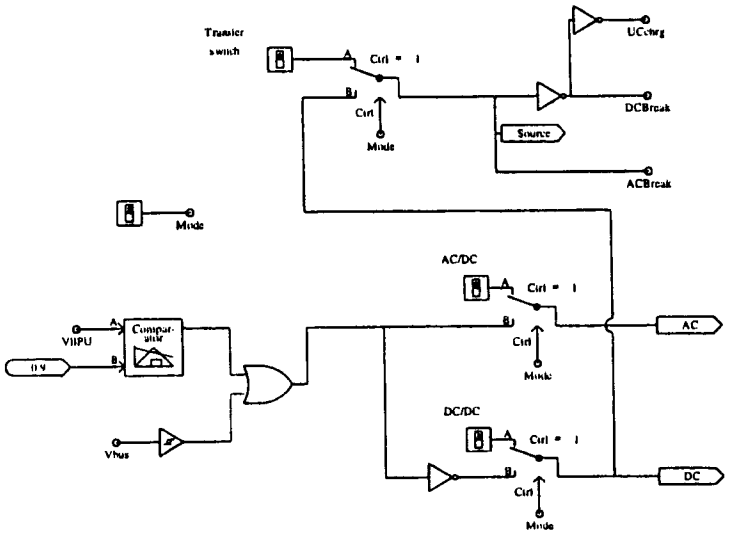

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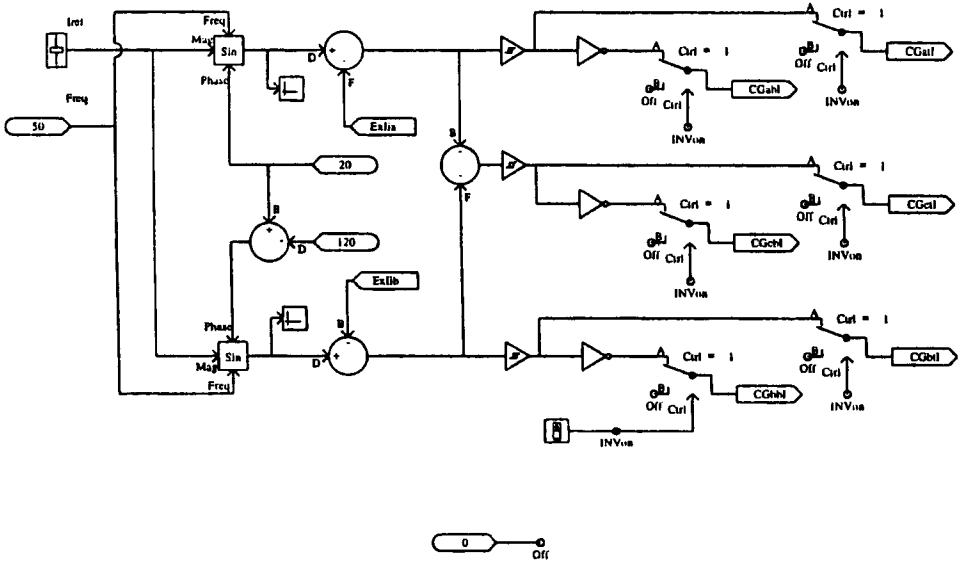

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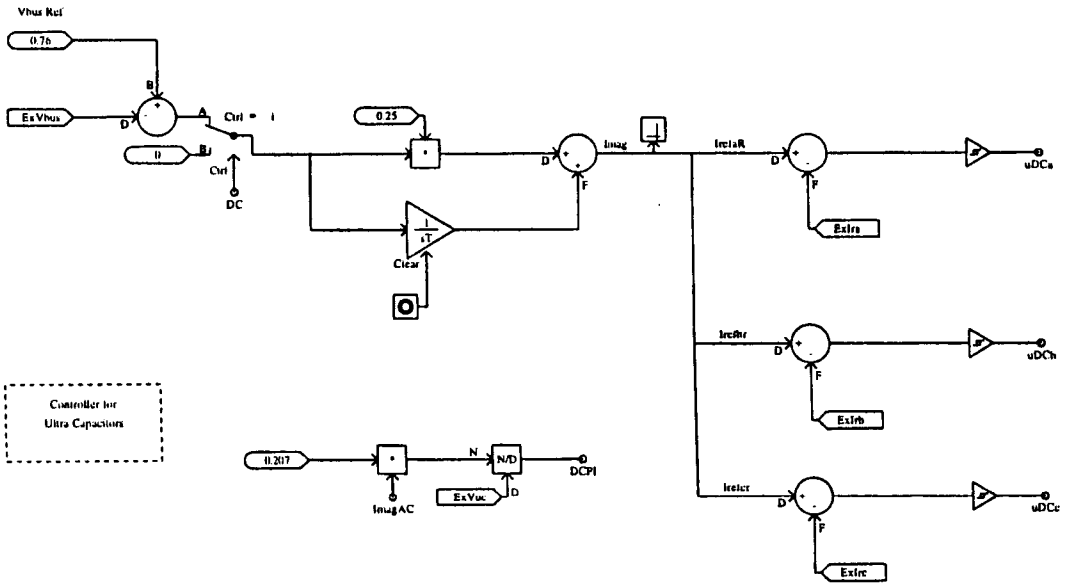

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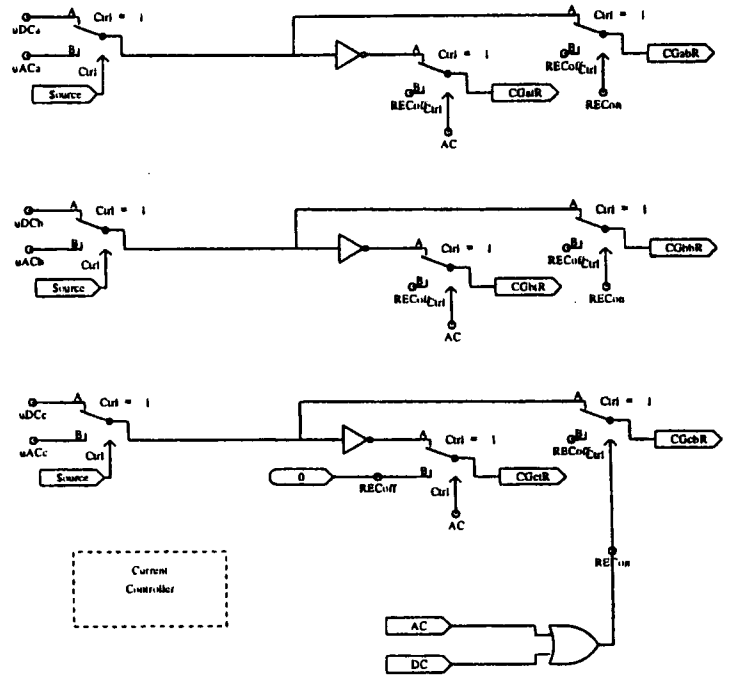

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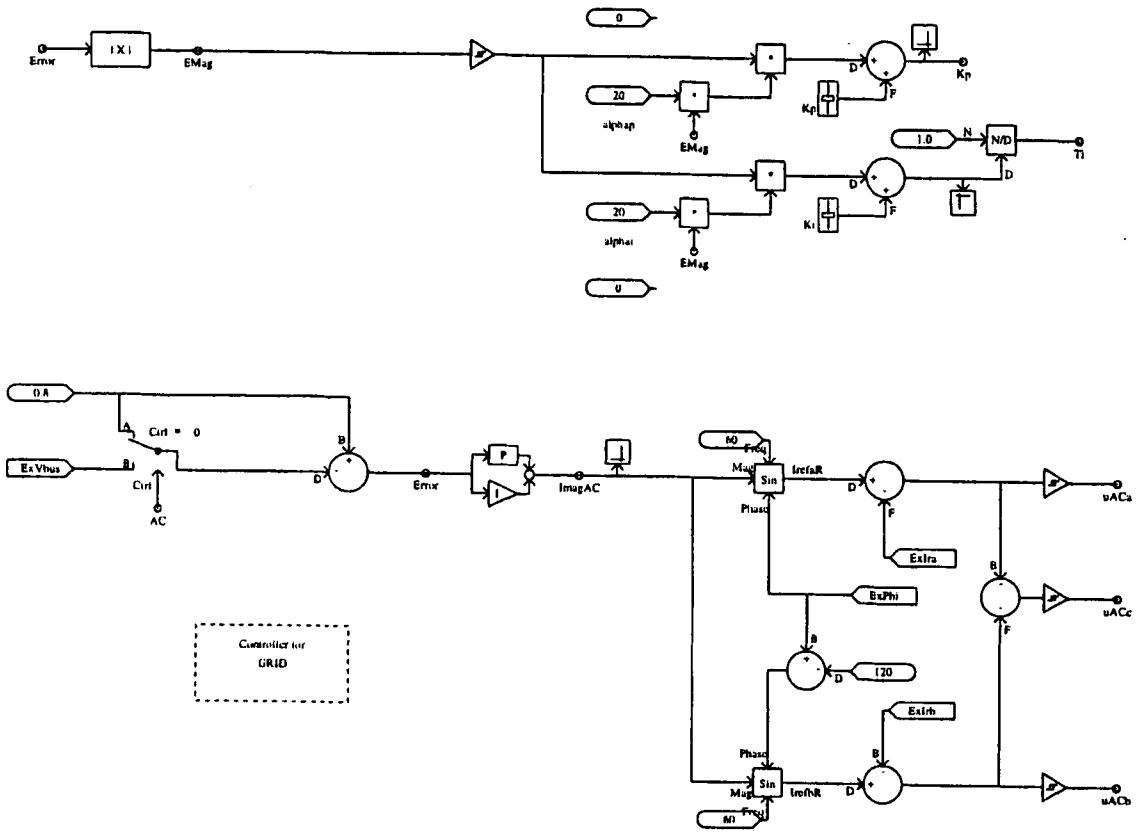

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APPENDIX B POWER DISSIPATION CALCULATIONS

In order to compare the efficiency of the rectifier used for AC/DC conversion and for DC/DC conversion, the losses under these two conversion schemes are calculated. Three POWEREX CM200DY-24H dual 200A/1200V IGBT modules are used for the rectifier. Each of these modules contains a complete phase arm and the three modules are externally connected to form a three phase converter and are all mounted on the same heatsink.

The losses are calculated for a nominal rectifier input power of 111kW and under nominal operating conditions for AC/DC conversion, the peak rectifier input current is

$$I_{rec,peak} = \frac{P_{rec,in}}{\sqrt{3}V_{ll,nom}} \times \sqrt{2} = \frac{111kW \times \sqrt{2}}{\sqrt{3} \times 480V} = 189A \qquad \textbf{(A.1)}$$

In order to provide ride-through for sags of up to 42%, a maximum peak current of 325A is required for the rectifier and therefore losses at that current are also calculated.

The maximum rectifier boost factor for DC/DC conversion is three, i.e. maximum duty cycle of 0.6667. The nominal dc bus voltage for DC/DC conversion is 760V and therefore the minimum ultra-capacitor voltage $V_{es,min}$ is equal to 760V ÷ 3 = 253V. For DC/DC conversion, the maximum input current is

$$I_{rec,\max} = \frac{P_{rec,in}}{3V_{es,\min}} = \frac{111kW}{3 \times 253V} = 146.2A \qquad \textbf{(A.2)}$$

A switching frequency of 10kHz is assumed for AC/DC and DC/DC conversion. The total losses in all of the IGBT modules combined are calculated by first calculating the losses in each IGBT and diode under AC/DC and then DC/DC conversion.

The values and formulas used to calculated the losses in the rectifier for AC/DC and DC/DC conversion respectively are given in Table 1. $V_{ce(pk)}$ is the peak voltage across the diode during recovery, t_{rr} is the diode reverse recovery time and R_{cf}, the thermal case to fin resistance, is defined per IGBT-diode pair. The total losses are calculated on a spreadsheet which is reproduced in Table 2.

The design of the heatsink is performed on a spreadsheet, reproduced in Table 3, using thermal resistance concepts to calculate the junction temperatures in the module, as shown in Figure 1. The variables in Figure 1 refer to the variables in the spreadsheet and are explained in Table 1. First the losses in the modules are determined, then the fin (heatsink), case and junction temperatures are calculated. The thermal resistance from heatsink (fin) to ambient R_{fa} is changed in the spreadsheet until all junction temperatures are under the maximum temperature (150°C) for the diodes and the IGBTs. The heatsink required has a thermal resistance R_{fa} of 0.03°C/W, therefore forced air will be required.

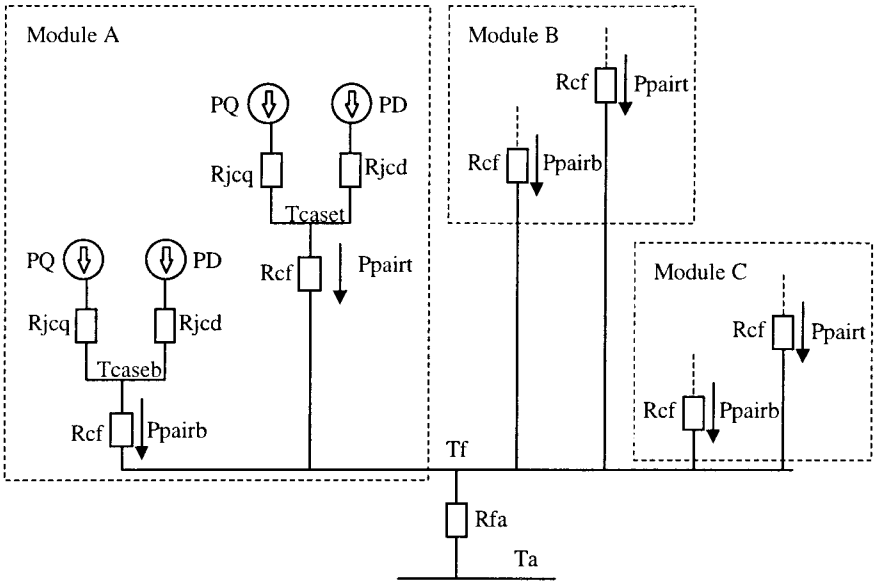

Figure 1 Thermal resistance model

Table 1 Explanation to headings in Table 2 and Table 3

Variable	Units	Description	Formula and values used for AC/DC	Formulas and values used for DC/DC
Icp	A	Peak current	189A and 325A	81.3A to 138.75A
Vce(sat)	V	Saturation voltage, collector-emitter	2.5V and 3V	2.5V
D		PWM duty factor	0.2 to 1.0	0.43 to 0.6667
PcondQ	W	Conduction loss per IGBT (PF = 1.0)	$P_{ss} = I_{cp} \times V_{ce(sat)} \times (\frac{1}{8} + \frac{D}{3\pi} \times PF)$	$P_{ss} = I_{cp} \times V_{ce(sat)} \times D$
Esw(on)	J	Energy loss when switching on	28mJ	28mJ
Esw(off)	J	Energy loss when switching off	2.5mJ	2.5mJ
PswQ	W	Switching loss per IGBT	$P_{sw} = \frac{1}{\pi} \times f_s \times (E_{sw(on)} + E_{sw(off)})$	$P_{sw} = f_s \times (E_{sw(on)} + E_{sw(off)})$
PQ	W	Total losses per IGBT	PQ = PcondQ + PswQ	PQ = PcondQ + PswQ
Irr	A	Diode peak recovery current	20A	20A
Vdf	V	Diode forward voltage drop	3.4V	3.4V
PcondD	W	Conduction loss per diode (PF = 1.0)	$P_{dc} = I_{cp} \times V_{df} \times (\frac{1}{8} - \frac{D}{3\pi} \times PF)$	$P_{dc} = I_{cp} \times V_{df} \times (1 - D)$
PrrD	W	Recovery losses in diode	$P_{rr} = 0.125 \times I_{rr} \times t_{rr} \times V_{ce(pk)} \times f_s$ $V_{ce(pk)}$ = 810V, t_{rr} = 0.25μs	$P_{rr} = 0.125 \times I_{rr} \times t_{rr} \times V_{ce(pk)} \times f_s$ $V_{ce(pk)}$ = 810V, t_{rr} = 0.25μs
PD	W	Total losses in one diode	PD = PcondD + PrrD	PD = PcondD + PrrD
Ppairt	W	Losses in top diode-IGBT pair	Ppairt = PD + PQ	Ppairt = PD
Ppairb	W	Losses in bottom diode-IGBT pair	Ppairb = Ppairt = PD + PQ	Ppairb = PQ
Pmodule	W	Losses in one module	Pmodule = Ppairb + Ppairt	Pmodule = Ppairb + Ppairt
Ptotal	W	Total losses in all three modules	Ptotal = Pmodule x 3	Ptotal = Pmodule x 3
Ta	°C	Ambient temperature in Celsius	30 °C	30 °C
Rfa	°C/W	Thermal resistance from heatsink (fin) to ambient	[design para]	[design para]
Tf	°C	Heatsink (fin) temperature	Tf = Ta + Ptotal x Rfa	Tf = Ta + Ptotal x Rfa
Tcaset	°C	Module case for top diode-IGBT pair	Tcaset = Tf + Ppairt x Rcf Rcf = 0.09 °C/W	Tcaset = Tf + Ppairt x Rcf Rcf = 0.09 °C/W
Tcaseb	°C	Module case for bottom diode-IGBT pair	Tcaseb = Tf + Ppairb x Rcf Rcf = 0.09 °C/W	Tcaseb = Tf + Ppairb x Rcf Rcf = 0.09 °C/W
TjD	°C	Junction temperature of diode	TjD = Tcaset + PD x Rjcd = Tcaseb + PD x Rjcd Rjcd = 0.18 °C/W	TjD = Tcaset + PD x Rjcd Rjcd = 0.18 °C/W
TjQ	°C	Junction temperature of IGBT	TjQ = Tcaseb + PQ x Rjcq = Tcaset + PQ x Rjcq Rjcq = 0.085 °C/W	TjQ = Tcaseb + PQ x Rjcq Rjcq = 0.085 °C/W

Table 2 Calculation of power dissipation in rectifier

Icp	Vce(sat)	D	PcondQ	Esw(on)	Esw(off)	PswQ	PQ	Irr	Vdf	PcondD	PrrD	PD	Ppairt	Ppairb	Pmodule	Ptotal
[A]	[V]		[W]	[J]	[J]	[W]	[W]	[A]	[V]	[W]	[W]	[W]	[W]	[W]	[W]	[W]
AC/DC – normal operation																
189.00	2.5	0.2	69.0893	0.0280	0.0025	97.0845	166.1738	20.0	3.4	66.6886	5.0625	71.7511	237.9249	237.9249	475.8498	1427.5493
189.00	2.5	0.4	79.1160	0.0280	0.0025	97.0845	176.2005	20.0	3.4	53.0522	5.0625	58.1147	234.3152	234.3152	468.6305	1405.8915
189.00	2.5	0.6	89.1428	0.0280	0.0025	97.0845	186.2273	20.0	3.4	39.4158	5.0625	44.4783	230.7056	230.7056	461.4112	1384.2337
189.00	2.5	0.8	99.1695	0.0280	0.0025	97.0845	196.2541	20.0	3.4	25.7794	5.0625	30.8419	227.0960	227.0960	454.1920	1362.5759
189.00	2.5	1.0	109.1963	0.0280	0.0025	97.0845	206.2808	20.0	3.4	12.1430	5.0625	17.2055	223.4863	223.4863	446.9727	1340.9181
AC/DC – maximum current																
325.00	3.0	0.2	142.5651	0.0280	0.0025	97.0845	239.6497	20.0	3.4	114.6762	5.0625	119.7387	359.3883	359.3883	718.7767	2156.3300
325.00	3.0	0.4	163.2553	0.0280	0.0025	97.0845	260.3398	20.0	3.4	91.2273	5.0625	96.2898	356.6296	356.6296	713.2593	2139.7779
325.00	3.0	0.6	183.9454	0.0280	0.0025	97.0845	281.0299	20.0	3.4	67.7785	5.0625	72.8410	353.8710	353.8710	707.7419	2123.2257
325.00	3.0	0.8	204.6356	0.0280	0.0025	97.0845	301.7201	20.0	3.4	44.3297	5.0625	49.3922	351.1123	351.1123	702.2245	2106.6736
325.00	3.0	1.0	225.3257	0.0280	0.0025	97.0845	322.4102	20.0	3.4	20.8809	5.0625	25.9434	348.3536	348.3536	696.7072	2090.1215
DC/DC																
81.30	2.5	0.4	81.3000	0.0280	0.0025	305.0000	386.3000	20.0	3.4	165.8520	5.0625	170.9145	170.9145	386.3000	557.2145	1671.6435
97.37	2.5	0.5	121.7125	0.0280	0.0025	305.0000	426.7125	20.0	3.4	165.5290	5.0625	170.5915	170.5915	426.7125	597.3040	1791.9120
121.70	2.5	0.6	182.5500	0.0280	0.0025	305.0000	487.5500	20.0	3.4	165.5120	5.0625	170.5745	170.5745	487.5500	658.1245	1974.3735
146.25	2.5	0.667	243.7622	0.0280	0.0025	305.0000	548.7622	20.0	3.4	165.7334	5.0625	170.7959	170.7959	548.7622	719.5581	2158.6743

Table 3 Calculation of junction temperatures in rectifier

PQ	Irr	Vdf	PcondD	PrrD	PD	Ppairt	Ppairb	Pmodule	Ptotal	Ta	Rfa	Tf	Tcaset	Tcaseb	TjD	TjQ
[W]	[A]	[V]	[W]	[W]	[W]	[W]	[W]	[W]	[W]	[C]	[C/W]	[C]	[C]	[C]	[C]	[C]
AC/DC – normal operation																
166.1738	20.0	3.4	66.6886	5.0625	71.7511	237.9249	237.9249	475.8498	1427.5493	30.0000	0.0300	72.8265	94.2397	94.2397	107.1549	108.3645
176.2005	20.0	3.4	53.0522	5.0625	58.1147	234.3152	234.3152	468.6305	1405.8915	30.0000	0.0300	72.1767	93.2651	93.2651	103.7258	108.2422
186.2273	20.0	3.4	39.4158	5.0625	44.4783	230.7056	230.7056	461.4112	1384.2337	30.0000	0.0300	71.5270	92.2905	92.2905	100.2966	108.1198
196.2541	20.0	3.4	25.7794	5.0625	30.8419	227.0960	227.0960	454.1920	1362.5759	30.0000	0.0300	70.8773	91.3159	91.3159	96.8675	107.9975
206.2808	20.0	3.4	12.1430	5.0625	17.2055	223.4863	223.4863	446.9727	1340.9181	30.0000	0.0300	70.2275	90.3413	90.3413	93.4383	107.8752
AC/DC – maximum current																
239.6497	20.0	3.4	114.6762	5.0625	119.7387	359.3883	359.3883	718.7767	2156.3300	30.0000	0.0300	94.6899	127.0348	127.0348	148.5878	147.4051
260.3398	20.0	3.4	91.2273	5.0625	96.2898	356.6296	356.6296	713.2593	2139.7779	30.0000	0.0300	94.1933	126.2900	126.2900	143.6222	148.4189
281.0299	20.0	3.4	67.7785	5.0625	72.8410	353.8710	353.8710	707.7419	2123.2257	30.0000	0.0300	93.6968	125.5452	125.5452	138.6565	149.4327
301.7201	20.0	3.4	44.3297	5.0625	49.3922	351.1123	351.1123	702.2245	2106.6736	30.0000	0.0300	93.2002	124.8003	124.8003	133.6909	150.4465
322.4102	20.0	3.4	20.8809	5.0625	25.9434	348.3536	348.3536	696.7072	2090.1215	30.0000	0.0300	92.7036	124.0555	124.0555	128.7253	151.4603
DC/DC																
386.3000	20.0	3.4	165.8520	5.0625	170.9145	170.9145	386.3000	557.2145	1671.6435	30.0000	0.0300	80.1493	95.5316	114.9163	126.2962	128.3671
426.7125	20.0	3.4	165.5290	5.0625	170.5915	170.5915	426.7125	597.3040	1791.9120	30.0000	0.0300	83.7574	99.1106	122.1615	129.8171	135.3812
487.5500	20.0	3.4	165.5120	5.0625	170.5745	170.5745	487.5500	658.1245	1974.3735	30.0000	0.0300	89.2312	104.5829	133.1107	135.2863	146.0247
548.7622	20.0	3.4	165.7334	5.0625	170.7959	170.7959	548.7622	719.5581	2158.6743	30.0000	0.0300	94.7602	110.1319	144.1488	140.8751	156.7766

In summary, for AC/DC conversion under normal conditions, i.e. with the rectifier input voltage equal to 480V, the total losses in all three of the rectifier modules are approximately 1.3% of the input power, i.e. 1.4kW, and when the maximum current of 230A is drawn, the total losses are approximately 1.9%. The total losses for DC/DC conversion increase from 1.5% to 1.8% as the duty ratio and input current increase.

The junction temperatures of the diodes and IGBTs in the modules were calculated and it was found that the diode junction temperatures under the worst case conditions for AC/DC conversion are 8°C higher than for the worst case DC/DC conversion conditions. The IGBT junction temperatures under the worst case conditions is 6 °C higher for DC/DC conversion than for AC/DC.

APPENDIX C MATLAB PROGRAM LISTING FOR ULTRA-CAPACITOR SIZING

```
% ultracap.m
% last modified 11/21/98
% Annabelle van Zyl
% Solves capacitor voltage for ultracap discharge, constant power load
% Equations contained in modelultracap.m

clear;

global R C P dvcdt;

figure(1);
clf;
subplot(3,1,1); hold on;
subplot(3,1,2); hold on;
subplot(3,1,3); hold on;

%Maxwell data
for nser = 8:1:9
 %nser = 9;        %number of ultracap units in series
 P = 100e3/0.9;      %assume 90% efficient converter
 R = nser*22e-3;
 C = 96/nser;
 Initcapvolt = [-nser*56];


 tspan = [0 6];
 t = 0;
 dvcdt = 0;
 capvolt = 0;
 capcurr = 0;
 energy = 0;

 options = odeset('MaxStep',0.01);
 [t,capvolt] = ode45('ultracapmodel',tspan,Initcapvolt,options);

 voltdiff = diff(capvolt);
 timediff = diff(t);
 capcurr = C*voltdiff./timediff;
 capvolt = capvolt(1:size(voltdiff,1));
 busvoltage = -capvolt-capcurr*R;
 lastvoltage = busvoltage(size(busvoltage,1));
 power = capcurr.*busvoltage;
 Enstored = 0.5*C*Initcapvolt^2;
 t = t(1:size(voltdiff,1));
 energy(1) = 0;
 for N = 2:size(t)
  energy(N) = power(N-1)*timediff(N-1)+energy(N-1);
 end
 energy = energy/Enstored*100;      % for %
 ss = size(energy);
 %energy = power.*t/Enstored;

 if nser == 8
  busvoltage8 = busvoltage;
  capcurr8 = capcurr;
  energy8 = energy;
 else
  busvoltage9 = busvoltage;
  capcurr9 = capcurr;
  energy9 = energy;
```

```
 end

end

figure(1);
subplot(3,1,1);
 plot(t,busvoltage8,t,busvoltage9,'--');
 legend('N = 8','N = 9',3);
 grid;
 ylabel('Capacitor voltage [V]');
subplot(3,1,2);
 plot(t,capcurr8,t,capcurr9,'--');
 legend('N = 8','N = 9',4);
 axis([0 6 0 600]);
 ylabel('Capacitor current [A]');
 grid;
subplot(3,1,3);
 plot(t,energy8,t,energy9,'--');
 legend('N = 8','N = 9',2);
 grid;
 ylabel('Delivered energy [%]');
 xlabel('Time [sec]');

print('-f1','-deps2','/nfs/stak/u2/v/vanzyl/phd/pictures/ucapsize.eps')
```

```
function dvcdt = modelcapvolt(t,capvolt);

global R C P dvcdt;

% ultracapmodel.m
% 26 January 1997
% Annabelle van Zyl
% Contains differential equations for ultracap.m.m

if t<1
 Pcap = 0;
else
 Pcap = P;
end

dvcdt = -R*C/capvolt*(dvcdt)^2 - Pcap/C/capvolt;
```

APPENDIX D EXPERIMENTAL EVALUATION OF ULTRA-CAPACITORS

More details about the experimental evaluation of the ultra-capacitors are given here which were not furnished in the main body of the thesis.

1.1 Experimental Setup for Constant Load Test

The parameters of the bipolar ultra-capacitor were calculated from the test results of a constant load test and the experimental setup is shown in Figure 2, with the system parameters listed in Table 4.

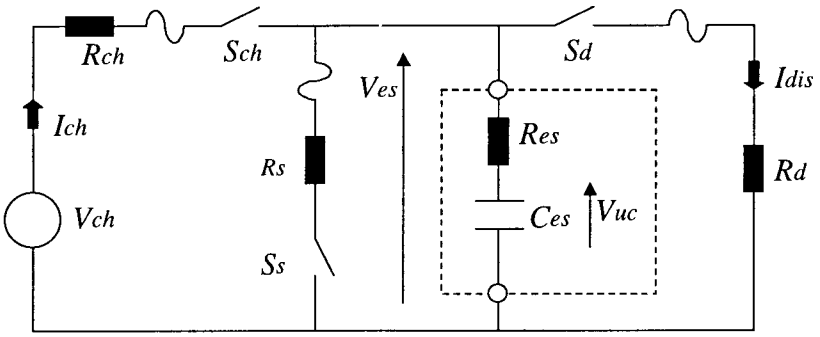

Figure 2 Experimental setup for constant load test

Table 4 System parameters for ultra-capacitor constant load test experimental setup

Voltage source	V_{ch}	variable, 0 – 600V
Charge resistance	R_{ch}	4.3Ω
Charge circuit breaker	S_{ch}	100A, 500V_{ac}
Short circuit resistance	R_s	1Ω
Short circuit breaker	S_s	40A, 250V_{dc}
Discharge circuit breaker	S_d	100A, 500V_{ac}
Discharge resistance	R_d	variable, 0 – 20Ω
Semiconductor fuses		60A, 450V_{dc}

1.2 Evaluation of Temperature Performance of the Bipolar Ultra-Capacitor

The same experimental setup as for the constant load test was used to evaluate the temperature performance of the bipolar ultra-capacitors under repeated discharge and charge cycles. The following procedure was followed:

1. Charge capacitor to 135V (measured while charge current is flowing) with *HP* dc power supply. The charging current is 8.5A for voltages below 115V and above 115V it drops gradually, reaching 5.5A at 135V.
2. Open charging circuit breaker S_{ch}
3. Record voltage V_{cf}, temperature T_f and time t_f five to ten seconds after breaker is opened
4. Discharge capacitor to 70V (measured while discharge current is flowing) into a resistance of 5.8Ω
5. Open discharging circuit breaker S_d
6. Record voltage V_{cf}, temperature T_f and time t_f five to ten seconds after breaker is opened

Due to heating in the load resistor, a fan was turned on during discharge #5 to cool down the load resistor. The test results are summarized in Table 5.

Table 5 Results of charge and discharge cycling test on bipolar ultra-capacitor

Cycle #	Charge				Discharge			
	V_{cf} [V]	T_f [°C]	t_f [min]	dT	V_{cf} [V]	T_f [°C]	t_f [min]	dT
1	127.20	26.40	0		84.50	26.90	2	0.50
2	127.50	27.84	5	0.94	84.20	28.20	6	0.36
3	127.90	29.20	8	1.00	84.00	29.55	10	0.35
4	128.10	30.40	13	0.85	82.70	30.75	15	0.35
5	128.50	31.62	17	0.87	82.90	32.00	19	0.38
6	128.50	32.82	21	0.82	82.60	33.30	23	0.48
7	128.60	34.10	26	0.80	82.20	34.56	28	0.46
8	128.80	35.42	30	0.86	82.30	35.82	32	0.40
9	128.80	36.60	34	0.78	82.20	37.00	36	0.40
10	128.90	37.85	38	0.85	82.20	38.26	40	0.41

APPENDIX E MATLAB PROGRAM LISTINGS FOR COMPENSATION STRATEGY COMPARISON

```
% Annabelle van Zyl
% ic.m
% Originally written in 1996, Last modified 11/18/98
% Program to calculate the needed compensating current for
% a shunt voltage sag compensator. The active component of the
% compensating current is minimized.

clear;
kmax = 197;
figure(1);
clf;
subplot(3,1,1); hold on;
subplot(3,1,2); hold on;
subplot(3,1,3); hold on;
figure(2);
clf;

%Normal bus voltage
Vbnom = 12e3;

%Desired load voltage amplitude
VloadA = 11.85e3;
%Line impedance
Zline = 0.01 + 2*pi*60*0.005*i;
Zline = 2*Zline;

cnts = 0;
%Calculate bus voltage under fault condition
for sag = 0:20:40
 cnts = cnts+1;
 Vb(cnts) = (100-sag)/100*Vbnom;

 %Equivalent load impedance at desired load voltage
 Zload = 45+16.5*i;
 phi = angle(Zload);

 %Calculate Ic for different load voltage angles
  for k = 1:(kmax+1)
   %Load voltage angle
   si(k) = -pi/18+(k-1)*pi/9/kmax;
   Vload(k) = VloadA*cos(si(k))+VloadA*sin(si(k))*i;
   Iload(cnts,k) = VloadA/abs(Zload);
   Iload(cnts,k) = Iload(cnts,k)*(cos(si(k)-phi)+sin(si(k)-phi)*i);
   Vline(cnts,k) = Vb(cnts) - Vload(k);
   Iline(cnts,k) = Vline(cnts,k)/Zline;
   Ic(cnts,k) = Iload(k) - Iline(cnts,k);
   tau(cnts,k) = angle(Ic(cnts,k));
   theta(cnts,k) = tau(cnts,k)-si(k);
   Icp(cnts,k) = abs(Ic(cnts,k))*cos(theta(cnts,k));
   Icq(cnts,k) = abs(Ic(cnts,k))*sin(theta(cnts,k));
   Sio(cnts,k) = Vload(k)*conj(Ic(cnts,k));
   Sline(cnts,k) = Vline(k)*conj(Iline(cnts,k));
   Sload(cnts,k) = Vload(k)*conj(Iload(cnts,k));
  end
  degrees = si/pi*180;

end

deg = degrees;
```

```
Sio = Sio/1e6;
Sline = Sline/1e6;
Sload = Sload/1e6;
Ic = Ic/1e3;
Iline = Iline/1e3;


figure(1);
subplot(3,1,1);
plot(deg,real(Sio(1,:)),deg,real(Sio(2,:)),'--',deg,real(Sio(3,:)),'-.');
subplot(3,1,2);
plot(deg,imag(Sio(1,:)),deg,imag(Sio(2,:)),'--',deg,imag(Sio(3,:)),'-.');
subplot(3,1,3);
plot(deg,abs(Ic(1,:)),deg,abs(Ic(2,:)),'--',deg,abs(Ic(3,:)),'-.');
subplot(3,1,1);
  grid;
  ylabel('Pc [MW]');
  legend('sag = 0%','sag = 20%','sag = 40%',4);
subplot(3,1,2);
  grid;
  ylabel('Qc [MVAr]');
  legend('sag = 0%','sag = 20%','sag = 40%',4);
subplot(3,1,3);
  grid;
  ylabel('Ic [kA]');
  legend('sag = 0%','sag = 20%','sag = 40%',4);
  xlabel('Psi [deg]');

figure(2);
plot(deg,abs(Iline(1,:)),deg,abs(Iline(2,:)),'--',deg,abs(Iline(3,:)),'-.');
 legend('sag = 0%','sag = 20%','sag = 40%',0);
 grid;
 ylabel('Iline [kA]');
 xlabel('Psi [deg]');


print('-f1','-deps2','/nfs/stak/u2/v/vanzyl/phd/pictures/ic.eps');
print('-f2','-deps2','/nfs/stak/u2/v/vanzyl/phd/pictures/ic2.eps');
```

```
% Annabelle van Zyl
% vc.m
% Originally written in 1996, Last modified 11/18/98
% Program to calculate the needed compensating voltage for
% a series voltage sag compensator.

clear;
kmax =197;
figure(1);
clf;
subplot(3,1,1); hold on;
subplot(3,1,2); hold on;
subplot(3,1,3); hold on;

%Normal bus voltage
Vbnom = 12e3;

%Desired load voltage amplitude
VloadA = 11.85e3;
%Line impedance
Zline = 0.01 + 2*pi*60*0.005*i;
Zline = 2*Zline;

cnts = 0;
%Calculate bus voltage under fault condition
for sag = 0:20:40
 cnts = cnts+1;
 Vb(cnts) = (100-sag)/100*Vbnom;

 %Equivalent load impedance at desired load voltage
 Zload = 45+16.5*i;
 phi = angle(Zload);

 %Calculate Ic for different load voltage angles
 for k = 1:(kmax+1)
  %Load voltage angle
  si(k) = -pi/18+(k-1)*pi/9/kmax;
  Vload(k) = VloadA*cos(si(k))+VloadA*sin(si(k))*i;
  Iload(cnts,k) = VloadA/abs(Zload);
  Iload(cnts,k) = Iload(cnts,k)*(cos(si(k)-phi)+sin(si(k)-phi)*i);
  Iline(cnts,k) = Iload(cnts,k);
  Vline(k) = Zline*Iline(k);
  Sline(cnts,k) = Vline(k)*conj(Iline(cnts,k));
  Vc(cnts,k) = Vb(cnts) - Vline(k) - Vload(k);
  tau(cnts,k) = angle(Vc(cnts,k));
  theta(cnts,k) = tau(cnts,k)+si(k)-angle(Zload);
  Vcp(cnts,k) = abs(Vc(cnts,k))*cos(theta(cnts,k));
  Vcq(cnts,k) = abs(Vc(cnts,k))*sin(theta(cnts,k));
  Svo(cnts,k) = -Vc(cnts,k)*conj(Iline(k));
  end
  degrees = si/pi*180;

end

deg = degrees;
Svo = Svo/1e6;
Vc = Vc/1e3;

figure(1);
subplot(3,1,1);
plot(deg,real(Svo(1,:)),deg,real(Svo(2,:)),'--',deg,real(Svo(3,:)),'-.');
subplot(3,1,2);
```

```
plot(deg,imag(Svo(1,:)),deg,imag(Svo(2,:)),'--',deg,imag(Svo(3,:)),'-.');
subplot(3,1,3);
plot(deg,abs(Vc(1,:)),deg,abs(Vc(2,:)),'--',deg,abs(Vc(3,:)),'-.');
subplot(3,1,1);
  grid;
  ylabel('Pc [MW]');
  legend('sag = 0%','sag = 20%','sag = 40%',4);
subplot(3,1,2);
  grid;
  ylabel('Qc [MVAr]');
  legend('sag = 0%','sag = 20%','sag = 40%',4);
subplot(3,1,3);
  grid;
  ylabel('Vc [kV]');
  legend('sag = 0%','sag = 20%','sag = 40%',4);
  xlabel('Psi [deg]');

print('-f1','-deps2','/nfs/stak/u2/v/vanzyl/phd/pictures/vc.eps');
```

APPENDIX F MATLAB PROGRAM LISTING FOR ADAPTIVE PI CONTROLLER

```
%DC bus voltage regulator for drive
%with constant power load until current limit
%used to generate results for June 98 Maxwell progress report
%ASDsagridethrough.m   last modified 11/16/98

global Vdcref Kp Ki IactRmax Idcl Vll sag efficINV efficREC P

figure(1);clf;
figure(2);clf;
t0 = 0;
tf = 1;
x = 0;
efficINV = 0.95;
efficREC = 0.95;
effic = efficINV*efficREC;

 Pinvout = 100e3;
 P = Pinvout;
 sag = 40;

 vdc0 = 800;
 Vll = 480;
 IactR0 = P/effic/sqrt(3)/Vll;
 x0 = [vdc0 IactR0]';
 tspan = [t0 tf];
 [t,x] = ode45('ASDsagridethroughmodel',tspan,x0);

 figure(1);
  plot((x(:,1)),x(:,2));
  hold on;

 figure(2);
  subplot(2,1,1);
   plot(t,x(:,1));
   hold on;
  subplot(2,1,2);
   plot(t,x(:,2));
   hold on;

figure(1);
 grid;
 axis([650 850 100 250]);
 ylabel('Rectifier input current [A]');
 xlabel('DC bus voltage [V]');

figure(2);
 subplot(2,1,1);
  axis([t0 tf 650 850]);
  xlabel('Time [sec]');
  ylabel('DC bus voltage [V]');
  grid;
 subplot(2,1,2);
  axis([t0 tf 100 250]);
  xlabel('Time [sec]');
  ylabel('Rectifier input current [A]');
  grid;

print('-f2','-deps2','/nfs/stak/u2/v/vanzyl/phd/OSUThesis/pictures/ASDsaggslim.eps')
print('-f2','-dtiff','/nfs/stak/u2/v/vanzyl/phd/OSUThesis/pictures/ASDsaggslim.tif')
```

```
print('-f1','-deps2','/nfs/stak/u2/v/vanzyl/phd/OSUThesis/pictures/ASDsaggsptlim.eps')
print('-f1','-dtiff','/nfs/stak/u2/v/vanzyl/phd/OSUThesis/pictures/ASDsaggsptlim.tif')
```

```
%Contains diff. eqn. for dc bus regulator
%constant power load until current limit
%Gain scheduling controller
%used to generate results for June 98 Maxwell progress report
%modelASDsagridethrough.m    last modified 11/16/98

function xp = modelASDsagridethrough(t,x)

global Vdcref Kp Ki IactRmax Idcl Vll sag efficINV efficREC P

%System constants
 Cdc = 10e-3;
 IactRmax = 310/sqrt(2);
 effic = efficINV*efficREC;
%Sag
 if (t>0.1) & (t<5)
  Vll = (100-sag)/100*480;
 else
  Vll = 480;
 end
%Gain scheduling
 Vdcref = 800;
 err = Vdcref-x(1);
 if abs(err)>(0.05*Vdcref)
  Kp = 0.5+0.1*abs(0.05*Vdcref-abs(err));
  Ki = 2.5+0.1*abs(0.05*Vdcref-abs(err));
else
% if abs(err)<(0.025*Vdcref)
  Kp = 0.5;
  Ki = 2.5;
end
%System equations
 Idcl = P/efficINV/x(1);
 if abs(x(2))>IactRmax
  xp(1) = (efficREC*sqrt(3)*Vll*x(2)/x(1)-Idcl)/Cdc;
  if x(1)<795
   xp(2) = 0;
  else
   xtemp = -Kp*efficREC*sqrt(3)*Vll*x(2)/Cdc/x(1);
   xp(2) = xtemp+Kp*Idcl/Cdc+Ki*(Vdcref-x(1));
  end
 else
  xp(1) = (efficREC*sqrt(3)*Vll*x(2)/x(1)-Idcl)/Cdc;
  xtemp = -Kp*efficREC*sqrt(3)*Vll*x(2)/Cdc/x(1);
  xp(2) = xtemp+Kp*Idcl/Cdc+Ki*(Vdcref-x(1));
 end
xp = xp';
%end
```

APPENDIX G MATLAB PROGRAM LISTING FOR ASD WITH ENERGY STORAGE

```
% DC bus voltage regulator for drive
% with constant power load until current limit
% and ultracapacitor unit
% ASDwEnSt.m   last modified 11/17/98

global VdcrefREC VdcrefBst Kp Ki IactRmax Idcl Vllnom BoostOn
global sag efficREC efficINV efficBst P nser Boost alphap alphai

ASDwEnStInit;

figure(1);clf;
%figure(2);clf;

efficREC = 0.95;            %efficiency of rectifier
efficINV = 0.95;            %efficiency of inverter
effic = efficINV*efficREC;
efficBst = 0.9;                     %efficiency of boost converter

 P = Pinvout;

 vdc0 = VdcrefREC;
 Vllnom = 480;
 Vll = Vllnom;
 IactR0 = P/effic/sqrt(3)/Vll;
 vuc0 = nser*56;
 x0 = [vdc0 IactR0 0 vuc0]';
 tspan = [t0 tf];
 options = odeset('MaxStep',2e-3);
 [t,x] = ode45('ASDwEnStmodel',tspan,x0,options);

 Vdcmin = min(x(:,1))

%Powers
 for cnt = 1:size(t,1)
  if t(cnt)<0.1
   Vllvector(cnt) = Vllnom;
  else
   Vllvector(cnt) = Vllnom*(100-sag)/100;
  end
 end
 Precin = sqrt(3)*Vllvector'.*x(:,2);
 PEnSt = x(:,3).*x(:,4);

%Plots
% figure(2);
%  plot((x(:,1)),x(:,2));
%  hold on;

 figure(1);
  subplot(3,1,1);
   plot(t,x(:,1));
%   hold on;
  subplot(3,1,2);
   plot(t,x(:,2));
%   hold on;
  subplot(3,1,3);
   plot(t,x(:,3));
%   hold on;
%  subplot(4,1,4);
%   plot(t,Precin/1000);
```

```
%   plot(t,x(:,4));
%   hold on;
%   plot(t,PEnSt/1000);
%   plot(t,(PEnSt+Precin)/1000);
%   hold off;

%figure(2);
% grid;
% axis([320 400 0 25]);
% ylabel('Rectifier input current [A]');
% xlabel('DC bus voltage [V]');

figure(1);
 subplot(3,1,1);
  axis([t0 tf 650 800]);
%  xlabel('Time [sec]');
  ylabel('DC bus voltage[V]');
  grid;
 subplot(3,1,2);
  axis([t0 tf 50 250]);
%  xlabel('Time [sec]');
  ylabel('Rectifier current[A]');
  grid;
 subplot(3,1,3);
  axis([t0 tf 0 max(150,ceil(max(x(:,3))/100)*100)]);
  xlabel('Time [sec]');
  ylabel('Ultra-cap. current[A]');
  grid;
% subplot(4,1,4);
%  axis([t0 tf 460 510]);
%  xlabel('Time [sec]');
%  ylabel('REC&Bst power[kW]');
%  grid;

print('-f1','-deps2',filenameeps)
%print('-f1','-dtiff',filenametif)
```

```
%ASDwEnStInit.m
%Annabelle van Zyl Last modifier 11/17/98
%Contains intial values for ASDwEnSt.m and modelASDwEnSt.m

filenameeps='/nfs/stak/u2/v/vanzyl/phd/pictures/ASDwEnStC.eps'

sag = input('sag magnitude [%] :');
Pinvout = input('load power [kW] :');
Pinvout = Pinvout*1e3;
VdcrefBst = input('boost reference voltage [V] :');
BoostOn = input('BoostOn voltage [V] :');

nser = 9;
IactRmax = 198;%200;
VdcrefREC = 800;

alphap = 0.05;
alphai = 0.1;
t0 = 0;
tf = 1;

t = 0;
x = 0;
VIIvector = 0;
Boost = 0;
```

```
% Contains diff. eqn. for dc bus regulator
% constant power load until current limit
% ultra-cpacitor energy sotrage unit
% ASDwEnStmodel.m    last modified 11/17/98

function xp = modelASD(t,x)

global VdcrefREC VdcrefBst Kp Ki IactRmax Idcl VllnomBoostOn
global sag efficREC efficINV efficBst P nser Boost alphap alphai

%State variables
% x(1)  Vdc      dc bus voltage
% x(2)  Irec     rectifier input current
% x(3)  Iuc      ultra-capacitor current
% x(4)  Vuc      ultra-capacitor terminal voltage

%System constants
 C = 10e-3;
 Ce = 96/nser;
 Re = nser*0.022;
 effic = efficREC*efficINV;
%Sag
 if (t>0.1) & (t<10)
  Vll = (100-sag)/100*Vllnom;
 else
  Vll = Vllnom;
 end
%Rectifier PI controller
 errREC = VdcrefREC-x(1);
 if abs(errREC)>(0.05*VdcrefREC)
  Kp2 = 0.5+alphap*abs(0.05*VdcrefREC-abs(errREC));
  Ki2 = 2.5+alphai*abs(0.05*VdcrefREC-abs(errREC));
 else
  Kp2 = 0.5;
  Ki2 = 2.5;
 end
%Boost PI controller
 errBst = VdcrefBst-x(1);
% if abs(errBst)>(0.05*VdcrefBst)
  Kp3 = 10;
  Ki3 = 50;
% else
%  Kp3 = 5;
%  Ki3 = 25;
% end

%System equations
 if abs(x(2))>IactRmax
  xp(1) = (sqrt(3)*efficREC*Vll*x(2)+x(4)*efficBst*x(3)-P/efficINV)/C/x(1);
  if x(1) < 0.98*VdcrefREC
   xp(2) = 0;
  else
   xp(2) = Ki2*(VdcrefREC-x(1))-Kp2*xp(1);
  end
 else
  xp(1) = (sqrt(3)*efficREC*Vll*x(2)+x(4)*efficBst*x(3)-P/efficINV)/C/x(1);
  xp(2) = Ki2*(VdcrefREC-x(1))-Kp2*xp(1);
 end

 if Boost == 0
  xp(3) = 0;
  xp(4) = 0;
```

```
 if x(1) < BoostOn
  Boost = 1;
 end
else
 xp(3) = Ki3*(VdcrefBst-x(1))-Kp3*xp(1);
 xp(4) = -x(3)/Ce-Re*xp(3);
 if x(3)<0
  Boost = 0;
  xp(3) = 0;
  xp(4) = 0;
 end
end

xp = xp';
```

APPENDIX H MATLAB PROGRAM LISTING WITH RECOGNITION

```
% DC bus voltage regulator for drive
% with constant power load until current limit
% and ultracapacitor unit
% Measure Vll to see if REC can handle sag alone
% recognize.m   last modified 11/18/98

global VdcrefREC VdcrefBst Kp Ki IactRmax Idcl Vllnom BoostOn
global sag efficREC efficINV efficBst P nser Boost alphap alphai
global checked REConly tstart Vstart Istart

recognizeInit;

figure(1);clf;
efficREC = 0.95;            %efficiency of rectifier
efficINV = 0.95;            %efficiency of inverter
effic = efficINV*efficREC;
efficBst = 0.9;                     %efficiency of boost converter

 P = Pinvout;

 vdc0 = VdcrefREC;
 Vll = Vllnom;
 IactR0 = P/effic/sqrt(3)/Vll;
 vuc0 = nser*56;
 x0 = [vdc0 IactR0 0 vuc0]';
 tspan = [t0 tf];
 options = odeset('MaxStep',2e-3);
 [t,x] = ode45('recognizemodel',tspan,x0,options);

 Vdcmin = min(x(:,1))
 Bvector = ones(size(x,1),1)*BoostOn;
 Ireczero = x(10,2)
 Irecsag = x(size(x,1),2)

%Powers
 for cnt = 1:size(t,1)
  if t(cnt)<0.1
   Vllvector(cnt) = Vllnom;
  else
   Vllvector(cnt) = Vllnom*(100-sag)/100;
  end
 end
 Precin = sqrt(3)*Vllvector'.*x(:,2);
 PEnSt = x(:,3).*x(:,4);

%Plots

 figure(1);
  subplot(3,1,1);
  plot(t,x(:,1),t,Bvector,'--');
  legend('Vdc','Vdc,thr',0);
  axis([t0 tf 650 800]);
  ylabel('DC bus voltage[V]');
  grid;

  subplot(3,1,2);
  plot(t,x(:,2));
  axis([t0 tf 50 250]);
  ylabel('Rectifier current[A]');
  grid;
```

```
subplot(3,1,3);
plot(t,x(:,3));
axis([t0 tf 0 max(150,ceil(max(x(:,3))/100)*100)]);
xlabel('Time [sec]');
ylabel('Ultra-cap. current[A]');
grid;


print('-f1','-deps2',filenameps)
```

```
%recognizeInit.m
%Annabelle van Zyl Last modified 11/18/98
%Contains intial values for recognize.m and modelrecognize.m

filenameps='/nfs/stak/u2/v/vanzyl/phd/pictures/recognizeF.eps'

sag = input('sag magnitude [%] : ');
Pinvout = input('load power [kW] : ')*1e3;

nser = 9;
IactRmax = 200;
VdcrefREC = 800;
VdcrefBst = 760;
BoostOn = 700;
alphap = 0.05;
alphai = 0.1;
t0 = 0;
tf = 1;

t = 0;
x = 0;
VlInom = 480;
VlIvector = 0;
Boost = 0;
checked = 0;
```

```
% Contains diff. eqn. for dc bus regulator (recognize.m)
% constant power load until current limit
% ultra-cpacitor energy sotrage unit
% Measure Vll to see if REC can handle sag alone
% recognizemodel.m   last modified 11/18/98

function xp = modelASD(t,x)

global VdcrefREC VdcrefBst Kp Ki IactRmax Idcl Vllnom BoostOn
global sag efficREC efficINV efficBst P nser Boost alphap alphai
global checked REConly tstart Vstart Istart

%State variables
% x(1)  Vdc      dc bus voltage
% x(2)  Irec     rectifier input current
% x(3)  Iuc      ultra-capacitor current
% x(4)  Vuc      ultra-capacitor terminal voltage

%System constants
 C = 10e-3;
 Ce = 96/nser;
 Re = nser*0.022;
 effic = efficREC*efficINV;
%Sag
 if (t>0.101) & (t<10)
  Vll = (100-sag)/100*Vllnom;
 else
  Vll = Vllnom;
 end
%Rectifier PI controller
 errREC = VdcrefREC-x(1);
 if abs(errREC)>(0.05*VdcrefREC)
  Kp2 = 0.5+alphap*abs(0.05*VdcrefREC-abs(errREC));
  Ki2 = 2.5+alphai*abs(0.05*VdcrefREC-abs(errREC));
 else
  Kp2 = 0.5;
  Ki2 = 2.5;
 end
%Boost PI controller
 errBst = VdcrefBst-x(1);
% if abs(errBst)>(0.05*VdcrefBst)
  Kp3 = 10;
  Ki3 = 50;
% else
%  Kp3 = 5;
%  Ki3 = 25;
% end

%System equations
 if abs(x(2))>IactRmax
  xp(1) = (sqrt(3)*efficREC*Vll*x(2)+x(4)*efficBst*x(3)-P/efficINV)/C/x(1);
  if x(1) < 0.98*VdcrefREC
   xp(2) = 0;
  else
   xp(2) = Ki2*(VdcrefREC-x(1))-Kp2*xp(1);
  end
 else
  xp(1) = (sqrt(3)*efficREC*Vll*x(2)+x(4)*efficBst*x(3)-P/efficINV)/C/x(1);
  xp(2) = Ki2*(VdcrefREC-x(1))-Kp2*xp(1);
 end

%Energy storage equations and controller
```

```
if Boost == 0

 xp(3) = 0;
 xp(4) = 0;
 if abs(errREC) < 0.02*VdcrefREC
  tstart = t;
  Vstart = x(1);
 else
  if ((t-tstart) > 0.001) & (checked == 0)
   checked = 1;
   ts = tstart;
   Vs = Vstart;
   te = t;
   Ve = x(1);
   Irec0 = 1/(te-ts)*C/2/sqrt(3)/efficREC*(Vs^2-Ve^2)/(VlInom-Vll)
   Irecsag = Irec0/(1-sag/100)
   if (Irecsag)<IactRmax
    BoostOn = 700;
   else
    BoostOn = 760;
   end
  end
 end
 if x(1) < BoostOn
  Boost = 1;
 end

else

  xp(3) = Ki3*(VdcrefBst-x(1))-Kp3*xp(1);
  xp(4) = -x(3)/Ce-Re*xp(3);
  if x(3)<0
   Boost = 0;
   xp(3) = 0;
   xp(4) = 0;
  end

end

xp = xp';
```

APPENDIX I MATLAB PROGRAM LISTING WITH FUZZY CONTROLLER

```
% DC bus voltage regulator for drive
% with constant power load until current limit
% and ultracapacitor unit
% Measure Vll to see if REC can handle sag alone
% Fuzzy controller to decide when to engage energy storage
% fuzzy controller has two inputs, R and S
% ASDfuzzyRS.m   last modified 11/18/98

global VdcrefREC VdcrefBst Kp Ki IactRmax Idcl Vllnom BoostOn
global sag efficREC efficINV efficBst P nser Boost alphap alphai
global checked REConly tstart Vstart Istart
global Renst1 Renst0 Rrec1 Rrec0 Bmin Bmax Bl0 Bh0 Bh1 Bl1
global Ss1 Ss0 Sl0 Sl1 Smin Smax Rmin Rmax

ASDfuzzyInitRS;

figure(1);clf;
%figure(4);clf;
efficREC = 0.95;            %efficiency of rectifier
efficINV = 0.95;            %efficiency of inverter
effic = efficINV*efficREC;
efficBst = 0.9;                     %efficiency of boost converter

 P = Pinvout;

Ireczero = Pinvout/efficINV/efficREC/sqrt(3)/Vllnom;
Irecdel = Ireczero*100/(100-sag)-Ireczero;

 vdc0 = VdcrefREC;
 Vll = Vllnom;
 IactR0 = P/effic/sqrt(3)/Vll;
 vuc0 = nser*56;
 x0 = [vdc0 IactR0 0 vuc0]';
 tspan = [t0 tf];
 options = odeset('MaxStep',2e-3);
 [t,x] = ode45('ASDfuzzymodelRS',tspan,x0,options);

 Vdcmin = min(x(:,1))
 Bvector = ones(size(x,1),1)*BoostOn;

%Powers
 for cnt = 1:size(t,1)
  if t(cnt)<0.1
   Vllvector(cnt) = Vllnom;
  else
   Vllvector(cnt) = Vllnom*(100-sag)/100;
  end
 end
 Precin = sqrt(3)*Vllvector'.*x(:,2);
 PEnSt = x(:,3).*x(:,4);

%Plots

 figure(1);
 subplot(3,1,1);
   plot(t,x(:,1),t,Bvector,'--');
   legend('Vdc','Vdc,thr',4);
   axis([t0 tf 650 800]);
   ylabel('DC bus voltage[V]');
   grid;
```

```
subplot(3,1,2);
  plot(t,x(:,2));
  axis([t0 tf 50 250]);
  ylabel('Rectifier current[A]');
  grid;

subplot(3,1,3);
  plot(t,x(:,3));
 maxIbst = max(150,ceil(max(x(:,3))/50)*50);
 axis([t0 tf 0 maxIbst]);
 xlabel('Time [sec]');
 ylabel('Ultra-cap. current[A]');
 grid;


print('-f1','-deps2',filenamep)
```

```
%ASDfuzzyInitRS.m
%Annabelle van Zyl Last modified 7/22/98
%Contains intial values for ASDfuzzyRS.m and ASDfuzzymodelRS.m

filenamep = '/nfs/stak/u2/v/vanzyl/phd/pictures/ASDRSf.eps'

sag = input('sag [%] = ');
Pinvout = input('Pinvout [kW] = ');
Pinvout = Pinvout*1e3;

efficREC = 0.95;              %efficiency of rectifier
efficINV = 0.95;              %efficiency of inverter
effic = efficINV*efficREC;
efficBst = 0.9;               %efficiency of boost converter
nser = 9;
IactRmax = 199;%200;
VdcrefREC = 800;
VdcrefBst = 760;
BoostOn = 710;
alphap = 0.05;
alphai = 0.1;
t0 = 0;
tf = 1;

fuzzyRSInitD;
R = 0;
S = 0;

t = 0;
x = 0;
VllnomRS = 480;
VllvectorRS = 0;
Boost = 0;
checked = 0;
```

```
%fuzzyRSInitD.m
%Annabelle van Zyl Last modified 11/18/98
%Initial values for fuzzyRS.m

%This version is inbetween

R = 0.6:0.01:1;
Renst1 = 0.95;
Renst0 = 0.8;
Rrec1 = 0.75;
Rrec0 = 0.9;
Rmin = 0.2;
Rmax = 1;

S = 0.5:0.01:1;
Ss1 = 0.5;
Ss0 = 0.85;%0.9;
Sl1 = 0.85;%0.9;
Sl0 = 0.6;
Smin = 0.01;
Smax = 1;

Vdcref = 800;

Bmin = 0.8375*Vdcref;
Bmax = 1*Vdcref;
Bl0 = 0.95*Vdcref;
Bh0 = 0.875*Vdcref;
Bh1 = 0.95*Vdcref;
Bl1 = 0.875*Vdcref;
Blower = 0;
Bupper = 1;

filembp = '/nfs/stak/u2/v/vanzyl/phd/pictures/RSDmemb.eps';
filesurfp = '/nfs/stak/u2/v/vanzyl/phd/pictures/RSDsurf.eps';
fileplotp = '/nfs/stak/u2/v/vanzyl/phd/pictures/RSDplot.eps';
```

```
% Contains diff. eqn. for dc bus regulator ASDfuzzyRS.m
% constant power load until current limit
% ultra-capacitor energy sotrage unit
% Measure Vll to see if REC can handle sag alone
% Fuzzy controller for BoostOn - extended to consider Irec0
% ASDfuzzymodelRS.m   last modified11/18/98

function xp = ASDfuzzymodelRS(t,x)

global VdcrefREC VdcrefBst Kp Ki IactRmax Idcl Vllnom BoostOn
global sag efficREC efficINV efficBst P nser Boost alphap alphai
global checked REConly tstart Vstart Istart
global Renst1 Renst0 Rrec1 Rrec0 Bmin Bmax Bl0 Bh0 Bh1 Bl1
global Ss1 Ss0 Sl0 Sl1 Smin Smax Rmin Rmax R S

%State variables
% x(1)  Vdc      dc bus voltage
% x(2)  Irec     rectifier input current
% x(3)  Iuc      ultra-capacitor current
% x(4)  Vuc      ultra-capacitor terminal voltage

%System constants
 C = 10e-3;
 Ce = 96/nser;
 Re = nser*0.022;
 effic = efficREC*efficINV;
%Sag
 if (t>0.101) & (t<10)
  Vll = (100-sag)/100*Vllnom;
 else
  Vll = Vllnom;
 end
%Rectifier PI controller
 errREC = VdcrefREC-x(1);
 if abs(errREC)>(0.05*VdcrefREC)
  Kp2 = 0.5+alphap*abs(0.05*VdcrefREC-abs(errREC));
  Ki2 = 2.5+alphai*abs(0.05*VdcrefREC-abs(errREC));
 else
  Kp2 = 0.5;
  Ki2 = 2.5;
 end
%Boost PI controller
 errBst = VdcrefBst-x(1);
 if abs(errBst)>(0.05*VdcrefBst)
  Kp3 = 10;
  Ki3 = 50;
 else
  Kp3 = 5;
  Ki3 = 25;
 end

%System equations
 if abs(x(2))>IactRmax
  xp(1) = (sqrt(3)*efficREC*Vll*x(2)+x(4)*efficBst*x(3)-P/efficINV)/C/x(1);
  if x(1) < 0.98*VdcrefREC
   xp(2) = 0;
  else
   xp(2) = Ki2*(VdcrefREC-x(1))-Kp2*xp(1);
  end
 else
  xp(1) = (sqrt(3)*efficREC*Vll*x(2)+x(4)*efficBst*x(3)-P/efficINV)/C/x(1);
  xp(2) = Ki2*(VdcrefREC-x(1))-Kp2*xp(1);
```

```
end

%Energy storage equations and controller
if Boost == 0

 xp(3) = 0;
 xp(4) = 0;
 if abs(errREC) < 0.02*VdcrefREC
  tstart = t;
  Vstart = x(1);
 else
  if ((t-tstart) > 0.001) & (checked == 0)
   checked = 1;
   ts = tstart;
   Vs = Vstart;
   te = t;
   Ve = x(1);
   delPrecout = -1/(t-tstart)/2*C*(x(1)^2-Vstart^2);
   delPrecin = delPrecout/efficREC;
   delIrec = delPrecin/sqrt(3)/Vll;
   Irec0 = delIrec*Vll/(Vllnom-Vll);
   Irecsag = delIrec+Irec0;
   %Fuzzy controller
   S = Irec0/IactRmax
   %Input S fuzzify
   %small
   if S>Ss0
    small = Smin;
   elseif S<Ss1
    small = Smax;
   else
    small = Smin+(Smax-Smin)*(S-Ss0)/(Ss1-Ss0);
   end
   %large
   if S<Sl0
    large = Smin;
   elseif S>Sl1
    large = Smax;
   else
    large = Smin+(Smax-Smin)*(S-Sl0)/(Sl1-Sl0);
   end
   R = Irecsag/IactRmax
   %Input R fuzzify
   %rec
   if R>Rrec0
    rec = Rmin;
   elseif R<Rrec1
    rec = Rmax;
   else
    rec = Rmin+(Rmax-Rmin)*(R-Rrec0)/(Rrec1-Rrec0);
   end
   %enst
   if R<Renst0
    enst = Rmin;
   elseif R>Renst1
    enst = Rmax;
   else
    enst = Rmin+(Rmax-Rmin)*(R-Renst0)/(Renst1-Renst0);
   end

   %Defuzzify BoostOn
   %high
```

```
  Bh = Bh0+(Bh1-Bh0)*enst*large;
  Bcghtri = 2*Bh/3+Bh0/3;
  Bcghblock = (Bh+Bmax)/2;
  Bcgh = ((Bmax-Bh)*Bcghblock+(Bh-Bh0)/2*Bcghtri)/(Bmax-Bh/2-Bh0/2);

  %low
  Bl = Bl0+(Bl1-Bl0)*rec*small;
  Bcgltri = 2*Bl/3+Bl0/3;
  Bcglblock = (Bl+Bmin)/2;
  Bcgl = ((Bmin-Bl)*Bcglblock+(Bl-Bl0)/2*Bcgltri)/(Bmin-Bl/2-Bl0/2);

  %BoostOn
  Alow = rec*small*(Bl1/2-Bmin+Bl0/2);
  Ahigh = enst*large*(Bmax-Bh0/2-Bh1/2);
  Bcg = (Bcgl*Alow+Bcgh*Ahigh)/(Alow+Ahigh);
  BoostOn = Bcg
 end
end
if x(1) < BoostOn
 Boost = 1;
end

else

 xp(3) = Ki3*(VdcrefBst-x(1))-Kp3*xp(1);
 xp(4) = -x(3)/Ce-Re*xp(3);
 if x(3)<0
  Boost = 0;
  xp(3) = 0;
  xp(4) = 0;
 end

end

xp = xp';
```

APPENDIX J MATLAB PROGRAM LISTING FOR OFF-LINE EVALUATION

```
%Annabelle van Zyl
%Last modified 11/18/98
%Program using experimental results from SPOT to
%test fuzzy controller
%spotnew.m
%Uses three phase voltage measurements from SPOT

spotnewInit;

t = 0:sampleT:sampleT*(size(va,1)-1); t = t';

%First order butterworth filter for vdc measurement
samplerate = 1/sampleT;
Wnvdc = cutoffvdc/(samplerate/2);
[bf,af] = butter(1,Wnvdc);
%Butterworth filter for irec and isag
Wnvph = cutoffvph/(samplerate/2);
[bph,aph] = butter(1,Wnvph);
%Butterworth filter for irec and isag
Wnirec = cutoffirec/(samplerate/2);
[Bf,Af] = butter(1,Wnirec);
%[Bf,Af] = butter(2,Wnirec);          %second order

%vdc
vdcfilt(1) = vdc(1);
for count = 2:size(t,1)
 vdcfilt(count) = -af(2)/af(1)*vdcfilt(count-1);
 vdcfilt(count) = vdcfilt(count)+bf(1)/af(1)*vdc(count);
 vdcfilt(count) = vdcfilt(count)+bf(2)/af(1)*vdc(count-1);
end

Vdcmin = min(vdcfilt)

%irec
irecfilt(1) = irec(1);
%irecfilt(2) = irec(2);
for count = 2:size(t,1)
 irecfilt(count) = -Af(2)/Af(1)*irecfilt(count-1);
% irecfilt(count) = irecfilt(count)-Af(3)/Af(1)*irecfilt(count-2);
 irecfilt(count) = irecfilt(count)+Bf(1)/Af(1)*irec(count);
 irecfilt(count) = irecfilt(count)+Bf(2)/Af(1)*irec(count-1);
% irecfilt(count) = irecfilt(count)+Bf(3)/Af(1)*irec(count-2);
end
irecoffset = mean(irecfilt(zoom1:zoom1+2*sampleN));
irecfilt = irecfilt-irecoffset*ones(1,size(irecfilt,2));

%va,b,c
vafilt(1) = va(1); %vafilt(2) = va(2);
vbfilt(1) = vb(1); %vbfilt(2) = vb(2);
vcfilt(1) = vc(1); %vcfilt(2) = vc(2);
for count = 2:size(t,1)
 vafilt(count) = -aph(2)/aph(1)*vafilt(count-1);
% vafilt(count) = vafilt(count)-aph(3)/aph(1)*vafilt(count-2);
 vafilt(count) = vafilt(count)+bph(1)/aph(1)*va(count);
 vafilt(count) = vafilt(count)+bph(2)/aph(1)*va(count-1);
% vafilt(count) = vafilt(count)+bph(3)/aph(1)*va(count-2);
 vbfilt(count) = -aph(2)/aph(1)*vbfilt(count-1);
% vbfilt(count) = vbfilt(count)-aph(3)/aph(1)*vbfilt(count-2);
 vbfilt(count) = vbfilt(count)+bph(1)/aph(1)*vb(count);
 vbfilt(count) = vbfilt(count)+bph(2)/aph(1)*vb(count-1);
```

```
% vbfilt(count) = vbfilt(count)+bph(3)/aph(1)*vb(count-2);
 vcfilt(count) = -aph(2)/aph(1)*vcfilt(count-1);
% vcfilt(count) = vcfilt(count)-aph(3)/aph(1)*vcfilt(count-2);
 vcfilt(count) = vcfilt(count)+bph(1)/aph(1)*vc(count);
 vcfilt(count) = vcfilt(count)+bph(2)/aph(1)*vc(count-1);
% vcfilt(count) = vcfilt(count)+bph(3)/aph(1)*vc(count-2);
end
vaoffset = mean(vafilt(zoom1:zoom1+2*sampleN));
vafilt = vafilt-vaoffset*ones(1,size(vafilt,2));
vboffset = mean(vbfilt(zoom1:zoom1+2*sampleN));
vbfilt = vbfilt-vboffset*ones(1,size(vbfilt,2));
vcoffset = mean(vcfilt(zoom1:zoom1+2*sampleN));
vcfilt = vcfilt-vcoffset*ones(1,size(vcfilt,2));

%isag
if havelsag == 'y'
 isagfilt(1) = isag(1); isagfilt(2) = isag(2);
 for count = 3:size(t,1)
  isagfilt(count) = -Af(2)/Af(1)*isagfilt(count-1);
%  isagfilt(count) = isagfilt(count)-Af(3)/Af(1)*isagfilt(count-2);
  isagfilt(count) = isagfilt(count)+Bf(1)/Af(1)*isag(count);
  isagfilt(count) = isagfilt(count)+Bf(2)/Af(1)*isag(count-1);
%  isagfilt(count) = isagfilt(count)+Bf(3)/Af(1)*isag(count-2);
end
isagoffset = mean(isagfilt(zoom1:zoom1+2*sampleN));
isagfilt = isagfilt-isagoffset*ones(1,size(isagfilt,2));
end


%rms calculations for va,b,c and irecfilt
for count = 1:rmssamplevph
 vafilt(count) = 0;
 vbfilt(count) = 0;
 vcfilt(count) = 0;
end
for count = 1:rmssampleirec
 irecfilt(count) = 0;
 isagfilt(count) = 0;
end
vasq = vafilt.*vafilt;
vbsq = vbfilt.*vbfilt;
vcsq = vcfilt.*vcfilt;
irecfiltsq = irecfilt.*irecfilt;
if havelsag == 'y'
 isagfiltsq = isagfilt.*isagfilt;
end

Ruu = zeros(size(t,1),5);
for count = rmssamplevph+1:1:size(t,1)
  temp = 1/rmssamplevph*(vasq(count-rmssamplevph)-vasq(count));
 Ruu(count,1) = Ruu(count-1,1) - temp;
  temp = 1/rmssamplevph*(vbsq(count-rmssamplevph)-vbsq(count));
 Ruu(count,2) = Ruu(count-1,2) - temp;
  temp = 1/rmssamplevph*(vcsq(count-rmssamplevph)-vcsq(count));
 Ruu(count,3) = Ruu(count-1,3) - temp;
end
for count = rmssampleirec+1:1:size(t,1)
  temp = irecfiltsq(count-rmssampleirec)-irecfiltsq(count);
  temp = 1/rmssampleirec*temp;
 Ruu(count,4) = Ruu(count-1,4) - temp;
 if havelsag == 'y'
   temp = isagfiltsq(count-rmssampleirec)-isagfiltsq(count);
```

```
  temp = 1/rmssampleirec*temp;
  Ruu(count,5) = Ruu(count-1,5) - temp;
 end
end

varms = sqrt(Ruu(:,1));
vbrms = sqrt(Ruu(:,2));
vcrms = sqrt(Ruu(:,3));
irecfiltrms = sqrt(Ruu(:,4));
 varmspresag = mean(varms(4*sampleN:7*sampleN));
 vbrmspresag = mean(vbrms(4*sampleN:7*sampleN));
 vcrmspresag = mean(vcrms(4*sampleN:7*sampleN));
vrmspresag = [varmspresag vbrmspresag vcrmspresag];
vrmspresagprint = [vrmspresag mean(vrmspresag)];
 varmssag = mean(varms(zoomh:zoomh+2*sampleN));
 vbrmssag = mean(vbrms(zoomh:zoomh+2*sampleN));
 vcrmssag = mean(vcrms(zoomh:zoomh+2*sampleN));
vrmssag = [varmssag vbrmssag vcrmssag];
vrmssagprint = [vrmssag mean(vrmssag)];
irecfiltrmspresag = mean(irecfiltrms(4*sampleN:7*sampleN));

if havelsag == 'y'
 isagfiltrms = sqrt(Ruu(:,5));
 isagfiltrmssag = mean(isagfiltrms);
end



%Global controller

for cnt = 1:size(t,1)
 if checkedIrec0 == 0;
  if (vdcfilt(cnt) < Vdccrit)
   vaintegral = rmssamplevph*sampleT*(varmspresag-varms(cnt));
   vbintegral = rmssamplevph*sampleT*(vbrmspresag-vbrms(cnt));
   vcintegral = rmssamplevph*sampleT*(vcrmspresag-vcrms(cnt));
   Vs = vdcfilt(cnt-rmssamplevph);
   Ve = vdcfilt(cnt);
   te = t(cnt);
   vintsum = vaintegral+vbintegral+vcintegral;
   Irec0 = -C/2*(Ve^2-Vs^2)/efficREC0/vintsum
   checkedIrec0 = 1;
   vrmsmin = Vphnom;      %to force first calculation of BoostOn
   Irecestimate = Irec0*ones(cnt,1);
   Irecsag = Irec0;            %to avoid a zero in Irecestimate
  end
 elseif (varms(cnt)<varms(cnt-1))|(vbrms(cnt)<vbrms(cnt-1))|(vcrms(cnt)<vcrms(cnt-1))
  vrmsmin = sum([varms(cnt) vbrms(cnt) vcrms(cnt)]);
  Irecsag = sum(vrmspresag)/vrmsmin*Irec0;
  Irecsag = Irecsag*1.0;    %fudge factor 0.93

  %Fuzzy controller

  %Input S fuzzify
  S = Irec0/IactRmax;
  %small
  if S>Ss0
   small = Smin;
  elseif S<Ss1
   small = Smax;
  else
   small = Smin+(Smax-Smin)*(S-Ss0)/(Ss1-Ss0);
```

```
    end
    %large
    if S<Sl0
     large = Smin;
    elseif S>Sl1
     large = Smax;
    else
     large = Smin+(Smax-Smin)*(S-Sl0)/(Sl1-Sl0);
    end

    %Input R fuzzify
    R = Irecsag/IactRmax;
    %rec
    if R>Rrec0
     rec = Rmin;
    elseif R<Rrec1
     rec = Rmax;
    else
     rec = Rmin+(Rmax-Rmin)*(R-Rrec0)/(Rrec1-Rrec0);
    end
    %enst
    if R<Renst0
     enst = Rmin;
    elseif R>Renst1
     enst = Rmax;
    else
     enst = Rmin+(Rmax-Rmin)*(R-Renst0)/(Renst1-Renst0);
    end

    %Defuzzify BoostOn
    %high
    Bh = Bh0+(Bh1-Bh0)*enst*large;
    Bcghtri = 2*Bh/3+Bh0/3;
    Bcghblock = (Bh+Bmax)/2;
    Bcgh = ((Bmax-Bh)*Bcghblock+(Bh-Bh0)/2*Bcghtri)/(Bmax-Bh/2-Bh0/2);

    %low
    Bl = Bl0+(Bl1-Bl0)*rec*small;
    Bcgltri = 2*Bl/3+Bl0/3;
    Bcglblock = (Bl+Bmin)/2;
    Bcgl = ((Bmin-Bl)*Bcglblock+(Bl-Bl0)/2*Bcgltri)/(Bmin-Bl/2-Bl0/2);

    %BoostOn
    Alow = rec*small*(Bl1/2-Bmin+Bl0/2);
    Ahigh = enst*large*(Bmax-Bh0/2-Bh1/2);
    Bcg = (Bcgl*Alow+Bcgh*Ahigh)/(Alow+Ahigh);
    BoostOn = Bcg;
  end
 Irecestimate(cnt) = Irecsag;
 BoostOnVector(cnt) = BoostOn;
 end
 Irecsagfinal = Irecestimate(size(Irecestimate,1))
 BoostOnfinal = BoostOn(size(BoostOnVector,1))

 figure(1);
 clf;

 tzoom = t(zooml:zoomh);
 vafiltzoom = vafilt(zooml:zoomh);
 vbfiltzoom = vbfilt(zooml:zoomh);
 vcfiltzoom = vcfilt(zooml:zoomh);
 varmszoom = varms(zooml:zoomh);
```

```
vbrmszoom = vbrms(zooml:zoomh);
vcrmszoom = vcrms(zooml:zoomh);
vdczoom = vdc(zooml:zoomh);
vdcfiltzoom = vdcfilt(zooml:zoomh);
ireczoom = irec(zooml:zoomh);
irecfiltzoom = irecfilt(zooml:zoomh);
irecfiltrmszoom = irecfiltrms(zooml:zoomh);
Irecestimatezoom = Irecestimate(zooml:zoomh);
BoostOnVectorzoom = BoostOnVector(zooml:zoomh);
if havelsag == 'y'
 isagfiltrmszoom = isagfiltrms(zooml:zoomh);
end

tlaxis = zooml/1e4;
thaxis = zoomh/1e4;

subplot(3,1,1);
 plot(tzoom,varmszoom,tzoom,vbrmszoom,'--',tzoom,vcrmszoom,'-.');
 grid; axis([tlaxis thaxis 60 140]);
 legend('Va,rms','Vb,rms','Vc,rms',0);
 ylabel('Vph,rms [V]');
subplot(3,1,2);
 plot(tzoom,vdcfiltzoom,tzoom,BoostOnVectorzoom,'--');
 grid; axis([tlaxis thaxis 320 400]),
 legend('Vdc','Vdc,thr',0);
 ylabel('Vdc & Vdc,thr [V]');
subplot(3,1,3);
 plot(tzoom,irecfiltrmszoom,tzoom,Irecestimatezoom,'--');
 grid; axis([tlaxis thaxis 0 10]);
 hold off;
 xlabel('Time [sec]');
 legend('Irec','Irec,estimate',0);
 ylabel('Irec [A]');

print('-f1','-deps2',filenamep)
```

```
%Annabelle van Zyl
%Last modified 11/18/98
%spotnewInit.m
%Initialization for spotnew.m

clear;

filenamep = '/nfs/stak/u2/v/vanzyl/phd/pictures/spot22n.eps'
                        vafile=fopen('VA22.TXT','r');
                        vbfile=fopen('VB22.TXT','r');
                        vcfile=fopen('VC22.TXT','r');
                      vdcfile=fopen('VDCX22.TXT','r');
                     irecfile=fopen('IREC22.TXT','r');

havelsag = input('ISAG data available? (y/n) ','s');
if havelsag == 'y'
                     isagfile=fopen('ISAG7.TXT','r');
 isag = fscanf(isagfile,'%f');
 isag = isag/0.01*5;
end

va = fscanf(vafile,'%f'); va = 192/1.6*va;
vb = fscanf(vbfile,'%f'); vb = 192/1.6*vb;
vc = fscanf(vcfile,'%f'); vc = 192/1.6*vc;
vdc = fscanf(vdcfile,'%f');
irec = fscanf(irecfile,'%f');
irec = irec/0.01*5;

fclose(vafile);
fclose(vbfile);
fclose(vcfile);
fclose(vdcfile);
fclose(irecfile);
if havelsag == 'y'
 fclose(isagfile);
end

fundf = 60;    %Hz
fundT = 1/fundf;
T = fundT;
sampleT = 100e-6;
sampleN = round(T/sampleT);
rmssampleirec = round(1.0*sampleN);    %*T
rmssamplevph = round(1.5*sampleN);     %*T
cutoffvdc = 100;   %Hz
cutoffvph = 100;   %Hz
cutoffirec = 1e3;  %Hz
zooml = 1400;
zoomh = 3400;

Vphnom = 134.5; %in Rm 6, rms
VdcrefREC = 380;
Vdccrit = 0.945*VdcrefREC; %0.945 for original results
C = 1240e-6;
efficREC0 = 1;
efficREC1 = 1;
IactRmax = 8;


Boost = 0;
BoostOn = 0.875*VdcrefREC;
cnt = 0;
```

```
checkedIrec0 = 0;
Irec0 = 0;
Irecsag = 0;
tstart = 0;
vaintegral = 0;
vbintegral = 0;
vcintegral = 0;
vrmsmin = Vphnom;

%Fuzzy controller parameters
fuzzyRSInitspot;
```

```
%fuzzyRSInitspot.m
%Annabelle van Zyl Last modified 8/17/98
%Initial values for spot.m, included in spotInit.m

%This version is inbetween

Renst1 = 0.95;
Renst0 = 0.8;
Rrec1 = 0.75;
Rrec0 = 0.9;
Rmin = 0.2;
Rmax = 1;
R = Rrec1-0.05:0.01:Renst1+0.05;

Ss1 = 0.5;
Ss0 = 0.85;%0.9;
Sl1 = 0.85;%0.9;
Sl0 = 0.6;
Smin = 0.01;
Smax = 1;
S = Ss1-0.05:0.01:Sl1+0.05;

Vdcref = 380;

Bmin = 0.8375*Vdcref;
Bmax = 1*Vdcref;
Bl0 = 0.95*Vdcref;
Bh0 = 0.875*Vdcref;
Bh1 = 0.95*Vdcref;
Bl1 = 0.875*Vdcref;
Blower = 0;
Bupper = 1;

filememb = '/nfs/stak/u2/v/vanzyl/phd/OSUThesis/fuzzyRSspotmemb.ps';
filesurf = '/nfs/stak/u2/v/vanzyl/phd/OSUThesis/fuzzyRSspotsurf.ps';
fileplot = '/nfs/stak/u2/v/vanzyl/phd/OSUThesis/fuzzyRSspotplot.ps';
```

APPENDIX K RESULTS OF OFF-LINE EVALUATION OF ENERGY STORAGE SYSTEM CONTROLLER

Table 7 contains a detailed account of the results of the off-line experimental verification of the enhanced energy storage system controller presented in Chapter 5 and the column entries are explained in Table 6. Data was collected of the response of the 3kVA laboratory prototype of an ASD with an active rectifier to a variety of sags of different magnitudes at different load conditions of the ASD. All the generated sags were balanced three phase sags.

Measured quantities refer to data collected with an oscilloscope, unless noted otherwise, and calculated and estiamted quantities refer to values generated in *MATLAB* using the experimental data.

These results were used to evaluate the performance of the enhanced ultra-capacitor system controller by rating the calculated threshold voltage $V_{dc,thr}$ as *good* or *poor*. In one case an undervoltage trip of the inverter was experienced.

Table 6 Explanation of column entries

Column entry	Units	Explanation
case #		Case number, identifier
Iinv*	A	Rms current reference for inverter, this reflects the load condition of the ASD
sag	%	Calculated sag magnitude, % of nominal rectifier input voltage
TX setting	%	Transformer setting, % reading from panel
finv*	Hz	Frequency reference for inverter
Vdc,min	V	Minimum measured dc bus voltage during sag. Labeled N/A if ASD tripped.
Vdc,sag	V	Measured (multimeter) dc bus voltage during sag. The rectifier input current and dc bus voltage were measured on one run and the three rectifier input phase voltages and dc bus voltage on a different run. Where the two runs had different dc bus voltages, two values are given. Labeled N/A if ASD tripped.
Vph,nom	V	Calculated rms rectifier input voltage before onset of sag, average of the three phases
Vph,sag	V	Calculated rectifier input voltage during sag, average of the three phases
Irec0	A	case # 1 –39: Calculated rms rectifier input current before onset of sag case # 40 : Rms reference current specified by the rectifier controller
Irec,sag	A	Rms rectifier input current during sag. Where available: case # 1 – 13 : Measured case # 14 – 40: Calculated Information not available when ASD trips due to sag
Prec0	kW	Calculated rectifier input power before onset of sag = 3×Vph0×Irec0
Prec,sag	kW	Calculated rectifier input power during sag = 3×Vph,sag×Irec,sag
Irec0	A	Estimated rectifier input current before onset of sag
Irec,sag	A	Estimated rectifier input current during sag
ε (Irec0)	%	Estimation error for Irec0 as % of measured Irec0
ε (Irec,sag)	%	Estimation error for Irec,sag as % of measured Irec,sag
Vdc,thr	V	Calculated threshold dc bus voltage
Result		Rating of calculated Vdc,thr on a scale of 1 (good) through 5 (poor) UVT = undervoltage trip

Table 7 Results of off-line experimental verification of energy storage system controller

case #	Iinv*	sag	TX setting	finv*	Vdc,min	Vdc,sag	Vph,nom	Vph,sag	Irec0	Irec,sag	Prec	Prec,sag	Irec0	Irec,sag	ε (Irec0)	ε (Irecsag)	Vdc,thr	Result
	Arms	%	%	Hz	V	V	V	V	A	A	kW	kW	A	A	%	%	V	
36	5.5	56.19	40	6	351.2	380	136.5	59.8	1.67	3.11	0.684	0.558	1.42	3.13	-14.97	0.64	333.7	1
1	6	26.86	63	60.6	362.0	380	137.0	100.2	2.15	2.85	0.884	0.857					332.5	1
14	6	25.13	63	6	361.2	380	134.9	101.0	1.93	2.56	0.781	0.776					332.5	1
35	6	42.97	50	6	359.3	380	137.3	78.3	2.05	3.05	0.844	0.716					332.5	1
2	6	45.71	48	60.6	353.6	380	136.5	74.1	2.11	3.65	0.864	0.811	2.23	4.07	5.69	11.51	333.7	1
15	6	45.43	48	6	353.0	380	134.7	73.5	1.93	3.31	0.780	0.730	2.39	4.50	23.83	35.95	333.7	1
16	6	70.70	30	6	326.7	380	136.2	39.9	1.86	5.20	0.760	0.622	2.12	7.56	13.98	45.38	339.2	1
38	7.8	30.92	60	6	354.6	380	135.5	93.6	3.08	4.17	1.252	1.171	2.93	4.06	-4.87	-2.64	333.7	1
39	7.8	42.33	50	6	349.2	380	135.6	78.2	3.30	5.02	1.342	1.178	2.89	4.89	-12.42	-2.59	333.7	1
17	8	17.16	70	6	360.6	380	135.2	112.0	3.44	3.84	1.395	1.290					332.5	1
5	8	16.61	70	60.6	363.9	380	136.7	114.0	3.51	4.25	1.439	1.454					332.5	1
37	8	17.58	70	6	362.0	380	136.5	112.5	3.19	3.83	1.306	1.293					332.5	1
4	8	29.65	60	60.6	356.0	380	135.9	95.6	3.53	4.95	1.439	1.420	3.15	4.42	-10.76	-10.71	333.7	1
18	8	29.85	60	6	356.1	380	135.0	94.7	3.41	4.52	1.381	1.284	3.55	4.87	4.11	7.74	333.7	1
19	8	42.19	50	6	349.7	380	135.1	78.1	3.44	5.36	1.394	1.256	3.34	5.71	-2.91	6.53	333.7	1
3	8	47.20	48	60.6	347.5	380	134.1	70.8	3.49	6.00	1.404	1.274	3.34	6.20	-4.30	3.33	334.8	1
22	8	50.00	45	6	343.2	380	135.6	67.8	3.29	5.84	1.338	1.188	3.13	6.18	-4.86	5.82	334.3	1
21	8	49.59	45	6	344.6	N/A /379	134.1	67.6	3.55		1.428		3.13	6.07	-11.83		334.4	2
20	8	55.79	40	6	N/A	N/A	135.5	59.9	3.14		1.276		3.12	6.92	-0.64		337.3	UVT
23	8	53.17	40	6	N/A	N/A	135.8	63.6	3.31		1.348		2.99	6.65	-9.67		336.7	2
6	8	55.62	40	60.6	N/A	360/ N/A	135.2	60.0	3.47	7.40	1.407	1.332	3.54	7.93	2.02	7.16	339.2	1
7	10	17.70	70	60.6	360.6	380	135.6	111.6	5.05	6.00	2.054	2.009					332.5	1
24	10	17.34	70	6	359.1	380	133.2	110.1	5.45	5.81	2.178	1.919					332.5	1
28	10	17.60	70	6	360.4	380	135.2	111.4	5.24	5.98	2.125	1.999					332.5	1
27	10	29.68	60	6	350.1	380	136.1	95.7	5.09	6.81	2.078	1.955	2.80	3.85	-44.99	-43.47	333.7	1
25	10	29.35	60	6	353.5	380	134.6	95.1	5.38	6.81	2.172	1.943	5.03	6.92	-6.51	1.62	344.6	1
8	10	29.10	60	60.6	355.0	380	134.7	95.5	4.99	6.95	2.016	1.991	3.55	4.82	-28.86	-30.65	333.7	1
29	10	28.48	60	6	351.8	380	135.2	96.7	5.27	6.92	2.138	2.007	3.30	4.53	-37.38	-34.54	333.7	1
31	10	36.90	55	60.6	349.1	380/360	134.7	85.0	5.05	7.21	2.041	1.839	3.52	5.30	-30.30	-26.49	333.7	1
30	10	36.14	55	6	N/A	N/A	135.3	86.4	5.46		2.216		3.57	5.60	-34.62		333.7	5
26	10	38.21	50	6	N/A	N/A	135.3	83.6	5.04		2.046		7.50	12.61	48.81		362.3	1
9	10	42.30	50	60.6	334.3	350/340	135.0	77.9	5.05	7.70	2.045	1.799	4.98	8.60	-1.39	11.69	351.5	1
10	10	44.97	45	60.6	N/A	330/ N/A	134.3	73.9	4.98	7.70	2.006	1.707	4.46	8.25	-10.44	7.14	339.6	2
32	11	17.89	70	6	359.9	380	134.7	110.6	6.43	6.70	2.598	2.223					332.5	1
33	11	24.68	65	9	327.4	380	134.5	101.3	5.95	7.44	2.401	2.261	8.45	10.81	42.02	45.30	362.3	2
34	11	28.66	60	9	N/A	N/A	134.0	95.6	6.33		2.545		5.44	7.36	-14.06		354.2	1
11	12	17.49	70	60.6	361.4	380	133.8	110.4	5.57	6.65	2.236	2.202					332.5	1
40	12	23.50	65	20	333.6	340	134.9	103.2	6.3(REC)		2.550		5.16	6.52	-18.10		341.2	1
12	12	29.42	60	60.6	355.8	377	133.9	94.5	5.49	7.70	2.205	2.183	3.74	5.28	-31.88	-31.43	333.7	1
13	12	41.67	50	60.6	324.8	330	133.9	78.1	5.62	7.75	2.258	1.816	4.71	7.93	-16.19	2.32	339.9	1