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Passive components, including spiral inductors and transformers, fabricated on silicon-based substrates are placing an increasing demand on radio-frequency integrated circuit (RFIC) design. Performance of the RFIC suffers from several non-ideal effects that must be taken into account in order to create a successful design. In particular, monolithic transformers can be a major obstacle for Low-Noise Amplifiers (LNAs), mixers, Voltage Controlled Oscillators (VCOs), and other RFIC circuits. For designers to correctly analyze their designs that include monolithic transformers, lumped-element models suitable for circuit simulation and design optimization are required. This thesis work is mainly concerned with the analysis and the methodology of developing a wide-band compact equivalent circuit model for monolithic transformers fabricated on silicon substrates.

A new wide-band compact equivalent circuit model for monolithic transformers fabricated on silicon substrates is presented. The model achieves high wide-band accuracy through the use of the newly developed "Frequency-Dependent Transformer" (FDT) cell, which effectively takes into account the frequency-dependent conductor losses associated with the transformer's windings. A fast extraction tech-

nique that allows extraction of the circuit parameters from simulated or measured data is also described. Results are presented for various RFIC transformer configurations including stacked and interleaved topologies. This research provides a complete measurement or simulation-based modeling methodology for four-port transformers on lossy silicon substrates.

Analysis and Modeling of Monolithic On-Chip Transformers on Silicon Substrates

by

Yevgeniy Mayevskiy

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Analysis and Modeling of Monolithic On-Chip Transformers on Silicon Substrates

1. INTRODUCTION

1.1. Background and Motivation

It is well known that the integrated circuit (IC), since its introduction in 1958 [1], has affected nearly all parts of contemporary life. The major application of integrated circuits is in microprocessor design. Higher levels of integration have allowed the increase of the computational power and clock speeds of such devices. When digital circuitry became relatively small, the next logical step was to move the analog part onto the on-chip domain. Hence, the first CMOS analog circuits were developed in the mid-1970s. They implemented switched-capacitor concepts, which gave rise to so-called mixed-signal microelectronics. Further evolution of the analog on-chip circuits resulted in RF systems on chip (SOC) that came to existence in the mid-1990s [2]. The decreased size and increased operational frequency caused, in turn, off-chip passive devices to be the major obstacle in the way to reducing the overall system size. The common sense solution is to move the passive components, like capacitors, inductors, and transformers, from the board to the chip realm.

While the first implementation of monolithic inductors on silicon substrates for mixed-signal radio-frequency ICs (RFIC) circuits was achieved as far back as 1966 [3], making the use of integrated passive components practical took more than

two decades. The first useful design of a spiral inductor on silicon substrates is generally attributed to Meyer and Nguyen in 1990 [4]. A few years later, in 1995, advantages of using monolithic transformers in the design of low-voltage silicon bipolar receivers were demonstrated by John Long and Miles Copeland [5]. These researchers successfully incorporated monolithic transformers in preamplifier and mixer designs in a production $0.8\mu m$ BiCMOS process, effectively demonstrating significant improvements in performance compared to silicon broadband designs.

In recent years monolithic transformers have been successfully implemented in RFIC designs. At the time of this writing, monolithic transformers fabricated on silicon substrates are used in silicon RFICs enabling the implementation of high-frequency circuits such as Low Noise Amplifiers (LNAs) [6–9], Voltage-Controlled Oscillators (VCOs) [9–11], and mixers [5], [12].

Nevertheless, passive components implemented on silicon-based substrates suffer from several non-ideal effects that must be taken into account. For the IC designer to get a real benefit in the use of monolithic transformers, accurate compact models that work in time- and frequency-domain simulations are required. It is desirable for the model to have a minimum number of ideal circuit elements, as well as to provide insight into the physical behavior of the device. These requirements are effectively met when the compact model is built based on the measured data and topological features of the real device.

1.2. Types of Monolithic Transformers

A transformer can be considered a device, whose operation is based on mutual inductive coupling between two coils [13]. Fig. 1.1 shows a schematic diagram of an ideal two-coil transformer. Terminals 1 and 3 connect to the primary spiral and

terminals 2 and 4 to the secondary spiral. The reference directions for the currents and voltages are arbitrary. The dots shown near one terminal of each coil are used to indicate the relative orientation of the coils. If a reference ground plane is present, as in on-chip applications, the transformer is typically characterized in terms of a four-port network, where each terminal-ground pair defines a port.

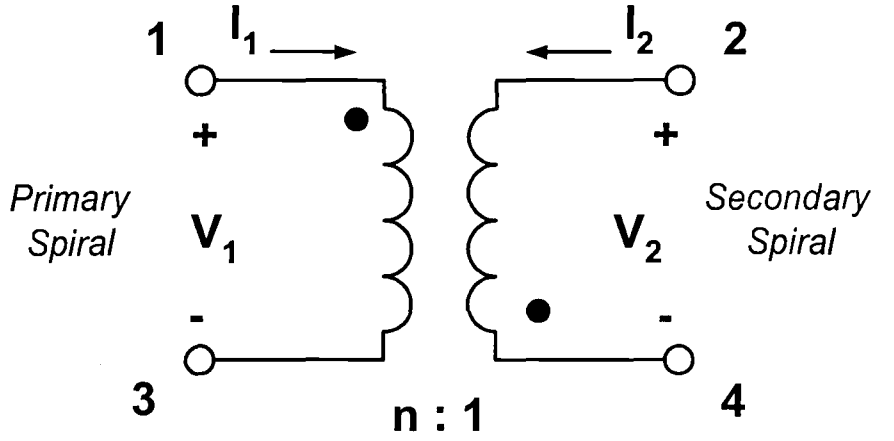


FIGURE 1.1. Schematic diagram of a two-coil transformer. Port 1 and port 3 represent the primary spiral, while port 2 and port 4 represent the secondary spiral.

The transformer performance depends on the relative positions of its coils. The transformer implementation in an integrated circuit is generally restricted to a planar geometry of the metallization layers and offers varying trade-offs among the self-inductance and series resistance of each spiral, the mutual coupling coefficient, port-to-port and port-to-substrate capacitances, resonance frequencies, symmetry and area. Since the monolithic transformer is constructed using conductors inter-wound in the same plane or overlaid as stacked metal, the RFIC implementation

of monolithic transformers can be divided into two major categories: stacked and interleaved transformers.

1.2.1. Stacked Transformers

The symmetrical stacked transformer topology is shown in Fig. 1.2. The primary and secondary windings lie in different planes, as illustrated in the cross-section at the right of the figure. The relative symmetry is achieved by using vias and underpasses in the metallization layer located directly underneath the transformer's spirals for each consecutive turn.

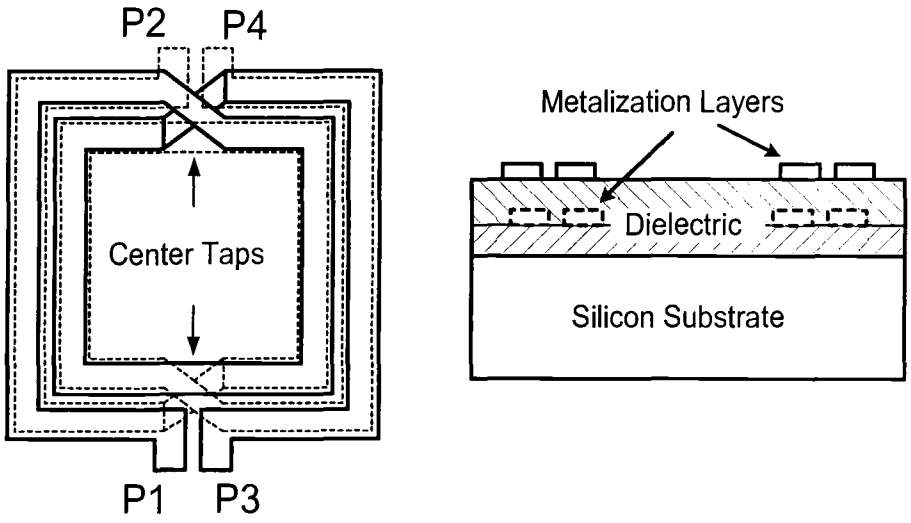


FIGURE 1.2. Generalized stacked transformer winding configuration. Port 1 and port 3 represent the primary spiral, while port 2 and port 4 represent the secondary spiral. The figure on the right shows the cross section of the device.

This transformer layout was first proposed by Rabjohn in [14]. It has also been realized as a balun by connecting center taps at the midpoints between the terminals [15] as indicated in Fig. 1.2. The transformer occupies multiple metal layers and takes advantage of both vertical and lateral magnetic coupling providing high area efficiency, self inductance and coupling. The stacked transformer could also be implemented in non-symmetrical configurations with underpasses in the lower metallization layers.

1.2.2. Interleaved Transformers

An example of interleaved transformer topology is shown in Fig. 1.3. The primary and the secondary windings lie in the same plane as illustrated in the cross-section at the right of the figure. The underpasses that were used to connect the inner terminals, P3 and P4, to the circuitry are not shown for simplicity. This interleaved transformer topology was introduced by Frlan in 1989 [16].

The interleaved transformers are constructed from two parallel conductors that are interwound to promote edge coupling of the magnetic field between windings [15]. The edge-coupling in these transformers allows for smaller interwinding capacitance compared with the stacked transformers, and therefore achieves higher resonant frequencies. The Frlan-style interleaved transformer is best suited for applications that require symmetry [17]. The interleaved transformers can also be constructed in asymmetrical configurations such as the Shibata coupler [18].

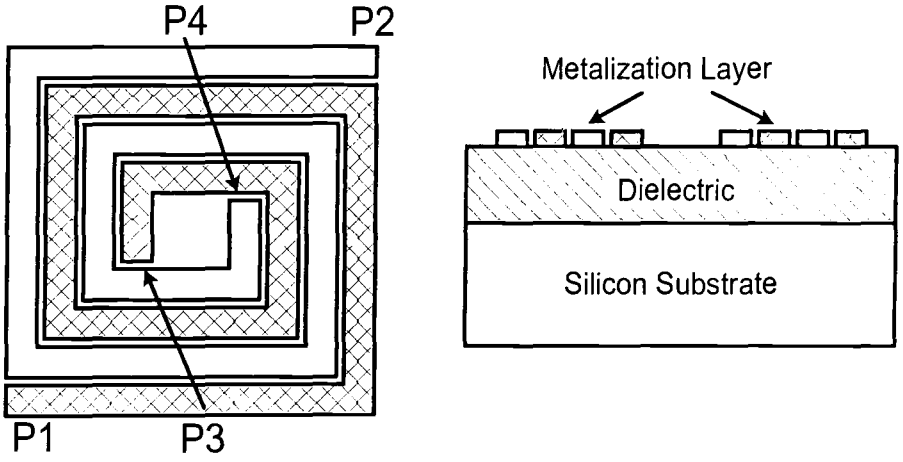


FIGURE 1.3. Generalized interleaved transformer winding configuration. Port 1 and port 3 represent the primary spiral, while port 2 and port 4 represent the secondary spiral. The figure on the right shows the cross section of the device.

1.3. Outline

This thesis presents a complete compact modeling methodology for spiral transformers fabricated on lossy silicon substrates. Emphasis is given to stacked and interleaved transformers as these are currently the most popular layouts on common CMOS and BiCMOS processes. The newly developed model is capable of capturing losses due to the metal windings of the transformers including skin and proximity effects. An automated extraction procedure for high-volume model extraction, which obtains the circuit values from available measured or EM - simulated S-parameter data, will be presented.

Chapter Two gives a review of the different loss mechanisms and commonly used modeling approaches for monolithic transformers in silicon-based ICs. Since the transformer could be considered as a pair of coupled coils, the modeling approaches for monolithic transformers fabricated on silicon-based substrates are similar to the

planar inductor modeling techniques. The major contributors to the transformer losses such as substrate and conductor losses, as well as the effect of interwinding capacitances are described. Based on the circuit topology the transformer models could be divided into three major categories: compact and distributed equivalent circuit models, and behavioral models.

Chapter Three introduces a new transformer model that is capable of modeling the major transformer losses including the mutual resistance. The modeling approach is formulated by solving for the unique network branches, separating the capacitance matrix, and synthesizing branches into ideal lumped elements for a complete equivalent circuit model.

Chapter Four discusses the results for the monolithic transformer modeling methodology presented in Chapter Three. The presented results compare measurement and full-wave electro-magnetic (EM) simulation data to extracted models for various four-port monolithic transformer designs. Results are presented for two major types of the monolithic transformers: stacked and interleaved.

Chapter Five will give conclusions and suggest further transformer modeling approaches.

2. REVIEW OF COMMONLY USED MODELING APPROACHES

2.1. Introduction

The various approaches that are used to model monolithic transformers have the goal of representing the actual measured or EM simulated behavior of the device. Ideally, the circuit model should replicate the device's response both in time and frequency domain. The modeling of monolithic transformers particularly is complicated by the presence of losses that exist due to metal conductors of the windings and the silicon substrate.

This chapter begins with a description of the loss mechanisms inherent to monolithic transformers. The commonly used modeling approaches associated with the different losses are also described. The chapter concludes with the description of common modeling techniques that are used to model monolithic transformers and inductors. The primary interest of this thesis, the development of a wide-band compact model for the monolithic transformer which effectively adapts some of the described loss models, will be considered in detail in Chapters Three and Four.

2.2. Loss Mechanisms in Monolithic Transformers

The performance optimization for monolithic inductors and transformers is usually done in terms of maximizing the quality factor (Q) of the device [19], which is defined as the ratio of the energy stored over the energy lost per unit cycle. This means that to obtain a better performance of monolithic transformers, the electromagnetic energy stored by the device needs to be maximized while minimizing the energy dissipation. Moreover, the useful operational frequency range of

the monolithic transformers is limited by the self-resonant frequency (SRF) value, which is defined as the frequency at which the parasitic capacitances resonate with the inductance of each winding [15]. The SRF depends mainly on the interwinding capacitance of the device. Consequently, the most important parasitics that affect the performance of monolithic transformers are due to conductor losses of the transformer windings, the conductive silicon substrate, and the silicon oxide insulation layer.

2.2.1. Conductor Losses

When time-varying current is applied to the ports of the primary spiral with self-inductance L_1, time varying magnetic fields are produced. These fields are linked with the secondary spiral with self inductance L_2 of the monolithic transformer and produce a time-varying voltage across the terminals of the secondary spiral. Thus, the spirals become magnetically coupled via a term known as mutual inductance (L_m or M). For an ideal transformer with negligible losses and no flux leakage, the following expression is true, $L_m = M = \sqrt{L_1 L_2}$.

The ideal situation changes when the transformer's windings are made of materials with finite conductance and the coupling is non-ideal. For conductors with rectangular cross-section, as typically used in the fabrication of planar spiral inductors and transformers, the low frequency (DC) resistance is expressed as

$$R_{DC} = \frac{l}{\sigma W t} \tag{2.1}$$

where W is the width, t is the thickness, l is the total length of the conductor, and σ is the conductivity of the conductor material. At higher frequencies, the series resistance becomes a complex function due to magnetically induced eddy currents [20]. Fig. 2.1 illustrates eddy current loops induced in a segment of the

transformer winding. Equation 2.1 can be modified to approximate these effects as [20]

$$R_{RF} = \frac{l}{\sigma W \delta (1 - e^{\frac{-t}{\delta}})} \tag{2.2}$$

where δ is the skin depth given by

$$\delta = \sqrt{\frac{2}{\omega \mu \sigma}}. \tag{2.3}$$

Here μ is the magnetic permeability of the material and ω is the operational frequency of the device. Moreover, eddy current losses result in magnetic flux reduction that in turn lowers the self inductance of each spiral [22]. Therefore, to accurately

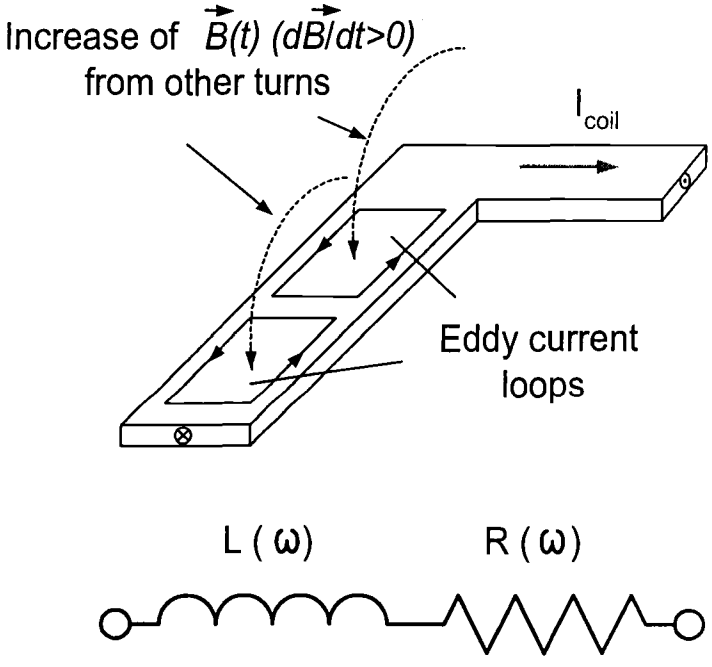


FIGURE 2.1. Illustration of conductor eddy currents and circuit representation of frequency-dependent conductor losses for each segment of the transformer's spirals [21].

model conductor losses of each spiral over a broad frequency range, it is imperative to consider the frequency-dependent inductance and resistance of each spiral. These are generally expressed as series $R(\omega)$ and $L(\omega)$ elements for each segment of a monolithic transformer's spirals, as illustrated by the circuit shown at the bottom of Fig. 2.1.

The frequency-depended circuit elements could be simulated directly in frequency-domain circuit simulators such as Agilent-ADS [23]. To obtain the broadband response of the series impedance elements in a time-domain simulator, the characteristics are typically represented in terms of an equivalent circuit consisting of ideal lumped elements such as ladder circuits [24] or transformer loops [25]. The same circuit representation is often used in compact modeling of transformers to represent the magnetic losses of each spiral of the transformer, which are coupled via a constant mutual inductance.

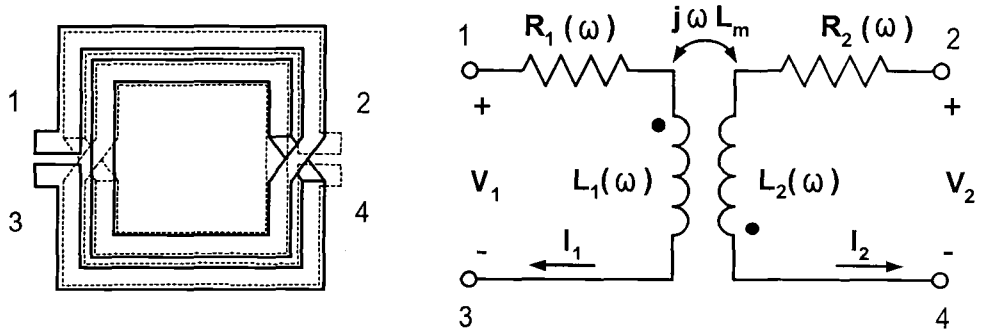


FIGURE 2.2. Left - the physical layout of two-winding stacked transformer configuration. Right - common circuit representation of conductor losses for a two-winding transformer, where L_m represents the mutual inductance term. The terminal labeling of the physical layout corresponds to the terminal labeling in the circuit representation.

Therefore, a generally accepted compact model that is supposed to capture conductor losses of the transformer is expressed by circuit depicted on the right of Fig. 2.2. The dot convention in the circuit defines the sign of the mutual inductance term based on input and output currents, and voltages, hence, one can write the following equations to relate the induced voltages through mutual coupling

$$V_1 = (R_1(\omega) + j\omega L_1(\omega))I_1 - j\omega L_m I_2 \tag{2.4}$$

$$V_2 = -j\omega L_m I_1 + (R_2(\omega) + j\omega L_2(\omega))I_2. \tag{2.5}$$

This approach, however, has the following weakness: frequency dependence of mutual inductance and mutual resistance, which exists in monolithic transformers [26] is not considered in this model.

2.2.2. Substrate Losses

The major drawback of monolithic transformers fabricated in CMOS technology is the extra loss due to the finite resistivity of the silicon substrate. The time-varying EM fields interact with the substrate causing two dominant loss parts: capacitive (electric loss) caused by finite resistance due to electrically induced conductive and displacement currents, and magnetic loss resulting from magnetically induced eddy current resistance.

When magnetic fields penetrate the heavily-doped silicon substrate they lead to currents into the substrate, called substrate eddy currents, which cause extra resistive loss. Fig. 2.3 illustrates the substrate eddy currents in a single spiral on a lossy silicon substrate. Current flowing in the substrate generates ohmic losses that cause an increase of self and mutual resistances of the transformer windings in a

frequency-dependent manner. This mechanism is similar to the substrate magnetic losses in spiral inductors [27, 28], and coupled interconnects [29, 30], and can be modeled using the same circuit as the one used to represent the conductor losses shown in Fig. 2.1.

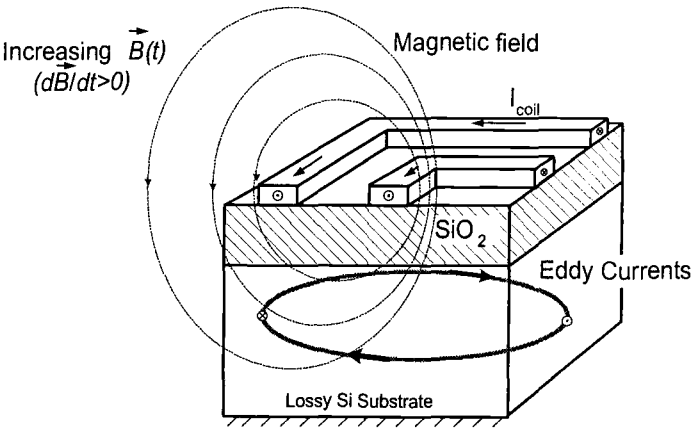


FIGURE 2.3. Currents and fields in a transformer coil fabricated on a lossy silicon substrate

The capacitive substrate loss is caused by the electric field, which is created by the surface charges of the spirals, and the transformer's spirals become coupled with the conductive substrate. The time-varying electric field causes displacement currents in the oxide layer and conduction and displacement currents in the conductive substrate [27] as illustrated in Fig. 2.4. These effects can be modeled with a shunt element composed of a capacitor (C_{ox}) in series with a parallel combination of substrate resistor (R_{sub}) and capacitor (C_{sub}) [15], as shown on the right side of Fig. 2.4. This substrate loss model is commonly referred as the $C - GC$ model.

This circuit model, which consists of ideal lumped elements, gives the broadband response of the shunt admittance $Y_{shunt} = G(\omega) + j\omega C(\omega)$ that is generally found in on-chip spiral inductors and transformers.

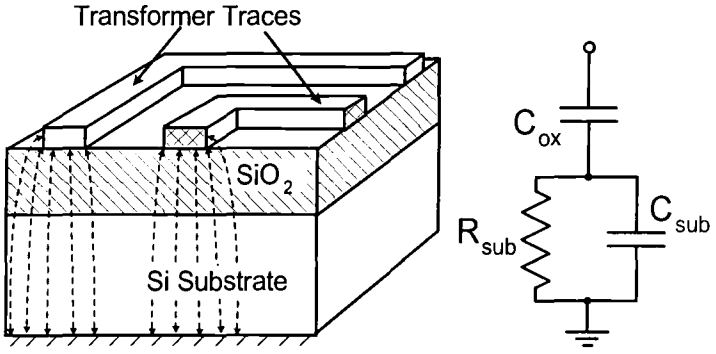


FIGURE 2.4. Shunt electric field in monolithic transformer and the circuit model to represent substrate losses

Both capacitive and magnetic substrate losses can be minimized if low-conductivity substrates are used [31]. Some research work has shown that the quality factor of the spiral inductors could be significantly improved if the substrate losses are minimized through the use of fabrication techniques such as micromachining [32, 33], applying a patterned ground shield [34], or using a high resistivity substrates [35, 36]. Moreover, it has been shown that stacked transformers are less prone to substrate magnetic losses compared to the interleaved (bifilar and nested) types of transformers [37] due to the shielding effect of the secondary winding located in between the primary winding and lossy substrate.

2.2.3. Interwinding Capacitance

The interwinding parasitic capacitance is caused by the differences in electric potentials between various parts of the transformer's metal windings structure. This term is also referred to as fringing capacitance. The lateral electric fields created as a result of such coupling are illustrated in Fig. 2.5. These fields produce displacement currents, which can be effectively modeled by capacitive circuit elements.

There are two major capacitive interactions in the four-port monolithic transformers: self capacitance of each spiral, i.e., in between the ports of each individual spiral, and mutual capacitance between the primary and secondary windings of the transformer. In a typical monolithic transformer, the effective mutual capacitance could be much greater than the self capacitance due to the large surface area between the spirals and greater potential difference between the primary and the secondary windings. Therefore, the interwinding self capacitance, which is commonly used in single inductor models, is usually neglected in compact transformer models [38].

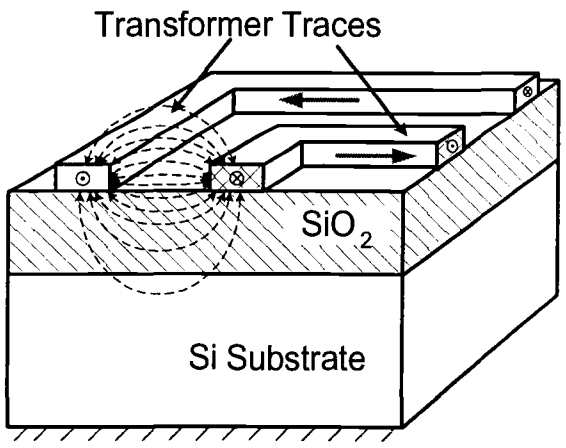


FIGURE 2.5. Lateral electric field in monolithic interleaved transformer.

2.3. Commonly Used Modeling Techniques

Although there are many kinds of the monolithic transformer models, they all can be subdivided into three major groups. The first two are electrical models for monolithic transformers that can be derived from the physical geometry and properties of the transformer structure. The third group contains models that can be built based on the electrical behavior of the devices, usually described by scattering parameters [39]. The first two approaches result in topological modeling which can be either distributed or compact, and the latter approach results in behavioral-type models. This section describes these techniques in regards to monolithic transformers fabricated on lossy silicon substrates.

2.3.1. Distributed Model

The distributed modeling approach is intended to represent all major geometrical features of the devices. For the transformer case, this could be loss contributions from each segment of the windings [40], or the circuit model could be created for each turn of the transformer model [41]. This subsection considers the most advanced of these model types, which take into account major loss mechanisms of monolithic transformers.

The first case can easily be understood by considering each segment of the primary winding. It has certain AC and DC resistances and is coupled to the substrate and adjacent traces of the same and the secondary windings. Therefore, the contribution of each segment to the overall characteristics could be described in terms of a model that is assembled using circuit components described in Section 2.2. An example of this model for a single segment of a transformer's winding is shown in Fig. 2.6. The circuit element values of this model are determined using closed

form expressions for self and mutual capacitances developed by Grover [42] and Wheeler [43].

A modified approach combines the characteristics of one turn of each spiral into a reduced circuit model resulting in a more compact model. A good example of this approach is a circuit model developed by Kythakyapuzha and Kuhn [41], who used lumped elements to represent the spirals on a turn-by-turn basis. The model for a three-turn stacked transformer is illustrated in Fig. 2.7. The model incorporates two sets of transformer loops. One set is intended to take into account substrate magnetic losses described in the section 2.2.2 (R_{ei}-L_{ei} loops). The second set of

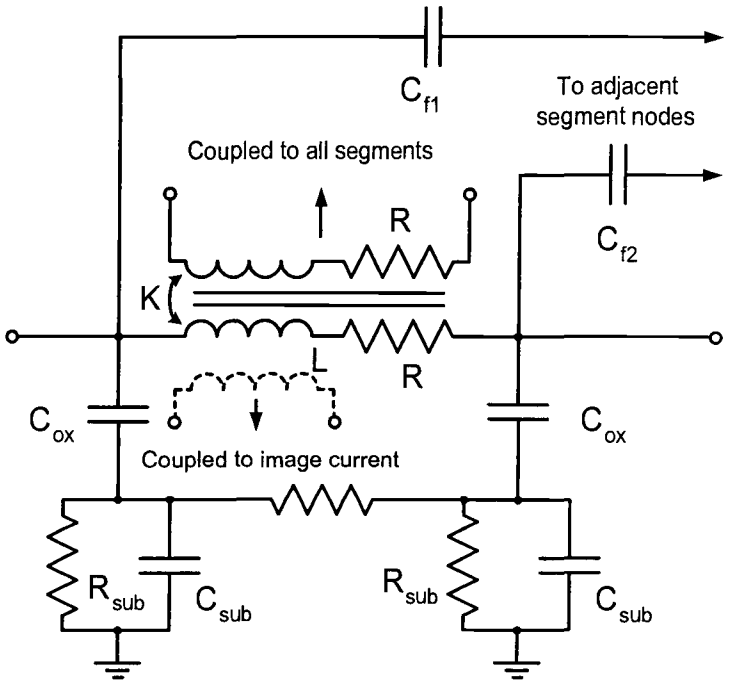


FIGURE 2.6. Equivalent two-port for one segment of the spiral inductor presented by Koutsoyannopoulos [40]. A similar model could be used to build a distributed model for monolithic transformers as well.

transformer loops (R_{ci}-L_{ci}) captures conductor losses explained in the section 2.2.1. Fringing capacitance is expressed by C_{fi} terms, oxide capacitance is modeled by C_{11}, C_{12}, C_{13}, C_{14}, C_{15} and C_{16} terms, and the secondary spiral is electrically coupled to the substrate via C_{subi}, R_{epii}, R_{si}, R_{subi} terms. Since only one spiral in the stacked

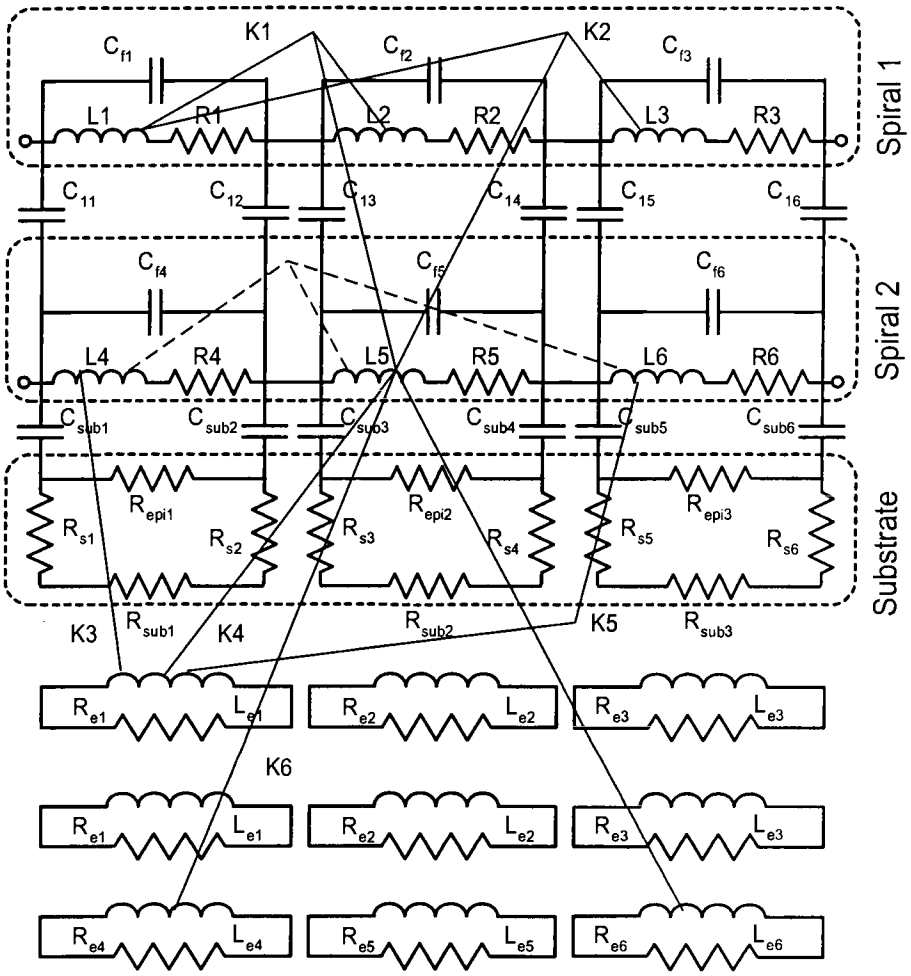


FIGURE 2.7. Equivalent model for two layer, three turn spirals developed by Kythakyapuzha [41] (not all coupling coefficients are shown).

configuration is located near the substrate layer, the substrate eddy current losses for the uppermost spiral are negligible and not required to be modeled.

2.3.2. Compact Model

The distributed transformer models described in the previous subsection may include hundreds of circuit elements. However, for the purposes of device characterization, efficient circuit modeling, and component library development, more simplified or compact models are required. Such models should accurately capture transformer losses over a wide frequency range and consist of ideal lumped elements allowing circuit simulation in time domain as well.

A variety of compact transformer models and circuit extraction approaches have been proposed in recent years. Analytical models and expressions to determine circuit values for interleaved and stacked transformers were developed in [17]. The equivalent circuit model for a pair of coupled inductors was introduced in [44]. A more generalized four-port transformer model with an ideal transformer in its core was described in [15], and is shown in Fig. 2.8.

This model has four independently driven ports (i.e., P, $\overline{P}$, S, $\overline{S}$) some of which could be shorted to ground in some applications. Primary (L_p, R_p) and secondary (L_s, R_s) impedances account for leakage of the magnetic flux between the windings. The interwinding capacitance is modeled with the capacitors connected between the ports of the transformer. The model utilizes shunt impedance branches (Z_{shi}) shown in Fig. 2.4 to take into account the parasitics between the ports and substrate. The core of the model is an ideal linear transformer with mutual inductance (L_m) and turns ratio $1 : n$. Although this model considers major losses of the monolithic transformers, it fails to provide an accurate response over a broad

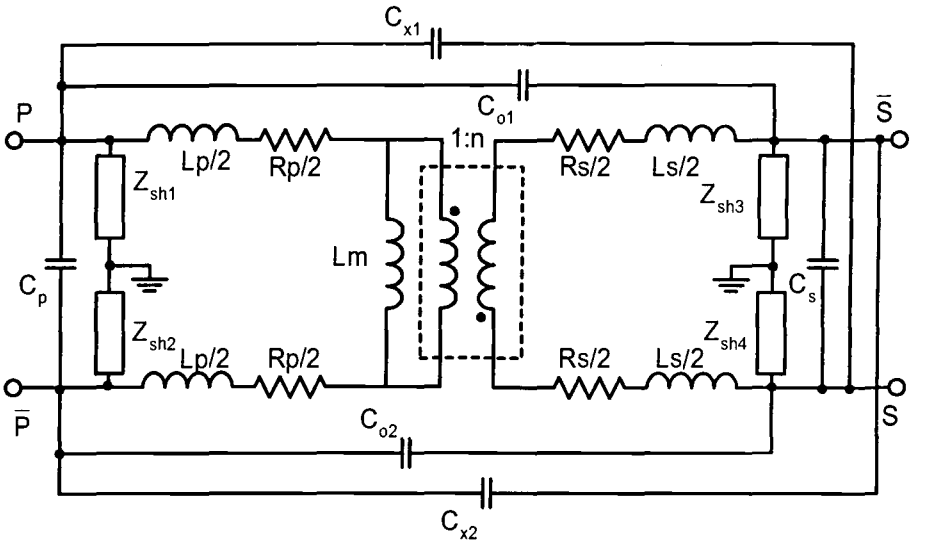


FIGURE 2.8. Equivalent compact model for a four-port $1 : n$ transformer presented by Long [15]. Shunt circuit elements Z_{sh} can be modeled using the circuit shown in Fig. 2.4.

frequency range. It neglects the frequency dependence of the self and mutual impedances of the transformer's windings, completely ignoring the mutual resistance term.

2.3.3. Behavioral Model

In some cases RF designers may not need the topological relation of the model to the actual device geometry; it is sufficient for them to have the accurate response of the simulated data. This demand is satisfied with so-called behavioral or data-driven types of models. The behavioral model is a circuit model that, when simulated, represents the electrical behavior of the device without considering the actual topology or physical layout of the structure. This model could be considered

a "black box" type of model because the user usually does not have the ability to control the circuit element values included in the model description.

Examples of such modeling approaches include MeasureXtractor modeler by TDA Systems [45], EMtoSPICE S-parameter-to-SPICE model converter by EM-Wonder [46] and black-box elements of Ensemble by Ansoft [47]. Data-driven models allow the user to bypass manual intervention in the modeling process and extract circuit netlists, which represent the behavioral characteristics of the devices being modeled. Since the data-driven models are based on the concept of multi-port networks and a system matrix, the user has to take measurements of all ports of the device to be able to characterize the model. An n-port network is generally characterized by an n by n system matrix, therefore requiring the measurement of the n by n S-parameter matrix.

Among the benefits of behavioral models are the ability to model various types of passive structures without user intervention and the ensured stability of the circuit models. Nevertheless, the frequency range for such models is limited by the abilities of the software algorithms to handle a certain number of poles. Data-driven models also do not provide much insight into the important topological characteristics of the devices and the generated netlists often contain negative circuit element values, which are not compatible with some circuit simulators.

2.4. Conclusion

The important losses and respective modeling techniques for the monolithic transformers fabricated for RFIC applications have been covered in this chapter. The ultimate goal of any modeling technique is to be able to capture major losses inherent to the passive structure over a wide frequency range. Various circuits could

be used to capture the individual losses in the conductors of the windings and silicon substrate, and then the final transformer model could be assembled as a distributed or compact model. Alternatively, the behavioral modeling approach can be used to generate a netlist that replicates data behavior.

While distributed and behavioral models are capable of capturing the losses, they have the drawback of being relatively large while providing little insight on the characteristics of the device. Compact models, on the other hand, are more intuitive and do not require as many computational resources as their behavioral or distributed counterparts. For this reason this work focuses on the development of an accurate compact model for monolithic transformers that is accurate over a wide frequency range.

3. NEW TRANSFORMER MODELING APPROACH

3.1. Introduction

While common transformer modeling approaches consider the monolithic transformer fabricated on silicon substrates as a pair of magnetically coupled inductors, the mutual frequency-dependent resistance due to conductor losses is usually ignored. This assumption was originally made for power transformers where the eddy current loss, the main source of the mutual resistance, was relatively small compared to the hysteresis losses [48]. Moreover, the mutual inductance in between the coils is assumed to be constant. However, failing to include the frequency-dependent mutual resistance and inductance terms into a compact circuit model results in an underestimation of the real coupling term (K_{Re}) given in [49] in the lower frequency range (up to the first SRF) at which transformers are usually designed to operate. This, in turn, may cause the circuit simulations to underestimate the power consumption and the noise figure value.

This chapter describes a new frequency-dependent transformer (FDT) model that effectively captures conductor losses in the transformer windings. It also describes an automated extraction procedure that allows the determination of the topology elements and the lumped element circuit values for the complete transformer model from measured or EM-simulated S-parameter data. The presented monolithic transformer model is compact and consists solely of frequency-independent lumped circuit elements, making it a perfect candidate for time domain circuit simulations.

3.2. Frequency-Dependent Transformer

The new monolithic transformer model introduced in this section is intended to capture the important losses that are exhibited by planar transformers fabricated on lossy silicon substrates but not included in previous models. The core of the model is the FDT cell shown in Fig. 3.6. The FDT cell captures the conductor losses of the transformer's windings including the frequency-dependent mutual inductance $L_m(\omega)$ and resistance $R_m(\omega)$. The AC conductor loss mechanism in monolithic transformers is primarily caused by eddy current losses, which are a combination of both skin and proximity effects. These losses are highly dependent on the physical and geometrical properties of the metal windings. Even though significant efforts to improve the transformer's performance have been reported in recent years [50, 51], monolithic transformers still exhibit a significant amount of conductor losses.

The following subsections will show that the conductor losses in monolithic transformers fabricated for RFIC applications need to be characterized not only in terms of conductor losses of the individual spirals, but also in terms of the frequency-dependent mutual inductance and resistance. A new circuit model that accurately captures conductor eddy current losses is proposed. The circuit model is synthesized in terms of ideal lumped elements and controlled sources.

3.2.1. Frequency Dependent Mutual Resistance and Inductance

The transformer implementation in an integrated circuit is generally restricted to a planar geometry, and the fabrication is done on a substrate having finite conductivity. The planar geometry is not optimal for device performance and greatly contributes to the conductor loss. When a high resistivity substrate is

used for the transformer design, electric and magnetic substrate losses described for inductors in [20] are minimized, and conductor loss dominates at low frequencies.

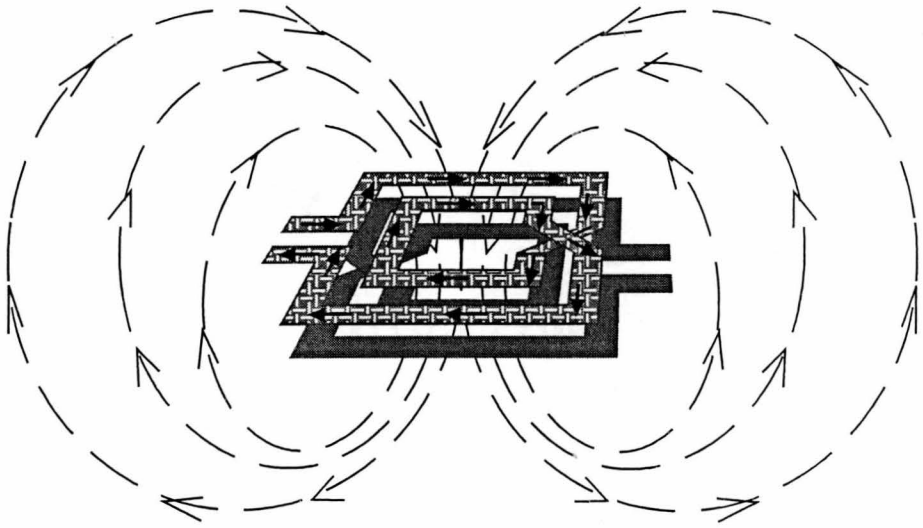


FIGURE 3.1. Magnetic fields in the windings of monolithic transformer. The uppermost spiral is the primary spiral where the direction of alternating current is shown by arrows.

The conductor loss mechanism in planar transformers can be easily understood by considering a stacked monolithic transformer configuration as shown in Fig. 3.1. According to the Faraday - Lenz law, when a time-variant current is applied across the input terminals of an upper coil, known as the primary spiral, the resulting magnetic fields are linked to the spiral below, known as the secondary spiral, and produce a voltage that can be measured at its terminals. Ideally, all magnetic flux generated by the transformer would be confined in the hollow opening of the transformer, where its classical counterpart would have a magnetic core. Nevertheless, part of the magnetic flux penetrates the metal windings of the transformer.

This magnetic flux has non-tangential components with respect to the metal windings creating in turn eddy currents within the traces [21], as illustrated in Fig. 2.1. This effect, also known as current crowding, constricts the current flow in the spirals resulting in higher resistances and lower self and mutual inductances compared with DC behavior.

The loss from the eddy currents was often neglected in the classical transformers (transformers that have a magnetic core to provide a continuous magnetic path) due to its relatively low contribution to the overall transformer losses [48, 52]. However, with increasing operational frequency, eddy current losses in conductors become more pronounced and need to be included in the transformer analysis. It has been shown that eddy current loss in multi-layer coil designs would be significantly underestimated if only losses due to an isolated conductor and an external magnetic field are considered [53]. Some years later, the formulation of a general, complete electrical terminal representation of eddy current loss in transformer windings was presented by Spreen [54]. Interestingly, Spreen has derived an approximate expression for mutual resistance (R_m) in a two-foil winding with a shield, which is given by

$$R_m(\omega) = -\frac{1}{2}\frac{\rho\lambda}{b\delta}G(h_3/\delta) \tag{3.1}$$

where

b is the width of the conductor as illustrated in Fig. 3.2

h is the thickness of the conductor

ρ is the resistivity of the conductor

δ = usual skin depth = $\sqrt{\frac{2\rho}{\omega\mu}}$

ω = radian frequency

μ = permeability of the conductor

$G(x)$ is a geometrical factor $= \frac{sinh(x)-sin(x)}{cosh(x)+cos(x)}$.

This formulation deserves special attention. Eddy currents are induced in a conductor when it is immersed in time-varying magnetic fields. This effect is governed by Faraday-Lenz's law, and it happens independently whether or not the conductor carries current. Eddy currents in their turn, produce their own magnetic fields that oppose the change in the original field. Therefore, not only do they increase the AC resistance, but they also decrease mutual inductance in transformers. Now, if the shield's thickness h_3 is treated as the surface area of the metal windings subjected to the non-tangential magnetic fields, then expression (3.1) draws an important conclusion: the greater the coil's conductor surface area that is perpendicular to the magnetic flux direction the greater the mutual resistance and the smaller the mutual inductance values are expected to be. The formula also indicates that the mutual resistance equals zero at DC and increases as the operational frequency increases.

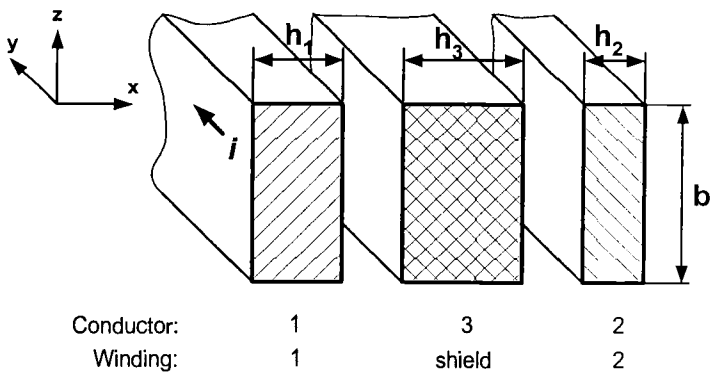


FIGURE 3.2. Geometry used to derive expression (3.1) for mutual resistance in a two-foil winding with a shield [54].

To test this assumption, an experiment was designed where two simple transformer structures were simulated with HFSS. The simulated structures, which resemble one turn test transformers are shown in Fig. 3.3. They both have the same distance between the primary and secondary windings, as well as overlap area to keep the interwinding capacitance the same. The outer diameter of the transformers was designed in such a way so that the trace length difference between the two structures was minimized. Since the opening of Structure 1 is smaller than the opening of the Structure 2, and the orientation of spirals in Structure 2 is more in parallel to the magnetic flux direction, it is expected that the Structure 2, will produce a smaller value of $R_m(\omega)$.

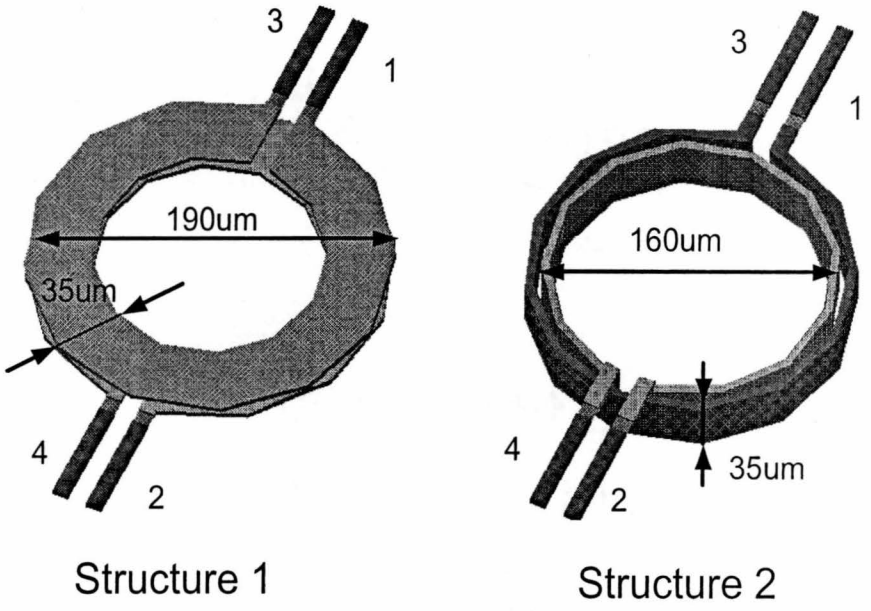


FIGURE 3.3. Single-turn transformers used to verify mutual resistance (R_m). Ports of the primary spiral are labeled as 1 and 3, and ports of the secondary spiral are labeled as 2 and 4. Conductor thickness is $4\mu m$, and the gap between conductors is $5\mu m$.

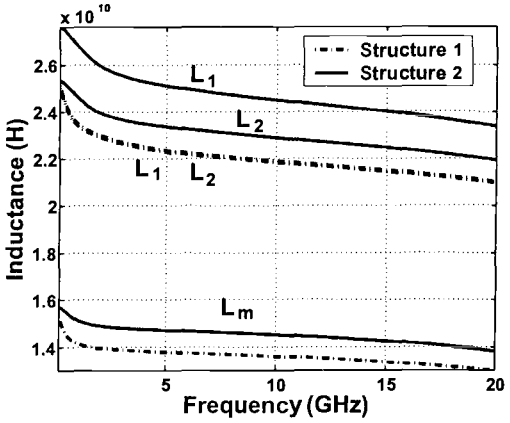


FIGURE 3.4. Frequency dependent self (L_1, L_2) and mutual (L_m) inductances.

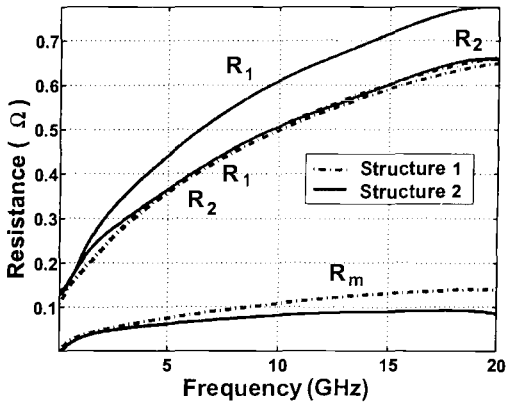


FIGURE 3.5. Frequency dependent self (R_1, R_2) and mutual (R_m) resistances.

The simulation results, which are shown in Figs. 3.4-3.5, confirm the expected response. The eddy currents have less effect on the inductive values of Structure 2, and, despite the approximately equal trace lengths, the self (L_1, L_2) and mutual (L_m) inductances are higher than in the Structure 1. Fig. 3.5 illustrates the eddy current effect on the self (R_1, R_2) and mutual (R_m) resistances. While the DC values of the self-resistances are nearly the same, the AC series resistance of the primary spiral (R_1) of Structure 2 has greater value than the AC series resistance of the secondary spiral (R_2). The greater increase of R_1 compared to R_2 for Structure 2 may be due to the location of the coils with respect to the magnetic flux inside of the transformer's hollow opening. The mutual resistance (R_m) of the Structure 2, however, is lower than that of Structure 1, confirming that the mutual resistance depends on the overall area of the non-tangential magnetic flux penetration.

Another important conclusion that can be drawn from Fig. 3.5 is that the frequency-dependent mutual resistance may have a relatively large value and needs to be included in the transformer models. Structure 1 shows that at 10 GHz $R_m =$

$0.2R_1$ even for this simple configuration. In the real monolithic transformer, the spirals are usually located in the plane perpendicular to the magnetic flux direction, similar to Structure 1, confirming the need for modeling frequency-dependent mutual inductance and resistance.

3.2.2. Equivalent Circuit Model

It was shown in the previous section that the frequency-dependent mutual inductance and resistance make a significant contribution to the overall conductor losses in monolithic transformers due to their inherent planar geometry. Therefore, monolithic transformers have to be represented with a more accurate model than a pair of coupled lossy inductors model. The proposed circuit for the conductor losses of the monolithic transformers, named a frequency-dependent transformer (FDT) cell, is shown by the dashed box in the Fig. 3.6. This circuit is a realization of the general governing equations for the conductor losses of the transformer defined by the equations (3.2) and (3.3).

$$V_1 = (R_1(\omega) + j\omega L_1(\omega))I_1 - (R_m(\omega) + j\omega L_m(\omega))I_2 \tag{3.2}$$

$$V_2 = -(R_m(\omega) + j\omega L_m(\omega))I_1 + (R_2(\omega) + j\omega L_2(\omega))I_2 \tag{3.3}$$

The voltages and currents in equations (3.2) and (3.3) for the FDT cell are not shown in Fig. 3.6 due to lack of space but are defined in Fig. 2.2.

These equations not only take into account the frequency-dependent self impedances but also define the loss contribution from the frequency-dependent mutual inductance and resistance. In these equations, the components $R_1(\omega)$, $L_1(\omega)$, and $R_2(\omega)$, $L_2(\omega)$ are the self resistances and inductances of the primary and secondary

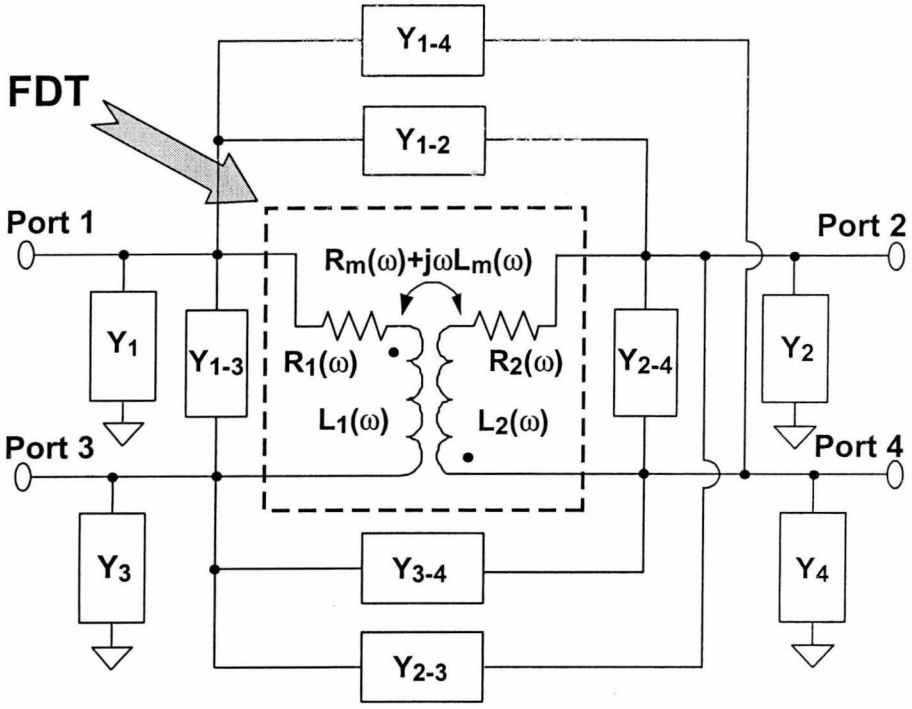


FIGURE 3.6. Generalized compact network topology for the monolithic transformers in RFICs and circuit representation of the FDT cell. Port 1 and port 3 represent the primary spiral, while port 2 and port 4 represent the secondary spiral.

windings, respectively. The transformer windings are coupled via the mutual impedance term $R_m(\omega) + j\omega L_m(\omega)$, which can be seen to induce a voltage in one of the coils due to a current in the other coil. The directions of voltages and currents are defined in Fig. 2.2. Since the windings are electrically isolated at DC, the mutual resistance term $R_m(\omega)$ must approach zero value as the frequency approaches zero.

When the FDT cell is incorporated into the compact model, taking into account all major loss contributors, it results in the topology shown in Fig. 3.6. Although, the circuit elements of the FDT cell shown in the figure are frequency dependent, this topology can be easily synthesized in terms of ideal lumped pas-

sive circuit elements and ideal controlled sources. The compact circuit can realize the frequency dependence of the self and mutual terms of the FTD cell with ideal lumped elements using a ladder [24] or transformer loops [27] circuit representation. The current-to-voltage transformation can be realized by utilizing the configuration described for coupled interconnects in [55]. The resulting circuit schematic is shown in Fig. 3.7, where the interwinding capacitances are not shown for simplicity.

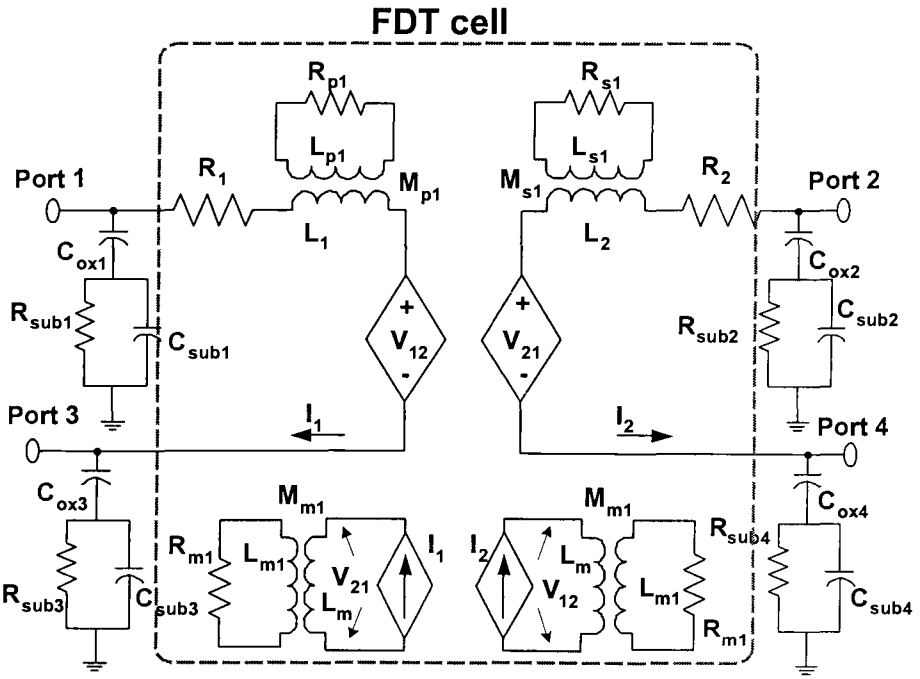


FIGURE 3.7. Complete lumped-element circuit model for monolithic transformers fabricated on silicon substrates. Port-to-port and mutual capacitances are not shown for simplicity.

3.3. Extraction Procedure

Although some of the model parameters could be extracted using analytical expressions developed for monolithic transformers similar to those described in [17, 56], an approach that allows one to obtain the parameters directly from measurements or full-wave simulation results appears to be more advantageous, especially at the design verification stage. The extraction procedure is based on the general extraction methodology described for spiral inductors in [57, 58]. In this extraction procedure, the network topology branch functions are determined first, and then each branch function is approximated as an ideal lumped-element circuit.

In order to perform the extraction in an automated way, the algorithm shown in Fig. 3.8 was designed. Once the S-parameter data are loaded, they are converted to the admittance matrix. The admittance matrix provides unique branch functions for shunt admittances, and allows to predetermine possible ranges for the branches that represent interwinding capacitances and conductor losses of the monolithic transformer. Finally, the interwinding capacitances are searched for the best possible combination, and the circuit-element values are extracted for the selected data set. This procedure allows to determine circuit-element values for the model shown in Fig. 3.7 and is described in more detail in the following subsections.

3.3.1. Admittance Matrix Solution

The four-port admittance matrix of the transformers obtained by measurement or EM simulation can provide an important insight into how the solution for the proposed model topology may be determined. The separation of the admittances in the generalized network topology shown in Fig. 3.6 yields three important terms of the admittance matrices expressed by equation (3.4). These three matri-

ces provide a decoupled representation of the major loss mechanisms described in Section 2.2.

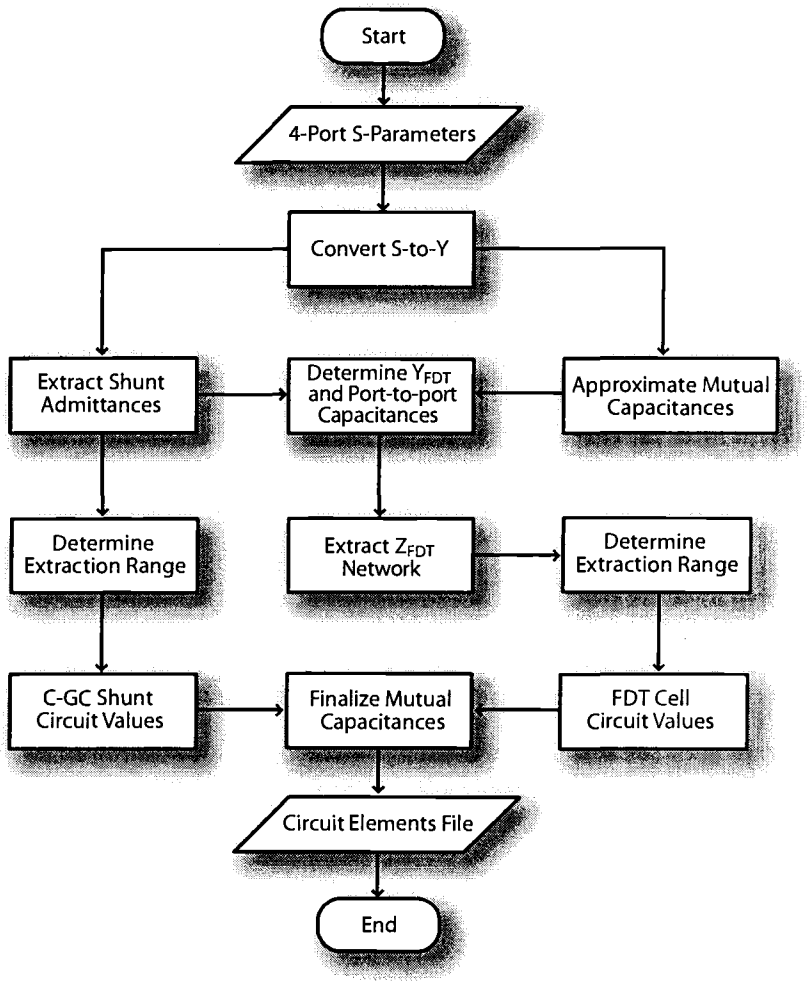


FIGURE 3.8. Extraction algorithm for automated determination of the circuit values of the monolithic transformer model.

$$[Y] = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{12} & Y_{22} & Y_{23} & Y_{24} \\ Y_{13} & Y_{23} & Y_{33} & Y_{34} \\ Y_{14} & Y_{24} & Y_{34} & Y_{44} \end{bmatrix} = \begin{bmatrix} Y_1 & 0 & 0 & 0 \\ 0 & Y_2 & 0 & 0 \\ 0 & 0 & Y_3 & 0 \\ 0 & 0 & 0 & Y_4 \end{bmatrix}$$

$$+ \begin{bmatrix} Y'_{11} & Y'_{12} & -Y'_{11} & -Y'_{12} \\ Y'_{12} & Y'_{22} & -Y'_{12} & -Y'_{22} \\ -Y'_{11} & -Y'_{12} & Y'_{11} & Y'_{12} \\ -Y'_{12} & -Y'_{22} & Y'_{12} & Y'_{22} \end{bmatrix}$$

$$+ j\omega \begin{bmatrix} C_{1-2}+C_{1-3}+C_{1-4} & -C_{1-2} & -C_{1-3} & -C_{1-4} \\ -C_{1-2} & C_{1-2}+C_{2-4}+C_{3-2} & -C_{2-3} & -C_{2-4} \\ -C_{1-3} & -C_{2-3} & C_{2-3}+C_{3-4}+C_{1-3} & -C_{3-4} \\ -C_{1-4} & -C_{2-4} & -C_{3-4} & C_{1-4}+C_{2-4}+C_{3-4} \end{bmatrix} \tag{3.4}$$

The first term in equation (3.4) represents port-to-substrate admittances which characterize substrate losses in the monolithic transformer structure. The second term consists of four identical 2 x 2 matrices located in each of its four quadrants. These admittance matrices represent the conductor losses of the FDT cell defined in Fig. 3.6 when the nodes of ports 3 and 4 are shorted to ground. The third term in equation (3.4) represents the interwinding capacitive interactions between the ports of the monolithic transformer. Therefore, the individual network topology elements can be determined by separating the loss contributions of each term from the measured or EM simulated admittance data.

3.3.2. Shunt Circuit

The shunt branches Y_1, Y_2, Y_3, and Y_4 shown in Fig. 3.6 represent port-to-substrate interactions of the monolithic transformer. They can be uniquely determined simply by the summation of row elements in the admittance matrix $[Y]$ of the system as it is shown in the equation below.

$$\begin{bmatrix} Y_1 \\ Y_2 \\ Y_3 \\ Y_4 \end{bmatrix} = \begin{bmatrix} Y_{11} + Y_{12} + Y_{13} + Y_{14} \\ Y_{12} + Y_{22} + Y_{23} + Y_{24} \\ Y_{13} + Y_{23} + Y_{33} + Y_{34} \\ Y_{14} + Y_{24} + Y_{23} + Y_{44} \end{bmatrix} \tag{3.5}$$

Each shunt admittance term (Y_n) in equation (3.5) can be expressed in terms of the frequency-dependent conductances ($G_n(\omega)$) and capacitances ($C_n(\omega)$) as follows:

$$Y_n(\omega) = G_n(\omega) + j\omega C_n(\omega). \tag{3.6}$$

This shunt admittance could be realized in the $C - GC$ circuit topology described in Section 2.2.2. The typical trends of the $C - GC$ topology are shown in Fig. 3.9. It is seen that $C_n(\omega)$ decreases with frequency, while $G_n(\omega)$ increases. The input impedance of the shunt circuits shown in Fig. 2.4 is:

$$Z_{shunt_n}(\omega) = Y_n^{-1}(\omega) = \frac{1}{j\omega C_{ox_n}} + \frac{1}{G_{sub_n} + j\omega C_{sub_n}} \tag{3.7}$$

where the subscript n denotes the shunt branch number. The C_{ox_n} term is extracted from the low-frequency asymptote of the shunt admittance data, and the remaining terms are determined using the Cauchy method described in [27].

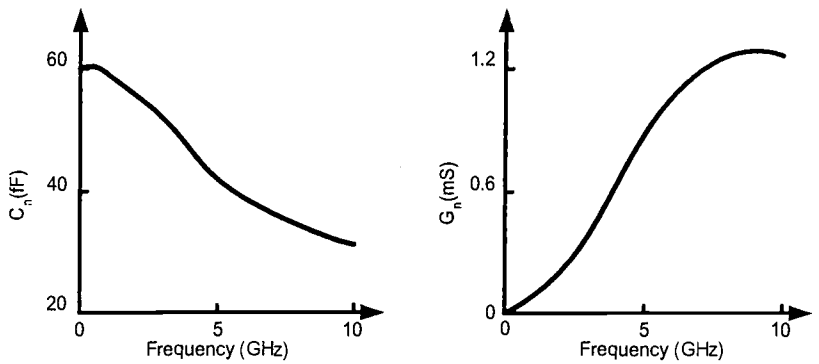


FIGURE 3.9. Capacitive (left) and conductive (right) trends of the $C-GC$ circuit topology.

3.3.3. Capacitance Separation

The third term defined in equation (3.4) is a capacitance matrix, which represents electrical coupling in the oxide layer of the transformer structure. It is tightly coupled with the second term of the equation, which represents magnetic coupling of the transformer. Therefore, its values could be determined if the following assumptions are made: first of all, it is assumed that the electrical coupling in this layer is purely capacitive, meaning that only imaginary parts of matrix elements exist. This is a valid assumption because the silicon dioxide (SiO_2) layer is a good insulator having high breakdown voltage [59]. Another assumption is that the capacitance values are positive and constant with frequency.

Naming the second term in equation (3.4) as $[Y_{FDT}]$, the analysis of the last two terms of (3.4) reveals that when the capacitance matrix is properly extracted, the following relations should be satisfied:

$$Y'_{11} = Y_{FDT_{11}} = Y_{FDT_{33}} = -Y_{FDT_{13}},$$

$$Y'_{22} = Y_{FDT_{22}} = Y_{FDT_{44}} = -Y_{FDT_{34}}, \text{ and}$$
$$Y'_{12} = Y_{FDT_{12}} = -Y_{FDT_{14}} = -Y_{FDT_{23}} = Y_{FDT_{34}}. \tag{3.8}$$

Finally, the assumptions made together with the relationship described by equations (3.8) predetermine the possible range for each of the C_{1-2}, C_{1-4}, C_{2-3}, C_{3-4}, C_{1-3}, and C_{2-4} elements. Then, each set of capacitance values is tried, and the RMS error between the parameters of the FDT admittance matrix (3.8) can be recorded. Finally, the set of C_{1-2}, C_{1-4}, C_{2-3}, C_{3-4}, C_{1-3}, and C_{2-4} elements that produces the smallest RMS error is selected as the capacitance matrix of the network. Then, the third term in equation (3.4), the frequency dependent transformer ($[Y_{FDT}]$) matrix, can be separated from the rest of the data.

3.3.4. FDT cell Extraction

Once the primed values of the second term in equation (3.4) are determined, the impedance matrix of the FDT cell ($[Z_{FDT}]$) is found by simple matrix inversion:

$$Z_{FDT} = \begin{bmatrix} Y'_{11} & Y'_{12} \\ Y'_{12} & Y'_{22} \end{bmatrix}^{-1} = \begin{bmatrix} Z'_{11} & Z'_{12} \\ Z'_{12} & Z'_{22} \end{bmatrix}$$
$$= \begin{bmatrix} R_1(\omega) + j\omega L_1(\omega) & -(R_m(\omega) + j\omega L_m(\omega)) \\ -(R_m(\omega) + j\omega L_m(\omega)) & R_2(\omega) + j\omega L_2(\omega) \end{bmatrix}. \tag{3.9}$$

Matrix ($[Z_{FDT}]$) determined by equation (3.9) represents the impedance matrix of the FDT cell defined in Fig. 3.6 when ports 3 and 4 are shorted to ground. Each element of this matrix exhibits specific impedance trends of the transformer's windings under the presence of conductor losses, such as increasing resistive and decreasing inductive values as the frequency of operation increases. These impedance

functions are synthesized with ideal lumped elements, as shown in Fig. 3.7. The impedance of each element of the Z_{FDT} matrix is then expressed as

$$\begin{aligned} Z'_{11} &= R_1 + j\omega L_1 - \frac{M_{p1}^2(j\omega)^2}{R_{p1} + j\omega L_{p1}}, \\ Z'_{22} &= R_2 + j\omega L_2 - \frac{M_{s1}^2(j\omega)^2}{R_{s1} + j\omega L_{s1}}, \text{ and} \\ Z'_{12} &= -j\omega L_m + \frac{M_{m1}^2(j\omega)^2}{R_{m1} + j\omega L_{m1}}. \end{aligned} \tag{3.10}$$

Finally, the self resistances of the spirals (R_1 and R_2) are extracted from the low frequency asymptote of the series impedance data, and the remaining terms are determined using the Cauchy method described in [27].

3.4. Conclusion

A new frequency-dependent transformer (FDT) modeling approach has been presented. The new model effectively captures conductor losses in the transformer windings including the frequency-dependent mutual resistance and inductance. An extraction procedure that determines the topology and lumped-element circuit values from S-parameter data obtained by measurements or EM-simulation has also been described. The presented monolithic transformer model is compact and consists solely of frequency-independent lumped circuit elements, making it a perfect candidate for time- and frequency-domain circuit simulations.

4. RESULTS

4.1. Introduction

To verify the wide-band capabilities of the presented model, the results for several monolithic transformer models are shown in this chapter. The transformers tested include both stacked and interleaved topologies; they have different inductance ratios and are fabricated on a 10 Ω·cm CMOS substrate. Table 4.1 summarizes important geometrical dimensions of the devices under test (DUT). The four-port S-parameter data were obtained with the 3-D electromagnetic full-wave simulator HFSS by Ansoft [47] after calibration with two-port measurement data provided by National Semiconductor Corporation [60]. The models for stacked transformers are compared with available measurement data as well.

Transformer	Type	Shape	Inductance Ratio (*Primary* : *Secondary*)
A	Stacked	Square	3:1
B	Stacked	Square	4:1
C	Stacked	Square	4:2
D	Interleaved	Square	1:1
E	Interleaved	Octagonal	1:1
F	Interleaved	Square	4:5

TABLE 4.1. Monolithic transformers used to test the new transformer model. The inductance ratios are approximate.

4.2. Monolithic Transformer Characteristics

To analyze the overall model performance, a transformer configuration of the circuit shown in Fig. 3.7 with ports 3 and 4 grounded was used. The resulting two-port impedance matrix was analyzed using the following commonly used quantities to evaluate model performance. In the formulas shown below $\omega = 2\pi f$, where f is the frequency of operation in Hertz (Hz).

Self inductances (L_{11}, L_{22}) and resistances (R_{11}, R_{22}) of the primary and the secondary spirals are respectively:

$$\mathrm{L_{11}} = \frac{\mathrm{Im(Z_{11})}}{\omega}, \quad \mathrm{L_{22}} = \frac{\mathrm{Im(Z_{22})}}{\omega}, \quad \mathrm{R_{11}} = \mathrm{Re(Z_{11})}, \quad \mathrm{R_{22}} = \mathrm{Re(Z_{22})}. \tag{4.1}$$

The input quality factors are the overall performance measures of the monolithic inductors and transformers. In monolithic transformers the input quality factors for primary (Q_{11}) and the secondary (Q_{22}) spirals are measured with the other coil left open [49]. They are given in terms of the Z-parameters as

$$\mathrm{Q_{11}} = \frac{\mathrm{Im(Z_{11})}}{\mathrm{Re(Z_{11})}}, \quad \mathrm{Q_{22}} = \frac{\mathrm{Im(Z_{22})}}{\mathrm{Re(Z_{22})}}. \tag{4.2}$$

The mutual resistive (k_{Re}) and mutual reactive (k_{Im}) coupling factors are given by equations (4.3). The k_{Im} coupling factor is a function of frequency due to the parasitic capacitances in the transformer windings. At DC it equals the mutual magnetic coupling factor and then deviates from it as frequency increases [49]. The k_{Re} coupling factor approaches zero value at DC, and it increases with increasing operational frequency reaching its maximum at SRF.

$$\mathrm{k_{Re}} = \sqrt{\frac{[\mathrm{Re(Z_{12})}]^2}{\mathrm{Re(Z_{11})Re(Z_{22})}}}, \quad \mathrm{k_{Im}} = \sqrt{\frac{[\mathrm{Im(Z_{12})}]^2}{\mathrm{Im(Z_{11})Im(Z_{22})}}}. \tag{4.3}$$

Maximum available gain (Gm_{max}) is used as an intrinsic figure of merit for passive RF components independent of termination impedances [31, 61]. Equa-

tion (4.4) expresses Gm_{max} in terms of the input quality factors of the coils, as well as the reactive and resistive mutual factors defined by (4.3).

$$\mathrm{Gm_{max}} = \mathrm{x} - \sqrt{\mathrm{x}^2 - 1}, \quad \mathrm{x} = \frac{1 + 2(1 - \mathrm{k}_{\mathrm{Re}}^2)}{\mathrm{k}_{\mathrm{Re}}^2 + \mathrm{k}_{\mathrm{Im}}^2 \mathrm{Q}_{11}\mathrm{Q}_{22}}. \tag{4.4}$$

The transformer turns ratio, n, is defined by the equation below.

$$\mathrm{n} = \sqrt{\frac{\mathrm{L}_{11}}{\mathrm{L}_{22}}}. \tag{4.5}$$

4.3. Stacked Transformers

The stacked transformers considered in this section have the general topology shown in Figure 4.1. The different inductance ratios were achieved by varying the number of turns of each spiral. The monolithic transformers were fabricated in a BiCMOS process with substrate conductivity of approximately 10 Ω·cm; the dielectric layer is formed by silicon dioxide. The outer diameter of the transformer is 180 μm. The primary spiral is located in the upper, "thick," metallization layer which helps to reduce the series resistance of the spiral. The individual turns of the spirals are connected using underpasses that are fabricated in the next metal layer below each respective spiral. This configuration requires four metal layers to implement the transformer.

The figures in this section present three data sets: EM Simulation, Circuit Model, and Measurement. The Measurement data set was used to calibrate the EM-simulator by changing the physical properties of the dielectric material and the metal layer conductivities to match the self-resonant frequency (SRF). Then the four-port EM Simulation data was used to extract the circuit element values for the new model. The extracted values for the circuit elements are listed in Table 4.2.

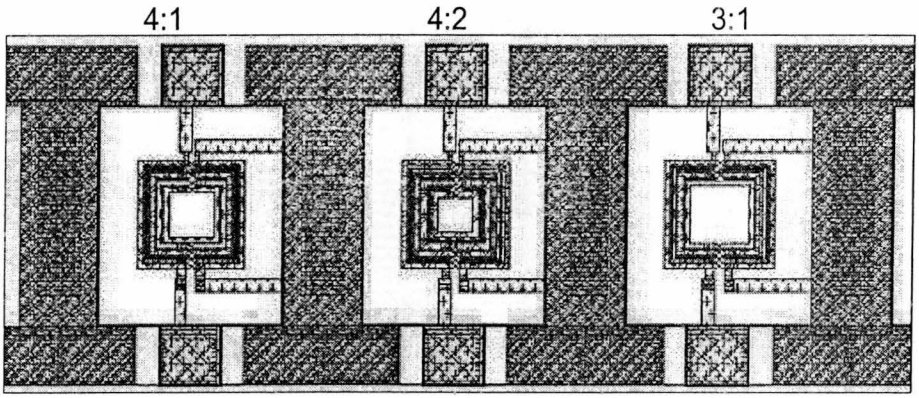


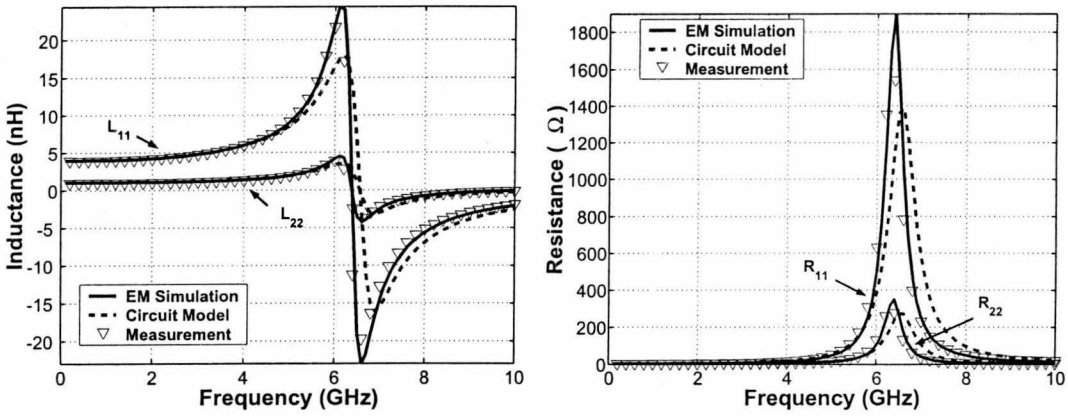
FIGURE 4.1. Stacked transformers fabrication layout. The numbers on top indicate approximate inductance ratios.

The graphs in this chapter are presented for Transformer B, and the graphs for Transformer A and Transformer C are presented in Appendix A.

The self inductances and resistances defined by equation (4.1) are shown in Fig. 4.2. The compact model data indicates excellent correlation with both measured and EM simulated data sets up to the SRF value. The results are also displayed in the vicinity of the SRF because this parameter defines a frequency point where the transformer's self inductances change to the capacitive behavior making the transformer impractical after this frequency. The SRF, therefore can be considered as an important figure of merit of the monolithic transformers [15].

The corresponding input quality factor defined by equation (4.2) and the turns ratio defined by equation (4.5) are shown in Fig. 4.3. It can be observed that the modeled data captures the measured and simulated trends very well up to the SRF. The slight deviation between the measured and EM simulated input quality factors can be explained by the imperfections in the HFSS vs. measurement calibration procedure. The model accuracy in terms of quality factors can be improved

if general optimization in the circuit parameters were used. The plot of turns ratio also indicates that the circuit model is able to provide excellent agreement up to the SRF.

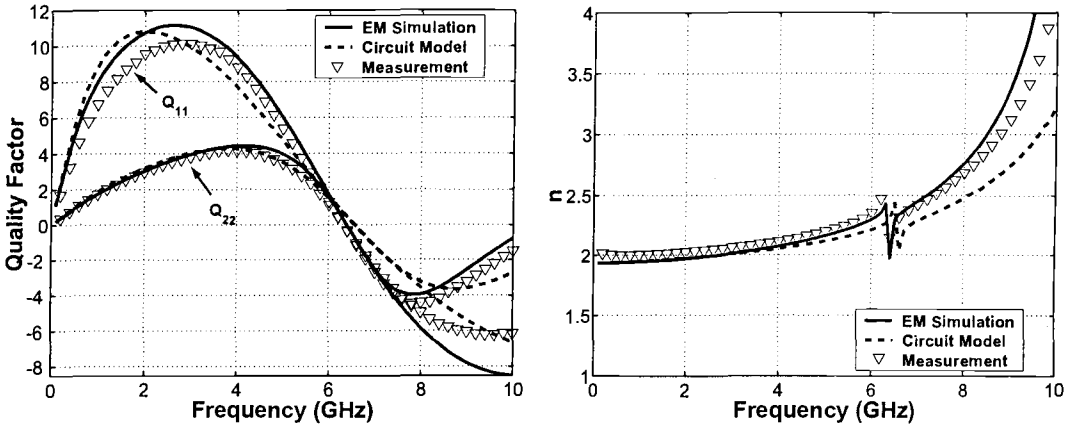


(a) (b)

FIGURE 4.2. Frequency-dependent series self-impedance parameters of Transformer B with 4:1 inductance ratio. (a) Self inductances of the primary (L_{11}) and the secondary (L_{22}) spirals. (b) Self resistances of the primary (R_{11}) and the secondary (R_{22}) spirals.

TABLE 4.2. Extracted equivalent circuit parameters for stacked transformers

Circuit Parameters	Transformers A	B	C	Circuit Parameters	Transformers A	B	C
Primary				*Mutual Capacitance*			
R_1 (Ω)	1.80	2.09	2.33	C_{12} (fF)	39.5	47.0	55.8
L_1 (nH)	3.19	3.96	3.95	C_{14} (fF)	44.1	35.2	63.2
R_{p1} (Ω)	16533	15861	17460	C_{32} (fF)	46.4	36.5	62.3
L_{p1} (μH)	1.0	1.0	1.0	C_{34} (fF)	37.0	45.4	50.1
M_{p1} (nH)	15.6	16.8	21.3	*Interwinding Capacitance*			
Secondary				C_{13} (fF)	0.0	5.98	0.0
R_2 (Ω)	3.27	3.21	6.30	C_{24} (fF)	0.0	0.0	0.0
L_2 (nH)	1.05	1.06	2.17	*Shunt Admitances*			
R_{s1} (Ω)	14839	13553	17541	C_{ox1} (fF)	19.9	24.5	11.7
L_{s1} (μH)	1.0	1.0	1.0	C_{sub1} (fF)	18.9	18.1	24.8
M_{s1} (nH)	10.1	10.2	14.8	R_{sub1} (Ω)	1306	1182	2109
Mutual				C_{ox2} (fF)	82.0	80.2	114
L_m (nH)	1.33	1.46	2.26	C_{sub2} (fF)	27.6	26.2	28.8
R_{m1} (Ω)	13553	11377	15719	R_{sub2} (Ω)	367	391	323
L_{m1} (μH)	1.0	1.0	1.0	C_{ox3} (fF)	19.6	24	11.2
M_{m1} (nH)	9.95	10.3	14.9	C_{sub3} (fF)	18.8	17.9	23.7
				R_{sub3} (Ω)	1370	1214	2295
				C_{ox4} (fF)	81.4	79.8	115
				C_{sub4} (fF)	27.3	26.1	29.1
				R_{sub4} (Ω)	374	396	327



(a) (b)

FIGURE 4.3. Results for a stacked transformer B with 4:1 inductance ratio. (a) Quality factors for primary (Q_{11}) and secondary (Q_{22}) spirals. (b) Turns ratio.

The final set of characteristics, consisting of maximum available gain (Gm_{max}), the mutual resistive (k_{Re}) and mutual reactive (k_{Im}) coupling coefficients, is shown in Fig. 4.4. Again, excellent agreement between the circuit model and EM Simulation/Measurement data sets is achieved. Figure 4.4 shows the plot of k_{Re} (dotted line) of the model when the frequency-dependence in the mutual inductance and resistance is neglected in the transformer model (case with $R_m = 0$ and constant L_m). The plot indicates that k_{Re} term is clearly underestimated at a frequency of operation of, for example, 2.4 GHz.

4.4. Interleaved Transformers

The interleaved transformers considered in this section have the general topology shown in Fig. 1.2. These transformers have approximately the same inductance ratios and were designed for a BiCMOS process with substrate conductivity

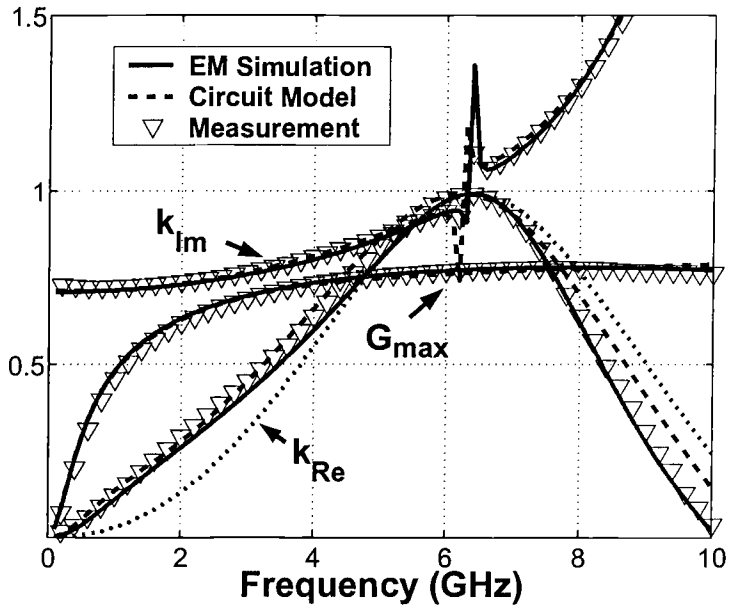
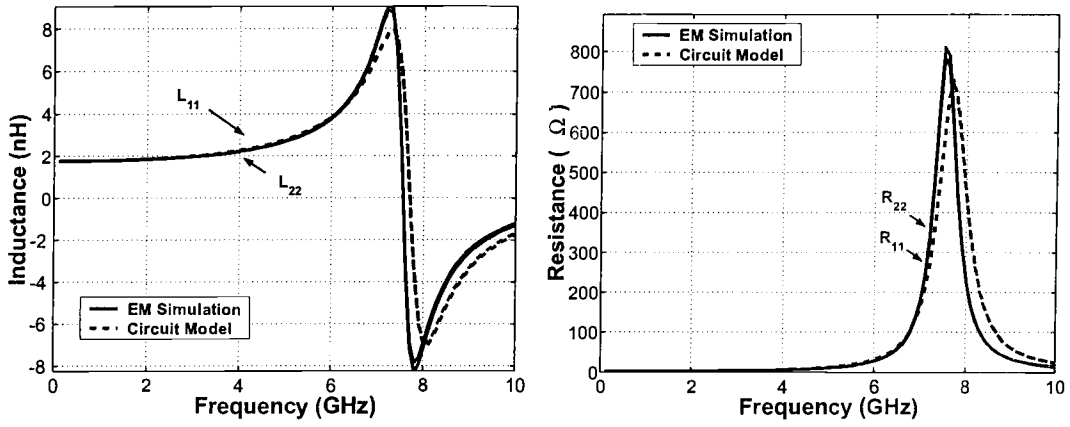


FIGURE 4.4. Maximum available gain (Gm_{max}), real (k_{Re}) and imaginary (k_{Im}) coupling coefficients of a transformer B with 4:1 inductance ratio. The dotted line represents k_{Re} for the case with $R_m = 0$ and constant L_m.

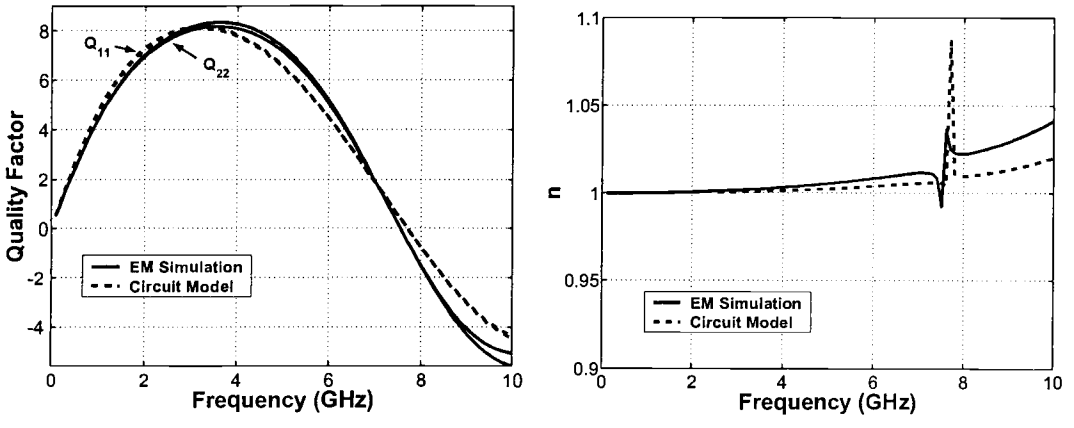
of 10Ω·cm; the dielectric layer is formed by silicon dioxide. Both primary and secondary spirals are located in the upper, "thick" metallization layer which helps to reduce the series resistance of the spirals. The individual turns of the spirals are connected using underpasses in the metal layer below the spirals. The transformers' outer diameters (OD) vary from 160 μm to 250 μm. Table 4.3 shows the circuit element values for the three transformers. The results for Transformer D are shown in this section in Figs. 4.5-4.7, whereas the results for Transformer E and Transformer F are shown in Appendix A.

The circuit model extracted for interleaved transformers indicates a good correlation with full-wave simulation data up to SRF for all investigated characteristics. Therefore, the presented model and developed extraction procedure are



(a) (b)

FIGURE 4.5. Frequency-dependent series self-impedance parameters of square transformer D with OD = 160 μm. (a) Self inductances of the primary (L_{11}) and the secondary (L_{22}) spirals, and (b) Self resistances of the primary (R_{11}) and the secondary (R_{22}) spirals.



(a) (b)

FIGURE 4.6. Results for an interleaved transformer D with OD = 160 μm. (a) Quality factors for primary (Q_{11}) and secondary (Q_{22}) spirals. (b) Turns ratio.

robust and able to represent the behavior of interleaved monolithic transformers in circuit simulators.

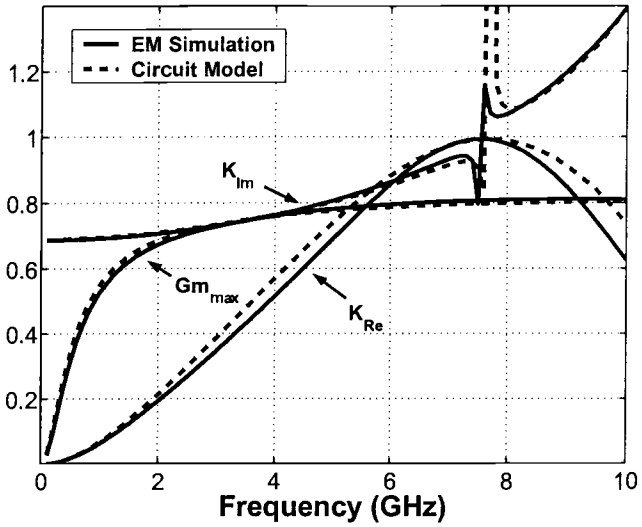


FIGURE 4.7. Maximum available gain (Gm_{max}), real (k_{Re}) and imaginary (k_{Im}) coupling coefficients of a transformer D with OD = 160 μm.

4.5. Conclusion

The results for several examples of monolithic transformers on silicon substrates have been presented. The analyzed transformer characteristics indicate a good correlation between the extracted circuit models and EM simulated or measured data sets. The compact model consists entirely of ideal lumped circuit elements and is capable of capturing major loss mechanisms in monolithic transformers over a wide frequency range from DC up to the self-resonant frequency.

TABLE 4.3. Extracted equivalent circuit parameters for interleaved transformers

Circuit Parameters	Transformers D	E	F	Circuit Parameters	Transformers D	E	F
Primary				*Mutual Capacitance*			
R_1 (Ω)	2.11	2.81	2.78	C_{12} (fF)	3.54	23.8	46.5
L_1 (nH)	1.77	2.97	3.69	C_{14} (fF)	128	140	409
R_{p1} (Ω)	22794	12799	14248	C_{32} (fF)	127	148	430
L_{p1} (μH)	1.0	1.0	1.0	C_{34} (fF)	3.69	25.6	40.3
M_{p1} (nH)	12.0	10.8	21.6	*Interwinding Capacitance*			
Secondary				C_{13} (fF)	0.0	0.0	0.0
R_2 (Ω)	2.09	2.68	6.30	C_{24} (fF)	0.0	0.0	0.0
L_2 (nH)	1.77	2.71	2.17	*Shunt Admitances*			
R_{s1} (Ω)	22688	13406	13272	C_{ox1} (fF)	28.5	45.0	51.1
L_{s1} (μH)	1.0	1.0	1.0	C_{sub1} (fF)	30.4	38.3	26.9
M_{s1} (nH)	11.9	10.1	20.3	R_{sub1} (Ω)	472	321	626
Mutual				C_{ox2} (fF)	24.9	36.6	81.5
L_m (nH)	1.22	2.32	3.51	C_{sub2} (fF)	14.3	21.9	31.1
R_{m1} (Ω)	28079	19413	14580	R_{sub2} (Ω)	754	537	306
L_{m1} (μH)	1.0	1.0	1.0	C_{ox3} (fF)	25.0	44.5	54.9
M_{m1} (nH)	9.25	7.4	18.4	C_{sub3} (fF)	14.4	38.1	27.0
				R_{sub3} (Ω)	1370	745	649
				C_{ox4} (fF)	28.4	36.9	81.9
				C_{sub4} (fF)	30.4	21.81	33.2
				R_{sub4} (Ω)	465	550	309

5. CONCLUSIONS AND FUTURE WORK

5.1. Conclusions

A new wide-band compact model for monolithic transformers fabricated on lossy silicon substrates has been presented. The model consists of a newly developed frequency-dependent transformer (FDT) cell in its core to model frequency-dependent conductor losses including mutual resistance. The wide-band accuracy of the FDT cell model is accomplished through the use of "transformer-loops" to model both self and mutual frequency-dependent inductances and resistances. Substrate loss and interwinding capacitance are modeled as well. The new compact model is useful for frequency- and time-domain simulations in any SPICE-compatible circuit simulation software.

A robust, automated extraction technique is also presented. It determines the values of the ideal circuit elements used in the transformer model from measurement or EM simulation S-parameter data. The extraction process includes two major parts: solution for network branches, and determining the circuit elements values using Cauchy's method based on a least-square fitting technique. Together, the new transformer model and extraction procedure provide a complete measurement-based modeling methodology for four-port monolithic transformers fabricated on silicon-based substrates that enables automated model generation within minutes.

To verify the accuracy of the proposed transformer modeling methodology, both stacked and interleaved monolithic transformers were considered. Wide-band compact models were extracted for stacked and interleaved transformers from full-wave EM simulation data. Good agreement between the circuit model and EM simulation data was demonstrated up to the self-resonant frequency of the devices.

The new measurement-based modeling methodology for monolithic transformers will benefit RF and mixed-signal integrated circuit designers by providing a robust accurate transformer model that consists entirely of ideal circuit elements.

5.2. Future Work

The future work of this research mainly lies in the area of extending the modeling methodology to include other transformer structures such as baluns. These devices have more ports than a regular four-port transformer and include additional center taps that are used to provide ground terminations to the middle points of the spirals.

While the core of the model would still be the FDT cell, other elements such as center taps will need to be modeled. The difficulty of such modeling could arise from the fact that the center taps are electrically and magnetically coupled to the transformer's spirals, and separation of these effects from the overall transformer performance may prove to be challenging. To overcome this difficulty, two approaches are suggested: selective de-embedding of center tap effects from the overall transformer data or approximating the effects of the center taps and then subtracting them from the measured data.

Since more than four-port S-parameter data is not readily available and usually is obtained by combining the data from multiple two- or four-port measurements with a Vector Network Analyzer (VNA), full-wave EM-simulations might be useful in providing a first approximation of the circuit element values. Once a good approximation is achieved, the final circuit values could be optimized using measured data.

Another area that needs to be investigated in regard to multiple port measurements and center tap de-embedding is the time-domain network analysis (TDNA) [62], which allows one to determine frequency-domain S-parameter data from time-domain measurements. Moreover, the time-domain data may allow selective de-embedding similar to the gating function of regular VNAs. The more direct benefit of the TDNA method is that some recent time-domain instruments, such as the Tektronix TDS8200, allow measurement of up to eight ports, as well as true differential signaling.

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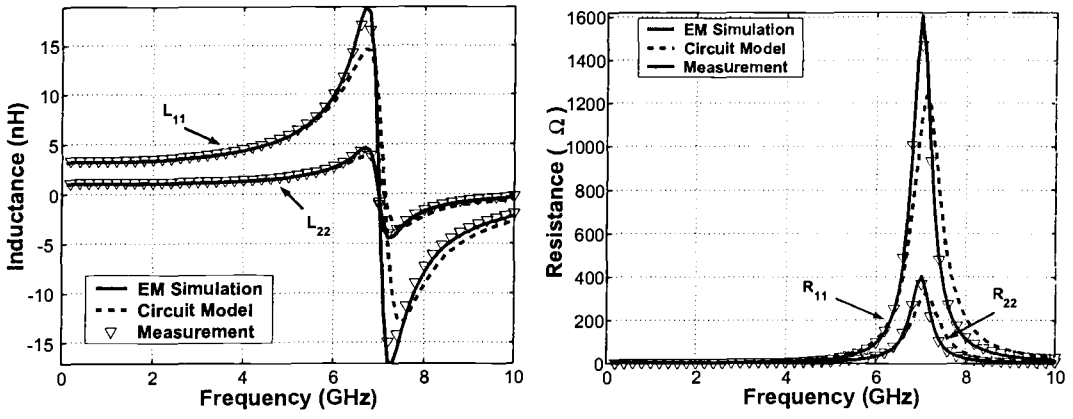
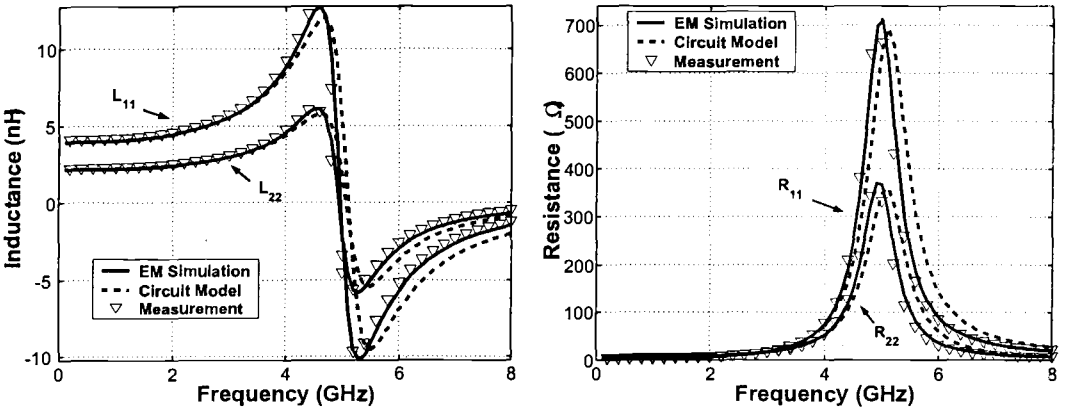
APPENDICES

APPENDIX A. Extraction Results

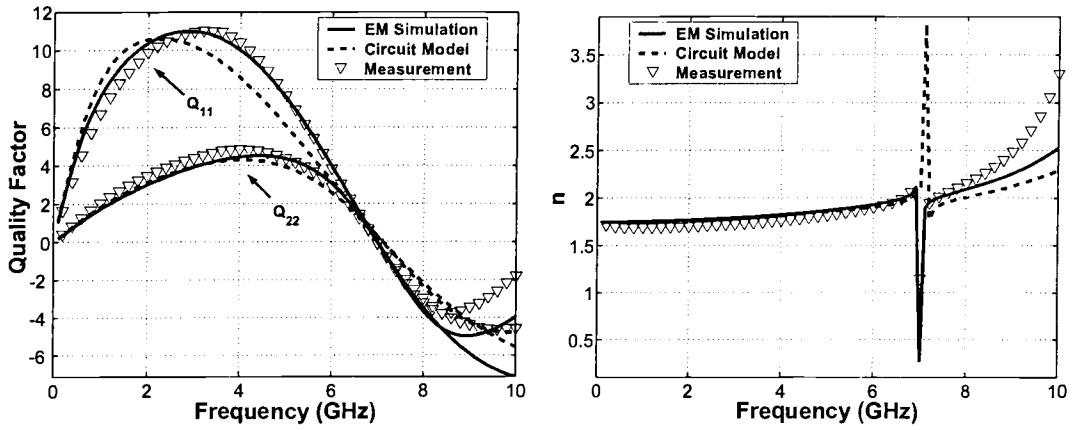


(a)

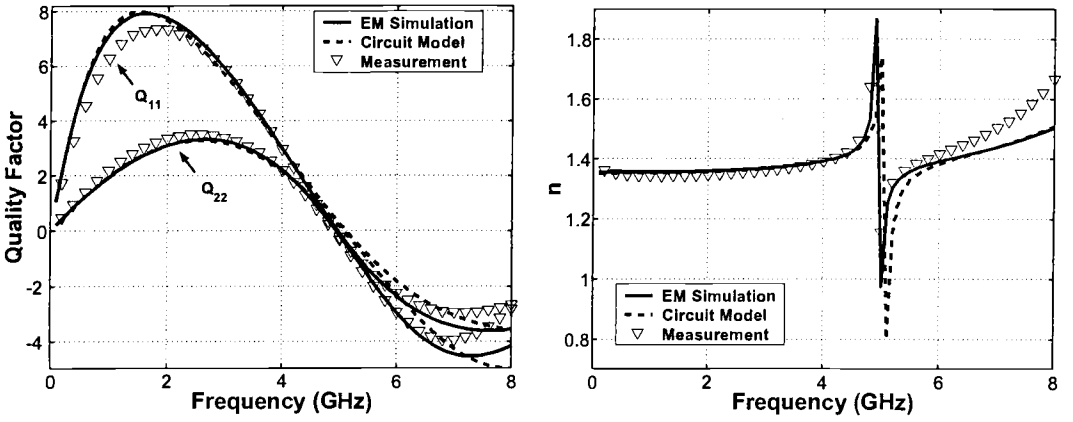


(b)

FIGURE A.1. Frequency-dependent series self-impedance parameters of the stacked transformers. (a) Transformer A with 3:1 inductance ratio. (b) Transformer C with 4:2 inductance ratio.

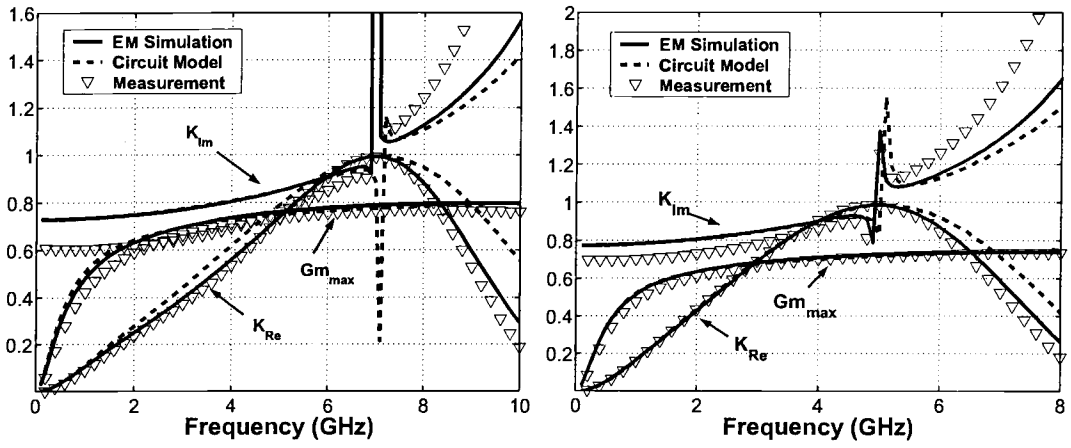


(a)



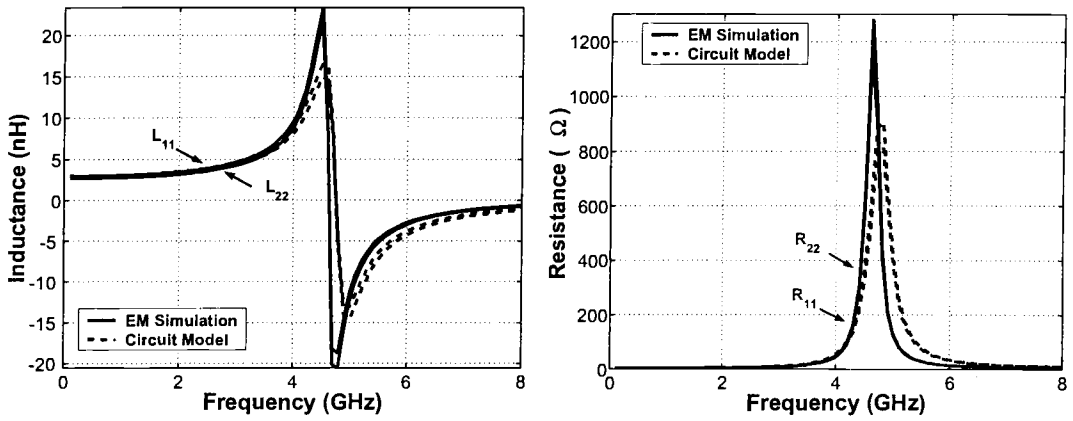
(b)

FIGURE A.2. Quality factors for primary (Q_{11}) and secondary (Q_{22}) spirals and turns ratio for stacked transformers. (a) Transformer A with 3:1 inductance ratio. (b) Transformer C with 4:2 inductance ratio.

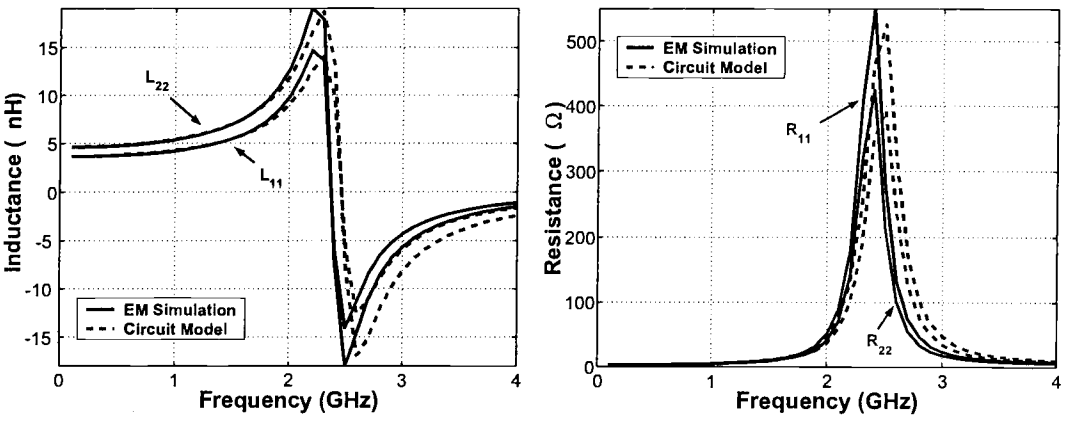


(a) (b)

FIGURE A.3. Maximum available gain (Gm_{max}), real (k_{Re}) and imaginary (k_{Im}) coupling coefficients. (a) Transformer A with 3:1 inductance ratio. (b) Transformer C with 4:2 inductance ratio.

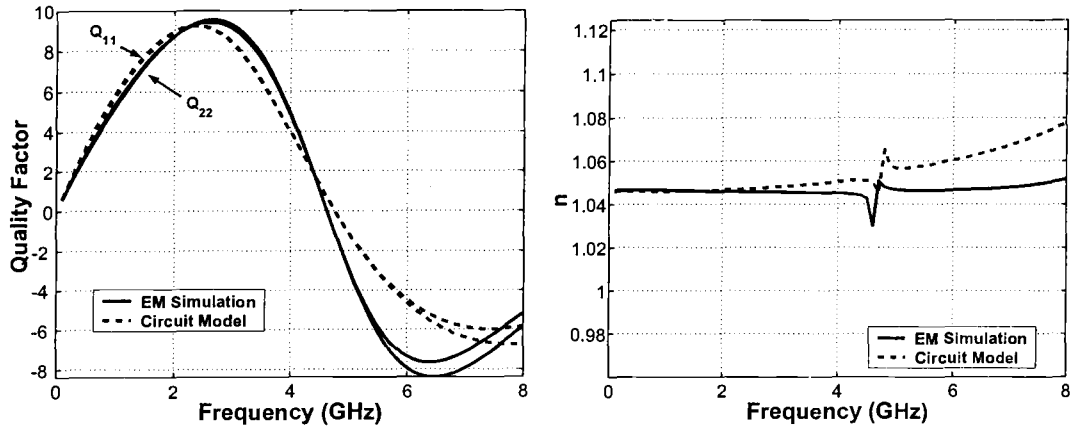


(a)

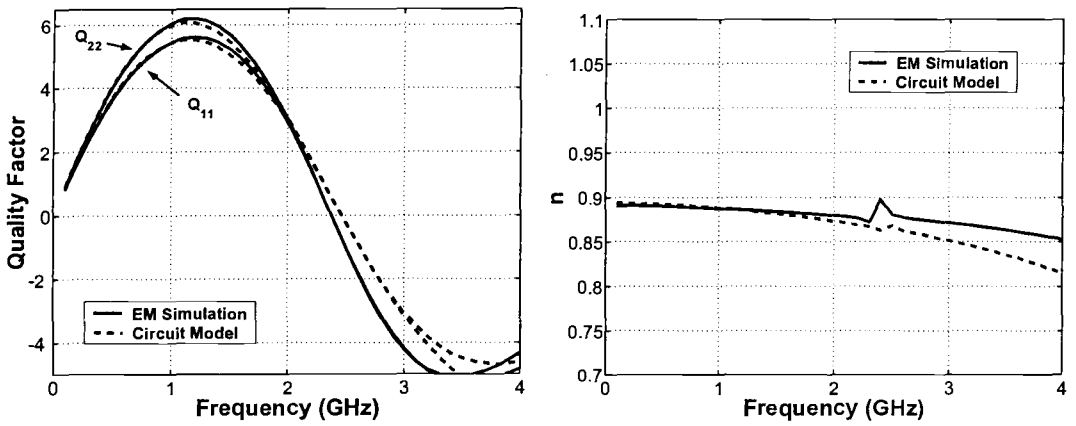


(b)

FIGURE A.4. Frequency-dependent series self-impedance parameters of the interleaved transformers. (a) Transformer E with OD = 250 μm (octagonal shape). (b) Transformer F with OD = 250 μm (square shape).

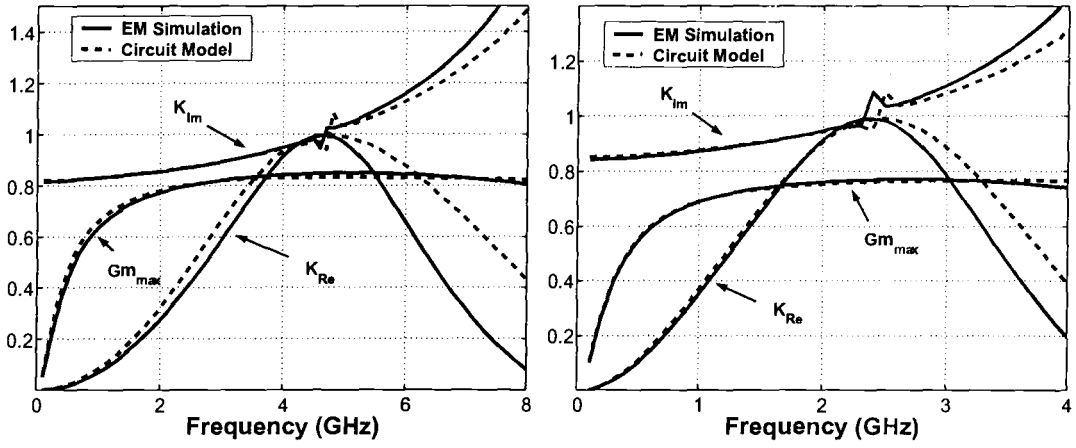


(a)



(b)

FIGURE A.5. Quality factors for primary (Q_{11}) and secondary (Q_{22}) spirals and turns ratio for interleaved transformers. (a) Transformer E with OD = 250 μm (octagonal shape). (b) Transformer F with OD = 250 μm (square shape).



(a) (b)

FIGURE A.6. Maximum available gain (Gm_{max}), real (k_{Re}) and imaginary (k_{Im}) coupling coefficients. (a) Transformer E with OD = 250 μm (octagonal shape). (b) Transformer F with OD = 250 μm (square shape).