AN ABSTRACT OF THE THESIS OF

Aline C. Sadate for the degree of Master of Science in

Electrical and Computer Engineering presented on December 8, 2000.

Title: A Substrate Noise Coupling Model for Lightly Doped CMOS Processes

Abstract approved: Kartikeya Mayaram Terri S. Fiez

This thesis presents a design-oriented model for lightly doped CMOS substrates. The model predicts the substrate noise coupling between noisy digital and sensitive analog blocks in the early stages of the design. The model scales with the size and separation of these blocks and it is validated with device simulations and with measurements on two different test chips. The effectiveness of different isolation techniques is investigated for lightly doped CMOS processes using device simulations and it is shown that P+ guard rings offer the best isolation, supppressing the noise by as much as 45dB when the guard rings are within a few microns of the noise injector. Finally, the model is used to predict noise coupling between an inverter and an amplifier, with both circuit simulations and measurements on a chip fabricated in the TSMC 0.35μm CMOS process.

A Substrate Noise Coupling Model for Lightly Doped CMOS Processes

by

Aline C. Sadate

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APPROVED:

Co-Major Professor, representing Electrical and Computer Engineering

Co-Major Professor, representing Electrical and Computer Engineering

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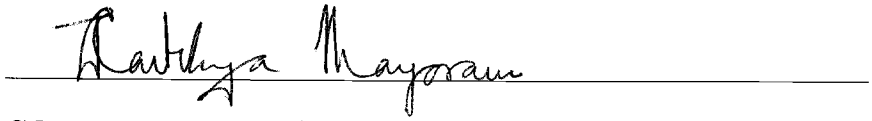

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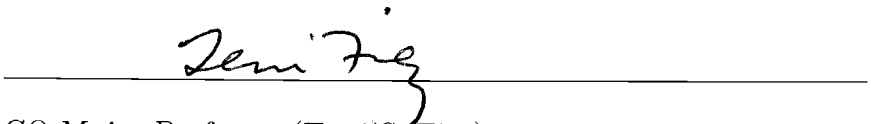

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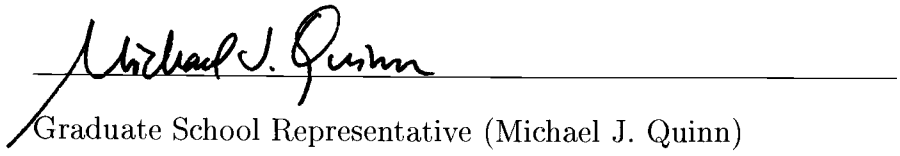

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF TABLES

A SUBSTRATE NOISE COUPLING MODEL FOR LIGHTLY DOPED CMOS PROCESSES

1. INTRODUCTION

Integrating RF, analog, and digital components on the same chip gives rise to many new challenges. One of these challenges involves noise coupling from the digital components to their analog counterparts through the common silicon substrate. In order to avoid the degradation in the circuit performance that results from substrate noise, designers rely on different isolation techniques without knowing their effectiveness. These isolation techniques include the use of guard rings, Nwells or separation between the noisy and the quiet circuit blocks [1]. Although some of these techniques can be effective, there is currently no method for quantitatively predicting the improvement in the signal-to-noise performance. In order to avoid large area penalties during the layout when applying these isolation techniques, a model that can quantify the isolation is required.

The increasing importance of substrate noise coupling in IC's has resulted in many studies on this topic. Many methods of analysis of substrate coupling as well as models for the substrate have been developed [1-17]. Although some of these studies have been done on lightly doped substrates [2,18], most of the work has focused on heavily doped substrates. One of the main drawbacks of lightly doped substrates has been latch-up related issues. However these issues are minimized

as power supplies are scaled down. Also, studies have shown that lightly doped substrates may suppress the noise better than heavily doped substrates [19]. Furthermore, lightly doped CMOS substrates are very cost efficient, which makes them attractive to industry. This motivates the need for investigating substrate models for lightly doped processes.

In [3], a scalable design-oriented macromodel was presented that predicts substrate noise coupling between blocks based on their separation and size. This macromodel makes it possible for designers to simulate the effects of substrate noise in their circuits during the design phase. The model was developed for heavily doped substrates. In this paper, a similar model is developed for lightly doped CMOS processes. The substrate model derived for point and scaled contacts is presented in Section I. Applications of the model are presented in Section II and the conclusions are provided in Section III.

2. SUBSTRATE MODEL

In order to derive the model, 2D simulations were performed using MEDICI [20]. MEDICI generates current flow lines and Y or Z parameters from process information including doping concentrations and layer thicknesses. To illustrate the derivation of the model, the cross section of the process shown in Figure 2.1 is used. The cross section shows two distinct layers: a P+ channel-stop implant which is heavily doped and which has a resistivity of $15m\Omega$-cm; and a uniform lightly doped substrate which has a resistivity of 20Ω-cm [6]. A substrate thickness of 150μm is used, instead of 675μm as specified by the process information, because the simulator can handle only a limited number of grid points.

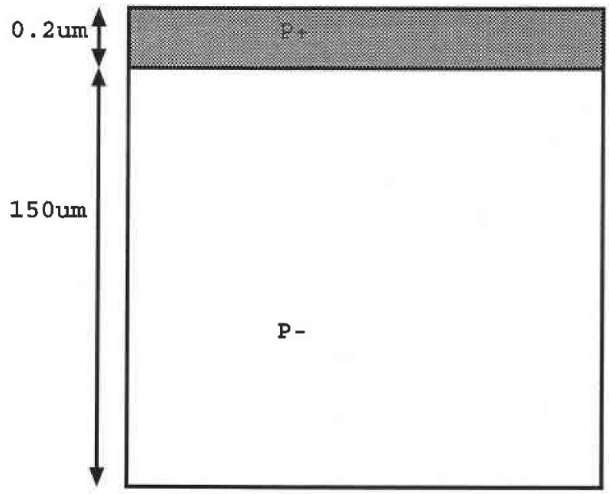


FIGURE 2.1.: Cross section of lightly doped substrate.

2.1. Point-to-Point Contact Model

To derive the model for two point contacts, the setup used for the simulations is given in Figure 2.2. A unit voltage is applied to an injector contact from which a sensor is placed at a distance that can be varied. The distance is considered to be from the inner edge of the injector to the inner edge of the sensor. The sensor and the backplane are grounded. From this setup, information about Y-parameters and current flow lines can be obtained. The flow lines are shown in Figures 2.3 (a) and (b) for separations of 10μm and 100μm, respectively. It is observed that almost all of the current flows from the injector to the sensor when these two contacts are close. This behavior can be explained by the presence of the heavily doped channel stop-implant which offers a low resistance path through which the current can flow. As the separation between the two contacts is increased some of the current starts flowing to the backplane. Therefore, it can be concluded that the conductance to

the backplane increases with separation while the cross conductance between the injector and the sensor decreases as the separation increases.

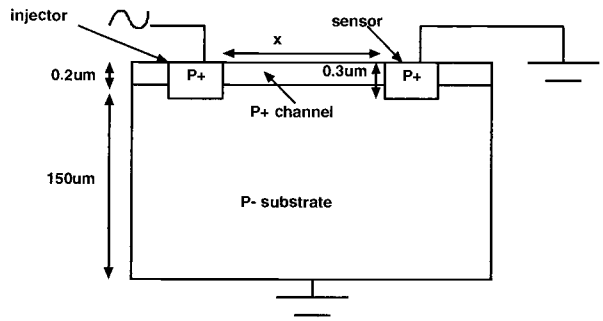
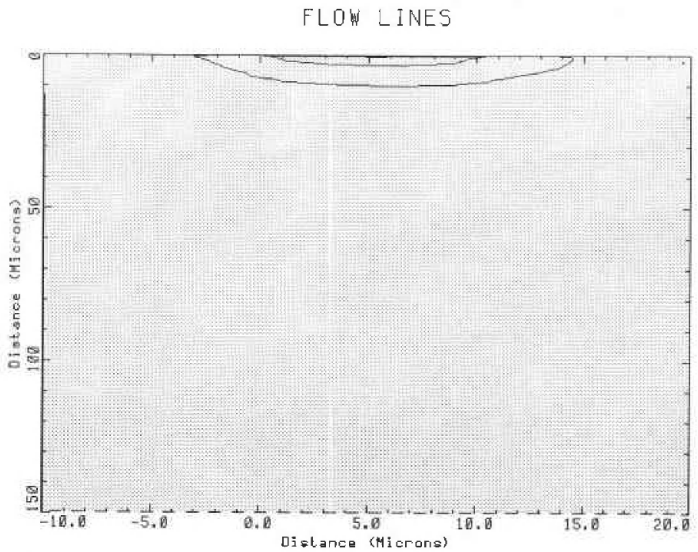
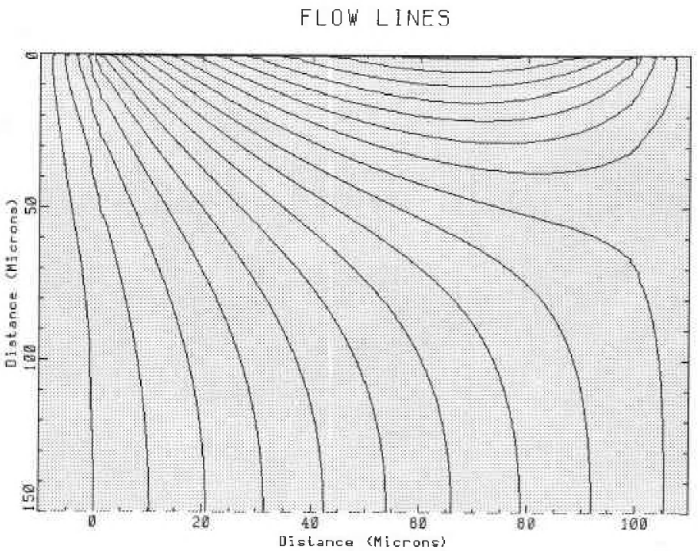


FIGURE 2.2.: MEDICI simulation setup used to determine the substrate coupling between two point contacts in a lightly doped process.

The current flow lines, which show resistive paths from the injector to the backplane and from the injector to the sensor, indicate that the low-frequency substrate model proposed in [3], Figure 2.4, is also valid for lightly doped substrates. G11 (G22) represents the conductance from the injector (sensor) to the backplane while G12 represents the cross conductance from the injector to the sensor. In [21], it was shown that a resistive model for the substrate was only valid up to a certain frequency. In order to determine this frequency of interest for the process used, the conductance (Y-real) and the susceptance (Y-imaginary) were compared, both for Y11 and Y12. Figures 2.5 (a) and (b) show that the conductance is higher in magnitude than the susceptance. For Y12 the difference in magnitude between the imaginary and real parts is significant up to 10GHz but for Y11 the conductance is larger than the susceptance only for frequencies up to 2GHz. Thus, this resistive model is accurate up to about 2GHz.



(a)



(b)

FIGURE 2.3.: Current flow lines in a lightly doped substrate for two different separations between the injector and the sensor: (a) 10μm and (b) 100μm.

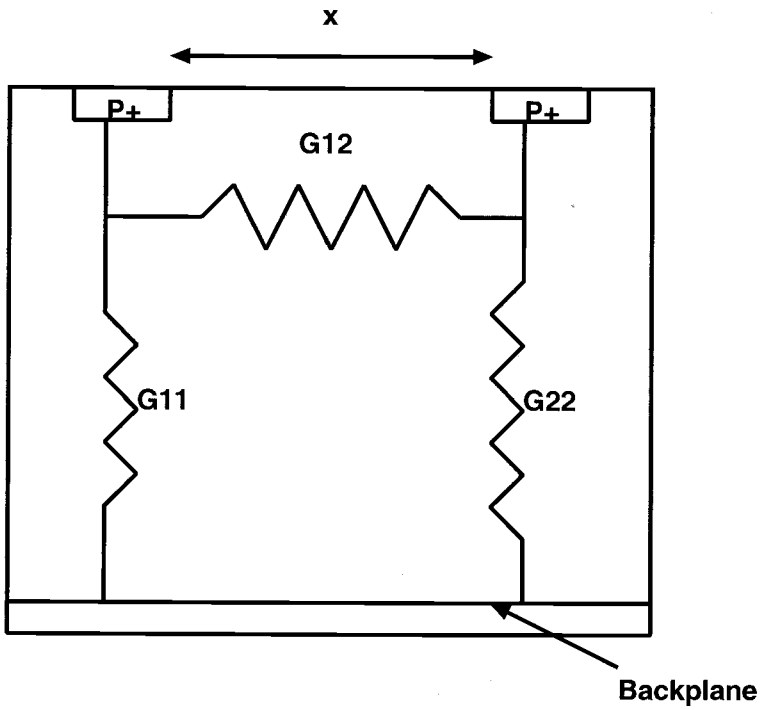
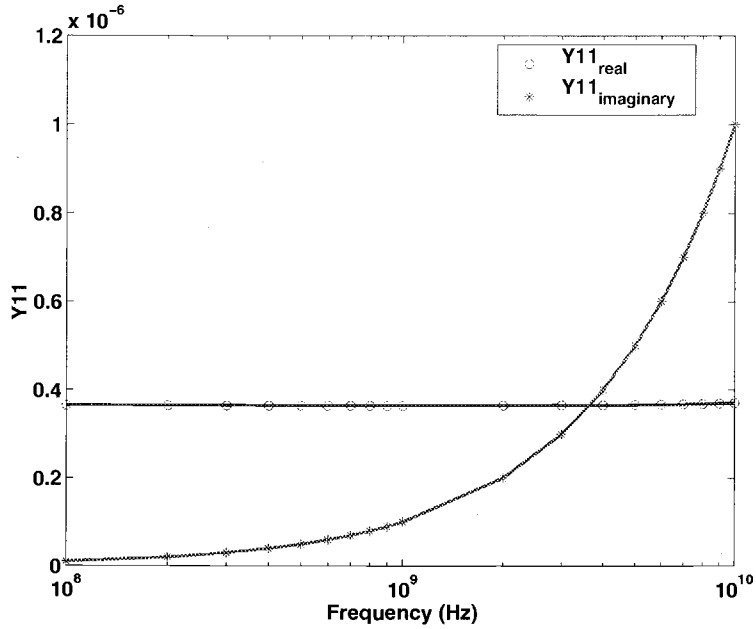
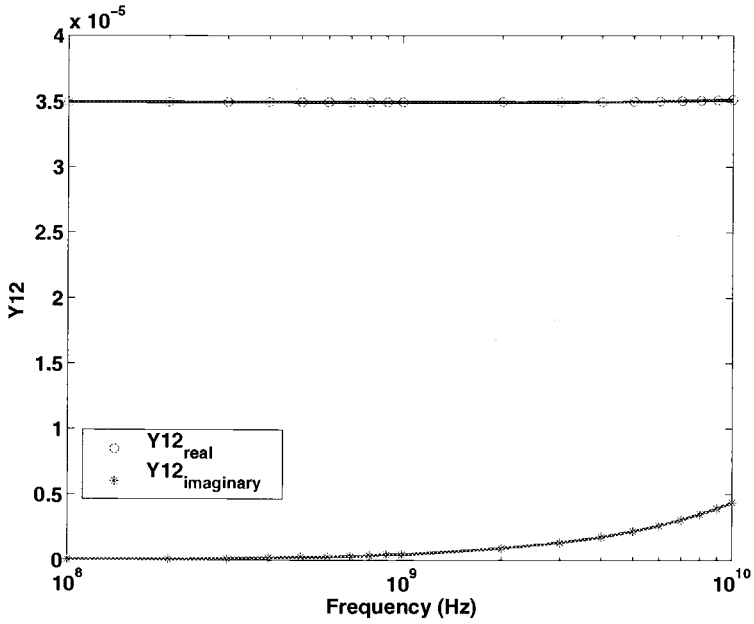


FIGURE 2.4.: Resistive model for lightly doped substrate.



(a)



(b)

FIGURE 2.5.: Y-parameters as a function of frequency: (a) Y11 and (b) Y12. The real part of the Y-parameter is the conductance and the imaginary part is the susceptance.

The data extracted from simulations is used to plot G11 as a function of the separation between the contacts. Figure 2.6 shows that G11 increases linearly with the separation, x. Since MEDICI can handle only a limited number of grid points, it is impossible to simulate large separations for a substrate depth of 150μm. In order to observe the behavior of G11 for larger separations, simulations were done for a 10μm deep substrate. Figure 2.7 is a plot of G11 as a function of the separation, where the separation has been normalized to the substrate thickness. It can be observed that although G11 changes linearly for some separations as observed previously, it saturates at 14 times the depth of the substrate used. Since most processes have a very deep substrate, it is expected that this behavior will not be observed in practice. Therefore a linear model can be assumed for G11, that is:

$$G11(x) = Ax + B \tag{2.1}$$

where A and B are extracted process parameters.

From the simulations, G12 can also be extracted as a function of the separation. A curve fit on the data shows that G12 can be modeled as:

$$G12(x) = \alpha e^{-\beta x^{\kappa}} \tag{2.2}$$

where α, β and κ are process dependent parameters that can be extracted from either device simulations or measurements from test chips. The model shows that the resistance between the injector and the sensor increases with separation. Figure 2.8 illustrates that there is good agreement between the model and the simulations.

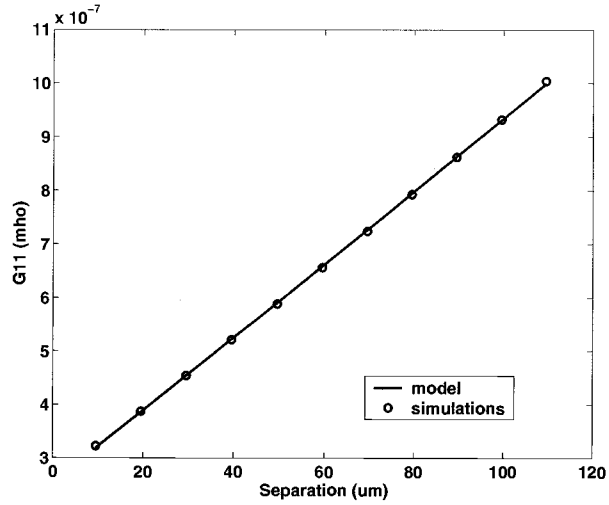


FIGURE 2.6.: G11 as a function of separation for a substrate thickness of 150μm.

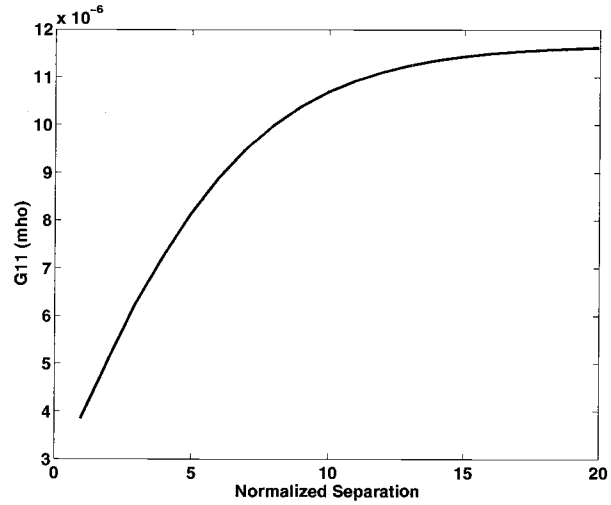


FIGURE 2.7.: G11 as a function of the separation normalized to a substrate thickness of 10μm.

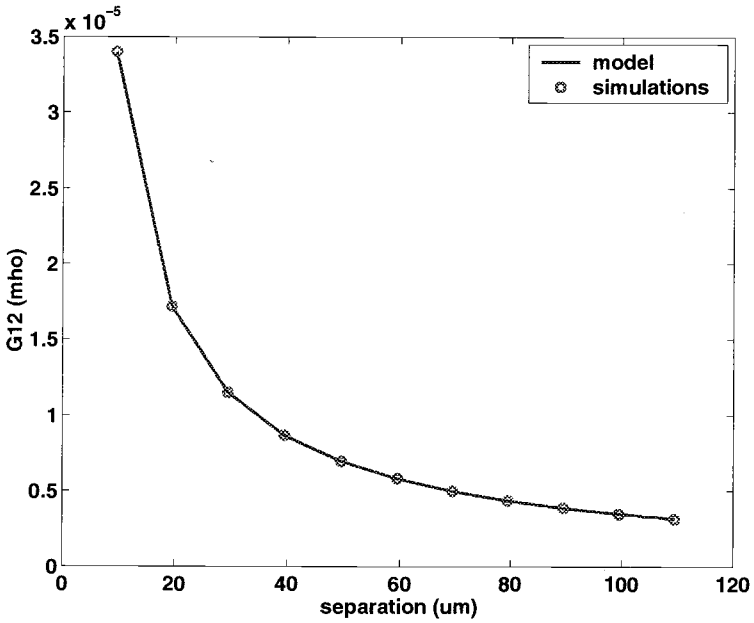


FIGURE 2.8.: Comparison of the model for G12 with device simulations.

In order to validate the proposed model, two test chips were fabricated using the Cypress Semiconductor 0.6μm CMOS and the TSMC 0.35μm CMOS lightly doped processes. The test chip fabricated using the Cypress process is shown in Figure 2.9. The chip includes different p+ test structures of various sizes placed at different separations from each other. G12 was measured and as indicated in Figures 2.10 (a) and (b) it is seen that there is good agreement between the model and the measurements obtained from both these chips.

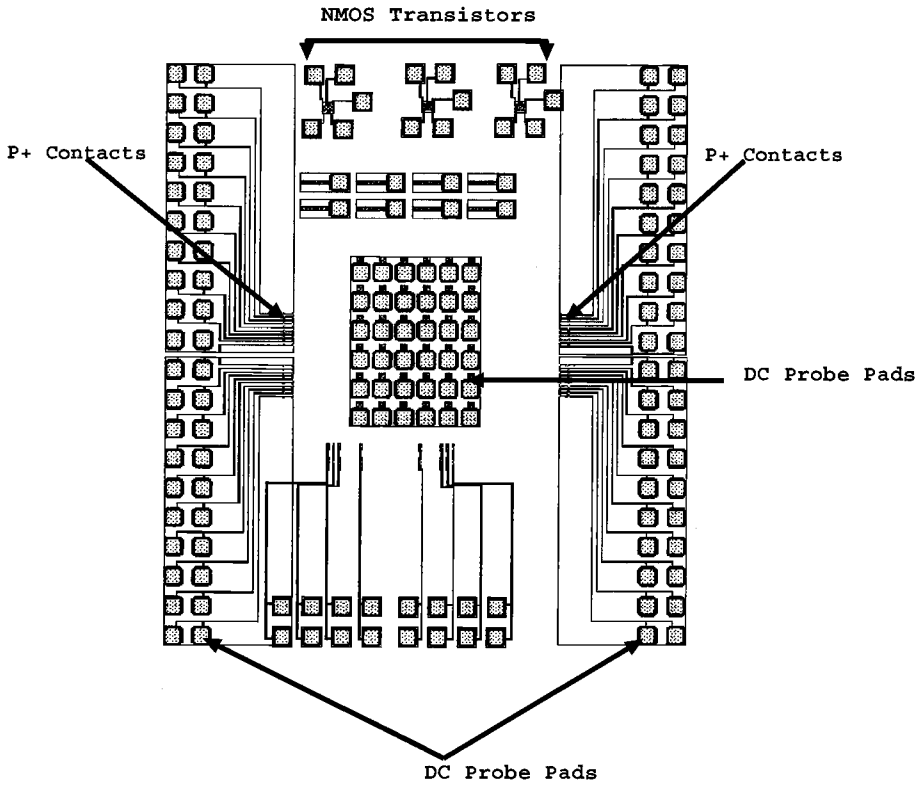
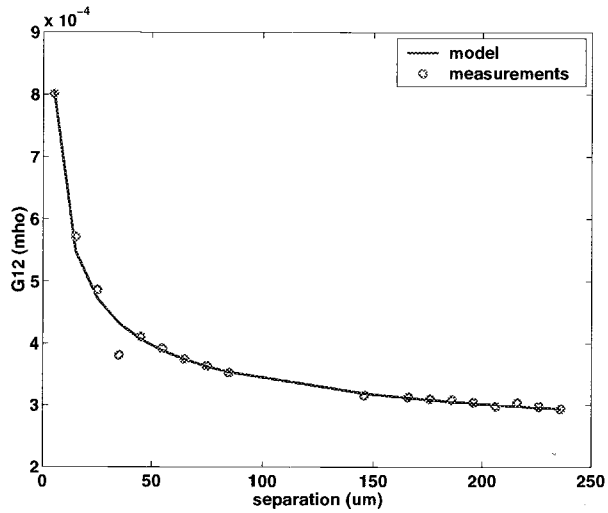
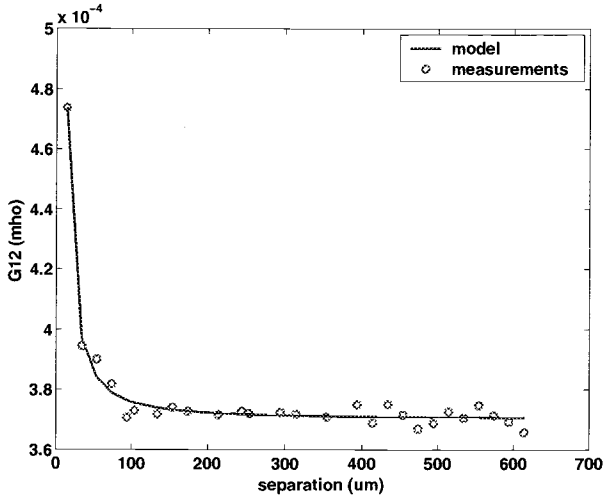


FIGURE 2.9.: Test chip fabricated in the Cypress semiconductor 0.6μm CMOS lightly doped process.



(a)



(b)

FIGURE 2.10.: Comparison of measurements and model for: (a) Cypress Semiconductor 0.6μm CMOS process and (b) TSMC 0.35μm CMOS process.

2.2. Scaled Contacts

To extend the model to various widths of substrate contacts, the setup in Figure 2.11 was used. For fixed separations between two contacts, the injector width was varied, from 2μm to 16μm, while the sensor remained a point contact. The separation was assumed to be the distance between the inner edge of the injector to the inner edge of the sensor. The sensor and the backplane were connected to ground. Simulations were done for many different separations.

An observation of the data extracted from simulations (Figure 2.12) shows that G11 increases linearly with the width of the contact for a given separation. This translates mathematically into the following model:

$$G11(W, x) = \mu W + Ax + B \tag{2.3}$$

where μ, A and B are process dependent parameters. μ in expression (2.3), can be extracted for each separation through curve fitting. In Figure 2.13, a plot of μ as a function of separation shows μ is approximatively constant.

The cross-conductance values, G12, are also extracted from the simulations. It is found that G12 remains constant for different widths, Figure 2.14.

One explanation for G12 being constant is that the current flows from the inner edge of the injector to the inner edge of the sensor. This implies that for the same separation, the width of the contact does not affect the value of G12.

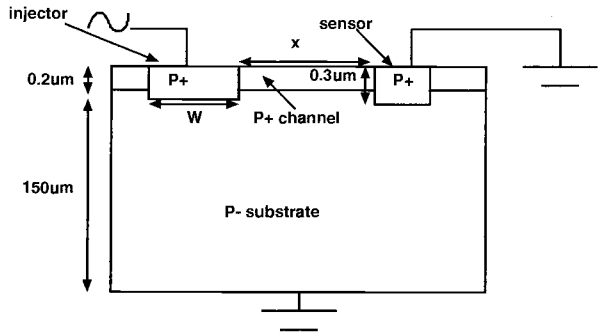


FIGURE 2.11.: Setup used for wide contact simulations.

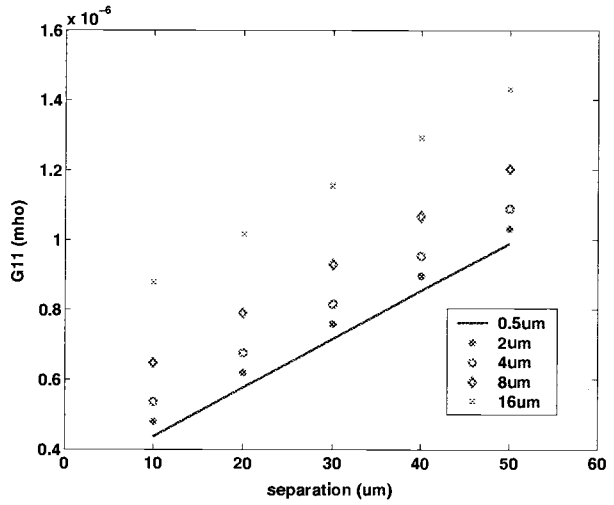


FIGURE 2.12.: G11 as a function of the separation for different injector contact widths.

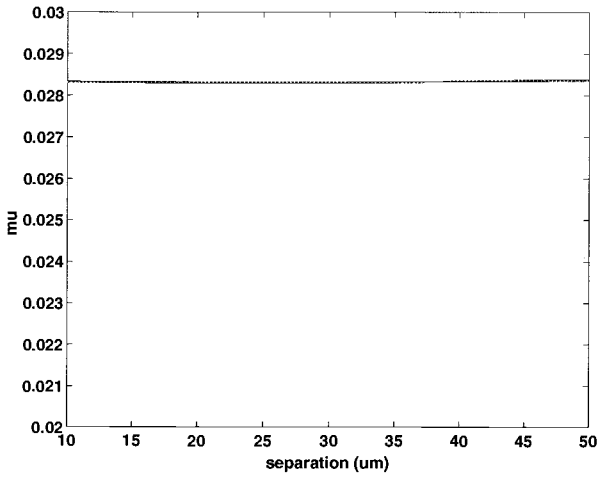


FIGURE 2.13.: μ as a function of separation.

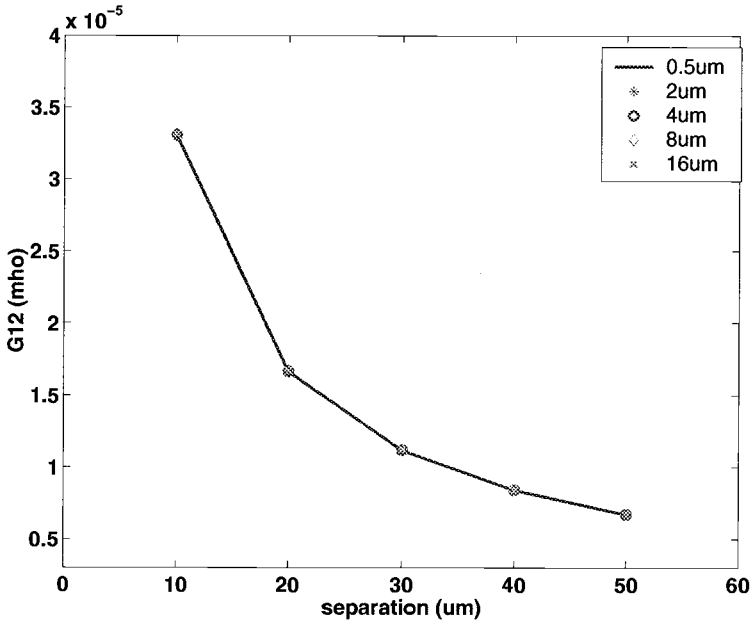


FIGURE 2.14.: G12 as a function of the separation for different injector contact widths.

3. APPLICATIONS

Many isolation techniques are used to attenuate the effect of the substrate noise [4,22]. Some of these techniques and their effectiveness are studied in the first part of this section, using both device and SPICE simulations. In the second part of this section, an example that illustrates the use of the model with a circuit is presented.

3.1. Separation Between Injector and Sensor Contacts

Separation between the noisy and sensitive circuitry is one of the techniques used to control the effects of substrate noise. By placing the noise injector far enough away, the noise will be sufficiently attenuated when it reaches the sensor. In order to verify the effectiveness of this technique for CMOS lightly doped processes, the isolation for point contacts was found as a function of separation. This was done by first using MEDICI and then doing SPICE simulations using the model. The setup shown in Figure 3.1 was used for SPICE simulations. A signal is applied to the injector with the sensor and the backplane grounded. The isolation, which is the amount of noise that is attenuated, is computed as [3]:

$$Isolation = 20 \log \left| \frac{I_{sensor}}{I_{injector}} \right| \tag{3.1}$$

Figure 3.2 shows that the improvement obtained up to a separation of 90μm, is less than 2dB, which is not significant. The poor isolation in this case is explained by the presence of the P+ channel-stop implant, through which, most of the current flows. In order to observe the isolation for large separations, device simulations were done for a substrate depth of 10μm. It is observed that for large separations, the isolation is better, as illustrated in Figure 3.3. As the resistance to the backplane

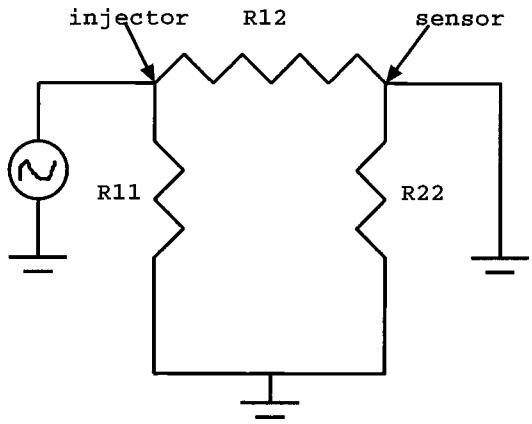


FIGURE 3.1.: Circuit used to simulate the isolation in SPICE.

becomes comparable to the resistance from the injector to the sensor, an alternate path is created for the current to flow.

Therefore, separation is found to be effective for isolation as long as the separation used is considerably larger than the substrate thickness. In this case, as illustrated in Figure 3.3, an isolation of 20dB requires a separation 10 times as large as the substrate thickness. With a typical substrate thickness of 650μm, this would require a separation of 6.5mm which is impractical on most IC's. Therefore, due to area constraints, this is not an effective technique for isolation in practice.

3.2. P+ Guard Rings

Another technique for reducing substrate noise is the use of guard rings. The idea behind this technique is that the noise leaving the injector can be "picked up" by the guard ring before it reaches the sensor. Figures 3.4 (a) and (b) [2] show the setup used to observe the effect of the guard ring using MEDICI and SPICE3,

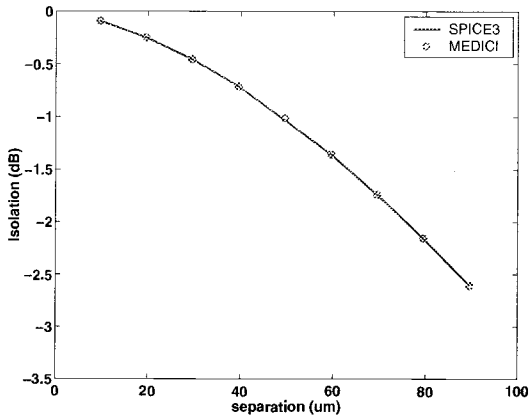


FIGURE 3.2.: Isolation as a function of separation for a substrate depth of 150μm.

respectively. Simulations were done for a 5μm wide guard ring connected to ground directly and through pin inductances. It was also assumed that the backplane and the sensor were connected to ground. The separation between the guard ring and the injector was varied while the separation between the injector and the sensor was kept fixed at 90μm.

A plot of the current flow lines given in Figure 3.5 helps to illustrate how a guard ring works in this case. Most of the current flows from the injector to the guard ring. This behavior translates into a good isolation as illustrated in Figure 3.6. It is seen that the guard ring is effective, especially when it is placed close to the injector. For the frequency of operation (500 MHz), the isolation obtained is not affected by the pin inductance connected to the guard ring, Figure 3.7.

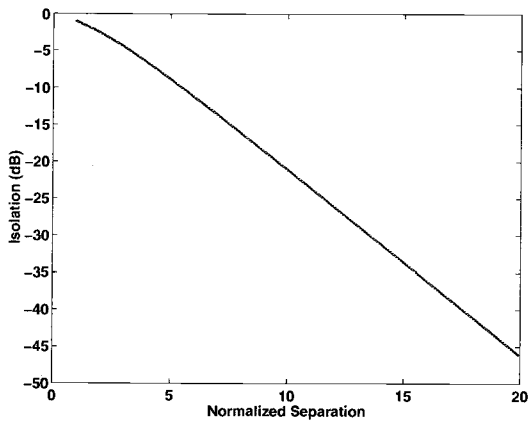
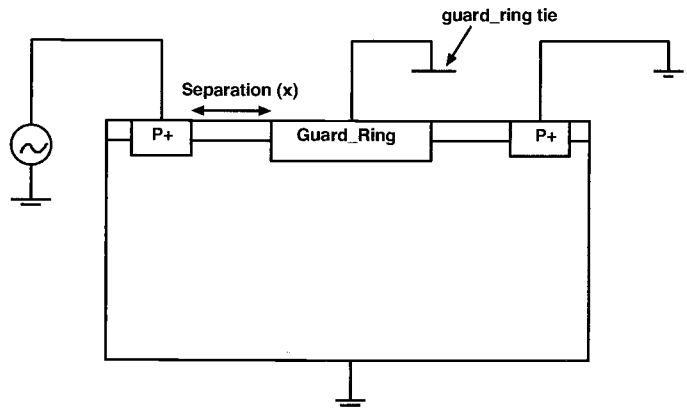
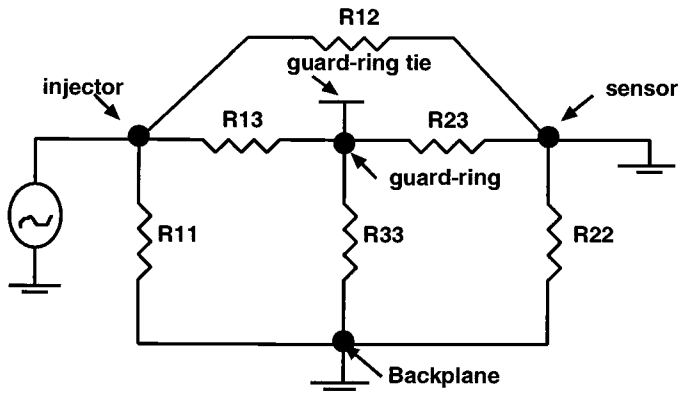


FIGURE 3.3.: Isolation as a function of the separation normalized to a substrate depth of 10μm.



(a)



(b)

FIGURE 3.4.: Simulation used to evaluate the effectiveness of guard-rings in:(a) MEDICI and (b) SPICE3.

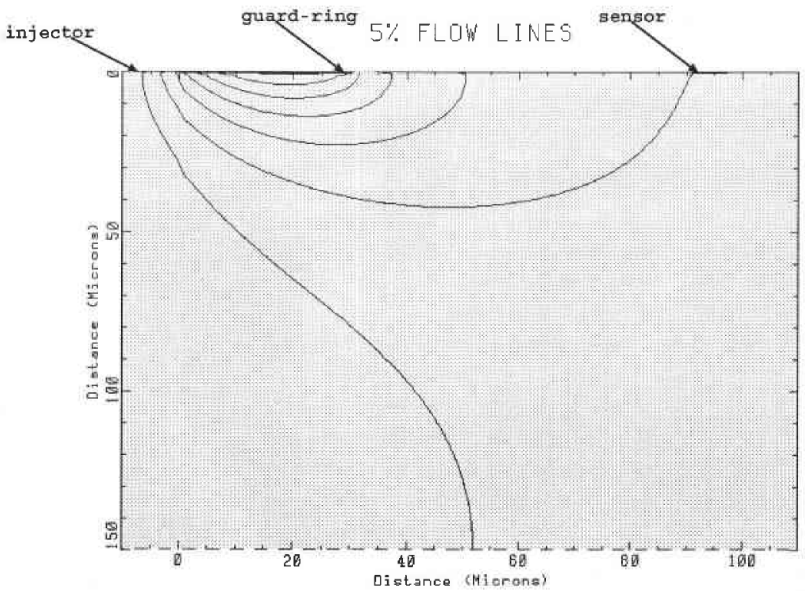


FIGURE 3.5.: Current flow lines to illustrate how a P+ guard ring isolates the sensor from the noise of the injector.

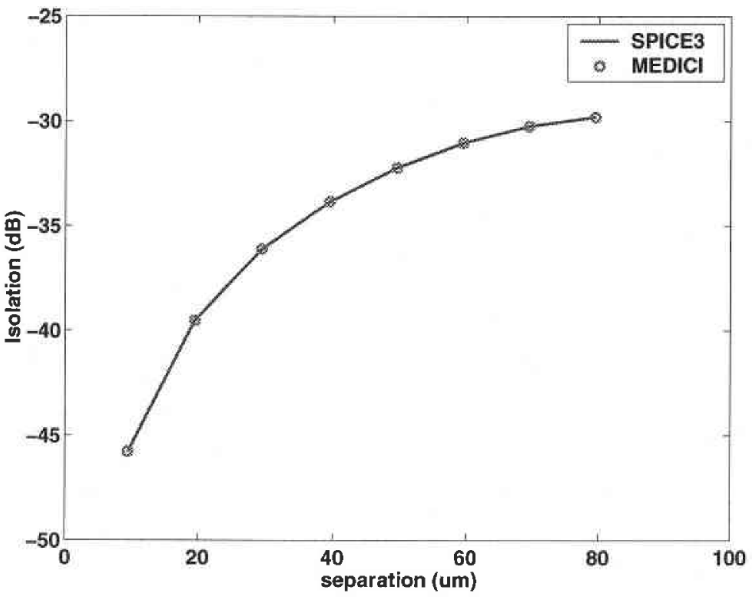


FIGURE 3.6.: Isolation between the source and the sensor with P+ guard rings when the backplane and the guard ring grounded.

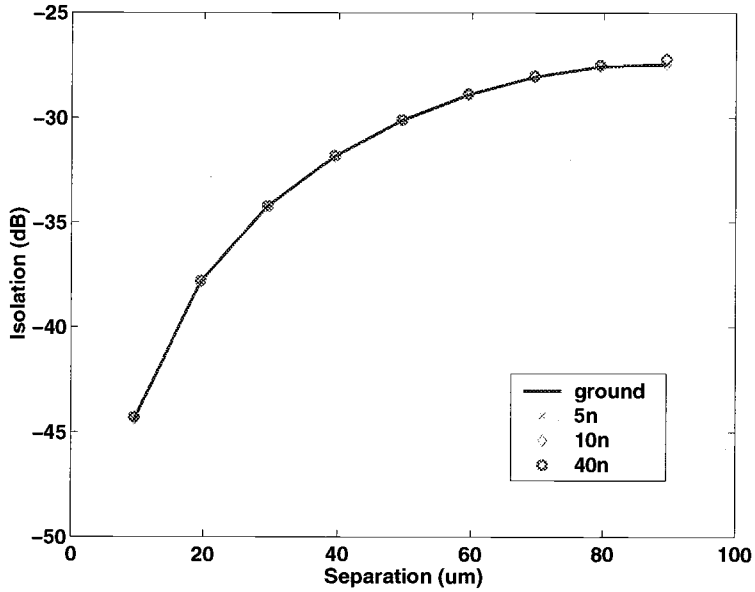


FIGURE 3.7.: Isolation with P+ guard rings. Simulated results for the P+ guard ring connected to various pin inductances and the backplane grounded are shown.

3.3. Nwell Guards

The use of Nwells is also one of the techniques used for reducing substrate noise coupling. In order to determine the effectiveness of this technique, the isolation obtained from Nwells was compared to that obtained using the two techniques presented previously (separation and P+ guard rings). The setup used for P+ guard rings was utilized with an Nwell replacing the P+ guard ring. The Nwell chosen was 5μm wide. The Nwell and the backplane were connected to ground for all the simulations. Current flow lines given in Figure 3.8 show that the well pushes some of the current down to the substrate while the rest flows to the sensor.

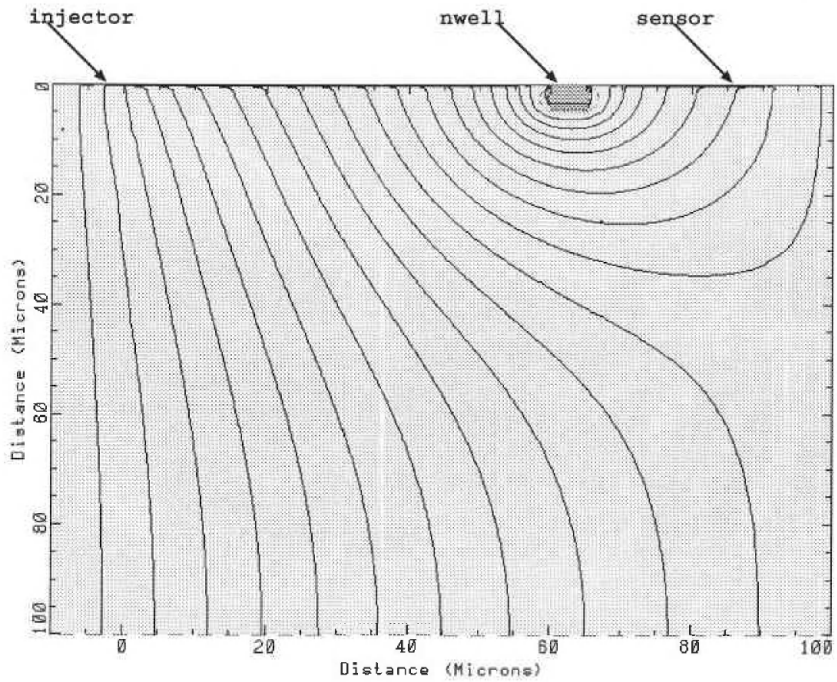


FIGURE 3.8.: Current flow lines with an Nwell. The Nwell and the backplane are grounded.

Figure 3.9 summarizes the results. It is observed that the use of P+ guard rings is the best isolation technique for CMOS lightly doped processes. It is also

observed that the isolation with P+ guard rings is independent of frequency while the isolation with Nwells increases as frequency is increased. As the frequency increases, the amount of noise picked up by the Nwell through the depletion capacitor also increases, thereby improving the isolation. Finally, among the three techniques studied, separation was found to provide the worst isolation.

Table 3.1 gives a comparison of some of the typical values obtained for the lightly doped process and those obtained in [3] for a heavily doped process. Resistance values are given for point contacts, and isolation values obtained are also included for two separations, $10/mu$m and $40/mu$m.

	Lightly doped	*Heavily doped*
R_{11} ($x = 10\mu$m)	3.1M	20K
R_{12} ($x = 10\mu$m)	28.4K	37.8K
R_{11} ($x = 40\mu$m)	1.9M	14.5K
R_{12} ($x = 40\mu$m)	113.5K	1.0M
Isolation with separation ($x = 10\mu$m)	-0.2dB	-5dB
Isolation with separation ($x = 40\mu$m)	-0.7dB	-40dB

TABLE 3.1.: Comparison of resistance and isolation values in the CMOS lightly and heavily doped processes.

3.4. Circuit Example

A folded-cascode amplifier (analog block) surrounded by inverters (digital block) was designed and fabricated in the TSMC 0.35μm process. Experimental results were compared to simulated results obtained using the model.

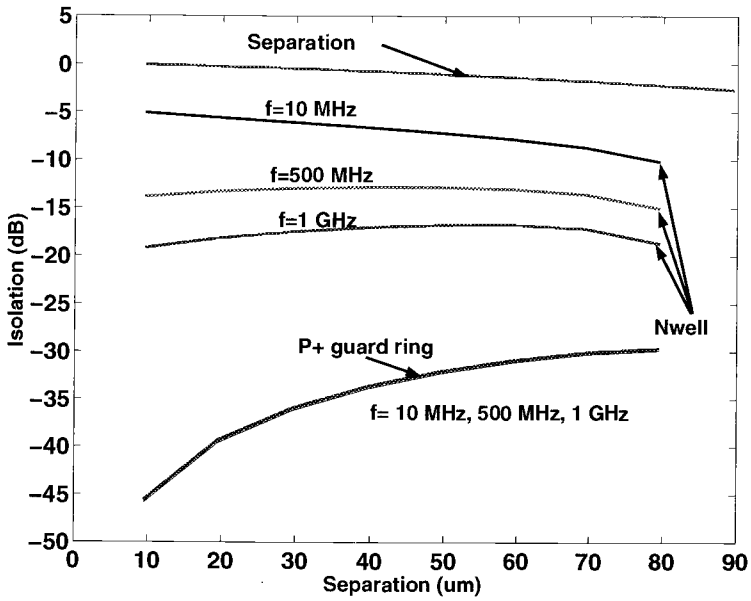


FIGURE 3.9.: Comparison of different isolation techniques for different separations and different frequencies.

Figure 3.10 (a) shows the setup used for SPICE simulations. In order to observe the effects of substrate noise coupling, a single-ended configuration was chosen for the folded cascode amplifier. Each digital block consisted of two inverters of different sizes: a big inverter with W(pmos)=200μm and W(nmos)=100μm, and a small inverter with W(pmos)=50μm and W(nmos)=25μm. The channel length chosen was L=0.8μm for all the transistors. This digital block configuration was chosen so that the effects of the size of the noise injector could be studied. Packaging and wiring parasitics (Cp and Cp3) were added in both the analog and the digital circuits during the simulations [13],[14]. Simulations were run with the amplifier connected in a unity-gain configuration. Using the method described in [3] the resistive network shown in Figure 3.10 (b) was derived from the layout information. The layout consisted of four main active areas, hence a four-port network

was assumed. On the network, N1 represents the node to which all the substrate ties of the amplifier PMOS transistors are connected through the nwell capacitor, Cwell. The amplifier NMOS transistors substrate ties are connected to N2. On the digital block, the NMOS and the PMOS substrate ties are connected to N3 and N4, respectively. Cwd represents the nwell capacitances seen by the digital PMOS transistors. The backplane is connected to a 5nH inductor.

The floorplan used to derive the substrate network is shown in Figure. 3.11. Table 3.2, given below, summarizes the contact sizes, the values of the resistances along with the separations between the contacts.

$A_i(\mu m^2)$	$A_j(\mu m^2)$	$x(\mu m)$	R_{ii}	R_{jj}	R_{ij}
N1: 716	N2: 287	29.4	77.0K	236.0K	108.4K
N1: 716	N3: 560	35.8	77.0K	99.3K	98.2K
N1: 716	N4: 1120	55.0	77.0K	40.9K	83.6K
N2: 287	N3: 560	20.4	108.4K	99.3K	101.7K
N2: 287	N4: 1120	79.6	24.0K	40.9K	144.2K
N3: 560	N4: 1120	77.0	99.3K	40.9K	110.5K

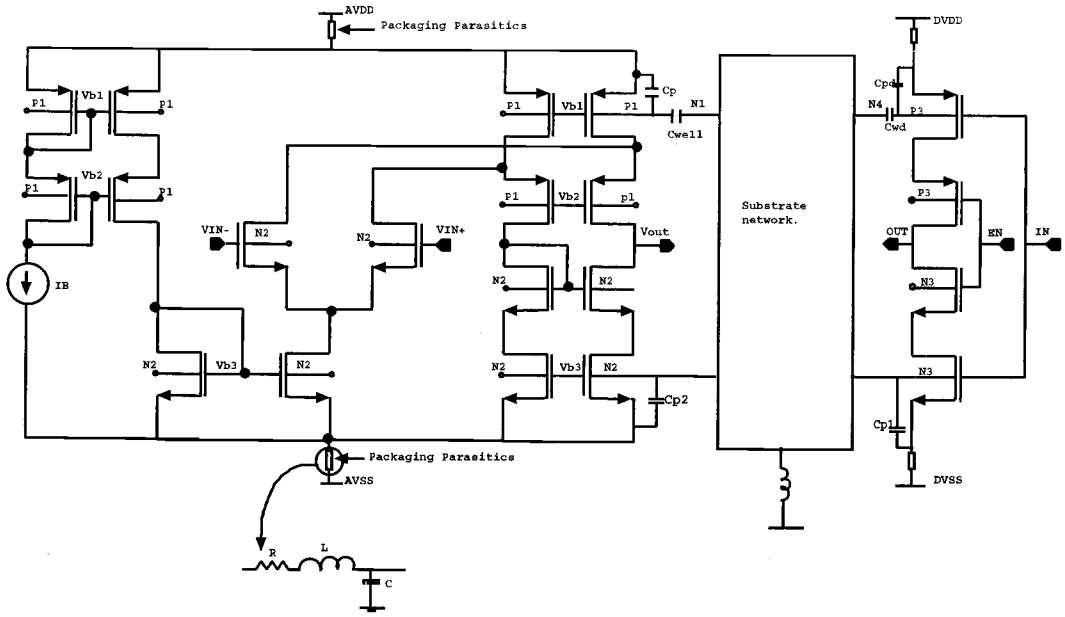
TABLE 3.2.: Contact areas, separation and computed resistance values for the circuit example.

In this table, A_i and A_j, where i=1,2,3 and j=2,3,4, represent the contact areas N1-N4. The resistances to the backplane are represented by R_{ii} and R_{jj}, and the coupling resistances between contacts, separated by a distance x, are represented by R_{ij}.

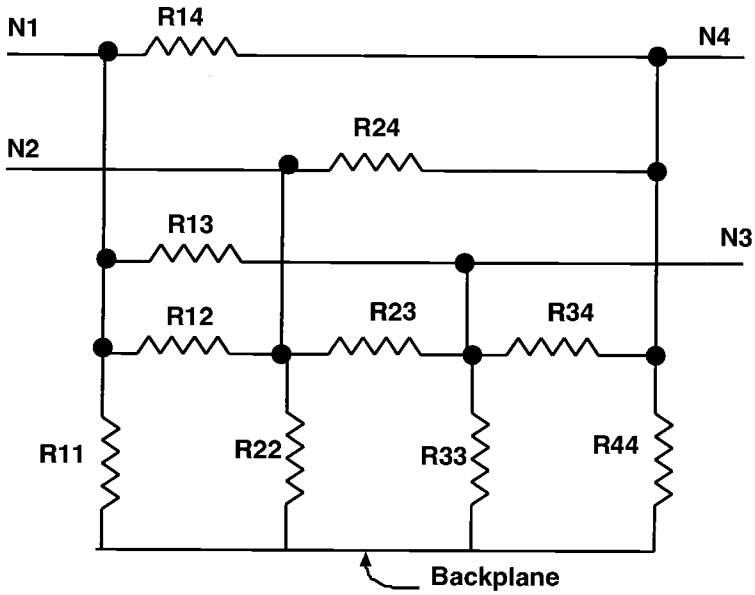
Figure 3.12 (a) shows the spectrum of the output of the amplifier when a 4KHz signal, with an amplitude of 250mV, is applied at its input with all inverters

inactive. The output contains the fundamental at 4KHz as expected and some harmonics resulting from the nonlinearities associated with the amplifier. For the second simulation, one small(big) inverter is turned on by applying a voltage bias at the gate labeled 'EN'('IN') and a clock running at 1MHz at the gate labeled 'IN'('EN'). Figures 3.12 (b) and (c) show the amplifier output spectrum for the two cases. The output spectra with the inverters on show the presence of a tone at the clock frequency, 1MHz, which indicates that there is noise coupling through the substrate. The magnitude of the tone is -79dB. Harmonics of the clock also appear at the output of the amplifier.

Measurements were taken to validate the results obtained from measurements. Figure 3.13 (a) shows the output of the amplifier with a 4 KHz signal input and all the inverters inactive. The measurement shows a good agreement with the simulation for this case. The results obtained from the measurements with the inverters on are plotted in Figures 3.13 (a) and (b) for the small inverter and the big inverter, respectively. In both cases, tones can be seen at 1MHz and harmonics of the clock as in the simulations. However, the magnitudes of these tones are very different from the simulated results. Measurements show the first harmonic of the clock at -45dB while simulations predicted this tone at -79dB for the small inverter on, and at -88dB for the big inverter on.



(a)



(b)

FIGURE 3.10.: (a):Circuit used to determine noise coupling between an inverter and an amplifier in SPICE and (b) substrate network used.

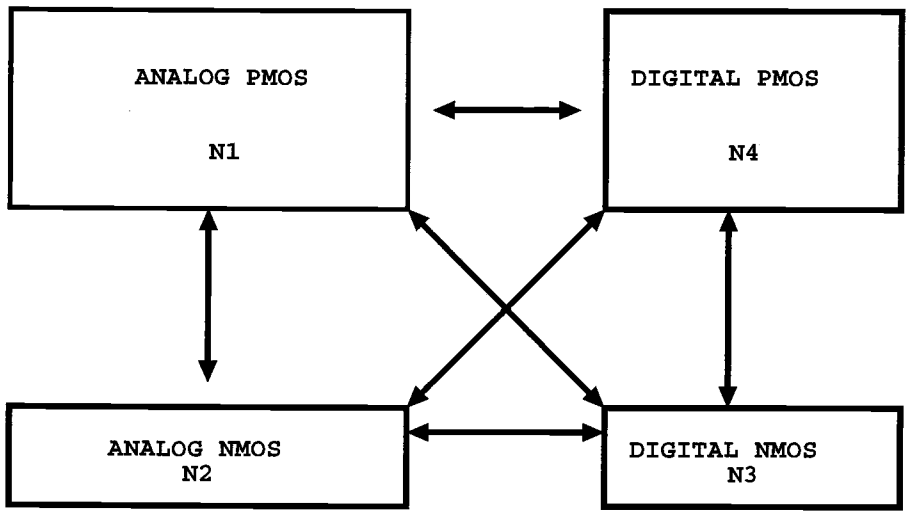
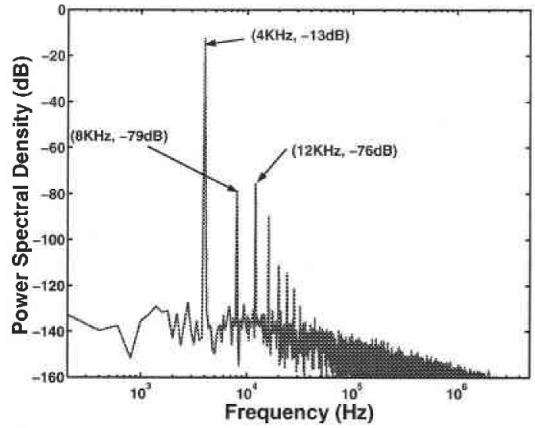
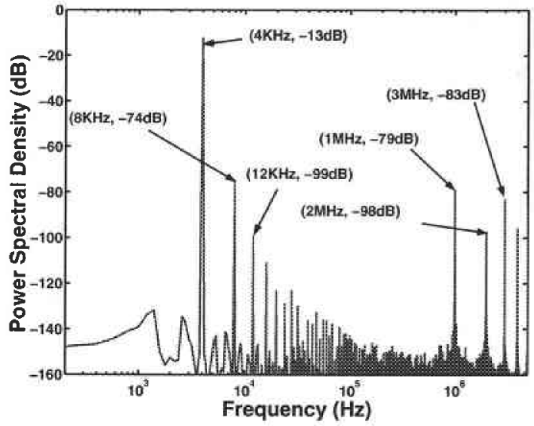


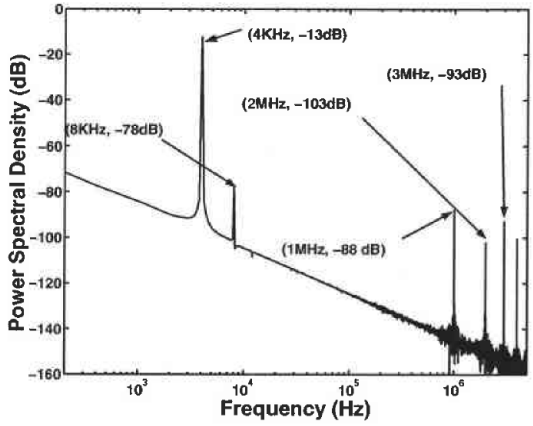
FIGURE 3.11.: Floorplan used to derive the substrate resistive network.



(a)

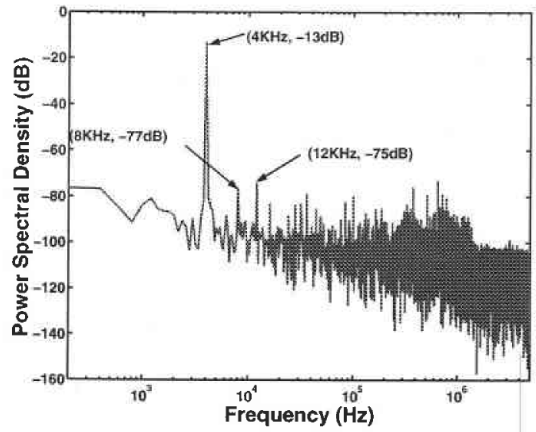


(b)

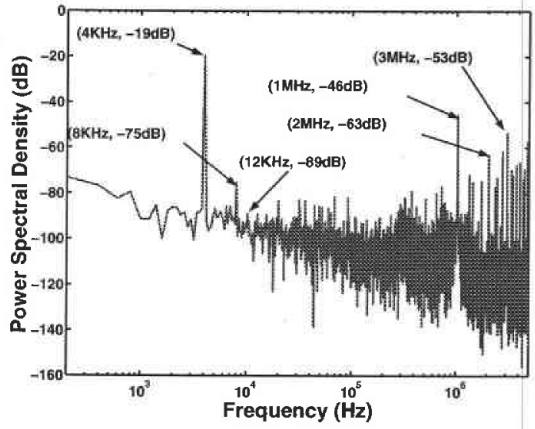


(c)

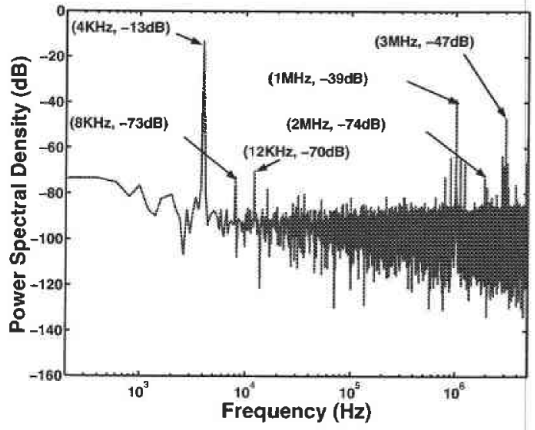
FIGURE 3.12.: Amplifier output spectrum from simulations: (a) without any digital gates on, (b) with a small inverter turned on and (c) with a big inverter turned on.



(a)



(b)



(c)

FIGURE 3.13.: Amplifier output spectrum from measurements: (a) without any digital gates on, (b) with a small inverter turned on and (c) with a big inverter turned on.

4. CONCLUSION

A design oriented model for lightly doped processes has been developed. The model has been validated with device simulations and with measurements of two different chips. The effectiveness of different isolation techniques has been investigated. The model has been used to predict the coupling between an amplifier and an inverter using simulations. Measurements on a circuit example have shown the predicted substrate noise injection values to be significantly different than the actual values. This reflects that more attention has to be focused on the modeling of the substrate noise coupling. As an example, the coupling through the bond pads has not been taken into consideration.

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APPENDICES

APPENDIX A. MEDICI Point Contact Input File

```
COMMENT   SUBSTRATE COUPLING
TITLE     TMA MEDICI
COMMENT   Specify a rectangular mesh

  MESH    SMOOTH=1
X.MESH    X.MIN=-10 X.MAX=-1  H1=1.2
X.MESH    X.MIN=-1 X.MAX=1  H1=0.25
X.MESH    X.MIN=1 X.MAX=99  H1=1.2
X.MESH    X.MIN=99 X.MAX=101  H1=0.25
X.MESH    X.MIN=101 X.MAX=110  H1=1.2

Y.MESH    N=1   L=-0.01
Y.MESH    N=3   L=0.
Y.MESH    N=10  L=0.5
Y.MESH    N=15  L=1
Y.MESH    N=150  L=150

COMMENT   Eliminate some unnecessary substrate nodes
ELIMIN    COLUMNS  Y.MIN=0.5 X.MIN=-10 X.MAX=-1
ELIMIN    COLUMNS  Y.MIN=0.5 X.MIN=101 X.MAX=110

COMMENT   Specify oxide and silicon regions
REGION    SILICON
REGION    OXIDE    IY.MAX=3

COMMENT   Electrode definition
ELECTR    NAME=Substrate  BOTTOM
ELECTR    NAME=Source  X.MIN=0 X.MAX=0.5  IY.MAX=3
ELECTR    NAME=Sensor   X.MIN=100 X.MAX=100.5  IY.MAX=3

COMMENT   Specify impurity profiles and fixed charge
PROFILE   P-TYPE  N.PEAK=3E14  UNIFORM   OUT.FILE=coup100uaDS
PROFILE   P-TYPE  N.PEAK=4.1E17  Y.CHAR=.2
PROFILE   P-TYPE  N.PEAK=9.5E19  Y.JUNC=.3  X.MIN=0.0  WIDTH=0.5
+         XY.RAT=.75
PROFILE   P-TYPE  N.PEAK=9.5E19  Y.JUNC=.3  X.MIN=100  WIDTH=0.5
+         XY.RAT=.75
INTERFAC  QF=1E10
PLOT.2D   GRID  TITLE="Initial Grid"  FILL
```

```
COMMENT   Specify contact parameters
COMMENT   Specify physical models to use
MODELS    CONMOB  FLDMOB  SRFMOB2
PLOT.1D   DOPING  X.START=1 X.END=1  Y.START=0  Y.END=20
+         Y.LOG  POINTS  BOT=1E12  TOP=1E20  COLOR=2
+         TITLE="Example 1 - Substrate Impurity Profile(150ua)"
PLOT.2D   BOUND  TITLE="Example 1 - Impurity Contours"  FILL
CONTOUR   DOPING  LOG  MIN=16   MAX=20   DEL=.5  COLOR=2
CONTOUR   DOPING  LOG  MIN=-16  MAX=-15  DEL=.5  COLOR=1  LINE=2
SAVE OUT.FILE=coup100uaMS MESH W.MODELS

COMMENT   Symbolic factorization, solve, regrid on potential
SYMB      CARRIERS=0
METHOD    ICCG  DAMPED
SOLVE

COMMENT   Solve using the refined grid, save solution for later use
SYMB      CARRIERS=0

COMMENT   Impurity profile plots
PLOT.1D   DOPING  X.START=.25  X.END=.25  Y.START=0  Y.END=20
+         Y.LOG  POINTS  BOT=1E12  TOP=1E21  COLOR=2
+         TITLE="Source Impurity Profile"
PLOT.1D   DOPING  X.START=100.25  X.END=100.25  Y.START=0  Y.END=20
+         Y.LOG  POINTS  BOT=1E12  TOP=1E21  COLOR=2
+         TITLE=" Sensor Impurity Profile"
PLOT.1D   DOPING  X.START=6  X.END=6 Y.START=0  Y.END=20
+         Y.LOG  POINTS  BOT=1E12  TOP=1E20  COLOR=2
+         TITLE=" Substrate Impurity Profile"
PLOT.1D   DOPING  X.START=-2  X.END=-2 Y.START=0  Y.END=20
+         Y.LOG  POINTS  BOT=1E12  TOP=1E20  COLOR=2
+         TITLE=" Substrate Impurity Profile"
PLOT.2D   BOUND  TITLE="Example 1 - Impurity Contours"  FILL SCALE

CONTOUR   DOPING  LOG  MIN=15   MAX=18   DEL=.5  COLOR=2
CONTOUR   DOPING  LOG  MIN=-18  MAX=-15  DEL=.5  COLOR=1  LINE=2

SYMB      CARRIERS=1 NEWTON
METHOD    ICCG  DAMPED
SOLVE
SYMB      CARRIERS=2 NEWTON
METHOD    ICCG  DAMPED
```

```
SOLVE
Solve V(Source)=0.1 ELEC=Source
LOG  OUT.FILE=coup100ua.log
SOLVE OUT.FILE=coup100uaS

PLOT.2D BOUND JUNC DEPL TITLE=" FLOW LINES" FILL
CONTOUR FLOWLINES NCONT=50 COLOR=1
COMMENT PLOT.2D GRID BOUND JUNC DEPL TITLE=" 5% FLOW LINES" FILL
COMMENT CONTOUR FLOWLINES NCONT=21 COLOR=1
COMMENT   Use Newton's method with 2 carriers

SYMB      NEWTON  CARRIERS=2
COMMENT   Setup log file for I-V and AC data
LOG       OUT.FILE=coup100uaFI
COMMENT   Forward bias the base-emitter junction and
COMMENT   calculate the admittance matrix at 500 MHz
SOLVE     AC.ANAL  FREQ=500E06 VSS=1  TERM=Source
+OUT.FILE=coup100uaS7
```

APPENDIX B. SPICE Netlist

```
.SUBCKT ANALOG VINP VINM VOUT
*INPUT PAIRS
M1 8 VINM 7 6 NMOS W=14.4u L=0.8u
M2 9 VINP 7 6 NMOS W=14.4u L=0.8u

*NMOS BIASING
M3 7 5 6 6 NMOS W=28.8u L=0.8u
M4 5 5 6 6 NMOS W=4.8u L=0.8u

*NMOS CASCODE
M5 13 5 6 6 NMOS W=14.4u L=0.8u
M6 12 5 6 6 NMOS W=14.4u L=0.8u
M7 11 11 13 6 NMOS W=14.4u L=0.8u
M8 VOUT 11 12 6 NMOS W=14.4u L=0.8u

*PMOS CASCODE
M9 11 3 9 1 PMOS W=19.2u L=0.8u
M10 VOUT 3 8 1 PMOS W=19.2u L=0.8u
M15 9 2 1 1 PMOS W=115.2u L=0.8u
M16 8 2 1 1 PMOS W=115.2u L=0.8u

*PMOS BIASING
M11 2 2 1 1 PMOS W=19.2u L=0.8u
M12 4 2 1 1 PMOS W=19.2u L=0.8u
M13 3 3 2 1 PMOS W=19.2u L=0.8u
M14 5 3 4 1 PMOS W=19.2u L=0.8u

*MODIFICATION FROM SHORT
VS 2 3 DC 0
VB 3 0 DC 0.23

.ENDS ANALOG

.SUBCKT DIGITAL IN EN OUT
*BIG INVERTER
MP1 OUT EN 10 40 PMOS W=200u L=0.8u
MN1 OUT EN 60 0 NMOS W=100u L=0.8u
*SMALL INVERTER
MP2 10 IN 40 40 PMOS W=50u L=0.8u
```

```
MN2 60 IN 0 0 NMOS W=25.2u L=0.8u
.ENDS DIGITAL

.SUBCKT NETWORK Panalog Pdigital N3 N4 BK

*NWELL CAPS
Canalog Panalog N1 100e-15
Cdigital Pdigital N2 129e-15

R11 N1 BK  77.0e3
R12 N1 N2 108.4e3
R13 N1 N3  98.2e3
R14 N1 N4  83.6e3
R22 N2 BK 236.0e3
R23 N2 N3 101.7e3
R24 N2 N4 144.2e3
R33 N3 BK  99.3e3
R34 N3 N4 110.5e3
R44 N4 BK  40.9e3

.ENDS NETWORK
```

APPENDIX C. MATLAB code used to derive the substrate resistive network

Steps to derive the network:

1. Determine number of contacts.
2. Determine separation between contacts.
3. Determine sizes of contacts: W x L
4. Extract Z11 for point contacts(0.5u x 0.5u) by scaling value obtained from Cypress measurements by K. H. Kwang
5. Scale Z11 and Z22 with the areas of the contacts
6. Compute Z12t which is the impedance for a separation x=0
7. Compute Z12 using the model for G12, with alpha replaced by Z12t
8. Compute N-Port Z matrix
9. Compute N-Port Y matrix
10. Extract resistances

```
%MATLAB Code
%Calculation of substrate parameters for n contacts
%Start from z11 for point contact, scale with area and
%obtain z12 using the model for G12

close all;
clear all;

%number of contacts

a=4;
%enter separation between contacts (1-2,1-3,...1-n,2-3,..2-n.....(n-1)-n)
D=zeros(a,a);
W=zeros(1,a);

D(1,2)=29.4e-6;
D(1,3)=35.8e-6;
D(1,4)=55e-6;
D(2,3)=20.4e-6;
D(3,4)=77e-6;
```

```
D(2,4)=79.6e-6;


D=D+D';

for m=1:1:a-1

   for n=m+1:1:a

%enter different contact widths and lengths
%N1=Analog PMOS, N2=Analog NMOS, N3=Digital NMOS, N4=Digital PMOS

  L=[4.8 2.4 11.2 11.2]*1e-6;
  W=[149.2e-6 119.4e-6 50e-6 100e-6]
        W1=W(1,m);
        W2=W(1,n);
        L1=L(1,m);
        L2=L(1,n);
         x=D(m,n);

%Model Parameters from measurements

alpha=3.5e-3;
kappa=-1.4120;
beta=-3.1207e-8;


%Z11 for point contact obtained by scaling Z11 from Kwang's thesis\\
z11p=13.6e6;

%Scaling Z11 with size of contact
s=0.5e-6*0.5e-6;
z11=z11p*s/(W1*L1);
z22=z11p*s/(W2*L2);

%Define new area and extract z12t, that is, z12 for x=0;
z12t=z11p*s/((W1*L1)+(W2*L2));

%Calculating z12 using formula for G12, with alpha=z12t
z12=z12t*exp(-beta*x^kappa);
z21=z12;
```

```
%computing Z matrix for n contacts
Z(m,m)=z11;
Z(n,n)=z22;
Z(m,n)=z12;
Z(n,m)=z21;

end
   end

Y=inv(Z);

%Computing Resistances
R=zeros(a,a);
     for i=1:1:a
       for j=1:1:a
         if (i==j)
          R(i,j)=1/sum(Y(i,:));
         else
        R(i,j)=-1/Y(i,j);
       end
    end
    end
 end
         end
 end
```