AN ABSTRACT OF THE THESIS OF

Kaushal Kestur Biligiri for the degree of Master of Science in Electrical and Computer Engineering presented on September 09, 2014.

Title: Grid Emulator for Wave Energy Converter Testing

Abstract approved:

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Annette von Jouanne and Ean Amon

Power generation has been an ever growing exigency since the invention of electric power. The world is gradually inching away from conventional generation toward renewable generation. Advancements in renewable energy generation have been at a steady positive pace over the past few decades with different resources developing to be feasible alternatives. A smooth and gradual transition from conventional generation to predominantly renewable energy sourced generation is what the world is looking toward in the next couple of centuries. The grid emulator is a device that will facilitate the testing and development of wave energy generators, thereby enabling the inclusion of energy generated using wave power into the existing generation mix, without causing adverse effects to the host system. The grid emulator will enable testing of wave energy devices under different grid disturbances as well as provide isolation between the devices and the grid during initial testing. This thesis presents the preliminary functions planned using the grid emulator, the specifications of the device, the design details and simulation results. The grid emulator under development is currently limited to wave energy devices, however, anomalous devices could be developed for the research and development of other under developed and untapped renewable resources.

Grid Emulator for Wave Energy Converter Testing

by

Kaushal Kestur Biligiri

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Dean of the Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Kaushal Kestur Biligiri, Author

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1. INTRODUCTION

1.1 Wave Energy

Renewable energy accounts for about 16% of the world's energy production [1]. Wave energy being one of the most dense, abundant and easily accessible energy resources, has the potential of taking it to greater heights. Waves get their energy as a result of the wind passing over open bodies of water, where wind itself is derived from solar energy. As long as the sun shines, wave energy will never be depleted [2]. The primary advantages of wave energy over other renewable energy resources are the availability, power density, predictability and consistency [3].

i) Availability: Availability is how often the resource is available, i.e., how often the waves are rolling. Wave energy is easily available along the coast and about 50% of the world's population lives near oceans, which eliminates the need for long distance power transmission lines.

ii) Power Density: A typical solar photovoltaic generates power in the range of hundred watts per square meter, a wind turbine generates a thousand watts per square meter of swept area, whereas wave energy is typically in the range of tens of thousands of watts per meter of wave front [3].

iii) Predictability: Satellites can be used to forecast wave energy supply several days in advance allowing the utilities time to plan their short-term electricity scheduling needs [4].

iv) Consistency: This is related to availability, where wave energy is "seasonal", though- much more consistent, e.g., as compared to other renewables such as wind that can disappear without notice.

The annual wave energy potential worldwide is predicted at 2 million megawatt hours per year. The World Energy Council estimates that about 10% of worldwide electricity demand could be met by harvesting ocean energy. The annual energy consumption in

the United States is about 4000 TWh. The Electric Power Research Institute (EPRI) has estimated an annual total wave energy resource along the outer continental shelf at 2640 TWh. However, due to competing use of ocean and environmental concerns in sensitive areas such as shipping, commercial fishing and naval operations, this energy cannot be fully harvested. EPRI estimates the total recoverable wave resource along the U.S. shelf edge to be 1170 TWh/year, which is about one-third of the annual electricity demand. The region-wise recoverable wave energy resource is estimated as below [5]:

West Coast (WA, OR, CA): 250 TWh/year

East Coast (ME thru FL): 160 TWh/year

Gulf of Mexico: 60 TWh/year

Alaska: 620 TWh/year

Hawaii: 80 TWh/year

Puerto Rica: 20 TWh/yr

Figure 1.1 illustrates the potential wave energy as a function of kW/m of the wave crest length.

Figure 1.2 shows the wave energy data as a function of kW/m of the crest length along the Oregon Coast. Oregon has a 300 mile coastline that is characterized by powerful waves and steady and constant winds. A 2011 EPRI study showed that the annual wave energy available along the inner shelf of the Oregon coast is about 143 TWh/year [6].

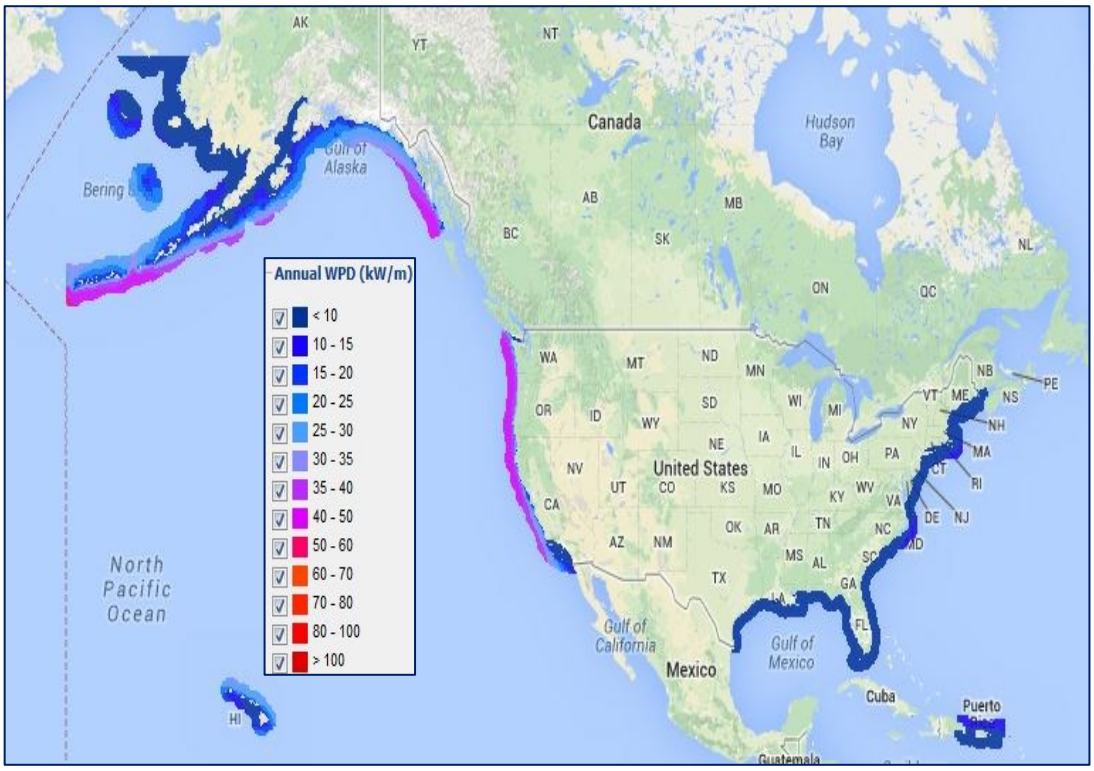


Figure 1.1. Wave Energy Potential for United States (NREL 2013).

Oregon has a strong port infrastructure and available electrical grid capability. The proximity of manufacturing operations to the Oregon coast and well-developed transportation systems make it optimal for early stage technology developers looking to test and develop in the same location [7].

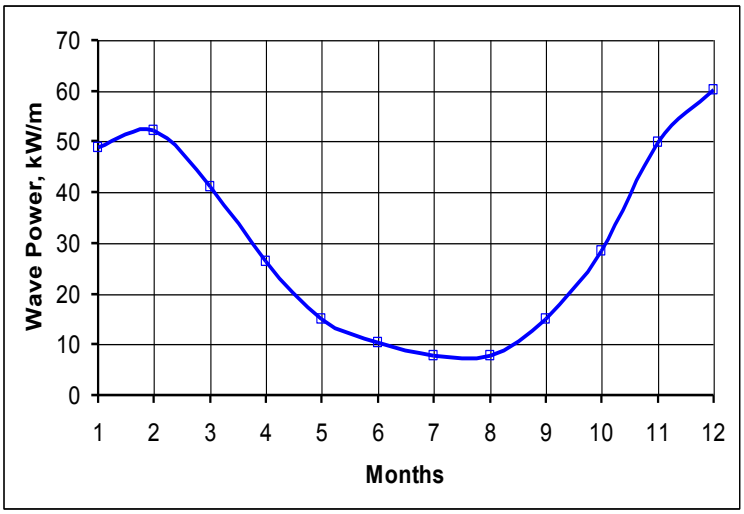


Figure 1.2. Wave data, power estimated from 5 buoys off the Oregon coast over 10 years [National Date Buoy Center].

1.2 Wave Energy Converter

A machine that is capable of extracting the wave power and converting it to usable energy is called a Wave Energy Converter (WEC). The first wave power plant was proposed by a Persian named Monsieur Girard and his son [2]. Since then, there have been thousands of patented WEC designs, although less than 5MW is currently delivered to the grid.

Wave energy is a nascent resource as compared to wind energy, which has gone through years of optimization and has finally settled with the most economical and efficient design of a horizontal axis wind turbine with three blades. Numerous WEC designs have materialized in the past couple of decades and the ongoing research is yet to choose the best from the lot. Different WEC designs have naturally led to dissimilar power take off mechanisms in these devices, thereby leading to a unique power profile from each device. The most common types of WECs are as listed below:

1.2.1 Point absorber

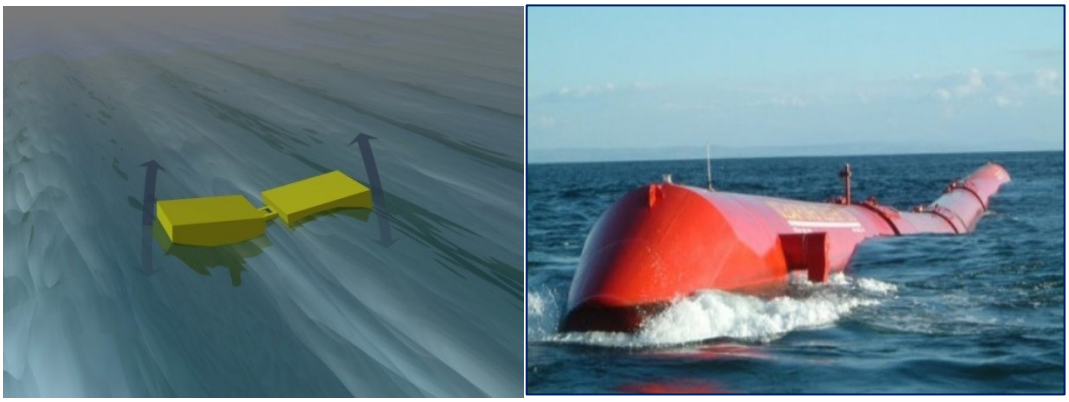
A point absorber works on the principle of relative motion between two segments. The moving portion of the WEC could either be floating or bottom mounted. The relative motion could directly be utilized to generate energy in a linear machine, utilized to alternate the compression of a gas or liquid in a container or converted into rotational movement of the power generator. Due to the symmetrical design of this device, a point absorber is independent of the wave direction [8]. Example WECs using this technology are manufactured by Ocean Power Technologies (see Figure 1.3) and WaveStar.

Concept [9] Ocean Power Technologies [10]

Figure 1.3. Point Absorber.

1.2.2 Surface Attenuator

A surface attenuator is a floating device with multiple segments connected with a series of joints that generate power as the waves move them up and down through hydraulic rams and a generator. The symmetrical axes of surface attenuators are oriented perpendicular to the incoming waves [11]. Example WECs using this technology are manufactured by Pelamis Wave Power (see Figure 1.4) and Checkmate SeaEnergy.

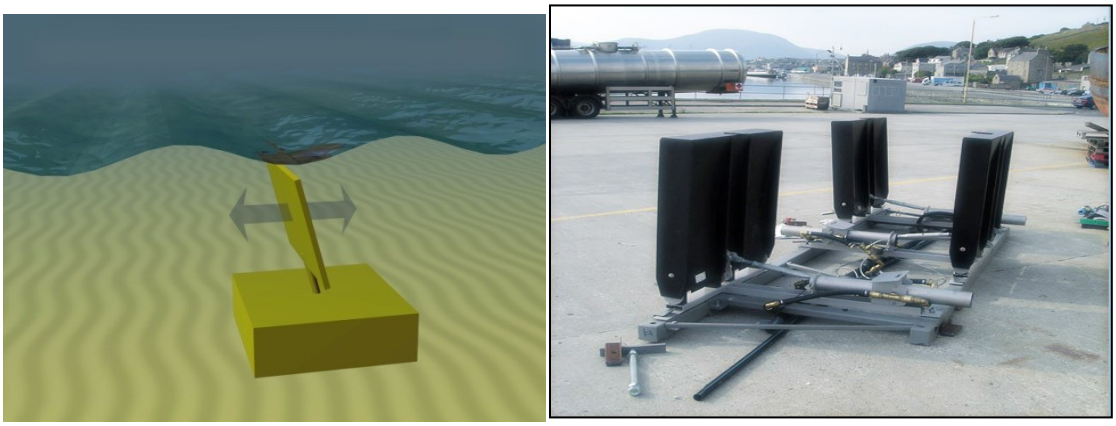


Concept [9] Pelamis Wave Power [12]

Figure 1.4. Surface Attenuator.

1.2.3 Oscillating Wave Surge Converter

Oscillating wave surge converters are usually placed in shallow waters and are partially or completely submerged. These extract energy from wave surges and the rotary movement of water particles within them. The moving panels transfer energy on to a hydraulic piston pump which in turn pumps the hydraulic fluids inside a closed hydraulic circuit. Example WECs using this technology are manufactured by AW Energy (see Figure 1.5), Wavepiston and Aquamarine Power.

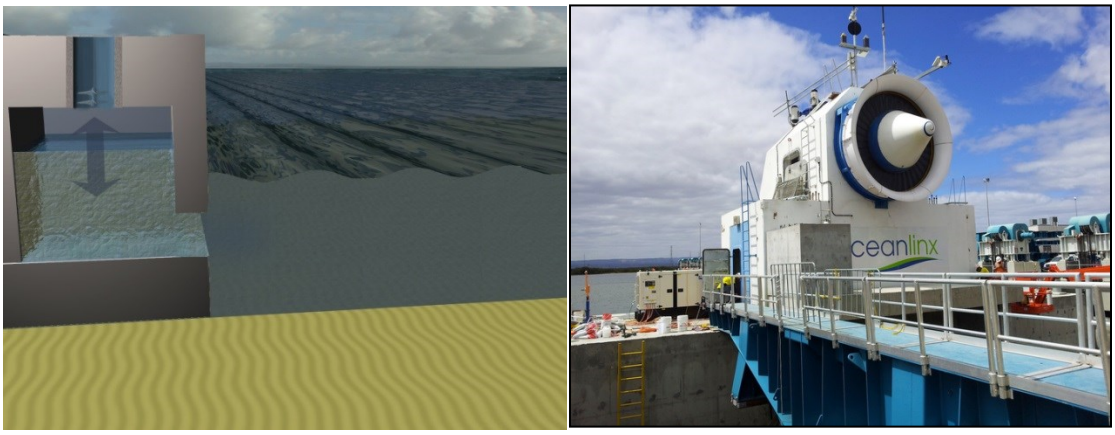


Concept [9] AW Energy [13]

Figure 1.5. Oscillating Wave Surge Converter.

1.2.4 Oscillating Water Column

Oscillating water columns are partially submerged, hollow structures in which the up and down movement of waves replicate the action of a piston to continuously pressurize and depressurize an air column. The compressed air is allowed to flow back and forth to the atmosphere via a turbine. Example WECs using this technology are manufactured by Oceanlinx (see Figure 1.6).



Concept [9] Oceanlinx [14]

Figure 1.6. Oscillating Water Column.

1.2.5 Overtopping Device

Overtopping devices capture water as waves break into a storage reservoir which is above the sea level. The water is then allowed to flow back to the sea via a low head turbine. Reflecting walls may be used to increase the amount of water captured. An example of an overtopping device is the Wavedragon (see Figure 1.7).

Concept [9] Wavedragon [15]

Figure 1.7. Overtopping Device.

1.3 Wave Energy Converter Development

Technology developers in the wave energy sector have been constrained primarily by a shortage of capital and, in particular, the reluctance on the part of the investors generally to commit to the significant level of capital necessary to demonstrate commercial feasibility. Some utilities have provided financial support to developing new technologies although more on a project to project basis rather than a direct investment in the technologies.

A number of failures over the past decade have shown that it is quite easy to underestimate the difficulties involved in designing a robust WEC, given the extreme conditions to which it may be exposed. There is no standard design, although the development has gained pace in the past decade. There are at least two dozen designs that are being considered for different wave conditions around the world [16].

One of the most advanced WECs is the Pelamis wave energy generator, which has two grid connected P2-750 kW WECs deployed offshore at EMEC's Billia Croo test site. These were built for utility customers E.ON and Scottish Power Renewables. The project utilizes electrical subsea cables, a substation and grid connection at EMEC.

Pelamis is also developing wave farms ranging from 10 MW to 20 MW at Farr Point, Shetland, Bernera and Agucadoura [12].

The WEC development has picked up pace in the USA, with Ocean Power Technologies, Colombia Power Technologies, Ecomerit Technologies, Waveberg and others testing their prototypes, scaled and fully developed machines.

1.4 Northwest National Marine Renewable Energy Center

The Northwest National Marine Renewable Energy Center (NNMREC) is one of three U.S. Department of Energy-funded centers charged with facilitating the development of marine renewable energy technology, with the other two locations in Florida and Hawaii. NNMREC was established in 2008 as a partnership between Oregon State University (OSU), University of Washington (UW) and the National Renewable Energy Laboratory (NREL). OSU focusses on wave energy, whereas UW emphasizes tidal energy. Center activities of the NNMREC include:

i) Development of facilities to serve as an integrated, standardized test center for developers of wave and tidal energy.
ii) Evaluation of potential environmental, ecological and social impacts, focusing on the compatibility of marine energy technologies in areas with sensitive environments and existing users.
iii) Device and array optimization for effective deployments.
iv) Improved forecasting.

All of NNMREC's marine energy converter testing facilities are part of the Pacific Marine Energy Center (PMEC). These facilities can be leased by commercial WEC developers. PMEC includes scaled laboratory testing facilities for wave and tidal converters and intermediate and full-scale open water wave converter testing in both Oregon and Washington [17].

Facilities at Oregon State University campus include a linear test bed (see Figure 1.8) for dry testing of the WEC drive trains at the Wallace Energy Systems and Renewables Facility (WESRF) and two other wave tanks at the O.H. Hinsdale Wave Research Laboratory:

i) The Tsunami Wave Basin equipped with the capability of generating varying wave types ranging from regular, irregular, multidirectional or user defined, with a period ranging from 0.5 to 10s and wave velocity of 2 m/s (see Figure 1.9).
ii) The Large Wave Flume capable of creating regular, irregular, tsunami or user defined wave types with wave periods of 0.5 to 10s and wave height of 1.7m at 5s in2.7m water [18] (see Figure 1.10).

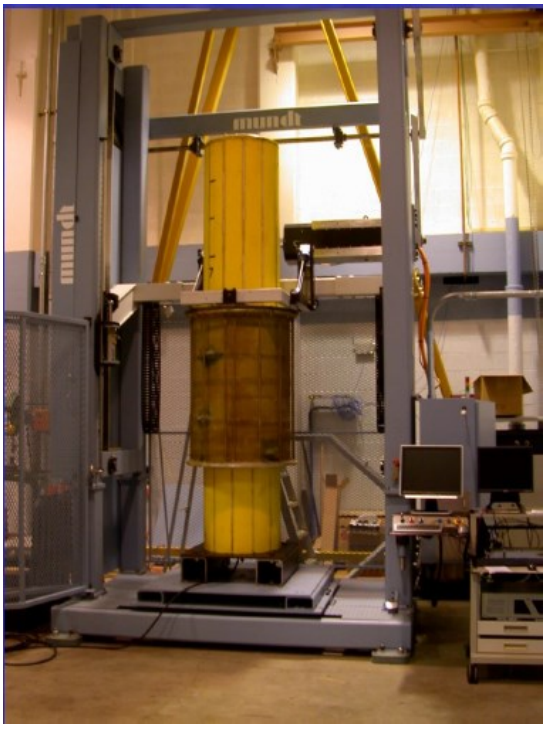


Figure 1.8. Linear test bed [17].

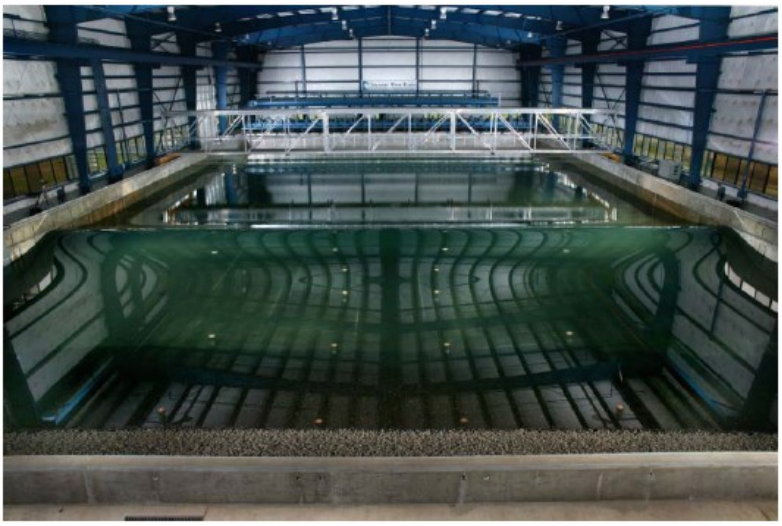


Figure 1.9. Tsunami Wave Basin [18].

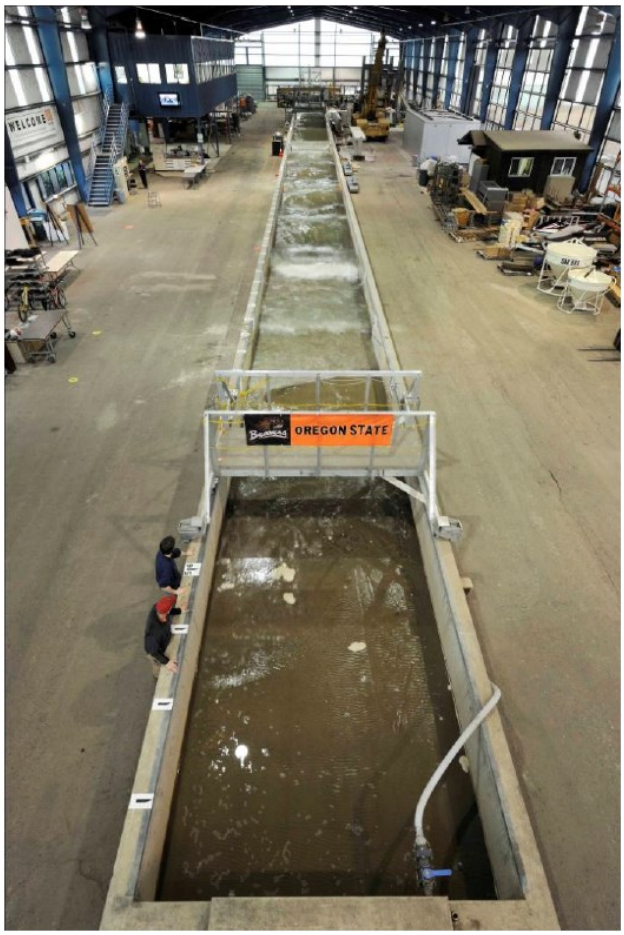


Figure 1.10. Large Wave Flume [18].

NNMREC's wave energy open-ocean testing facilities are being developed in a multi-step process. The PMEC North Energy Test Site (NETS), established in 2012 is intended for stand-alone testing of scaled WEC devices up to 100 kW that are ready for field trials, but are not sufficiently mature to be connected to the electrical grid for commercial power production. PMEC-NETS is now a permitted open ocean test site north of Newport, OR, ranging in depth from 45-52 m and located 2-3 miles from shore. NNMREC has developed the Ocean Sentinel Instrumentation Buoy to facilitate stand-alone WEC testing at this site. The Ocean Sentinel is a floating platform that can be deployed at the test site along with the device being tested; when connected to the device being tested through an umbilical cable, the Ocean Sentinel can provide the electrical interface and loading necessary for stand-alone operation [17,19].

Figure 1.11. NNMREC's PMEC open ocean test sites [17].

1.5 South Energy Test Site

NNMREC's open ocean grid connected test facility, the South Energy Test Site (SETS), located in Newport, Oregon is the first proposed utility scale, cable-to-shore, grid connected wave energy test site in the US [19]. SETS, ranging in depth from 60-70 m and 5-6 miles from shore, will offer up to four test berths connected by subsea cables to a substation onshore. Each test berth will be capable of testing prototype and commercial scale wave energy converters or arrays and is expected to be available in ~2017. The onshore facility will house a grid emulator to enable WEC developers to test synchronization, power delivery, characterization of electrical generator performance, power quality verification and fault testing before a device is directly connected to the actual power grid. Appropriate switchgear at the onshore facility would enable a single device (or cable) from the PMEC-SETS, or an array of devices (or multiple cables) to be connected to the grid emulator (see Figure 1.12).

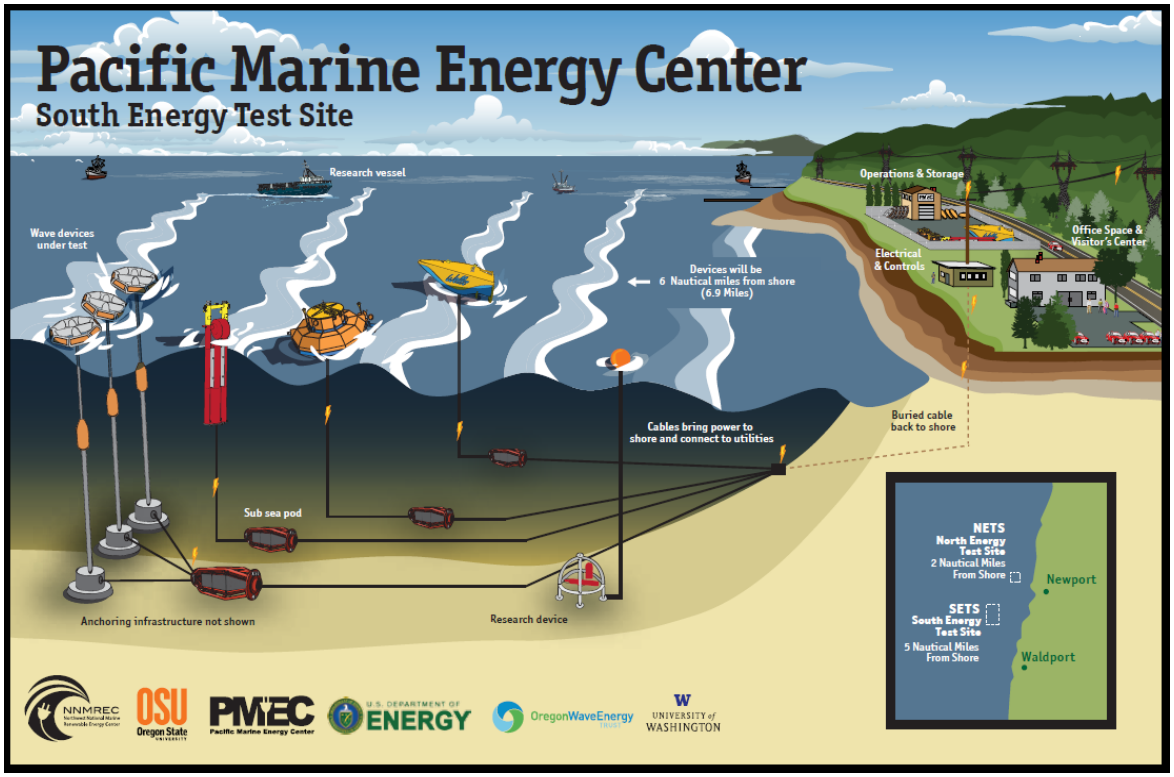


Figure 1.12. Pacific Marine Energy Center – South Energy Test Site [17].

1.6 Grid Emulator

The tremendous potential of wave energy, spurred by advancements in WEC developments, calls for further research on the integration of this source of energy to the power grid. Wave energy, being a relatively new source of renewable energy, does not have a standardized mechanism of energy extraction. WECs being developed around the world have different power take-off mechanisms, and when connected to the distribution grid, can introduce fluctuations in the grid voltage due to their variable power output, which is primarily a function of the intensity of the wave at any given point in time and the dominant wave period. This variable power generation could adversely affect the normal operation of other loads and generators connected to the grid. The stability of the electric power grid varies from point to point and with time, determined by the level of generation, loads and power system equipment operation. WECs, when connected to a point on the grid should be able to handle grid disturbances and generate outputs in compliance with grid standards [20]. In case of grid faults, it is not practical to disconnect and reconnect grid-interconnected systems [21]. WECs, when connected to a point on the grid should be able to handle grid disturbances and generate outputs in compliance with grid standards. Hence, it becomes increasingly necessary to test the generator's ability to ride-through short-duration grid disturbances using a grid emulator.

In recent years, the increasing integration of renewable energy resources to the electric grid has driven the need for a grid emulator device designed to emulate different grid conditions. The variable nature of the WEC power has been one of the main hurdles in its development as a major source of generation [22]. This variable power generation could affect the normal operation of loads and generators connected to the grid. This makes it necessary for them to be assessed and validated before connection to the power grid. This gives rise to the development of a grid emulator that will be able to emulate different grid conditions, thereby evaluating the performance of the WECs under a variety of grid conditions and certifying their grid compatibility. The grid emulator under development by NNMREC will not only enable WEC developers to

test the synchronization and power delivery of their devices to a conventional power grid, but also advise the local utility to ensure the connection of WECs without negative impacts on the grid. Developers would be able to test generator performance, verify power quality and conduct device fault testing.

2. GRID EMULATOR

Various topologies have been proposed for a grid emulator and only a few options are available in the market. The grid emulator can be a standalone device powered by a conventional energy source, or a device that draws power from an existing electric infrastructure. A few existing and proposed designs for grid emulators are discussed in this chapter.

2.1 NREL's Technologies:

NREL proposed two grid simulator topologies for standalone offshore operation of wind turbines. A key factor for the stable operation of a power system is the continuous matching between generation and load. A controllable load bank was included as part of the grid emulator for this purpose. The system should also be able to provide sufficient reactive power for the voltage support and transient stability. The two proposed methods are detailed below.

2.1.1 Battery and Inverter Based Grid Simulator Topology

The battery and inverter based grid simulator arrangement is shown in Figure 2.1. The design consists of a battery bank and an inverter. The inverter is used to maintain both the voltage and frequency of the grid or the system, enabling operation of the wind turbine. The fast-response resistive load bank is used for dynamic operation and control of the grid simulator. Smooth and continuous electric power can be enabled by fast rate of switching of the load bank. The power flowing to/from the battery is the difference between the turbine power and the ability of the load bank to absorb the same amount of power. If the load bank is completely matched with the turbine power, there will be no power flowing in or out of the battery. The power flow to the battery can be controlled by adjusting the load bank at a desired power level. The grid simulator supervisory control oversees the entire system operation, taking care of the battery state of charge, operation/inhibition of the wind turbine, fault detection, protection, data logging, among others [23].

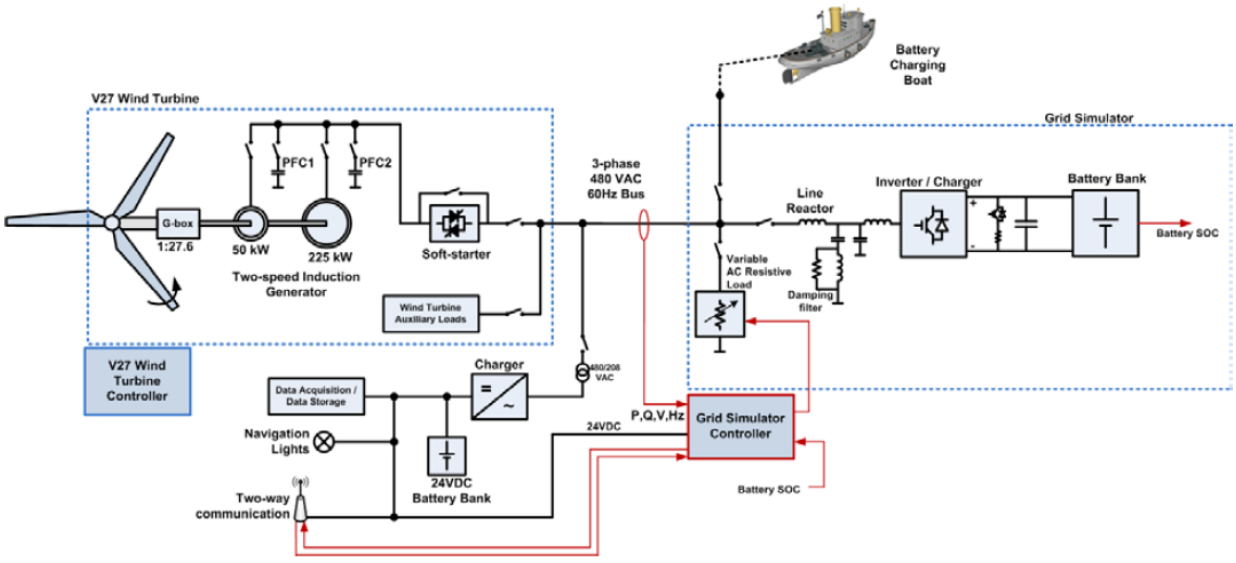


Figure 2.1. Battery/ Inverter topology [23].

2.1.2 Diesel Generator Based Grid Simulator Topology

The design of the diesel generator grid simulator topology is shown in Figure 2.2. It consists of a diesel generator and a resistive AC load bank for providing smooth load matching for the wind turbine power. The difference in this case is that the load bank is controlled based on the measured electrical frequency. The resistance on the load bank could be tuned to consume more power in case of a frequency swell and may consume very little power in case of a frequency dip. The main purpose of the diesel generator is to provide the deficit power required by the grid to maintain the grid frequency and voltage, it should also be capable of providing the reactive power needed during the start-up of the wind turbine. A similar supervisory control is employed in this case which takes care of the load bank tuning, operation or inhibition of the wind turbine, operation of the diesel generator, and data logging among others [23].

The capacity of the diesel generator used in the topology can be reduced with the use of synchronous condenser along with the diesel generator topology. The diesel generator is used to set up the system voltage and frequency, the synchronous generator is brought up to speed and synchronized with the diesel generator. The diesel generator could be turned off after connecting the synchronized condenser to the main bus. The load bank could be controlled to maintain the system frequency.

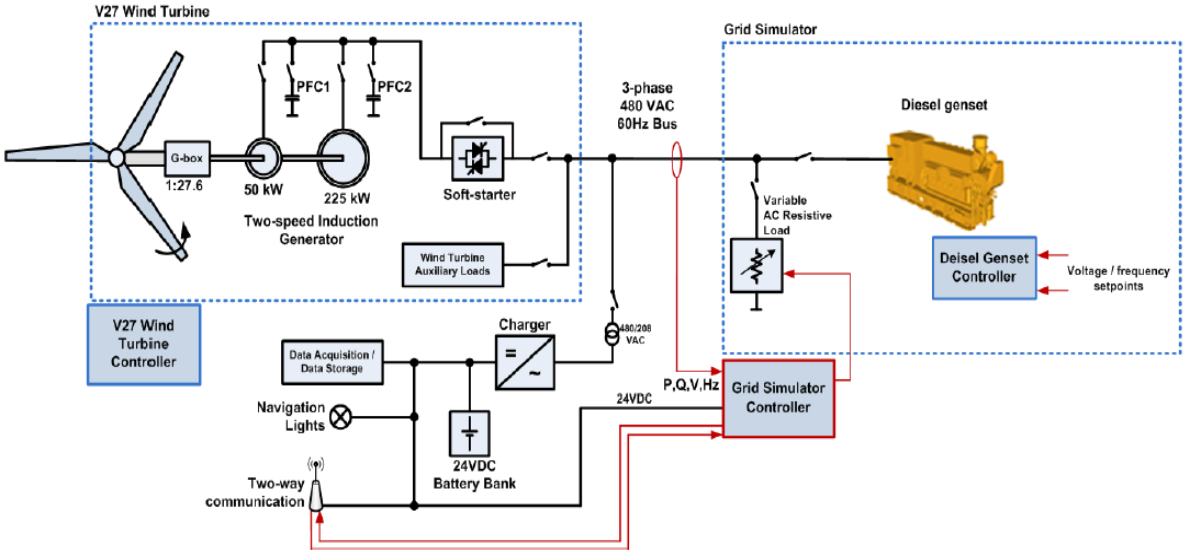


Figure 2.2. Diesel Generator topology [23].

2.1.3 NREL's Controllable Grid Interface

NREL has developed a power electronic Controllable Grid Interface (CGI) (see Figure 2.3) capable of testing utility grid connection of wind, solar, energy storage devices and other renewable energy. CGI has facilities for Hardware-In-the-Loop (HIL) testing of wind turbines using the National Wind Technology Center's dynamometers, utility scale solar and wind turbines and energy storage devices. The CGI is capable of generating various grid disturbances and effects of generator responses on the grid. CGI makes use of ABB's ACS6000 electrical topology for variable frequency drive converter blocks. The unit is composed of four inverters on the test article side, thereby capable of providing high short circuit currents. The inverters are connected to

a unique transformer layout allowing each phase to be controlled individually. The CGI is rated at 7 MVA with a 39 MVA short circuit capacity for 2 s. It is also capable of generating all kinds of frequency anomalies that might exist in a power system [24].

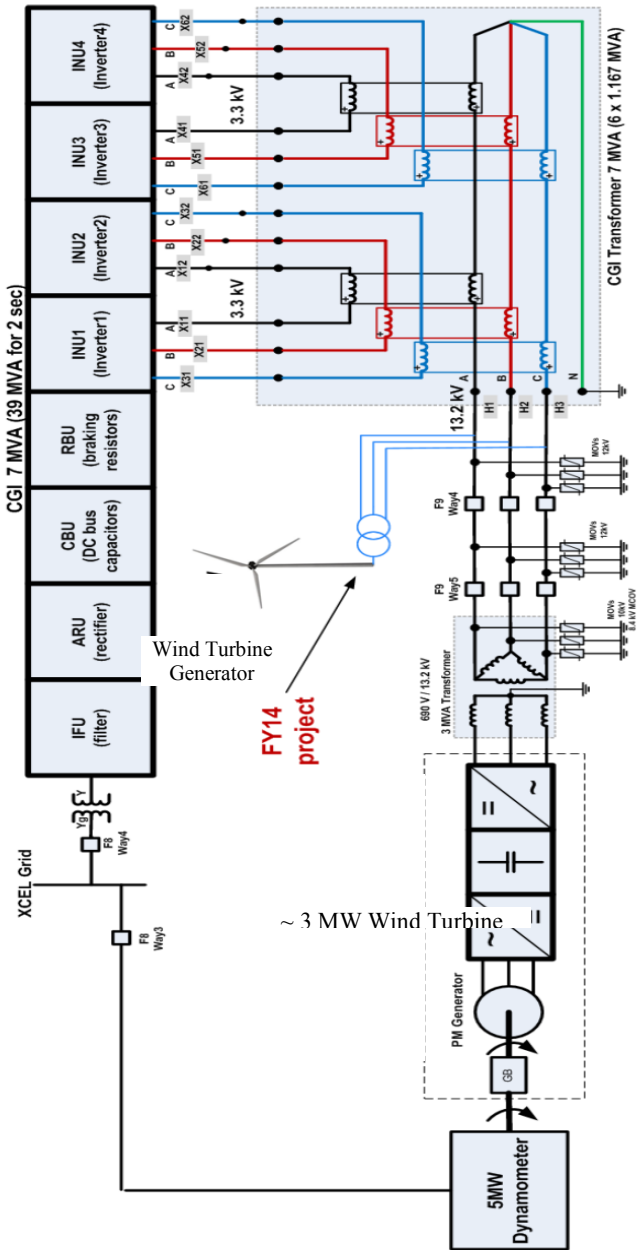


Figure 2.3 NREL's CGI interconnection (*Courtesy of NREL*).

2.2 Clemson University

A HIL grid simulator using eight parallel seven level Series-Connected H-Bridge (7L-SCHB) converter topology is being developed by Clemson University. The system uses Real-Time Digital Simulator (RTDS), capable of solving power system models in real time, it includes FACTs devices and a total of 192 system buses. The device is rated for a nominal power of 15 MVA, a nominal voltage of 24 kV, a frequency range from 45 – 65 Hz and capability to operate in 3 wire or 4 wire sequences. The device is capable of power quality evaluations, grid fault ride-through testing, and open loop testing. This device can be used over a multitude of applications such as micro-grid, distributed generation, solar PV converter and EV charging stations [25].

2.3 Other Topologies

The design and control of a hardware grid simulator for lab testing of grid-connected inverter systems was proposed by researchers at the Indian Institute of Science (IISc.). The system uses a high power inverter capable of generating voltages to simulate different fault conditions in a power system. In order for the over-current resulting from faults on the power system not to trip the grid simulator, the inverter used was rated for a higher power capacity than the system. A back-to-back inverter set-up, along with a controller board was used in order to supply active, reactive and harmonic power (see Figure 2.4). The impedances in the power system were emulated by taking the difference between the inverter voltage, $v_{grid}(t)$ and the voltage drop caused due to the grid impedance, $v_{drop}(t)$.

$$v_{ref}(t) = v_{grid}(t) - v_{drop}(t)$$

Where,

$v_{ref}(t) is\ the\ reference\ voltage\ for\ the\ inverter$

The impedance calculations are done in the controller and there are no actual physical impedances involved, therefore adding the flexibility of emulating different impedances, allowing emulation of different situations depending upon site conditions.

The emulation of the voltage drops due to resistance $v_{drop_R}(t)$ and inductance $v_{drop_L}(t)$ were calculated as follows.

$v_{drop_R}(t) = R.i(t)$ and $v_{drop_L}(t) = L.\frac{di(t)}{dt}$

The waveforms for the different test situations were achieved by using a timed zone approach consisting of five zones.

Zone 1 maintains the nominal grid voltage and frequency over a period of time until the fault starts. Zone 2 exists for one cycle of the sine wave, at the end of which, the zero crossing point is reached. Zone 3 selects the angle at which the fault occurs. Zone 4 represents the voltage magnitude and frequency of the fault. Zone 5 represents the system's switch back to nominal operating conditions. The disturbances itself were created by programming the controller to generate waveforms under different X/R ratios of the grid [21].

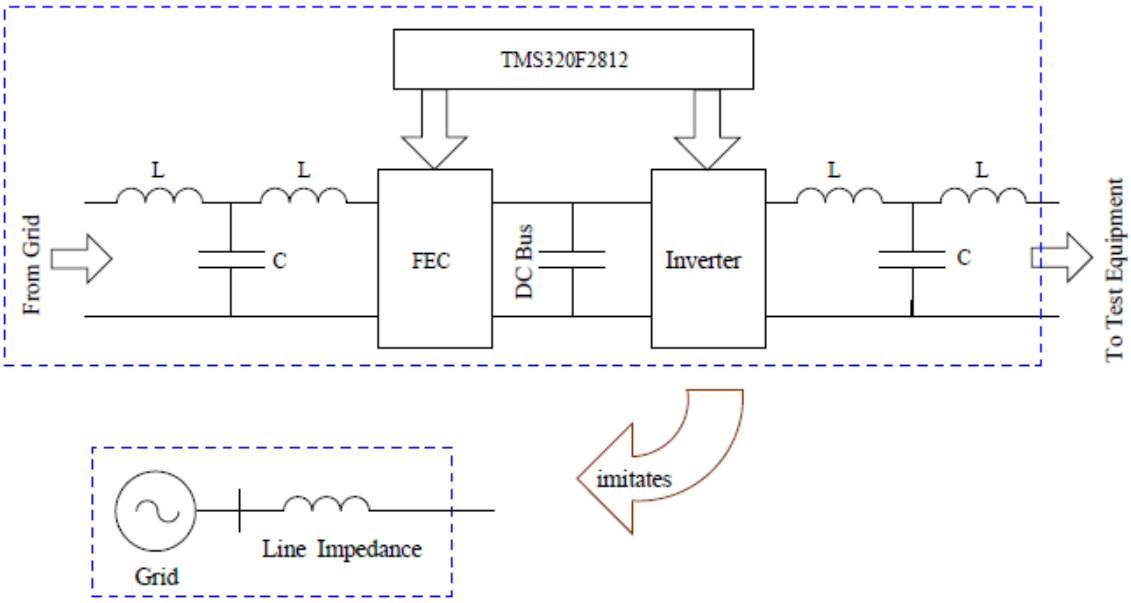


Figure 2.4. Grid simulator hardware set-up [21].

Another approach for a grid emulator development has been proposed by researchers at the University of Kiel, Germany. The proposed system is able to reproduce various types of distributed grid voltages like symmetrical and unsymmetrical voltage dips,

overvoltage, harmonic disturbances and frequency variations. The system employs static control methods and state space control methods for good dynamic performance. The system is rated at 30 kVA, has a nominal output voltage of 400 V and is able to handle peak currents up to 150 A. In order to generate arbitrary output voltages, independent of the mains, and to keep the penetration of the mains caused by the test setup as low as possible, the grid emulator is switched sequentially between the mains and the investigated system. The test system is a back to back converter connected permanent magnet synchronous generator (see Figure 2.5). The line side converter maintains the voltage on the DC link and serves as a power supply for the grid emulator and therefore, for the test system. The line side converter is designed to the nominal active power of the test bench. The DC link has the ability to decouple the emulator side converter from the line side converter, thereby having the capacity to provide short term higher currents than the mains allow. The inverter output voltages were generated utilizing a PWM controller. An LC filter was used to keep the ripple in the output voltage below one percent in order for them to have the quality of mains [26].

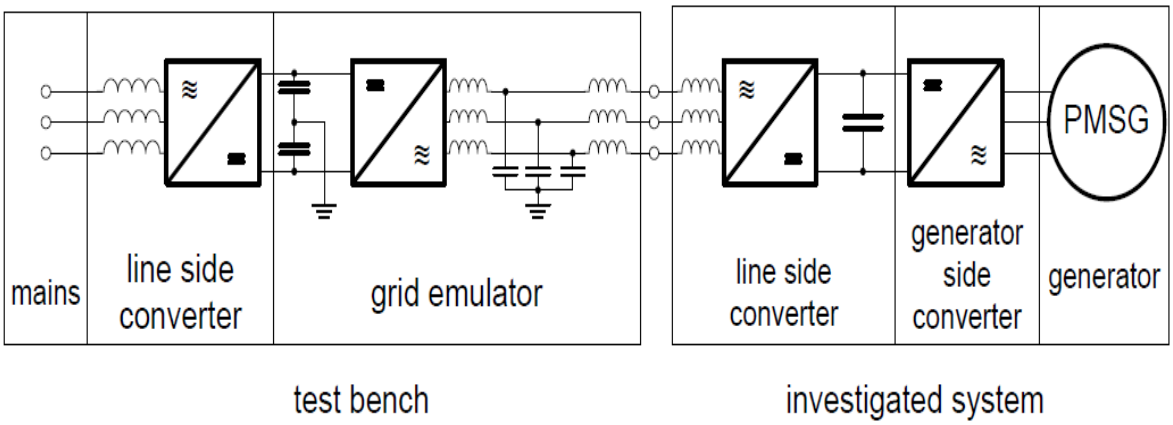


Figure 2.5. Overview of the structure of the test bench with connected investigated system [26].

2.4 Resource Induced Flicker in Wave Energy Converters

This section provides a preliminary 'go/no-go' flicker assessment for a WEC. In the case of WECs, the wave resource has a typical period of 5-20 s depending on the location of the site. Mechanical power is produced twice per wave cycle and therefore has half the period of the input resource. This periodic change in the power produces a change in the voltage, thereby a proportional change in the power at the same frequency. The coupling of these wave energy generators to the power grid has the potential to manifest itself as a flicker problem at the point of connection (POC). Flicker is measured in flicker severity and is normally given in terms of short-term flicker P_{st} and long-term flicker P_{lt}. The weighted average flicker severity over 10 min is P_{st} and the cubic average of P_{st}values over 120 min is P_{lt} [27]. IEC 61000-3-7 gives the flicker standards for medium voltage and high voltage connections [28].

2.4.1 Voltage Flicker Calculation:

The following analysis is taken from [28]. The voltage fluctuation (ΔU) caused by a load or generator at a node in the power system are calculated using the following analysis:

$$a = \frac{U_n^2}{2} - (RP + XQ)$$

$$b = (P^2 + Q^2) * Z^2$$

$$\Delta U = \sqrt{a + \sqrt{a^2 - b}}$$

Where,

U_n is the nominal system voltage

P and Q, are the amount of active and reactive power to or from the generator ($S = P + jQ$)

R and X, are the resistance and reactance of the grid at the POC ($Z = R + jX$)

The flicker emission is unity when it is at the threshold of perception. The unity threshold of flicker emission is shown in Figure 2.6 at 120 V and 230 V levels. At 8.8 Hz, the flicker unity is at its lowest value ($\sim 0.3\%$) of voltage fluctuation ($\Delta U/U$) [28]. The area of particular interest for wave energy is the frequency range of 0.05 – 0.2 Hz (typical wave period 5-20 s). Since the output power of a WEC is at double the frequency of the source, the range of actual interest reduces to 0.1 – 0.4 Hz, as seen in Figure 2.7. This gives a voltage fluctuation range of $\sim 0.85 - 1.3\%$.

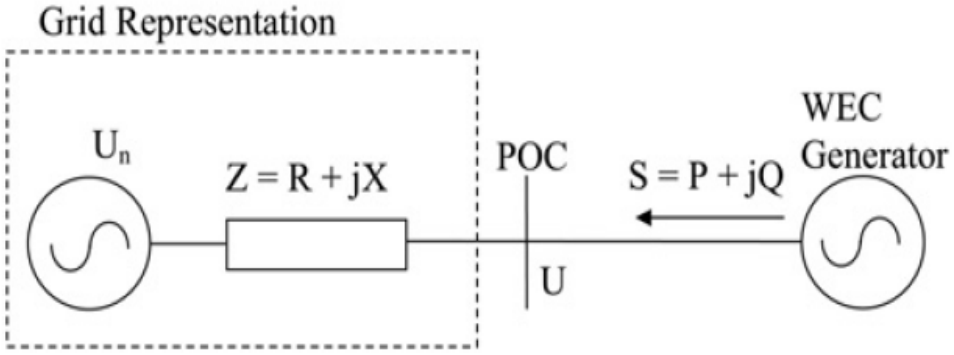


Figure 2.6. Simple representation of generator connected to the grid [28].

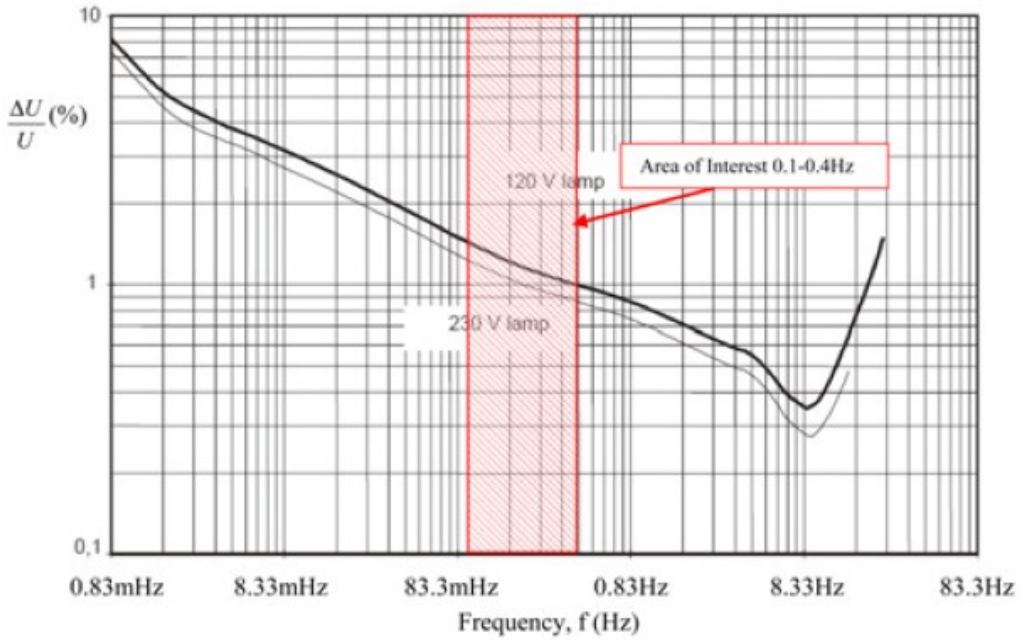


Figure 2.7. Voltage fluctuation corresponding to flicker emission unity threshold for 120 V and 230 V lamp [29].

2.4.2 Flicker assessment

2.4.2.1 Basic Flicker Assessment

As a first pass, assessment of potential flicker can be done by the assessment of percentage voltage change for a balanced three phase voltage system, given in [28],

$$\Delta U(\%) = \frac{100 * S_n}{S_k}\%$$

Where,

S_n *is the nominal generator power (MVA)*

S_k *is the short-circuit power (MVA) or fault level*

A value $> 0.85 - 1.3\%$ indicates that the generator exceeds the flicker limits. However, this method makes a number of assumptions, resulting in potentially inaccurate analysis.

2.4.2.2 Flicker Assessment Charts

For a quick and more accurate flicker assessment of the generator, flicker assessment charts have been developed in [28]. A flicker assessment chart has the unity flicker plots for different generator power factors, with grid X/R ratio on the abscissa and ratio of fluctuating generator power to the grid fault level $\Delta S_n/S_k$ on the ordinate. However, in [28] the charts have been developed based on the following assumptions.

(i) The power output is assumed to be continuously oscillating with a fixed amplitude and frequency.
(ii) The power oscillation is assumed to occur at the most flicker severe frequency, i.e., 0.4 Hz.
(iii) The power oscillations are assumed to be rectangular, which is the worst case.

Along with the following assumptions, the following set of data is necessary to utilize the graphs:

(i) Grid fault level, S_k- can be derived from the grid impedance, Z or short-circuit current, I_k.
(ii) Grid X/R ratio.
(iii) WEC maximum power fluctuation(ΔS_n).
(iv) WEC output power factor($cos\ \theta$).
(v) P_{st} and P_{lt} limits at the POC.

Knowing the system parameters, a suitable graph is selected for a WEC. The intersection of $\Delta S_n/S_k$ and X/R is marked. If the intersection lies above the applicable power factor line, then there will be a potential issue with flicker for the chosen system parameters. If it lies below, then there will be no issue with flicker even in the worst case scenario. A flicker assessment chart with three examples in Table 2.0 is shown in Figure 2.8.

Table 2.0. Parameters to use the flicker assessment charts [28].

Parameters	**Example 1**	**Example 2**	**Wavebob**
$\Delta S_n/S_k$ %	2.5	3.3	0.00164
Grid X/R ratio	2	5	1.87
WEC power factor (cosθ)	1	1	1

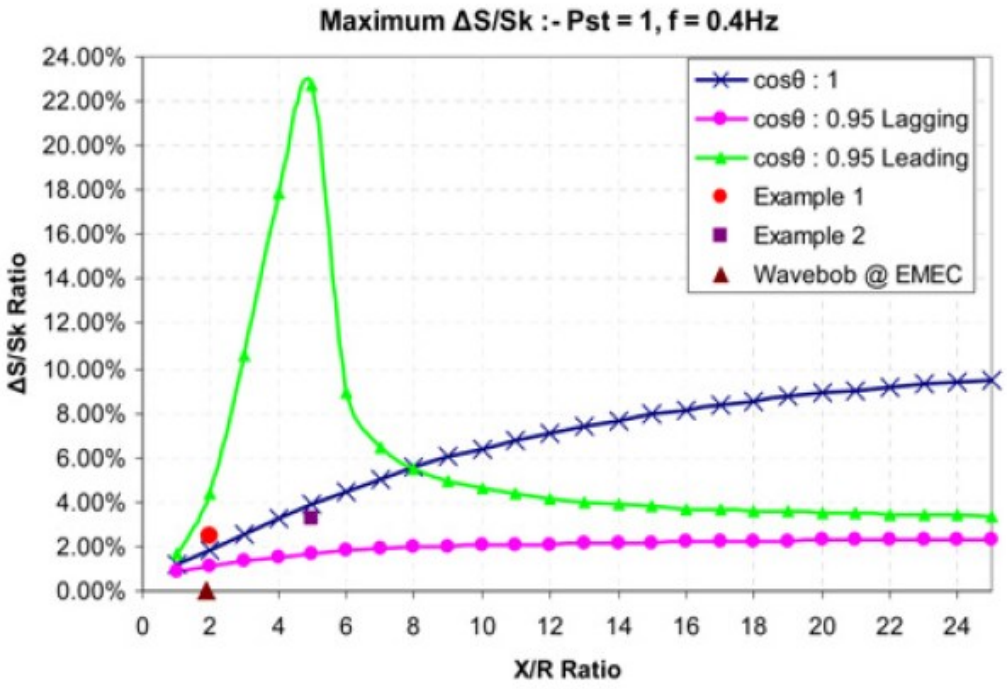


Figure 2.8. Flicker assessment chart along with example generator intersections [28].

3. DESIGN SPECIFICATION

3.1 Introduction

In the previous chapter, various grid emulator topologies and their ratings were discussed. Extensive research was carried out to identify the first potential customers at the grid connected wave energy testing site (PMEC-SETS). Wave energy device manufacturers were surveyed in order to determine the ratings of the existing and proposed future development of WECs in order to come up with the power rating needed for the grid emulator under development. Also considered were the ratings of the submarine cable design, bus voltage, and grid conditions at the point of interconnection.

3.2 Grid Emulator Specifications

Table 3.0. Grid Emulator specifications.

Item	Specification
Nominal rating	5 MVA
Supply line voltage	12.47 kV
Line voltage tolerance	±10%
Phases	3
Nominal supply line frequency	60 Hz
Line frequency tolerance	±1 Hz
Grid impedance	5% min, 7% max on a 25 MVA base at 12.47 kV

Available fault current	14x min, 20x max on a 25 MVA base at 12.47 kV
Rectifier rating	5 MVA, 125 % overload capacity for short periods
Rectifier power factor	> ± 0.95
Inverter rating	5, 10, 15 MVA, 125 % current overload capacity
Output voltage regulation	± 1%
Output frequency regulation	50 Hz ±1% 60 Hz ±1%
Inverter output droop characteristics	± 10% system impedance
Inverter fault testing conditions	The output inverter shall generate or support the following fault conditions upon command: • Frequency variations: 50 or 60 Hz ±3 Hz at 1 Hz/s maximum rate, • Symmetrical voltage variations: 12.47 kV ±10%, at 1% V/s maximum rate, • Low Voltage Ride Through (LVRT) test prescribed in IEC 61400-21, utilizing the inductive voltage divider described there-in; This test includes symmetrical and non-symmetrical fault conditions created by the inductive fault simulator, • LVRT test will be performed without the IEC 61400-21 inductive voltage divider, with the inverter itself generating the symmetrical and non-symmetrical fault conditions; these test will be performed at reduced WEC MW ratings up to the current limit of the output inverter, • High voltage ride through testing as described in NERC PRC-

	02401_Draft1_2009 Feb17, • Sub-harmonic frequency oscillations: Voltage magnitude modulation oscillations of 10% at 3-10 Hz.
Rectifier/Inverter switching technology	NNMREC does not intend to specify switching technology for the rectifier or inverter, however, IGBT or IGCT technology is anticipated in the proposal.

3.3 Grid Emulator Architecture

The design of the grid emulator follows from the CGI developed by NREL at the NWTC. The topology uses five identical voltage source converters split into one grid-tie converter and 4 WEC-side converters. The converters use the topology of a Three Level Neutral Point Clamped Voltage Source Converter (3L-NPC-VSC). For ease of designing, the grid-tie converter is modeled as a rectifier and the WEC-side converters are modeled as an inverter. The four inverter topology is being used in order to increase the momentary short circuit current capacity of the grid emulator. The rectifier is connected to the distribution grid from which the system sources and sinks power. The WEC or the test equipment is connected on the output of the inverter through a transformer developing the required grid voltage level.

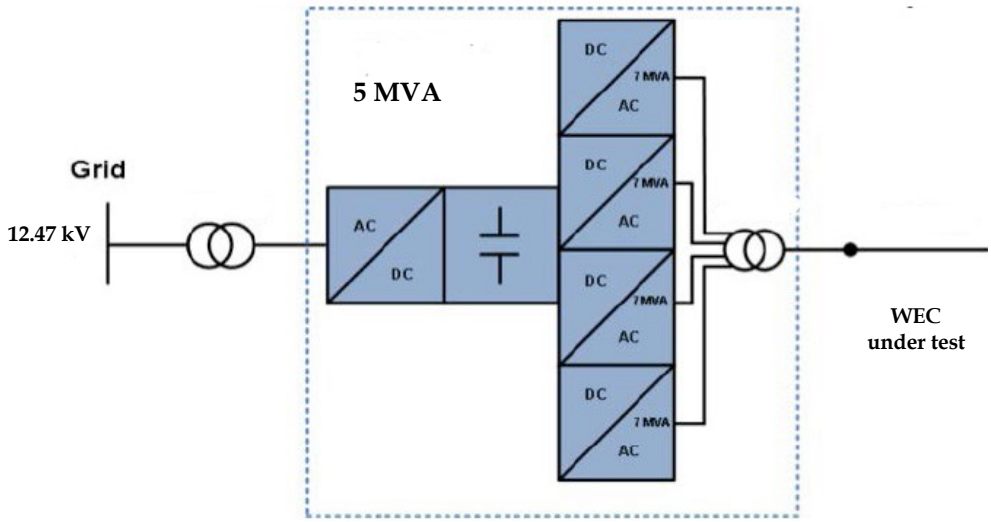


Figure.3.0. Grid Emulator topology [24].

3.4 Preliminary Functions

The grid emulator will primarily be used to test the synchronization and power delivery of WECs to a conventional power grid. The tests conducted using the grid emulator can also be used to advise the local utilities to ensure the connection of WECs without negative impacts to the grid. The grid emulator, in addition to allowing the testing of the WECs, provides electrical isolation between the grid and the distributed generators during testing. WEC developers would be able to test generator performance, verify power quality, and conduct device fault testing. The following tests for the WEC using the grid emulator are formulated in part based upon analogous previous studies on wind turbines:

i) Voltage fluctuation:
   a. Continuous operation
   b. Switching operation
ii) Current harmonics, inter-harmonics, high frequency components
iii) Response to balanced and unbalanced low and high voltage faults
iv) Active power:

a. Maximum measurement
b. Ramp rate limitation
c. Set point control
d. Inertial response

v) Reactive power:
a. Reactive power capability
b. Set point control

vi) Grid protection

vii) Reconnection time.

4. GRID EMULATOR SIMULINK MODEL

4.1 Introduction

Various proposed and existing grid emulator models were discussed in chapter two. This chapter describes the topology of the grid emulator being used in simulation and a detailed design of the controller used in the grid emulator modeling. Each of the converters in the grid emulator houses a Three-Level Neutral Point Clamped Voltage Source Converter (3L-NPC-VSC), with each converter capable of both rectification and inversion, thereby having the ability of being used as AC/DC or DC/AC converters interchangeably.

4.2 Three-Level Neutral Point Clamped Voltage Source Converter

The 3L-NPC-VSC was introduced by Nabae in 1981 [30] and is one of the most popular multilevel converter topologies for high voltage, high power applications. Most multilevel converters use odd number of voltage levels in order to access the neutral voltage. A 3L-NPC-VSC (see Figure 4.1) was chosen for the converter topology due to inherent advantages over a two level converter. In the case of a three level converter, each phase leg has four switches, resulting in each switch blocking only one half of the DC bus voltage (V_{dc}), in the case of a two level converter, the switch blocks the full DC bus voltage, therefore medium voltage rated semiconductors can be used to construct the converters for higher voltage, high power applications. In case of a three level converter, the output voltages have lesser harmonics due to the increased switching states.

4.2.1 Topology:

The following details have been derived from [31]. The topology of the 3L-NPC-VSC is shown in Figure 4.1. It has twelve unidirectional active switches having inverse diodes and six neutral point clamping diodes. The switches are categorized into outer switches and inner switches.

Outer switches: $T_{11}, T_{21}, T_{31}, T_{14}, T_{24}, T_{34}$

Inner Switches: $T_{12}, T_{22}, T_{32}, T_{13}, T_{23}, T_{33}$

Inverse diodes: $D_{11}, D_{21}, D_{31}, D_{12}, D_{22}, D_{32}, D_{13}, D_{23}, D_{33}, D_{14}, D_{24}, D_{34}$

Clamping Diodes: $D_{11c}, D_{21c}, D_{31c}, D_{12c}, D_{22c}, D_{32c}$

The switches are operated as complementary pairs. Switch T_{x1} and T_{x3} is one pair and switch T_{x2} and T_{x4} the other complementary pair.

The converter has three voltage states M_0 and M_2 which represent one half of the positive and negative of the DC bus voltage respectively and M_1 which is the zero DC bus center point. Each leg of the converter can be switched between these three voltage states.

$$M_0 = -\frac{V_{dc}}{2} = V_{c2}$$

$$M_1 = 0\ V$$

$$M_2 = \frac{V_{dc}}{2} = V_{c1}$$

Where,

$V_{c1}\ and\ V_{c2} are\ the\ voltages\ across\ capacitors\ C_1\ and\ C_2$

One challenge in this topology is maintaining the voltage balance in the two capacitors connected across the DC bus. The first solution to this is to connect each of the capacitors to an independent DC source. The other solution is to balance the capacitor voltages by feedback control [31].

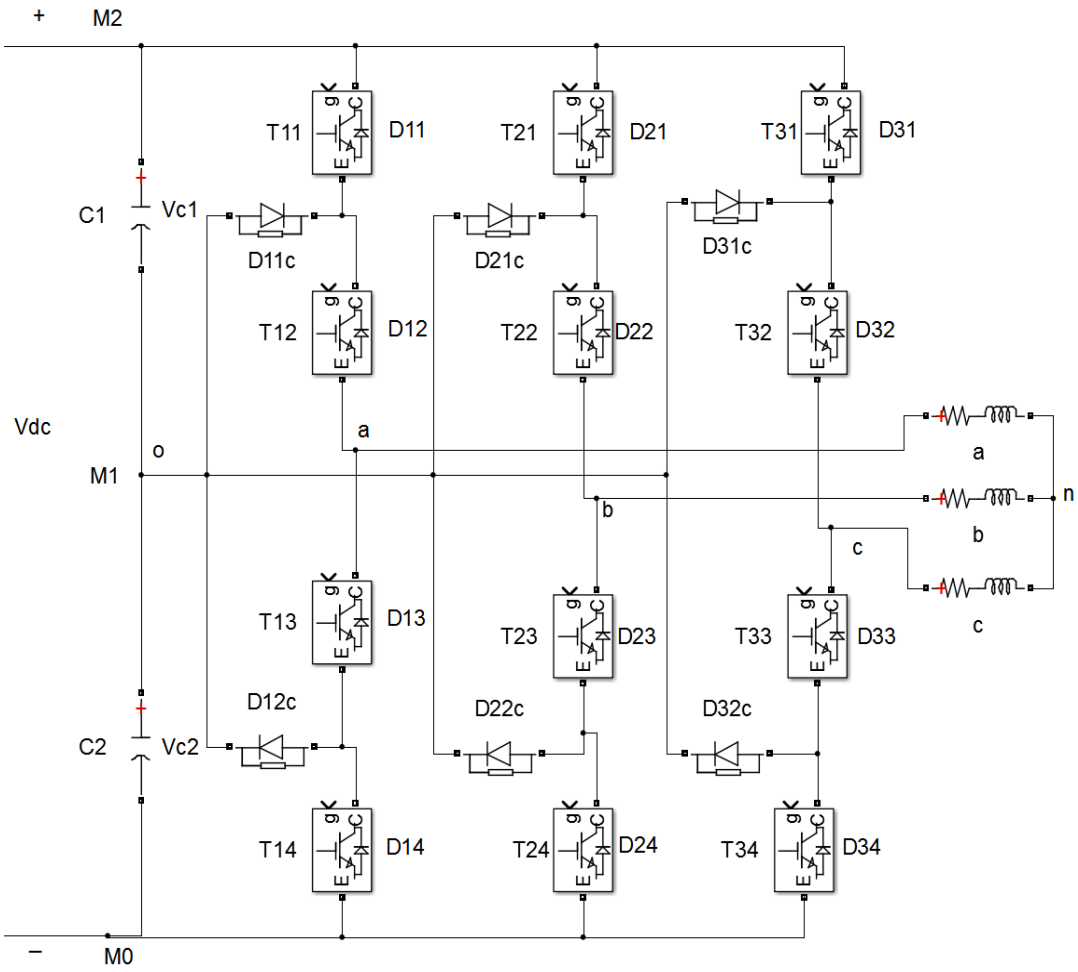


Figure 4.1. Three-Level Neutral Point Clamped Voltage Source Converter [31].

4.2.2 Switching States and Commutation

The converter is operated in such a way that only two of the switches in each leg are turned on or off at any time. The nodes of the three legs (a,b and c) can be connected to any of the three intersections of the capacitor bank (M_0, M_1, and M_2). The number of switching states will then be,

$$n = N^{ph} = 3^3 = 27$$

Where,

$n = Number\ of\ switch\ states$

$N = Number\ of\ voltage\ levels\ in\ the\ DC\ link$

$ph = Number\ of\ phases$

Three level converters behave like a two level converter when connected to the states M_0 and M_2 of the capacitor bank. These states can be achieved by simultaneously switching both T_{x1} and T_{x2} (x refers to any phase, a, b or c) on or off in each phase. Both these states yield a phase voltage equal in magnitude to half the DC bus, $\frac{V_{dc}}{2}$ or $-\frac{V_{dc}}{2}$. The connection to the state M_1 (0 V) is achieved by gating T_{x2} on and T_{x1} off, which results in switching on of the complementary switch T_{x3}. This state forces the current to flow into the junctions between the outer and the inner switch through the clamping diodes. If the current in a phase leg is positive, then the current flows through D_{x1c} and it flows through D_{x2c} if the current is negative. Therefore, both T_{x2} and T_{x3} should be turned on in the zero state to provide a conduction path in case the phase current reverses. Table 4.1 gives the phase voltage of each leg for different switch positions.

Table 4.1. Switch status on one phase of the 3L-NPC-VSC [31].

State (Phase voltage/leg)	$\boldsymbol{T_{x1}}$	$\boldsymbol{T_{x2}}$	$\boldsymbol{T_{x3}}$	$\boldsymbol{T_{x4}}$
Positive "M_2" $\left(\frac{V_{dc}}{2}\right)$	ON	ON	OFF	OFF
Zero " M_1" (0)	OFF	ON	ON	OFF
Negative " M_0 " $\left(-\frac{V_{dc}}{2}\right)$	OFF	OFF	ON	ON

In any of the switch states, two semiconductors in each phase lie in series within the current path; two active switches, two diodes, or a diode and an active switch. For a positive current in each phase, i.e., current flowing from the DC source to the load, the

active switches T_{x1} and T_{x2} conduct in the positive state, the diode D_{x1c} and active switch T_{x2} conduct in the zero state, and the diodes D_{x3} and D_{x4} conduct in the negative state. In case of a negative current flowing in the converter (from load to the source), the diodes D_{x1} and D_{x2} conduct in the positive state, the diode D_{x2c} and active switch T_{x3} conduct in the zero state, and the active switches T_{x3} and T_{x4} conduct in the negative state. Table 4.2 shows the conduction losses that occur for different current flows [31].

Table 4.2 Conduction losses in a 3L-NPC-VSC [31].

State	T_{x1}	D_{x1}	T_{x2}	D_{x2}	T_{x3}	D_{x3}	T_{x4}	D_{x4}	D_{x1c}	D_{x2c}
Positive phase current										
Positive	X		X							
Zero			X						X	
Negative						X		X		
Negative phase current										
Positive		X		X						
Zero					X					X
Negative					X		X			

The commutation for the transition from a positive state to zero state can be described using a positive phase current. In the positive state, the current is flowing through the active switches T_{x1} and T_{x2} with T_{x3} and T_{x4} turned off. The transition from positive to zero state is initiated by the commutation of the active switch T_{x1} from on to off, thereby forcing the current to flow through diode D_{x1c}. After T_{x1} has completely turned off (including the dead time – duration for which no device conducts), the switch T_{x3} is turned on, while T_{x4} remains turned off. During this process, D_{x1c} doesn't experience significant turn on loss since it doesn't take over a voltage,

however, the switch T_{x1} experiences a turn off loss. The switch T_{x3} although turned on, does not experience a loss since it doesn't carry any current.

In case of reverse commutation for a positive current (from zero to positive state), all the switching transitions occur in reverse direction. Firstly, T_{x3} is turned off and T_{x1} is turned on after a dead time, transferring the voltage in that phase back to the positive bus. T_{x3} doesn't experience any loss since it doesn't conduct any current, however, diode D_{x1c} experiences a recovery loss and T_{x1} experiences turn on loss.

In case of transition from the zero state to negative state two devices are turned off and two devices are turned on. In the zero state, the diode D_{x1c} and switch T_{x2} are conducting. The active turn off of the switch T_{x2} changes the path of the current from D_{x1c} and T_{x2} to diodes D_{x3} and D_{x4}. The active switch T_{x3} would be on through both the states. The switch T_{x4} is turned on after a dead time, post turn off of T_{x2}. T_{x2} experiences turn off loss, D_{x1c} doesn't experience a turn off loss since there is no significant voltage across it after commutation [31].

In case of reverse commutation from the negative to zero state, the active switch T_{x4} is first tuned off, after a dead time, the active switch T_{x2} is turned on, the diodes in D_{x3} and D_{x4} stop conducting thereby changing the path of the positive current from diodes D_{x3} and D_{x4} to D_{x1c} and active switch T_{x2}. Switch T_{x2} experiences turn on loss and since all the blocking voltage is applied across the diode D_{x4}, the diode D_{x4} experiences recovery loss. The switching losses are represented in the Table 4.3.

Table 4.3 Switching losses in a 3L-NPC-VSC [31].

State	T_{x1}	D_{x1}	T_{x2}	D_{x2}	T_{x3}	D_{x3}	T_{x4}	D_{x4}	D_{x1c}	D_{x2c}
Positive phase current										
+ $\longleftrightarrow$ 0	X								X	
0 $\longleftrightarrow$ -			X					X		
Negative phase current										

+ ⟷ 0		X			X					
0 ⟷ -							X			X

4.2.3 Converter Output Voltage Levels

The output voltage at each phase leg V_{xo} can be determined using the equation:

$$V_{xo} = \frac{V_{dc}}{2} * (m_{x1} - m_{x3})$$

The variables m_{x1} and m_{x3} represent the switch combinations T_{x1} & T_{x2} and T_{x3} & T_{x4} in each phase leg. They are one when both the switch pairs are on and zero otherwise. The output phase to neutral voltages can be determined using the equations below [32]:

$$V_{an} = \frac{2}{3} * \frac{V_{dc}}{2} * [(m_{a1} - m_{a3} - \left(\frac{1}{2}\right) * (m_{b1} - m_{b3} + m_{c1} - m_{c3})]$$

$$V_{bn} = \frac{2}{3} * \frac{V_{dc}}{2} * [(m_{b1} - m_{b3} - \left(\frac{1}{2}\right) * (m_{a1} - m_{a3} + m_{c1} - m_{c3})]$$

$$V_{cn} = \frac{2}{3} * \frac{V_{dc}}{2} * [(m_{c1} - m_{c3} - \left(\frac{1}{2}\right) * (m_{a1} - m_{a3} + m_{b1} - m_{b3})]$$

The output line voltages can be computed:

$$V_{ab} = V_{ao} - V_{bo} = \left(\frac{V_{dc}}{2}\right) * (m_{a1} - m_{a3} - m_{b1} + m_{b3})$$

$$V_{bc} = V_{bo} - V_{co} = \left(\frac{V_{dc}}{2}\right) * (m_{b1} - m_{b3} - m_{c1} + m_{c3})$$

$$V_{ca} = V_{co} - V_{ao} = \left(\frac{V_{dc}}{2}\right) * (m_{c1} - m_{c3} - m_{a1} + m_{a3})$$

With this ability to generate three voltage levels at each phase leg, the 3L-NPC-VSC is capable of generating five unique line-to-line voltage levels and nine unique phase to

neutral voltage levels caused by imparting the neutral voltage on the phase to midpoint voltage.

Line-line voltage levels: $\pm V_{dc}$, $\pm\frac{V_{dc}}{2}$ and 0 V

Phase to neutral voltage levels: $\pm\frac{2V_{dc}}{3}$, $\pm\frac{V_{dc}}{2}$, $\pm\frac{V_{dc}}{3}$, $\pm\frac{V_{dc}}{6}$ and 0 V.

4.2.4 Sine-Triangle Modulation

To obtain the three phase balanced sinusoidal output voltages, various modulation strategies could be used, such as staircase modulation, carrier based multilevel pulse-width modulation, switching optimal pulse-width modulation and space vector modulation [33]. Carrier based pulse with modulation was chosen in this design due to its simplicity.

The switching signals are generated by comparing a pair of two stepped triangle waveform with three balanced sinusoidal waveforms which are 120° out of phase with each other. A frequency modulation (m_f) of 9 is used taking into account future hardware development of the design. The following strategy is used in order to trigger the switches:

$$U_{sine} > U_{tri\_up} \Longrightarrow V_{xo} = \frac{V_{dc}}{2}$$

$$U_{sine} < U_{tri\_low} \Longrightarrow V_{xo} = -\frac{V_{dc}}{2}$$

$$else \Longrightarrow V_{xo} = 0$$

The controlled three phase reference voltage used in this case is a sinusoidal waveform, given by:

$U_{sine}(t) = \overline{U}_{sine} * \sin(wt)$

Where,

$\overline{U}_{sine} = peak\ of\ the\ desired\ fundamental\ component$

Figure 4.2 shows the three phase sinusoidal control signal and the two level triangular waveforms. The switching signal for the switch T_{x1} is generated by the comparison of the control signal with the upper triangular carrier waveform, as shown in Figure 4.3.

The complementary of this switching signal is fed to the switch T_{x3}. Switching signal for the switch T_{x2} is generated by the comparison of the sinusoidal control waveform with the lower triangular carrier waveform, as shown in Figure 4.4. The complementary of this signal is fed to the switch T_{x4}.

Figure 4.5 shows the phase to midpoint voltage for a single phase. This voltage varies between the three DC bus voltages of $\frac{V_{dc}}{2}$, 0 and $\frac{-V_{dc}}{2}$.

Figure 4.6 and Figure 4.7 shows the five level line to line voltage and the nine level phase to neutral voltage (imparted due to the imposition of neutral voltage on the phase to midpoint voltage) respectively.

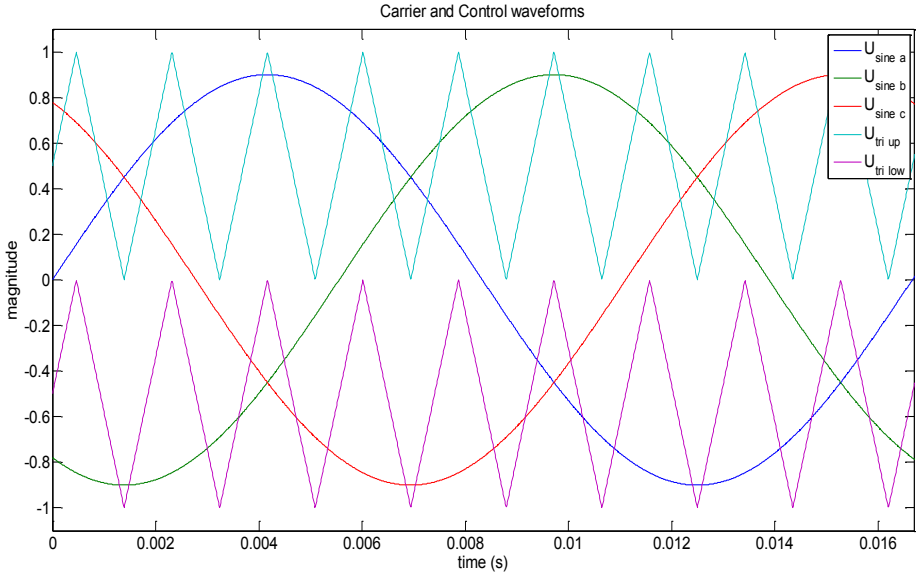


Figure 4.2. Sinusoidal control and dual triangle carriers.

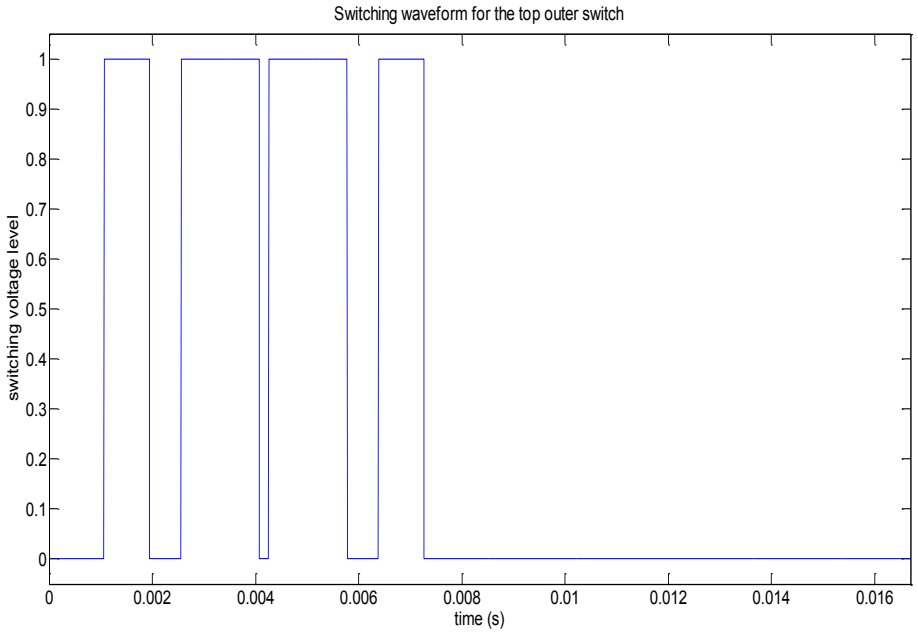


Figure 4.3. PWM signal for switches T_{x1}(physical model).

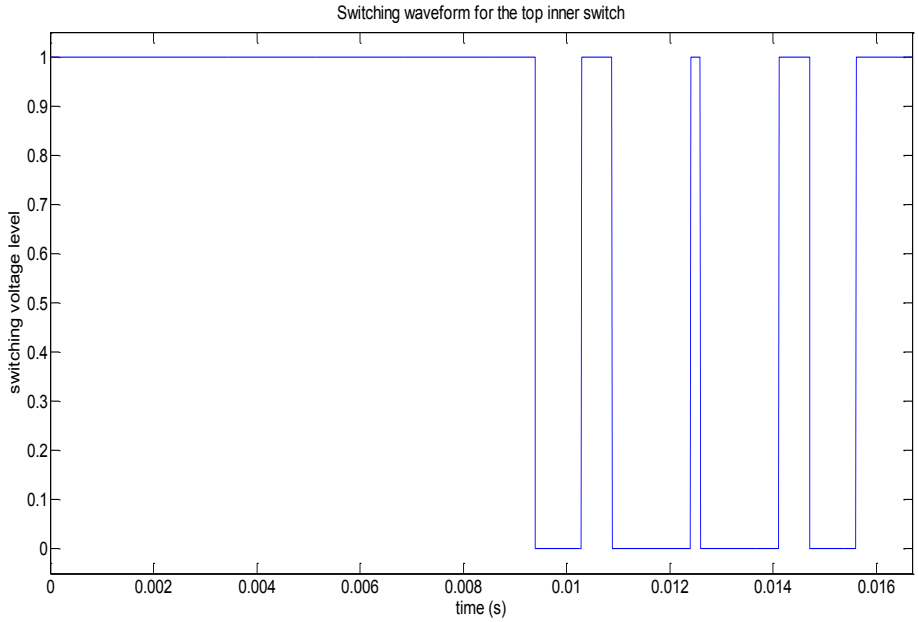


Figure 4.4. PWM signal for switches T_{x2}(physical model).

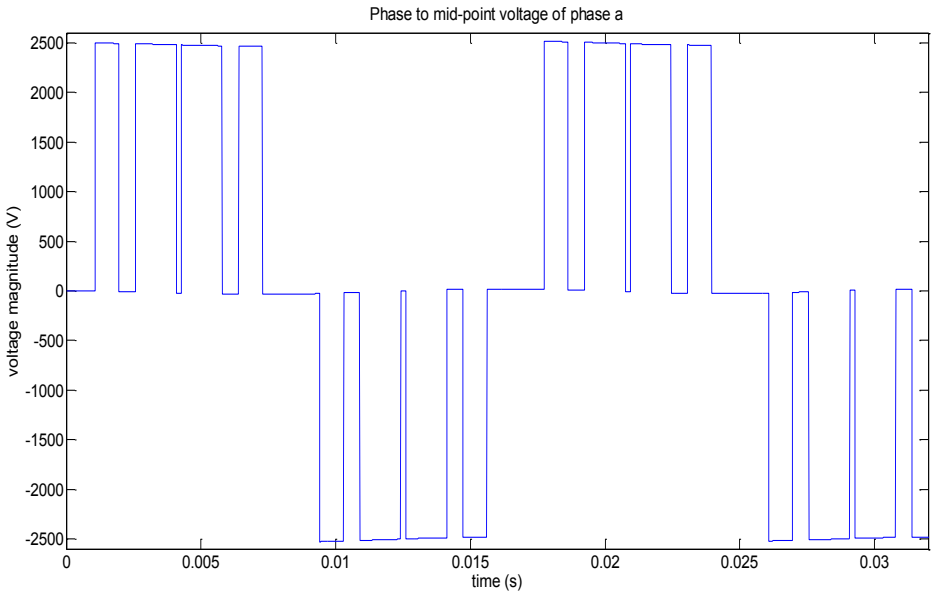


Figure 4.5. Phase to midpoint voltage of the converter (physical model).

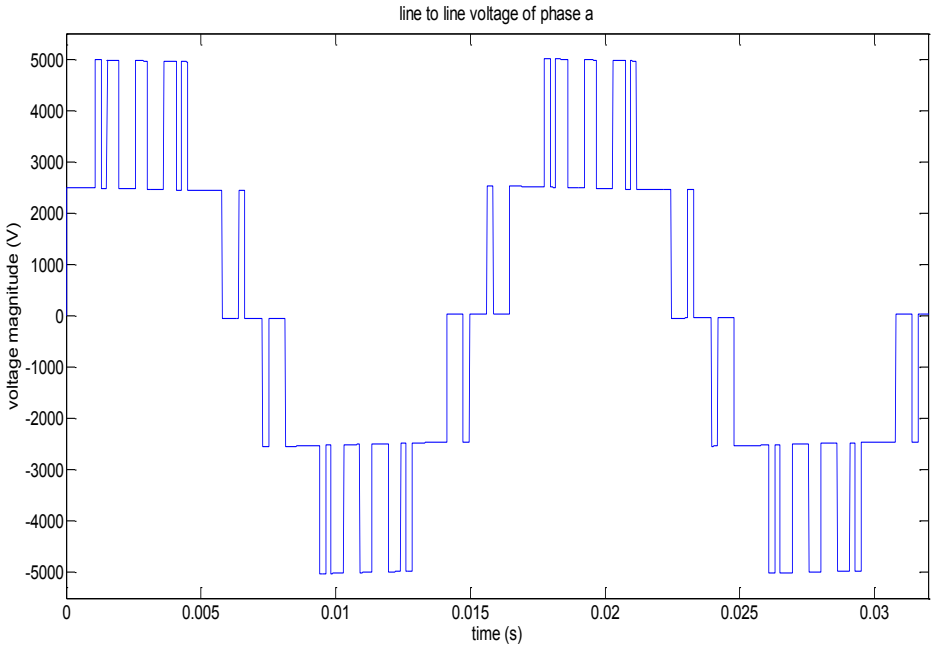


Figure 4.6. Line to line voltage of the converter (physical model).

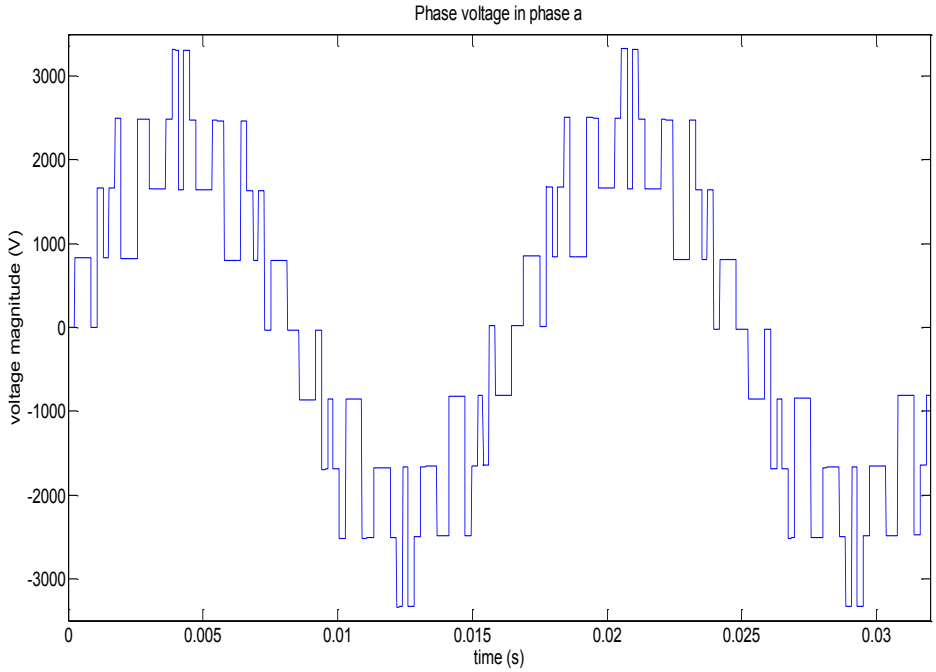


Figure 4.7. Line to neutral voltage of the converter (physical model).

With a total DC bus voltage of $V_{dc} = 5000$, the following voltage levels can be seen, generated on the waveforms.

$Phase\ to\ mid-point\ voltages$: $-2500, 0$ and 2500

$Phase\ to\ neutral\ voltages$:

$-3333.33, -2500, -1666.67, -833.33, 0, 833.33, 1666.67, 2500, 3333.33$

$Line-to-line\ voltages$: $-5000, -2500, 0, 2500, 5000$

The line to line voltage of a three level converter changes in steps of $\frac{V_{dc}}{2}$ unlike a two level converter, where the change is in steps of V_{dc}. There is also a reduction in the switching losses since the commutation voltage in a three level converter reduces to $\frac{V_{dc}}{2}$.

4.2.5 Sine-Triangle PWM in Simulink

The generation of the PWM signals is vital to maintain the states of the switches, in order to generate the required voltage output and avoid shorting of the DC bus. The simulation of the sine-triangle is explained in detail in the following section. Figure 4.8 shows the Simulink model of the sine triangle PWM. In this case, there are two triangle waveforms and three sine waves, representing the three phases. The sine waves are compared with both triangles simultaneously. The comparator compares the two waveforms as per the logic explained earlier. The resulting waveform is then passed through a saturation block, wherein all the values greater than zero are saturated at unity, indicating that the respective switch remains on at that interval and all the values less than zero are saturated at zero, indicating that all the respective switch remain off during that time interval.

From Figure 4.8 it can be seen that the switch T_{x3} receives a switching signal complementary to that received by the switch T_{x1} and switch T_{x4} receives the complementary signal received by switch T_{x2}. Owing to this, the switch pairs T_{x1}, T_{x3} and T_{x2}, T_{x4} can never be turned on at the same time.

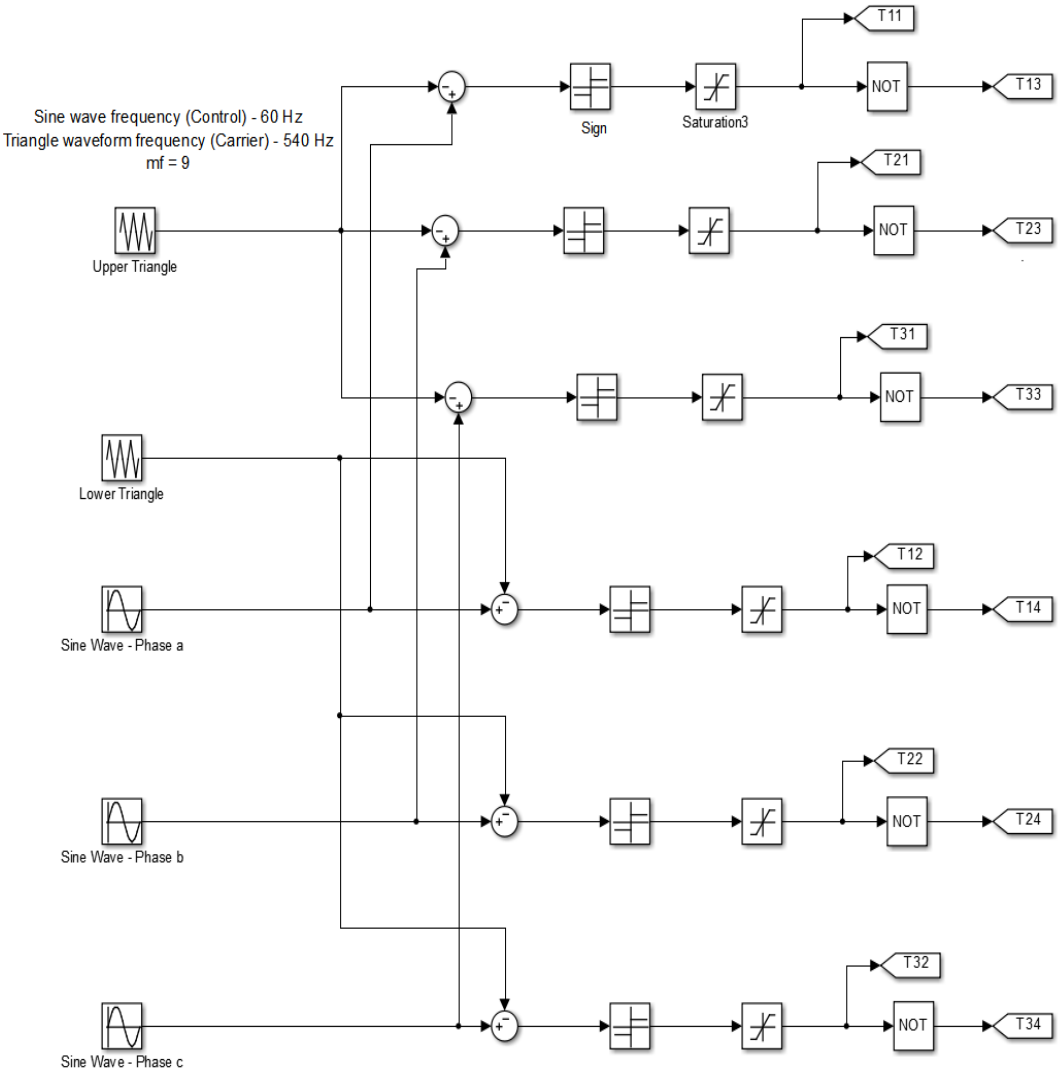


Figure 4.8. Simulink model of the sine-triangle PWM.

4.2.6 Inverter Modeling in Native Simulink

The converter model explained thus far was modeled in SimPowerSystems toolbox in the Simulink environment of MATLAB. The model must be capable of hardware-in-the-loop testing. To enable this, it was run on a Real Time Simulator (RTI), which in this case is a dSPACE 1103 controller board. It was observed that the Power System Blockset models need stiff solvers with variable step-size. However, Real-Time

Workshop supports only fixed-step integrators. To obtain stability, the Power System Blocksets require very small step size which cannot be achieved in real time. The best sampling frequency the model functioned at was 100 µs, which was not an acceptable number for a switching frequency of 540 Hz. Hence, the converter was modeled in native Simulink, without the use of multifunctional Power System Blocksets.

4.2.7 Switching Logic in Native Simulink

In case of native Simulink models, the actual switch will be replaced by a logic circuit emulating the action of the active switch, in other words, the on and off positions of the switch will be controlled using the PWM as done in case of a physical model. In order to design an inverter, the primary requirement is to arrive at a logic that will provide the same resulting phase mid-point voltage of each inverter leg as would the physical model. In case of a three level inverter, it is clear from previous sections that the phase mid-point voltages are:

i) $\frac{V_{dc}}{2}\ when\ T_{x1}\ and\ T_{x2}\ are\ on$

ii) $0\ when\ T_{x2}\ and\ T_{x3}\ are\ on$

iii) $-\frac{V_{dc}}{2}\ when\ T_{x3}\ and\ T_{x4}\ are\ on$

It is also known that the PWM signals/switching signals for the switches T_{x3} and T_{x4} are complementary to that received by switches T_{x1} and T_{x2}. This results in the following logic table to find the resulting phase mid-point voltage, with just two switching signals.

Table 4.4. Inverter switching logic.

Switching signal received by T_{x1}	**Switching signal received by T_{x2}**	**Phase mid-point voltage**
1	1	$\frac{V_{dc}}{2}$
0	1	0

0	0	$-\frac{V_{dc}}{2}$
1	0	$Case\ doesn't\ exist$

The logic further results in the following equation for the phase mid-point voltage of the inverter:

$$Phase\ mid\ point\ voltage = (State\ of\ switch\ T_{x1} + State\ of\ switch\ T_{x2} - 1) * \frac{V_{dc}}{2}$$

$$State\ of\ switches\ T_{x1}\ or\ T_{x2} = \begin{cases} 1 & if\ the\ switch\ is\ on \\ 0 & if\ the\ switch\ is\ off \end{cases}$$

This above logic was implemented in native Simulink using multi-port switches with the switching logic within. The output of the multi-port switch gave the appropriate phase mid-point voltage of each inverter phase leg. The schematic is as shown in Figure 4.9. It shows the generation of the phase midpoint voltages V_{ao}, V_{bo}, V_{co} , calculation of the neutral voltage V_n calculation of the phase to neutral voltages V_{an}, V_{bn}, V_{cn} and calculation of line to line voltages V_{ab}, V_{bc}, V_{ca}

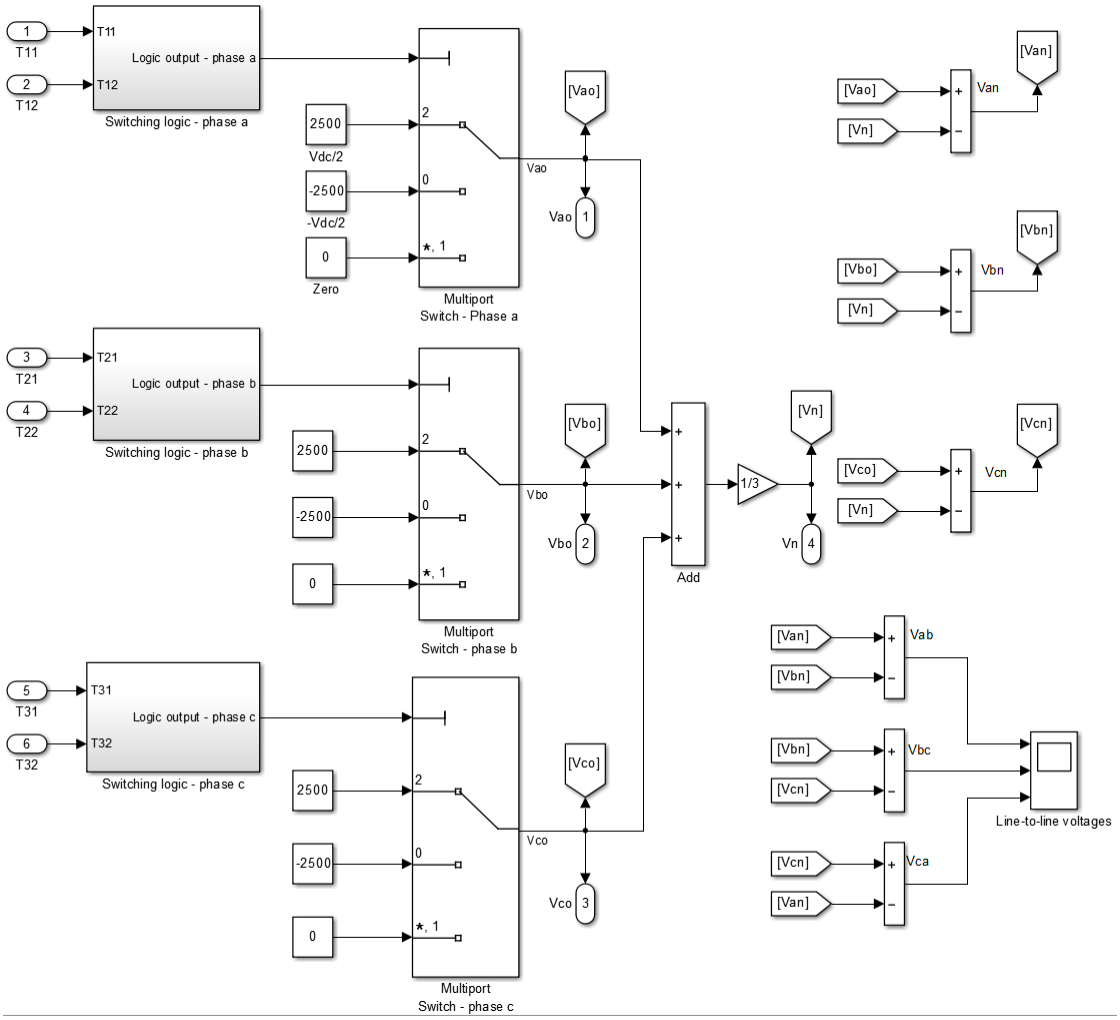


Figure 4.9. Model showing the three level inverter in native Simulink.

The voltages V_{ao}, V_{bo}, V_{co} represent the phase mid-point voltages of the three phase of the inverter. The neutral point voltage of the inverter V_n is given by the equation below:

$$V_n = \frac{1}{3} * (V_{ao} + V_{bo} + V_{co})$$

The nine level phase to neutral voltage of the three level inverter can be obtained using the following relation between the neutral voltage and the phase mid-point voltages:

$$V_{an} = V_{ao} - V_n$$

$V_{bn} = V_{bo} - V_n$

$V_{cn} = V_{co} - V_n$

The five level line-to-line voltage of the three level inverter can be obtained using the relation between the phase to neutral voltages as below:

$V_{ab} = V_{an} - V_{bn}$

$V_{bc} = V_{bn} - V_{cn}$

$V_{ca} = V_{cn} - V_{an}$

Referring back to Figure 4.1, the line current in the inverter flowing through the wye connected RL load $(0.05\ \Omega\ and\ 0.5\ mH)$ can be calculated as below. The native Simulink model representing the equations is shown in Figure 4.10.

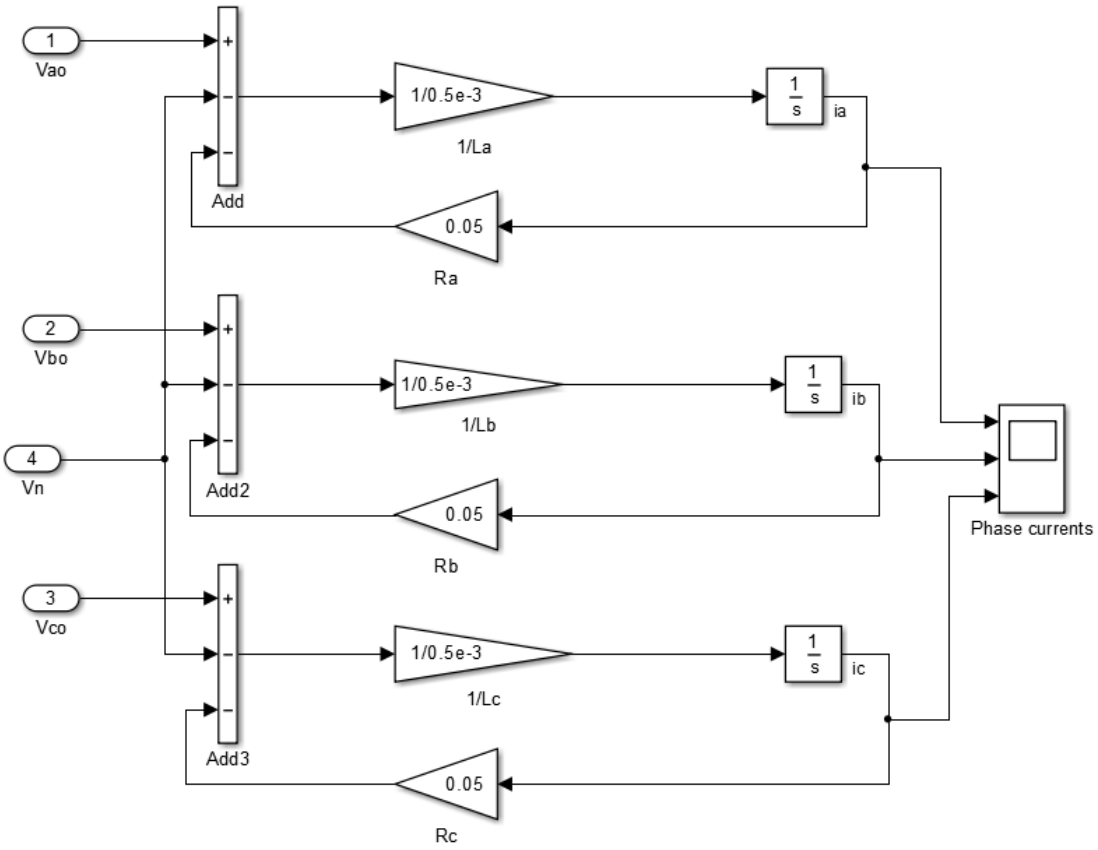


Figure 4.10. Native Simulink model of the inverter connected to a three phase RL load.

$$V_{ao} - V_n = i_a * R_a + L_a \frac{di_a}{dt}$$

$$V_{ao} - V_n - i_a * R_a = L_a \frac{di_a}{dt}$$

$$\frac{di_a}{dt} = \frac{1}{L_a} * (V_{ao} - V_n - i_a R_a)$$

Similarly, for phases b and c

$$\frac{di_b}{dt} = \frac{1}{L_b} * (V_{bo} - V_n - i_b R_b)$$

$$\frac{di_c}{dt} = \frac{1}{L_c} * (V_{co} - V_n - i_c R_c)$$

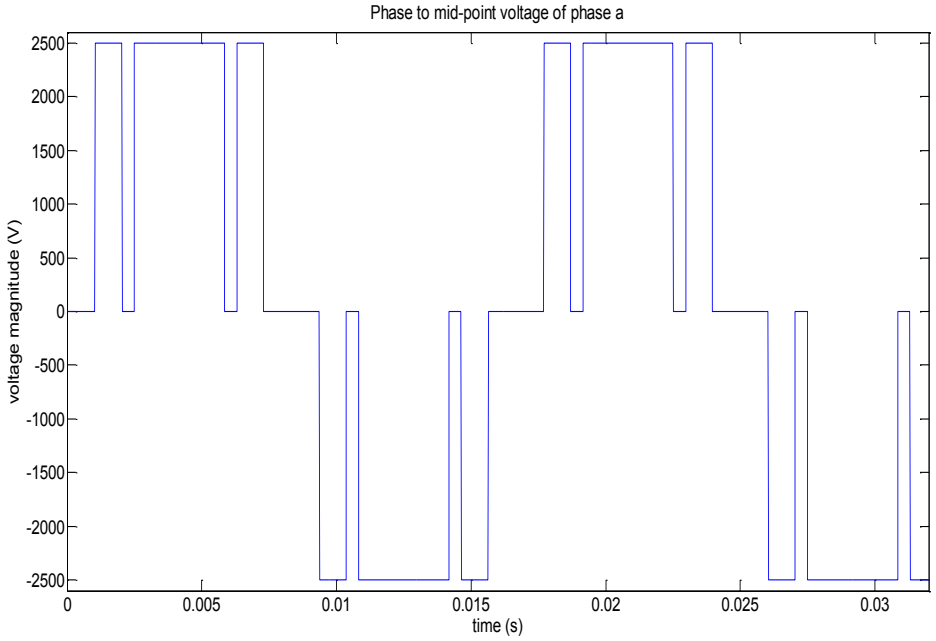


Figure 4.11. Phase midpoint voltage of the inverter (native Simulink model).

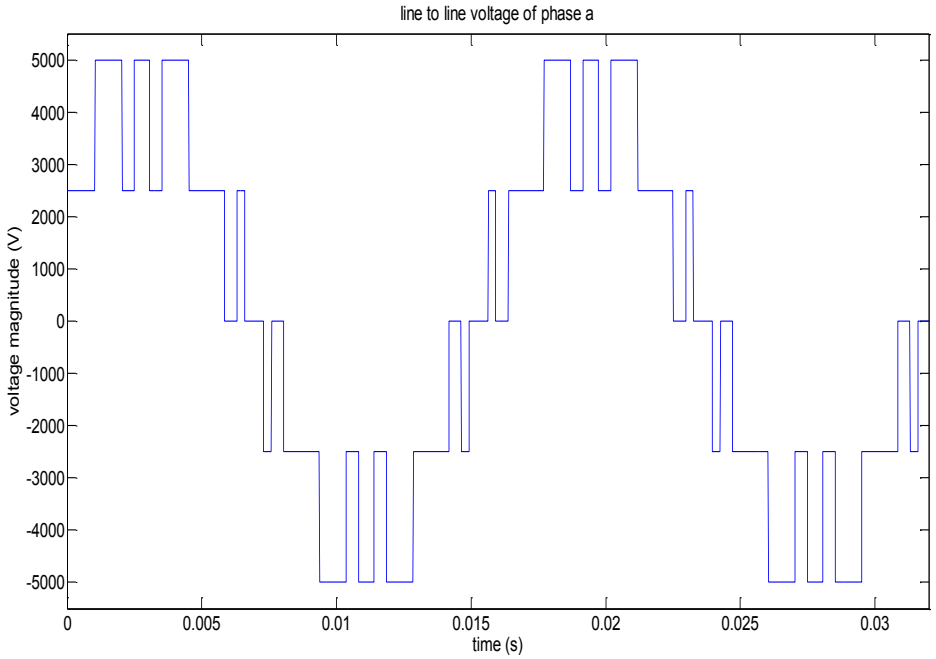


Figure 4.12. Line to line voltage of the inverter (native Simulink model).

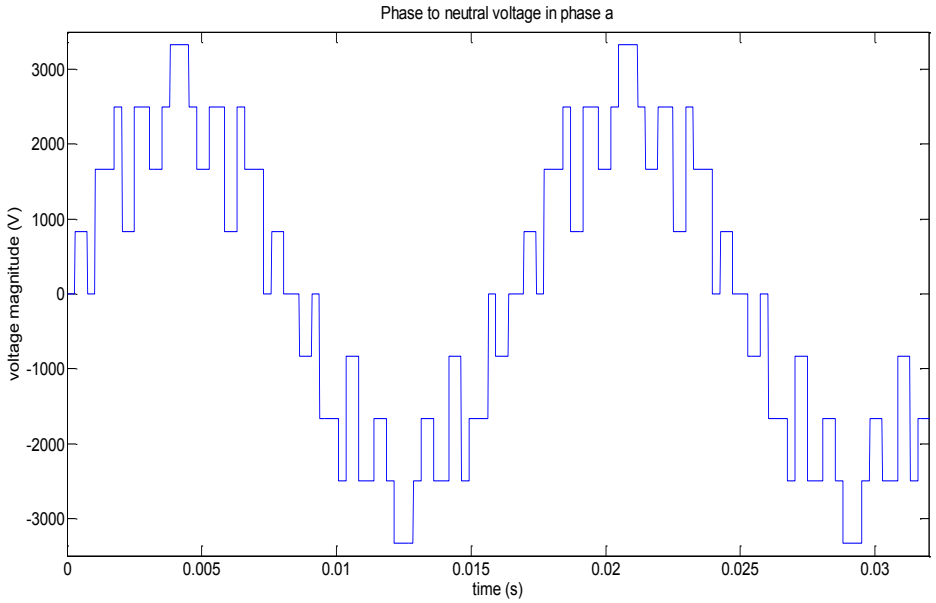


Figure 4.13. Line to neutral voltage of the inverter (native Simulink model).

The results obtained using the native Simulink model of the inverter were satisfactorily equivalent to the design of the three level inverter in native Simulink.

4.3 Inverter Open Loop Control

The inverter system topology is currently being modeled in open loop. The inverter topology consists of four, three level inverters modeled in Simulink, with each inverter receiving switching signals from a unique PWM generator. The PWM used is similar to the one described earlier in this chapter. Each inverter receives power from the capacitor bank charged using the grid-tie converter. The capacitor bank has three voltage levels $\frac{V_{dc}}{2}$, 0 and $-\frac{V_{dc}}{2}$. The inverters are grouped into two pairs. Each pair of inverters is connected to a transformer primary and are producing voltages in phase opposition, meaning the control voltage waveforms for the second inverter in each pair are 180° out of phase to that given to the first inverter.

Each inverter produces a three level phase midpoint voltage in steps of $\frac{V_{dc}}{2}$, 0 and $\frac{-V_{dc}}{2}$. The transformer primaries are connected between the phase midpoint terminals of each inverter pair. The resulting voltage owing to the phase opposition of the two three-level voltages is a five level voltage in steps of V_{dc}, $\frac{V_{dc}}{2}$, 0, $\frac{-V_{dc}}{2}$ and $-V_{dc}$.

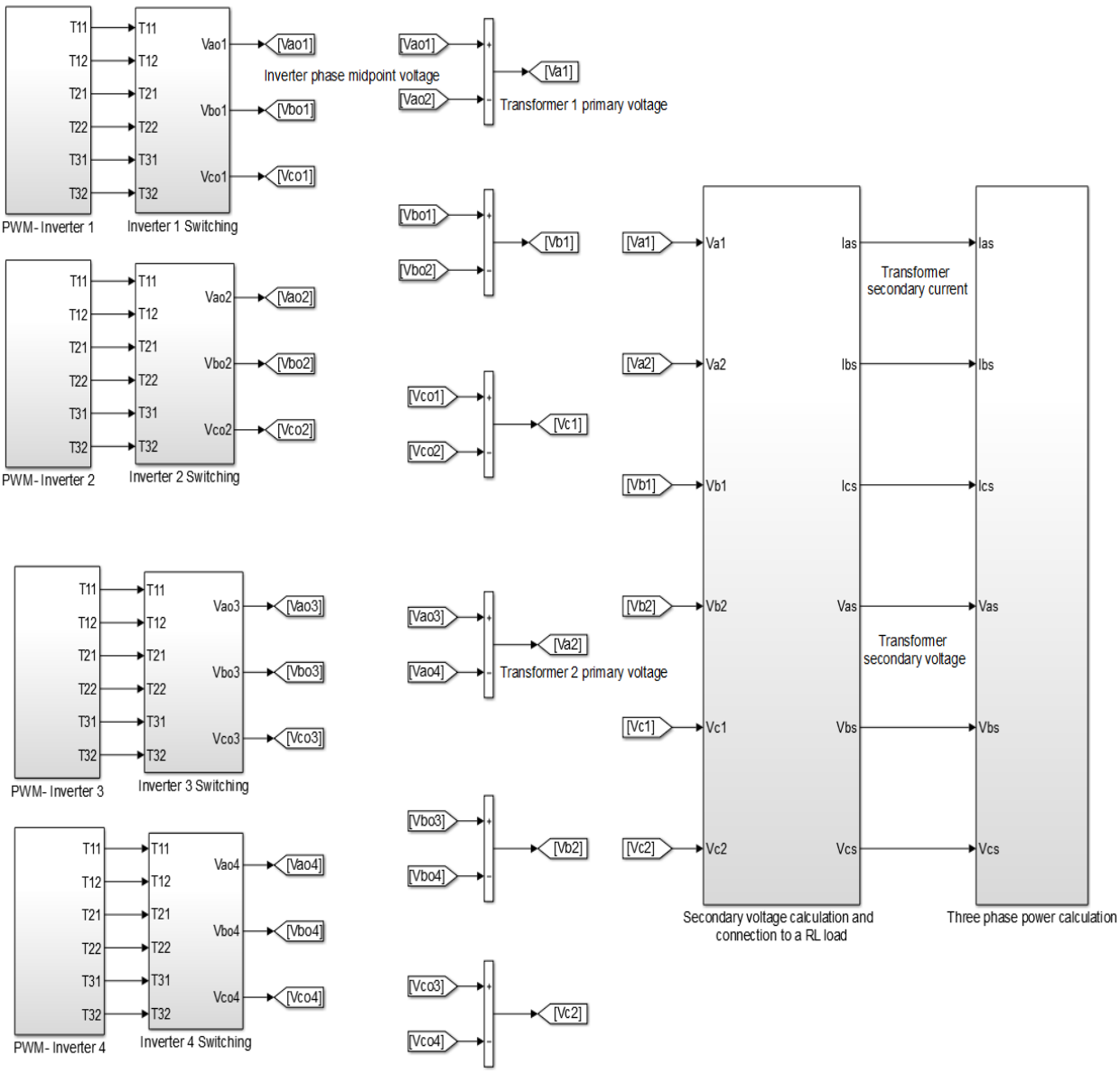


Figure 4.14. Topology of the four inverter open loop control.

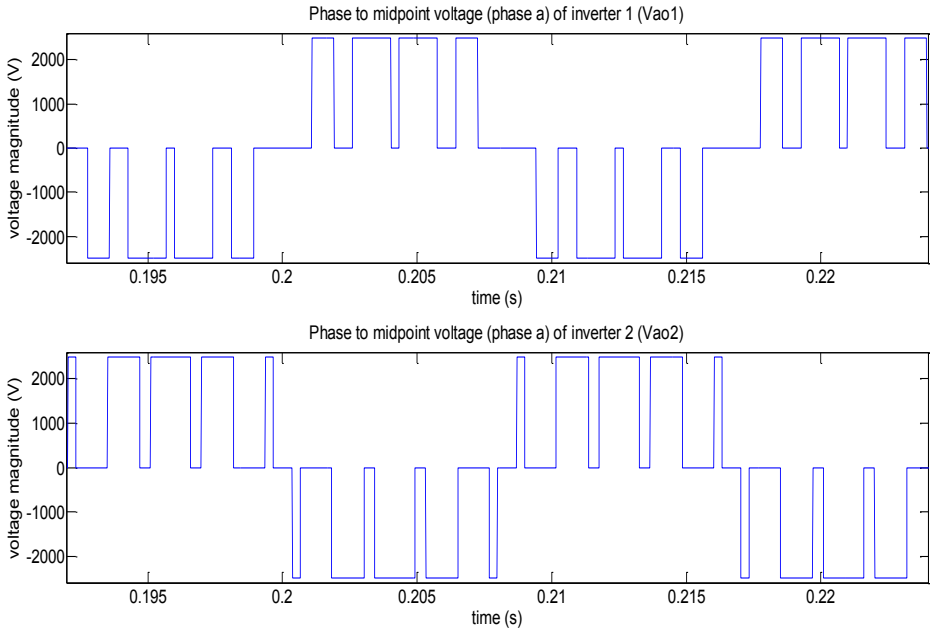


Figure 4.15. Phase midpoint voltages of the first inverter pair.

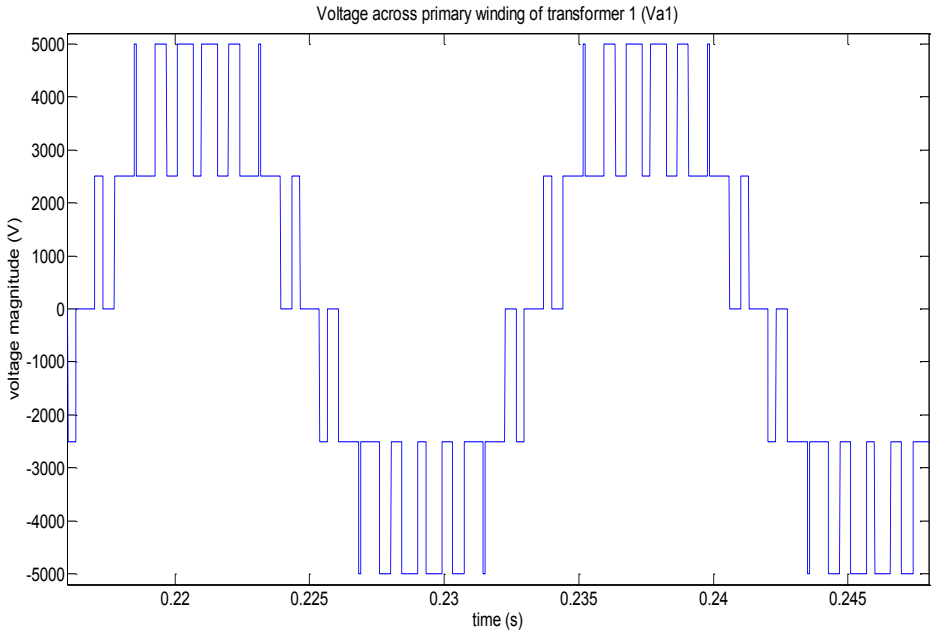


Figure 4.16. Voltage across transformer primary.

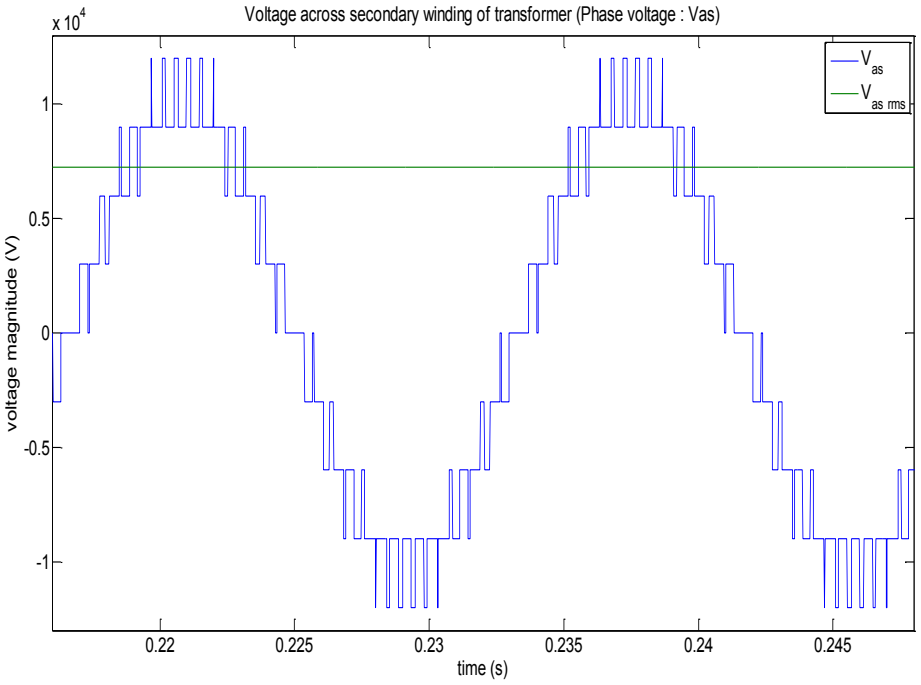


Figure 4.17. Voltage across transformer secondary.

The end result is to increase these levels even further to reduce the harmonic content. In order to achieve this, a shift has been introduced in the carrier waveforms for the second inverter pair. In the current simulation, this phase shift has been set at 90°. This method essentially generates a five level voltage at the primary of the second transformer, but with a phase shift of 90°, with respect to the voltage across the primary of the first transformer. The inverter windings on the secondary are in series and the resulting voltage is a sum of the two voltage waveforms and a product of the transformer turns ratio.

The voltage on the transformer secondary represents the distribution grid voltage. The nominal grid voltage at the site of grid emulator connection (PMEC-SETS) is 12.47 kV (L-L). The following parameters were used in the Simulink model in order to achieve this.

Modulation index, $m_i = 0.84$

Transformer turns ratio, $N = 1.2$

The transformer turns ratio was first set at 1.2 and the modulation index was tuned in order to obtain a phase voltage of $\frac{12.47*10^3}{\sqrt{3}} \cong 7200$ V. The resulting waveform is a nine level phase voltage across the terminals of the transformer secondary.

A load consisting of a resistance and an inductance (RL load) is connected across the secondary terminal of the transformer representing ~5.5 MW power drawn from the source. With this load in place, the phase current on the transformer secondary was found to be ~ 252 A (rms). The current in the primary windings of the transformer can be found by the product of transformer secondary winding current and the transformer turns ratio.

Transformer secondary currents,

$|I_{as}| = |I_{bs}| = |I_{cs}| = 252\ A$

Transformer primary currents,

$|I_{a1}| = |I_{b1}| = |I_{c1}| = 252 * 1.2 = 302.4\ A$

4.3.1 Transformer Design

For ease of simulation, the transformer is designed using two cores for each phase of the inverter voltage. The primary windings of the transformer, or the converter side, are independent and the secondary windings of the transformer, or the test article side, are connected in series. The purpose of this design is to increase the number of voltage levels on the voltage waveform, thereby bringing it closer to the quality of the mains, further reducing the harmonic content.

The use of this particular transformer design increases the momentary overcurrent capacity of the WEC-side converter, since each of the four converters share a quarter of the total load under nominal operating conditions. The increased number of voltage levels reduces the harmonics in the resulting voltage. The use of single phase transformers allows voltage control capability on each phase.

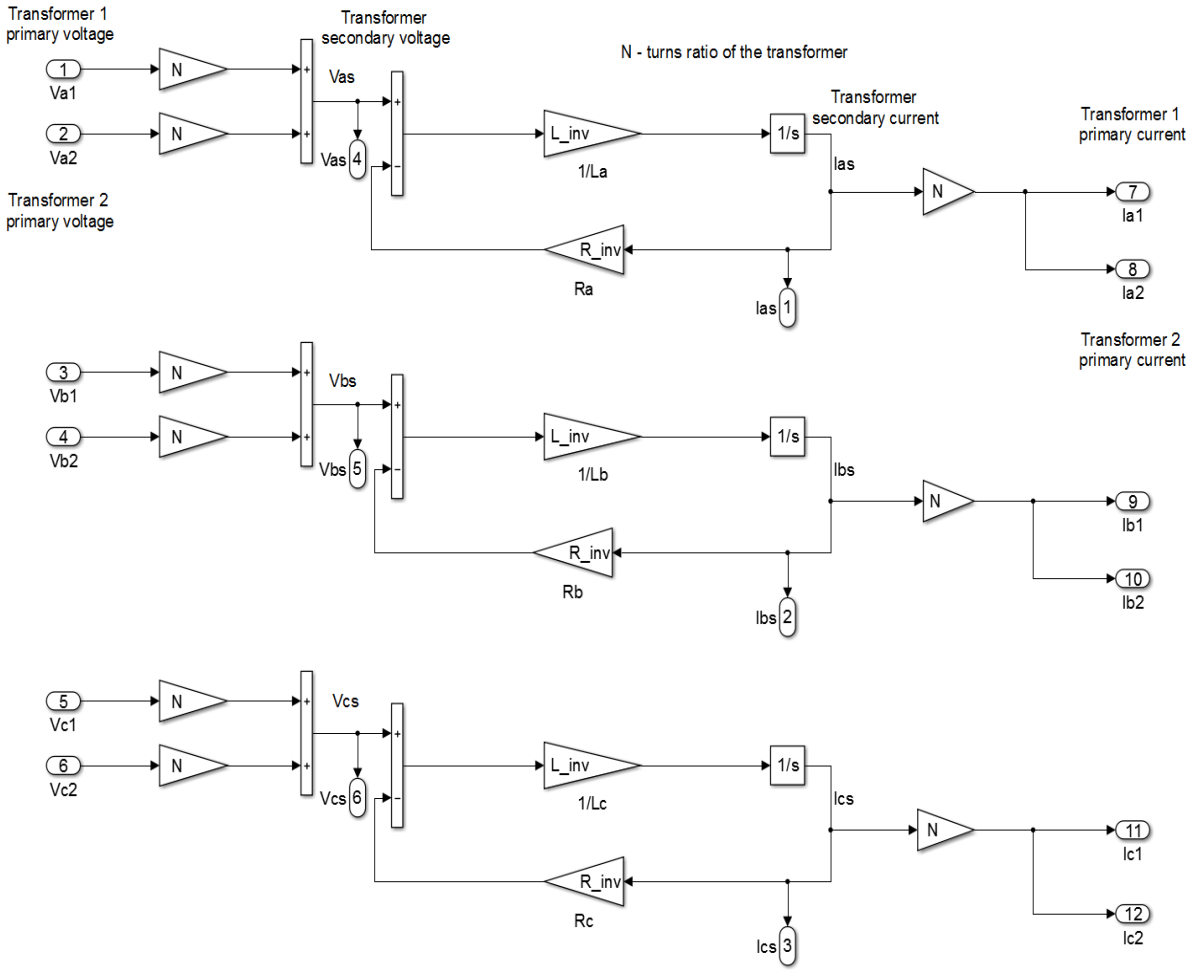


Figure 4.18. Transformer design and RL load.

4.4 Design of Three Level Rectifier

The topology of the three level rectifier is similar to that of a three level inverter. The PWM signals which determine the switching of the rectifier switches are generated in the same way as done for an inverter. The active rectifier will draw balanced three phase ac power from an interconnection transformer at 3.3 kV on the AC side and is modeled to produce a DC output voltage of 5000 V between the positive and negative

dc rails. The output between the DC rails is split into 2500 V and -2500 V using a capacitor bank, which in turn is fed to the three level inverter of the grid emulator. As stated earlier, the SimPowerSystems model of the rectifier cannot be utilized in the simulation because of compatibility issues. Hence, the rectifier is designed in native Simulink.

4.4.1 Native Simulink Modeling of the Rectifier

The design of the rectifier in native Simulink is detailed in this section. The topology of the three level rectifier is shown in Figure 4.19.

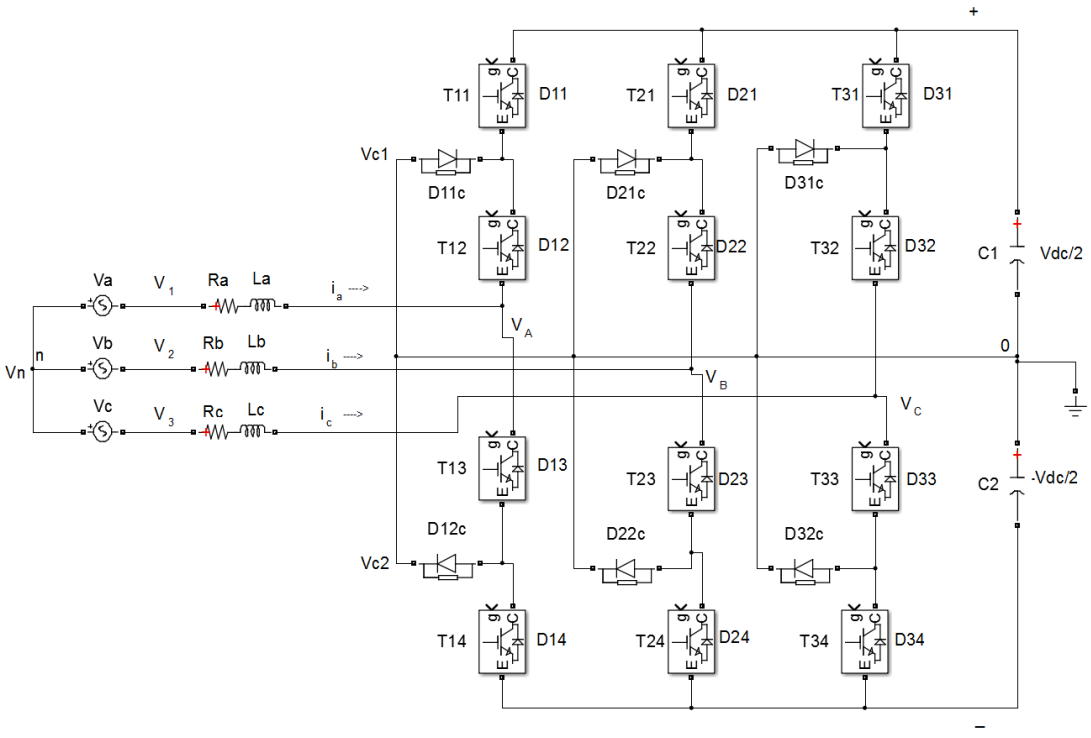


Figure 4.19. Rectifier Topology.

The rectifier has three balanced wye connected voltage sources, V_a, V_b, and V_c on the AC side. In reality, these are the voltages from the low voltage side of a three phase transformer. The voltages have a magnitude of V_m and are phase shifted in space by 120°. The neutral point voltage is termed V_n. The AC sources are connected to the

converter via line impedances constituting resistance R and inductance L. The voltages V_1, V_2 and V_3 are given by the relations:

$$V_1 = V_a + V_n = V_m * \sin(\omega t) + V_n \qquad Eqn.\,1.1$$

$$V_2 = V_b + V_n = V_m * \sin(\omega t - 120°) + V_n \qquad Eqn.\,1.2$$

$$V_3 = V_c + V_n = V_m * \sin(\omega t - 240°) + V_n \qquad Eqn.\,1.3$$

The rectifier currents are referenced as positive current flowing toward the capacitor bank. These are obtained from the relations

$$L * \frac{di_a}{dt} + R * i_a = V_1 - V_A \qquad Eqn\ 2.1$$

$$L * \frac{di_b}{dt} + R * i_b = V_2 - V_B \qquad Eqn.\,2.2$$

$$L * \frac{di_c}{dt} + R * i_c = V_3 - V_C \qquad Eqn.\,2.3$$

The voltages V_A, V_B, and V_C are obtained by referring the potentials at the phase mid-points of each inverter leg to the DC mid-point of the capacitor bank. The table below shows the phase midpoint voltages at different switch states.

Table 4.5. Switching states of rectifier switches

State of switch T_{x1}	**State of switch T_{x2}**	**Phase mid-point voltage V_X**
1	1	$\frac{V_{dc}}{2}$
0	1	0
0	0	$-\frac{V_{dc}}{2}$
1	0	$Case\ doesn't\ exist$

From table 4.5:

$$V_A = (State\ of\ switch\ T_{11} + State\ of\ switch\ T_{12} - 1) * \frac{V_{dc}}{2} \qquad Eqn.3.1$$

$$V_B = (State\ of\ switch\ T_{21} + State\ of\ switch\ T_{22} - 1) * \frac{V_{dc}}{2} \qquad Eqn.3.2$$

$$V_C = (State\ of\ switch\ T_{31} + State\ of\ switch\ T_{32} - 1) * \frac{V_{dc}}{2} \qquad Eqn.3.3$$

For a balanced three phase system, the sum of the three phase currents is zero

$$\therefore\ i_a + i_b + i_c = 0 \qquad Eqn.4$$

Add the three equations, 2.1, 2.2 and 2.3 and using the relation given by equation 4,

$$L * \frac{d(i_a + i_b + i_c)}{dt} + R * (i_a + i_b + i_c) = (V_1 + V_2 + V_3) - (V_A + V_B + V_C)$$

$$\Longrightarrow V_1 + V_2 + V_3 = V_A + V_B + V_C \qquad Eqn.5$$

Adding equations 1.1, 1.2, and 1.3 yields

$$V_1 + V_2 + V_3 = 3 * V_n$$

Using this relation in Eqn.5 yields the relation between the neutral voltage and the phase mid-point voltages as

$$V_n = \frac{1}{3} * (V_A + V_B + V_C)$$

The neutral voltage generation has been modeled using Native Simulink. The Figure 4.20 shows the neutral voltage calculation.

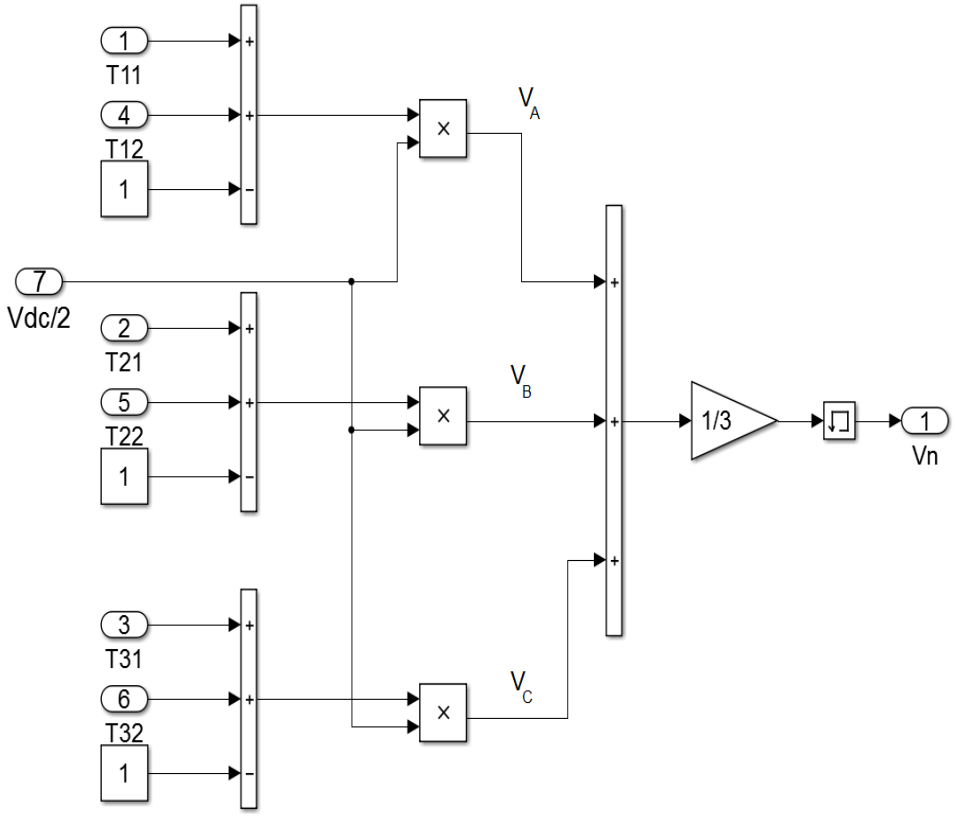


Figure 4.20. Rectifier neutral voltage calculation.

4.4.2 Reference Frame Transformation

The rectifier is modeled with an outer voltage control loop and an inner current control loop. For ease of modeling, reference frame transformation has been employed. The a-b-c reference frame has been transformed to the d-q reference frame. Since this modeling is done for a balanced system, the zero sequence is not considered here.

In Figure 4.19, the currents are referenced as positive line currents flowing from the AC source toward the capacitor bank. Using this, the V_1, V_2, and V_3 are given by the

equations 1.1, 1.2, and 1.3. Converting this three phase balanced system to a space vector would result in a vector of set magnitude rotating in space at a certain defined speed. Figure 4.21 shows the calculations for voltages V_1, V_2, and V_3

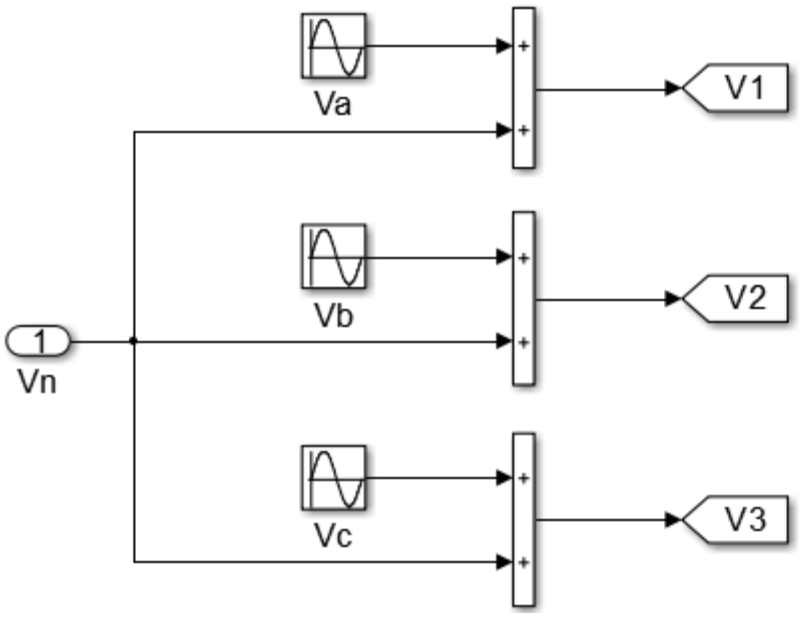


Figure 4.21. Generation of voltages V_1, V_2, and V_3.

Multiplying eqn. 1.1 by e^{j0} , eqn. 1.2 by $e^{j2\pi/3}$ and eqn. 1.3 by $e^{j4\pi/3}$ gives

$$(V_1 = L * \frac{di_a}{dt} + R * i_a + V_A) * e^{j0} \qquad Eqn\ 6.1$$

$$(V_2 = L * \frac{di_b}{dt} + R * i_b + V_B) * e^{j2\pi/3} \qquad Eqn\ 6.2$$

$$(V_3 = L * \frac{di_c}{dt} + R * i_c + V_C) * e^{j4\pi/3} \qquad Eqn\ 6.3$$

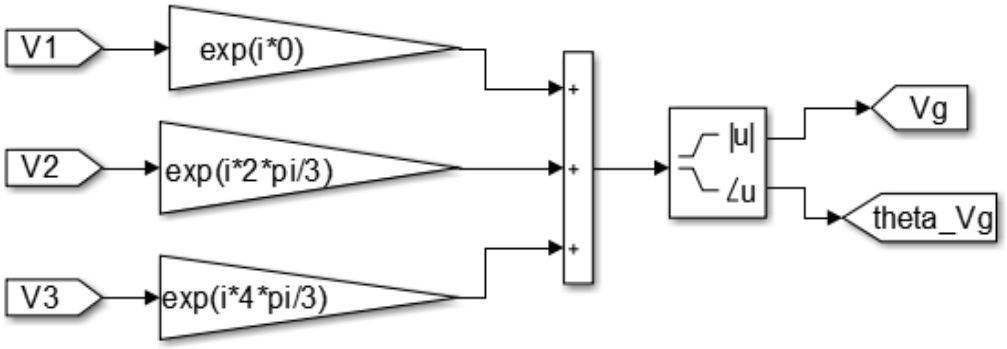


Figure 4.22. Generation of voltage space vector (V_g) and θ_d.

Where,

$$e^{j0} = \cos(0) + j * \sin(0)$$

$$e^{j2\pi/3} = \cos\left(\frac{2\pi}{3}\right) + j * \sin\left(\frac{2\pi}{3}\right)$$

$$e^{j4\pi/3} = \cos\left(\frac{4\pi}{3}\right) + j * \sin\left(\frac{4\pi}{3}\right)$$

Taking the sum of eqns. 6.1, 6.2 and 6.3 results in the space vector, $\vec{V}_g$ given by

$$\vec{V}_g = L\frac{d}{dt}\left(i_a * e^{j0} + i_b * e^{\frac{j2\pi}{3}} + i_c * e^{\frac{j4\pi}{3}}\right) + R\left(i_a * e^{j0} + i_b * e^{\frac{j2\pi}{3}} + i_c * e^{\frac{j4\pi}{3}}\right)$$
$$+ (V_A * e^{j0} + V_B * e^{j2\pi/3} + V_C * e^{j4\pi/3})$$

The current and voltage summations can be represented by their equivalent space vectors $\vec{\imath}$ and $\vec{V}$.

$$\therefore \vec{V}_g = L\frac{d}{dt}(\vec{\imath}) + R * \vec{\imath} + (\vec{V}) \qquad Eqn.7$$

The above vector relation can be resolved into a real (α) and imaginary (β) axis. Consider a *d-q* reference frame as shown in Figure 4.23, where the *q* axis is orthogonal to the *d* axis. The angle between the d axis and the real axis is θ_d. The space vector in *Eqn. 7* referenced to the *d-q* axis is given by the relation:

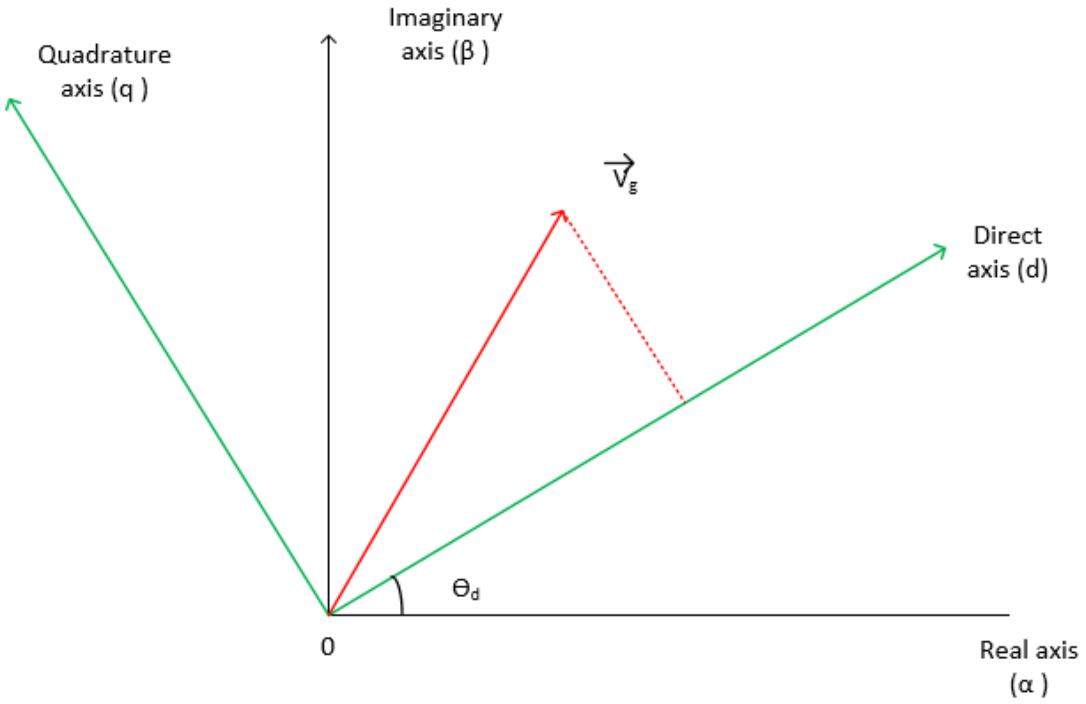


Figure 4.23. a-b-c to d-q reference frame transformation.

$$\vec{V}_g^d * e^{j\theta_d} = L\frac{d}{dt}\vec{\imath}^d * e^{j\theta_d} + R * \vec{\imath}^d * e^{j\theta_d} + \vec{V}^d * e^{j\theta_d}$$

$$\vec{V}_g^d * e^{j\theta_d} = L(e^{j\theta_d}\frac{d}{dt}\vec{\imath}^d + \vec{\imath}^d * \frac{d}{dt}e^{j\theta_d}) + R * \vec{\imath}^d * e^{j\theta_d} + \vec{V}^d * e^{j\theta_d}$$

$$\vec{V}_g^d * e^{j\theta_d} = L * e^{j\theta_d}\frac{d}{dt}\vec{\imath}^d + L * \vec{\imath}^d * e^{j\theta_d} * j * \frac{d}{dt}\theta_d) + R * \vec{\imath}^d * e^{j\theta_d} + \vec{V}^d * e^{j\theta_d}$$

Dividing the above equation by $e^{j\theta_d}$

$$\therefore \vec{V}_g^d = L\frac{d}{dt}\vec{\imath}^d + L * \vec{\imath}^d * j * \frac{d}{dt}\theta_d + R * \vec{\imath}^d + \vec{V}^d$$

In the above equation, $\frac{d}{dt}\theta_d = \omega_d$

Where, ω_d= speed of rotation of the space vector.

Splitting the space vector into its *d* and *q* components, i.e., into its rectangular components, yields

$$V_{gd} + jV_{gq} = L\frac{d}{dt}(i_d + ji_q) + Lj\omega_d(i_d + ji_q) + R(i_d + ji_q) + V_d + jV_q$$

Grouping the real and imaginary terms of the above equation results in the following two relations

$$V_{gd} = L\frac{d}{dt}i_d - L\omega_d i_q + V_d + Ri_d$$

$$V_{gq} = L\frac{d}{dt}i_q + L\omega_d i_d + V_q + Ri_q$$

In order to obtain the voltages V_{gd} and $V_{gq}$from voltage V_1, V_2, and V_3, the following reference frame transformation relations have been used.

$$V_{gd} = \frac{2}{3} * \left(cos\theta_d * V_1 + \cos\left(\theta_d - \frac{2\pi}{3}\right) * V_2 + \cos\left(\theta_d + \frac{2\pi}{3}\right) * V_3\right)$$

$$V_{gq} = \frac{2}{3} * \left(sin\theta_d * V_1 + \sin\left(\theta_d - \frac{2\pi}{3}\right) * V_2 + \sin\left(\theta_d + \frac{2\pi}{3}\right) * V_3\right)$$

The Figure 4.24 shows the reference frame transformation from a-b-c to the d-q reference frames using the above relations. The angle $\theta_d$used here is the instantaneous angle of the rotating space vector.

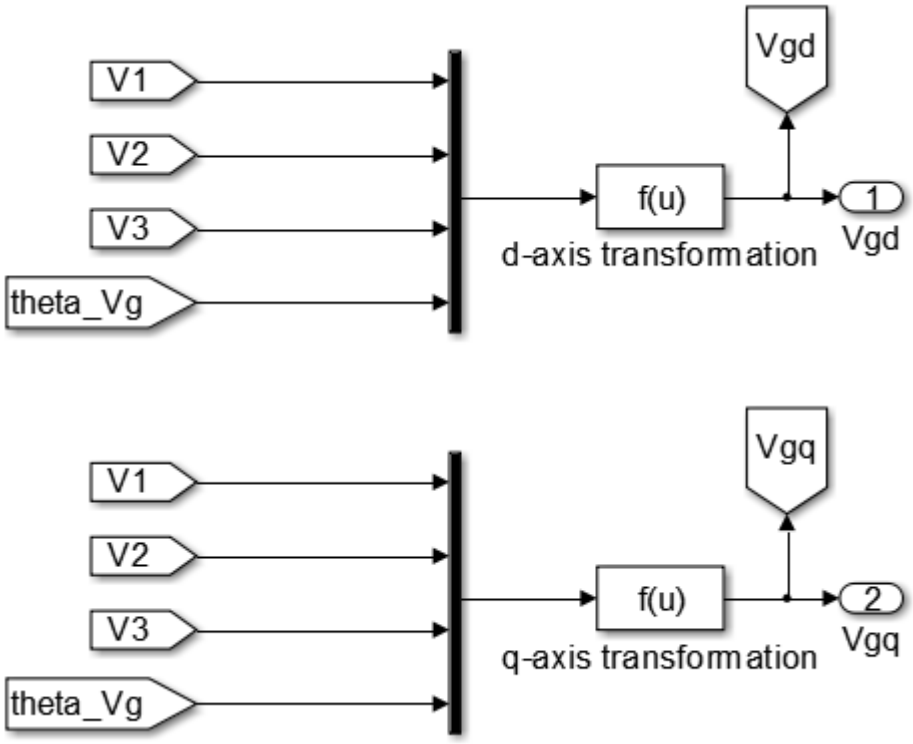


Figure 4.24. a-b-c to d-q reference frame transformation in Simulink.

Figure 4.25 shows the voltage control loop of the rectifier. The voltage loop is commanded with half the DC bus voltage of 2500 V (assuming the voltage across both the capacitors are balanced). A current of 1100 A is assumed to be drawn from the rectifier which will be explained in a later section. Figure 4.26 shows the current controlled current loops of the rectifier. The design of the PI controller is explained in a further section.

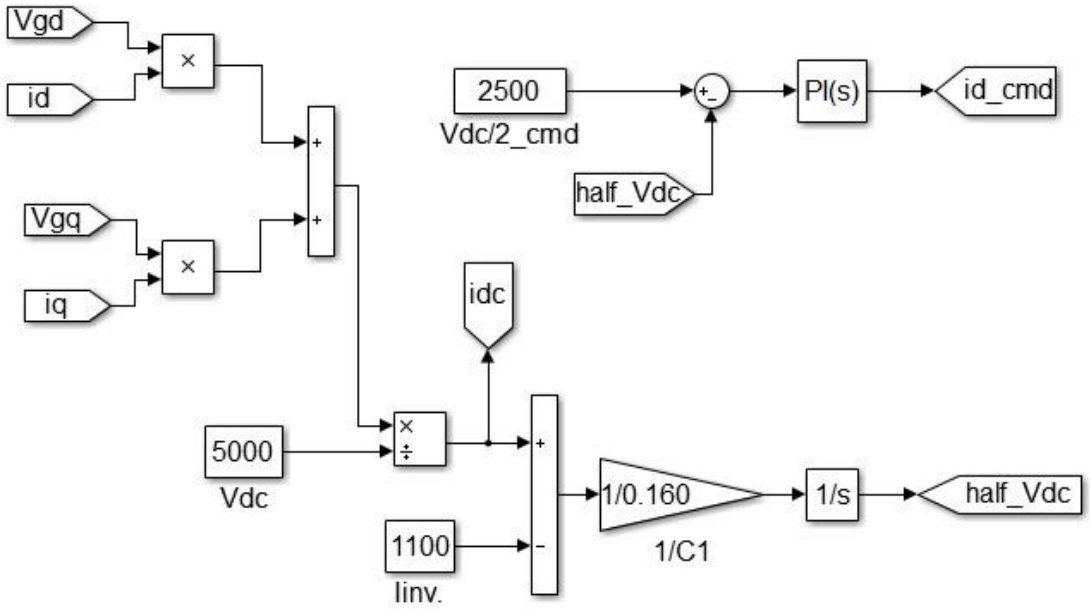


Figure. 4.25. Design of the outer voltage loop.

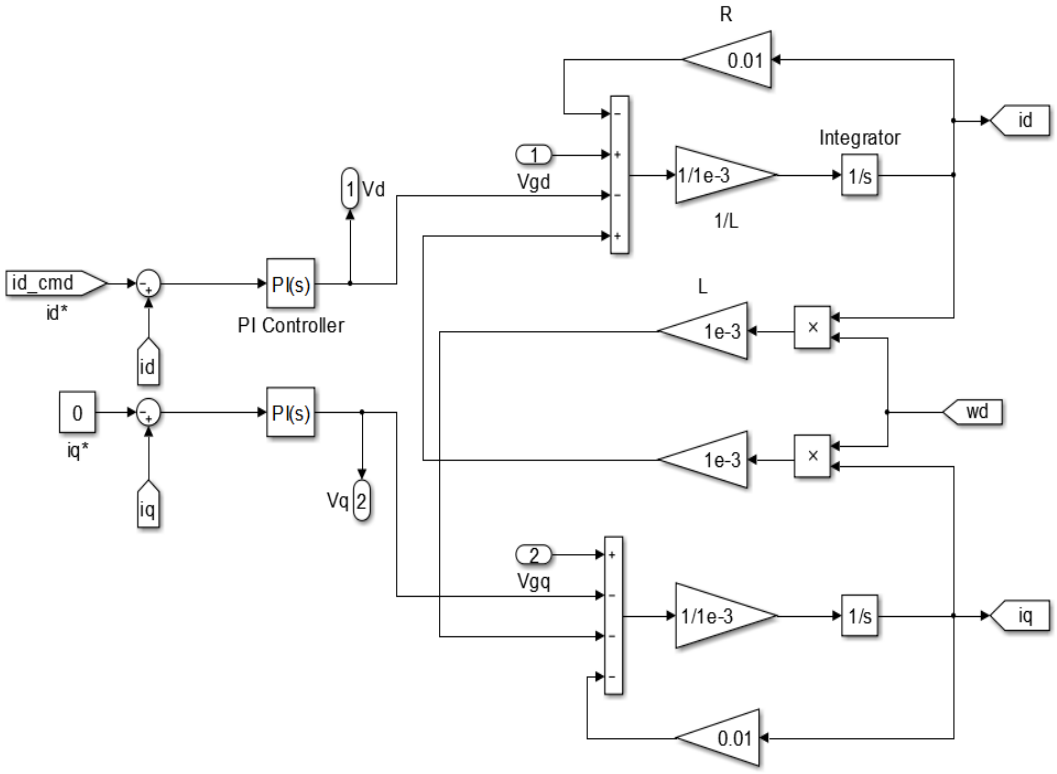


Figure 4.26. Design of the inner current control loop.

V_d and V_q are outputs of the d axis and q axis current controllers respectively. These voltages are transformed back to the a-b-c reference frame and input as the modulation signals to the PWM. In order to convert them back to sinusoidal quantities, the angle of the space vector (θ_d) rotating at 60 Hz is created and the following transformations are applied.

$$m_a = \left(\cos(\theta_d) * V_d - \sin(\theta_d) * V_q\right) / \frac{1}{3300 * \sqrt{\frac{2}{3}}}$$

$$m_b = \left(\cos\left(\theta_d - \frac{2\pi}{3}\right) * V_d - \sin\left(\theta_d - \frac{2\pi}{3}\right) * V_q\right) / \frac{1}{3300 * \sqrt{\frac{2}{3}}}$$

$$m_c = \left(\cos\left(\theta_d + \frac{2\pi}{3}\right) * V_d - \sin\left(\theta_d + \frac{2\pi}{3}\right) * V_q\right) / \frac{1}{3300 * \sqrt{\frac{2}{3}}}$$

The resulting waveforms are brought down to a scale of -1 to +1 by passing these signals through a gain block, where the signals are multiplied by the reciprocal of the amplitude of the input phase voltage.

4.4.3 Rectifier Controller Gain Calculations

4.4.3.1 Design of Controller Gains for the Current Loop

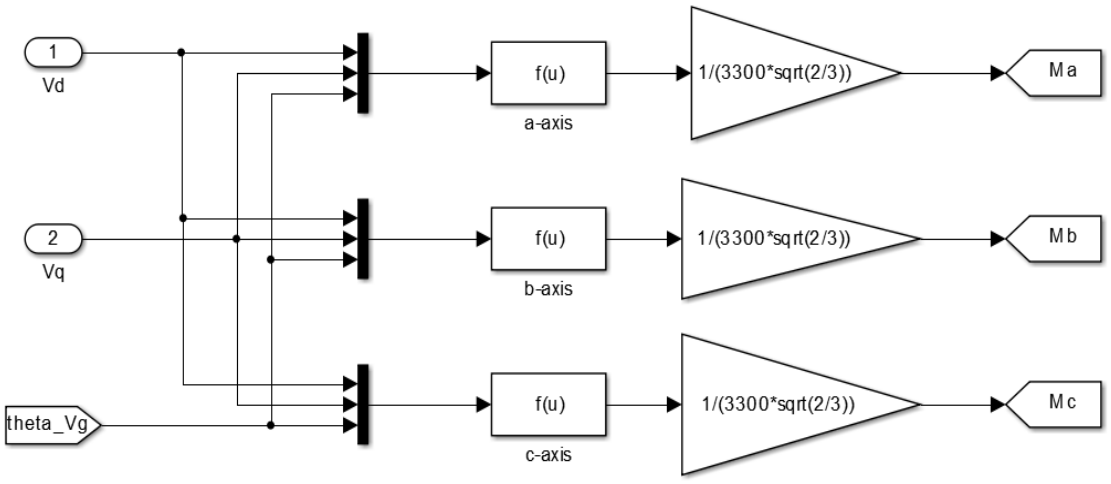


Figure 4.27. d-q to a-b-c reference frame transformation.

The reference frame transformation of the rectifier currents have been shown in the previous section, and as shown, it is definitely simpler to handle the two axis equivalent of the three phase currents in the d-q reference frame than in the a-b-c reference frame.

From the system model derived in the previous section, there are two current control loops; one for the *d*-axis current and another for the *q*-axis current. In case of an RL load, the d-axis inductance is equal to the q-axis inductance and hence, the controller gain values derived for one controller will hold good for the other controller. Consider the system model shown in Figure 4.28. The system has a commanded *d*-axis current, i_d^*, which is compared with the feedback i_d, the difference is passed through the PI controller. The controller output is the voltage, V_d. For ease of simplification, a part of the system consisting of V_g^d and $L\omega_d i_q$ are considered as offsets in the system. Although cross coupled, a satisfactory controller design could be achieved by assuming them at unity. The transfer function of the plant is given by

$$G(s) = \frac{i_d(s)}{V_d(s)} = \frac{1}{sL + R}$$

The transfer function of the PI controller can be represented as

$$C(s) = \frac{V_d(s)}{e(s)} = \frac{K_I}{s} + K_P = \frac{1}{s} + 1 \ (Assuming\ intial\ values\ of\ K_P = K_I = 1)$$

Assuming the feedback gain to be unity, the closed loop transfer function of the system is given by

$$H(s) = \frac{i_d(s)}{i_d^*(s)} = \frac{C(s)G(s)}{1 + C(s)G(s)}$$

Under conditions where the controller gain $C(s)G(s) \gg 1$, the numerator of the closed loop transfer function is approximately equal to the denominator and the output closely tracks the commanded input.

The two main performance criteria in determining the controller gains are the phase margin and the crossover frequency. Phase margin determines the stability and speed

of the system, and is the difference between the phase of the system measured in degrees and 180°. A system with a very low phase margin risks instability, but it also can be a system that is very fast. A good approximation is to obtain the system parameters at a phase margin of 60°. Another design constraint is to determine where the cross over frequency occurs. A higher crossover frequency gives the flexibility of system operation over a wide range of frequencies. In this case, the system could perform well even at very low frequencies, since the quantities that are being tracked are the *d* and *q* axis currents which are dc values. A general approximation is to control the system at $\frac{1}{10}^{th}$ the switching frequency. In this case, the switching frequency is 540 Hz, therefore, a crossover frequency of $\cong 2 * \pi * 54 \cong 340\ rad/s$. Assuming an initial value of $\frac{K_P}{K_I} = 1$ and $K_P = 1$, the system bode plot was plotted using the SISO design tool in Simulink. The system pole and zero were adjusted to set the system to a phase margin of 60° and crossover frequency at 341 rad/s. With this, the following values for the controller gains were obtained.

$$K_I = 87.492\ and\ \frac{K_P}{K_I} = 0.0028 \implies K_P = 0.0028 * 87.492 = 0.245$$

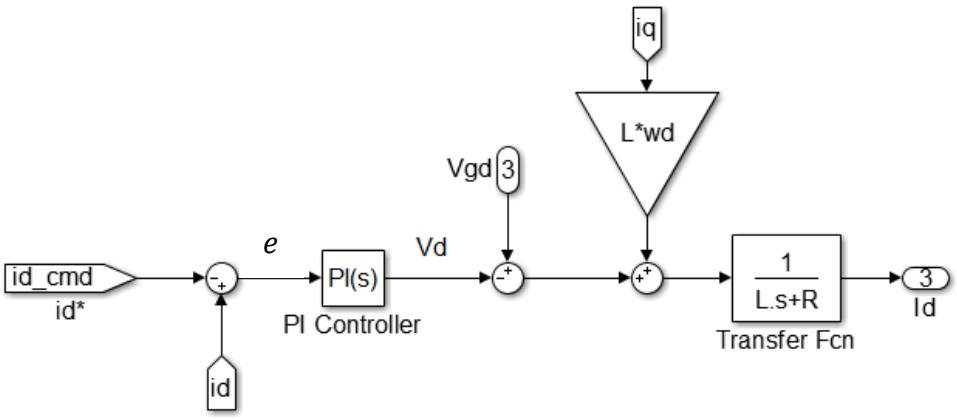


Figure 4.28. Simplified schematic of the current control loop.

4.4.3.2 Design of the Controller Gains for the Voltage Loop

The outer voltage loop, along with the inner current loop form the structure of a cascaded control loop. The inner loop is designed to be 10 times faster than the outer loop, in other words, the inner loop can be maintained at unity for calculation of control gains of the voltage loop. Therefore, the voltage control loop is designed for a crossover frequency of around 34 rad/s. One half the DC bus voltage is the commanded voltage for voltage control loop. The system design consisting the plant model and the controller model for this loop are as shown in Figure 4.29.

$$G(s) = \frac{V_{dc}(s)}{i_d(s)} = \frac{V_{gd}}{V_{dc}} \cdot \frac{1}{sC_1}$$

The controller model is assumed to be

$$C(s) = \frac{1}{s} + 1$$

The SISO design tool was used to design the controller. With a phase margin of 68.8° and a crossover frequency of 33 rad/s, the following values were obtained for the controller gains.

$$K_I = 117 \; and \; \frac{K_P}{K_I} = 0.078 \implies K_P = 0.078 * 117 = 9.126$$

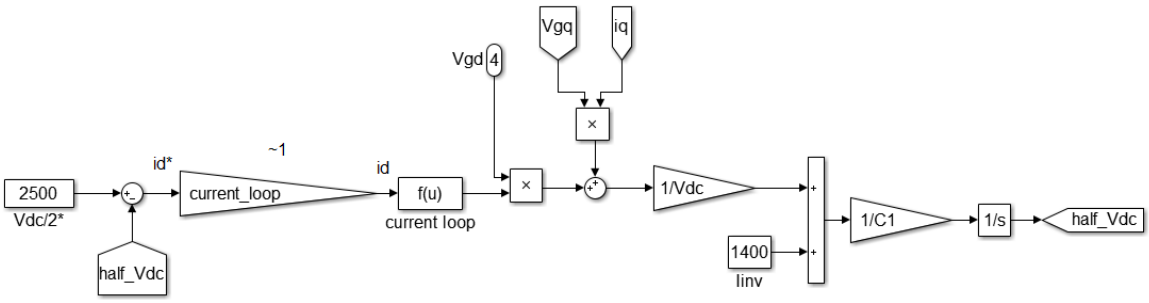


Figure 4.29. Simplified schematic of the voltage control loop.

4.4.4 Rectifier Waveforms Along With a Load

The inverter sources and sinks current with the rectifier, the current drawn by the inverter assuming zero loss can be calculated by equating the power balance between the DC and AC sides.

$$I_{inv} = \frac{V_{as} * I_{as} + V_{bs} * I_{bs} + V_{cs} * I_{cs}}{V_{dc}}$$

Where,

I_{inv} *is the current drawn from the rectifier*

The settling of the DC bus, to the commanded voltage, with an RL load on the system is shown in Figure 4.30.

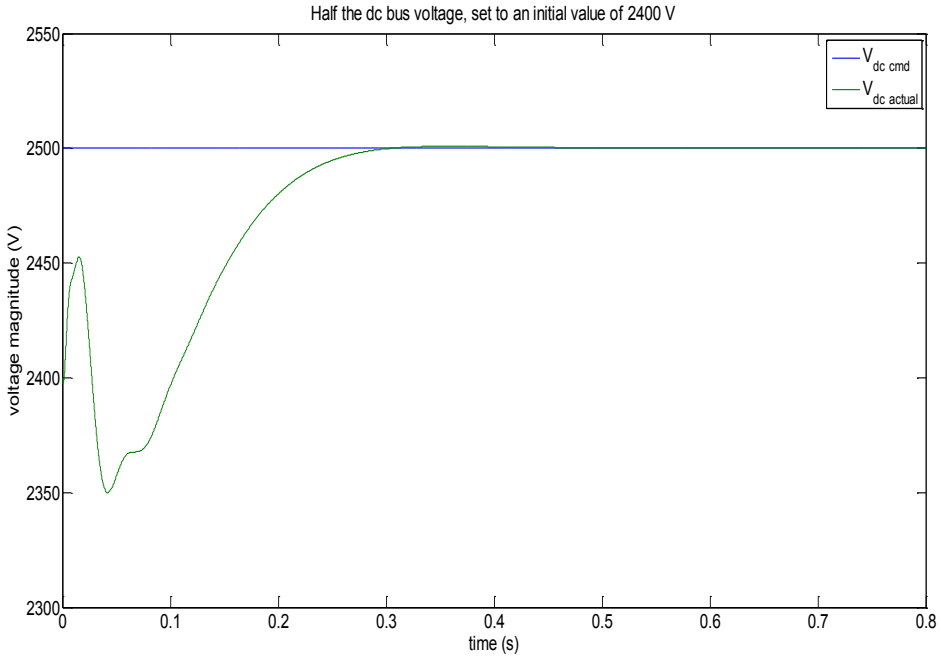


Figure 4.30. Settling of half the DC bus voltage set to an initial value of 2400 V.

5. SETUP FOR IN-LAB HARDWARE-IN-THE-LOOP SIMULATION OF THE GRID EMULATOR

Prior to development of the grid emulator into a full scale device, it will undergo an extensive hardware-in-the-loop testing at the WESRF at OSU. A block diagram of the setup is shown in Figure 5.0.

In Figure 5.0, the hardware units are the ABB AC 800 PEC Control System and the dSPACE 1103 input/output controller board. The remainder of the system will be modeled in MATLAB Simulink and transferred on to the dSPACE controller's Real Time Interface (RTI) for hardware validation. The grid emulator- sources and sinks power from the local utility grid, which is at 12.47 kV, where the interconnection transformer steps down this voltage to a level desired by the three level rectifier. The rectifier converts this to a DC voltage and maintains the voltage on the DC bus capacitors within range to enable the operation of the three level inverters. The rectifier is running in a closed loop control determined by the level of the DC bus voltage. The gating signals required for the inverter switching is generated by ABB's AC 800 PEC, which are passed on to dSPACE controller through an optical link and to the inverter switches on the RTI. The AC 800 receives voltage and current feedbacks from the simulated inverters indicating the present condition of the emulated grid. The feedback signals are fed to the PEC as analog signals after processing in the dSPACE controller.

The transformer configuration enables asymmetrical fault testing using the grid emulator. The line impedances will be modeled from the chosen submarine cable specification. The WEC in simulation will be modeled as a current source with a certain power profile. This power profile could be varied to represent different WECs.

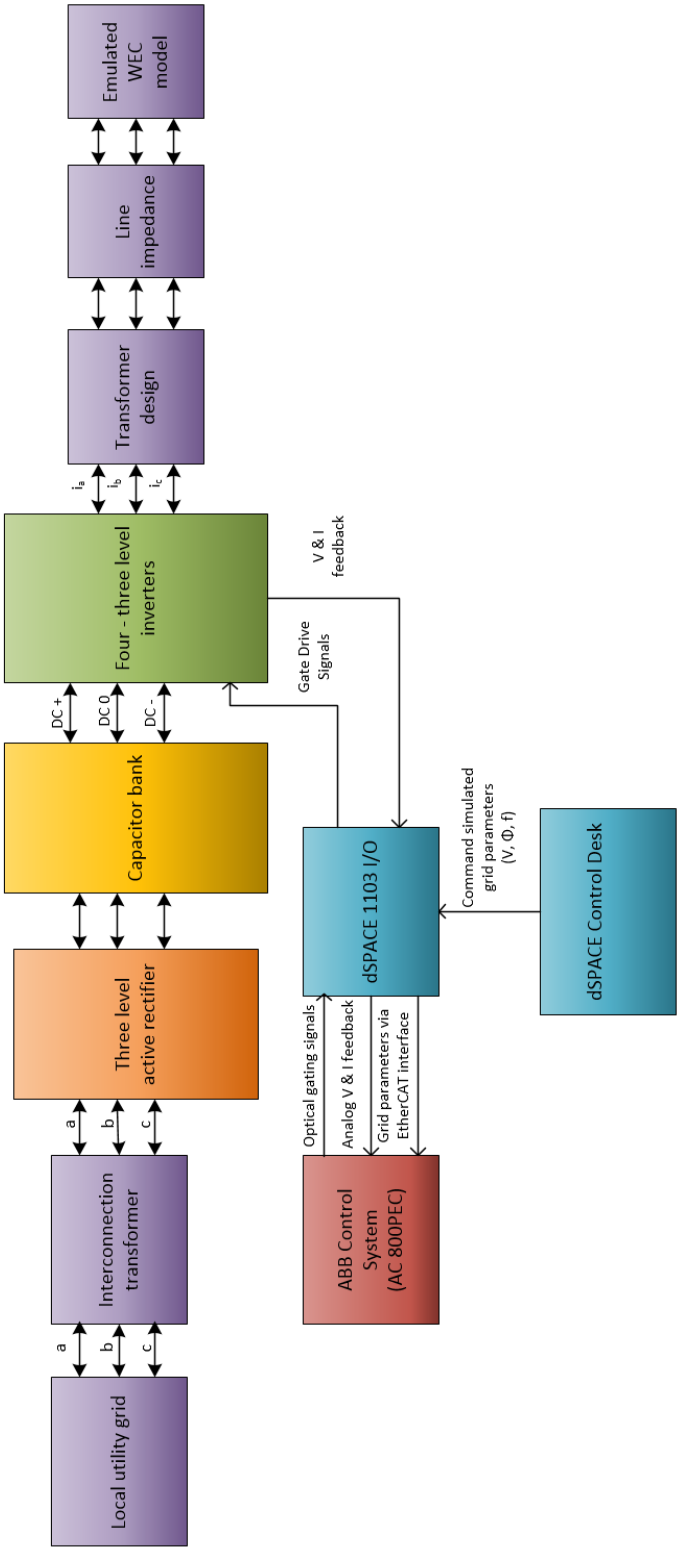


Figure 5.0. Hardware-In-the-Loop set up of the grid emulator at WESRF.

The HIL testing more accurately simulates the hardware solution using the AC 800 controller. This allows for more accurate simulation of the effects of the grid emulator on the local utility during normal operation and grid disturbance testing. An EtherCAT interface is used to transmit the parameters of the desired disturbances through the dSPACE controller to the PEC. The dSPACE control desk is used to command the output quantities at the grid emulator terminals. The following inputs are given to the PEC using the control desk:

i) Voltage amplitude: To set magnitude of the under, over voltages etc.
ii) Phase: To select the phase on which the disturbance is occurring.
iii) Frequency: To determine the frequency of the output waveforms.

The primary applications of the grid emulator as applied to WECs have been detailed in chapter 3. The HIL setup utilizing the AC 800 PEC will eliminate the need to modify the design for different tests, thereby, speeding up the performance of these tests on the grid emulator.

6. CONCLUSION AND FUTURE WORK

6.1 Conclusion

This thesis began with an introduction to wave energy and wave energy devices. The lack of standardized design in the development of WEC and the variety of WEC's around the world has been detailed. The problems arising due to a lack of uniformity in the WEC design and also the need for the process of certification and faster development have been elucidated. The existing and proposed grid emulator topologies were discussed. The problems associated with connection of wave energy converters directly to the power grid have been analyzed. The need for a grid emulator was discussed and then the specifications of the grid emulator were illustrated. This research aims at providing the preliminary research findings into the grid emulator technology to be installed at the PMEC-SETS, which would speed up the process of grid connection of wave energy by identifying appropriate WECs for different sea states and varying grid conditions. The grid emulator is capable of emulating different grid conditions, thereby allowing manufacturers around the world to utilize this facility and reduce the certification time of their devices.

The specifications for the grid emulator under development and the preliminary tests that are planned in using this device were discussed. The design of the grid emulator followed from the design of NREL's CGI and the working of a 3L-NPC-VSC topology were described. Due to compatibility issues between the physical model and the dSPACE 1103 controller board in providing satisfactory results, the converters

were modeled in native Simulink. The results between the physical model and the native Simulink model were illustrated and found to correlate well. The native Simulink model represents the converters to a sufficient degree of accuracy.

With an increase in the renewable energy portfolio, devices like the grid emulator will definitely help in increasing the grid integration of distributed energy resources and with an increased renewable energy penetration, the states and countries inch toward their renewable energy goals.

6.2 Recommendations for Future Work

This report details the modeling of the rectifier and inverter in native Simulink. Parameters such as the capacitor bank ratings, the transformer ratings and dc bus voltage levels used for simulations were taken from NREL's CGI. Determining these quantities for this specific design would result in more accurate representation of the actual hardware to be developed.

The converter modeling in Simulink does not consider dead times in commutation and the switching loss, however, an actual hardware converter has both dead time between switch commutation as well as switching loss. Simple LC filters could be used at the inverter output terminals in order to reduce the harmonics in the waveforms. The control loop models for both the inverter and rectifier involve reference frame transformation from a-b-c to d-q. These control loops will provide sufficiently accurate results in the case of balanced systems. In the case of an unbalance in the system, a zero sequence component should be added to the d-q reference frame

leading to d-q-0 reference frame, thereby increasing the complexity of the model. The details for the in lab HIL setup of the grid emulator have been detailed in chapter 5. The first step in the hardware interfacing is placing the dSPACE I/O blocks in the Simulink model and replacing the sine-triangle PWM on the WEC-side converters to receive switching signals from the ABB AC 800 PEC.

The model should be able to transfer power in both the directions i.e., the converters behave like a rectifier and inverter interchangeably. Energy storage systems have to be integrated in order to smoothen the power before delivery to the grid.

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