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Frederick Martin Senk, Jr. for the M. S. in Electrical Engineering
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Title THE DESIGN AND EVALUATION OF AN ELECTRONIC ESTIMATOR OF PROBABILITY DENSITY DISTRIBUTIONS

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This thesis discusses the design and evaluation of an instrument that can estimate the probability density distributions of band-limited, aperiodic, electrical phenomena.

This estimator can obtain the probability density estimates of signals that are contained within the frequency range of 100 cps. to 20 kcs. However, the basic design logic of the instrument can serve as a design foundation for a device that should be capable of estimating the distributions of signals that range in frequency from a fraction of a cycle to 50 kcs.

Transistors and solid-state diodes are used in the instrument's circuitry. This device, however, is not a transistorized version of another instrument.

Area error, form factor, and end-point error evaluation techniques are discussed, modified and then combined to develop a

procedure which will determine an instrument's frequency-dependency characteristics. The author also introduces an evaluation technique (the pseudo impulse test) that involves the use of a test signal that has a theoretical probability density distribution which contains a series of impulse functions. The pseudo impulse test is a powerful technique which will reveal the operating capabilities of an instrument. All the evaluation techniques discussed here may be used to evaluate any device that is designed to estimate probability density distributions.

The appendix contains information that may be helpful to those who would like to duplicate or improve the instrument.

# THE DESIGN AND EVALUATION OF AN ELECTRONIC ESTIMATOR OF PROBABILITY DENSITY DISTRIBUTIONS

by

FREDERICK MARTIN SENK, JR.

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Redacted for privacy

Head of Electrical Engineering

Redacted for privacy

Dean of Graduate School

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## PARTIAL LIST OF SYMBOLS AND ABBREVIATIONS

| | |
|---|---|
| AND-n | Gate which performs the logical "and" operation. * |
| CON-n | Control. * |
| DC AMP | Direct-coupled amplifier. |
| EF-n | Emitter follower. * |
| EPE | End-point error. |
| INT RESET | Integrator reset. |
| M-n | Mono-stable multivibrator. * |
| OR-n | Gate which performs the logical "or" operation. * |
| P | Sampling interval. |
| PA-n | Pulse amplifier. * |
| PDD | Probability density distribution. |
| PIA-n | Pulse-inverting amplifier. * |
| PW | Pulse width. |
| ST-n | Schmitt trigger. * |
| SW | Slit width |

*n is the number of the specific device.

# THE DESIGN AND EVALUATION OF AN ELECTRONIC ESTIMATOR OF PROBABILITY DENSITY DISTRIBUTIONS

## INTRODUCTION

The engineer is forced, with the increase of complexity and sophistication of modern engineering, to acquire extensive knowledge about the environment in which he works. Therefore, statistical concepts and techniques are rapidly finding application in many engineering investigations. It may be helpful, in some cases, to obtain a rapid and inexpensive estimate of the probability density distribution of the phenomenon in question.

This thesis will discuss the design and evaluation of an electronic estimator of probability density distributions of band-limited electrical phenomena. The input information, as supplied to the instrument, is electrical in form but the device is capable of estimating the probability density distributions (hereafter referred to as PDDs) of any phenomena that can be converted into the electrical domain.

Instruments that estimate PDDs have been made before (1, 4, 5). All past designs involve the use of vacuum tubes and some even use optical devices to obtain the desired result.

The instrument described herein employs transistors and

solid-state diodes in its circuitry. This is not a transistorized version of another instrument. Therefore, the basic instrument logic and circuitry have not been used, to this writer's knowledge, for this purpose before. Transistors were selected because they can do more in less space, with less input power and with much greater reliability than the vacuum tube.

Subsequent pages will show that the basic principles of estimating PDDs are common to all known instruments that attempt to perform this task. What differ , between instruments, are the methods employed to implement these ideas.

It is not an easy task to evaluate the performance and accuracy of an instrument that is designed to estimate PDDs. The section on system evaluation will explore several techniques that will be helpful in evaluating the PDD estimator. Some of the techniques are new and are presented here for the first time.

All PDD estimators are band-limited. The upper-frequency limit of past estimators has been about ten kcs or less. The instrument described here is capable of producing good PDD estimates of periodic or aperiodic phenomena that extend in frequency to 20 kcs. or higher. With some circuit improvement this system should be capable of estimating the PDDs of signals that extend up to 50 kcs. with excellent results.

The appendix contains information that will be helpful to anyone that would like to duplicate this particular instrument.

# BASIC CONCEPTS

This section will discuss the basic philosophy that is common to all known estimators of probability density distributions.

## The Quantizing Process

Let us take a signal e(t), as shown in figure one, and arbitrarily strike off 5 equally spaced quantizing intervals. A tabulation can be made of the total time e(t) remains in each interval during a predetermined time P. P is called the sampling period. The total time e(t) is in interval one during P is:

$$\text{Total Time} = t1 + t2 + t3 \tag{1}$$

The probability that e(t) is within the confines of interval one during P is:

$$Pr(1) = \frac{t1 + t2 + t3}{P} \tag{2}$$

Probability calculations for the remaining four intervals can be made by following this same procedure.

The sampling period is the same for each calculation, and so the total time e(t) spends in a particular interval is directly proportional to the probability that e(t) is in this interval. Physical

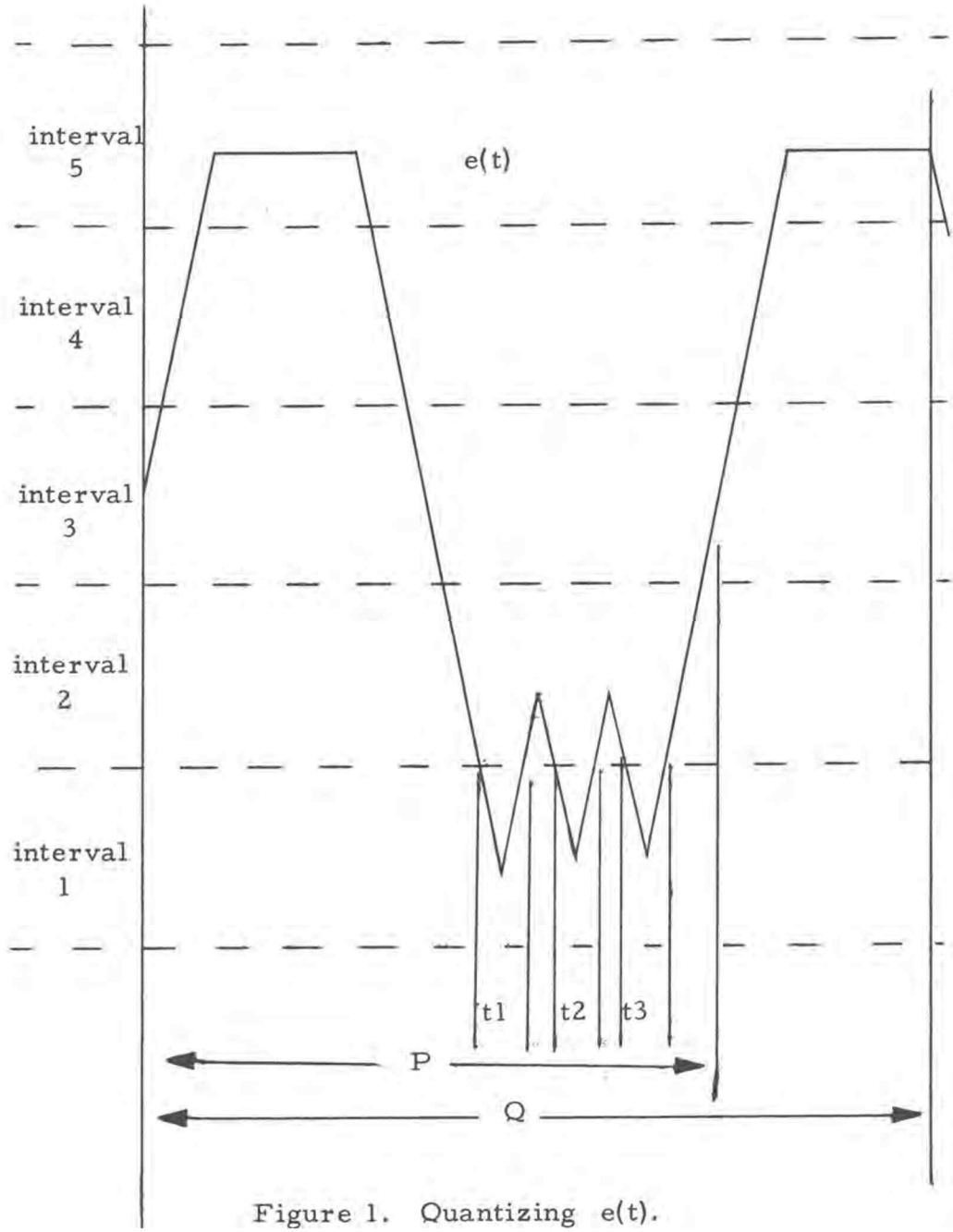


Figure 1. Quantizing e(t).

division by P, to obtain the probability of any e(t) within any interval, is not necessary if P is constant for all e(t)s. [1] The sampling time, with this method, corresponds to a probability of one. The probabilities obtained, by applying the above method to an e(t), can be used to construct a line graph as shown in figure two. The ordinate is calibrated in probability and abscissa in intervals which correspond to voltage intervals. [2] The sum of the line heights equal one.

A histogram can also be constructed from the same probability data, but the ordinate calibration must be adjusted so that the total area contained within the histogram is equal to one.

If the number of quantizing levels is increased and the interval spacing made smaller, a point will be reached where the histogram will, for practical purposes, become similar to a line graph. In the limit, as the increment widths approach zero and the number of quantizing levels approach infinity the histogram becomes a smooth curve that is called a continuous probability density distribution (2, p. 24). The application of the methods described in the preceding paragraphs will yield estimates of the probability density distributions for any e(t). However, the inability to approach the limit,

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1 This procedure will yield a number that is only proportional to the time e(t) is in a particular interval.

2 The abscissa will be calibrated so as to correspond to the phenomenon under investigation; eg, if a force relationship is being investigated it will be necessary to employ a transducer to convert the mechanical information into the electrical domain.

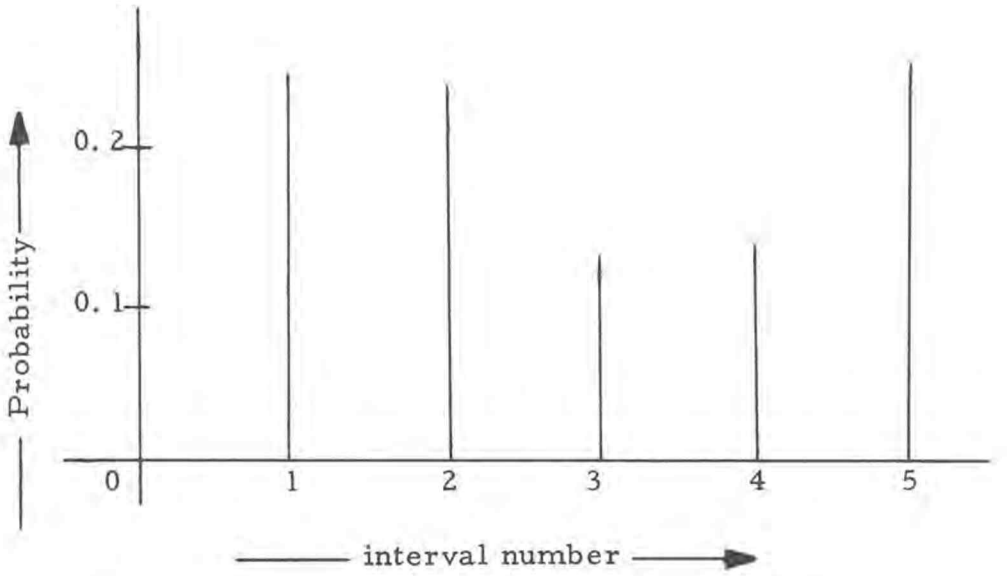


Figure 2. Line graph with sampling period P.

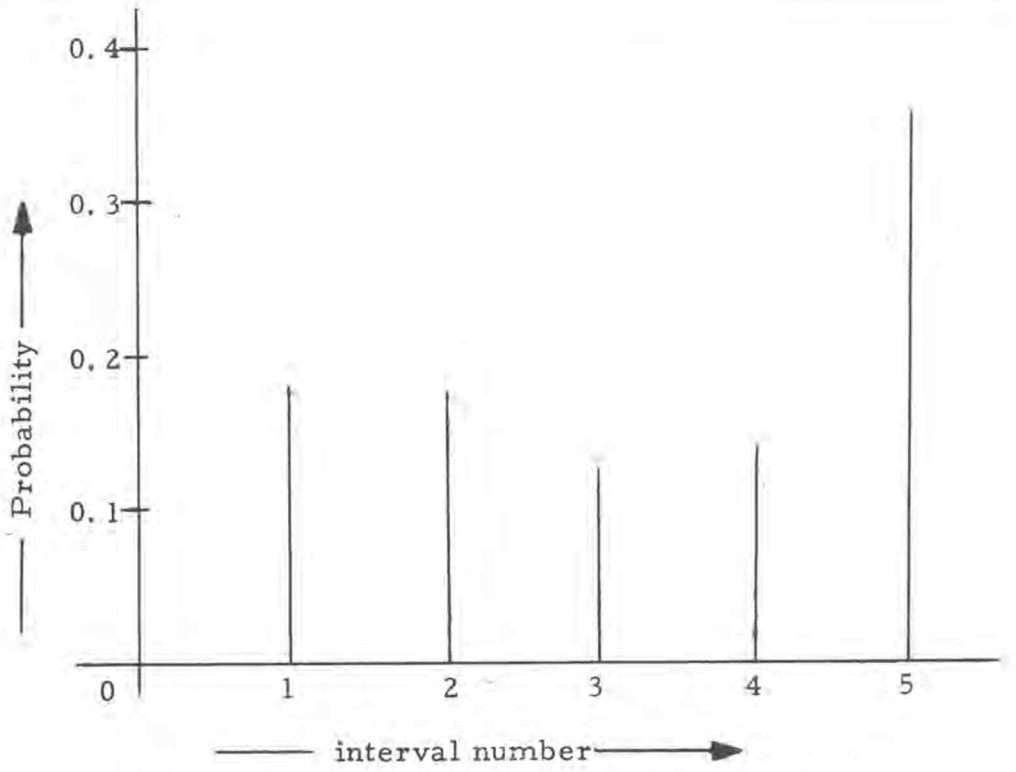


Figure 3. Line graph with sampling period Q.

in practice, forces acceptance of a discreet probability density distribution that, it is hoped, will approach a line graph.

The Sampling Period

The length of the sampling period P will influence the accuracy of a distribution estimate. If e(t) is periodic and P is equal to an integral multiple of the period of e(t), there is no problem. A glance at figure 1 will illustrate the problem that will occur when P is not an integral multiple of the period of e(t). Let the sampling period for this example equal Q. Figure 3 is the line graph of this condition. Comparison with figure 2 illustrates the effect of this type of error.

The obvious solution to this dilemma is to make the sampling period much longer than the longest possible period of e(t). Bocharov and Stakhovskii (1, p. 155) state that P should be about 10 to 15 times larger. The author has found that experimentally, this is a realistic estimate for the length of P. There will be some error but it will be small. [1]

All known electronic devices that have been built to estimate probability density distributions (PDD) use, as a basis of design,

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[1] Five percent error results if e(t) is sinusoidal and the period of P is ten times longer than that of e(t).

the ideas given in the preceding paragraphs.

The PDDs of periodic phenomena may be directly obtained by calculation or by graphically applying the above techniques when calculation becomes difficult. This is not the case with aperiodic phenomena as there isn't one specific waveform or equation that will describe type processes in the time domain. Herein lies the justification, other than for academic reasons, for developing a device that can estimate probability density distributions. Periodic functions will still be used to describe and illustrate the various logical operations of a PDD estimator. Periodic functions also serve the important function of being calibration standards. A considerable portion of the evaluation section will be devoted to this topic.[1]

## Parallel Interrogation

It was noted earlier that many closely spaced quantizing levels are needed to obtain a reasonable estimate of a PDD. This method is called parallel interrogation and when electronically implemented, requires many components and consequently is expensive.

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[1] See page 44.

Serial Interrogation

Serial interrogation is a simple and less expensive method of estimating PDDs.

This method makes use of a single quantizing interval. Instruments such as the gamma-ray spectrometer also use a single interval which is called the window. In the following discussion the term slit will be used, as a slit is generally narrower than a window and therefore implies a greater power of discrimination.

Conceptually, the simplest method of serial interrogation involves the use of a single slit that can be changed in position. For example, let us place a slit, with a width that is equal to one of the intervals shown in figure 1, in the location of interval 1. Let the slit occupy this interval for one sampling period, P, and then move to the location formerly occupied by interval 2. The slit will remain in interval 2 for one P, then it will move to the location of interval 3. This process will continue until all the interval locations have been visited. Once the slit has occupied interval 5 for one P it will "reset" back to the location of interval 1 and the process will start anew. In this example, one moveable slit has done the job of five fixed slits. Therefore, serial interrogation can replace the large number of intervals needed for successful parallel interrogation by

a single slit with variable position. Unfortunately, it is very difficult to use electronic circuitry to vary the slit location accurately.

An alternate but practical method of serial interrogation is shown in figures 4, 5 and 6. The signal under investigation e(t), (figure 4) is added to a staircase scanning signal, e(scan), (figure 5) to yield the waveform shown in figure 6. The single-fixed quantizing interval (the slit) is bounded by zero and v(s). e(t) + e(scan) is within the quantizing interval when:

$$0 \leq e(t) + e(scan) \leq v(s) \qquad (3)$$

This method will yield results that are identical to those obtained by using the variable slit. In the first but impractical method the slit is scanned across the signal whereas in the second method the signal is scanned across the slit.

Linear Scanning

The number of interval locations may be increased by increasing the number of individual steps in the staircase, e(scan). The step heights, h, will be reduced if the total staircase height, 2 Em, is fixed and the number of steps in the staircase is increased. A point will be reached, in this process, where the staircase function may be replaced by a linear scanning signal. The adoption of a

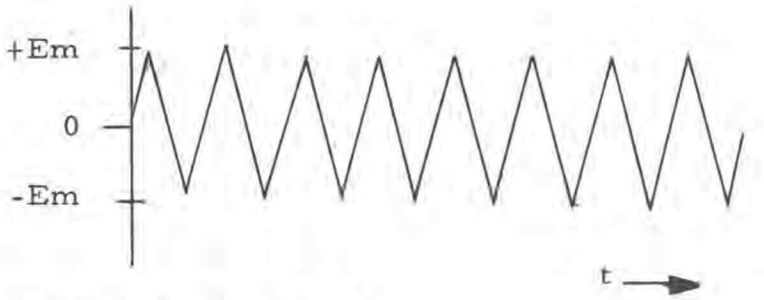


Figure 4. Signal e(t).

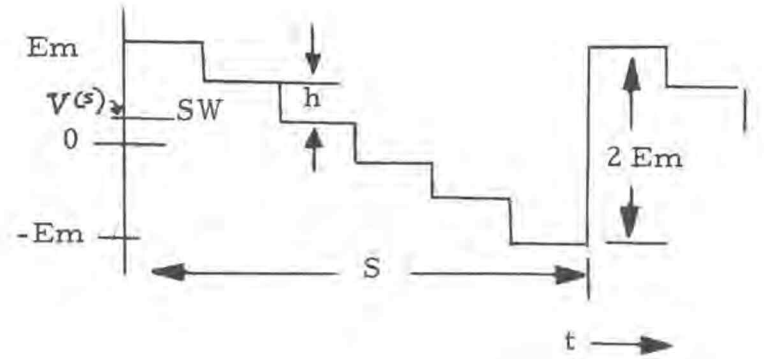


Figure 5. Staircase scanning signal e(scan).

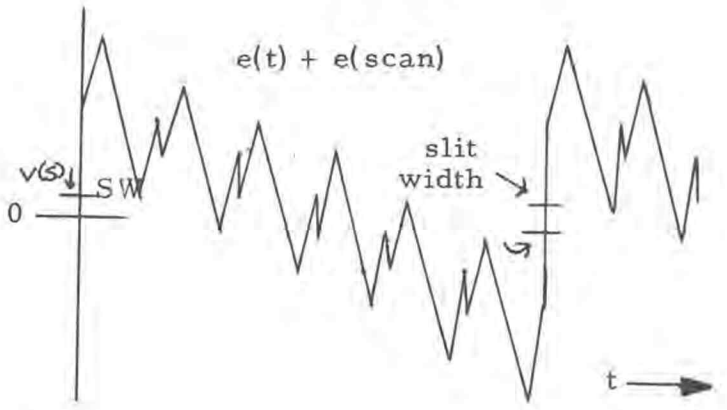


Figure 6. e(scan + e(t).

linear-scanning signal further reduces interrogation cost.

System Speed

Parallel interrogation is faster than serial methods by a factor that is about equal to the period of the scanning signal less the sampling period. It is conceivable that the total serial-interrogation time could be hours, perhaps even days. There will be a point where the time expense will be greater than the instrumentation cost; then parallel interrogation, or the marriage of the two systems, will become economically feasible.

Effective Interrogation

For an effective interrogation of e(t) the slit-width (SW) should be as narrow as possible and the magnitude of e(t) as large as possible. However, e(t) maximum must be equal to, or less than e(scan) maximum.

The instrument described in this thesis uses the system of serial interrogation with linear scanning.

# THE SYSTEM

This section will discuss the system logic and circuit requirements of the probability density distribution estimator. The fold-out, figure 37, on page 101 is the complete block diagram of this system.

## The Basic System

A simplified block diagram of this system is shown in figure 7. This instrument employs the method of serial interrogation and therefore has many interrogation cycles per scanning period. There are three cycles to each interrogation cycle and they are, in proper timing sequence: sample, record, and reset.

The input signal, e(t), is scanned across the slit by a linear scanning voltage of e(scan). The period of e(scan) is much longer than the sampling period.[1] The interrogation path is from the negative extreme of e(t) to the positive extreme.

The slit will interrogate e(t) only during the sample portion of the interrogation cycle. The output of the slit is in pulse form.

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[1] The period of e(scan) will be about one hundred to two hundred times as long as the sampling period (interval), P. With P of 100 milli-seconds the scanning signal's period will be about 20 seconds. An example of a PDD estimate that was obtained with a 20 second, e(scan), period may be found on page 71.

Everytime e(t) traverses the slit a pulse, that has a width that is proportional to the time e(t) is within the confines of the slit, appears at the slit's output. The pulse's magnitude and rise-fall times are constant. Only the width of the pulses vary.

An integrator, driven by the slit output, acts as a time summer during each sampling cycle. The output of the integrator is proportional to the total time e(t) is in the slit during each sampling cycle.

The vertical output circuitry combines the integrator output with a pulse (called the read pulse) of constant magnitude and width to yield an output pulse whose height is proportional to the output voltage of the integrator. This operation is done during the record cycle. When the record cycle is over, the integrator is set to zero and the sampling cycle starts anew. The vertical output signal is connected to the vertical input of the display cathode-ray oscilloscope (CRO).

The horizontal input of the display CRO is driven by the sweep signal generated within the internal control unit by the same circuitry that generates the scan signal. The sweep and scan logic will be called the sweep-scan logic. The vertical output of the estimator is a voltage that is proportional to the probability that e(t) is in a particular interval. The horizontal output is a linear voltage

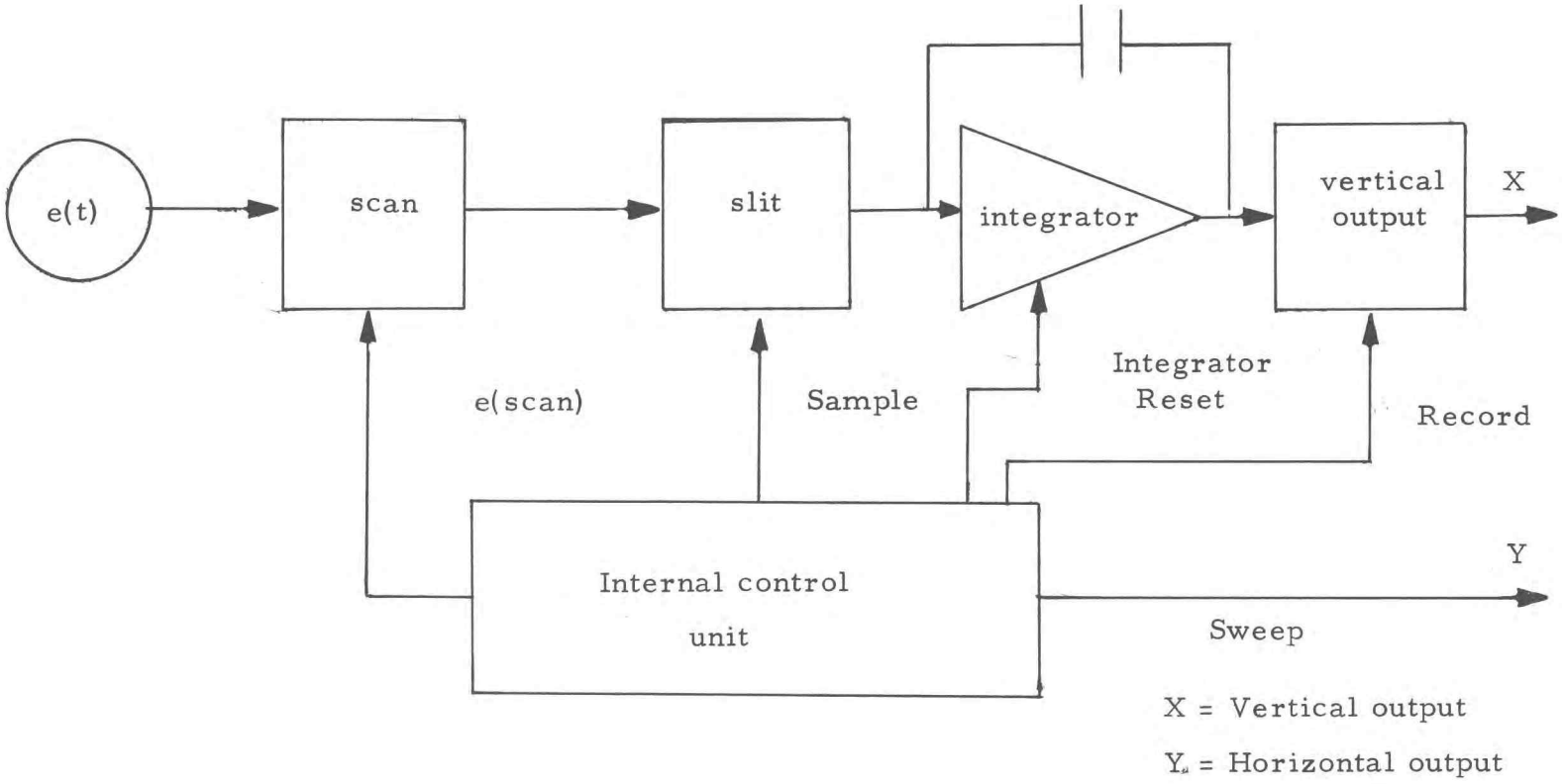


Figure 7. Simplified system logic for the PDD estimator.

whose displacement is proportional to that interval. The horizontal deflection of the display is therefore proportional to the level of e(t) that is being interrogated. A waveform that corresponds to the probability density distribution of e(t) will be presented on the screen of the display CRO. Display direction is from left to right (negative to positive).

## Detailed Logic

Let us look in detail, with the overall picture in mind, at the complete logic of this instrument. Figure 37, page 100 will be used as a guide.

### Input

The input signal, e(t), is applied to the input emitter follower EF-1. EF-1 isolates the input signal from the internal circuitry. The input to EF-1 is capacitor coupled but all other logic used in this instrument are direct coupled. The maximum magnitude of e(t) is limited to three volts. This limitation is due, in part, to the low supply voltages that are used in the instrument.[1]

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[1] The supply voltages are ten volts. Low supply voltages are necessary so that all the transistors, used in the instrument, are operating well within their voltage ratings.

Scanning Circuitry

The scanning circuitry consists of a simple resistance adder. The output voltage of this adder is directly proportional to the sum of e(t) and e(scan). The centering control, CON-1, can be used to adjust the PDD estimate's horizontal display position.

The Slit

The basic logic components that make up the slit circuit are: EF-2, PIA-1, AND-1, and PA-1.[1] Slit operation will be shown by using actual photographs (figures 8 and 9) that were taken during one sample cycle.

The output of EF-2 is connected to one input of AND-1. EF-2's output is also coupled to the slit-width control CON-2 (figure 8A). The variable tap of CON-2 is connected to the input of PIA-1. The output voltage of PIA-1 is called the inhibit signal. The output of PIA-1 (figure 8B) is connected to the other input of AND-1. AND-1 will open (an output) when the inhibit signal is positive and when there is also a positive voltage appearing on the output of EF-2. Inhibiting (closing the gate) occurs when the output of PIA-1 goes to zero.

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[1] See the symbol key for definition of terms.

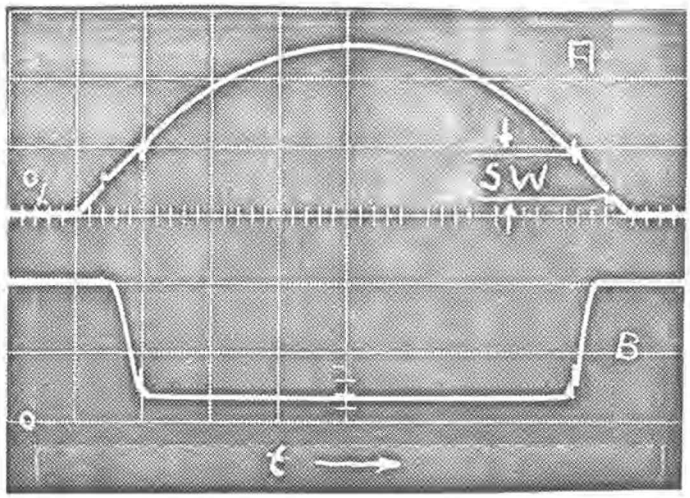


Figure 8. A. The output of EF-2. The ordinate is 2.0 volts per large division. Abscissa is 10 micro-seconds per large division.

B. The inhibit signal. The ordinate is 5.0 volts per large division. Abscissa is 10 micro-seconds per large division.

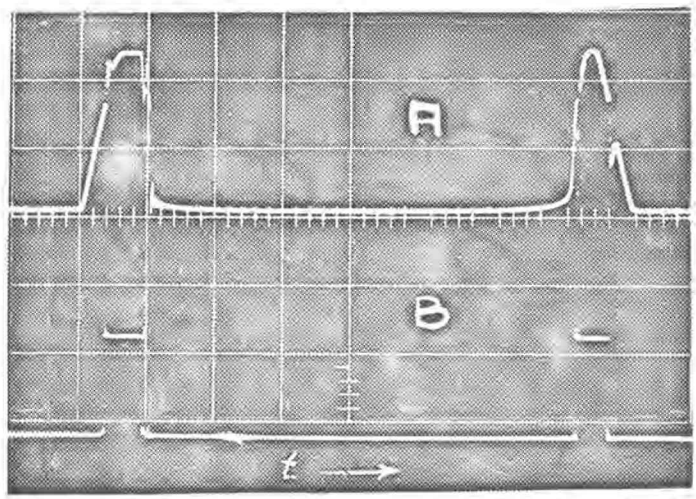


Figure 9. A. The primitive slit output. The ordinate is 0.5 volts per large division. Abscissa is 10 micro-seconds per large division.

B. The output of PA-1. The ordinate is 5.0 volts per large division. Abscissa is 10 micro-seconds per large division.

The slit-width control acts as a triggering-threshold control for PIA-1. PIA-1 can be turned on (inhibit) at any point along the output waveform of EF-2.

The output of AND-1 will be a pulse (figure 9-A) whose base width is equal to the time that the output waveform of EF-2 has gone from zero volts to the point where PIA-1 triggers. The triggering-threshold level of PIA-1 is in effect the primitive slit-width.

Unfortunately, the output of AND-1 is not a very good pulse; it varies in magnitude, width, and rise-fall times. The function of PA-1 is to hold the magnitude of the rise and fall times of the slit's output pulses constant.

Figure 10-B illustrates a typical output pulse group coming from PA-1. Note the fast rise and fall times (less than 50 nanoseconds). The fixed triggering threshold level of PA-1 tends to narrow the slit. The slit narrows from one volt to about 0.8 volts.

The output of the resistance adder, k [e(t) + e(scan)] is amplified by a direct-coupled feedback amplifier, DC AMP. The principal function of this amplifier is to effectively narrow the instrument's slit width. The true, or effective, slit width may be defined as:

$$\text{Effective slit width} = \frac{\text{PASW}}{\text{SA}} \qquad (4)$$

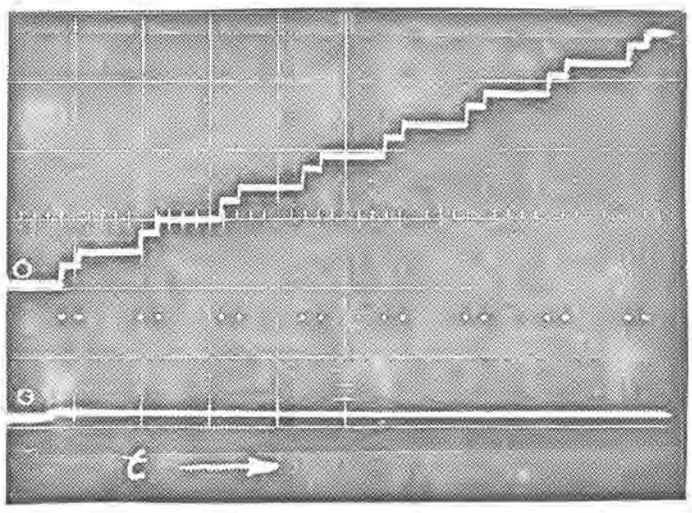


Figure 10. A--Upper trace. The integrator output.
Ordinate 0.1 volts per large division.
Abscissa 10 milli-seconds per large division.

B--Lower trace. The input to the integrator.
Ordinate 5.0 volts per large division.
Abscissa 10 milli-seconds per large division.

PASW is the slit width that was measured by comparing the output of PA-1 with the output of EF-2.[1] SA is the system's voltage amplification factor. SA is measured from the input of EF-1 to the output of EF-2. The calculation of the effective slit-width is simple. From the information obtained from figures 9 and 10, the value of PASW will be equal to 0.8 volts. The gain of the DC AMP is adjusted so that the AS will be equal to 10. The effective slit width, using equation 4, will be equal to 0.08 volts.[2] It is very important to note that a small change of PASW (from component drift, etc.) will have very little effect on the width of the effective slit. Therefore, the addition of a direct coupled feedback amplifier to the basic slit logic is a simple method of obtaining a narrow and stable slit.

The instrument's input signal, e(t), is a sinusoidal, but a glance at figure 8-A will reveal that the output voltage of EF-2 is not a sine wave.[3] This limitation, however, will have little effect on the end result. The DC AMP, if properly designed, will always

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[1] See figures 8-A and 9-B.

[2] A better and more practical method of determining an instrument's effective slit width is given in the section covering instrument evaluation. See page 56 for details.

[3] Supply voltages that are greater than 30 volts, as well as a different complement of transistors, are needed to amplify the entire waveform of [e(t) + e(scan)]. Supply voltages of 10 volts are used in this instrument.

linearly amplify the portion of e(t) that is being interrogated. The amplifier must possess excellent overload recovery characteristics, as it will be operating a good portion of the time in its cut-off or saturated regions.[1]

The slit's output amplifier, PA-1, is connected to the integrator only during the sample cycle. AND-2 performs this logic.

EF-3 was included in the logic late in the instrument's debugging operation. Its main function is to reduce the effect of the distributed circuit capacitance that is present between AND-2 and the integrator. There is a good possibility that this particular emitter follower could be eliminated by using better component lay-out techniques.

## The Integrator

The integrator used in this instrument must provide an output voltage during each sampling cycle that is porportional to the sum of the widths of the pulses coming from the slit logic. Therefore, this integrator is a time-summing device. This integrator, however,

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[1] Amplifier overload is the condition that exists when the input signal's magnitude is so large that the amplifier is forced to operate in its non-linear region. The amplifiers transistors, in the extreme case of overload, will be in either a cutoff or saturated condition. Good amplifier overload recovery means that the amplifier must be able to go, from a saturated or cutoff condition, rapidly into a linear region.

does not have to perform all the varied tasks that are demanded of an operational-amplifier type integrator. The integrator used in the PDD estimator should be capable of responding to pulses which vary in width from 100 milli-seconds to 100 nano-seconds or less.[1] The actual input-output response of the integrator is shown in figure 10.

Figure 10-A shows the integrator output over one sampling interval. The sampling interval, P, is equal to 100 milli-seconds.

Figure 10-B is the trace of the input pulses that are responsible for the response seen in 10-A. The input pulses appear to be dots, as the rise times were too rapid to register on this particular photograph.

## The Vertical Output Logic

The vertical output logic which involves the use of a two-input and gate, AND-3, combines the integrator output and the record timing pulse to give an output pulse whose height is proportional to the integrator's output voltage.

The envelope switch, CON-10, can disconnect AND-3 from this record bus. With CON-10 off the complete integration cycle

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[1] See page 36.

will appear in the vertical output waveform. See figures 25, 26, 31, and 32.

## Integrator Reset

Once the record cycle has been completed, the integrator will be reset. The reset function is performed by the INT-RESET logic. OR-1 supplies the reset circuitry with pulses coming from the integrate-reset generator, M-4, or from the sweep-scan reset bus. The sweep-scan reset signal will prevent integrator response during the sweep-scan reset cycle.

## The Control Unit

The control unit must:

1. Supply the sweep and scan signals.
2. Supply the sample, record, integrator reset timing signals.
3. Coordinate the above two functions into a workable sequence. This logic will prevent the sweep-scan signal from being reset until the interrogation cycle in process is completed. For example, if a sampling or record function is in process, the logic will prevent the sweep-scan circuitry from being reset until the integrator-reset cycle occurs. When the sweep-scan reset cycle has been completed, the new interrogate cycle will begin with the sample period.

## Sweep-Scan Logic

The sweep-scan function may be performed manually by using the manual sweep control, CON-9, or automatically with the sweep-scan generator.

The sweep-scan generator is a Miller-sweep circuit. The sweep-scan rate is controlled by the sweep-rate control, CON-3. EF-5 drives the resistance adder and a direct-coupled amplifier which inverts the scan signal to form the sweep signal. This inversion allows the output sweep signal to vary from ground potential to plus ten volts. The scan signal linearly decreases from plus ten volts to ground. The inversion process is necessary so that the horizontal sweep of the display CRO will sweep from left to right. The inverting amplifier should have a voltage amplification of about one.

## The Sweep-Retrace Clamp

The sweep-retrace clamp is used to reduce the sweep retrace time. The reset time of the scan signal is not effected by this logic.

EF-6 is the instrument's horizontal output amplifier. This particular emitter follower also drives a Schmitt-trigger circuit, ST-1. ST-1 triggers the reset for the sweep-scan logic. The

triggering threshold is adjusted by the sweep length control, CON-4.

The sweep-scan reset timing generator, M-1, is set to "reset" by the Schmitt trigger through PIA-2. M-1 is a mono-stable multivibrator which is designed to trigger on negative-going pulses so as to reduce the possibility of falsely triggering the device with noise. PIA-2, then, supplies the needed negative-going triggering signal as soon as the Schmitt trigger fires. The timing of M-1 is controlled by CON-5. A system start-reset push button, CON-11, is connected to M-1. This switch, when depressed, will start the system operation or reset the sweep-scan generator so as to start a new interrogation sequence.

PIA-3 was added to the circuit logic to improve the rise time of the not-sweep reset signal generated within M-1.[1]

## The Interrogate Sequence

This sequence is composed of the sample, record and integrator-reset cycles. This timing is controlled by M-2, M-3, and M-4 respectively. All are monostable multivibrators.

A regenerating closed-loop condition exists between M-2, M-3, and M-4 if the not-sweep signal is present. When M-2 turns

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[1] Many hours of debugging time were spent finding this particular cause of erratic operation.

off (to the not-sample state) M-3 is triggered. M-4 is triggered by M-3 in a similar manner. This loop is open during the sweep-scan reset period. M-4 will be retriggered, via OR-2 and EF-8 when the sweep-scan reset signal goes off.

The not-sample and not-record outputs of M-2 and M-3 feed, along with the reset output of M-1, the input of AND-4. A sweep-scan reset signal is present when all the inputs of AND-4 are up. This is the logic that will allow the interrogation cycle in process to complete its sequence before the sweep-scan signal is reset.

# KEY CIRCUITS

The slit and integrator are the key circuits used in the PDD estimator. The discussion concerning the slit and integrator logic may be found in the preceding section. This section will discuss the circuits that are used to implement this logic.

A brief discussion of the other, but more conventional, circuits used in the device may be found in appendix I.

The complete schematic diagram, figure 38, of the PDD estimator may be found in appendix VI, page 101.

Appendix II contains a table which will correlate transistor number and type to the logical block in which it is contained. This table may be used to correlate the complete schematic diagram with the system logic.

## The Slit

The slit circuit that was selected for use in this estimator is the result of about a month of experimentation. Many circuits such as the Schmitt trigger and transistor - pulse amplifiers were designed and then connected in various, and sometimes complex, configurations to obtain the desired slit effect. The best results, however, were obtained with the simple circuit shown in figure 11.

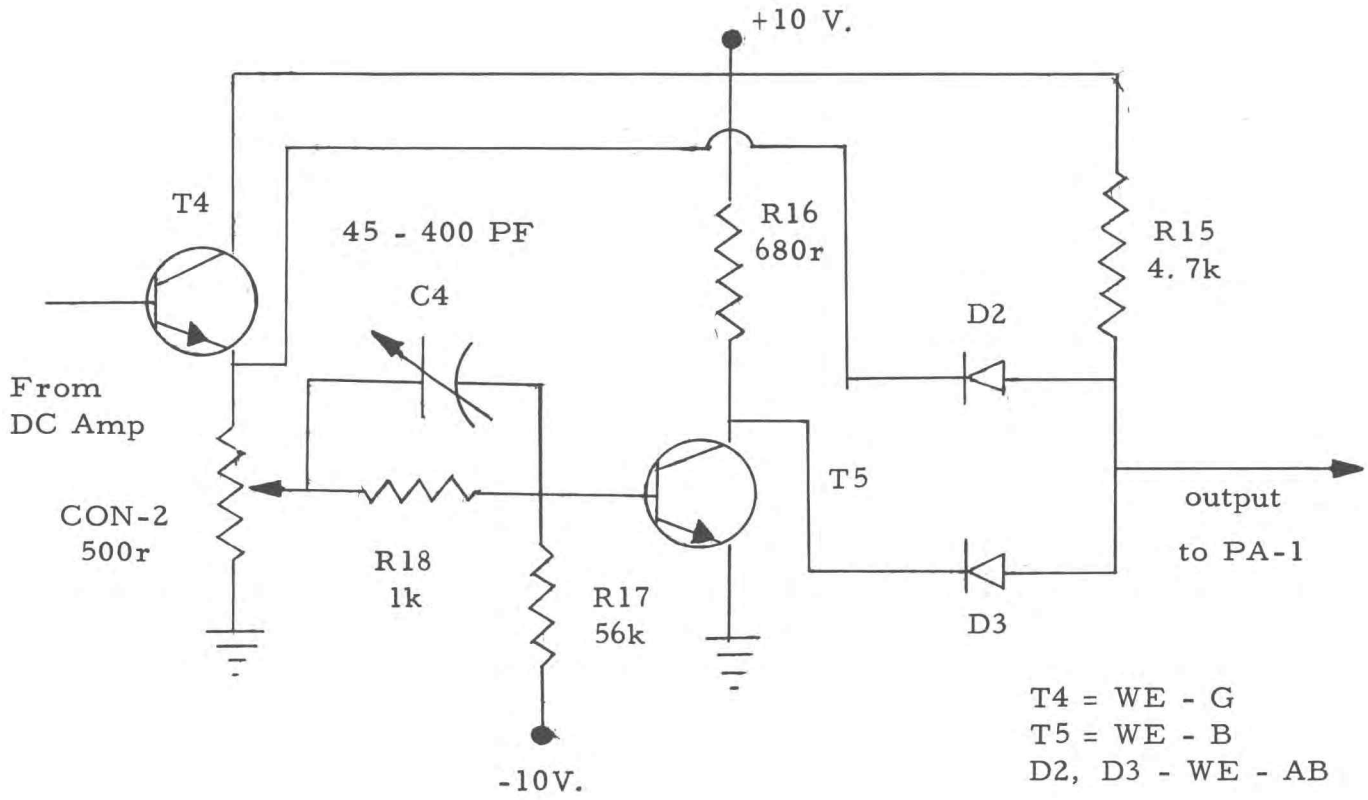


Figure 11. The primitive slit circuit.

The first stage of primitive slit circuit is an emitter-follower amplifier EF-2. EF-2 contains, CON-2, the 500 ohm slit-width potentiometer, and T4.

T4 will be cut off when the output voltage of the DC amplifier is zero. There will, however, still be a voltage drop across CON-2. This voltage is due to the current path that runs from the ten volt supply through R15, D2 and CON-2 to ground. The output of the primitive slit under zero signal conditions will be equal to the sum of the voltage drops across D2 and CON-2. This output voltage should be made as small as possible. Therefore, the value of CON-2 should also be as small as possible. The dissipation rating of T4, which uses CON-2 as a load, is the factor that limits the value of this potentiometer to 500 ohms.

The center tap of CON-2 feeds the input of the resistance-coupled pulse amplifier, PIA-1. This amplifier consists of the input resistor R18, a variable speed-up capacitor C4, a bias resistor R17, a load resistor R16, and the transistor T5. T5 will normally be operating in a cut-off or saturated condition. The alignment procedure that involves C4 may be found in appendix IV, step number 18.

R15 is the "and" resistor for AND-1. The value of R15 was determined experimentally and with the circuit shown in figure 11, should be kept within the range of 3.3k to 5.6k ohms for good slit

operation. However, the frequency response of AND-1 can be improved by reducing the value of R15 to 1 k ohms or less. If this is done the value of the slit-width potentiometer (CON-2) must be proportionally reduced and a transistor with a higher dissipation rating must be selected for T4. Care also must be taken to insure that the ratings of D2, D3 and T5 are not exceeded.

The output of the primitive slit is coupled to the pulse amplifier, PA-1. The function of PA-1 is to hold the magnitude and the rise and fall times of the slit's output pulses constant. The circuit of this pulse amplifier may be found on the complete schemetic, page 101. PA-1 uses T6 and T7. This amplifier was designed using worse case techniques that were recommended by Texas Instruments (7).

Photographs of the slit operation may be seen in figures 8 and 9, page 19.

Slit Width Characteristics

The following is a discussion of the effect of slit width on the high-frequency performance of the probability density distribution estimator:

A sine wave will be used in the discussion. The input signal is equal to:

$$e(t) = Em \sin wt$$

where wt is in radians.

e(t) is placed in the system in such a way that its center is at the same voltage level as the center of the slit. This condition is shown in figure 12.

The rate of change of e(t) is the fastest at the points where wt is equal to $\pi(n-1)$, where $n=1, 2, 3, \ldots\ldots\ldots\ldots$

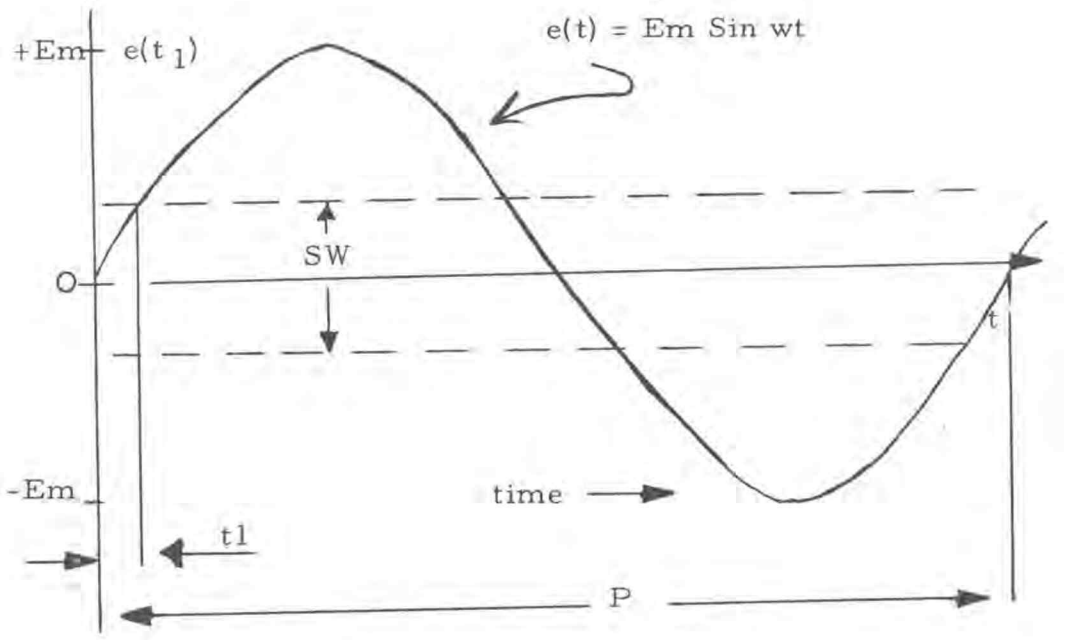


Figure 12. e(t) and the slit.

The signal and the slit, in figure 12, are positioned so that the time e(t), remains in the slit, is the shortest of all the possible position combinations of e(t) and the slit.

Let $t_t$ equal the total time that e(t) spends in the slit during P. It can be seen, from figure 12, that:

$$t_t = 4t_1 \tag{5}$$

Where:

$$t_1 = \frac{\text{Arcsin}\left[\frac{e(t)}{Em}\right]}{w} \tag{6}$$

Hence:

$$t_t = \frac{4}{w}\ \text{Arcsin}\left[\frac{e(t)}{Em}\right] \tag{7}$$

Let:

$$w = 2\pi f\ ,$$

where f is the frequency in cycles per second. If $\frac{e(t1)}{Em}$ is small, for our purposes less than . 25 radians:

$$t_t = \frac{2e(t1)}{\pi f Em} \tag{8}$$

But e(t1) equals $\frac{SW}{2}$ where SW is the slit width in volts.

HENCE:

$$t_{t_{Min.}} = \frac{SW}{\sqrt{\pi f Em}} \qquad (9)$$

Figure 13 is the plot of equation 9. A value of two volts was selected for Em so that the plot can be correlated, if desired, to the PDD estimates displayed in figures 23 through 36.

The slit circuitry will generate a pulse that has a width which is proportional to the time e(t) is in the slit. Generally, this width will be slightly less than the time e(t) is in the slit. Of course this is no problem as long as the proportionality is maintained. Unfortunately, the proportionality cannot be maintained because a finite time is required for the circuitry to "recognize" the presence of the signal, respond, recognize the lack of a signal and respond again.

From figure 13 we can see that the pulse width rapidly decreases as the frequency is increased from zero to 10 kcs. Leveling-off begins from 10 to 20 kcs - depending on the slit width used. It is understandable, then, why past estimators have not been too successful in estimating the PDD's of signals that extend beyond 10 kcs.

Modern transistors in well designed circuitry have: short delay, rise, storage, and fall times. The results shown in figure 13

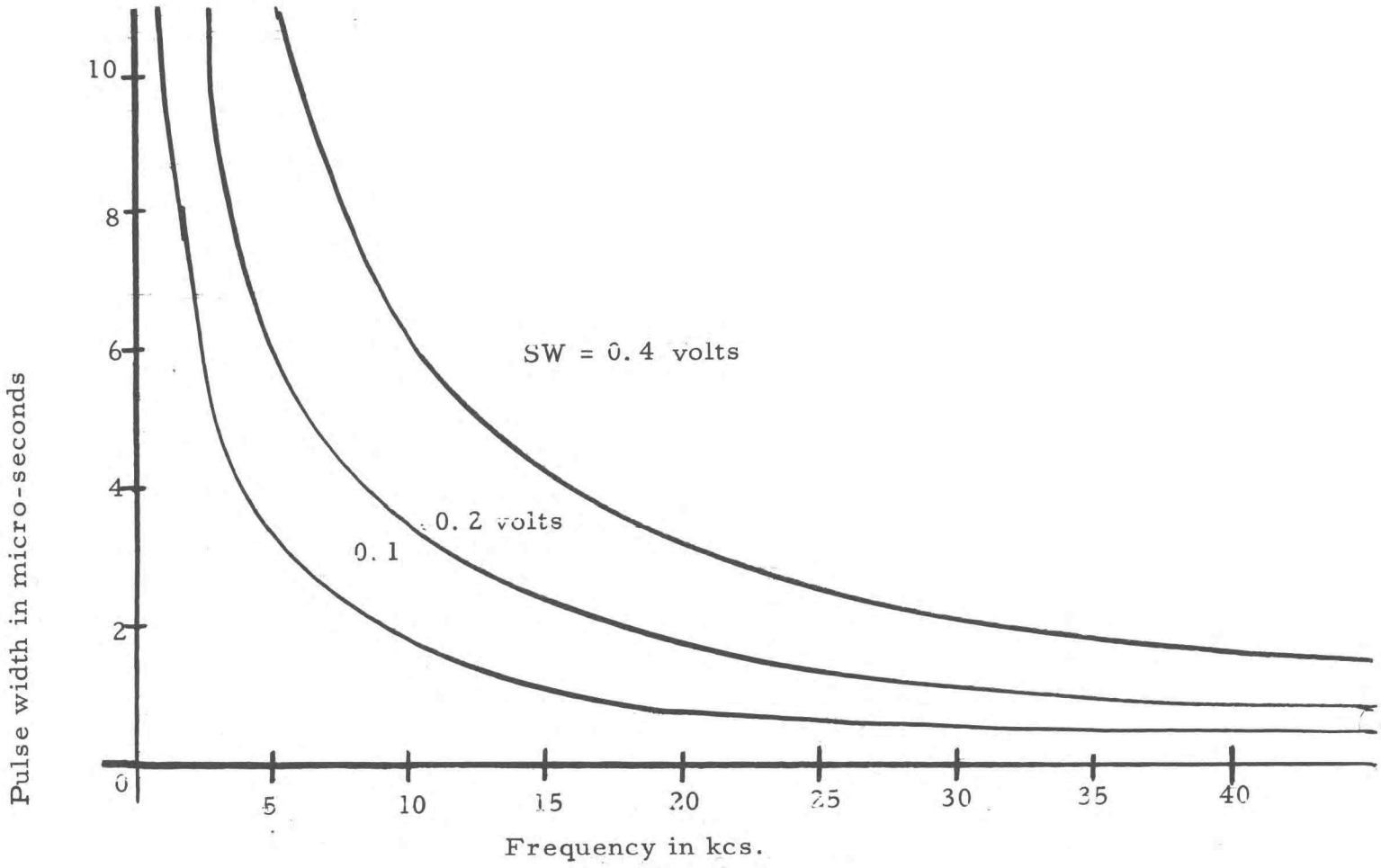


Figure 13. Plot of $t_t = \frac{SW}{Min \cdot Em}$ Where Em = 2 volts.

indicate that PDD estimates of signals extending up to at least 50 kcs. should be easily obtained by using such devices in the circuitry of the instrument.

The slit and integrator circuits are the points where pulse techniques must be applied.

## The Integrator

The function of the integrator, shown in figure 14, is to provide an output voltage, during each sampling cycle, that is proportional to the sum of the widths of all the pulses coming from the slit.

The output voltage swing, of the integrator, must be linear over its entire range. This integrator must not saturate when the input pulse width is equal to or greater than the sampling period.[1]

T10 is a PNP transistor which is connected in the emitter-follower configuration. The stage driving this emitter follower has converted the positive-going pulses coming from the slit into negative-going pulses.[2] Pulse widths and rise-fall times have been

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[1] This condition exists when the input of the instrument is connected to a voltage source that is not a function of time: eg, a DC level - or a source that appears to be time independent over one sampling period.

[2] T9 is part of the pulse-inverting circuit. This circuit may be seen on the complete schematic, page 101.

unaltered in the conversion process.

T13 is operated in the grounded-base configuration and will act as a constant current source. When the emitter voltage of T10 goes negative, T13 will start to conduct and C11 will linearly discharge. The collector voltage of T13 is ten volts immediately after the integrator-reset cycle. When the emitter of T10 goes negative, this voltage will linearly decrease toward ground. The rate of discharge is a direct function of the product of R35 and C11 as well as the output voltage of the emitter follower and T13's beta. However, all of the above factors are constant. The amount that C11 will discharge, in volts, will be:

$$\text{Amount C11 discharges} = (DR)(PW). \qquad (10)$$

where DR is equal to the discharge rate in volts per second and PW is equal to the width of the pulse, coming from the slit, in seconds.

DR will always be constant, hence the circuit will act as an integrator of pulse widths.

One problem that is common with this type of circuit is the difficulty encountered in coupling the integrator's output to additional circuitry. If the collector of T13 is connected to the relatively low input resistance of a transistor amplifier, integrator linearity will suffer. The collector of T1, therefore, is loosely coupled to the

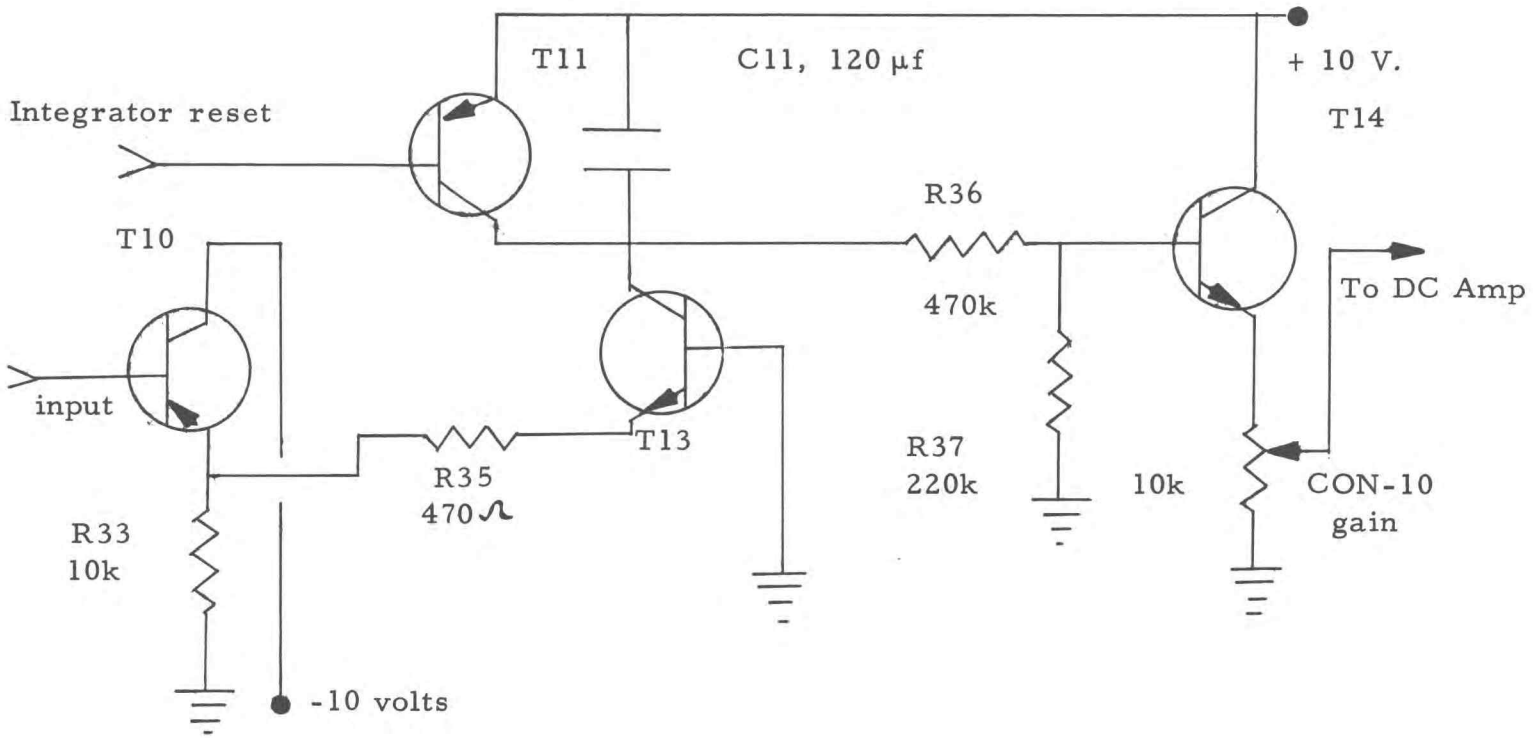


Figure 14. The integrator

base of T14 by R36, which was made as large as possible and will still be able to separate the integrator's output from the circuit noise.

C11 should have one effective discharge path and that is via T13. Unfortunately there are other extraneous paths present, and they are:

1. Through R36.
2. From the collector to the base and emitter of T11.
3. From the collector to the base and emitter of T13.
4. The internal leakage path of C11.

The above extraneous discharge paths will allow C11 to discharge when T13 is cut-off and thus contribute to instrument error. This detrimental effect may be minimized by:

1. Making R36 as large as possible. This particular step will also improve integrator linearity.
2. T11 and T13 should be good silicon transistors with low ICBO's. T13 is a WE-B silicon transistor[1] with a room temperature ICBO of 0.1 micro-amperes DC at 25 degrees centigrade. T11 has an ICBO of 0.4 micro-amperes.
3. Capacitor leakage is minimized by selecting good tantalum capacitors for C11.

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[1] See page 90 for possible replacements for the WE type transistors.

Integrator resolution may be defined as:

$$\text{Resolution} = \frac{Vs}{P} \qquad (11)$$

Vs is the integrator's total output voltage swing in volts and P is the sampling interval in seconds. For example: if P is 100 milli-seconds and Vs is 10 volts the integrator resolution will be equal to 100 volts per second.[1] Herein lies one of the major disadvantages of a system that uses this type of integrator. The integrator input will receive pulses with widths ranging from 100 milli-seconds to 100 nano-seconds. The output, then, is capable of being at any level ranging from ten micro-volts to 10 volts. The output circuitry must be able to respond linearly to voltages within this range. Unfortunately, the lower end of this voltage range will be obscured in the integrator's amplifier noise.

The size of C11 will have an effect on integrator linearity. The larger the capacitance the better the linearity. Unfortunately an increased integrating capacitance, with a constant sampling interval, will reduce the total output voltage swing. Thus, resolution suffers. One apparent solution to this dilemma is to select an integrating capacitor that will allow the collector of T13 to swing over the complete ten volt range during one sampling cycle. This

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[1] 100 volts per second is poor. An ideal case would be where the integrator resolution is $10^5$ volts-per-second.

approach was followed and was met with moderate success, as the linearity of the integrator was poor.

A 120 uf capacitor, a compromise, was finally selected for C11. This capacitor will permit a linear swing of the collector of T13 of ten to six volts during a sampling period of 100 milli-seconds.

The integrator-system output swing is from 0.5 volts to nine volts. The inversion and amplification of the signal appearing on the collector of T13 is accomplished with T15 and associated circuitry. Two potentiometers, R38 and R43, were used to manipulate the amplifier's gain and quiescent operating point while the effect of various sizes of integrating capacitors were being investigated.

Alignment procedures for the integrator will be found in part 16 of appendix IV.[1]

A procedure that may be used to see if the integrator has good dynamic input-pulse output-voltage response is given as follows:

1. Obtain a pulse generator that is capable of delivering good positive-going pulses with magnitudes of ten volts or more. The

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[1] For alignment reasons, the physical input connector to the integrator should be a banana plug combination.

pulse repetition-rate should be variable from 10 rps to at least 20 krps.

2. Adjust the generator so that the pulse "on" time is equal to the pulse "off" time.
3. Connect the generator to the input of the integrator and note the maximum output voltage of the integrator.
4. Perform this same test at different repetition rates making sure that the on and off times are equal.
5. The integrator's output voltage level should be the same regardless of the pulse repetition rate. This is not true when the repetition rate becomes less than ten times the sampling frequency.

# SYSTEM EVALUATION

How well does an estimator of probability density distributions actually estimate a distribution? How does one go about evaluating the accuracy and performance of such an instrument?

This section will attempt to answer the above questions. The following techniques will not only be an aid in evaluating the instrument described in this thesis but are applicable to any device that is designed to estimate probability density distributions.

Some of the techniques developed here appear to be new (the pseudo impulse function test) and have not been found in the literature.

## Standard Signal

Instrument performance can be evaluated by comparing a theoretical PDD with a PDD estimate. Therefore, it would be helpful to have available a standard signal from which the response of the instrument may be determined theoretically.

The sine wave, in the sense of the Fourier analysis, is basic. Its probability density function is easily calculable (6, p. 388) and fortunately sine wave generators are readily available. The probability density function of a sine wave, $e(t) = Em \sin(wt)$, where

wt = θ, is given as:

$$P\,e(t) = \frac{1}{\pi \sqrt{Em^2 + Ei^2}} \qquad (12)$$

$-Em \leq Ei \leq Em$ and $\theta$ must be uniformly distributed.

The continuous distribution of EmSin(wt) is shown in figure 15. By definition the area under the theoretical distribution will be equal to one.

Error Types

Experience has shown that there are two basic types of PDD estimate error. Figures 16 and 17 illustrate the two error types. The dashed lines outline the instrument's response (PDD estimate) and the solid line the theoretical distribution. In the ideal case the theoretical PDD and estimated PDD waveforms will completely overlap and any deviation of the actual PDD estimate from the theoretical distribution will constitute an error.

Figure 16 illustrates a type of form error. Here the shape of the PDD estimate is different from the shape of the theoretical distribution.

The area under estimate 1, in figure 17, is less than unity

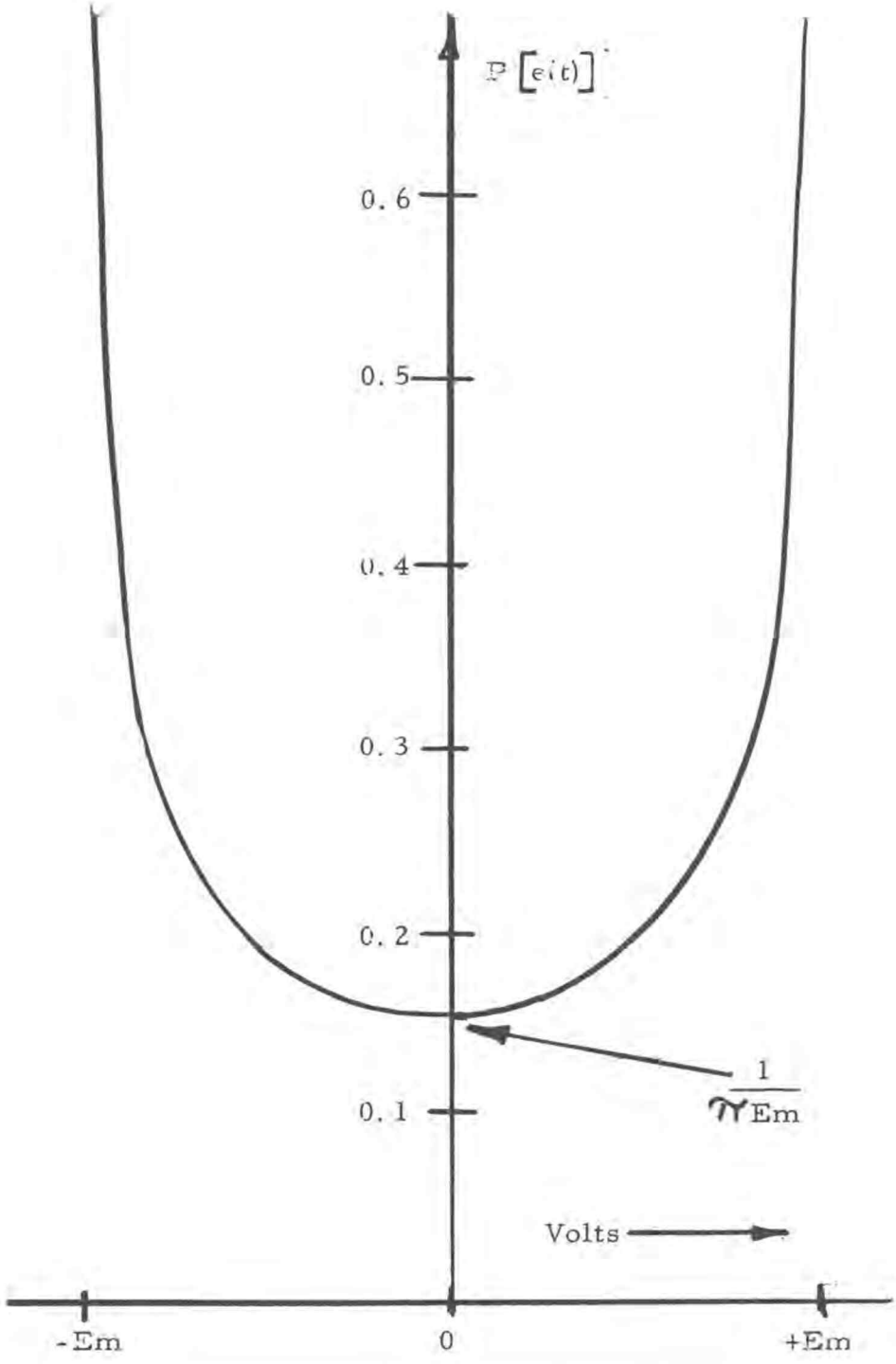


Figure 15. Theoretical distribution for e(t) = EmSinwt.

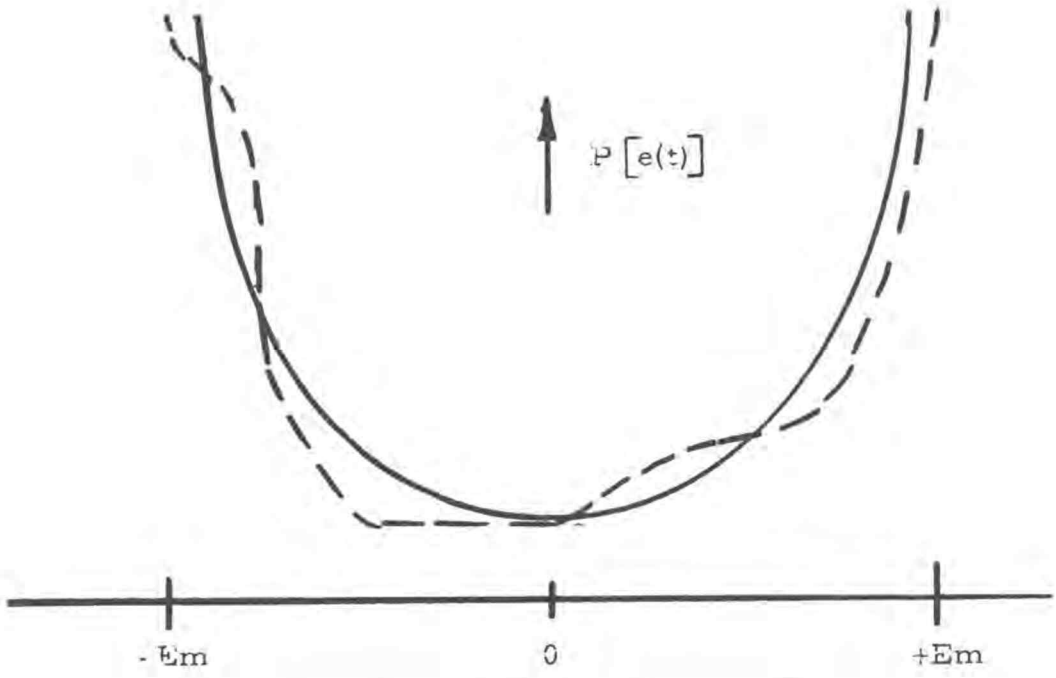


Figure 16. An example shape distortion.

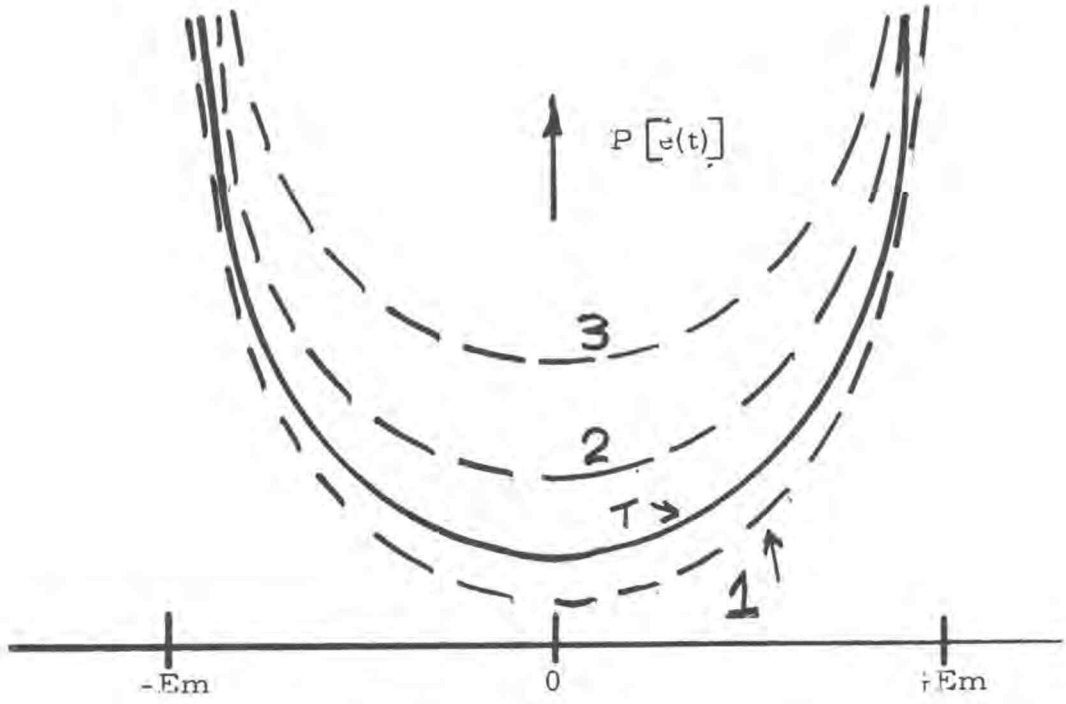


Figure 17. An example of area error.

whereas the areas under estimates 2 and 3 exceed one. Here, then, is a case of area error.[1] Form error, in this illustration, is not present as curves 1, 2, and 3 form a family of curves that differ only in their vertical positions. The curves can be shifted along the ordinate so that they all completely overlap the theoretical distribution.

Figure 18 (end-point error) illustrates a special case of area error that is prevalent in some instruments. The horizontal scale of the PDD estimate has been compressed so the area under this curve will be less than one.

## Area-Error Calculation

The area error of a PDD estimate may be obtained by comparing the area under the theoretical distribution with the area contained under the estimate. The error figure will be given in percent as:

$$\text{Area Error} = \left[\frac{\text{Area under theoretical - area under estimate}}{\text{Area under theoretical}}\right] X\ 100 \qquad (13)$$

There is good chance in practice that the scales used to plot the theoretical and estimated distributions may be different. The scales of the PDD estimate must be adjusted so that they correspond to the scales of the theoretical distribution.

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[1] There is also a good possibility that the estimate in figure 16 also has a degree of area error.

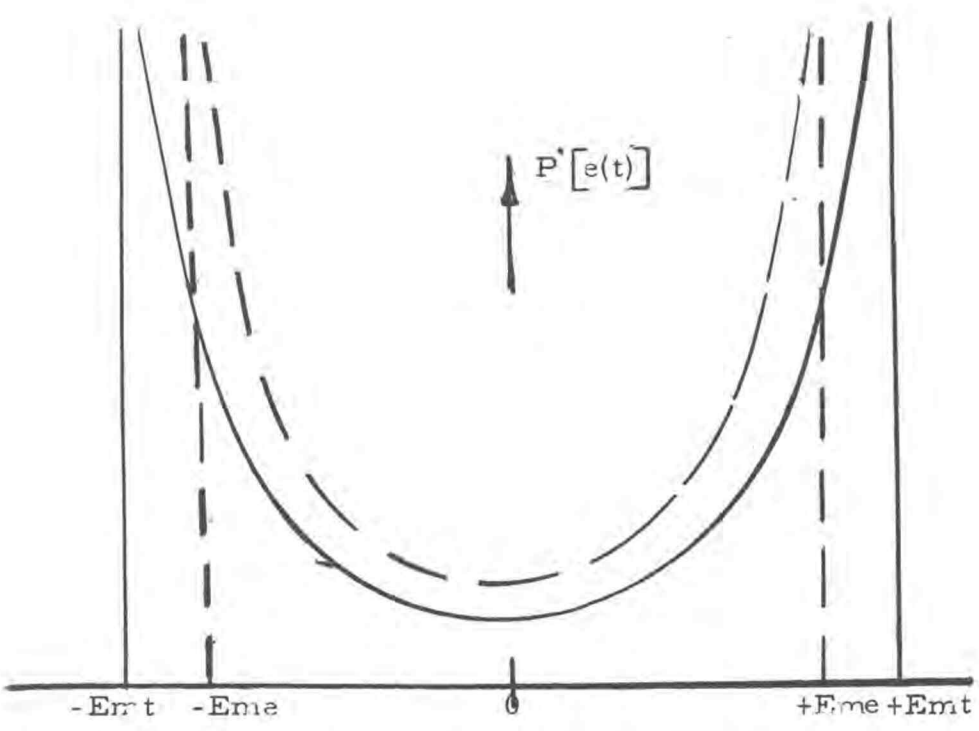


Figure 18. An illustration of end-point error.

Vertical scale correction in most cases will require the use of a scale factor. The low point of a sinusoidis theoretical distribution is equal to:

$$\text{Low Point} = \frac{1}{\pi \ \text{Em}} \tag{14}$$

The low point of the PDD estimate can be adjusted so that it will correspond to the low point of the theoretical PDD. The scale factor will be equal to:

$$\text{Scale factor} = \frac{\frac{1}{\pi \ \text{Em}}}{\text{Low point of PDD estimate}} \tag{15}$$

A glance at equation 12 will reveal that the value of $P\ [e(t)]$ will approach infinity as Ei approaches $\pm$ Em. It will therefore be impossible to compare graphically the area under the theoretical probability density distribution with the total area under the estimated distribution. As a compromise, the area error calculations will involve only the area of the theoretical and estimated PDDs that fall below a practical value of $P = [e(t)]$. The upper limit of $P\ [e(t)]$ should be as large as possible.[1]

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[1] $P\ [e(t)] = 0.4$ was found to be a reasonable starting point for sinusoidal waves.

Form Factor Calculation

Area error is meaningless when used alone. It is conceivable that the area under the estimated and theoretical PDD's will be equal whereas the shapes of the two distributions will drastically differ. What is needed is some type of form-factor measurement which will yield a figure of merit that will indicate how much the shape of the estimated PDD deviates from the shape of the theoretical distribution.

A modified mean-square-error (variance) analysis can be used to obtain a reasonable figure of merit. If we:

Let $P(A)_{Ei}$ equal the value of P [e(t)] of the estimated PDD at any Ei.

Let $P(T)_{Ei}$ equal the value of P [e(t)] of the theoretical PDD at any Ei.

Let N equal the number of Ei samples used in the computation.

The form factor will be equal to

$$\text{Form Factor} = 10^6 \sum_{Ei=-Em}^{Ei=+Em} \frac{\left(P(A)_{Ei} - P(T)_{Ei}\right)^2}{N} \qquad (16)$$

The constant, $10^6$, was incorporated into equation 2 so that the form factor will generally fall between 1 and 100. The magnitude of the form factor will be indirectly proportional to the shape deviation of the estimate. A zero form factor will indicate that a perfect match exists between the estimated and theoretical distributions.

The magnitude of the form factor for the PDD estimate shown in figure 18 is large. However the shapes of the estimated and theoretical PDDs' are almost identical. Only the dimensions of the two distributions differ.[1] Therefore equation 2 will be valid only if the dimensions of the PDD estimate are adjusted so that they correspond to the dimensions of the theoretical PDD. This adjustment may be made by equating the positive Eme and $\frac{1}{\pi \text{ Eme}}$ points of the PDD estimate to the positive Emt and $\frac{1}{\pi \text{ Emt}}$ points of the theoretical PDD.

The use of a sinusoid as a standard signal will make it necessary, as with the area-error calculations, to select all the data points needed to calculate the form factor below a particular value of $P[e(t)]$.[2]

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[1] Area error calculations will reveal errors that are due to PDD size variation.

[2] See page number 50.

A word of caution is appropriate at this point. A good PDD estimator will be able to detect slight imperfections in the test signal's waveform. Therefore, the test PDD estimate will appear to be in error if the standard sinusoidal signal is rich in harmonics. A simple RC low-pass filter must be used, in all instrument evaluations that involve the use of sinusoids, to eliminate PDD distortions that are due to harmonics.

End-Point Error Calculation

End-point error is present when the end points, ± Eme, of the PDD estimate are not equal to the end points, ± Emt, of the theoretical PDD. Figure 18 illustrates end-point error (EPE). The calculation of the percent of EPE is simple if we:

Let Emt equal the positive end point of the theoretical PDD.
Let Eme (+) equal the positive end point of the estimated distribution.
Let Eme (-) equal the negative end point of the estimated distribution.
The EPE will be:

For the positive half of the PDD estimate

$$EPE = \left[\frac{|Eme(+)| - |Emt|}{Emt}\right] X\ 100 \qquad (17)$$

For the negative half of the PDD estimate

$$EPE = \left[\frac{|Emt| - |Eme(-)|}{Emt}\right] X\ 100 \qquad (18)$$

Note that the EPE calculations must be made before the dimension adjustments (page 52) of the PDD estimate take place.

Frequency Dependence Test

Equation 1 will disclose that the probability density distribution of a sinusoid is frequency-independent. The estimate of this distribution should also display this property.

An evaluation of an instrument's frequency dependency characteristics may be obtained by comparing the PDD estimates of a number of sinusoids. The sinusoids differ only in frequency. The area error, EPE, and form factor techniques are incorporated into the procedures that are used to evaluate an instrument's frequency characteristics.

The following is a list which can serve as a guide to those who wish to determine the frequency characteristics of a PDD estimator.

1. Select a sine-wave generator that can be varied in frequency from 25 cps to 100 kcs.
2. Set the magnitude of the test signal equal to the instrument's maximum input-signal voltage rating.
3. Take PDD estimates at 100 cps, 1.0 kcs, 5.0 kcs, 100 kcs, 50.0 kcs and 100 kcs.[1] The magnitude, $Em_i$ of the test signal should be constant. Low-pass filters must be used.
4. The slit width should be set and then held constant for all the PDDs taken in step three. However, an instrument's frequency dependency characteristics may be influenced by the width of the slit. Therefore, step 3 should be repeated with several slit-width settings.
5. Select a standard signal frequency and standard instrument slit width.
6. Obtain the scale factor, (equation 15) of the PDD estimate of the signal that is on the standard frequency.
7. Correct the vertical scale dimensions of all the PDD test estimates with the scale factor obtained in step 6.
8. Calculate the area error of each sample (equation 13). These data will show the instrument's area error versus frequency

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[1] These frequencies are given only as a guide. The actual test signal frequencies will depend on the instrument under investigation.

and area error versus slit-width characteristics

9. Calculate the EPE (equation 17) of each sample.

10. Calculate the form factor of each sample. These data will show the effects of signal frequency and instrument's slit width on an estimated distribution's form factor.

The Pseudo Impulse Test

A great deal can be learned about a probability density estimator by observing how the instrument handles signals whose theoretical distributions contain impulse functions. However, no instrument can exactly duplicate an impulse function.

The theoretical probability density distribution of a constant voltage is an unit impulse with its abscissa point located at the value of the voltage's amplitude. An example of a signal (a symmetrical square wave) and its theoretical density distribution is given in figures 19 and 20.

A repeating staircase function makes an excellent and practical test signal. A signal of this type is shown in figure 21. The heights "h" of each step are equal. The widths of each step are also equal with the exception of the center step which has a width V. The width of V should be variable from zero to 10W. The theoretical density distribution of the staircase function with V equal to 2W is

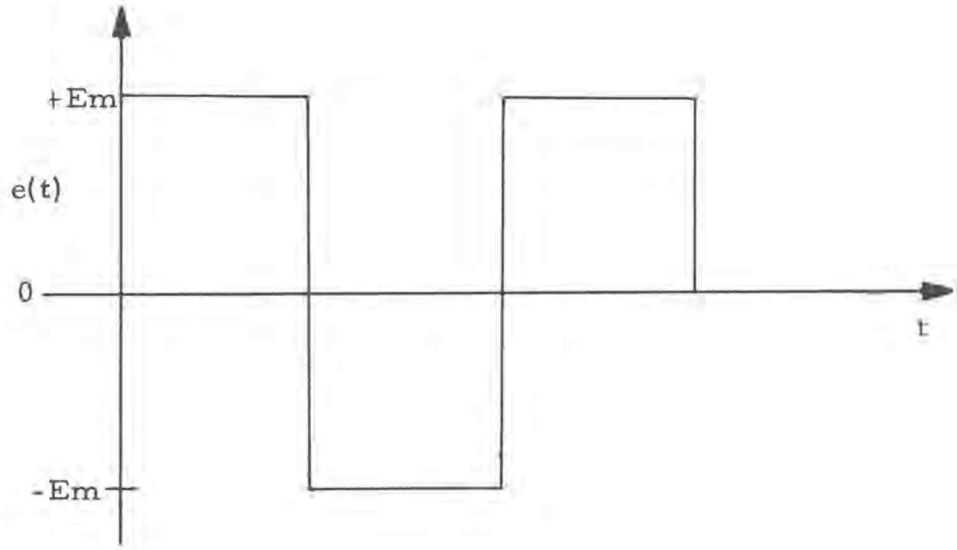


Figure 19. A symmetrical square wave.

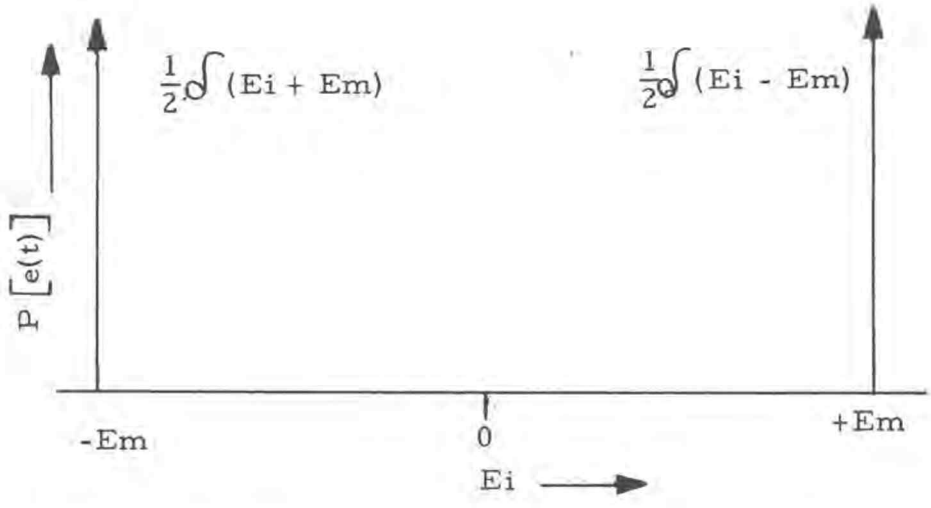


Figure 20. Theoretical PDD of the symmetrical wave.

shown in figure 22.

An instrument's estimate of the staircase function's PDD should closely resemble the theoretical distribution. However, no instrument can exactly duplicate the impulse function. There the estimated impulse magnitude will be finite (pseudo impulses) and the width of the impulses should be equal but not zero. The sum of the areas contained within the confines of the impulses, once normalized, should be equal to one.[1]

An instrument that can estimate PDD's which contain impulse functions must possess a good dynamic amplitude output response. The instrument's output must be linear over a wide voltage amplitude range. The variable step V, in figure 17, can be used to test instrument linearity. The following is a procedure that could be used to test the output linearity of a PDD estimator.

1. Connect the test signal to the input of the instrument. The test signal must be carefully designed as any variations in the signal's size or shape will be reflected in the PDD estimate.
2. Vary the pulse width, V, from zero to 10W. When V = W all the pseudo impulses should be equal in magnitude. When V = 2W,

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[1] By definition the area under any valid PDD should be unity. Therefore, the areas under all PDD estimates, once normalized, should also be equal to each other.

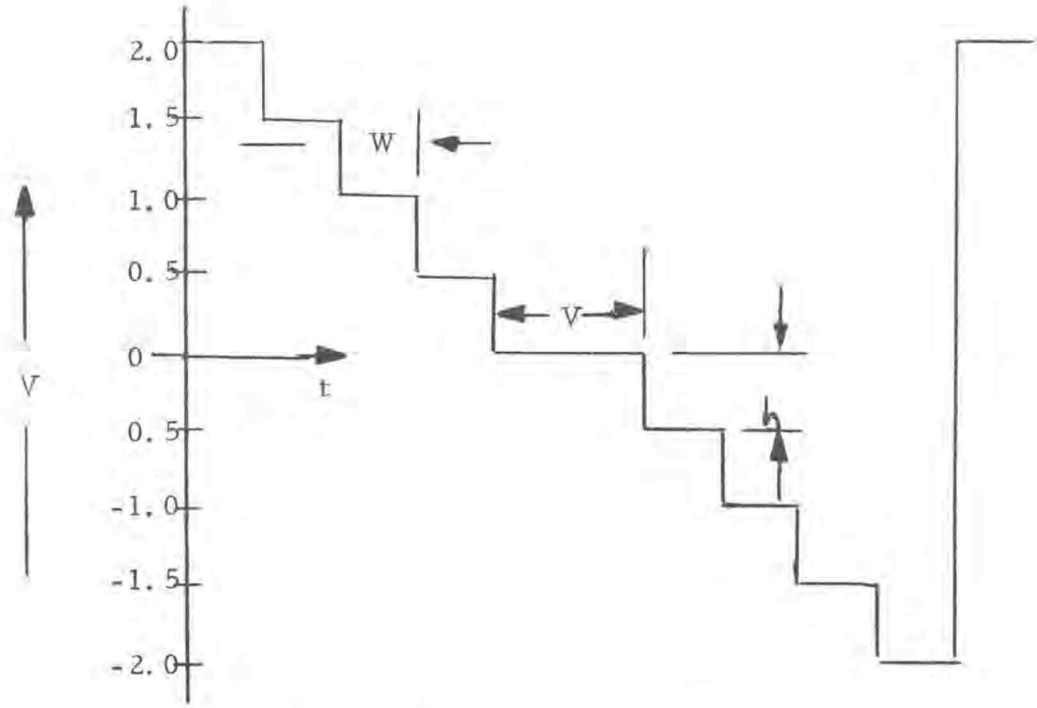


Figure 21. Staircase test signal.

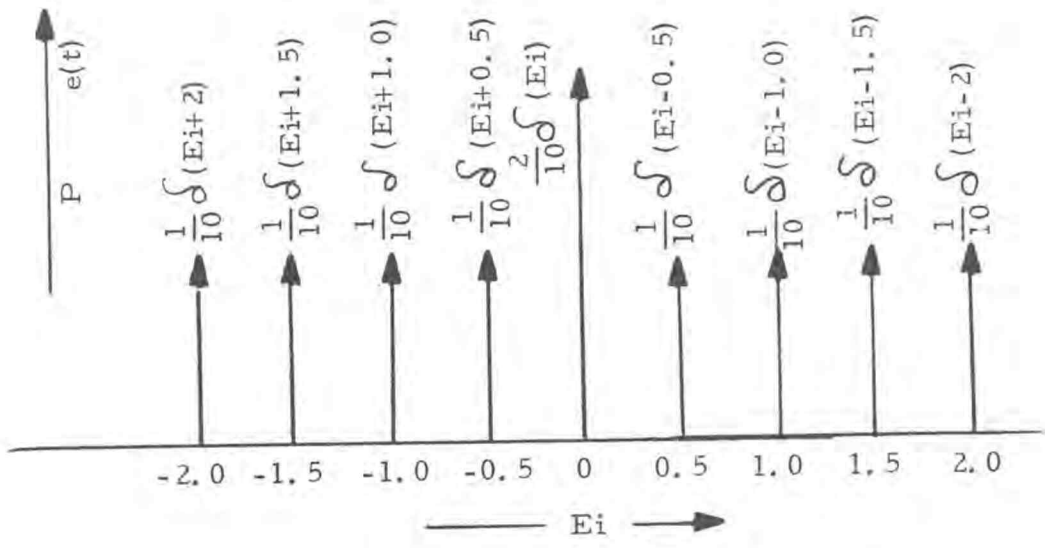


Figure 22. Theoretical PDD of the staircase function shown in Figure 17.

the center impulse should be twice high as its brothers. There will be a point between $0 \leq V \leq 10W$ that the center impulse will no longer increase linearly with V. This point will mark the system's vertical-amplitude limit.

3. Disconnect the test signal and ground the instrument's input. This step should reveal the full magnitude of the pseudo unit impulse. The region between the level determined by step 2 and the magnitude of the pseudo unit impulse will have little value, and estimates falling in this region will have little meaning.

Impulse testing will also reveal other instrument performance characteristics. For example, let us use a test signal as shown in figure 17 and set $V = 2W$.

1. The width of each impulse should be equal and will be a realistic measure of the instrument's slit width. If the widths are not equal, the slit (or slits) is (are) magnitude or rate-sensitive. Slit-width measurement is one way to tell how well an instrument can estimate PDD's. Slit-width measurements should be taken when area-error, form factor, and frequency-dependency data are being taken. If a test step function is not available, the pseudo unit impulse obtained by grounding the instrument's input will be a reasonable measure of slit-width at $e(t) = 0$. One should note, however, that a slit-width measurement is

meaningless unless the instrument's maximum input voltage limit is also given.

2. Unequal impulse magnitudes, (with the exception of the center impulse) will indicate an unstable sample timing cycle. If the magnitude of the center impulse is not twice the magnitude of any of the other impulses, the instrument has poor vertical linearity.
3. Unequal impulse spacing will indicate non-linearity in the instrument's signal amplifiers. In some instruments there is a possibility that the sweep or scan linearity may have an effect on the impulse spacing.

There is a point to remember when using a step function type test signal. The sampling period must be much longer than the period of the step function. A good rule of thumb to follow is to adjust the step function's period to be equal to one milli-second when $V = 10W$.

The frequency response of the instrument may be limited so the step function may be distorted in the instrument's internal circuitry, but sinusoid frequency dependency tests will reveal this fault.

A good PDD will certainly point out any errors that are present in the step function's construction, and so for this to be a valid

test, good wave forms must be generated or means must be available to record the test signal's wave shape.

## A Brief Summary of Instrument Evaluation Techniques

Area Error The percentage of area error is determined by comparing the area under the estimated distribution with the area under its theoretical distribution. Area error data has the greatest meaning when it is given with the form factor, EPE, SW, and the test signal's magnitude, Em.

Form Factor This technique gives a relative measure of the deviation of the shape of a PDD estimate away from the shape of its theoretical distribution.

End Point Error EPE is a special case of area error. The percentage of EPE will tell how far the end points of the estimated distribution deviate from the end points of its theoretical distribution.

Frequency Dependency test This test will reveal how the area error, form factor, and EPE are effected by the frequency of the signal under investigation.

Pseudo Impulse test The pseudo-impulse test involves the use of a test signal whose theoretical PDD contains impulse functions. This

is a rigorous test which will reveal much about the capabilities of an instrument. The pseudo impulse test can be used as a supplement to the above techniques and, if properly performed, will reveal the possible causes of area error, poor form factor and EPE. Therefore an instrument's evaluation is complete only when the results of a pseudo impulse test are given.

In General

The calculation and measurement techniques of form factor, area error, EPE, and frequency dependency are tedious to perform. However, sine wave generators are readily available.

The pseudo impulse test is simple to perform and requires few calculations. Unfortunately, the test signal's generator is difficult to build.

For an evaluation to be complete all the test results should include information such as slit width and the maximum voltage amplitude of the test signal.

# RESULTS

## Complete Operating Characteristics

The following is a tabulation of the probability density distribution estimator's operating characteristics:

### Interrogation Timing Cycle

| | |
|---|---|
| Sample | 100 milli-seconds |
| Record | 3 milli-seconds |
| Integrator Reset | 30 milli-seconds |

### Sweep-Scan Rate

| | |
|---|---|
| Variable from | 5 to 100 seconds |

### Slit Width

| | |
|---|---|
| Variable from | 0.05 to 0.06 volts |

### Area Error

| | |
|---|---|
| Slit width | 0.2 volts |
| Signal frequency | 1.0 kcs |
| Area error | 1.2% |
| EPE | Too small to be measured |

Frequency Dependency Data

Slit width 0.2 volts

Standard frequency 1.0 kcs.

| Frequency | Area Error | Form Factor |
|---|---|---|
| 10 cps | -5.5%* | -- |
| 100 cps | -3.3% | 17.8 |
| 1.0 kcs | 1.2% | 24.3 |
| 10.0 kcs | 4.7% | 11.5 |
| 20.0 kcs | 13.2% | 37.2 |
| 50.0 kcs | 25 %* | -- |

*Estimate

Maximum input voltage

Em 3.0 volts

Power Requirements

± 10 volts at 500 ma.

Frequency Dependency Measurements

The frequency dependency data were taken from the photographs shown in figures 23 through 29. The technique of measurement is

simple but effective. Each photograph was projected, by an opaque-optical projector, on a solid white screen. Measurements are taken directly off the screen. Projection errors were corrected by using a sheet of K and E type 358-14 (10x10) graph paper as a standard.

The distribution of the 10 cycle wave, figure 23, illustrates the multiple trace problem which is encountered when the period of the signal that is being measured approaches the sampling period. This photo was also used to estimate the 10 cps area error that is given in the above tabulation.

The distribution of the 100 kcs sine wave, figure 30 illustrates the case where the form factor and area error are extreme. Note, however, that the end points, the discontinuities at two volts, still compare favorably with the kcs. (Low EPE) standard estimate shown in figure 25.

Other Comments

Figure 31 contains photograph of random but supposedly gaussian distributed noise PDD estimates. The effect of the envelope switch CON-10 may also be noted. The band width of the interrogated noise spectrum was limited to 20 kcs. Note the slight negative skew. The skew becomes more pronounced as the noise band width is increased The author is not certain if the skew increase

is due to instrument distortion, noise amplitude skew or both. The author intuitively feels that the latter reason is probably the correct one.

Figure 33 shows the method employed in rectifying the random noise whose distribution is shown in figure 34. Note that the distribution of the rectified noise is shifted toward the left (more negative) whereas theory would predict that the positive-half of the rectified PDD should overlap the positive-half of the non-rectified one. This error is due to the use of an input capacitor at EF-1. This one photograph points out the need of complete direct coupling within the instrument's circuitry. Therefore, considerations other than frequency response determine the type of circuit coupling needed for proper instrument operation.

Figure 36 is the PDD estimate of the staircase test signal shown in figure 35. Compare this PDD with the theoretical one shown in figure 22.[1] They are quite alike. The pseudo impulse widths are about equal, indicating good slit-width linearity. The center impulse is about twice as high as any of the other impulses. The impulses oneither side of zero have almost equal heights. A glance at the photograph of the test signal will reveal the cause of

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[1] See page 59.

the slight height differences. The widths of each step are not exactly equal. This is indication that a good test signal source or a method of recording the test signal's wave form must be available during instrument evaluation.

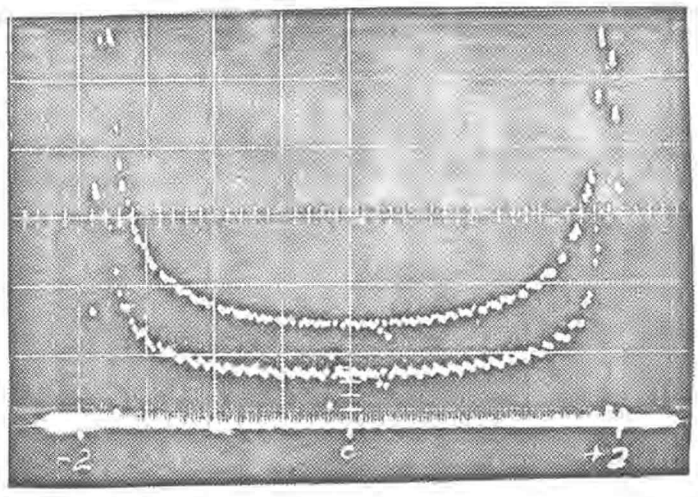


Figure 23. PDD estimate of e(t) = 2Sin wt at a frequency of 10 cycles. Ordinate 0. 2 volts per large division. Abscissa 0. 5 volts per large division SW is 0. 2 volts. Display time is 20 seconds.

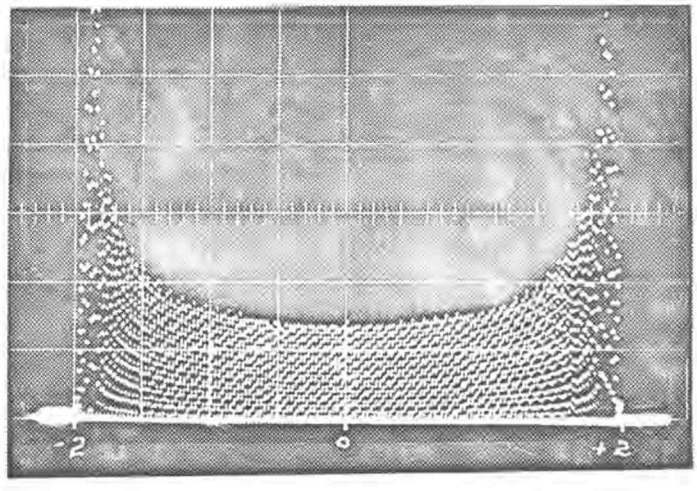


Figure 24. PDD estimate of e(t) = sin wt at a frequency of 100 cycles. Ordinate 0. 2 volts per large division. Abscissa 0. 5 volts per large division. SW is 0. 2 volts. Display time 20 seconds.

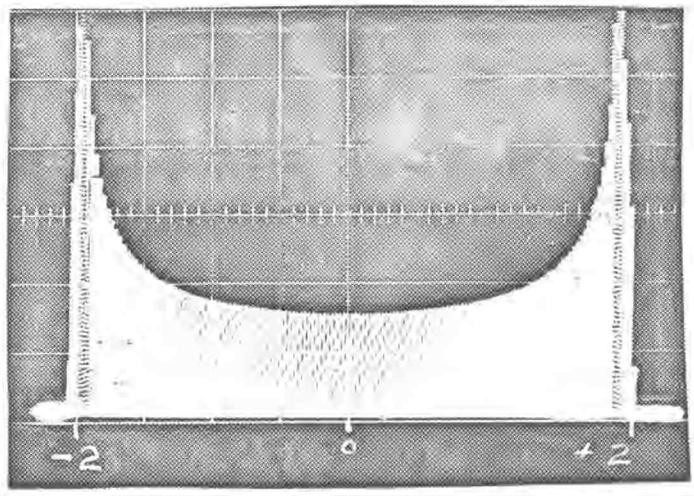


Figure 25. PDD estimate of e(t) 2-Sin wt at a frequency of 1 kcs. Envelope switch, CON-10, is off. Ordinate 0.2 volts per large division. Abscissa 0.5 volts per large division. SW is 0.2 volts. Display time is 20 seconds.

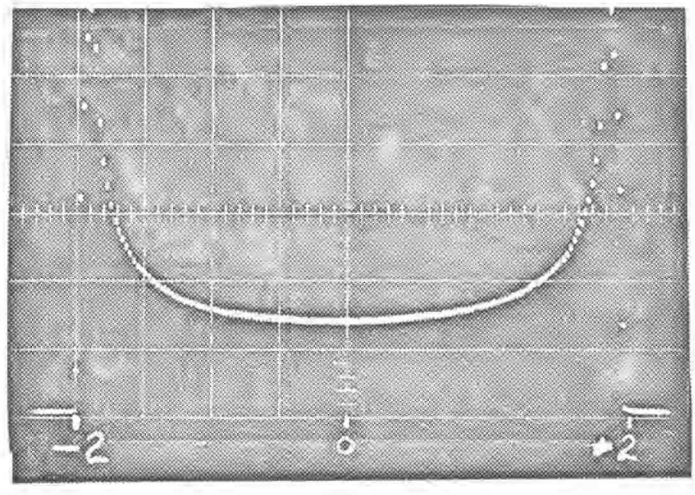


Figure 26. PDD estimate of e(t) = 2Sin wt at a frequency of 1 kcs. Envelope switch, CON-10, is on. Ordinate 0.2 volts per large division. Abscissa 0.5 volts per large division. SW is 0.2 volts. Display time is 20 seconds.

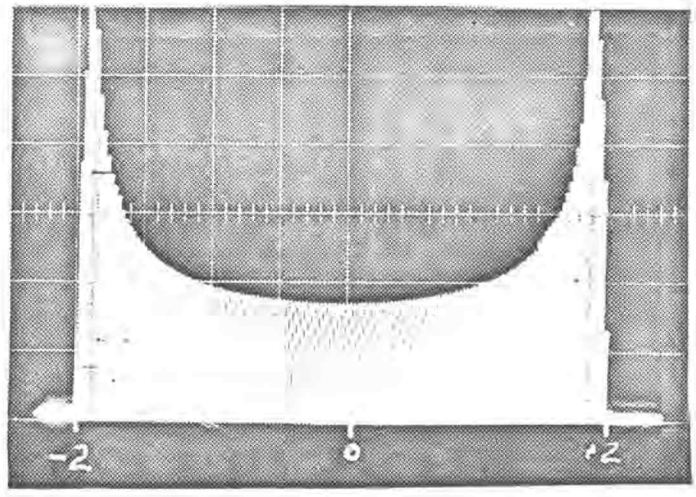


Figure 27. PDD estimate of e(t) = 2Sin wt at a frequency of 10 kcs. Ordinate 0.2 volts per large division. Abscissa 0.5 volts per large division. SW is 0.2 volts. Display time is 20 seconds.

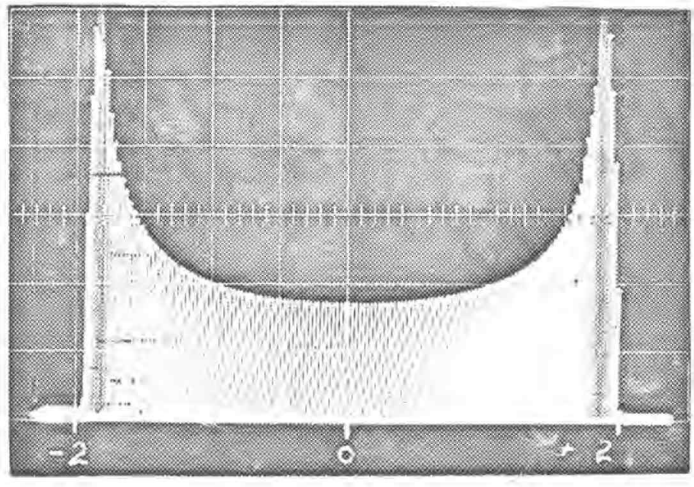


Figure 28. PDD estimate of e(t) = 2 Sin wt at a frequency of 20 kcs. Ordinate 0.2 volts per large division. Abscissa, 0.5 volts per large division. SW is 0.2 volts. Display time is 20 seconds.

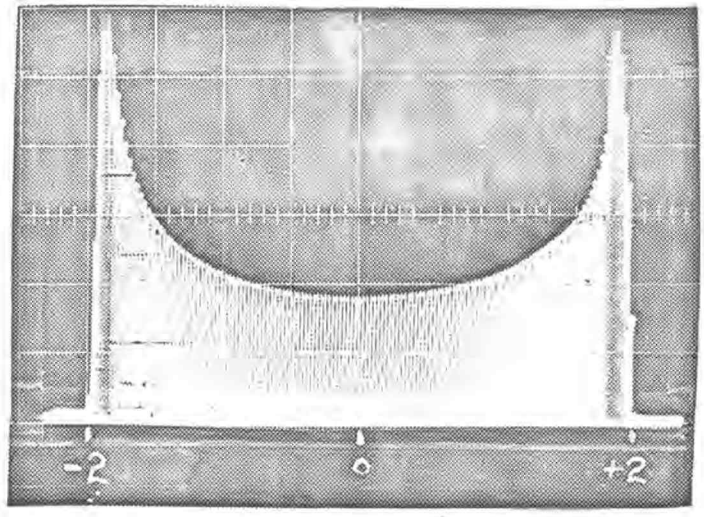


Figure 29. PDD estimate of e(t) = 2Sin(wt) at a frequency of 50 kcs. Ordinate 0.2 volts per large division. Abscissa 0.5 volts per large division. SW is 0.2 volts. Display time is 20 seconds.

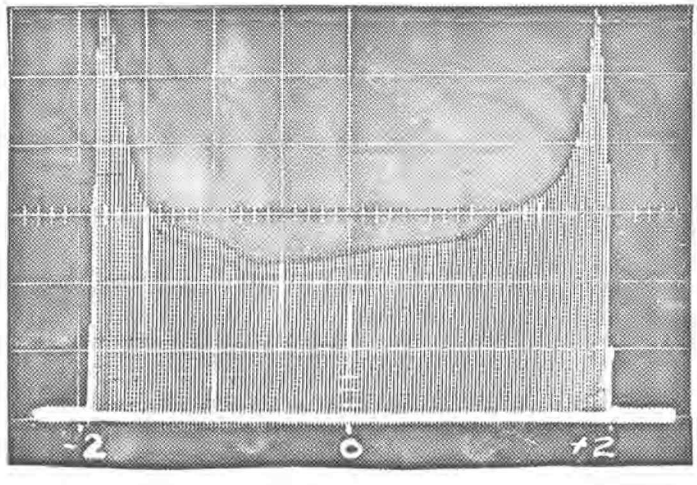


Figure 30. PDD estimate of e(t) = 2Sin(wt) at a frequency of 100 kcs. Ordinate 0.2 volts per large division. Abscissa 0.5 volts per large division. SW is 0.2 volts. Display time is 20 seconds.

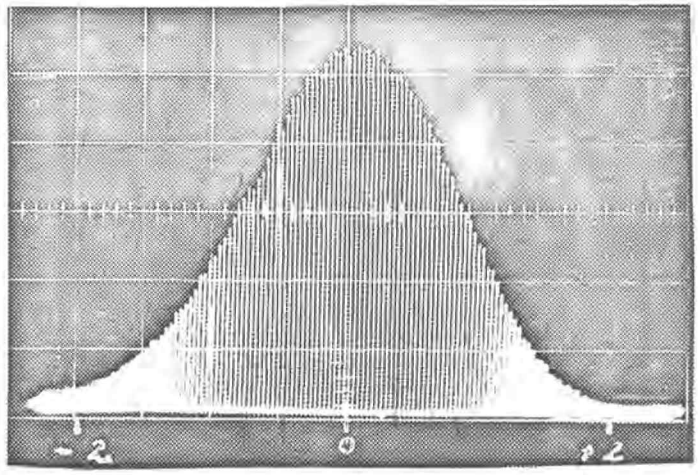


Figure 31. PDD estimate of random e(t). Envelope switch, CON-10, off.

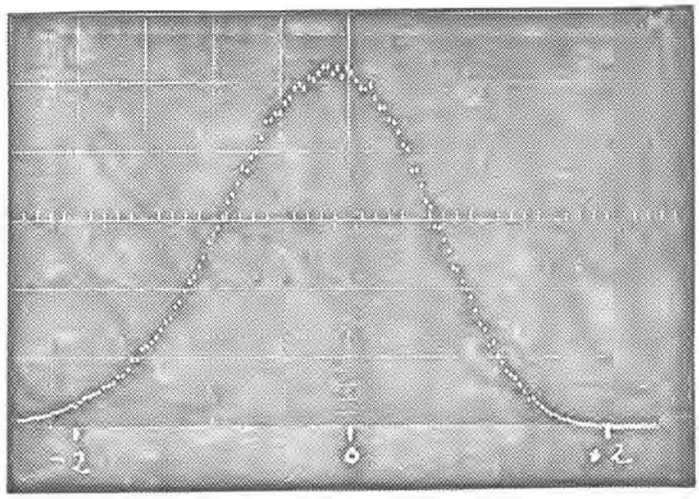


Figure 32. PDD estimate of random e(t). Envelope switch, CON-10, on.

The random signal, e(t), was obtained from a GR type 1390-B noise generator with an upper frequency limit of 20 kcs. The ordinate for both figures is calibrated at 0. 2 volts per large division. The Abscissa 0. 5 volts per large division. The SW is 0. 2 volts. Display time is 20 seconds.

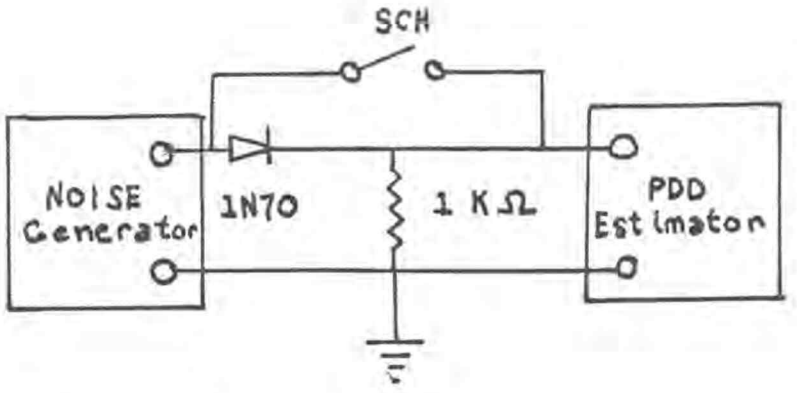


Figure 33. Method of rectifying random noise.

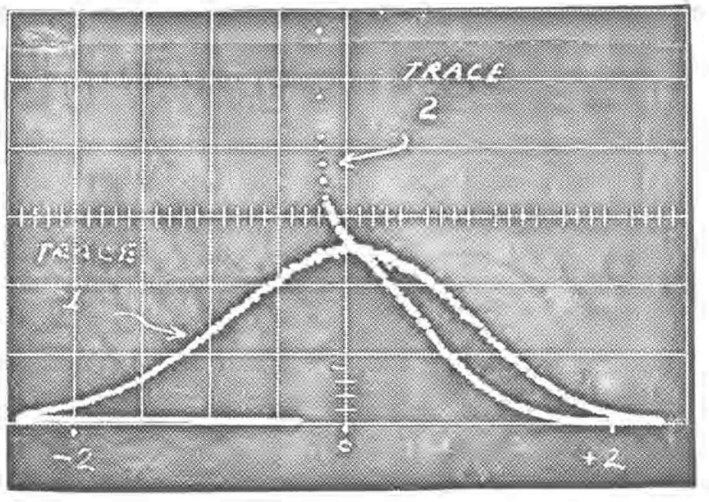


Figure 34. PDD estimates of random noise. Ordinate 0.5 volts per large division. Abscissa 0.2 volts per large division. SW is 0.2 volts. Display time 60 seconds.

Trace 1. SCH closed.
Trace 2. SCH open.

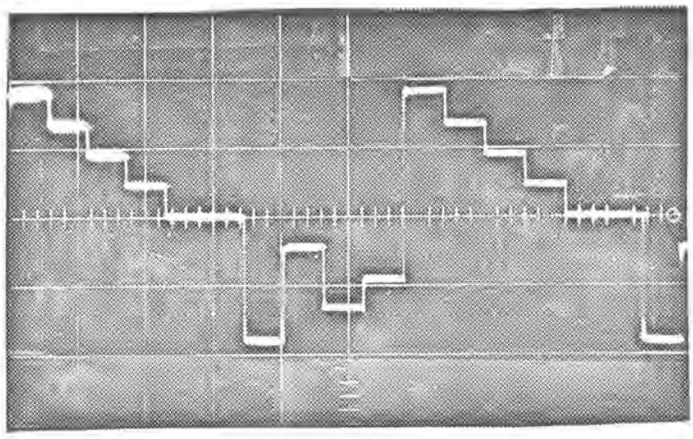

Figure 35. Photo of staircase test signal. Ordinate 1 volt per large division. Abscissa 50 micro-seconds per large division.

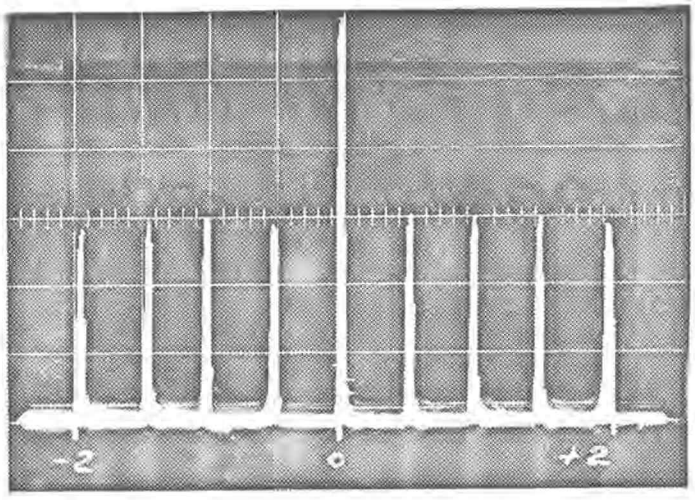


Figure 36. PDD estimate of the staircase test signal shown in figure 36. Ordinate 0.5 volts per large division. Abscissa is 0.5 volts per large division. Display time is 90 seconds.

# IN RETROSPECT

If the writer were able to go back in time and start this project anew with the knowledge he has acquired, what would he do differently--what changes would be made? This brief section will attempt to answer this question.

The first thing the author would do is to investigate the possibility of increasing the supply voltages. A different complement of transistors would have to be selected. The following is a list of possible improvements that would come about if the supply voltages were increased.

1. There would be a greater integrator output-voltage swing, thus giving the device better vertical resolution.
2. The DC amplifier that drives the slit would be moved before the resistance adder thus eliminating the problem of over-load recovery.
3. Simplified sweep-scan circuitry would be used.

The following is a list of circuit logic changes that will simplify the instrument's construction without appreciably degrading performance.

1. The logic that is used to perform the coordinating functions that

are described on page 25 may be eliminated if one is willing to accept a large error on the first and last interrogation cycle of each sweep-scan period. The conversion is simple and will eliminate EF-7, OR-2, AND-5, AND-4, and PIA-2. This change will eliminate seven inexpensive diodes and two inexpensive transistors. Once the above logic block has been eliminated, connect the output of M-4 to the input of M-2. The reset generator, M-1, will be directly connected to EF-5. This change will make the sweep-scan and interrogation cycles independent of each other. The system start-reset switch, CON-11, must be connected into the interrogation timing loop.

2. PIA-2 may be eliminated by connecting the output of EF-5 to the input of the Schmitt trigger, ST-1. This particular change in logic will have no effect on instrument performance.

3. There is a possibility that the sweep-scan circuitry can be simplified if there has been a supply voltage increase. This change will inject the same type of error that is mentioned in step 1. The Miller sweep circuit may be replaced by some type of simple relaxation oscillator that has a self-reset characteristic. This is true because poor sweep linearity does not affect instrument accuracy. This change would eliminate ST-1, M-1, EF-5 and the sweep retrace clamp would be eliminated.

If all the above logic changes were made the component reduction would be: 11 transistors and seven diodes. Therefore, such changes are worth considering. Please note that changes 1 and 2 can be made without supply voltage change and would result in a savings of: seven diodes and three transistors.

Figure 34 illustrates the need for all the instrument's circuitry to be direct-coupled.

The sweep-scan timing is quite slow. Therefore, it is difficult to see a complete PDD estimate on the face of the display CRO. It would be advisable to have available outputs that are capable of driving an X-Y recorder.

# CONCLUSION

An estimator of probability density distributions has been designed, constructed, and evaluated.

Results are good. The instrument is capable of estimating the PDDs of signals with band widths that range from 100 cps to ten kcs with low form factors and less than five percent frequency area error. About a ten percent frequency-area error was achieved with signals with band widths ranging from 100 cps to 20 kcs. The form factor and end point error in this range were also low.

The instrument's logic is sound and the overall design, although not polished for production, can serve as a solid basis for further development.

This writer is confident that, with improved circuitry, the frequency-area error of PDD's of signals with band widths that range from a fraction of a cycle to 50 kcs. can be achieved to about the five percent level with low form factors.

The output horizontal sweep is too slow for convenient waveform observation on the display CRO. Photographs of the waveform display are difficult to obtain and evaluate. Therefore, circuitry to drive a x-y recorder should be included in any further instrument design effort. The outputs for the display CRO should be retained,

however.

The author attempted to improve the techniques that are used in evaluating the performance of PDD estimators The technique of using a test signal whose theoretical PDD's involve impulse functions was introduced and demonstrated with success. Much can be learned about the character of a particular PDD estimator by using such test signals.

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# APPENDICES

# APPENDIX I

## DISCUSSION OF CONVENTIONAL CIRCUITRY

A discussion concerning the conventional circuitry used in the probability density estimator follows. This discussion will follow the complete schematic diagram of the system that is given in appendix VI, page 101.

### Input Circuitry

EF-1 is a capacitive coupled emitter follower which consists of T1 and associated components. The quiescent operating point of this amplifier is adjusted so that the voltage across R3 is about 5 volts with no signal input. C2, a mica capacitor, is shunted across the electrolytic C1 to reduce circuit ringing. The optimum value of C2 depends on the construction of C1, so it would be advisable to check this particular configuration by connecting the input of the instrument to a pulse source that is capable of delivering 3 volt peak-to-peak pulses at a repetition rate of 100 kcs. The value of C2 is then adjusted for a minimum of ring.

### Resistance Signal-Sweep Adder

The resistance adder circuit consists of the resistances: R4,

R5, R7 and R8 and the centering control, CON-1. The resistor values are kept low (4.7k) to reduce the effects of distributed circuit capacitance.

DC Amplifier

This is a two-transistor (T2 and T3) diode-coupled (D1) feedback amplifier. T2 is directly driven from the resistance adder through R9. The external negative feedback loop is controlled by R100. Feedback is necessary for the following reasons:

1. Improves operating-point stability.
2. Tends to reduce the effects of component value drift. Thus, the amplifier's voltage amplification is constant.
3. For this particular application, the most important reason of all is that feedback reduces the effect of beta fall-off at high current levels.[1]

The closed-loop voltage gain, measured from the input of the amplifier to the emitter of T4, is 45. The voltage application of the system, measured from the input of the instrument to the output of EF-2 (the emitter of T4), is 10. The amplifier, therefore,

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[1] This effect was quite pronounced when the amplifier was operating with an open feedback loop. Negative feedback reduced this distortion to the point where it was barely perceptible.

compensates for the signal loss in the Kirchhoff adder as well as furnishing the additional gain required to reduce the slit-width (see page 47). The frequency response of this configuration is flat from 10 cps. to 100 kcs. The preceding characteristics were obtained with the amplifier operating entirely in its linear region.

The ability of the amplifier to recover from overload[1] conditions is excellent at frequencies up to ten kcs. The recovery characteristics deteriorate at frequencies above ten kcs. Overload recovery is highly dependent on the type of transistor used. Transistors that would normally be used in audio-amplifier circuits produce extremely poor overload characteristics. The WE-G transistor was found to work satisfactorily in this circuit. The WE-G has an alpha cut-off of 230 mcs. R10 and R14 were adjusted to give the best overload recovery characteristics with the WE-G transistor. Their values are not critical, however.

Vertical Output Circuitry

AND-3 is a conventional gate with R44 selected so that loading effects on the integrator's circuitry are minimized. Laboratory

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[1] Amplifier over-load is the condition that exists when the input signal's magnitude is such that the amplifier is forced to operate in its non-linear region. In the extreme case of overload, the amplifier's transistors will be either in a cut-off or saturated condition.

tests reveal that this gate has good linearity. EF-4, with T16, is directly driven by AND-3 and is the vertical output amplifier of the instrument. R46, a 10k ohm resistor is inserted between the vertical output terminal and the emitter of T16. This resistor is one attempt to "idiot-proof" the instrument. If R46 were omitted and the instrument operator accidentally grounded the vertical output terminal, there would be an excellent chance that T16 would be permanently damaged.[1]

Control Unit

The Miller sweep circuit is conventional. The design of such circuits are found in the literature.

The sweep-scan rate can be varied from 5 to 100 seconds by CON-3. Sweep-scan linearity is poor at high sweep-scan rates. Fortunately, poor sweep-scan linearity does not effect the exactness of the PDD estimate. Poor linearity means that the input signal, e(t), will be interrogated unevenly. Uneven serial

---

[1] The instrument designer must attempt to foresee operator error and design his equipment so as to prevent internal damage from such errors. In the past, good equipment has received a poor reputation because the equipment was unable to withstand extreme voltage or current overloads that were the result of poor judgment on the part of the operator.

interrogation will not effect the value of the probability analog obtained at each level. If the sweep-scan rate is much less than the sampling period (which is always the case) the harmless effects of non-linearity will not be noticed.

EF-5 with T19 is conventional.

The inverting amplifier, with T20, again uses conventional design techniques. R50, the sweep-balance control (CON-9) is used in the process of aligning the sweep circuitry.

The horizontal output amplifier (EF-6) with T21, is identical to the vertical output amplifier EF-4.

The design of the Schmitt trigger (ST-11) followed the ideas outlined by Corsiglia. (3). CON-4 controls the threshold level of ST-1.

The mono-stable multivibrators M-1, M-2, M-3, and M-4, with the exception of the timing capacitor, are exactly alike. The design is conventional and the techniques that are employed are outlined by Strauss (8).

A word of caution, if the reader intends to experiment with the timing of the interrogation cycle: Mono-stable multivibrators have recovery times that are approximately equal to three times the product of the timing capacitor and the collector resistor of the normally cut-off transistor. For example, in M-2, the sampling

generator, the timing capacitor (C20) is 8 uf. and the collector resistance, R67, has a value of 1k ohms. The recovery time of M-2 will be equal to about 24 milli-seconds. For a reliable timing operation, the sum of the record and integrator reset cycles should never be less than 24 milli-seconds.

# APPENDIX II

The following is a table which will correlate transistor number and type to the logical block in which it is contained.

| LOGIC | DEVICE NUMBER | DEVICE TYPE |
|---|---|---|
| EF-1 | T1 | WE-B |
| DC-AMP | T2 | WE-G |
| | T3 | WE-G |
| | D1 | WE-AB |
| EF-2 | T4 | WE-G |
| AND-1 | D2 | WE-AB |
| | D3 | WE-AB |
| PIA-1 | T5 | WE-B |
| PA-1 | T6 | WE-B |
| | T7 | WE-B |
| AND-2 | D4 | WE-AB |
| | D5 | WE-AB |
| EF-3 | T8 | WE-B |
| INTEGRATOR | T9 | WE-A* |
| | T10 | WE-A** |
| | T13 | WE-B |
| | T14 | 2N1566 |
| | T15 | 2N1566 |
| INT-RESET | T11 | WE-A* |
| | T12 | 2N1305* |

(Continued)

| LOGIC | DEVICE NUMBER | DEVICE TYPE |
|---|---|---|
| AND-3 | D6 | 1N70 |
| | D7 | 1N70 |
| EF-4 | T16 | 2N1566 |
| MILLER-SWEEP | T17 | IBM-075 |
| Miller-SWEEP RESET | T18 | 2N1304 |
| EF-5 | T19 | IBM 075 |
| DC-INV-AMP | T20 | IBM 075 |
| SWEEP-RETRACE CLAMP | T22 | IBM 075 |
| EF-6 | T21 | IBM 075 |
| ST-1 | T23 | IBM 075 |
| | T24 | IBM 075 |
| PIA-2 | T25 | IBM 075 |
| M-1 | T33 | IBM 075 |
| | T34 | IBM 075 |
| AND-4 | D12 | 1N70 |
| | D13 | 1N70 |
| | D14 | 1N70 |
| EF-7 | T32 | 2N1304 |
| OR-1 | D8 | 1N70 |
| | D9 | 1N70 |
| M-2 | T26 | IBM 075 |
| | T27 | IBM 075 |

(Continued)

| LOGIC | DEVICE NUMBER | DEVICE TYPE |
|---|---|---|
| M-3 | T28 | IBM 075 |
| M-4 | T30 | IBM 075 |
| | T31 | IBM 075 |
| EF-8 | T36 | 2N1304 |
| OR-2 | D10 | 1N70 |
| | D11 | 1N70 |
| AND-5 | D15 | 1N70 |
| | D16 | 1N70 |

All transistor types are NPN except when noted by *. The WE type transistors are educational gifts given to Oregon State University by Western Electric Company. The IBM transistors are educational gifts given to Oregon State University by International Business Machines, Inc.

The IBM 075 may be replaced by the 2N1304

WE-B by 2N706

WE-A by 2N705

# APPENDIX III

## A TABULATION OF CONTROL TYPE AND LOCATION

The first column is the control number; the second, the control function, and the third, the recommended control location. The fourth, the control resistance in ohms. The control location column is included to serve as an aid to those who desire to duplicate, or improve on, the instrument. E is the designation for front panel (external) mounting. I for internal mounting.

| | | | |
|---|---|---|---|
| CON-1 | Sweep-Centering | I | 5 k |
| CON-2 | Slit-Width | E | 500 ohms |
| CON-3 | Sweep-scan rate | E | 500 k |
| CON-4 | ST-1 Threshold level | I | 10 k |
| CON-5 | Sweep-Scan reset timing | I | 25 k |
| CON-6 | Sample timing | I | 25 k |
| CON-7 | Record timing | I | 25 k |
| CON-8 | Integrator-reset timing | I | 25 k |
| CON-9 | Manual sweep | E | 25 k |
| CON-10 | Envelope switch | E | Not applicable |
| CON-11 | System start-reset switch. (push button) | E | Not applicable |
| CON-12 | Integrator gain | I | 10 k |

| | | | |
|---|---|---|---|
| CON-13 | Integrator bias | I | 250 k |
| CON-14 | Manual-Auto sweep switch | E | Not applicable |
| CON-15 | Sweep balance | I | 100 k |

# APPENDIX IV

The following is the complete alignment procedure for the PDD estimator: (It is assumed that all circuitry is functioning properly. This is not a trouble shooting guide).

## Test Equipment

1. A good DC oscilloscope, such as the Tektronix 535, 585 etc. This will be called the test CRO.
2. A good probe for the test CRO.
3. An audio signal generator that can give a 10 to 15 kcs. sine wave with a peak magnitude of three volts.

## Alignment Procedure

1. Set the following controls to:
   a. The manual-auto-sweep switch (CON-14) to auto.
   b. ST-1 threshold control (CON-4) to maximum.
   c. Manual sweep-scan control (CON-9) to mid-scale.
   d. Sweep-scan reset (CON-5) to maximum.
   e. Sample timing (CON-6) to maximum.
   f. Record timing (CON-7) to maximum.
   g. Integrator-reset timing (CON-8) to maximum.
   h. Sweep-scan rate (CON-3) to minimum (fastest sweep).

i. Envelope switch (CON-10) to envelope. Switch is turned off.

2. Connect the vertical input of the display CRO to the vertical output of the instrument.
3. Connect the horizontal input of the display CRO to the horizontal output of the instrument.
4. Place a three volt (peak) sinewave on the input of the instrument. The frequency of the input signal should be between 10 and 15 kcs.
5. Place the probe of the test CRO on the emitter of T19. This point should be at zero volts.
6. Press the system-start-reset button (CON-11) and observe the following waveform: The emitter voltage of T19 should go slowly from zero to about plus ten volts, remain there for awhile, then linearly decrease back to zero again. This process will repeat everytime the push button is pushed.
7. Place the probe of the test CRO on the emitter of T21. There should be plus-ten volts at this point. If not adjust, the sweep balance control, CON-15, so there is.
8. Press the start button, CON-11. The voltage should rapidly decrease from ten volts to about zero volts, remain there for a short time, and then linearly increase toward ten volts. There will be a small positive jump just before the linear sweep

starts. This waveform should be repeatable every time the start push button is pushed.

9. Adjust the sweep-balance control, (CON-15), so that the small positive jump is about 0.5 volts high. Now, every time the push button is pressed the observer should note: the voltage will rapidly decrease from ten volts to zero, remain at zero for a short time, then rapidly jump to 0.5 volts and then linearly increase to ten volts again. This point will remain at ten volts until the start button is again pressed.
10. Adjust the ST-1 threshold-level control, CON-4, so that the sweep automatically repeats itself.
11. Adjust, CON-4, so that reset occurs at plus-nine volts. The waveform will like the following: the voltage will stay at zero for a short time, a small positive jump and then linearly increase toward nine volts. When the sweep reaches the nine volt level it will reset rapidly to zero and the cycle will automatically repeat.
12. Place the test probe back on the emitter of T19. The reader should observe the following: the waveform will linearly decrease from ten volts to a value greater than zero, reset to ten volts slowly and stay at ten volts until the cycle begins anew. Adjust the sweep-scan-reset timing control, CON-5,

so that the linear sweep will start at 200 milli-seconds after the reset portion of the cycle has been completed. It will be noted that this condition will appear to be unstable; ie, the reset will not occur 200 milli-seconds after the ten volt point is reached every time. This condition is due to the logical interaction between the interrogation and sweep-scan circuitry.

13. Adjust the sweep-scan reset timing, (CON-5), so that minimum time the waveform is at the ten volt level is 200 milli-seconds.
14. Connect the probe of the test CRO on the collector of T27. The sample timing pulses can be seen here. Adjust the sample timing pulse width, CON-6, to 100 milli-seconds.
15. Adjust the record timing pulse width to three milli-seconds. The CRO probe will be on the collector of T29. CON-7 will be adjusted.
16. The following are the integrator alignment procedures:
    a. Disconnect the input of the integrator. Here is where a banana plug connection is useful.
    b. Connect the integrator's input, via a 470 ohm resistor, to plus-ten volts.
    c. Place the probe of the test CRO on the collector of T13.
    d. The waveform at this point should resemble a repeating saw-tooth which starts at plus ten volts and linearly decreases

toward zero. Reset will occur before the voltage reaches the zero point. Once reset, the voltage will remain at ten volts for a short while before it will start discharging toward zero again. If the above waveform is not present, check the setting of the integrator reset timing control, CON-8. It should be set for maximum.

e. Now adjust CON-8 so that the waveform remains at ten volts for 15 milli-seconds.

f. Move the probe of the test CRO to the collector of T13.

g. Juggle the integrator's gain, CON-12, and bias control, CON-13, so that the waveform swings over the full ten volts. The response that was seen at the collector of T13 is now inverted and amplified so the integration process will start from zero and progress toward plus-ten volts.

h. Rejuggle the gain and bias controls so that the integration process starts as 0.5 volts.

i. Reconnect the input of the integrator (the banana plug again) to its normal operating condition.

17. Set the manual-auto-sweep switch, CON-14, to manual.

18. The following is the slit alignment procedure:

a. A glance back at the photos shown in figures 8 and 9 will help the experimenter to understand the slit-alignment procedure.

b. Attach the probe of the test CRO on the emitter of T4.

c. Adjust the manual sweep control, CON-14, so that a waveform such as that shown in figure 8-A is obtained.

d. Adjust the slit-width control, CON-2, so that the primative slit-width is from one to 1.5 volts wide. There will be a slight loading effect noted on the waveform so the width can be easily adjusted by observing the spacing of the loading disturbances.

e. Connect the probe of the test CRO to the collector of T7. A waveform like the one shown in figure 10-B should be noted.

f. Adjust C4 until both pulses have the same width. Figure 9-B shows us that the slit is in need of realignment. The slit must be religned if it is found necessary to replace a transistor in the slit circuitry.

19. Set the manual-auto-sweep switch back to automatic.

20. Adjust the sweep-scan rate, CON-3, to 15 seconds. It should now take 15 seconds to make one complete trace across the face of the display CRO.

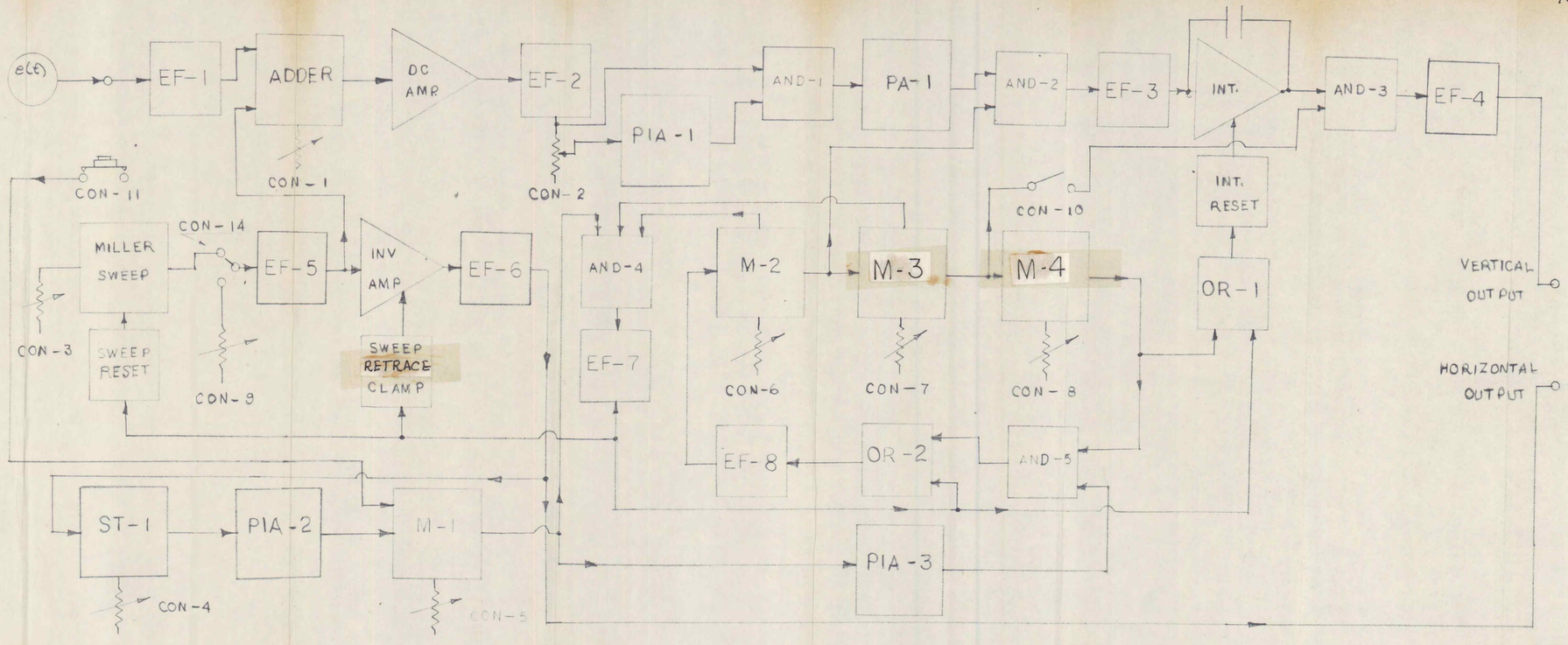
21. A waveform similar to that shown in figure 27 should be observed on the face of the display CRO. Note the vertical scale calibration. CON-1 is used to center the waveform. The end-points of the estimate will be at plus-and-minus three volts.

Adjust the horizontal sweep length (CON-4) so that the end-points of the waveform occur at the beginning and the end of the sweep. The centering control, CON-1, should be used to keep the image centered while this adjustment is being made.

Step 22 concludes the alignment procedure of the probability density estimator. If a step-test signal such as shown in figure 36 is available, it could be used to calibrate the horizontal scale of the instrument.

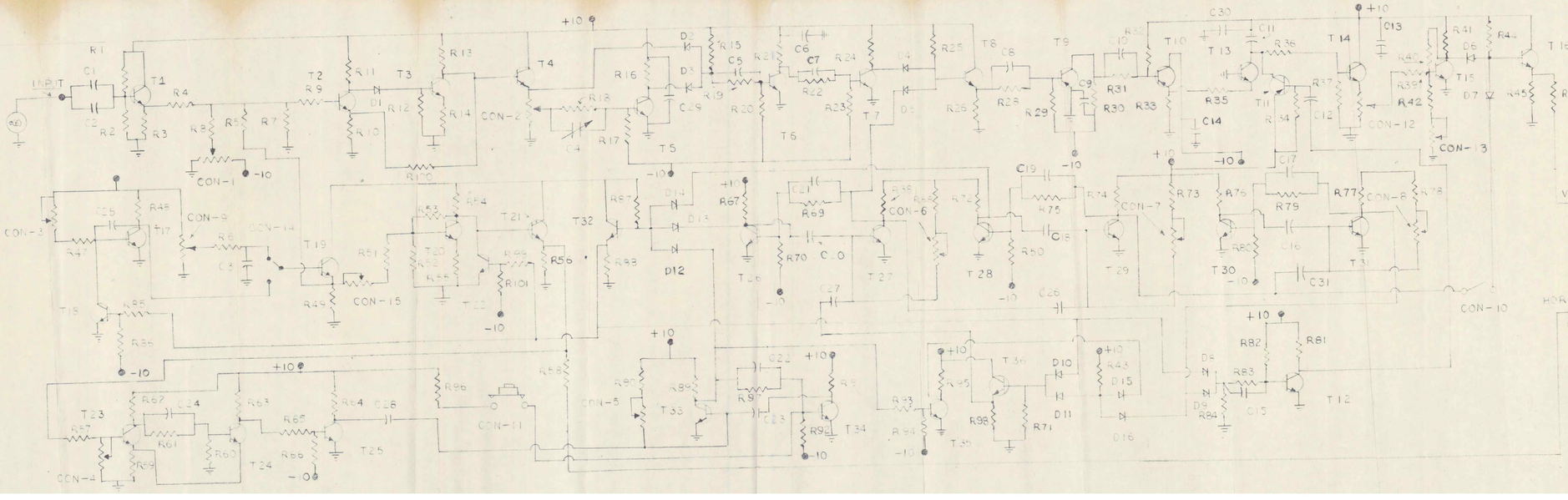
# APPENDIX V

FIGURE 37. THE COMPLETE LOGICAL DIAGRAM OF THE PDD ESTIMATOR.



# APPENDIX VII

FIGURE 38. THE COMPLETE SCHEMATIC DIAGRAM OF THE PDD ESTIMATOR.



# COMPONENT LIST

Resistors in ohms. All resistors have five percent tolerance, 1/2 watt ratings, (unless noted).

| | | | |
|---|---|---|---|
| R 1 | 3.3 k | R 55 | 47 |
| R 2 | 4.7 k | R 56 | 1 k |
| R 3 | 1.5 k | R 57 | 10 k |
| R 4 | 4.7 k | R 58 | 10 k |
| R 5 | 4.7 k | R 59 | 100 |
| R 6 | 2.2 k | R 60 | 10 k |
| R 7 | 4.7 k | R 61 | 2.2 k |
| R 8 | 4.7 k | R 62 | 4.7 k |
| R 9 | 6.8 k | R 63 | 4.7 k |
| R10 | 330 | R 64 | 4.7 k |
| R11 | 6.8 k | R 65 | 10 k |
| R12 | 22 k | R 66 | 22 k |
| R13 | 4.7 k | R 67 | 1 k |
| R14 | 100 | R 68 | 4.7 k |
| R15 | 4.7 k | | |
| R16 | 680 | R 69 | 4.7 k |
| R17 | 56 k | R 70 | 22 k |
| R18 | 1 k | R 71 | 10 k |
| R19 | 1 k | R 72 | 1 k |
| R20 | 10 k | R 73 | 4.7 k |
| R21 | 680 | R 74 | 1 k |
| R22 | 1 k | R 75 | 4.7 k |
| R23 | 6.8 k | R 76 | 1 k |
| R24 | 680 | | |
| R25 | 1 k | R 77 | 1 k |
| R26 | 470 | R 78 | 4.7 k |
| R27 | 470 | R 79 | 4.7 k |
| R28 | 1 k | R 80 | 22 k |
| R29 | 10 k | R 81 | 2.2 k |
| R30 | 1 k | R 82 | 56 k |
| R31 | 4.7 k | R 83 | 4.7 k |
| R32 | 56 k | R 84 | 10 k |
| R33 | 10 k | R 85 | 4.7 k |
| R34 | 56 k | R 86 | 22 k |
| R35 | 470 | R 87 | 4.7 k |

| | | | |
|---|---|---|---|
| R36 | 470 k | R 88 | 4.7 k |
| R37 | 220 k | R 89 | 1 k |
| R38 | 1 k | | |
| R39 | 4.7 k | R 90 | 4.7 k |
| R40 | 47 k | R 91 | 1 k |
| R41 | 10 k | R 92 | 22 k |
| R42 | 1 k | R 93 | 10 k |
| R43 | 15 k | | |
| R44 | 33 k | R 94 | 22 k |
| R45 | 1 k | R 95 | 4.7 k |
| R46 | 10 k | R 96 | 4.7 k |
| R47 | 1 k | R 97 | 4.7 k |
| R48 | 470 1 Watt | R 98 | 1 k |
| R49 | 1 k | R 99 | 4.7 k |
| R50 | 22 k | R100 | 22 k |
| R51 | 4.7 k | R101 | 22 k |
| R52 | 1 k | | |
| R53 | 36 k | | |
| R54 | 2.2 k | | |

Capacitors

| | |
|---|---|
| C 1 | 30 µf. 50 volts |
| C 2 | 1000 µf. Mica |
| C 3 | 5 µf. 20 volts |
| C 4 | 4 -380 pf. trimmer |
| C 5 | 500 pf. |
| C 6 | 30 µf., 50 volts |
| C 7 | 500 pf. |
| C 8 | 500 pf. |
| C 9 | 30 µf, 50 volts |
| C10 | 500 pf. |
| C11 | 120 µf. 50 volts, tantalum. |
| C12 | 30 µf., 50 volts |
| C13 | 30 µf, 50 volts |
| C14 | 30 µf, 50 volts |
| C15 | 500 pf |
| C16 | 3 µf, 15 volts |
| C17 | 500 pf. |
| C18 | 3 µf, 15 volts |
| C19 | 500 pf. |
| C20 | 8 µf. |

| | |
|---|---|
| C21 | 500 pf. |
| C22 | 500 pf. |
| C23 | 250 μf, 15 volts |
| C24 | 500 pf. |
| C25 | 2000 μf, 50 volts |
| C26 | .001 μf, paper. |
| C27 | .001 μf, paper. |
| C28 | .001 μf, paper. |
| C29 | 1000 pf mica |
| C30 | 30 μf, 50 volt. |
| C31 | .001 μf |

The Control function and value list may be found in appendix III.

Transistor types may be found in appendix II.