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Oversampled delta-sigma ($\Delta\Sigma$) modulators have been more and more widely used in the high-resolution analog-to-digital (A/D) data conversions. These converter architectures trade the high speed of circuit operation and the high degree of complexity in the digital signal processing (DSP) circuitry for the high resolution in data conversion which is otherwise hard to achieve under current VLSI technology [1].

Stability limitation in single-stage single-bit $\Delta\Sigma$ modulators makes their implementations more difficult [1]. And although the multibit single-stage $\Delta\Sigma$ modulators do not have stability limitations, they suffer from the nonlinearity error in the multibit digital-to-analog (D/A) converter in the feedback loop [1]. Thus another kind of modulators, namely dual-quantization $\Delta\Sigma$ modulators have attracted more and more attentions recently. Without stability limitation, this kind of modulators can ideally achieve very high signal-to-noise-ratio (SNR) at a relatively low oversampling ratio (OSR). However, this kind of modulators rely on the perfect matching between the analog and digital circuit transfer functions which is

hard to achieve. As a result, the SNRs of the A/D converters based on this kind of modulators are far below the ideal SNRs.

This thesis studies the effects of the nonideal analog circuitry on the SNR performance in various kinds of dual-quantization $\Delta\Sigma$ modulators. The possibility of digital estimation and compensation of these nonidealities is explored. Estimation algorithms and compensation schemes are presented. Both theory and simulation results showed that 10-20 dB SNR recovery is possible using these compensation schemes at a cost of a little more complicated digital circuitry.

Effects and Compensation of the Analog Integrator Nonidealities in Dual-Quantization Delta-Sigma Modulators

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Effects and Compensation of the Analog Integrator Nonidealities in Dual-Quantization Delta-Sigma Modulators

Chapter 1. Introduction

1.1 How Oversampled Delta-Sigma A/Ds Work

As an example, consider the first-order oversampled ΔΣ A/D shown in Figure 1, where $I(z) = z^{-1}/(1-z^{-1})$. The modulator consists of an analog filter, a one-bit A/D converter (also called quantizer) and a one-bit D/A converter in the feedback loop. It converts the analog input, a signal bandlimited by f_s but sampled at a much higher clock frequency f_c, to a one-bit digital signal at the same clock rate. The digital decimation filter following the modulator decimates the modulator output, which is a low resolution but high frequency digital signal, to a high-resolution signal at the Nyquist rate ($2f_s$).

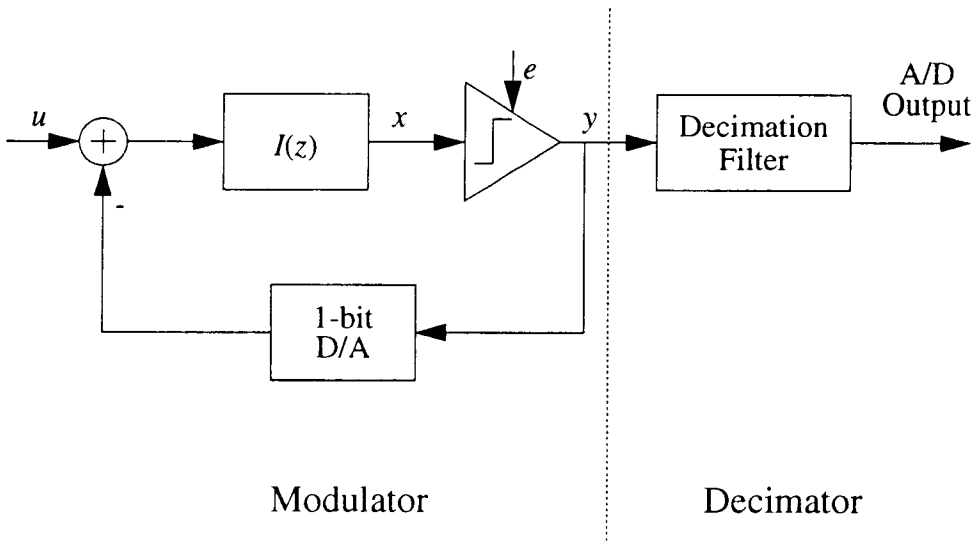

Figure 1. Oversampled ΔΣ A/D converter

The input-output relationship of the modulator can be shown as

$$y(nT) = u(nT-T) + e(nT) - e(nT-T), \tag{1.1}$$

where $e = y - x$ is the quantization error of the one-bit quantizer, and T is the clock period. Thus the z domain input-output relationship of the modulator is

$$Y(z) = z^{-1} \cdot U(z) + (1 - z^{-1}) E(z), \tag{1.2}$$

where z^{-1} is the signal transfer function (STF) of the modulator, and $1 - z^{-1}$ is the noise transfer function (NTF). Thus the input signal is passed to the output without any change except for a delay, which is usually insignificant, and the quantization noise e is filtered by a high-pass transfer function so that it has less spectrum density in the low frequency range, where the input signal has most of its energy in. Most of the noise energy is in the frequency range of $[f_S, f_C/2]$, and are removed by a low-pass digital decimation filter following the modulator.

If we model signal e as a white noise, the noise energy from $[0, f_S]$ is

$$n_0^2 = \frac{\pi^2}{3 \cdot OSR^3} \cdot \sigma_e^2 \tag{1.3}$$

[1], where OSR is defined as $f_C/2f_S$, and σ_e^2 is the mean square value of the quantization noise.

It can be shown that if the transfer function of the analog filter in the modulator shown in Figure 1 is modified, more efficient NTFs can be achieved [1]. More specifically, the z domain input-output relationship of an Lth-order $\Delta\Sigma$ modulator is

$$Y(z) = z^{-1} \cdot U(z) + (1 - z^{-1})^L E(z), \tag{1.4}$$

and its in-band noise energy is

$$n_0^2 = \frac{\pi^{2L}}{(2L+1) \cdot OSR^{2L+1}} \cdot \sigma_e^2 \tag{1.5}$$

[1]. From the above equation we know that with a given *OSR*, the higher the modulator order is, the less the in-band noise energy. However, this kind of straightforward design has a severe limitation, namely the high-order (L>2) single-stage single-bit modulators are usually unstable [1]. Although they can be stabilized by using IIR NTFs [2], the SNRs may be degraded significantly compared to those achieved by the modulators with transfer functions shown in Eq. (1.4). Single-stage multibit modulators can be guaranteed to be stable if the multibit quantizer has enough resolution, and can achieve the NTFs shown in Eq. (1.4), but they suffer from the nonlinearity error introduced by the multibit feedback D/A. Without the above limitations dual-quantization $\Delta\Sigma$ modulators have attracted more and more attentions recently as introduced below.

1.2 How Dual-Quantization Delta-Sigma Modulators Work

Dual-quantization $\Delta\Sigma$ modulators usually have a low order modulator as its first stage, and feed the first-stage quantization noise or the input of the first-stage quantizer to the second stage, which is usually another low order modulator or simply a multibit quantizer, and then the outputs of the two stages are combined appropriately to give the final output of the modulator. Because there are no high-order modulators in either stage, and there are no feedbacks between the two stages, stability is guaranteed.

As an example, consider the first-order Leslie-Singh modulator [3] shown in Figure 2. If the analog integrator is ideal, namely

$$I(z) = \frac{z^{-1}}{1 - z^{-1}}, \tag{1.6}$$

and the outputs of the two stages are combined properly by choosing

$$H_1(z) = z^{-1} \tag{1.7}$$

and

$$H_2(z) = 1 - z^{-1}, \tag{1.8}$$

it can be shown that its z domain input-output relationship is

$$Y(z) = z^{-1} \cdot U(z) + (1 - z^{-1}) \cdot E_2(z), \tag{1.9}$$

where $e_2 = y_2 - x$ is the second-stage quantization noise. It is obviously from Eq. (1.9) that ideally the first-stage quantization noise e_1 is perfectly cancelled, and the only noise which appears in the final output is the second-stage quantization noise, which is smaller due to the high resolution of the second-stage quantizer. Thus the in-band noise energy is much reduced and the SNR improved. Using similar ideas, higher order modulators can be designed. However, the above results are based the fact the analog transfer function shown in Eq. (1.6) can be ideally achieved, otherwise it can be shown the first-stage quantization noise will not be completely cancelled, instead a small part of its energy will appear in the final output and thus degrade the overall SNR of the modulator.

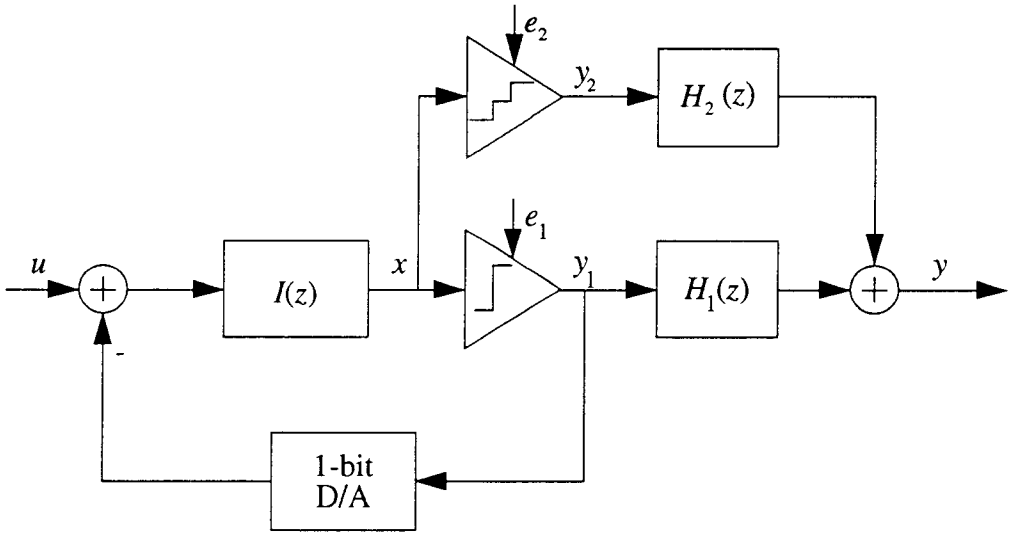

Figure 2. First-order Leslie-Singh Modulator

1.3 Nonidealities in the Analog Integrators

For most $\Delta\Sigma$ modulators the integrators are the most important analog circuit blocks, and are usually implemented by switched capacitor (SC) circuits. Thus understanding its nonidealities is important to the $\Delta\Sigma$ modulator design.

Consider the delaying SC integrator shown in Figure 3, where nominally $C_1 = C_2$, and $A = \infty$. It can be shown that if the opamp has an finite DC gain of A, and a capacitor mismatch δ defined as $C_1/C_2 - 1$, its z domain transfer function is

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{(1-\alpha)z^{-1}}{1-(1-\beta)z^{-1}} \tag{1.10}$$

[4], where

$$\alpha = \frac{2/A + \delta/A - \delta}{2/A + \delta/A + 1}, \tag{1.11}$$

$$\beta = \frac{1/A + \delta/A}{2/A + \delta/A + 1}. \tag{1.12}$$

Thus the integrator has both the gain error α and the pole error β. In the usual $\Delta\Sigma$

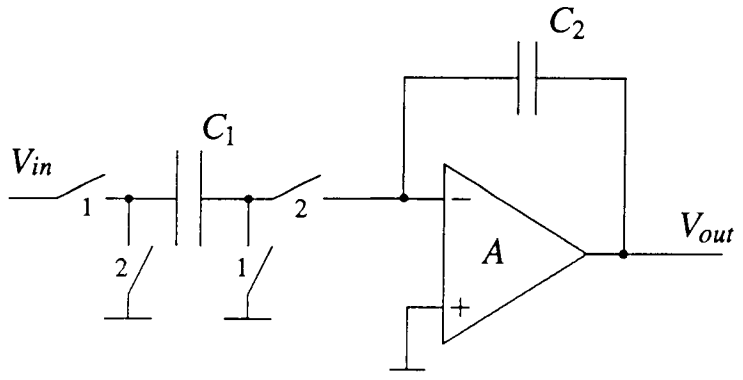

Figure 3. Switched Capacitor Integrator

A/D circuit implementations, the opamp DC gains are in the range of 55 - 70 dB depending on the design specifications. Thus if we define $\mu = 1/A$, μ is in the

range from 0.0003 to 0.002. On the other hand, the capacitance mismatch between two unit capacitors can be quite small, usually in the range of 0.1% to 0.4%, therefore δ is in the range from -0.004 to 0.004. Thus to a good approximation, Eq. (1.11) and (1.12) can be simplified as follows,

$$\alpha \approx 2\mu - \delta, \tag{1.13}$$
$$\beta \approx \mu. \tag{1.14}$$

Notice that the above derivation assumes that nominally $C_1/C_2 = \kappa = 1$, it can be shown that generally if $\kappa \neq 1$ the gain and pole errors are

$$\alpha \approx \mu(\kappa + 1) - \delta, \tag{1.15}$$
$$\beta \approx \mu\kappa, \tag{1.16}$$

where $\delta = C_1/C_2 - \kappa$. Notice that if $\kappa < 1$ effectively the integrator pole error is reduced. Throughout the rest of the thesis, $\kappa = 1$ is assumed for simplicity of discussion.

Thus the gain error α is usually in the range from -0.0034 to 0.008, and the pole error β is usually in the range from 0.0003 to 0.002. One interesting observation is that the pole error is only caused by the opamp finite gain but the gain error is caused by both the opamp finite gain and the capacitor mismatch.

Notice that other opamp nonidealities such as DC offset, finite bandwidth, etc., may also affect the overall performance. However these nonidealities are usually less significant in terms of the SNR degradation or can be remedied by proper design techniques. For example, the opamp DC offset voltages only affect the DC characteristics of the converters, and the DC offset voltages of the converters are usually cancelled during the power-up calibration time. The ratio between the opamp unity-gain bandwidth and the sampling clock frequency determines the settling of the integrator. Incomplete settling is usually equivalent to an additional gain error apart from the one indicated in Eq. (1.11) as long as the settling is linear.

In high resolution applications, usually enough settling time is allowed to eliminate the possibility of the harmonic distortion introduced by nonlinear settling. In this thesis it is assumed that enough settling is allowed so that the gain error of the integrator is only introduced by the opamp finite gain and capacitor mismatch.

Chapter 2. Effects of Integrator Nonidealities on SNR of Dual-Quantization Delta-Sigma Modulators

In this chapter, the effects of gain and pole error of the SC integrators on the SNR of the dual-quantization ΔΣ modulators are discussed. Due to the unavoidable mismatch between the analog and digital circuit transfer functions, the cancellation of the first-stage quantization noise is incomplete. Therefore the SNRs of this category of modulators may be limited by the amount of the first-stage quantization noise leaking into the final output. And it is shown that the pole error is much more crucial in terms of the SNR degradation than the gain error. The impacts of these nonidealities on the choice of design parameters are also discussed.

2.1 First-order Leslie-Singh Modulator

As discussed in Chapter 1.2, ideally first-order Leslie-Singh modulator can perfectly cancel the first-stage quantization noise e_1 and the only noise source in the final output will be the second-stage quantization noise e_2. From Eq. (1.9) and Eq. (1.5), ideally the in-band noise energy is that of the second-stage quantization noise,

$$n_2^2 = \frac{\pi^2 \cdot \sigma_{e_2}^2}{3 \cdot OSR^3}. \tag{2.1}$$

If no significant overloading occurs, we can assume e_2 is a random signal uniformly distributed in the range of [-Δ/2, Δ/2], where Δ is the quantization step [1]. For an M-bit quantizer with a non-overloading input voltage range of [$-V_{ref}$, $+V_{ref}$], $\Delta = 2V_{ref}/2^M$. Thus if for simplicity we assume $V_{ref} = 1$, the energy of the second-stage quantization noise can be calculated as

$$\sigma_{e_2}^2 = \frac{\Delta^2}{12} = \frac{1}{3 \cdot 4^M}. \tag{2.2}$$

From Eq. (2.1) and Eq. (2.2) we can get the root-mean-square (RMS) value of the ideal in-band noise as the following,

$$\overline{n_2} = \frac{\pi \cdot 2^{-M}}{3 \cdot OSR^{3/2}}. \tag{2.3}$$

For the simplicity of later discussion, we express the noise energy in dB,

$$\overline{n_2}\,(\mathrm{dB}) = -6.02M - 9.03osr + 0.4, \tag{2.4}$$

where osr is defined as $\log_2 OSR$.

One thing to notice here is that Eq. (2.3) and Eq. (2.4) are obtained based on the assumption that the input to the multibit quantizer seldom exceeds the non-overloading conversion range of the multibit quantizer. However this is usually not true, especially in high-order dual-quantization modulators. In circuit implementations, the reference voltages of the first and the second-stage quantizer are usually made the same for hardware simplicity. It can be shown that this arrangement will cause frequent overloading of the second-stage quantizer. Notice that the overloading occurs much more frequently for the multibit quantizer than the single-bit one because the non-overloading input range for the former is only $\pm(V_{ref} + \Delta/2)$ while the latter has a non-overloading input range as large as $\pm 2V_{ref}$. Also the consequence of the overloading in the second-stage quantizer is much more severe than in the first-stage quantizer because it will increase the energy of the second-stage quantization noise, which is directly present in the modulator output. One solution to this problem is to place a gain stage with a gain G smaller than 1, in front of the second-stage quantizer to prevent overloading. Typical values of G are 0.6 to 1.0 for first-order Leslie-Singh modulator, and 0.25 to 0.5 for the high-order dual quantization modulators depending on the second-stage quantizer resolutions. But after the quantization is finished, the quantized signal usually needs to be amplified by $1/G$ to maintain the original loop gain. The consequence is that the second-stage quantization noise is also amplified by the same factor. It can be

shown that other arrangements such as using two different reference voltages for the two quantizers will result in the same conclusion, that is, the overloading make the second-stage quantization noise increases by a factor of $1/G$. Thus Eq. (2.4) becomes

$$\overline{n_2}\,(\mathrm{dB}) \;=\; -6.02M - 9.03osr + 0.4 - 20\log G. \tag{2.5}$$

One very interesting thing here is that since usually $G<1$ is implemented by making the feedback capacitor larger than the input capacitor in the integrator, the pole error of the integrator is reduced according Eq. (1.16). And as discussed below, this will help reduce the first-stage leakage noise.

As shown in Chapter 1.2 and Figure 2, if there is any gain or pole error in the analog integrator, the cancellation of the first-stage quantization noise is incomplete and the leakage noise can be expressed in z domain as

$$E_{lk}(z) \;=\; E_1(z) \cdot \left(NTF_1(z) - H_2(z)\right) \tag{2.6}$$

where NTF_1 is the NTF of the first-order $\Delta\Sigma$ modulator. If the transfer function of the analog integrator has gain and pole errors as shown in Eq. (1.10), it can be shown that

$$NTF_1(z) \;=\; \frac{1 - bz^{-1}}{1 + (a-b)\,z^{-1}}, \tag{2.7}$$

where $a = 1 - \alpha$, and $b = 1 - \beta$. As shown in Appendix 1 and [4], the in-band leakage noise energy is approximately

$$\overline{n_{lk}}\,(\mathrm{dB}) \cong -3.01osr - A\,(\mathrm{dB}) - 4.8 \tag{2.8}$$

as long as the opamp DC gain is between 40 dB to 75 dB, and the oversampling ratio is over 32. If the opamp DC gain is so high that the SNR degradation caused by the integrator pole error is so small that the SNR degradation caused by the integrator gain errors can no longer be neglected, Eq. (2.8) will not be valid and Eq. (A.1.7) must be instead.

Thus both the first-stage leakage noise and the second-stage quantization noise contribute to the noise in the final output. If we assume these two noise sources are uncorrelated, the final in-band noise energy is

$$\overline{n_o} = \sqrt{n_2^2 + n_{lk}^2}. \tag{2.9}$$

Shown in Figure 4 are the simulated SNR versus integrator opamp DC gain curves when the first-stage leakage noise dominates the overall in-band noise energy. The curves agree with Eq. (2.8) quite well and show the conclusion that the SNR degradation is approximately independent of the capacitor mismatches. Notice that the zig-zags in the curves are caused by the non-random character of the quantization noise despite of the dither signal. Shown in Figure 5 are the SNR versus second-stage quantizer resolution curves. They show that for small M the first-stage leakage noise is negligible and thus if the M increases by 1 bit, the second-stage quantization noise decreases by 1 bit or 6 dB and the overall SNR increases by 6 dB. However if M is so high that the first-stage leakage noise can not be neglected, the SNR increase becomes smaller and finally saturates. Figure 5 shows that Eq. (2.8) predicts the leakage noise energy (around -90 dB) accurately.

From Figure 5 we see that in dual-quantization modulators the choice of the second-stage quantizer resolution depends on the first-stage leakage noise energy. This is true because the increase in the second-stage quantizer resolution M, which means the increase in hardware complexity, does not always increase the overall SNR by the same amount as shown in Figure 5. In fact, it is cost-effective to increase M only when the second-stage quantization noise dominates the overall in-band noise. In other words, a cost-effective design for an uncompensated dual-quantization modulators must make the second-stage noise the dominant noise source. Thus for a given design problem, one should start with the estimation of the leakage noise energy, from Eq. (2.8) in this case, and obtain the required opamp gain for the integrator and the oversampling ratio. If the required opamp

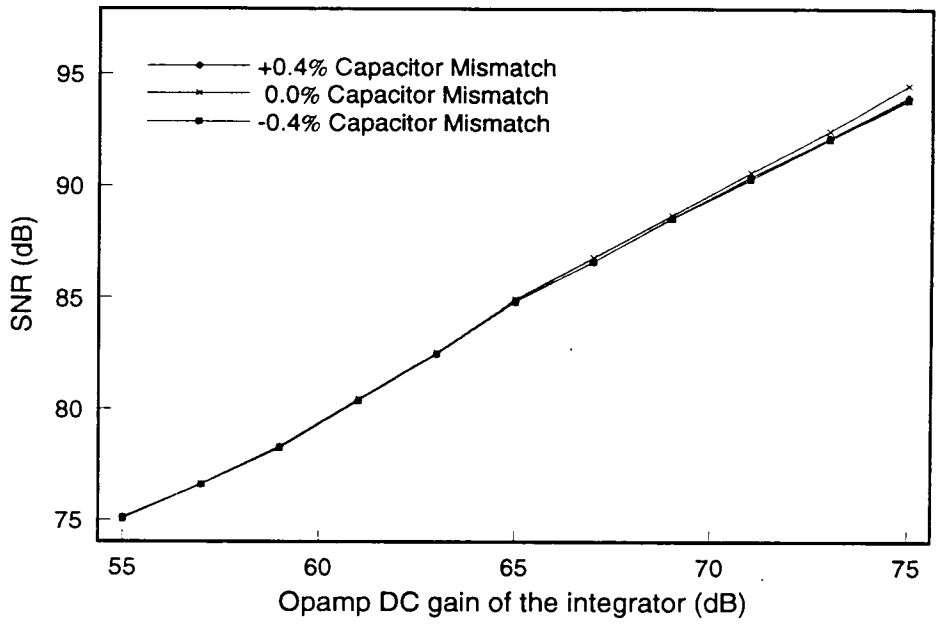

Figure 4. SNR versus analog integrator opamp DC gain curves in a 1-bit/8-bit first-order Leslie-Singh modulator with -10 dB input and an oversampling ratio of 128.

DC gain and the OSR are practical then the second-stage quantizer resolution can be determined accordingly otherwise different modulator topology with less leakage noise must be chosen.

2.2 Second-order Leslie-Singh Modulator

Shown in Figure 6 is the block diagram of a 1-bit/M-bit second-order Leslie-Singh modulator which employs a second-order modulator as its first stage and a multibit quantizer as its second stage with the digital correction transfer functions of $H_1(z) = z^{-1}(2 - z^{-1})$ and $H_2(z) = (1 - z^{-1})^2$. It can be shown that if both integrators in the modulator are ideal, i.e., if $I_1(z) = 1/(1 - z^{-1})$ and $I_2(z) = z^{-1}/(1 - z^{-1})$ are satisfied, the cancellation of the first-stage quantization noise is perfect and the input-output relationship is

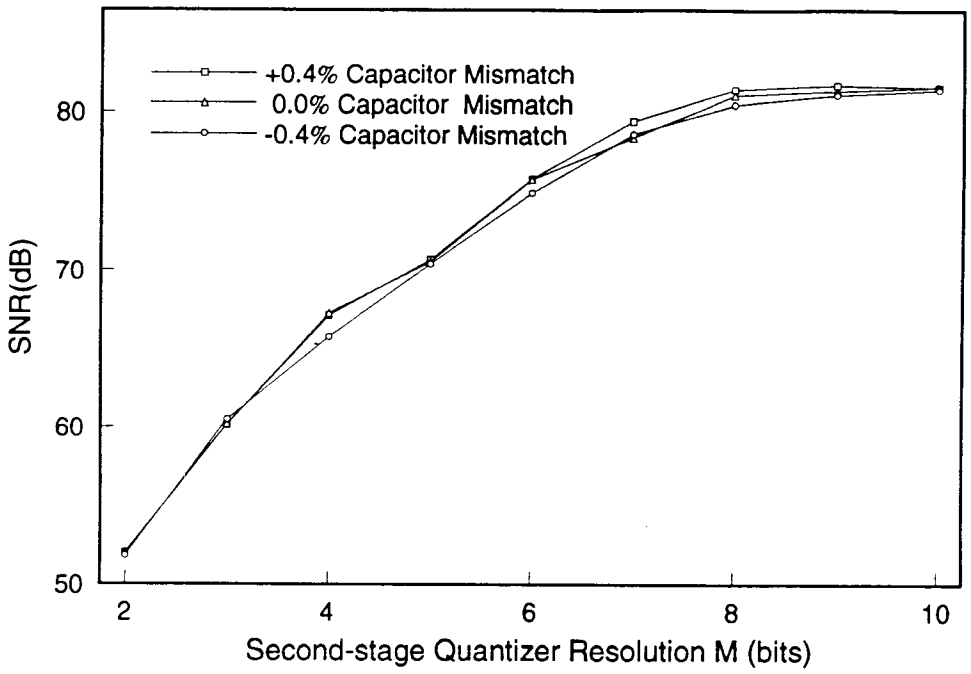

Figure 5. SNR versus second-stage quantizer resolution curve in a first-order Leslie-Singh modulator with a -10 dB input and an integrator opamp DC gain of 65 dB and an oversampling ratio of 128.

$$Y(z) = z^{-1} \cdot U(z) + (1 - z^{-1})^2 E_2(z) . \qquad (2.10)$$

Thus from Eq. (1.5) it can be shown the in-band second-stage quantization noise energy is

$$\overline{n_2}(\mathrm{dB}) = -6.02M - 15.05osr + 8.13 - 20\log G, \qquad (2.11)$$

where $G<1$ is the gain of the second-stage quantizer to prevent overloading as discussed in Chapter 2.1.

However, if the integrators have phase and gain errors, the cancellation of the first-stage quantization noise is incomplete and as shown in Appendix 2, the in-band leakage noise energy is approximately

$$\overline{n_{lk}}(\mathrm{dB}) \cong -9.03osr - \bar{A}(\mathrm{dB}) + 0.8 , \qquad (2.12)$$

where $\bar{A} = 1/(1/A_1 + 1/A_2) = A_1A_2/(A_1 + A_2)$ is the combined opamp DC

gain of the two integrators, while A_1 and A_2 are the DC gains of the opamps in the first and second integrator respectively. Again the above equation is only valid for opamp DC gains below 75 dB and oversampling ratios over 32, otherwise Eq. (A.2.9) must be used instead. The total in-band noise energy can be easily obtained from Eq. (2.9) assuming the two noise sources are uncorrelated.

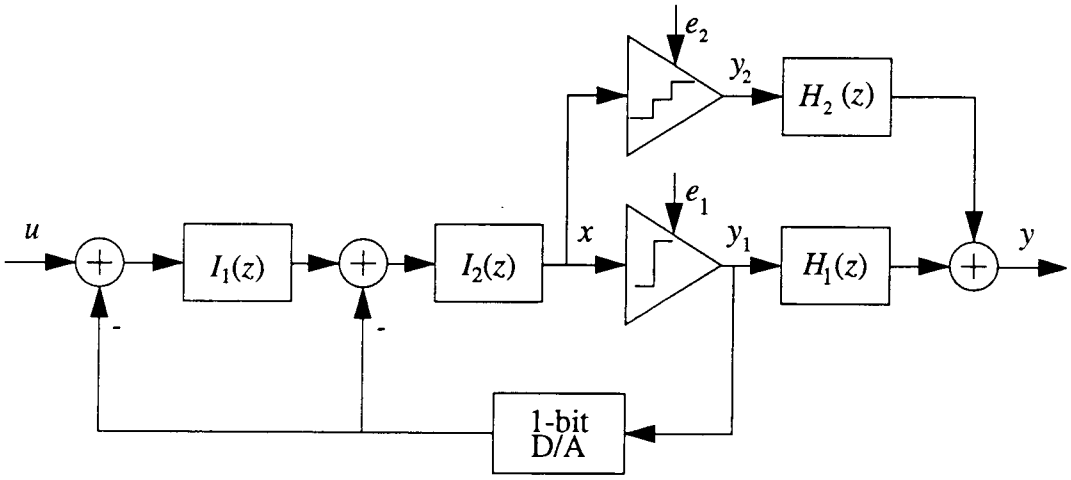

Figure 6. Second-order Leslie-Singh Modulator

Figure 7 and Figure 8 show the simulated SNR versus $\bar{A}$ curves when the first-stage leakage noise energy dominates the overall in-band noise energy. These curves agree with Eq. (2.12) quite well by showing the fact that the first-stage leakage noise energy is nearly independent of the capacitor mismatch and individual opamp DC gains of the integrators as long as the combined DC gain of the two opamps remains the same. Figure 9 and Figure 10 show the simulated SNR versus second-stage quantizer resolution curves. Again, the increase in the second-stage quantizer resolution M is efficient only when the second-stage quantization noise energy is significantly larger than that of the first-stage leakage noise.

Comparing the first and second-order Leslie-Singh modulators it is obvious that the latter has a much smaller leakage noise. Thus the requirement on the opamp DC gain of the integrators is much lower for a given SNR and OSR specifi-

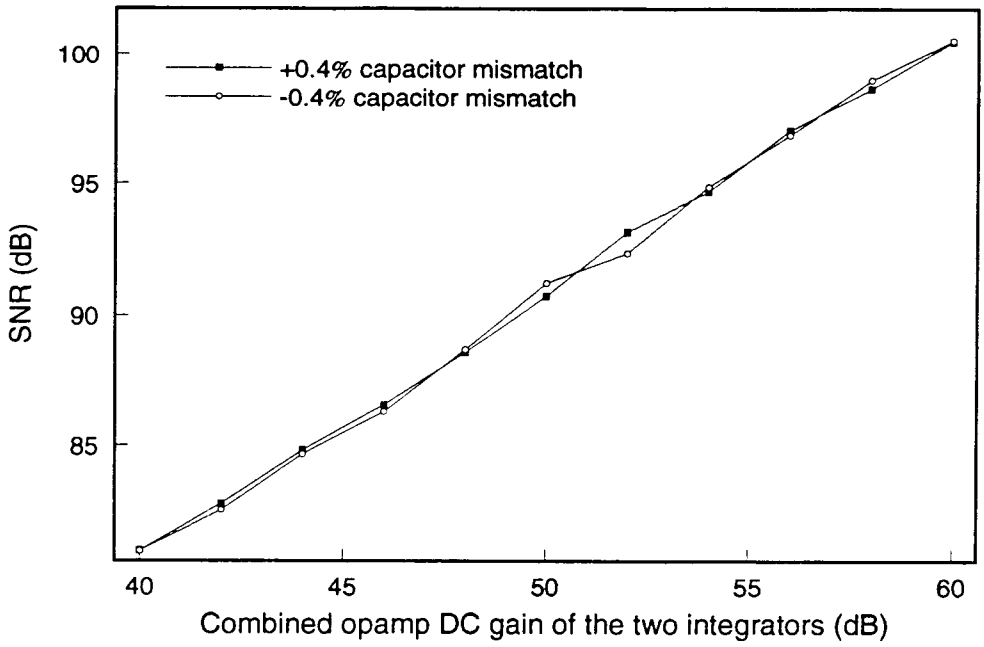

Figure 7. SNR versus combined integrator opamp DC gain curves of a 1-bit/8-bit second-order Leslie-Singh modulator with -10 dB input and an oversampling ratio of 64. (Both opamps have the same DC gain.)

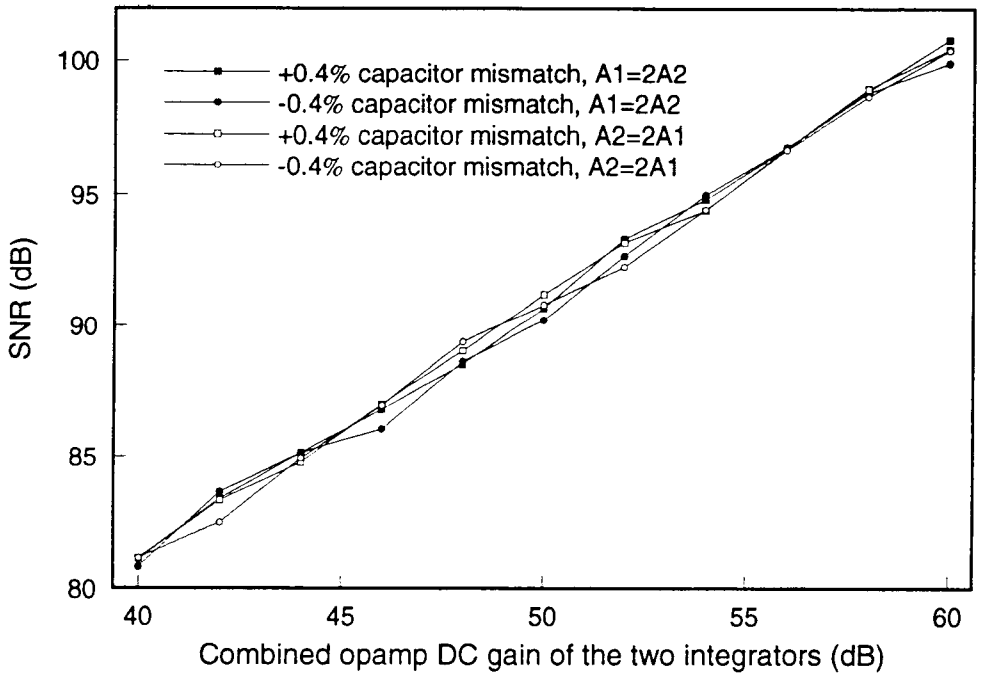

Figure 8. SNR versus combined integrator opamp DC gain curves in a 1-bit/8-bit second-order Leslie-Singh modulator with -10dB input and an oversampling ratio of 64. (Individual opamps have different DC gains.)

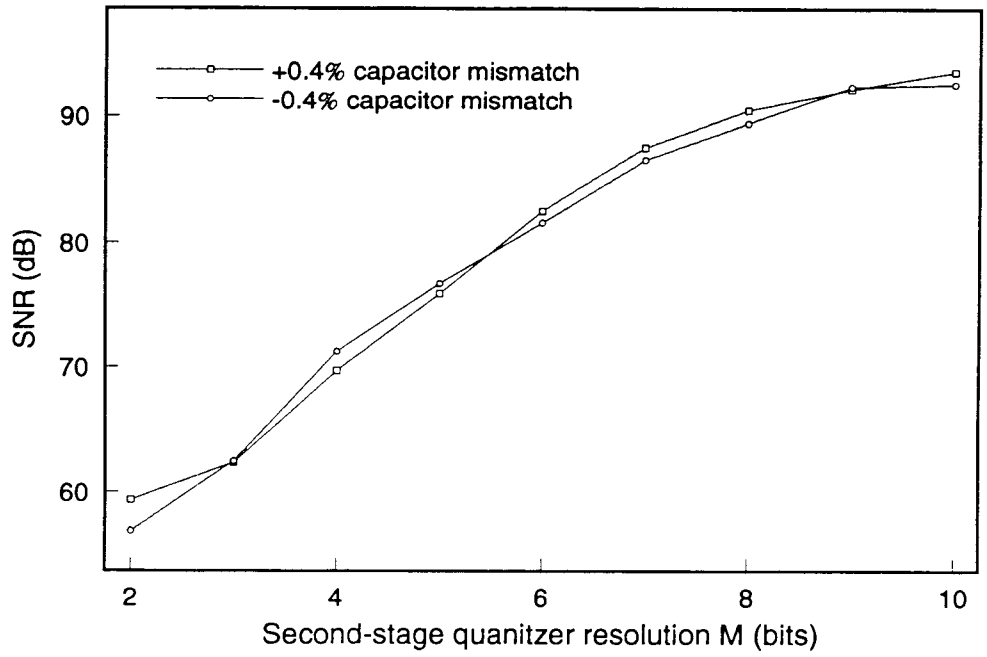

Figure 9. SNR versus second-stage quantizer resolution curves in a second-order Leslie-Singh modulator with a -10dB input, an oversampling ratio of 64 and combined integrator DC gain of 65 dB. (Both opamps have the same DC gain.)

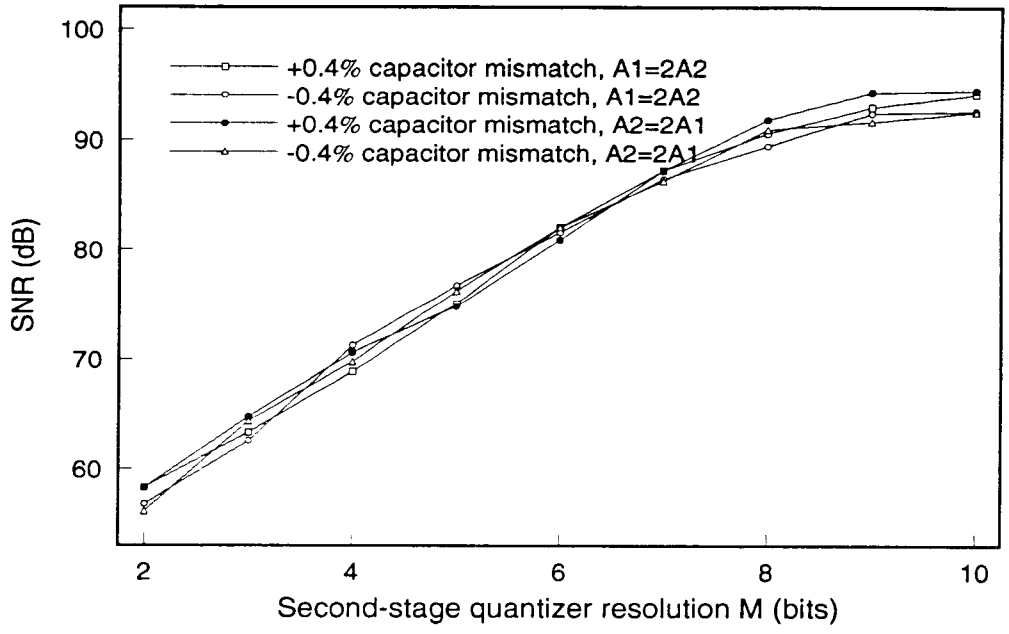

Figure 10. SNR versus second-stage quantizer resolution curve in a second-order Leslie-Singh modulator with a -10dB input, an oversampling ratio of 64 and a combined opamp DC gain of 65 dB. (Individual opamps have different DC gains.)

cation. However, the second-stage quantization noise energy of second-order Leslie-Singh modulator is not low enough because it is only second-order high-pass shaped and the overloading demands an amplification of $1/G$ in its amplitude, thus the second-stage quantizer must have a quite high resolution, about 8 bits, to achieve a SNR around 90 dB under a reasonable oversampling ratio such as 64. This means increased hardware complexity in both the second-stage quantizer and the decimation filter. To avoid this problem, higher order dual-quantization modulators are introduced.

2.3 Cascade 2-1 Modulator with Multibit Second-Stage

Shown in Figure 11 is the block diagram of a cascade 2-1 multibit modulator where the modulator employs a second-order single-bit modulator as its first stage and a first-order multibit modulator as its second stage, this structure is also known as Brandt-Wooley structure, named after its inventors [5].

It can be shown that if all the integrators in the modulator are ideal, namely $I_1(z) = 1/(1-z^{-1})$, and $I_2(z) = I_3(z) = z^{-1}/(1-z^{-1})$, the first-stage quantization noise is perfectly cancelled and the third-order shaped second-stage quantization noise is the only noise source appearing in the final output with an in-band energy of

$$\overline{n_2}\,(\mathrm{dB}) \approx -6.02M - 21.07osr + 16.6 - 20\log G, \qquad (2.13)$$

where G here is the inter-stage scaling factor to avoid overloading in the second stage. Notice that the second-stage quantization noise is not perfectly third-order shaped because due to the phase and gain errors in the second-stage integrators the NTF of the second-stage first-order modulator noise changes from perfect high-pass function $1-z^{-1}$ to a leaking one $1-\beta_3 z^{-1}$, however as shown in [1] and can be proved from Eq. (A.1.4.), as long as the opamp DC gain is at least twice as large

as the OSR, which is almost always the case, the increase in the in-band noise energy due to a leaking NTF is less than 0.3 dB. Moreover, it is followed by the digital transfer function $H_2(z)$, which is a perfect second-order high-pass transfer function $(1-z^{-1})^2$, thus the in-band energy of the second-stage quantization noise is hardly changed from the ideal situation.

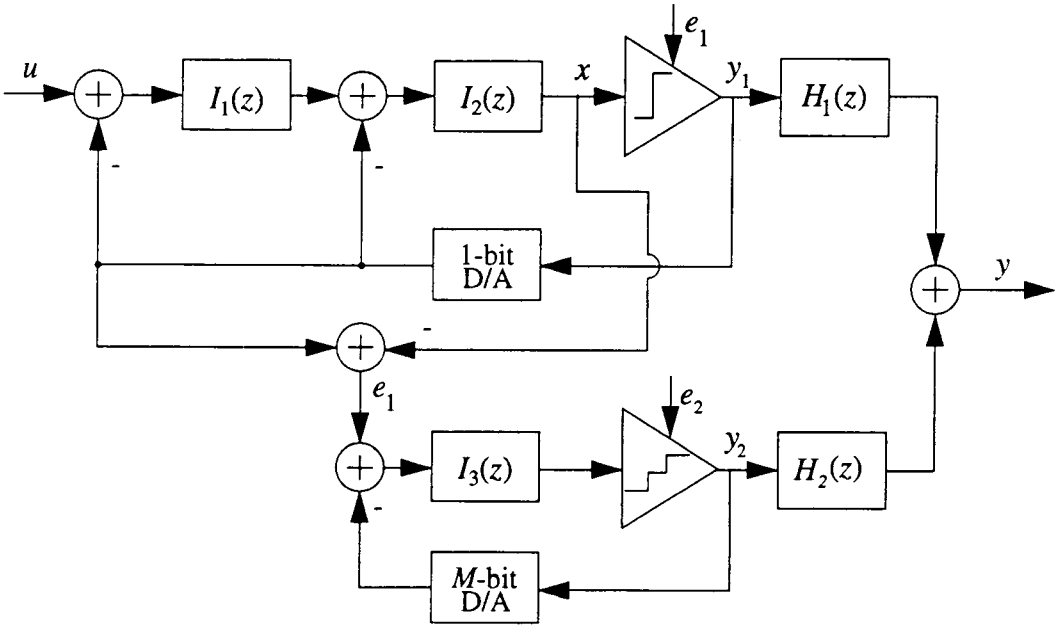

Figure 11. Block diagram of a multibit cascade 2-1 modulator

If the integrators have pole and gain errors, the cancellation of the first-stage quantization noise is incomplete and as shown in Appendix 2.2, the in-band leakage noise energy is approximately

$$\overline{n_{lk}}\,(\mathrm{dB}) \cong -9.03\,osr - \bar{A}\,(\mathrm{dB}) + 0.4\ , \qquad (2.14)$$

where $\bar{A} = A_1A_2/(A_1+A_2)$ is the combined opamp DC gain of the first-stage integrators, while A_1 and A_2 are the DC gains of the opamps in the first and second integrator respectively. In other words, this modulator has approximately the same in-band leakage noise energy as the second-order Leslie-Singh modulator. Therefore, its leakage noise energy is nearly independent of the pole and gain errors of the second-stage integrator and thus the opamp DC gain of the second-stage inte-

grator A_3. As before, the above equation is valid for low or medium opamp DC gains and medium to high oversampling ratios.

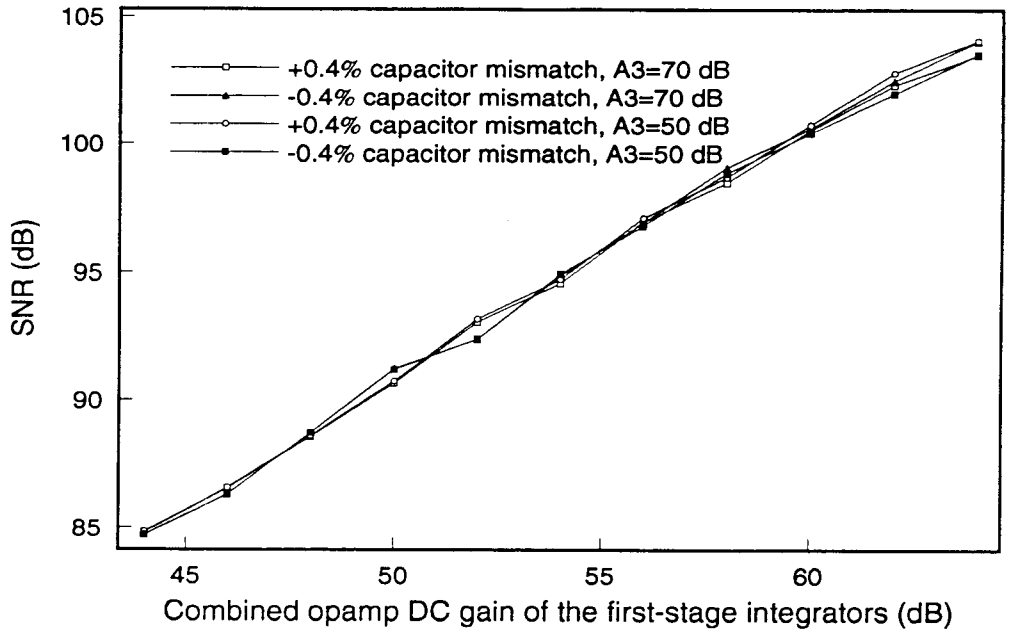

Figure 12. SNR versus combined opamp DC gain of the first-stage integrators curves in a 1-bit/8-bit cascade 2-1 modulator with a -10dB input and an oversampling ratio of 64. (Both opamps in the first-stage have the same DC gain.)

Figure 12 and 13 show the fact that the leakage noise energy is nearly independent of integrator gain errors, second-stage integrator pole error, and individual opamp DC gains of the first-stage integrators as long as the combined opamp DC gain remains the same. Figure 14 shows the fact that due to the increase in the order of the modulator, the in-band energy of the second-stage quantization noise is much reduced and consequently the required second-stage quantizer resolution for a given SNR is much lowered. With the same first-stage combined opamp DC gain, this modulator needs only a 4-bit second-stage quantizer at the oversampling ratio of 32 to achieve an overall SNR around 90 dB, while a second-order Leslie-Singh modulator needs to have a 8 or 9-bit second-stage quantizer. Also, the high order of noise shaping makes it suitable for high-speed medium SNR applications [5]. It can be expected that the further increase in the order of the modulator can

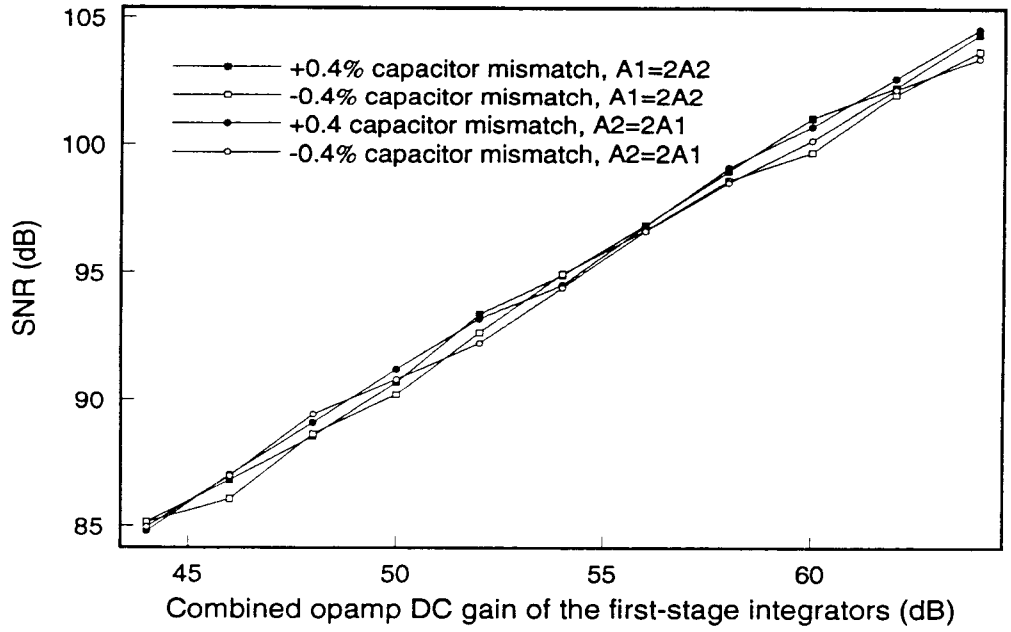

Figure 13. SNR versus combined opamp DC gain of the first-stage integrators curves in a 1-bit/8-bit cascade 2-1 modulator with a -10dB input and an over-sampling ratio of 64. (Individual opamps in first-stage have different DC gains, A_3=50 dB.)

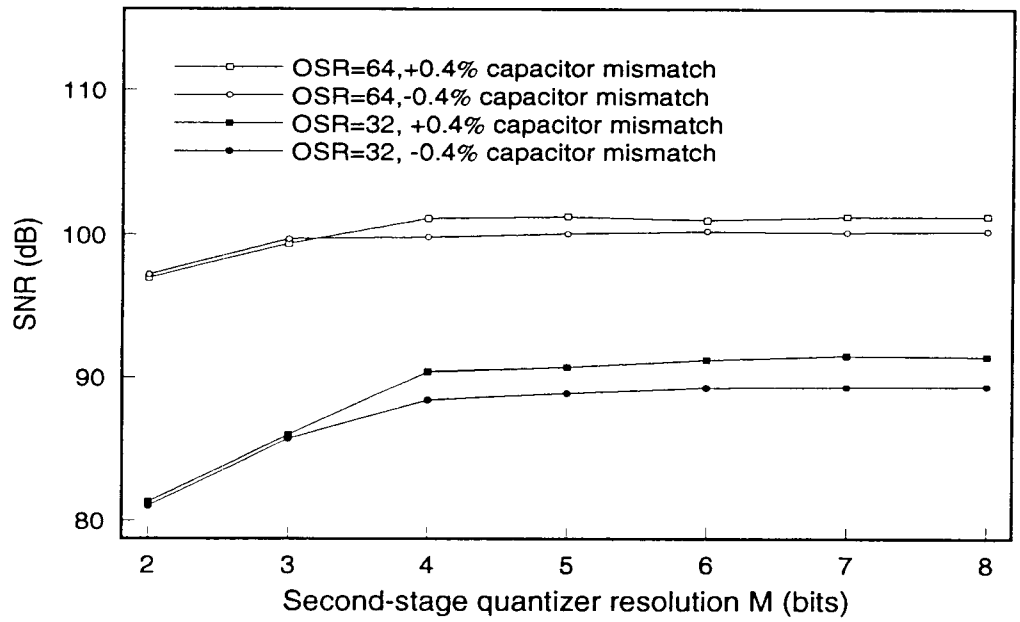

Figure 14. SNR versus second-stage quantizer resolution curves in a multibit cascade 2-1 modulator with a -10dB input, an oversampling ratio of 32 or 64, A_3=50 dB, A_1=A_2=63.01 dB, (first-stage combined opamp DC gain = 60 dB).

even eliminate the necessity of a multibit second-order quantizer, a single-bit one can be used instead.

2.4 Cascade 2-2 Modulator

Shown in Figure 15 is the block diagram of a single-bit cascade 2-2 modulator where $H_1(z) = z^{-1}$ and $H_2(z) = (1-z^{-1})^2$. It can be shown that if $I_1(z) = I_3(z) = 1/(1-z^{-1})$ and $I_2(z) = I_4(z) = z^{-1}/(1-z^{-1})$, the cancellation of the first-stage quantization noise is perfect and the only noise source appearing in the final output is the perfectly fourth-order shaped second-stage quantization noise e_2 with an in-band energy of

$$\overline{n_2}\,(\mathrm{dB}) = -27.09osr + 25.5 - 20\log G, \qquad (2.15)$$

where G is the inter-stage scaling factor used to avoid overloading in the second stage. As before, the nonidealities in the second-stage will change the NTF of the second-stage quantization noise but again, both theory and simulation results show that for reasonably high opamp DC gains and practical OSRs the increase in the in-band energy of the second-stage quantization noise due to the second-stage integrator gain and pole errors is negligible.

If there are pole and gain errors in the integrators, the noise cancellation of the first-stage quantization noise is incomplete and it is shown in Appendix 2.2 that the in-band leakage noise energy is approximately

$$\overline{n_{leak}}\,(\mathrm{dB}) \cong -9.03osr - \bar{A}\,(\mathrm{dB}) + 0.4, \qquad (2.16)$$

where $\bar{A}$ is the combined opamp DC gain of the first-stage integrators defined the same way as before. Again the in-band leakage noise is nearly independent of the integrator gain errors and also independent of the pole errors of the second-stage integrators for low to medium opamp DC gains and medium to high oversampling ratios.

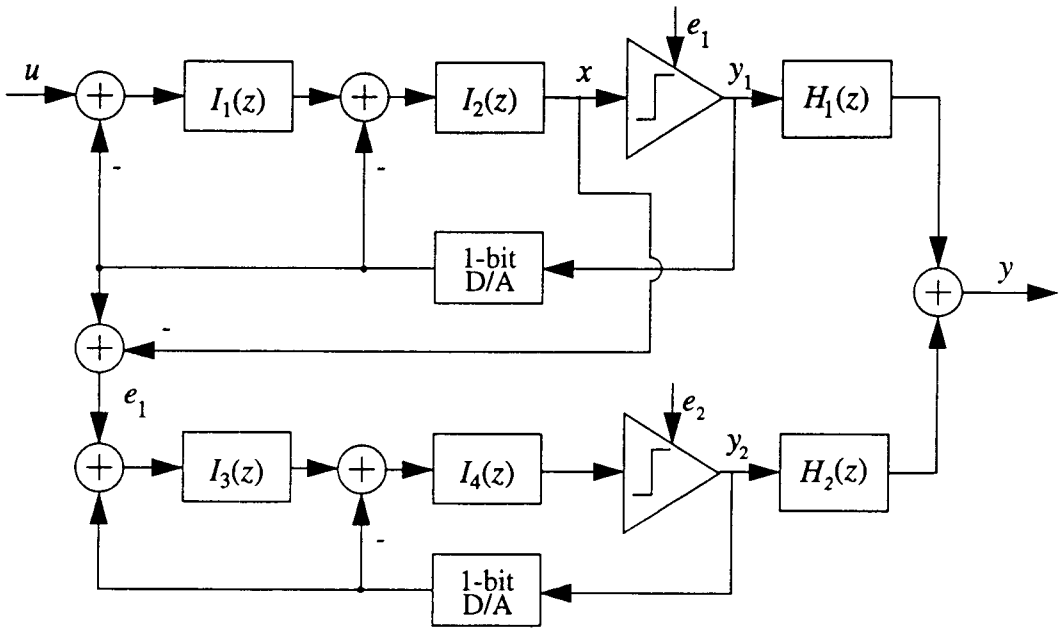

Figure 15. Block diagram of cascade 2-2 modulator

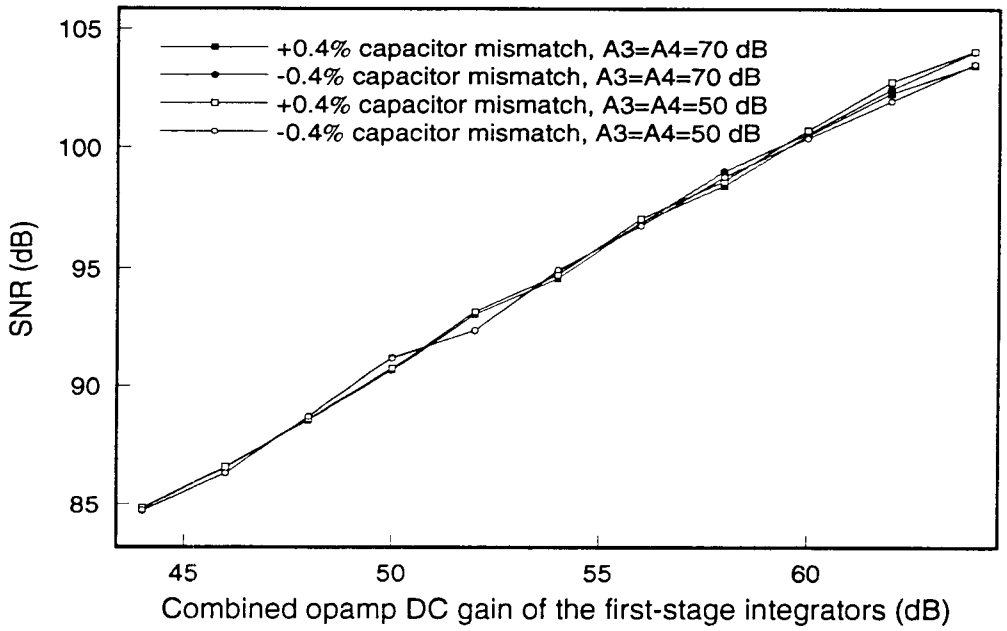

Figure 16. SNR versus combined opamp DC gain of the first-stage integrators curves in a single-bit cascade 2-2 modulator with a -10dB input and an over-sampling ratio of 64. (Both opamps in the first stage have the same DC gains.)

Figure 16 and 17 support the above conclusion and show that the even with a

single-bit second-stage quantizer the second-stage quantization noise is still negligible compared with the in-band leakage noise for reasonable opamp DC gains at an oversampling ration of 64. As a matter of fact, from Eq. (2.15) even for an OSR of 32 the in-band second-stage noise energy is still around -100 dB, which is sufficient for most applications. If, however, the specification demands an even lower OSR and a relatively high SNR, it may be necessary to use a multibit second-stage quantizer.

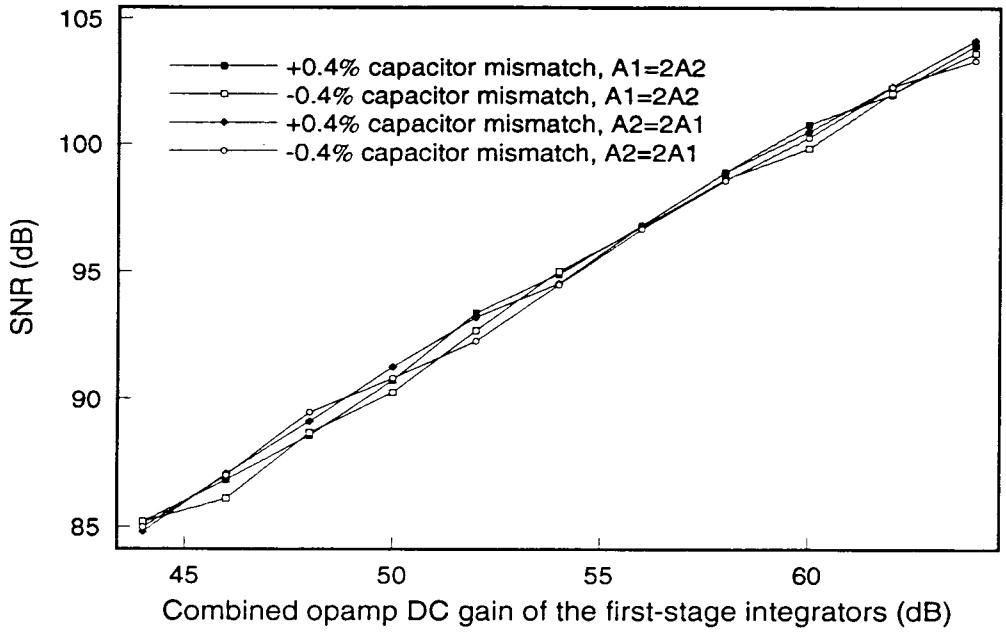

Figure 17. SNR versus combined opamp DC gain of the first-stage integrators curves in a single-bit cascade 2-2 modulator with a -10dB input and an oversampling ratio of 64, A_3=A_4=50 dB. (Individual opamps in the first stage have different DC gains.)

Chapter 3. Digital Compensation for Analog Integrator Nonidealities in Dual-Quantization Delta-Sigma Modulators

We saw in Chapter 2 that in dual-quantization $\Delta\Sigma$ modulators due to the mismatch between the analog and digital transfer functions caused by the nonidealities in the analog integrators, the first-stage quantization noise will not be completely cancelled and will appear in the final output, and thus degrade the SNR of the modulator. However, if the estimation of the above nonidealities is available, digital compensation can be implemented by modifying the digital transfer function so that a better matching between the analog and digital transfer functions and consequently a better cancellation of the first-stage quantization noise can be achieved, and therefore the SNR of the modulator can be increased. Generally speaking, digital compensation can, at the price of more complicated digital circuitry, get higher conversion accuracy out of a dual-quantization $\Delta\Sigma$ modulator with poor analog integrators or, more specifically, with low integrator opamp DC gains. This technique may also increase the conversion rate of the modulator because the opamps, which usually cause the speed limitation of the whole modulator, can now be faster since its DC gain requirement is much lowered by using the digital compensation.

Apart from these merits, digital compensation may be quite costly in implementation due to the following facts: firstly, it requires estimation circuits for the integrator nonidealities, which will be discussed in Chapter 4; secondly, it increases the decimator complexity significantly; and thirdly, since the digital compensation only reduces the first-stage leakage noise, to reduce the total in-band noise energy the second-stage quantization noise must be reduced as well by increasing either the second-stage quantizer resolution or the order of the modulator. In this chapter, digital compensation and its corresponding decimation schemes are discussed for various dual-quantization $\Delta\Sigma$ modulators.

3.1 Compensation for First-Order Leslie-Singh Modulator

From Chapter 2.1 we know that to cancel perfectly the first-stage quantization noise, the first-stage leakage noise transfer function (LNTF) must be equal to zero,

$$LNTF = NTF_1 \cdot H_1 + (NTF_1 - 1) \cdot H_2 = 0, \tag{3.1}$$

where all the transfer functions in the above equations are defined in Chapter 2. It can be shown that if H_1 and H_2 are FIR functions, there is a unique solution, except for a common factor, to Eq. (3.1), namely $H_1 = \alpha z^{-1}$, and $H_2 = 1 - (1 - \beta) z^{-1}$.

Thus if the estimation of the integrator gain error, denoted by $\hat{\alpha}$, and the estimation of the integrator pole error, denoted by $\hat{\beta}$, are available the digital compensation can be implemented by choosing $H_1 = \hat{\alpha} z^{-1}$, and $H_2 = 1 - (1 - \hat{\beta}) z^{-1}$. However, both theoretical derivation and computer simulation showed that the correction for all integrator nonidealities is unnecessary for common circuit parameters. Therefore, to save the hardware complexity in both estimation and decimation circuitry only the correction for the integrator pole errors is implemented. Thus the correction transfer function of the compensated first-order Leslie-Singh modulator is

$$H_1 = z^{-1}, H_2 = 1 - (1 - \hat{\beta}) z^{-1}. \tag{3.2}$$

As shown in Appendix 1, the in-band leakage noise energy after compensation is then approximately

$$n_{lkc}^2 \cong \sigma_{e_1}^2 \cdot \frac{(\beta - \hat{\beta})^2}{OSR} \cong n_{lk}^2 \cdot K^2. \tag{3.3}$$

where $K = (1 - \hat{\beta}/\beta)$ is the relative estimation error of β, and n_{lk}^2 is the in-band leakage noise energy of the uncompensated scheme. The value of K usually ranges from 0.05 to 0.15 if the estimation algorithm described in Chapter 4 is used. In

other words, the reduction of the in-band leakage noise energy due to the digital compensation is around 17-26 dBs. Figure 18 shows the compensated SNR versus opamp DC gain curves with different values of K.

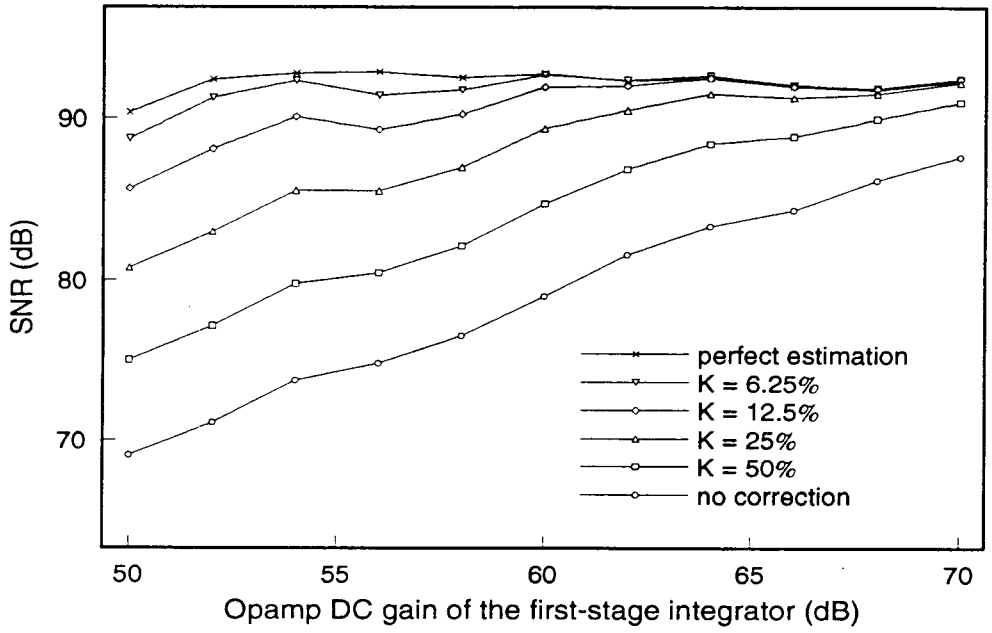

Figure 18. SNR versus the opamp DC gain of the first-stage integrator in a compensated 1-bit/10-bit first-order Leslie-Singh modulator with different estimation accuracy of the integrator pole error (0.4% capacitor mismatch, OSR=128, -10 dB input).

A few things here are worth noticing. First, the compensation only reduces the in-band energy of the first-stage leakage noise, and does not reduce the in-band energy of the second-stage quantization noise. In other words, it only increases the upper limit of the achievable SNR of the modulator in the presence of first-stage leakage noise. To increase the overall SNR, the second-stage quantization noise must be reduced as well by either increasing the resolution of the second-stage quantizer or employing a high-order second stage. Second, the modification of the correction transfer function H_2 changes the transfer function of the second-stage quantization noise from $1-z^{-1}$ to $1-\hat{\beta}z^{-1}$, in other words, now the second-stage quantization noise is no longer perfectly first-order high-passed. However, it can

be shown from Eq. (A.1.4.) that if the opamp DC gain of the integrator is at least twice as large as the OSR, the increase in the in-band noise energy is negligible. Third, from Figure 18 we see that if the estimation error is very small, say smaller than 0.06-0.1, the reduction of the in-band energy of the leakage noise is not as big as that predicted by Eq. (3.3) either because the integrator gain error is no longer negligible or, more often, because the second-stage quantization noise becomes dominant. And for higher opamp DC gain, the required estimation accuracy is lower for a given in-band second-stage quantization noise energy. From the above observations, it becomes obvious that the compensation works better for relatively low opamp DC gain as long as the opamp DC gain is at least twice as large as the OSR so that the modification of H_2 does not increase the in-band energy of second-stage quantization noise significantly, and that a relative error of pole error estimation around 5% is sufficient to recover most of the SNR loss due to the first-stage leakage noise. Thus there is no need to include compensation for integrator gain errors or to use a very accurate pole error estimation circuit.

3.2 Compensation for Second-Order Leslie-Singh Modulator

It can be shown that if the estimations of the first and second integrator pole errors, denoted by $\hat{\beta}_1$ and $\hat{\beta}_2$ respectively, are available, the digital compensation for the second-order Leslie-Singh modulator can be implemented by choosing

$$H_1 = z^{-1}(2 - z^{-1}),\ H_2 = (1 - z^{-1})^2 - (\hat{\beta}_1 + \hat{\beta}_2) \cdot z^{-1}(1 - z^{-1}). \quad (3.4)$$

As shown in Appendix 2.3, the in-band energy of the first-stage leakage noise is

$$n_{lkc}^2 \cong \sigma_{e_1}^2 \cdot \frac{(\beta_1 + \beta_2 - \hat{\beta}_1 - \hat{\beta}_2)^2}{3 \cdot OSR^3/\pi^2} \cong n_{lk}^2 \cdot K^2, \quad (3.5)$$

where $K = 1 - (\hat{\beta}_1 + \hat{\beta}_2)/(\beta_1 + \beta_2)$ is the relative estimation error of combined pole errors of the first-stage integrators, and n_{lk}^2 is the in-band leakage noise

energy of the uncompensated scheme. Shown in Figure 19 is the simulated compensated SNR versus combined opamp DC gain curves with different estimation accuracy.

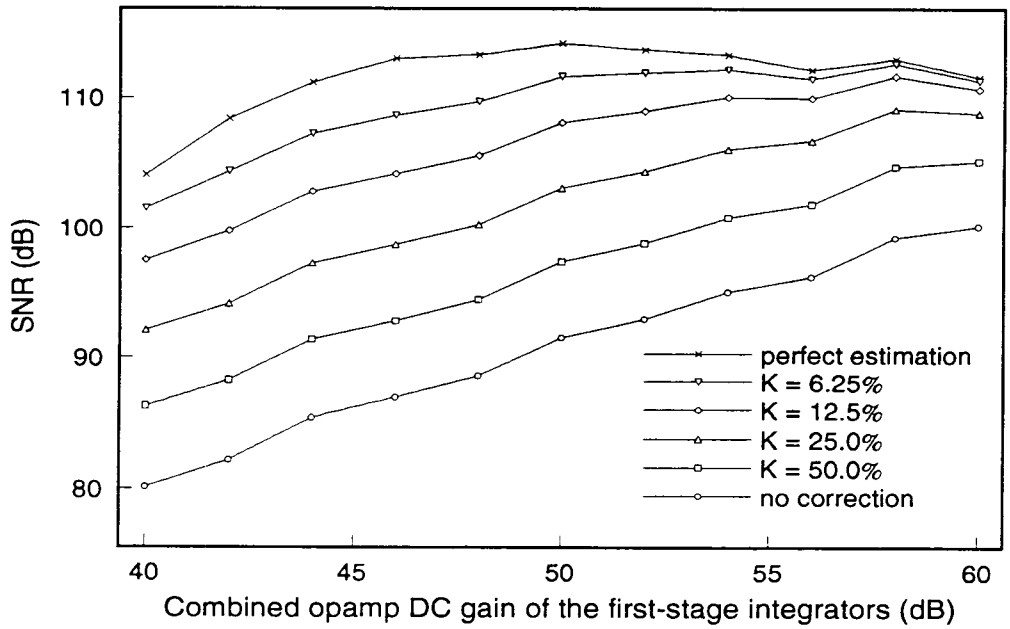

Figure 19. SNR versus the combined opamp DC gain of the first-stage integrators in a compensated 1-bit/10-bit second-order Leslie-Singh modulator with different estimation accuracy of the integrator pole errors. (0.4% capacitor mismatch, OSR=64, -10 dB input)

Again these curves match the theoretical derivations quite well by showing that each time K is halved, or the estimation accuracy doubled, the in-band energy of the first-stage leakage noise is reduced by roughly 6 dB until the improvement saturates when other noise becomes dominant. There is one thing worth noticing here: from the figure we see that for opamp DC gain smaller than 46 dB, even if the estimation is perfect, the SNR is degraded by 8-9 dB compared to the ideal case. This is because the compensation modifies the transfer function of the second-stage noise (Eq. (3.4)) in such a way that the its in-band energy is significantly larger unless the opamp DC gains are sufficiently high, in this case, higher than 50 dB. Thus the digital compensation can recover about 20-25 dB SNR with modest estimation accuracy for an opamp DC gain lower than 50 dB.

3.3 Compensation for Cascade 2-1 Modulator

It can be shown that if the estimations of the first and second integrator pole errors, denoted by $\hat{\beta}_1$ and $\hat{\beta}_2$ respectively, are available, the digital compensation for the cascade 2-1 modulator can be implemented by choosing

$$H_1 = z^{-1}, H_2 = (1-z^{-1})^2 - (\hat{\beta}_1 + \hat{\beta}_2) \cdot z^{-1}(1-z^{-1}). \tag{3.6}$$

As shown in Appendix 2.4, the in-band energy of the first-stage leakage noise is

$$n_{lkc}^2 \cong \sigma_{e_1}^2 \cdot \frac{(\beta_1 + \beta_2 - \hat{\beta}_1 - \hat{\beta}_2)^2}{3 \cdot OSR^3/\pi^2} \cong n_{lk}^2 \cdot K^2, \tag{3.7}$$

where $K = 1 - (\hat{\beta}_1 + \hat{\beta}_2)/(\beta_1 + \beta_2)$ is the relative estimation error of combined pole error of the first-stage integrators, and n_{lk}^2 is the in-band leakage noise energy of the uncompensated scheme. Shown in Figure 20 are the simulated compensated SNR versus combined opamp DC gain curves with different estimation accuracy.

The curves are similar to the ones before. Each doubling the accuracy in the estimation of combined integrator pole error gives an decrease of 6 dB in the in-band energy of the first-stage leakage noise, and if the leakage noise is the dominant noise source, an increase of 6 dB in the overall SNR. If the combined opamp DC gain of the first-stage integrators is larger than 50 dB, the decrease of SNR due to modification of the second-stage NTF is negligible.

3.4 Compensation for Cascade 2-2 Modulator

It can be shown that if the estimations of the first and second integrator pole errors, denoted by $\hat{\beta}_1$ and $\hat{\beta}_2$ respectively, are available, the digital compensation for the cascade 2-2 modulator can be implemented by choosing

$$H_1 = z^{-1}, H_2 = (1-z^{-1})^2 - (\hat{\beta}_1 + \hat{\beta}_2) \cdot z^{-1}(1-z^{-1}). \tag{3.8}$$

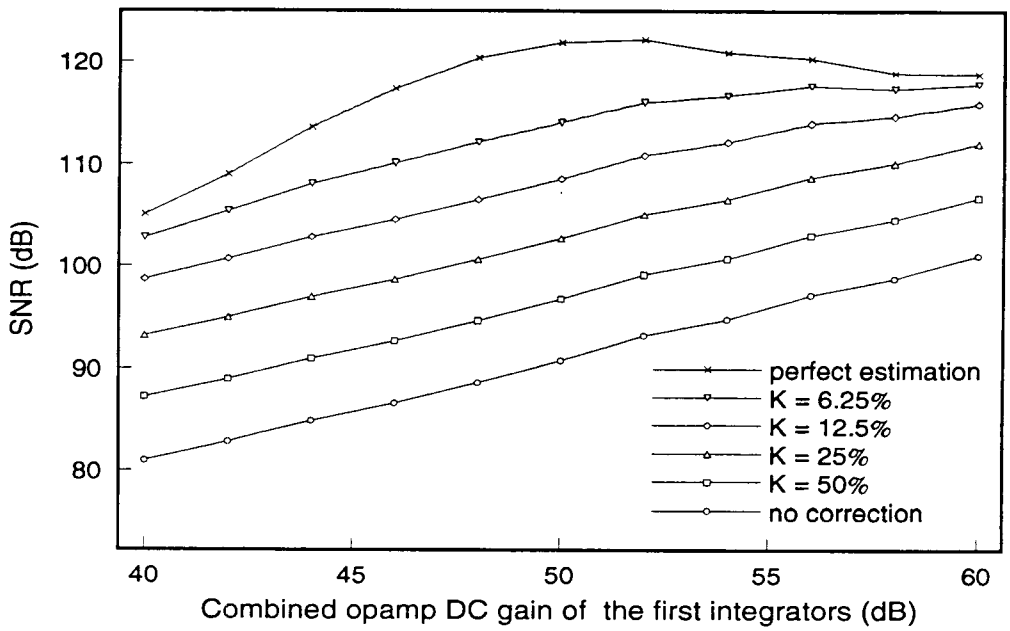

Figure 20. SNR versus the combined opamp DC gain of the first-stage integrators in a compensated 1-bit/10-bit cascade 2-1 modulator with different estimation accuracy of the integrator pole errors. (0.4% capacitor mismatch, OSR=64, -10 dB input, second-stage opamp DC gain 50 dB)

As shown in Appendix 2.4, the in-band energy of the first-stage leakage noise is approximately the same as those of second-order Leslie-Singh and cascade 2-1 modulators,

$$n_{lkc}^2 \cong \sigma_{e_1}^2 \cdot \frac{(\beta_1 + \beta_2 - \hat{\beta}_1 - \hat{\beta}_2)^2}{3 \cdot OSR^3/\pi^2} \cong n_{lk}^2 \cdot K^2, \tag{3.9}$$

where $K = 1 - (\hat{\beta}_1 + \hat{\beta}_2)/(\beta_1 + \beta_2)$ is the relative estimation error of the combined pole errors of the first-stage integrators, and n_{lk}^2 is the in-band leakage noise energy of the uncompensated scheme. Shown in Figure 21 is the compensated SNR versus combined opamp DC gain curves with different estimation accuracy.

The curves are similar to the ones before: each doubling of the estimation accuracy gives an decrease of 6 dB in the in-band energy of the first-stage leakage noise, and if that is the dominant noise source, an increase of 6 dB in the overall

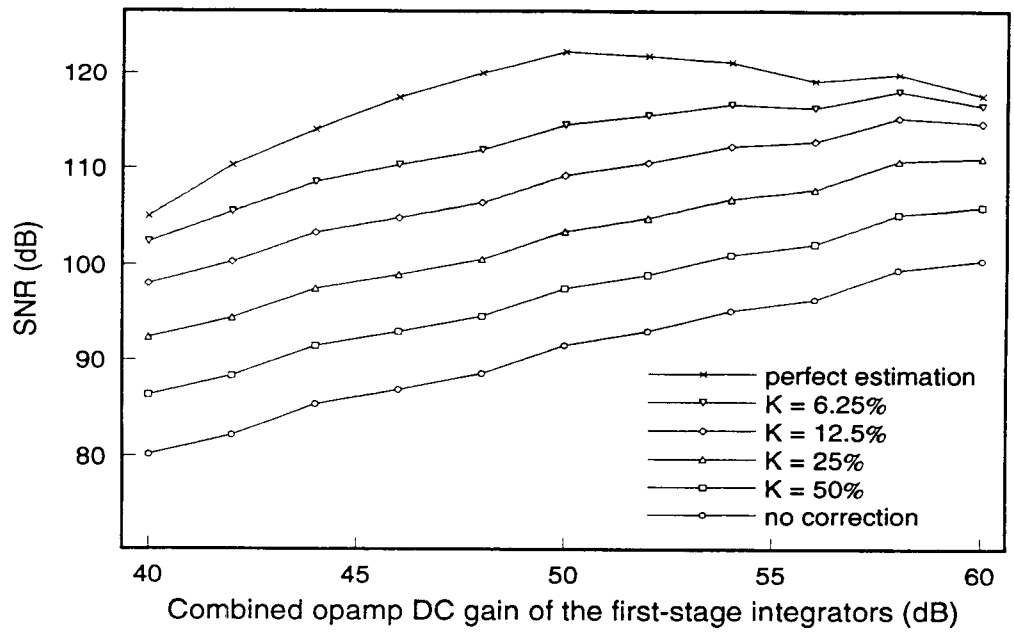

Figure 21. SNR versus the combined opamp DC gain of the first-stage integrators in a compensated 1-bit/3-bit cascade 2-2 modulator with different estimation accuracy of the integrator pole errors. (0.4% capacitor mismatch, OSR=64, -10 dB input, second-stage opamp DC gain 50 dB)

SNR. If the combined opamp DC gain of the first-stage integrators is larger than 50 dB, the decrease of SNR due to modification of the second-stage noise transfer function is negligible.

3.5 Decimation Filtering of the Compensated Dual-Quantization Delta-Sigma modulators

The decimation filtering for compensated dual-quantization $\Delta\Sigma$ modulators is more complicated because now H_2 contains multiplication operations (unless a one-bit quantizer is used in the cascade 2-1 or 2-2 structure), namely $\hat{\beta} \cdot y_2(n-1)$ for first-order Leslie-Singh modulator or $(\hat{\beta}_1 + \hat{\beta}_2) \cdot (y_2(n-1) - y_2(n-2))$ for other modulators discussed in this thesis. One straightforward choice, the so-called before-compensation decimation, is to compensate the modulator output signal $y(n)$ in each clock cycle and then feed the compensated modulator output to

the decimator. However, if the modulator is clocked at a very high frequency, the multiplication needed in each clock cycle may be a problem especially when M, the second-stage quantizer resolution, is high. Another problem is that if the compensation is performed before decimation, the compensated output $y(n)$ must have many more bits, which means a significant increase in the decimator complexity. Without compensation, the output $y(n) = y_1(n) + y_2(n) - y_2(n-1)$ can be represented by a M+2-bit binary code. On the other hand, as shown below, the compensated output of first-order Leslie-Singh modulator (or similar for any other compensated dual-quantization modulator) is

$$y(n) = y_1(n) + y_2(n) - y_2(n-1) + \hat{\beta} \cdot y_2(n-1), \qquad (3.10)$$

which requires many more bits to represent. Since $\hat{\beta} \ll 1$, it may be preferable to express and store it digitally as

$$\hat{\beta} = 2^{-P} \cdot B, \qquad (3.11)$$

where P and B are integers. Since the truncation of $\hat{\beta}$ will introduce additional error to the pole error estimation, the number of bits of B, denoted by Q for simplicity, must be quite large. It can also be shown that the worst-case relative error introduced by rounding $\hat{\beta}$ is 2^{-Q}. Thus, depending on the estimation accuracy requirement, Q may range from 4 to 7, corresponding to an 0.8% to 6% error due to the quantization effect alone. Therefore, from Eq. (3.11), normally P is around 13 to 18 for normal integrator pole errors. Now from Eq. (3.10) we find that if no addition truncation is performed the output $y(n)$ is M+P+2-bit long, which is not acceptable.

Fortunately, another decimator scheme, namely post-decimation compensation, can be used and is usually far superior to the pervious one. Since the decimation process of $\Delta\Sigma$ A/Ds is (at least at the present time) a linear time-invariant one, the order of decimation operation and multiplication operation can thus be inter-

changed, therefore the multiplication can be performed after the decimation. Figure 22 shows the block diagram of post-decimation compensation, where $H_1(z)$ and $H_2(z)$ are the original digital transfer functions in the modulators as shown in their block diagrams, and $H_c(z)$ is equal to z^{-1} for a first-order Leslie-Singh modulator and $z^{-1}(1-z^{-1})$ for high-order dual-quantization modulators discussed in this thesis.

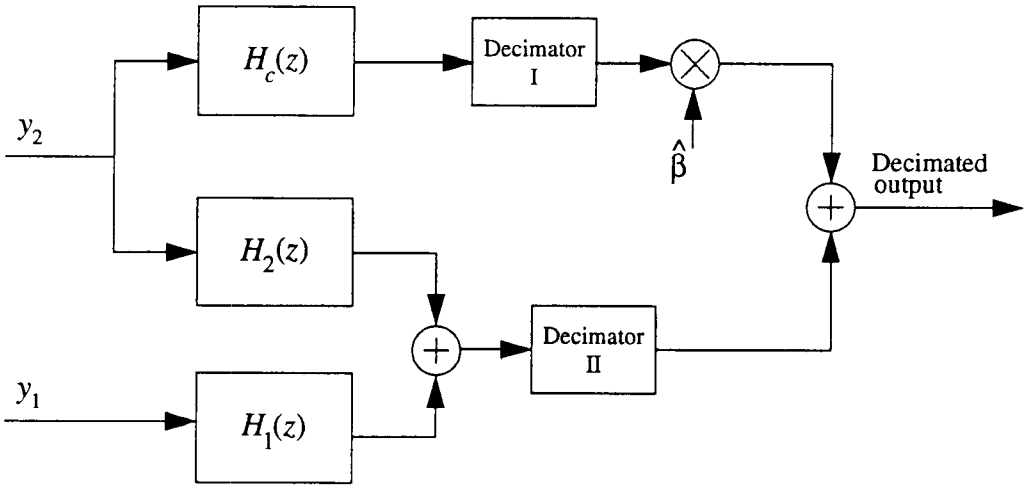

Figure 22. Block diagram of post-decimation digital compensation for integrator nonidealities in dual-quantization $\Delta\Sigma$ modulators

Because after decimation the clock frequency is much lowered, the implementation of multiplier is much easier and cheaper. Instead of implementing two separate decimators, it is much more efficient to implement a decimator which is twice as fast so that it can be shared to perform the decimation for the two data sequences. After examining the common structures of decimation filters, it is found that most of the area-consuming circuit elements such as multipliers, adders and ROM for storing the coefficient of decimation transfer functions etc. can be shared if the input and output data to them are properly multiplexed and demulti-

plexed. As a matter of fact, in audio-purpose $\Delta\Sigma$ A/Ds the decimation filter is usually shared between two channels anyway. Thus after adding some more control circuitry and some other circuit elements such as the input shift registers, multiplexers and demultiplexers etc., most parts of the decimator can be shared and a large chip area can be saved. Finally, another advantage of the post-decimation compensation is that the truncation of data is much easier to manage because no truncation before decimation is necessary.

Chapter 4. Off-line Estimation of Integrator Pole Errors in Dual-Quantization Delta-Sigma Modulators

As mentioned in Chapter 3, the idea of digital compensation is based on the assumption that the estimation of the integrator pole errors, which happen to be inversely proportional to the opamp DC gain of the integrators, is available. Although there is on-line estimation algorithm specially for the first-order Leslie-Singh modulator [4], it is quite complex and its extension to high-order cases is too complicated to be practical. Thus usually the estimation of the integrator pole errors can only be performed off-line during the calibration period, which is usually needed for offset cancellation purpose anyway. Thus if more than one integrator's pole error needs to be estimated, as in the case of high-order dual-quantization modulators, it can be done one by one.

The estimation method presented in this chapter fully utilizes the existing hardware in the dual-quantization $\Delta\Sigma$ modulators and thus is quite simple yet accurate. As shown in Figure 23, the required circuit contains basically one offset-compensated SC integrator, one comparator and one reference voltage equal to 3/4 V_{ref} (both are parts of a flash type multibit A/D converter), and a digital counter, all of which are usually needed in the modulator anyway. Another major advantage of this estimation method is that the estimation result is directly available in digital form, unlike common opamp gain measuring circuits which require the measurement of analog voltages. Because of these advantages, this method may be useful in other circumstances where the opamp DC gain measuring is necessary.

Shown in Figure 23 is the single-ended version of the estimation circuit, while the real circuit is going to be fully differential to reduce the clock feedthrough and other common-mode noises. C_{III} is charged to opamp offset voltage V_{os} in the precharge phase and will hold that voltage in the discharge phase,

thus the offset voltage is cancelled during the operation. Capacitors C_I and C_{II} serve as a voltage amplifier for V_y. As will be shown in the next section, this will both reduce the number of clock cycles needed for the discharge and overcome the problem of the small value of the amplitude of V_y to reduce the effect of clock feedthrough noise in the discharge phase. Other parts of the circuit are quite simple and self-explanatory.

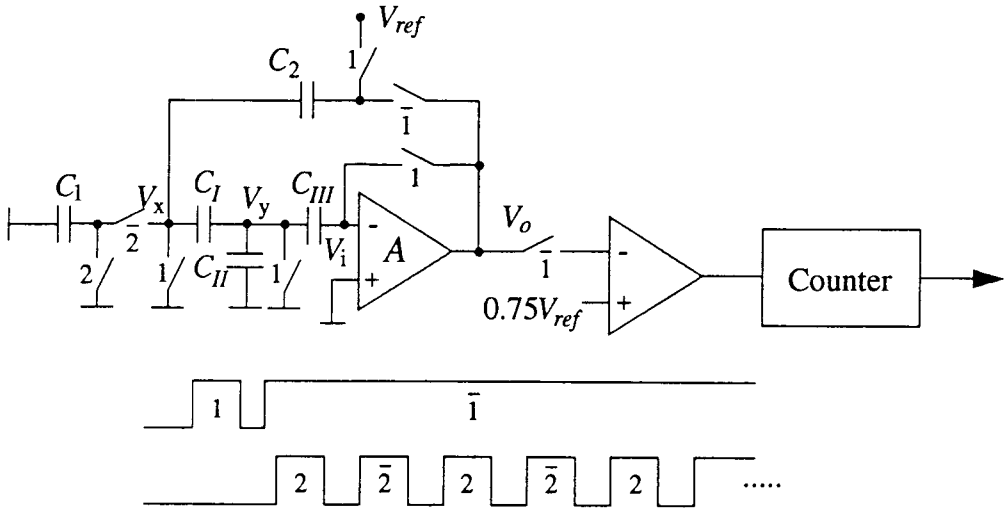

Figure 23. Single-ended version of the estimation circuit

The estimation method consists of three steps — a pre-charge phase, an initialization phase, a discharge phase, and a calculation phase, — which will be discussed one by one in the following sections.

4.1 Precharge Phase ($\Phi_1 = 1$)

In the precharge phase, all the switches labeled "1" are closed while the others remain open, thus C_2 is charged to V_{ref}, which is usually in the range of 3 to 5 volts, while C_I and C_{II} are completely discharged. Since the opamp output is connected to the inverting input of the opamp, C_{III} is charged to $V_i = V_{os}/(1+\mu) \approx V_{os}$, where $\mu = 1/A$.

4.2 Initialization and Discharge Phase ($\overline{\Phi_1} = 1$)

Next, as shown in Figure 23, when clock phase "1" goes low, C_2 is connected between the opamp output and the inverting input through C_I and C_{III}, while all other switches are open. This phase is called the initialization phase. As will be shown below, the opamp output voltage remains approximately V_{ref} during this phase. Since now the inverting input of the opamp is floating, any change in V_i will cause the same change in V_y. In other words,

$$V_i(n) - V_y(n) = V_i(0) - V_y(0) = V_{os}/(1+\mu). \tag{4.1}$$

Since no current is flowing through C_{III}, the current flowing through C_I and C_{II} are identical, thus

$$C_I \cdot (V_x(n) - V_x(n-1)) = (C_{II} + C_I) \cdot (V_y(n) - V_y(n-1)), \tag{4.2}$$

since $V_x(0) = V_y(0) = 0$,

$$V_x(n) = g \cdot V_y(n), \tag{4.3}$$

where $g = 1 + C_{II}/C_I$ maybe chosen in the range of 10-20. The amplitude of V_y is approximately the output of the opamp divided by the opamp DC gain, and thus is usually in the millivolts range. The amplitude of V_x, however, is amplified by g, and thus is in the tens of millivolts range.

From the law of charge conservation, the difference equation in the initialization phase can be obtained:

$$C_2(V_o - V_{ref}) = (gC_2 + C_{II})(-\mu)(V_o - V_{os}/(1+\mu)). \tag{4.4}$$

Thus the initial opamp output voltage can be found as

$$V_o = \frac{V_{ref} + (g+\kappa_{II}) \cdot \mu V_{os}/(1+\mu)}{1+\mu(g+\kappa_{II})} \approx V_{ref}, \tag{4.5}$$

where $\kappa_{II} = C_{II}/C_2$.

After the initialization is finished, Φ_2 goes high and low alternatively, and the C_2 gradually discharges through C_1 due to the opamp finite DC gain as shown in Figure 23. From the number of clock cycles it takes V_o to discharge from V_{ref} to 3/4 V_{ref}, we can estimate the integrator pole error, which is inversely proportional to the DC gain of the opamp in the integrator. The digital counter counts until the output of the comparator changes sign. As shown below, the number of cycles recorded in the counter, denoted by N, is the only data we need to estimate the integrator pole error. From the law of charge conservation, the output of the integrator during this phase (discharge phase) is

$$\kappa_1 g V_y(n) = V_o(n) - V_o(n-1) - (g+\kappa_{II}) \cdot \Delta V_y(n), \tag{4.6}$$

where $\kappa_1 = C_1/C_2$, which can be set to 1, while according to Eq. (4.1),

$$\Delta V_y(n) = V_y(n) - V_y(n-1) = -\mu (V_o(n) - V_o(n-1)). \tag{4.7}$$

Thus Eq. (4.6) becomes

$$V_o(n) = (1-\beta') \cdot V_o(n-1) + \mu \kappa_{os} V_{os}, \tag{4.8}$$

where

$$\beta' = \frac{\mu \kappa_1 g}{1+\mu\kappa'}, \tag{4.9}$$

$$\kappa_{os} = \frac{\kappa_1 g}{(1+\mu\kappa')(1+\mu)} \approx \kappa_1 g, \tag{4.10}$$

and

$$\kappa' = \kappa_{II} + g(1+\kappa_1). \tag{4.11}$$

Notice here β' is used to distinguish from the pole error β of the original integrator as given in Eq. (1.16). However, from Eq. (1.16) and Eq. (4.9) we see that there is a simple relationship between these two errors and thus once the pole error of the estimation integrator is obtained, the other one can be obtained very easily. From Eq. (4.9) we see that β' is about g times larger than β, the original integrator pole

error. If g is 10 and μ is around 0.001, β' is around 0.01.

The solution to Eq. (4.8) is

$$V_o(n) = (1-\beta')^n V_o(0) + \frac{1-(1-\beta')^{n+1}}{\beta'}(\mu\kappa_{os}V_{os}) \quad (4.12)$$

$$\approx (1-\beta')^n V_o(0) + (1-(1-\beta')^{n+1})V_{os}. \quad (4.13)$$

Thus the opamp output voltage will decay exponentially according to the above equation. As mentioned before, a digital counter records the number of clock cycles N for the output voltage to drop from V_{ref} to $0.75V_{ref}$, in other words,

$$V_o(N) = 0.75V_{ref}. \quad (4.14)$$

Since $V_o(0) \approx V_{ref}$, $V_{os} \ll V_{ref}$, and $N \gg 1$, the pole error can be obtained from Eq. (4.13) and Eq. (4.14) as follows

$$\beta' \approx 1 - \left(\frac{V_o(N)}{V_o(0)}\right)^{1/N} = 1 - e^{-\ln\frac{V_o(N)}{V_o(0)}/N} \approx \frac{\ln\frac{V_o(0)}{V_o(N)}}{N} \approx \frac{0.288}{N}. \quad (4.15)$$

Thus if β' is around 0.01, N is around 30.

4.3 Effects of Circuit Nonidealities on the Pole Error Estimation

The basic principle of the off-line estimation method introduced in last section is fairly simple. However, in real circuit implementations circuit nonidealities such as opamp offset, comparator offset, clock feedthrough and other noises, etc. must be considered. The effects of these nonidealities are discussed in this section.

4.3.1 Error in $V_o(0)$ and $V_o(N)$

As shown in Eq. (4.13)

$$\beta' \approx \frac{\ln V_o(0) - \ln V_o(N)}{N}, \quad (4.16)$$

thus the error in the initial opamp output voltage and the output voltage around

$0.75V_{ref}$ will both cause some error in the estimation. The relative error caused by these errors can be calculated as follows:

$$\frac{\Delta\beta'}{\beta'} \approx \frac{\frac{\partial\beta'}{\partial V_o(0)}\Delta V_o(0) + \frac{\partial\beta'}{\partial V_o(N)}\Delta V_o(N)}{\beta'} \tag{4.17}$$

$$\approx \frac{1}{\ln(\frac{4}{3})}\left(\frac{\Delta V_o(0)}{V_o(0)} - \frac{\Delta V_o(N)}{V_o(N)}\right) \approx 3.47\left(\frac{\Delta V_o(0)}{V_o(0)} - \frac{\Delta V_o(N)}{V_o(N)}\right), \tag{4.18}$$

where $\Delta V_o(0) = V_o(0) - V_{ref}$, and $\Delta V_o(N) = V_o(N) - 0.75V_{ref}$ are the absolute errors in the output voltage at clock period 0 and N respectively.

As shown in Eq. (4.5), the error in $V_o(0)$ caused by the opamp offset voltage is of the order of μV_{os}. This is in the microvolts range, and is thus negligible. Assuming $g + \kappa_{II} \approx 10$ and $\mu \approx 0.001$, the relative error in the initial voltage is about -1%. The resulting error in β' is -3.5%. If this error is not tolerable, it can be corrected during the calculation phase because $g + \kappa_{II}$ is known to the designer from the very beginning and after discharge phase, and the approximate value of μ is known as well. Thus with these two parameters, the error due to inaccurate initial voltage can be almost eliminated. The error in $V_o(N)$ is contributed by the error in the $0.75V_{ref}$ reference voltage, comparator offset, and the opamp offset as shown in Eq. (4.11) and the circuit noises, which will be discussed separately. The combined error due to the inaccuracy in dividing the reference voltage and comparator offset may be around 10mV, and from Eq. (4.11) we know the error in $V_o(N)$ due to V_{os} is approximately $0.25V_{os}$, around 2-4 mV. Assume a reference voltage of 3 volts, the relative error of $V_o(N)$ is around 0.5%, which causes about 1.9% error in the pole error estimation.

4.3.2 Errors due to Circuit Noises

The noises present in the circuit are clock feedthrough noise, opamp thermal noise, kT/C noise, and low frequency flicker noise. It is obvious that since the pre-charge phase only takes one clock cycle, the noise hardly affects the output voltage. However, according to Eq. (4.13) and (4.7), the discharge phase usually takes 20-60 clock cycles, and thus the output voltage error due to the circuit noises during the discharge phase may not be negligible.

In the discharge phase, the clock feedthrough noise, due to the fully differential circuit topology, is completely common-mode and will be mostly cancelled by the common-mode feedback. However, in the absence of voltage amplification provided by capacitors C_I and C_{II}, i.e., if C_{III} is connected to C_1 directly, the charge C_1 takes in each clock cycle is very small, roughly of the same order as the clock feedthrough charge injection. Thus the accuracy of the estimation must rely on the cancellation of the clock feedthrough noise. Using the voltage amplification as shown in Figure 23, V_x can be made much larger than V_y by making $g \gg 1$. Then the charge C_1 takes out each clock cycle is much larger and thus the cancellation of the clock feedthrough noise is much less critical than in the previous case. Also, as shown in Eq. (4.7) and (4.13), by making $g \gg 1$ we can reduce the number of clock cycles the output voltage takes to decay, which will greatly speed up the estimation also.

Next, we shall estimate the effects of the opamp input-referred noise. From the law of charge conservation, the output voltage due to the opamp input-referred noise is

$$V_{on}(n) = (1-\beta')\,V_{on}(n-1) + V_{n1}(n) + V_{n2}(n), \qquad (4.19)$$

where

$$V_{n1}(n) \approx \kappa_{II}\,(V_{in}(n) - V_{in}(n-1)), \qquad (4.20)$$

$$V_{n2}(n) \approx \kappa_1 (1+f)\,(V_{in}(n) - V_{in}(0)), \qquad (4.21)$$

while $V_{in}(n)$ is the opamp input-referred noise voltage at the nth clock cycle. From Eq. (4.18) and (4.19) it is obvious that due to the auto-zeroing offset compensation technique, any DC noise component will be completely cancelled and will not appear in the output, and at the same time, the low frequency flicker noise are greatly suppressed. However, the white noise sources such as opamp thermal noise is not cancelled or suppressed. Their effects are analyzed as the following.

From Eq. (4.17), the output noise at the Nth clock cycle due to $V_{n1}(n)$ is

$$V_{on1}(N) \approx \kappa_{II}\left(V_{in}(N) - \beta' \sum_{i=0}^{N-1} (1-\beta')^{N-i} V_{in}(i)\right). \qquad (4.22)$$

Suppose $V_{in}(n)$ is a white noise, the RMS value of the output noise at the Nth clock cycle due to $V_{n1}(n)$ is approximately $\sqrt{17}\kappa_{II}\sigma_i/4 \approx \kappa_{II}\sigma_i$, where σ_i is the RMS value of opamp input-referred white noise, which is usually around 10-50μV. Therefore its effect on the output voltage is negligible. The output noise at the Nth clock cycle due to $V_{n2}(n)$ is

$$V_{on2}(N) \approx \kappa_1 (1+f) \sum_{i=0}^{N-1} ((1-\beta')^{N-i} (V_{in}(i) - V_{in}(0))). \qquad (4.23)$$

Assuming $V_{in}(n)$ is a white noise, from Eq. (4.21) we find the RMS noise voltage in the output is approximately $\frac{\kappa_1 (1+f)}{4\beta'}\sigma_i \approx \frac{A\sigma_i}{4}$, where A is the opamp DC gain. Thus the RMS value of the output noise voltage may range from 1mV to 30 mV depending on the opamp DC gain and the RMS value of the opamp input-referred white noise voltage. This is mainly due to the integration of $V_{in}(0)$ as shown in Eq. (4.21), otherwise the RMS value of the output noise voltage is somewhere between $\sqrt{A}\sigma_i/4$ and $A\sigma_i/4$. Assuming a worst-case 30 mV RMS noise output, from Eq. (4.16) we see that the relative error in the estimation is around 4.5%. Thus a low noise opamp will help to achieve a high estimation accuracy. Another

solution to this problem is to perform the estimation for several times, since one estimation only takes tens of clock cycles, and then average the results to reduce to effect of random error caused by the opamp input-referred white noise.

The kT/C noise will also cause random error in the output voltage. First, in the discharge phase, kT/C noise will appear on C_1. It will cause an random error in the output voltage with a RMS value of $\sqrt{2\kappa_1 AkT/C_1}$, which is usually in the millivolts range and can usually be neglected. Second, in the precharge phase, kT/C noise will appear in V_x and V_y. This is equivalent to increase the RMS value of $V_{in}(0)$. It will cause a random error in the output voltage with a RMS value approximately equal to $\sqrt{kT/C_{II}} \cdot A/4$, which may range from 1mV to 10mV if C_{II} is around 10pF. Thus it may cause a 1.5% error in the pole error estimation. Again, if the overall error in the estimation can not be accepted, several estimations can be performed and the results can then be averaged to reduce the RMS value of the noise.

4.4 SWITCAP Simulation Results

SWITCAP simulation was performed to verify the functionality of the opamp gain measuring circuit shown in Figure 23. The circuit nonidealities included in SWITCAP simulation were the opamp offset voltage, capacitance mismatches, finite on-resistance of the switches, clock feedthrough of the MOS switches, stray capacitances, and finite common-mode rejection ratio (CMRR) of the opamp.

First, the effects of the opamp DC offset voltage were simulated. The results are shown in Figure 24. As predicted by Eq. (4.5) and Eq. (4.13), after using offset cancelling technique, the error in the opamp output voltage due to the opamp DC offset is in the millivolt range and is thus negligible. Eq. (4.15) can be used to cal-

opamp output voltage. This effect was simulated and the results are shown in Figure 25, where C_{is} is the stray capacitance associated with i node, and C_{xs} is the stray capacitance associated with x node.

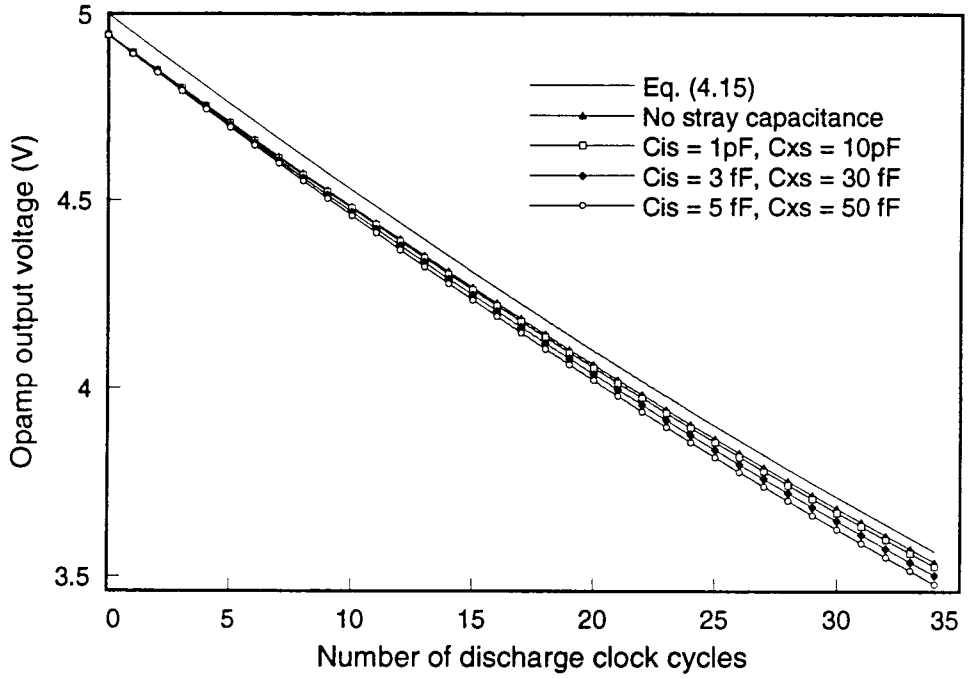

Figure 25. Effects of stray capacitances on the estimation accuracy

In the simulation, a 1% mismatch was assumed between symmetrical capacitors in the fully differential structure. The capacitances used in the simulation are: $C_1 = C_2 = 10$ pF, $C_I = 1$ pF, $C_{II} = 9$ pF (thus $g = 10$), and $C_{III} = 0.1$ pF. It can be seen from Figure 25 that the errors due to the stray capacitances are usually in the range of 5 to 50 mV around 3/4 V_{ref} (3.75 Volts), thus according to Eq. (4.18), the resulting relative error in the estimation is in the range of 0.3% to 4%. If it is a concern, the main capacitances can be made larger to reduce the effects of stray capacitances.

As mentioned before, clock feedthrough will also affect the accuracy of the estimation accuracy if the clock feedthrough noise is not completely common-mode. The simulation was performed for different gate and bulk capacitances and

different matching percentages between the switches. The switch model presented in SWITCAP Manual [10] was used, and a 4 KΩ on-resistance was assumed. Three simulations were performed and the results are shown in Figure 26. In the first simulation, a 10% mismatch between switches was assumed, and the assumed clock signal coupling capacitances of the switches were $C_{gs} = C_{gd} = 5$fF, and $C_{sb} = C_{db} = 50$ fF. In the second one, 20% mismatch, $C_{gs} = C_{gd} = 10$fF, and $C_{sb} = C_{db} = 100$ fF was assumed. In the third one, 30% mismatch, $C_{gs} = C_{gd} = 15$fF, and $C_{sb} = C_{db} = 150$ fF was assumed.

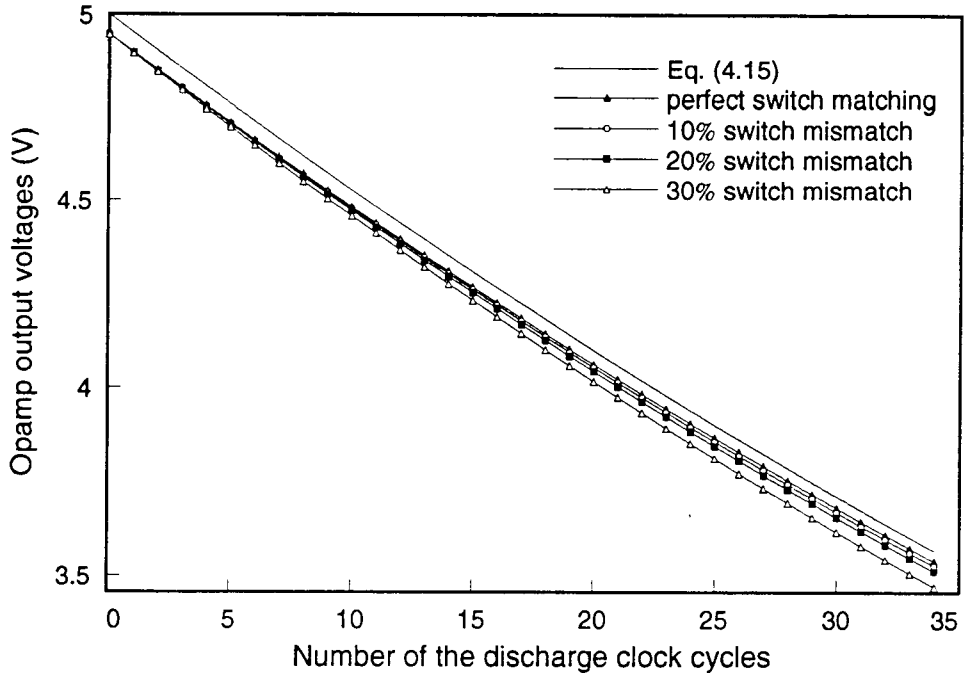

Figure 26. Effects of the clock feedthrough noise on the estimation accuracy

The simulation results show that unless the matching between the switches is very poor (more than 30% mismatch) and the sizes of the switches are big, the error caused by the clock feedthrough noise is smaller than 3%. Now the necessity of the voltage amplification of V_y (a factor of g provided by C_I and C_{II}) is obvious. If no voltage amplification is available, the requirement on the matching percentage between the transistors would be g times higher.

A final simulation with all the above nonidealities was performed as shown in Figure 27. The simulation shows an overall relative error of 10.4% with 1% capacitance mismatches, C_{is} = 50 fF, C_{xs}= 500 fF, CMRR = 70 dB, switch mismatch of 20%, $C_{gs} = C_{gd}$ = 10fF, and $C_{sb} = C_{db}$ = 100 fF in the switches. These parameters were picked randomly, and may not represent the actual design and nonideality parameters. In circuit implementation, after the nonideality parameters are available, the design parameters can be chosen accordingly to ensure an acceptable estimation accuracy. For example, if the effects of the stray capacitances are intolerable, larger capacitances can be chosen to reduce it.

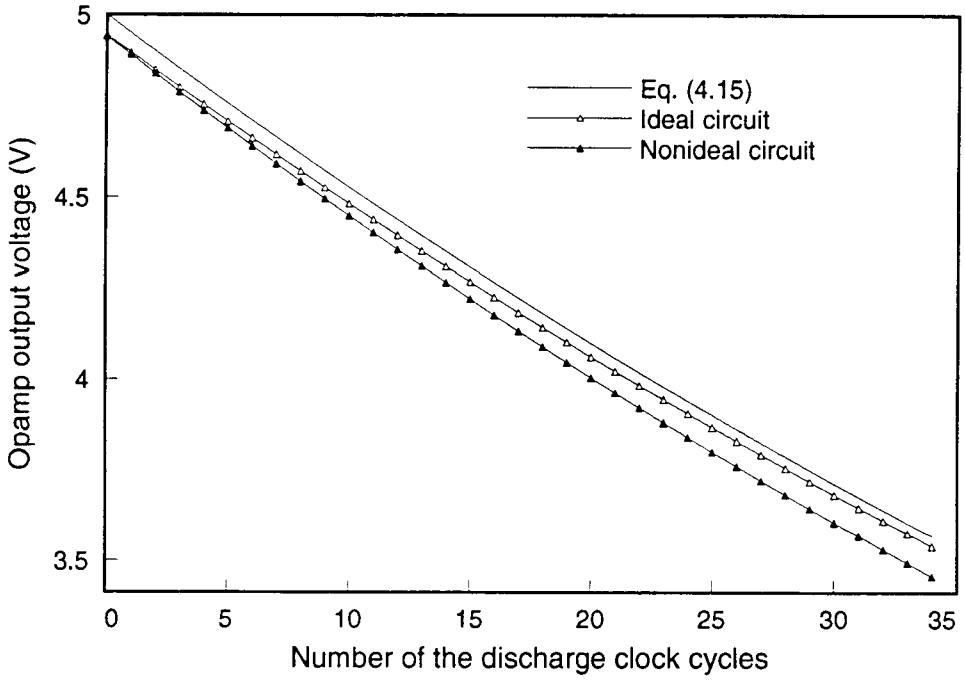

Figure 27. Effects of circuit nonidealities on the estimation accuracy

4.5 Calculation Phase

The estimation formula Eq. (4.13) requires an inverse operation which is costly to implement in digital circuitry. This problem can be solved by the combination of table-lookup method and linear interpolation.

The constant factor $\ln(4/3)$ or the capacitor ratios in Eq. (4.13) can be combined with the result of $1/N$ and stored in a ROM for each value of N. Notice that a ROM is usually necessary for the decimation filter anyway, and the overhead cost is not significant. Usually the estimation takes only 20-60 clock cycles, thus storing around 40 digital values in the ROM should not be a problem. If for some reason, the estimation takes many more clock cycles the linear interpolation method can be used. Suppose the values of $1/N$ are stored for $N_1 < N_2 < \ldots < N_m$, then any N can be interpolated between these base points as follows,

$$N = kN_x + (1-k)N_y, \tag{4.24}$$

where $0 < k < 1$, and $N_z < N_y$ are both base points. The relative error caused by replacing $1/N$ by $\frac{1}{\hat{N}} = \frac{k}{N_x} + \frac{(1-k)}{N_y}$, which can be obtained by table-lookup and simple multiplication, is

$$\frac{\frac{1}{\hat{N}} - \frac{1}{N}}{\frac{1}{N}} = \frac{k(1-k)\,(N_x - N_y)^2}{N_x N_y} \le \frac{(N_x - N_y)^2}{4N_x N_y}. \tag{4.25}$$

Thus even for N=70, the minimal spacing between consecutive base points can be as large as 8 if an 0.5% relative error is required. Notice that as N increases the spaces between base points increase dramatically, for example, for N larger than 500 the space between the base points can be as large as 100 for an 1% relative error! Also notice that if $N_x - N_y$ is the 2 to the power of an integer there is no division required in interpolation procedure.

From the above discussion we see that if carefully implemented, the off-line estimation method presented here can achieve an overall estimation error smaller than 10%, corresponding to a opamp DC gain estimation error less than 0.86 dB. Therefore a SNR around 20 dB can be recovered if the digital compensation is properly implemented.

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Appendices

Appendix 1. First-stage Leakage Noise Calculation of First-Order Leslie-Singh Modulator

Consider the situation when a white noise signal *ein* is passed through a general first-order NTF (with arbitrary delay) $H(z) = z^{-k}(c - dz^{-1})$. The base-band energy of the output noise e_{out} can be calculated as follows:

$$n_{out}^2 = \int_0^{w_b} |c - de^{-j\omega}|^2 \cdot |e^{-jk\omega}|^2 \cdot \frac{n_{in}^2}{\pi} \cdot d\omega \qquad \text{(A.1.1.)}$$

$$= n_{in}^2 \cdot ((c-d)^2 \cdot w_b + 2cd \cdot (w_b - \sin w_b)) \qquad \text{(A.1.2.)}$$

$$= \frac{n_{in}^2}{\pi} \cdot \left((c-d)^2 \cdot w_b + 2cd \cdot \left(\frac{w_b^3}{3!} - \frac{w_b^5}{5!} + \frac{w_b^7}{7!} - \ldots \right) \right). \qquad \text{(A.1.3.)}$$

In our case $w_b = \pi/OSR \ll 1$, thus

$$n_{out}^2 \cong n_{in}^2 \cdot \left(\frac{(c-d)^2}{OSR} + \frac{2cd \cdot \pi^2}{3! \cdot OSR^3} \right). \qquad \text{(A.1.4.)}$$

From Eq. (2.7) it can be shown that for an uncompensated first-order Leslie-Singh modulator, the leakage noise transfer function (LNTF)

$$LNTF(z) = NTF_1(z) - H_2(z) \qquad \text{(A.1.5.)}$$

$$\cong z^{-1} \cdot (-\alpha + (\alpha - \beta) z^{-1}). \qquad \text{(A.1.6.)}$$

Thus using Eq. (A.1.4.) the in-band leakage noise energy is

$$n_{leak}^2 \cong \sigma_{e_1}^2 \cdot \left(\frac{\beta^2}{OSR} - \frac{\alpha(\alpha - \beta)\pi^2}{3 \cdot OSR^3} \right). \qquad \text{(A.1.7.)}$$

For usual values of integrator gain and pole errors discussed in Chapter 1.3, it is obvious that the first term in the above equation is dominant if *OSR*>32, thus

$$n_{leak}^2 \cong \sigma_{e_1}^2 \cdot \frac{\beta^2}{OSR}. \qquad \text{(A.1.8.)}$$

Expressing n_{leak}^2 in dB, and noticing that the energy of the first-stage quantization

noise $\sigma_{e_1}^2$ is 1/3, Eq. (2.8) is easily obtained.

From Chapter 2.1 and 3.1, it can be shown that the first-stage LNTF of a compensated first-order Leslie-Singh modulator is

$$LNTF(z) = NTF_1(z) \cdot (H_1(z) + H_2(z)) - H_2(z) \qquad \text{(A.1.9.)}$$

$$= \frac{1-\hat{\beta}z^{-1}}{1+(a-b)z^{-1}}(1-bz^{-1}) - (1-\hat{b}z^{-1}) \qquad \text{(A.1.10.)}$$

$$\approx (1-bz^{-1})f - (1-\hat{b}z^{-1}), \qquad \text{(A.1.11.)}$$

where

$$\hat{b} = 1-\hat{\beta}, f = 1 - \frac{\beta-\hat{\beta}+\alpha}{1+\beta-\alpha} \approx 1-\alpha. \qquad \text{(A.1.12.)}$$

Thus Eq. (A.1.4.) can be used and

$$n_{leak}^2 \equiv \sigma_{e_1}^2 \cdot \left(\frac{(\hat{\beta}-f\beta)^2}{OSR} + \frac{\pi^2\alpha^2}{3 \cdot OSR^3} \right) \equiv \sigma_{e_1}^2 \cdot \frac{(\beta-\hat{\beta})^2}{OSR}. \qquad \text{(A.1.13.)}$$

Thus from Eq. (A.1.8.) and (A.1.13.), Eq. (3.3) can be easily obtained.

Appendix 2. First-stage Leakage Noise Calculation for High-Order Dual-Quantization Delta-Sigma Modulators

Consider the situation when a white noise signal *ein* is passed through a general second-order NTF (with arbitrary delay) $H(z) = z^{-k}(pz + q + rz^{-1})$. The base-band energy of the output noise e_{out} can be calculated as follows:

$$n_{out}^2 = \int_0^{w_b} \left|pe^{-j\omega} + q + re^{-j\omega}\right|^2 \cdot \left|e^{-jk\omega}\right|^2 \cdot \frac{n_{in}^2}{\pi} \cdot d\omega \qquad \text{(A.2.1.)}$$

$$= \frac{n_{in}^2}{\pi} \cdot \left((p^2 + q^2 + r^2) \cdot w_b + 2(pq + rq)\sin w_b + pr\sin 2w_b \right). \qquad \text{(A.2.2.)}$$

If $w_b = \pi/OSR \ll 1$, we get

$$n_{out}^2 \cong n_{in}^2 \left(\frac{(p+q+r)^2}{OSR} - \frac{(pq+qr+4pr)\pi^3}{3 \cdot OSR^3} \right). \qquad \text{(A.2.3.)}$$

2.1 Uncompensated Second-Order Leslie-Singh Modulator

It can be shown that the LNTF of a second-order Leslie-Singh modulator is

$$LNTF(z) = NTF_1(z) \cdot H_1(z) + (NTF_1(z) - 1) \cdot H_2(z) \qquad \text{(A.2.4.)}$$

$$= NTF_1(z) - H_2(z), \qquad \text{(A.2.5.)}$$

where $NTF_1(z)$, the NTF of the first-stage second-order modulator when there are gain and pole errors in the integrators, can be shown as

$$NTF_1(z) = \frac{(1 - b_1 z^{-1})(1 - b_2 z^{-1})}{(1 - b_1 z^{-1})(1 - b_2 z^{-1}) + a_2 z^{-1}(1 + a_1 - b_1 z^{-1})}. \qquad \text{(A.2.6.)}$$

Here $a_i = 1 - \alpha_i$, and $b_i = 1 - \beta_i$, i=1,2, while α_1 and α_2 are the gain errors of the first and second integrator respectively, β_1 and β_2 are the pole errors of the first and second integrator respectively.

Direct analysis of Eq. (A.2.5.) using Eq. (A.2.6.) is very complicated. Thus Eq. (A.2.6.) is simplified by assuming its denominator remains approximately constant in the band of interest as long as OSR is big enough and therefore the band of interest is narrow enough. For simplicity, we assume it takes its DC value $\beta_1\beta_2 + (1-\alpha_2)(1+\beta_1-\alpha_1) \approx 1+\beta_1-\alpha_1-\alpha_2$. This assumption is justified by the good agreement between the theoretical estimation based on it and the computer simulation results.

Thus Eq. (A.2.5.) becomes

$$LNTF(z) \cong (1-c)(1-b_1 z^{-1})(1-b_2 z^{-1}) - (1-z^{-1})^2 \qquad \text{(A.2.7.)}$$

where

$$c = 1 - \frac{1}{1+\beta_1-\alpha_1-\alpha_2} \approx \alpha_1+\alpha_2-\beta_1 \ll 1. \qquad \text{(A.2.8.)}$$

Thus using Eq. (A.2.3.) for the NTF shown in Eq. (A.2.5.), the in-band leakage noise energy is

$$n_{lk}^2 \cong \sigma_{e_1}^2 \cdot \left(\frac{P}{OSR} - \frac{Q \cdot \pi^2}{3 \cdot OSR^3} \right). \qquad \text{(A.2.9.)}$$

where

$$P = (1-c)^2 \cdot \beta_1^2 \cdot \beta_2^2 \approx \beta_1^2 \cdot \beta_2^2, \qquad \text{(A.2.10.)}$$

$$Q = -2c(1-c)\beta_1\beta_2 - (1-c)^2((\beta_1+\beta_2)^2 - \beta_1\beta_2(\beta_1+\beta_2))$$
$$\approx -(1-c)^2(\beta_1+\beta_2)^2 \approx -(\beta_1+\beta_2)^2. \qquad \text{(A.2.11.)}$$

For usual values of integrator gain and pole errors discussed in Chapter 1.3, it is obvious that the first term in the above equation is dominant as long as $OSR<300$ assuming the pole errors are smaller than 0.003 or opamp DC gains are above 50 dB. Thus the in-band leakage noise energy is approximately

$$n_{lk}^2 \approx \sigma_{e_1}^2 \cdot \frac{\pi^2(\beta_1+\beta_2)^2}{3 \cdot OSR^3}. \qquad \text{(A.2.12.)}$$

Expressing n_{lk}^2 in dB and noticing that the energy of the first-stage quantization noise $\sigma_{e_1}^2$ is 1/3, Eq. (2.12) is easily obtained.

2.2 Uncompensated Cascade 2-1 and 2-2 Modulators

From Chapter 2.3 it can be shown that the first-stage LNTF of a multibit cascade 2-1 modulator is

$$LNTF(z) = NTF_1(z)H_1(z) - STF_2(z)H_2(z), \qquad \text{(A.2.13.)}$$

where $NTF_1(z)$ is the NTF of the first-stage second-order modulator as shown in Eq. (A.2.6.), and $STF2(z)$, the STF of the second-stage first-order modulator, can be shown as

$$STF_2(z) = \frac{(1-\alpha_3)z^{-1}}{1+(\beta_3-\alpha_3)z^{-1}} \cong (1-d)z^{-1} \qquad \text{(A.2.14.)}$$

where

$$d = 1-(1-\alpha_3)/(1+\beta_3-\alpha_3) \approx \beta_3 \qquad \text{(A.2.15.)}$$

and α_3 and β_3 are the gain and pole errors of the second-stage integrator respectively. Again assuming the denominator of both $NTF_1(z)$ and $STF2(z)$ remains constant in the band of interest, we get

$$LNTF(z) \approx (1-d)z^{-1}\left((1-f)(1-b_1z^{-1})(1-b_2z^{-1}) - (1-z^{-1})^2\right) \qquad \text{(A.2.16.)}$$

where

$$f = 1-(1-c)/(1-d) \approx \alpha_1+\alpha_2-\beta_1-\beta_3 \ll 1, \qquad \text{(A.2.17.)}$$

and c is defined in Eq. (A.2.8.). Thus using Eq. (A.2.7.) to (A.2.12) in Appendix 2.1, it can be shown that

$$n_{leak}^2 \approx (1-c)^2 \cdot \sigma_{e_1}^2 \cdot \frac{\pi^2(\beta_1+\beta_2)^2}{3 \cdot OSR^3} \approx \sigma_{e_1}^2 \cdot \frac{\pi^2(\beta_1+\beta_2)^2}{3 \cdot OSR^3}, \qquad \text{(A.2.18.)}$$

and Eq. (2.14) can be easily obtained. It can be shown from Chapter 2.4 that the LNTF of the cascade 2-2 modulator is also in the form of Eq. (A.2.16), the only difference is that here f is different from the one shown in Eq. (A.2.17). Instead,

$$f = 1 - (1-c)/(1-d) \approx \alpha_1 + \alpha_2 - \beta_1 + \alpha_3 + \alpha_4 - \beta_3, \qquad \text{(A.2.19.)}$$

where in this case

$$d = 1 - \frac{1}{1 + \beta_3 - \alpha_3 - \alpha_4} \approx -\alpha_3 - \alpha_4 + \beta_3, \qquad \text{(A.2.20.)}$$

while α_3, α_4 and β_3, β_4 are the gain and pole errors of the second-stage two integrators respectively. However, since $f \ll 1$ the previous results can be duplicated, thus in-band leakage noise power of the cascade 2-2 modulator is approximately the same as that of the cascade 2-1 modulator, and Eq. (2.16) can be easily obtained.

2.3 Compensated Second-Order Leslie-Singh Modulator

It can be shown that after compensation, the LNTF of a second-order Leslie-Singh modulator is

$$LNTF(z) \equiv (1-c)\,(1-b_1 z^{-1})\,(1-b_2 z^{-1}) - (1-\hat{b}_1 z^{-1})\,(1-\hat{b}_2 z^{-1}), \qquad \text{(A.2.21.)}$$

where c is defined in Eq. (A.2.8.), and $\hat{b}_i = 1 - \hat{\beta}_i$, i=1,2. Thus Eq. (A.2.3.) can be used by replacing

$$p = 1 - c, \qquad \text{(A.2.22.)}$$
$$q = s - \hat{s} - c\,(2-s), \qquad \text{(A.2.23.)}$$
$$r = s - \hat{s} + c\,(1-s), \qquad \text{(A.2.24.)}$$

where $s = \beta_1 + \beta_2$, and $\hat{s} = \hat{\beta}_1 + \hat{\beta}_2$.

After some complicated calculation, it is found that

$$n_{lk}^2 \equiv \sigma_{e_1}^2 \cdot \left(\frac{P}{OSR} - \frac{Q \cdot \pi^2}{3 \cdot OSR^3} \right), \tag{A.2.25.}$$

where

$$P \approx \beta_1\beta_2 - \hat{\beta}_1\hat{\beta}_2, \tag{A.2.26.}$$

$$Q = c^2 s^2 + 2cs(s - \hat{s}) - (s - \hat{s})^2 \approx -(s - \hat{s})^2. \tag{A.2.27.}$$

For usual values of OSR and integrator pole errors the second term is usually dominant, and thus Eq. (3.5) can be obtained.

2.4 Compensated Cascade 2-1 and 2-2 Modulator

It can be shown that after compensation, the LNTF of a cascade 2-1 modulator is

$$LNTF(z) \approx (1 - d) z^{-1} \cdot G(z), \tag{A.2.28.}$$

where

$$G(z) = (1 - f)(1 - b_1 z^{-1})(1 - b_2 z^{-1}) - (1 - \hat{b}_1 z^{-1})(1 - \hat{b}_2 z^{-1}) \tag{A.2.29.}$$

and d and f are defined in Eq. (A.2.15) and (A.2.17) respectively. Since $I(z)$ takes the form of Eq. (A.2.21), and both d and f are much less than 1, the results in Appendix 2.3 can be used and thus the in-band leakage noise energy is

$$n_{lk}^2 \equiv (1 - d)^2 \sigma_{e_1}^2 \frac{(\beta_1 + \beta_2 - \hat{\beta}_1 - \hat{\beta}_2)^2}{3 \cdot OSR^3/\pi^2} \equiv \sigma_{e_1}^2 \frac{(\beta_1 + \beta_2 - \hat{\beta}_1 - \hat{\beta}_2)^2}{3 \cdot OSR^3/\pi^2}, \tag{A.2.30.}$$

the same as that of compensated second-order Leslie-Singh modulator.

For compensated cascade 2-2 modulator, the leakage NTF takes approximately the same form as that of cascade 2-1 modulator, except that d and f are defined in Eq. (A.2.20) and (A.2.19) instead. However, since $f \ll 1$ and $d \ll 1$, Eq. (A.2.30) still holds, and thus Eq. (3.9) is proved.