AN ABSTRACT OF THE THESIS OF

Tushar Uttarwar for the degree of Master of Science in Electrical and Computer Engineering

presented on November 21, 2011

Title: A Digital Multiplying Delay Locked Loop for High Frequency Clock Generation

Abstract approved:

Pavan Kumar Hanumolu

As Moore's Law continues to give rise to ever shrinking channel lengths, circuits are becoming more digital and ever increasingly faster. Generating high frequency clocks in such scaled processes is becoming a tough challenge. Digital phase locked loops (DPLLs) are being explored as an alternative to conventional analog PLLs but suffer from issues such as low bandwidth and higher quantization noise. A digital multiplying delay locked loop (DMDLL) is proposed which aims at leveraging the benefit of high bandwidth of DLL while at the same time achieving the frequency multiplication property of PLL. It also offers the benefits of easier portability across process and occupies lesser area.

The proposed DMDLL uses a simple flip-flop as 1-bit TDC (Time Digital Converter) for Phase Detector (PD). A digital accumulator acts as integrator for loop filter while a Δ-Σ DAC in combination with a VCO acts like a DCO. A carefully designed select logic in conjunction with a MUX achieves frequency multiplication. The proposed digital MDLL is taped out in 130nm process and tested to obtain 1.4GHz output frequency with 1.6ps RMS jitter, 17ps peak-to-peak jitter and -50dbC/Hz reference spurs.

A Digital Multiplying Delay Locked Loop for High Frequency Clock Generation

by

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A THESIS

Submitted to

Oregon State University

in partial fulfillment of

the requirements for the

degree of

Master of Science

Presented November 21, 2011

Commencement June 2012

Master of Science thesis of Tushar Uttarwar presented on November 21, 2011

APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Director of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Tushar Uttarwar, Author

ACKNOWLEDGEMENTS

I cannot thank my advisor Dr. Pavan enough for giving me an opportunity to work in his illustrious group for my MS Thesis. He has been unbelievably patient, generous and resourceful all along. If it was not for his encouragement and guidance, I would have never made it through. He is truly an expert in his field and working under him has been a great learning experience for me. I would also like to thank him for his timely help whenever I faced issues, be it weekends or late nights! His grasp on the subject is incredible and the passion he shows towards his research work is something everyone in their respective fields should strive to emulate. He will remain a role model for me in my future endeavors.

A very special thanks is due to Amr Elshazly for his amazing help with my Thesis work starting from the conception of idea to final testing in the lab and even during writing this Thesis. How he has so much energy and enthusiasm is beyond me! His constant support was really very helpful. I am also grateful to Rajesh Inti for always helping me out with my doubts and also for his considerable help during tape-out and testing. A big thanks to Mrunmay, Qadeer, Sachin, Brian and Seokmin for their constant help and insightful suggestions during my Thesis work. Working in this research group with such incredibly talented and experienced people was a truly rewarding as well as a humbling experience for me. I am also thankful to all my friends who made this journey in Corvallis very memorable and I apologize for not spelling out all of their names here. And lastly, I would like to dedicate this Thesis to my parents for being behind me all this while and encouraging me to pursue my dreams. No matter how bad things were, they always convinced me to have faith.

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1. INTRODUCTION

As CMOS technology has advanced due to Moore's Law of process scaling, on-chip clock multiplication has become a necessity for nearly all digital integrated circuits (ICs) in order to realize high speed clock signals from lower speed external sources such as crystal oscillators. The typical approach to achieve such clock multiplication is to employ a charge-pump phase-locked loop [1] (CPPLL) circuit consisting of a phase detector, analog loop filter, frequency divider, and voltage-controlled oscillator (VCO). Unfortunately, the analog component of PLLs prevents their design from simple compatibility with a typical digital design flow. There are other disadvantages of analog PLLs such as capacitive leakage, low supply voltage design issues, low-intrinsic gain, higher area due to integrating capacitor etc. Digital PLLs (DPLLs) [2, 3, 4] have been proposed to counter these problems and also to get easier design portability across process. Another advantage of a digitally-enhanced PLL is the ability of self-calibration to mitigate performance degradation due to process, voltage and temperature (PVT) variations. However, the low bandwidth of DPLL still remains an issue which leads to higher phase noise at the output. Moreover, DPLLs have higher deterministic jitter due to higher quantization noise.

Multiplying Delay-Locked Loops (MDLL) [5, 6, 7, 8] have been introduced recently as an alternative to PLLs for clock multiplication. MDLLs suppress the VCO phase noise more effectively than PLLs by periodically replacing the rotating edge with a clean reference edge. The effect of this operation is the suppression of the VCO phase noise at a bandwidth much higher than which is typically possible in PLLs. The cost of this advantage is that the reference must be clean, in addition to deterministic jitter that would occur if the reference edge does

not replace the rotating edge of the ring oscillator at exactly the right instant. This thesis proposes a digital MDLL which combines the benefits of a high-bandwidth MDLL as well as a digital PLL, to generate high frequency clock with very low jitter.

1.1 OVERVIEW OF PHASE LOCKED LOOP (PLL)

A basic block diagram of a PLL is shown in Fig. 1.1. It consists of a phase detector (PD), a loop filter (LF), a voltage-controlled oscillator (VCO) and a divider. The PD detects the phase difference between reference clock REF and feedback clock OUT and generates an output that is proportional to the phase difference. The LF filters the PD output and its output acts as a control signal of the oscillator which adjusts VCO output frequency FOUT. The divider in the feedback path divides down OUT to a lower feedback clock frequency FREF and achieves phase lock with FREF, therefore FOUT is N times larger than FREF.

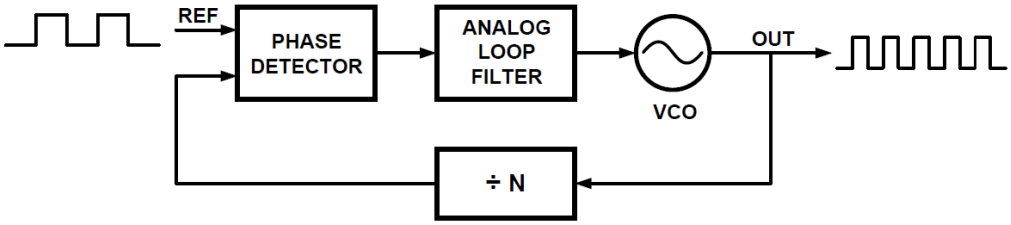

Figure 1.1.1 PLL Block Diagram

The CPPLL (Charge-Pump-PLL) is the most commonly used architecture in PLL designs. The block diagram of a charge-pump PLL is shown in Fig. 1.2. A phase and frequency detector (PFD) compares the frequency and phase difference between FREF and FV and then provides information about phase or frequency difference through UP and DN outputs. The charge pump (CP) injects the charge into or out of the loop filter capacitor. If the CP receives an UP

signal, current is driven into the LF. Conversely, if it receives a DN signal, current is drawn from the LF. The combination of CP and LF is an integrator that generates an average value proportional to phase error. Based on the average control voltage, the VCO oscillates at a higher or lower frequency, which affects the phase and frequency of the feedback clock. The VCO stabilizes once FREF and FV have the same phase and frequency. The LF filters out jitter by removing glitches from the CP.

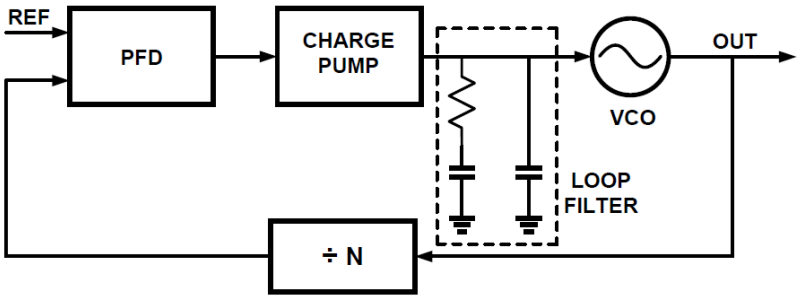

Figure 1.1.2 CPPLL Block Diagram

An alternative to CPPLL is a Digital PLL (DPLL). The simplified block diagram of a DPLL is shown in Fig. 1.3. The PD in analog PLL is replaced with a time-to-digital converter (TDC) that converts the phase difference into digital output. A bang- bang phase detector (BBPD) that is implemented by a simple D flip-flop (DFF) is a 1bit TDC. The digital output of TDC is filtered by the digital loop filter (DLF) and then given to control the input bits of a digitally-controlled oscillator (DCO). Using a digital-to-analog converter (DAC) in front of a VCO to convert digital input to voltage or current is one way to design a DCO.

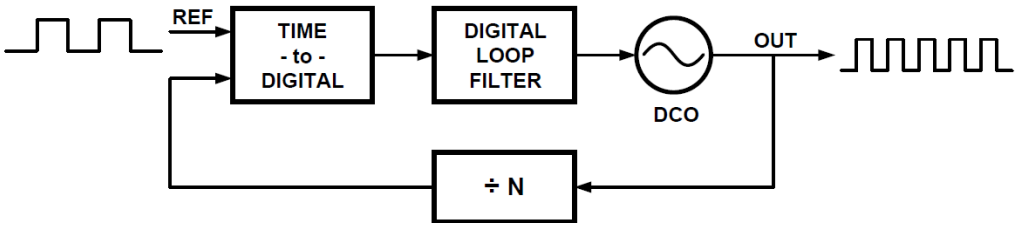

Figure 1.1.3 DPLL Block Diagram

When evaluating the performance of a phase-locked loop, jitter is one of the most important factors. Phase Noise is an essential parameter which determines root-mean-square (RMS) jitter. The phase noise spectral density of a PLL system refers to the noise power of the PLL versus the offset frequency. Close to the carrier, within the loop bandwidth of the PLL, this noise is commonly dominated by the PD, and farther out, it is typically dominated by the VCO. The PLL loop bandwidth is often chosen as high as possible to minimize RMS phase error contributed by VCO. But to maintain stability over process and temperature extremes, the PLL loop bandwidth cannot be more than (1/20) times the reference frequency [1].

Deterministic Jitter (DJ) is another jitter contributor in PLL, which mainly comes from reference spurs, loop delay, quantization error, mismatch etc. Reference spurs are spurious tones that occur from the carrier frequency at an offset equal to the reference frequency. These are usually caused by leakage and mismatch in the charge pump of a CPPLL. The loop latency causes delay in DPLL loop response and dithering jitter at the output. Quantization error usually exists in the digitally-assisted PLL that is aggravated by the finite resolution in digital circuits.

1.2 OVERVIEW OF MULTIPLYING DELAY LOCKED LOOPS

Efforts have been made to improve the phase noise performance of the PLL using different DLL based techniques in order to reduce RMS jitter. One of those techniques [5] involves using an edge-combiner block in a DLL to get frequency multiplication as shown in Fig 3.1. This technique takes the benefit of the high bandwidth of DLL (=FREF) which leads to superior phase noise performance compared to PLL. However, it has some critical issues in that it

needs perfect matching of all the delay cells as any mismatch will result in Deterministic Jitter in the output. Moreover, for frequency multiplication, the number of delay cells required is equal to the multiplication factor which leads to higher power and area.

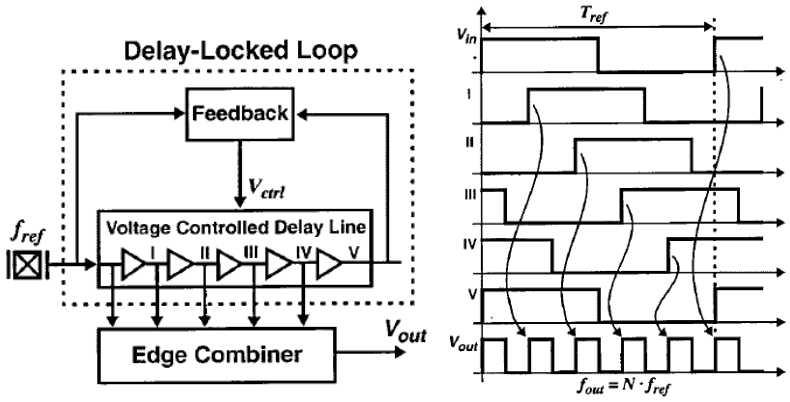

Fig 1.2.1 DLL-based frequency multiplier block diagram and concept [5]

Other techniques explored include Realigned PLL (RPLL) [6] as shown in Fig 1.2.2 and analog Multiplying DLL (MDLL) [7] as depicted in Fig 1.2.3. In both cases, control logic is designed in order to achieve frequency multiplication. Every M-th cycle, clean Reference edge is inserted into the VCO in order to reset jitter accumulation. This achieves higher bandwidth needed for better phase noise performance. However, implementation issues lead to deterministic jitter which worsens the total jitter specification on the output. Also, as mentioned earlier, limitations of analog PLL like loop filter area and capacitive leakage hold true for analog MDLL as well. A first attempt towards digital MDLL [8] was made in which a complex power-hungry GRO TDC chip was used as a Phase-Detector for the MDLL core chip, to reduce quantization noise. It also used multiple different things like FPGA board and external DAC & RC filter to achieve good jitter performance. This thesis work proposes a single chip digital MDLL.

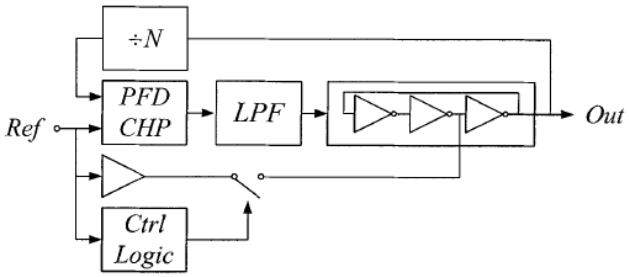

Fig 1.2.2 Realigned PLL Block Diagram [6]

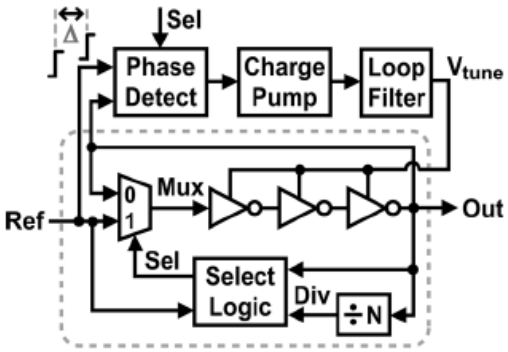

Fig 1.2.3 Analog MDLL Block Diagram [8]

2. PROPOSED MDLL ARCHITECTURE

Fig 2.1 shows the proposed Digital MDLL (DMDLL). Here Sense Amplifier Flip-Flop (SAFF) acts as a Phase Detector (PD) or a simple 1-bit TDC (Time-to-Digital-Converter). It gives out '+1' or '-1' output based on whether the REF edge is lagging or leading the OUT edge, respectively. The digital accumulator (ACC) acts as loop filter (integrator). ACC output is given to the DCO (Digitally Controlled Oscillator) which consists of a Δ-Σ DAC providing control voltage (V_{CTRL}) to the delay-cells. The select logic (SEL) is designed so that every N-th cycle SEL signal goes to VDD for a short-duration during which the clean Ref edge is inserted into the DCO through the MUX. Extreme care has to be taken to ensure that the process of this Ref edge insertion is accurate as otherwise it will lead to reference spurs in the output.

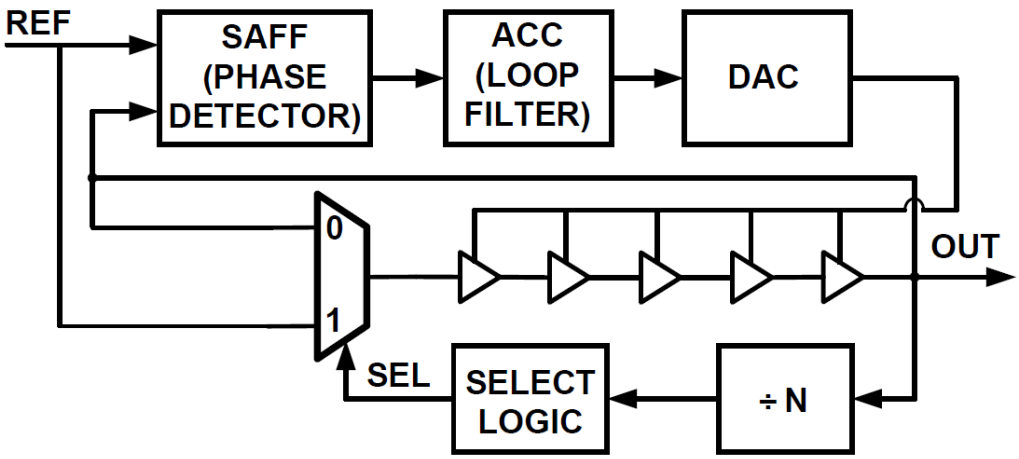

Fig 2.1 Proposed Digital MDLL

Following subsections will elaborate upon the process of phase noise suppression achieved by this MDLL in order to decrease RMS Jitter (RJ) as well design choices made for minimizing Deterministic Jitter (DJ).

2.1 PHASE NOISE SUPPRESSION USING MDLL

MDLL is a special case of Realigned PLL (RPLL) where β=1. As illustrated in [6], RPLL phase noise model is compared with that of conventional PLL in Fig 2.1.1 and 2.1.2. There are two notable differences in the form of H_{rl} and H_{up} defined as follows:

$$H_{rl}(jw) = 1 - \frac{\beta}{1 + (\beta - 1)e^{-jw\,T_r}} * e^{-jw\,T_r/2} * \frac{\sin\left(\frac{wT_r}{2}\right)}{\frac{wT_r}{2}}$$

$$H_{up}(jw) = \frac{N\beta}{1 + (\beta - 1)e^{-jw\,T_r}} * e^{-jw\,T_r/2} * \frac{\sin\left(\frac{wT_r}{2}\right)}{\frac{wT_r}{2}}$$

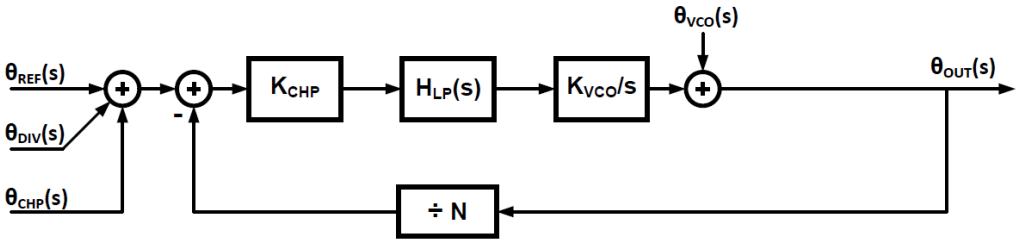

Fig 2.1.1 Phase Noise Model of a Conventional Integer-N PLL [6]

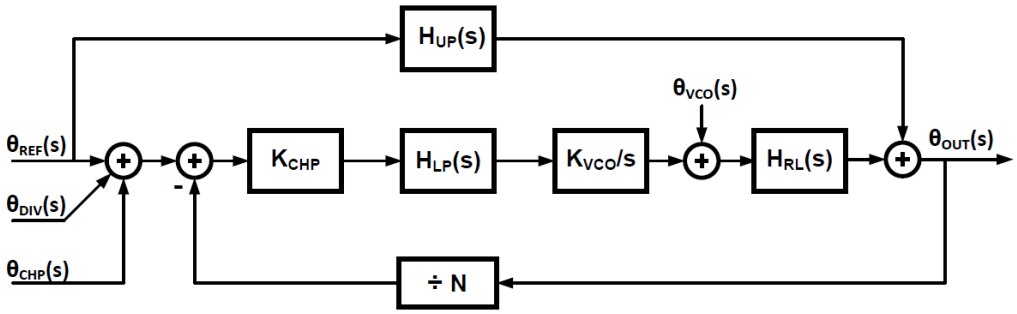

Fig 2.1.2 Phase Noise Model of a Realigned PLL [6]

H_{rl} represents the phase realignment effect while H_{up} represents the up conversion of input reference noise to the VCO output. As can be seen from the plots in Fig 2.1.3 and Fig 2.1.4, MDLL offers a high bandwidth low-pass frequency response for reference noise while it provides high-pass response for VCO phase noise. So reference should be clean in MDLL so that it can offer superior phase noise response (compared to PLL). It should be noted that β=0 corresponds to the case of PLL and clearly MDLL with β=1 has a much better phase noise response than PLL as seen in Fig 2.1.5.

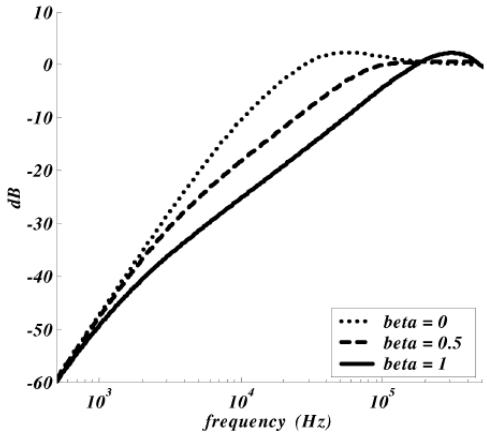

Fig 2.1.3 VCO NTF Frequency Response [6]

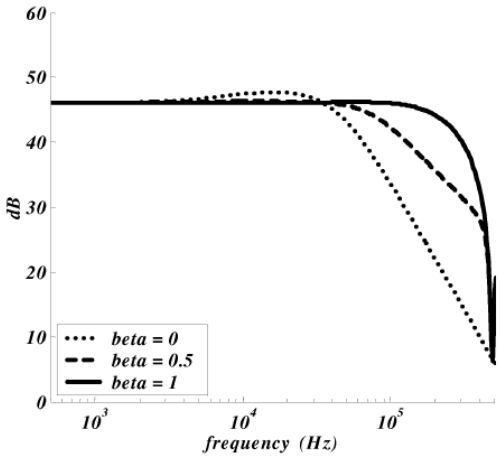

Fig 2.1.4 H_{up} frequency Response [6]

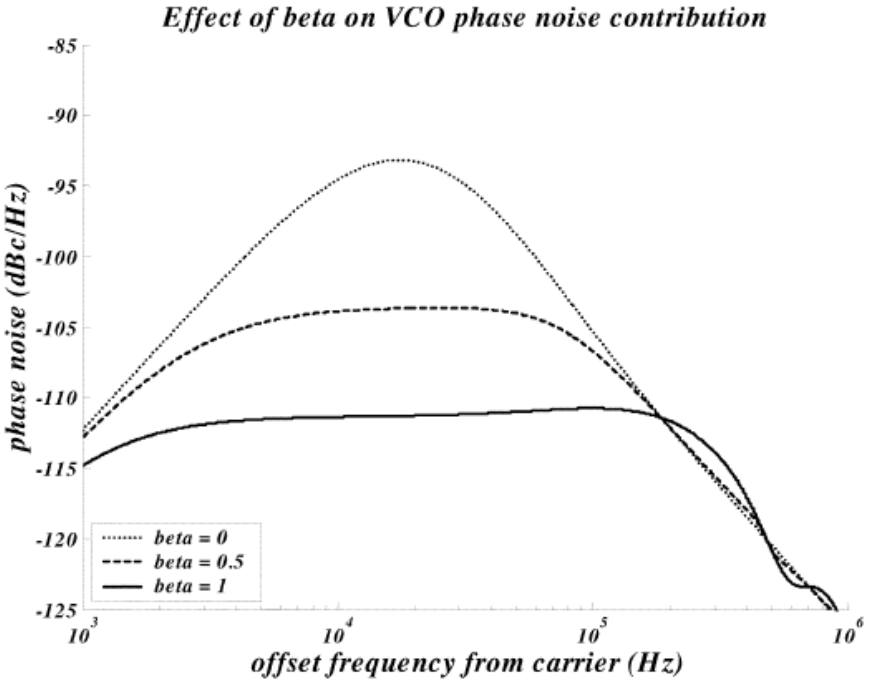

Fig 2.1.5 Phase Noise Filtering by RPLL [6]

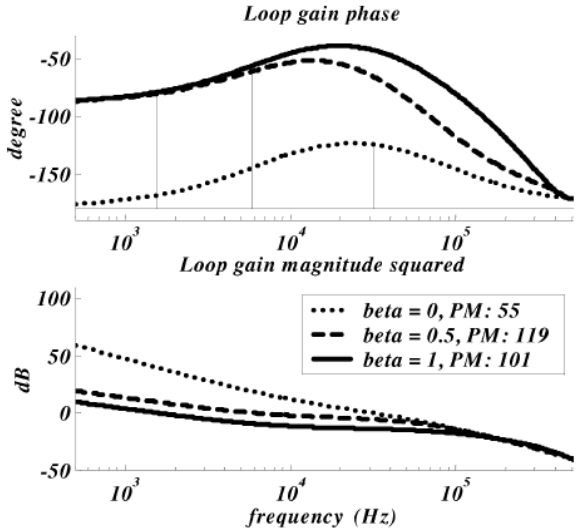

Fig 2.1.6 Effect of Beta on Loop Gain [6]

2.2 QUANTIZATION NOISE IN DIGITAL MDLL

Phase noise of the DCO is the major contributor of random noise in a Digital PLL while TDC contributes quantization noise due to its finite resolution. It can be shown that the NTF (Noise Transfer Function) from TDC to the DPLL output is low-pass while for DCO it is high-pass. As shown in Fig 2.2.1, there is a trade-off between filtering noise from DCO and TDC. Usually in DPLLs, quantization noise from TDC is the major contributor of deterministic jitter and hence, the loop bandwidth is chosen to minimize this source of jitter. Thie results in low DPLL bandwidth which causes less filtering of DCO phase noise resulting in more random jitter in DPLL output. However, in our proposed Digital MDLL, the phase noise of the DCO is filtered by the MUX resetting action and hence, as long as the loop is stable, we get the same filtering response irrespective of the loop bandwidth. In fact, as shown in Fig 2.1.6, with a beta=1 (RPLL as MDLL), the loop bandwidth is much lower than that for beta=0 (RPLL as PLL). It can also be seen that the loop is more stable for MDLL as it has a much higher phase margin.

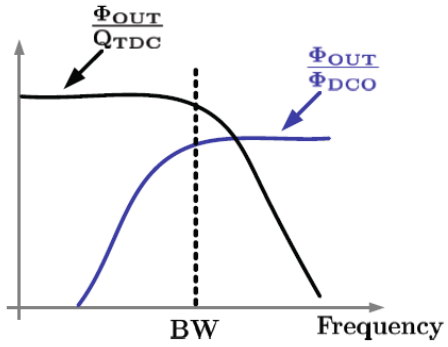

Fig 2.2.1 Noise Bandwidth Tradeoff in Digital PLL

Another source of deterministic jitter in the DMDLL is due to loop latency and limit cycling due to bang-bang nature of SAFF-based PD. In order to counter these issues, we drop 4 LSBs of the ACC output and use the remaining 14 MSBs for DSM. This doesn't lead to any change in the DAC resolution and helps in minimizing deterministic jitter. The only minor penalty is in the form of marginally more area and power of the 18-bit ACC as against 14-bit ACC.

3. CIRCUIT DESIGN

As shown in Fig 2.1 and Fig 3.1, our proposed DMDLL has the following blocks: SAFF (Sense Amplifier Flip-Flop) as Phase Detector, ACC as Integrator, Δ-Σ DAC based DCO, Select Logic, Divider (N=32) and MUX. This chapter discusses these different blocks and the circuit design involved.

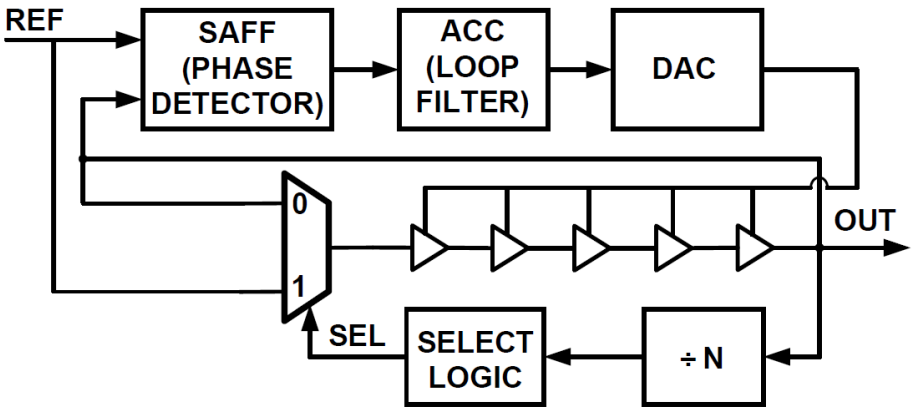

Fig 3.1 Proposed MDLL Architecture

3.1 PHASE DETECTOR

Flip-flop acts as a PD and for our purpose a SAFF (Sense-Amplifier Flip-Flop) [9] is used to minimize the set-up time induced phase error. Fig 3.1.1 shows the schematic of the SAFF. The SAFF consists of the SA in the first stage and the slave set-reset (SR) latch in the second stage. The SA stage provides a negative pulse on one of the inputs to the SR latch (S or R) depending whether the output is to be set or reset. It senses the true and complementary differential inputs and produces monotonic transitions from one to zero logic level on one of the outputs, following the leading clock edge. Any subsequent change of the data during the active clock interval will not affect the output of the SA.

The SR latch in the second stage captures the transition and holds the state until the next leading edge of the clock arrives. After the clock returns to inactive state, both outputs of the SA stage assume logic one value. Therefore, the whole structure acts as a flip-flop. Fig 3.1.2 shows the transfer characteristic of the SAFF. The reason for flattening or 'dead-zone' near zero phase error is due to metastability window of the flip-flop and also because of the fact that reference clock has some finite jitter. This dead-zone is the reason behind finite resolution of SAFF and leads to quantization noise.

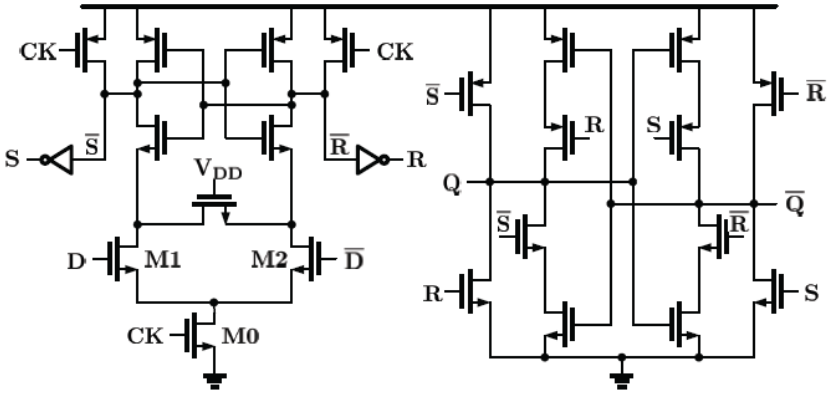

Fig. 3.1.1 Sense Amplifier Flip-Flop Schematic

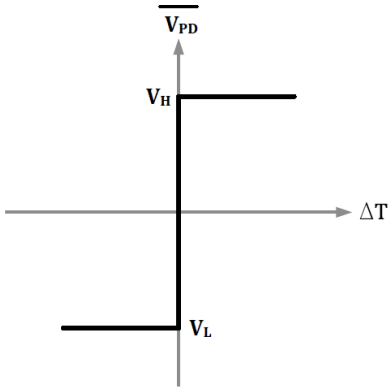

Fig. 3.1.2 Transfer Characteristic of SAFF

3.2 SYNTHESIZED DIGITAL BLOCKS

As MDLL is a first order system, it only needs an integrator in the loop filter. The simplest form of integrator in digital domain is an accumulator (ACC) which is driven by the PD in our implementation. ACC increments by 1 for every S=1 and decrements by 1 for every R=1 of the SAFF. Due to this bang-bang nature of SAFF and latency in the loop, there is limit-cycle on the ACC output in which the output of the ACC toggles between a minimum and maximum value as show in Fig 3.2.1. This leads to unnecessary deterministic jitter and in order to reduce this, we drop 4 LSBs of the 18-bit ACC before connecting it to the DSM (Delta-Sigma-Modulator).

DSM is a 2^{nd} order 14-bit modulator and is also obtained from synthesis like ACC. The 4-bit binary output resulting from truncation of the 14-bit digital input by the DSM drives a 15-level thermometer coded current-mode DAC as can be seen in Fig 3.2.2. The block diagram of the delta-sigma modulator is shown in Fig 3.2.3. A second order error feedback architecture is used to feed the quantization error back to the input through a simple loop filter implemented by two delay elements. In this implementation, the noise transfer function $(1 - z^{-1})^2$ with two zeros at DC is achieved by co-effcients that are multiples of 2, thereby obviating the need for a multiplier. The input to the DSM is a 14-bit word and it and generates 4-bit output. The in-band quantization error at the output of a DSM greatly depends on the over-sampling ratio (OSR). Defining OSR as the ratio of the clock frequency FREF to the LPF bandwidth, it can be easily seen that OSR scales linearly with FREF. For this design, LPF is a 2^{nd} order RC filter with R=100KOhm and C=3.2pF.

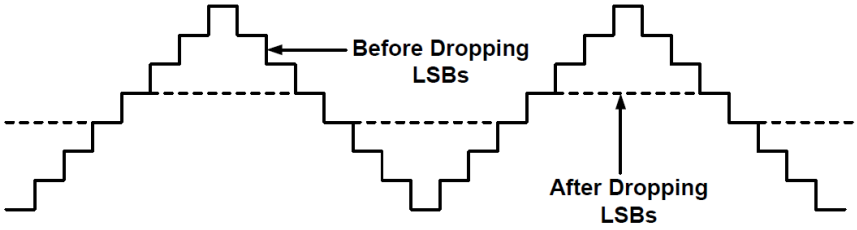

Fig 3.2.1 Limit Cycle in MDLL

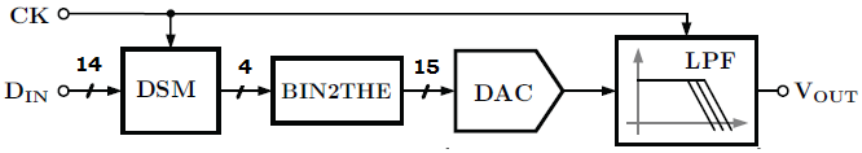

Fig 3.2.2 Digital to Analog Converter

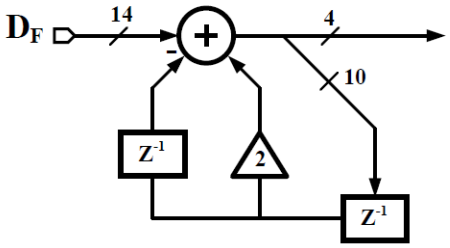

Fig 3.2.3 Delta Sigma Modulator

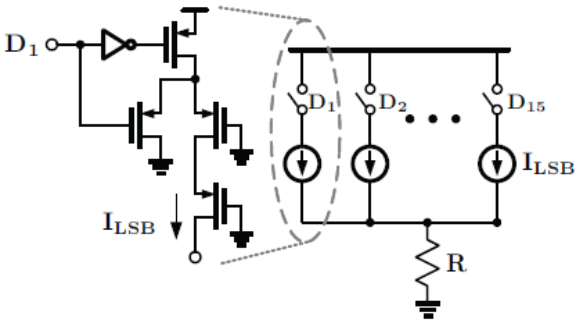

Fig 3.2.4 DAC Current Element

3.3 MULTIPLEXED VCO

Fig 3.3.1 shows a multiplexer (MUX) combined with a 5-stage ring oscillator acting as MUX-ed VCO in the proposed DMDLL. As mentioned earlier, the main reason for phase noise suppression in MDLL is the resetting action of MUX. The accumulated jitter of the VCO is reset after every N cycles by the clean REF edge insertion by MUX. This process of REF edge insertion using Select logic will be discussed in the next section. Fig 3.3.2 shows MUX schematic in which transmission gates (TG) are used. Care must be taken to make sure that the path delay for both VCO edge and REF edge through the MUX must match as otherwise it will lead to deterministic jitter.

Fig 3.3.2 also shows the Kim-Lee delay cell [14] used in each of the 5 stages of the ring oscillator. The cross-coupled pMOS transistors guarantee the differential operation of the delay cell without a tail-current bias. The two main reasons for choosing this kind of delay cell is: 1) Rail-to-rail swing and 2) Differential behaviour. MUX passes VCO edge every cycle except the Nth cycle when it passes the REF edge. So voltage swing of REF and VCO must match as otherwise it will lead to deterministic jitter. Moreover, the MUX should pass the edge with minimum delay and without any distortion and these requirements can be met if the swing is rail-to-rail. Also, differential nature of the delay cells help in improving supply-noise response.

An important design consideration of the multiplexed ring oscillator is to match the slope of the edges of the two inputs feeding into the multiplexer, which correspond to the output of the last delay cell and the reference input, in order to minimize deterministic jitter [11]. In

addition, care must be taken to avoid influence of the SEL signal on the edges running through the multiplexer since such influence would also lead to increased deterministic jitter [12]. To deal with the first issue, the reference input signal is buffered using two delay cells that are identical in design and tuning to the oscillator delay stages, as shown in Fig 5.3.1. Each of these delay stages are placed in close proximity to each other in the chip layout in order to achieve good matching between them. As for the second issue, the impact of SEL is sought to be minimized by striving for fast edges going through the multiplexer [12] so that there is a smaller time window for SEL to influence them. To this end, the number of delay cells is chosen to be as large as possible while still supporting the desired frequency range of the oscillator, which leads to less delay per stage and, therefore, faster edges. It should be noted that increasing the number of delay stages does not have a significant impact on phase noise [13]. In this 0.13 um CMOS design, the choice of five delay stages allows oscillation frequencies high enough to achieve our 1.6 GHz target with a comfortable design margin. Edges going in and out of the multiplexer are kept sharp by eliminating external loading on its input and output. Differential load balancing in the oscillator delay stages produces a more symmetric waveform, and thus, lowers 1/f noise [13]. To achieve that goal, care was taken to provide matching loads for all delay cells. Proper design of the multiplexer is required to avoid mismatch between the Out and Ref edges while they pass through it. This issue is especially problematic for architectures like ours which detects the error by comparing the edges of the two multiplexer inputs since the measurement circuitry will not be able to detect any error due to path mismatch in the multiplexer which occurs after the observation nodes.

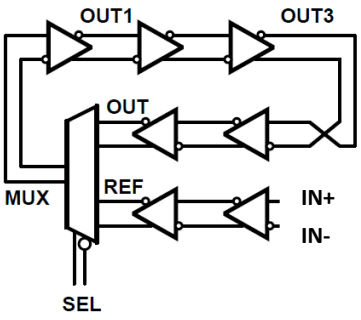

Fig 3.3.1 MUX-ed VCO

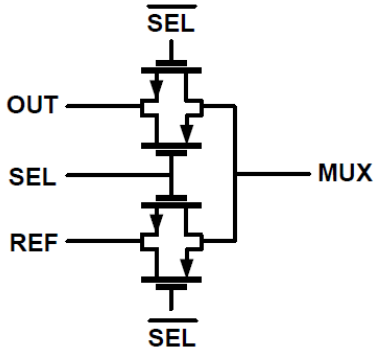

Fig 3.3.2 Multiplexer

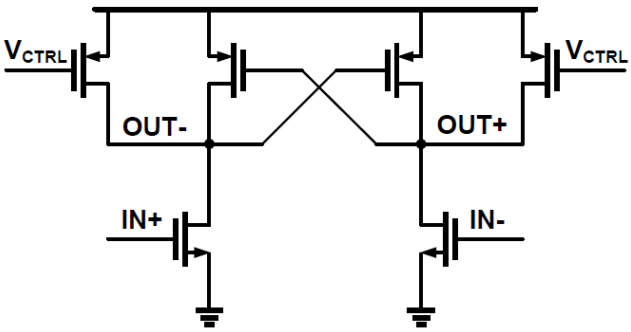

Fig 3.3.3 Kim-Lee Delay Cell

3.4 SELECT LOGIC

The select logic is a key element of this MDLL in order to minimize deterministic jitter. Its job is to pulse the REF edge every N cycles so that VCO jitter accumulation can be reset at a bandwidth close to FREF/3 as against FREF/20 in conventional PLLs. The select logic used here is similar to the one used in [8] and is shown in Fig 3.4.1.

The select logic circuit and its timing diagram are illustrated in Fig 3.4.1. The main goal of this block is to generate a select signal, SEL, with sharp edges that are sufficiently separated in time from the falling OUT and the rising REF edges, such that the SEL signal edges fall in approximately the middle of the ring oscillator transitions. This is important in order to minimize the influence of multiplexing on the edges passing through the multiplexer around the time of its switching, and reduce the effect of multiplexing nonidealities, e.g. charge injection and the feedthrough from the SEL signal.

In normal operation, the select logic is enabled (by pulling the signal MODE high), and the select signal is generated as follows: the last falling edge of OUT3 (before multiplexing REF) causes the divider output, DIV, to rise and trigger a TSPC D flip-flop with reset (DFFR), which allows the NAND gate and the subsequent inverter to generate a rising SEL edge after a rising OUT1 edge. The falling OUT1 edge, which occurs after the REF edge is passed, causes SEL to fall and resets the DFFR (when MODE is high) to make it ready for the next select cycle. The signal OUT1 is specifically chosen to drive the select logic in order to guarantee that the multiplexer switches at a time that is approximately in the middle of the OUT transition, or specifically, after the edge has fully passed the multiplexer. This design alleviates the

challenge of optimal positioning of the SEL signal as posed in [11], in addition to providing large timing margins that enhance its robustness. However, for a much higher output frequency or for slower processes, it might be necessary to reevaluate the retiming budget and the choice of the oscillator branch that drive the divider. In that case, it must be made sure that the multiplexer is completely switched before the rise of the last OUT edge at the highest target frequency of the oscillator.

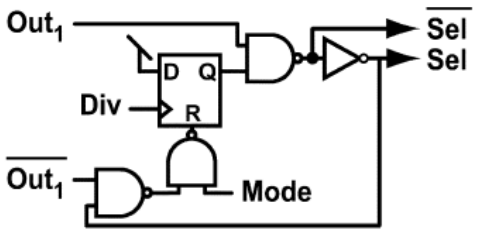

Fig 3.4.1 SELECT Logic Block

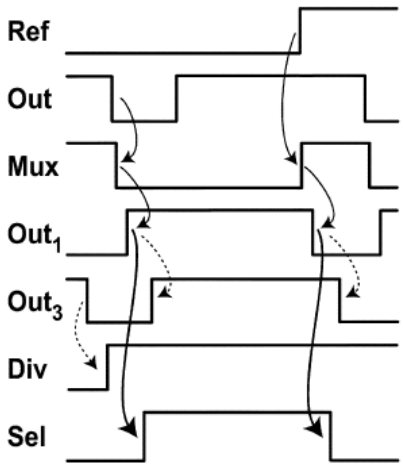

Fig 3.4.2 SELECT Logic Timing Diagram

3.5 DIVIDER

The divider used in this MDLL divides the output by 32 by using 5 TSPC flip-flops connected in series. Fig 3.5.1 shows the divider block while Fig 3.5.2 shows the TSPC flip-flop schematic. The primary reason for using TSPC (True-Single-Phase-Clock) flip-flop [10] is that it consumes lower power as compared to SAFF.

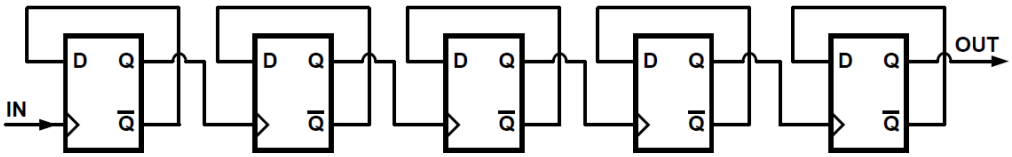

Fig 3.5.1 Divider Using TSPC Flip-Flop

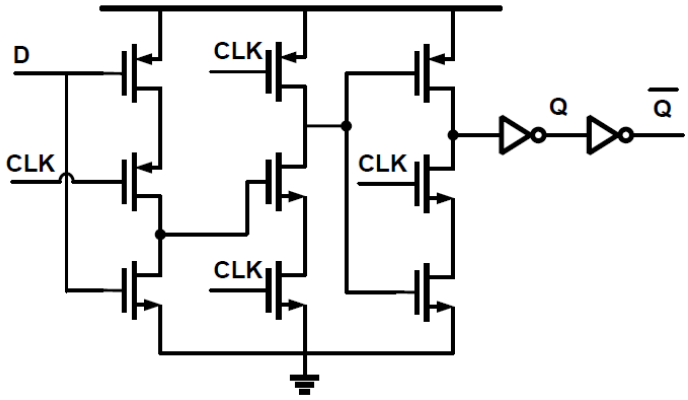

Fig 3.5.2 TSPC Flip-Flop Schematic

4. CHIP RESULTS:

Fig 4.1 shows the die photo of the prototype Digital MDLL and it can be seen that it occupies only 250um X 300um (0.075 mm^2). Fig 4.2 shows the set-up used for testing the prototype. To evaluate the overall jitter performance, Tektronix DSA8200 serial analyzer is used while the reference clock is obtained from Tektronix AWG 7122B. Fig 4.3 shows the overall jitter of 1.99ps (rms) and 16.9ps (peak-to-peak) for 1.4GHz output frequency obtained from 43.75MHz reference frequency.

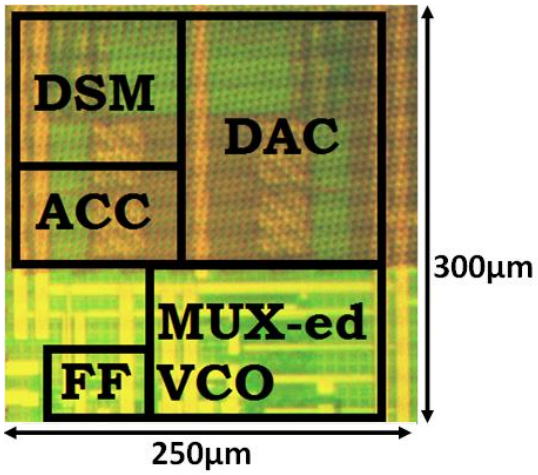

Fig 4.1 Die Photgraph

For the same output frequency, the overall long term jitter obtained is 2.2ps (rms) and 20.2ps (peak-to-peak) for 1 million hits, as shown in Fig 4.4. It should be noted that the reference (43.75MHz) has an overall jitter of 800fs (rms) and 8ps (peak-to-peak), as shown in Fig 4.5. To observe the reference spurs, spectrum analyzer (Agilent E4440A) is used and it can be seen from Fig 4.5 that the reference spurs at 43.75MHz are -50.25dBc/Hz. As an additional

measure of the performance, the phase noise of the MDLL output was measured using the same spectrum analyzer and is shown in Fig 4.6. The random jitter was estimated by integrating the measured phase noise from 4 kHz to 40 MHz, and is found to be 1.57 ps (rms). The phase noise measured at 1MHz offset frequency is found to be -112dBC/Hz.

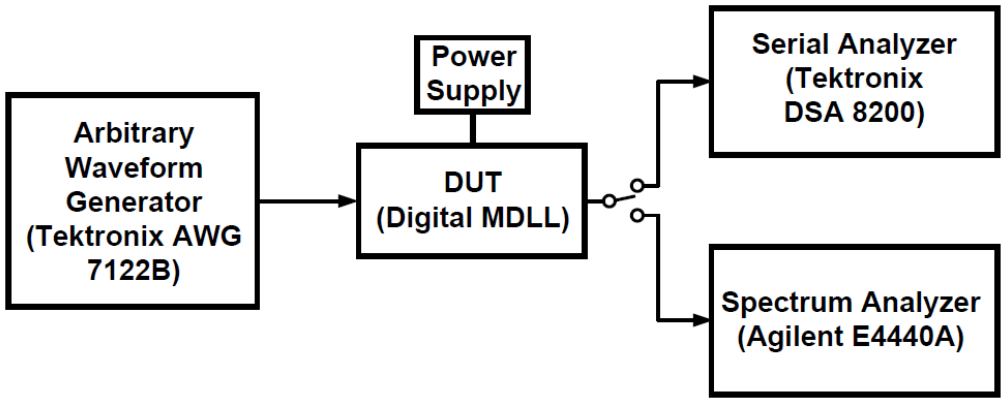

Fig 4.2 Digital MDLL Test Setup

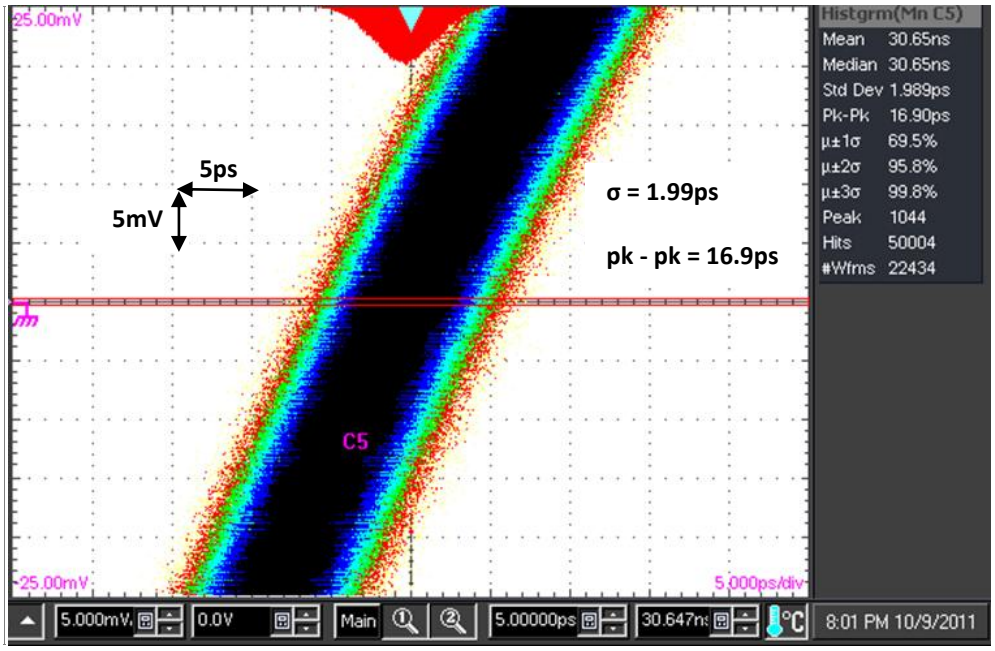

Fig 4.3 Jitter Histogram at 1.4GHz (50K Hits)

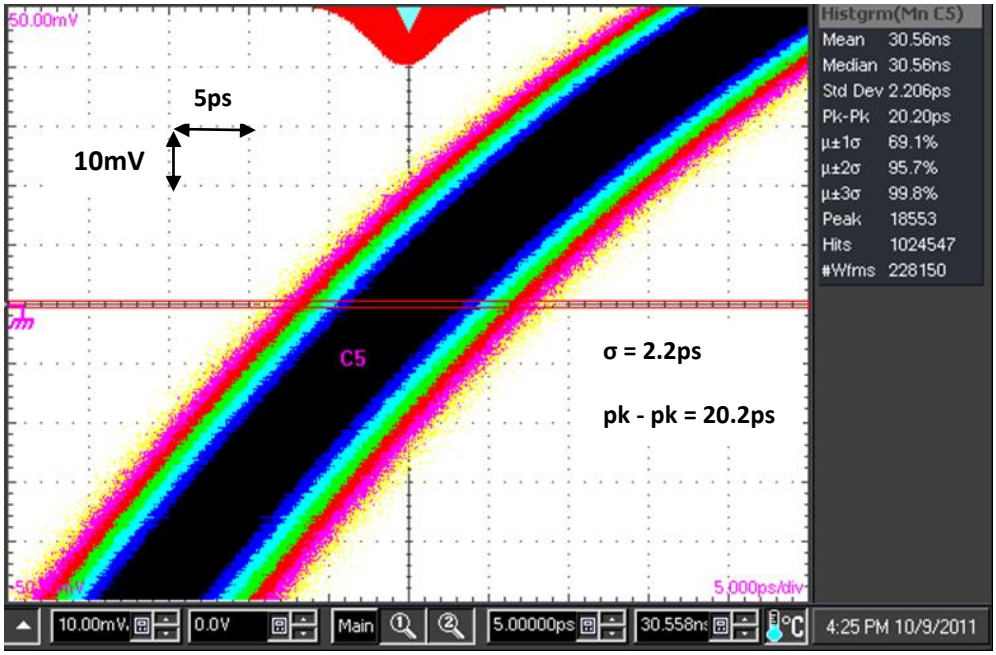

Fig 4.4 Jitter Histogram at 1.4GHz (1M Hits)

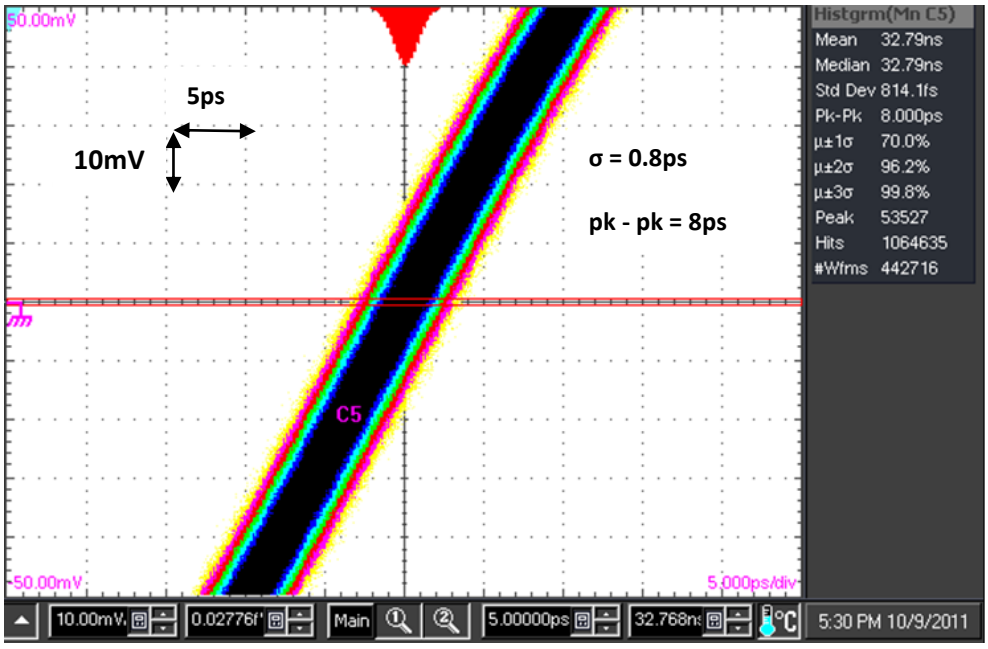

Fig 4.5 Reference Clock Jitter Histogram at 43.75MHz (1M Hits)

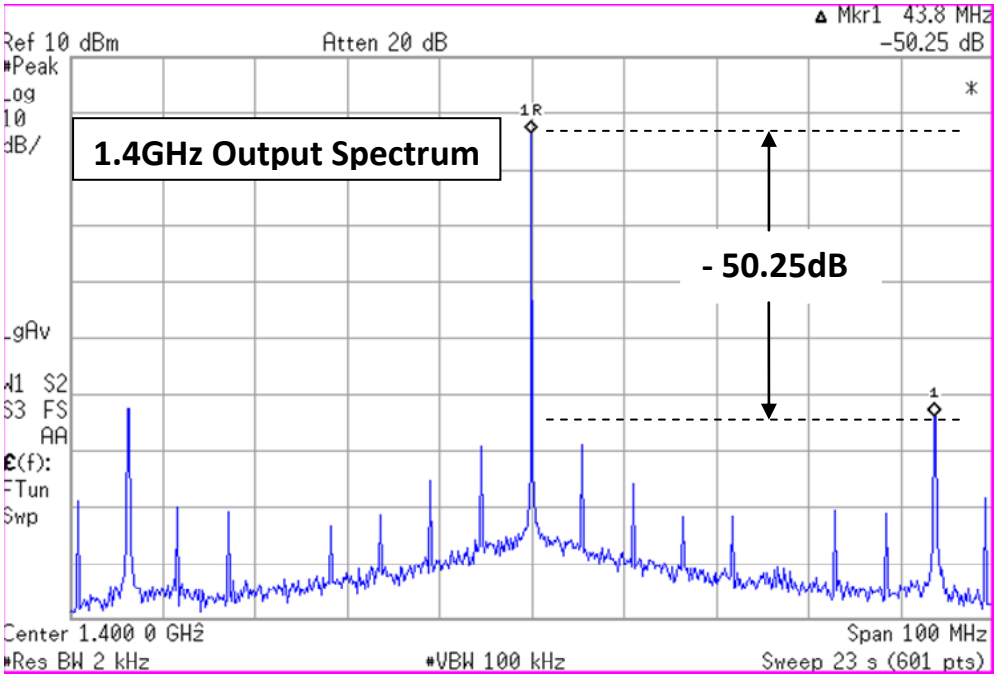

Fig 4.6 Measured Reference Spur at 1.4GHz Output

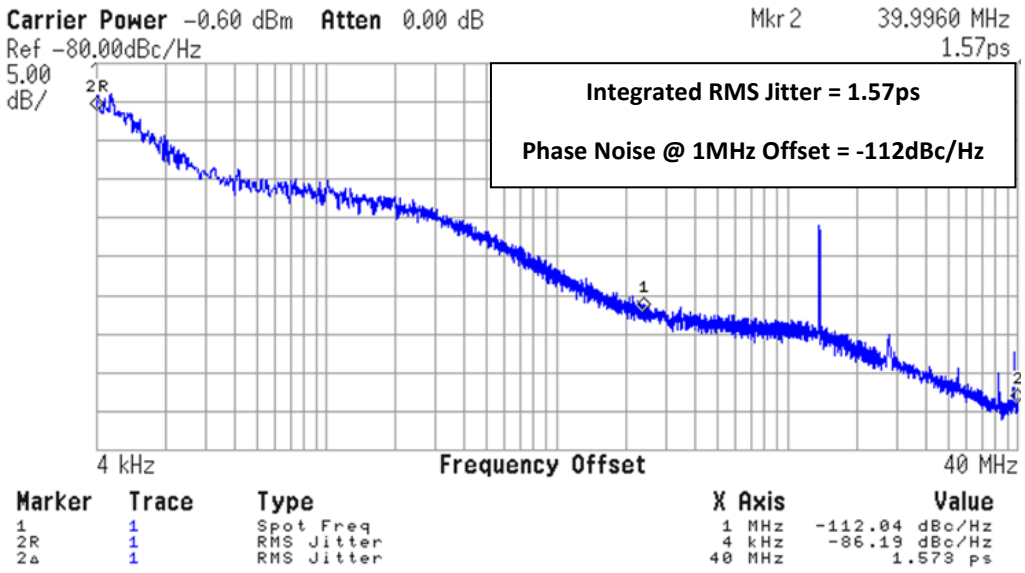

Fig 4.7 Measured Phase Noise at 1.4GHz Output

Table 4.1: Performance Summary

Technology	**130nm**
Supply Voltage	**1.3V**
Output Frequency	**1.4GHz**
Reference Frequency	**43.75MHz**
RMS Jitter (integrated)	**1.57ps**
Peak-to-Peak Jitter	**16.9ps**
Reference Spurs	**-50.3dBc/Hz**
Power	**4.1mW**
Area	**0.075mm^2**

Table 4.2: Measured Performance Comparison

	[7] JSSC '02	[15] CICC '06	[8] JSSC '08	[17] JSSC '10	[19] ISSCC '11	This Work
Technology (nm)	180	180	130	130	90	130
Supply Volt (V)	1.8	1.8	1.2	1.2	1	1.3
Out Freq (GHz)	2	2.16	1.6	1.35	2.5	1.4
Ref Freq (MHz)	250	108	50	50	625	43.75
Divider (N)	8	20	32	27	4	32
Jitter (RMS / PK-PK) (ps)	1.73 / 13.1	1.6 / 12.9	0.93 / 11.1	3.7 / 32	0.9 / 11.6	1.99 / 16.9
Spurs (dBc/Hz)	-37	-46.5	-58.3	-49.3	-50.1	-50.3
Power (mW)	12	19.8	11	16.5	1.6	4.1
Normalized Power (mW/GHz)	6	9.17	6.9	12.22	0.64	2.88
Area (mm^2)	0.05	0.08	0.06 (TDC + MDLL) + 0.7 (DAC) + 0.01 (FPGA) + RC	0.2	0.36	0.075
Implementation	Analog MDLL	Analog MDLL	Digital MDLL	Digital PLL (frac-N)	Digital PLL (int-N)	Digital MDLL

5. CONCLUSIONS

This final chapter of thesis will summarize the contributions of the research work followed by suggestions for future research.

5.1 SUMMARY:

High performance digital systems are ubiquitious these days and there is a continued interest for developing solutions which improve speed (frequency) and accuracy (jitter) in this area. For this very reason, high frequency clock synthesis is an area of active research wherein innovations are needed for better circuit and system-level performance. Phase-locked loop is a traditional clock generation method in which there is still a significant amount of research in progress. The most important motivation of this research was to find an alternative way of high frequency clock synthesis in order to overcome the limitations of phase-locked loops. Some of the major issues with PLLs are: 1) low loop bandwidth which limits rms jitter specification; 2) TDC quantization error and 3) loop delay which cause high deterministic jitter.

A Digital Multiplying Delay Locked Loop (DMDLL) is proposed which seeks to offer a solution to the aforementioned problems. Chapter 1 compared a regular MDLL with a PLL (both analog and digital) and showed how its inherent high bandwidth can be leveraged for better phase noise performance. This was followed by Chapter 2 in which the Digital MDLL architecture is proposed and discussed in brief. Circuit design of each of the blocks of the proposed DMDLL is described in Chapter 3 and is followed by the experimental results of the prototype in Chapter 4. It is observed that the prototype DMDLL fabricated in 130nm Dongbu

Hitek process delivers on its promise and when compared with other state of the art implementations (see Table 1), has a comparable performance in terms of both random jitter and deterministic jitter resulting from reference spurs.

5.2 FUTURE RESEARCH:

As with everything else in life, there is room for improvement for this DMDLL too. One of the issues which could limit the performance of this DMDLL is the set-up time of the SAFF which acts as Phase Detector. The set-up time would appear as static phase offset and cause deterministic jitter in the form of reference spurs.

The DCO in this DMDLL uses a DAC to generate control voltage which controls its oscillation frequency. There is an inherent trade-off between the DAC resolution and DCO frequency range. Circuit techniques could be explored to break this trade-off in order to get both high resolution and high output frequency range. The desired frequency range was obtained in this design using manual tuning for coarse control while the MDLL loop controlled the fine path.

Finally, power supply noise effects in this DMDLL were nullified using sufficient decoupling on the supply pins. However, it is not always possible to use a lot of decoupling which may lead to severe deterministic jitter in the output. Hence, circuit techniques to counter supply noise issues are very much needed and recommended.

BIBLIOGRAPHY:

[1] F. Gardner, “Charge-pump phase-lock loops," *IEEE Trans. Communications*, vol. 40, pp. 849-858, Nov. 1980.

[2] R. Staszewski et, al., “All-digital pll and transmitter for mobile phones," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 2469-2482, Dec. 2005.

[3] J. Lin, et. al., “A pvt tolerant 0.18mhz to 600mhz self-calibrated digital pll in 90nm cmos process," in *ISSCC Digest of Technical Papers*, pp. 488-489, Feb. 2004.

[4] M. Song, et. al., “A 10mhz to 315mhz cascaded hybrid pll with piecewise linear calibrated tdc," in *Custom Intergrated Circuits Conference*, pp. 243-246, Sep. 2009.

[5] G. Chien and P. Gray, “A 900-MHz local oscillator using a DLL-based frequency multiplier technique for PCS applications,” *IEEE J. Solid-State Circuits*, vol. 35, pp. 1996–1999, Dec. 2000.

[6] S. Ye, L. Jansson, and I. Galton, “A multiple-crystal interface PLL with VCO realignment to reduce phase noise,” *IEEE J. Solid-State Circuits*, vol. 37, pp. 1795–1803, Dec. 2002.

[7] R. Farjad-rad et al., “A low-power multiplier DLL for low-jitter multigigahertz clock generation in highly integrated digital chips,” *IEEE JSSC*, vol. 37, pp. 1804–1812, Dec. 2002.

[8] B. Helal et al., “A Highly Digital MDLL-Based Clock Multiplier That Leverages a Self-Scrambling Time-to-Digital Converter to Achieve Subpicosecond Jitter Performance,” *IEEE J. Solid-State Circuits*, vol. 43, pp. 855–863, Apr. 2008.

[9] B. Nikolic, et. al, “Improved Sense-Amplifier Based Flip-Flop: Design and Measurements”, *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 876-884, June. 2000.

[10] J. Rabaey, et. Al., “Digital Integrated Circuits,” 2nd Edition, Prentice Hall, 2003

[11] P. Maulik et. al., “A DLL-Based Programmable Clock Multiplier in 0.18 um CMOS With -70 dBc Reference Spur," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1642-1648, Aug. 2007.

[12] R. Farjad-Rad, et. al, “A low-power multiplying DLL for low-jitter multigigahertz clock generation in highly integrated digital chips," *IEEE JSSC*, vol. 37, no. 12, pp. 1804-1812,Dec 02.

[13] A. Hajimiri, S. Limotyrakis, and T. Lee, “Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 790-804, Jun. 1999.

[14] J. Lee and B. Kim, “A Low-Noise Fast-Lock Phase-Locked Loop with Adaptive Bandwidth Control,” in *IEEE J. Solid-State Circuits*, vol. 35, pp. 1137-1145, Aug. 2002.

[15] Q. Du, J. Zhuang, and T. Kwasniewski, “An Anti-Harmonic Locking, DLL Frequency Multiplier with Low Phase Noise and Reduced Spur,*” IEEE CICC,* pp. 761-764, 2006

[16] J. Tierno, A. Rylyakov, and D. Friedman, “A wide power supply range,wide tuning range, all static CMOS all digital PLL in 65 nmSOI,” IEEE J. Solid-State Circuits, vol. 43, no. 1, pp. 42–51, Jan. 2008.

[17] D. Kim, H. Song, T. Kim, S. Kim, and D. Jeong, “A 0.3-1.4 GHz alldigital fractional-N PLL with adaptive loop gain controller,” *IEEE J.Solid-State Circuits*, vol. 45, no. 11, pp. 2300–2311, Nov. 2010.

[18] Chen, et. al., “A Calibration-Free 800MHz Fractional-N Digital PLL with Embedded TDC,” *ISSCC Dig. Tech. Papers*, p.p. 472-473, Feb. 2010.

[19] Yin, et. al., “A 0.7-3.5 GHz 0.6-to-2.8 mW Highly Digital Phase-Locked Loop With Bandwidth Tracking,” *IEEE J.Solid-State Circuits*, vol. 46, no. 8, pp. 1870–1880, Aug. 2011.