AN ABSTRACT OF THE DISSERTATION OF

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Terri S. Fiez

There is a significant need in recent mobile communication and wireless broadband systems for high-performance analog-to-digital converters (ADCs) that have wide bandwidth (BW>5-MHz) and high data rate (>100-Mbps). A delta-sigma ADC is recognized as a power-efficient ADC architecture when high resolution (>12-b) is required. This is due to several advantages of the delta-sigma ADC including relaxed anti-aliasing filter requirements, high signal-to-noise and distortion ratio (SNDR) and most importantly, reduced sensitivity to analog imperfections. In this thesis, several structures and design techniques are developed for the implementation of continuous-time (CT) and discrete-time (DT) delta-sigma ADCs. These techniques save the total power consumption, reduce the design complexity, and decrease the chip die area of delta-sigma modulators.

First a 4th-order single stage CT delta-sigma ADC with a novel single-amplifier-biquad (SAB) based loop filter is presented. By utilizing the SAB networks in the loop filter of an Nth-order CT delta-sigma modulator, it requires only half the number of active amplifiers and feed-forward branches used in the conventional modulator architecture, thus decreasing the power consumption and area by reducing the number of amplifiers. The proposed scheme also enables the modulator to use a switch-capacitor (SC) adder due to the reduced number of feedforward branches to its summing block. As a sequence, it consumes less power compared to a conventional CT adder. With a 130-nm CMOS technology, the fabricated prototype IC achieves a dynamic range of 80 dB with 10 MHz

signal bandwidth and analog power dissipation lower than 12 mW. Presented as the second scheme to save power consumption and chip die area in ΔΣ modulators is a new stage-sharing technique in a discrete-time 2-2 MASH ΔΣ ADC. The proposed technique shares all the active blocks of the modulator second stage with its first stage during the two non-overlapping clock phases. Measurement results show that the modulator designed in a 0.13-um CMOS technology achieves 76 dB SNDR over a 10 MHz conversion bandwidth dissipating less than 9 mW analog power.

Wide-Bandwidth, High-Resolution Delta-Sigma Analog-to-Digital Converters

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I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

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To my dearest parents for their unconditional sacrifice and support

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CHAPTER 1. TRADEOFFS IN CIRCUIT DESIGN FOR HIGH PERFORMANCE CT AND DT ΔΣ ADCs

Abstract

This chapter presents a review of the circuit design tradeoffs and issues for high speed, high resolution continuous-time (CT) and discrete-time (DT) delta-sigma (ΔΣ) modulators. After dealing with the fundamental circuit and system limitations, solutions and tradeoffs are discussed in detail. Thee effects of thermal noise, clock jitter, and the modulator active block finite gain and bandwidth are discussed as the main source of non-idealities in the both modulators. Finally, several techniques are reviewed to minimize these undesired effects.

1.1 INTRODUCTION

Analog-to-digital converters are important components in applications requiring the interface between analog and digital domains. There are numerous applications such as digital radio systems, military and medical sensors, and wire-line and wireless communication systems. There are a number of different ADC architectures available to accomplish the data conversion task; however, no single architecture is suitable for all applications. As illustrated in Fig. 1.1, these architectures span a range of intended resolutions and conversion speeds. Meanwhile, wireless and wire-line communication applications demand analog-to-digital converters (ADCs) with megahertz signal bandwidth and 12-bit or better resolution. Compared with Nyquist-rate ADCs, oversampling ADCs use more digital signal processing to perform analog-to-digital conversion, with the advantage of significantly relaxed matching requirements for the analog components, while still achieving medium to high resolution [1]. Moreover, thanks to the oversampling delta-sigma ADCs, they do not need steep roll-off antialias filtering, which is usually required in Nyquist-rate ADCs. Power-hungry high-order high-linearity antialias filters with accurate cutoff frequencies are thus avoided. Oversampling ADCs are traditionally used in instrumentation, seismic, voice, and audio applications, with low signal bandwidth and high resolution. In recent years, due to improvements in

CMOS technology and architecture/circuit design techniques, ADCs can achieve higher input signal bandwidth and medium to high resolution (12–16 bits), and enjoy wide deployment in wireless and wire-line communication applications [2], [3].

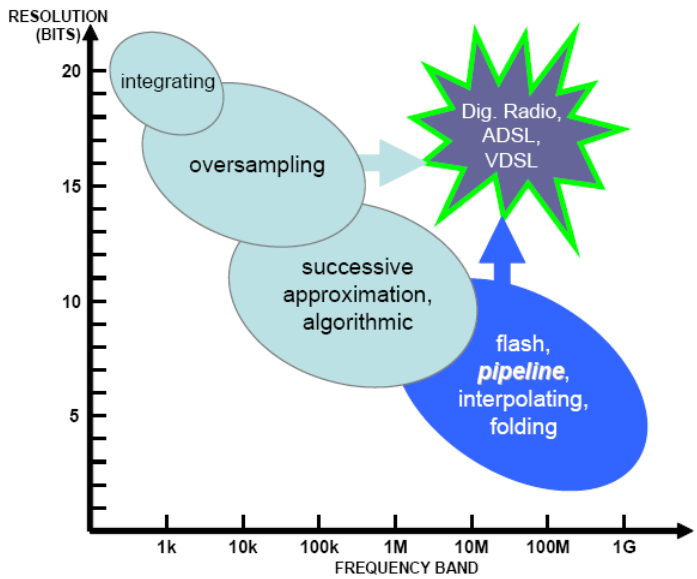


Fig. 1.1: Application of the different types of ADCs.

In this chapter, we focus on the design challenges and tradeoffs of CT and DT delta-sigma modulators, as well as reviewing the ideas and techniques to alleviate limitations and improve the performance.

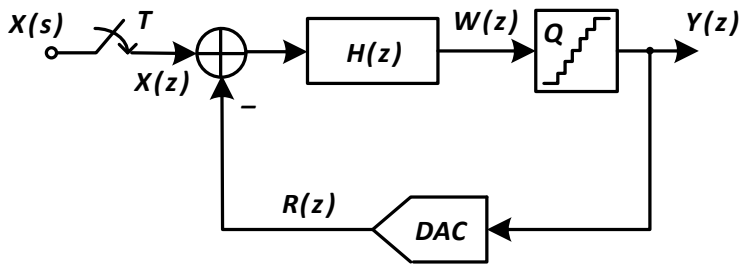
1.2 SYSTEM LEVEL ANALYSIS OF ΔΣ MODULATORS

1.2.1 Brief Review of ΔΣ Modulators

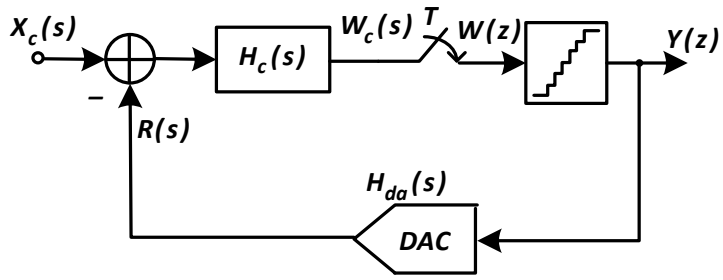
As the core of a ΔΣ A/D converter, the analog modulator normally has three primary components which includes loop filter, quantizer and feedback DAC as shown in Fig. 1.2 [4], [23].

1.2.1.1 LOOP FILTER

It contains a discrete or continuous time transfer function which has large gain within the signal band while it attenuates out-of-band signals. A loop filter is realized by switched-capacitor integrators in a DT implementation and continuous-time integrators in a CT implementation such as active-RC, Gm-C, and passive architectures.



(a)



(b)

Fig. 1.2: Simplified model of (a) A discrete-time ΔΣ (b) A continuous-time ΔΣ.

1.2.1.2 QUANTIZER

The quantizer works as an internal A/D converter to convert sampled analog signals and generates the modulator's output. Its output can be single-bit or multi-bit depending on the system requirements. A single-bit quantizer is realized by a comparator. A multi-bit quantizer is normally implemented by a flash ADC to obtain high speed conversion.

1.2.1.3 FEEDBACK DAC

The DAC feedback converts back the digital output word from the quantizer output to an analog signal or pulse. It is then substracted from the input signal. Hence, creating a negative feedback loop. This DAC can be implemented with switched-capacitor (SC), current-steering, resistive or other circuit types. Every ΔΣ ADC requires at least one DAC at its input.

In ΔΣ A/D modulators, since the quantizer is essentially non-linear, the modulator cannot be considered as a linear feedback system. However, if quantization noise in the quantizer can be modeled as white noise, the nonlinear quantizer can thus be approximated as an adder. As a result, the system transfer function for the DT ΔΣ modulator can be easily derived in the z-domain as follows:

$$Y(z) = \frac{H(z)}{1 + H(z)}.X(z) + \frac{1}{1 + H(z)}.E(z) \tag{1.1}$$

$$\mathrm{Y(z) = STF(z).X(z) + NTF(z).E(z)} \tag{1.2}$$

where $STF(z)$ and $NTF(z)$ are the signal and noise transfer functions (TFs), respectively. From the equation above, we see that the poles of $H(z)$ become the zeros of $NTF(z)$. For $H(z) \gg 1$, the modulator output approximates the input as shown below.

$$Y(z) \approx X(z) \tag{1.3}$$

In other words, the output signal contains the unfiltered input plus the high-passed quantization noise (for the case of a low-pass converter) or band stopped quantization noise (for the case of a band-pass converter). Since the quantization noise is largely pushed out-of-band, high in-band signal-to-noise ratio (SNR) can be obtained. For a L-th order modulator with a noise transfer function of $(1 - z^{-1})^L$, the total in-band quantization noise can be calculated as:

$$P_N = \int_{-f_B}^{f_B} S_{QS}(f)\ \partial f \approx \left(\frac{\pi^{2L}}{2L+1}\right)\left(\frac{1}{M^{2L+1}}\right)\frac{\Delta^2}{12} \tag{1.4}$$

Where $S_{QS}(f)$ is the quantization noise power spectral density (PSD), M is the oversampling ratio (OSR), Δ is the quantizer step size, L is the modulator loop order and f_B is the signal bandwidth. The signal to quantization noise ratio (SQNR) is:

$$\mathrm{SQNR} = \frac{P_S}{P_N} = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(2^N - 1)^2 M^{2L+1} \tag{1.5}$$

1.2.2 Transformation of DT ΔΣ Modulator to CT ΔΣ A/D

For designing a DT ΔΣ modulator, the commonly used Delta-Sigma Matlab® Toolbox is utilized [4]. To do so, all the design parameters such as oversampling ratio, resolution, signal bandwidth, out of band noise gain, etc. are considered. As a result, quantizer resolution, loop filter order, and arrangement of NTF zeros are defined for an optimum design [5]. Meanwhile, the design method of a CT ΔΣ modulator depends on the design of its DT version because there is no direct design approach to extract the loop filter (LF) transfer function, and optimize performance of the CT modulator. Consequently, different mapping methods are used to map the DT loop filter (LF) transfer function, $H(z)$, of an optimized DT ΔΣ A/D to loop filter TF, $H(z)$, of a CT modulator. Common mapping methods are Impulse Invariant Transform (IIT), Modified Z-Transform, and State-Space Method.

1.2.2.1 IMPULSE INVARIANT TRANSFORM

As shown in Fig. 1.2, unlike the DT modulator, sampling is not at the front-end input in a CT modulator. In this case, sampling is at the input of the quantizer. There is no doubt that if they produce the same output bit sequence in the time-domain for the same time instant, they can be considered equivalent. This “same-output” condition can be

satisfied by ensuring the inputs to both quantizers are the same at each sampling instant. As mentioned above, the two modulators are equivalent if their quantizers have the same inputs at each sampling instant, meaning:

$$W[n] = W_c(t)|_{t=nT} \tag{1.6}$$

This can be satisfied if the open loop impulse responses are the same at sampling instants, which can be written as [5]:

$$Z^{-1}(H(z)) = L^{-1}(H_{da}(s)H_c(s))|_{t=nT} \tag{1.7}$$

Or in the time-domain:

$$h[n] = [h_{da}(t) * h_c(t)]|_{t=nT} \tag{1.8}$$

where $h[n]$, $h_{da}(t)$ and $h_c(t)$ are the impulse responses of the DT loop filter $H(z)$, the CT feedback DAC pulse and the CT loop filter impulse response, respectively. This transformation between the DT and CT domains is called the Impulse Invariant Transformation (IIT), as implied by its name [6].

1.2.2.2 STATE–SPACE METHOD

In the state-space approach, the loop-filter $H_c(s)$ is described by a set of equations in the time domain [6]:

$$\frac{du(t)}{dt} = F.u(t) + G.r(t) \tag{1.9}$$

$$w(t)=C.u(t)$$

Where $u(t)$ is the state–vector and F is an NxN matrix called the state matrix, G is an NxN matrix and C an $Nx1$ vector, N is the system order, which represents the number of

integrators in a minimal system implementation. Note that in these equations the input signal is omitted and $r(t)$ represents the feedback signal. The solution of the state–equations in (1.9) starting from the initial state $u(t_0)$ is [7]:

$$u(t) = e^{F(t-t_0)}.u(t_0) + \int_{t_0}^{t} e^{F(t-\Omega)}\, G.r(\Omega)\, d\Omega \tag{1.10}$$

Supposing an initial state $u[n]$ at $t_0 = nT$ and replacing $t = nT + T$ in (1.10), the state of the system at the end of clock $[n+1]$ becomes [7]:

$$u[n+1] = e^{FT}.u[n] + y[n] \int_{0}^{T} e^{F(T-\varphi)}\, G.h_{da}(\varphi) d\varphi \tag{1.11}$$

On the other hand, the DT modulator is described by a similar set of DT-state equations

$$u[n+1] = A.u[n] + B.y[n] \tag{1.12}$$

$$w[n] = C.u[n]$$

Comparison of (1.11) and (1.12) yields the transformation equations between two systems as:

$$A = e^{FT}$$

$$B = \int_{0}^{T} e^{F(T-\varphi)}\, G.h_{da}(\varphi) d\varphi \tag{1.13}$$

1.2.2.3 MODIFIED Z-TRANSFORM

An alternative method for calculating the coefficients of a CT modulator is computing the input of the quantizer in the CT modulator at the sampling instant and subsequently,

equating it with the quantizer input of the DT modulator, i.e., $w[n] = w_c[nT]$. The input signal to the D/A block of a CT-modulator is a train of DT impulses weighted by the modulator output. Upon receiving each impulse, the D/A generates an output signal with a duration of τ which cannot practically be longer than one clock period. Hence, the feedback signal is given by:

$$w(nT) = \sum_{i=0}^{\infty} y[i].\int_0^T h_{da}(\varphi).h_c(nT - iT - \varphi)d\varphi \tag{1.14}$$

On the other hand, the quantizer input of a DT modulator is related to the modulator output through the DT convolution [7]:

$$w[n] = \sum_{i=0}^{\infty} y[i].h[n-i] \tag{1.15}$$

Where $h[n]$ is the impulse response of the DT modulator's loop-filter, $H(z)$. Comparing equations (1.14) and (1.15) and taking the Z- transform:

$$H(z) = \int_0^T h_{da}(\varphi).H_c\left(z, 1 - \frac{\varphi}{T}\right)d\varphi \tag{1.16}$$

1.3 CIRCUIT DESIGN TRADEOFFS IN ΔΣ ADCs

According to the explanations in the previous section, all the system level specifications of a DT or CT ΔΣ A/D modulator can be extracted using optimum design methods to satisfy parameters such as resolution, sampling rate and speed requirements. But in reality, there are various non-idealities in all three core blocks of a modulator. As the non-idealities, finite opamp gain, bandwidth, and slew rate of the integrator blocks in the loop filter, quantizer delay, offset, hysteresis, and metastability, also the multi-bit feedback DAC element mismatch, excess loop delay and clock jitter adversely affect the performance of ΔΣ A/D modulators. However, due to their different mechanisms and

locations inside the modulator, their effects are different. To guarantee a successful design, a thorough understanding of these non-ideal phenomena is required. In this section, we present details of these "unwanted" effects, derive mathematical models which can be included in system level simulations, and also describe commonly used solutions to overcome these issues.

1.3.1 Integrator Non-Idealities

The operational amplifier is one of the fundamental analog blocks in analog circuit design. It is also used in different parts of a ΔΣ A/D modulator such as the loop filter to implement active integrators or delay blocks, in the adder block in front of the quantizer, and also in the sample and hold block of the CT modulator to sample the CT data before the quantizer block. All the non-idealities related to the amplifier in the first stage of the loop filter will not undergo any attenuation since the modulator frontend does not see any noise shaping. Hence, it will impact the modulator performance to a large extent.

1.3.1.1 OPAMP FINITE DC GAIN AND BANDWIDTH

A. OpAmp Finite Gain & BW Effects in DT ΔΣ A/D

The dc gain of a switch-capacitor (SC) integrator described by (1.17) is infinite. In practice, however, the gain is limited by circuit constraints. The opamp finite DC gain effect in the integrator block, known as the leakage effect, is that only a fraction, $\boldsymbol{a}$, of the previous output of the integrator is added to each new input sample. The transfer function of the integrator with the leakage effect is presented by (1.18) [8].

$$H(z) = \frac{bz^{-1}}{1 - z^{-1}} \tag{1.17}$$

$$H(z) = \frac{bz^{-1}}{1 - a.z^{-1}} \tag{1.18}$$

As an example, Fig. 1.3 shows a typical single-ended delaying switched-capacitor (SC) integrator. C_1 and C_2 are the sampling and integration capacitors, respectively. φ_1 and φ_2 are two non-overlapping clock phases.

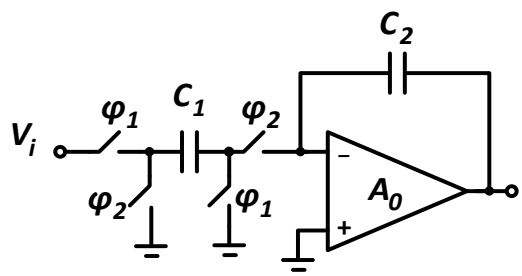


Fig. 1.3: Single-ended SC integrator used in DT ΔΣ modulator.

The integrator samples the input during φ_1 while it performs integration while φ_2 is high. Although only a single-ended integrator is shown here for the analysis, fully differential circuits are normally adopted for better common-mode noise rejection. The integrator Z-domain transfer function considering the finite gain is given by (1.18) where its parameters are given.

$$a = \frac{1}{1 + \frac{1}{1 + A_0} . \frac{C_1}{C_2}}, \quad b = \frac{A . \frac{C_1}{C_2}}{1 + A_0 + \frac{C_1}{C_2}} \tag{1.19}$$

To find the effect of the opamp finite bandwidth (BW) in the integrator block, evolution of the output node during the nth integration period (while φ_2 is high) is [8]:

$$V_O(t) = V_O(nT - T) + \alpha\, V_s\left(1 - e^{\frac{-t}{\tau}}\right) \tag{1.20}$$

$$nT - \frac{T}{2} \leq t \leq nT$$

Where $V_s = V_{in}(nT - T/2)$, α is the integrator leakage factor and $\tau = 1/(2\pi.\beta.A_0.BW)$ is the time constant of the integrator. As mentioned before, the first integrator in the loop filter of a ΔΣ A/D modulator is very important in terms of accuracy. Therefore, considering a finite dc gain for the opamp, the dc gain of the integrator is restricted to $b/(1-\alpha)$ instead of infinity. Also, the pole of the integrator is shifted from $z = 1$ $(s = 0)$ to $= \alpha$ $(\alpha < 1)$. Limited dc gain and shifted pole of the integrator directly affects signal-to-quantization-noise-ratio (SQNR) in the band of interest. Furthermore, these effects change the optimum NTF and may result in instability of the modulator. The unity-gain-bandwidth (UGB) of opamps in SC circuits should satisfy (1.21) where N is the resolution in number of bits, and β is the feedback factor. For settling within 0.1% accuracy and $\beta=0.5$, the UGB of the opamp should be at least five times the sampling frequency [9], [10].

$$UGB \geq {(N+1)\ln(2).f_s}/{\pi\beta} \tag{1.21}$$

B. OpAmp Finite Gain & BW Effects in CT ΔΣ ADCs

Modeling the non-idealities in a CT integrator depends on its implementation. A CT integrator can be as simple as an active-RC integrator, a transconductor based Gm-C integrator, or even an LC resonator. In this section, we will concentrate on the active-RC integrator approach. Equation (1.22) presents the first order approximation of the opamp transfer function considering the finite gain and BW of the opamp utilized in the RC integrator [11].

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_0}}, \quad UGB = \omega_0.A_0 \tag{1.22}$$

This is a good approximation for a single-stage amplifier with large phase margin. Figure 1.4 shows a commonly used active-RC integrator in CT ΔΣ A/D modulators. As explained before, the first stage of the loop filter or first integrator of the single loop CT modulator is usually an active-RC architecture because of its higher linearity. The clocked current source(s) in the integrator acts as a simple DAC to provide feedback from the single-bit or multi-bit quantizer. Considering the opamp nonideal effects such as finite gain and finite bandwidth, the modified transfer function of the integrator is:

$$\frac{V_o}{V_i} = \frac{-kf_s}{s} \cdot \frac{1-\alpha}{1+\frac{s}{\omega_1}}, \qquad kf_s = \frac{1}{R_{in}C} \tag{1.23}$$

$$\alpha = \frac{kf_s}{UGB + kf_s}, \qquad \omega_1 = UGB + kf_s$$

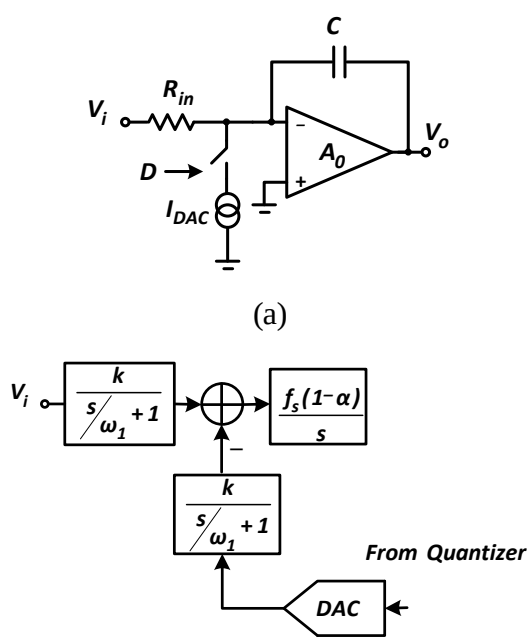


Fig. 1.4: Single-ended active-RC integrator used in CT ΔΣ A/D with finite gain and bandwidth (a) Circuit level (b) System level.

Where α is the gain error with respect to an ideal integrator gain. Integrator gain error can be reduced by increasing the k factor. The added second pole, ω_1, has no effect on the

input signal path as long as it is much larger than the maximum signal frequency, which is easy to satisfy. However, it will generate an extra loop delay in the feedback path. As will be discussed later, excess loop delay can lead to modulator instability so that it must be well controlled. As an advantage of the CT ΔΣ modulators, UGB of the opamps used in the loop filter integrator blocks does not need to satisfy (1.21). Since there is no settling requirement, UGB can be close to the modulator sampling frequency [4].

1.3.1.2 THERMAL NOISE OF THE INTEGRATOR BLOCK

A. Integrator Thermal Noise in DT ΔΣ ADCs

The most important noise sources affecting the operation of a DT ΔΣ modulator are the thermal noise associated with the sampling switches and the intrinsic noise of the operational amplifiers. The total noise power of the circuit is the sum of the theoretical loop quantization noise power, switch noise power and the opamp noise power. Because of the large low-frequency gain of the first integrator, noise performance of the ΔΣ modulator is determined mainly by the switch noise and op-amp noise of the input front-end. Again referring to Fig. 1.3, $R_{on,s}$ is the "on" resistance of the sampling phase switches which are in series with the integrator's sampling capacitor, C_1. During phase φ_1, thermal noise of the sampling switches is sampled on C_1. Noise power stored in C_1 during the sampling phase is:

$$V_{C_1,n_1}^2 = \int_0^{\infty} \frac{4KT\,(2R_{on,s})}{1+\left[2\pi(2R_{on,s})C_1.f\right]^2}\,df = \frac{KT}{C_1} \tag{1.24}$$

Next, when φ_2 rises, two integration phase switches are closed. As a result, thermal noise of these switches will contribute to the total noise. To make the analysis more specific, a single-stage opamp is assumed in the noise calculation during the integration phase. Equation (1.25) shows the value of the noise power around C_1 caused by the integration phase switches.

$$V_{C_1,n_2}^2 = \frac{KT}{\left(1+\frac{1}{x}\right)C_1} \tag{1.25}$$

$$x = 2.R_{on,i}.g_m$$

Where $R_{on,i}$ is the "on" resistance of the integration switches and g_m is the transconductance of the single-stage opamp. The operational amplifier used in the integrator also adds to the noise charged in C_1 which is demonstrated in (1.26). Therefore, the total noise power in the DT integrator is derived by summing all three noise sources mentioned above [1], [12], [13].

$$V_{C_1,n_{op}}^2 = \frac{2\gamma KT}{(1+x)C_1}, \qquad \gamma \approx \frac{2}{3} \tag{1.26}$$

$$V_{C_1,n_{total}}^2 = V_{C_1,n_1}^2 + V_{C_1,n_2}^2 + V_{C_1,n_{op}}^2 = \frac{KT}{C_1}\left(\frac{2x+\frac{7}{3}}{1+x}\right) \tag{1.27}$$

B. Integrator Thermal Noise Effect in CT ΔΣ ADCs

As explained before, thermal noise is one of the fundamental limitations when designing high-resolution A/D converters. For CT ΔΣ modulators, a critical design parameter is the thermal noise of the first integrator since it is not shaped by the order of the modulator, unlike the quantization noise. As shown in Fig. 1.5, the noise sources that contribute principally to the overall thermal noise power are the input resistance, the amplifier broad-band noise and the feedback current source's thermal noise. The in-band thermal noise contribution from the input resistance is shown in (1.28) which is doubled for the differential topology.

$$V_{R_{in},n}^2 = 4KTR_{in}.\Delta f \tag{1.28}$$

As the other thermal noise source in the CT modulator front-end, current sources of the current steering DAC add to the modulator in-band thermal noise. The total value of the DAC thermal noise depends on its topology. For a single-ended current steering DAC, the total noise power is calculated as described as:

$$V_{DAC,n}^2 = \frac{8KT\gamma I_{DAC} R_{in}^2}{V_{OV}} . \Delta f \tag{1.29}$$

Where V_{OV} is the overdrive voltage of the current source's tail current source transistor, and I_{DAC} is the DAC current source value. The front-end integrator's opamp is the other thermal noise source in the CT modulator. A simple single-stage 5-transistor opamp with an nMOS input devices is considered for the first integrator. Consequently, the thermal noise contribution of the opamp is:

$$V_{op,n}^2 = \frac{8KT\gamma}{g_{mN}} . (1 + \frac{g_{mP}}{g_{mN}}) \Delta f \tag{1.30}$$

where g_{mN} and g_{mP} stand for the transconductance of the nMOS and pMOS devices of the single-stage opamp. As a result, the total input referred thermal noise in a CT ΔΣ ADC consisting of the noise contributions from the input resistor, DAC current source, and integrator operational amplifier is[13-14]:

$$V_{in,n_{total}}^2 = V_{R_{in},n_1}^2 + V_{DAC,n_2}^2 + V_{op,n_{op}}^2$$

$$= 4KT \left(\frac{2\gamma}{g_{mN}} \left(1 + \frac{g_{mP}}{g_{mN}} \right) + \frac{2\gamma I_{DAC} R_{in}^2}{V_{OV}} + R_{in} \right) \Delta f \tag{1.31}$$

It is clear that for the first stage of the loop filter having smaller R_{in} is better in terms of thermal noise but it has a tradeoff with linearity of the first integrator (1.32) with thermal noise where the higher DAC current output impedance improves the front-end linearity [15].

$$HD_3 \propto \frac{V_{in}^2}{R_{in}^3}.(1+\frac{R_{in}}{R}_{DAC,o})\Delta f \tag{1.32}$$

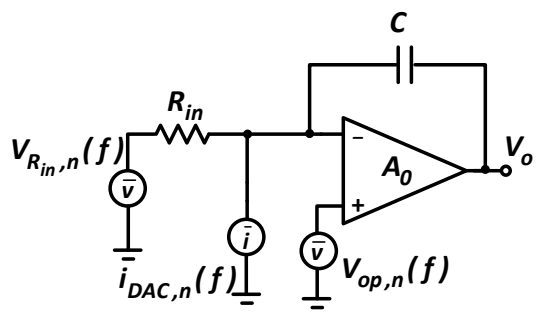


Fig. 1.5: Thermal noise sources in an active-RC integrator used in CT ΔΣ modulator.

1.3.2 Quantizer And DAC Non-Idealities

1.3.2.1 EXCESS LOOP DELAY IN ΔΣ MODULATORS

Practical quantizers have non-zero time to generate the correct outputs. This delay, mainly determined by comparator design and IC process, together with the finite time for the feedback DAC to respond, comprises the delay between the quantizer clock edge and valid DAC output. The total delay is called excess loop delay. It should be noted that in many modulators employing multi-bit feedback DACs, dynamic element matching (DEM) or calibration circuitry may be included in the feedback path to suppress DAC element mismatch errors. These extra signal processing blocks add more delays. Also, while the real circuit implementation of the loop filter uses non-ideal integrators, there is an excess loop delay in this pass. For DT modulators, the excess loop delay can be nearly as high as one clock period without compromising modulator performance and stability. However, this is not the case for CT modulators. This problem is illustrated in Fig. 1.6 for three different rectangular DAC pulse shapes. As shown, excess loop delay shifts the DAC output pulse to the right by the time constant of τ_d. Therefore, the DAC transfer function will deviate from its ideal expression. Consequently, while all the proceeding mapping methods consider a specific DAC output pulse, the extracted CT loop filter will

not be the optimized one. Usually excess loop delay increases the order of the loop filter and makes the modulator unstable [16], [17], [18].

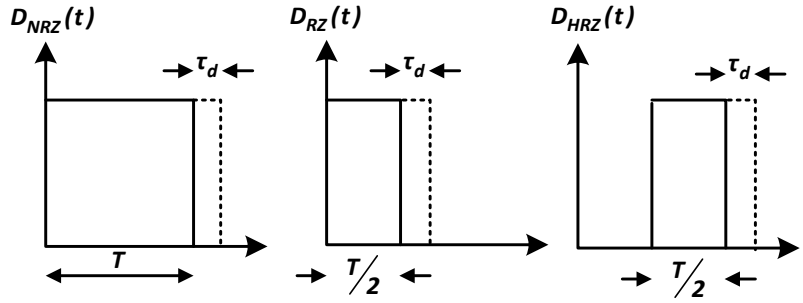


Fig. 1.6: Excess loop delay on NRZ, RZ, and HRZ DACs.

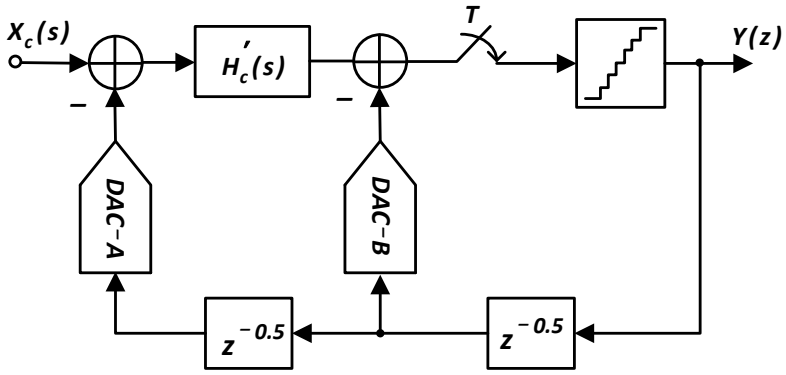


Fig. 1.7: CT ΔΣ A/D with extra feedback to overcome loop delay.

Excess loop delay effects in the NRZ and HRZ DAC pulse shape shifts the pulses to the next sampling instance and increases the order of the loop filter while the RZ DAC pulse shape does not exceed T due to the excess loop delay. There are different ways to overcome the loop delay effect. One of the commonly utilized approaches is depicted in Fig. 1.7 in which one clock delay is purposely introduced in front of DAC_A in the main noise-shaping loop. To keep the output of the new loop filter unchanged at the sampling instants, a feedback path is added from the output to the input of the internal ADC, formed by a half clock cycle delay and DAC_B [17].

1.3.2.2 JITTER NOISE IN ΔΣ MODULATORS

A. Jitter Noise effect in DT ΔΣ Modulator

The clock jitter effect in a DT ΔΣ modulator is described considering its effect on the sampling of the input signal. This is because the whole implementation of the DT ΔΣ modulator uses SC circuitry; therefore, variations of the clock period have no direct effect on the modulator performance. On the other hand, the effect of clock jitter in a DT ΔΣ modulator is independent of the structure or order of the modulator.

For a sinusoidal input signal, the sampling error is ΔV_{in} by assuming a clock jitter of Δt at the sampling instant of t as given by [19]:

$$\Delta V_{in}(t) = \frac{d\,V_{in}(t)}{dt}\Delta t$$

$$= 2\pi f_{in}\,A\,\Delta t\cos(2\pi f_{in}t + \omega_0) \qquad (1.33)$$

where f_{in} and A are the frequency and the amplitude of the input sinusoidal signal. Considering the clock jitter as a white noise with a Gaussian distribution, and standard deviation of $\sigma_{\Delta t}$, the resultant error has uniform power spectral density from dc to $f_s/2$, with a total power of:

$$P_{jitter} = E[\Delta^2 V_{in}(t)] = (2\pi f_{in} A\,\sigma_{\Delta t})^2 \qquad (1.34)$$

$$SNR_{jitter} = \frac{P_s}{P_{sjitter}} = \frac{A^2/2}{(2\pi f_{in} A\,\sigma_{\Delta t})^2/(2OSR)}$$

$$= \frac{OSR}{(2\pi f_{in} A\,\sigma_{\Delta t})^2} \qquad (1.35)$$

According to (1.35) SNR_{jitter} is independent of the input signal amplitude.

B. Jitter Noise effect in CT ΔΣ Modulator

In CT ΔΣ A/D modulators, both the quantizer and the feedback DAC are clocked. Sampling error due to clock jitter at the quantizer is shaped by the order of the loop filter like the quantization noise. Therefore, it adds little noise to the modulator output. However, clock jitter in the feedback DAC generates noise which appears in the modulator output without attenuation and affects the modulator performance significantly.

Assuming a CT modulator with NRZ and RZ feedback DAC waveforms, the clock jitter effect is illustrated in Fig. 1.8. Meanwhile, the error sequence for NRZ and RZ DAC pulse shapes can be expressed by (1.36) and (1.37), respectively [20].

$$e_{NRZ}(n) = (y[n] - y[n-1]).\frac{\Delta t(n)}{T_s} \tag{1.36}$$

$$e_{RZ}(n) = 2y[n].\frac{\Delta t(n)}{T_s} \tag{1.37}$$

where $y[n]$ is the nth output bit, Δt is the clock edge timing error and T_s is the clock period.

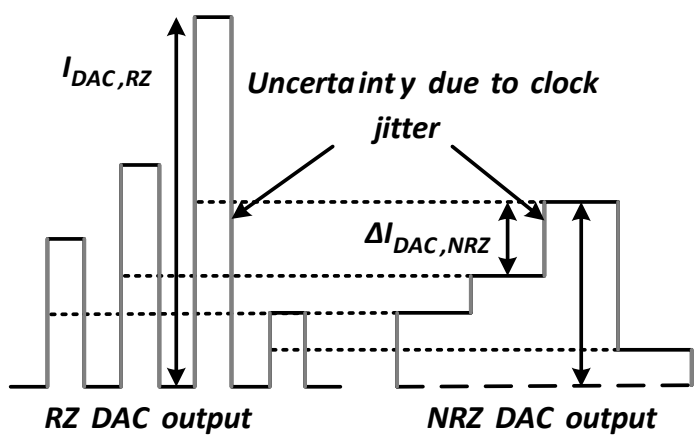


Fig. 1.8: NRZ and RZ pulse shaping for a multi-bit DAC.

For a wideband uncorrelated clock jitter, jitter error energy can be written as[21]:

$$\sigma_{e_{NRZ}}^2 = \sigma_{\Delta y,NRZ}^2 \frac{\sigma_{\Delta t}^2}{T_s^2} \tag{1.38}$$

$$\sigma_{e_{RZ}}^2 = 8\,\sigma_{y,RZ}^2 \frac{\sigma_{\Delta t}^2}{T_s^2} \tag{1.39}$$

As shown, the RZ DAC is more sensitive to clock jitter than the NRZ DAC because the clock jitter affects both the rising edge and falling edge of every clock while in NRZ pulses only one edge is affected by jitter noise during T_s. In addition, RZ DAC pulses have smaller duty-cycles. In NRZ, the variance of the error is proportional to the difference of the two adjacent output levels while in RZ, it is related to the current output level as shown in Fig. 1.8. Consequently, using a multi-bit quantizer in the CT modulator will reduce the jitter noise effect appearing in NRZ. SNR improvement using a NRZ pulse shape over a RZ pulse is:

$$SNR_{NRZ-RZ} = 10\,log_{10}\left(\frac{8\,\sigma_{y,RZ}^2}{\sigma_{\Delta y,NRZ}^2}\right) \tag{1.40}$$

In addition to the current steering DACs with rectangular pulse shapes, exponentially decaying DACs, also called switch-resistor-capacitor (SRC) DACs, are used in the CT ΔΣ modulator. This type of DAC operates like a SC DAC used in the DT modulator. Fig. 1.9 shows the simplified circuit diagram of an RC integrator with SCR feedback DAC [22]. The feedback is applied through charging and discharging a capacitor. A resistor can be added in series with the DAC capacitor to adjust the time constant.

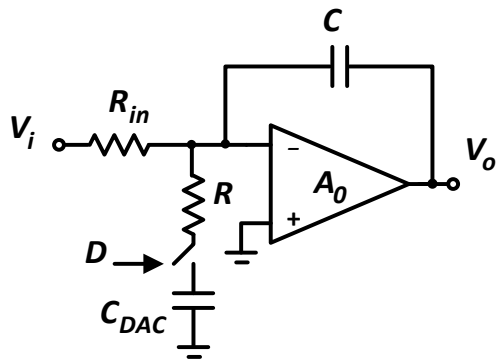


Fig. 1.9: Active-RC integrator with SCR feedback DAC.

Since the DAC output is much lower at the end of integration phase compared to the beginning of the phase, clock jitter has less impact on the transferred charge in the SRC DAC than rectangular pulse DACs where the DAC output is constant in every cycle. However this implementation suffers from several drawbacks. First, the front-end integrator's opamp suffers from degredation of the feedback factor as in conventional SC-DAC. For high-speed applications, the value of the resistor *R* needs to be small to allow complete charge transfer in each clock phase, resulting in high spike currents which will increase the slewing requirements of the opamp. In general the most effective way to reduce the effect of the clock jitter is to use a multi-bit quantizer and employ the NRZ-DAC pulse shape.

1.4 PERFORMANCE COMPARISON OF THE CT AND DT ΔΣ MODULATORS

Table 1.1 summarize the performance comparison between the state-of-the-art CT and DT ΔΣ modulator designs. To have a better comparison, Fig. 1.10 plots the figure-of-merit (FOM) versus SNDR, where the FOM is defined as:

$$FOM = \frac{Power}{2.BW.2^{(\frac{SNDR-1.76}{6.02})}} \tag{1.41}$$

TABLE 1.1: PERFORMANCE COMPARISON

Reference	*Type*	*Process [µm]*	*SNDR [dB]*	*BW [MHz]*	*Power [mW]*	*FOM [pJ/conv.]*
[18] Z. Li	CT	0.25	80.5	2.5	50	1.15
[24] R. Schoofs	CT	0.18	65	10	7.5	0.24
[25] G. Mitteregger	CT	0.13	74	20	20	0.12
[26] P. Malla	DT	0.09	64	20	27.9	0.52
[27] V. Dhanasekaran	CT	0.065	60	20	10.5	0.32
[28] S. D. Kulchycki	CT-DT	0.18	67	7.5	63.6	2.1
[29]T. Christen	DT	0.25	63	10	20.5	0.9
[30] T R. Veldhoven	CT	0.065	77	0.2	0.95	0.43
[31] H. Park	DT	0.18	95	0.025	0.87	0.39
[32] P. Crombez	CT	0.09	65	10	6.8	0.23
[33] K. Matsukawa	CT	0.11	62.5	10	5.32	0.24
[34] R. Van Veldhoven	CT	0.045	56.3	15	9	0.58
[35] K. Lee	DT	0.18	81	2.5	15	0.33
[36] L. Bos	DT	0.09	65	2	6.83	1.17
[37] M. Bolatkale	CT	0.045	65	125	256	0.7
[38] J. G. Kauffman	CT	0.09	63.5	25	8	0.13
[39] F. Michel	DT	0.13	61	0.01	0.0075	0.41
[40] B. R. Carlton	DT	0.032	63	20	28	0.61
[41] O. Rajaee	DT	0.18	73.7	5.33	13.9	0.33
[42] Y. Ke	CT	0.09	58	20	8.5	0.32
[43] M. Vahidpour	CT	0.065	84	0.1	2.1	0.81
[44] J. Chae	DT	0.18	63	20	16	0.35
[45] Paramesh	DT	0.09	63	20.5	78	1.64
[46] R. Jiang	DT	0.18	81.6	2	149	3.8

It is clear from Fig. 1.10 that the design having lower FOM with higher SNDR is the most optimum design. The lowest FOM between the DT deigns in Table 1.1 is 327fJ/conversion having a BW and SNDR of 2.5 MHz and 81 dB, respectively. Among the CT modulator designs, the most optimum design in term of FOM has an FOM of 129 fJ/conversion with an SNDR and BW of 73.5 dB and 20 MHz, respectively. Considering Fig. 10, it is obvious that the CT modulators were able to achieve lower FOM compared to the DT modulators.

Hence achieving a high SNDR along with a wide BW is challenging in design of the ΔΣ modulators, Fig. 1.11 shows the modulator BW versus SNDR for the state-of-the-art CT and DT ΔΣ modulators. The highest BW among the CT modulators is 125 MHz with an SNDR of 65 dB. Between the DT ΔΣ modulators, the most optimum design in term of BW and SNDR has a BW of 20 MHz and SNDR of 67 dB. Again the performance comparison among the CT and DT ΔΣ modulators shows that the CT modulators have achieved higher signal BWs.

As a result of these two comparison factors, a modulator with higher SNDR and BW, and lower FOM will be an optimum and also challenging design.

1.5 SUMMARY

In this chapter, a review of discrete-time and continuous-time delta-sigma modulators has been presented. Oversampling ΔΣ modulators are the best choice for the high resolution and high speed applications such as wireless and wire-line communication. However, there are several practical issues that will limit their performance. These effects were studied and some solutions and techniques were discussed. Consequently, in the next two chapters, different circuit and system level innovative approaches are introduced in both CT and DT ΔΣ modulators which make their design optimum and efficient in terms of power consumption and chip area with a reduced FOM factor.

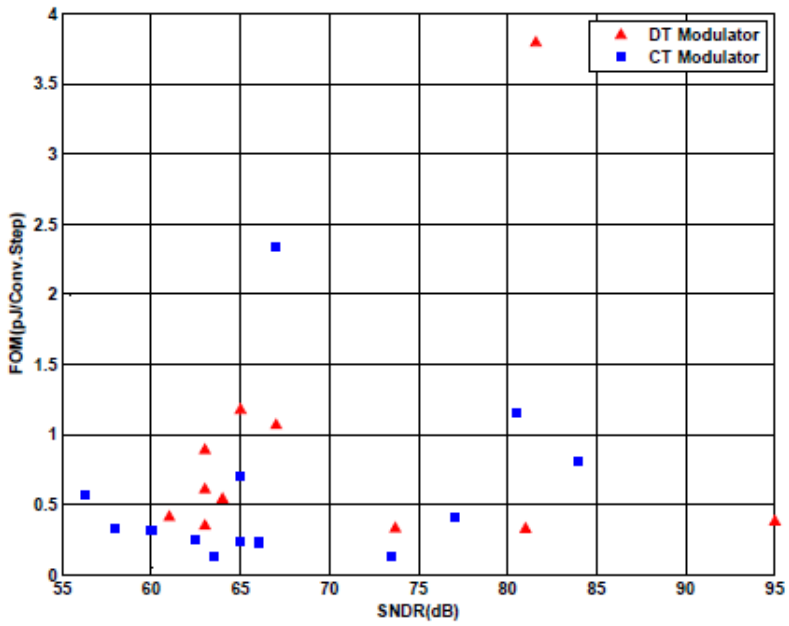


Fig. 1.10: FOM versus SNDR for CT and DT modulators.

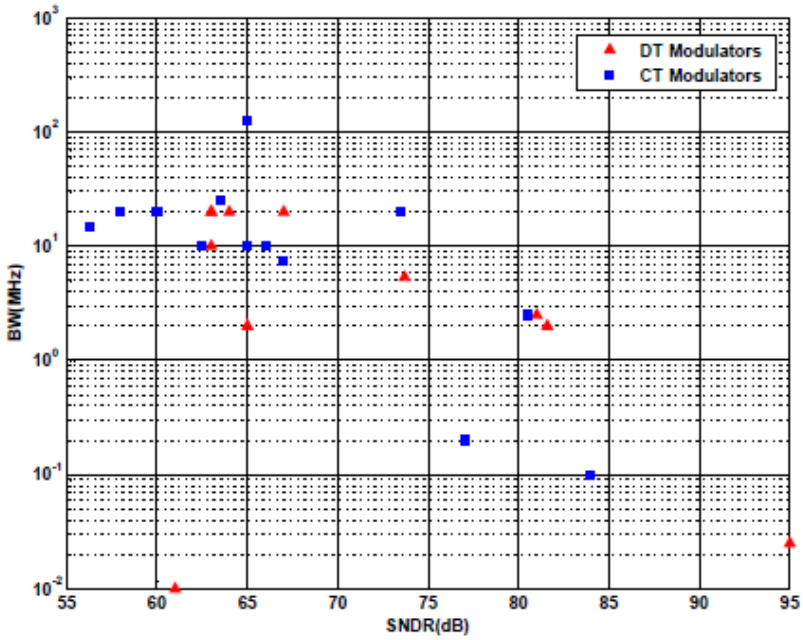


Fig. 1.11: BW versus SNDR for CT and DT modulators.

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CHAPTER 2. AN 80-dB DR, 10-MHz BANDWIDTH SINGLE-OPAMP-BASED CT ΔΣ MODULATOR DISSIPATING 11.4-mW

Abstract

A novel low power compact loop filter using a single amplifier biquad (SAB) filter is presented for continuous-time (CT) delta-sigma (ΔΣ) modulators. This new technique saves power consumption and die area by minimizing the number of active elements in the modulator. Additionally, because the new technique reduces the feedforward branches to the summing block in the modulator, a switch-capacitor (SC) adder replaces the commonly used CT adder and the sample & hold blocks in the conventional architecture. These two techniques simplify the design and implementation of the high-order continuous-time ΔΣ modulator. The proposed loop filter is a general filter which can be used for both high and low oversampling ratios (OSRs). A 4th-order low pass continuous-time ΔΣ modulator is designed and implemented in 130nm IBM process to confirm the effectiveness of the proposed techniques. With a 10 MHz signal bandwidth, the measured dynamic range and SFDR of this prototype IC are 80 dB and 82.4 dB with an analog power consumption of 11.4 mW.

2.1 INTRODUCTION

There is a significant need in the future wireless communication products for high-performance analog-to-digital converters (ADCs) that have a wide signal bandwidth in the region of several megahertz and a resolution of more than 10 bits. However, the reduction in supply voltage that accompanies reduced transistor dimensions makes it difficult to realize high performance analog circuits. With the reduction in supply voltage, the dynamic range is also reduced. To keep the same performance, either the architecture must be changed or the thermal noise of the analog components must be reduced, which in turn will normally increase the power dissipation. The conventional architecture for a wireless communication ADC is a pipelined architecture [1]. This architecture requires an analog anti-aliasing filter (AAF) and, while the supply voltage is reduced, it is increasingly difficult to meet the required accuracy of >10 bits. Discrete-time (DT) ΔΣ

ADCs normally operate with very large oversampling ratios (OSR) [2]. They can operate at very low supply voltages, but still requires a simple analog AAF because of the sampled nature of the circuit. It is challenging to extend the signal bandwidth while achieving a resolution >12 b because of the unity-gain frequency requirements of the amplifiers in SC integrators. Recent research has led to DT modulators with nearly 4 MHz bandwidth but with resolutions of 11 bits [3], [4]. The largest signal bandwidth reported recently for a DT modulator is 4.5 MHz, but with only 11 bits of resolution [5].

Compared with DT converters, CT converters have the advantages of lower power consumption and inherent anti-aliasing filtering. Plus, they do not suffer from noise aliasing because of the continuous-time (non-sampled) loop filter. The non-sampled CT ΔΣ circuits also make the circuit less susceptible to high-frequency noise pickup, such as substrate noise generated by digital circuits. Moreover, the absence of stringent settling requirements enables CT converters to digitize signals up to several hundred MHz, which is still not possible for their DT counterparts. All these advantages result in an extended battery life and reduced system complexity, which are especially important for portable wireless devices.

Recent CT modulators have achieved bandwidths of 10 MHz in 0.18-µm CMOS technology [6], [7] and 15 MHz [8] and 20 MHz [8] in 0.13-µm CMOS technology, all with a resolution of 11 bits or more. These results suggest that CT implementations are capable of operating at signal bandwidths difficult to achieve with DT designs while still maintaining high resolution.

This chapter describes the architecture design and circuit realization of a biquad filter-based CT ΔΣ modulator with an increased stability range, implemented in 0.13-µm CMOS technology. A novel single amplifier biquad (SAB) network is developed to be utilized in the proposed modulator topology which can be used in either high or low OSR applications. In other word, both zero-optimized and non-zero-optimized modulator noise transfer functions (NTFs) can be realized by the proposed network. Using a SAB network decreases the power consumption and die area of the CT ΔΣ modulator by reducing the number of active blocks in the modulator. In addition to the proposed SAB networks, an SC adder is used as a summing block in the modulator instead of the conventionally utilized CT adder and the sample-hold block.

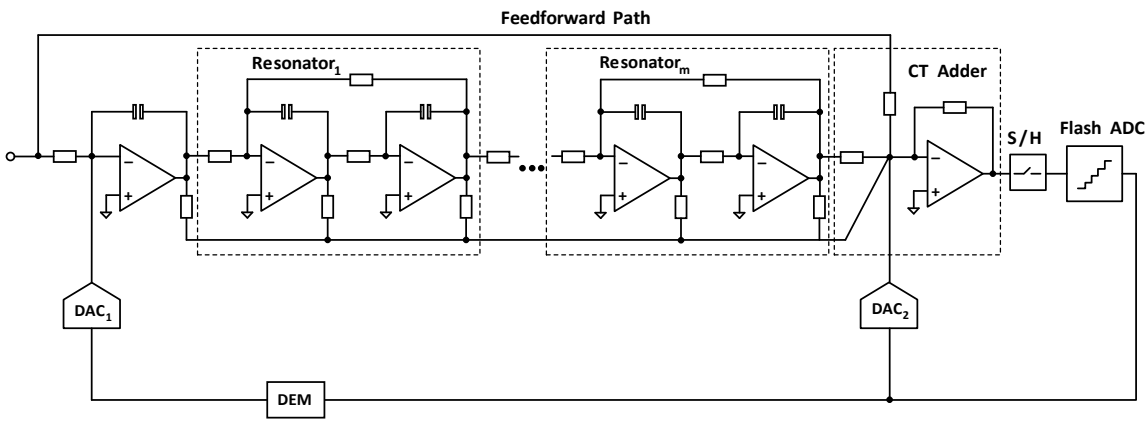


Fig. 2.1: General block diagram of a conventional Nth-order CT ΔΣ modulator.

2.2 GENERAL ARCHITECTURE OF THE SAB BASED CT ADC

Figure 2.1 shows a typical *Nth*-order configuration of feedforward CT ΔΣ ADC which has the most suitable configuration of the loop filter for low power [10]. The modulator loop filter has *N* active integrator blocks and *N* feed forward branches going to the adder block. The modulator utilizes a flash-ADC as a multi-bit quantizer and also uses a dynamic element matching (DEM) to decrease the nonlinearity effect of the front-end DAC. The zero order feedback path to the input of the quantizer is required to improve the modulator stability and compensate excess loop delay introduced by the circuit delays from the output of the sampler block to the output of the DAC blocks [11]. To realize the modulator with over 12 bit accuracy and bandwidth higher than 5 MHz, a 4th-order noise transfer function with at least one pair of in-band zeros and a multi-bit quantizer is required. However, high-order modulators require more operational amplifiers (opamps), because each first-order integrator consists of an opamp, a resistor and a capacitor. The finite gain bandwidth (GBW) of the opamps in the integral path of the modulator causes large phase delay, which makes the feedback loops unstable. More analog power consumption is required to enhance the opamp GBW and improve the loop phase delay effect. Therefore, reducing the number of opamps in high order modulators will enhance the achievable figure of merit (FOM), because that greatly decreases the power consumption, loop phase delay, and modulator total die area. Before introducing the

proposed SAB network and other techniques used in the CT modulator, recently published power saving techniques for CT ΔΣ ADC are explained in detail. Advantages and disadvantages of those methods are described and a new network which overcomes the limitations of existing techniques is proposed in Section 2.2.2.

2.2.1 Conventional Power Saving Techniques for CT ΔΣ

The loop filter is the main block of a CT ΔΣ modulator. It dissipates a significant amount of the total energy and occupies a major portion of the modulator die area. It has a continuous-time transfer function (TF) with large gain within the signal band while it attenuates out-of-band signals. There are two types of commonly used continuous-time active integrators to realize a loop filter: R-C integrators, Gm-C integrators. Active-RC based loop filters have the widest dynamic range, but they consume more power due to the larger number of active blocks. In addition to the active integrators, it is more common to use passive networks because they do not consume power. Meanwhile, using all passive networks is not practical in CT ΔΣ modulators because the gain of a passive network is less than one. Consequently, it will attenuate in-band signals and will make it more difficult to design a sensitive and fast comparator with very low input referred noise [12]. As an alternative, SAB networks which are a combination of active and passive filters and use just one operational amplifier, instead of two, can be used in the modulator loop filter to reduce the power consumption. SAB-based loop filters have all the benefits of the both active and passive filters.

Figure 2.2 depicts an *Nth*-order CT ΔΣ modulator architecture with *m* cascaded biquad networks in the loop filter (the last integrator is removed for an odd number of N). As examples, [13], [14] have developed CT modulators with cascaded biquad filters. In [13], a single amplifier resonator (SAR) network is introduced for a 5th-order CT ΔΣ modulator. It is demonstrated in Fig. 2.3 and it is suitable for high bandwidth (or low OSR) applications.

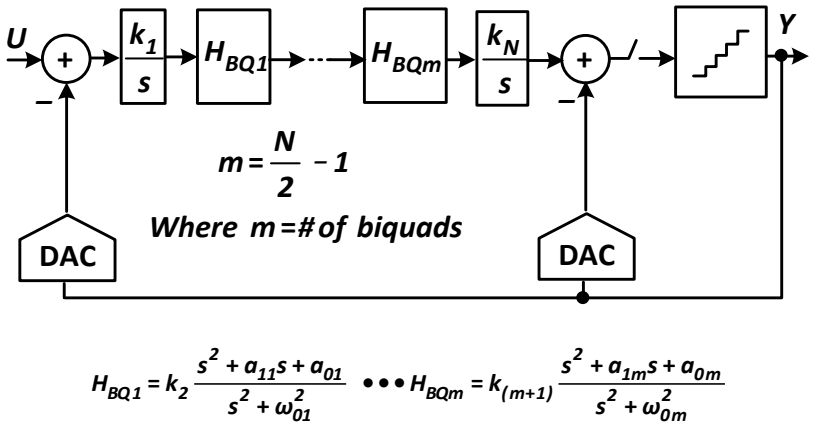


Fig. 2.2: *Nth*-order CT ΔΣ modulator topology with cascaded biquad stages.

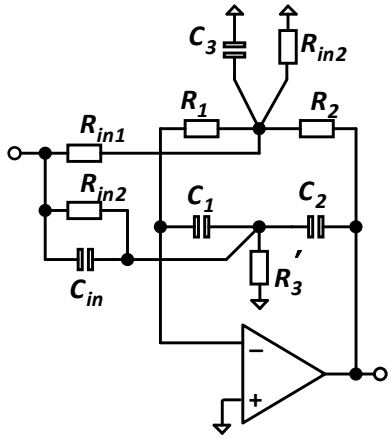


Fig. 2.3: Single Amplifier Resonator developed by [13].

This network uses one active block for a second-order network saving power and area especially for the higher order modulators. Also, it does not include a first-order Laplace term in the denominator meaning that the network has a resonating transfer function which can be utilized to implement zero optimized noise transfer functions. However, the proposed SAR network in [13] originally had a third-order transfer function instead of a second-order. By considering the two assumptions shown in (2.2), the initial third-order TF reduces to a second-order TF according to (2.1). Satisfying these assumptions is not guaranteed because of the process variations which changes the value of the network resistors and capacitors. As a result, the modulator will not have the desired NTF which can consequently result in modulator instability.

$$\frac{V_{out}}{V_{in}} = -\frac{\frac{C_{in}}{C_2}s^2 + \frac{1}{C_2 R_{in2}}s + \frac{1}{C_1 C_2 R_1 R_{in1}}}{s^2 + \frac{1}{C_1 C_2 R_1 R_2}} \tag{2.1}$$

$$R_3' \, II \, R_{in2} = R_1 \, II \, R_2 \, II \, R_{in2} \, II \, R_{in1} \tag{2.2}$$

$$C_3 = C_1 + C_2 + C_{in}$$

As the other disadvantage of this SAB network, it cannot be used in the ADC front-end, the most power hungry block of the modulator, since the input signal is not applied to the virtual ground of the operational amplifier in the network.

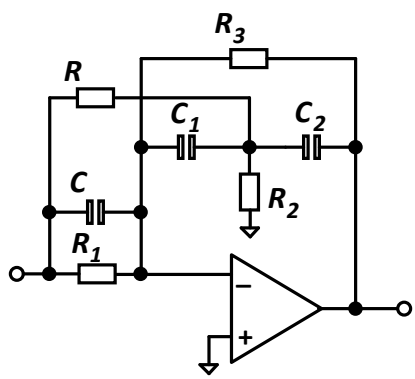


Fig. 2.4: Single Amplifier Biquad developed by [14].

On the other hand, a fifth-order CT ΔΣ modulator with cascaded biquad networks is introduced in [14] which uses a single amplifier biquad networks in the loop filter. Figure 2.4 demonstrates a SAB network which initially has a second-order TF with a reduced number of passive components compared to [13]. According to (2.3) and (2.4), the SAB network includes a first-order Laplace term in the denominator unlike [13]. This term creates a leakage effect in the modulator final performance but it can be attenuated by choosing a relatively high value for R_3.

$$\frac{V_{out}}{V_{in}} = -\frac{s^2 + \frac{1}{C_1}(\frac{2}{R_1} + \frac{3}{2R} + \frac{1}{2R_2})s + \frac{1}{C_1C_2R_1}(\frac{1}{R_2} + \frac{1}{R})}{s^2 + \frac{2}{C_1R_3}s + \frac{1}{C_1C_2R_3}(\frac{1}{R_2} + \frac{1}{R})} \tag{2.3}$$

$$C_1 = C_2 = 2C \tag{2.4}$$

The other advantage of this network is that it can be utilized in the ADC front-end because the input signal is applied to the operational amplifier virtual ground, unlike [14]. As mentioned before, both techniques [13]-[14] are applied in the loop filter of the CT ΔΣ modulators with cascaded biquad networks. These modulator topologies require amplifiers with higher gain bandwidth (GBW) requirements. That is due to of the accumulated delay in the loop filter from the ADC front-end to the input of the quantizer block and it can cause instability.

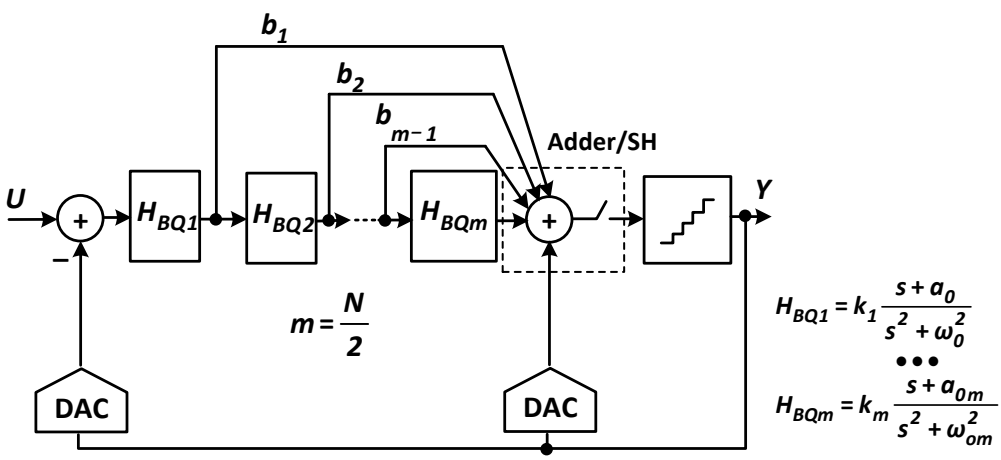


Fig. 2.5: Stability improved biquad based CT ΔΣ modulator architecture.

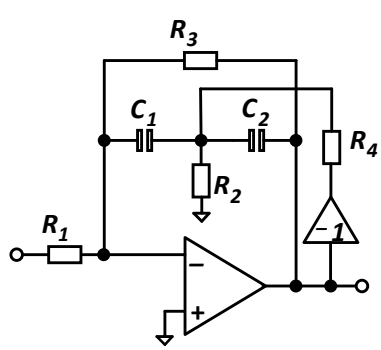


Fig. 2.6: Proposed single amplifier biquad network.

2.2.2 The Proposed Stability Improved Topology

Figure 2.5 shows the proposed biquad based CT ΔΣ modulator with improved stability. In this topology, feedforward branches from the output of the biquad networks to the adder block increase the stability range of the modulator. This is due to the reduced delay introduced by the finite GBW of the loop filter active blocks. This modulator architecture uses an active adder block instead of a passive one used in [13]. As the main drawbacks of a passive adder, it introduces a gain attenuation which needs to be compensated by boosting the loop filter gain and an extra pole at the input of the quantizer which can reduce the modulator stability range. While this architecture decreases the number of feedforward branches from *N* to *N/2*, the feedback factor of the active adder block is enhanced compared to an *Nth*-order conventional CT ΔΣ modulator as depicted in Fig. 2.1. Consequently, a SC adder block can be utilized instead of the commonly used CT adder and sample-and-hold blocks in the conventional architecture. In this way, the SC adder will act both as a summing block and the sampler block eliminating one more active block reducing power and die area. Figure 2.6 depicts the improved SAB network which has all the advantages of the network introduced in [14], plus the positive feedback path using R_4 in the proposed network removes the first-order Laplace term from its TF denominator as demonstrated in (2.5). This can be done by properly setting the value of R_4 according to (2.6).

$$\frac{V_{out}}{V_{in}} = -\frac{1}{C_1 C_2 R_1} \cdot \frac{(C_1 + C_2)s + (\frac{1}{R_2} + \frac{1}{R_4})}{s^2 + \frac{1}{C_1 C_2 R_3}(\frac{1}{R_2} + \frac{1}{R_4})} \tag{2.5}$$

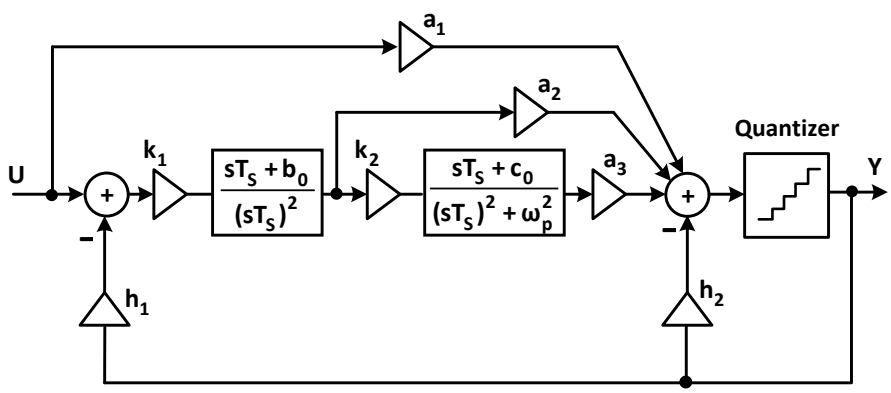
$$R_4(C_1 + C_2) = R_3 C_1 \tag{2.6}$$

Eliminating the first-order Laplace term in the SAB transfer function shifts the complex-conjugate poles of the SAB TF from the LHP to the imaginary axes. This helps the NTF of the modulator have a perfect pair of optimized zeros. As a benefit of R_2, it improves the phase margin of the operational amplifier embedded in the SAB network and along with R_4 can be used as the common-mode detector for the opamp in the

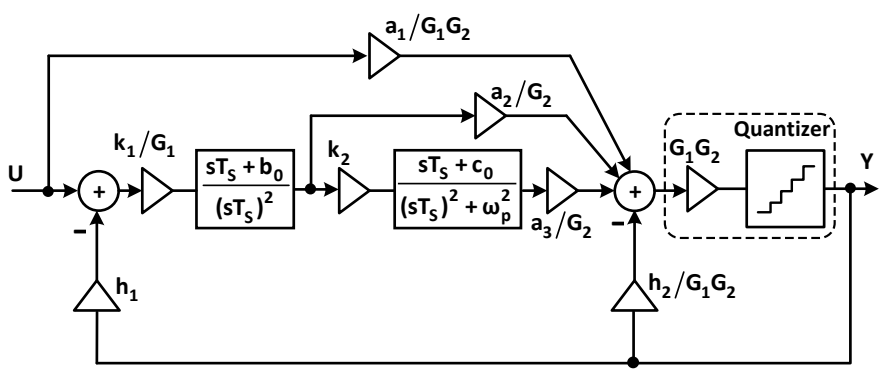
differential topology. While the SAB network is used in the loop filter of the modulator with an overall negative feedback, the local positive feedback in the network cannot cause any instability.

2.3 SYNTHESIS OF THE PROPOSED 4th-ORDER SAB BASED CT ΔΣ

The target specification for the proposed SAB based CT modulator in this paper is defined to be 13 bits with an input signal bandwidth of 10 MHz. The modulator maximum power dissipation is aimed to be less than 15 mW using different circuit level and system level techniques. Firstly, all the noise sources of a CT modulator such as quantization noise of the inner flash- ADC, thermal noise of the all circuit components, clock jitter, DAC unit mismatches, and the quantizer imperfections are analyzed for the noise budgeting.



(a)



(b)

Fig. 2.7: Proposed 4th-order SAB based CT modulator architecture (a) without gain scaling (b) with gain scaling techniques.

TABLE 2.1: MODULATOR NOISE BUDGETING

Noise Source	*Noise Budget (%)*	*SNR (dB)*
Quantization Noise	8	89.2
Thermal Noise	25	84.3
Clock Jitter	35	82.8
Quantizer Error	7	89.8
DAC Mismatch	15	86.5
Other Noise Sources	10	88.3

Furthermore, these are the main noise sources for the modulator non-idealities which degrade the performance. Noise budgeting is summarized in Table 2.1 based on the power consumption reduction and also the practical design challenges and limitations in the CT ADC design. As shown, thermal noise and clock jitter are the two dominant noise sources in the CT modulator design. The clock jitter noise budget is determined by the phase noise of the off-chip clock source.

2.3.1 Modulator Gain Coefficient Scaling Techniques

Based on extensive simulations in MATLAB, a fourth-order, 4-bit (with 16 output levels) topology is chosen. The clock frequency is 250 MHz for a 10 MHz input signal bandwidth. Taking only quantization noise into account, the ideal peak SNDR is about 90 dB. Figure 2.7(a) depicts the system level block diagram of the 4th-order CT modulator using the biquad networks and feedforward branches. In this architecture, the modulator NTF has one pair of non-optimized zeros and another pair of optimized zeros introduced by the first and the second biquad filters, respectively. The modulator architecture utilizes a feedforward path from the modulator input to the adder block implementing the low-distortion architecture. The low-distortion architecture bypasses the input signal term from the loop filter and directly applies it to the summing block. As demonstrated in Fig. 2.7(b), two different system level scaling techniques are utilized in the proposed modulator topology to optimize the design and relax the modulator complexity. First

scaling technique is introducing $G_1(>1)$ in front of the flash-ADC block and consequently reducing the gain factors in SAB_1, DAC_2 and the direct feedforward path by G_1. This decreases the output swing and GBW requirements of the operational amplifier in SAB_1 [15]. However, decreasing the gain of SAB_1 has a trade-off with either increased resistor or capacitor values used in the first biquad network as illustrated in (2.5). Increasing the resistor sizes in SAB_1 enhances the modulator input referred thermal noise and requires more power. On the other hand, having larger capacitors increases the power consumption of the SAB opamp and occupies more die area on the chip. The second scaling approach is accomplished by amplifying the signal at the input of the quantizer by $G_2(>1)$ and putting $1/G_2$ gain attenuation through all the feedforward branches connected to the adder block. This method boosts the adder block's feedback factor to reduce the power consumption and lowers the signal swing at the output of the summing block to decrease the amplifier output swing requirement. Therefore, larger amplitude input signals can be applied to the modulator front-end to enhance ADC dynamic range. That is feasible due to the absence of the input signal in the loop filter of this architecture. Meanwhile, the input signal gets attenuated after the adder block to prevent saturation of the inner quantizer. Now the only concern is how to efficiently amplify the signal by $G_1.G_2$ after the adder block. The most power efficient way to implement $G_1.G_2$ is by shrinking the the flash-ADC reference voltages by $1/(G_1.G_2)$. Meanwhile, there is a trade-off between scaling down the quantizer reference and the increased complexity in the design of the quantizer comparators with reduced quantization intervals. As a result, there is an optimum value of $G_1.G_2$ for which SAB_1 and the adder blocks have relaxed opamp requirements and comparators do not have circuit complexity. Table 2.2 shows all the gain coefficients of the proposed modulator for optimum gain scaling.

2.3.2 Clock Jitter Sensitivity

The clock jitter effect as one of the design challenges for a CT modulator and is a dominant factor in the front-end DAC block since it is not attenuated by the order of the modulator. This is unlike the jitter noise introduced in the SC adder and the second DAC

which will be shaped by the modulator. Jitter sensitivity of a CT A/D modulator is also determined by the DAC choice. In this design, a non-return-to-zero (NRZ) DAC pulse shape is chosen mainly for its low sensitivity to clock jitter. An approximate equation which expresses the signal-to-jitter noise ratio of a CT ΔΣ modulator is illustrated in (2.7) while A is the sinusoidal input signal amplitude, OSR is the oversampling ratio, T is the sampling clock period, $\sigma_{\Delta t}$ is the clock jitter standard deviation, and $\sigma_{\Delta y,NRZ}$ is the standard deviation of adjacent modulator output difference [16].

$$\begin{aligned} SNR_{jitter} &= \frac{P_s}{P_{jitter}} \\ &= \frac{A^2/2}{\sigma^2 e_{NRZ}/OSR} \\ &= \frac{OSR.A^2}{2\sigma^2_{\Delta y,NRZ}(\frac{\sigma_{\Delta t}}{T})^2} \end{aligned} \tag{2.7}$$

The NRZ DAC pulse will result in reduction of the jitter sensitivity because of the lower value of $\sigma_{\Delta y,NRZ}$. On the other hand, it does not go to zero between the two adjacent output data unlike the RTZ and HRZ DAC pulse shapes. Figure 2.8 shows the simulated SNDR for -1.5 dBFS input for different clock jitter rms values. It should be noted that the simulations include both the quantization noise and the jitter noise. To ensure that the total power of the quantization noise and the jitter noise is 82 dB below the input signal power, the clock jitter rms value must be less than 3.2 ps, placing a very stringent requirement on the clock signal generator.

2.3.3 Loop Filter Coefficient Variations

One of the major disadvantages of CT modulators is the large time constant variations compared to DT modulators and thus careful examination at the system level is needed. A worse case simulation is shown in Fig. 2.9 where RC time constants in the two SAB networks are assumed to vary by the same percentage. As shown in Fig. 2.9, when the time constants, i.e., the products of resistors and capacitors, become smaller than their

nominal values, the integrator gains increase and the SNR improves. However, when the time constants decrease by -13% of their nominal values, the SNR decreases and the modulator becomes unstable due to excessive loop gain. On the other hand, if the time constants are larger than their nominal values, the loop gain decreases so that the noise shaping is less efficient; as a result, SNDR drops gradually.

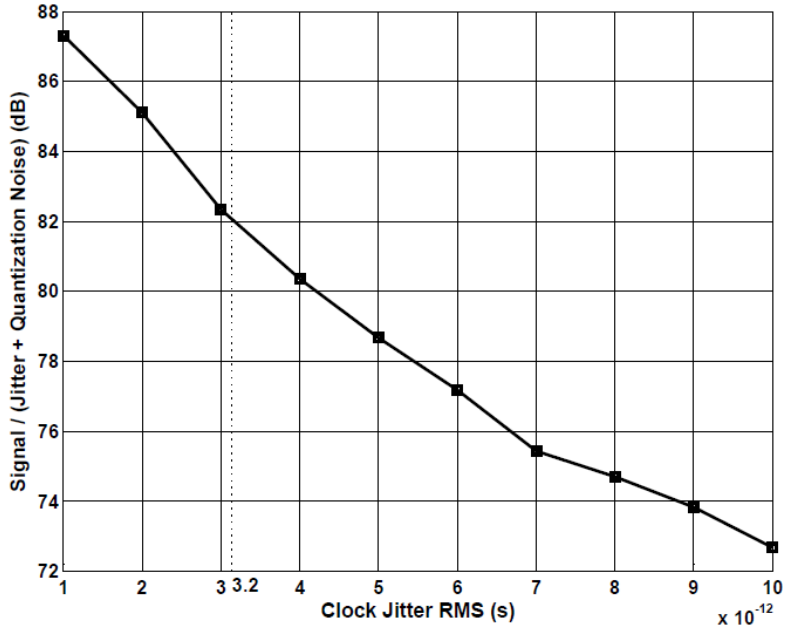


Fig. 2.8: SNDR sensitivity to clock jitter.

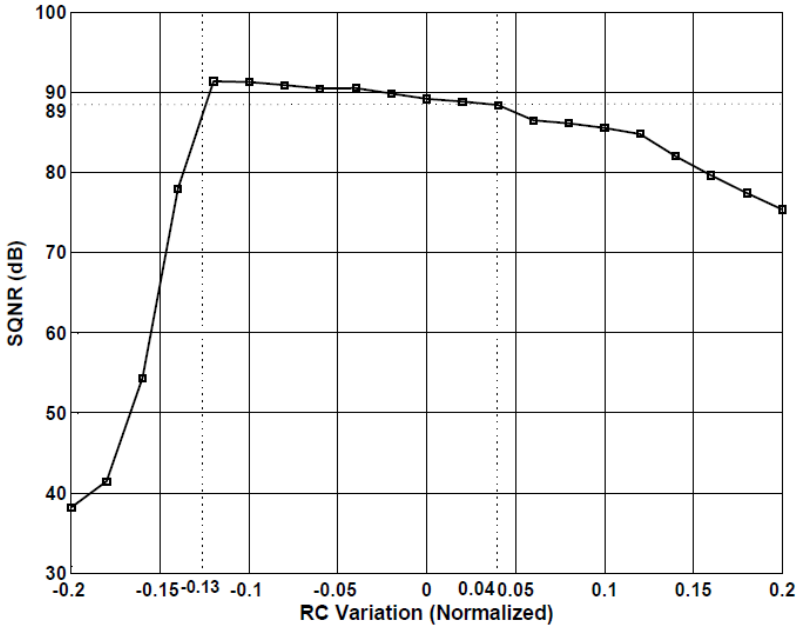


Fig. 2.9: SNDR (-1.5 dBFS input) vs. the normalized time constant.

TABLE 2.2: MODULATOR GAIN COEFFICIENTS.

Gain	*Value*
a_1	3
a_2	0.63
a_3	0.63
k_1	2.36
k_2	0.32
h_1	1
h_2	2
b_0	0.32
c_0	0.45
G_1	2
G_2	1.5
ω_p	0.21

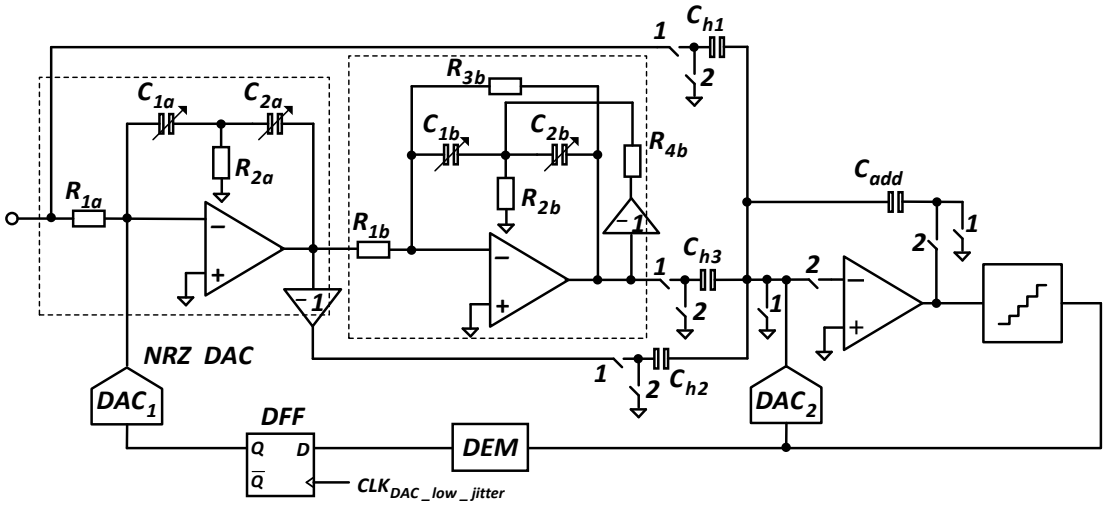


Fig. 2.10: Block diagram of the proposed 4th-order ΔΣ ADC.

From Fig. 2.9 we see that for time constants in the range of -13% and 4%, the modulator can achieve more than 89 dB SNDR for -1.5 dBFS input. To extend the tolerable time constant variation, the loop filter coefficients are centered at -8% of the nominal time constant. By doing this, the time constants can vary by almost ±8% without

significantly degrading SNDR. Since it is not uncommon for the *RC* time constants to vary by 25%, some on-chip tuning is still needed.

2.4 CIRCUIT REALIZATION OF THE PROPOSED CT ΔΣ ADC

Figure 2.10 illustrates the configuration of the proposed fourth-order low-pass, 4-bit CT ΔΣ ADC. Single-opamp biquad filters are embedded for low power operation. Reducing the number of opamps is the most effective means to reduce power consumption and improve the phase delay and the modulator stability. As mentioned before, an SC adder circuit is utilized to simplify the design. While the proposed SAB based topology decreases the number of feedforward branches going to the adder block and consequently boosts the feedback factor of the adder block's opamp, the SC adder becomes a power efficient solution by eliminating the sample and hold block.

2.4.1 Loop Filter

The fourth-order loop filter of this design is implemented with a single-stage, dual-loop CIFF (Chain of Integrators with Feed-Forward branches) architecture, as shown in Fig. 2.10. The loop filter consists of two SAB networks to implement the modulator NTF.

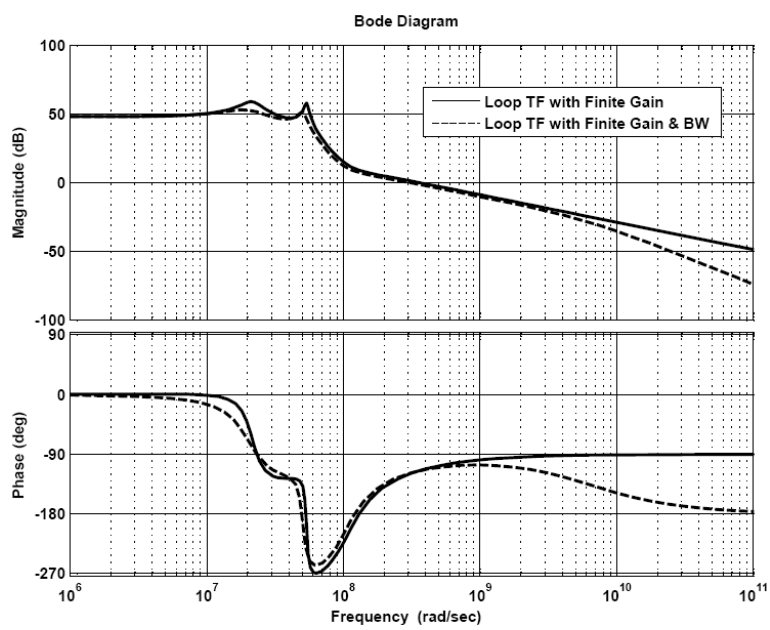


Fig. 2.11: Frequency response of the SAB base loop filter.

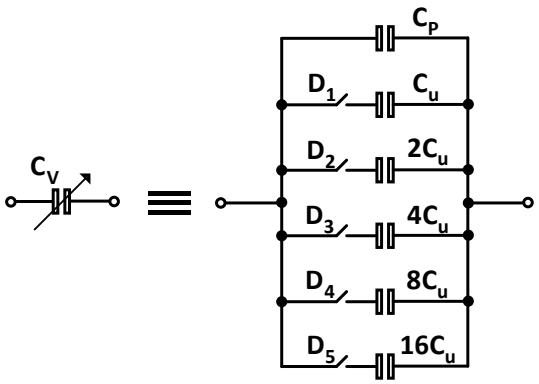


Fig. 2.12: Tunable capacitor array.

The first SAB (SAB_1) realizes the non-optimized zeros of NTF and the second SAB network resonates at the frequency of the NTF optimized zeros. SAB_1 is located at the ADC front-end; hence, it has few resistors compared to SAB_2, it will have lower input referred thermal noise. Figure 2.11 depicts the magnitude and the phase response of the loop filter considering the finite gain and bandwidth effects of two SAB amplifiers.

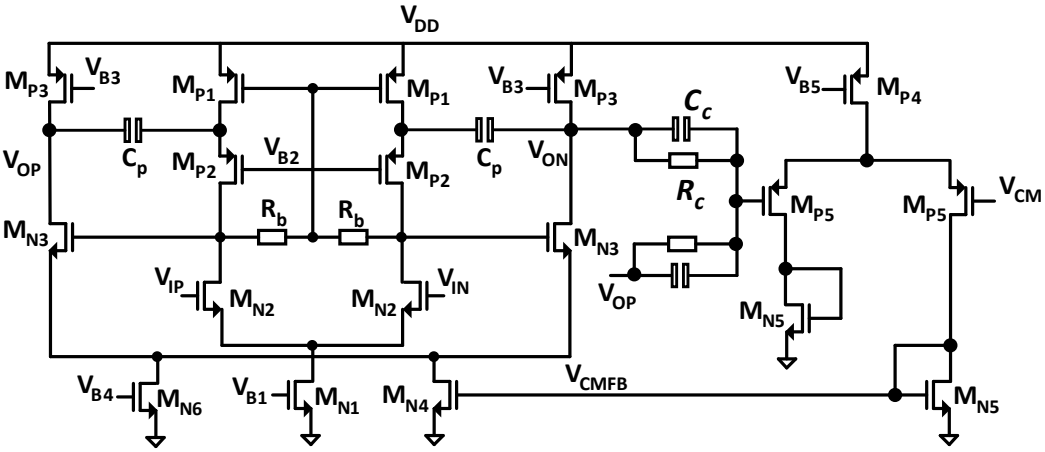


Fig. 2.13: Two-stage amplifier with cascode compensation utilized in the first SAB network.

As shown in Fig. 2.11, the peaking close to the signal bandwidth is created by SAB_2 resonating poles while the other magnitude peaking at lower frequency is caused by the

opamp finite gain effect in SAB_1. This desirable effect automatically optimizes and moves the non-optimized NTF zeros from the origin on the unit circle in z-domain.

Unlike the DT A/D modulator where the loop coefficients are determined by capacitor ratios and can be as accurate as 0.1%, the loop coefficients in CT A/D modulators are determined by products of resistor and capacitor values which can vary by as much as 25% in today's CMOS processes. In this design, integration capacitors in all integrators are realized by an adjustable capacitor array as shown in Fig. 2.12 [11]. The capacitors in the arrays are binary-sized except the "always-in-use" capacitors. This sizing method provides constant tuning steps with the least number of capacitors. The 5-bit digital control codes are fed externally to choose which capacitors to use. The value of C_P and C_U are chosen such that $(C_P + 8C_U)$ equals the nominal value of the integration capacitor. The ratio between C_P and C_U is chosen to be 24, thus, the tuning range and tuning accuracy are 2.3 and 3.1%, respectively. This is enough to meet the requirements for the gain coefficient variation according to simulation results shown in Fig. 2.9.

Input resistors of the first SAB network play a critical role in defining the total input-referred thermal noise of the modulator. Therefore, choosing a smaller resistance results in bigger capacitors for the front-end SAB filter. To achieve sufficient resistive and capacitive load drivability with higher voltage swing, a two-stage amplifier topology is employed in SAB_1. The amplifier schematic is shown in Fig. 13. The first stage of the amplifier is a telescopic circuit, providing most of the amplifier dc gain. The second stage of the amplifier is a simple 5-transistor amplifier with an nMOS input differential pair instead of a common-source pair with pMOS loads. This will make the biasing points of the second stage almost independent from the first stage. The second stage has minimal voltage gain but provides a low output impedance to drive the resistive load from SAB_2, common-mode sensing resistors and the amplifier load. The CT integrator amplifier employs cascode-compensation instead of the miller-compensation because the cascade-compensation reuses the first stage to realize the compensation resistor without consuming an extra power. The output common-mode (CM) voltage is then sensed by resistor R_c. With the common-mode feedback circuit, the integrator output common-mode voltage is set to a reference voltage V_{CM}. The capacitor C_c in parallel with R_c is used to improve the amplifier phase margin by putting a left-half-plane (LHP) zero in the

amplifier TF. For the first stage of the amplifier, the R_b resistor acts as the common-mode detector which feeds back the sensed CM voltage directly to transistor M_{P1}. A simple single-stage telescopic amplifier is used in the second SAB filter and the summing block which is power efficient and fast. While these two blocks have lower swing requirements and reduced resistive and capacitive loads because of the noise scaling in the loop filter, there is no need for the two-stage amplifier. The performance specifications of the CT amplifiers are summarized in Table 2.3. For a nominal sampling frequency of 250 MHz, the CT SAB amplifier unity-gain frequencies are relatively low. For a comparable DT integrator amplifier, assuming the amplifier unity-gain frequency must be at least five times the modulator sampling rate, the amplifier unity-gain frequency for a sampling rate of 250 MHz system would be 1.25 GHz compared to 0.875 GHz in this design and would dissipate significantly more power than the CT implementation.

TABLE 2.3: SPECIFICATION TABLE OF THE AMPLIFIERS.

Amplifier	*Type*	*Gain (dB)*	*Gain BW (Hz)*	*Cap Load (pF)*	*Current (mA)*
1st SAB	Two-Stage	50	$3.5xf_{CK}$	3.5	4.5
2nd SAB	Telescopic	35	$1.5xf_{CK}$	*1.2*	*1.3*
Adder	Telescopic	50	$2.5xf_{CK}$	*1*	*1.4*

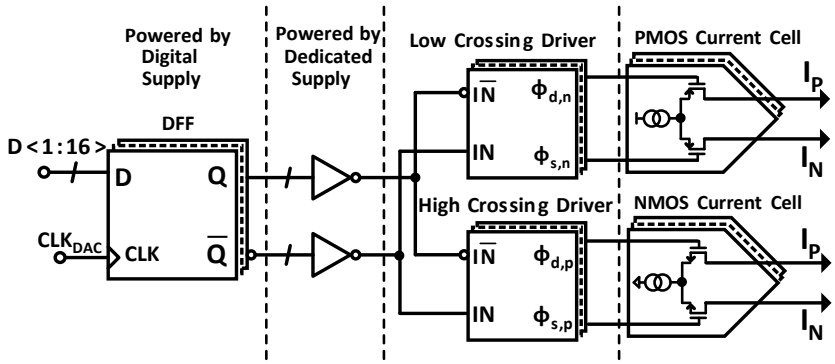


Fig. 2.14: Front-end feedback DAC block of the CT ΔΣ ADC.

2.4.2 Feedback DAC

The CT switched-current-source DAC outputs drive the virtual ground nodes of the CT integrators. Each DAC unit element comprises three separate circuits: a retiming DFF, low-swing high-crossing pMOS and low-swing low-crossing nMOS drivers, and n-type and p-type switched-current sources as shown in Fig. 2.14.

Fig. 2.15 depicts the circuit diagram of the current feedback *DAC* and its biasing circuit. Capacitors C_{bp} and C_{bn} are two off-chip capacitors which can filter out the noise generated by the voltage and current reference circuits and biasing circuit itself. There are 16 identical unit-cells for the I_{DAC}. In each unit cell, the cascode transistor is used to increase the output resistance of current mirror. The pMOS and nMOS current sources are controlled by the complementary switches to charge or discharge the SAB filter capacitors. The current source devices $M_{4,j}$ and $M_{4,k}$ are sized to achieve approximately 0.1% matching (10-bit accuracy) according to (2.8) where A_β and A_{VTH} are process dependent coefficients.

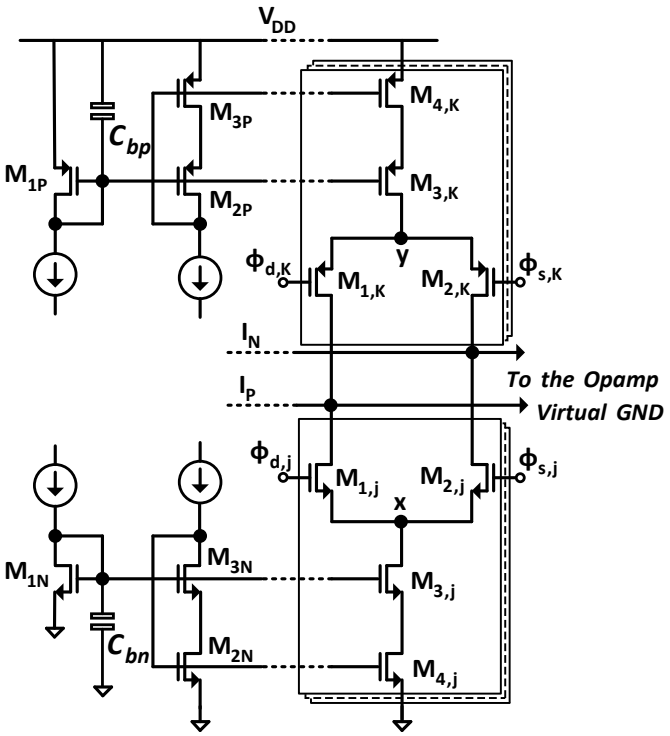
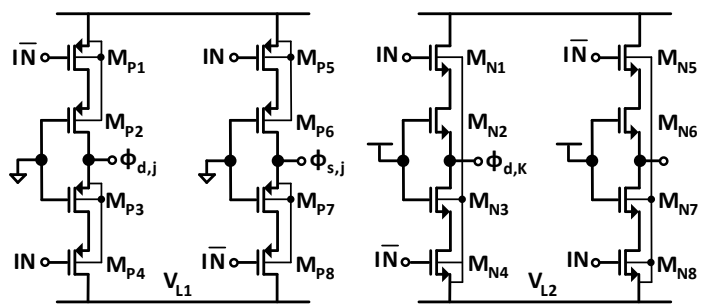


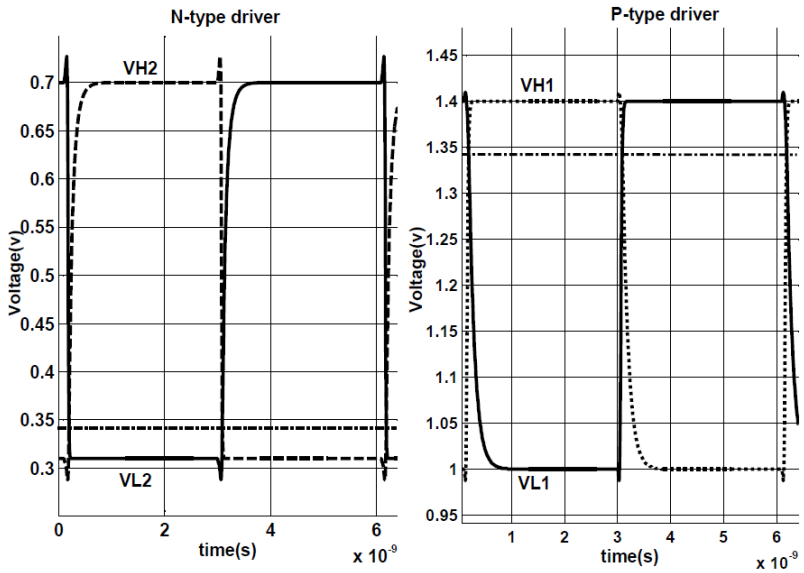
Fig. 2.15: P-type and n-type full-bridge current steering DAC.

$$W.L > \frac{A_{\beta}^{2} + \frac{4A_{VTH}^{2}}{(V_{GS} - V_{TH})^{2}}}{(\frac{\sigma_{I}}{I})^{2}} \tag{2.8}$$

However, a DEM block is used to improve the initial matching accuracy of the first DAC block from 10-bit to around 14-bit by averaging and first-order shaping the DAC unit mismatches. As one of the CT DAC design issues, the clock feedthrough is introduced while switching input data which can lead to voltage excursions at current switch $M_{1,2,j}$and $M_{1,2,k}$'s drain and source nodes. As a result, the output current needs more time to settle. This problem can be alleviated by using low-swing input data.



(a)



(b)

Fig. 2.16: (a) Circuit diagram and (b) timing diagram of the low-swing high-crossing p-type and low-swing low-crossing n-type voltage limiters.

As another design issue, for a period of time $M_{1,2,j}$ or $M_{1,2,k}$ are turned off, their source nodes x or y, in Fig. 2.15, will drop significantly and then rise back to their normal values when one of the switches is turned on. This glitch can cause a long settling time of the output current. The delay and the shape deviation from its ideal output current will change the transfer function of the DAC. As a consequence, the modulator performance may be degraded. Full pMOS low-swing, high-crossing and full nMOS low-swing, low-crossing generators are used in this modulator to convert full-swing and middle-crossing and to low-swing, high-crossing digital signals for the n-type switching current source, and low-swing, low-crossing digital signal for the p-type switching current source as shown in Fig. 2.16 [11], [19]. A low-swing digital input can reduce clock feedthrough and high-crossing and low-crossing can prevent the n-type current switches and two p-type current switches, respectively, from turning off simultaneously to minimize glitch energy. In the generator, the relative sizes of the transistors in the stacks determine the crossing point and rising and falling time of the outputs. The cascode transistors are added to reduce the coupling between the full swing input signals and the low swing output signals.

2.4.3 Modulator Front-End Device Noise Analysis

The device noise at the modulator front-end is not attenuated and thus it is a limiting factor in the total input referred noise of the modulator. There are three sources of noise at the front-end; 1) noise of the two input resistors, 2) noise of the telescopic opamp, and 3) noise of the current-steeringDAC_1. In this design, the total biasing current of the two-stage opamp is chosen as 4.5 mA to ensure low thermal noise. Large nMOS devices are used to lower the flicker noise and offset, and reduce the overdrive voltage of the input transistors, thus leading to wide output swing with high linearity. The nominal value of the two input resistors are chosen to be 680 Ω, generating thermal noise power 95.5 dB lower than the full-scale input signal considering the worse case 20% process variation for the resistor values. The signal-to-noise ratio (SNR) due to total in-band input-referred thermal noise from DAC_1 can be derived as

$$SNDR = \frac{I_{DAC} \cdot V_{OV}}{8KT\gamma\Delta_f} \tag{2.9}$$

where K represents the Boltzmann constant, T represents absolute temperature, V_{OV} is the over-drive voltage of $M_{4,j}$ and $M_{4,k}$ (they have nearly equal over-drive voltages in this design), I_{DAC} is the full scale output current of DAC_1 when the quantizer input is close to its highest reference voltage, γ is the MOS noise factor, and Δ_f is the signal bandwidth. In this design, $I_{DAC} = 1$ mA, $V_{OV} = 0.32$ V; substituting these quantities into (2.9), we obtain SNR 89.6 dB. Simulation in Spectre shows that the input referred in-band device noise due to SAB_1 (including its resistors and the opamp) and DAC_1 is $1.1\,\mathrm{nV}^2$.

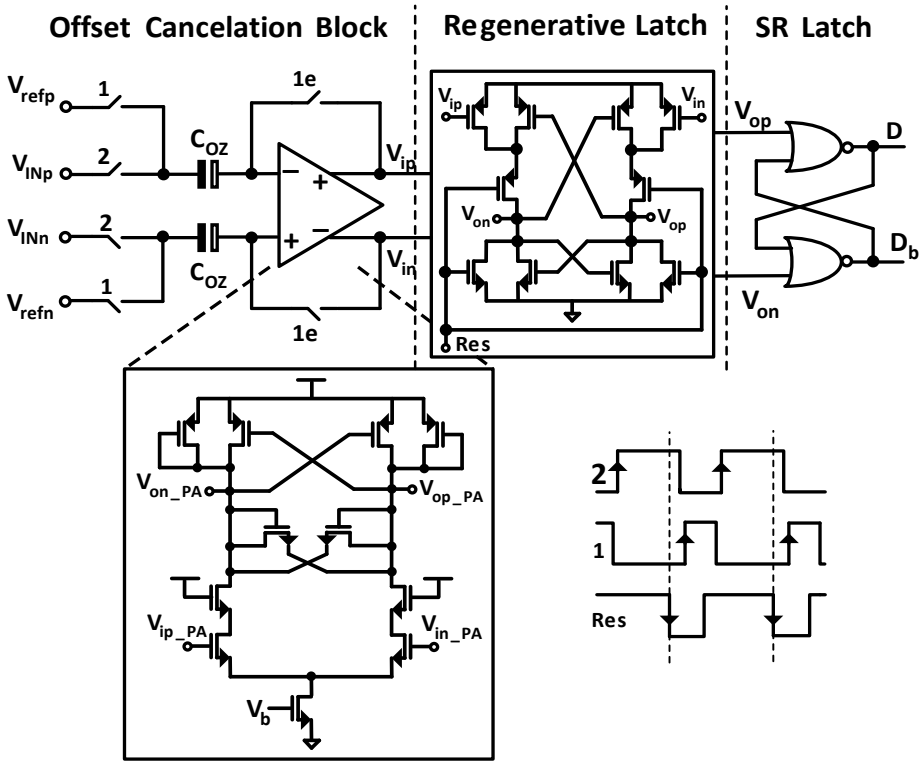


Fig. 2.17: Circuit diagram of the comparator including its timing diagram.

2.4.4 Quantizer

The quantizer in the prototype is a 4-bit flash ADC. It comprises 16 differential comparators, with the 16 reference voltages derived from a resistor ladder between the positive and negative reference voltages. The resistor values in the ladder were chosen small enough to ensure settling to within a few mV at the 250 MHz sampling rate. Because the output range of the adder circuit is only one third of the full-scale input range, the reference voltages to the quantizer only span $1/3$ of the input full-scale range, that is, $V_{REFP} = 940\text{mV}$ and $V_{REFN} = 460$ mV. Notice that the resolution of the quantizer is 5.5 bits relative to the modulator's full-scale input range. The comparator circuit used in the 4-bit quantizer, shown in Fig. 2.17, is based on a regenerative latch [20]. The comparator has a pre-amplifier stage to reduce kick-back noise. In addition, a switched capacitor input offset cancelation technique is adopted to suppress offset from both the pre-amplifier and latch stages. The pre-amplifier is a low gain single-stage amplifier with gain of 15. The two nMOS transistors acting as a limiter in the pre-amplifier can constrain the swing of the pre-amplifier for faster speed. The capacitance of C_{OZ} must be chosen carefully because this capacitor and its parasitics contribute to the load seen by the sampling and summing circuit. Also, the time constant of this capacitor with the resistive ladder resistance defines the settling time of the offset sampling cycle in the comparator. However, the capacitive divider formed by C_{OZ} and the parasitic capacitance of the latch input attenuates the input signal during the comparison cycle, and hence increases the input-referred offset of the latch. The regenerative latch outputs are pulled down to zero when the reset signal is high to eliminate the memory effect. When reset goes low, the regenerative latch amplifies the difference at its input to full scale. For a typical 0.13-µm CMOS technology and $C_{OZ} = 100\text{fF}$, simulations with the sampling circuit show that the overall input-referred offset of the comparator in the worst case is less than quarter an LSB.

2.5 MEASUREMENT RESULTS

The proposed CT ADC was fabricated in a 130 nm eight-metal (IBM_CMRF8SF) CMOS process. The die microphotograph of the chip is shown in Fig. 2.18. The ADC active area is 1 mm x 1.3 mm. Minimizing the coupling between digital and analog blocks and reducing offset and parasitic capacitors and resistors are the major considerations for the floorplan. Several commonly used layout techniques were employed, such as common-centroid layout for capacitors and resistors, inter-digitation for transistors, guard rings and shielding. A deep n-well was inserted in DAC_1 between the array of digital control logic and current cells to further reduce the noise coupling. Large decoupling capacitors have been used for supply lines and critical analog DC biasing lines. While all the non-idealities of DAC_1 such as unit cell mismatches will degrade the modulator performance, to decrease the gradient effect all the unit cells have been divided into two portions to be positioned in the common-centroid configuration. Therefore, x-axis and y-axis gradient effects will be eliminated. The basic idea of this technique is illustrated by Fig. 2.19. Two test boards were designed. One board houses the prototype chip, signal generation, and low jitter clock generation circuitry. On the other board are supply voltage generation circuitry, and DC biasing circuitry. The two boards communicate through board-to-board connectors.

Fig. 2.20 illustrates the measured spectrum of the output digital code. The input signal and the clock frequency are a 1MHz sine wave with -1.5 dBFS amplitude, and 185 MHz, respectively. The FFT size is 32k data points and the output data is a weighted Hanning window. The clock signal is provided by a pulse generator and its RMS jitter is less than 2.5 ps. The measured peak SNR, peak SNDR and peak spurious-free dynamic range (SFDR) were 78.2 dB, 76.9 dB and 83.1 dB in a 7.2 MHz bandwidth with DEM, respectively. As can be seen from the noise-shaping characteristics, the loop filter has 80 dB/dec. noise suppression. The third-order harmonic distortion (HDs) degrades SNDR, and the noise floor is determined by the thermal noise. Amplitude of the third-order harmonic is around -85.3 dB which does not change by sweeping the input signal frequency showing that it is coming from the ADC front-end since it does not get shaped. Post lay-out simulation proves that the source of the 3rd-order harmonic is the ADC front-

end and specifically it comes from the routing mismatch of the 16-DAC unit elements. The SNDR and SNR plots for varying input signal amplitudes is shown in Fig. 2.21 for 185 MHz sampling rate and input clock frequency of 1 MHz. The measurement results summarized in Table 2.4 demonstrate the effectiveness of this modulator.

TABLE 2.4: SUMMARY OF MEASUREMENT RESULTS

Sampling Frequency	*185 MHz*	*185 MHz*
Signal BW (MHz)	7.2	10
Fin (MHz)	1	1
SFDR (dB)	83.1	82.4
SNDR (dB)	76.8	71.9
SNR(dB)	78.2	73.4
FOM (pJ/conv)	0.16	0.21
Input Range (Diff)	2.8 Vp-p	2.8 Vp-p
Power (mW)	11.4(A),2.3(D)	11.4(A),2.3 (D)

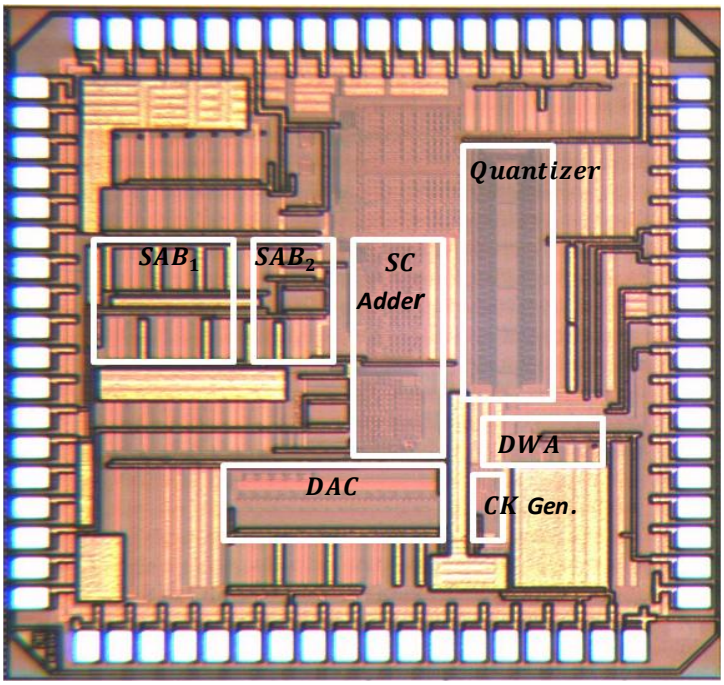


Fig. 2.18: Chip die microphotograph.

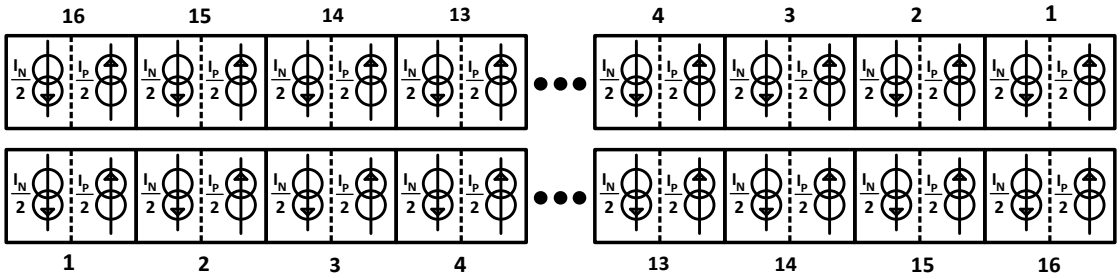


Fig. 2.19: Common centroid current steering DAC layout.

2.6 SUMMARY

A new power efficient, compact SAB based CT ΔΣ modulator was presented. The proposed modulator utilizes a new SAB network which reduces the power consumption and die area by reducing the number of active blocks.

Additionally, because the new technique also decreases the feed forward branches to the adder block in the modulator, a switch-capacitor (SC) adder replaces the CT adder and sample and hold blocks used in the conventional architecture. These two techniques make the design and implementation of the high-order continuous-time modulator easier. A 4th-order low pass CT ΔΣ modulator was designed and implemented in 130-nm IBM process to confirm the effectiveness of the proposed techniques. The modulator has achieved SNR, SNDR, and DR of 78.2 dB, 76.8 dB and 80 dB, respectively in a bandwidth of 7.2 MHz, and a FOM of 0.16 pJ/cov.

In Table 2.5, a comparison of this design to the recently published works [6]–[9] and [11]–[18] is shown. In this comparison, the FOM is defined as the following equation (2.10). This ADC is ranked as second position.

$$FOM = \frac{Power}{2.Bandwidth.2^{ENOB}} \tag{2.10}$$

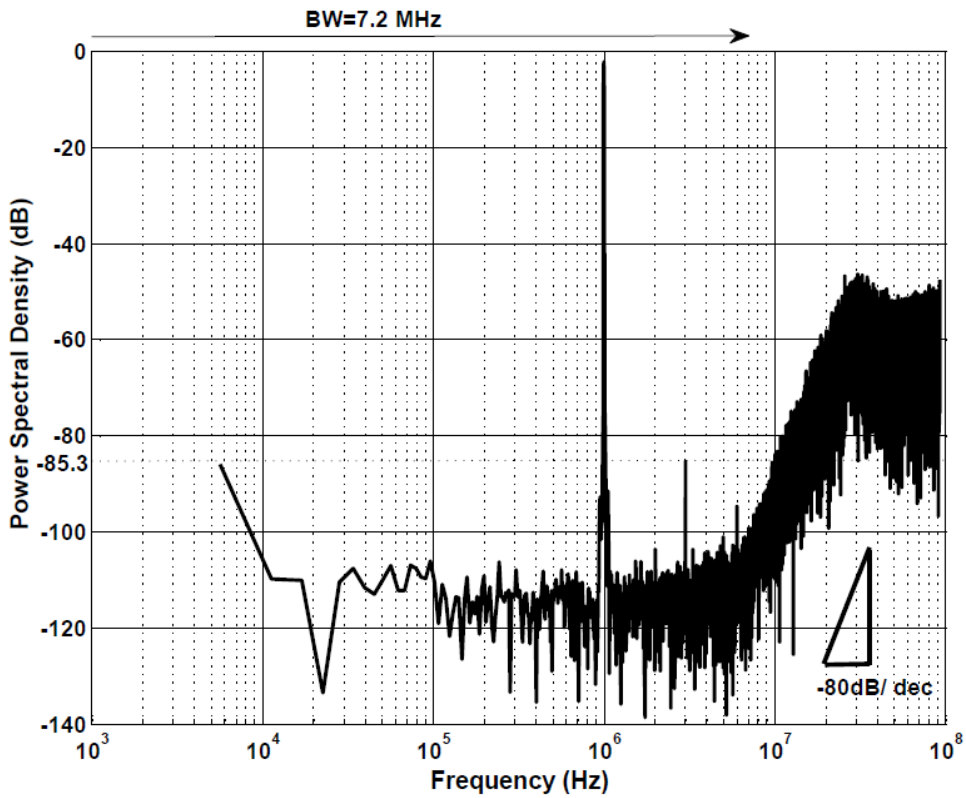


Fig. 2.20: Measured FFT spectrum.

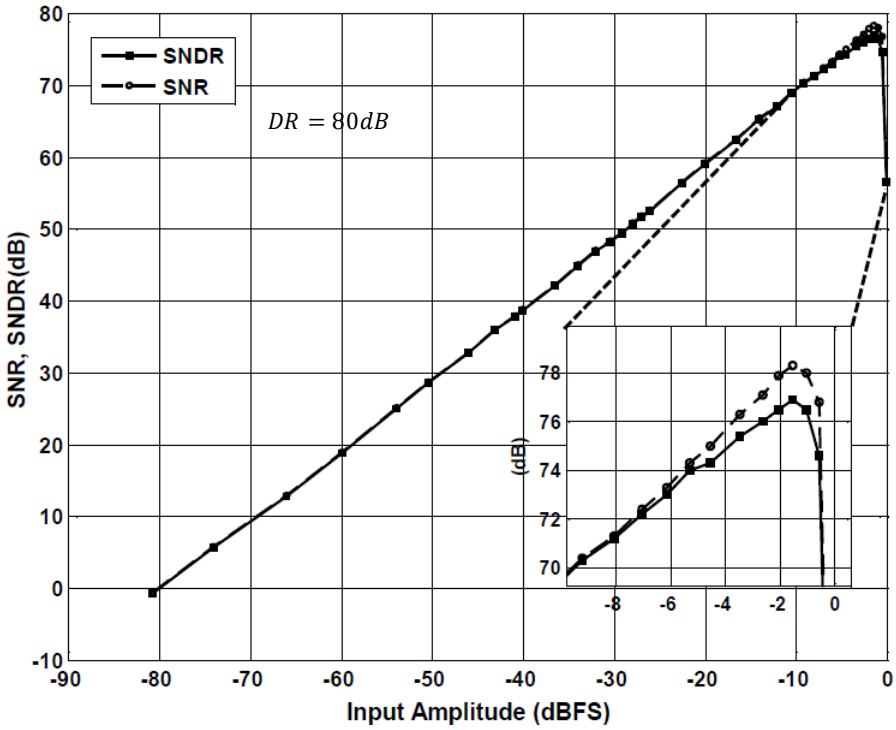


Fig. 2.21: Measured SNDR, SNR versus input amplitude.

TABLE 2.5: PERFORMANCE COMPARISON.

Reference	*Type*	*Process [µm]*	*FOM [pJ/conv.Step]*	*BW [MHz]*	*Power [mW]*	*SNDR [dB]*
[6] L. Breems	CT-DT	0.18	5.3	10	68	63
[7] R. Schoofs	CT	0.18	0.24	7.5	10	66
[8] A. Giandomenico	CT	0.13	2.3	15	70	61
[9] G. Mitteregger	CT	0.13	0.12	20	20	74
[11] S. Yan	CT	0.5	2.5	1.1	62	83
[12] T. Song	CT	0.25	0.57	2	2.7	63.4
[13] K. Matsukawa	CT	0.11	0.25	10	5.32	62.5
[15] S. D. Kulchycki	CT-DT	0.18	2.1	7.5	63.6	67
[16] Z. Li	CT	0.25	1.15	2.5	50	80.5
[17] P. Malla	DT	0.09	0.5	20	27.9	64
[18] V. Dhanasekaran	CT	0.065	0.32	20	10.5	60
This Work	CT	0.13	0.16	7.2	13.7	76.8

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CHAPTER 3. A 75-dB SNDR, 5-MHz BANDWIDTH STAGE-SHARED 2-2 MASH ΔΣ MODULATOR DISSIPATING 9-mW

Abstract

This chapter presents a new stage-sharing technique in a discrete-time (DT) 2-2 MASH delta-sigma (ΔΣ) ADC to reduce the modulator power consumption and chip die area. The proposed technique shares all active blocks of the modulator second stage with its first stage. The 2-2 MASH modulator utilizes second-order Chain of Integrators with Weighted Feed-forward Summation (CIFF) and Cascade of Integrators with Distributed Feedback Branches (CIFB) architectures for the first and second stages, respectively. Using the proposed technique, the second integrator and the adder op-amps of the modulator first stage are shared with the first and second integrator op-amps of the second stage. In addition to the stage-sharing scheme, other techniques are introduced to improve the modulator dynamic range (DR) and power dissipation. Measurement results show that the modulator designed in a 0.13 um CMOS technology achieves 75 dB SNDR over a 5 MHz signal bandwidth with a clock frequency of 130 MHz, while dissipating less than 9 mW analog power.

3.1 INTRODUCTION

Wireless communication systems typically require high-performance analog and RF circuit building blocks with low power operation so that battery life can be extended. A key building block in communication systems is the analog-to-digital converter. Oversampling ADCs use digital post processing making it possible to reconfigure the converter for various specifications. Oversampled delta-sigma ADCs also have the advantage of relaxed matching requirements on analog components, while still achieving medium to high resolution [1]. Furthermore, oversampling ADCs do not need steep roll-off anti-alias filtering typically required in Nyquist-rate ADCs. Conceptually, ΔΣ ADCs provide high resolution and linearity while using a low-resolution quantizer by taking

advantage of oversampling and noise shaping. Figure 3.1 shows the general block diagram of an *N-th* order single-loop CIFF delta-sigma modulator.

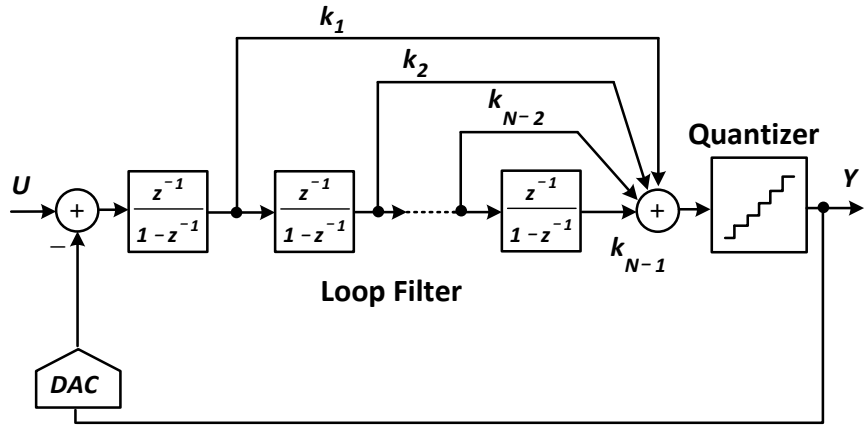


Fig. 3.1: Block diagram of a general Nth-Order CIFF ΔΣ ADC.

There are three essential parameters for design of a ΔΣ modulator: quantizer resolution, oversampling ratio (OSR), and loop filter order. Increasing any of these parameters improves the modulator SQNR [1, 2]; meanwhile, it creates trade-offs with several other design parameters such as power dissipation, area, and complexity. The impact of each of these key parameters on the other design parameters is briefly discussed next.

Utilizing a high resolution quantizer in the modulator increases the modulator power consumption. This is primarily due to the increased number of comparator units in the quantizer and also the increased complexity in the feedback DAC design. OSR is the second essential parameter in delta-sigma modulators. It is desirable to increase the OSR which necessitates higher clock frequencies for applications where higher signal bandwidth is required. Thus, the main limitations for boosting OSR by increasing the clock frequency for a given signal bandwidth is the specific technology chosen for the design and the amplifiers' power consumption requirements. The Double-Sampling (DS) approach introduced in [3, 4] is an alternative way to improve SQNR by increasing OSR without changing the modulator clock frequency. This approach reuses all the active block of the modulator during the two non-overlapping clock phases thus doubling the effective sampling rate. Finally, increasing the modulator order can enhance SQNR,

providing aggressive noise shaping. Nevertheless, this may reduce the modulator stability in a single loop configuration [5]. Boosting the modulator order also increases the power dissipation by adding more active blocks to the modulator. One option to increase the modulator overall order and still maintain stability is to use the Multistage-Noise-Shaping (MASH) delta-sigma modulator [5]. Figure 3.2 depicts the block diagram of a two-stage MASH modulator. As shown in Fig. 3.2, the quantization error, E_1, of the input stage is derived by subtracting the input to its internal quantizer from its output. It is then fed to the other ΔΣ loop forming the second stage

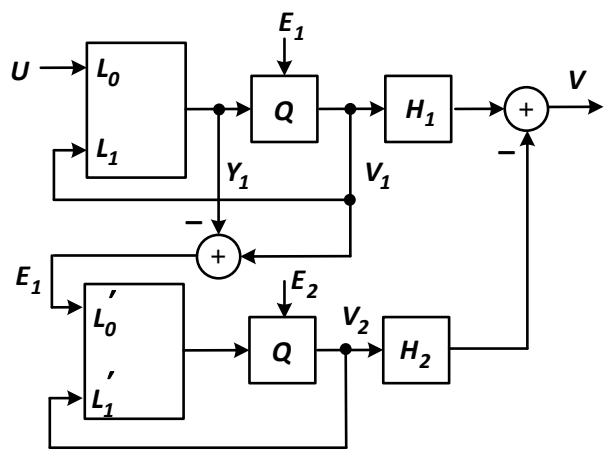


Fig. 3.2: Block diagram of a two-stage MASH ΔΣ ADC.

of the modulator. The overall output of the two-stage MASH modulator is given by:

$$V = H_1 . V_1 - H_2 . V_2$$

$$= STF_1 . STF_2 . U - NTF_1 . NTF_2 . E_2 \qquad (3.1)$$

$$Where\ H_1 = STF_2\ and\ H_2 = NTF_1$$

The MASH ΔΣ modulator achieves a higher overall order by cascading lower order stages and thus, benefiting from the stability of the lower order stages. Increasing the number of active blocks in the modulator trades off reduced power consumption for stability.

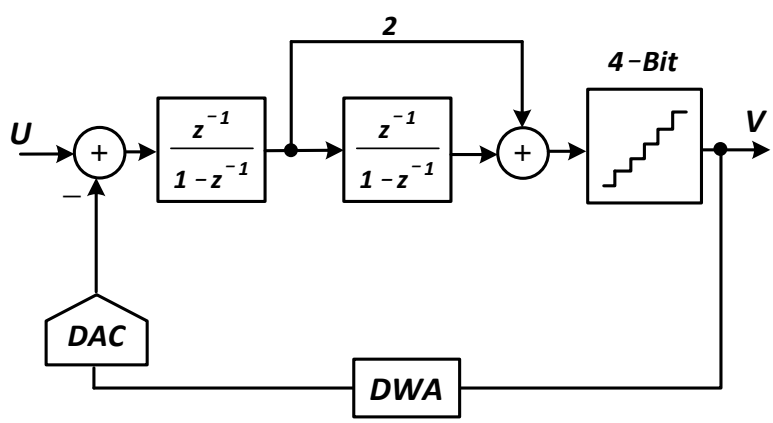
3.2 ARCHITECTURES OF THE PERFORMANCE IMPROVED DT ΔΣ MODULATORS

3.2.1 Existing Performance Improving Techniques

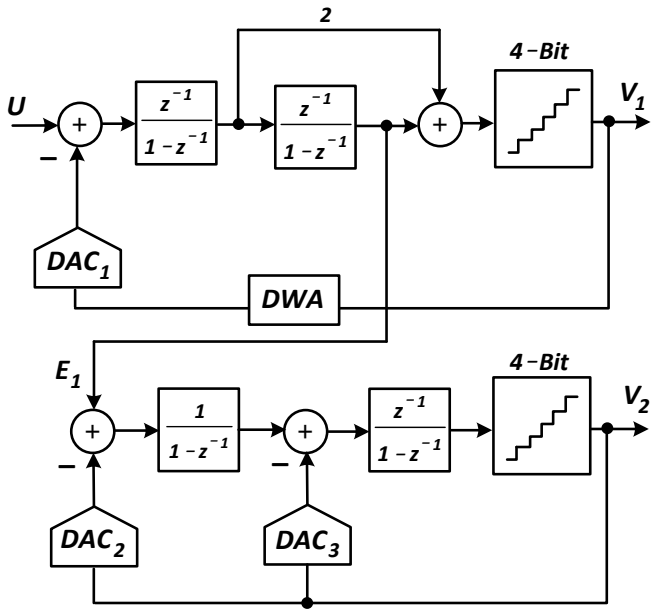
As mentioned before, two of the most effective techniques that can be used to improve the modulator SQNR in ΔΣ ADCs without significantly increasing the power consumption are the double sampling scheme and the cascaded modulator with a MASH architecture. To make an optimum choice between these two techniques, a detailed comparison is provided.

In the double-sampling technique, SQNR improvement is achieved by doubling the sampling rate for a fixed clock frequency. This technique does not increase the number of active blocks in the modulator, it simply reuses all active blocks in two different non-overlapping clock phases to double the oversampling ratio. A second-order double-sampled modulator is shown in Fig. 3.3 (a). In the system level diagram, it is the same as the 2nd-order modulator without double-sampling, but it has twice the effective oversampling ratio. The SQNR enhancement for an *N-th* order modulator is:

$$SQNR_{Improvement}(dB) = 10.(2N+1).Log_{10}(2) \tag{3.2}$$



(a)



(b)

Fig. 3.3: (a) Block diagram of a 2nd-order double-sampled (DS) modulator (b) Block diagram of a 2-2 MASH ΔΣ ADC.

Since the double-sampling approach reuses all the modulator active blocks, it does not increase the power dissipation of the loop filter. As a drawback of this technique, the quantizer and the dynamic element matching blocks, in this case data weighted averaging (DWA) blocks, have to operate during the non-overlapping time between two clock phases. This makes it difficult to meet the design requirements of those blocks and increases the power consumption.

Using the MASH technique shown in Fig. 3.3(b), the modulator performance increases proportionally to the order of the stages. Equation (3.3) presents the SQNR improvement over a conventional 2nd-order single loop modulator, while N_1 and N_2 are the order of the first and second stages of MASH modulator, respectively. Meanwhile, the modulator power consumption goes up depending on the order of the stages.

$$SQNR_{Improvement}(dB) = 20N_2.Log_{10}(OSR) - 10Log_{10}\left[\frac{\pi^{2N_2}(2N_1+1)}{2(N_1+N_2)+1}\right] \qquad (3.3)$$

TABLE 3.1: COMPARISON OF 2nd-ORDER DS AND 2-2 MASH ΔΣ MODULATORS.

Modulator	*Sampling Rate*	$SQNR_{IMpr.}$	*Quan. Res.*	*Num. of Active Blocks*
2nd-Order DS	260 MHz	15 dB	4-Bit	2
2-2 MASH	130 MHz	28 dB	4-Bit	4

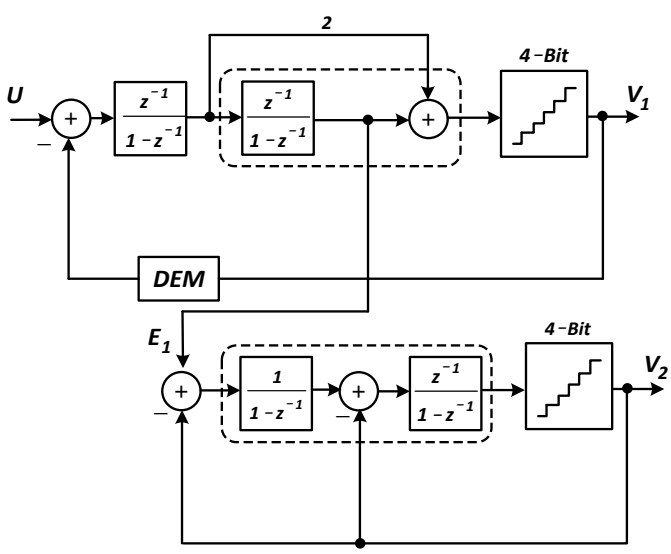
As an example, Table 3.1 summarizes the comparison between second-order single-loop double-sampled (DS) and 2-2 MASH ΔΣ modulators for a 5 MHz signal bandwidth (BW) and 130MHz clock frequency, shown in Fig. 3.3. The second-order DS modulator has lower power consumption due to the reduced number of active blocks; alternately, the 2-2 MASH modulator achieves greater SQNR improvement.

3.2.2 The Proposed Stage-Sharing Technique

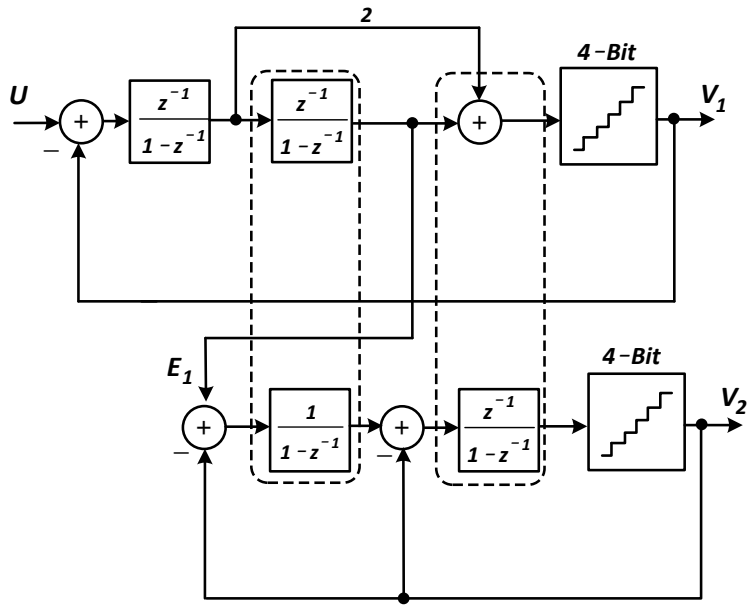
Since the SQNR improvement of the modulator using the cascading statges is 2-bit more than the DS scheme for a BW of 5 MHz in this case, utilizing a technique to reduce the power dissipation and chip area of the MASH topology makes it suitable for a low-power high-bandwidth application. To do so, the proposed stage-sharing technique is applied to the conventional 2-2 MASH modulator topology. This technique reduces the number of active blocks in the modulator architecture to save power and chip die area. Furthermore, it overcomes the power dissipation increase due to an increase in the MASH architecture order, by reusing all active blocks in the second stage with the first stage during the two different non-overlapping clock phases. This is done by sharing the operational amplifiers (opamps) of the second stage with the first stage. As a sequence, in a two-stage MASH structure, the second stage will boost the modulator overall order without adding any active blocks to the modulator.

There are different ways to implement the opamp sharing technique in the 2-2 MASH modulator, including horizontal-sharing, and vertical-sharing. Fig. 3.4 shows both the vertical and horizontal sharing schemes in a 2-2 MASH modulator. In the horizontal sharing, the 2nd integrator's amplifier is shared with the adder amplifier of the 1st stage and the 3rd integrator's opamp is shared with the 4th amplifier in the 2nd stage in two clock phases. The circuit level implementation of the horizental-sharing results is more complex because it only leaves the non-overlaping clock time for the first quantizer and DWA block to operate. This is also an issue for the DS technique in the circuit-level implementation which requires a fast quantizer block and a DWA with a low propagation delay. Consequently, the vertical-sharing scheme has been chosen to implement the opamp-sharing scheme that gives a half clock period for the first stage quantizer and DWA block to operate and also the same for the second stage quantizer. As described in the previous section, the second stage of the modulator is a 2nd-order CIFB architecture. There are generally two ways to implement a 2nd-order CIFB architechture. One uses delayed-integrators for both of the integrator stages and the other one has delayed and non-delayed integrators.

In the proposed 2-2 MASH stage-shared modulator, a second-order CIFB topology with delayed and non-delayed integrators is utilized. This topology gives more flexibility in opamp sharing by providing proper clock phases for the second stage switches as discussed further in the circuit implementation section.



(a)



(b)

Fig. 3.4: Block diagram of the 2-2 MASH with (a) Horizontal-sharing (b) Vertical-sharing.

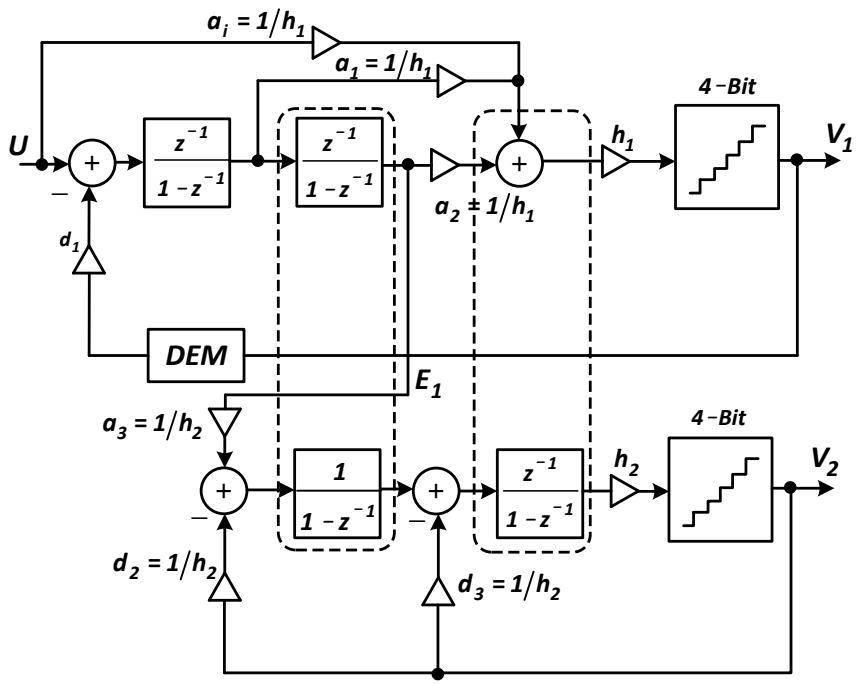


Fig. 3.5: Block diagram of the 2-2 stage-shared MASH after scaling.

3.3 SYNTHESIS OF THE PROPOSED DT STAGE-SHARED 2-2 MASH ΔΣ MODULATOR

3.3.1 Modulator Gain Coefficient Scaling Techniques

After selecting the proper sharing scheme for the modulator, i.e. vertical-sharing, gain scaling techniques are applied to the system-level diagram of the modulator to further reduce the power consumption and boost the dynamic range, as shown Fig. 3.5. The first gain scaling technique introduces a gain attenuation of $1/h_1$ ($h_1 > 1$) in the summing block. This gain attenuation has a few advantages such as relaxing the swing requirement of the adder amplifier as well as improving the adder's feedback factor (β_{add}) to save power. Since a low-distortion architecture is embedded in the first stage using the feedforward pass from the input to the adder block, input signal does not travel through the first and second integrators. Furthermore, the low-distortion architecture bypasses the input signal from the loop filter and directly applies it to the adder's input. In the conventional CIFF modulator architecture with a low-distortion topology, swing of the adder opamp defines the maximum allowable input signal amplitude to be applied to the modulator. Consequently, having a gain attenuation of ($1/h_1$) in the adder block using the first scaling technique allows the input signal amplitude to be increased by a factor of h_1 which boostes the modulator DR with the same rate. Since the modulator system level transfer-function (TF) needs to be the same after appling the gain attenuation, a gain of $h_1 > 1$ is introduced at the input of the quantizer to compensate the gain attenuation of $1/h_1$. Scaling down the quantizer reference voltages by a factor of h_1 is equivalent to amplifying the signal at the input of the quantifer by h_1. By using this implementation of the gain (h_1), the power is reduced. The quantizer input referred offset sets the lower limit on the scaling factor of the quantizer reference voltages. Furthermore, the quantizer initially has a 4-bit LSB which is reduced by h_1 after applying the gain amplification:

$$LSB_{new} = (V_{rpq} - V_{rnq})/(h_1.(2^4 - 1)) \tag{3.4}$$

To design a quantizer with a reduced LSB (because of shrinking the quantizer reference voltages by h_1) but still with a 4-bit resolution (with 16 comparator unit cells), it is necessary to increase the robustness of the quantizer comparators against the offset. In other words, the comparator total input-referred offset needs to be much smaller than the reduced LSB. Thus is accomplished by either dissipating more power or increasing the circuit complexity. Consequently, an optimum value of h_1 is considered for this design. To furthermore show the effectiveness of the scaling technique implemented in the summing block and the quantizer references, signals at the input of the modulator and at the output of the summing blocks are depicted in Fig. 3.6 without using a scaling technique ($h_1 = 1$) and with the gain scaling scheme ($h_1 = 2$). Maximum output voltage swing of the amplifier in the summing block is the main limiting factor for the modulator dynamic range since it is around $2xV_{dsat}$ below the single-ended full scale range ($V_{FS} = 1.4\ V$) from each side, using a single-sage opamp. Figures 3.6(a) and 3.6(b) show the modulator input signal with an amplitude of -7.4 dBFS and summing block output swing both around the common-mode voltage ($V_{cm} = 0.7\ V$) before applying the scaling approach. By applying a scaling factor of 2 (as an example), input signal range is doubled to have the same voltage swing at the output of the adder block as shown in Fig. 3.6(c) and 3.6(d). The scaling technique with an scaling factor of two boosts the modulator dynamic range by 6 dB.

A similar technique is utilized in the second stage by applying an attenuation factor of h_2 at the output of the fourth integrator and compensating it by scaling down the second quantizer reference voltages. Shifting the $1/h_2$ gain attenuation to the inputs of the 3rd and 4th integrators improves the feedback factors $\beta_{Int.3}$ and $\beta_{Int.4}$ and further reduces the power consumption. Table 3.2 summarizes all the gain coefficients of the proposed 2-2 MASH modulator after applying the scaling techniques.

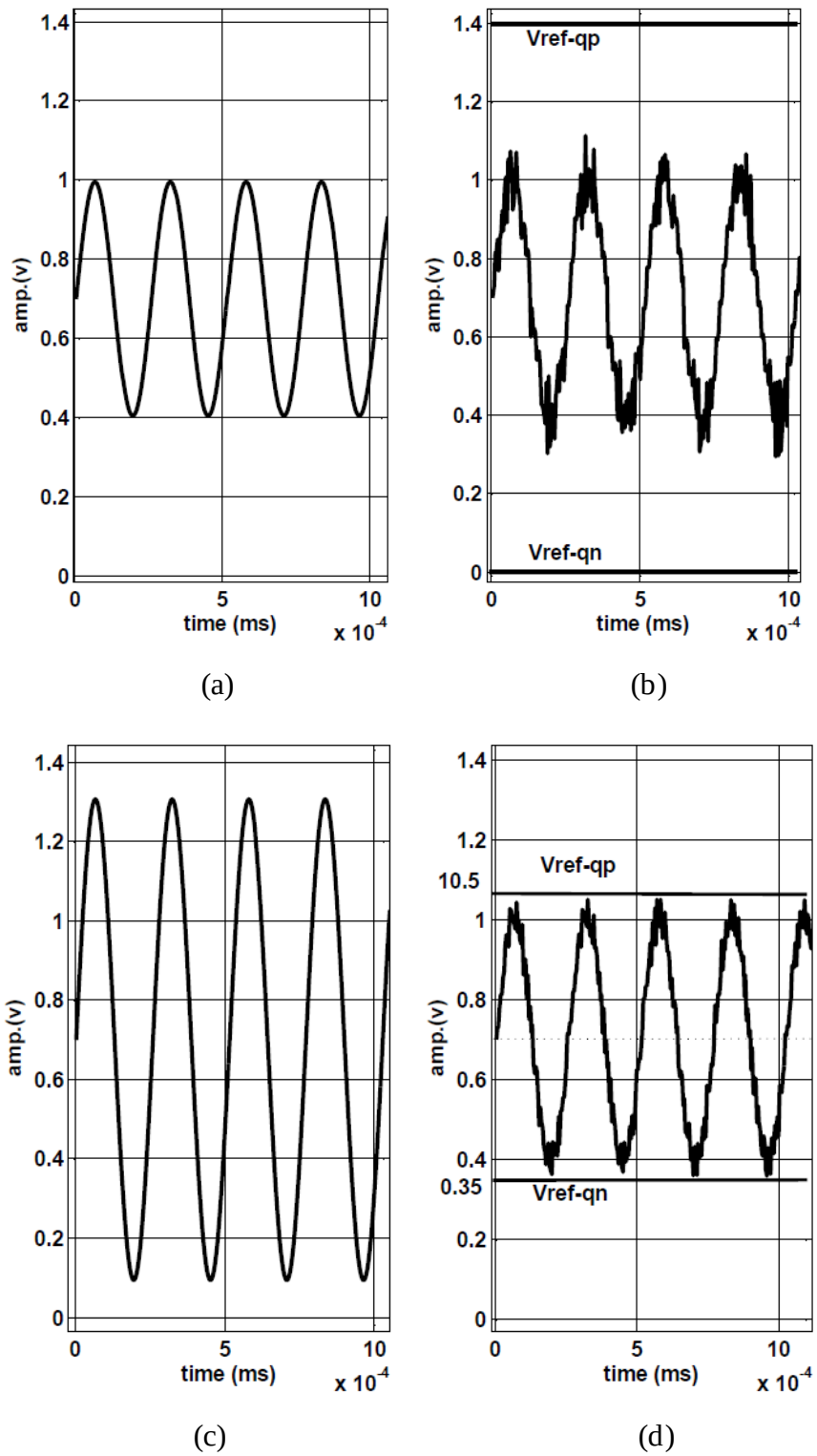


Fig. 3.6: Before scaling scheme (a) maximum applicable modulator input signal (b) maximum signal swing of the adder block, after scaling scheme (c) Maximum applicable modulator input signal (d) maximum signal swing of the adder block.

3.3.2 Detailed System Level Analysis of the Modulator

The target specification for the proposed DT stage-shared modulator is defined to be 13 bits with an input signal bandwidth of 5 MHz. The modulator maximum analog power dissipation is targeted for less than 9 mW. To initiate the design, all the noise sources of a DT modulator including quantization noise of the inner flash-ADC, thermal noise of the all circuit components, DAC unit mismatches, and the quantizer imperfections are analyzed for noise budgeting, Table 3.3. These are the main sources of the modulator non-idealities considering the practical design challenges and limitations including power dissipation and area. As shown, thermal noise is the dominant noise source in the DT modulator design.

In design of the oversampled ΔΣ, the first integrator is the most critical and power hungry block among all the analog blocks. Any imperfections in this block will not be noise shaped and directly appear at the modulator output. Therefore, an opamp with adequate finite gain and finite BW must be considered for the first integrator. Modulator SQNR performance versus the finite gain of the first integrator's amplifier is illustrated in Fig. 3.7. It is shown that the modulator can achieve the expected performance with a gain of at least 50.

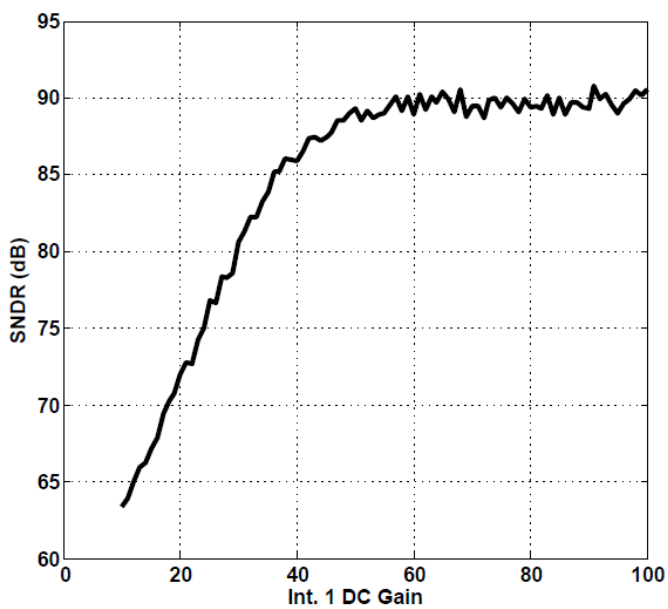


Fig. 3.7: Modulator SNDR versus the first integrator finite gain.

TABLE 3.2: MODULATOR GAIN COEFFICIENTS.

Gain	*Value*
a_1	0.66
a_2	0.33
a_3	0.5
a_i	0.33
h_1	3
h_2	2
d_1	1
d_2	0.5
d_3	0.5

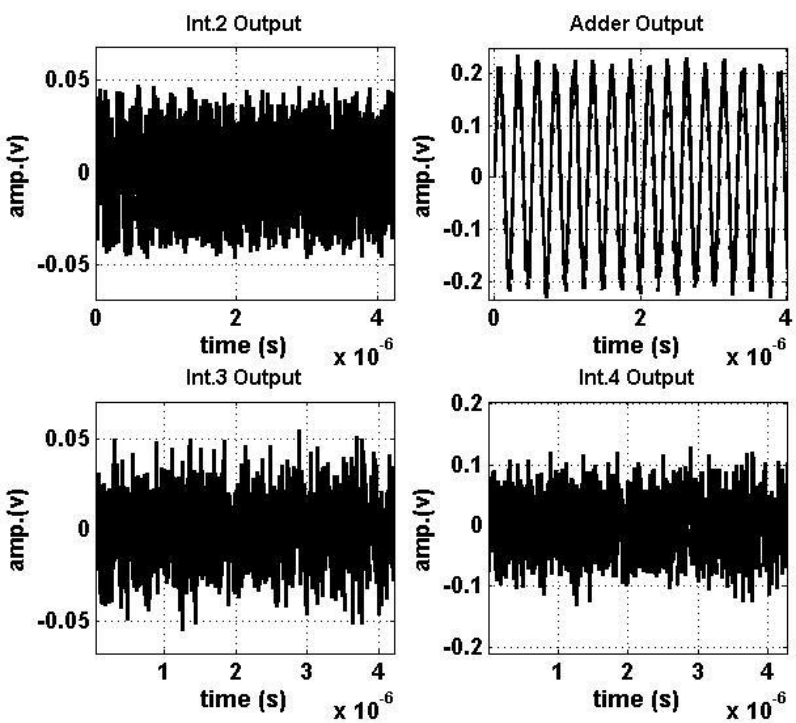


Fig. 3.8: Outputs of the 2nd, 3rd, and 4th integrators and also the adder block output after scaling.

To demonstrate the swing requirements of the modulator amplifiers, Fig. 3.8 depicts the outputs of the 2nd, 3rd, and 4th integrators, and also the adder block after scaling. As shown, all the integrator outputs include only the shaped quantization noise except the adder's output which also has the attenuated input signal term.

TABLE 3.3: MODULATOR NOISE BUDGETING

Noise Source	*Noise Budget (%)*	*SNR (dB)*
Quantization Noise	20	87
Thermal Noise	45	83.5
Quantizer Error	10	90
DAC Mismatch	15	88.2
Other Noise Sources	10	90

3.4 DESIGN OF THE 2-2 STAGE-SHARED MASH

3.4.1 Circuit Level Diagram of the Modulator

The single-ended circuit level diagram of the 2-2 MASH modulator of Fig. 3.5 before applying the sharing scheme is shown in Fig. 3.9. To apply the vertical-sharing scheme to the modulator circuit diagram, appropriate integrator architectures and clock timing are considered. The modulator utilizes two delayed integrators for the first stage and a non-delayed integrator along with a delayed integrator for the second stage.

In the circuit diagram, the first integrator samples the input signal at φ_1 and integrates it during φ_2. The second integrator and the adder block both are in the operating mode during φ_2 while the third and fourth integrators are in their active modes during φ_1. Furthermore, the amplifiers of the second integrator and the summing block are in use only during φ_2. During φ_1 the adder block is in the reset mode, so its amplifier is idle, but it is still dissipating power. During φ_1, the second integrator's amplifier is dissipating power to hold the previous charge on C_{i2}. In the second stage, both the third and last integrators are in the integrating mode at φ_1. At φ_2, their amplifiers are holding the previous charges on their integrating capacitors, C_{i3} and C_{i4}. Analyzing the operation of the modulator stages for two non-overlaping clock phases shows that the amplifiers of the 2nd integrator and the adder block in the first stage can be shared with the amplifiers of the 3rd and 4th integrators of the second stage implementing the vertical-sharing to save power and area.

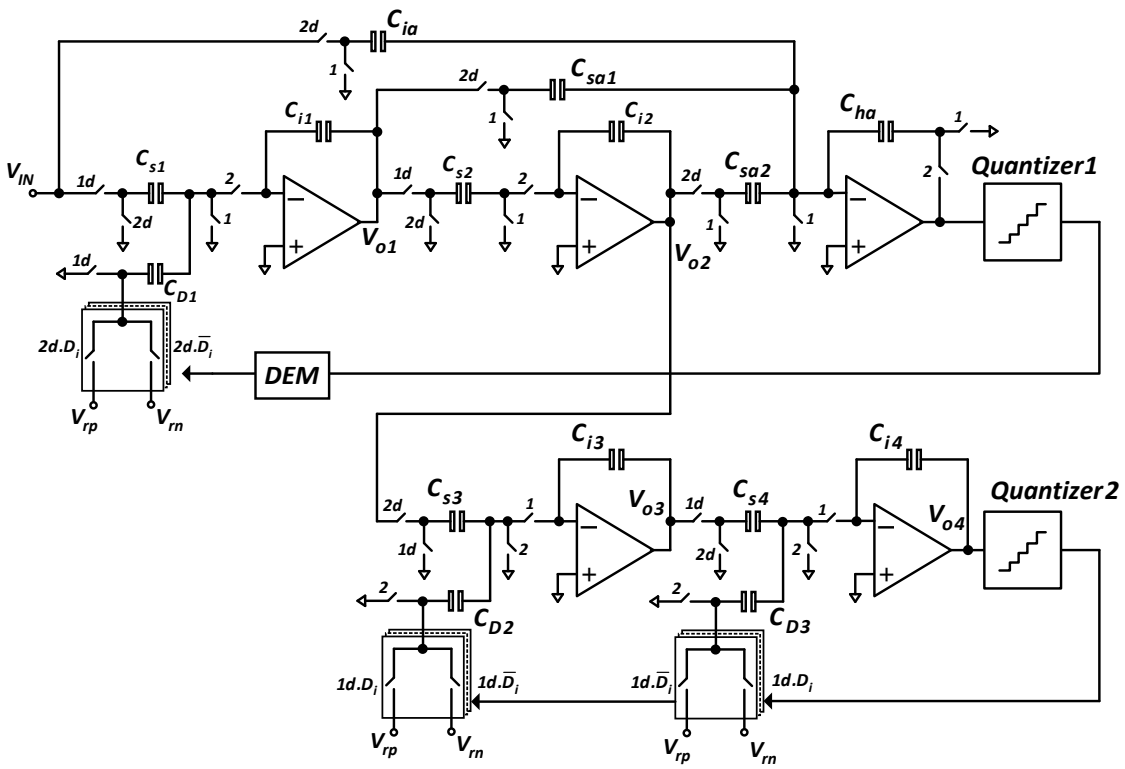
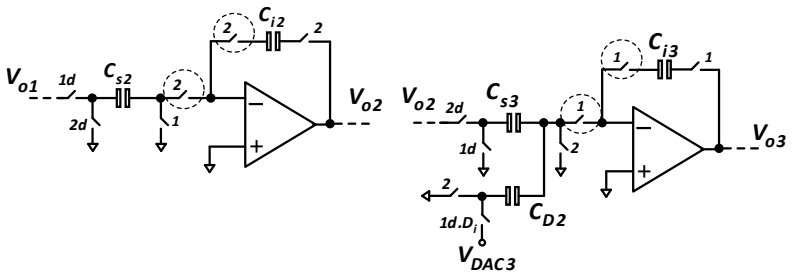


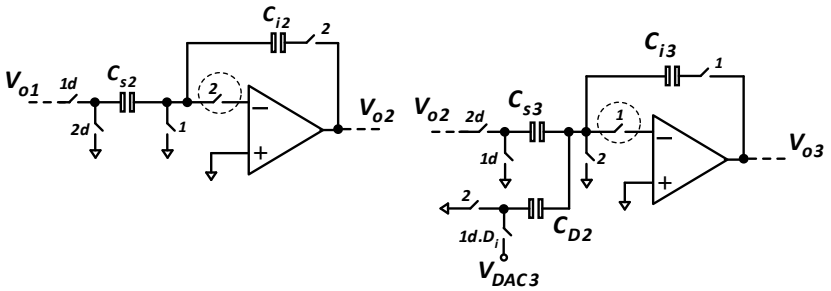
Fig. 3.9: Circuit-level block diagram of the 2-2 MASH without the opamp sharing technique.

Sharing the amplifiers of the first stage with the second stage requires the isolation of the integrating capacitors except C_{i1} from their amplifiers during the opamp sharing phase. This is done by adding two switches around the integrating capacitors as depicted in Fig. 3.10(a) [6]. This figure shows the isolation of C_{i2} and C_{i3} capacitors from the amplifier while this amplifier will be shared between these two integrators. For the summing block, isolation of the adding capacitor is not required since it is discharged during the sharing phase. The second integrator and the summing block are both operating during φ_2 resulting in a long signal path for the signal to go through. There is also a long signal path through the second stage during φ_1 while the third and fourth integrators are integrating at the same time. To have enough settling accuracy within the clock time, all the switches need to have proper sizing to reduce the "on" resistance. Adding two extra switches for each integrating capacitor adds more resistance to the long paths thus slowing down the settling time of the blocks. Figure 3.10(b) shows the switch merging technique used to reduce the number of switches through the long paths. Since

during the isolation phase of the integrating capacitor, the sampling capacitor must be separated from the amplifier's virtual ground, these two switches which have the same clock phases can be merged and shifted to the virtual ground of the amplifier. In this way, the shifted switch will not add extra resistance to the long path while it is out of the long path. Meanwhile, the integrating capacitor's second isolation switch which disconnects it from the amplifier output still is required.



(a)



(b)

Fig. 3.10: Integrators with the integrating capacitor isolation switches (a) before and (b) after the switch merging technique.

The circuit level diagram of the proposed modulator after applying the sharing scheme is depicted in Fig. 3.11. This circuit diagram also shows the switch matching technique utilized in the integrator blocks except the first integrator. The vertical-sharing scheme is between the second and third integrators. Also, the adder block and the fourth integrator share their amplifiers during two non-overlaping clock phases.

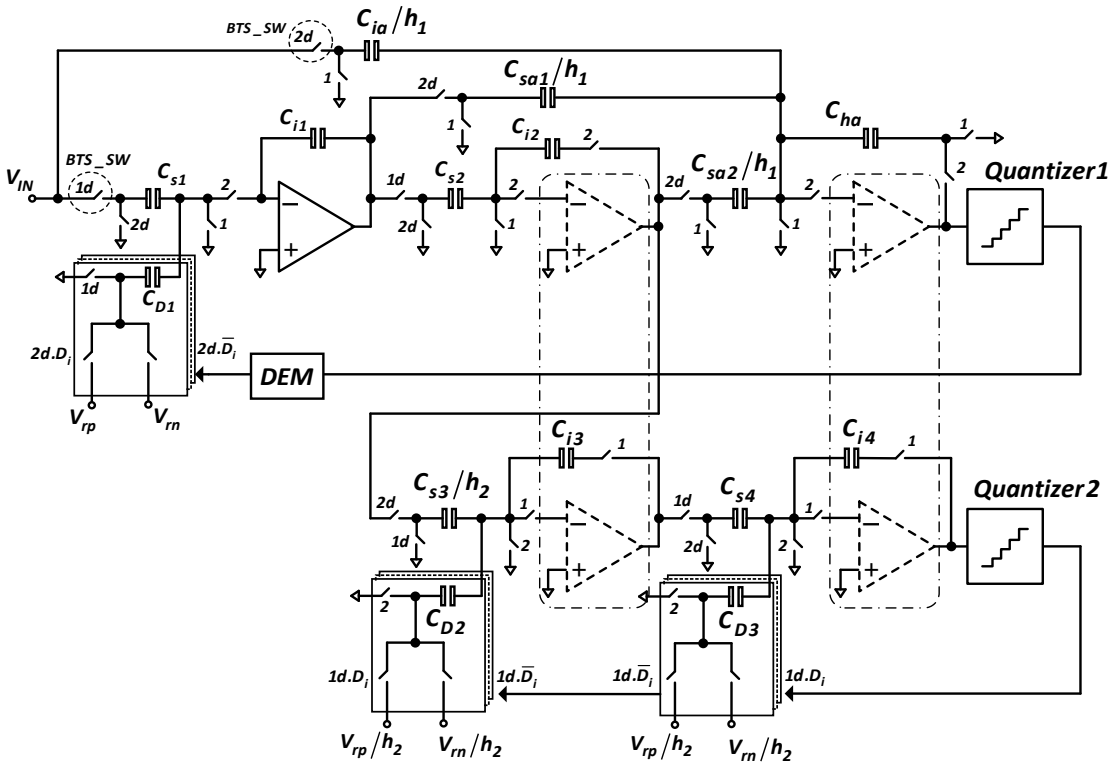


Fig. 3.11: Circuit level block diagram of the 2-2 MASH with the opamp sharing technique.

Two coefficient scaling techniques are also applied to the modulator. As illustrated in the circuit diagram, all the capacitors going to the summing block are scaled by a factor of h_1. According to (3.5), the gain attenuation of $1/h_1$ improves the adder block's feedback factor (β_{add}) which consequently decreases the unity-gain-bandwidth (UGB) requirement of the block to save power:

$$\beta_{add} = \frac{C_{ha}}{\left(\frac{C_{ia} + C_{sa1} + C_{sa2}}{h_1} + C_{ha}\right)} \tag{3.5}$$

$$UGB_{add} > \frac{(N+1).Ln(2)}{\pi.\beta_{add}}.f_{ck} \tag{3.6}$$

Where N is the settling accuracy, and f_{ck} is the modulator sampling frequency.

3.4.2 Thermal Noise Analysis and Capacitor Sizing

Finding the value of the capacitors in the modulator starts from the first integrator's sampling capacitor. Since all the non-idealities from the following integrator blocks are shaped depending on the position of the integrator, the value of the other capacitors are calculated by scaling down the capacitor value of the first integrator. Thermal noise is an essential factor defining the sampling capacitor value of the first integrator. The main sources of thermal noise in the switch-capacitor (SC) integrators are the "on" resistances of the switches and the thermal noise of the opamp. The total input referred thermal noise of the first integrator is [5]:

$$V_{Int1,ntotal}^2 = \frac{4KT}{C_{s1}} \cdot \frac{(2.x + \frac{7}{3})}{(1+x).OSR} \tag{3.7}$$

$$x = 2.R_{on,i}.g_m$$

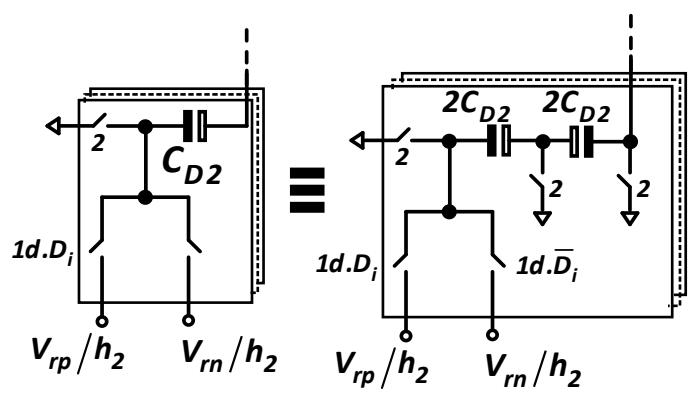


Fig. 3.12: Technique to decrease the effective capacitance value of the DAC unit cells.

Where $R_{on,i}$ is the "on" resistance of the integration switches and g_m is the transconductance of the single-stage opamp. Since the final implementation of the modulator is a differentional topology, the total input-referred thermal noise is multiplied by a factor of 2. There is another factor of 2 in the total input-referred noise of the first integrator while the modulator front-end is not sharing the sampling capacitor C_{s1} and the

DAC_1 capacitor, C_{D1} as depicted in Fig. 3.11. By selecting the signal-to-thermal-noise-ratio (STNR) value from the modulator noise budgeting table and considering that 85% of the total modulator input-referred thermal noise is coming from the modulator front-end, the first integrator capacitor value is estimated to be 1.3 pF.

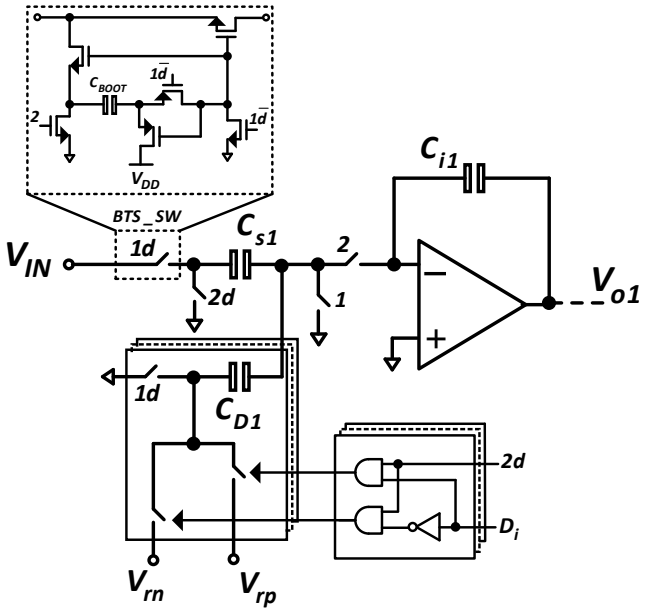


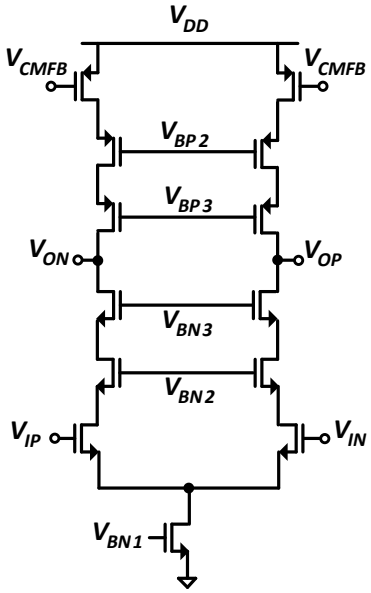
Fig. 3.13: Modulator front-end.

The sampling capacitor considered for this design is 1.5 pF taking into account the 15% process variations for the capacitors. Since the thermal noise contribution of the second stage integrators is a small portion of the total thermal noise budget, the second stage sampling capacitors are scaled down. The limiting factor in selecting the smallest capacitor value for the second stage DAC unit capacitors is the minimum available metal-isolator-metal (MIM) capacitor in the process ($C_{MIM\_Min} = 60$ fF). Two techniques are utilized to reduce the effective capacitance value of the second stage DAC unit capacitors since they define the values of the C_{i3} and C_{i4} capacitors. As illustrated in Fig. 3.12, by putting two minimum MIM capacitors in series, the effective equivalent capacitance will be half of the original value. To eliminate the charge trapping problem at the top-plate connection of the two series capacitors, a switch connected to ground is utilized to discharge this node during the reset phase. The other technique is shrinking the DAC

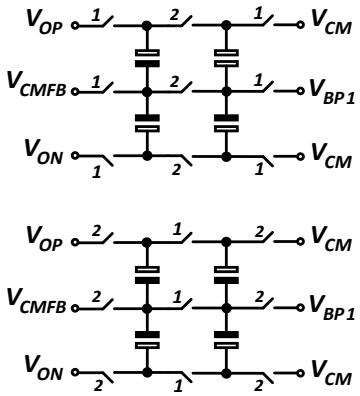
reference voltages to implement the gain reduction instead of decreasing the DAC unit capacitance values where

$$q = \left(\frac{C_{D2}}{h_2}\right).\ V_{ref} = C_{D2}.\left(\frac{V_{ref}}{h_2}\right) \tag{3.8}$$

The final capacitance values of C_{s3} and $C_{s4}$are 0.24 pF and 0.48 pF, respectively.



(a)



(b)

Fig. 3.14: (a) First integrator's amplifier (b) SC common-mode feedback of the first integrator.

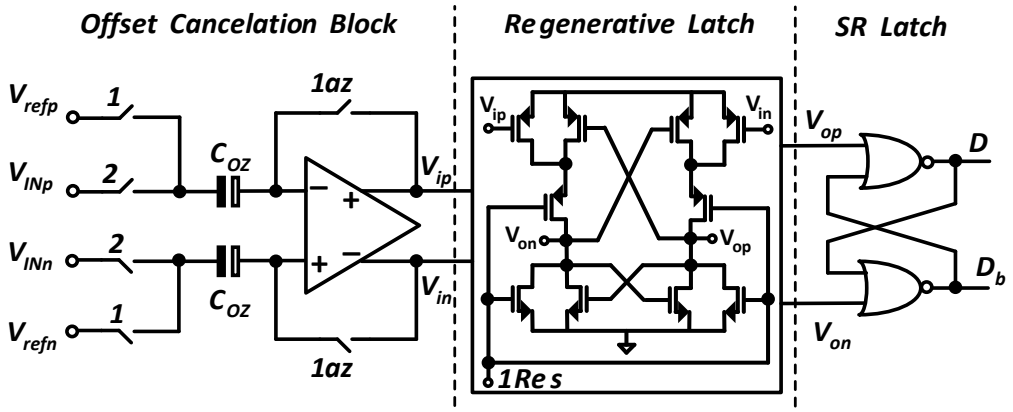


Fig. 3.15: Circuit diagram of the comparator used in the 4-bit Flash ADC.

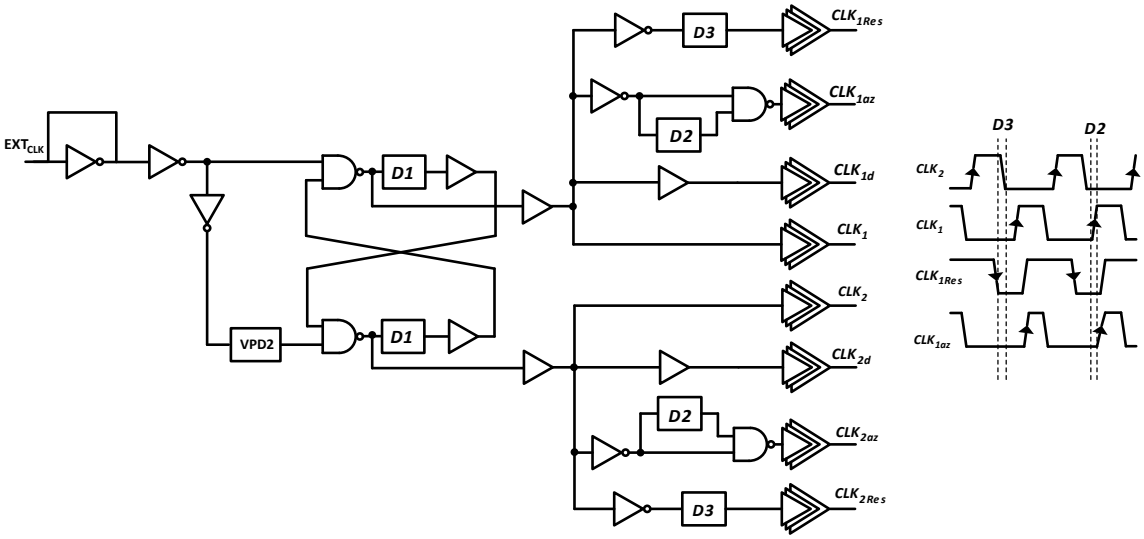


Fig. 3.16: Modulator non-overlapping clock generator.

3.4.3 Modulator Front-End Cirrcuit Implementation

Figure 3.13 shows the modulator front-end. Bootstrapped clock signals are applied to ensure linear sampling at the critical input switches [7]. As mentioned in the thermal noise analysis section, two separate capacitors C_{s1} and C_{D1} are utilized in the first integrator. Though this increases the input-referred thermal noise of the modulator, it

avoids detrimental reference errors caused by signal-dependent loading of the reference driver [8]. The signal swing of the loop filter of the low-distortion multibit modulator is greatly reduced. This allows the use of the power-efficient and low-noise telescopic double-cascode opamp with a 1.2 V supply (Fig. 3.14). To minimize the noise contribution from two top pMOS transistors controlled by the common-mode feedback voltage, the transconductances of these devices were made much smaller than those of the input differential pair, by assigning a bigger overdrive voltage for the given output swing requirement. The peak-to-peak differential output signal swing of the opamp is 0.38 V. A power-efficient SC common-mode feedback with dual branches is used in the first integrator as well as the other active block since all the amplifiers are in the operating mode during both non-overlapping clock phases. Fig. 3.14 shows the opamp structure, along with the SC common-mode feedback. It achieves a GBW of 1.25 GHz and a dc gain of 50 dB, while drawing 2.8 mA bias current. For the second and third amplifiers used in the sharing scheme, simple telescopic cascode opamps similar to the first stage opamp with scaled sizings are utilized.

3.4.4 Quantizer and Clock Generator Circuit Implementations

Both stages of the modulator utilize a 4-bit flash-ADC. As depicted in Fig. 3.15, each comparator contains a gain boosted preamplifier stage with a cross-coupled active load, to prevent kick-back noise and to speed up signal amplification, followed by a track-and-latch and a set-and-reset (SR) latch [9, 10]. An input offset sampling scheme is employed in the preamplifier stage to minimize the effects of offset errors. The threshold voltages of the quantizer are generated by a resistor string. The value of the auto-zeroing capacitor, C_{az}, is defined considering the time constant of the preamplifier stage during the offset sampling phase (introduced by the resistive string and C_{az}) and the input parasitic capacitance of the preamplifier. Data-weighted averaging (DWA) was applied to shape the mismatch errors of the 16-level DAC [11].

The non-overlapping clock generator used in this design is shown in Fig. 3.16. The delay cell D_1 defines the pulse width of both non-overlapping clock phases. D_2

determines the rising edge and the pulse width of the auto-zeroing clock while D_3 defines the falling edge of the reset pulse.

3.5 MEASUREMENT RESULTS

The proposed architecture was designed and fabricated in an eight-metal (IBM_CMRF8SF) 130-nm CMOS process. The die photograph is shown in Fig. 3.17. The total ADC active area is $1.6\,\mathrm{mm}^2$. The 2-2 stage-shared MASH modulator contains three main blocks (the loop filter shared between the first stage and second stage, the quantizer blocks, and the DAC blocks). Minimizing the coupling from the digital to the analog blocks and reducing offset and parasitic capacitors and resistors are the major considerations for the floor plan. Several commonly used layout techniques were employed, such as common-centroid layout for capacitors, inter-digitation for transistors, guard rings and shielding. A deep n-well was inserted in DAC_1 between the array of digital control logic and the DAC unit cells to further reduce the noise coupling. Large decoupling capacitors have been used for supply lines and critical analog DC biasing lines. Two test boards were designed. One board houses the prototype chip, signal generation, and clock generation circuitry. The other board contains supply voltage generation circuitry and DC biasing circuitry. The two boards communicate through board-to-board connectors. The measured output spectrum is shown in Fig. 3.18 for 130 MHz sampling rate and 0.5 MHz input signal. The peak SNDR and SNR are 74.9 dB and 76.4 dB, respectively at a signal bandwidth of 5 MHz. The 80 dB/dec slope of the quantization noise demonstrates that fourth-order noise shaping is achieved. As depited in the figure, there are 2nd-order and 3rd-order harmonics in the modulator power-spectral-density with amplitudes around -90 dB and -83.7 dB. Sweeping the input signal frequency shows a 2nd-order shaping on the amplitude of the harmonics which proves that the hormanics are coming from either the adder block or the quantizer block of the first stage. The SNDR and SNR plots for varying input signal amplitudes are shown in Fig. 3.19 for a 130 MHz sampling rate (OSR of 13) and an input clock frequency of 500 KHz. At 130 MHz, lower supply voltages (1.2 V Analog, 1.1 V Digital) are used to decrease

the power consumption. The measurement results summarized in Table 3.4 demonstrate the effectiveness of this modulator.

Figure 3.20 illustrates a comparison of this design to the recently published state-of-the-art DT ΔΣ modulators [2] and [12]–[21]. In this comparison, the FOM is defined as:

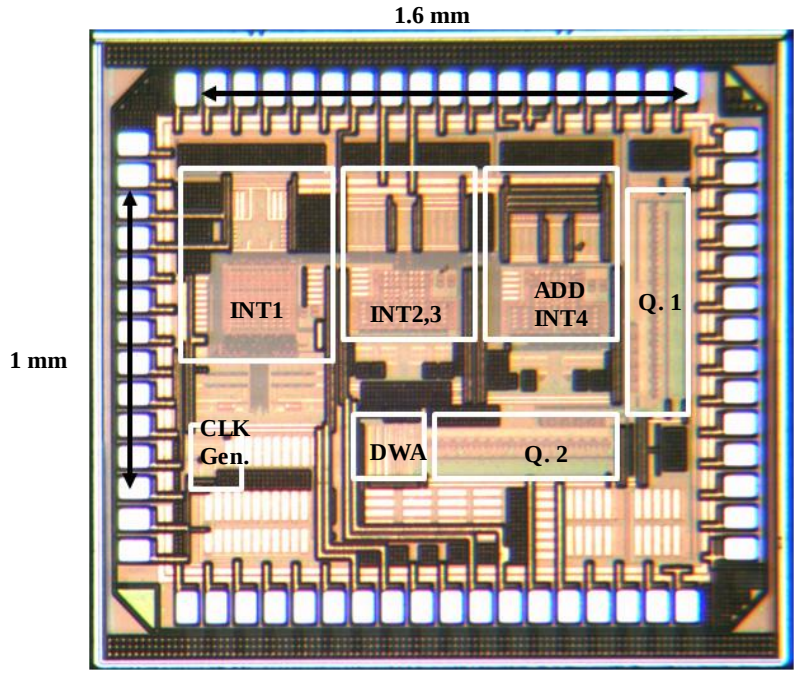


Fig. 3.17: Chip die micrograph.

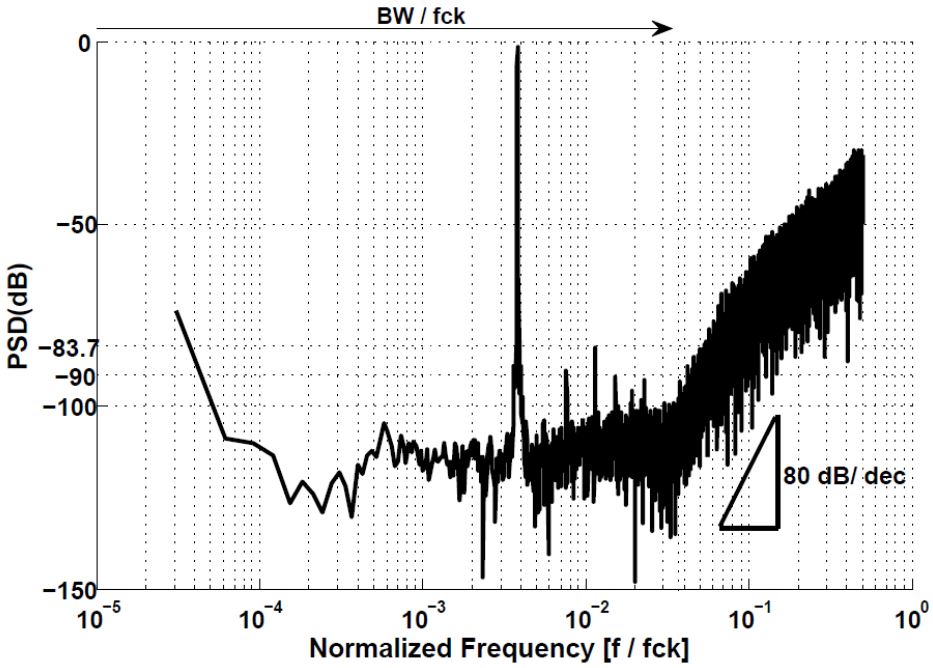


Fig. 3.18: Measured FFT spectrum (32K points FFT).

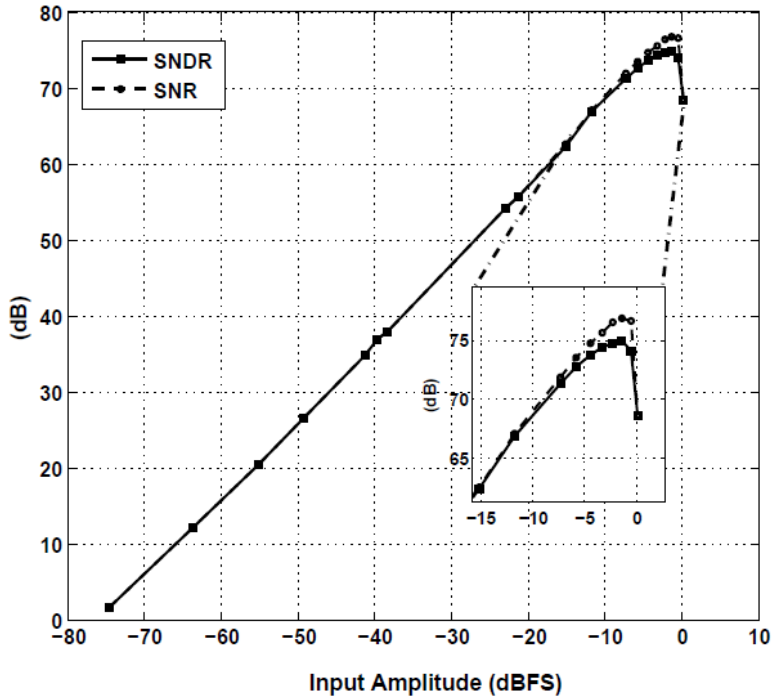


Fig. 3.19: Measured SNDR, SNR versus input amplitude.

$$FOM = \frac{Power}{2.BW.2^{(\frac{SNDR-1.76}{6.02})}} \tag{3.9}$$

As shown in Fig. 3.20, [15], [19] and [20] are the closest designes in term of FOM to this ADC design. The main distinguishing factor of this design is the maximum input range of the modulator since it utilizes the proposed scaling technique. Maximum input range of this design is 2.4 Vpp (peak-to-peak) differential which is higher than the other designs, making it easier to transfer the design to an advanced process with lower supply voltage.

3.6 SUMMARY

A new stage-sharing technique was presented for a low-power wide-bandwidth DT MASH ΔΣ ADC. This technique eliminates active elements from the second stage of the MASH modulator to save power and chip die area. Furthermore, the proposed technique shares the op-amps of the modulator first stage with its second stage amplifiers during

two different non-overlapping clock phases. The coefficent scaling techniques also were applied to the proposed modulator to boost the DR and reduce the power dissipation. The required system and circuit details were described. A 2-2 stage-shared MASH delta-sigma modulator was designed and tested to verify the effectiveness of the stage-sharing technique. The modulator has achieved SNR, SNDR, and DR of 75.7 dB, 75.8 dB and 78 dB, respectively in a bandwidth of 5 MHz, and a FOM of 0.32 pJ/cov.

TABLE 3.4: SUMMARY OF MEASUREMENT RESULTS.

Sampling Frequency	**130MHz**	**130MHz**
Signal BW (MHz)	**5**	**5**
Fin (KHz)	**75**	**500**
SFDR (dB)	**97**	**82.4**
SNDR (dB)	**75.7**	**74.9**
SNR(dB)	**75.8**	**76.4**
FOM (pJ/conv)	**0.32**	**0.35**
Input Range (Diff)	**2.8 Vp-p**	**2.8 Vp-p**
Power (mW)	**8.9(A),7.1(D)**	**8.9(A),7.1(D)**

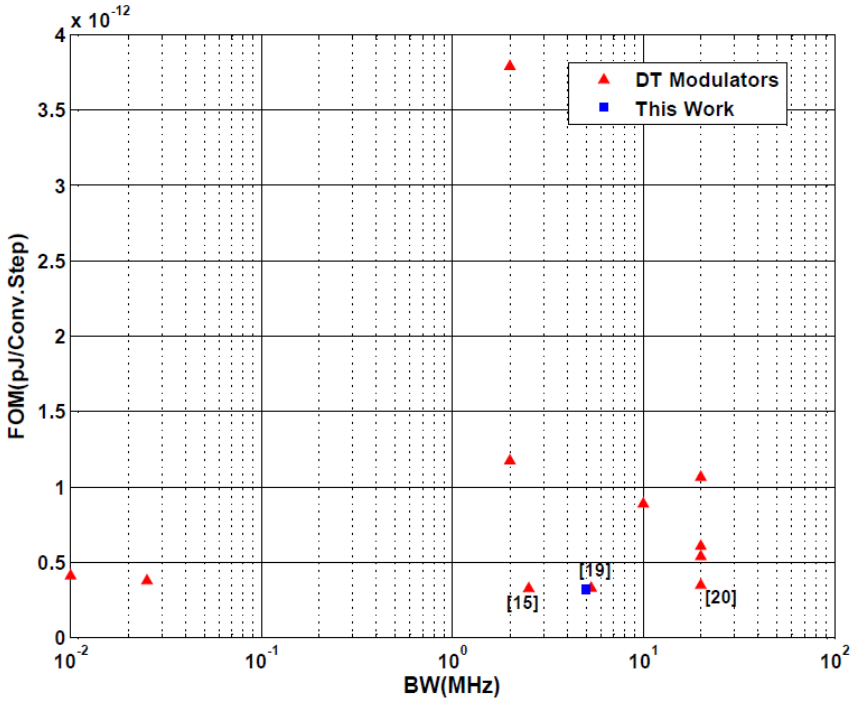


Fig. 3.20: Comparison with other state-of-the-art DT modulators.

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CHAPTER 4. CONCLUSIONS

There is increasing demand for high efficiency delta-sigma modulation data converters in a variety of applications, such as wired and wireless communication, instrumentation, medical and automotive electronics as well as consumer electronics. Large SNR over the signal band, along with excellent linearity and wide dynamic range, should be provided in a power-efficient manner for these data converters. It is also important to extend the signal bandwidth for these data converters substantially without performance degradation to accommodate fast-growing recent wideband applications. Architectural innovations, together with efficient circuit design, are required to accomplish the design goals and to meet various stringent design specifications. In this dissertation, several enabling design techniques to improve the efficiency of delta-sigma modulation data converters were introduced, and the effectiveness of the proposed techniques was verified by experiments with state-of-the-art prototype designs.

In chapter 1, a review of discrete-time and continuous-time delta-sigma modulators was presented. As mentioned, oversampling ΔΣ modulators are the best choice for the high resolution and high speed applications such as wireless and wire-line communication. However, there are several practical issues that will limit their performance. These effects were studied and some solutions and techniques were discussed.

In chapter 2, a novel low power compact loop filter using a single amplifier biquad (SAB) filter was presented for continuous-time (CT) delta-sigma (ΔΣ) modulators. This new technique saves power consumption and die area by minimizing the number of active elements in the modulator. Additionally, because the new technique reduces the feedforward branches to the summing block in the modulator, a switch-capacitor (SC) adder replaces the commonly used CT adder and the sample & hold blocks in the conventional architecture. These two techniques simplify the design and implementation of the high-order continuous-time ΔΣ modulator. The proposed loop filter is a general filter which can be used for both high and low oversampling ratios (OSRs). A 4th-order

low pass continuous-time ΔΣ modulator was designed and implemented in 130nm IBM process to confirm the effectiveness of the proposed techniques. With a 10 MHz signal bandwidth, the measured dynamic range and SFDR of this prototype IC are 80 dB and 82.4 dB with an analog power consumption of 11.4 mW.

In chapter 3, a new stage-sharing technique was presented for a low-power wide-bandwidth DT MASH ΔΣ ADC. This technique eliminates active elements from the second stage of the MASH modulator to save power and chip die area. Furthermore, the proposed technique shares the op-amps of the modulator first stage with its second stage amplifiers during two different non-overlapping clock phases. Coefficent scaling techniques also were applied to the proposed modulator to boost the DR and reduce the power dissipation. The required system and circuit details were described. A 2-2 stage-shared MASH delta-sigma modulator was designed and tested to verify the effectiveness of the stage-sharing technique. The modulator has achieved SNR, SNDR, and DR of 75.7 dB, 75.8 dB and 78 dB, respectively in a bandwidth of 5 MHz, and a FOM of 0.32 pJ/cov.

4.2 FUTURE WORK

In recent years, WiMAX emerged as an option for broadband wireless communication access, achieving high data rates and mobile coverage. The standard is deployed in licensed worldwide spectrum allocations at 2.3 GHz, 2.5 GHz, 3.3 GHz, and 3.5 GHz frequency bands. For flexible spectrum utilization, scalable channel bandwidths are allowed in this standard, ranging from 1.25 MHz to 20 MHz. Orthogonal frequency division multiplexing (OFDM) is used for improved multi-path performance, while various modulation techniques can be supported to improve bandwidth efficiency, including quadrature phase shift keying (QPSK), 16-QAM, and 64-QAM [1].

For WiMAX receivers, a direct-conversion (DC) architecture is usually preferred because of lower power consumption and fewer external components compared to a super-heterodyne approach [2, 3]. To successfully demodulate low-level channel signals along with high power interferers, blocker filtering can be performed in the radio frequency (RF) front-end, which consists of a low noise amplifier (LNA) and I/Q downconversion mixers, or analog baseband signal chain. In the most commonly used architectures, a high linearity baseband channel select filter is used to suppress interferers.

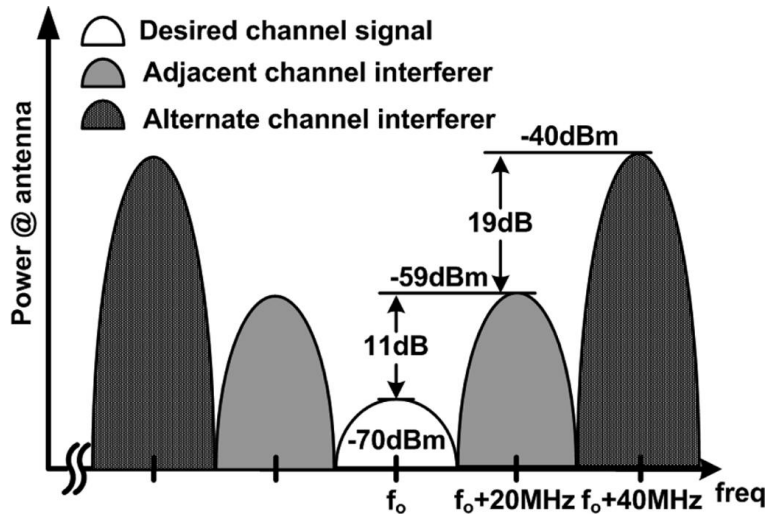

Fig. 4.1: WiMAX blocker profile for 16-QAM modulation with a half coding rate.

As an example, Fig. 4.1 shows the template of the desired signal and interferer levels for 16-QAM with a half coding rate [4]. The desired-channel power is set at 3 dB above the sensitivity levels, which is 70 dBm while the adjacent (20 MHz offset) and alternate channel (40 MHz offset) interferers have 59 dBm and 40 dBm power levels.

Since most baseband systems have inherently lower pass-band corners, the component values required by all passive implementations are relatively high. To save power consumption, a high-order passive filter or a surface acoustic wave (SAW) filter can be used, but it would take more silicon or printed circuit board (PCB) area and have a higher insertion loss with respect to active implementations. Most of the state-of-the-art approaches indeed favor integrated active filters over discrete (or passive) filters. However, the noise and linearity characteristics of a high-order active filter leads to considerable power consumption. Figure 4.2 shows the system level diagram of the DC receiver. After down converting the received signal to the IF band, an IF low-pass (LP) filter is used to attenuate both the adjacent channel and the blocker interferers. Between the LP filter and the ADC, a variable gain amplifier (VGA) is utilized to adjust the dynamic range and also further reduce the gain in the present of an strong blocker interferer. The feedback from the digital-signal-processing (DSP) unit to the VGA block properly selects the gain prior to the ADC block. As the drawbacks of this architecture, it has an Nth-order LP filter increasing the power dissipation and the chip area since an active filter is used. In addition, the VGA block decreases the gain in the presence of a strong blocker interferer through the feedback from the DSP block showing that the ADC has been saturated.

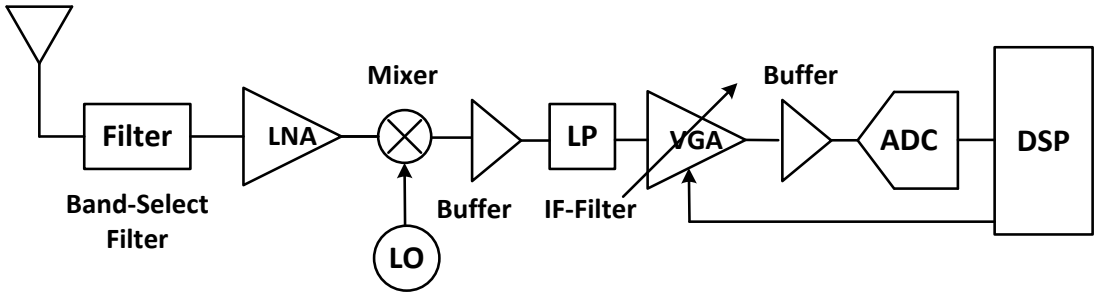

Fig. 4.2: Conventional direct-conversion receiver architecture.

Furthermore, a strong blocker detection in this approach is accomplished by saturating the ADC with the blocker. As a sequence, the data during the time that the ADC is saturated will be missed. To optimize power consumption and reduce the area and also create' an adaptive blocker detection scheme is proposed which avoids the saturation of the ADC in the presence of an strong blocker. Figure. 4.3 shows the proposed DC receiver architecture which utilizes an adaptive blocker interferer detection sheme to quickly detect the blocker in the analog domain and provide the feedback signal to the VGA block. In this topology, the location of the VGA and LP filter are swapped so that the LP filter can be merged to the ADC front-end (in this case a CT delta-sigma ADC). By combining the LP filter with the ADC front-end, there is no need to have extra active blocks for the LP filter which saves power and chip die area.

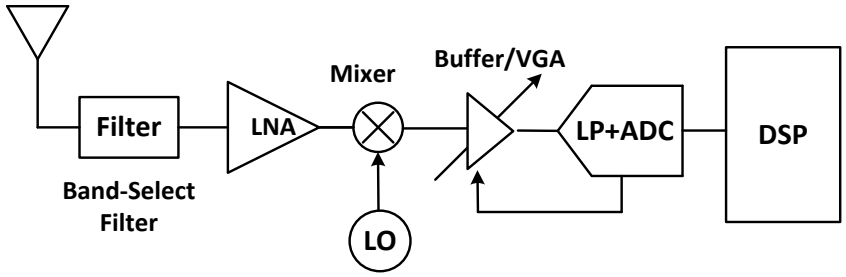

Fig. 4.3: Direct-conversion receiver architecture with the proposed adaptive blocker detection scheme and the compact low-IF section.

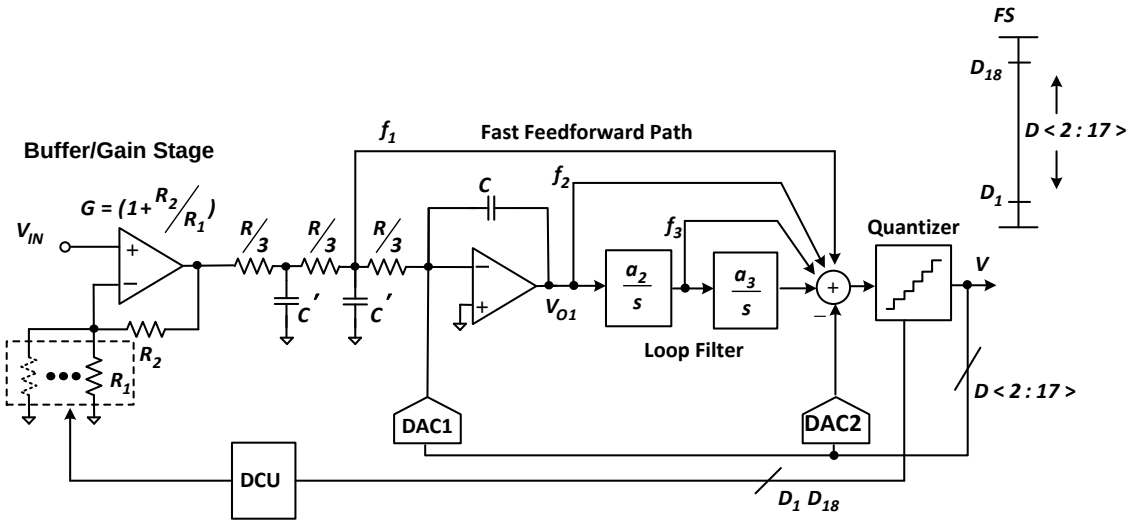

Fig. 4.4: Implementation of the proposed compact low-IF section of the DC receiver with an adaptive blocker detection scheme.

Figure 4.4 illustrates the circuit diagram of the proposed compact low-IF section of a DC receiver architecture. The ADC used in this topology is a 3rd-order CT delta-sigma modulator which a 2nd-order LP filter is combined with its front-end taking benefit of the front-end amplifier's virtual ground. Combining the LF filter with, the ADC front-end eliminates the need for the active blocks in the LP filter. In this topology, the modulator inner quantizer is acting also as the blocker detector. Since the low-distortion architechture is utilized in the modulator, the input signal directly appears at the input of the quantizer instead of going through the loop filter. As a result, the loop filter is not saturated in the presence of an strong blocker because the feedforward path bypasses the input signal from the loop filter. Consequently, the quantizer which uses two extra levels to detect an over ranged amplitude, detects the presence of the blocker and quickly sends the 2-bit digital feedback signal to the buffer/ VGA block to reduce the gain to attenuate the blocker.

Figure 4.5 shows that in the presence of an interferer, the VGA block gain is reduced to one, so it acts as a buffer stage. Meanwhile, in the absence of the blocker, the VGA block boosts the gain to maximize the modulator SNDR as depicted in Fig. 4.6. Consequently, this new approach reduces the base-band section power and area by combining the low-pass filter block with the ADC front-end and also make the blocker rejection mechanisim fast and robust utilizing the ADC inner quantizer as the blocker detector block. Since the blocker does not go through the modulator loop filter and it is applied to the quantizer input using the low-distortion architecture, the modulator will not be unstable during the blocker detection phase to not to lose the coming data.

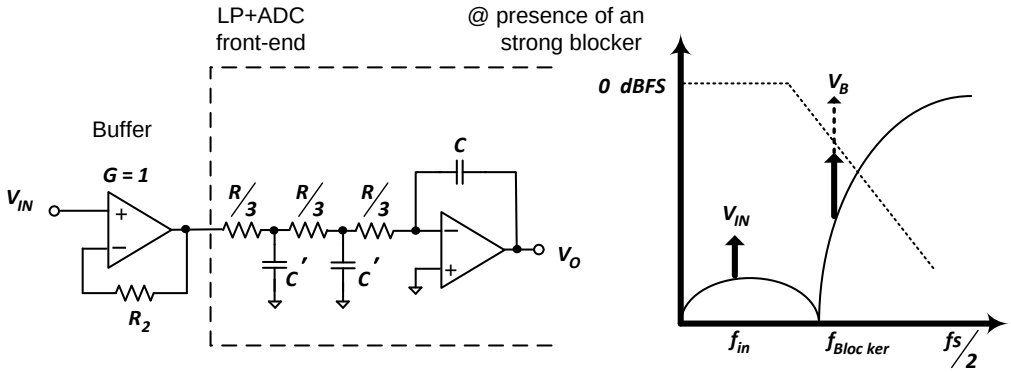

Fig. 4.5: Operation at the presence of an interferer.

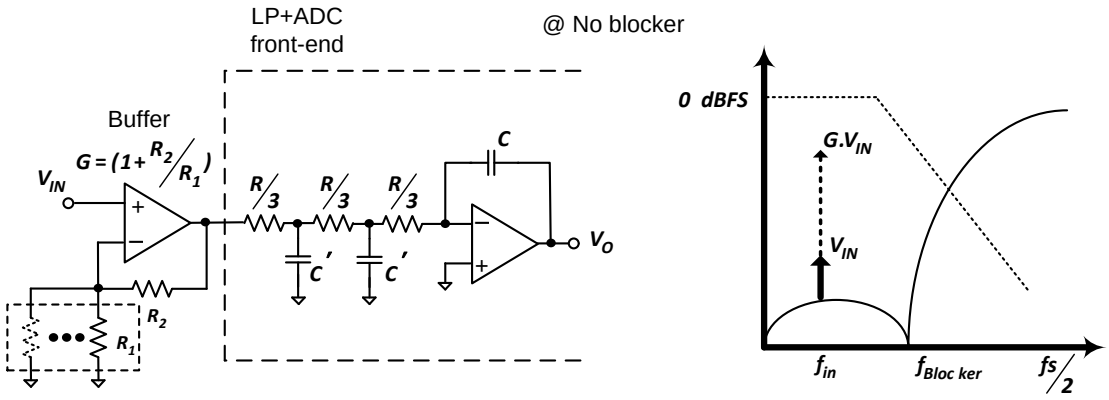

Fig. 4.6: Operation in the absence of an interferer.

As the next step, the proposed blocker rejection scheme will be implemented to prove the the effectiveness of the scheme.

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APPINDEX A. A NEW ZERO-OPTIMIZATION SCHEME FOR NOISE-COUPLED ΔΣ ADCs

Abstract

This Chapter presents a new zero-optimization scheme for noise-coupled ΔΣ analog-to-digital converters (ADCs). The proposed technique enhances the signal-to-quantization-noise-ratio (SQNR) by optimizing noise-transfer-function (NTF) zero locations to get maximum in-band noise shaping. The amount of SQNR improvement using the new scheme depends on the order of the modulator. Therefore, zero optimization will be used in a first-order and a second-order modified noise-coupled ΔΣ ADCs. The proposed technique enhances the SQNR of the first-order and second-order noise-coupled ΔΣ modulators by 4.5 dB and 8.5 dB, respectively.

A.1 INTRODUCTION

There is a large demand in wired and wireless communication systems for high-performance analog-to-digital converters which have a wide signal bandwidth and high resolution. Oversampling ADCs use more digital signal processing to perform analog-to-digital conversion compared with Nyquist-rate ADCs. The advantage is significantly relaxed matching requirements on analog components, while still achieving medium to high resolution [1]. Furthermore, oversampling ADCs do not need steep roll-off anti-alias filtering typically required in Nyquist-rate ADCs. Conceptually, delta-sigma ADCs provide high resolution and linearity while using a low-resolution quantizer by taking advantage of oversampling and noise shaping. There are several design parameters: quantizer resolution, loop filter order, oversampling ratio (OSR). Increasing any of these parameters improves the SQNR [1, 2]. Meanwhile, for wide-band applications, the OSR of the modulator cannot be too high because of the amplifiers power consumption requirements. Consequently, one of the options to meet the demanding target with low OSR is increasing the modulator order. But a modulator with higher order loop filter will also result in more power dissipation by adding more active blocks. As an alternate solution, the noise-coupling technique was introduced by [3, 4] to enhance quantization

noise shaping in ΔΣ modulators without adding any active circuit blocks. As shown in Fig. A.1, a first-order noise shaping enhancement can be achieved by extracting the quantization noise and coupling it to the loop filter output after a one-cycle delay. According to (A.1), the noise-coupling technique adds just one zero to the NTF at DC ($z = 1$).

$$NFT = \frac{1}{1 + H_{LF}(z)} \ (1 - z^{-1}) \qquad (A.1)$$

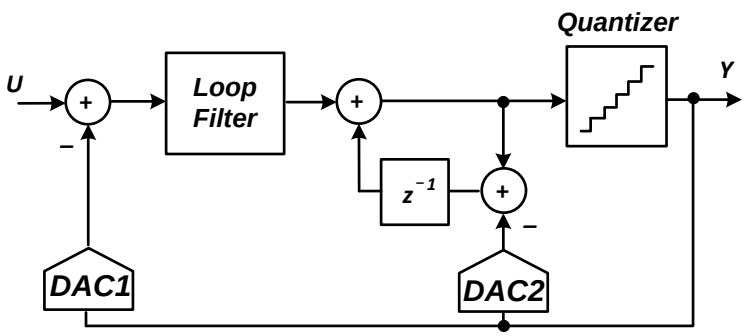

Fig. A.1: The block diagram of general feed-forward ΔΣ ADC.

This chapter presents zero optimization in the noise-coupled ΔΣ modulators to achieve more noise shaping enhancement. New architectures are proposed for the first-order and

A. 2 1st-ORDER NOISE-COUPLED ΔΣ WITH THE PROPOSED ZERO OPTIMIZATION SCHEME

The block diagram of a conventional second-order ΔΣ ADC with feed-forward branches is depicted in Fig. A.2. There is a negative feedback path creating a resonator in the loop filter transfer function as shown in (A.2). This moves the NTF zeros from their initial location ($z = 1$) according to equation (A.3).

$$LF(z) = \frac{2z^{-1} - z^{-2}}{(1 - z^{-1})^2 + gz^{-2}} \qquad (A.2)$$

$$NTF(z) = \frac{(1 - z^{-1})^2 + gz^{-2}}{1 + gz^{-2}} \qquad (A.3)$$

The NTF pole/zero location of the second-order modulator for different feedback values are depicted in Fig. A. 3. For $g = 0$ (no resonator), zeros and poles are placed at DC and infinite frequencies, respectively. Moving zeros from DC can improve in-band noise shaping, but there is an optimum value for g to achieve maximum SQNR enhancement. The magnitude of $NTF(z) = (1 - z^{-1})^2$ in the pass-band is approximately ω^2; then, by shifting NTF zeros from $z = 1$ to $z = e^{\pm j\alpha}$, the magnitude of the NTF in the band of interest becomes $(\omega - \alpha)^2$. The integral of the square of this quantity over the pass-band is a measure of the in-band noise [5], and can be minimized by choosing α such that $I(\alpha)$ is minimized in (A.4).

$$I(\alpha) = \int_0^{\omega_B} (\omega^2 - \alpha^2)^2 \, \partial\omega \qquad (A.4)$$

where ω_B is the signal bandwidth. As a result, the optimum value for α will be:

$$\alpha_{opt} = \omega_B \cdot \frac{T}{\sqrt{3}} = \pi/(OSR.\sqrt{3}) \qquad (A.5)$$

After finding the optimum frequency of the shifted NTF zeros, the optimum value for the feedback path weight can also be calculated:

$$z|_{\cdot NTF=0} = 1 \pm j\sqrt{g} \qquad (A.6)$$

$$g_{opt} \approx \alpha_{opt}^2 \qquad (A.7)$$

Depending on the OSR of the modulator, the optimum value of the feedback path weight will change. Figure A.4 plots the variation of g_{opt} versus the OSR, using (A.7) and an exact optimization approach. It is clear that the optimum value of g utilizing the

approximate calculation is close to the exact optimization approach for medium-to-high OSRs. Additionally, by increasing the OSR, g_{opt} becomes smaller, and this makes the zero optimization more practical for low-to-medium OSR applications. While the noise-coupling technique just adds a zero to the NTF at DC frequency as shown in equation (A.1), it cannot move zero locations to optimize the maximum achievable in-band noise shaping. Figure A.5 illustrates the block diagram of a noise-coupled first-order ΔΣ modulator with zero-optimizing feedback path which is found by signal flow graph (SFG) manipulations. The extracted loop filter and noise transfer functions are identical to (A.2) and (A.3). Therefore, the proposed idea optimizes both the zero of the noise-coupling scheme and the zero of the last integrator.

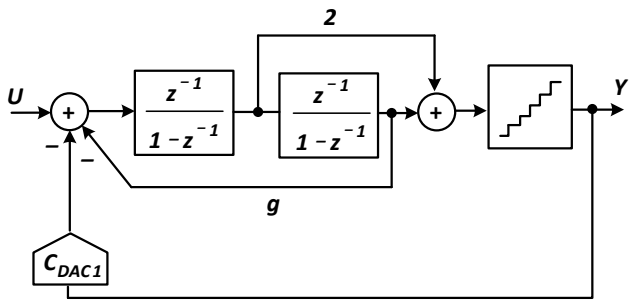

Fig. A.2: Block diagram of a 2nd-order conventional ΔΣ ADC.

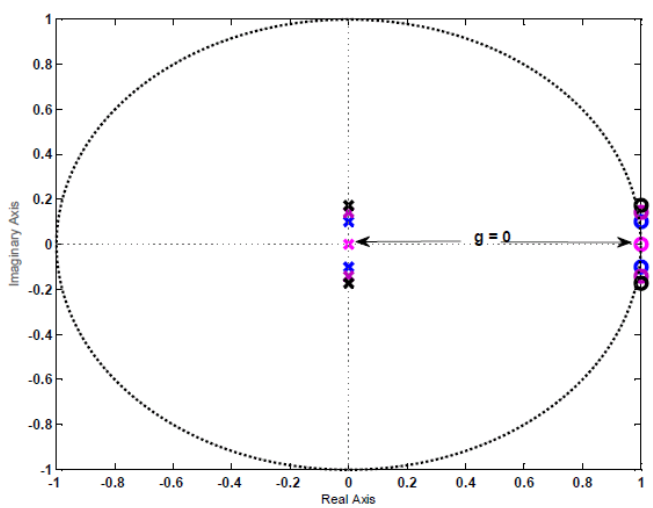

Fig. A.3: The NTF Pole/ zero location of a 2nd-order modulator for different feedback path weights.

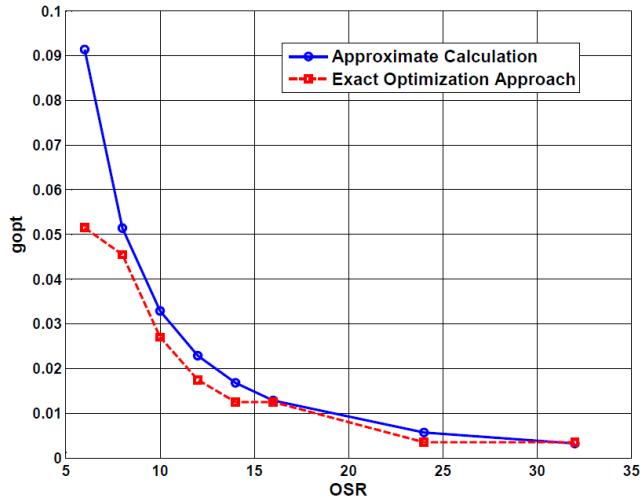

Fig. A.4: The g_{opt} variation versus the OSR for a zero-optimized 2nd-order ΔΣ modulator.

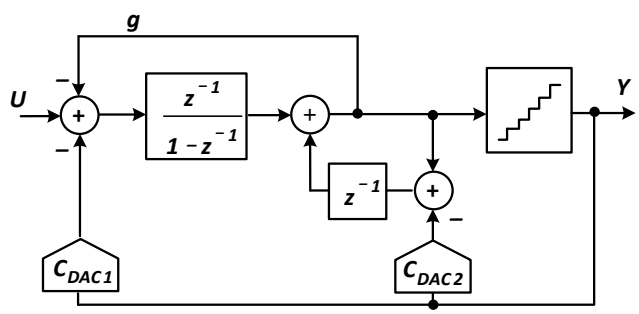

Fig. A.5: The block diagram of the first-order noise-coupled ΔΣ ADC with zero optimization.

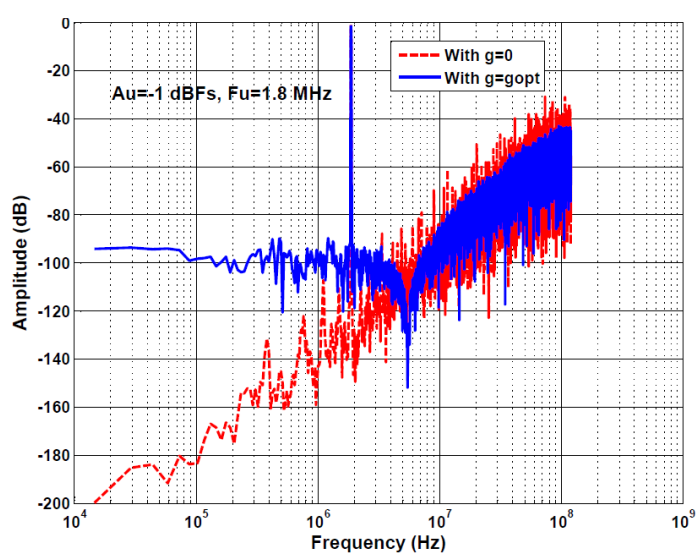

Fig. A.6: PSD of the proposed 1st-order noise-coupled ΔΣ ADC.

Matlab simulation results show 4.5 dB SQNR improvement for the first-order noise-coupled modulator using the zero optimization scheme. The modulator has an OSR, and signal bandwidth of 12 and 10 MHz, respectively. Output power spectral densities of the modulator with and without zero optimization have been depicted in Fig. A.6. It should be mentioned that shifting zeros from DC decreases the noise filtering around DC. Zero-optimized modulator can achieve SQNR of 71 dB with an input signal amplitude and frequency of -1 dBFs and 1.8 MHz, respectively.

A. 3 2nd-ORDER NOISE-COUPLED ΔΣ WITH THE PROPOSED ZERO OPTIMIZATION SCHEME

The block diagram of a 3rd-order conventional ΔΣ ADC with feed-forward branches is shown in Fig. A.7. Again, using a feedback path, one pair of zeros is shifted from DC to enhance the modulator SQNR. Equations (A.8) and (A.9) illustrate the modulator loop filter and noise transfer functions. Four active components are required to realize three integrators and one adder block of the modulator. Using the modified second-order noise-coupled ΔΣ ADC depicted in Fig. A.8, one active block can be saved. In the proposed modulator, the negative feedback path from the output of the last adder to the input of the second integrator creates a resonator for the loop filter of the noise-coupled ΔΣ ADC. The second feed-back DAC (DAC2) has been added to enhance the modulator stability. Furthermore, the proposed 2nd-order noise-coupled modulator has the same loop filter and noise transfer functions as the conventional 3rd-order modulator.

$$LF(z) = \frac{3z^{-1} - 3z^{-2} + (3g+1)z^{-3}}{(1-z^{-1})[(1-z^{-1})^2 + gz^{-2}]} \qquad (A.8)$$

$$NTF(z) = \frac{(1-z^{-1})[(1-z^{-1})^2 + gz^{-2}]}{1 + gz^{-2} + 2gz^{-3}} \qquad (A.9)$$

Figure A.9 shows the output power spectral densities of the proposed 2nd-order noise-coupled modulator with and without zero optimization. The OSR and signal bandwidth of

the modulator are 12 and 10 MHz, respectively. In this case, zero optimization improves the SQNR by 8.5 dB; also, noise at lower frequencies is reduced because of the third zero at DC. The zero-optimized modulator can achieve an SQNR of 87 dB with an input signal amplitude and frequency of -1 dBFs and 1.8 MHz, respectively. To generalize the zero optimization scheme for the noise-coupled ΔΣ ADCs with different orders, Table A.1 illustrates the optimized NTF zero locations (using approximate calculation) and the SQNR improvement of the modulator.

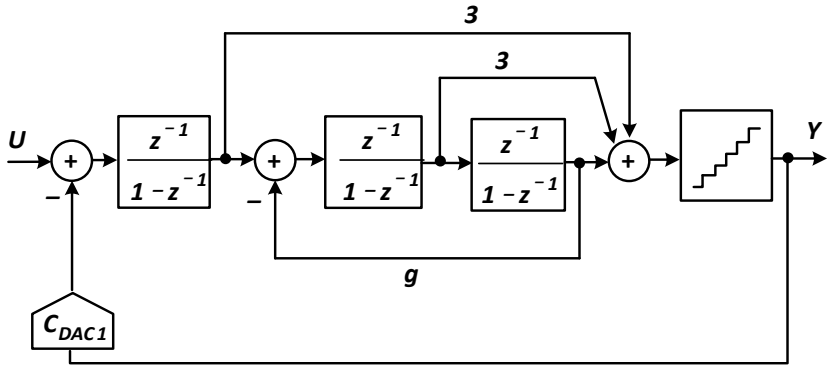

Fig. A.7: PSD of a 3rd-order conventional ΔΣ ADC.

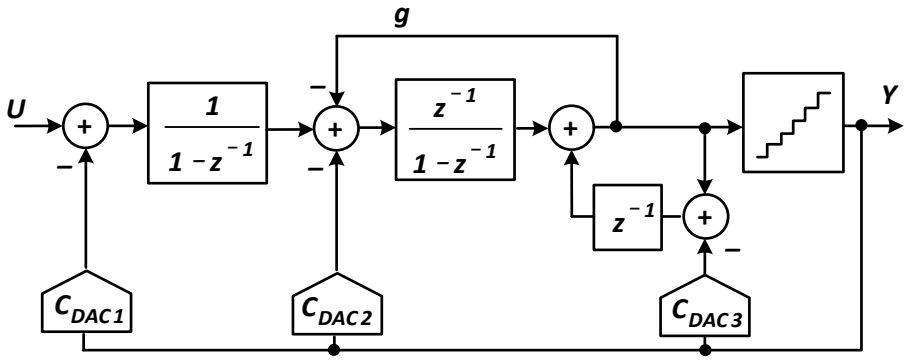

Fig. A.8: The block diagram the proposed 2nd-order noise coupled ΔΣ ADC with zero optimization.

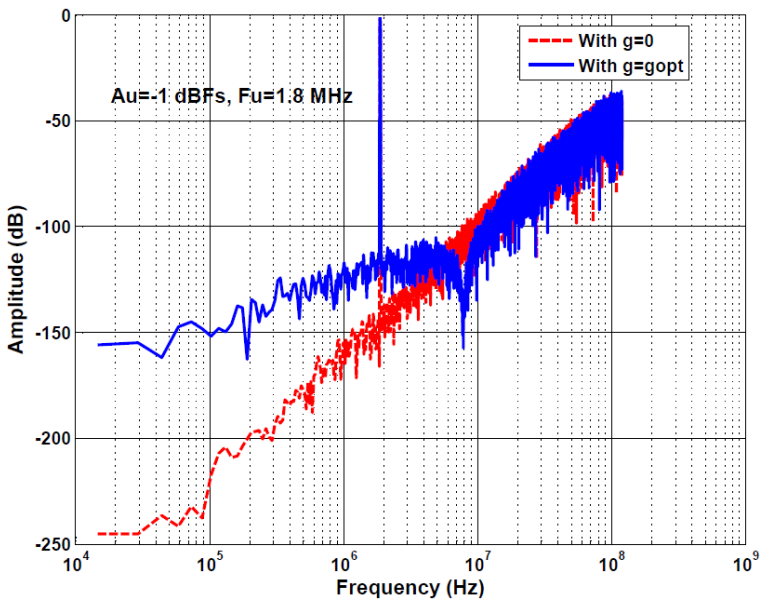

Fig. A.9: PSD of the proposed 2nd-order noise-coupled ΔΣ ADC.

Table A.1: OPTIMIZED NTF ZERO LOCATIONS AND SQNR IMPROVEMENT FOR DIFFERENT ORDER A NOISE COUPLED ΔΣ ADC

N	Optimized Zero Locations	SQNR Imp.
1	$\pm\omega_B/\sqrt{3}$	4.5 dB
2	$0, \pm\omega_B\sqrt{3/5}$	8.5 dB
3	$\pm\omega_B\sqrt{3/7 \pm \sqrt{(3/7)^2 - 3/35}}$	14 dB
4	$0, \pm\omega_B\sqrt{5/9 \pm \sqrt{(5/9)^2 - 5/21}}$	19.5 dB

A.4 DESIGN EXAMPLE

As a demonstration of the proposed zero optimization scheme in a noise-coupled ΔΣ ADC, the circuit diagram of the first-order modulator has been shown in Fig. A.10. For simplicity just a half circuit diagram has been drawn. The delay cell utilized in the noise-coupling technique has two sets

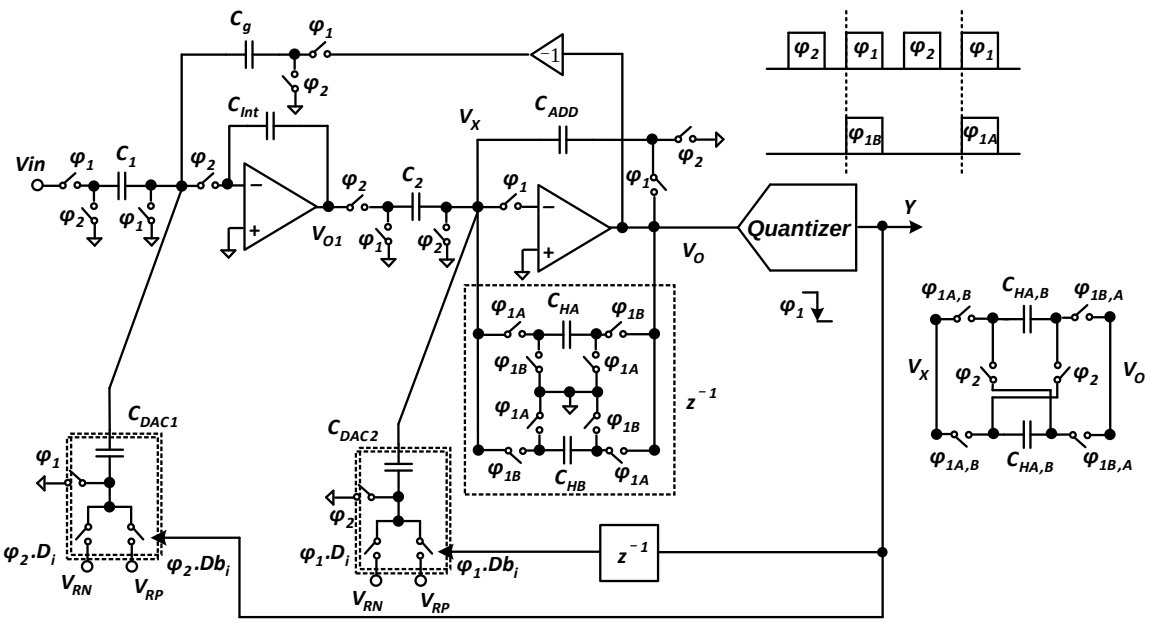

Fig. A.10: The circuit diagram of the 1st-order noise-coupled ADC ΔΣ with zero optimization.

of capacitors C_{HA} and C_{HB} to sample and hold the adder output at two clock phases φ_{1A} and φ_{1B} which can be generated using a frequency divider in the clock generator. When φ_1 is high, the front-end integrator is in the sampling mode, and the adder block is operating by summing the pre-sampled data; meanwhile, one of the delay cell capacitors is connected between the common-mode voltage and the adder virtual ground, depending on φ_{1A} and φ_{1B} clock phases. At the falling edge of φ_1, the data becomes ready at the quantizer output. When φ_2 is high, the first stage and the adder are in the integrating and resetting modes, respectively. At the same time, the charge on C_{HA} and C_{HB} is held by cross-coupling and connecting the same capacitors with opposite polarity in the complementary circuit, as illustrated in Fig. A. 10. The simulated output spectrum of the modulator with a -1 dBFs input signal assuming a 10 MHz signal bandwidth, an oversampling ratio of 12, and 4-bit quantizer is depicted in Fig. A.11. The macro model op-amps used in the noise-coupled modulator have 50 dB finite gain to achieve an SNDR of 68.5 dB.

A. 5 SUMMARY

A new zero optimization scheme is proposed for noise-coupled ΔΣ ADCs. This technique improves the in-band noise shaping by optimizing the NTF zero locations. The proposed technique enhances the SQNR of first-order and second-order noise-coupled ΔΣ ADCs by 4.5 dB and 8.5 dB, respectively.

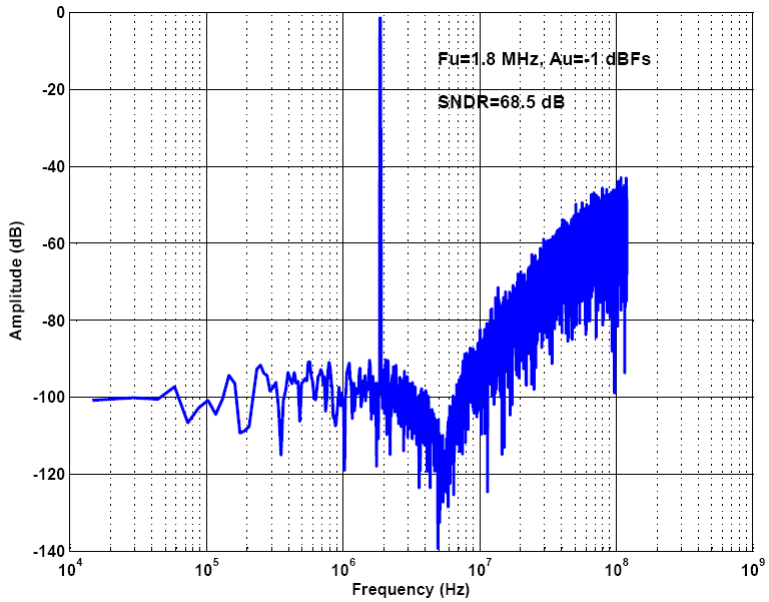

Fig. A.11: Spectre PSD of the 1st order noise-coupled ΔΣ ADC with zero optimization.

As an example, a first-order noise-coupled delta-sigma modulator was designed and simulated to verify the effectiveness of the proposed scheme.

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APPENDIX B. AN OPAMP SHARING TECHNIQUE FOR CONTINUOUS-TIME ΔΣ MODULATORS

Abstract

This chapter presents a new operational amplifier sharing technique for a continuous-time ΔΣ analog-to-digital converter (ADC). This technique saves power consumption by reducing the number of active elements in the modulator. Furthermore, the shared amplifier acts both as an adder and integrator in two different clock phases. The proposed technique also can be realized in a noise-coupled delta-sigma ADC. To verify the idea, a 2nd-order continuous-time ΔΣ modulator has been designed and simulated successfully with and without noise-coupling techniques.

B. 1 INTRODUCTION

There is a significant need in wired and wireless communication systems for high-performance analog-to-digital converters which have a wide signal bandwidth and high resolution. Oversampling ADCs use more digital signal processing to perform analog-to-digital conversion compared with Nyquist-rate ADCs. They have the advantage of significantly relaxed matching requirements on analog components, while still achieving medium to high resolution [1]. Furthermore, oversampling ADCs do not need steep roll-off anti-aliasing filters, which is usually required in Nyquist-rate ADCs. A majority of ΔΣ modulators are based on switch-capacitor (discrete-time) circuit techniques. Alternately, ΔΣ modulators with continuous-time (CT) loop filters can potentially achieve higher clock frequencies and/ or consume less power [2]. Additionally, continuous-time ΔΣ ADCs exhibit an inherent anti-alias filter function, due to the non-sampled input stag. This attribute enables the design of alias-free ADCs [3]. Figure B.1 shows a CT delta-sigma modulator with feed-forward architecture, which is one of the most commonly used architectures for wideband high performance ΔΣ ADCs.

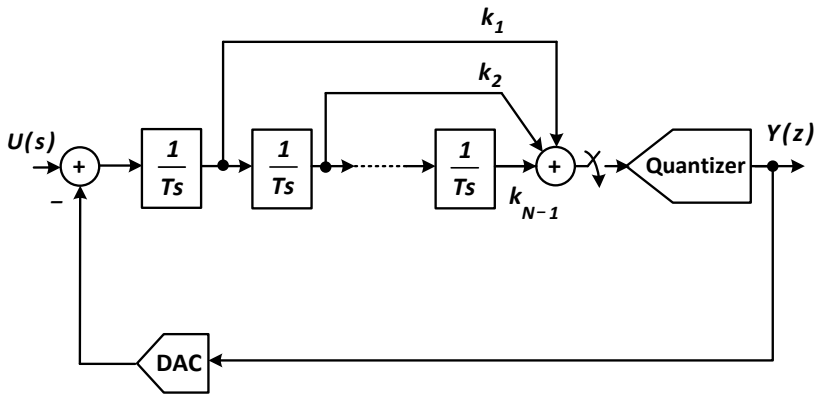


Fig. B.1: Block diagram of general feed-forward ΔΣ ADC.

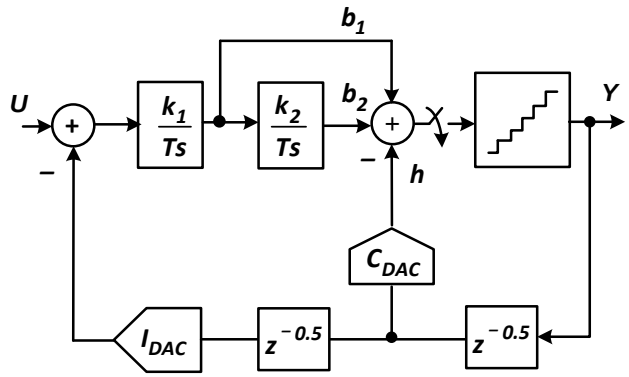


Fig. B.2: Block diagram of a 2nd-order CT ΔΣ ADC.

B.2 2nd-ORDER CT ΔΣ WITH THE PROPOSED OPAMP SHARING TECHNIQUE

The block diagram of a conventional second order ΔΣ ADC with feed-forward branches is depicted in Fig. B.2. In CT delta-sigma ADCs, the signal is sampled happens at the input of the quantizer. Consequently, the loop filter and the feedback DAC operate continuously. As a current steering DAC, I_{DAC} is utilized to compensate excess loop delay. This unwanted effect, which could make the modulator unstable, is due to the timing delay created by non-ideal effects of the quantizer, loop filter, and the other digital blocks following the quantizer [4]. The adder block, adding the feed-forward and C_{DAC} feed-back signals, is also a CT adder, either active or passive. When implemented by a passive circuit, it does not consume any power. But, a passive adder is limited to a gain less than one resulting in magnified input referred quantizer non-idealities like noise. There are two options for an active adder. It can be either an opamp or a Gm

(transconductance) based adder. Consequently, there is a trade-off between power consumption and attenuation of the non-ideal effects [5]. With the op-amp as the primary active component for the integrators of the loop filter, the adder, and the sample & hold (S/H), the modulator will need four amplifiers.

There has been extensive work to decrease the number of active blocks of ΔΣ ADCs using different techniques [5-7]. Figure B.3 shows an alternative architecture for the conventional 2nd-order CT ΔΣ modulator, in which the S/H and the adder blocks have been merged and the last integrator of the loop filter has been mapped to a discrete-time integrator. Unlike the conventional architecture, the second feedback DAC and the adder blocks in the alternative architecture are switch-capacitor circuits. The modulator uses a multi-bit quantizer and non-return-to-zero (NRZ) current pulse for I_{DAC}. Furthermore, the multi-bit quantizer reduces the in-band quantization noise and lowers the clock jitter sensitivity if a NRZ multi-bit DAC is used [4]. Eliminating one active component by merging the adder and S/H blocks reduces the power consumption. It is a possible to further reduce the active blocks using the proposed opamp sharing technique. This technique shares opamps of the adder and last integrator blocks.

Figure B.4 illustrates the circuit diagram of the second-order CT ΔΣ ADC without the opamp sharing technique. When φ_1 is high, the second integrator is in the sampling mode, then the output of the first stage is sampled on to C_2. During this phase, the integrator's opamp is just holding the previous charge on C_{Int}. At the same time, the adder block is in the adding mode. When φ_2 is high, the second stage is in the integrating mode and uses its opamp. During the same phase, the adder is in the reset mode and its opamp is idle. Observing both clock phases, it is possible to eliminate one opamp if the charge of C_{Int}at φ_1 can be maintained. Figure B.5 depicts the circuit diagram of the same modulator utilizing the proposed opamp sharing technique. The circuit operation of the modulator is identical to the previous circuit, except it uses one less active block, thus reducing the power dissipation. The charge on C_{Int} at φ_1 is held by cross-coupling the C_{Int} capacitors in the complimentary circuit. (The circuit diagram of the modulator has been drawn in single-ended format just for simplicity.) To verify the effectiveness of the opamp sharing technique, the dynamic behavior of the 2nd-order CT ΔΣ modulator circuit is simulated in

Cadence Spectre simulator. Assumed a 10 MHz signal bandwidth, an oversampling ratio of 12, and 4-bit quantizer, the simulated output spectrum of the modulator with a -1 dBFs input signal is shown in Fig. B.6. The opamps are represented by macro models with finite gains and finite bandwidths ($55dB$ & $4xf_{Clk}$). Also, the modulator achieves an SNDR of 62 dB.

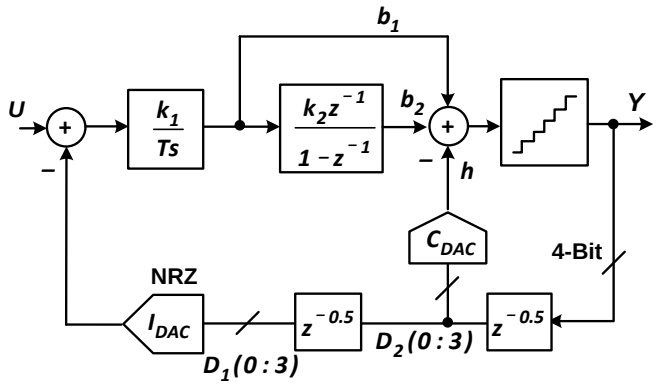


Fig. B.3: Block diagram of an alternative 2nd-order CT ΔΣ ADC.

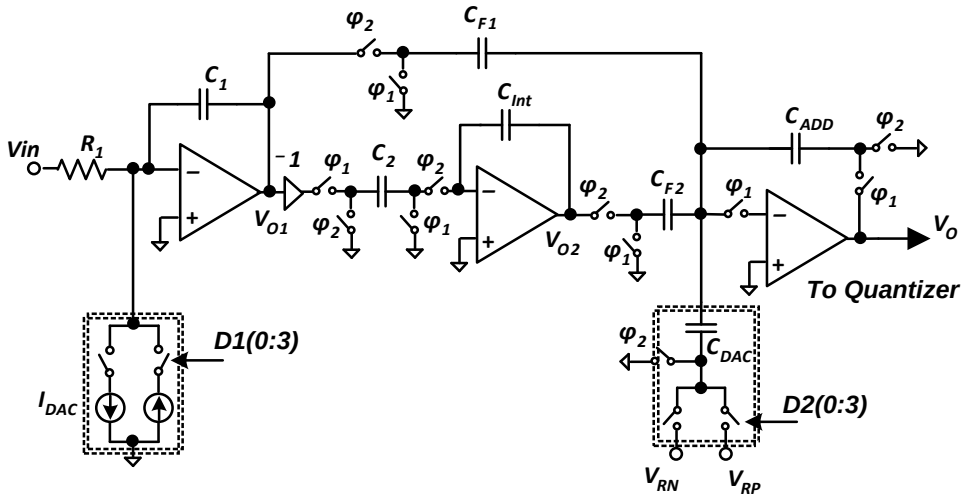
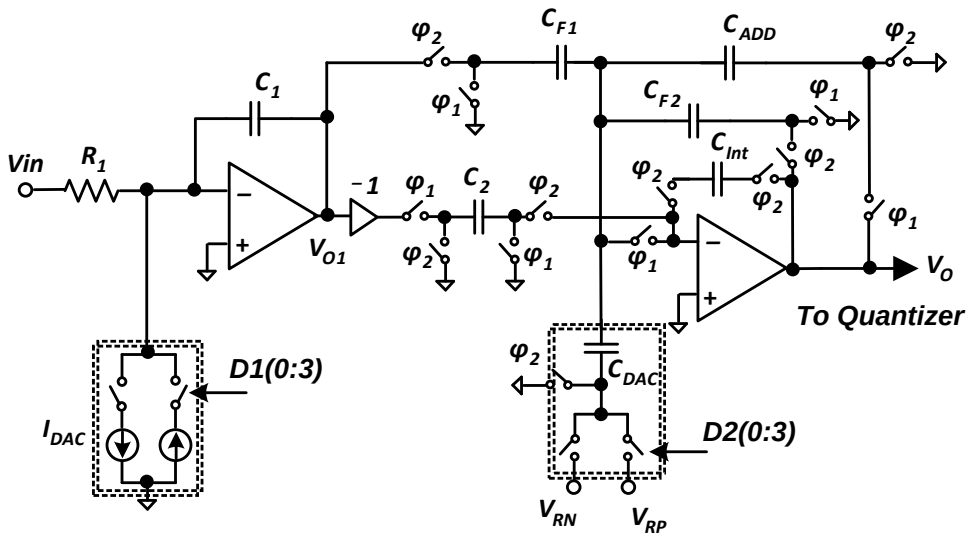
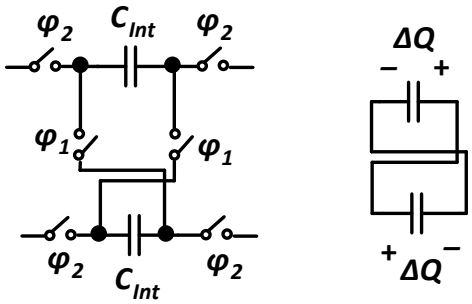


Fig. B. 4: Circuit diagram of the 2nd-order CT ΔΣ ADC without opamp sharing.



(a)



(b)

Fig. B.5: (a) Circuit diagram of the 2nd-order CT ΔΣ ADC with opamp sharing (b) Cross-coupling C_{Int} in the complementary circuit.

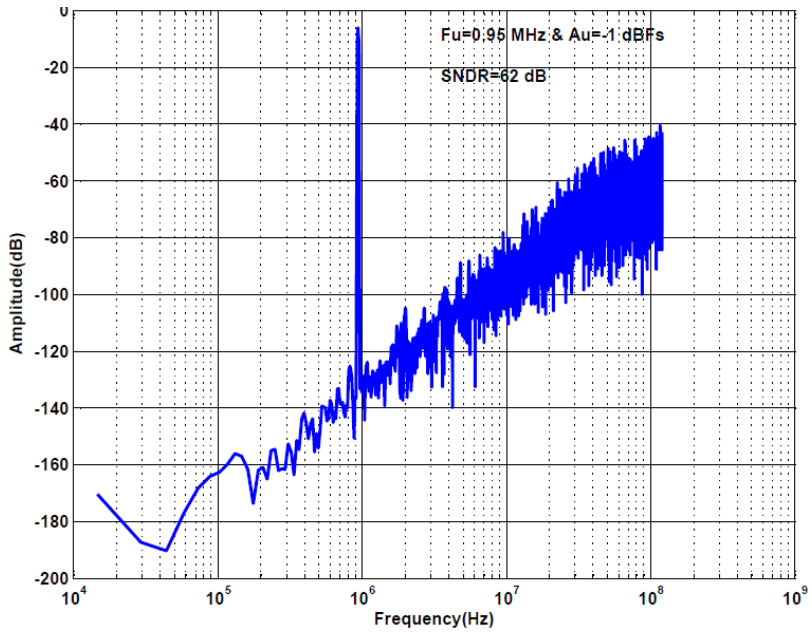


Fig. B.6: PSD of the 2nd-order CT ΔΣ ADC with opamp sharing.

B. 3 2nd-ORDER NOISE-COUPLED CT ΔΣ WITH THE PROPOSED OPAMP SHARING TECHNIQUE

One technique for decreasing an active component in the ΔΣ modulators is noise coupling, which has been introduced by [6], [8]. As is illustrated in Fig. B. 7, if the quantization noise is extracted and then coupled to the loop filter output after a one-cycle delay, a first-order noise-shaping enhancement can be achieved. Since there is a second feed-back path to the input of the quantizer in CT ΔΣ modulator to compensate excess-loop-delay, some parts of the noise-coupling scheme can be merged to simplify the system-level block diagram. The simplified second-order noise-coupled CT ΔΣ modulator is shown in Fig. B. 8, in which one DAC block has been eliminated.

The circuit diagram of the noise-coupled modulator without the op-amp sharing technique is depicted in Fig. B. 9 (for simplicity, just a half-circuit diagram has been drawn). The delay cell utilized in the noise-coupling technique has two sets of capacitors (C_{HA} and C_{HB}) to sample and hold the adder output. Unlike the other delay cell blocks, the proposed delay cell just needs two extra clock pulses (φ_{1A} and φ_{1B}) which can be generated using a frequency divider in the clock generator. When φ_1 is high, like the

previously described second order CT ΔΣ modulator, the last integrator is in the sampling mode, and its opamp holds the previous charge on C_{Int}. During the same phase, the adder block is summing the pre-sampled data; meanwhile, one of the delay cell capacitors is connected between the common-mode voltage and adder virtual ground depending on φ_{1A} and φ_{1B} clock phases. When φ_2 is high, the opamp of the second-stage is used for integration but the adder is resting. By applying the proposed opamp sharing technique, the last integrator opamp can be shared with the adder, as illustrated in Fig. B. 10. As in the circuit without noise-coupling, the charge held on C_{Int} at φ_1, and C_{HA} and C_{HB} at φ_2 is realized by cross-coupling and connecting the same capacitors with opposite polarity in the complementary circuit.

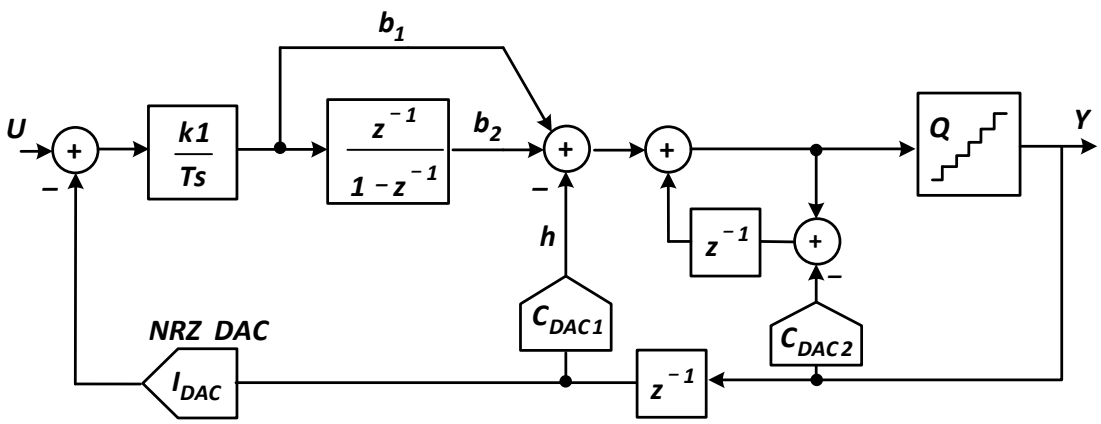


Fig. B.7: Block diagram a 2nd-order noise coupled CT ΔΣ ADC.

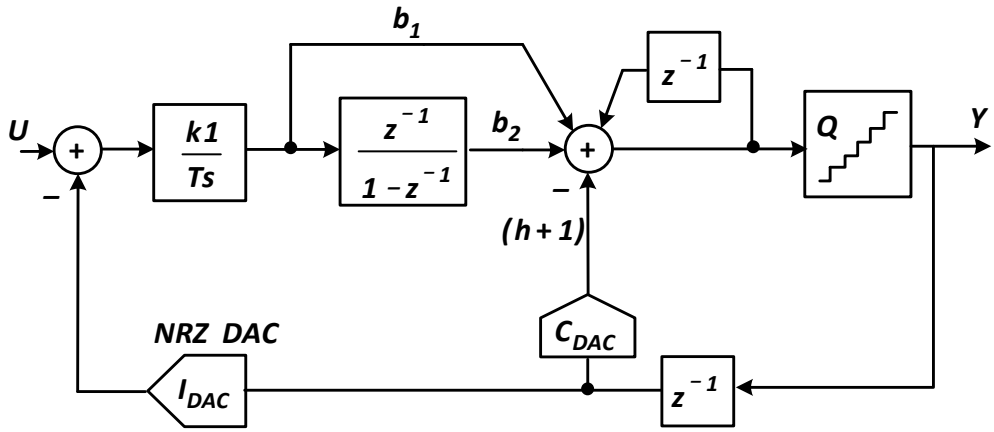


Fig. B.8: Block diagram the simplified 2nd-order noise-coupled CT ΔΣ ADC.

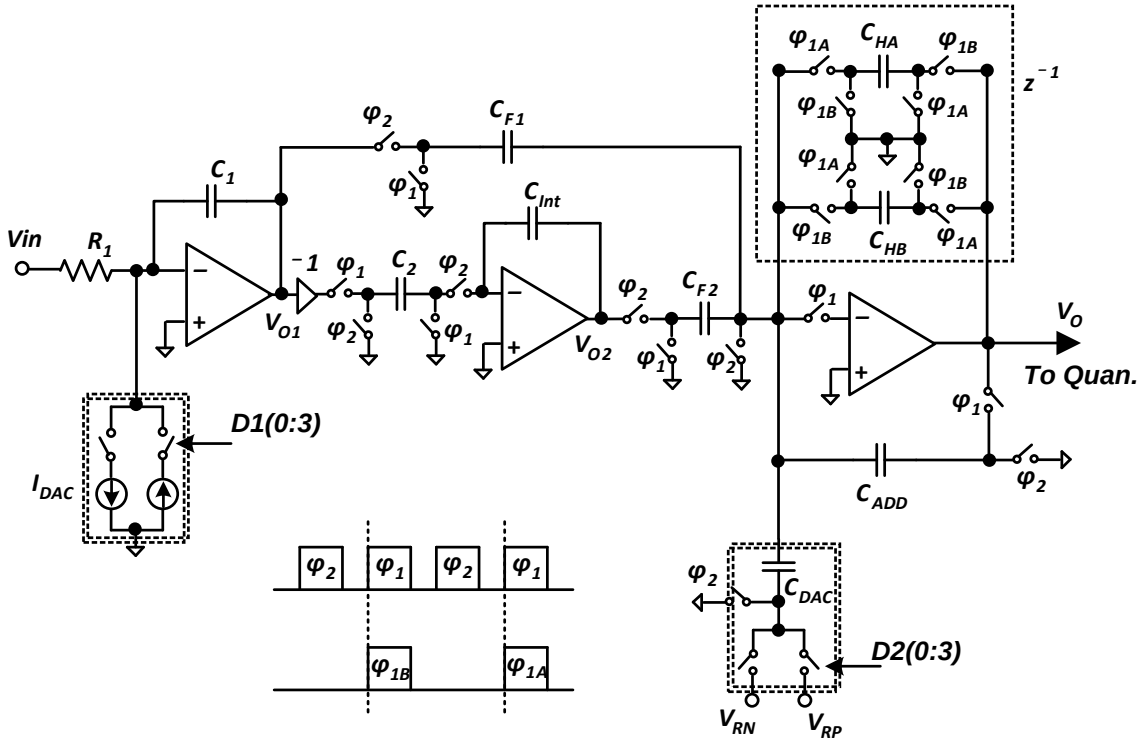
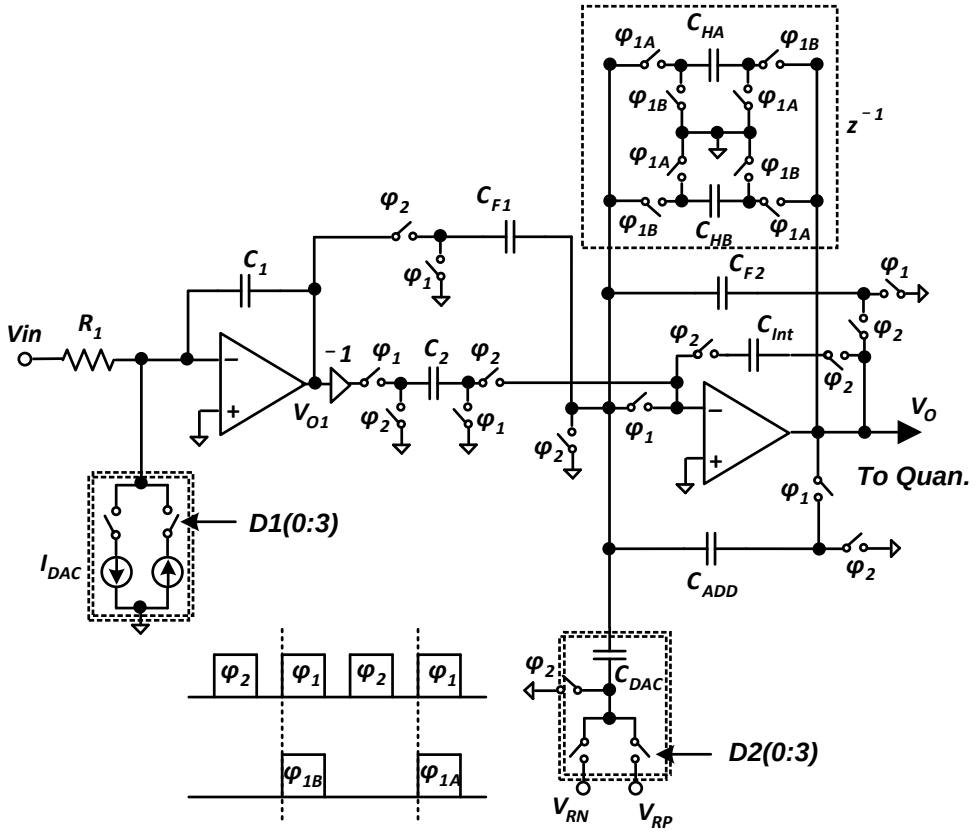
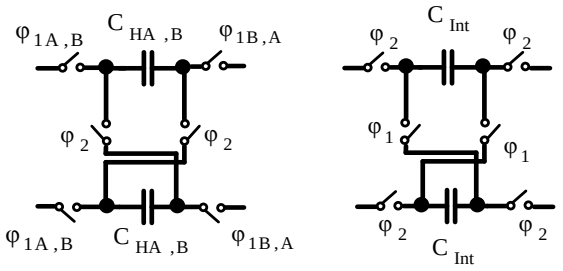


Fig. B.9: Circuit diagram of the 2nd-order noise-coupled CT ΔΣ ADC without opamp sharing.



(a)



(b)

Fig. B.10: (a) Circuit diagram of the 2nd-order noise-coupled CT ΔΣ modulator with opamp sharing (b) Cross-coupling C_{Int}, C_{HA} and C_{HB} in the complementary circuit.

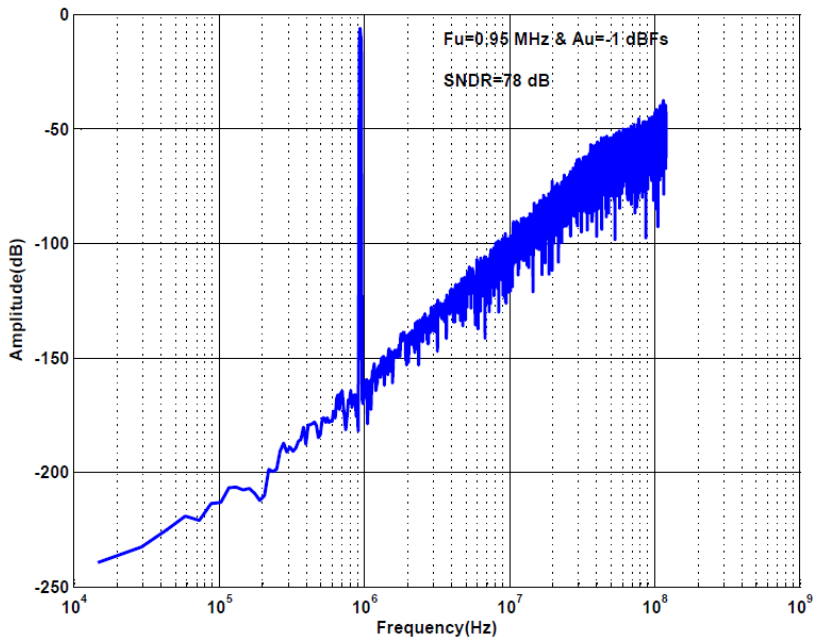


Fig. B.11: PSD of the 2nd-order noise-coupled CT ΔΣ ADC with opamp sharing.

Figure B.11 shows the simulated output spectrum of the modulator with a -1 dBFs input signal assuming a 10 MHz signal bandwidth, an oversampling ratio of 12, and 4-bit quantizer. The macro model opamps used in the noise-coupled modulator have a finite gain and finite bandwidth of 60 dB and 4.5 times clock frequency, respectively, to achieve an SNDR of 78 dB.

B. 4. SUMMARY

A new opamp sharing technique is presented for a low-power continuous-time ΔΣ ADC. This technique eliminates one active element from the modulator to save power. Furthermore, the proposed technique shares the amplifier of the adder block with the amplifier of the last integrator stage during two different clock phases. The required system and circuit details were described. Two second-order delta-sigma modulators with and without noise-coupling scheme were designed and simulated to verify the effectiveness of the opamp sharing technique.

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