AN ABSTRACT OF THE THESIS OF

Nicole L. Dehuff for the degree of Master of Science in

Electrical Engineering & Computer Science presented on March 7, 2005.

Title: Fabrication and Characterization of Thin Film

Electromagnetic Coils and Heaters for Microchannel Applications

Redacted for privacy

Abstract approved: _____

Thomas K. Plant

The focus of this thesis involves developing general fabrication processes relevant to the manufacture of two new devices for the Microscale technology Energy and Chemical Systems (MECS) program at Oregon State University. The two MECS devices developed, capture dots and transparent thin-film heaters (TTFHs), require unique process development for successful manufacture. Thick photolithography is required for the capture dots and its development is detailed. The capture dots also require copper electroplating. The copper electroplating system and process development are detailed. The TTFHs require a unique heater material, indium tin oxide (ITO). The heater deposition utilizes an ultrasonic lift-off method, also detailed. The complete manufacturing process steps of both the capture dots and the TTFHs are described. Both devices are successfully demonstrated and their electrical properties are discussed.

Fabrication and Characterization of Thin-Film Electromagnetic Coils and Heaters for Microchannel Applications

by

Nicole L. Dehuff

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Presented March 7, 2005
Commencement June 2005

Master of Science thesis of Nicole L. Dehuff presented on March 7, 2005

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ACKNOWLEDGMENTS

Thank you to everyone who has helped shape the person I am today.

"For attractive lips, speak words of kindness. For lovely eyes, seek out the good in people. For a slim figure, share your food with the hungry. For beautiful hair, let a child run his/her fingers through it once a day. For poise, walk with the knowledge that you never walk alone. People, even more than things, have to be restored, renewed, revived, reclaimed, and redeemed; never throw out anyone. Remember if you ever need a helping hand, you will find one at the end of each of your arms. As you grow older, you will discover that you have two hands; one for helping yourself, and the other for helping others."

-Audrey Hepburn

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FABRICATION AND CHARACTERIZATION OF THIN-FILM ELECTROMAGNETIC COILS AND HEATERS FOR MICROCHANNEL APPLICATIONS

1. INTRODUCTION

The goal of this thesis is to develop processes to fabricate thin-film electromagnetic coils and heaters for application in microchannel fluidic sensors and separators. The coils are devices that should produce a magnetic field strong enough to capture and hold, against channel flow, alginate beads with embedded ferroelectric/magnetic particles and sensor cells on the bead surface. This device is herein referred to as a "capture dot". The spherical, ferroelectric, alginate beads are approximately 300 μm in diameter, flowing in a square channel 500 μm by 500 μm. Figure 1.1 shows an example of the ferroelectric beads. Betta fish cells are harvested and adhere to the outer surface of the beads. Figure 1.2 shows the design for examining these fish cells. As the beads flow gently along the channel, the capture dot is activated, producing enough magnetic field to attract and hold the ferroelectric bead. When the capture dot deactivates, the magnetic field is lost and the ferroelectric bead can continue down the channel.

Also discussed are processes developed for Nickel-Chromium (NiCr) and Indium Tin Oxide (ITO) long, thin film, microscale heaters needed for separation experiments. The unique lift-off process developed to fabricate these devices is also applied to transparent electronic devices and circuit fabrication. The heaters are fabricated with copper pads, and passivation is done with plasma enhanced chemical vapor deposition (PECVD). The heaters are then placed in microchannels, used to separate a Lithium-Bromide liquid flowing in a channel slightly narrower than the actual heater width.

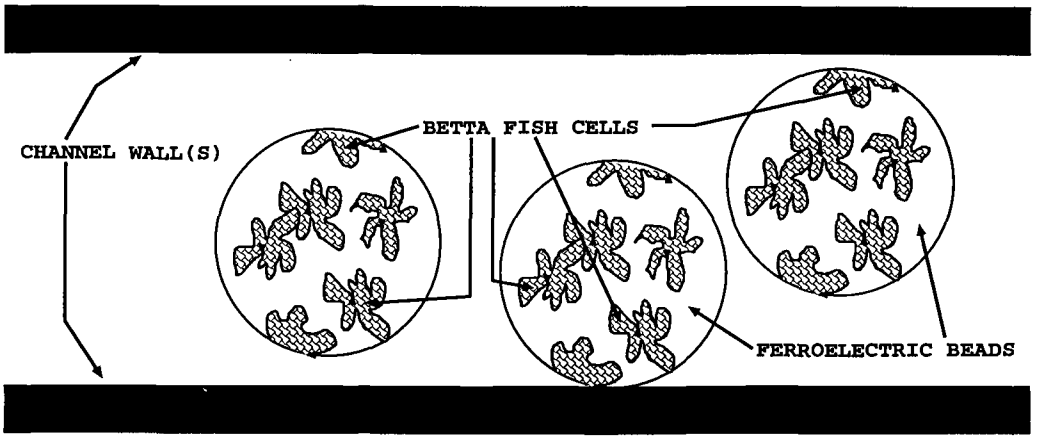

Figure 1.1: Ferroelectric beads with Betta fish cells adhered to the outer surface of the beads.

Figure of plain ferro elect. beads in the Channel-3D

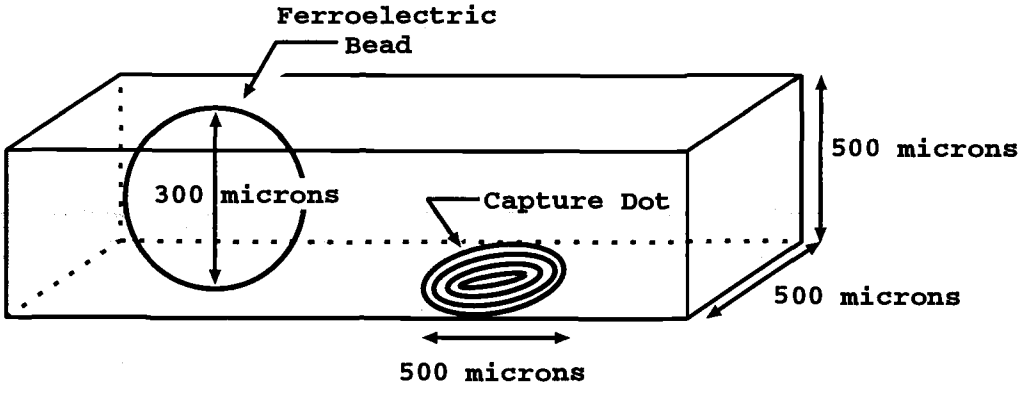

Figure 1.2: Design for bead capture.

2. LITERATURE REVIEW AND BACKGROUND

Micro Electro Mechanical Systems (MEMS) influence many areas of current technology [1]. This chapter reviews recent advances in MEMS devices. Also reviewed here are processing methods that enable MEMS technology to be manufactured. [2, 3, 4] MEMS encompasses a large body of research in industry and the academic setting. [5, 6, 7, 8] Medical devices, motor and novel electronic devices continue to become cheaper, mass produced, and more reliable with improvements made possible with MEMS technology. [9, 10] MEMS has been loosely defined as "an emerging set of technologies that make it possible to miniaturize and mass-produce large numbers of integrated sensors, actuators and computers" or as "a fabrication approach that conveys the advantages of miniaturization, multiple components and microelectronics to the design and construction of integrated electromechanical systems." [5]

2.1 Devices

MEMS devices can be as simple as tiny inductors, or as complicated as tiny motors involving multiple processing steps. [1, 11, 12] Development often demands researchers be innovative to achieve required benchmarks, pushing technology farther. [13] Novel MEMS processing has been particularly instrumental in the success of applications requiring the integration of biological components with novel electron devices, filling a void in the medical field.

One void to be filled involves cancer cell detection. Cancer research has left many doctors and patients frustrated, with needs of early detection necessary for successful treatment. To date the best method of early detection requires examining groups of polyps, looking for groups that have mutated. If groups of polyps do

not hold enough mutated cells, the cancer is not detected since an average of all the cells is considered. Individual cells can be examined; however, this is time consuming and not realistic without an automated method. An automated method of examining these individual cells, flagging ones with potential mutations is in the works, involving the use of micro-actuated arms holding individual cells to be viewed.

Other MEMS devices currently improving the medical field include: variable capacitance type sensors. The variable capacitance sensors are used to measure three items: force, bending and torsion in artificial fertilization. A cell's ability to adhere to materials is of great importance for a device's ability to become compatible with existing procedures in the medical field. Without this knowledge, devices requiring cell screening could not move forward. MEMS force sensors have the ability to determine the strength of adhesion of individual cells, length of cell adhesion and mechanism of cell detachment. [14]

Reduction of device size is of continued interest. Reduction of actuator sizes, commonly found in automated systems in cars, condense systems to such a level that, one time, bulky measurement tools are now more accurate, light weight, often compact enough to fit into one's pocket. [15, 16] Electro-thermally and laterally driven polysilicon actuator devices act as micro tweezers as small voltages are applied, the 1 μm by 2 μm and 750 μm long device is able to apply a force of 2.8 μN. [15]

More involved than these devices are micro-motors. Today intricate magnetic micro-motors with excellent performance are reproducible and integrative as microactuators for future sensor applications. [16, 17] High speed rotation was demonstrated on the micron scale dating back to the late 50's. [18] These high speed motors are manufacturable and highly reliable thanks to LIGA. [17] LIGA,

X-ray lithography, electroforming and molding. The LIGA acronym is actually derived from the German form of X-ray Lithography, Electroforming and molding.

The LIGA system was first demonstrated in the United States at Sandia National Laboratories in California. LIGA is a joint endeavor by Sandia and private industry. LIGA fabrication combines deep x-ray lithography and electroplating, rapidly producing intricate devices. [19] The LIGA system produces x-ray's for lithography by use of a synchrotron, this allows for extremely small critical dimension. The x-ray lithography allows both polarities of resist to be utilized. Common electroplated materials used in LIGA are copper and nickel. [20, 17]

2.2 Photolithography

Photolithography involves spin-coating photoresist onto a substrate, followed by a pre-bake, subsequent wavelength-critical exposure, development, and post-bake (optional). After the initial spin, a pre-bake removes much of the solvent required to keep the photoresist in a liquid form (necessary for spin coating). All photoresist has a range of possible thicknesses. [21, 22] The speed at which the resist is spun on determines the final thickness. The pre-bake leaves behind approximately 5% of the original solvent. Ultraviolet (UV) (350 nm-450 nm) or deep UV (193 nm-248 nm) exposure of the resist through a mask follows next using either a mercury lamp or excimer laser light. Masks used to patterning the photoresist in the UV/deep UV range are typically chrome-plated quartz plates (although other mask types, like Mylar, are used also). The substrate is next submerged in developer, leaving either the negative or positive of the exposed pattern. Depending on the subsequent processes the resist has to stand up to, occasionally a post bake is required. Finally, the exposed pattern is developed and either the positive or negative of the exposed mask image remains depending on the type of photoresist used. [23, 24, 25, 26]

2.2.1 Photoresist Composition

Both polarities of optical resists, positive and negative, are composed of three components: a photoactive component (PAC), a resin and a solvent. How the resist components respond to radiation in the two separate polarities of photoresists is quite different. [26]

PAC, is the only component of photoresist that responds to light energy, encountered during exposure. The solvent and resin components remain unchanged throughout exposure. In ***positive* resists** the PAC photochemically decomposes into indene carboxylic acid (ICA). As more light energy is absorbed, more PAC converts to ICA, until all the underlying resist is converted to ICA. PAC positive optical resists (diazonaphthoquinones) are soluble in developer *but* dissolve slowly, their decomposed counterpart, ICA, is highly soluble in basic aqueous developers. In ***negative* resists** the PAC (bis-arylazide) is *soluble* in the organic solvent-based developer unless it has been irradiated. When exposed and developed, the PAC in negative resist forms nitrene, creating the cross linking between individual polymers.

Resin, in both resist polarities, dissolves rapidly in appropriate developers, even after experiencing suitable bake times and temperatures. Positive resists use novolac resin; negative resists use cyclized synthetic rubber resin. Resin gives the photoresist its "mechanical" properties: resistance to ion bombardment, resistance to chemical wet etches, and viscosity.

Solvent is designed to keep the photoresist in a liquid form until the resist is ready to be dispensed. Solvent in positive photoresist is propylene-glycol-monomethyl ether (PGME) or ethyl lactate or another similar compound is used. Negative resist is dissolved in an aromatic solvent to maintain a liquid form.

Positive developers are basic (pH $>$ 7) aqueous solutions dissolving the previously mentioned ICA. Negative developers are organic solvents, requiring a nitrogen

ambient to achieve best results. Positive developers are more environmentally and worker friendly. This makes positive resist attractive as public outcry for stricter environmental standards increases and employees demand safer working environments. Negative developers typically employ organic solvents toluene or xylene, both of which are known to cause birth defects.

2.2.2 Photoresist Type

Optical photoresists have two polarities: positive or negative. Polarity is also the most general way to categorize photoresist. Figure 2.1 shows photoresist already spun onto a substrate, with an aligned chrome mask, awaiting exposure. This photoresist could be either positive or negative photoresist. With both resist types we start with a clean substrate, spin coat the photoresist at the appropriate spin speed (to achieve required film thickness), then expose with the appropriate wavelength. After the development stage, either the positive or negative patterns take form as seen in Figures 2.2 and 2.3, respectively. With the *positive* resist, shown in Figure 2.2, the "positive" image forms leaving solid photoresist remaining in the *unexposed* regions. For the *negative* resist, shown in Figure 2.3, the opposite exposed image forms, leaving photoresist only in the *exposed* regions; hence the naming convention.

2.2.2.1 Negative PR

Negative photoresist was the more popular choice for photolithography until device dimensions became small enough to become distorted by resist swelling during the development stage. During the developing phase the exposed negative photoresist crosslinks and absorbs a small amount of the organic developer, causing the photoresist pattern to swell.

Negative photoresist has superior adhesion to substrates, higher photosensitivity and is less costly. Adhesion is key for obvious reasons; if your photoresist does

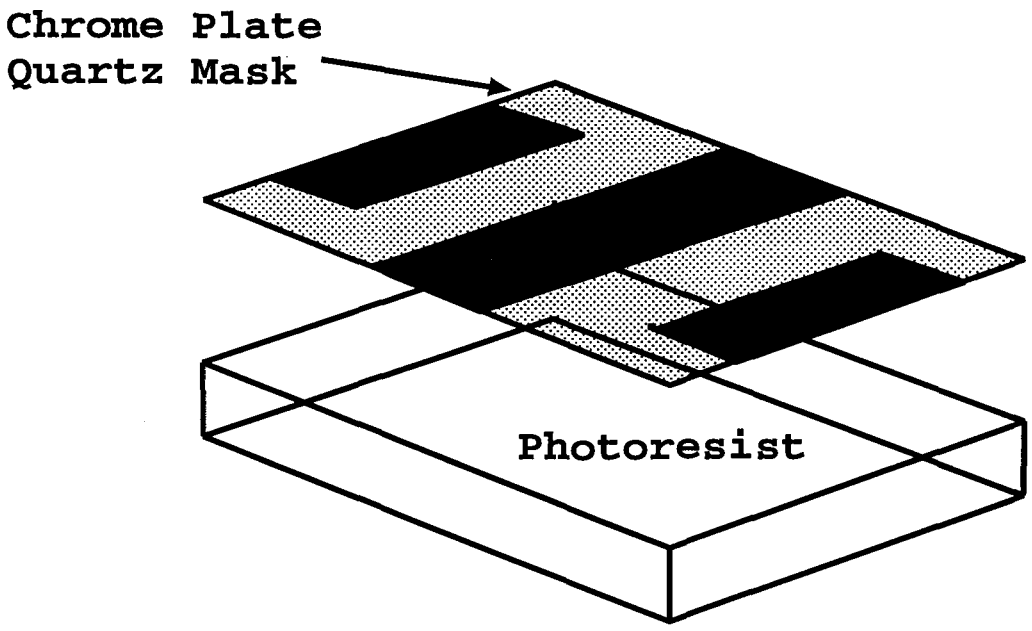

Figure 2.1: Chrome mask aligned above unexposed photoresist.

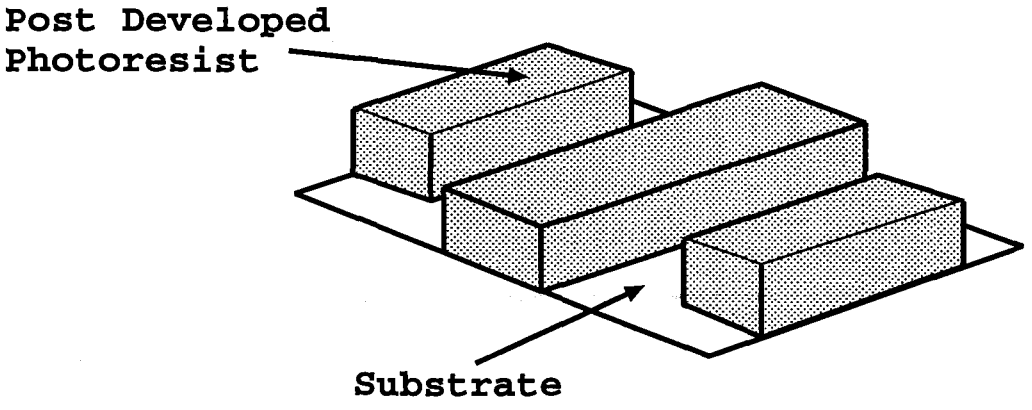

Figure 2.2: Post Developed Positive Photoresist Image of Figure 2.1, after exposure and developing.

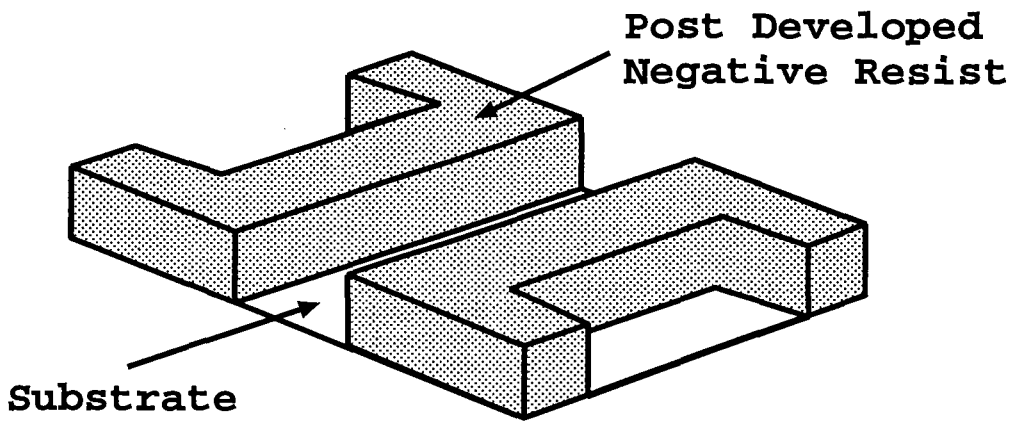

Figure 2.3: Post Developed Negative Photoresist Image of Figure 2.1, after exposure and developing.

not adhere properly to the substrate further, reproducible processing is doubtful. Positive resist often needs a costly pre-spin to promote adhesion. Since a pre-spin is omitted with negative resists, throughput is increased. Less energy is required to expose negative resists, reducing exposure times and improving throughput. Negative resists cost approximately a third the cost of positive resists.

Negative photoresist absorbs a portion of the solvent in the development stage, where crosslinking occurs. This absorbtion causes line width distortion for patterns less than 2 - 3 μm, depending on the application. With increasingly smaller critical dimensions the development of deep-ultraviolet (DUV) negative resist is bringing back negative resists. [27, 28] Combine lower cost with increased throughput, lower power consumption due to negative resist having higher photosensitivity, reduced process complexity and better adhesion, the usefulness of negative resists becomes clear when printed image quality is not severely compromised.

2.2.2.2 Positive PR

Positive photoresist was exclusively employed throughout industry by the late 90's and is still dominant due to its high resolution of small critical dimensions and the availability of relatively inexpensive i-Line (365 nm) and g-Line (436 nm) exposure sources. Positive photoresist is required when device critical dimensions fall below 2 - 3 μm. [29, 26] This is primarily due to positive resists ability to withstand swelling in the development stage.

As stated earlier, both, i-Line and g-Line photoresists are composed of three components: a novolac resin, a solvent, and a PAC. Novolac resin provides the photoresist mechanical properties: thickness (e.g. 1.2 μm thick or 7 μm thick common for SPR 220), adhesion, flexibility, and is largely responsible for determining how well the resist will stand up to subsequent processing steps (e.g. ion implantation or etching). Solvent maintains the resist in a liquid state prior to photoresist spin coating. Diazonaphthoquinone PAC, used in i-line (365 nm) and g-line (436 nm) positive resist, is the only component chemically modified when irradiated.

The PAC has two purposes (see Figure 2.4). First, it acts as an *inhibitor*. When unexposed PAC is introduced to developer, the PAC withstands the developer, dissolving at a relatively slow rate. Second, PAC acts as an *enhancer*. The radiated PAC chemically decomposes to ICA. This chemical decomposition of PAC to ICA allows accelerated removal of the exposed resist in developer because ICA is highly soluble in basic (pH $>$ 7) aqueous solutions.

Both exposed and unexposed areas in positive resist dissolve in a corresponding basic developer. General use resists have a dissolution rate ratio of exposed to unexposed resist of 100:1. Specialized resists have been manufactured to have dissolution ratio rates, exposed to unexposed, as good as 1000:1. With decreasing critical dimensions, PACs with a stronger resistance against dissolving are required.

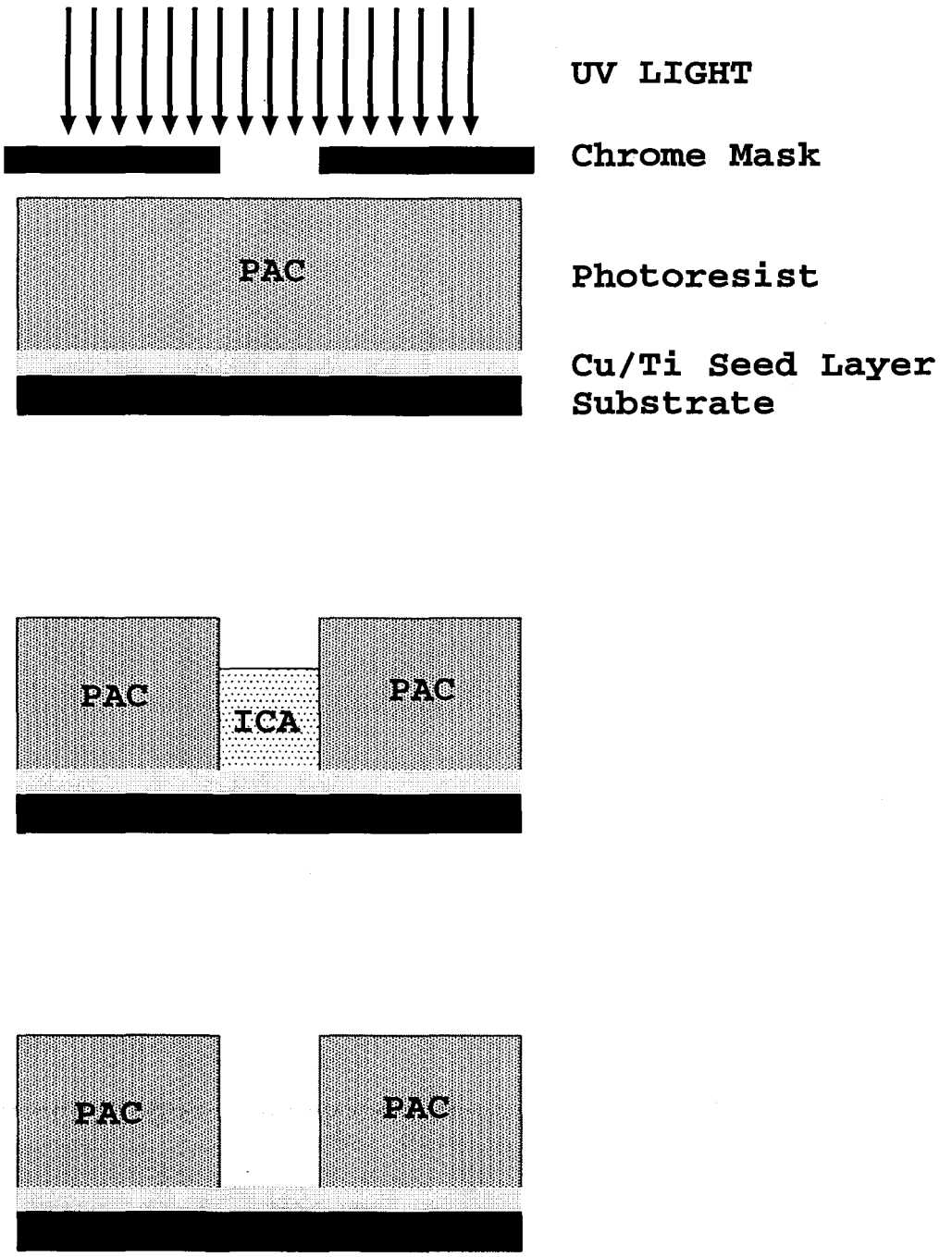

Figure 2.4: PAC to ICA conversion: During exposure, Development, and Post Development

Ion implantation, RIE, wet etching and electroplating also require thicker and/or more resistant resists. Current IC processing resists are typically 2 μm to 3 μm thick and need to withstand process steps (ion implantation, electroplating, etching) to protect underlying substrate regions.

After proper exposure, enough energy is absorbed to chemically decompose the PAC from the surface to the substrate into ICA. Once the pattern is exposed, it is developed, unless a post-bake is necessary. A post bake is used to drive out more solvent, helping to reduce standing wave patterns. Rate of pattern development and line width control is dictated primarily by developer concentration. The higher the concentration of developer, the faster ICA is removed. At first it may seem that faster development times are desirable due to increased throughput; however, the contrary is true. With the increased developer concentration the ICA rapidly dissolves but the PAC also dissolves more rapidly. Every resist and developer combination has a proper concentration of developer necessary to allow ICA dissolution to progress without detrimentally dissolving the PAC and causing unnecessary line width distortion.

Positive resists require corresponding developers, manufactured specifically for how the resist will most likely be used. General use positive resists, e.g. Shipley S1813, have concentrated developers requiring the process technician to dilute one part developer into three to five parts deionized water. The same resist will dissolve at different rates as developer concentration varies, yielding small variations in pattern thickness, sidewall angle among other details. To achieve best photolithography results environment and equipment set-up are considered. To determine the best operating conditions, sensitivity and contrast curves are needed. *Sensitivity* and *contrast* are important, descriptive features of optical photoresists. With knowledge of these features, excellent photoresist resolution can be achieved.

Sensitivity, in positive resist, is the amount of light energy required to change the PAC to ICA. Higher sensitivity of a resist allows for shorter exposure times, yielding higher throughput. Sensitivity, as defined by Wolf, "the input energy required to cause a specified degree of chemical response in the resist, which results (after development), in the desired resist pattern." [30, 26]

$$\Phi \equiv Sensitivity\ Response \tag{2.1}$$

$$\Phi \equiv \frac{(number\ of\ photons) - (induced\ events)}{number\ of\ photons\ absorbed} \tag{2.2}$$

Resists are designed to respond to a specifically designed range of wavelengths. Some resist have a narrow range of wavelengths they decompose at; other resist, like multi-purpose photoresist respond to more than one range of wavelengths allowing for more than one source to be used. Resist sensitivity varies with different wavelengths and is therefore dependant on both the light source and the light source-to-substrate spacing. Higher sensitivity is usually sought after. Two mercury light sources may require different exposure times due to spectral or intensity difference between the two sources.

Contrast (γ_p) (for positive photoresists) is in simplest terms this is the rate at which the appropriate resist decomposed or crosslinks, where γ is contrast. Higher contrast photoresists are most desirable. Resists with high γ result in the best resolution. Besides contrast aiding in resolution measurement, contrast can be used to calculate side wall angles and smallest printable feature size.

$$\gamma_p \equiv Contrast \tag{2.3}$$

$$\gamma_p \equiv \frac{1}{\log \frac{Dc}{Do}} \tag{2.4}$$

$$Dc \equiv Minimum\ Exposure\ Energy\ for\ 100\%\ Film\ Loss. \tag{2.5}$$

$$Do \equiv Maximum\ Exposure\ Energy\ for\ 0\%\ Film\ Loss. \tag{2.6}$$

Whether or not the contrast is good or poor depends on your process, only the process engineer can say if the contrast is good enough. However, as a general rule a higher number γ_p is desired, the closer to 1 the better. If Dc is far larger than Do, then a small contrast will result. Dc is the critical exposure dose required to completely remove the photoresist during development.

2.3 Electroplating

Electroplating (electrodeposition) is the process of producing a coating on a surface by electric current. When electroplating was first developed, direct current (DC) power supplies were utilized. Italian, Luigi V. Brugnatelli developed gold electroplating in 1805. Later in the 19th century copper plating was used extensively in Russia to plate religious statues. [31]

Electroplating is a reliable method of deposition. Devices requiring relatively thick films (on the order of microns), low temperature processing, large device areas, combined with uniform thickness require more effective deposition techniques than sputtering, evaporation, or chemical vapor deposition (CVD) and other high vacuum deposition techniques commonly used in the integrated circuit (IC) industry. Electroplating benefits include high throughput, simple, low temperature, non-vacuum

implementation and a wide range of possible deposition thicknesses: several hundred microns (10^{-6} m), or as thin as several hundred Angstroms (10^{-10} m), as device requirements dictate. [31]

In the past two decades, great attention has been paid to electroplating. [32] Although a wide variety of materials are deposited by electroplating, this section will focus entirely on copper electroplating used in the capture dot process (chapter 4). [33, 34] Copper is a low resistivity metal, highly prone to electromigration in silicon, an issue overcome by current IC manufacturers. [26] Electromigration is the movement of conducting atoms as a result of momentum transfer from current-carrying electrons. Printed circuit board and IC manufacturers have found that through-hole plating, deep trench filling and high-throughput interconnects for microprocessors can be effectively produced by electroplating. High-throughput manufacturing of electroplating allows for reduced device costs. An excellent source of information on copper electroplating can be found through Think and Tinker, Ltd.'s website: www.thinktink.com.

2.3.1 Electroplating Set-Up

Figure 2.5 shows a basic acid bath copper electroplating setup: copper acid bath, anode, cathode, and a direct current (DC) power supply. The anode and cathode are submerged in the plating bath solution, a small voltage difference is applied across them. The positive terminal of the DC supply is connected to the solid copper anode, allowing a continuous supply of Cu^{2+} ions. The negative terminal of the DC supply is connected to the cathode, supplying electrons. The cathode is the conducting part onto which electroplating occurs.

The copper anode is not required for electroplating to proceed; however, without it the acid bath becomes depleted of copper ions. To maintain bath properties,

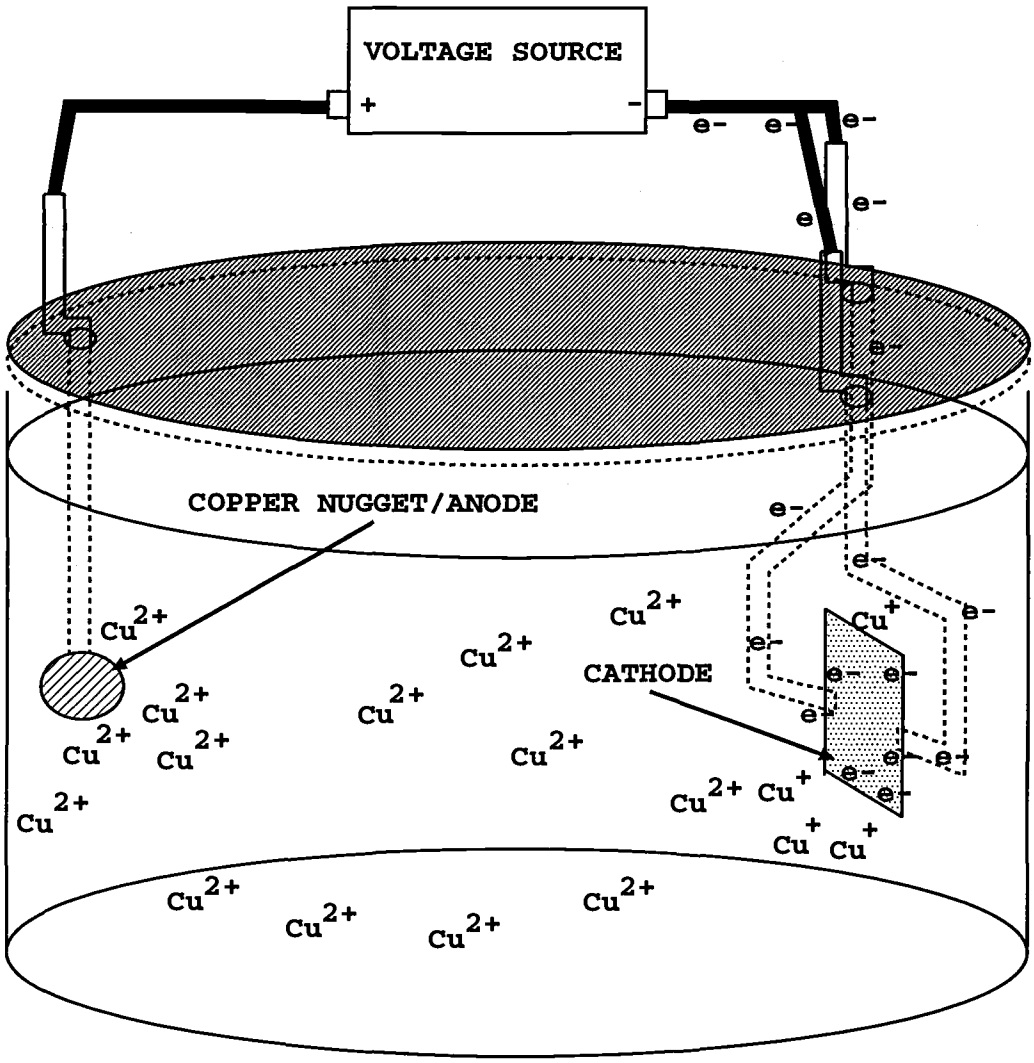

Figure 2.5: Basic Electroplating Set-Up

the copper anode, a copper nugget 99.5% copper with 0.5% phosphorous, should be viewed as a requirement. The anode provides a continual supply of copper to be oxidized during electroplating. Reduction of copper occurs at the cathode, resulting in plating out of copper on all parts of the conducting sample, exposed directly to the electroplating solution.

As knowledge of electroplating chemistry progresses, so does the technology used in current, modern systems. Modern acid bath electroplating systems contain a cathode, anode, power supply, air/nitrogen sparger, dam, and a plating solution with proper additives, in a container with carefully designed dimensions. Complex bath chemistry (additives) and complex pulse plating methods further the usefulness of electroplating.

2.3.2 Current Density

Current density (amperes per unit area) determines the deposition rate at the cathode. When the seed layer (a thin, conducting film) on the cathode is uniform in thickness, the current density will also be uniform across the substrate and uniform deposition is achieved. [35] However, more commonly, the current density varies across the cathode which in turn varies the rate of deposition across the substrate (cathode). Areas of the cathode with greater current density plate more quickly than areas of lower current density, as shown in Figure 2.6.

Anything that goes into the plating bath affects the current density. For example: cell design, anode-to-cathode spacing, and additives all play important roles in current density distribution. It has been established by the printed circuit board (PCB) industry that cell geometry design, anode-to-cathode surface area ratio, air/nitrogen sparging (gentle bath agitation to break up the potential at the cathode) and anode replacement affect current density the greatest as first order

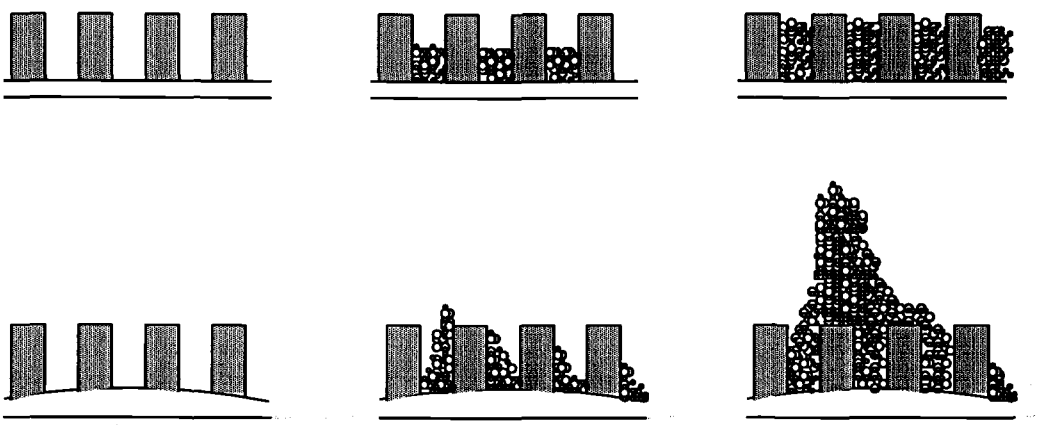

Figure 2.6: Effects of electroplating on a non-uniform seed layer.

effects. [36, 37] The acid bath chemistry (copper sulfate, sulfuric acid and chloride concentration) is a second order effect in current density. [38] Finally, additives are considered to play an even smaller role on effective current density, but even this third order effect requires great attention. Effects of current density distribution, relating to cell geometry and chemistry will be further investigated in Chapter 4.

Film quality is the final product and ultimately, if the quality is poor, changes need to be made to ensure a quality film. However, if film quality is poor, before going to costly thin-film analysis, like scanning electron microscopy (SEM), often examining how the cathode diffusion layer is affected by changes made to the electroplating system will yield valuable information even before electrodeposited films are made.

The cathode diffusion layer controls plating speed and uniformity, has low metal content, and is water rich. The cathode diffusion layer is a 10 μm to 200 μm thick region surrounding the cathode. The diffusion layer thickness is controlled by solution agitation, temperature, and metal concentration. With agitation or increased agitation the diffusion layer is decreased. As the diffusion layer decreases,

plating time is reduced. [39] Bath temperature affects several things, often the most obvious being the additives, since at higher temperature organic molecules can dissolve into smaller molecules. However, temperature also affects the convection-diffusion transport of ions (copper and chloride ions are used). [40] As the bulk (in solution) metal concentration decreases, the limiting current decreases, reducing cathode efficiency and slowing deposition rate. [41]

2.3.3 Plating Types

DC electroplating has been around since the early 1810's and has remained acceptable for a wide range of plating applications. However, in recent years pulsed and reverse-pulsed plating has become a necessity for even plating of surfaces with small and/or deep feature sizes. [42, 43, 44] In 1991 IBM published the first demonstration of dual-damascene processing for IC's. Since this time, the IC industry has invested great time and resources into investigating the benefits of pulse plating current schemes. When examining different current plating schemes, Faraday's Law, current efficiency, and the cathode diffusion layer are given greater attention to discover the most appropriate current for a given process.

Faraday's law is a way of counting electrons. 96,400 amp-seconds = 1 gm of electrons. [45] The Electrochemisty Encyclopedia describes Faraday's Law as: "(1) In any electrolytic process the amount of chemical change produced is proportional of the total amount of electrical charge passed through the cell. (2) The mass of the chemicals changed is proportional to the chemicals' equivalent weight. The proportionality constant being the Faraday Number." The Faraday Number gives the amount of electrical charge needed to change one gram-equivalent of substance by electrochemical reaction. [46]

Current efficiency is the ratio between the actual amount of metal deposited to that expected theoretically from Faraday's law. [46] The current determines the quantity or amount of copper plated. During copper electroplating the following processes occurs at the anode and cathode:

$$Anode : Cu \rightarrow Cu^{2+} + 2e^{-} \tag{2.7}$$

$$Cathode : Cu^{2+} + 2e^{-} \rightarrow Cu^{o} \tag{2.8}$$

Electroplating systems employ one of several types of plating current schemes like: direct current (DC), pulse plating (PP), periodic reverse (PR) or pulsed periodic reverse (PPR) (shown in Figure 2.7). The type of plating current used depends on the application and material being deposited. In PCB copper through-hole plating, pulsed periodic reverse plating has had the greatest success for adequate filling of through holes. For damascene or dual-damascene structures, pulse plating is best for patterns with a seed layer while DC plating is best for non-critical plating. [47, 45]

2.3.3.1 Direct Current Plating

DC, direct current, plating has been used since electroplating was first developed. In DC plating the applied voltage remains constant throughout the plating process. In copper sulfate baths where additives are utilized, the current density (approximately 20 amps per square foot (ASF)) should remain low for optimal (uniformly thick, low stress, low porosity) film characteristics.

Initially, current density starts out high and consequently, the plating deposition rate also starts out high. However, as plating progresses, the total area of the

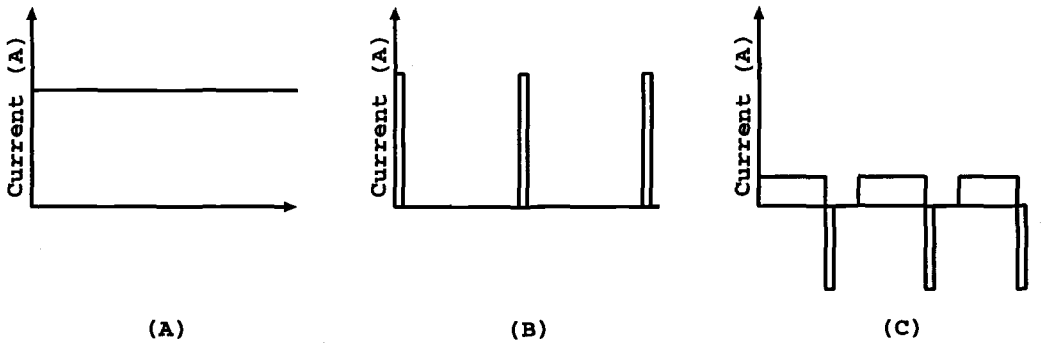

Figure 2.7: Plating Current Schemes: (A) Direct Current (DC), (B) Periodic Pulse (PP), (C) Periodic Pulse Reverse (PPR). All plots are current versus time.

cathode metal layer increases, decreasing the overall resistance, as shown below in equation 2.9. This decrease in resistance drives the current up (equation 2.10).

$$R \equiv \rho(L/A) \tag{2.9}$$

$$I \equiv V/R \equiv V/[\rho(L/A)] \tag{2.10}$$

R = resistance (cathode resistance), copper $\rho = 1.77(10^{-8}$ ohm*meter), L = length (total length of coils), A = area (cross-sectional area of coil trace), I = current, V = voltage (applied cathode-to-anode voltage)

With higher current, higher current density is seen in areas of low resistance and areas with high electric field like corners and edges. Any non-uniformity in the seed layer will experience an avalanche effect: sections with the least resistance and highest electric fields have greater deposition rates. This causes even larger electric fields which causes plating to occur more and more rapidly at that section of high

electric field intensity. These areas, plating at a rapid rate, monopolize the reduced number of cupric ions in the diffusion layer, not allowing nearby areas to plate. The result is large dendrites (overplating growth) of copper surrounded by largely unplated sections. Nonuniform plating in DC plating can be reduced by the use of levellers (suppressors), an organic that suppresses currents. However, even levellers can not be expected to give uniform deposits with sub-micron patterns or with high aspect ratios. [45]

2.3.3.2 Pulse Plating

This section looks closely at pulse plating and periodic reverse plating, shown in Figure 2.7. [48, 49] The positive sections of the pulse are cathodic amp minutes, the negative pulses are anodic pulses. To plate, the cathode receives more cathodic amp minutes than anodic amp minutes; otherwise, the underlying copper seed layer will be removed.

During pulse electroplating deposition, crystal formation greatly depends on two processes: the rate of nucleation and grain growth. [50] During electroplating higher nucleation rate and slow grain growth are desirable for finer grained structures. With finer grain structure the copper has a lower porosity, higher tensile strength, higher elongation, and reduced stress.

The duty cycle of the pulse is the *on* time (t_{on}) divided by the *on* plus *off* time (t_{off}). It is recommended that for seed layer plating, the duty cycle be close to 10%. [20] To reduce grain size, reduce the duty cycle; lower duty cycle has finer grains. However, copper can recrystalize into larger grains if the duty cycle drops below 10%. Grain size control is important: tensile strength is inversely proportional to the square root of the grain size. Typically, elongation is inversely proportional to grain size. Small grains pack together better and reduce porosity and stress. [45, 31]

Nucleation, the initial stage in a phase transformation, is increased with increased current density. [51] Pulsing increases the probability of new grains forming. More new grains form at high current density. This high current density increases concentration of adatoms (electrodeposited copper atoms) on the surface and leads to more nucleation sites.

In pulse plating deposition, control of t_{on} and t_{off} yields control over pulse length, forward current, reverse current, time between pulses, peak current and average current. By varying these parameters, the cathodic overpotential (the deviation of an electrode potential from its equilibrium value required to produce a net flow of current across an electrode/solution interface) is controlled.

With cathodic overpotential control, the nucleation rate and activation energy of nucleation is controlled. High cathodic overpotential yields a low activation energy, increasing nuclei formation. The peak current and pulse length establish the number of ions discharged into the plating bath during a pulse. Higher deposition rates deplete the ion concentration near the cathode, so slower deposition rates are more desirable for smooth, uniform electrodepositions.

The time between pulses controls the repetition rate but this also determines the time for the Cu^{2+} ions to migrate toward the electrode (cathode). Cu^{2+} ions are continually introduced into the electroplating bath from the anode, the copper nugget.

2.3.4 Electroplating Bath Properties

There are three common types of electroplating baths: cyanide, pyrophosphate, and acidic. [50] Acid baths and cyanide baths are the two plating bath types found most frequently in industry. Low cost, low toxicity and high deposition rates

make acidic baths the most widely implemented copper electroplating bath. This section reviews the electroplating acid baths.

2.3.4.1 Plating Solution

In all copper electroplating solutions copper ions are available to be deposited. Typical acidic solutions contain copper sulfate, sulfuric acid and deionized water. [26, 50]

In an acid bath the following reactions take place:

$$CuSO_4(s) + H_2SO_4(aq) + 2H_2O(l) \rightarrow Cu^{2+}(aq) + 2SO4^{2-}(aq) + 2H_3O^+(aq) \tag{2.11}$$

$$Cu^{2+} + e^- \rightarrow Cu^+ \tag{2.12}$$

$$Cu^+ + e^- \rightarrow Cu^0 \tag{2.13}$$

$$2Cu^+ \rightarrow Cu^{2+} + Cu^0 \quad (competing\ reaction) \tag{2.14}$$

When a voltage is applied between the anode and cathode, an electric field is established. The field lines begin at the positive charge, which is the anode, and end at the negative charge at the cathode. The Cu^{2+} ions (where the electric field starts) in the bath are attracted to the cathode (where the electric field ends). The Cu^{2+} ions are reduced by a single electron to a Cu^+ ion (Equation 2.12). Two reactions can occur to this Cu^+ ion. It can be reduced again to elemental copper (Equation

2.13) by another electron from the cathode and adhere to the cathode. This is the desired reaction. Otherwise, two Cu^{+} ions can combine to form elemental copper and the more favorable oxidation state, Cu^{2+}, this being the less desirable reaction.

2.3.4.2 Bath Dimensions

Proper spacing and positioning between anode and cathode is critical in copper electroplating. There are also minimum dimensions that are crucial for repeatable, manufacturable electroplating. The overall size of the plating bath depends on what tools are needed in the plating bath.

Common to plating designs are: air/N2 sparger (supplying many small bubbles to break up potential at cathode surface), heating elements (to maintain bath temperature), dams (to direct ion flow to cathode), and often multiple anodes and cathodes. In general, plating baths should be no less than 10 inches wide. After the substrate (i.e. cathode) is submerged into the final position, the substrate should be four inches from the bottom of the plating cell, have at least 1.5 inches of clearance on either side and should remain three inches away from other substrates if multiple substrates are plated simultaneously.

2.3.4.3 Organic Additives

The most popular copper electroplating solution, the acid bath, is utilized for a variety of uses, from electroforming, to PCBs, to delicate interconnects on ICs. Surprisingly, acid bath electroplating chemistry changes little for this wide range of applications. However, much attention is granted to the small amounts of organic additives. [52, 53] Critical in electroplating are additive type and size. [37, 54] There are three possible organic additives: Levelers (brighteners), suppressors (carrier), accelerators, and one inorganic additive: chloride ion. [45]

Levelers and suppressors slow down the electroplating by decreasing the current density. Levelers slow down plating by replacing accelerators as trenches are filled. Suppressors reduce current density at areas of unlevel copper deposition, where overplating has occurred. Accelerators increase current density; therefore, accelerating electroplating. Where accelerators accumulate, for example at the bottom of trenches or lithography patterns, absorption occurs, increasing current density and plating rate.

The amount of accelerator molecules needed varies greatly with the plating requirements. When through-hole plating, the bath will have an increased level of accelerators, allowing more even plating in the holes by increasing the current density and distributing the potential more evenly throughout the hole. Superfilling (filling of deep/narrow dimensions) also requires more accelerator molecules present. [55] Accelerators are most likely consumed by film incorporation. However, since superfilling is a recent requirement by IC manufacturers, it may be years before it will be known whether the accelerators are consumed by film incorporation or a chemical reaction on going in trenches, due to proprietary processes being highly guarded by industry.

Levelers and suppressors are relatively large organic molecules/polymers that slow the plating process, breaking up areas of high potential. This is useful because there are always small differences in the local resistance of the seed layer, changing the potential at different points on the electroplated seed layer. The areas of higher potential have high current density and as a result plate thicker and faster which can be disastrous, ruining the electroplated layer and the fabricated device. Brighteners are smaller molecules that accelerate plating in through-holes on PCB boards or in deep trenches. When balanced properly, levelers and brighteners allow nanostructures to be plated successfully. However, it is not just a matter of finding

the right amount and size of organic additives that make an electroplating solution successful.

The organic additives' size and structure vary with the pH of the electroplating bath. [51] For example an organic additive, Zolotukhim, is a positive ion in an acid bath, has one negative charge when the bath is neutral, and has two negative charges in an alkaline bath, making the bath appear dark blue. The organic size relates closely to the grain size as plating occurs. Higher bath temperatures also cause variations in the organic size. Organics have an increased dissociation with higher temperatures, increasing Cu^{2+} concentration. This increased Cu^{2+} level reduces the cathodic overpotential forming larger grains. Once the electroplating bath solution, pH, temperature, and pulse parameters are chosen, the plating bath should never have to be replaced if taken care of properly. [56]

Great care in organic monitoring is critical for proper electroplating. [57, 58] As mentioned earlier in this section, superfilling technology depends on the organic additives levelers and accelerators. However, accelerators are consumed or decompose over short periods of time. SPS, an accelerator additive often used in superfilling plating baths, decomposes in 12 hours into smaller organics that impede plating. [53]

An array of organic molecules are used as additives in electroplating: carboxylic acid, tartaric acid, citric acid, malonic acid, and hydroxide groups. Organics specific to sub-micron trench filling issues for high aspect ratios, with seed layers of PVD copper, have been investigated in recent years with much success. [59, 60, 11] Chemists have identified multiple accelerator/suppressor/leveler specific combinations that have been successfully demonstrated. [52]

Employees at Dynatronix have shown that plating utilizing periodic reverse pulse plating (see Figure 2.7 c) without additives can be as effective as DC plating

with organic additives. [61] They operate square wave pulses at 1 MHz or higher to take the place of the additives that allow for a high throw power. Plating is done at 100 to 120 ASF. It is beneficial to plate without additives since additives are costly and waste removal is more simple.

3. DEPOSITION, PROCESS AND CHARACTERIZATION TOOLS

This section covers the processing equipment utilized to create the capture dots and transparent thin-film heaters. A general overview is given of the process tools and the specific models used are covered. These process tools are used during typical micro-electro-mechanical-systems (MEMS) and microtechnology-energy and chemical-systems (MECS) development.

The high vacuum systems have two pumps. The first pump (mechanical pump) takes the process chamber from atmosphere to low vacuum pressures. The second pump (diffusion pump) takes the process chamber from low vacuum pressures to high vacuum pressures. The diffusion pump input must see pressures in low vacuum ranges to operate; therefore, after the mechanical pump takes the process chamber from atmosphere to low vacuum pressures the mechanical pump(s) back the diffusion pump(s) to maintain the process chamber at high vacuum levels.

3.1 Process Equipment Measurement Tools

This section discusses the measurement tools used in many vacuum systems. All the vacuum equipment used at Oregon State University use one of all of these tools. The usefulness and limitations are explored to allow the reader to better understand the process equipment and procedure used.

3.1.1 Thermocouple Gauge

Thermocouple (TC) gauges are useful for measuring low pressure ranges seen in the process chamber when the mechanical fore pump(s) take the process chamber from atmospheric pressure (760 Torr) to lower pressure. Thermocouple gauges have

the ability to give a reasonable measurement of the pressure, in the 10-10^{-3} torr range. The thermocouple gauge gives an accurate reading within 10% of the actual pressure. This accuracy is only valid for the specific gas for which the gauge was calibrated for (usually N_2). The gauge works by measuring the temperature change of a thin tungsten filament with a thermocouple. As pressure decreases, the filament temperature rises due to thermal conductivity of the gas decreasing with decreasing pressure. The TC gauge is a simple, accurate and effective gauge. [26]

3.1.2 Ionization Gauge

The Bayard-Alpert ionization gauge, more commonly called an "ion gauge", can measure pressure from 10^{-3} to 10^{-8} torr. The more user friendly model of the ion gauge uses a single thoriated tungsten filament. Thoriated tungsten has a lower work function than non-thoriated and can withstand failure when brought to atmosphere from low pressures. When vacuum equipment is not completely automated, often the ion gauge status (on/off) is regulated and monitored by the tool user. The thoriated filament is more forgiving to forgetful process tool users. An ionization gauge costs approximately $100 U.S. dollars.

3.1.3 Crystal Monitor

Many of the vacuum deposition equipment systems are outfitted with a crystal monitor to monitor the deposition rate of the material. The crystal monitor utilizes a thin, flat, half inch diameter thin-film gold deposited on quartz crystal oscillating at 5 MHz in a stainless steel holder. Using the density and impedance of the evaporated material, the monitor system calculates the deposition thickness from the change in the crystal oscillator frequency with mass of material deposited onto the crystal face. Crystal monitors common in evaporation and sputter deposition system are

best suited for metal depositions, although they can be used for semiconducting and insulating materials, also. Film deposition rates are measured as the thickness of material deposited in an area per second, (Å/(cm^2*s)).

3.2 Evaporation

In evaporation, a thin-film deposition method, a crucible holder containing the material to be deposited is slowly heated, under mid or high vacuum conditions, until a controlled rate of the material deposited on the crystal and subsequently the substrate is achieved, see Figure 3.1. The deposition rate of the material is monitored by a crystal monitor (section 3.1.3). Evaporation is a point source deposition method. Point source deposition is a deposition that originates from a single source, radiating out, similar to a light bulb. As the crucible is heated, the material melts or sublimes (subliming is where the atoms of the material come directly from the material as a solid, without first melting), then adhere to the substrate.

Evaporation is a line-of-sight process. The evaporated material atoms adhere to the first item that interrupt the evaporated atoms path. We desire the substrate to be the end of the path, but at higher pressures more particles are present in the evacuated chamber, if the atom contact these particles the evaporated atoms will either not make it to the substrate or will incorporate some of these particles as they deposit on the substrate as a thin-film. Contaminates in deposited films and increased particle count come from: impurities in the evaporated source material, the source crucible, background gases and/or particles from previous evaporations. As more particles are evacuated the pressure reduces. The lower the pressure, the less evaporated material will be lost to particle collisions. This can also be explained in terms of the "mean free path".

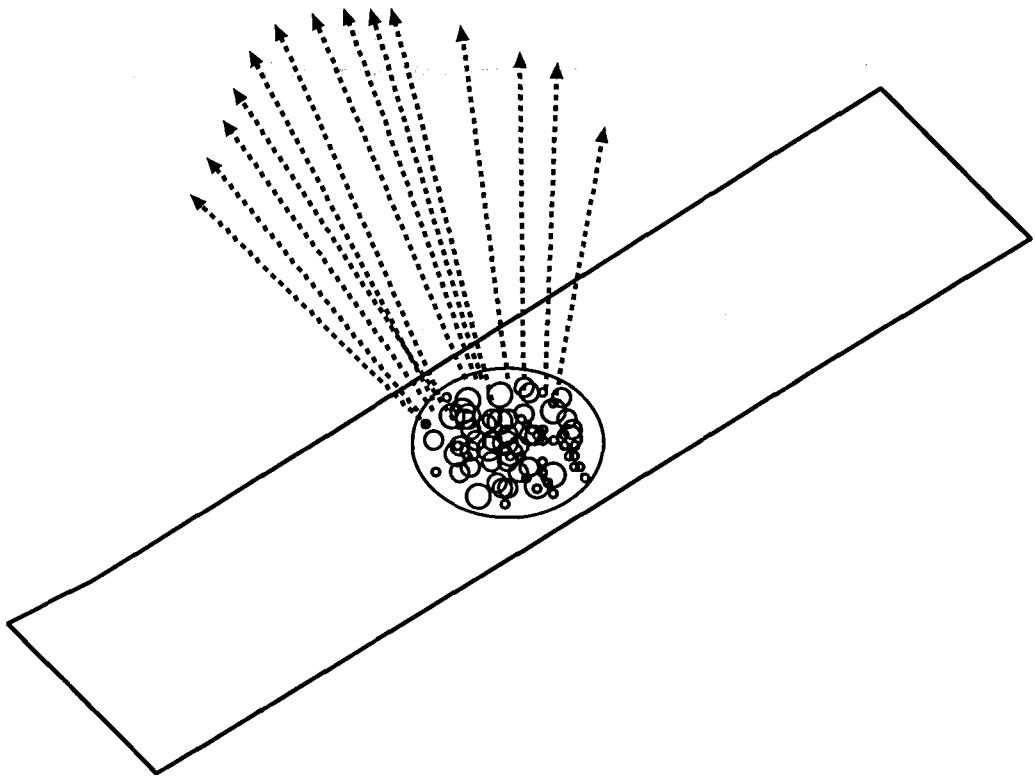

Figure 3.1: Crucible holder with heated material depositing non-uniformly as a Cosine distribution.

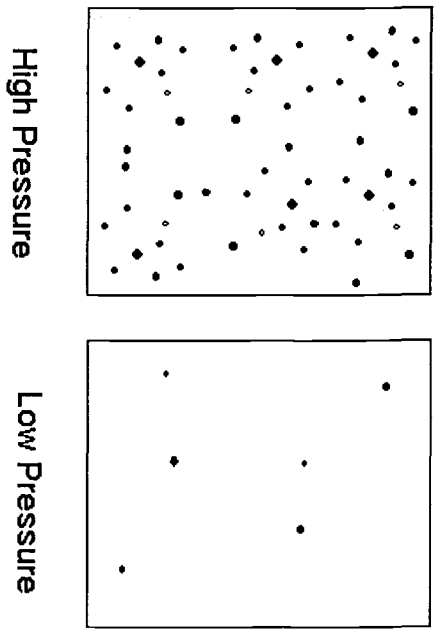

Figure 3.2: Two boxes representing high and low pressure. As particles are evacuated through the pumps, the pressure lowers and the mean free path increase.

The evaporated material has a longer mean free path length at lower pressures. The mean free path is a measure of how far (distance from material origin to collision) the atoms will travel before they collide with another particle, see Figure 3.2. The lower the pressure, the longer the mean free path and hence the fewer particles are present. Evaporation takes place in the mid-pressure range, 10^{-6} torr, or lower.

Evaporated metals deposit as individual atoms or groups of atoms. NiCr (an alloy of 80% Ni, 20% Cr) atoms, like other alloys, are less tightly bound than pure metals or metal oxides. The nickel and chrome tend to evaporate almost completely independent of each other. These metals enter the vapor phase acting like "pure" metals, making evaporation less ideal for alloys than other vacuum deposition methods. Another limitation of evaporation is its has poor step coverage due to the line-of-site deposition. Poor step coverage is usually undesirable; however, is a necessity for lift-off.

At Oregon State University the Veeco evaporator system has a diffusion pump backed by a mechanical pump. The evaporation chamber is brought down from atmosphere (760 torr) to the mTorr range with the mechanical pump. The diffusion pump (backed by the mechanical pump) brings the chamber down from the mTorr range to the low μTorr range. Once the process chamber falls into low to mid-μTorr range, the boat or crucible holding the material is heated and thermal evaporation is achieved. The pressures are monitored by a thermocouple and ionization gauge. Thin film deposition rates are monitored by a crystal monitor.

3.3 Electroplating

This section explores the electroplating set-up for copper electrodeposition, specific to the capture dot manufacturing (a more general discussion of electroplat-

ing can be found in section 2.3). Electroplating is a powerful deposition technique, providing excellent, uniform coverage to areas with large deposit area, concomitantly providing high quality films with high throughput. Many metals, alloys and transparent conductive oxides (TCO's) are deposited by electro- or electroless- plating. However, only copper electrodeposition will be detailed here.

3.3.1 Electroplating Set-Up

The plating set-up here follows the same requirements specified in chapter two. The largest print size of the capture dot photolithography layers is approximately 1 inch by 1.25 inches. A nine inch round (2.2 liter volume) Tupperware polyethylene container houses our electroplating solution, with proper anode/cathode placement. To remove undesired organics, the tupperware container is leached in 10% sulfuric acid solution, for more than two hours prior to use. Leaching is an acid soak: 10% sulfuric acid, 90% de-ionized water. [As with diluting all acids, add the acid to the water, NOT the other way around.]

To promote globally uniform depositions, a bubbler (interchangeable with a N_2 sparger) and dam are included in the deposition design. Global uniformity, i.e. long range uniformity, is a measure of how uniform the deposition is across the entire substrate. The bubbler is a $\frac{1}{4}$" PVC tube. At half inch intervals $\frac{1}{8}$ holes are drilled through the PVC tube, the end of the tube is capped. This PVC tube is submerged in the electroplating solution after leaching. The PVC tube runs one inch from the bottom of the tupperware container, out of the plating bath to a small fish tank aeration pump. The small fish tank aeration pump provides gentle air agitation. Air agitation, during plating, breaks up areas of high potential in front of the cathode, improving uniformity across the entire wafer area. The dam (Figure 3.3) has a two inch circular hole cut through it, centered between the cathode and

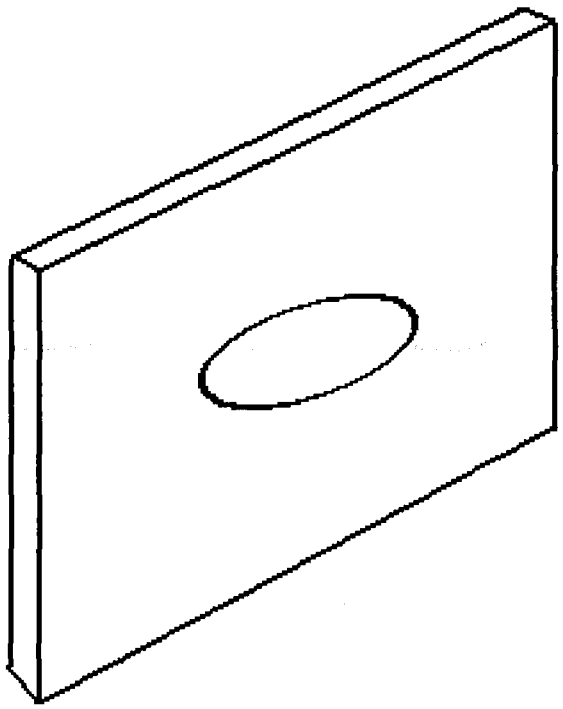

Figure 3.3: Dam, separating anode and cathode. The hole in the dam acts as a way of controlling the flow of ions.

anode, to provide a more directional flow for the cupric ions to flow through from the anode to the cathode.

All items which will contact the electroplating solution are leached for a minimum of four hours to reduce contamination. Once a successful electroplating solution has been developed, great care must be taken to ensure the electroplating solution is not compromised by foreign organics. As a final preventative measure to reduce foreign organics, an hour long pre-plating is completed to remove any particles that may have been introduced into the plating solution during development. If the electroplating bath has sat for any considerable length of time, sludge

particles from the anode will enter the plating solution and pre-plating is needed to remove this. The great caution to reduce foreign organics will become clearer as the importance of organic additives is explored.

Foreign organics ruin electroplating baths and degrade film quality by introducing undesired particles into the depositing film and produce less ideal films; therefore steps are taken to remove particles before they enter the plating solution, such as leaching. Photoresist, an organic material, is often a culprit for introducing foreign organics into the electroplating bath. To reduce the chance of the photoresist organic polymer from becoming incorporated into the electroplating bath, the patterned photoresist is put back underneath the UV lamp and re-exposed the original time it was exposed prior to developing. If re-exposing films is not desired, re-baking an additional minute or so will yield a similar result. The extra exposure or bake makes more solvent drive out of the patterned photoresist, reducing the probability of organics inadvertently becoming incorporated to the plating solution.

3.3.2 Electroplating Solution

A general purpose acid bath solution (see Table 1) is used in combination with an organic additive solution developed for MEMS circuits, similar to the capture dots. Lea Ronal, an organic additive with two classes of organics, levelers (also referred to as brighteners) and carriers, is used to control film growth. During plating, the recommended resistance, $R = \frac{V}{I}$, should remain between 0.015 and 0.025 ohms during operation. For pulse plating the average current and voltage are used. Our present acid bath solution has a resistance of approximately 140 ohms. The high resistance measured could be due a number of reasons; however, the method of measuring the electroplating bath was probably not accurate. To decrease the resistance the current density must increase. We maintain a low voltage, since we

are plating onto a seed layer, burning the seed layer becomes more of a problem as the voltage is increased.

There are many ways to increase the current density. Additional organic additives can increase the current density; so can the inorganic additive. Chlorine (the inorganic additive), is necessary for high current densities since it aids in reducing the dendrite (tree-like) deposits. Decreasing the copper sulfate concentration decreases the resistance. More importantly as the sulfuric acid concentration increases a dramatic decrease in the resistance is witnessed. Had it been easy to change solution, increasing the sulfuric acid concentration and organic additives would have been investigated.

To determine the optimum plating time and current, we can use the follow equations. Acid baths employing Lea Ronal plate 28 μm of copper an hour, at 20 ASF.

Electroplating time, t, assumes 5 μm thick plated coils.

$$t = [5\mu m/(28\mu m/hr)]*60 \text{ min./hr.} = 10.71 \text{ minutes}$$

Plating current depends on the area of the device. It is reasonable to estimate the capture dot area by their pad areas:

$$\text{Area} = \text{Length} * \text{Width} = 8e^{-6} \text{ m}^2$$

There are 18 coil-pad combinations, for a total area of:

$$\text{Total Area} = 18 * 8e^{-6} \text{ m}^2 = 0.000144 \text{ m}^2$$

Plating occurs at 20 ASF, amps per foot. Totally area is converted to inches and current calculated:

$$\frac{20A}{144in^2} * \frac{0.2232in}{1} = 0.031 \text{ A}^2 = \text{Current}$$

Chemical	DI H_2O	Copper Sulfate Crystals $CuSO_4$ $5H_2O$	H_2SO_4 98%	H_2SO_4 35%	HCl 35%	Lea Ronal Copper Gleam PCM+
Volume	Liters	Grams	Liters	Liters	ml	ml
100 Liters	70.9	7500	—	28.6	16.6	500
2 Liters	1.786	150	0.204	—	0.332	10

Table 3.1: Basic Copper Electroplating Solution.

3.3.3 Plating Void of Additives

Through out the development of the electroplating system, at Oregon State University, effects on deposited film uniformity have been examined using acid baths without organic additives. In the early stages of process development a DC supply without organic additives would not allow for even plating. Dendrite (striated deposited) areas of severe overgrowth, of copper were electroplated as thick as 73 microns, leaving areas on the cathode substrate with coils left unplated. The best copper electro-deposited films (using the aforementioned bath without the additives) are so non-uniform passivation is unachievable. These severely non-uniform films are due to non-uniform current density (from a non-uniform seed layer) balanced only with the inorganic Chloride additive. Areas of higher current density attract the cupric ions, deposition occurs in these areas of high current density, furthering the imbalance because these areas with thicker layers of copper have increased current density, therefore attracting more cupric ions and increasing deposition in these areas exclusively.

Far more successful results are seen when electroplating in pulsed or periodic pulse plating modes. It is well known that with periodic pulse plating, sections that plate up faster and therefore thicker due to a non-uniform current density are un-plated, removed, during the negative (anodic) part of the pulse wave form. Pulse plating yields improved local planar films, allowing high quality films to be achieved by reducing grain size (allowing lower porosity, higher tensile strength, high elongation, reduced stress) and reduces hydrogen embittelment. [45]

Plating was done at higher current density. Current density was increased from 20 ASF up to 100 to 120 ASF and pulse plating was utilized. The higher current density combined with pulse plating, produced the most uniform films, but the films were dull and not as uniform as the electroplating bath with the Lea Ronal

and Chloride additives. By combining pulse and pulse reverse current it has been reported in literature that deposits have been produced without additives that are comparable to films with additives. [62]

3.3.4 Plating Uniformity

Uniformity in electroplating is a measure of how evenly thick the piece plated up is. Electrodeposited film quality uniformity can be measured with a number of different methods. Field-emission scanning electron microscopy (FESEM) and transmission electron microscopy (TEM) are common methods to measure electrodeposition thicknesses. [63] XRD examines other properties of interest: grain size, microstress, grain size distribution. At OSU the most reliable way to measure surface uniformity is with an alpha-step 500 profilometer. The alpha-step 500 can measure film thickness accurately to within one angstrom under ideal lab conditions. Due to the exhaust plumbing for the vacuum equipment being close to the profilometer system, the accuracy is closer to 5 angstroms.

Uniformity of the electroplated copper film was of most interest because without uniform coils, complete passivation of the electroplated structure is not possible. Without passivation the multiple electroplated layers used in the capture dot fabrication will have a path (electrically) to each other, shorting the device and rendering it useless. Although grainsize, its distribution and microstress were of interest, XRD was not available. With an optical microscope, viewing the electroplated film surface revealed other details: relative surface grain size, surface quality (dull or shiny films). To achieve highly uniform electroplated copper structures, uniformity in the seed layer was needed. Based on common knowledge of deposition methods, sputtering the seed layers was chosen over an evaporated seed layer (see Chapter 4 for more discussion on electroplating on evaporated vs. sputtered seed layers)

3.3.5 Direct Current (DC) Plating

DC copper electroplating was used first. Three different forms of DC electroplating were investigated. First, DC electroplating with no additives at 20 ASF. Second, DC electroplating with Chloride (the inorganic additive) at 20 ASF. Third, DC electroplating with LeaRonal (organic additive) and Chloride (inorganic additive). It should be noted that higher current density was not investigated because it is well known that with the high resistance of the seed layer, higher current will require higher voltages, and these higher voltages will burn the seed layer off.

The first DC electroplating system looked at a sulfate bath without a dam, without air agitation, without any additives. All of the films had such severe over-plating that none of the eighteen possible coils had any hope of passivation. In most cases the over-plating left most of the seed layer unplated and an overplated area between 50 - 100 μm high (recall the critical dimension is 10 μm).

After these poor results, a dam, (a blocker with 2 inch hole) and chloride (inorganic additive) were added to the electroplating solution/system. The resulting films still experienced over plating; however, not as extreme as seen previously. The films on average showed at least some plating across the entire film surface and the over plating was reduced to 20 - 30 μm. These films were not uniform enough to passivate but gave hope that, with bath agitation and additives, quality films using DC plating were possible.

The addition of the organic additive and air agitation helped to reduce the amount of over plating. However, overall the film quality was to still to poor to passivate successfully. There was an overall trend of traces and the contact pads to be thinner on one side, increase gradually in thickness across the pad to the thickest area. The films with the additives gave brighter films, this due to the leveller additive.

The overall trend of increasing thicker films is not surprising. The DC plating is constantly building up a copper film wherever the largest potential is. The agitation will break up this potential, but cannot redistribute the potential to areas of lower potential. Also the leveller and suppressors will indeed slow plating; however, again they can redistribute the potential and therefore areas of high potential will have thicker deposits.

3.3.6 Forward Pulse Plating

Forward pulse plating uses short cathodic current pulses followed by an off time. [45] When plating with seed layers, the resistance of the seed layer should be higher than the solution resistance. This was the case for the capture dots. Pulse plating allows for higher current density, giving more new grain nucleation and reducing the duty cycle control forces smaller grain size (grain size is proportional to duty cycle).

Square waves change quickly from anodic to cathodic, improving film quality by increasing the uniformity of the deposited copper. Square waves get to the maximum voltage and current quickly, minimizing reactions that can take place at lower voltages, long on and short off times eliminate effects of charging and discharging double layer, short on and long off times maximize effects from charging double layer. Using lower duty cycle pulses, high frequency pulse plating on seed layers gives better uniformity.

Forward pulse plating is best for applications with seed layers. Two different recipes using pulse plating were examined to see which one would yield the best results: first, the complete electroplating system with both organic and inorganic additives for a current density of 20 ASF; second, the same electroplating system and bath without any additive and a current density of 120 ASF.

The pulse plating with additives gave shiny, locally and globally uniform films. The local uniformity was so good that no over-plating or areas of higher plating were seen. Global uniformity was also excellent. From one corner to another on the 1 inch by 1.25 inch electroplated area no more than $\pm$ 1 μm change could be seen. This global uniformity improved when the cathode and air mixer were aligned better.

Pulse plating without additives at higher current densities gave inconsistent results. Films with good uniformity, globally and locally were achieved; however, often poor global uniformity was also seen. This is attributed to placement of the contacts on the sides of the substrate. The contacts on the cathode were placed in approximately the same relative position. Also the films required a longer overall plating time to achieve the same film thickness, this could be do more dense films being deposited or to long of an of off time. Finally, the tended to be slightly more dull than pulse plating with additives. With more exact placement of contacts to the cathode or if the contacts ran along the entire side of the cathodes, then pulse plating without additives would be more easily optimized. Until those upgrades to the electroplating system are integrated the more controllable organic electroplating is more reproducible.

3.3.7 Periodic Reverse

Periodic reverse plating was examined with the same two bath conditions: first, the completed electroplating system with both organic and inorganic additives and a current density of 20 ASF; second, the same electroplating system and bath without any additive with a current density of 120 ASF.

The lower current density (with additive) electrodeposited films had poorer local uniformity than the forward pulse films, but the films were shiny (although not as bright as the forward pulse). The global uniformity was comparable to the

forward pulse recipe. These films were also more reliably uniform, allowing for some error in the cathode placement.

The higher current density films produced dull films. The surface of the films looks like larger grain sizes are forming. This is opposite to what is expected. Higher current density yields a larger number of nucleation sites. It could be that the square pulse is losing its "square" shape with the the quick on-to-reverse pulsing.

Even though pulse periodic reverse plating is often reserved for through hole plating in industry applications, periodic reverse pulse plating improves macroscopic throwing power, for deposits made in vias on the micron size. [50] As device sizes are reduced for the capture dots or electroplating in pursued other MECS applications, pulse periodic reverse plating should be optimized.

3.3.7.1 Results

Below is a summary of the plating results. The most reliable recipe for copper electroplating of the capture dots in the designed electroplater is listed first; then the second most reliable, and so on.

1. Pulse Plating - 20 ASF, organic and inorganic additives
2. Periodic Reverse - 20 ASF, organic and inorganic additives
3. Periodic Reverse - 120 ASF, no additives
4. Pulse Plating - 120 ASF, no additives
5. Direct Current - 20 ASF, organic and inorganic additives
6. Direct Current - 20 ASF, inorganic additive only
7. Direct Current - 20 ASF, no additives

3.4 Sputtering

Two types of sputtering systems are available for processing at Oregon State University: two planar magnetron sputter tools and one ion beam sputter tool. The ion beam sputter tool is a Vecco Microetch, with one 3 inch substrate with no heating and a non-water cooled rotating target holder, capable of holding three 6 inch targets. This system is a DC triode system; a neutralizer filament neutralizes insulating and conductive targets. A DC voltage maintains the plasma discharge that accelerates argon ions, a grid stabilizes the discharge.

The Tang and CPA sputter tools are RF magnetron sputtering systems. They both have water cooled targets. This is desirable since during the progression of sputtering runs, the targets become heated from ion bombardment, excess heating allows for thermal evaporation of the target. For obvious reasons (difficult reproducibility) this is undesirable. Magnetron sputtering was developed to reduce heating from electron bombardment of the substrate. A magnetic field traps free electrons, but is small enough to allow large ions (Ar^+) to be left relatively unaffected.

3.4.1 Ion Beam Sputtering

Sputtering is a process of momentum transfer. A glow discharge containing ionized atoms of the process gas (Ar or $Ar/O_2(80/20)$) is focused by a series of grids to impinge on the surface of the target. Heavier gases, like argon, are needed to sputter, allowing for efficient momentum transfer. Few targets have reasonable sputter rates in lighter gases like nitrogen or oxygen. However, lighter gases like nitrogen and oxygen are often required to be part of the sputter gas, depending on the results the process engineer desires to achieve. Oxygen is used in reactive

sputter and is used for the ITO thin-film heaters, to increase film stoichiometry by replacing oxygen lost from the target (reword).

In ion beam sputtering, a neutralizer filament between the focusing grids and the target surface provides electrons to neutralize the argon ions. The now neutralized argon atoms still have enough momentum to eject atoms from the surface of the target to the sample. There cannot be an excess of electrons or positively charge argon atoms, otherwise a target current builds up and the ejected atoms will not travel in the predicted direction to the sample. Therefore, neutralizer current is constantly monitored and adjusted to keep target current as minimal as possible.

Sputtering is capable of producing more uniform films than evaporation due to the close target-to-substrate distance. Reactive sputtering is also possible with this close target-to-substrate distance. Reactive sputtering is important for films that need to be oxidized, as is the case with TCO's. In reactive sputtering an oxygen/argon gas mixture is used for the process gas. The argon atoms provide the necessary energy to eject atoms from the target surface and the oxygen oxidizes at two places: the target surface and at the sample surface. Sputtering has a smaller mean free path compared to the evaporation mean free path. Due to sputtering pressure greater than evaporation pressures. The distance from source-to-substrate much smaller in sputtering; therefore, particles are not the issue they are in evaporation.

3.4.2 CVD: Chemical Vapor Deposition

In most plasma enhanced chemical vapor deposition (PECVD) systems, a glow discharge is excited by an RF signal/power supply. Electron energies are typically 1 eV to 10 eV, enough to decompose the gas molecules into free radicals, ions, atoms, molecules in their ground state and excited molecules. Direct or conventional

PECVD has reactant gas product, substrate and glow discharge all in the same chamber space. Conventional PECVD, like ours at Oregon State University, has a parallel-plate plasma deposition reactor and is capacitively coupled. Our system, versus down stream PECVD where substrates are not in the glow discharge area, has poorer film stoichiometry. By-product gases get into the film. Oxygen, nitrogen, and hydrogen are all common to have incorporated into silicon dioxide films deposited via PECVD.

PECVD oxides are compressively stressed, due to energy in species bombarding the growing film. The benefits of PECVD versus other chemical vapor deposited films includes lower process temperatures and non-directional coating. Many thin films and materials used in MEMS processes require conformal passivation layers; however, these films cannot stand higher processing temperatures. In low-pressure chemical vapor deposition (LPCVD) another thin-film deposition method, the lowest process temperature is 700 C°. Our PECVD system process is optimized at 350 C°.

3.4.3 RTA: Rapid Thermal Anneal

A rapid thermal anneal (RTA), or rapid thermal process (RTP) system enables rapic heating of samples. The systems contains a quartz water cooled chamber. With two thermocouples (not to be confused with the thermocouples used in monitoring chamber pressure): one monitoring the silicon wafer base temperature and the other monitoring the temperature of the substrate being annealed. Ambient gas flows at a constant rate. The RTA takes the sample from room temperature to the desired temperature in a short time, on the order of a few minutes. RTA and RTP processing is done at atmospheric pressure and not under vacuum. The advantage

of RTA is less diffusion of dopants or interdiffusion of films, since the samples are at high temperatures for a relatively short time.

3.4.4 RIE: Reactive Ion Etch

The reactive ion etch (RIE) has the ability to selectively, anisotropically etch. Anisotropic etching occurs when the etch is vertical and etches little, if at all in the horizontal direction. A glow discharge, of the appropriate processing gas, is created in the vacuum process chamber. The ions selectively react with the patterned thin-films at the substrate film surface. Typically, patterned photoresist masks off areas where etching is undesirable.

The OSU RIE has four process gas lines and a nitrogen line for flushing and venting the chamber safely. A mixture of trifluoro-methane CF_3H and O_2 is used for optimal etching of the SiO_2 and photoresist, also referred to as ashing. To etch SiO_2 or silicon, two or four fluorine combine with the silicon atoms (forming SiF_2 or SiF_4) and are carried away with the O_2. The organic photoresist is burned or ashed, by the O_2 in the plasma. The large oxygen atoms break the bonds at the surface of the organic photoresist. Often there is a residual trace amount of the ashed resist on the substrate surface, if this occurs a short AMD clean will remove the remaining resist. [26]

3.4.5 Spin Coater/Mask Aligner

A CEE spin coater provides accurate spin times and speeds. The CEE spin coater controls: rate at which final speed is achieved, final spin speed with in $\pm$ 2 rpm, time at full spin speed and the rate of reducing spin speed to a stop. The substrate is held to the spin chuck with a gentle vacuum. A Karl-Suss MJB3 mask aligner is used in the photolithography steps. This system has the ability to align

to $\pm$ 1 μm and utilizes a mercury lamp as its source for exposure. The mercury lamp can be used with i-Line and g-Line sensitive photoresists.

3.4.6 Ultrasonic Cleaners

Ultrasonic cleaning provides vibrational, non-contact scrubbing, removing particles on the substrate surface. High intensity sound waves generate a pressure flux, producing microscopic bubbles. Bubbles form and collapse, creating shock waves. When these shock waves contact the substrate they loosens and eventually dislodge particles from the substrate surface.

Two ultrasonic cleaners are used in the heater lift-off process; one for cleaning the substrates and the other for the lift-off developed for TCO's. A dilute concentration of Contrad 70 (a surfactant) aids in cleaning the surface of the samples. A 100% acetone bath is used for removing the photoresist after sputtering in the TCO heater lift-off process.

3.4.7 Profilometer

The alpha-step 500, measures thin-film thicknesses with a stylus. A stylus (a narrow, pointed metal piece, see Figure 3.4) is lowered carefully onto the surface of the substrate. The stylus, now in direct contact with the sample, is lightly dragged across the substrate at a pre-determined rate. As the stylus follows the contour of the surface, its vertical motion is measured and a corresponding voltage is produced. The structure depth, height, relative uniformity and linewidth shape is obtained.

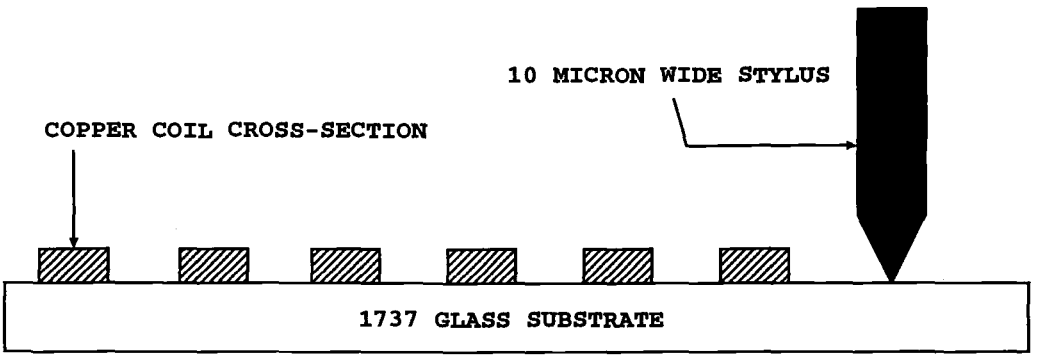

Figure 3.4: Stylus.

3.5 Summary

This section reviewed the basics of process equipment used in the development of the capture dots and thin-film transparent heaters. For more in-depth discussion, the referenced material should be examined more thoroughly.

4. CAPTURE DOT FABRICATION

This chapter describes the processes developed for the fabrication of the capture dots in general, before discussing the specific process flow. The capture dot fabrication steps can be viewed in a step-by-step list in their entirety in Appendix C, along with the probability of the success of each process step. For successful fabrication of the capture dots: photolithography, electroplating, etching, and other deposition techniques have been developed.

Capture dots are coil devices that produce a magnetic field to capture the beads in a channel. The capture dots are fabricated using photolithography, electroplating, etching and other common device fabrication methods. The details of developing these process are explored in this chapter. A close up of one of the fully processed capture dots can be seen in Figure 4.6 of Section 4.4. The coil (capture dot) produces the magnetic field, the two contact pads (partially viewable in figures 4.2, 4.3, 4.5 and 4.6) allow a low voltage to be applied and are formed by etching through a passivation layer required to electrically isolate the coils from the liquid flowing in the channel.

4.1 Photolithography Process Development

This section details the development of the photolithography processes developed for electroplating, RIE and lift-off, paying particular attention to thick (> 3 μm) photolithography. For the capture dots to produce the necessary magnetic field to attract a ferroelectric bead, initial calculations revealed copper lines as thick as 5 μm were necessary for a 500 μm wide coil with 10 μm line widths and line width spacing or for 15 μm line widths and line spacing. Figure 4.1 shows the first of four photolithography layers. This pattern defines the electroplated copper coil. The

Figure 4.1: Photoresist pattern of the first lithography layer of a square capture dot with 10 μm lines and 10 μm spacing between electroplated lines.

pattern is slightly overexposed, creating electroplated layers that are slightly wider than 10 μm. This overexposure is done on purpose, since after electroplating, a copper etch to remove the underlying seed layer also etches the sides of the electroplated layers. Over exposing produces lines that are no less than 10 μm. Figure 4.5 shows the coils just after etching the seed layer. Figures 4.2 and 4.3 show one of the circular patterns and one of the square patterns. Both of these patterns are defined in chrome on a quartz mask and are the patterns that are transferred after exposure during the first photolithography step.

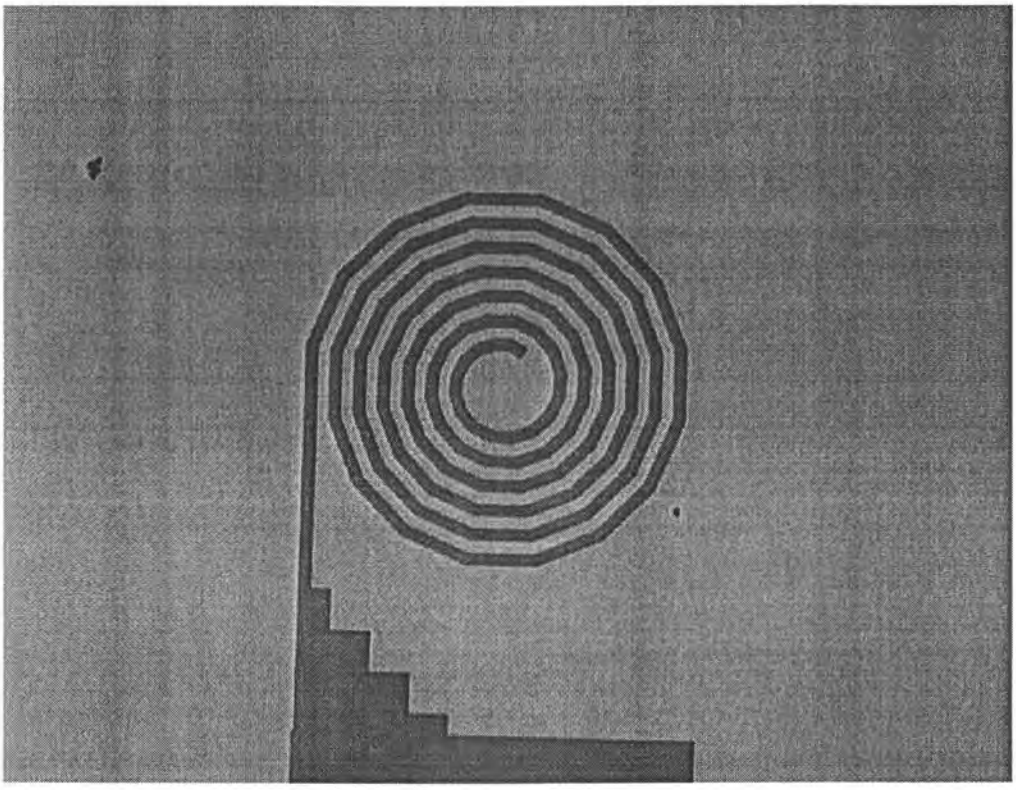

Figure 4.2: Chrome plated quartz photomask for layer 1 of a 500 μm circular capture dot with 100 μm hole.

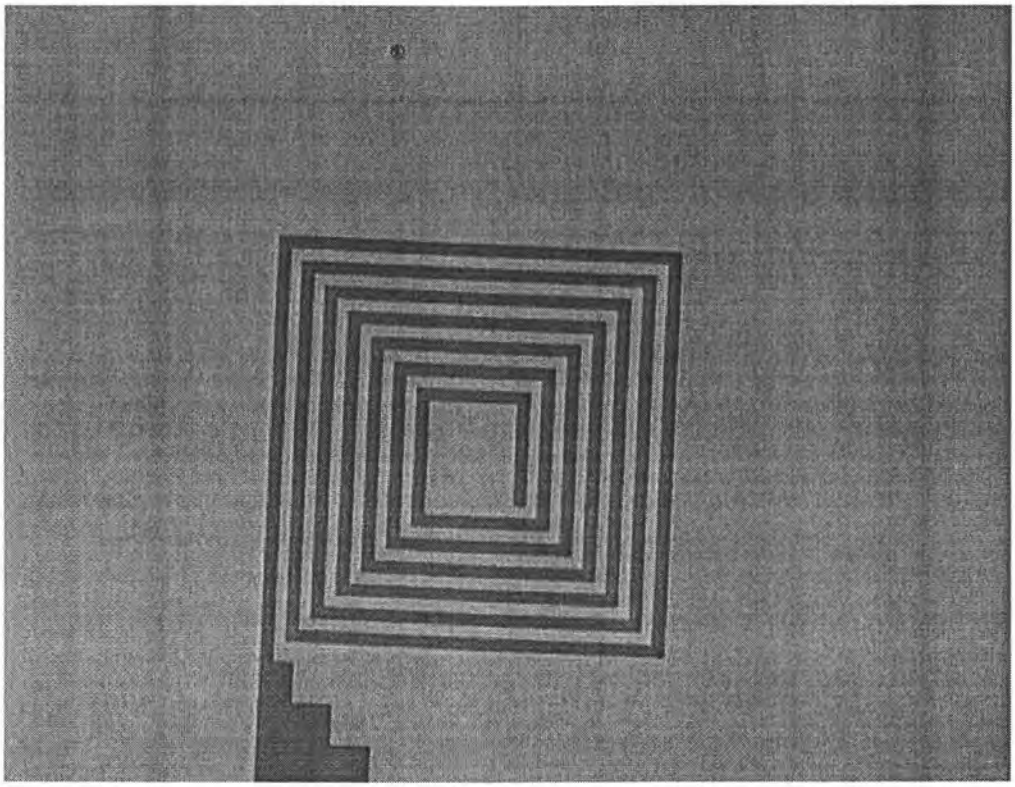

Figure 4.3: Chrome plated quartz photomask for layer 1 of a 500 μm square capture dot with 100 μm hole.

4.1.1 Photoresist Selection

To achieve the necessary 5 μm thick copper lines, electroplating is needed since conventional thin-film methods cannot deposit such thick coatings as easily, as reliably and certainly not with the through-put that electroplating provides. To create the pattern for the electroplated layer(s) either thick photoresist (> 5 μm) or multi-layers (requiring photoresist that adheres to itself) of thin photoresist are required. Since a single layer of spin coated photoresist is far less complicated than a multi-layer process, a single coat process was developed.

Five positive photoresists were examined: AZ1800, AZ1350, SPR 220 (7 μm), SPR 220 (1.2 μm), and Shipley S1813. Only SPR 220 (7 μm) provides a single coat thick enough to allow a one-layer process. Supporting SPR 220 (7 μm) as the primary resist to develop the capture dots process is its ability to adequately withstand a five minute RIE etch in a CHF_3/O_2 plasma, to withstand multiple wet chemical etches and to hold up to a 15 minute highly acidic electroplating bath. SPR 220 also adhesres well to a wide range of metals, TCO's, insulators, glass and silicon and retains a thickness of no less than 5 μm with a single spin coat.

Photoresist thickness, adhesion, etch resistance properties, flexibility and thermal flow stability are decided primarily by the quantity and type of photoresist resin. Resist is rated for a range of thicknesses. Final resist thicknesses are determined by varying bake time, initial spin speed, final spin speed, time duration of spin, amount of initial photoresist on the wafer, and wafer area. [26] The remainder of this section will examine these properties of SPR 220 in detail.

4.1.2 SPR 220 Chemistry

SPR 220 photoresist is composed of ethyl lactate, anisole, diazo photoactive compound, cresol novolak resin, cresol, 2-Methyl Butyl Acetate, n-amyl acetate and

organic siloxane surfactant (see MSDS Appendix E for details). The shelf life of this photoresist, as with all photoresists, is extremely important to monitor. All SPR 220 resists have a shelf life of approximately 1 year. After the shelf life of the resist expires, the photoresist starts changing its properties; for example, its ability to stand up to certain wet and dry etches will degrade. The PAC starts decomposing to ICA without the previously necessary UV exposure (see Section 2.2.1 for a detailed description of PAC/ICA). This degradation makes processing unreliable.

4.1.3 Photoresist Thickness

Photoresists come in a variety of viscosities and formulations designed to provide specific thicknesses. In the semiconductor industry the push for smaller dimensions has pushed photoresist to be ultra thin. At Intel current 90 nanometer processes use 0.3 μm thick photoresist. On the other end of the spectrum MicroChem Corporation produces several thick photoresists. They have an SU 8 line that is available for films as thick as 200 μm.

Two thickness of the SPR 220 photoresist have been developed: SPR200 (1.2 μm) and SPR 220 (7.0 μm). There is no difference in the components of the two resists; however, the amount of cresol novolak resin is greater in the 7.0 μm photoresist than in the 1.2 μm photoresist. Both resists vary in thickness depending on the spin conditions. The 1.2 μm and 7.0 μm are thicknesses representative of the *recommended* thickness the SPR 220 series resists can be. Slow spin speeds are required to achieve the thickest coating, increased spin speed allows for thinner coatings.

4.1.3.1 Thin Photolithography (1.2 μm)

SPR 220 (1.2 μm) is the less viscous of the SPR 220 photoresists used for the capture dot fabrication. Depending on how the SPR 220 (1.2 μm) is processed, the thickness varies between 1.5 μm and 1.1 μm, with a single coat. [64] The SPR 220 (7.0 μm) resist could be used in place of the SPR 220 (1.2 μm) and originally that was how the capture dot process was developed, using only SPR 220 (7.0 μm). The benefits of using only the SPR 220 (7.0 μm) resist include lower cost and less process development. However, during the second photolithography step, aligning the vias to +/- 1.0 μm, is far more difficult with the thicker resist due to a limited depth of field. Alignment is the most limiting process step to creating successful capture dot devices. By reducing the via layer photoresist thickness, the probability of creating a successful capture dot improves dramatically, making the SPR 220 (1.2 μm) well worth the cost.

4.1.3.2 Thick Photolithography (7.0 μm)

SPR 220 (7.0 μm) is used for electroplating 5 μm of copper. Depending on how the SPR 220 (7.0 μm) is processed, the thickness varies between 6.5 μm and 10.2 μm. Due to depth of field problems that arise when aligning thick photoresists, the resist is processed so that the thickness is only 6.5 μm. The numbers mentioned above for photoresist thickness range will vary slightly when different photoresist developers are utilized.

4.1.4 Spin Coating

The SPR 220 (1.2 μm) and (7 μm) differ in viscosity. To achieve the thinnest possible version of both, the resist is spun on in a two part spin coating. After the substrate is held lightly, but firmly, in place on a vacuum spin chuck, approximately

2mL - 3mL of photoresist is deposited via an eye dropper. The CEE spin coater first spins the substrate and resist at 1000 rotations per minute (rmp) for 6 seconds, then increases to 4000 rpm for 60 seconds. The increase in spin speed takes 3 seconds and is included in the 60 seconds.

4.1.5 Exposure Time

Two combination exposure/alignment systems were used during the capture dot process development. Both alignment systems use a mercury source (350 nm - 450 nm) for the ultra-violet (UV) wavelength exposure. The SPR 220 series is most responsive to the UV wavelengths. In Covell Hall an Oriel Solar Simulator system is used for exposure, in Owen Hall a Carl-Suss MJB3 system is used. The Covell Hall lab lamp is approximately nine inches from the substrate being exposed, requiring an exposure time of twenty-eight seconds to allow all the PAC to convert to ICA. The Advanced Materials Lab lamp has a spacing closer to three inches from the substrate and takes seven seconds for complete exposure. The Carl-Suss MJB3 has an exposure power of 275 - 276 Watts.

4.1.6 Soft Bake Time(s)

SPR 220 has a bake time of 120 seconds at an oven temperature of 90 C° on glass or silicon substrates. The insulating substrate did not increase the bake time, since the oven bakes the photoresist from all sides; unlike a hotplate bake, where the photoresist is baked only from the substrates underside. For Plexiglass substrates, the bake time is increase to six hours at 60 C° to prevent warping of the less temperature-tolerant plastic. When a hot plate is used for glass or silicon substrates, the bake temperature is increased to 115 C° and the time reduced to 90 seconds. The same bake times were adequate for the dimensions used in the

capture dot and heaters; however, it should be noted that it is likely the silicon substrates are slightly thinner, having more solvent driven out during the hotplate bake since the silicon substrate conducts heat better than that of the quartz glass substrates. These process parameters yield SPR 220 - 7 μm thickness of 5.5 μm to 6.0 μm. The variation in film thickness is attributed to several parameters: variation in initial amount of photoresist deposited, lab temperature, alignment time, substrate material. With increased alignment time more solvent in photoresist is lost, consequent reducing overall thickness and increasing exposure time.

4.1.7 Development Step

SPR 220 can be developed in several developers. For best results with the capture dots, having a 10 μm critical dimension, the manufacture suggested developer used is Microposit MF702. Many multi-purpose photoresists have a developer that comes concentrated and is diluted; however, MF702 is manufactured to be used exactly as it comes shipped; no dilution is required.

Developers of positive photoresist are designed to remove the photoresist wherever UV exposure illuminates the photoresist. Throughout the capture dot processing, immersion developing is used. This is a process where the substrate, and exposed photoresist pattern are submersed in the developer, and the developer is gently agitated until a pattern is seen through the resist to the substrate below in the photoresist. For thick resists, like the SPR 220 (7 μm), the agitation is needed to removed the decomposed photoresist from the patterns. ICA, initially removed, can settle back into the pattern, not leaving a clean pattern. The total time the substrate spends in the developer is dependant on photoresist thickness and the exposure dose. The thicker the photoresist, the longer the developer time is. For SPR 220 (7 μm) developed in MF702, development time is approximately 135 seconds.

After the substrate is removed from the developer, it is rinsed in deionized water and dried with dry nitrogen. When rinsing with deionized water, care is taken to carefully rinse any ICA that may have settled in the exposed pattern. During the nitrogen dry, the nitrogen pressure is reduced, at higher pressure the coil patterns can shift on the substrate.

4.1.8 Photoresist Removal

Once successful patterning has been accomplished, removal of the old photoresist is required. There are three common methods of positive photoresist removal: acetone rinse, RIE ashing and/or rinse in photoresist-specific stripper. Two methods of removing the SPR 220 series photoresists were developed: acetone rinse and RIE ashing.

One of the benefits of using a positive photoresist is the ability to use acetone, a common and in-expensive solvent, for photoresist removal. This is particularly nice for the capture dot fabrication because an AMD clean is already required after the photoresist removal steps. AMD is short a rinse first in acetone, then methanol, and finally in deionized water. Ashing is a dry etch (dry meaning to chemical bath), often performed in an RIE. Ashing is utilized after the RIE etch of SiO_2. In ashing, the vacuum chamber is evacuated with a nitrogen purge and an oxygen glow discharge is struck. The oxygen plasma, dark blue in color, bombards the surface of the photoresist and removes the photoresist with the high energy oxygen ions (this is commonly refereed to as "burn-off"). Stripper, specific to the photoresist being used, is supplied by Shipley, the SPR 220 manufacture. Strippers specific to the resist remove the resist at a controllable rate; however, like the SPR 220 stripper, they are often costly and most are toxic.

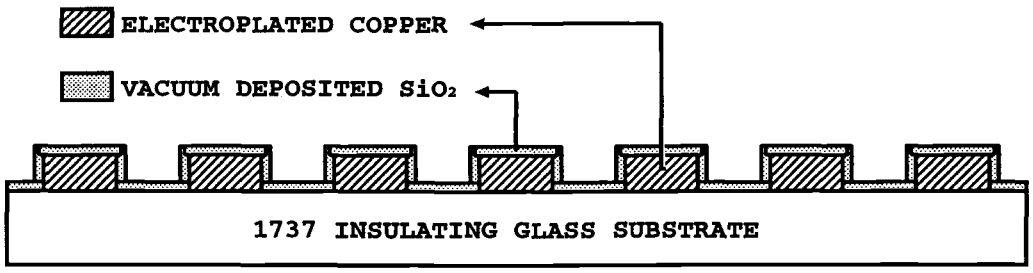

Figure 4.4: Ideal film uniformity of the passivation layer between the two electroplated copper layers.

4.2 Passivation Layer

A high quality SiO_2 insulating layer is needed to electrically isolate the two electroplated layers from each other except at the via. This is no trivial task since the electroplated layers are 5 μm thick and the coil lines are spaced so closely together (10 μm spacing between lines). The sharp corners of the electroplated copper layer(s) makes conformal coating of SiO_2 across the electroplated layer difficult. However, it is possible to passivate adequately and two separate methods of depositing the SiO_2 for the passivation layer have been developed. Figure 4.4 shows an ideal cross-section of the passivation layer between the two electroplated copper layers.

4.2.1 Ion Beam Sputtered SiO_2

Ion beam sputtered SiO_2 is deposited from a six inch diameter target in an oxygen/argon (90%/10%) gas mixture or a pure argon gas. Poor stoichiometry results when pure argon is used for sputtering oxide targets like the SiO_2. The benefit of using a pure argon ambient is saving time, the following Copper layer sputtered cannot be oxidized. The layers deposited after the passivation layer are titanium and copper. These two metal layers constitute the seed layer before electroplating

and both are deposited in pure argon gas. To reduce process time, all three layers are sputtered in argon: SiO_2, Ti, and Cu.

SiO_2 ion-beam sputtered in an oxygen/argon (90%/10%) mixture had been presumed to increase the yield of the capture dot fabrication by improving the stoichiometry and hence improving the quality of the dielectric between the electro-plated layers. When ion beam sputttered SiO_2 was integrated into the capture dot fabrication no increase in the capture dot yield was seen. Process time increases with the sputtering in oxygen, since following metal layers cannot be deposited in the oxygen plasma.

The ion beam sputtered passivation layer is off-angle sputtered. The corners of the coils and the bottom of the trenches are passivated; however, breaks in the SiO_2 along the sidewall are a serious concern due to sputtering being a line of sight deposition. The side walls have less deposited SiO_2 than elsewhere on the substrate.

4.2.2 PECVD SiO_2

PECVD is a popular method for lower temperature deposition of SiO_2, since reasonably high quality SiO_2 with few pin holes can be deposited at 350 C° for 40 minutes. Conformal coverage of the coils is difficult due to the SiO_2 not depositing as thick on the corners of the coils as elsewhere on the substrate. Also the PECVD process at OSU is not highly repeatable, due to lack of a well-established deposition method. After a well established PECVD process is in place, PECVD SiO_2 requires little attention compared to ion beam sputtering.

4.2.3 Conclusions

A relative thick layer of SiO_2 is deposited no matter which method of SiO_2 deposition is used. Due to increased process time and lack of improved capture

dot yield, the ion beam sputtered SiO_2 in 100% argon was utilized. Time is saved by processing other wafers when PECVD can be used. Both have their benefits; however, PECVD is the passivation layer of choice when the PECVD system is working reliably. The PECVD should be a better dielectric for a couple reasons. First, the PECVD layer is grown with with NO_2 gas, incorporating some Nitrogen into the SiO_2 film, which increases the dielectric constant. Also, ion beam sputtering in pure Argon will be less stichometric, lowering the dielectric constant.

4.3 Etching Method(s)

After the electroplating is completed, the plated structures need to be electrically isolated from each other. To isolate the structures an etch is needed to remove the conductive seed layer (titanium and copper), by removing the 2000 $\AA$ seed layer. Before the second electroplated layer is deposited, vias are etched through the passivating SiO_2 layer. The capture dot process involves four different etchant recipes for etching SiO_2, Ti and Cu layers. This section discusses the recipes and reasons for choosing these etchants over others.

4.3.1 Reactive Ion Etch (RIE)

Reactive ion etch (RIE) is a high throughput method for anisotropic etching. In RIE one or more gases flow (via mass flow controllers) into the process chamber, a glow discharge is struck and maintained with the appropriate process gases. This glow charge provides high energy ions available for bombarding the surface of the substrate. The gases provide selective etching of materials. RIE can be used to effectively etch a wide range of materials: metals, TCO's, insulators, organics.

The RIE had been down for a several year period, instructions for its operation are included in the Appendix. This tool has four inlets for process gases and a

nitrogen vent line also used for purging. Currently the RIE is set up with process gas used to etch organics, SiO_2, PZT and TCO's. To etch the deposited SiO_2 by reactive ion etching triflouro-methane is used. Including a small amount of oxygen increases the etch rate. However, oxygen also burns the photoresist used to define the patterns being etched. Therefore, the thicker SPR 220 photoresist is desirable for the RIE SiO_2 etches. The RIE etches SiO_2 at 80 $\AA$ per minute at 50 watts, 4 sccm of CF_3H, 5 sccms of oxygen at 30 mTorr. An etch rate was not determined for the photoresist ashing.

4.3.2 Isotropic Chemical Etches

Wet etching, an isotropic etch, removes material in all directions, both vertically (downward) and horizontally (outward). Anisotropic etching is typically more desirable, since isotropic etching leads to undercutting. However, isotropic etching of the copper has proven to be best suited for the electroplated layers. The sharp corners of the copper make passivation difficult, but since the copper wet etch etches in both directions, the edges become rounded, making passivation more achievable than is possible with an anisotropic etch.

4.3.2.1 Copper Etch

For the capture dots, isotropic etching the Cu was most desirable. The thinnest coils are 10 microns wide and 5 microns thick. When etching down 5000 $\AA$, the width is only reduced 5% while the coil thickness is reduced 10%. Diluted ferric chloric acid (ferric chloride) is used to selectively etch the copper. This wet etch removes 5000 $\AA$ and will continue to etch away at the coils if the substrate is not quickly removed from the etching solution and rinsed in deionized water. The copper etchant saturates (saturation occurs when the solution is unable to etch the copper because the reactants in the copper etch that remove the thin copper layer are used

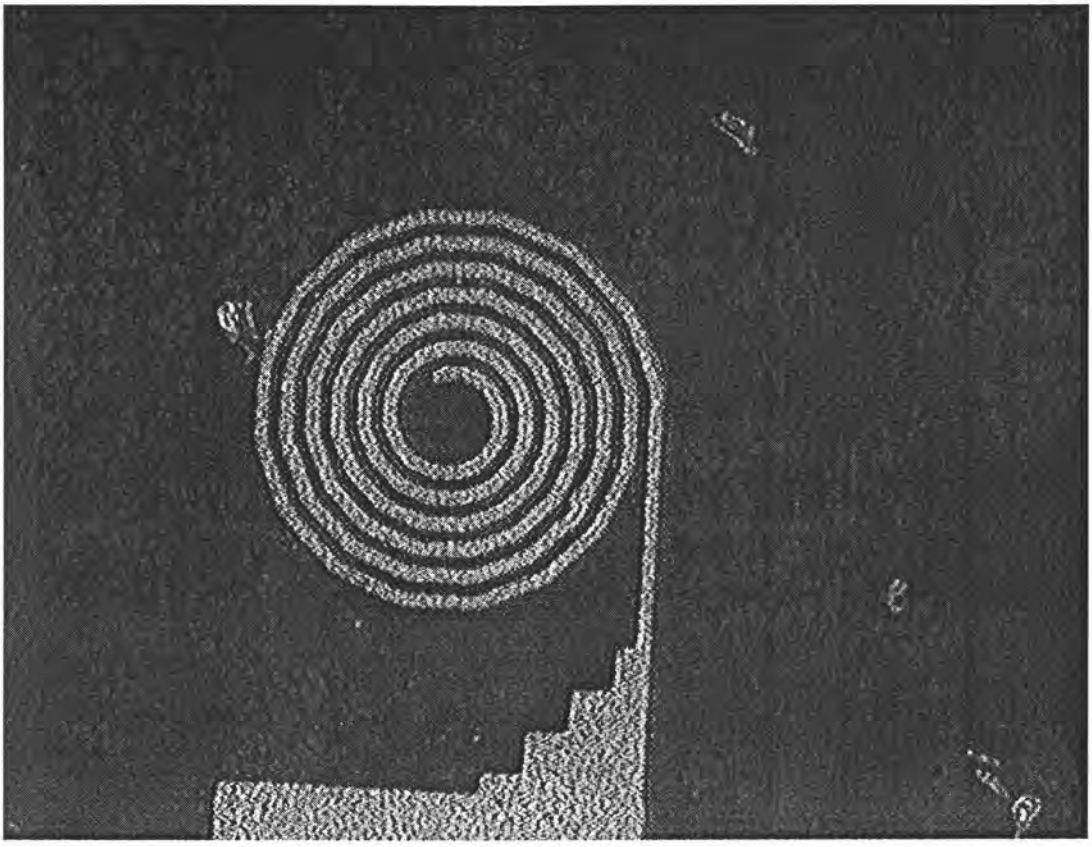

Figure 4.5: Electroplated coil after wet chemical etches have removed copper and titanium seed layers.

up). Therefore, new solution is developed after only a few etches. The copper etchant stops at the underlying titanium. Figure 4.5 shows the coil structure after the underlying copper and titanium etches have completely removed the conductive seed layers. The copper etch has also slightly rounded the edges of the electroplated copper, reducing the chance of a short between the two electroplated layers. An approximate of etch rate of 100 $\mathring{A}$/minute was the goal for etching the copper.

4.3.2.2 Titanium Etch

The titanium is an adhesive for the copper seed layer and subsequent electroplated copper. When the capture dots are processed without an adhesive layer they start to lift off of the substrate within a 24 to 48 hour period. Originally, evaporated chromium was used as an adhesive layer, but the wet etches for etching chromium rapidly etched the 5 μm of electroplated copper before etching the intended chromium. The titanium etch, selectively etches titanium, leaving copper, silicon, and silicon dioxide relatively unaffected. The titanium etch (20 H_2O:1 H_2O_2:1 HF) etches approximately 50 $\AA$ per minute. This makes titanium a highly effective way of preventing lift-off while at the same time leaving the coil structures electrically isolated. The titanium etch is never reused to avoid saturation and maintain etch rate.

4.3.2.3 Silicon Dioxide Etch

After the coils are electrically isolated, a passivation layer of silicon dioxide, is deposited. To make contact to the coils, a wet etch that selectively etches SiO_2, leaving titanium, copper, silicon, and photoresist unaffected was necessary. There are several etches for SiO_2. The etch used in the coil process is a wet etch commonly, but mistakenly referred to as buffered HF, it will be called dilute HF. Dilute HF is comprised of hydrofluoric acid diluted with de-ionized H_2O. Dilute HF ratio commonly varies from 50:1 (de-ionized H_2O:HF) to 6:1, depending on desired etch rate. The 10:1 dilute HF was implemented for the capture dot via etch. This solution rapidly etched the SiO_2. The slide was put into the solution for a short period of time (approximately 20 seconds), removed, rinsed in de-ionized H_2O, and viewed under a microscope. This process was repeated until the SiO_2 started to etch under the thin SPR 220 photoresist layer. There are other forms of SiO_2 etches called

buffered HF. Some forms have NH_4F, or HNO_3 or HCl in combination with the dilute HF just discussed. [65]

4.4 Capture Dot Fabrication

To fabricate the capture dots, a 2" by 3" pyrex microscope slide is AMD (acetone/methanol/di-water rinse) cleaned to remove particles. The pyrex slide is then ion beam sputter coated with titanium (200 to 300 $\AA$). Without breaking vacuum, a copper seed layer is ion beam sputtered (2000 to 5000 $\AA$). Next, the first photolithography step leaves 18 coil patterns in photoresist that is between 5.5 μm - 6 μm formed in the SPR 220 (7μm) photoresist. 5 μm of copper is electroplated through the photoresist pattern and the photoresist is removed with an AMD clean and N_2 dry.

The titanium and copper seed layers are removed with the appropriate wet etches. The wet etches serve two purposes: to electrically isolate the electroplated coils from each other and because a wet etch is an isotropic etch, the etch removes sharp edges from the copper coils making passivation easier to accomplish. (see Figure 4.4)

Passivation follows after the electroplated structures are electrically isolated. As described previously two methods have been developed to passivate the electroplated layers. The ion beam sputtered SiO_2 provided acceptable isolation and is used to complete the capture dot structure. The PECVD SiO_2 never created a reliable enough passivation layer to electrically isolate the copper layers. Substrate heating of 350 C° is typical of PECVD SiO_2. However, shortly after deposition the substrate is removed from the system and small cracks in the SiO_2 formed. This cracking is attributed to the difference in thermal expansion coefficient between copper and SiO_2. SiO_2 has a CTE of approximately $5.8*10^6/C^o$, copper has a CTE

of $17*10^{-6}/C°$. [66] When the substrate temperature was reduced to 200 C° less cracking occured; however, more particles were created, creating pin holes in the SiO_2.

After the SiO_2 passivation another photolithography step is completed using the SPR 220 (1.2 μm) photoresist. The thinner resist allows aligning to be more accurate. After aligning, exposure and development, 18 total 10 μm by 10 μm square vias are left in the photoresist that will allow the two electroplated layers to be connected to each other in that single area. The substrate goes through a short RIE to anisotropically etch the SiO_2 vias, leaving an opening to the first electroplated copper layer. Initially the vias were opened up with a chemical wet etch using HF, HF is dangerous chemical, making RIE favorable. The RIE run then ashes the photoresist by purging with N_2 and re-striking a plasma with only O_2. Often a residual layer of photoresist is left. When this occurs, an AMD clean followed with a N_2 dry follows.

After the vias have been established, another seed layer of titanium and copper is ion beam sputtered. The ion beam sputtering is done slightly off angle to ensure the edges and sides of the first layer and vias of the capture dots are completely coated. After the second seed layer is sputtered, another photolithography step is completed to create 18 lead patterns starting at the center of the coils, where the vias are, and travelling out across the passivated coils to a contact pad pattern. This pattern is electroplated, followed by a chemical wet etch to electrically isolate the copper pads from each other.

Another sputtered SiO_2 layer is deposited by ion beam sputtering to passivate the coil leads from the liquid solution and cells they will come into contact with when integrated into the channel. The final photolithography step is completed with the SPR 220 (1.2 μm) photoresist and a large square contact pad over each copper

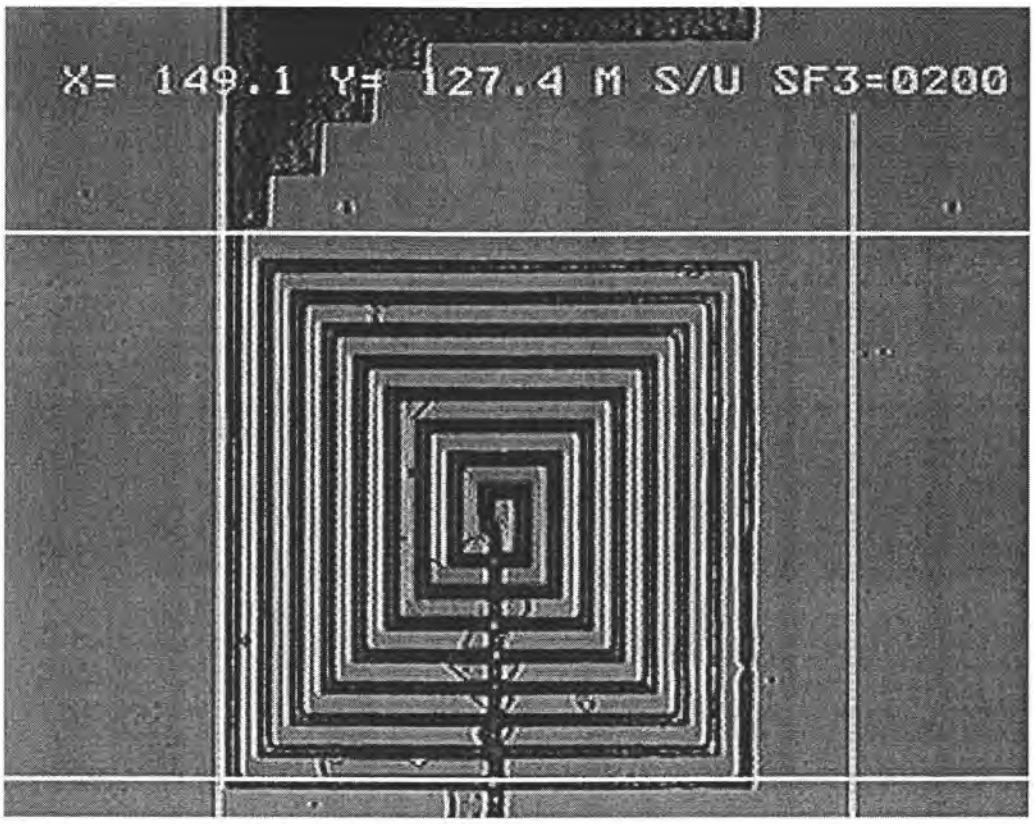

Figure 4.6: Fully processed square pattern capture dot with 10μm line spacing and 10 μm electroplated copper line width.

contact area is exposed and developed. A wet etch then removes a large portion of the SiO_2 layer covering two contact pads to make contacting to the capture dots more accessible. Lastly, the substrate goes through a final AMD clean and N_2 dry. See appendix C for a complete step-by-step fabrication list with approximate percent chance of the specific process step completing successfully. Figure 4.6 shows a complete, electrically active device.

4.5 Electrical

Current-voltage measurements of the capture dots were made to verify that sufficient current could be applied at low voltages. Milli-amps of current at low voltages are necessary if the capture dots are to be portable. To achieve 100 milli-amps of current an average applied voltage of 0.9 volts was necessary, this is taking the average of all the coils, recall that there were several designs, coil and circular patterns both with line thickness and spacing of either 10 μm or 15 μm. Of all tested capture dots the highest voltage to achieve 100 milli-amps is 1.09 volts and the lowest voltage to achieve 100 milli-amps of current is 0.44 volts. None of the capture dots failed during testing, all coils were measured at least twice. The capture dots also showed linear current-voltage measurements allowing one to concluded that heating was effecting the electrical properties. It is also worth noting that several coils could be activated at simultaneously by a 5 volt battery if the capture dots were in a system where it was required to look at multiple ferro-magnetic beads concurrently or in rapid succession.

4.6 Conclusion

Successful capture dot structures were developed with the aforementioned processing. However, with the large number of process steps and low overall probability of creating a completed, working capture dot structure, more attention needs to be awarded to process steps with low yield (aligning, passivation) and for process steps that have the potential to irreversibly damage the capture dots (electroplating, passivation) during process.

5. TRANSPARENT CONDUCTIVE HEATERS

This chapter discusses the development, fabrication and characterization of transparent Indium Tin Oxide (ITO) thin-film heaters. Transparent thin-film heaters are needed to controllably heat and boil a liquid lithium bromide/heater interface. Lithium bromide has a boiling point of 1265 °C. It has been estimated that five watts of power are required to achieve this. The heater requires high transmissivity in the mid-wave infrared (MWIR) wavelengths (3 μm to 5 μm) and high transmissivity in the visible wavelengths (400 nm to 700 nm). The transparency in the visible range is needed for alignment of the heater to the channel where the lithium bromide liquid flows. The transparency in the MWIR range is needed for an IR camera to see through, from the back side of the heater, to show heating effects at the heater/lithium bromide interface.

5.1 Transparent Conductive Oxide (TCO) Heater Fabrication

There are many well-known transparent conductive oxides (TCO's) that are highly transparent over the visible wavelengths: Zinc Oxide (ZnO), Zinc Tin Oxide (ZTO), Indium Tin Oxide (ITO), Zinc Indium Oxide (ZIO) and Gallium Indium Oxide (GIO), to name a few. Conductivity and transparency vary with process temperature; however, in general all the previously listed TCO's are no less than ~75% transparent in the visible wavelength range, making all acceptable to use for channel alignment.

5.1.1 Heater Material

ZIO, GIO and ITO are highly transparent over most of the MWIR wavelengths. ITO is strongly absorbing from 1.0 - 1.5 μm, whereas neither ZIO or GIO

absorb strongly at these wavelengths. However, since the interest was in the MWIR region (3.0 μm - 5.0 μm), ITO is still an acceptable candidate. To make a choice between these three, resistivities are compared. GIO is about 10 times as resistive as ITO and ZIO is no better than one and half times more resistive than ITO. ITO has an advantage over other TCO's due to its high conductivity. Indeed ITO is the least resistive of all reported TCO's. Therefore, due to ITO's low absorption in the visible and MWIR wavelengths and its low resistance, ITO is expected to be the best candidate for fabricating a thin film transparent heater.

5.1.2 Heater Substrate

CaF_2 is highly transparent from 0.19 μm (ultraviolet wavelengths) all the way through 7.2 μm (deep IR wavelengths). CaF_2 is a commonly used infrared optical material for lenses and windows, but it is not an ideal substrate for device fabrication. CaF_2 is a difficult material to fabricate heaters onto due to: brittleness, does not cleave along a particular length, does not cut well with a saw, does not handle compressive stress well and it does not heat uniformly, causing thermal stress during SiO_2 deposition.

The substrate only needed to transmit from 3 μm to 5 μm, for the infrared camera (IR) camera to see through the substrate and heater to image the liquid/heater interface. Silicon (Si) is mostly transparent from 1.5 μm - 8 μm and is well understood for processing. Si is a tough material and although it does not take compressive stress well it is better than CaF_2. Si is easy to cleave and can be cut nicely with a saw. Sputtered thin-films and PECVD thin-films adhere to Si nicely. Silicon also transmits heat through it well and it is well known how to grow an insulating layer of SiO_2 on silicon for passivation. Also silicon can be acquired quickly from multiple vendors at a lower cost than CaF_2.

5.1.3 Fabrication

The heater has to be very accurately placed ($\pm$ 5μm) on a Si/SiO_2 substrate. The surface of the substrate has to remain unscratched; even minimal scratching underneath the heater causes premature failure of the heater in that area, causing the ITO to heat up locally and burn out in these areas. To combat the scratches the initial three inch wafer was given a 2000 $\AA$ PECVD SiO_2 coating. The wafer was then cut into smaller pieces with a saw before alignment marks were cut into the Si substrate with a laser.

After the substrates received the alignment marks necessary for proper heater alignment, the protective SiO_2 is removed by RIE. A thick (greater than 1 μm) SiO_2 layer is then grown in by dry thermal oxidation. Since dry thermal oxidation is not a well established process at Oregon State University, the silicon wafer is left in the furnace long enough that 1.5 μm has been grown, to insure at least 1 μm of SiO_2. The substrates then go through a 30 minute ultrasonic bath in dilute Contrad 70, a mild detergent, followed by an AMD rinse. Great care in substrate cleaning is warranted to ensure no particles are on the substrate where the heater will later be deposited. If particles are left on the substrate, the following lift-off procedure will remove the deposited ITO and ruin the device.

After the cleaning, spr 220 (7 μm) is spun on and baked at 90 C° for 2 minutes. The heater pattern is exposed through a mylar mask with a Karl-Suss MJB3 mask aligner and mercury source. Development in a lightly agitated MF-702 developer takes approximately 2 to 3 minutes to remove the exposed photoresist, leaving the heater pattern. Once rinsed in deionized water and dried in nitrogen, a two inch RF magnetron sputter target 90% indium, 10% tin (by weight) is sputtered in a pure argon gas at a pressure of 30 mTorr directly in front of the heater pattern. Once 1 μm of ITO is sputter deposited, the substrate is placed in an ultrasonic bath containing

100% acetone. The ultrasonic bath is needed to remove the flags that would be left behind without the ultrasonic pulses to remove them. "Flags" are sections of ITO that have been deposited on the sides of the photoresist pattern, typically they are thin and brittle. A gentle rinse in acetone will not remove these flags and further processing will lead a more difficult time passivating. The ultrasonic pulses are strong enough to break these flags, creating a surface that is easy to passivate.

ITO increases in conductivity with an increasing number of oxygen vacancies. Therefore, a low temperature, 300 C°, argon anneal is done next to increase the heater conductivity, without significantly comprising visible transmissivity. Next, copper contact pads are evaporated directly onto the ITO heater through a finely machined, stainless steel shadow mask made in the IME department at OSU.

It is necessary to insulate and protect the heater from the lithium bromide; therefore, a 2000 $\mathring{A}$ SiO_2 PECVD layer is deposited over the entire substrate. The PECVD process substrate temperature is reduced to 200 C°. The lower PECVD substrate temperature helps alleviate the difference in the ITO and SiO_2 coefficient of thermal expansion (CTE). Finally, photoresist is spun on and an area is opened up with acetone to make contact through the SiO_2 to the contact pads. The exposed SiO_2 is etched in the RIE to make electrical contact to the heater at the copper contact pads. Figure 5.1 shows the final heater structure. See Appendix D for a complete step-by-step fabrication list.

5.2 ITO Heater Current-Voltage Measurements

The ITO heaters are characterized by a Cascade Microtech RF-1 probe station. Current-Voltage measurements are taken, like the one shown in Figure 5.2. The measured I-V curves should ideally have a linear relation, a straight line with a large slope ideally. However, the the I-V curves of the ITO heaters consistently

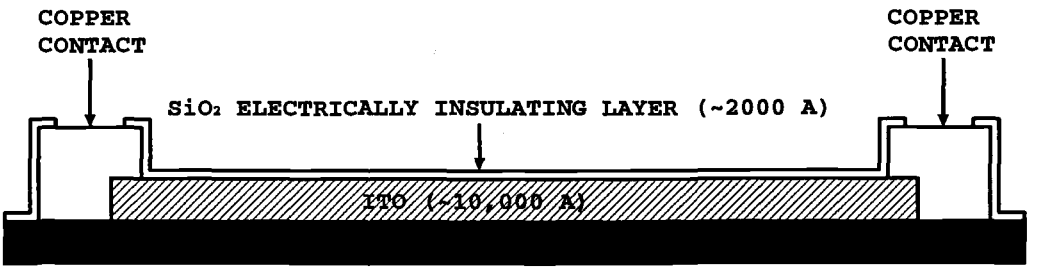

Figure 5.1: Final heater structure.

show hysteresis behavior, most severely with the 1200 $\AA$ thick heaters deposited on glass, Figures 5.2 (I-V measurements) and 5.3 (Power-Voltage measurements). The heaters that are 1 μm thick, deposited on silicon showed less of a hysteresis and were much closer to the expected linear I-V measurements.

Two heater thickness have been fabricated: 1 μm and 1200 $\AA$, both on two substrates types: glass and silicon. The general trend of the current-voltage (I-V) curves are that thicker (1 μm) heaters on silicon substrates have more ideal electrical properties than that of thinner heaters (1200 $\AA$) on silicon and than those heaters (either thickness) deposited on glass substrates. The I-V measurement with the most deviation from the ideal straight line I-V curve are the thin-film heaters.

It seems reasonable to attribute the non-ideal electrical characteristics to uneven heating. As more voltage is dropped across the resistor, the ITO starts to physically heat, as is seen in Figure 5.2 this heating is very apparent. It is well accepted that ITOs electrical conductivity increases with increasing oxygen vacancies and changes in electrical conductivity affect material resistance. It is the author's belief that physio-absorbed H_2O and O_2 on the ITO heater is released as the heater is physically heated. With the lost of the physio-absorbed H_2O and O_2, the ITO becomes more oxygen deficient and hence more conductive. This affect would be less apparent with the thicker ITO heaters because the physio-absorbed H_2O and

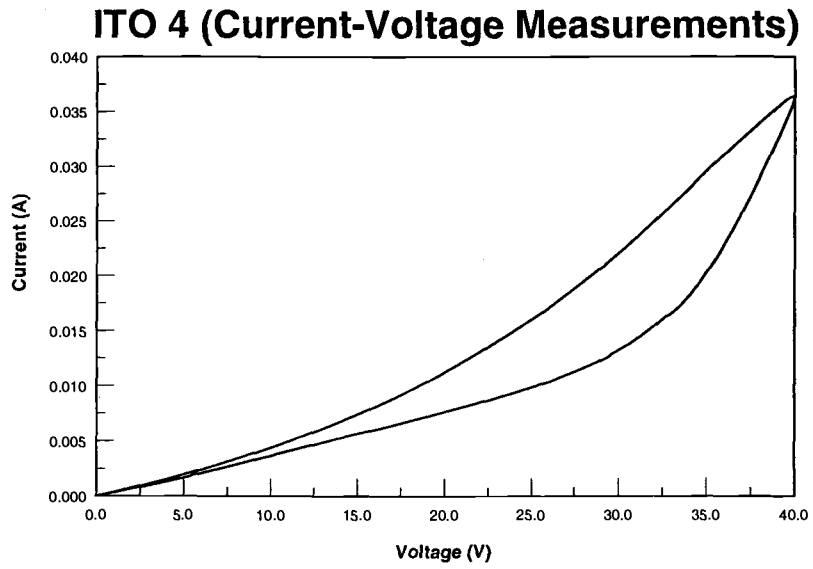

Figure 5.2: Current-Voltage measurements of 1200 $\AA$ thick ITO thin-film heater on 1737 glass substrate. The bottom line is the first pass (increasing Voltage) of the I-V measurement and the top line is the second pass (decreasing Voltage) of the I-V measurement.

O_2 is only at the surface and the surface area of the ITO heaters is essentially the same, regardless of the heater thickness. Another contributing factor are the ITO carriers dependance on thermal energy. As the temperature of the ITO increases, a larger number of the valence band electrons have enough energy due to thermal excitation to transition from the valence band to the conduction band. This also effectively increases the ITO conductivity.

In figure 5.4 an infrared image of a 1 μm thick ITO heater, deposited on a silicon substrate can be seen. Uneven heating is seen across the ITO heater. The very light spots, surrounded by dark is a contrast of the heat locally. Oval rings can also be seen around the heater, the substrate is allowing heat to be transferred away from the heater. The uneven heating also explains the differences seen with the glass versus silicon substrates. ITO heaters deposited on both substrates will have uneven heating; however, the silicon substrate will allow the heat produced by the ITO heater to be pulled away. On the other hand, the glass substrate will hold the heat locally, magnifying the localized heating and ultimately affecting control of power dissipation.

Power = Current * Voltage = Current^2 * Resistance

Figure 5.3 shows the power versus current of a 1200 $\AA$ thick ITO thin-film heater on 1737 glass substrate. Measurements of the heaters have been done with an IR camera. The heaters produced enough heating to be useful for the lithium-bromide separation experiments. The measurement set-up to measure the current and voltage of the devices is limited to a maximum of 40 V; otherwise, measurements at higher voltages would have been shown to demonstrate higher power dissipation of the heaters. An external power supply and a digital multi-meter (DMM) measured the required 5 Watts of dissipated power with a 1 μm thick ITO heater, deposited on 1737 glass, to demonstrate that the ITO heaters did indeed meet the 5 Watt power

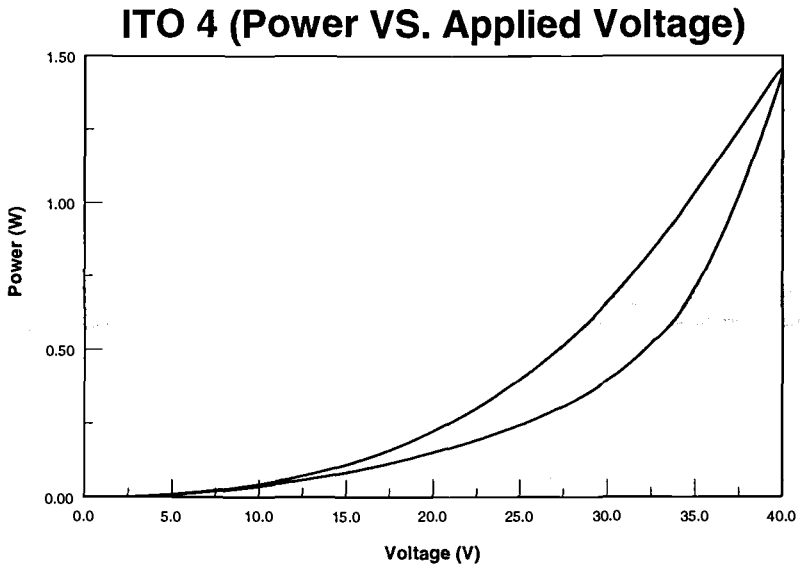

Figure 5.3: Power-Voltage measurements of 1200 $\AA$ thick ITO thin-film heater on 1737 glass substrate. The bottom line is the first pass (increasing Voltage) of the P-V measurement and the top line is the second pass (decreasing Voltage) of the P-V measurement.

requirements. All numbers and graphs of power have been taken as the current times the voltage.

5.3 ITO Heating Effects

Figure 5.4 is a thermal image of a transparent Indium Tin Oxide (ITO) thin-film heater (1 μm thick) deposited on a silicon substrate. The ITO heater is 250 μm x 5 mm. Figure 5.4 represents a differential intensity map of temperature between the heated and unheated images are recorded using an infrared microscopic thermal imaging system. The ITO indeed meets the requirements; however, the bright areas

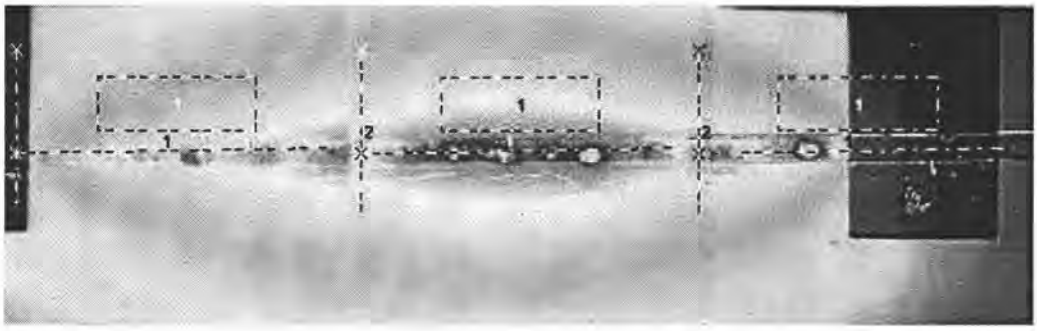

Figure 5.4: Transparent Indium Tin Oxide (ITO) thin film heater shown with Infared (IR) Imaging to show relative heating. ITO 1 μm thick on silicon substate.

or "hot spots" seen are of some concern. These areas are more likely to burn out, causing device failure. Even though this device and others tested did not fail initially, repeated use could lead to device failure. With the silicon substrates, heat is conducted away from the heater more quickly, reducing but not eliminating localized heating. Further lifetime testing is required.

5.4 Conclusions

ITO works adequately as a transparent heater for the visible range through the MWIR range (450 nm - 5 μm), absorbing strongly in the 1 - 1.5 μm range. Initial testing of the heaters shows that the heater is controllably heated and can achieve the power output required. If lower absorption is needed or lower power is required, several other materials look nearly as promising as ITO, although heaters thickness or width will have to increase due to other TCO's increased resistance. The same process to fabricate the ITO heaters has been used to make Nichrome heaters. If transparency is not important and/or higher conductivity is required, metals may also be fabricated with the same process.

5.5 Future Work

With the proper alignment system now in place, the capture dots can be reproduced reliably, using either chrome on quartz or ink on mylar. If the capture dots or a similar technology required thicker deposition a multi-layer spin coating process of the SPR 220 line has been developed for two and three layers thick, corresponding to 10.5 and 15 μm thick patterns, post develop.

Also, with the ongoing transparent conductive oxide research at Oregon State and Hewlett-Packard, a totally transparent inductor should and could be pursued. The first layer has already been completed successful, by RF sputtering ITO onto 1737 glass with layer 1 coils patterned via SPR 220 (7 μm). The same lift-off process is used for the ITO coils as is used to pattern the ITO heaters.

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APPENDICES

A. RIE: REACTIVE ION ETCH INSTRUCTIONS

Reactive Ion Etcher (RIE) Instruction Sheet:

1) TURN ON SCRUBBER!!!

2) TURN ON SCRUBBER!!!

3) TURN ON SCRUBBER!!!

4) After turning on the scrubber that will carry away the nasty chemicals used to etch turn on the 'POWER' button on the bench top.

5) Press the 'POWER' button on the PC. It will take a minute to boot up if and error occurs while booting up the PC press 'RESTART'.

6) After the PC has finished booting up the C prompt will be for a command, type in 'WIN'. This command will bring up window version 3.1.

7) Click on the 'PROGRAM MANAGER'

8) Click on 'MAIN'

9) Click on the 'SYSTEM'

10) A dialog box should now appear requesting a user name and password. The default user name and password are '3333'. If this doesn't work the user name and password has been changed. Request user name and password from the all knowledgeable Chris Tasker.

11) A new window appears. On the bottom of the screen will be several commands, click on 'STANDBY'.

12) Now go to the 'UTILITIES' menu and select 'VENT'. The calibration for what the RIE believes to be atmosphere has drifted, until it is re-calibrated watch the chamber to see when the seal physical is broken. When you can see that the chamber is vented to back into the 'UTILITIES' menu and select 'CLOSE GATES'.

13) Open RIE chamber and place in sample(s).

14) Go back into 'UTILITIES' menu and select 'PUMP CHAMBER'. IMPORTANT: You must physical hold down chamber during start of pumping the chamber down. You will hear a distinct beep sound, this is the RIE telling you that the roughing value is being closed and the throttle is being opened.

15) AGAIN CHECK THAT SCRUBBER IS ON AND OPERATING PROPERLY BEFORE PROCESSING! If you are not sure what proper operation looks like check with Chris Tasker or senior graduate student familiar with RIE processing.

16) Go in to 'PROCESS' menu and select load, next select program to load.

17) After loading desired program select 'READY' at the bottom of the screen, in the process dialog box.

18) Physically open gas values used in your process.

19) Select 'RUN' at the bottom of the screen, in the process dialog box.

20) Wait for run to complete. You can see where in the run the RIE is at by viewing the PC screen.

21) At the end of the run the 'AUTOMATIC PURGE' should run, when the RIE is finished purging a dialog box titled appropriately 'PROCESS COMPLETE' appears. Press 'OK' in the 'PROCESS COMPLETE' dialog box.

22) Remove sample(s)

23) Go back into the 'ULTILITIES' menu and select 'CLOSED GATES' to end the venting.

B. STEP-BY-STEP CAPTURE DOT FABRICATION STEPS

The layers in the manufacture process are as follows: Start with clean Si wafer or glass 2 by 2 substrate. Next to each process or group of process steps (in the parenthesis) the highest probability of that specific process step completing successfully is provided. The best overall success rate of completing a working device is: 4.4 percent. This number is obtained by multiplying all the process step probabilities together. The probability is slightly skewed because some of the process steps are easily recovered. If an alignment for in a photoresist layer goes poorly the photolithography step can be redone.

- Thermal SiO_2 passivation layer (Si wafer only): (99%)
- Sputter Ti (200A), Sputter Cu (1500A): (99%)
- Spin on PR SPR-220 (7.0 μm): (95%)
- Soft bake PR (115 C for 2 minutes): (99%)
- Expose to i-line UV wavelength: (99%)
- Develop photoresist pattern in corresponding MF-702 developer: (95%)
- Electroplate layer 1 pattern (5 um): (50%)
- Remove photoresist with acetone, AMD clean with Nitrogen dry: (99%)
- (Coil Isolation) Etch back Cu seed layer and Ti seed layer: (99%)
- Ion beam sputter SiO_2 or alternatively PECVD SiO_2 5000 angstroms: (50%)
- Spin coat SPR-220 1.2 μm photoresist: (99%)
- Align photolithography layer 2 to underlying cross hairs in first electroplated layer and expose to i-line UV light: (75%)
- Develop: (99%)
- RIE SiO2 vias to underlying coils: (99%)

- Ash photoresist, AMD clean substrate: (95%)
- Ion beam sputter Ti (200A): (99%)
- Ion beam sputter Cu (1500A): (99%)
- Spin on SPR-220 (7um), Soft bake PR (115 Co): (95%)
- Expose i-line photoresist to UV wavelength: (99%)
- Electroplate layer 2 pattern (5 um): (75%)
- Remove photoresist with acetone, AMD clean with Nitrogen dry: (99%)
- (Structure Isolation) Etch back Cu seed layer and Ti seed layer: (95%)
- Ion beam sputter SiO_2 or alternatively PECVD SiO_2 5000 angstroms: (50%)
- Spin coat SPR-220 1.2 μm photoresist: (99%)
- RIE SiO_2: (95%)
- AMD clean and test: (99%)

These process steps yield 18 capture dots on a single slide. The total success is 4.4 percent, a yield this high was never achieved. During much of the capture dot development various vacuum equipment would be down, and capture dots could not be completed and waited several weeks to continue processing. The original alignment system used to develop the capture dots was not designed for alignment of critical dimensions as small as 10 μm, making device alignment hit or miss.

C. STEP-BY-STEP THIN-FILM TRANSPARENT CONDUCTIVE OXIDE MICRO HEATERS

Below the complete step-by-step list of process steps for the thin-film transparent conductive oxide heater is listed. Next to each process or group of process steps (in the parenthesis') the highest probability of that specific process step completing successfully is provided. The best overall success rate of completing an operating device is 4.5 percent. This number is obtained by multiplying all the process step probabilities together. The probability is slightly skewed because some of the process steps are easily recovered; for example, if an alignment for the contact pad goes poorly the photolithography step can be redone. However, if the ultrasonic lift-off fails, the ITO is etched and the process starts over.

- Ultrasonic clean substrate: (90%)
- AMD clean substrate: (95%)
- Photolithography (spin coating): (95%)
- Alignment and exposure (heater pattern): (50%)
- Pattern development and N_2 dry: (95%)
- Ion Beam Sputter ITO ($\sim$1200 $\AA$): (95%)
- Ultrasonic acetone bath (lift-off): (35%)
- Copper pad evaporation: (95%)
- PECVD passivation: (90%)
- Photolithography (spin coating): (95%)
- Alignment and exposure (contact pads): (95%)
- Pattern development and N_2 dry: (95%)
- SiO_2 etch: (50%)

- AMD clean substrate: (95%)

These process steps yield a working heater for use in lithium bromide separation experiments. NiCr heaters have also been deposited in place of the ITO, forming a NiCr heater.