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Title:
Design and Analysis Techniques for Nano-Joule ADCs and Sampling Linearity

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Terri S. Fiez

Two aspects of ADC system performance are addressed in this work. First, the combination of the ADC and its associated reference are co-designed for an energy constrained remote sensing system. Second, sampling linearity is mathematically analyzed as a function of frequency to provide enhanced understanding into an ADC's requisite sampling network.
Low energy analog design techniques for emerging systems powered by energy scavenging are demonstrated in the context of an analog-to-digital converter system. It is composed of a variable gain sample-and-hold amplifier, a low voltage reference, a 1.5 bit per stage 9-b cyclic ADC, clock generation, reference buffers, and control logic. A novel Class-AB current mirror amplifier together with correlated level shifting enable wide swing and enhanced gain operation at low supply voltages while reducing current draw. The use of subthreshold

MOSFETs instead of bipolar junction transistors allows the use of traditional bandgap circuit techniques to be employed for a 530 mV reference that is less than a diode voltage drop. Operating from a 750 mV supply voltage and 20.48 kSPS, the ADC and reference consume 9.5μA and 1.5μA, respectively. The measured 7.9-bit ENOB results in an FoM of 2.24 pJ/step. The total energy consumption is 535 pJ per conversion for the entire system.

A novel model predicts tracking nonlinearity (NL) in the form of harmonic distortion (HD) for weakly NL (i.e. SFDR>30dBc) first order open-loop sampling circuits. The mechanisms for the NL are exponential settling, amplitude modulation, phase modulation and discrete-time modulation. The model demonstrates that HD typically increases at 20 dB per decade over most standard operating ranges and is a function of input frequency, sampling bandwidth, input amplitude, the sample rate and component nonlinearity. Application of the model is reduced to the equivalent of frequency-independent nonlinearity analysis over this range, requiring only a Taylor series expansion of the NL time constant. Design insight is given for common MOS switch types, revealing a high correlation between HD and bandwidth. The first method to quantify the trade-off between thermal noise (SNR) and linearity (SFDR) for sampling circuits is presented. Measured HD2, HD3, HD4, and HD5 versus frequency at multiple sample rates of a Sample and Hold test chip fabricated in a 0.25μm 1P5M CMOS process and Spectre simulation results support the findings. The results broadly apply to switched capacitor circuits in general and sampling circuits specifically, regardless of technology.

Design and Analysis Techniques for Nano-Joule ADCs and Sampling Linearity

by

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APPROVED:

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Dean of the Graduate School

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Thomas Brown, Author

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Chapter 1 – Introduction and Objectives

1.1 Overview

Analog-to-digital converters (ADC) are an essential part of modern digital systems because they translate the physical, real world, analog signals into quantized form to enable storage, processing and communication digitally. Various aspects of the ADC directly impact the performance of the overall system. These include speed, power, resolution, accuracy, and linearity. Two different aspects of ADC systems are considered in this work. First, the combination of an ultra-low-power ADC and its requisite reference voltage for passively powered sensor nodes is considered. The objective is the simultaneous reduction of both power and energy consumption. The second aspect considered is a detailed mathematical analysis into frequency-dependent sampling linearity of an ADC's input network. This is particularly important for high-speed applications in communication systems. The result of the design and analysis techniques introduced in this work provides design intuition and results in optimized ADC performance.

1.2 ADC Systems for Nano-Joule Sensing

Applications for low-resolution, ultra-low-power analog-to-digital converters have arisen in battery-free systems for sensing and measurement. These systems must

be able to accurately measure, collect, process, store, transmit and receive data. Research and product development are presently being conducted for applications such as Smart Dust [1], tire-pressure monitoring [2] and wireless sensor networks [3, 4]. Moreover, many medical-monitoring applications with similar functionality are possible [5, 6]. These battery-free systems derive power from energy scavenging from the environment and provide storage for use on demand. Possible energy sources include solar, kinetic (e.g., a rotating tire) and electro-magnetic (e.g., radio frequency (RF) carriers) [7, 8]. Because the energy accumulation can currently and for the foreseeable future only provide limited reserves, power consumption is the most critical aspect in the design of these systems. Moreover, the power/energy budget is at least an order of magnitude more restrictive than that of traditional battery powered electronics. Consequently, this directly affects all aspects of design, from the system level all the way down to transistor sizing, all of which must primarily be geared toward power savings. To do so, both speed and resolution must be carefully considered. Thus the focus of this work is to develop low to medium resolution (6-9b) ADCs for low speed (<100 kSPS) with a reduction of power/energy consumption by an order of magnitude over the current state of the art [1, 9].

1.2.1 Intended Application

This work focuses on an ADCs for a proposed wireless temperature sensor network [10]. The network will be deployment in a watershed in the H.J. Andrews

Long-term Ecological Research Site in the Oregon Cascade Mountains and log temperature fluctuations with high temporal and spacial resolution. The purpose is to enable better understanding of cold-air drainage which will enhance knowledge of ecological processes in watersheds. Figure 1.1 illustrates the planned deployment. The sensors, approximately 0.5m off the ground, will be spaced 10m apart in a radial pattern about the three 30m tall base-stations (BS). Data is to be transmitted in a peer-to-peer fashion radially toward the BS, with sensors up to 50m away from each BS.

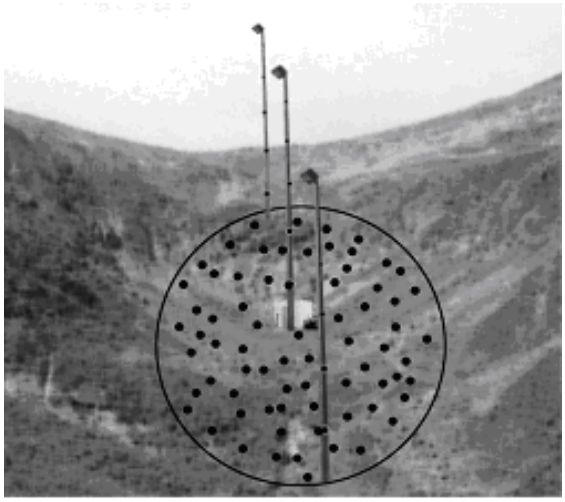


Figure 1.1: Proposed passive sensor network.

The passively powered peer-to-peer network operates in the 902-928 MHz license-free ISM spectrum using differentially-coherent binary phase-shift keying (DBPSK) direct-sequence spread spectrum (DSSS) with time division multiple access (TDMA). A total of 1024 time slots will be allocated over a five minute span. Each sensor will have to wake up to measure temperature, compress and store the data, trans-

mit data to its closest (inner) neighbor as well as receive data from its closest (outer) neighbor. Figure 1.2 shows the block diagram of the sensor node. There are two ADCs, one to measure temperature and another to quantize the RF receive channel for demodulation and processing. Sufficient signal-to-noise-and-distortion ratio (SNDR) in the receive path has been determined to be 30 dB, translating to a 5-6b converter with an effective number of bits (ENOB) of at least 4.69b. With a chip rate of 4.096 MCPS, the RF ADC must have 3-4 times the bandwidth of the chip rate for digital demodulation, necessitating a sample rate in the range of 24.6 MSPS to 32.8 MSPS. The sensor ADC must be able to resolve temperature to $\pm 0.5^{o}$C over a range from -10^{o}C to +40^{o}C, implying a 7-8b ADC; samples are to be taken once during each five minute time slot, leaving the choice of the sampling rate as an additional degree of freedom in the design.

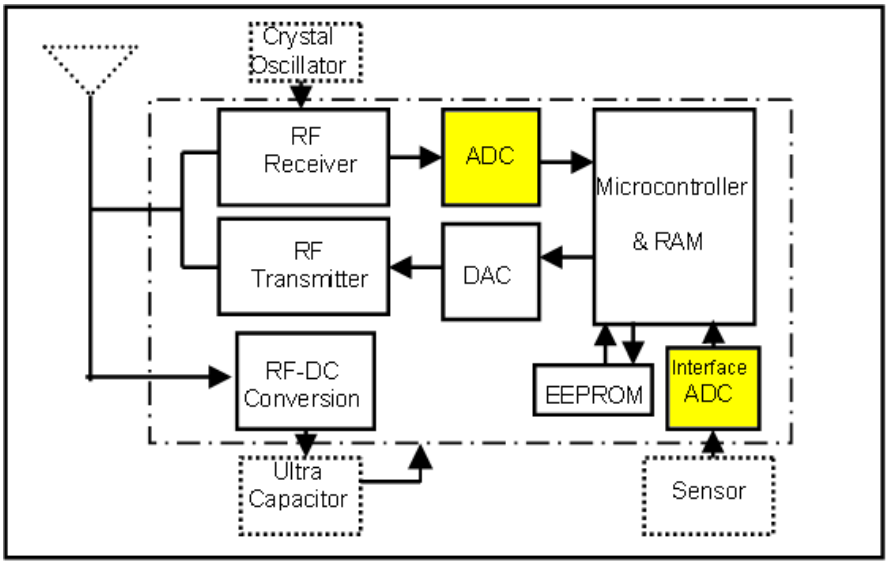


Figure 1.2: Sensor node block diagram.

In order to comprehend just how little power can be dissipated in this application, it is insightful to know how much energy each sensor will accumulate over time. For a single 5 MHz channel in the 902-928 MHz license-free ISM spectrum, the maximum radiated power level is 1W peak [11]; a carrier from each BS will power the sensors from this source. Using Hata's path loss model [12], the received power level may be estimated[1]. Presuming conversion efficiency of 50%, the energy absorbed over the 5 minute span is graphed in Figure 1.3. A low-power (e.g., 1 mW) ADC would burn 300 mJ of energy if run continuously over the same 5 minute span. Yet the closest sensor would accumulate only approximately 1.6 mJ of energy. The factor of 187.5 difference underlies the need for ultra-low-power ADCs, as they may only use a fraction of the energy budget.

1.2.2 General Low-Power ADC Considerations

Common to all low-power ADC design, regardless of where the particular design fits in the speed/power/accuracy space, there are general practices to adhere to. First, the number of active elements (e.g., amplifiers and comparators) should be minimized because they are the greatest power sinks in ADCs and analog design in general. After reducing the number of active elements, the power consumed by the active elements should be diminished. To do so, capacitance must be minimized; extra capacitance slows down amplifiers, requiring higher bias currents and

[1]It should be noted that this model can at best give the order of magnitude of the received power because it was never intended to work over such short distances (< 200m). More accurate models for this type of environment are not available.

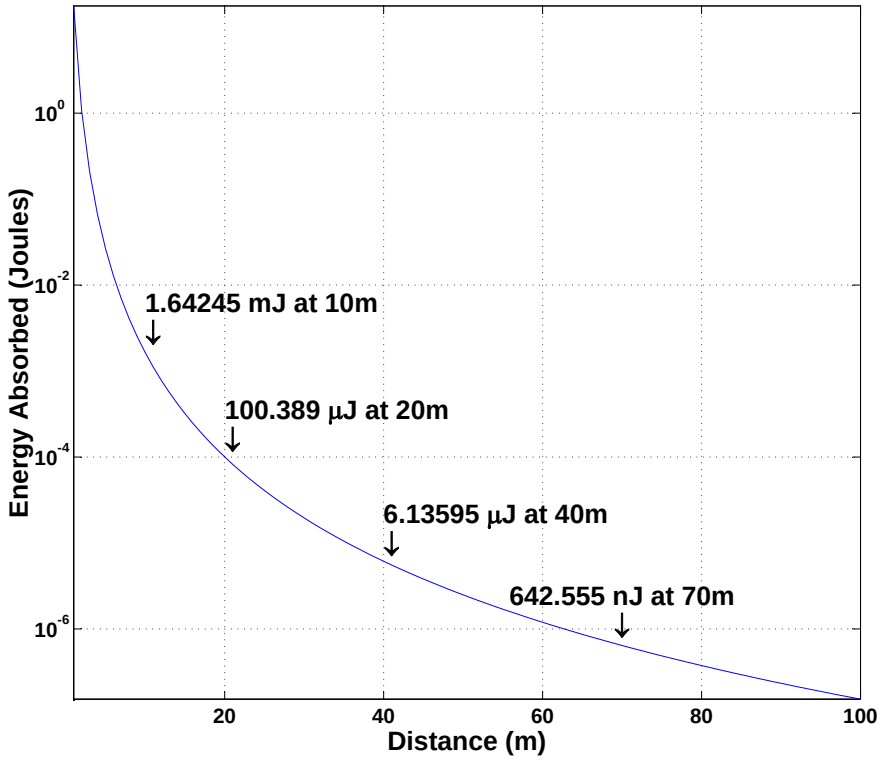


Figure 1.3: Estimated sensor node energy absorbed over a 5 minute duration as a function of distance for a 1W peak (28.5 dBm) spread carrier. 50% conversion efficiency is assumed.

hence power to charge them. The amplifiers may be slowed via either slew limiting or an increased feedback factor. Matching considerations dictated by the converter/stage resolution typically set the lower bound on capacitance. Techniques such as dynamic biasing [13,14] and optimal settling time compensation (i.e. phase margin) [15,16] can be used to diminish the requisite current dissipation in a given application. Moreover, circuit techniques (i.e. architecture or error compensation) that can tolerate less accurate components also lead to reduced power consump-

tion. However, only a fractional improvement is available via optimization, shifting the burden to the system level for large (i.e. an order of magnitude or better) improvements by reducing the required speed and/or resolution.

Over 10 ADCs with power consumption less than 500μW have been reported in the last decade [1, 17–28]. Table 1.1 summarizes their characteristics. Architectures vary from SAR to various forms of $\Delta\Sigma$ modulators and Extended Counting ($\Delta\Sigma$ for MSBs and SAR/algorithmic for LSBs). Additionally, a logarithmic ADC using an integrating (Dual Slope) architecture has also been published [28]. Power dissipations range from just under 1μW to 340μW, with supply voltages from 0.7 V to 3.3 V, resolutions (ENOB) from 7-13b and bandwidths[2] up to 75 kHz. The energy per sample per effective bit ranges from 4.43 pJ/bit to 2.5nJ/bit, with the SAR ADCs outperforming the $\Delta\Sigma$ modulators. This is underscored by the absence of on chip decimation filters for the $\Delta\Sigma$ modulators.

1.2.3 Voltage Reference Power Implications

A reference circuit that is independent of external parameters such as supply voltage and temperature variations is vital to an ADC's performance. Errors in the reference directly lead to errors in the quantized output. For this reason, using supply voltage as a reference [1, 30, 31] is not a robust solution since it is poorly controlled in battery-free systems. Consider that even a 5 % variation in the supply voltage used as a reference limits performance to 4.3 bits. Moreover, the reference

[2] i.e. Effectively half the sample rate of an equivalent Nyquist rate ADC, $F_s/2$.

Table 1.1: Micro-Power ADCs

Ref.	**Power (μW)**	**BW (kHz)**	**ENOB (b)**	**Vdd (V)**	**E/bit* (pJ/b)**	**Process**	**Architecture**
[1]	3.1	50	7.0	1	4.43	0.25μm CMOS	SAR
[17]	40	16	10.01	0.9	124.92	0.5μm CMOS	$\Delta\Sigma$-3, OSR=96
[18]	37.7	10	12.0	0.9	157.08	0.18μm CMOS	$\Delta\Sigma$-2, OSR=200
[19]	60	8	10.34	1	362.71	0.35μm CMOS	$\Delta\Sigma$-3, MASH 2-1, OSR=64
[21]	250	3.906	12.5	2	2560.5	1.0μm CMOS	$\Delta\Sigma$-3, OSR=64
[20]	230	20	12.5	3.3	460.06	1.2μm CMOS	Passive $\Delta\Sigma$-2, OSR=250
[29]	340	8	11.17	1.95	1902.51	1.2μm CMOS	$\Delta\Sigma$-3, OSR=64
[23]	216	24.3	8.68	2.7	512.17	2.0μm CMOS	$\Delta\Sigma$-2, OSR=50
[24]	30	75	8.21	1	24.35	0.18μm CMOS	SAR
[24]	0.85	2.05	6.9	0.5	30.04	0.18μm CMOS	SAR
[26]	135	25	11.34	1.5	238.19	0.5μm CMOS	$\Delta\Sigma$-3, OSR=48
[25]	80	8	10.84	0.7	461.37	0.18μm CMOS	$\Delta\Sigma$-3, OSR=64
[27]	340	25	7.9	1	860.76	1.2μm CMOS	SAR
[22]	150	8	13.0	1.2	721.34	0.8μm CMOS	Extended Counting ($\Delta\Sigma$-1 & SAR)
[28]	3	0.15	8	3	1250	1.5μm BiCMOS	Dual Slope (logarithmic)

* Calculated as Power/2/BW/ENOB

must be able to drive the ADC to meet current draw and settling without a loss in accuracy.

For micro-power ADCs, the power required to generate the reference voltage is significant. Even low power references consume power on the order of 10 to 100 μA [32]. For a 1 V supply, this translates to power consumption of 10 to 100 μW. With a 10 μW ADC, an increase in power consumption by a factor of 2 to 10 results. Following this observation, power saving in the ADC are negated by the reference power consumption. Consequently, micro-power ADC systems require that the ADC and reference voltage be co-designed for the maximum possible power savings. For applications that require battery-free operation, ADC and reference co-design is of vital importance.

1.3 Frequency Dependent Sampling Linearity

The sampling process converts a continuous time signal with a continuous amplitude range into a discrete-time signal with a continuous amplitude range. In other words, it quantizes the input into discrete time steps but leaves the amplitude unchanged. The quality of this process is vital to overall system performance because errors cannot be removed once they occur. ADCs require a high performance sample-and-hold amplifier (SHA) to change a fast moving signal into effectively a DC one that facilitates accurate quantization.

One of the most important characteristics of the sampling process is the linearity in terms of harmonic distortion. This is because harmonic distortion produces spurs in the frequency domain that corrupt the spectrum. Increasing input frequency exacerbates the problem as linearity degrades. In a communication system in particular, these spurs make it impossible to distinguish a small signal in the presence of the nonlinearity of a larger signal. Furthermore, large spurs limit the overall accuracy of the ADC that the SHA precedes in the form of total harmonic distortion (THD). The net effect is degradation of the ADC's signal to noise and distortion ratio (SNDR) and its the effective number of bits (ENOB), a measure of the effective resolution of the SHA and ADC system.

For these reasons, understanding the mechanisms by which a sampling circuit introduces harmonic distortion as a function of the input frequency plays a vital role in improving the performance of communication systems. Improved understanding of nonlinearity mechanism facilitates the transmission of more information

in future communication systems. This work provides an in-depth analysis of the frequency dependent linearity of the sampling circuit.

1.4 Outline of Dissertation

The remainder of this dissertation is as follows: Chapter II analyzes the ultra-low-power/energy sensor ADC. Chapter III derives expressions for sampling circuit harmonic distortion terms as a function of the input frequency and provides design insight into sampling network design considerations. Chapter IV summarizes the findings, drawing conclusions, and points to directions for future research.

Chapter 2 – A nano-Joule Analog-to-Digital Converter for Battery-free Sensing Systems

2.1 Abstract

Low energy analog design techniques for emerging systems powered by energy scavenging are demonstrated in the context of an analog-to-digital converter system. It is composed of a variable gain sample-and-hold amplifier, a low voltage reference, a 1.5 bit per stage 9-b cyclic ADC, clock generation, reference buffers, and control logic. A novel Class-AB current mirror amplifier together with correlated level shifting enable wide swing and enhanced gain operation at low supply voltages while reducing current draw. The use of subthreshold MOSFETs instead of bipolar junction transistors allows the use of traditional bandgap circuit techniques for a 530 mV reference that is less than a diode voltage drop. Operating from a 750 mV supply voltage and 20.48 kSPS, the ADC and reference consume 9.5μA and 1.5μA, respectively. The measured 7.9-bit ENOB results in an FoM of 2.24 pJ/step. The total energy consumption is 535 pJ per conversion for the entire system.

2.2 Introduction

Severely energy limited systems (ELS) present considerable design challenges compared to traditional battery powered applications. Whether passively powered by scavenging energy or running off of a single battery for long periods, ELS remain dormant in long sleep states and only wake up for brief bursts of activity before returning to sleep. In order to maximize performance and functionality, ELS must be optimized to minimize the energy, not power, required to perform any given operation. Moreover, because the peak power available from the energy storage device limits the maximum power available even in a short burst, low overall power draw is also a requirement.

Considerable work has been done to improve the energy efficiency of analog-to-digital converters (ADC) in terms of energy per conversion step [33]. The most energy efficient ADCs are typically low resolution and low speed, consuming primarily dynamic energy [33]. While some reported designs do include the dynamic power drawn from voltage references or the input, they exclude the power required to generate the voltage reference and its associated buffers. At low speeds, where low energy ADCs have very low power consumption, this additional power easily exceeds that of the ADC core [9]. Consequently, for ELS that must generate a reference locally, energy optimization must include these additional blocks.

The goal of this work is to demonstrate core building blocks for signal processing, quantization, and sensing in an energy limited environment. A block diagram of such a system is shown in Fig. 2.1. The objective is to push the limits on power

savings by reducing both the supply voltage and operating current. Simultaneous reduction in the 'on' time also decreases the energy consumption. Included in the prototype design are a subthreshold MOSFET voltage reference, a variable gain preamplifier for external small signal inputs, and a 9 bit ADC core. Systematic circuit optimization enables dramatic improvements in power and energy use without sacrificing precision.

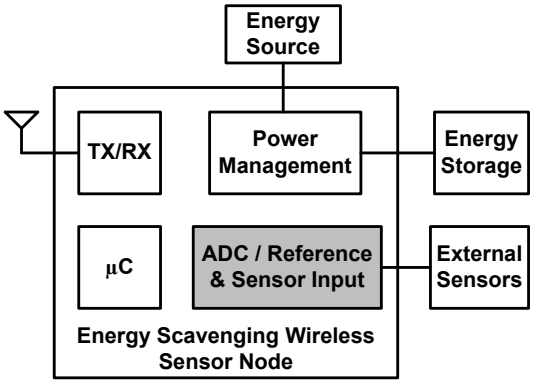


Figure 2.1: A system block diagram of an energy scavenging wireless sensor node.

The remainder of this chapter is organized as follows: Section 2.3 describes the underlying principles to low energy design. Section 2.4 discusses the circuit design details of the prototype energy optimized system. Section 2.5 presents the measured performance of the prototype design. Finally, Section 2.6 summarizes the results and puts them in context compared to competing designs from the literature.

2.3 Low Energy Design Fundamentals

Considerations for low power/energy design of analog circuitry in general and ADCs specifically are discussed. This directly leads to insight into ADC architecture choice, as well as design trade-offs therein. The larger ADC system that includes the reference voltage circuit and its buffer is also included. For low-power ADCs in particular, generating and buffering the reference consumes a nontrivial portion of the power/energy budget.

Low energy design differs from low power design in that the time duration over which a circuit operates also comes into play. Mathematically, the energy consumed may be expressed as

$$E = \int_0^T P dt, \tag{2.1}$$

where E is energy, P is power, and T is the duration of the operation. Assuming constant values that do not vary as a function of time, (2.1) reduces to

$$E = VIT, \tag{2.2}$$

where V is the voltage and I is the current. From (2.2) it is clear that there are three ways to reduce energy consumption: 1) reduce the supply voltage, 2) decrease the current draw, and 3) decrease the 'on' time duration. In the limit that T goes to infinity and the circuit operates continuously, low energy and low power design are equivalent. While it is possible to reduce energy consumption by decreasing

only one of the three, the largest reductions come about through reductions in all three simultaneously. However, reductions in any of these terms entail circuit design trade-offs that limit the extent of the reduction that is attainable without adversely affecting other design requirements. The rest of this section delves into these trade-offs.

2.3.1 Low Voltage

Reductions in the supply voltage provide a means to reduce power and energy at the expense of available headroom. This reduced headroom limits the maximum signal swing possible within the supply rails. Thus, an upper bound is placed upon the signal power. Consequently, for a given signal-to-noise ratio (SNR), the noise floor must be lowered at the expense of higher power consumption in the form of increased current draw. The noise power (V_n^2) for a given SNR and a rail-to-rail input signal bound by the power supply voltage V_{DD} is found by applying the definition of SNR:

$$V_n^2 = \frac{{V_{DD}}^2}{8SNR}. \tag{2.3}$$

At a 1V supply and SNR of 60 dB or equivalently 10 bits, V_n must be less than 353.6 μV. Furthermore, as the required SNR increases, the noise floor requirement becomes even more difficult to meet such that 22.3 μV is required at the 14 bit level. A three decibel improvement in SNR results for a fully-differential implementation since the signal adds directly while uncorrelated noise power combines in a root-sum-square manner.

When considering the thermal noise for a MOSFET in strong inversion, the maximum noise floor can be directly related to the current draw. The thermal noise is expressed as ${V_n}^2 = \frac{8K_BT\Delta f}{3g_m}$, where K_B is the Boltzman's constant, g_m is the device's transconductance, T is the temperature in degrees Kelvin, and Δf is the bandwidth. After substituting $g_m = \sqrt{2\mu C_{OX}\frac{W}{L}I_D}$, where μ, W, L, and C_{OX} are the electron mobility, transistor width, transistor length and oxide capacitance per unit area, respectively, the minimum drain current can be shown to be

$$I_{D,min} = \frac{(64K_BT\Delta f\ SNR)^2}{18\mu C_{OX}\frac{W}{L}V_{DD}^4}. \tag{2.4}$$

From (2.4), a 1 bit improvement, or a factor of 2 increase in SNR directly leads to a four fold increase in the required current.

Aside from SNR considerations, decreases in supply voltage complicate amplifier design. First, reduced headroom limits the ability to cascode transistors as a means to enhance output impedance and thus gain. While a cascode is possible at 1V, at 0.5V there is insufficient headroom. In either case, a wide swing output stage is required. Without a wide swing output stage, signal power must be reduced. Accounting for the range limitations of the output stage, the maximum peak-to-peak swing reduces to $V_{DD} - 2V_{DSAT}$, where V_{DSAT} is the minimum drain-source voltage to keep a MOSFET in saturation. Given this, the maximum root-mean-square noise floor decreases to

$$V_n^2 = \frac{(V_{DD} - 2V_{DSAT})^2}{8SNR}. \tag{2.5}$$

For comparison, the noise floor reduces to 212.1 μV and 13.4 μV for 10 and 14 bit systems, respectively, with $V_{DSAT} = 200$ mV and $V_{DD} = 1$V. Because two gain stages are required to meet swing and gain requirements, additional current is drawn in the extra amplifier stages. Moreover, compensation for stable closed loop operation becomes more challenging since the additional poles introduced require higher current draw to push them to higher frequencies. These additional poles close dominant pole reduce the attainable bandwidth.

Dynamic energy due to capacitor charging and discharging decreases with the signal swing. This affects both digital gates and switched capacitor operation. The energy required to switch a capacitance is proportional to the value of the capacitance and the square of the voltage across it

$$E = \frac{1}{2}CV^2, \tag{2.6}$$

where C is the capacitance and V is the switching voltage. Thus decreased voltage directly leads to energy savings proportional to the square of the voltage difference. The switching energy is independent of the time required to charge the capacitance.

2.3.2 Low Current

The second means to reduce energy draw comes about by decreasing current consumption. Paramount in this is decreasing the loading that the active circuitry has to drive. Thus, resistances must be increased to reduce current, while ca-

pacitances decreased to reduce charge. Yet, each comes with design compromises discussed shortly. Furthermore, decreasing current draw in active circuits also increases thermal noise since the transconductance is reduced, thereby increasing the input referred noise.

Large resistances entail large physical areas with small widths that result in poor matching and large parasitic capacitances; the combination of large resistances and capacitances creates low frequency poles that limit the maximum obtainable bandwidth. Larger resistances result in a corresponding increase in thermal noise. Resistances become an issue for reference circuits in particular.

Since capacitors represent the primary loading in switched capacitor circuits, decreased capacitance provides an important means to decrease loading. Smaller capacitance reduces power in that poles are pushed to higher frequencies at a given current, while also increasing amplifier slew rates. The penalty for lower capacitance in switched capacitor circuitry is a degradation in matching and thus accuracy. Calibration may be required if the capacitances are decreased aggressively. However, capacitances can only be decreased to the thermal noise limit imposed by the band limited noise power in terms of K_BT/C.

Another means to reduce the current draw is to increase the current efficiency. Subthreshold biasing accomplishes this by decreasing the current density through increased device size. Significant savings can occur in this manner since the transconductance of a device in the subthreshold regime is proportional to the quiescent current. In traditional strong inversion operation, the transconductance is proportional to the square root of the quiescent current. A doubling of the

transconductance entails a doubling of the current in weak inversion, while strong inversion operation necessitates a quadrupling of the current draw. Consequently, subthreshold operation realizes a factor of two reduction in current for a given transconductance.

However, subthreshold operation does not scale to very high frequencies because the larger physical size of the transistors results in comparatively large parasitic capacitances that decrease bandwidth. At low frequencies, this is not a concern. Subthreshold design also suffers from degraded matching relative to strong inversion because of an increased dependence on a transistor's threshold voltage leading to greater offset voltage and current mirror mismatches.

Significant current reductions occur from decreasing the number of active blocks needed to implement the desired function. Architecture choice and the associated algorithm that the circuit implements directly affect this. For example, a successive approximation ADC has only a single active component in its comparator, whereas a pipeline ADC requires multiple amplifiers and comparators [34]. If both structures are able to meet the design requirements, the successive approximation ADC will do so with a lower current due to the reduced number of active components.

2.3.3 Time Duration

Finally, energy may be saved by reducing the duration that the active circuitry operates. Implicit in this is the assumption that the circuit does not operate

continuously. Thus, the circuit switches between active and sleep states. Assuming that the sleep state is sufficiently long, the duration of operation becomes a vital design parameter in low energy design. As a result, both the speed of operation as well as the latency of the algorithm implemented affect the 'on' time. This presents an opportunity in the form of an extra degree of freedom in the system design. A short duration typically entails a larger 'on' current draw than a longer duration, but lower current draw. Moreover, since speed does not increase linearly with increasing current, an optimum active duration results. However, other design constraints such as accuracy and power must also be balanced.

2.3.4 Accuracy

Another consideration in low energy design is the accuracy required of the overall system and the individual components within it. Higher accuracy requirements directly lead to higher energy consumption because of the inherent speed-accuracy trade-off. In other words, higher accuracy requires larger power consumption due to the need for more complete settling and better matching. Because of this, careful allocation of system requirements to only the absolute minimum level required to implement the desired function becomes of paramount priority.

Quantifying the speed-accuracy-power trade-off is possible by relating the number of time constants needed to meet first-order exponential settling. For a single dominant pole ω_o defined by its reciprocal time constant τ, the resolution in num-

ber of bits N, and the clock period T,

$$\frac{1}{2^{N+1}} > e^{-T/\tau}. \tag{2.7}$$

Substituting $1/\tau = \omega_o = g_m/C = \sqrt{2\mu C_{OX}\frac{W}{L}I_D}/C$ and $T = \frac{1}{2F_{CLK}}$ in (2.7) and solving for the current,

$$I_D > \left(\frac{C}{2(N+1)F_{CLK}\ln(2)}\right)^2 \frac{L}{2\mu C_{OX}W}. \tag{2.8}$$

From (2.8), it is clear that the required current increases quadratically with changes in both the speed of operation and resolution in bits, in addition to the capacitive loading C.

2.4 Circuit Implementation

The design of the sensor ADC for the remote sensing system discussed in Section 1.2 is now discussed. It includes a 9 bit ADC to achieve an 8 bit ENOB, the reference circuitry and all related bias and clocking. Considerations for low-power/energy design discussed in the previous section are applied to the prototype ADC and reference voltage system.

2.4.1 System Architecture

Fig. 2.2 shows the block level diagram of the prototype system. It contains a 9-bit ADC, a variable gain sample-and-hold amplifier (SHA), clock generation, a low-voltage reference, and common-mode drivers. The system operates at supply voltages from 1V down to 650mV. A single 200 kHz clock signal is used to generate full speed non-overlapping clock signals for the reference circuit, while half speed four phase non-overlapping clocks are required to implement correlated level shifting for gain and swing enhancement in the SHA and ADC core. All drivers for the reference and common-mode signals are included on-chip.

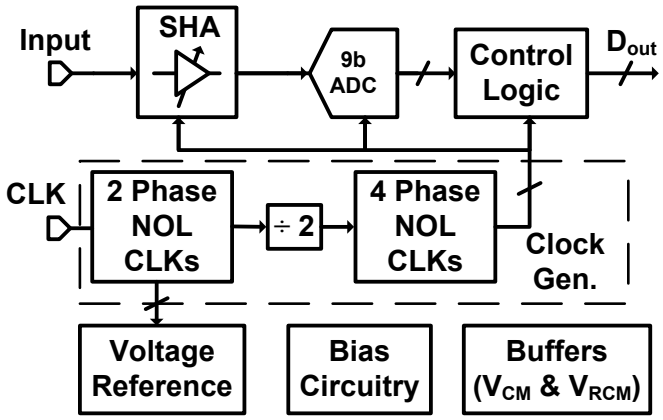


Figure 2.2: The ADC and reference voltage system block diagram.

The system is designed to minimize both the overall energy required for a single conversion as well as the peak power consumption while operating at low supply voltages. A successive approximation ADC architecture has traditionally been the first choice for minimum power consumption due to its single active component and mostly dynamic power consumption. However, its large capacitive load of 2^N

times the unit capacitance, C, presents a very large load for the reference buffer to drive for an N bit conversion. As a result, the burden of reducing the overall system power is merely moved to the reference and drivers in the system as opposed to the ADC core itself.

For this design, a cyclic ADC similar to a 1.5 bit per stage pipeline ADC is chosen. Such a structure reuses the first two stages of a pipeline ADC to save area and power at the expense of a reduced sample rate. This choice drastically reduces the capacitive load that the reference buffer must drive to $2C$, a reduction on the order of 2^{N-1} relative to an N bit SAR ADC. The overall power required for three amplifiers each driving a capacitive load on the order of the unit capacitance C is significantly less power than a single reference driver amplifier driving $2^N C$. A lower bound for the power savings may be approximated by the difference in the capacitance driven for each case. Furthermore, an amplifier is necessary to implement the sample-and-hold amplifier (SHA) for either ADC structure. With the cyclic ADC, one of the two amplifiers may be reused for this functionality without the need for additional hardware as is the case for a SAR ADC.

2.4.2 1.5 b per stage Cyclic ADC

Fig. 2.3(a) shows a block diagram of the cyclic ADC architecture. It is a 1.5 bit per stage structure like that in [35]. When the clock is high, the input is sampled into the first stage. After the sample is taken, the clock goes low and the each stage resolves 1.5 bits per clock cycle and produces a residue voltage for the next

stage to quantize. After a complete conversion, the clock goes high, a new sample is taken and the process is repeated. It does so in a cyclic manner, hence the name. A single 9 bit conversion including the sample-and-hold operation occurs in five clock cycles. Every half clock cycle a single bit is resolved. For a clock rate of 100 kHz, the sample rate is 20 kSPS.

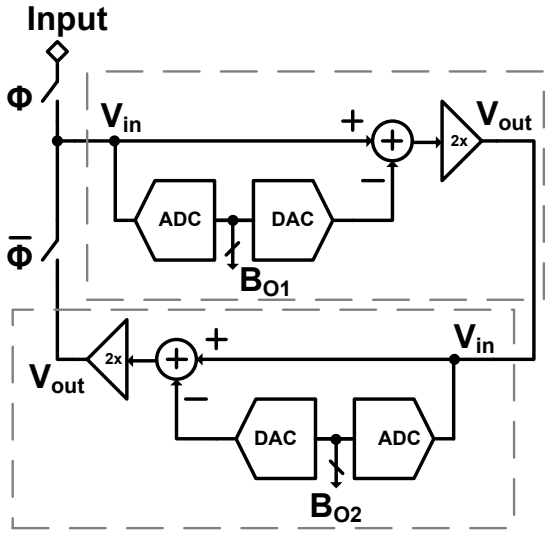
A fundamental advantage of this ADC architecture is its tolerance to relatively large comparator errors due to redundancy and digital error correction. Consequently, the critical component limiting ADC performance is the amplifier in the multiplying digital-to-analog converter (MDAC) used to calculate the residue for the next phase of the conversion. The MDAC converting the first residue must settle to within half an LSB of the overall ADC accuracy. For a 9 bit system, it then follows that roughly 60 dB of open loop gain is necessary for the amplifier.

At low supply voltages simultaneously meeting both the swing and gain requirements while consuming only a few microamps of current is onerous. A switched capacitor technique that simultaneously improves both the limited gain and swing was presented in [36]. This allows a simpler, lower power and lower gain amplifier to be used. Correlated level shifting uses two level shifting capacitors at the output of the amplifier to first estimate the output. Next, the charged capacitors are reused as floating batteries to force the amplifier output to their common-mode level while simultaneously allowing the outputs to swing to nearly the supply rails. The result is both an increase in output swing and the effective gain. Power savings ensue because the simpler amplifier has fewer poles that have to be pushed to high frequency with quiescent current consumption. The cost is two settling

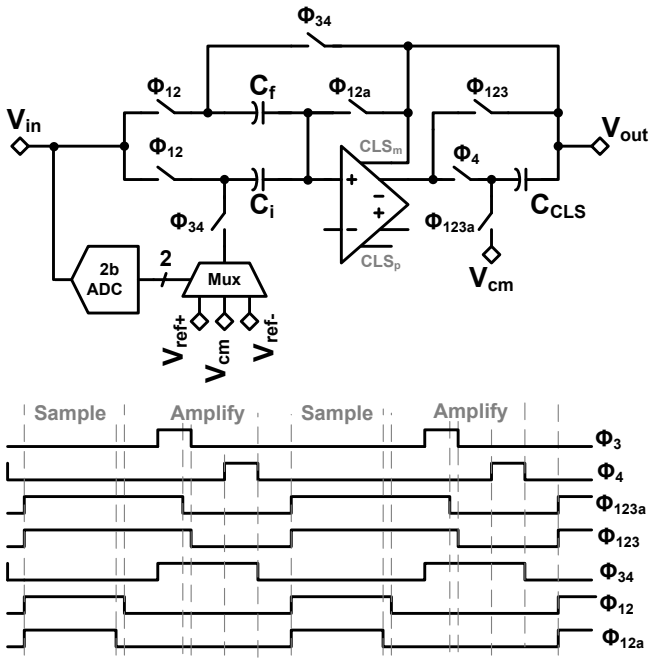
phases that necessitate 4 phase clocking.

Fig. 2.3(b) shows the schematic of a single stage of the 1.5b per stage cyclic ADC along with the clock timing. For simplicity only one polarity of the differential structure is shown. Input sampling occurs during ϕ_{12}. On the falling edge of ϕ_{12a}, a three level comparison is made to determine whether the input V_{in} is within the following ranges: (00) $-V_{ref} < V_{in} < -V_{ref}/4$, (01) $-V_{ref}/4 < V_{in} < V_{ref}/4$, or (10) $V_{ref}/4 < V_{in} < V_{ref}$. Note that correlated double sampling [37] is used to sample the offset voltage of the amplifier during the sample phase (ϕ_{12}) and cancel it on the amplification phase (ϕ_{34}).

During the sample phase of ϕ_{34}, the amplifier forces charge transfer resulting in a residue voltage of $2 \times V_{in} + k \times V_{ref}$, where $k = 1$ for code 00, $k = 0$ for code 01, and $k = -1$ for code 10. The estimation phase of correlated level shifting occurs during ϕ_3 and is exactly the same as the traditional switched capacitor settling phase. Here partial charge transfer from C_i to C_f occurs and the level shifting capacitor C_{CLS} is charged up to an estimate of the output. Next, during ϕ_4, the charged level shifting capacitor acts as a floating battery to keep the amplifier output near the common-mode voltage while permitting the output nodes to swing to the supply rails, thus enhancing swing. Because charge transfer is more complete than for traditional switched capacitor operation [36], the effective amplifier gain is enhanced.



(a) Architecture



(b) Implementation

Figure 2.3: Schematics of (a) the 1.5b per stage cyclic ADC architecture and (b) the switched capacitor implementation of a single stage.

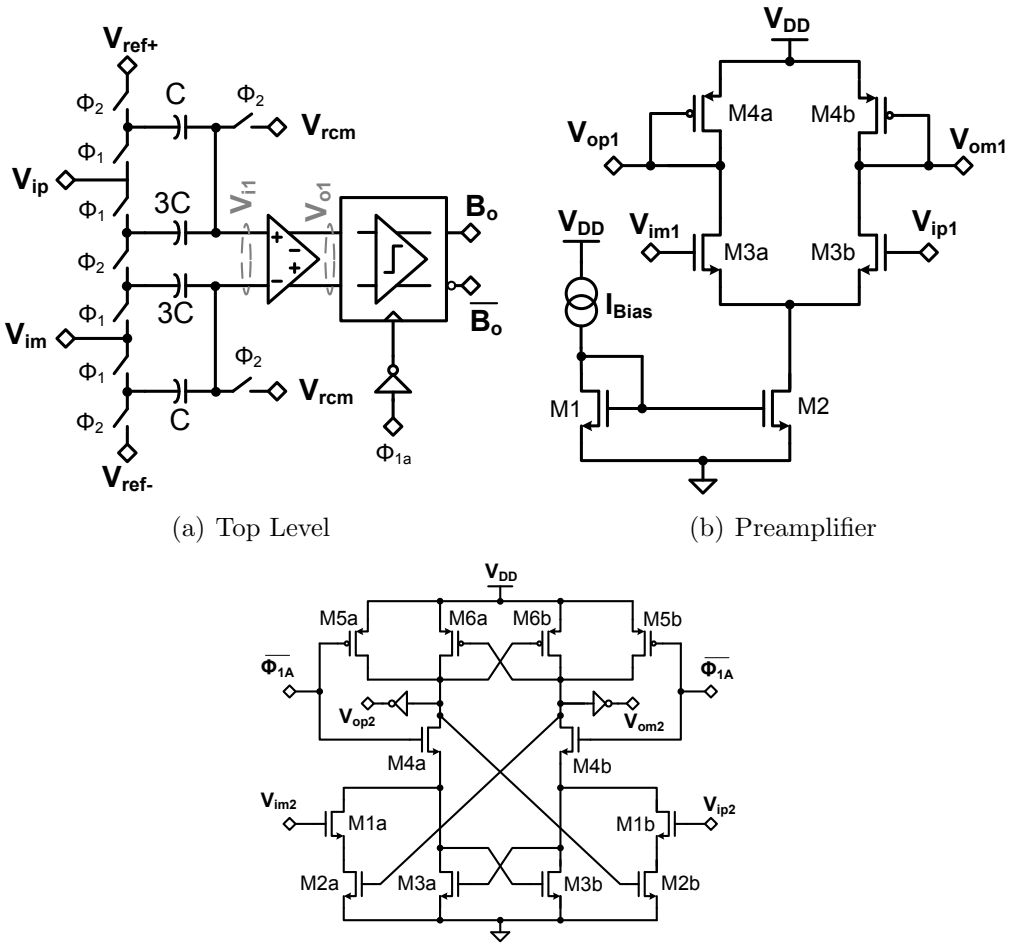
2.4.2.1 Comparator Design

The two bit sub-ADC used in each cyclic stage in Fig. 2.4.1 is composed of two comparators. From these two comparators, the two bit sub-ADC determines if the input with 1) less than $-V_{ref}/4$, 2) between $-V_{ref}/4$ and $V_{ref}/4$, or 3) greater than $-V_{ref}/4$. The design of these comparators is now discussed.

A simplified schematic of one of the two comparators used in each two bit sub-ADC is shown in Fig. 2.4(a) [38]. Switched capacitor charge sharing synthesizes the required $\pm V_{ref}/4$ values while simultaneously subtracting the input voltage such that the polarity of $V_{in} - V_{ref}/4$ is determined.

A preamplifier, shown in Fig. 2.4(b), buffers the input switched capacitor circuitry from charge kickback from the dynamic latch that follows while also reducing the input referred offset do to the latch. Biased in weak inversion, the preamplifier consumes 375nA. Transistors $M4a$ and $M4b$ are sized with much larger lengths than widths to decrease their transconductance relative to the transconductances of $M3a$ and $M3b$ to realize a gain of approximately 5 dB.

The regenerative dynamic latch is the second stage of the comparator, Fig. 2.4(c). It has push-pull positive feedback from $M3a$, $M3b$, $M6a$, and $M6b$ for enhanced gain and fast settling. While the clock ϕ is high, the outputs are reset. On the falling edge of ϕ, a decision is made. Devices $M2a$ and $M2b$ prevent input transistors $M1a$ and $M1b$ from conducting after a decision is made to save power. Not shown, a flip flop latches the settling output a quarter clock cycle after the falling edge of ϕ.



(a) Top Level

(b) Preamplifier

(c) Dynamic Latch

Figure 2.4: Schematics of the comparator (a) switched capacitor top level that uses two phase non-overlapping clocking, (b) the preamplifier, and (c) the second stage dynamic latch.

2.4.2.2 SHA Circuit

Figure 2.5 shows a simplified schematic of the switched capacitor circuit of the input cyclic ADC stage in SHA mode. It operates in SHA mode during the first of the five cycles of a conversion. During the other four states, it reconfigures to the circuit in Fig. 2.3(b). The default unity gain setting sets $G = 0$ (switch open), opening the C_g path. The gain in this mode is $C_i/C_f = 1$ since C_i and C_f are identical. However, in high gain mode, $G = 1$ (switch closed) and the gain becomes $(C_i + C_g)/C_f$, resulting in a boost of 13 dB. As with the ADC operation in Fig. 2.3(b), correlated level shifting enhances both the gain and output swing of the amplifier for enhanced low voltage operation.

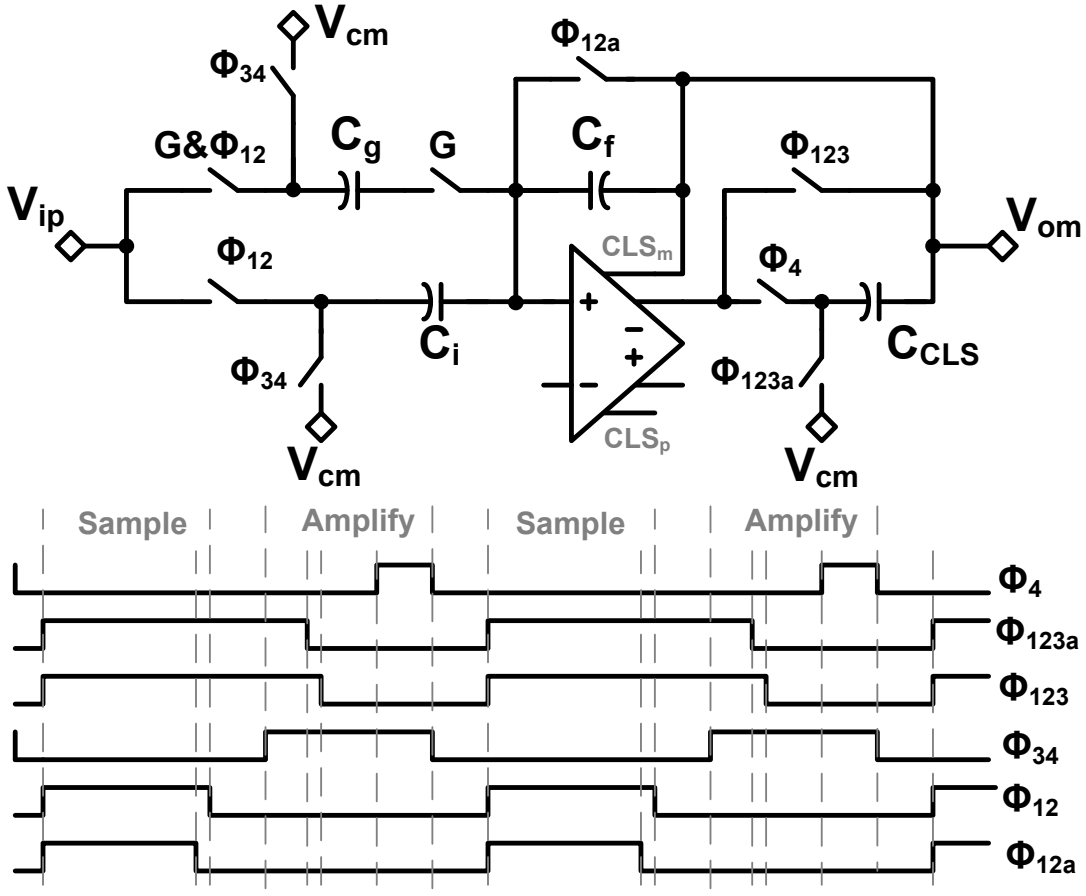


Figure 2.5: Simplified schematic of multi-purpose switched capacitor amplifier that functions as a preamplifer SHA, temperature sensor signal processor and cyclic ADC stage.

2.4.2.3 OTA Design

Fig. 2.6(a) contains a schematic of the OTA used for both stages of the cyclic ADC. It is an enhanced fully differential version of an amplifier first reported in [39], shown in Fig. 2.6(b). The OTA is a fully differential Class-AB current mirror architecture. It eliminates redundant current mirror branches to save power, while providing a means to apply common-mode feedback directly to the output stage. Its extremely large slew rate and current efficiency reduces power by a factor of three to four compared to a traditional miller compensated two-stage amplifier.

A high slew rate is of critical importance for weak inversion operation since the bias currents are in the nano-Ampere range. Even modest capacitive loads of less than a pico-Farad, will result in low slew rates particularly when transistors are biased in weak inversion.

The Class-AB input circuit consists of transistors M_{1a}-M_{1d} and M_{6a}-M_{6b}. Transistors M_{1b} and M_{1c} correspond to those in a traditional differential pair. However, an opposite polarity signal is applied to each from the source terminals of M_{1a} and M_{1d}, driven by the source-follower action from the differential inputs. Therefore, the input signal applied to M_{1b} and M_{1c} is doubled, doubling the transconductance. An additional benefit is that the slew rate scales as the differential input voltage to the fourth order (V_{id}^4) instead of second order (V_{id}^2), reducing the required quiescent current to meet slew rate settling concerns. Together with the current mirror structure, the net result is the elimination of slew rate settling time with nearly the entire settling period now used for small signal exponential settling alone. Because

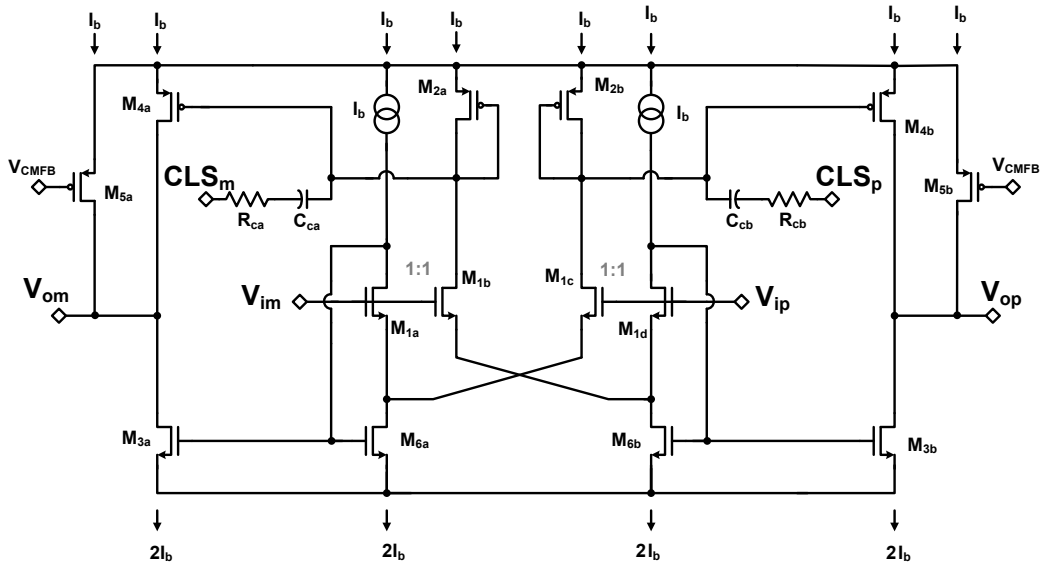
of the small bias currents less than a micro-Ampere, this overcomes a fundamental limitation for weak inversion operation.

Examination of the optimized OTA in Fig. 2.6(a) compared to the conventional version in Fig. 2.6(b) reveals that two current branches consisting of transistors M_{7a}, M_{7b}, M_{8a} and M_{8b} are removed in the optimized version. This simplification is possible because the AC currents that M_{7a}, M_{7b}, M_{8a} and M_{8b} send to the pull-down output transistors M_{3a} and M_{3b} is already present in the bias transistors M_{6a} and M_{6b} of the Class-AB input stage. Simply mirroring the currents from M_{6a} and M_{6b} directly to output stage transistors M_{3a} and M_{3b} eliminates the superfluous current mirrors.

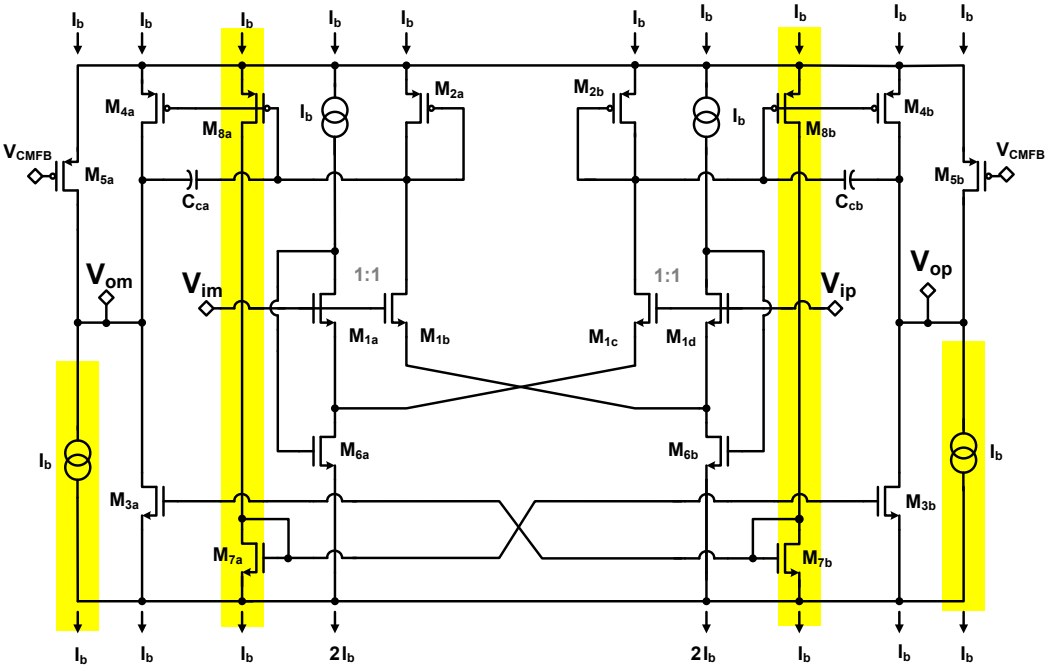
Additionally, since the currents of M_{6a} and M_{6b} contain a DC component that was not in the M_{7a}, M_{7b}, M_{8a} and M_{8b} branches, the DC portion must be subtracted from the output with M_{5a} and M_{5b}. This provides a simple means to apply common-mode feedback directly to the output stage. Typically, applying common-mode feedback directly to the output stage of a current mirror OTA requires additional current branches shunted to the output stage as seen in Fig. 2.6(b) with transistors M_{5a} and M_{5b} and the additional current sources. An enhancement of the output impedance and thus open loop gain results.

Each of the two OTAs in the ADC consume approximately 4.5 μA including biasing. Compensated by Miller capacitors, the open loop gain is estimated to be 40 dB from simulations with a unity gain bandwidth of 3.5 MHz. When used with the correlated level shifting gain and swing enhancement, separate output terminals, CLS_p and CLS_m for the compensation capacitors provide a additional

6 dB gain boost [36].



(a) Optimized



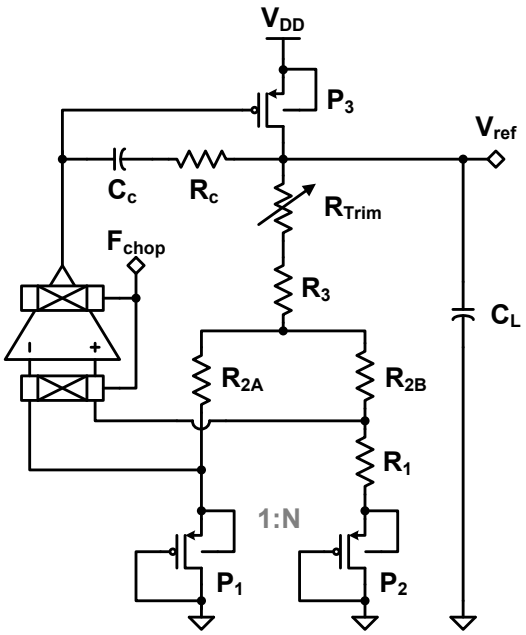
(b) Standard

Figure 2.6: Schematics of (a) the optimized version that saves power by eliminating two current branches and (b) A fully differential version of the class-AB current mirror OTA adapted from [39]. The components eliminated from the optimized version in this work are shaded for clarity.

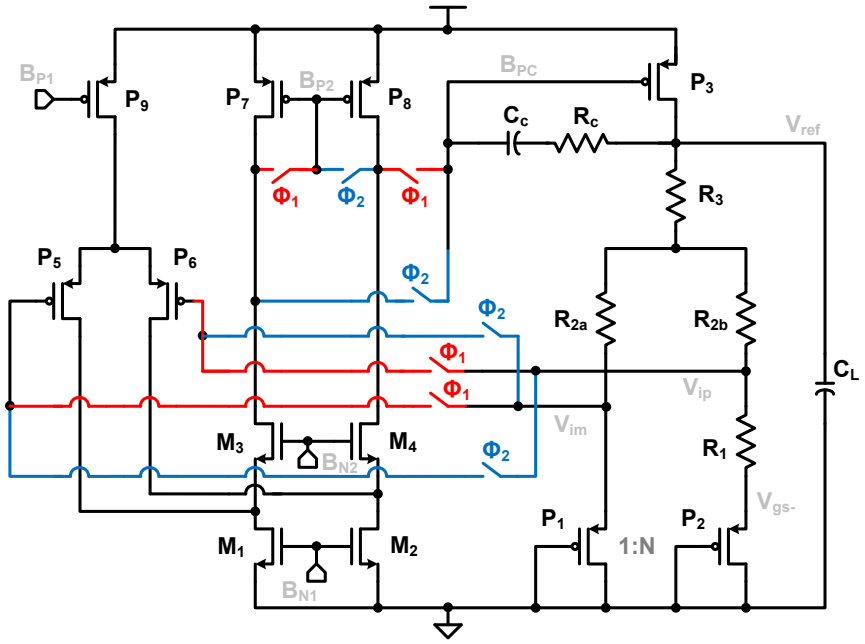
2.4.3 Low Voltage Reference

The minimum supply voltage of 650 mV required for this application precludes the use of a traditional band-gap [40, 41] or even its low voltage derivatives [42] since there is insufficient headroom for a diode drop, let alone a current source to bias it. Consequently, an alternative structure must be employed [9, 42–44].

A simplified schematic of the reference is shown in Fig. 2.7(a). It is a variation of a traditional bandgap reference that replaces the base emitter junction diode sensor with a MOSFET biased in weak inversion [9]. This enables low voltage operation due to the smaller diode drop of the subthreshold MOSFETs while also overcoming the problem posed by small current gain factors (β) of parasitic bipolar transistors in CMOS technologies that result in inaccuracy without compensation due to collector current errors.



(a) Architecture



(b) Chopped OTA

Figure 2.7: (a) Simplified schematic of the low voltage reference circuit. Weak inversion PMOS devices P_1 and P_2 replace the BJTs in a traditional bandgap reference. (b) Simplified schematic of the chopper stabilized OTA.

The reference implements the function:

$$V_{REF} = V_{GS,P1} + n\frac{K_B T}{q} \ln\left(\frac{S1}{S2}\right) \frac{R_2 + 2R_3 + 2R_{Trim}}{R_1}, \tag{2.9}$$

where $V_{GS,P1}$ is the gate-source voltage of P_1, $S1$ and $S2$ are the sizes of the transistors $P1$ and $P2$ such that $S1 = W1/L1$ and $S2 = W2/L2$, and n is the weak inversion slope factor. The negative temperature coefficient of $V_{GS,P1}$ is canceled by the scaled positive temperature coefficient of the difference in gate-source voltage of P_1 and P_2, ΔV_{gs}. A reference voltage of 530 mV results. The proportional-to-absolute-temperature (PTAT) trimming technique from [41] provides a means to improve the accuracy further via resistor R_{Trim} and a single trim at room temperature. A 6-bit trimming code allows the reference voltage to be set within 250 μV.

Since the amplifier loop forces its input terminals to the same potential, the current consumption in both $P1$ and $P2$ is then

$$I_{P1,2} = \frac{\Delta V_{gs}}{R_1}, \tag{2.10}$$

$$\Delta V_{GS} = \frac{nK_B T}{q} \ln\left(\frac{S1}{S2}\right). \tag{2.11}$$

A value of 185 kΩ for $R1$ and $S1/S2 = 4$ set the current to approximately 600 nA in the output stage, a value sufficient to drive the low capacitive loading of the two ADC stages and reference common-mode circuit needed for the sub-ADC comparators. An additional 1.5 μA is used in the amplifier and its bias circuitry

to set total reference current draw at 2.1μA.

Ostensibly transistors with lower threshold voltage might seem advantageous for low voltage operation in the sensor diodes P_1 and P_2. However, smaller threshold voltages for P_1 and P_2 limit the range of values for $V_{gs-P1,P2}$ while remaining safely in weak inversion. At high temperatures with $V_{gs-P1,P2}$ decreasing, drain-source voltages less than approximately 100 mV force the device to stop behaving with an exponential gate-source voltage to drain current relationship that is required for proper circuit operation. To overcome this limitation and extend the temperature range, high voltage I/O transistors with nominal threshold voltages of 0.7 V were used.

Fig. 2.7(b) shows a simplified schematic of the reference amplifier and chopping switches. The amplifier is a folded cascode with PMOS input transistors to accommodate the low input voltage level. A cascode is not used on the supply voltage side of the cascode stage so that low voltage operation is possible. All devices are biased in weak inversion. Chopping [37] reduces errors to to amplifier offset voltages and flicker noise. In order to reduce the output noise of the reference given its low quiescent current and nearly 1.5 $M\Omega$ total resistance, a 30 pF compensation capacitor (C_c) and 0.1uF off-chip bypass capacitor (C_L) are employed.

2.4.4 Common-mode Buffers

Fig. 2.8 shows a schematic of the circuit used to derive the one half V_{DD} reference voltage and buffer to drive the switched capacitor common-mode circuits. It uses

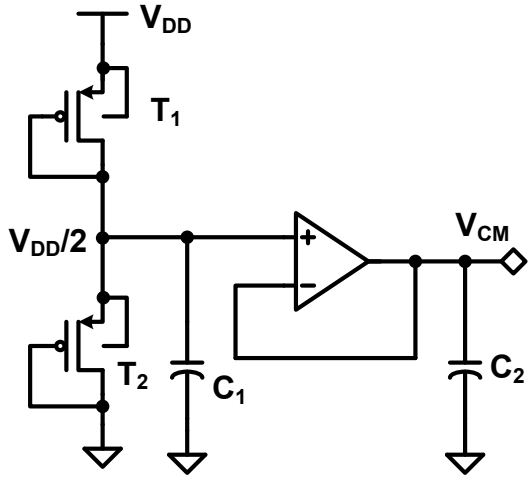


Figure 2.8: Schematic of the common-mode generator and buffer.

diode-tied thick oxide PMOS devices to act as high impedance resistors to split the supply without consuming excess current, avoiding the use of resistors and saving area as well. The amplifier is a PMOS input differential pair with a current mirror active load. A similar circuit is employed to generate the $V_{ref}/2$ signal used in the ADC's comparator signal processing. Less than 1μA total current is consumed in both buffers combined.

2.5 Measurement Results

The prototype integrated circuit was fabricated in an IBM 1P8M CMOS process, Fig. 2.9. The total die area including pads encompasses 2.4 mm x 1.475 mm. The chip operates from supply voltages of 650 mV to 1.0 V. At a 750 mV supply voltage and 204.8 kHz clock rate, the total power consumption of the 9 bit ADC, reference voltage, buffers, logic and bias circuitry is 10.95 μW. Of the total 14.6 μA, 2.1 μA

is used in the reference voltage circuit, 4.5 μA in each of the two amplifiers, with the rest used for buffers, clocks and biasing.

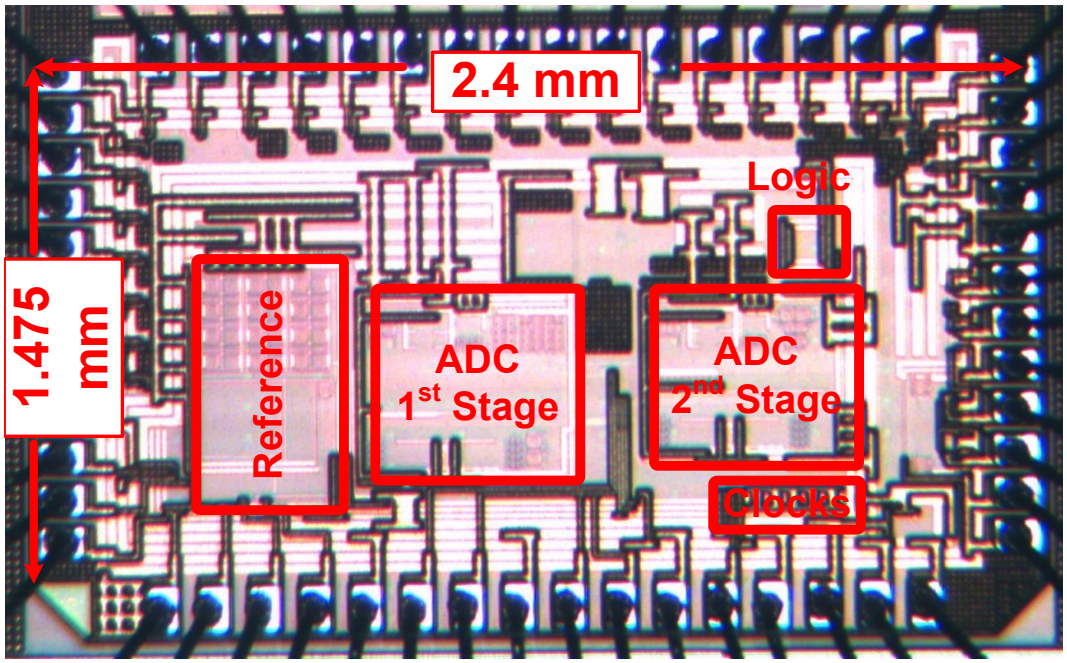


Figure 2.9: Die photo of the 130 nm CMOS 1.475 mm by 2.4 mm integrated circuit.

Fig. 2.10(a) shows a plot of the spectrum of the ADC and reference system at a sample rate of 20.48 kSPS and 750 mV supply voltage. The prototype 9 bit ADC and reference achieve an SNDR of 49.31 dB resulting in an ENOB of 7.9 bits. The SNDR is linearity limited, with a noise floor of -55.6 dBFs for zero input. With an external reference in lieu of the on-chip reference, there is negligible change in performance. With the SHA in high gain mode with a gain of 4.5 at 20.48 kSPS, the measured performance of 46.95 dB SNDR translates to an ENOB of 7.51 bits. In Fig. 2.10(b), the measured DNL and INL are seen to be +0.15/-0.45 LSB and +1.6/-1.5 LSB, respectively.

The measured noise performance of the on-chip reference voltage circuit is shown in Fig. 2.11. With chopping turned on, the flicker noise corner reduces from 500 Hz to within the noise of the Audio Precision used for measurements. Thermal noise is below the Audio Precision noise floor.

A performance summary and a comparison with state-of-the-art low power ADCs that include the reference circuit [1,9] is seen in Table 2.1. While [9] includes an on-chip reference that consumes 11μW, [1] makes use of the supply voltage to save power. However, even a 5% variation in the supply voltage limits ADC performance to 4.3 bits. Comparatively, the reference in this work consumes only 1.5μW, a seven fold improvement compared to [9] while working in a system that has three additional bits of resolution. The 35% overall power reduction and three additional bits of resolution compared to [9] underscore the effectiveness of the design techniques employed in this work. A highly digital flash ADC is presented in [45] demonstrates an alternative approach, but with 5.56b ENOB. In [46] a reconfigurable SAR ADC acheives very low power consumption and high energy efficiency, but requires an externally scaled supply voltage, an externally generated reference, and an external reference buffer.

Additional perspective into the effectiveness of the power reduction techniques in this work is seen by plotting SNDR versus power consumption. Fig. 2.12 plots this for this work and ADCs from ISSCC and SVLSI from 1997-2010 [33]. The power consumption of the ADC and reference combined for this work is less than the total power consumption for all but two ADCs [30, 31]. However both [30] and [31] use the supply voltage as the reference; this is not a practical solution

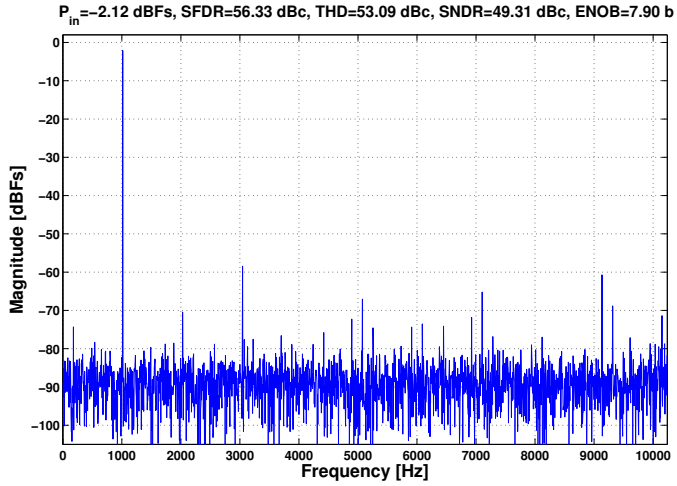
Table 2.1: Performance summary and comparison table of low power ADCs with and without on-chip reference voltage generation.

Reference	V_{DD} **[V]**	V_{ref} **[mV]**	**Power** [μ**W**]	**Ref. Power** [μ**W**]	**Fs** [**S/s**]	**Resolution** [**bits**]	**ENOB** [**bits**]	**FoM** [**pJ/step**]	**Technology** [**nm**]
Gambini (JSSC 11/2007)	0.5	260	17	11	1.5 M	6	5.07	0.5	90
Scott (JSSC 7/2003)	1.4	V_{DD}	4.2	n/a	100 k	8	7	0.24	250
Daly (JSSC 11/2009)	0.4	n/a	2.84	n/a	400 k	6	5.56	0.15	180
Yip (ISSCC 2/2011)	0.55	n/a	0.21	n/a	20 k	10	8.84	0.022	65
This Work (SHA Gain=1)	0.75	530	10.95	1.5	20.48 k	9	7.9	2.4	130
This Work (SHA Gain=4.5)	0.75	530	10.95	1.5	20.48 k	9	7.5	3.2	130

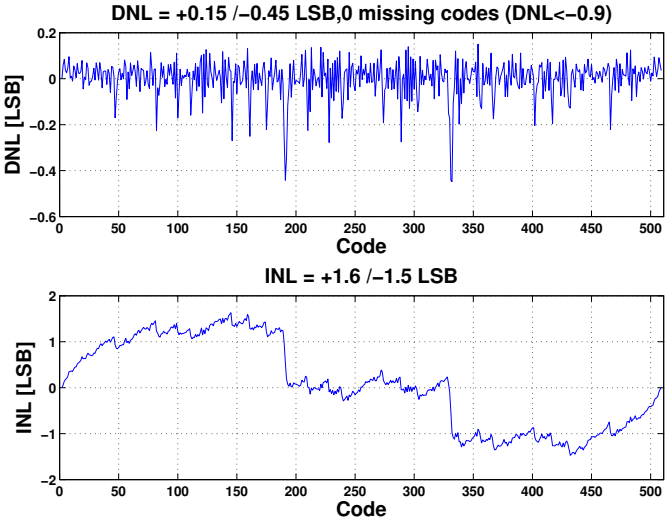
because even a low supply variation of 5% limits performance to 4.3 bits. Moreover, precision supply regulation consumes a significant amount of power for micro-watt systems just as a reference circuit does. Even so, the difference in power consumption is less than 10μW.

2.6 Conclusion

A 750 mV, 9 bit ADC including an on-chip 530 mV reference for remote sensing applications is presented. The system is optimized for energy minimization including subthreshold operation, a novel fully differential Class-AB current mirror OTA, and a low voltage reference. The measured performance 7.9 bit ENOB represents a 2.83 bit or equivalently a 17 dB improvement compared to prior low energy ADC and reference system performance.



(a) FFT



(b) DNL / INL

Figure 2.10: Measured performance of the 9-bit ADC at 750 mV at 20.48 kSPS: (a) spectrum, and (b) DNL and INL.

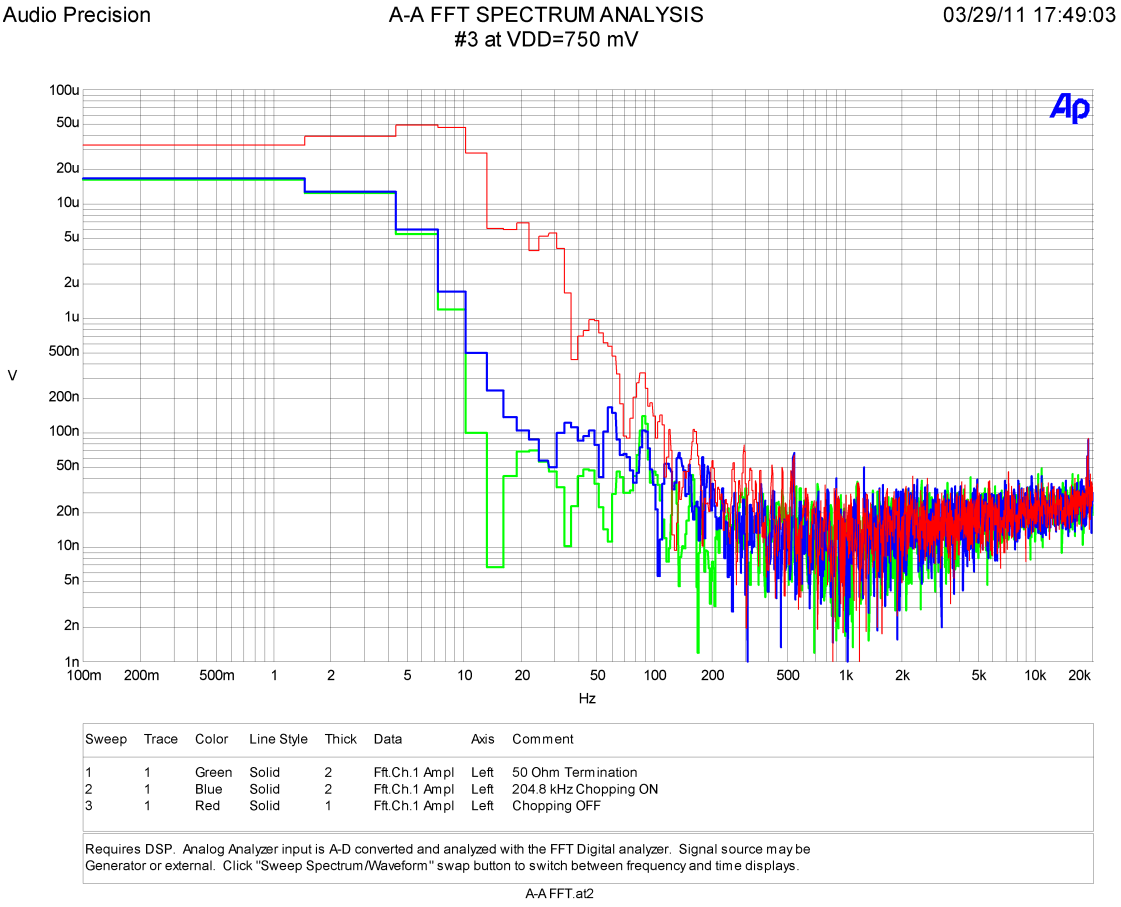


Figure 2.11: Measured performance of the reference voltage at a 750 mV supply: (a) Noise. With chopping on, the reference noise is within the noise floor the the Audio Precision test system. (b) Reference voltage variation versus temperature.

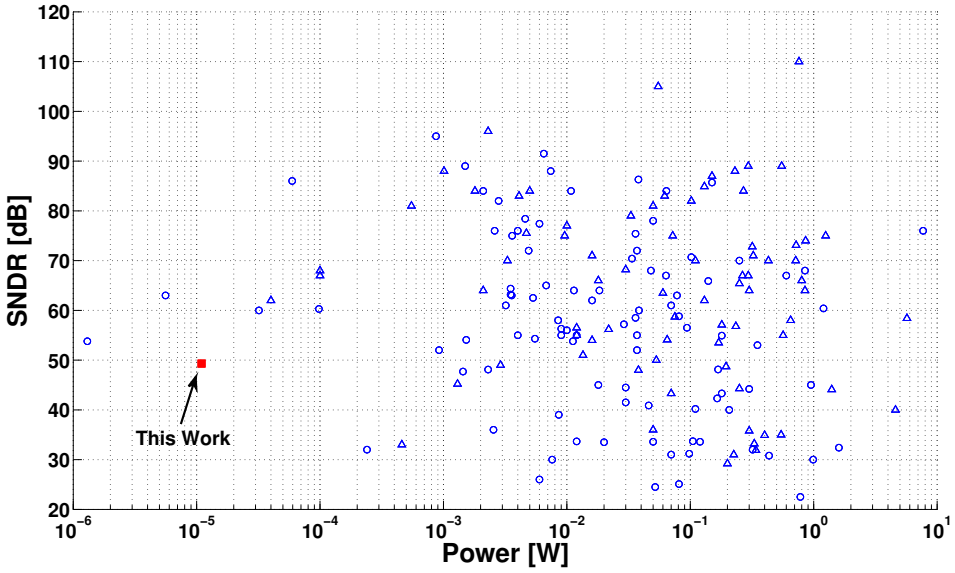


Figure 2.12: Plot of SNDR versus power consumption for ADCs from ISSCC and SVLSI from 1997-2011 [33].

Chapter 3 – Frequency Dependent Sampling Linearity

3.1 Abstract

A novel model predicts tracking nonlinearity (NL) in the form of harmonic distortion (HD) for weakly NL (i.e. SFDR>30dBc) first order open-loop sampling circuits. The mechanisms for the NL are exponential settling, amplitude modulation, phase modulation and discrete-time modulation. The model demonstrates that HD typically increases at 20 dB per decade over most standard operating ranges and is a function of input frequency, sampling bandwidth, input amplitude, the sample rate and component nonlinearity. Application of the model is reduced to the equivalent of frequency-independent nonlinearity analysis over this range, requiring only a Taylor series expansion of the NL time constant. Design insight is given for common MOS switch types, revealing a high correlation between HD and bandwidth. The first method to quantify the trade-off between thermal noise (SNR) and linearity (SFDR) for sampling circuits is presented. Measured HD2, HD3, HD4, and HD5 versus frequency at multiple sample rates of a Sample and Hold test chip fabricated in a 0.25μm 1P5M CMOS process and Spectre simulation results support the findings. The results broadly apply to switched capacitor circuits in general and sampling circuits specifically, regardless of technology.

3.2 Introduction

Sample and Hold (S/H) circuits are often the most critical signal path block in analog to digital converters (ADC) because they must process rapidly changing, high frequency inputs with accuracy and precision at least equal to that of the ADC. Since the value at the end of the track period is sampled, tracking errors, including nonlinearity (NL), directly affect the sampled value. For high frequency inputs, tracking errors tend to limit the overall system, both S/H and ADC, performance. Communication applications in particular, such as IF sampling, stand to benefit from improved high speed linearity of sampling circuits.

Traditional approaches to frequency dependent linearity analysis for weakly nonlinear circuits use the Volterra series [47] or variations of it. Evaluation of the Volterra kernels, or coefficients, entails n dimensional convolution integrals in the time domain or equivalently n dimensional impulse responses in the frequency domain for the n^{th} order response, where $n = 1$ corresponds to the linear response. When applied to circuits, each order of response desired must be linearly solved with the appropriate nonlinear source corresponding to the kernel of interest applied. Consequently, Volterra based approaches strive to simplify the mathematics required. Common among the simplifying assumptions are a steady-state (SS) response limited to second and third order nonlinearity. Even so, the math required largely remains untenable for hand calculations for all but the simplest circuits with low order kernels. Further details related to circuit application of the Volterra series may be found in [48, 49].

Published frequency dependent nonlinearity analysis for integrated circuits covers a broad array of circuits, they primarily makes use of the Volterra series and encompasses circuits ranging from single transistors to larger functional blocks such as amplifiers or mixers [48–65]. Less detailed Volterra series based analysis of circuits similar to that analyzed in this work may be seen in [49,64,66,67]. Analysis and corroborating measurements, when performed, rarely extend past third order (i.e. HD3, IP3, etc.) and are limited to steady-state conditions.

Expanding upon the method first reported in [68], this work presents an alternative to Volterra based techniques that greatly facilitates the ability to obtain design intuition from frequency dependent nonlinearity analysis. A first order low pass filter model, as is typically set by design for sampling circuits, contributes to simplification of the analysis presented here. The nonlinearity is interpreted as modulating the linear response, as opposed to linearizing the circuit and injecting nonlinear sources. This interpretation results in familiar amplitude and phase modulation (AM & PM) of the forced response, in addition to nonlinear exponential settling of the natural response. Thus, SS settling and discrete-time NL behavior are also quantified. Moreover, evaluation of higher order harmonics now becomes accessible. Weak NL is interpreted conservatively to mean that SFDR $>$ 30dBc in this work, an easily achieved condition for practical open-loop sampling circuits to meet.

The scope of this work is intentionally limited to just the sampling network, thus making an implicit distinction between the separate sample and hold operations, excluding the hold operation from analysis herein. Nonidealities in the hold

operation will further degrade performance beyond that limited from the sampling operation. Likewise, other effects such as input dependent sampling time also degrade performance, but occur after the tracking errors described in this work, which set an upper bound for sampling linearity.

The remainder of this article is outlined as follows: Section 3.3 reviews system linearity issues and the consequences of not resetting the sampling capacitor. Section 3.4 summarizes the model (derived in Appendix 3.9), giving simplified expressions for harmonic distortion terms in three frequency regions. Section 3.5 demonstrates how to apply the model to circuits with examples for TGATE and pumped NMOS switch types. Section 3.6 derives the trade-off between thermal noise (SNR) and linearity (SFDR). Section 3.7 supports the theory with silicon measurements of a S/H test chip. Finally, Section 3.8 summarizes the findings.

3.3 System Linearity

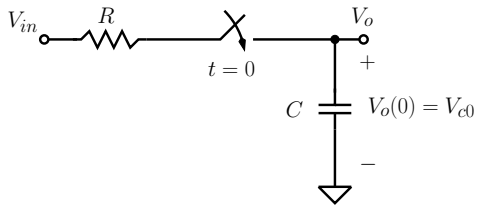


Figure 3.1: Sampling circuit model.

Consider the sampling circuit model presented in Fig. 3.1 with a time constant $\tau = RC$, an ideal switch and an initial capacitor voltage $V_o(0) = V_{c0}$. Its response

after the switch has been closed is described by the differential equation

$$V_{in} = \tau V_o' + V_o. \tag{3.1}$$

Assuming a sinusoidal input such that

$$V_{in}(t) = A\cos(\omega t + \phi), \tag{3.2}$$

the solution to (3.1) for the given initial condition and specific input is

$$\begin{aligned} V_o(t) &= \underbrace{V_{c0}e^{-t/\tau}}_{1} - \underbrace{\frac{A\cos(\phi-\theta)}{\sqrt{1+\omega^2\tau^2}}e^{-t/\tau}}_{2} \\ &\quad + \underbrace{\frac{A}{\sqrt{1+\omega^2\tau^2}}\cos(\omega t + \phi - \theta)}_{3} \end{aligned} \tag{3.3}$$

where $\theta = \arctan(\omega\tau)$. Equation (3.3) is a sum of the zero-input (ZI) response (term 1) and the zero-state (ZS) response. The complete solution (3.3) can be expressed as the sum of two terms in two different ways: either as the sum of the ZI and ZS responses or as the sum of the forced (particular) response (FR - term 3) and natural (homogeneous) response (NR - terms 1 & 2). A distinction between NR/FR and ZI/ZS is of significance here because of the grouping of the linear and (possibly) nonlinear terms. The zero-input response consists of a decaying exponential initiating from V_{c0}. The zero-state response adds a natural frequency

(steady-state) settling term to a scaled and phase-shifted version of the input sinusoid.

Despite the use of linear components, (3.1) describes a nonlinear system for any theoretical arbitrary nonzero initial condition[1]. For a S/H circuit this implies that the sampling capacitor would have to be reset to the same voltage prior to each sampling period for system linearity to be guaranteed. This would require an architecture choice, such as charge-redistribution, where it inherently does this or, alternatively, the addition of a costly reset phase. However, in practice, only two cases are realistic, resetting to the same potential and not resetting at all. Not resetting the capacitor introduces memory into the circuit, but ensures linearity, as shown below.

S/Hs that do not reset the initial capacitor voltage force the initial condition to the previous sample, i.e. $V_{c0} = V_o(n-1)$, introducing discrete time filtering. Sampling (3.3) and rewriting in terms of zero-state and zero-input responses,

$$V_o(n) = e^{-T_s/\tau} V_o(n-1) + V_{o,zs}(n) \tag{3.4}$$

where T_s is the settling period, which is less than the sampling period[2]. Clearly $V_o(n)$ is linear. Taking the Z-transform and rearranging,

$$V_o(z) = \frac{1}{1 - e^{-T_s/\tau} z^{-1}} V_{o,zs}(z). \tag{3.5}$$

[1]Intuitively, in linear systems, zero input yields zero output [69]. Therefore setting $A = 0$ in (3.3) would force $V_o(t)$ to zero if the system is linear, a condition that an arbitrary nonzero V_{c0} precludes.

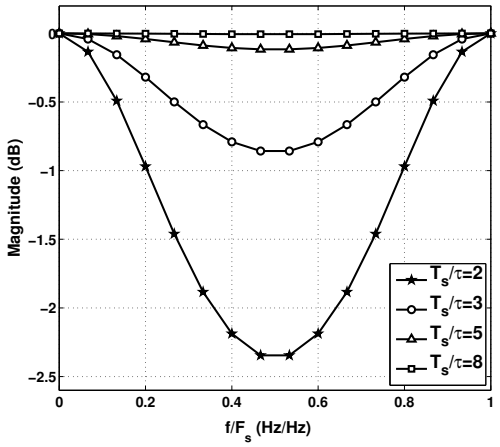
[2]For two phase non-overlapping clocks, $T_s \approx T/2$ where T is the inverse of the sample rate.

From (3.4) and (3.5), the memory manifests itself as a first order recursive discrete-time low pass filter (LPF) [69]. The discrete-time LPF's effect can be seen in Fig. 3.2 which plots the frequency dependent attenuation and phase shifts introduced for a range of T_s/τ values. Even for slow circuits with modest T_s/τ ratios, the magnitude and phase approach unity and 0^o respectively, implying that to first order, the discrete-time LPF can be ignored for reasonably fast implementations.

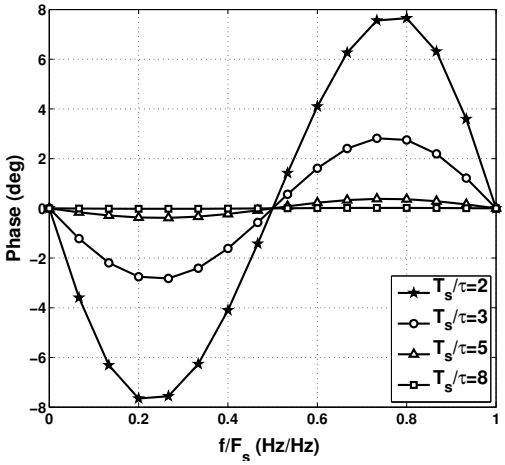
Although the exponential term responsible for steady-state settling in the natural response (term 2 in (3.3)) may also appear nonlinear, it introduces no nonlinearity for two reasons. First, the magnitude of its coefficient scales exactly with the sinusoid's amplitude (term 3 in (3.3)) regardless of frequency. Furthermore, though this term results in a decaying exponential within a single sampling period, it always settles to the same level over a sequence of multiple samples, adding only a DC shift. Therefore, a longer time constant does not degrade linearity. However, because signal attenuation increases with τ, SNR decreases, favoring the reduction of τ.

3.4 Component Nonlinearity

Taking the sampling network in Fig. 3.1 and implementing it with real components introduces nonlinearity due to their imperfections and input dependencies. Thus replacing τ with $\hat{\tau}(V_{in})$ allows the model to be generalized for more complex, practical circuits. For example, employing a MOS switch changes the resistor to the MOS drain-source resistance. This has input dependence in both the gate-source



(a) Magnitude versus sampled frequency.



(b) Phase versus sampled frequency.

Figure 3.2: Frequency response of the discrete-time LPF due to not resetting the sampling capacitor.

and threshold voltages. The reversed biased pn-junction capacitance from the drain/source to bulk shunts the sampling capacitor. Moreover, this approach lends itself equally well to Bipolar or BiCMOS circuits, with the only condition required being that a closed form expression for a dominant pole open loop sampling circuit

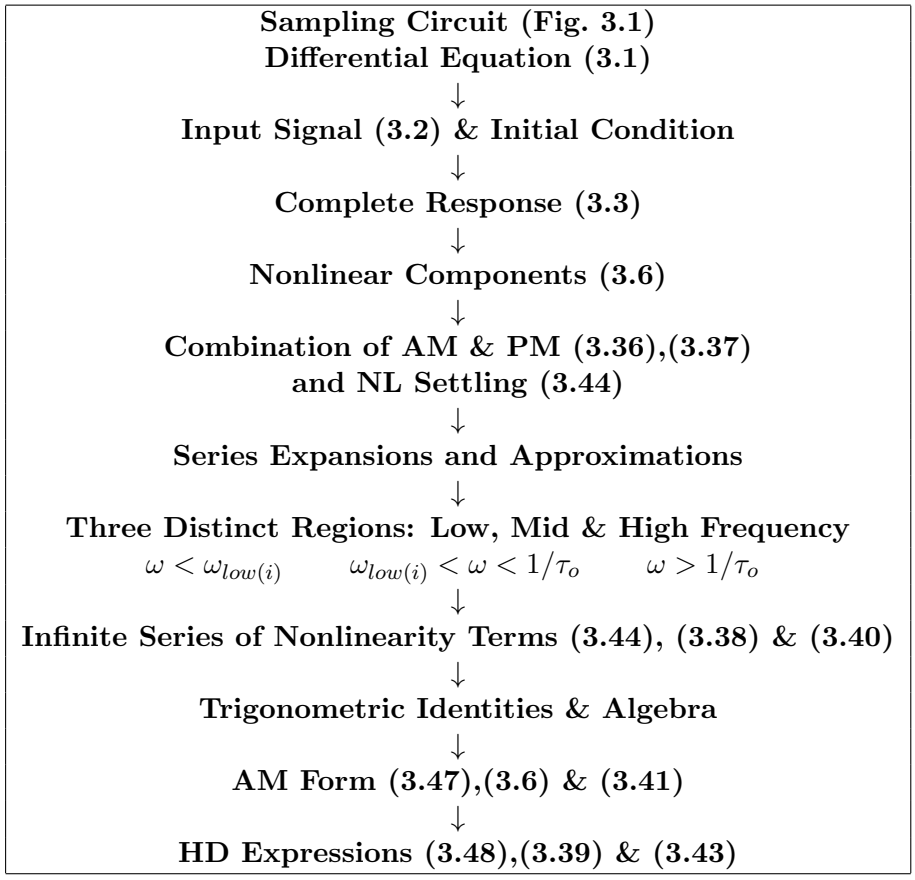


Figure 3.3: Overview of harmonic distortion derivation.

be available.

Functionally, nonlinearity in the sampling network may be described as perturbations in its 3dB bandwidth. These perturbations cause a pure sinusoid at the input to produce the fundamental at the output (i.e. sampling node) as well as spurs that are a function of the specific nonlinearity and frequency. Conceptually, the derivation of the harmonic distortion behavior flows as described in Fig. 3.3 leading to the (typical) frequency response terms (Fig. 3.4) of *each har-*

monic. Mathematically, the harmonics are infinite summations on the power (n) of ($\omega\hat{\tau}(V_{in})$) shown later in (3.38). Yet most real systems can be amply characterized by a single expression within each of the three regions: low, mid and high frequency.

Results from the complete derivation, shown in Appendix 3.9, are summarized here, only supplying mathematical representations which lead to design insight. It is expected that the mid frequency region will be the typical operation region for most practical circuits as explained below.

For the forgoing analysis, the nonlinear time constant is defined as

$$\hat{\tau}(V_{in}) = \tau_o + \alpha_1 V_{in} + \alpha_2 V_{in}^2 + \alpha_3 V_{in}^3 + \cdots \tag{3.6}$$

where τ_o represents the linear portion of the time constant and each α_i corresponds to the coefficient of the i-th order nonlinearity term, having units of $seconds/Volt^i$. Note that in (3.6), V_{in} corresponds to its AC component only. Given a closed form expression for the nonlinear time constant, $\hat{\tau}$, they may be found as follows:

$$\tau_o = \left.\hat{\tau}(V_{in})\right|_{V_{in}=V_{cm}}, \tag{3.7}$$

$$\alpha_i = \left.\frac{\partial^i \hat{\tau}(V_{in})}{\partial {V_{in}}^i}\right|_{V_{in}=V_{cm}}, \tag{3.8}$$

where V_{cm} is the input common-mode voltage.

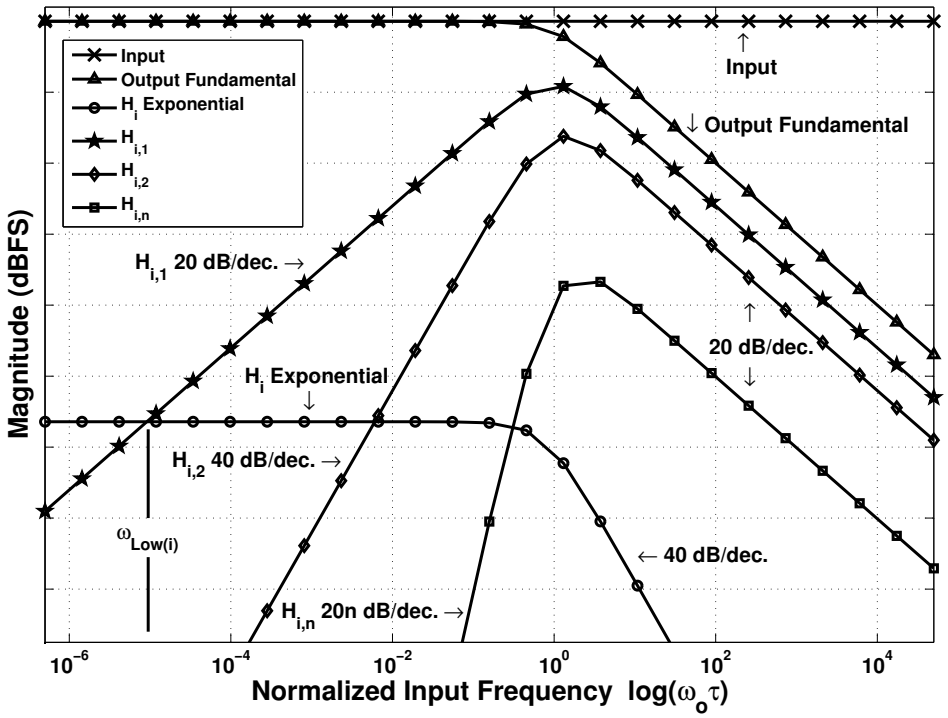


Figure 3.4: Each harmonic (e.g. HD2, HD3, etc.) may be represented as an infinite summation. The components of the summations are plotted along with the input and output fundamental tones for reference. The largest spurious component sets the HD value at a given frequency. In effect, this is a drawing of the NL terms that compose each harmonic as described mathematically in Appendix 3.9.

3.4.1 Explanation of Low, Mid and High Frequency Regions

Each harmonic is modeled as an infinite summation of frequency dependent terms that correspond to the order of nonlinearity, graphically depicted in Fig. 3.4. Each harmonic (e.g. $2^{nd}, 3^{rd}, \ldots$) may be represented by such a plot. Combining all the terms in a root sum square provides the overall nonlinearity. However, dominant

terms arise in low, mid, and high frequencies.

The high frequency region consists of input frequencies beyond the half power bandwidth, $\omega > 1/\tau = 1/(RC)$, of the low pass circuit. Together, the low and mid frequency regions span from DC to the 3 dB bandwidth. Low frequency behavior is constant until the mid frequency term surpasses it at $\omega_{Low(i)}$, as seen in Fig. 3.4. This frequency is different for every harmonic. Spanning from this low frequency transition to the half power bandwidth, $\omega_{Low(i)} < \omega < 1/(RC)$, is the mid frequency region. It is expected that the mid frequency region will be the typical operating region for sampling circuits. Furthermore, as explained later, the low frequency region of a well designed sampling network will be below the noise floor of an accompanying ADC, and thus the $\omega_{Low(i)}$ transition frequency will not be observable.

3.4.2 Mid Frequency HD ($\omega_{Low(i)} < \omega \ll 1/\tau$)

After applying trigonometric identities, the forced response (term 3 of (3.3)) of the general solution to the system differential equation, (3.1), modulated by the nonlinear time constant may be written as

$$\hat{V}_{o,F}(t) = A \underbrace{\left(\frac{1}{\sqrt{1+\omega^2\hat{\tau}^2}}\right)}_{AM-even} \left[\underbrace{\left(\frac{1}{\sqrt{1+\omega^2\hat{\tau}^2}}\right)}_{PM-even} \cos(\omega t)$$

$$+\underbrace{\left(\frac{\omega\hat{\tau}}{\sqrt{1+\omega^2\hat{\tau}^2}}\right)}_{PM-odd}\sin(\omega t)\Bigg]. \tag{3.9}$$

In (3.9), the contributing nonlinearity sources are indicated by origin (i.e. AM or PM) and whether or not they are even or odd functions of $\omega\hat{\tau}(V_{in})$. Note that PM has been expressed in the form of AM (e.g. using in-phase and quatrature components). Applying the series expansion of $1/(1+x) \approx 1 - x + x^2 - x^3 + \ldots$,

$$\begin{aligned}\hat{V}_{o,F}(t) = A\Big[&\Big(1-\omega^2\hat{\tau}^2+\omega^4\hat{\tau}^4+\ldots\Big)\cos(\omega t)\\ &+\Big(\omega\hat{\tau}-\omega^3\hat{\tau}^3+\omega^5\hat{\tau}^5+\ldots\Big)\sin(\omega t)\Big].\end{aligned} \tag{3.10}$$

Slopes of $20n$, where n is the power of $\omega\hat{\tau}$, dB per decade result from the respective terms. What is interesting from an intuition standpoint is that only PM gives rise to odd order terms. Because the lowest order term, 1^{st}, nominally dominates the response over this broad frequency range of operation, AM does not make a significant contribution in most practical cases. Mathematical justification lies in that $\omega\hat{\tau} \ll 1$ and consequently $(\omega\hat{\tau})^n \gg (\omega\hat{\tau})^{n+1}$. This may be counterintuitive because, even for low frequencies, a small, ostensibly insignificant, modulated phase shift dominates the distortion. The implication is that PM should not be neglected in frequency dependent linearity analysis.

Shown later in Section 3.9, further mathematical development, consisting of substituting in the input signal and nonlinear time constant, applying trigonometric identities, collecting terms, and reducing to amplitude modulation (carrier

present) form, reduces the problem so that the HD expressions for this region may be expressed as

$$\text{HDj} \approx \frac{1}{2}\omega\beta_{i,1}, \tag{3.11}$$

where $j = i + 1$. The $\beta_{i,1}$ terms are simply the power series expansion of the input sinusoid, $V_{in} = A\cos(\omega t)$, in (3.6) rearranged in terms of increasing multiples of ω. These are shown in Table 3.3 in Appendix 3.9. For the first two harmonics, this yields

$$\text{HD2} \approx \frac{1}{2}\omega\left(\alpha_1 A + 3\alpha_3 A^3/4 + \cdots\right), \tag{3.12}$$

$$\text{HD3} \approx \frac{1}{2}\omega\left(\alpha_2 A^2/2 + \alpha_4 A^4/2 + \cdots\right). \tag{3.13}$$

Familiar low frequency power series amplitude scaling [48] is exhibited together with a linear increase in HD with increasing frequency.

In essence, the problem has been reduced to the equivalent of frequency-independent nonlinearity analysis and represents an enormous reduction in problem complexity compared to nearly all frequency dependent linearity analysis in the literature. Given this result, it is actually pragmatic to perform hand calculations, as is shown later, to further advance understanding and design insight. More importantly, the (typical) increase of 20 dB per decade trend, allows the designer to extrapolate and predict what the HD would be at another, presumably higher, frequency given a single known value at some frequency. Moreover, higher order terms (i.e. HD4 and higher) are accessible since they only require additional derivatives of the nonlinear time constant with respect to the input. This is also

contrary to previously published work.

3.4.3 Low Frequency HD ($\omega < \omega_{Low(i)}, \omega\tau \ll 1$)

Low frequency HD arises from two sources, both related to exponential settling, that for a linear system reach the same value from one period to the next as discussed in Section 3.3. Component nonlinearity within the system causes modulation, input dependency, in the final value at the end of the settling period. When the sampling capacitor is reset, no discrete-time effects occur. However, when the sampling capacitor is not reset and the initial condition is directly proportional to the previous sample, discrete-time modulation occurs. Both cases give rise to similar expressions, with some caveats. Both may be expressed in the following form:

$$\text{HDj} \approx e^{-T_s/\tau_o} g_j(\alpha_i, A, T_s, \tau_o), \tag{3.14}$$

where $g_j(\alpha_i, A, T_s, \tau_o)$ is some function of the specific nonlinearity and input amplitude for the harmonic of interest and T_s is the settling period. Because these functions are relatively complex, they are not particularly insightful from a design perspective due to the excessive algebra and relatively small effect compared to the exponential. The major distinction between discrete-time modulation and just nonlinear exponential settling is that discrete-time modulation has direct modulation with the delayed carrier, input fundamental, leading to $|g_j(\alpha_i, A, T_s, \tau_o)|$ that are larger for a given harmonic since they are one order lower and the $|\alpha_i|$ are less than one. Thus, non-resetting sampling circuits will exhibit elevated HD

magnitudes at low frequency, but not dramatically so.

The most important observations here are that HD behavior is independent of frequency and scaled by an exponential, implying that the best way to improve the performance is to make the circuit faster or give it more time to settle. Because $g_j(\alpha_i, A, T_s, \tau_o)$ is a function of α_i, it is reduced by the same mechanisms as the mid frequency region. Moreover, the low frequency limit dictates that HD cannot be infinitely reduced by lowering the input frequency as (3.11) might be interpreted.

It is likely that most practical, wide-band sampling circuits won't be limited by the sampling network low frequency linearity. Fundamentally, this is due to the reduction by the exponential. For example, settling of ten time constants reduces (3.14) by 86.9 dB before taking into account $g_j(\alpha_i, A, T_s, \tau_o)$, which has a magnitude much less than one. The HD levels in the low frequency region are conservatively expected to be well below the noise floor of an accompanying ADC for implementations with absolute settling accuracies near the ADC LSB level, and likely much lower. Additionally, the transition frequency, where mid frequency surpasses the low frequency limit is reasonably in the kilohertz range or lower, below frequencies of interest in many applications where an open-loop sampling circuit would find use.

3.4.4 High Frequency HD ($\omega \gg 1/\tau$)

The high frequency region, frequencies beyond the linear 3 dB bandwith ($\omega_{3dB} = 1/\tau_o$), results are largely academic because operation beyond the half power band-

width may be generously characterized as atypical due to deteriorating signal power and consequently SNR among other issues. Additional poles and zeros, ignored in this work are also likely to be significant at these frequencies, hundreds of megahertz to gigahertz.

Relative to the input signal, high frequency HD decreases at the same rate as the output fundamental. This implies that it remains constant relative to the output fundamental. Thus the HD level does not deteriorate once it reaches it's worst case, near the half power bandwidth. Mathematically, this may be expressed as

$$\text{HDj} \approx \frac{1}{2}\frac{\beta_{i,1}}{\omega {\tau_o}^2}. \tag{3.15}$$

3.4.5 Caveats

The expressions shown for low, mid, and high frequency HD are broadly expected to be the typical case. However, it is possible that other, higher order, terms may dominate under certain circumstances. One such circuit example is shown in Section 3.5.3 with a pumped NMOS switch. These cases tend to occur when there are singularities, the absence or great reduction, in the α_i nonlinear coefficients. In such cases, slopes of 40 dB per decade or higher may be observed in the mid frequency region. These may be anticipated when $|\alpha_i| \ll |\alpha_{i+1}|$. Additionally, this type of behavior is more likely to occur at higher frequencies and for higher order harmonics. Here, more care should be taken and examination of the full derivation in Appendix 3.9 provides further detail.

Within the mid frequency region, if the 20 dB per decade asymptote crosses the output fundamental before the half power bandwidth, the underlying assumption of weak nonlinearity blurs since $\omega\hat{\tau}$ is no longer appreciably less than unity. As a result, a reduction in slope occurs. Simulations indicate that this slope is approximately 10 dB per decade. Very slow NMOS switch circuits are candidates for this degeneration of the model. An estimate of when the reduced slope of the HD begins is near the -35 dBc level.

The models for the three regions may be made continuous over frequency by combining the terms in the same fashion as bode asymptotes are. However, behavior near the half power bandwidth is not handled precisely. This may result in errors in both the peaking frequency, which is roughly the 3 dB bandwidth, and consequently the value at the peak. Because this would unnecessarily complicate the analysis with little gain in understanding and since practical sampling circuits are not typically operated here, it is omitted from this work.

3.5 Application to Circuits

In applying the harmonic distortion models presented to practical circuits, two switch types are examined: a TGATE switch and a pumped NMOS switch. An NMOS switch was examined in [68]. The goal is to identify the parameters that have the most influence on harmonic distortion and how much they affect them. A simplified sampling circuit model is employed together with 'text book' device models that omit higher order effects and curve fitting parameters inherent in most

simulator models. When more detail is required, together with higher order MOS device characteristics, the method of open-circuit time constants [70] may be used to estimate the time constant of more complicated sampling circuit models before applying series expansions.

In this analysis the triode MOSFET model drain source resistance (R_{ds}), threshold voltage and junction capacitance (C_{sb}) are taken as

$$R_{ds} = \frac{L}{\mu C_{OX} W (V_{gs} - V_t - V_{ds})}, \tag{3.16}$$

$$V_t = V_{t0} + \gamma\Big(\sqrt{V_{sb} + 2\phi_F} - \sqrt{2\phi_F}\Big), \tag{3.17}$$

$$C_{sb} = \frac{C_{jo}\left(A_S + \frac{1}{2}WL\right)}{(1 + \frac{V_{sb}}{\phi_o})^m}, \tag{3.18}$$

where γ, ϕ_F, ϕ_o, A_s, m, and C_{jo} are the body-effect parameter, surface inversion potential, built-in contact potential of junction to bulk, source junction area, bulk-to-junction grading coefficient, an junction depletion capacitance respectively [34]..

The time constant of the simplified sampling circuit model in Fig. 3.5 is

$$\hat{\tau} = (R_s + R_{ds})\,(C_H + C_{sb})\,. \tag{3.19}$$

Although C_{sb} is not generally a dominant contributor to overall nonlinearity, it is included to emphasize the point that the model is of a nonlinear time constant, not just the switch resistance, and to illustrate the impact of a large linear series resistance. Though, for the sake of mathematical simplicity, it is only shown in the pumped NMOS switch case.

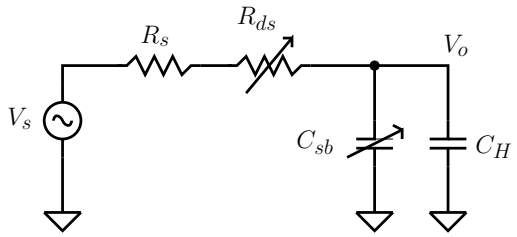


Figure 3.5: Sampling circuit reduced model.

Inherent linearity improvements come about from minimizing the nonlinear coefficient magnitudes, $|\alpha_i|$. Generally speaking, they are reduced as a whole and not optimized individually. Consequently, evaluating the first two terms reveals trends that extend to higher order. A commonality among the switch types is the strong correlation between speed and linearity. This occurs because the same mechanisms that make the various switch types faster by increasing their conductance, reduce the nonlinear coefficients. The largest improvements come about from a larger overdrive voltage, $V_{OD} = (V_{gs} - V_t)\Big|_{V_i=V_{cm}}$, where V_{cm} is the input common-mode or DC voltage, which typically exhibits quadratic or higher order dependence. Conversely device size changes offer merely linear improvements.

3.5.1 TGATE Switch

A TGATE improves upon an NMOS switch because of the complementary nature of parallel N and P type switches. As one increases impedance, the other reduces, resulting in less input dependence in the combined switch 'on' resistance, while increasing available signal swing. For the NMOS device, $V_{ds} \approx 0$, $V_{gs-n} = V_{dd} -$

$V_{cm} - V_{in}$ and $V_{sb-n} = V_{cm} + V_{in}$. Similarly for the PMOS, $V_{ds} \approx 0$, $|V_{gs-p}| = V_{cm} + V_{in}$ and $|V_{sb-p}| = V_{dd} - V_{cm} - V_{in}$. These conditions are shown in Fig. 3.6(a).

From the Taylor Series expansion,

$$\tau_o = (R_s + R_{dso})\, C_H \tag{3.20}$$

$$\alpha_1 = C_H {R_{dso}}^2 \left[\mu_n C_{ox} \frac{W_n}{L_n} \left(-1 + \frac{\gamma}{2\sqrt{V_{cm} + 2\phi_F}} \right) + \mu_p C_{ox} \frac{W_p}{L_p} \left(1 - \frac{\gamma}{2\sqrt{V_{dd} - V_{cm} + 2\phi_F}} \right) \right], \tag{3.21}$$

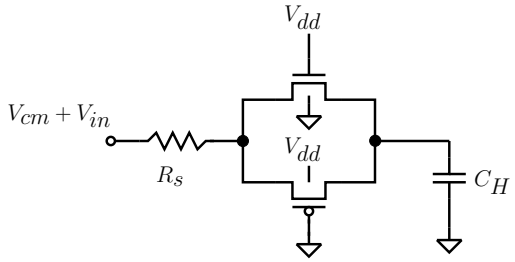
$$\begin{aligned} \alpha_2 = {R_{dso}}^3 C_H \Bigg[& -\frac{\gamma}{8R_{dso}} \left(\frac{\mu_n C_{ox} \frac{W_n}{L_n}}{(V_{cm} + 2\phi_F)^{3/2}} + \right. \\ & \left. \frac{\mu_p C_{ox} \frac{W_p}{L_p}}{(V_{dd} - V_{cm} + 2\phi_F)^{3/2}} \right) \\ & + \left\{ \mu_n C_{ox} \frac{W_n}{L_n} (1 - \frac{\gamma}{2\sqrt{V_{cm} + 2\phi_F}}) \right. \\ & \left. + \mu_p C_{ox} \frac{W_p}{L_p} (1 - \frac{\gamma}{2\sqrt{V_{dd} - V_{cm} + 2\phi_F}}) \right\}^2 \Bigg], \end{aligned} \tag{3.22}$$

where

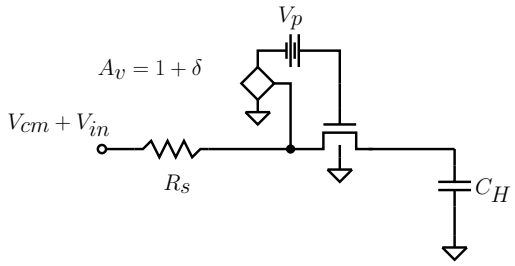
$$R_{dso} = \frac{1}{\mu_n C_{ox} \frac{W_n}{L_n} V_{OD,n} + \mu_p C_{ox} \frac{W_p}{L_p} V_{OD,p}}, \tag{3.23}$$

$$V_{OD,n} = V_{dd} - V_{cm} - V_{tno} + \gamma \left(\sqrt{V_{cm} + 2\phi_F} - \sqrt{2\phi_F} \right), \tag{3.24}$$

$$V_{OD,p} = V_{cm} - |V_{tpo}| + \gamma \left(\sqrt{V_{dd} - V_{cm} + 2\phi_F} - \sqrt{2\phi_F} \right). \tag{3.25}$$



(a) TGATE switch circuit.

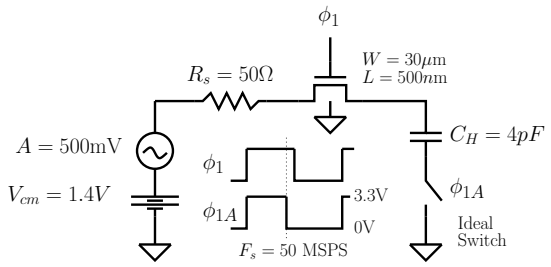


(b) Pumped NMOS switch circuit.

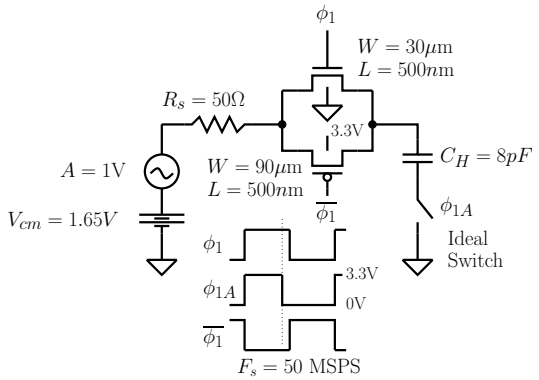
Figure 3.6: Circuit bias for Taylor series expansion of each of the switch types.

A TGATE is more linear than an NMOS switch because of both reduced input dependence in R_{ds} and increased speed, shifting the HD curves lower in magnitude and higher in frequency. Unlike a lone NMOS switch, a TGATE gives the opportunity to greatly reduce the nonlinear coefficients through device sizing. Eq. (3.21) and (3.22) imply that by setting V_{cm} to $V_{dd}/2$ and sizing the NMOS and PMOS such that $\mu_n C_{ox} \frac{W_n}{L_n} = \mu_p C_{ox} \frac{W_p}{L_p}$, not for equal conductances, this reduction is possible. This cancelation is not exact because of model limitations and higher order effects ignored to simplify the math. Though not shown, junction capacitance nonlinearity is reduced at the expense of larger net capacitance. Otherwise, the same conditions apply to reduce the nonlinearity of either switch individually as

that of the lone NMOS.



(a) NMOS switch circuit.

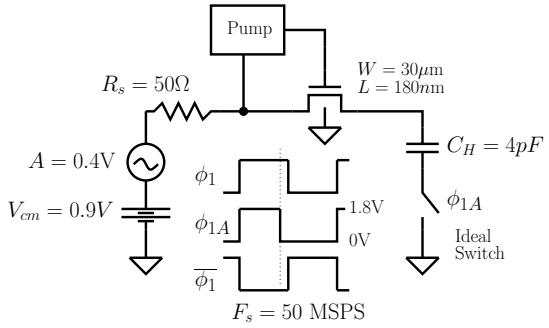


(b) TGATE switch circuit.

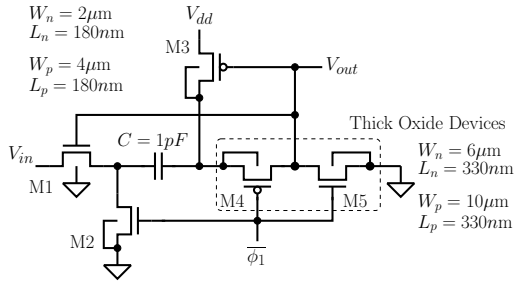
Figure 3.7: NMOS and TGATE switch circuits for Spectre transient simulations using EKV device models.

3.5.2 Pumped NMOS Switch

By driving a MOS switch with a signal that follows the input with a level shift, a pump switch driver is implemented, with the advantage that, to first order, V_{gs} becomes independent of the input signal. For this derivation, a linear pump gain error, δ, results in the circuit model in Fig. 3.6(b). Now $V_{ds} \approx 0$, $V_{gs} = V_p + \delta V_{in}$ and $V_{sb} = V_{cm} + V_{in}$. In physical terms, δ and V_p measure the quality of the pump



(a) Pumped NMOS switch circuit.



(b) Pump circuit from [71]. Devices M4 and M5 have thick gate oxides for reliability.

Figure 3.8: Pumped NMOS switch circuit for Spectre transient simulations with 0.18μm BSIM3v3 device models.

circuit, quantifying tracking accuracy and speed with δ and the ability to overdrive up to the oxide breakdown voltage for the process with V_p. Thus,

$$\tau_o = (R_s + R_{dso})(C_H + C_{sbo}) \tag{3.26}$$

$$\begin{aligned}\alpha_1 = &-(C_H + C_{sbo})\frac{R_{dso}}{V_{OD}}\left(\delta + \frac{\gamma}{2\sqrt{V_{cm} + 2\phi_F}}\right) \\ &-(R_s + R_{dso})C_{sbo}\frac{m}{V_{cm} + \phi_o}\end{aligned} \tag{3.27}$$

$$\alpha_2 = (C_H + C_{sbo})\frac{R_{dso}}{V_{OD}}\left[\frac{\gamma}{8(V_{cm} + 2\phi_F)^{3/2}}\right.$$

$$+\frac{1}{V_{OD}}\left(\delta+\frac{\gamma}{2\sqrt{V_{cm}+2\phi_F}}\right)^2\Bigg]$$
$$+(R_s+R_{dso})C_{sbo}\frac{m(m+1)}{2(V_{cm}+\phi_o)^2}$$
$$+\frac{R_{dso}C_{sbo}}{V_{OD}}\left(\delta+\frac{\gamma}{2\sqrt{V_{cm}+2\phi_F}}\right)\frac{m}{V_{cm}+\phi_o} \tag{3.28}$$

Where,

$$R_{dso}=\frac{L}{\mu_n C_{ox}WV_{OD}} \tag{3.29}$$
$$V_{OD}=V_p-V_{tno}+\gamma\left(\sqrt{V_{cm}+2\phi_F}-\sqrt{2\phi_F}\right) \tag{3.30}$$
$$C_{sbo}=\frac{C_{jo}\left(A_s+\frac{1}{2}WL\right)\phi_o{}^m}{\left(V_{cm}+\phi_o\right)^m}. \tag{3.31}$$

Compared to the simple NMOS switch case, V_{OD} is much larger, significantly reducing nonlinearity coefficients because the dominant terms in α_1 and α_2 remain proportional to $L/\left(WV_{OD}{}^2\right)$ and $L/\left(WV_{OD}{}^3\right)$. Moreover, because direct input dependence has been greatly reduced from one to δ, threshold variations increase in relative importance and remain unchanged from the simple NMOS switch case. The same may be said of nonlinear junction capacitance. From a design perspective, the challenge is to implement the pump with as little phase shift and gain error as possible in the signal band in order to minimize δ and to pump as close to the oxide breakdown voltage as safely possible, maximizing V_{OD}.

Though a large linear series resistance, R_s, might superficially appear to offer linearity enhancements, this is not the case. Low frequency HD levels would rise dramatically because of the longer time-constant, τ_o, and the exponential depen-

dence shown in (3.14). Moreover, no benefit to drain-source resistance linearity comes about. However, junction capacitance HD will rise in direct proportion to the increase in R_s as seen in (3.27) and (3.28).

3.5.3 Transistor Level Simulation Examples

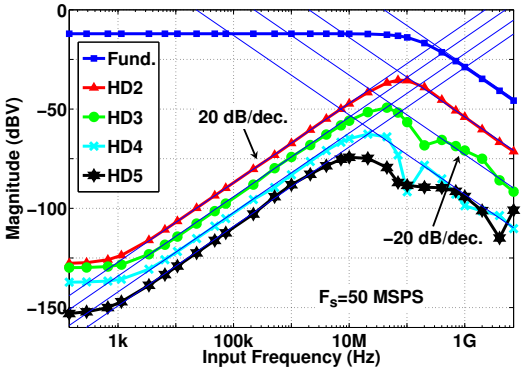
To reinforce the predicted behavior of the proposed model, transistor level simulations of the three switch types were run with Cadence's Spectre simulator. Because BSIM models exhibit a singularity for changes in the polarity of the drain and source that undermines linearity simulation accuracy [72], EKV device models were used for NMOS and TGATE switches, Fig. 3.7, for a 0.5μm process. A pumped NMOS switch using 0.18μm BSIM3v3 device models, Fig. 3.8 is also evaluated. Using strobed coherent sampling, the input frequency was swept from 71 Hz to 7 GHz. Fig. 3.7 and 3.8 outline the circuit operating conditions. Note that circuit parameters and voltages vary from one example to the next. The purpose is to illustrate different possibilities and the expected curve shapes, not to make direct comparisons.

The NMOS and TGATE plots, Fig. 3.9(a) and 3.9(b) exhibit the typically expected curve shapes.[3] Each shows a flat HD frequency response in the low frequency region, before the linear increase with respect to frequency in the mid frequency region surpasses it. The predicted 20 dB per decade slopes are present

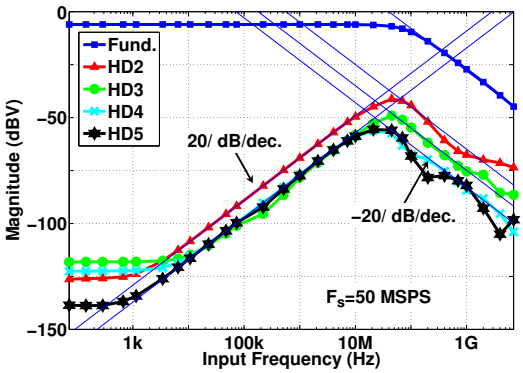
[3]The deviations that occur at high frequency are primarily attributable to simulator tolerance setting limitations. Tightening the simulator settings, *vabstol* and *reltol* in particular, improves the accuracy but at the cost of dramatically increased simulation time. Higher order effects may also play a role.

for all shown HD terms. HD peaks near the 3 dB bandwidth and then decreases at the predicted -20 dB per decade slope.

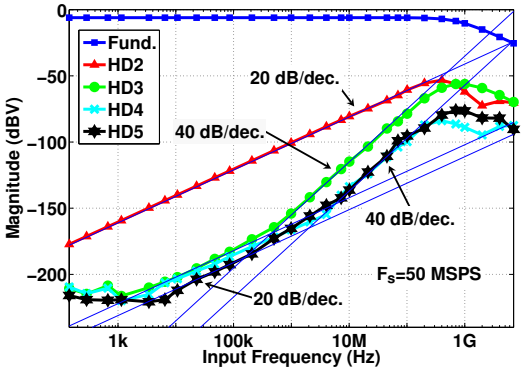
Fig. 3.9(c) shows the simulated pumped NMOS switch HD2-HD5 that has more complicated behavior. For each harmonic, the low frequency limit is either below the simulator accuracy settings or occurs lower in frequency than simulated. HD2 follows the predicted typical curve in both the mid and high frequency regions. HD3-HD5, however, illustrate how a higher order slope manifests. Initially, HD3-HD5 rise above the simulation accuracy noise floor and increase at 20 dB per decade before being surpassed by the 2^{nd} order term attributable to $\beta_{i,2}$ at higher frequency with a slope of 40 dB per decade. The large V_{OD} value greatly reduces the nonlinear coefficients to the point where, at large enough frequency, faster slopes move to the forefront.



(a) 0.5μm EKV NMOS switch.



(b) 0.5μm EKV TGATE switch.



(c) 0.18μm pumped BSIM3v3 NMOS switch.

Figure 3.9: Simulated HD2-HD5 vs input frequency of three switch types. Spectre transient simulations were run on the circuits in Fig. 3.7 and 3.8. Using strobed data at the end of the hold phase, DFTs were taken and the HD2-HD5 saved for plotting. These plots show what the harmonics would look like if all other effects were negligible. Some simulator artifacts are present.

3.6 Design Implications

3.6.1 Relationship Between SNR and SFDR

In Section 3.4 the behavior of HD was characterized over frequency. Of primary interest is the mid frequency range because this is where sampling circuits typically operate. Within this region HD2 $\approx \frac{1}{2}\omega\alpha_1 A$, HD3 $\approx \frac{1}{4}\omega\alpha_2 A^2$, etc. Furthermore, α_i may be expressed as some function f_i of the specific nonlinearity multiplied by the linear time constant $\tau_o = R_o C_o$, where $|f_i| \ll 1$ typically and $C_o \approx C_H$. Thus, SFDR may be expressed as

$$\text{SFDR} = 1/\left(\omega\tau_o |f_i| A^i\right). \tag{3.32}$$

Eq. (3.32) allows for SFDR to be set by any harmonic, presuming the typical 20dB per decade slope, but may be easily modified to allow for faster slopes when singularities are present, like that shown in Fig. 3.9(c).

Assuming S/H noise is dominated by its thermal component, SNR becomes

$$\text{SNR} = \frac{A^2}{2m^2\frac{kT}{C_o}}, \tag{3.33}$$

where m is a circuit dependent factor, reasonably in the range of five to ten[4].

[4]The parameter m accounts for additional noise in the circuit and has a high correlation to the overall amount of switching in the circuit. This is why a flip-around architecture has a smaller m and thus lower noise than a charge-redistribution architecture.

Solving (3.33) for C_o and substituting into (3.32),

$$\mathrm{SFDR} = 1/\left(2\omega R_o m^2 kT|f_i|A^{i-2}\mathrm{SNR}\right). \tag{3.34}$$

It then follows that

$$\Delta\mathrm{SFDR}_{\mathrm{dB}} = -\Delta\mathrm{SNR}_{\mathrm{dB}}. \tag{3.35}$$

Because both SFDR and SNR may be expressed as explicit functions of the sampling capacitor, (3.34) and (3.35), result. In essence, (3.34) and (3.35) quantify the bandwidth tradeoff between harmonic distortion nonlinearity and thermal noise performance due to sampling capacitor size. Since SNR is defined as a power ratio while SFDR as an amplitude ratio, the 3 dB, one to one, tradeoff that (3.34) and (3.35) suggest may be misleading; comparing amplitude ratios directly, instead of a power ratio to an amplitude ratio, a 3 dB gain in "SNR" results in a 6 dB loss in SFDR. Additionally, this result represents the upper bounded limit. As parasitics grow, direct dependence upon the the sampling capacitor is degraded, reducing the factor of two amplitude difference when compared on a logarithmic scale.

Measurably nonlinear sampling networks provide results within the roughly 90 dB range limited by the filtered signal source, the ADC linearity and their noise floors. Intentionally limited sampling linearity is an important distinction because it is unusual among frequency dependent linearity analysis. Without doing so, the predicted curves would be unreasonably difficult to characterize experimentally due to measurement limitations. Additionally, it is emphasized that the amplifier is over designed so that it does not limit performance.

To substantiate the proposed model, specifically Eqs. 3.11-3.13 and Eq. 3.34, measurements from multiple S/Hs with varying capacitor sizes are shown. Because the nonlinear coefficients[5], α_i, are almost directly proportional to the sampling capacitor size, a doubling should result in a 6 dB reduction in HD2 and HD3. Moreover, as is well understood, thermal noise reduces by 3 dB. Simply put, showing 6 dB changes from a doubling or halving of the sampling capacitor size validates the proposed model in the mid-frequency region as well as the SNR and SFDR tradeoff. Furthermore, existence of the low frequency nonlinear exponential settling and/or discrete time modulation nonlinearity is verified by varying the sampling rate.

3.7 Silicon Verification

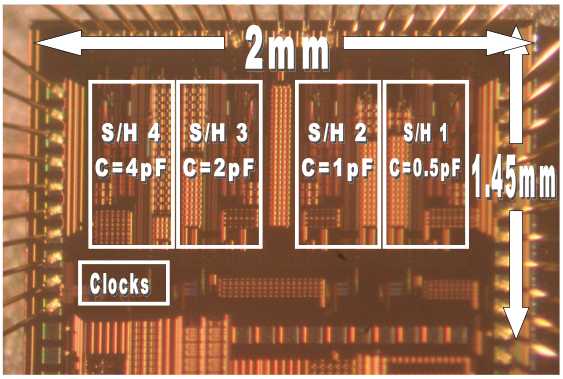


Figure 3.10: Die photo of the test chip.

[5]Specifically, Eqs. 3.21-3.22 for a TGATE switch and Eqs. 3.27-3.28 for a pumped MOS switch. Reference [68] shows α_1 and α_2 for an NMOS switch.

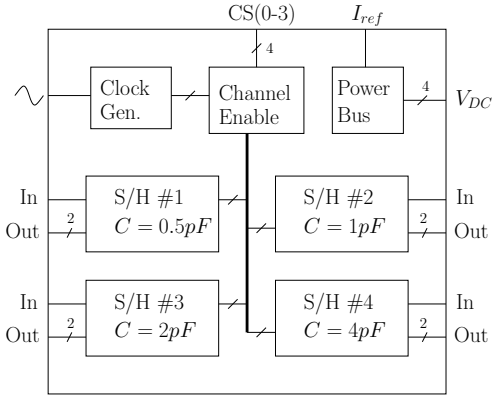


Figure 3.11: Top level block diagram of test chip.

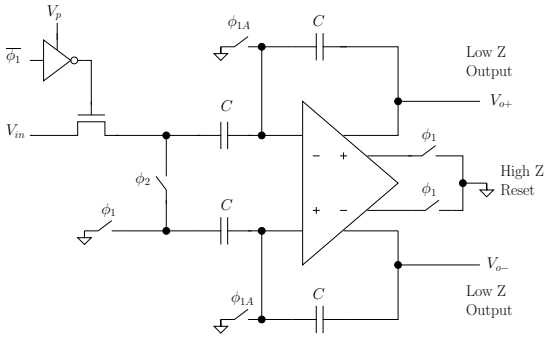


Figure 3.12: Simplified S/H test circuit. An NMOS sampling switch of size 15/0.35 μm is used. Supply V_p provides a means to adjust the sampling time constant to fit the HD curves within the limited measurement bandwidth.

3.7.1 Test Chip

S/H test circuits were designed in a 1P5M 0.25μm CMOS process, Fig. 3.10. The four discrete S/H circuits, Fig. 3.11, differ only in capacitor size, operate on a 3.3V supply and consume a collective 59mA. The unity gain charge redistribution S/H topology, Fig. 3.12, has single-ended input and differential output, while operating on two phase non-overlapping clocks. Single-ended to fully-differential conversion

is accomplished by charge sharing between the equally sized input capacitors of the amplifier and the common-mode properties of the amplifier. Intentionally over-designed to not limit the switch linearity measurements, the amplifier has continuous time common-mode feedback and low impedance outputs to drive the off-chip ADC directly.

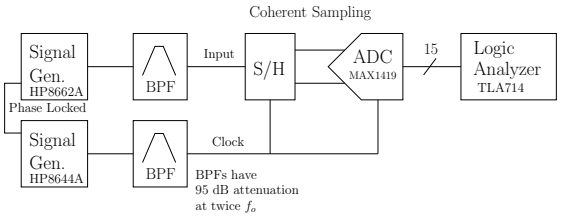


Figure 3.13: Measurement setup.

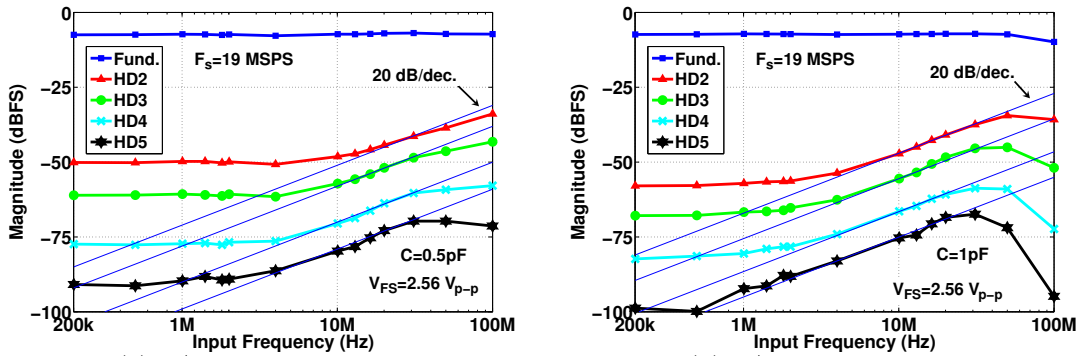
3.7.2 Measurement Setup

The measurement setup, Fig. 3.13, consisted of phase-locked, signal sources, filtered by precision bandpass filters with 95 dB attenuation at twice the center frequency. Input frequencies were limited to the center frequencies of the available bandpass filters. AC coupled to the S/H, a 15-b 65MSPS ADC, MAX1419, quantized the S/H's differential outputs.

3.7.3 Measurement Results

Fig. 3.14 plots the fundamental together with HD2, HD3, HD4, and HD5 versus input frequency for each of the four S/Hs on the test chip for a sample rate of 19

MSPS and an input amplitude -7 dBFS, relative to the MAX1419's 2.56 V peak to peak full scale range. Fig. 3.15 plots the same for S/H #4, $C_H = 4$pF, for sample rates of 13 and 31 MSPS. Twenty dB per decade asymptotes are shown for clarity.



(a) S/H # 1, $C_H = 0.5pF$ (b) S/H # 2, $C_H = 1pF$

(c) S/H # 3, $C_H = 2pF$ (d) S/H # 4, $C_H = 4pF$

Figure 3.14: Measured fundamental, HD2, HD3, HD4, and HD5 versus input frequency at $F_s = 19MSPS$.

With approximately the same input amplitude, the four plots in Fig. 3.14 demonstrate the effects of increasing the sampling capacitor size. As shown in Table 3.1, roughly the predicted 6 dB change was measured for each doubling of capacitor size, when taken from the mid frequency region, showing the predicted

20 dB per decade slope. Since the smallest capacitor, $C_H = 0.5$pF on S/H #1, is more susceptible to parasitics, the change from S/H #1 to S/H #2 measured less than the expected 6 dB change. HD2, HD3, and HD4 for the other two transitions all measured slightly less than 6 dB change. HD5 differed by roughly 4.5 dB for all three transitions.

As the sampling capacitor increased, the curves shifted lower in frequency, exposing high frequency behavior, around the 3 dB bandwidth and beyond. For all six plots in Fig. 3.14 and 3.15, HD2 peaks near the 3 dB bandwidth, before decreasing at 20 dB per decade, as the proposed model predicts. HD3, HD4, and HD5, however, each peaks at slightly lower frequency than the previous, before decreasing at progressively faster rates, both results that the proposed model does not predict, but the transistor level simulation of the simple NMOS switch predicted.

Low frequency behavior has two competing causes: 1) charge injection as a result of the absence of differential cancellation from the single-ended sampling and 2) nonlinear exponential settling for larger sampling capacitors and faster sample rates. Table 3.2 lists the low frequency, 200 kHz, values for HD2-HD5 on each S/H for sample rates of 13 and 19 MSPS as well as for a sample rate of 31 MSPS for S/H #4 with $C_H = 4p$F. For the first three S/Hs, there was negligible or very little change in HD2-HD5 by changing the sample rate. Doubling the sampling capacitor size yielded roughly a 6 dB improvement in linearity, strongly suggesting charge injection as the underlying cause and allowing for progressively larger regions where the predicted mid frequency behavior shows.

While doubling the sampling capacitor size decreased the proportional depen-

dence of the HD terms to charge injection, it also slowed down the circuit, eventually to the point where low frequency nonlinear exponential settling became the dominant source of distortion. This is the case for S/H #4 at sample rates of 19 MSPS and 31 MSPS. Whereas the low frequency asymptotes previously decreased with increasing capacitance, here it went up. Moreover, increasing the sampling rate from 19 MSPS to 31 MSPS brought the levels up farther. Lowering the sampling rate from 19 MSPS to 13 MSPS had the opposite effect, pushing the nonlinear exponential settling almost out of measurable range.

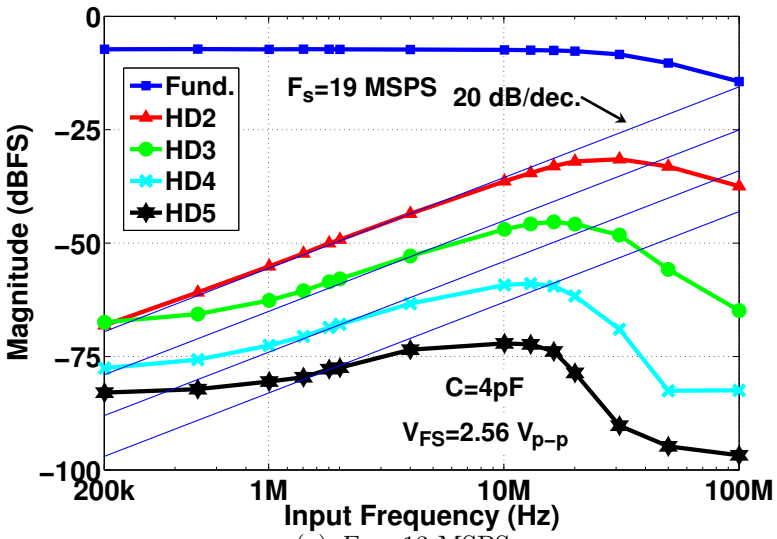
Table 3.1: $F_s = 19MSPS$ Mid Frequency Harmonic Distortion in dBFS.

	$f_{in} = 20MHz$			$f_{in} = 10MHz$			$f_{in} = 2MHz$		
	S/H #1	S/H #2	Δ	S/H #2	S/H #3	Δ	S/H #3	S/H #4	Δ
Fund.	-6.99	-7.14	-	-7.28	-7.18	-	-7.26	-7.28	-
HD2	-44.32	-40.71	3.61	-47.17	-41.33	5.84	-55.08	-49.23	5.85
HD3	-51.91	-45.58	6.33	-55.51	-50.25	5.26	-63.32	-57.88	5.44
HD4	-63.75	-60.60	3.15	-66.45	-60.65	5.80	-73.53	-67.91	5.62
HD5	-72.87	-68.65	4.22	-75.31	-70.81	4.50	-82.18	-77.45	4.73

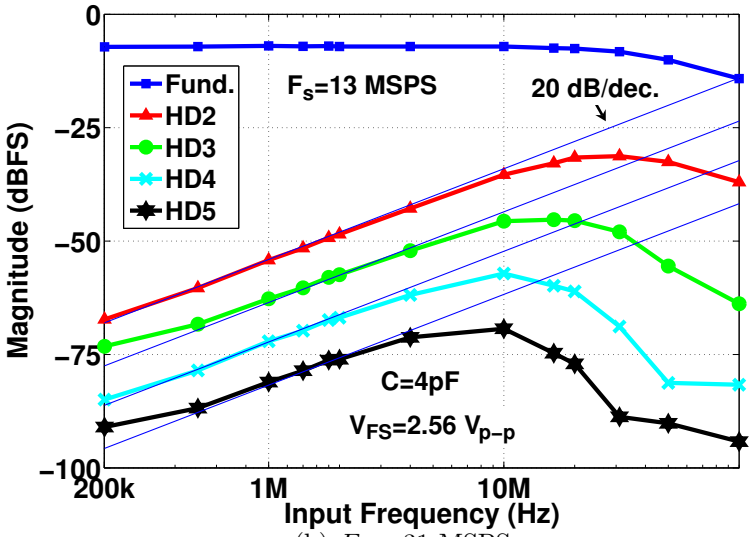
Table 3.2: Low Frequency, $f_{in} = 200kHz$, Harmonic Distortion, dBFS, due to charge injection and exponential settling.

	S/H #1, $C = 0.5pF$		S/H #2, $C = 1pF$		S/H #3, $C = 2pF$		S/H #4, $C = 4pF$		
	$F_s = 13M$	$F_s = 19M$	$F_s = 13M$	$F_s = 19M$	$F_s = 13M$	$F_s = 19M$	$F_s = 13M$	$F_s = 19M$	$F_s = 31M$
Fund.	-7.29	-7.47	-7.19	-7.36	-7.19	-7.39	-7.18	-7.27	-7.25
HD2	-49.76	-50.11	-57.77	-57.93	-63.79	-66.24	-67.27*	-67.43*	-52.56
HD3	-60.39	-61.08	-67.26	-67.88	-73.48	-72.23	-73.2*	-68.10	-55.71
HD4	-76.40	-77.40	-81.60	-83.32	-85.13	-88.03	-84.95*	-77.56	-64.36
HD5	-88.21	-90.87	-99.00	-98.77	-97.32	-98.96	-90.99*	-82.97	-71.93

* Low frequency asymptote not yet reached.



(a) $F_s = 13$ MSPS



(b) $F_s = 31$ MSPS

Figure 3.15: Measured fundamental, HD2, HD3, HD4, and HD5 vs. Input Frequency on S/H #4, $C_H = 4pF$.

3.8 Conclusion

A novel model that predicts harmonic distortion for weakly nonlinear open-loop sampling circuits with a dominant pole has been derived. The model facilitates

understanding of the mechanisms of harmonic distortion by breaking them down into amplitude modulation, phase modulation, nonlinear exponential settling and discrete time modulation, predicting dominant behavior over three frequency regions. For most practical circuit implementations, the proposed model predicts all harmonics will typically increase at 20 dB per decade approaching the 3 dB bandwidth; here the mathematics necessary to apply the model to practical circuits is reduced to the equivalent of frequency-independent nonlinearity analysis. The first analysis to predict and quantify a tradeoff between thermal noise and linearity due to competing bandwidth and amplitude trends was presented. Measured data from a prototype S/H chip fabricated in a 1P5M CMOS process as well as transistor level simulations support the results.

3.9 Harmonic Distortion Derivation

The derivation of HD expressions is broken down into sections according to frequency range because the dominant contributors vary from region to region. Within each region, the component with the largest magnitude dominates, though other contributions remain present. Weak NL is interpreted conservatively to mean that SFDR $>$ 30dBc. The overall HD is the root sum square of the summation of all terms. Furthermore, all HD expressions are expressed relative to the *input* fundamental.

3.9.1 Mid Frequency Harmonic Distortion Model

Introducing a nonlinear time constant to the sampling circuit presented in Fig. 3.1 leads to a FR

$$\hat{V}_{o,F}(t) = \frac{A}{\sqrt{1+\omega^2\hat{\tau}^2(V_{in})}}\cos(\omega t + \phi - \hat{\theta}(V_{in})) \tag{3.36}$$

where $\hat{\theta}(V_{in}) = \arctan(\omega\hat{\tau}(V_{in}))$. Setting the arbitrary phase to zero for mathematical convenience, $\phi = 0$, applying trigonometric identities and rearranging, (3.36) becomes

$$\hat{V}_{o,F}(t) = A\frac{\cos(\omega t) + \omega\hat{\tau}(V_{in})\sin(\omega t)}{1+\omega^2\hat{\tau}^2(V_{in})}. \tag{3.37}$$

Approximating the nonlinear amplitudes for $\omega\hat{\tau}(V_{in}) \ll 1$ such that $1/(1+x) \approx 1 - x + x^2 - \cdots$, (3.37) becomes

$$\begin{aligned}\hat{V}_{o,F}(t) \approx A\Big[&(1-\omega^2\hat{\tau}^2+\omega^4\hat{\tau}^4-\cdots)\cos(\omega t)\\ &+(\omega\hat{\tau}-\omega^3\hat{\tau}^3+\omega^5\hat{\tau}^5-\cdots)\sin(\omega t)\Big].\end{aligned} \tag{3.38}$$

Rewriting (3.38), substituting (3.6) and (3.2) with $\phi = 0$, applying trigonometric identities,

$$\begin{aligned}\hat{V}_{o,F}(t) \approx\ & A\cos(\omega t) + A\sin(\omega t)\sum_{i=0}^{\infty}\sum_{n}^{odd}\omega^n\beta_{i,n}\cos(i\omega t)\\ &+A\cos(\omega t)\sum_{i=0}^{\infty}\sum_{n}^{even}\omega^n\beta_{i,n}\cos(i\omega t).\end{aligned} \tag{3.39}$$

Table 3.3: Expansion of $\beta_{i,n}$ terms in (3.39) for each Harmonic

Harmonic	$\omega\hat{\tau}$ $(n=1)$	$(\omega\hat{\tau})^{\mathbf{2}}$ $(n=2)$	$\cdots$
$-$	$\beta_{0,1} = \tau_o + \frac{1}{2}\alpha_2 A^2 + \frac{3}{8}\alpha_4 A^4 + \frac{5}{16}\alpha_6 A^6 + \cdots$	$\beta_{0,2} = \tau_o^2 + (\tau_o\alpha_2 + \frac{1}{2}\alpha_1^2)A^2 + (\frac{3}{8}\alpha_2^2 + \frac{3}{4}\alpha_1\alpha_3)A^4 + \frac{5}{16}\alpha_3^2 A^6 + \cdots$	$\cdots$
$\mathbf{2}\omega(\mathbf{i}=\mathbf{1})$	$\beta_{1,1} = \alpha_1 A + \frac{3}{4}\alpha_3 A^3 + \frac{5}{8}\alpha_5 A^5 + \frac{35}{64}\alpha_7 A^7 + \cdots$	$\beta_{1,2} = 2\tau_o\alpha_1 A + \frac{3}{2}(\tau_o\alpha_3 + \alpha_1\alpha_2)A^3 + \frac{5}{4}\alpha_2\alpha_3 A^5 + \cdots$	$\cdots$
$\mathbf{3}\omega(\mathbf{i}=\mathbf{2})$	$\beta_{2,1} = \frac{1}{2}\alpha_2 A^2 + \frac{1}{2}\alpha_4 A^4 + \frac{15}{32}\alpha_6 A^6 + \cdots$	$\beta_{2,2} = (\tau_o\alpha_2 + \frac{1}{2}\alpha_1^2)A^2 + (\alpha_1\alpha_3 + \frac{1}{2}\alpha_2^2)A^4 + \frac{15}{32}\alpha_3^2 A^6 + \cdots$	$\cdots$
$\mathbf{4}\omega(\mathbf{i}=\mathbf{3})$	$\beta_{3,1} = \frac{1}{4}\alpha_3 A^3 + \frac{5}{16}\alpha_5 A^5 + \frac{21}{64}\alpha_7 A^7 + \cdots$	$\beta_{3,2} = \frac{1}{2}(\tau_o\alpha_3 + \alpha_1\alpha_2)A^3 + \frac{5}{8}\alpha_2\alpha_3 A^5 + \cdots$	$\cdots$
$\mathbf{5}\omega(\mathbf{i}=\mathbf{4})$	$\beta_{4,1} = \frac{1}{8}\alpha_4 A^4 + \frac{3}{16}\alpha_6 A^6 + \cdots$	$\beta_{4,2} = (\frac{1}{4}\alpha_1\alpha_3 + \frac{1}{8}\alpha_2^2)A^4 + \frac{3}{16}\alpha_3^2 A^6 + \cdots$	$\cdots$
$\mathbf{6}\omega(\mathbf{i}=\mathbf{5})$	$\beta_{5,1} = \frac{1}{16}\alpha_5 A^5 + \frac{7}{64}\alpha_7 A^7 + \cdots$	$\beta_{5,2} = \frac{1}{8}\alpha_3\alpha_2 A^5 + \cdots$	$\cdots$
$\vdots$	$\vdots$	$\vdots$	$\ddots$

*** Note that $\beta_{i,n}$ are negative for $n \in 2, 3, 6, 7, \cdots$**

Table 3.3 defines the $\beta_{i,n}$ terms, with units of $(seconds^n)$, where the index i refers to the harmonic location, $(i+1)\omega$, and the index n corresponds to the power of $\hat{\tau}$ in (3.38). As (3.39) is in the form of AM (carrier present), the HD terms are

$$\text{HDj} \approx \frac{1}{2}\sum_{n=1}^{\infty} \omega^n \beta_{i,n}, \tag{3.40}$$

where $j = i + 1$. Note that (3.40) presumes that $\beta_{0,n} \ll 1$ for simplicity, but may be taken into account by including this additional energy at the fundamental frequency, combined with the input accordingly, in the denominator.

3.9.2 High Frequency Harmonic Distortion Model

When $\omega\tau_o \gg 1$, (3.37) may be approximated as

$$\hat{V}_{o,F} \approx A\left[\frac{1}{\omega^2\hat{\tau}^2(V_{in})}\cos(\omega t) + \frac{1}{\omega\hat{\tau}(V_{in})}\sin(\omega t)\right]. \tag{3.41}$$

Since both the first and second order ω terms in (3.41) have the same magnitude at $\omega\tau_o = 1$, the second order term quickly becomes insignificant with increasing frequency and is dropped. Dividing (3.6) by τ_o, assuming that $\tau_o \gg |\alpha_k A^k|$,

$$\hat{V}_{o,F} \approx \frac{A\sin(\omega t)}{\omega\tau_o(1 + \frac{\alpha_1}{\tau_o}V_{in} + \frac{\alpha_2}{\tau_o}{V_{in}}^2 + \cdots)}. \tag{3.42}$$

Once again applying the series expansion $1/(1+x) \approx 1 - x + x^2 - \cdots$ and trigonometric identities, (3.42) becomes

$$\hat{V}_{o,F} \approx \frac{A}{\omega\tau_o}\left(1 - \sum_{i=1}^{\infty}\sum_{n=1}^{\infty}\frac{\beta_{i,n}}{{\tau_o}^n}\cos(\omega t)\right)\sin(\omega t). \tag{3.43}$$

This equation is now in the form of AM (carrier present). Thus the HD terms beyond the 3 dB bandwidth are approximately

$$\mathrm{HD_j} \approx \frac{1}{2}\sum_{n=1}^{\infty}\frac{\beta_{i,n}}{\omega{\tau_o}^{n+1}}. \tag{3.44}$$

3.9.3 Low Frequency Harmonic Distortion Model

The natural response may be expressed as

$$\hat{V}_{o-N}(V_{in}) = \frac{\tilde{A}}{1+\omega\hat{\tau}} e^{-T_s/\hat{\tau}}, \tag{3.45}$$

where $\tilde{A} = V_{c0} - A$ for a non-resetting circuit that accounts for the initial condition. When there is discrete-time modulation, $\tilde{A} = -A$, and the initial condition is handled in Appendix 3.9.4. Using the series expansion applied for the mid and high frequency regions yields

$$\hat{V}_{o-N}(V_{in}) = \tilde{A}\left(1 - \omega\hat{\tau} + \omega^2\hat{\tau}^2 - \cdots\right) e^{-T_s/\hat{\tau}}. \tag{3.46}$$

The AM terms may be dropped since they are much smaller than unity in this frequency range. Taking the Taylor series expansion about $V_{in} = 0$:

$$\hat{V}_{o-N}(V_{in}) = \tilde{A} e^{-T_s/\tau_o}\left[1 + \sum_{l}^{1,2,\cdots} k_l(\alpha_i) {V_{in}}^l\right], \tag{3.47}$$

where k_l are the (factored) Taylor coefficients (Table 3.4). Substituting (3.2) with $\phi = 0$ into (3.47) and applying trigonometric identities,

$$\hat{V}_{o-N}(V_{in}) = \tilde{A} e^{-T_s/\tau_o}\left[1 + \sum_{i}^{1,2,\cdots} \chi_i(k_l(\alpha_i))\cos(i\omega t)\right], \tag{3.48}$$

Table 3.4: Taylor Coefficients of $V_{o-N}(V_{in})$

l	$k_l(\alpha_i)$
1	$T_s\alpha_1/{\tau_o}^2$
2	$T_s\left(2\alpha_2{\tau_o}^2 - 2\tau_o{\alpha_1}^2 + T_s{\alpha_1}^2\right)/2{\tau_o}^4$
3	$T_s\left(6{\tau_o}^4\alpha_3 - 12{\tau_o}^3\alpha_1\alpha_2 + 6{\tau_o}^2{\alpha_1}^3 + 6{\tau_o}^2T_s\alpha_1\alpha_2 - 6T_s{\alpha_1}^3\tau_o + {T_s}^2{\alpha_1}^3\right)/6{\tau_o}^6$
4	$-T_s(48{\tau_o}^5\alpha_1\alpha_3 + 24{\tau_o}^5{\alpha_2}^2 - 72{\tau_o}^4\alpha_2{\alpha_1}^2 + 24{\tau_o}^3{\alpha_1}^4 - 24T_s\alpha_1{\tau_o}^4\alpha_3 + 72T_s{\alpha_1}^2{\tau_o}^3\alpha_2$ $-36T_s{\alpha_1}^4{\tau_o}^2 - 12T_s{\tau_o}^4{\alpha_2}^2 - 12{T_s}^2{\tau_o}^2{\alpha_1}^2\alpha_2 + 12{T_s}^2\tau_o{\alpha_1}^4 - {T_s}^3{\alpha_1}^4)/24{\tau_o}^{-8}$
$\vdots$	$\vdots$

Table 3.5: Expansion of $\chi(k_l)$

i	Harmonic	$\chi_i(k_l(\alpha_i))$
1	2ω	$k_2A^2/2 + k_4A^4/2 + 15k_6A^6/32 + \cdots$
2	3ω	$k_3A^3/4 + 5k_5A^5/16 + \cdots$
$\vdots$	$\vdots$	$\vdots$

where the dimensionless $\chi_i(k_l)$ terms are defined in Table 3.5. Low frequency HD is then

$$\text{HDj} \approx \frac{1}{2}\frac{\tilde{A}}{A}e^{-T_s/\tau_o}\chi_i(k_l(\alpha_i)). \tag{3.49}$$

3.9.4 Discrete-time Modulation

Sampling (3.3) and expanding term 1 of (3.3) with the Taylor Series presented in Appendix 3.9.3, the output becomes

$$\begin{aligned}\hat{V}_o(n) = {} & \hat{V}_{o-ZS}(n) \\ & + \hat{V}_o(n-1)e^{-T_s/\tau_o}\left[1 + \sum_{l=1}^{\infty} k_l {V_{in}}^l(n)\right].\end{aligned} \tag{3.50}$$

Table 3.6: Expansion of $d(k_l(\alpha_i))$

i	Harmonic	$d_i(k_l)$
1	2ω	$k_1 A + \frac{3}{4}k_3 A^3/2 + \cdots$
2	3ω	$\frac{1}{2}k_2 A^2/4 + \frac{1}{2}k_4 A^4 + \cdots$
3	4ω	$\frac{1}{4}k_3 A^3 + \frac{5}{16}k_5 A^5 + \cdots$
4	5ω	$\frac{1}{8}k_4 A^4 + \frac{3}{16}k_6 A^6 + \cdots$
$\vdots$	$\vdots$	$\vdots$

$\hat{V}_{o-ZS}(n)$ is the sampled ZS output, including the spurs characterized in Appendix 3.9.1, 3.9.2 and 3.9.3. The nonlinearity modulates the previous output. Invoking the weak linearity presumption, $\hat{V}_{o-ZS}$ may be approximated as V_{in}. Then

$$\begin{aligned}\hat{V}_o(n) \approx V_{in}(n) \\ +\hat{V}_o(n-1)e^{-T_s/\tau_o}\left[1+\sum_{l=1}^{\infty} k_l {V_{in}}^l(n)\right].\end{aligned} \tag{3.51}$$

Eq. (3.51) shows the same linear low pass filter as before, along with modulation of the previous output with the series expansion of the nonlinearly decaying ZI exponential. As long as the 3 dB bandwidth is well beyond the sample rate,

$$\text{HDj} \approx \frac{1}{2}e^{-T_s/\tau_o}d_i, \tag{3.52}$$

where d_i are shown in Table 3.6.

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Chapter 4 – Conclusion and Directions for Future Work

4.1 Conclusion

Two aspects of analog to digital converter systems have been addressed. The first aspect is the low energy and power design of an ADC and reference voltage for remote sensing. Next, frequency dependent sampling linearity of an ADC's input network is analyzed.

Low energy and power design analog design techniques for remote sensing applications were demonstrated in the context of a 9 bit, 20 kSPS ADC and 530 mV reference voltage with a combined power consumption of 11 μW. The combined power consumption, resolution and sample rate demonstrate the essential components for digitization of sensors for energy constrained systems.

Second, a detailed mathematical analysis of an ADC's sampling network was performed versus the input frequency, the sample rate and the specific component nonlinearity. The analyzes improve design insight was obtained for common practical sampling networks. Furthermore, a fundamental trade-off between linearity and thermal noise was derived.

4.2 Directions for Future Work

4.2.1 Nano-Joule ADC

A variety of applications could benefit from adaptations of the low energy and power design techniques developed in this work. These applications include various forms of monitoring where small (battery) size and low available energy are critical criteria. Examples are bio-medical, home energy management, building monitoring, environmental monitoring, military, and bridge stress monitoring. For each application, specific tailoring of an ADC, reference voltage and sensor input, or even embedding the sensor on-chip would make it possible to provide solutions where it is not possible today due to constraints in the power and energy budgets.

The need that the lower power design techniques can specifically fulfill is that of a universal interface for analog inputs because real world digital systems need ADCs. Various input types with differing input voltage spans and dynamic ranges would have to be quantized. This necessitates reconfigurability in the ADC system to simultaneously optimize the power consumption for both low and high dynamic range signals. Traditionally, this has been a difficult problem because settling, matching, and power requirements change substantially for low and high resolution applications. An example of a possible implementation is to reconfigure the cyclic ADC presented in this work to operate as a second order $\Delta\Sigma$ modulator for increased dynamic range at the expense of speed. Alternatively, an incremental ADC variation of a $\Delta\Sigma$ modulator may be chosen for improved DC accuracy and linearity.

By integrating sensor interfaces into the ADC and reference system, power and area savings are possible for these applications. In doing so, the smaller physical size of the system would enable functionality not possible today. Medical examples include heart rate and body temperature monitoring. Similarly, for military or first responders, the health of a soldier or firefighter could be monitored in real time and transmitted back to a command center. For buildings and bridges, long term stress, temperature and pressure logging become possible with minimal source energy to power the system.

4.2.2 Sampling Linearity

The underlying technique of modeling nonlinearity in a system with memory (frequency dependent) as modulating the linear response can be extended to other classes of circuits. Digital to analog converters are an obvious example. Another possibility is amplifier stages, both simple common-source amplifier and operational amplifiers. In each case, simplifying frequency-dependent nonlinearity to just a Taylor series expansion would represent a considerable simplification compared to a Volterra series based analysis.

References

[1] M. D. Scott, B. E. Boser, and K. S. J. Pister, "An ultra-low energy ADC for smart-dust," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 123–1129, Jul. 2003.

[2] M. Flatscher, M. Dielacher, T. Herndl, T. Lentsch, R. Matischek, J. Prainsack, W. Pribyl, H. Theuss, and W. Weber, "A robust wireless sensor node for intire-pressure monitoring," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, feb. 2009, pp. 286 –287,287a.

[3] J. Ayers, N. Panitantum, K. Mayaram, and T. Fiez, "A 2.4Ghz wireless transceiver with 0.95nJ/b link energy for multi-hop battery-free wireless sensor networks," in *2010 IEEE Symposium on VLSI Circuits (VLSIC)*, jun. 2010, pp. 29 –30.

[4] J. Ayers, K. Mayaram, and T. Fiez, "An ultra-low-power receiver for wireless sensor networks," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1759 –1769, sept. 2010.

[5] Y.-T. Liao., H. Yao, B. Parviz., and B. Otis, "A 3μW wirelessly powered CMOS glucose sensor for an active contact lens," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, feb. 2011, pp. 38–39.

[6] S. Lee, L. Yan, T. Roh, S. Hong, and H.-J. Yoo, "A 75 μW real-time scalable network controller and a 25 μw ExG sensor IC for compact sleep-monitoring applications," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, feb. 2011, pp. 36 –37.

[7] T. Le, J. Han, A. von Jouanne, K. Mayaram, and T. Fiez, "Piezoelectric micro-power generation interface circuits," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1411 – 1420, june 2006.

[8] T. Le, K. Mayaram, and T. Fiez, "Efficient far-field radio frequency energy harvesting for passively powered sensor networks," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1287 –1302, may 2008.

[9] S. Gambini and J. Rabaey, "Low-power successive approximation converter with 0.5 v supply in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2348–2356, Nov. 2007.

[10] B. Bond, T. Fiez, L. Mahrt, H. Liu, and T. T. Dietterich, "Sensor: A wireless network of energy-passive sensors to explore bio-atmoshphere interactions in complex environments," *NSF Proposal 0330274*, feb. 2004.

[11] "FCC codes of regulation, part 15." [Online]. Available: http://www.fcc.gov/oet/rules/part15/part15_8_23_02.pdf

[12] M. Hata, "Emperical formula for propagation loss in land mobile radio services," *IEEE Trans. on Vehicular Technology*, vol. VT-29, no. 9, pp. 137–325, Aug. 1980.

[13] D. Kasha, W. Lee, and A. Thomsen, "A 16-mW,120-dB linear switched-capacitor delta-sigma modulator with dynamic biasing," *IEEE J. Solid-State Circuits*, vol. 34, no. 2, pp. 921–926, Jul. 1999.

[14] N. Krishnapura and Y. Tsividis, "Noise and power reduction in filters through the use of adjustable biasing," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1912–1920, Dec. 2001.

[15] H. Yang and D. Allstot, "Considerations for fast settling operational amplifiers," *IEEE Transactions on Circuits and Systems*, vol. 37, no. 3, pp. 326 –334, mar 1990.

[16] U. Chilakapati and T. Fiez, "Settling time design considerations for sc integrators," in *Proceedings of the 1998 IEEE International Symposium on Circuits and Systems*, vol. 1, jun 1998, pp. 492 –495.

[17] V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, and W. Sansen, "A 900-mv low-power $\Delta\Sigma$ A/D converter with 77-db dynamic range," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1887–1897, dec 1998.

[18] Y. Hu, Z. Lu, Z. Lu, and M. Sawan, "A low-voltage 38μw sigma-delta modulator dedicated to wireless signal recording aplications," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, Jan. 2003, pp. I1073–I1076.

[19] R. L. Reverend, I. Kale, G. Delight, D. Morling, and S. Morris, "An ultra-low power double-sampled A/D MASH $\Delta\Sigma$ modulator," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, Jan. 2003, pp. I1001–I1004.

[20] F. Chen and B. Leung, "A 0.25-mw low-pass passive sigma-delta modulator with built-in mixer for a 10-mhz IF input," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 774–782, jun 1997.

[21] S. Kiriaki, "A 0.25mw sigma-delta modulator for voice-band applications," in *Symposium on VLSI Circuits, Digest of Technical Papers*, Jun. 1995, pp. 35–36.

[22] P. Rombouts, W. D. Wilde, and L. Weyten, "A 13.5-b 1.2-v micro-power extended counting A/D converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 2, pp. 308–319, feb 2001.

[23] H. Rapakko and J. Kostamovaara, "Micro-power 10-bit sigma-delta A/D-converter," in *Proceedings of the 1998 IEEE International Symposium on Circuits and Systems*, 1998, pp. 341–I343.

[24] J. Sauerbrey, D. Schmitt-Landsiedel, and R. Thewes, "A 0.5-v 1-μw successive approximation ADC," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 1261–1265, dec 2003.

[25] J. Sauerbrey, T. Tille, D. Schmitt-Landsiedel, and R. Thewes, "A 0.7-v MOSFET-only switched-opamp $\Delta\Sigma$ modulator in standard digital CMOS technology," *IEEE J. Solid-State Circuits*, vol. 37, no. 4, pp. 1662–1669, dec 2002.

[26] F. Gerfers, M. Ortmanns, and Y. Manoli, "A 1.5-v 12-bit power-efficient continuous-time third-order $\Delta\Sigma$ modulator," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 1343–1352, dec 2003.

[27] S. Mortezapour and K. Lee, "A 1-v, 8-bit successive approximation ADC in standard CMOS process," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 642–646, apr 2000.

[28] J. Sit and R. Sarpeshkar, "A micropower logarithmic A/D with offset and temperature compensation," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 308–319, feb 2004.

[29] S. Au and B. Leung, "A 1.95-v, 0.34-mw, 12-b sigma-delta modulator stabilized by local feedback loops," *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 321–328, mar 1997.

[30] Y. Chae and G. Han, "A low power sigma-delta modulator using class-c inverter," in *Symposium on VLSI Circuits, Digest of Technical Papers*, june 2007, pp. 240 –241.

[31] S.-K. Lee, S.-J. Park, Y. Suh, H.-J. Park, and J.-Y. Sim, "A 1.3 μw 0.6v 8.7-ENOB successive approximation ADC in a 0.18 μm CMOS," in *Symposium on VLSI Circuits, Digest of Technical Papers*, june 2009, pp. 242 –243.

[32] K. Sanborn, D. Ma, and V. Ivanov, "A sub-1-v low-noise bandgap voltage reference," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2466–2481, nov 2007.

[33] B. Murmann, "ADC performance survey 1997-2011." [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html

[34] D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: John Wiley & Sons, Inc., 1997.

[35] H. Lee, "A 12b 600 ks/s digitally self-calibrated pipelined algorithmic ADC," *IEEE J. Solid-State Circuits*, vol. 29, no. 4, pp. 509–515, Apr. 1994.

[36] B. R. Gregoire and U.-K. Moon, "An over-60 dB true rail-to-rail performance using correlated level shifting and an opamp with only 30 dB loop gain," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2620–2630, Dec. 2008.

[37] C. Enz and G. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584 –1614, Nov. 1996.

[38] A. M. Abo and P. R. Gray, "A 1.5-v, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1998.

[39] A. J. López-Martín, S. Baswa, J. Ramirez-Angulo, and R. G. Carvajal, "Low-voltage super class AB CMOS OTA cells with very high slew rate and power efficiency," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1068–1077, May 2005.

[40] Y. Tsividis, "Accurate analysis of temperature effects in $I_c - V_{BE}$ characteristics with application to bandgap reference sources," *IEEE J. Solid-State Circuits*, vol. SC-15, no. 6, pp. 1076–1084, Dec. 1980.

[41] G. Ge, C. Zhang, G. Hoogzaad, and K. Makinwa, "A single-trim CMOS bandgap reference with a 3σ inaccuracy of $\pm 0.15\%$ from -40c to 125c," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2010, pp. 78–79.

[42] P. K. Mok and K. N. Leung, "Design considerations of recent advanced low-voltage low-temperature-coefficient CMOS bandgap voltage reference," *2004 IEEE Custom Integrated Circuits Conference*, pp. 635–642, Oct. 2004.

[43] P. Kinget, C. Vezyrtzis, E. Chiang, B. Hung, and T. Li, "Voltage references for ultra-low supply voltages," *2008 IEEE Custom Integrated Circuits Conference*, pp. 715–720, Sep. 2008.

[44] H.-W. Huang, C.-Y. Hsieh, K.-H. Chen, and S.-Y. Kuo, "A 1v 16.9ppm/^{o}c 250nA switched-capacitor CMOS voltage reference," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2008, pp. 438–439.

[45] D. Daly and A. Chandrakasan, "A 6-bit, 0.2 v to 0.9 v highly digital flash adc with comparator redundancy," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3030 –3038, nov. 2009.

[46] M. Yip and A. Chandrakasan, "A resolution-reconfigurable 5-to-10b 0.4-to-1v power scalable sar adc," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, feb. 2011, pp. 190 –192.

[47] S. Schetzen, *The Volterra and Wiener Theories of Nonlinear Systems.* J. Wiley & Sons, 1980.

[48] P. Wambacq and W. Sansen, *Distortion Analysis of Analog Inetgrated Circuits.* Boston: Kluwer Academic Publishers, 1998.

[49] B. Hernes and T. Sæ ther, *Design Criteria for Low Distortion in Feedback OpAmp Circuits.* Boston: Kluwer Academic Publishers, 2003.

[50] R. G. Meyer, M. J. Shensa, and R. Exchenbach, "Cross modulation and intermodulation in amplifiers at high frequencies," *IEEE J. Solid-State Circuits*, vol. sc-7, no. 1, pp. 16–23, Feb. 1972.

[51] W. M. Sansen and R. G. Meyer, "Distortion in bipolar transistor variable-gain amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-8, pp. 275–282, Aug. 1973.

[52] A. M. Khadr and R. H. Johnston, "Distortion in high-frequency FET amplifiers," *IEEE J. Solid-State Circuits*, vol. sc-9, no. 4, pp. 180–189, Aug. 1974.

[53] C.-S. Yen, "High-frequency distortion in emitter-driven variable-gain pairs," *IEEE J. Solid-State Circuits*, vol. SC-15, no. 3, pp. 375–377, Jun. 1980.

[54] F. O. Eynde, P. Wambacq, and W. Sansen, "On the relationship between the CMRR or PSRR and the second harmonic distortion in differential amplifiers," *IEEE J. Solid-State Circuits*, vol. 24, no. 6, pp. 1740–1744, Dec. 1989.

[55] K. L. Fong and R. G. Meyer, "High-frequency nonlinearity analysis of common-emitter and differential-pair transconductance stages," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 548–555, Apr. 1998.

[56] P. Wambacq, G. G. E. Gielen, P. R. Kinget, and W. Sansen, "High-frequency distortion analysis of analog integrated circuits," *IEEE Trans. Circuits Syst. II*, vol. 46, no. 3, pp. 335–345, Mar. 1999.

[57] D. Aksin and F. Maloberti, "Very high-speed BJT buffer for track-and-hold amplifiers with enhanced linearity," in *Proceedings of the 2002 International Symposium on Circuits and Systems*, May 2002, pp. 569–572.

[58] R. A. Baki, C. Beainy, and M. N. El-Gamal, "Distortion analysis of high-frequency log-domain filters using volterra series," *IEEE Trans. Circuits Syst. II*, vol. 50, no. 1, pp. 1–11, Jan. 2003.

[59] G. Palumbo and S. Pennisi, "High-frequency harmonic distortion in feedback amplifiers: Analysis and applications," *IEEE Trans. Circuits Syst. II*, vol. 50, no. 3, pp. 328–340, Mar. 2003.

[60] Y. Palaskas and Y. Tsividis, "Dynamic range optimization of weakly nonlinear, fully balanced, Gm-C filters with power dissapation constraints," *IEEE Trans. Circuits Syst. II*, vol. 50, no. 10, pp. 714–727, Oct. 2003.

[61] A. Gothenberg and H. Tenhunen, "Performance analysis of sampling switches in voltage and frequency domains using Volterra series," in *Proceedings of the 2004 International Symposium on Circuits and Systems*, May 2004, pp. 765–768.

[62] J. Chen, E. Sánchez-Sinencio, and J. Silva-Martinez, "Frequency-dependent harmonic-distortion analysis of a linearized cross-coupled CMOS OTA and its application to OTA-C filters," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 3, pp. 499–510, Mar. 2006.

[63] S. O. Cannizzaro, G. Palumbo, and S. Pennisi, "Effects of nonlinear feedback in the frequency domain," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 2, pp. 225–234, Feb. 2006.

[64] J.-H. Chun and B. Murmann, "Analysis and measurement of signal distortion due to ESD protection circuits," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2354–2358, Oct. 2006.

[65] S. O. Cannizzaro, G. Palumbo, and S. Pennisi, "Distortion analysis of miller-compensated three-stage amplifiers," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 5, pp. 961–976, May 2006.

[66] J. Vuolevi, "Analysis, measurement and cancellation of the bandwidth and amplitude dependence intermodulation distortion in RF power amplifiers," Ph.D. dissertation, University of Oulu, Oulu, Finland, Nov. 2001.

[67] W. Huang and E. Sánchez-Sinencio, "Robust highly linear high-frequency CMOS OTA with IM3 below - 70 db at 26 MHz," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 7, pp. 1433–1447, Jul. 2006.

[68] T. Brown, M. Hakkarainen, and T. S. Fiez, "Prediction and characterization of frequency dependent MOS switch linearity and the design implications," *2006 IEEE Custom Integrated Circuits Conference*, pp. 237–240, Sep. 2006.

[69] A. V. Oppenheim and A. S. Wilsky, *Signals and Systems*, 2nd ed. Englewood Cliffs, NJ: Prentice Hall, 1975.

[70] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 1st ed. Cambridge, UK: Cambridge University Press, 1998.

[71] E. Siragusa and I. Galton, "A digitially enhanced 1.8v 15b 40 MS/s CMOS ADC," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2004, pp. 452–453.

[72] P. Bendix, P. Rakers, L. Lemaitre, W. Grabinski, C. C. McAndrew, X. Gu, and G. Gildenblat, "RF distortion analysis with compact MOSFET models," *2004 IEEE Custom Integrated Circuits Conference*, pp. 9–12, Oct. 2004.