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Abstract approved:

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Huaping Liu

Powerline communication (PLC), is becoming a more commonplace method for data transmission, however it is still a very new medium for data transmission, and international standards for powerline communication are still in the process of being developed and established. PLC can provide a means of simplifying the device connectivity to a network by reducing the dedicated wiring needed for communication channels, as well as provide a means for communication between devices that may have previously been impractical. With limited previous research regarding PLC transmission on low voltage direct current (DC) powerlines, and virtually no previous research regarding PLC communication within a computer, the information provided in this thesis begins to take on significant importance to help lead to further advancements in the use of this communication method within a computer.

The objective of this thesis is to discuss the feasibility and design theory for developing a low-cost sensor communication network within a desktop personal computer (PC), utilizing the preexisting powerline architecture. First, the channel characterization of the computer powerline structure is presented and discussed. From this channel characterization, the optimum frequency range for the sensor network is selected. A modulation scheme and demodulation scheme are then discussed and simulated. Finally, the results of the simulation are discussed and a simple circuit implementation for the sensor network is realized.

Sensor Communication Network within a Desktop Computer using the DC Powerline

by
Eileen Kei Bahniuk

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

Director of the School of Electrical Engineering and Computer Science

Dean of the Graduate School

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Eileen Kei Bahniuk, Author

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In dedication to my grandparents who could not be here today; I only hope I have taken all the opportunity to learn the things that were not available to them because they lived in a different day in time; and to my beloved cat Bunza, who sat with me through all my studies.

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1 Introduction

Powerline communication (PLC) is rapidly becoming a more commonplace method for data transmission, however it is still a very new medium for data transmission and international standards for powerline communication are still in the process of being developed and established. The HomePlug Organization, established in March 2000, was created with the primary purpose of helping to develop industry specific standards for the use of powerlines for communication applications. In June 2005, the IEEE P1901 Working Group was established to help develop international, globally recognized credible standards for high-speed powerline communication, with a focus on the first-mile/last-mile connection of the broadband infrastructure [1-3].

The HomePlug Organization established the HomePlug 1.0 specification in November 2001, which provided for peak rates of 14 Mbps at the PHY layer [4]. Released in August 2005, the HomePlug AV standard was developed to support higher bandwidth entertainment applications such as: audio, voice, and video, and delivers raw data speeds of up to 200 Mbps at the PHY Layer, as well as improve the security from the initial standard.

February 2007, 400 requirements were split into three clusters. By June 2007, 12 proposals were received to help develop the P1901 standard. In October 2007, the first round of voting reduced the number of proposals down to one per cluster. By September 2008, the second round of voting and a voluntary proposal merger by HomePlug and Panasonic resulted in the final proposal [5]. July 2009, the first draft

of IEEE standard P1901 was established and delivered for comment; by January 2010, all comments were resolved and the first draft standard was published by IEEE [6]. The HomePlug AV2 standard is still in the process of being established and is expected for late 2010; it will be brought into the IEEE P1901 standard once the specification is complete and is expected to have rates of 600+ Mbps at the MAC layer [7, 8].

Standards and technology development for high data rate transmissions utilizing direct current (DC) powerline architecture within a vehicle also have a great deal of recent research, however, no PLC specific standard for in-vehicle use has been developed [9-14]. Protocols such as CAN (controller area network), LIN (local interconnected network), and FlexRay are some examples of standard protocols used to implement in-vehicle communication networks, however, these methods still require dedicated communication cabling in addition to powerline cabling. June 21, 1995, patent 5,727,025 was filed by Yair Maryanka of Yamar Ltd. for devices that are used to transmit voice, music, video and data over DC wires [15]. Yamar Electronics does have some currently available devices specifically for in-vehicle use to provide a means for powerline communication, however, the maximum PLC data rate currently achievable is only 500 Kbps, whereas a dedicated communication method such as FlexRay can provide throughput data rates of up to 10 Mbps [14]. HD-PLC (Panasonic PLC standard) and HPAV (HomePlug AV standard), the currently existing commercial PLC solutions, were both tested for in-vehicle feasibility; it was concluded that using these commercially existing PLC solutions for home network use

is not only feasible, but provided for higher data rates than the currently existing FlexRay and Yamar technologies [14].

Understanding the established and developing methods of PLC communication is essential in making network design decisions, as well as being able to establish a baseline of where to begin testing, what sort of design to expect, and what kinds of rates are likely to be attainable. Home powerlines and personal computer (PC) powerlines differ greatly, namely, the difference between AC and DC lines, the distance the communication signal will need to travel and voltages on the carrier line. They are also significantly different in that powerlines can be outside, buried, or located within a home or building structure, which can make them more susceptible to surrounding external noise interference, such as radio transmissions. Vehicular powerlines and PC powerlines, however, have more similarities. First, both have end-point to end-point lengths of less than 10 m; next, both use power supplies that provide less than 24 V; most importantly, they are both DC PLC networks contained within a metal chassis. With previous research establishing that implementing the HomePlug standard within a vehicle is not only achievable but provides for better rates than previously developed devices, there is no reason to doubt that it is feasible for a desktop PC as well.

With virtually no available previous research regarding the use of a DC powerline as a communication channel within a desktop computer, the research, simulations and results presented in this thesis become vital and necessary. As with powerline communication for home use and vehicular use, there are several

advantages that powerline communication will be able to offer within the desktop computer. With further development based on the research provided in this thesis, it may eventually become possible to simplify the connectivity of devices within the computer, reduce the dedicated communication wiring, and to provide a means of transmitting additional data between components that would have previously been impractical due to the additional cabling requirements.

The objective of this thesis is to explore the feasibility and design theory for developing a low-cost sensor communication network within a desktop PC, utilizing the preexisting powerline architecture. The proceeding chapters of this thesis will outline this objective with an individual discussion focused on the following key topics: previous PLC research leading to the baseline for design and channel expectation, channel characterization, network design, simple circuit implementation, and simulation results.

First, the channel characterization of the computer powerline structure is provided and discussed. The powerline structure in the computer was tested using five points on the powerline as points to be used for transceiver locations. From this channel characterization, the optimum frequency range for the sensor network is selected. Based on previous PLC literature and the channel characterization, a modulation scheme and demodulation scheme are then discussed, optimized and simulated. The modulator and demodulators are discussed individually, in terms of their subcomponents. Finally, the results of the simulation are presented and a simple circuit implementation for the sensor network is provided.

2 Background

In this chapter, a review of the related technology as well as some background information that aided in the network design and simulation choices are discussed. Topics included in this section are topology, noise characterizations, frequency selection and modulation selections used for the HomePlug standards and vehicular PLC. Differences and similarities will be discussed as they apply to the design of the low data rate sensor network for the desktop computer. Other topics beyond the physical layer and design of the sensor network, such as encoding techniques, data loss recovery techniques and software will not be reviewed as they go beyond the scope of this thesis.

2.1 HomePlug PLC

A notable challenge faced by PLC for HomePlug usage is that there is no standard topology for how devices are connected to the power network. Conductors are joined together almost at random and electrical appliances connected to the powerline can generate noise into the high frequency spectrum, with high frequencies being between 1 MHz to 30 MHz. A typical powerline channel may have average attenuation of 40 dB to greater than 60 dB [16]. Similar to the home power grid, the desktop computer will not have a predictable topology. For a desktop computer, the most common power supply unit is an Advanced Technology Extended (ATX) type power supply. The wiring topology for these units can vary by manufacturer and model number. It is also important to note that the powerline channel is time-varying for both home use

and within the PC. This means that if there is any sort of change in the topology of the powerline, such as devices being added, removed, turned on and off, the channel transfer function will change almost as abruptly as the change of the topology [17].

The behavior of the impulse noise generated versus the noise of the line itself is also important to note. Electrical appliances that turn on and off, an example of impulsive noise on an AC line, generate cyclic noise as a function of the AC line cycle [16]. While the line noise itself also tends to fluctuate with the line cycle, impulsive noise tends to be different in that it is synchronous, and has limited occurrences on the line cycle [18]. Since DC power is not cyclic, it should be expected that noise from various components on the power line network will be less predictable.

In addition to this impulsive noise, on home powerlines induced radio frequency (RF) signals can impair some frequency channels. In the case of vehicles and the desktop computers, the metal chassis can help deflect some of these interfering frequencies. In the United States, “FCC Part 15 rules using the frequency band between 1.8 MHz to 30 MHz, at a maximum power spectral density (PSD) of -50 dBm/Hz” [16]. For home PLC use, the IEEE P1901 standard restricts the transmission frequencies by all classes of PLC devices used for broadband in the first/last mile of service, including local area networks (LANs) for buildings, and other data distribution applications to frequencies below 100 MHz [17]. The HomePlug AV standard uses frequencies ranging from 2 to 28 MHz, which falls within these restrictions.

For the HomePlug AV standard, orthogonal frequency-division multiplexing (OFDM) modulation is advantageous over other modulation schemes because of its adaptability to severe channel conditions such as narrowband interference, impulsive noise, and frequency selective channel fading due to multipath [16]. By using OFDM, frequency separation allows for the use of passive filtering to isolate low-band signals from the PLC spectrum; high-pass filtering, however, "does not prevent in-band broad-spectrum noise, as generated by home appliances, or EMI/RFI" [18].

2.2 Vehicular DC powerline communication

As with the home power grid, there is no set standard for the powerline topology within a vehicle. Because there is no standard topology for vehicles or home power, as stated in [11], "a direct transposition of the work done for in-house applications to in-vehicle communication is not trivial, since the structure of the cable network is quite different in both cases." Since the there is no standard topology in the PC as well, it should also be expected that the work done for in-house applications will also be relevant to the PC application because of the similarity of qualities shared by the PC powerline and vehicular powerline. With the PC and vehicle having greater similarities in powerline characteristics than the PC and home power grid, it is expected that any work of importance for vehicular PLC will also be important for the PLC network in a PC.

Since there is no exact cable structure or path standard set by an organization or manufacturer, the complex channel transfer function measurements performed on a

vehicle are specific to that individual instance. In [11], the channel transfer function for each topology is deduced by measuring the S_{21} scattering parameter using a vector network analyzer (VNA). The longest and shortest powerline cable distance in which S_{21} is measured in [11] are 9 m, an indirect path to the power source, and 6 m, a direct source to the power source. It is mentioned that the minimum distance between any transmitter and receiver is 50 cm, so that the impedance seen at frequencies greater than 10 MHz does not appear as a short-circuit.

When considering noise characteristics of the vehicular powerline versus the home powerline, background noises in special frequency ranges, such as public broad castings, these noises were damped by 20 to 30 dB by the metal body of the car [9]. In [9], further discussion about the noise goes on to state that disturbances can be further classified into continuous, periodical, non-periodical, narrow band and broad band categories. Impulse noise, a non-periodic noise, on the DC line can include items such as engine ignitions or lights powering on or off in a car.

In [9], based on the measured disturbances and physical attributes of the powerlines used in most vehicles, the frequency selected for their communication channel is around 200 MHz. However, in [10, 11], based on bi-directional measurements of S_{21} over several paths, the deduced transfer function provides that the ideal communication frequency should be between 10 MHz and 30 MHz. Using this band, it was found in [11] that the transfer function reaches a maximum attenuation of 20 dB, and then decreases with frequency by approximately 0.5 dB/MHz. The result for the direct and indirect path are stated to be similar, with the notable difference being

that there is stronger attenuation on the longer indirect path. When comparing the correlation coefficient for several systems, it was found that the direct path remains nearly equal to 1, while the indirect path remains smaller than 0.7 [11].

In [9, 12, 13], the modulation scheme used based on the HomePlug standard, OFDM, with each subcarrier differential binary phase shift keying (DBPSK) or differential quadrature phase shift keying (DQPSK) modulated. DBPSK is also chosen for its very low fault liability in low signal-to-noise (SNR) conditions. In [12, 13], 84 carriers are used within the 4 MHz to 21 MHz bandwidth; spacing between two subcarriers is 195.531 kHz. In [10], initial benchmarking using frequency shift keying (FSK) with a center modulation frequency of 20 MHz, rates of 1 Mbps and 5 Mbps were achieved with 4-FSK and 2-FSK, respectively. A noncoherent demodulation technique is used in [9] because it saves the costs associated with needing additional carrier recovery circuits.

In [9], the digital part of the modulation scheme is implemented using field-programmable gate arrays (FPGAs), while the frequency shift part is implemented with an analog solution. At the receiver, [10] suggests using a series capacitor for coupling. This capacitor would block the DC power voltage and allow for high frequencies to pass. By coupling with a capacitor and a terminating resistor, a high-pass filter is achieved.

2.3 Communication Schemes

In [19], the process for selecting the optimum binary receiver is discussed. In this discussion, three carrier systems, ASK (amplitude-shift keying), FSK (frequency-shift keying), and PSK (phase-shift keying) are compared. Coherent (synchronously) and noncoherently (by envelope detection) detection methods for each of these three carrier systems are also compared and discussed. In the proceeding, a summary comparing these schemes and their advantages and disadvantages will be provided.

Bit error rate (BER) performance for threshold detection – detection in which "messages m = 0 and 1 are transmitted with equal probability using a positive and a negative pulse, respectively" – is calculated and compared for each of these carrier systems [19]. Summaries of coherent and noncoherent equations for comparison are provided in Table 2, as well as other equations deduced from this optimum binary receiver selection process. Table 1 provides a summary of notations used in Table 2.

Name	**Symbol**
BER	$P_b = Q(\rho)$
Noise power spectral density	N
RF pulse	$p(t)$
Signal amplitude	A_p
Pulse energy, signal energy per bit	E_p
Baseband pulse	$p(t)'$
Baseband energy, signal energy per bit	E_b
Noise power	σ_n^2

Table 1: Summary of symbols used in the equations throughout this thesis.

	Coherent BER	**Noncoherent BER**
PSK	$P_b = Q\left(\sqrt{\frac{2E_b}{N}}\right) \approx$ $\frac{1}{2\sqrt{\pi E_b / N}} e^{-E_b/N} \quad E_b/N >> 1$	Not applicable.
ASK	$P_b = Q\left(\sqrt{\frac{E_b}{N}}\right)$ $\cong \frac{1}{2\sqrt{\pi E_b / N}} e^{-E_b/N/2} \quad , E_b/N >> 1$	$P_b \cong \frac{1}{2}\left(1 + \frac{1}{\sqrt{2\pi E_b / N}}\right) e^{-\frac{1}{2}E_b/N}$ $\cong \frac{1}{2} e^{-\frac{1}{2}E_b/N} \quad E_b/N >> 1$
FSK	$P_b = Q\left(\sqrt{\frac{1.217E_b}{N}}\right)$	$P_b = \frac{1}{2} e^{-\frac{1}{2}E_b/N}$

Table 2: Summary of BER expressions for PSK, ASK, and FSK schemes in an additive white Gaussian noise (AWGN) channel.

In terms of error probability, the performance of these three modulation schemes is expected to perform similarly, given the same transmitted signal power – the error probability of the optimum detector depends only on the pulse energy, not the pulse shape. There is some difference, however, in the pulse energy needed to achieve the same bit error rate. From Table 2, in comparing the bit error rate equations for PSK and ASK, we can see that for the same BER, ASK requires twice the pulse energy than PSK. If phase information is available, PSK is preferred over ASK for this reason, however, if the phase information is not available, a noncoherent detection method will be preferred.

For noncoherent detection, when $E_b / N >> 1$, the performance of ASK detection and FSK detection are essentially similar. In [19], it is stated that for noncoherent

detection, FSK is to be preferred over ASK because FSK has a fixed optimum threshold, whereas the optimum threshold of ASK depends on E_b / N . Hence ASK tends to be more susceptible to signal fading.

3 Materials and Methods

3.1 Understanding the Channel

The desktop computer characterized in this thesis is a mini-ITX form factor desktop PC. This PC uses an Intel D201GLY2 motherboard and Morex 3677 case with power supply. This computer was chosen for its low cost and simple internal power structure. For the measurements performed in this section, five arbitrary nodes were chosen on the ATX powerline for to the purpose of determine a frequency to simulate for determining PLC feasibility in the PC. Even though only five nodes were selected in this scenario, it can straightforwardly be extended to include more nodes. The power structure of this desktop PC is depicted in Figure 1. In this figure, the five measurement points are depicted with respect to their location within the computer on the ATX powerline.

The power flows through the network depicted in Figure 2. Lengths of the wire between the connections depicted in Figure 2 are provided in Table 3. The longest connection between nodes measured on the network analyzer is that between nodes 1 and 5, an indirect path; the shortest connection measured is that between nodes 4 and 5, a direct path.

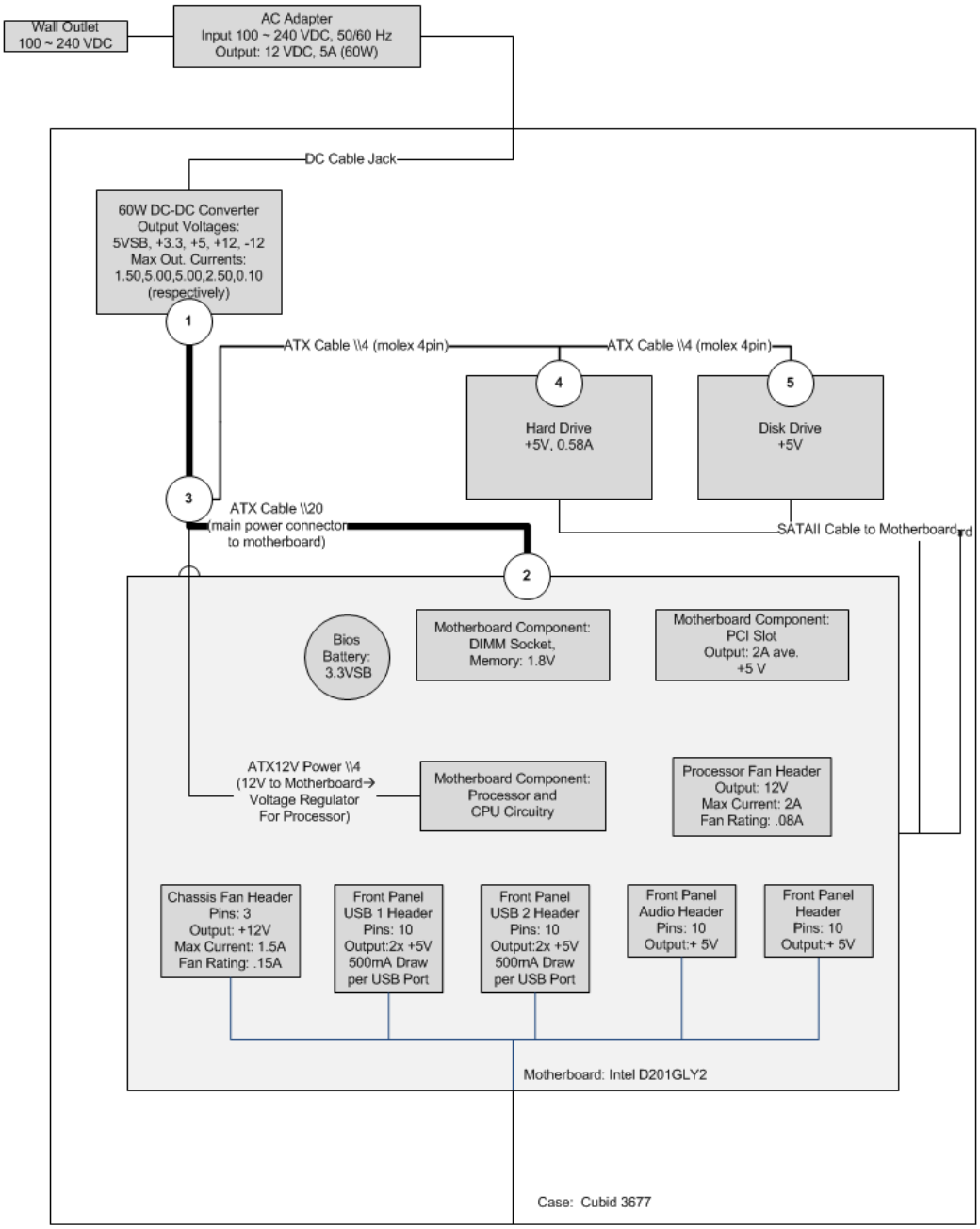

Figure 1. DC power distribution structure.

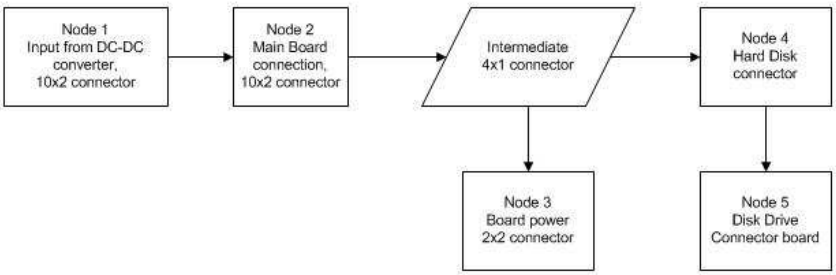

Figure 2. Power flow.

Channel Segment	**Length**
Node 1 to Node 2	~32cm
Node 2 to Node 3	~31cm
Node 3 to Node 4	~15cm
Node 4 to Node 5	~15cm

Table 3: Channel segment lengths.

As discussed in [11], measuring the S_{21} parameter can give a better perspective of what frequency is best suited for communication on the powerline. For the data provided here, the Hewlett Packard 8720ES S-Parameter Network Analyzer was used to measure channel attenuation by measuring the forward voltage, the S_{21} parameter. This model of network analyzer is capable of measuring the forward voltage by doing a sweep of the frequencies. The available frequency range for this device is between

50 MHz and 20 GHz, thus eliminating the ability to measure the range of frequencies used in the HomePlug standard.

When first powered on, the manufacturer suggests letting the device warm up for half an hour. After this warm up period, the device is then calibrated using a kit from the manufacturer. To calibrate the device, first the start and stop frequencies that will be swept are entered. For the initial set of measurements, a start frequency of 50 MHz is used and a stop frequency of 20 GHz is used to visualize the full spectrum available by the network analyzer. After entering these frequencies, the CAL button is pressed. Then, a set of options appear on the screen and the soft key next to the calibration menu option is pressed. From the next set of options on the screen, Full 2 port is selected and a calibration for each of the following: reflection, transmission and isolation is performed respectively. Two HP calibration cables are then connected to the network analyzer; one connected to each port on the analyzer. Note that the calibration cables remain connected to the network analyzer during the whole calibration process. Only the pieces at the end of the cables change. A simple calibration setup diagram is provided in Figure 3.

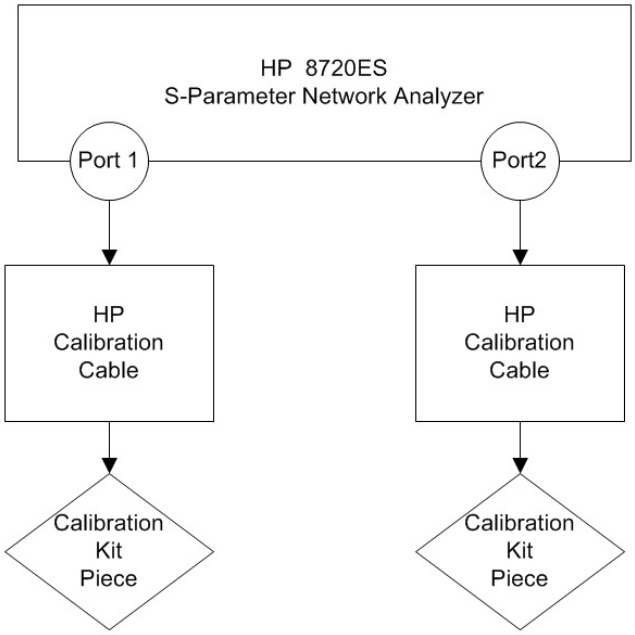

Figure 3. Calibration Setup.

First, the reflection calibration is performed. For the reflection calibration, a forward and reverse calibration is performed for the each of the following calibration pieces in the kit: open, short, and broadband. For the open calibration, there are two pieces in the kit; one piece is attached at the end of each calibration cable for each of the two ports. The calibration soft key is then pressed for both forward and reverse calibration of the open pieces and the same is then performed for the short pieces and broadband pieces. After these three calibrations are performed, a soft key is pressed to confirm the standards are done.

Next, the transmission setting is calibrated. This is done by connecting port 1 and 2 together via barrel connector. The calibration cables remain connected at each port,

with a barrel connector used for the calibration piece. The soft key for the option ‘do both’ is then pressed. Once the analyzer has beeped, the transmission setting has been calibrated.

For the isolation calibration parameter, the option of ‘omit isolation’ is selected. The option for ‘done 2 port cal’ is then pressed completing the device calibration and the measurement key is then pressed to begin measurement. The measurement performed is a frequency sweep between the start and stop points entered during calibration.

The calibration cables are then removed from both ports and a simple probing device is then connected to each port. This simple device is composed of two pieces of solid copper core wire approximately 12 cm in length each, a small gauge coaxial cable approximately 5 cm in length, and SubMinature version A (SMA) connectors were constructed to form a probing device and used to aid in taking measurements on nodes 1 through 4. At Node 5, two pieces of coaxial cable were soldered to the compact disc (CD) drive power connection board – one connected to the 12 volt power input and ground; one connected to the 5 volt power input and ground. At the end of these two connections, a SMA connector was soldered on to connect to the VNA. Figure 4 provides a simple diagram depicting how the connections of the probe components are made with respect to the network analyzer. Measurements taken of the setup in Figure 4 without connecting the ATX power cable will be referred to as ‘open circuit’ measurements in the proceeding text. This provides a comparison

baseline of the noise due to the measurement probes as well as the environmental noise surrounding the powerline in the measurement tool area.

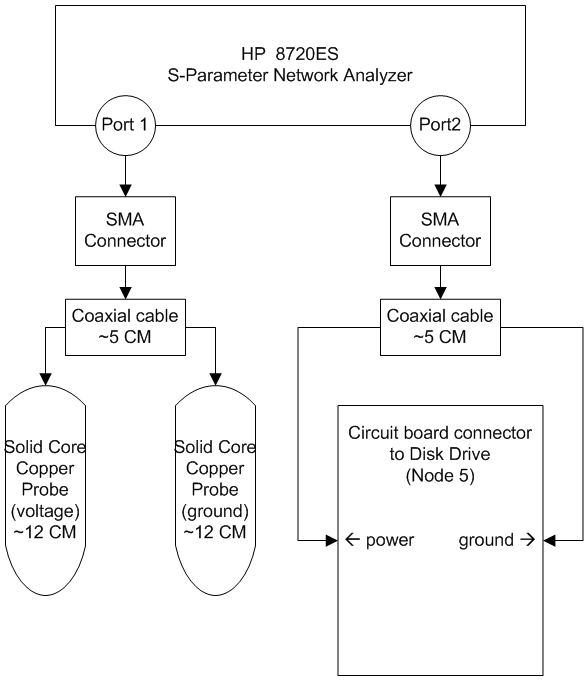

Figure 4. Measurement Probes.

From the data sheet for the network analyzer [20], the maximum input for the ports is listed as 10 dBm. With the computer powered on, an input of 5 V or 12 V to the network analyzer would damage the network analyzer, thus the measurements are performed with the computer powered off. When the computer is powered on, it is expected that the attenuation of the DC power lines at certain frequencies will not change significantly. Measurements were taken from five points on the motherboard

utilizing the simple probe devices described earlier. Measurements are performed at the connection for main power to board components, at the connector to power for the board, at the connector to the hard disk power, and at the connector to the CD drive power. These nodes were chosen because they would be the easiest locations to gain access to a communication channel on the power supply cabling, and would be the optimum locations to connect simple communication circuitry to. These are denoted as nodes 1 through 5, respectively and are depicted in Figure 1 as circles containing only a single numerical value.

Two sets of measurements were taken at each set of nodes: one set of measurements for the 5 volt line and one set of measurements for the 12 volt line. Four initial measurements were taken spanning the entire available frequency range on the network analyzer – 50MHz to 20GHz; one measurement for each node, 1 through 4, and their path to node 5. The 50MHz to 5GHz segment of these initial measurements is depicted in Figure 5a and Figure 5b, show that the range with the least attenuation for both the 5 volt line and 12 volt line is between 50MHz and 2GHz; the ideal frequency range for the communication range will be within this frequency band. Figure 5a represents the four measurements taken of the 12 volt line; Figure 5b represents the four measurements taken of the 5 volt line. From these initial measurements it is apparent that the range with the least attenuation for both voltage lines is within the 50MHz to 2GHz range.

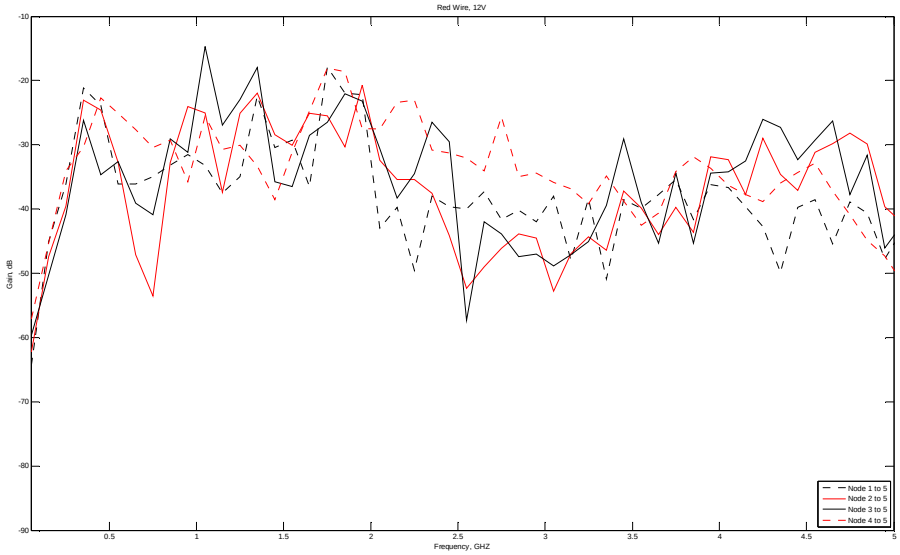

Figure 5a. Gain for 50 MHz to 5 GHz, 12 V line.

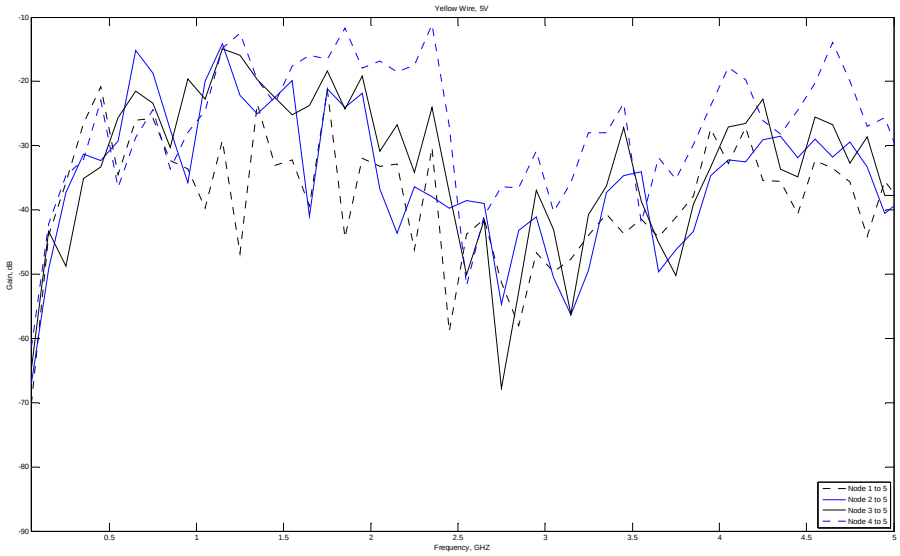

Figure 5b. Gain for 50 MHz to 5 GHz, 5 V line.

Figure 6b through Figure 6e provide individual measurements of the channel attenuation between the five nodes on the 5 V line for the optimum range depicted in Figure 5b, 50MHz to 2.0GHz, as well as an open circuit measurement for baseline comparison in Figure 6a. For Figure 6b through Figure 6e, the measurement is performed by placing the port 1 probe on node 1, 2, 3, and 4, respectively, and leaving the ATX power cable connected to node 5.

When comparing Figure 6b through Figure 6e, it is interesting to note that as the distance between the nodes decreases, the attenuation in the channel also decreases. With the shortest distance between nodes being that between nodes 4 and 5, the channel attenuation is approximately 20 dB for the prime frequency range, 50MHz and 2.0GHz. Visually inspecting the longest distance, the distance between nodes 1 and 5 depicted in Figure 6b, the average attenuation is approximately 40dB. These values are very close to those measured on the vehicular powerline in [9]. Table 4 summarizes the lengths between nodes based on the channel segments in Table 3.

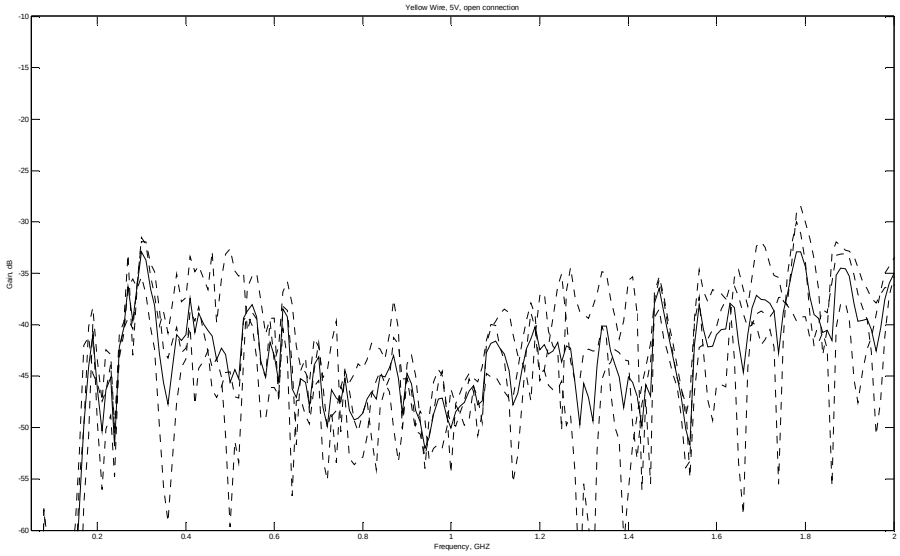

Figure 6a. 5 Volt line Gain, 50MHz to 2GHz, Open Circuit.

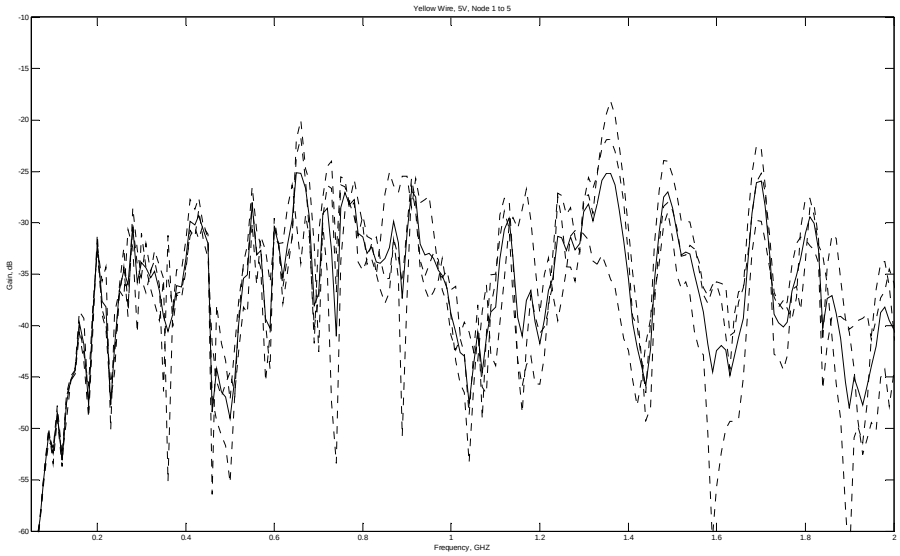

Figure 6b. 5 Volt line Gain, 50MHz to 2GHz, Node 1 to Node 5.

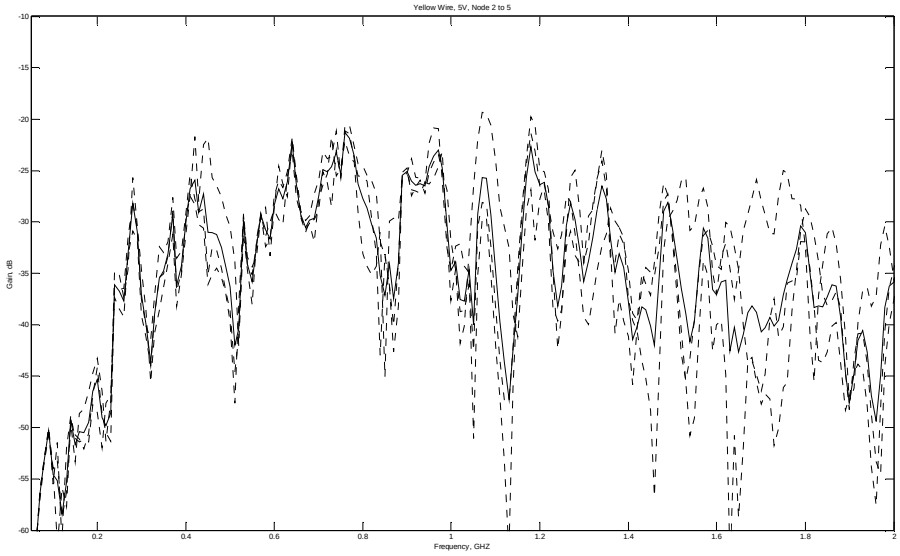

Figure 6c. 5 Volt line Gain, 50MHz to 2GHz, Node 2 to Node 5.

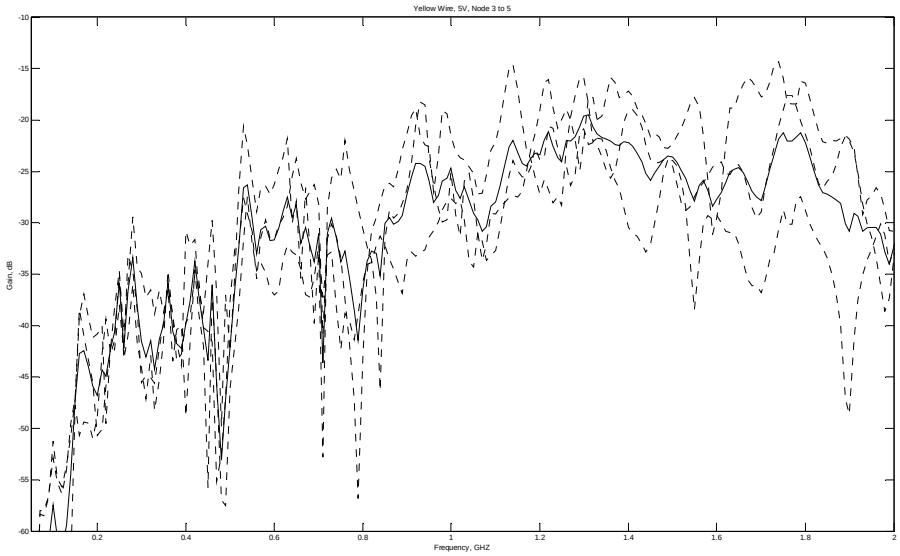

Figure 6d. 5 Volt line Gain, 50MHz to 2GHz, Node 3 to Node 5.

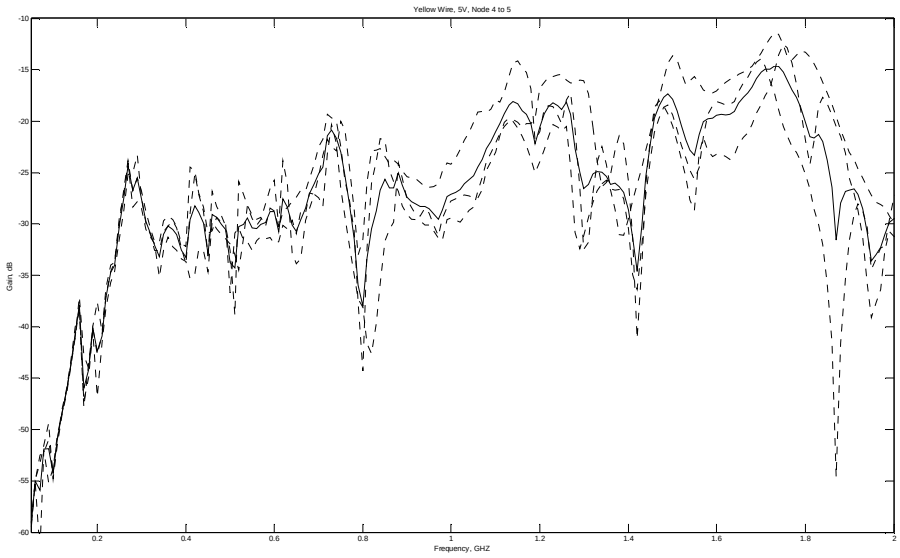

Figure 6e. 5 Volt line Gain, 50MHz to 2GHz, Node 4 to Node 5.

Channel Segment	**Length**
Node 1 to Node 5	~93cm
Node 2 to Node 5	~61cm
Node 3 to Node 5	~30cm
Node 4 to Node 5	~15cm

Table 4: Length between nodes.

Figure 7b thru Figure 7e provide individual measurements of the channel attenuation between the five nodes on the 12 V line for the optimum range depicted in Figure 5a, 50MHz to 2.0GHz, as well as an open circuit measurement for baseline comparison in Figure 7a. From visual inspection of Figure 7e and Figure 7b, the average channel attenuation on the 12 V line is between 25 dB and 35 dB, respectively. This is also very similar to the attenuation measured in [9]; both the vehicular powerline and the ATX powerline depicted in Figure 7b thru Figure 7e are approximately 12 V DC lines; thus this similarity in channel attenuation seems reasonable.

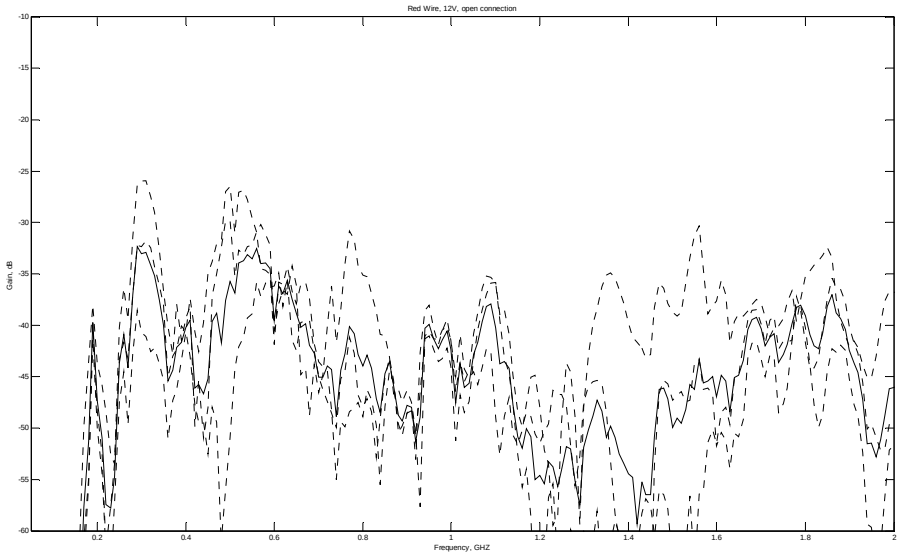

Figure 7a. 12 Volt line Gain, 50MHz to 2GHz, Open Circuit.

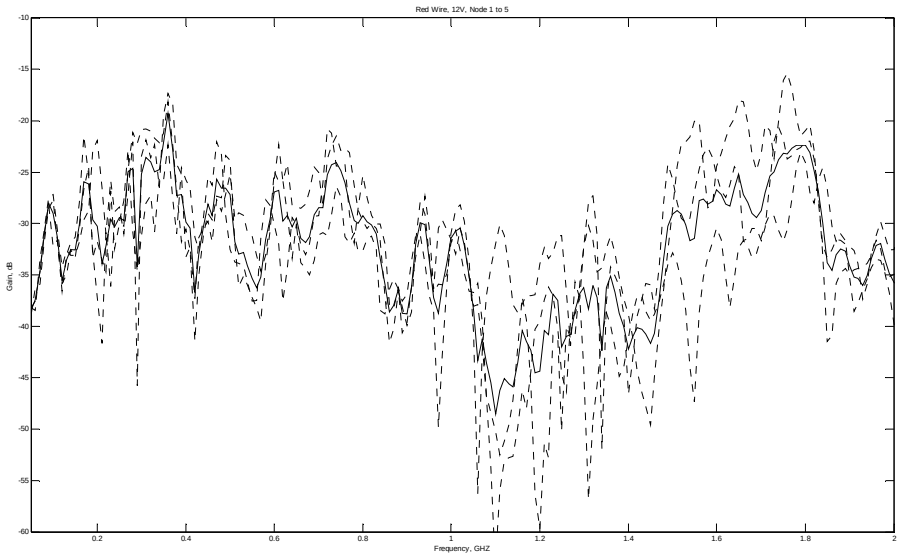

Figure 7b. 12 Volt line Gain, 50MHz to 2GHz, Node 1 to Node 5.

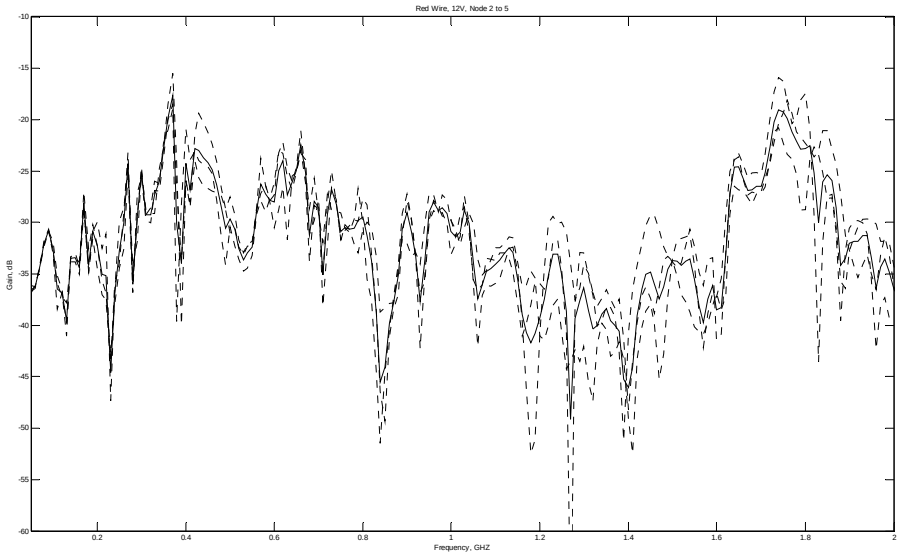

Figure 7c. 12 Volt line Gain, 50MHz to 2GHz, Node 2 to Node 5.

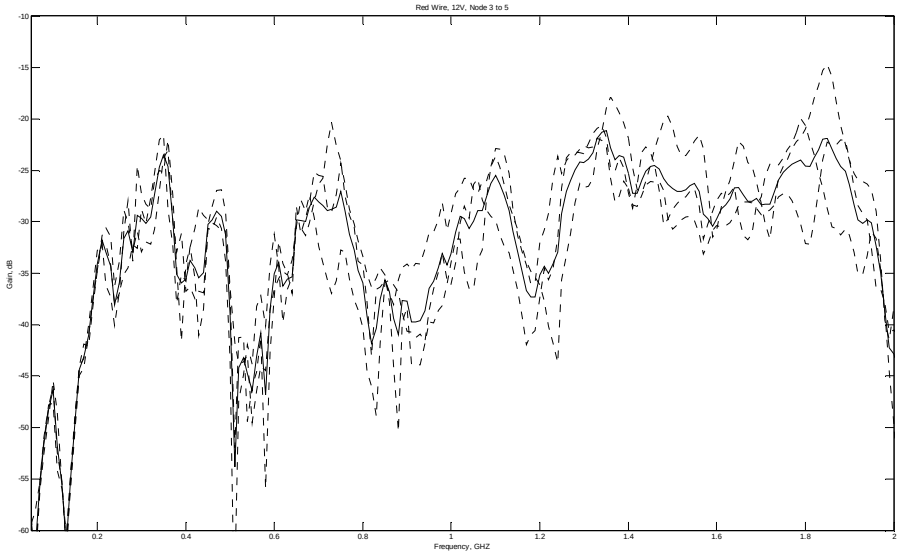

Figure 7d. 12 Volt line Gain, 50MHz to 2GHz, Node 3 to Node 5.

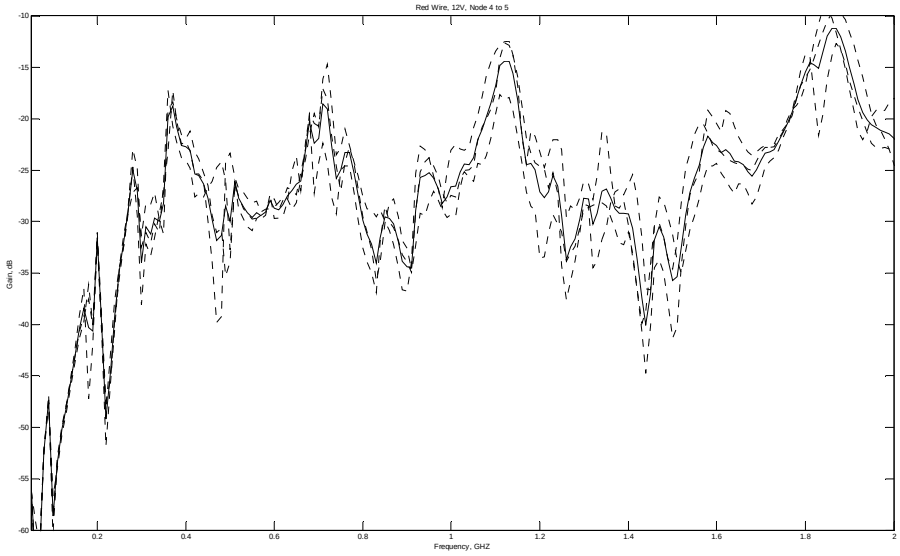

Figure 7e. 12 Volt line Gain, 50MHz to 2GHz, Node 4 to Node 5.

Table 5 provides a summary of the average attenuation values measured and plotted in Figure 6 a through e and Figure 7 a through e. From this table, it can be seen that the difference from the open circuit measurement and the average of all non-open circuit segments is approximately 11.8 dB, with the difference in attenuation from the longest length of wire to the shortest length of wire being approximately 1.1 dB. Comparing Table 4 with Table 5, there seems to be a direct relation between channel attenuation and length.

	Red Line, 12 V	**Yellow Line, 5 V**	**Average of 5V & 12V**
Open Circuit	46.4dB	44.4dB	45.4dB
Node 1 to Node 5	32.5dB	37.0dB	34.7dB
Node 2 to Node 5	32.1dB	35.0dB	33.7dB
Node 3 to Node 5	32.5dB	31.6dB	32.1dB
Node 4 to Node 5	27.5dB	27.36dB	27.4dB
Average, non-OC	31.2dB	32.8dB	33.6dB

Table 5: Average attenuation measurements.

Figure 8a compares the average channel attenuation for both the 5 V line and 12 V line. The attenuation for each segment on the 5 V line is averaged together and is depicted with a black dashed line. The average of the attenuation for the segments on the 12 V line is depicted with a red dashed line. The open circuit attenuation is depicted with a solid black line and solid red line for the 5 V and 12 V lines, respectively. It is clear that there is a difference between the open circuit measurement

and the closed circuit measurement of the channel— the difference between the two from visual inspection is approximately 15 dB. Figure 8b further illustrates that there is a difference between the communication channel attenuation and the attenuation of the open circuit measurement. The black dotted line represents the average of all the segment attenuation measured for both the 5 V line and the 12 V line; the solid black line represents the open circuit measurement; the dashed line represents the average of the channel attenuation with the open circuit measurement. This measurement establishes that if there is a break in the communication channel, the signal will attenuate in a noticeable amount.

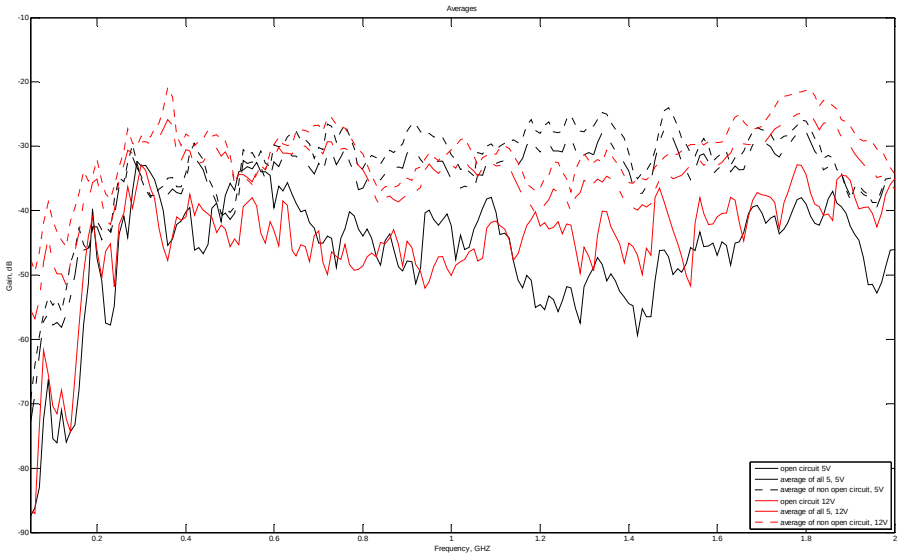

Figure 8a. Averages at 50MHz to 2GHz, comparison to open circuit measurement.

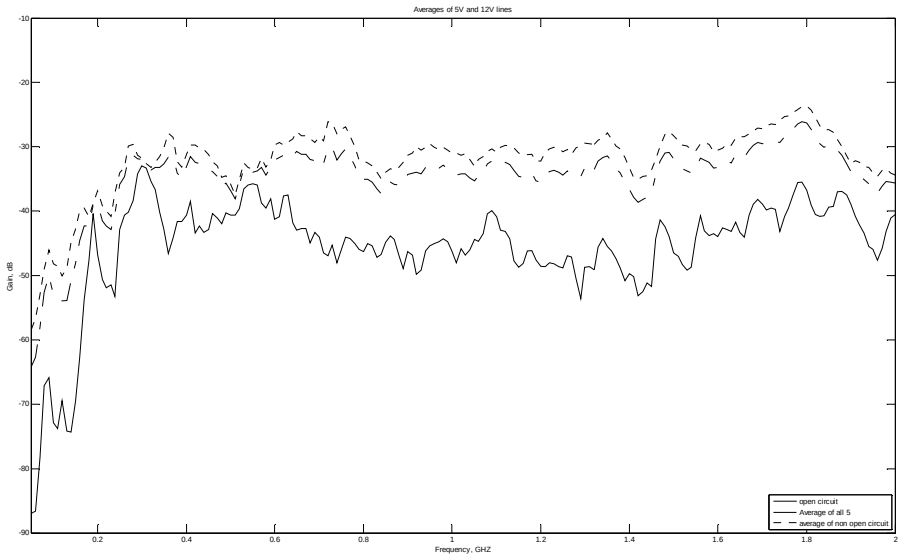

Figure 8b. Averages at 50MHz to 2GHz, 5V and 12V lines averaged together

Further inspecting Figure 8a for the ideal communication frequency band to be used, there are two ranges that look promising: 0.2GHz to 0.4GHz and 1.7GHz to 1.9GHz. Looking closely at the 0.2GHz to 0.4GHz range, it is evident that this range appears to be better for the 12 V line, but does not perform significantly better than the open circuit measurement for the 5 V line, and even attenuates more than the open circuit measurement for a few points. This eliminates the 0.2GHz to 0.4GHz range from the communication channel options and leaves the frequency range of 1.7GHz to 1.9GHz range as the preferred communication band.

The average attenuation and standard deviation over the full frequency range (50MHz to 20GHz), the sampled frequency range (50MHz to 2GHz), and the ideal frequency range (1.75GHz to 1.80GHz) were calculated for several measurements and

are provided in Table 6. Specific values for measurements between nodes 1 and 5, 2 and 5, 3 and 5 and 4 and 5 for the sample range and ideal range are provided in Table 7 and Table 8, respectively. In comparing Table 7 to Table 8, the ideal selected frequency range has the least amount of deviation from the mean. The average attenuation in the 1.75GHz to 1.80GHz range is nearly 10 dB higher than the 50MHz to 2GHz range and approximately 24 dB higher than that of the 50MHz to 20GHz range.

	Average Gain (dB)	**Standard Deviation**
50MHz to 20GHz	-46.389	11.04576
50MHz to 2GHz	-31.205	8.311214
1.75GHz to 1.80GHz	-22.692	4.341325

Table 6: Channel statistics.

	Average Gain (dB)	**Standard Deviation**
Node 1 to 5	-32.5916	7.465702
Node 2 to 5	-32.1119	6.567719
Node 3 to 5	-32.5963	8.705579
Node 4 to 5	-27.5202	9.131665

Table 7: Node specific statistics for 50MHz to 2GHz.

	Average Gain (dB)	Standard Deviation
Node 1 to 5	-22.6922	4.341325
Node 2 to 5	-21.3696	3.606259
Node 3 to 5	-24.5189	3.594969
Node 4 to 5	-18.5795	2.250324

Table 8: Node specific statistics for 1.75GHz to 1.80GHz.

Figure 9a highlights the 1.75GHz to 1.80GHz range within the 50MHz to 2GHz frequency sweep measurement. A zoomed-in view of the windowed area in Figure 9a is provided in Figure 9b. From Figure 6 b through e, Figure 7 b through e, and Figure 9b, an ideal center frequency for each node is selected. Table 9 provides a summary of the center frequencies selected for each node. These frequencies were chosen based on their standard deviation from the mean for the 1.75GHz to 1.80GHz range. The frequency with the least deviation for all the nodes was first selected; the next greatest standard deviation for the remaining frequencies and nodes was used to select the next node-frequency pair, until each node is paired with a unique center frequency.

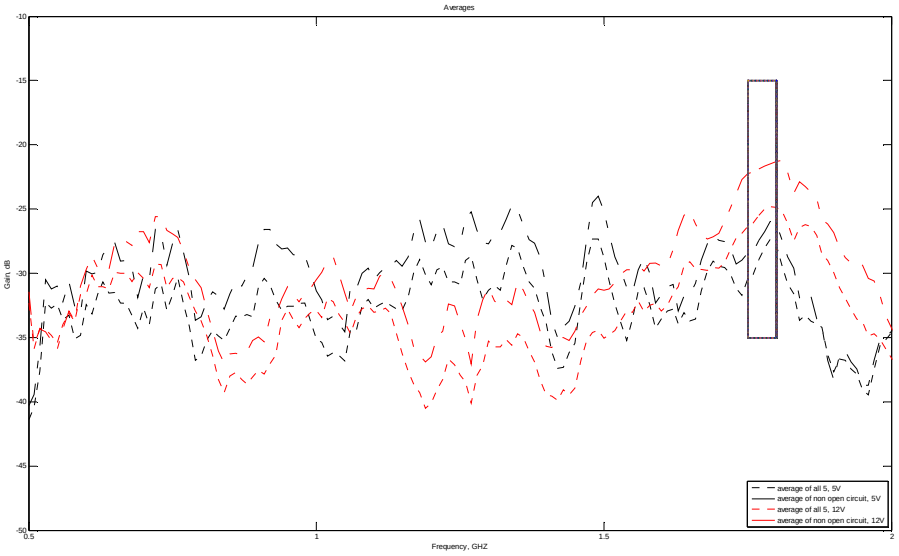

Figure 9a. Channel frequency selection for network, 50MHz to 2GHz.

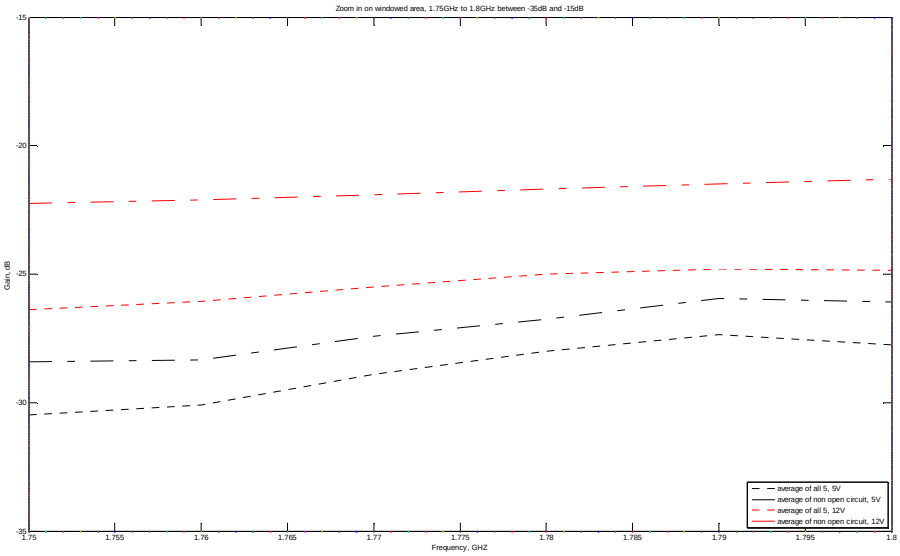

Figure 9b. Channel frequency selection for network, 1.75GHz to 1.80GHz.

Channel Segment	**Center Frequency**	**Standard Deviation**
Node 1	1.79GHz	0.814528
Node 2	1.78GHz	2.845652
Node 3	1.75GHz	1.821924
Node 4	1.77GHz	0.306857

Table 9: Center Frequencies for each Node, 1 thru 5.

In the next section, these center frequencies listed in Table 9 will be used as a base for designing the communication network architecture. These frequencies result in the smallest channel attenuation for both the 5 V and 12 V lines at the given nodes, thus the signal power needed for transmission will be the lowest possible of all the frequencies measured.

3.2 Communication Network Architecture

The sensor network is comprised of five transceiver devices; one at each of the main nodes used to collect sensor data, temperature, for example, through the powerline channel. Although only five nodes are chosen for the analysis and design in this thesis, the network architecture could be easily extended in a straightforward manner to a similar network with virtually any number of nodes. Since the goal is to have one node be able to access sensor data at all other nodes, this node will be designated as the primary node and all other nodes will be referred to as secondary nodes for simplicity. The primary node needs to be able to transmit information, for example, command to pull sensor data, to and receive the sensor data from all other nodes. It is possible that addressing all nodes is simultaneous, that is, the primary node needs to send information to each of other nodes at the same time. On the other hand, the secondary nodes only need to be able to communicate only with the primary node, but not their peers. Additionally, the network does not need to work at a full duplex mode; the secondary nodes will transmit information only when commanded by the main node, but the secondary nodes must be "listening" at all times for potential instructions from the primary node.

Based on the channel characterization results provided in section 3.1, it is found that for low-data-rate sensor networking, the bandwidth provided by the DC powerline channel is more than adequate, and leaves ample room for additional future channels. For the simplicity of implementing the network to determine feasibility, a frequency-division multiple-access scheme (FDMA) will be adopted. In this scheme, each

primary node-secondary node pair uses a different frequency band. For each pair of nodes, binary FSK will be adopted.

To implement the binary FSK demodulation at each of the secondary nodes, there will be a bandpass filter operating with its desired frequency band of choice. Within the transceiver of the primary node, there will be a bank of bandpass filters, each matching the frequency band of choice for each specific secondary node. There will be two different frequencies for each node pair – one to represent a bit '0' and one to represent a bit '1'; provided the ample bandwidth available for this communication channel, the frequencies used for these are able to be far apart, thus further reducing the chances for bit error.

Node 5, the connection furthest from the main power source, will serve as the primary node; it will be able to transmit and receive all frequencies within the designated range: 1.75GHz to 1.80GHz depicted in Figure 9b. The secondary nodes are nodes 1 thru 4. These nodes will only be able to receive the designated frequencies listed in Table 9. The top level schematic of the system for transmitting from node 5 is depicted in Figure 10; receiving at node 5 is depicted in Figure 11.

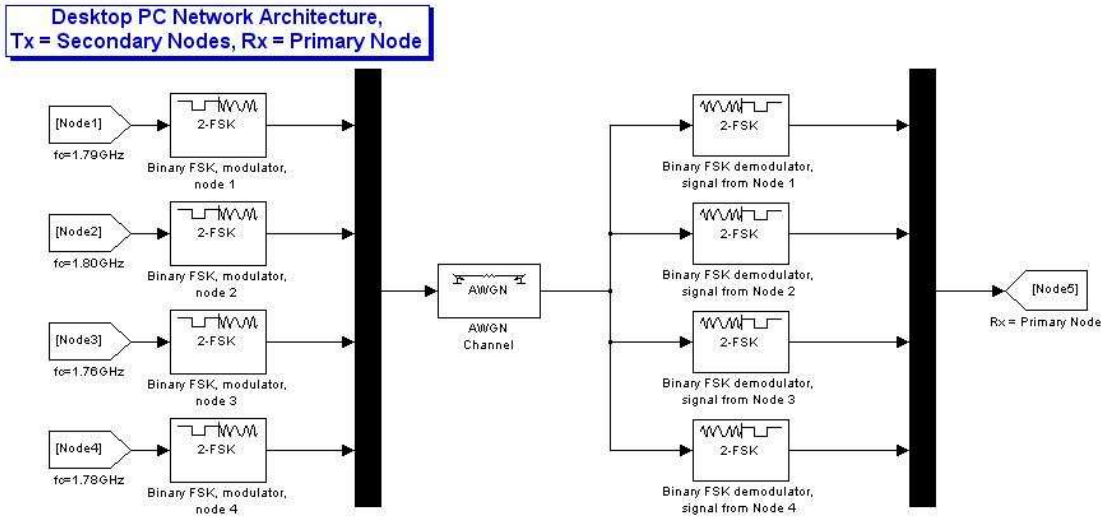

Figure 10. Receiver-transmitter architecture.

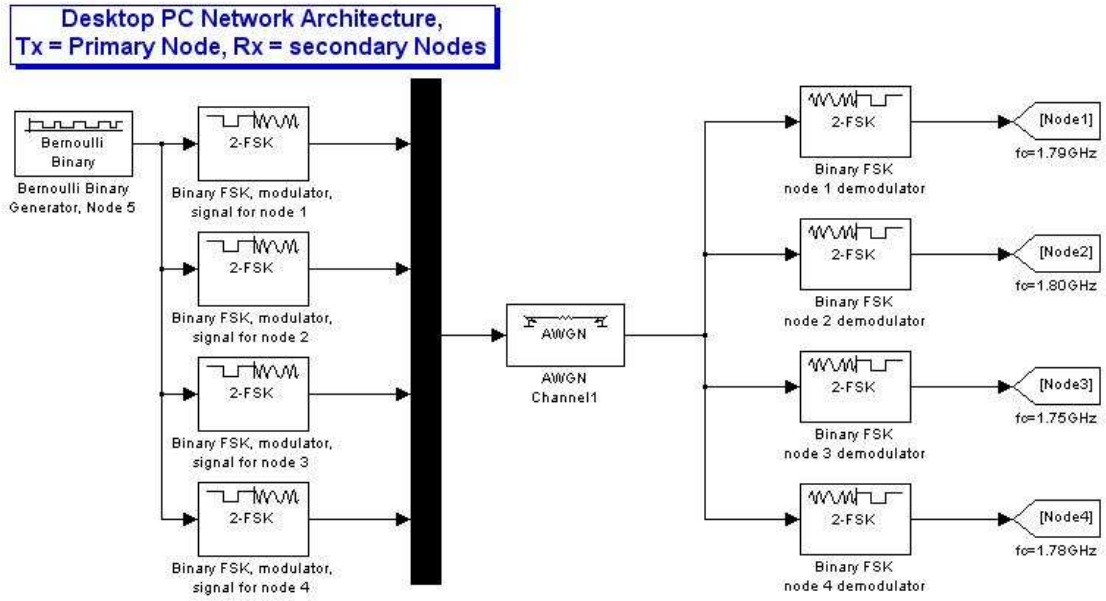

Figure 11. Transmitter-receiver architecture.

It is important to note that Figure 10 and Figure 11 are merely conceptual schematics to illustrate how the simulation will be modeled. These cannot actually be implemented and simulated nor do they exemplify the physical behavior of a network. Details regarding the actual simulation will be discussed in section 3.4.2.

3.2.1 FM Modulation

From [21], it is proved that an FM modulator is the equivalent of an integrator in series with a PM Modulator. In, [21], it continues in stating that, an angle-modulated signal, such as an FM signal, can be written in general as (1).

$$u(t) = A_c \cos\left(2\pi f_c t + \phi(t)\right) \tag{1}$$

By replacing A_c, the carrier amplitude, with (2), an expression containing bit interval duration, T_b, the equation for a frequency modulated signal of a specific bit is achieved.

$$A_c = \sqrt{\frac{2E_b}{T_b}} \tag{2}$$

In the most simple form of FSK, binary FSK, the modulated signal expression is for bit ‘0’ and bit ‘1’ representations are provided in (3), and (4), respectively.

$$u_0(t) = \sqrt{\frac{2E_b}{T_b}} \cos 2\pi f_0 t, \quad 0 \le t \le T_b \tag{3}$$

$$u_1(t) = \sqrt{\frac{2E_b}{T_b}} \cos 2\pi f_1 t, \quad 0 \le t \le T_b \tag{4}$$

The general expression for an *M*-ary FSK signal is provided in (5), where Δf represents the separation between frequencies, with f_c representing the center frequency and *m* representing the bit.

$$u_m(t) = \sqrt{\frac{2E_s}{T}} \cos(2\pi f_c t + 2\pi m \Delta f t), \quad m = 0,1,...,M-1, \quad 0 \le t \le T \tag{5}$$

In (5), it is apparent that the center frequency, f_c, remains constant, while the successive symbols vary in frequency from the initial symbol by $m\Delta f$. Note that for orthogonality in a binary FSK system, the ideal minimum separation between symbols is $1/2T$. For other systems with limited bandwidth, it is ideal maintain orthogonality to improve upon the bit error rate, however with the ample bandwidth available for this design, the minimum separation to maintain orthogonality will not be applied here.

3.2.2 Noncoherent FSK Demodulation

According to [19], coherent demodulation "has a superior performance in comparison to the latter method [noncoherent]," for this particular network, the ideal

choice is to use a noncoherent binary FSK modulation and demodulation scheme. This is the optimal choice for this sensor network since the phase as well as the amplitude of the received signal may not be known and it will not require as sophisticated of equipment to be able to achieve [19].

For the demodulator, the equation for the received signal at the input is provided by (6) [22].

$$r(t) = \sqrt{\frac{2E_s}{T}} \cos(2\pi f_c t + 2\pi m \Delta f t + \phi_m) + n(t) \tag{6}$$

This equation varies from (5), in that, ϕ_m represents the phase-shift of the *m*-th signal and $n(t)$ represents the additive bandpass noise, provided in (7).

$$n(t) = n_c \cos 2\pi f_c t - n_s(t) \sin 2\pi f_c t \tag{7}$$

It is implied that a noncoherent binary FSK detection device can be comprised of a pair of matched filters, followed by an envelope detector and decision device [19]. This is essentially a frequency discriminator, with the addition of a time based sampling device and the replacement of the summation with a comparator. Conceptual diagrams of a frequency discriminating demodulator and a noncoherent FSK demodulator are provided in Figure 12 and Figure 13 respectively.

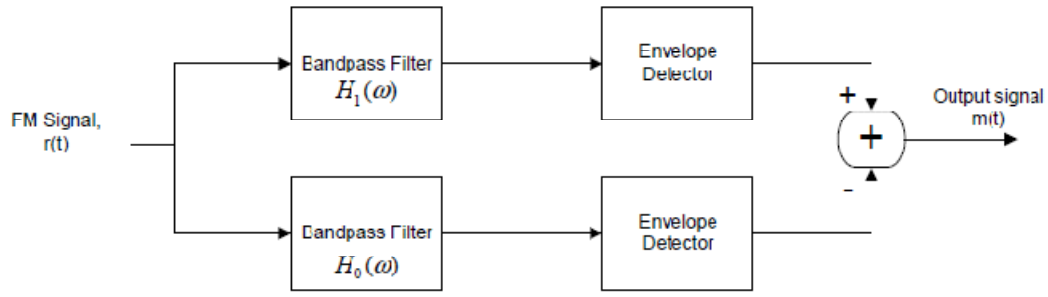

Figure 12. Demodulator: Frequency Discriminator.

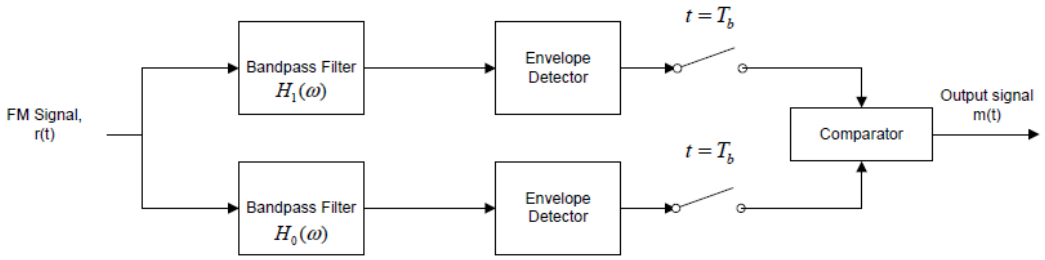

Figure 13. Demodulator: Noncoherent Binary FSK.

In both Figure 12 and Figure 13, the bandpass filter pair can be designed to create a slope circuit. Essentially, a slope circuit is comprised of two bandpass filters, offset in equal amounts of frequency from each other. By adding two offset bandpass filters, the additional tones created when modulating the signal can be cancelled out and adding the overlap of the two filters amplifies the signal. The offset filter response and addition is depicted in Figure 14.

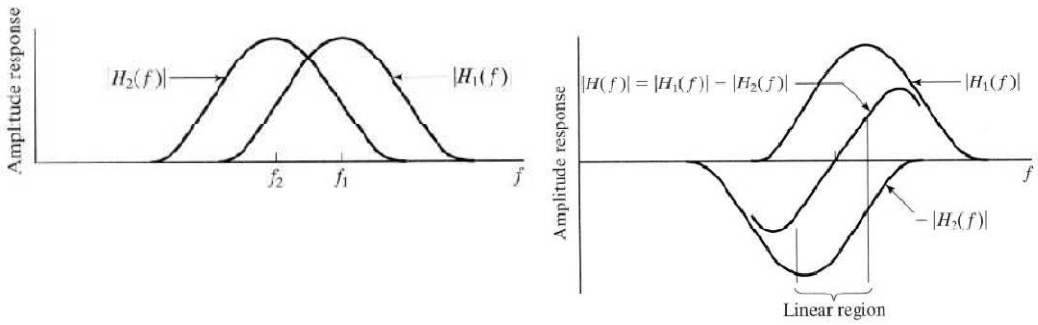

Figure 14: Slope Circuit [21].

Edge frequencies of these bandpass filters are calculated using Carson's rule (8), where B_c represents the effective bandwidth of the modulated signal, β represents the modulation index, further detailed in (9), and W represents the bandwidth of the message signal, $m(t)$. In (9), k_f represents the frequency deviation constant, and $\max[m(t)]$ represents the maximum amplitude of the message signal [21].

$$B_c = 2(\beta + 1)W \tag{8}$$

$$\beta = \frac{k_f \max[m(t)]}{W} \tag{9}$$

The envelope detector blocks can be created using a rectifier followed by a lowpass filter, depicted in Figure 15. Finding the upper saturation limit for the rectifier block in Simulink can be done by putting the signal into saturation and using a differential block after the modulated signal; the signal emitted from the differentiation block can be visually inspected using a scope block and the maximum

value, the value to be used for the upper saturation limit in the rectifier can be determined. For the lowpass filter block, the cut-off frequency should be set so that the maximum frequency that will be used, 1.8 GHz will be able to pass through.

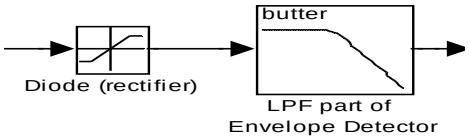

Figure 15. Envelope Detector

A guideline to the physical circuit components and process for circuit design of this noncoherent FSK demodulation scheme are further detailed in section 3.3.3. The following section will provide details regarding the circuitry design for the components discussed in this chapter.

3.3 Simple Circuit Architecture to Implement the Network

3.3.1 FM Modulator Circuitry

In [23], a very simple binary FSK modulator can be created by passing two signals through a pair of mixers then adding them together. The signal representing '0', (3) is created by mixing (2) and (10) through the first mixer; the signal representing '1', (4), is created by mixing (2) and (11) through the second mixer. This is depicted in Figure 16. These two signals, (3) representing a '0' bit, and (4) representing a '1' bit, respectively are then added together, resulting in $p(t)$, (6) without the additive bandpass noise, $n(t)$.

$$\cos(2\pi f_0 t) \tag{10}$$

$$\cos(2\pi f_1 t) \tag{11}$$

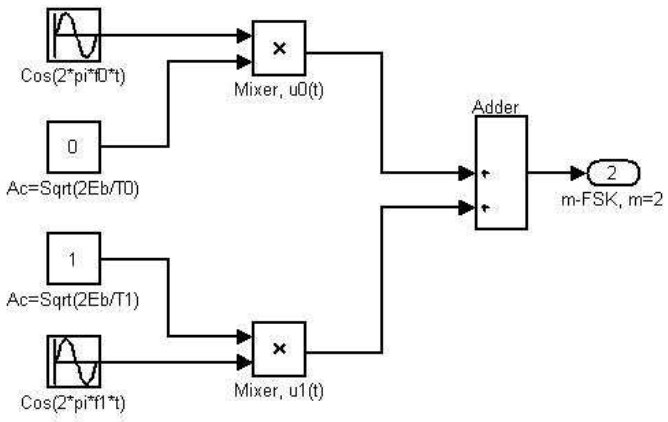

Figure 16. Simple conceptual model of an FSK modulator.

After passing $p(t)$ through the channel, the received signal at the demodulator, (6) can also be created with simple passive circuitry components. Further details on how the simple circuit for a noncoherent FSK demodulator can be created are detailed in the next section, 3.3.2.

3.3.2 Noncoherent FSK Demodulator Circuitry

From Figure 13, there are two main conceptual pieces to explain the simple circuitry for: the slope circuit and the envelope detector. The slope circuit is comprised of the two bandpass filters as depicted in the left portion of Figure 13; the envelop detector is comprised of a rectifier and a lowpass filter, as depicted in Figure 15. An explanation of the slope circuit composition will be provided first, with the envelope detector following the slope circuit explanation.

For the slope circuit, the two offset bandpass filters can be constructed using RC bandpass filters. An RC bandpass filter can be constructed by using a highpass filter followed by a lowpass filter, as depicted in Figure 17, where C1 and R1 comprise the highpass filter; R2 and C2 comprise the lowpass filter.

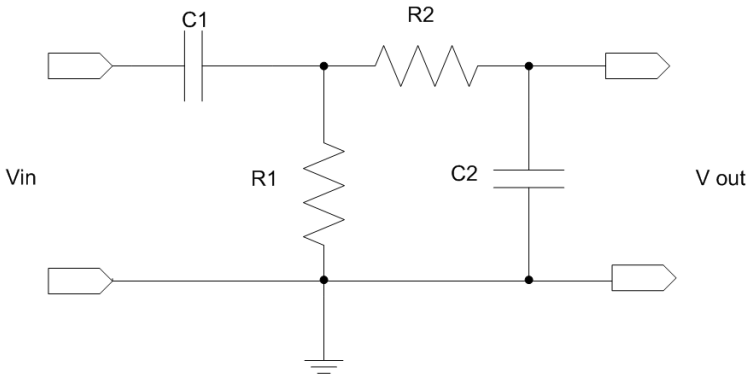

Figure 17. RC Bandpass Filter.

Transfer function equations for the highpass, lowpass and bandpass filters are provided in (12), (13), and (14) respectively.

$$H_{HP}(\omega) = \frac{R}{R + 1/j\omega C} \tag{12}$$

$$H_{LP}(\omega) = \frac{1/j\omega C}{R + 1/j\omega C} \tag{13}$$

$$H_{BP}(\omega) = \frac{j\omega_{HP} R_1 C_1}{(1 + j\omega_{HP} R_1 C_1)(1 + j\omega_{LP} R_2 C_2)} \tag{14}$$

Equation (14) can be derived by first multiplying (12) by the input voltage; this gives the lowpass filter input voltage. By multiplying (13) by this value and dividing by the input voltage to the highpass filter, (14), the equation for a RC bandpass filter can be achieved.

From (14), the transfer function for a bandpass filter, some specific numerical examples of potential resistance and capacitance values that could be used to implement the simple RC bandpass filter are provided in Table 10 and Table 11. Using (12) some example values for creating the highpass filter segment in Figure 17 are provided in Table 10; using (13), some example values for creating the lowpass segment are provided in Table 11.

Center	**Cut-off**	**Capacitance (fF)**	**Resistance (Ω)**
1.80GHz	1.79GHz	32.93088	0.27
1.79GHz	1.78GHz	33.11588	0.27
1.78GHz	1.77GHz	33.30298	0.27
1.76GHz	1.75GHz	33.68358	0.27

Table 10: Resistance and Capacitance example values for highpass filter.

Center	**Cut-off**	**Capacitance (fF)**	**Resistance (Ω)**
1.80GHz	1.81GHz	32.56700	0.27
1.79GHz	1.80GHz	32.74793	0.27
1.78GHz	1.79GHz	32.93088	0.27
1.76GHz	1.77GHz	33.11588	0.27

Table 11: Resistance and Capacitance example values for lowpass filter.

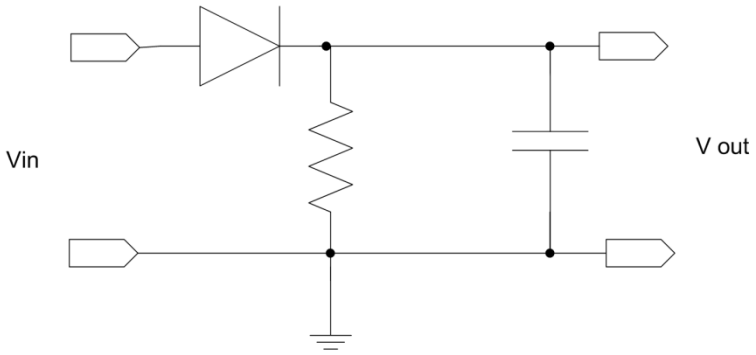

Figure 18. Envelope Detector.

An envelope detector can be created using a diode followed by a simple passive component lowpass filter as depicted in Figure 18. Example values for the resistor and capacitor can be found in Table 11 —the highest cut off frequency value can also be used to implement the envelope detector as well. For simulation purposes, to reduce the DC component, it is ideal to use lower order filters, however, in hardware, a first order filter does not always achieve the desired result thus for implementation, a higher order filter is advisable.

Since the intention of this thesis is only to discuss the feasibility of creating a network, actual implementation and optimization of the physical circuitry will not be discussed as it is beyond the scope of this thesis. Simulation analysis regarding the conceptual components for the discussion of communication feasibility will be detailed and discussed in the proceeding chapter.

3.4 Performance

3.4.1 Analysis

From [19, 21], the BER for a non-coherent binary FSK demodulation in a white Gaussian noise channel is given as (15), where ρ_b is the SNR per bit.

$$P_b = \frac{1}{2} e^{-\rho_b / 2} \tag{15}$$

An expression for ρ_b as a ratio of symbol energy to noise power is provided in (16).

$$\rho_b = \frac{E_b}{N_0} \tag{16}$$

N_0, the noise, and E_b, the energy per bit, can be represented as a ratio, (17), of the sensor data rate, R_b, to received signal power, P_r.

$$E_b = \frac{P_r}{R_b} \tag{17}$$

The ratio of symbol energy to noise ρ_b can be represented in terms of sensor data rate and received signal power, (18), by substituting (17) into (16).

$$\rho_b = \frac{N_0 P_r}{R_b} \tag{18}$$

By substituting (18) into (15), the resulting is (19), the equation for BER in terms of sensor data rate, received signal power, and noise.

$$P_b = \frac{1}{2} e^{-\frac{1}{2}\frac{N_0 P_r}{R_b}} \tag{19}$$

By solving (19) for R_b we arrive at (20), the equation for the sensor data rate in terms of channel noise, received signal power and BER.

$$R_b = -\frac{P_r N_0}{2\ln(2P_b)} \tag{20}$$

When solving (19) again for P_r, the expression, (21), is derived. This is the equation for received signal power in terms of BER, sensor data rate, and noise.

$$P_r = \frac{-2R_b \ln(2P_b)}{N_0} \tag{21}$$

For a white Gaussian noise channel, the noise has a power spectral density of $N_0 = -174\,\text{dBm/Hz}$. With this relationship, it can be calculated that in order to maintain a BER less than 10^{-6}, the typical range of the transmitted power over the DC line for sensor communications is microwatts to milli-watts.

3.4.2 Simulation

The simulation of the channel was constructed using Simulink. Note that Simulink does include FSK modulation and demodulation blocks, however, these blocks do not provide for the option of setting a specific center frequency as desired for the design provided in the previous chapter. To implement the four binary FSK modulators at node 5, the individual modulators were constructed using the blocks depicted in Figure 19.

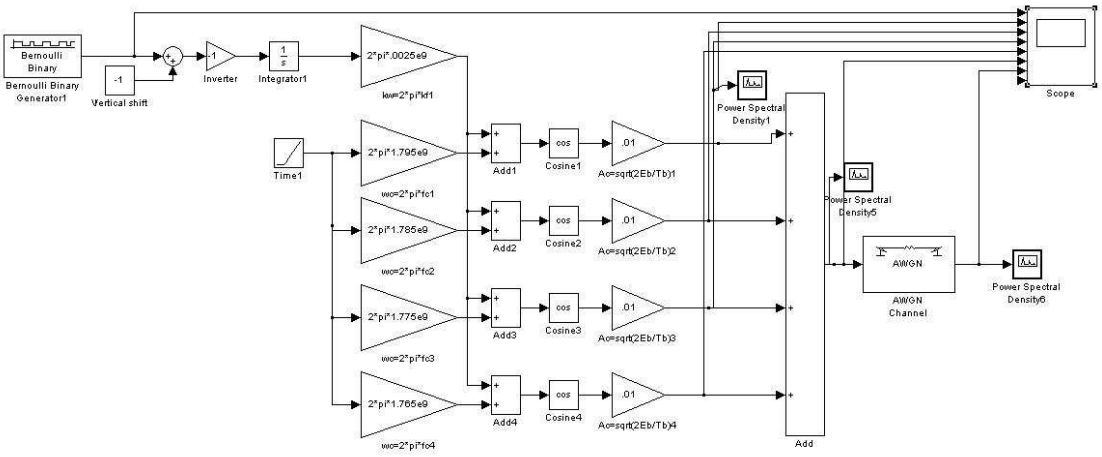

Figure 19. Signal transmission at Node 5 and Gaussian noise channel.

In Figure 19, the blocks following the binary generator, namely, a round addition block, a constant block with a value of negative one and an amplifier block with a value of negative one are for the purpose of inverting the signal. The simulated signal in this model is a Bernoulli randomly generated binary sequence. This same binary sequence is transmitted to all nodes for the purpose of reducing the simulation complexity and simulation time. Since Δf will remain constant for all four nodes, and the same message is being transmitted to all nodes, the message signal is input through this amplification constant block and routed to the input of an addition block for each individual modulator. By using these blocks to invert the signal, this provides that the higher frequency represents ‘1’; the lower frequency represents ‘0’.

For each of the four nodes, there are two frequency components from equation (5): one frequency component representing the ‘0’ bit, one frequency component representing the ‘1’ bit. With this, there will be eight symbol frequencies in total; four

of these are created with blocks that take a time input through an amplification block which in turn creates the value of the center frequency multiplied by time, *t.* The other four signals will be created by adding in the signal from the Δf constant block at each modulators' respective addition block.

From these four addition blocks, one for each respective node, the signal with two frequency values is then passed through a cosine block. After the signal is passed from the cosine block at each modulator, each modulator has an amplifier, represented by equation (2). For this simulation, an arbitrary value of 0.01 was chosen. In this implementation, the Bernoulli Binary Generating block is set to a sample time of 10^{-5}, and a seed generating value of 89. Solving equation (2) for the bit energy based on the arbitrary value and the sample time entered into the binary generator, the bit energy is solved to be 50 units. After the signal passes through the amplifier blocks, the four signals, one for each node are added together and passed through the AWGN (Gaussian White Noise) channel.

Figure 20 provides the simulation demodulation setup; this figure also depicts the modulated message going through the AWGN channel. From the AWGN channel, the signal passes to the slope circuit. The slope circuit is comprised of the two offset bandpass filters. From each filter, the signal then passes to the rectifier block, then to the lowpass filter block. As discussed in chapter 3, the combination of these two blocks, the rectifier and the lowpass filter comprise the envelope detector. The resulting two signals then pass through amplifiers to create a message signal that is strong enough to be evaluated by the comparison block. The resulting signal is the

transmitted message received at the specified node. Depending on the frequency settings entered to the bandpass filter blocks, the desired node will receive a binary information signal; to the other nodes, this signal will just appear as channel noise as their respective bandpass filters will eliminate this undesired frequency.

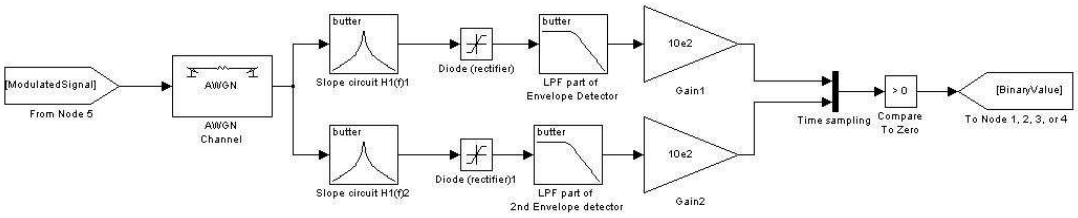

Figure 20. Simulation demodulator.

Band	Frequency (GHz)	Bit represented
1	$f_{10} = 1.76375$	0
	$f_{11} = 1.76625$	1
2	$f_{20} = 1.77375$	0
	$f_{21} = 1.77625$	1
3	$f_{30} = 1.78375$	0
	$f_{31} = 1.78625$	1
4	$f_{40} = 1.79375$	0
	$f_{41} = 1.79625$	1

Table 12: Simulation Frequencies

The specific values used for the various symbol frequencies in the simulation are provided in Table 12. Note that even though these values differ from those detailed in chapter 3, they are within the same desired band and should provide for a similar, if not better result. These values were modified from those listed in chapter 3 in order to simplify simulation computation and calculation. Results regarding this simulation will be provided in the following chapter.

4 Results

For the purpose of determining the feasibility of PLC on this desktop powerline, a data rate of 10 Kbps was chosen. Rates similar to this are more than sufficient for demonstrating applications such as sensing temperature, or gathering other statistics regarding other components on the network. For this rate R_b = 10 Kbps, the resulting symbol period is determined to be $T_b = 10^{-5}$seconds, based on the equations presented in section 3.4.1. Even though it was mentioned in the previous chapter that for binary FSK, the minimum frequency separation for orthogonallity is, $\Delta f_{\min} = 1/(2T_b)$, a frequency separation of 2.5 MHz was chosen instead of 50KHz due to the abundant bandwidth available by the DC powerline for this application.

Figure 21 depicts the simulated BER performance as a function of E_b/N_0. In this figure, it can be compared that the theoretical BER curve for a noncoherent binary FSK is very close to the simulated result. With the primary objective of the simulation being to determine the performance of the channel with multiple simultaneous binary FSK transmissions, this figure depicts that the resulting BER rate of the simulation is very close to being as expected from theoretical models.

In this simulation, all four bands transmit simultaneously and at the same power level. The BER was assessed based on the performance of band 2 from Table 12. Band 2 was chosen to represent the BER because it presents the worst-case scenario due to the two immediate adjacent bands.

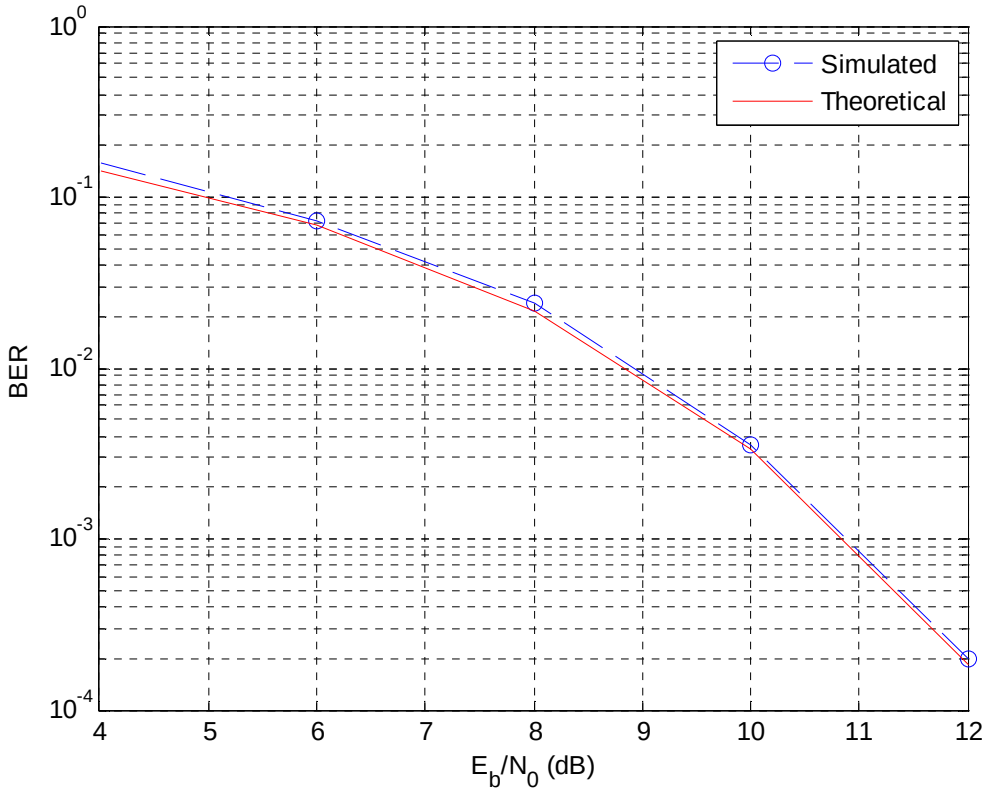

Figure 21. BER performance: Theoretical vs. Simulated.

Due to the nature of the simple bandpass filters used in the design, it is likely that there would be a small amount of cross-band interference. By comparing the simulated BER values to the theoretical values in Figure 21, it can be seen that the cross-band interference is negligible. This provides that since the gap between bands is relatively large, the anticipated cross-band interference experienced due to the simple nature of the bandpass filters should not be an issue when implementing the communication method with enough bandwidth.

With very high E_b/N_0 values, the simulated BER performance will be expected to perform slightly worse. This is because in the high E_b/N_0 range, cross-band interference will be more dominating. Since simulation for such cases takes an unreasonably long amount of time, such results are not included in this thesis. In any event, the system will not be expected to operate at such high E_b/N_0.

This simulation and result verifies that the choices of bands and frequency separation for low-data-rate sensor communications are appropriate, since the attenuation for each band is minimized and cross-band interference is negligible even with very simple passband filters.

5 Discussion

Table 13 provides a summary of the useful information pertaining to the design implementation choices regarding DC powerline communication for the desktop computer. In regards to transmission distance, the vehicle cable length is usually less than one-tenth the distance HomePlug typically transmits over. In the desktop PC, most powerline cabling is less than 1 m, thus there is a similar ratio between vehicle and PC as home power grid cable length and vehicle cable length. The biggest concern with the short cable length is that short cable lengths between nodes may be viewed as a short circuit, if terminated by small impedance. From measurements of the channel attenuation discussed in Section 3.1, and Table 4 there is a distinct difference between channel segments, even though measuring lengths less than the suggested 50 cm minimum.

Since much of the vehicular PLC research is regarding implementing the HomePlug standard directly on the vehicular line, the frequencies and modulation schemes for these are the same. For the experiments that did not use this approach, notably [9], frequencies of over 100 MHz are suggested, with their test using a center frequency of 200 MHz. From the measured results in Section 3.1, the results obtained seem to correspond with this suggestion of using frequencies greater than 100 MHz.

The most notable difference between PLC for the home use, PLC for the vehicular use and PLC for the desktop PC is the attenuation measured on the communication channel, and frequency band needed for PLC in the desktop PC. With

the home use PLC channel attenuation being 40 dB to 60 dB, and the vehicular channel attenuation being nearly half due to the metal body of the car, a similar attenuation should be expected for the desktop PC. From the measurements in chapter 3, the attenuation seen on the desktop computer powerline tends to be between 30dB and 40dB, between the values found for the home use and the vehicular use.

	HomePlug	**Vehicle**
Transmission Distance	1 mi ≈1.6 km	50 cm minimum to 9 m
Frequency Used	2 MHz to 28MHz	200 MHz [9]; 10 - 30 MHz [10, 11]; 4 - 21 MHz [12, 13]
Attenuation	40 dB to 60 dB	20 dB to 30 dB [9]
Modulation & Demodulation	OFDM modulation	OFDM modulation DBPSK or DQPSK modulated subcarrier; Spacing between 2 subcarriers is 195.531 kHz noncoherent demodulation
Achieved Data Rate	200 Mbps	5 Mbps [10]

Table 13: Summary of Background PLC Literature

6 Conclusion

In this thesis, a low-data-rate sensor communication network inside a computer chassis that employ the existing DC powerline is investigated. The goal is to design a very simple network that requires least amount of power and hardware resources. Whether it be for the HomePlug standard, within a vehicle, or within a desktop computer, powerline communication provides the advantage of a more simplified means for connecting components to an existing power network and can potentially reduce the need for dedicated communication cabling. In turn, reducing the physical complexity of a system as well as decreasing the amount of raw materials, cost, weight and volume needed for such dedicated communication cables.

Then a simple multiple access scheme that employ frequency division is designed and optimized. This network is also analyzed and simulated for effectiveness. Since the frequency spectrum provided by the DC power line channel is abundant for low-data-rate sensor communications, this resource is efficient exploited to virtually eliminate the potential interference among multiple parallel channels

In this thesis, the background information regarding the HomePlug standards, the IEEE P1901 standard and developing vehicle use implementation was provided and discussed. Since it was not possible to test the commercial standard frequency range provided in the background research, this thesis starts with obtaining measurements to understand the characteristics of the channel provided by the DC powerlines of a desktop computer. From these measurements, a simple multiple access scheme that employs frequency division is designed and optimized. It was

devised to use a bank of four FSK modulation devices at the primary node and single noncoherent FSK demodulation devices for this scheme. Since there is ample frequency provided by the DC powerline channel for low-data-rate sensor communications, this resource is efficiently exploited to virtually eliminate the potential interference among multiple parallel channels.

This devised network is then analyzed and simulated for effectiveness. By performing the analysis at band 2, the worst case scenario, results comparable to the theoretical estimated value for a BFSK system were obtained. Using the calculation values for a data rate of 10Kbps in the simulation has proven the system to be feasible for use as a low-data-rate sensor network.

With this thesis, a potential for future work regarding the development of the powerline within a PC as an additional means for gathering internal system data, as well as providing for the future potential of higher data rate communication systems has become more possible and realizable. Possible future work stemming from this research could include the physical implementation and optimization of this sensor network, assessment of the impact to the DC power when the sensor communication network is active, and further research regarding the power traces within the motherboard as means of communicating within the computer.

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