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As the demand for real-time information in engineering and health care systems keeps increasing, the need for wireless sensor nodes is also continuously increasing. As a result, the cost and effort involved in installing and maintaining batteries to power the numerous sensor nodes is growing exponentially. Providing a cost effective and maintenance free alternate energy source is the motivation behind the development of energy scavenging solutions for self-powered sensor networks.

In this research, an energy scavenging system that extracts energy from ambient radio-frequency waves transmitted in the 2.4 GHz ISM band is designed. The harvested energy is efficiently managed with an ultra low-power switched capacitor buck-boost DC-DC converter to wirelessly power the nodes in a wireless sensor network.

Analysis and optimization of the number of rectifier stages required to achieve efficient power conversion is carried out. To improve far field conversion efficiency and extend the scavenger sensitivity, the threshold voltage of the diodes in the recti-

fiers are reduced to about 50 mV by using the floating-gate programming technique. The active power consumption of the switched-capacitor DC-DC converter is around 1.2 μW. A micro-power analog to digital converter for variable gain selection and a sub-threshold linear voltage regulator for providing the start-up, are designed. The integrated system provides a fully autonomous micro-energy scavenging solution for the sensor nodes.

The simulated results suggest that the scavenger achieves a 10% higher conversion efficiency than the most recently reported work. The operational distance of this improved energy scavenging solution is 6 meters (in free space) from an intentional RF transmitter operating under FCC specifications at 2.4 GHz. The targeted application of this research is to provide an alternate energy solution for low power devices, including wireless sensor nodes and bio-medical applications.

Efficient RF Energy Scavenging and Ultra-Low Power Management for Powering Wireless Sensor Nodes

by

Vikrant P Arumugam

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I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

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1.1. Motivation for Energy Scavenging

As the wireless technology continues to evolve, the proliferation of sensor nodes in a wireless sensor network (WSN) also continues to increase. The primary source of power for the wireless sensor nodes is a battery. As the cost and effort involved in maintaining and replacing the batteries in these sensor nodes keeps increasing with the increase in the number of sensor nodes [1], the key focus shifts to finding alternate sources of energy.

Ambient sources of energy such as light, kinetic and heat have been harnessed for powering devices over a period of time dating back to a few decades. The process of harnessing energy from the ambient, or otherwise unused energy sources in the environment is referred to as *energy scavenging*. Energy scavengers can either eliminate the batteries by replacing them or increase the lifetime of the battery by replenishing the lost charge.

1.2. Types of Energy Scavengers

Typical energy scavengers are photoelectric (light) [2, 3], piezoelectric (vibration) [4, 5], thermoelectric (heat) [8, 9] and electromagnetic (radio-frequency). Electrical energy converted from these sources can be stored and used to power analog or digital circuitry. Table 1.1 shows the various ambient energy sources and the power density available for extraction [5].

TABLE 1.1: Most commonly available ambient energy sources. [5]

Energy Sources	Power density (μW/cm^3)
Solar/Light (Photovoltaic)	15000_{sunny} - 150_{cloudy}
Heat (Thermoelectric)	100 @ 1°C gradient [7]
Vibration (Piezoelectric)	200 [5]
Electromagnetic (Radio Frequency @ 2.4 GHz)	400 @ 1 m - 15.8 @ 5 m [35]

1.3. Generic Block Diagram of an Energy Scavenger

A generic block diagram of the scavenger circuit in an integrated system is shown in Figure 1.1. The system comprises of an energy capture (transducer) and convert circuit (power converter). The transducer transforms the input energy into an electrical output.

In many cases, the transducer is followed by an input matching network which ensures maximum power transfer into the system. The power converter circuit, depending on the energy source, can be a rectifier (AC-DC) or a DC-DC converter. The power converter is followed by a power conditioning circuit which provides current limitation and over voltage protection functionalities. The energy storage system (ESS) can be a rechargeable battery, a super capacitor or any other storage medium.

The output of the power conditioning circuit can vary depending on the power density available for havesting. This stored power needs to supply a device or load at a particular output voltage. The block implementing this power management

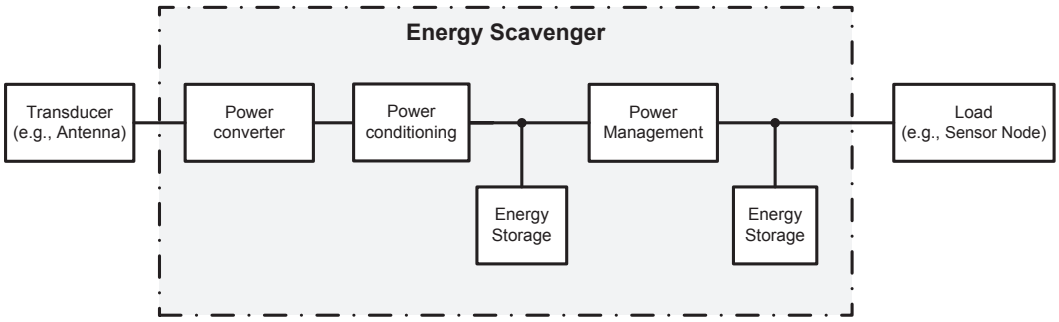


FIGURE 1.1: Block diagram of a typical energy scavenging system.

functionality can be a linear regulator or a switching converter, which converts a varying DC input to a constant DC output voltage. The extracted energy is stored in a charge storage element for future use.

1.4. Motivation for Radio Frequency Energy Scavenging

RF energy scavenging can play a significant role in powering and sustaining the numerous sensor nodes which are installed in harsh inaccessible environments. For wireless sensor networks powered by radio frequency (RF) waves [10, 14], a base station transmits the RF energy. The antenna acts as a transducer by capturing the incoming electromagnetic RF waves and converting them into electric current.

The primary advantage of harvesting RF energy over other energy sources is the availability of a controllable source in the form of an intentional radiator transmitting RF energy. Other sources are not always dependable for continuous supply of energy, such as solar energy where the energy available depends on the illuminated condition of the sensor location at a particular time. RF energy can be extracted

from the energy available during the transmission by public RF telecommunication networks, such as mobile phones and wireless routers.

The main challenge in RF energy scavenging is the efficient scavenging of the relatively low levels of available harvestable energy. It can be seen from Table 1.1, that depending upon the distance from the transmitter, the available RF energy is very limited. This makes it difficult to continuously drive loads requiring power on the order of a few hundred micro watts. In such cases, the extracted energy is stored in an energy storage element over a period of time. The loads can then be supplied energy for short time intervals. This is referred as the *burst mode* of operation for the scavenger.

1.5. Organization of the Thesis

This thesis discusses the design of an efficient RF energy scavenger circuit. Chapter 2 provides an overview of the various energy efficient techniques to harvest and store the ambient RF power. The details of the most recent work done in the area of efficient rectification and power conversion and the significant results obtained are compared and discussed.

Chapter 3 discusses the details of achieving an efficient RF rectification system. The regulations limiting RF energy transmission and the various definitions in a RF energy scavenging system are discussed. The analysis, optimization and design techniques for realizing an efficient power conversion circuit are presented.

Chapter 4 elaborates upon the system level description and component value optimization of the power management unit. The circuit details and the simulated performance of the switching power converter are presented and analyzed.

Chapter 5 investigates the simulated results on the performance of the overall RF energy scavenging circuit. It concludes with a comparison of results of the current design with other prior work.

Chapter 6 provides the conclusions of this work and future research problems in the area of energy scavenging.

2. SYSTEM LEVEL OVERVIEW AND LITERATURE REVIEW

2.1. Introduction

The previous chapter introduced the concept of energy scavenging from ambient energy sources. To extract radio frequency energy, a dedicated signal source is required that satisfies the FCC rules for transmission in certain ISM bands. The strength of the transmitted RF energy decreases rapidly as the distance from the RF source increases. In order to maximize the extracted energy from these low strength RF waves, design of ultra-low power circuits, which consume power in the order of nano or pico watts, is critical. In this chapter, prior work published in the area of RF energy harvesting is presented describing their key contributions and their shortcomings. Finally, a new architecture which overcomes these shortcomings is presented.

2.2. RF Power Transmission - Regulations and Limitations

The concept of wireless transmission and reception is shown in Figure 2.1. A transmitting station transmiting high power RF energy in the ISM (Industrial, Scientific, Medical) bands is chosen.

The maximum transmitter power is 4 Watts (30 dBm transmission + 6 dB antenna gain) of EIRP (Effective Isotropic Radiated Power) at 2.4 GHz, according to the Federal Communications Commission (FCC) specifications [11]. The strength of the transmitted signal decreases quadratically as the distance from the transmit-

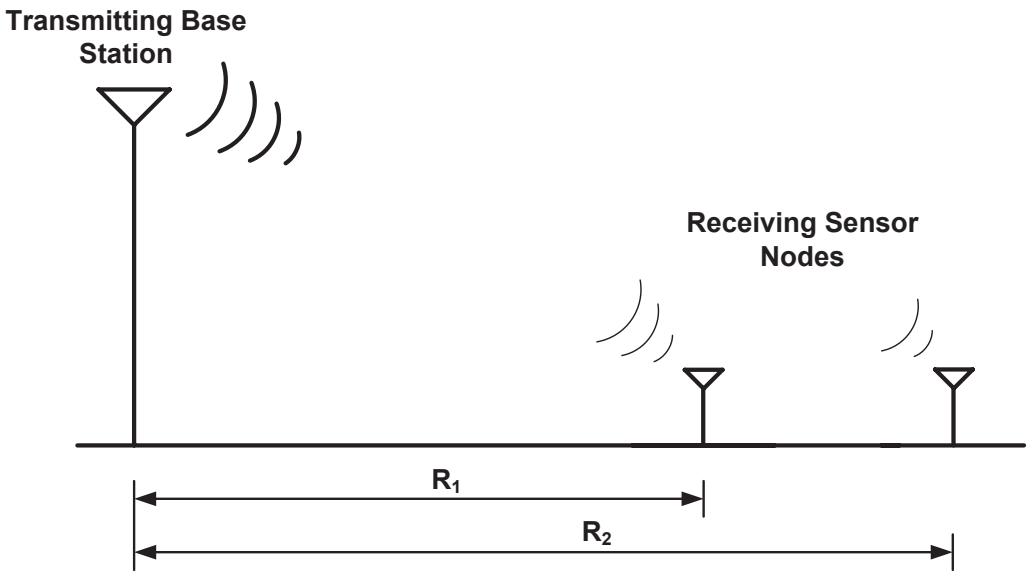


FIGURE 2.1: Wireless power transmission and communication network with sensor nodes.

ter increases. The power loss in free space is governed by the Friis transmission equation [35]. Equation (2.1) gives an ideal estimate of the received power given the transmitted power and the distance from the source.

$$P_r = P_t G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2 \tag{2.1}$$

where P_r and P_t are the received power and transmitted power in Watts at the antenna terminals, respectively. G_r and G_t are the antenna gain of the receiving and transmitting antennas, respectively, λ is the wavelength of the transmitted signal in meters and R is the distance in meters between the transmit and receive antennas.

Figure 2.2 shows that the received power for signals transmitted in a higher

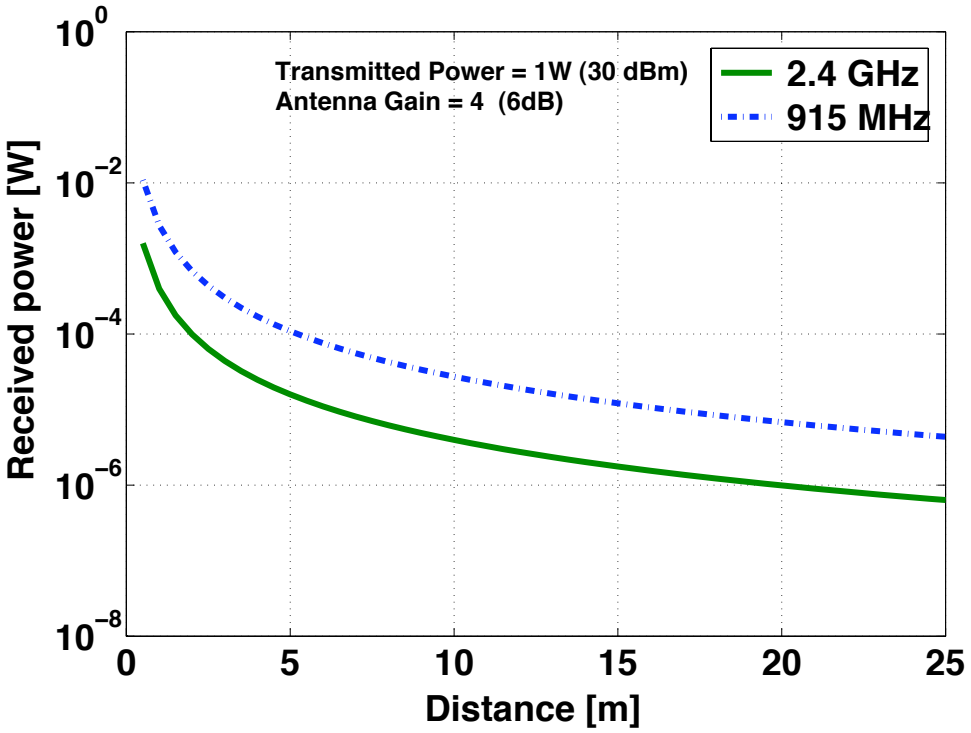


FIGURE 2.2: Received power as a function of free space distance from a 1 W RF source.

frequency ISM band (2.4 GHz - 2.4835 GHz) is smaller than that for signals transmitted in a lower frequency ISM band (905 MHz - 928 MHz).

2.3. Components in a RF Energy Scavenging System

An RF energy scavenging system in a passively powered wireless sensor node application is shown in Figure 2.3. The energy scavenger harvests the ambient RF energy, stores it across an energy storage element, and powers the RF and baseband signal processing circuitry.

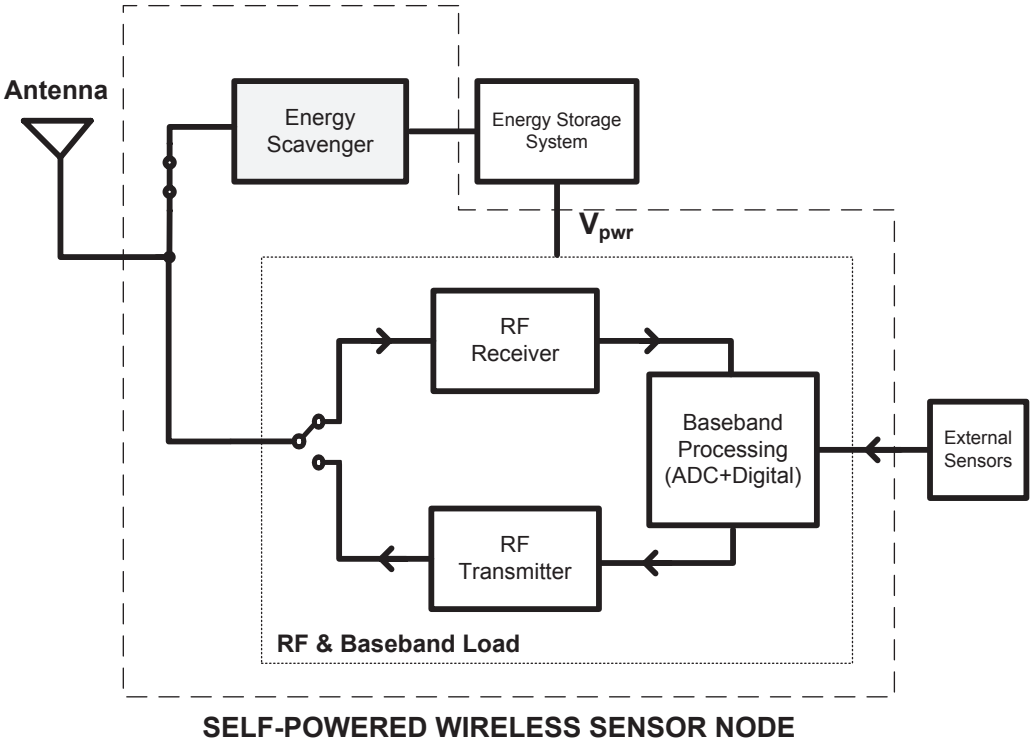


FIGURE 2.3: RF energy scavenger in a passively powered wireless sensor node.

The components of the RF energy scavenging system can be explained with the help of the block diagram shown in Figure 2.4. The system has four critical blocks to convert the RF energy to usable DC power.

1. An input matching network which provides lossless matching between the antenna source impedance and the input impedance of the circuit.

2. A full wave rectification stage which provides sinusoidal RF to DC signal conversion with programmable threshold voltage MOSFET diodes to achieve high efficiency rectification.

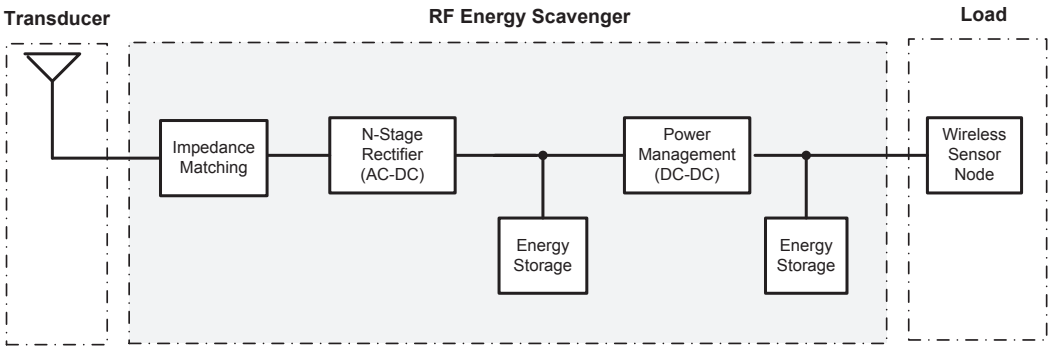


FIGURE 2.4: Block diagram of a typical RF energy scavenging system.

3. A power-efficient output voltage regulation scheme capable of driving a wide range of output loads. The output voltage of the rectifier can vary between a few hundred milli-volts to more than 5 volts, depending upon the incoming power. The regulator provides a stable supply voltage.

4. An energy storage unit which can either be a super-capacitor or a rechargeable battery.

From Figure 2.4 it can be observed that the efficiency of a RF energy scavenger is a function of two cascaded systems: a RF-to-DC conversion system (rectifier) and a DC-to-DC conversion system (regulator). In order to realize a highly efficient scavenger, the internal loss components in both functional blocks are identified and techniques to minimize the loss are found.

2.4. RF-to-DC Conversion - Rectification

The input signal received by the antenna of the energy harvester, as shown in Figure 2.4, is sinusoidal in nature. This sinusoidal RF input signal is converted into a DC voltage by a rectifier. The critical loss component in a rectifier is the on-resistance of the MOS diodes. In other words, the power lost in an active rectifier is defined as the amount of power required to overcome the threshold voltage of the diodes in the rectifier.

Earlier work on highly efficient rectifiers for RF energy scavengers focused on various techniques to reduce the threshold voltage of the MOS diodes. Apart from using Schottky diodes, native and low threshold voltage devices, the threshold voltage can be reduced by other techniques as proposed in [12, 13, 14].

2.4.1. Comparison of energy efficient rectifier architectures

The work done by Umeda in [12], presents an active switched capacitor circuit and an external gate-source bias voltage to bias the MOS diodes in the rectifier circuit. The extra circuitry required for the bias voltage generation and the requirement for secondary battery storage makes this three stage rectifier solution not feasible for autonomous energy scavenging operation.

A RFID tag described in [13] shows a double stacked one-stage rectifier performing the RF-to-DC conversion. The current sensing scheme used in this configuration helps reduce the threshold voltage of the PMOS diodes used in the rectifiers. But the reduction in the threshold voltage achieved using this scheme is not significant and the scheme dissipates some static power while using huge resistors occupying a larger area.

The work done in [14] shows 36 stages of rectifiers cascaded to realize a higher output voltage. The threshold voltage of the MOS diodes is reduced by using a single-poly floating gate programming technique as described in [16]. This solution is shown to generate a higher output DC voltage compared to the previous work under similar load conditions. The fundamental problem of achieving maximum rectification efficiency is not addressed by this solution since a larger number of stacked rectifier stages consume higher quiescent power for operation. In other words, the higher the number of active components in the system, the higher the internal loss and hence the lower conversion efficiency.

Shameli proposed a power harvester with an increased operating range. In [18], he claims that this increase is achieved by a passive voltage amplification of the incoming input signal with the help of a high Q impedance matching circuitry. The published results indicate that the minimum power required to achieve a 2 μW output power at 1 V output is about -14.1 dBm with a four-stage standard CMOS rectifier. The threshold voltage of the CMOS diodes remains unaffected and hence the dead zone for rectification is significant.

The power extraction system built for RFID applications by Mandal [20, 21] derives an optimization metric for realizing rectifiers with optimal performance. The number of rectifier stages and the sizing of the MOS diode tied transistors in the rectifiers are found by fixing the output voltage needed for a particular load current drive. The availability of low threshold voltage transistors in the process helps this design achieve a better power conversion efficiency than conventional rectifiers.

Recent work on energy scavenging by Salter [22], proposes an RF energy scavenging system implemented with a rectifier followed by a switched capacitor DC-DC converter. The rectifier circuit used in this design is a Villard voltage doubler in a

standard CMOS process. The rectifier outputs a DC voltage of 1 V driving a 200 nA load at a input power of -16 dBm. Hence, the operating range of this harvester at 2.2 GHz is restricted to 4 meters in free space.

2.4.2. RF rectification design challenges

A comparison of all the different rectifier configurations discussed earlier shows the need for an optimized rectifier configuration with a high far field RF rectification efficiency. A RF harvester with an efficient far field rectifier can operate at a longer distance from the transmitting source.

A study and design comparison of different rectifier configurations is done from [12, 13, 23, 21] and the voltage doubler configuration in [14] is chosen for the rectifier. The threshold voltage of the CMOS diodes is reduced by the floating gate programming technique proposed in [16, 17]. In this research the number of rectifier stages are optimized considering high RF rectification efficiency and high output voltage. Passive voltage amplification using a high-Q impedance matching network is achieved to increase the useful range of power harvesting.

2.5. DC-to-DC Conversion - Regulation

The input RF sinusoidal signal is converted to a DC output voltage by a rectifier circuitry. The output of the rectifier can vary between low to high DC voltages depending upon the distance of the scavenger from the transmitting base station. The load on the rectifier also defines the output voltage of the system. The DC output voltage is needed to power up devices having a supply voltage compliance range that is typically within +/- 5% of the nominal operating voltage.

Since the RF power available for extraction is in the range of micro-watts, the best choice for a voltage regulator is a switched capacitor DC-DC converter [24]. The switched capacitor converter, also called a charge-pump based converter, works on the principle of charge sharing between the input and output capacitors during non-overlapping clock phases. The losses related to this process are due to the non-ideal nature of the switches transferring the charge, the non-ideal capacitors, and the circuitry driving the switches. Several switched capacitor converter designs are available in the literature, but only a few of them are targeted to operating efficiently in ultra-light load conditions. A good converter design should have a high power efficiency across a wide range of DC input voltages. The typical efficiency of the converter for ultra-light loads in range of 20 μW is above 60% [25, 29].

2.5.1. Prior work on efficient regulator topologies

The analysis and optimization of components of a switched capacitor DC-DC converter for efficient conversion and output regulation is provided in [29, 30]. The converter conduction losses are modeled as a resistive output impedance which is derived for both the slow switching limit (SSL) [31] and the fast switching limit (FSL) conditions [32]. The optimization of the switching frequency, the size of the transfer capacitance and the on-state switch resistance is carried out for a particular load current drive at fixed output. In [27], a DC-DC converter for a wireless tire pressure sensor load which could regulate the output at load power levels as low as 20 μW with an efficiency of above 60% was presented. The primary reason for the lower efficiency at these light-loads is the active circuit power consumption of the converter.

In [25, 26], an output voltage scalable switched capacitor DC-DC converter

capable of driving loads in the range of 10 μW to 250 μW is presented. An output load voltage is regulated between 300 mV to 1.1 V with a constant input voltage of 1.2 V. The efficiency of the converter in the load range specified above is 75%. The converter operates in the pulse frequency modulation (PFM) mode, which is crucial in achieving high efficiency for a low power system such as an energy scavenger. The efficiency becomes less than 75% at very low load powers of about 4 μW, as the leakage in the PFM control circuitry dominates the losses.

The design of a resistor emulated switching converter for RF energy scavenging is presented in [28]. The converter is capable of driving ultra-light loads as low as 0.5 μW with an efficiency of 35%. The RF energy is scavenged by a RF rectifying antenna source with an rectification efficiency of 10 %. Hence the overall conversion efficiency of the entire RF harvesting solution is around 7% at received power levels of -18.2 dBm. The inductor based switching converter has a 300 μH off chip inductor which is not integrable for the sensor node applications.

2.5.2. Regulation design challenges

Highly efficient power management units in a RF energy scavenging application are needed that address the shortcomings of the previous published work. The power management solution should be capable of driving a light load at a constant DC output at low received power levels. A switched capacitor based converter solution is selected to achieve an integrated on-chip solution. The system and circuit level design of the power management unit is discussed in Chapters 4 and 5, respectively.

3. EFFICIENT FAR FIELD RF RECTIFICATION

3.1. Introduction

A system which harvests ambient RF energy would ideally transfer all the incoming input power to the output load. From the analysis of maximum power transfer, half the incoming power is lost across the source impedance of the receiving antenna. Hence the challenge is to deliver the maximum of remaining 50% of the input power to the output load. Building low power harvesters is the key challenge in realizing highly efficient energy scavenging systems.

3.2. Critical Parameters in a RF Energy Scavenging System

In this work, a RF-DC conversion circuit which converts the 2.4 GHz RF input signal to a DC output voltage under different load conditions is designed. The 2.4 GHz band is chosen over the 915 MHz band because of the feasibility of realizing smaller external on-board components such as the antenna and other passive impedance matching elements. However, the received power decreases by a factor of 6.8 ($\frac{2.4\ GHz}{0.915\ GHz}^2 \approx 2.6^2$) when operating in the higher frequency band.

The approach taken to realize higher power conversion efficiency is to decrease the number of active components in the design. Fewer active components in the system lowers the active power loss, thereby increasing the efficiency. An increase in the far field power conversion efficiency also implies a lower power-up range or an increase of the sensitivity of the harvester to lower input received power levels.

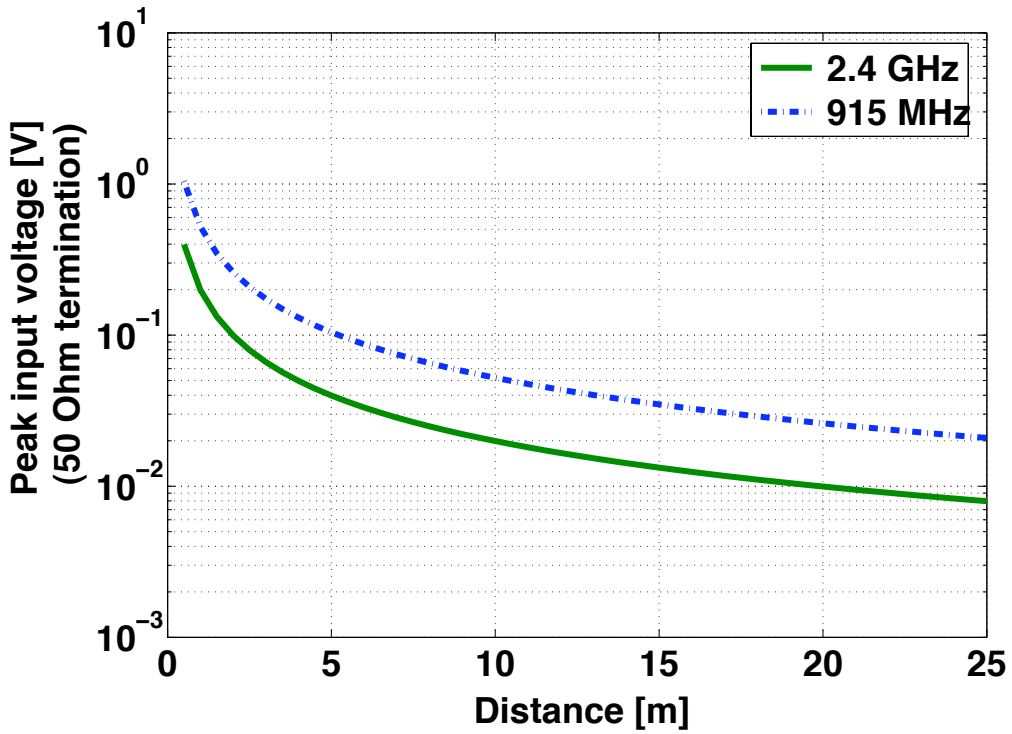


FIGURE 3.1: Peak voltage across a 50 Ω terminated system from a 1 W Source.

The incoming signal strength to the harvester depends on a number of factors, the first and foremost being the distance from the transmitting source. From Friis transmission equation, the power received at 5 meters away from the transmitter at 2.4 GHz is 15.8 μW. The corresponding peak input sinusoidal amplitude for a 50 Ω matched system is 40 mV (peak), as shown in Figure 3.1. This low input voltage level seen at the far field distance is below the threshold of the MOSFET diodes in the rectifier.

In practice, other interference phenomena like multi-path fading, reflection and absorption, can also significantly affect the input signal power reaching the harvester at a particular distance from the source. Since, these effects are not

modeled in the Friis transmission equation and most other designs have used the free-space assumption for received power calculations, the interference effects are not considered for comparison and evaluation.

3.2.1. Power-up threshold of the Scavenger

The threshold voltage of a typical CMOS diode is about 600 mV [41] and the input power required to overcome this threshold voltage in a typical 50 Ω input terminated system is given by:

$$Input\ Power\ (P_{in}) = \frac{V_{rms}^2}{R_s} = \frac{V_{pk}^2}{2R_s} = \frac{0.6^2}{100} = 3.6\ \text{mW} \tag{3.1}$$

where R_s is the characteristic impedance of the antenna and is typically 50 Ω.

Hence, the input power required by the energy harvesting system to build any significant voltage at the output of a single stage rectifier voltage is about 5.56 dBm (3.6 mW). This causes a *dead-zone* for the rectifier. The minimum power required to overcome the rectification dead zone is called the *power-up threshold* of the harvester [20].

From Friis equation, to extract 3.6 mW of received power, the scavenger needs to operate as close as 0.5 meters from the source. This distance is considered near field. In the interest of achieving efficient far field operation, the power-up threshold of the system needs to be minimized.

By reducing the threshold voltage of the rectifying diodes, the power-up threshold of the system can be minimized. A technique called as *single-poly floating-gate programming* has been used in [16] to reduce the threshold voltage of the CMOS devices. This technique gives a programmability option for the power-up threshold.

The second technique to increase the operating range or scavenger sensitivity is to overcome the power-up threshold of the scavenger for lower input power levels. Passive amplification of the voltage level of the ultra-low power signals reaching the harvester helps in overcoming the threshold. The matching network present at the input of the system, shown in Figure 2.4, provides passive voltage boosting. The following section analyzes the passive amplification of the incoming signal by choosing an appropriate input matching network.

3.2.2. Passive voltage amplification

The transmitted RF signal is received by a wireless node in a sensor network with the help of an antenna. The antenna used in a typical sensor network has certain characteristic impedance, R_s, typically 50 Ω, and is impedance matched to the rectifier through a passive lossless matching network. The impedance modeling of a RF energy scavenging circuit is shown in the Figure 3.2.

The input impedance of the rectifier circuit, Z_{rect}, is predominantly capacitive (C_{rect}) and resistive (R_{rect}).

$$Z_{rect} = R_{rect} \parallel \frac{1}{sC_{rect}} \tag{3.2}$$

The operation of the full-wave rectifier can be explained by two half cycle operations of the input AC sinusoid as shown in Figure 3.3. During the negative half of the input sinusoid, the diode D1 gets forward biased and the DC voltage across D1 is clamped to $(V_{inputpk} - V_{th})$. During the positive half input sinusoid the diode D2 gets forward biased and the output capacitor C2 is charged to $2(V_{inputpk} - V_{th})$. The rectified output voltage needs to be regulated over the entire operational range of the harvester.

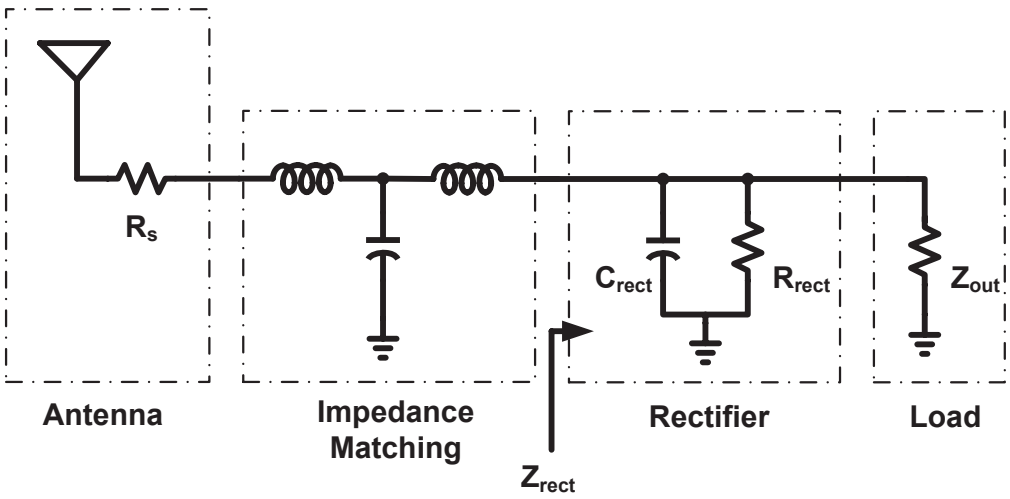


FIGURE 3.2: Impedance model of the RF energy scavenging circuit.

Cascading a number of rectifier stages affects the input impedance of the rectifier. Consider a full-wave rectifier model built from a simple diode model and, the input bypass and output storage capacitors. The addition of an extra rectifier stage decreases the reactive component by adding capacitances in parallel and reduces the resistive component by adding resistances in parallel to the existing network.

The passive impedance transformation network built using inductors and capacitors has a particular quality factor, Q, associated with it. At resonance, the resistive and capacitive components of the rectifier network can be transformed into a series R_{sr} and C_{sr} network, as shown in Figure 3.4.

At resonance [15],

$$R_{sr} = R_{rect}.\left(\frac{1}{1+Q_{rect}^2}\right) \tag{3.3}$$

$$C_{sr} = C_{rect}\left(\frac{1+Q_{rect}^2}{Q_{rect}^2}\right) \tag{3.4}$$

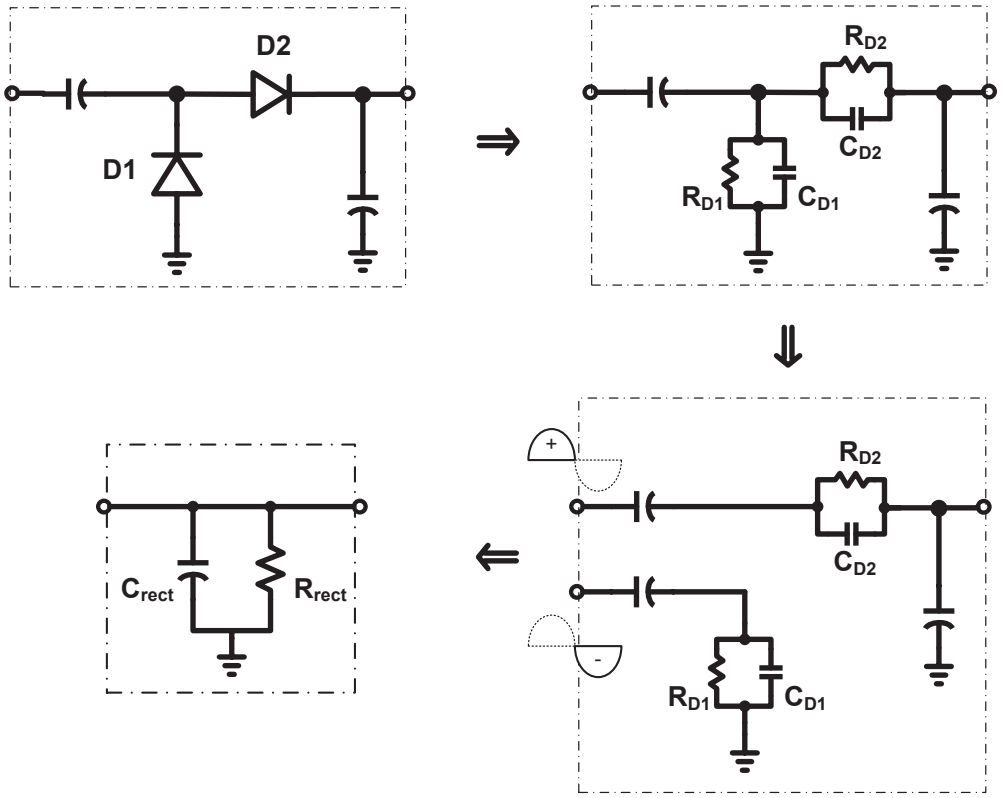


FIGURE 3.3: Impedance modeling of the full-wave rectifier.

where Q_{rect} is the quality factor of the rectifier circuit given by,

$$Q_{rect} = \omega_0 . R_{rect} . C_{rect} \tag{3.5}$$

with ω_0 being the resonant frequency of the matching network.

The model of a passive voltage amplification network is shown in Figure 3.5. When the received input signal strength is very low, the input voltage amplitude of the signal, V_1, is very low. The presence of the matching network can provide a passive input voltage amplification to V_1 with the loaded Q factor of the rectifier. The amplified input signal can overcome the threshold voltage of the MOSFET

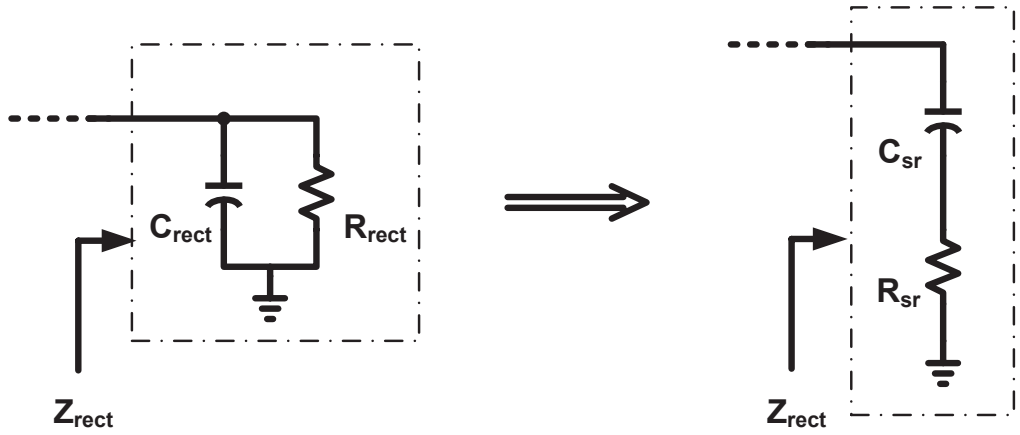


FIGURE 3.4: Parallel to series transformation of the full-wave rectifier impedance model.

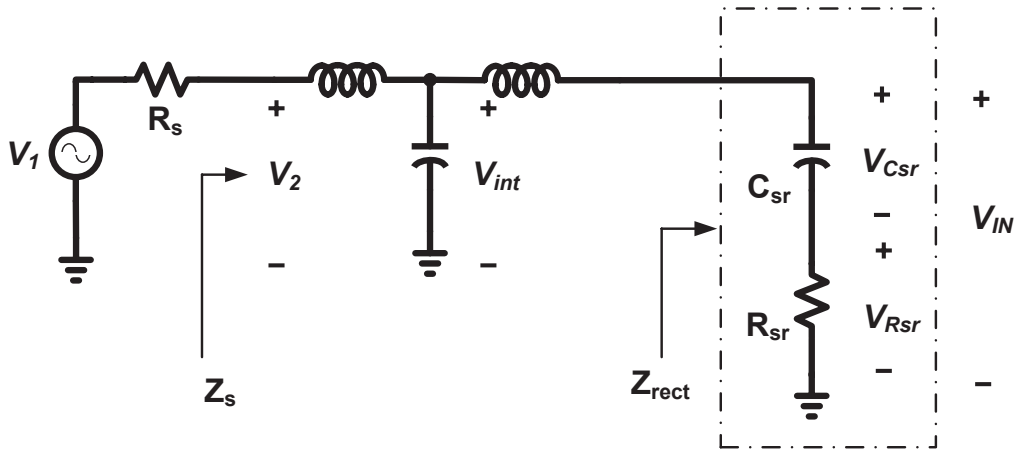


FIGURE 3.5: Model of the passive voltage amplification network.

diodes in the full-wave rectifier. The matching network being lossless also provides the rectifier circuit with a proportionally reduced drive current, by the same factor Q_{rect}. The analysis for passive voltage amplification follows.

At resonance,

$$Z_s = R_s \tag{3.6}$$

$$V_2 = 0.5 * V_1 \tag{3.7}$$

The power dissipated across the antenna characteristic impedance R_s is equal to the power dissipated across the only resistive component in the rectifier model, R_{sr}. The relationship between the voltages across R_s and R_{sr} is given by:

$$\frac{V_{Rsr}}{V_2} = \sqrt{\frac{R_{sr}}{R_s}} \tag{3.8}$$

At resonance, the voltage across the effective capacitance C_{sr} is Q_{sr} times the voltage across the effective resistance R_{sr}. Thus, the voltage at the rectifier input terminals V_{IN} is given by,

$$|V_{IN}| = |V_{Csr} + V_{Rsr}| \approx V_{Rsr}.Q_{sr} \tag{3.9}$$

Substituting (3.8) in (3.9),

$$Passive\ Voltage\ Gain : \frac{V_{IN}}{V_2} = Q_{sr}\sqrt{\frac{R_{sr}}{R_s}} \tag{3.10}$$

The above relationship between the passive voltage amplification and the Q factor of the rectifier, explains the significance of a high-Q matching network in energy harvesting applications. The amplification helps in increasing the sensitivity of the scavenger to lower received input power levels.

Under loaded conditions, the rectifier MOSFET diodes need to drive load currents at a fixed output voltage with the available incoming input power. Though the input voltage of the rectifier is amplified, the reduced input current drive to the rectifier is incapable of meeting the load current requirements and hence yields a lower rectified output DC voltage when loaded.

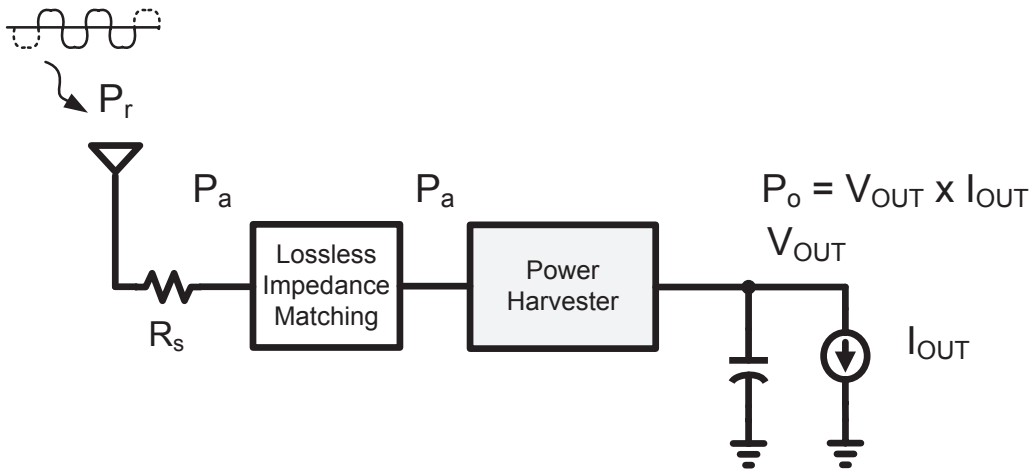


FIGURE 3.6: Block diagram showing the received, available and output power in the system.

3.2.3. Power Conversion Efficiency of the Scavenger

A critical metric which defines the performance of an energy harvesting circuit is the *power conversion efficiency (PCE)*. The conversion efficiency is defined as the ratio of output power available for driving the load, to the input power available at the rectifier input terminals. Figure 3.6 shows the components in an energy harvesting system and the power available at the input and output terminals.

$$\textit{Power Conversion Efficiency (PCE)} = \frac{P_o}{P_a} \tag{3.11}$$

where P_o and P_a are the output power driving the load and the power available at the rectifier input terminals, respectively.

According to maximum power transfer, under ideal input matched conditions, only one half of the input received power (P_r) is available at the rectifier input terminals for harvesting. The *power harvesting efficiency (PHE)* is defined as the

ratio of input received power to the output harvested power.

$$\textit{Power Harvesting Efficiency (PHE)} = \frac{P_o}{P_r} \tag{3.12}$$

where P_r is the power received at the antenna input terminals.

Under matched input conditions, the relation between PCE and PHE is,

$$PHE = 0.5 * PCE \tag{3.13}$$

In a conventional RF circuit, such as a low noise amplifier, the input matching is not dependent on the strength of the input signal. In a RF energy scavenging system, the resistive component of the rectifier, R_{rect}, reduces as the input signal level increases. The R_{rect} is a function of the diode on-resistance, which decreases with the increase in input current drive at higher power levels. Therefore, the input impedance, Z_{rect}, depends on the input signal level. However, in this work the problem is simplified by assuming *a constant input impedance*. This is a reasonable approximation at ultra-low input power levels closer to the power-up threshold of the harvester.

3.3. Single-Poly Floating-Gate Technique

The threshold voltage of the NMOS and the PMOS devices in the 180 *nm* process are 450 mV and 550 mV, respectively. In order to reduce the threshold voltage of these devices, several techniques can be used which require special processing in a standard CMOS process. The concept of achieving low threshold devices is derived from the EEPROM cells, where lower threshold voltages are required to

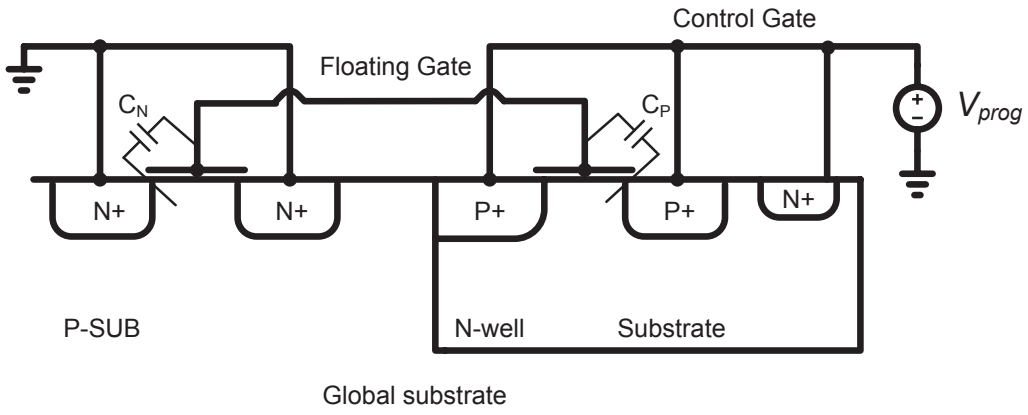


FIGURE 3.7: Single-poly floating-gate programming of a NMOS device.

have higher data retention over time. This is typically achieved by using special multi-polysilicon CMOS processes.

Earlier work on EEPROM by Ohsaki in [16] discusses the development of a single-poly pure CMOS *(SIPPOS)* cell, with options of high voltage electron tunneling on the polysilicon gates to reduce the threshold voltage of the MOS device. This tunneling process, referred to as Fowler-Nordheim tunneling, helps in injecting charge on the high-impedance gate oxide of the MOS device. The injected gate charge reduces the effective threshold voltage required to turn on the MOSFET device.

Figure 3.7 shows the structural arrangement of a typical NMOS SIPPOS cell. It consists of a NMOS and PMOS transistor with a common gate terminal, which is the *floating gate* of this SIPPOS cell. The *control gate* is a combination of the $p+$ diffusion and the inversion layer under the PMOS gate. Depending upon the gate capacitance ratio $\frac{C_P}{C_N}$, a high voltage pulse applied on this control node writes or erases charges on the floating gate of the cell.

3.3.1. Fowler Nordheim programming

The NMOS gate tunneling is achieved by programming the gate and the $n+$ diffusion. The $n+$ regions are grounded and the high voltage pulse V_{prog} is applied to the control gate. The gate capacitance ratio should be higher than 3.0 to induce tunneling [16]. A higher gate capacitance ratio gives more threshold voltage shift. The amplitude and duration of V_{prog} is critical to achieve tunneling. Typical amplitudes and durations vary between 9-15 volts and 100 ms, respectively.

The charge retentivity rate of the floating gate in a SIPPOS cell is lower when compared to the multi-polysilicon floating gate technique. A single-poly programmed cell holds the tunneled charge for 31 days [36], whereas the conventional multi-polysilicon floating gate technique retains the charge for ten years or more. The presence of both n-channel and p-channel devices to realize a floating gate MOS transistor makes the single-poly floating gate programming technique more area intensive.

Floating gate programming reduces the threshold voltage of the CMOS diodes used in the rectifiers. The threshold voltage reduction ensures lower power-up threshold requirements of the harvester and increases the overall conversion efficiency of the rectifier.

3.4. Analysis and Optimization of a N-Stage Rectifier

The top level system diagram in Figure 2.4, shows the input AC-DC rectification is successfully carried out by a N-stage rectifier. The number of rectifier stages affects the power conversion efficiency of the RF energy scavenging system. The

maximum achievable rectified output voltage also depends on the number of rectifier stages. Optimization techniques for the N-stage rectifier involve maximizing both the rectifier conversion efficiency and the rectifier output voltage.

3.4.1. Optimization for maximizing the rectified DC output voltage

Cascading a number of rectifier stages in series provides a higher output voltage, provided the scavenger system receives unconstrained levels of input power. The received RF signal power level is limited by the operational distance from the transmitter. To maximize the DC output voltage in a RF rectification block, the output power needs to be maximized. The analysis is given by (3.14) and (3.15).

If P_a is the power available at the rectifier input terminals and P_l is the power loss in a single stage of a N-Stage rectifier, then the output power of the rectifier P_{RECT} is given by:

$$P_{RECT} = P_a - N.P_l = \frac{V_{RECT}^2}{R_{oRECT}} \tag{3.14}$$

where V_{RECT} and R_{oRECT} are the output voltage and resistive load of the rectifier, respectively.

For a fixed resistive load at the output,

$$P_{RECT} \propto V_{RECT}^2 \tag{3.15}$$

From (3.14) it follows that reducing the number of rectifying stages (N), increases the rectifier output power (P_{RECT}). Hence, a single stage rectifier gives the maximum output power across a fixed resistive load. From (3.15) it can be concluded that the maximum output power produces the maximum output voltage in a RF rectification system. The upper bound on the rectified output voltage is set by

the rectifier configuration. The most commonly used rectifier structure is a voltage doubler configuration, where the output voltage is given by,

$$V_{out} = 2 * (V_{inputpk} - V_{th}) \tag{3.16}$$

where V_{th} is the threshold voltage of the rectifying diodes, and $V_{inputpk}$ is the peak voltage at the input of the rectifier.

3.4.2. Optimization for maximizing the conversion efficiency

The power conversion efficiency of the rectifier (PCE_{RECT}) is defined as the ratio of the rectifier output power (P_{RECT}) to the power available at the rectifier input terminals (P_a). Selecting the number of stages for achieving maximum rectifier power conversion efficiency is done by relating efficiency to the number of rectifier stages (N).

$$PCE_{RECT} = \frac{P_{RECT}}{P_a} = 1 - N.\frac{P_l}{P_a} \tag{3.17}$$

The expression for PCE_{RECT} shows that selecting a single stage rectifier helps achieving maximum power rectification efficiency.

The forward on-channel resistance (R_{on}) of the MOSFET diodes and the diode reverse leakage component (I_{rl}) are the primary sources of power loss in a full-wave rectifier. Hence, the smaller the number of active components used in the design the less is the power loss in the rectification system.

3.4.3. Optimization for maximizing the passive voltage amplification

Another reason for selecting a single stage rectifier is to maximize the sensitivity of the scavenger to low amplitude input received signals. As the number of rectifier stages increases, the effective capacitance C_{rect} increases and the effective

resistance R_{rect} decreases, as shown in the Figure 3.3. The maximum passive voltage amplification is related to the number of stages as given in (3.18) through (3.20).

$$Passive\ Voltage\ Gain = Q_{sr}\sqrt{\frac{R_{sr}}{R_s}} \tag{3.18}$$

$$= \frac{1}{\omega_0.C_{sr}.\sqrt{R}_{sr}.\sqrt{R}_s} \tag{3.19}$$

$$\approx \frac{\sqrt{R}_{rect}}{\sqrt{R}_s} \tag{3.20}$$

An increase in the number of stages decreases R_{rect}, thereby reducing the maximum achievable passive voltage amplification. The passive voltage gain is proportional to $\sqrt{R}_{rect}$ and is maximized by selecting the least number (N=1) of rectifier stages.

The quality factor of the matching network is determined by the ratio of the input impedance and the source impedance of the antenna. The quality factor for the single stage rectifier circuit is calculated to be around 30. The value closely matches with the maximum achievable quality factor for the 2.45 GHz band, which is given by the ratio of center frequency to the bandwidth occupied by the 2.45 GHz spectrum between 2.4 GHz and 2.5 GHz, $\frac{2.45\ GHz}{100\ MHz} = 24.5$. The component Q of the inductors and capacitors which realize the matching network is typically higher than 50. Passive components with self-resonant frequency above 3 GHz are chosen for the design. Thus the maximum achievable Q of the system for the single stage is not limited by the quality of the passive elements used in the matching.

The analysis and optimization of the N-stage rectification block in a RF energy scavenging system shows that to achieve a high rectified DC output voltage, maximum conversion efficiency, and increased harvester sensitivity, a single stage rectifier is desirable.

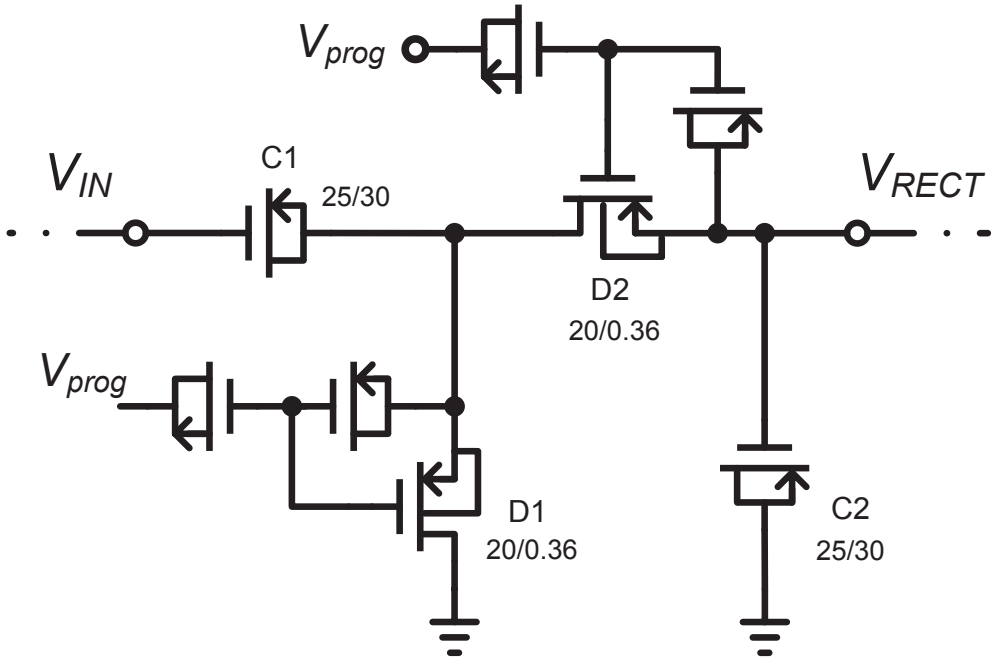


FIGURE 3.8: PMOS rectifier design in the 180 nm CMOS process.

3.4.4. Rectifier design

The design of a full-wave CMOS rectifier is implemented in a 180 nm process. The PMOS rectifier design with floating gate transistors is shown in Figure 3.8. The PMOS device is chosen for a MOS diode over a NMOS device because it reduces the number of body diodes connected to the high frequency nodes in the design. The junction capacitance of the body diodes provides a capacitive leakage component at higher frequencies. This loss component is less than 2% of the total power lost in rectification and is considered negligible.

The floating gate programming technique discussed in Section 3.5, helps in reducing the threshold voltage for the PMOS diodes in the rectifier to about 50 mV [36]. The lower threshold voltage devices have reduced turn-on voltages for

rectification and help increase the operating range of the RF energy harvester. Ultra-light load circuits which operate on a lower supply voltage ($\leq$ 500 mV) [37] can be operated by the RF energy harvester at the far-field (about 7 meters in free space).

Thick oxide devices with a higher gate voltage breakdown are chosen for the design. The minimum channel length of these devices is 360 nm. The device sizing of (20 μm/0.36 μm) is chosen for the MOS diode transistors ($D1, D2$) and (25 μm/30 μm) is chosen for the input (C1) and output (C2) PMOS capacitors. The devices are sized considering a fixed light-load current representing the far-field operation. The effective channel resistance, r_{ds}, of the MOS device is minimized, assuming a minimum dropout voltage across the diode transistors. The reduced channel resistance helps in maximizing the rectified output voltage (V_{RECT}) of the rectifier configuration.

4. DESIGN OF THE POWER MANAGEMENT UNIT

4.1. Introduction

The design of an efficient RF energy scavenging solution poses two different design challenges. The first step is to efficiently convert the incoming input RF signal into a DC voltage. The previous chapter described the optimization techniques required to achieve energy efficient rectification using a single-stage single-poly floating gate programmed full-wave PMOS rectifier.

The challenge in providing a stable supply voltage to the devices operating on the harvested DC power is discussed and solutions are presented in this chapter. A *power management circuit* which regulates the varying rectifier output voltage to a constant DC supply is necessary. Building an efficient power management unit is the key to achieving an efficient energy scavenging circuit.

4.2. Linear Regulator vs Switching Converter

There are two types of voltage regulation schemes to ensure a constant DC supply from a variable DC input voltage: linear regulation and switching regulation. The linear regulation scheme regulates voltage with a high supply noise sensitivity. The switching regulation scheme maintains the output voltage with high power efficiency.

4.2.1. Linear regulator

The simplest available DC-DC converter is a linear voltage regulator, which regulates any input voltage higher than the required output voltage to a targeted stable DC output voltage. The voltage difference between the input and the output, referred to as the *dropout voltage*, is dissipated as heat across a pass transistor in the output signal path as shown in Figure 4.1(a). This internal power loss makes the linear regulator the most inefficient power converter when used in a system where the required output voltage is significantly lower than the input voltage. The voltage gain of the linear regulator, VG_{LDO} is given by,

$$VG_{LDO} = \frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_{out} + V_{do}} \tag{4.1}$$
$$< 1 \Longrightarrow \textit{LDO always operates in step-down mode}$$

where V_{out}, V_{in} and V_{do} are the output, input and dropout voltages of the converter, respectively.

If I_{out} is the output load current and I_q is the internal circuitry loss, then the efficiency of the LDO is given as,

$$\textit{LDO Efficiency} : \eta_{LDO} = \frac{P_{out}}{P_{in}} = \frac{V_{out}.I_{out}}{V_{in}.(I_{out} + I_q)} \tag{4.2}$$

Assuming negligible losses in the regulator circuitry (I_q),

$$\eta_{LDO} \approx \frac{V_{out}}{V_{in}} \tag{4.3}$$

Equation (4.3) suggests that linear regulators are power efficient only when the output voltage is close to the input voltage. The efficiency of the LDO peaks

(a) (b)

FIGURE 4.1: Energy scavenger with the power management unit. (a) Linear LDO regulator. (b) Switching DC-DC regulator.

only when the dropout voltage is small. Earlier work done on energy harvesting using linear regulators in [36] suffers from low overall conversion efficiencies because of the larger difference between V_{in} and V_{out}.

4.2.2. Switching regulators - DC-DC converters

The second category of power converters are called *switching converters*. The output voltage is regulated by modulating the input received power levels, across varying loads. To maintain the high power efficiency at a fixed output voltage, the effective input impedance of the switching converter changes with respect to the incoming input power levels as shown in Figure 4.1(b). Another desirable feature with the switching converters is the input voltage to the converter can be higher or lower than the required output voltage. In other words, the switching regulators are capable of operating in the *step-up (boost)* or *step-down (buck)* modes. The voltage gain of the switching converter, VG_{DCDC} is given by,

$$VG_{DCDC} = \frac{V_{out}}{V_{in}} \tag{4.4}$$

$$< 1 : if\ V_{in} > V_{out} \Longrightarrow buck\ mode \tag{4.5}$$

$$> 1 : if\ V_{in} < V_{out} \Longrightarrow boost\ mode$$

If I_{mod} is the average frequency modulated input current from the rectified and stored output, then the efficiency of the switching converter is given as,

$$DC\text{-}DC\ Efficiency : \eta_{DCDC} = \frac{P_{out}}{P_{in}} \approx \frac{V_{out}.I_{out}}{V_{in}.I_{mod}} \tag{4.6}$$

When the system receives low input power, the rectifier output voltage is lower than the required output voltage. The boost mode of operation in the switching converter helps in pumping up this low rectified voltage to a higher output regulated voltage. During this mode the input charge is more frequently transferred to the output capacitor, thereby leading to a higher input current drive (I_{mod}) from the rectified and stored output. This increased I_{mod} leads to a higher conduction loss in the boost mode.

The high power efficiency and the boost mode operation in switching converters make it an ideal choice for power management units in energy harvesting solutions. The next section details the type of switching converter chosen for the RF energy scavenging circuitry.

4.3. Inductor Based vs Switched Capacitor Based Switching Converter

Switching converters can be widely categorized into inductive based and capacitive based converters. The inductive based converters regulate the output voltage

by low pass filtering a pulse width modulated input signal with a LC network. Controlling the charge transfer between the capacitors helps in regulating the output voltage in switched capacitor based converters.

4.3.1. Inductor based switching converters

The inductor based converter solution operates on the input voltage using a *Pulse Width Modulation (PWM)* technique to regulate the output voltage, is shown in Figure 4.2.

The voltage boosting operation of the inductive converter can be explained in two phases; the charging phase (ϕ_1) and the discharge phase (ϕ_2). During the charging phase, a DC input voltage causes the current through the inductor, L, to increase linearly with time. During the discharge phase the inductor current charges the output capacitor, C, until the steady state is reached. At steady state, the output voltage is given by $V_{OUT} = \frac{V_{IN}}{1-D}$, where D is the duty cycle of the PWM control signal.

The converter is capable of efficiently driving load currents in the range of a few hundred micro-amperes to amperes. The most common application is in high current LED flash drivers. The inductor size required to realize a highly efficient LC based converter at light loads is too large (typically in the range of 100 nH to 1 uH) to have an integrated on-chip solution.

4.3.2. Switched capacitor based switching converters

The switched capacitor based solution, operates on the principle of charge transfer between capacitors to build the required output voltage. The output is regulated using a *Pulse Frequency Modulation (PFM)* technique, which helps in maintaining the high efficiency over a wide range of input voltages. This converter

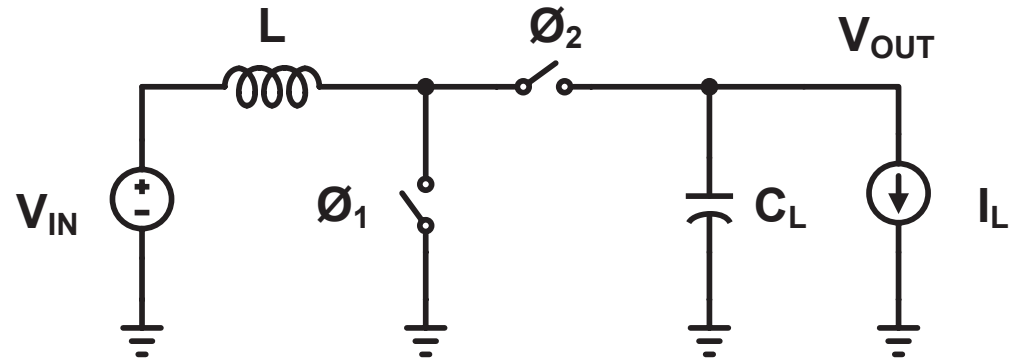


FIGURE 4.2: Inductor based switching converter.

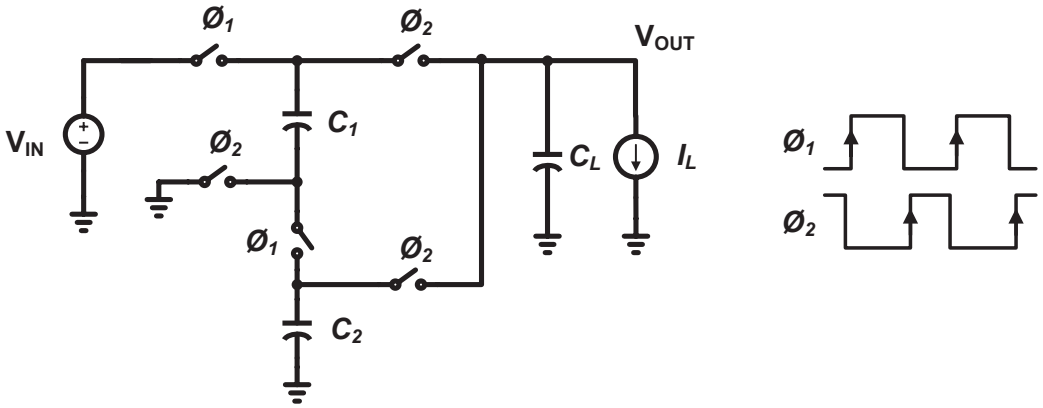


FIGURE 4.3: Schematic of a buck-mode switched capacitor converter.

is mainly used in applications requiring a lower load current which is within the range of tens of micro-amperes to a few hundred milli-amperes.

Typically, RF energy scavenging solutions, harvest power in micro-watts and a switched capacitor based switching converter is chosen for the micro-power harvesting. Another advantage of using a capacitor based solution is on-chip integration. Furthermore, electro-magnetic interference (EMI) issues are not as important as in inductor based solutions.

4.4. Analysis and Optimization of Switched Capacitor Buck-Boost Converter

The switched capacitor DC-DC converter provides an output voltage which can be lower or higher than the input rectified voltage depending on the selected conversion ratio setting. The input voltage conversion range can be extended by having many different conversion ratios depending on the number of capacitors and the number of switches available in the converter. Maksimovic's work in [31, 33] identifies the maximum conversion ratio feasible with a given number of capacitors in a converter topology.

4.4.1. Choosing the right SC based topology

Five different networks are considered for realizing a switched capacitor converter: Ladder, Dickson, Fibonacci, Doubler and the Series-Parallel network. Extensive analysis and comparison of these different topologies is done in [29]. An optimization technique using cost metrics involving optimal area and total capacitively stored energy is also presented. In this work, the series-parallel topology is chosen among the five networks, primarily due to the simpler structure for realizing various non-integer conversion ratios for DC-DC conversion. The series-parallel network has the best metric with the optimization constrained on the total available energy storage in the system. This metric suggests that the capacitors are more efficiently utilized in a series-parallel network than any other network-based converters.

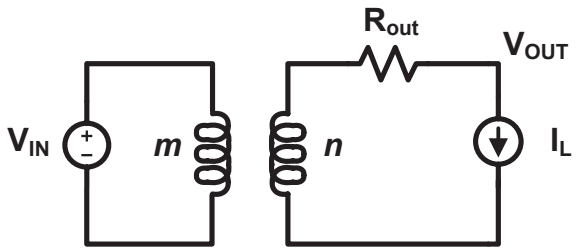


FIGURE 4.4: General model of a switching converter with losses modeled in R_{out}.

4.4.2. Losses in the switched capacitor DC-DC converter

The model of the converter with all the losses modeled as a resistive component in R_{out} is shown in Figure 4.4 [33]. An ideal transformer represents the voltage conversion gain, V_g, given by the turns ratio $\frac{n}{m}$. The different losses in switched capacitor DC-DC converters are discussed below.

4.4.2.1 Conduction loss

The switches in the switched capacitor converter are non-ideal with a finite on-resistance. The on-resistance leads to conduction losses in the switch network. The conduction loss (P_{cond}) is also dependent on the output load current (I_L) of the converter.

In an ideal dc-dc converter with zero switch on-resistance, the expected output voltage under loaded conditions is denoted as V_{ideal}. In the presence of non-ideal switches, the output voltage with loading becomes V_{OUT}. The difference between both the output voltage conditions is given by,

$$\delta V_{OUT} = V_{OUT} - V_{ideal} \tag{4.7}$$

In the interest of simplifying the conduction loss analysis, the resistive output impedance, R_{out}, is considered to account for the resistive conduction losses. Hence the conduction loss is given by,

$$P_{cond} = \delta V_{OUT}.I_L \tag{4.8}$$

where δV_{OUT} is the effective voltage drop across the resistance R_{out}. From the relation in (4.8), for a selected conversion gain, the conduction loss is the least when the loaded output voltage (V_{OUT}) is close to the corresponding ideal switch loaded output voltage (V_{ideal}).

4.4.2.2 Switching loss

The switches in the switching converter are controlled by the non-overlapping clock phases. The number of switches being switched simultaneously depends on the selected voltage gain configuration (V_g). The effective gate capacitance driven by the non-overlapping clocks from the gate driver circuit increases linearly with the number of active switches (N). Figure 4.5 shows a gate driver block driving an effective gate capacitance ($C_{g\_sw} = N.C_{gg}$) of the switches.

The switching losses or gate-driving losses in the converter are given by,

$$P_{swit} = N.C_{gg}.V_{RECT}^2.f_{sw} \tag{4.9}$$

where C_{gg} is the effective gate capacitance offered by a single switch, f_{sw} is the effective switching frequency of the circuit and V_{RECT} is the rectified DC output voltage, supplying power to the gate driver circuit.

The switching loss, P_{swit}, is linearly proportional to the effective frequency (f_{sw}) of the circuit. The number of active switches, N, depends on the gain con-

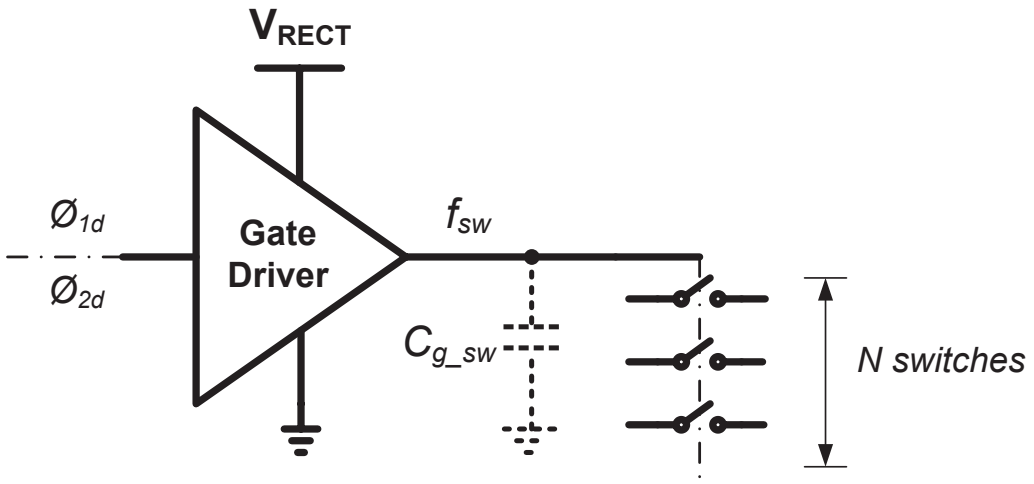


FIGURE 4.5: Gate driver block driving the gate capacitances.

figuration selected. The switching loss also increases quadratically as the output voltage of the rectifier (V_{RECT}) increases.

4.4.2.3 Bottom-plate capacitance loss

There are two types of capacitors in a SC based DC-DC converter: bypass or output capacitors, whose common mode voltage is at a fixed potential and flying capacitors whose common mode voltage with respect to ground is continuously changing during the non-overlapping clock phases. The bottom plate of the flying capacitors exhibit a loss component referred as bottom-plate losses, due to the varying voltages. In this work this loss is modeled and calculated as a part of conduction losses.

4.4.2.4 Loss in internal controller circuitry

One of the critical components causing an efficiency drop in the light-load switching converter circuit is the active power consumption of the internal circuit.

To achieve an efficient light-load converter, ultra-low power analog circuits are designed for the regulation scheme in the controller. The controller block comprises of a hysteretic comparator, a bandgap reference, an oscillator and a digital controller block, which need to reliably operate with nano-watts of power.

4.4.3. Efficiency analysis of light-load converters

Power efficiency is the most critical performance metric in a switching converter. The switched capacitor DC-DC converter suffers from a number of losses, the most dominant being the conduction loss and the switching loss. The active internal power consumption of the controller circuitry becomes important when considering the ultra light-load operation of the converter. In the efficiency analysis, light load condition is considered since the design of an efficient far-field RF energy scavenging system demands supplying low power loads, when operating at distances greater than 5 meters from the transmitting base station.

The efficiency of the converter, PCE_{DCDC}, is defined as the ratio of output power to the input power P_{in} supplied by the rectified and stored output. The effective output power of a DC-DC converter (P_O) is calculated as a function of the input power (P_{in}) and losses in the system. Hence the efficiency in terms of losses is given by,

$$PCE_{DCDC}\ (\eta_{dcdc}) = \frac{P_O}{P_{in}} = 1 - \left(\frac{P_{cond} + P_{swit} + P_{controller}}{P_{in}}\right) \tag{4.10}$$

where $P_{controller}$ is the power lost in the controller circuitry.

The efficiency of the converter can be increased by reducing the converter losses. The switching loss and the conduction loss are dependent on the sizing of switches in the switched capacitor matrix. The reduced switch sizing minimizes the

effective gate capacitance (C_{g_sw}) and thereby reduces the switching losses in the converter. The conduction losses can be minimized by increasing the sizing of the switches. The effective channel on-resistance (R_{on}) in the signal conduction path decreases and hence lowers the power dissipated across the switches.

The two conflicting requirements on the switch sizing drives the need for optimizing the effective sizes of the switches. The transfer capacitance, C_x, sizing and switching frequency (f_{sw}) also decide the achievable output voltage and efficiency of the converter. The controller loss is minimized by designing ultra-low power circuits. The loss is considered independent of the input rectified voltage (V_{RECT}) of the scavenger.

4.4.4. Calculating the output impedance of the converter

The effective power loss (P_{loss}) in a switching converter is modeled as a resistive output impedance R_{out} as shown in the Figure 4.4.

$$P_{loss} = I_L^2.R_{out} \tag{4.11}$$

To determine this output impedance, initially only the conduction loss due to non-ideal switches is considered for simplifying the analysis.

A relation between the output impedance R_{out} and the switch on-resistance R_{on} is derived below. The total power lost in the switches is equivalent to the sum of power lost in each switch during the active switch operation, P_{on}, is given by [29],

$$P_{loss} = \sum_{switches} P_{on}.D = D.\sum_{switches} R_{on}.I_i^2 \tag{4.12}$$

where D is the duty cycle of the clock phase operating the switches and is typically 50%, and I_i is the current flow through the switch during each period.

The current (I_i) can be expressed as a function of the effective charge transferred (q_i) during the on-state of the switch. This resulting expression for power loss is given by,

$$P_{loss} = D. \sum_{switches} R_{on}.\left(\frac{q_i.f_{sw}}{D}\right)^2 \tag{4.13}$$

$$= \frac{1}{D} \sum_{switches} R_{on}.(q_i.f_{sw})^2 \tag{4.14}$$

The power loss due to conduction increases quadratically with the charge transfer through each switch. The charge transfer increases proportionally with the output load current.

Equating (4.14) with (4.11), the output impedance R_{out} can be expressed as,

$$R_{out} = \frac{1}{D}\left(\frac{f_{sw}}{I_L}\right)^2 \sum_{switches} R_{on}.q_i^2 \tag{4.15}$$

The output impedance of the converter is proportional to the switch on-resistance. However, the switching losses increase with the increase in gate capacitance of the switches. To realize an efficient switching converter with lower losses the switch sizing needs to be optimized.

4.4.5. Optimization of switches and capacitor sizing

A comprehensive analysis of the switching converter is provided in [29] and two switching limits; Slow Switching Limit (SSL) and the Fast Switching Limit (FSL), are presented. The SSL and FSL help in finding optimal capacitor and switch values respectively.

The *slow switching limit* analysis introduced in [31], considers ideal switches and optimizes for the value of individual capacitors in the design. A constraint on total capacitance, C_t or equivalently, the total energy storage capability, helps

in realizing an expression for capacitance optimization [29]. It follows that each individual capacitor C_x in the series-parallel network is given by,

$$C_x = C_t * \textit{Fraction of charge across individual capacitor} \tag{4.16}$$

$$= C_t * \frac{q_{c_i}}{\sum_{switches} q_{c_i}} \tag{4.17}$$

where q_{c_i} is the charge flow related to the individual charge transfer capacitors.

The output impedance due to the SSL limit, R_{SSL}, decreases with increasing total capacitive storage [29]. In this design, the total capacitance value is constrained to $75\ pF$ for a maximum conversion gain of of 1/5. The individual equal valued capacitances in a serial-parallel switched capacitor network are given by, $C_x = \frac{75\ pF}{5} = 15\ pF$.

The *fast switching limit* analysis introduced in [32] considers non-ideal switches and optimizes the finite switch on-resistance. A relation between the conduction loss and switch on-resistance is expressed in Equation (4.13). The switch sizes are determined by budgeting the worst case power loss due to conduction at light load condition. To achieve a converter efficiency of 80% at light loads ($P_{out} \approx 9\ \mu W\ at\ 1.25V$), a conduction loss contribution of 60% in the overall power loss of the system is budgeted. The remaining 40% of the losses are assumed to be the internal circuitry active power consumption (30%) and switching losses (10%).

$$P_{cond} = 60\%.P_{loss} = 0.6 * (9\ \mu W * (\frac{1}{0.80} - 1)) = 1.35\ \mu W \tag{4.18}$$

Substituting $P_{cond} = 1.35\ \mu W$ in $P_{cond} = I_L^2.R_{out}$,

$$R_{out} = \frac{P_{cond}}{I_L^2} = 26.1\ k\Omega \tag{4.19}$$

The individual switch on resistances can be computed similar to the optimal capacitance value calculation in the SSL analysis. The effective switch conductance, G_t, expressed as a function of the conductance of a single switch $G_{on} = \frac{1}{R_{on}}$ is given by,

$$G_{on} = G_t * \textit{Fraction of charge across individual switches} \tag{4.20}$$

$$= G_t * \frac{q_{r_i}}{\sum_{switches} q_{r_i}} \tag{4.21}$$

where q_{r_i} is the charge flow related to individual switches.

The total conductance of the switches in the 5:1 $(m : n)$ converter is dervied in [29] and is given by,

$$G_t = \frac{2}{R_{out}}.\left(\sum_{switches} q_{r_i}\right)^2 \tag{4.22}$$

where the sum of charge flow related to switches is given by 4.(m-n).

$$G_t = \frac{2}{R_{out}}.[16.(m-n)^2] = 19.6\ mS \tag{4.23}$$

Substituting $G_t = 19.6\ mS$ in the expression for G_{on},

$$G_{on} = 19.6\ mS \frac{q_{r_i}}{\sum_{switches} q_{r_i}} \tag{4.24}$$

The fraction of charge transfered from each switch in a 5:1 converter is given by $\frac{1}{4.(m-n)}$.

$$G_{on} = \frac{19.6\ mS}{4.(m-n)} = 1.23\ mS \tag{4.25}$$

$$\implies R_{on} = 815.63\ \Omega \tag{4.26}$$

The switches in the switching converter are sized in order to achieve an on-resistance lower than the calculated value of 815.63 Ω.

4.4.6. Optimal frequency selection and output ripple specifications

The converter output voltage ripple is caused by the switching operation of the converter and the modulation of the PFM controller. The frequency of the ripple depends on the effective modulated frequency (f_{sw}) of the operating loop and the amplitude is determined by the supply voltage ripple specifications of the load, typically a wireless sensor node.

The maximum operating frequency ($f_{sw_{max}}$) of 3 MHz is selected by simulation, after optimizing for minimum switching losses (P_{swit}) over a wide range of switch sizing ($R_{on} \leq 815.63\ \Omega$). The switching frequency deviation, due to variation in the ring-oscillator generating the clock, can be tolerated by the feedback loop of the switching converter. The switching DC-DC converter regulates the output voltage with a +/- 5% variation over its nominal value. The loop modulates the effective switching frequency ($f_{sw} \leq f_{sw_{max}}$) while regulating the output voltage within a tolerable ripple range, thereby reducing the overall average power consumption.

4.5. Proposed RF Energy Scavenging System

The proposed system level architecture for the RF energy scavenging solution is shown in the Figure 4.6. As previously discussed, the system consists of an AC-DC rectification block which comprises of a one stage rectifier, and the power management unit which consists of a switching converter for achieving efficient power conversion at a fixed output voltage over varying range of loads.

The rectifier has a programming circuit which operates approximately once a month to engage the floating gate programming for the MOSFET diodes in the

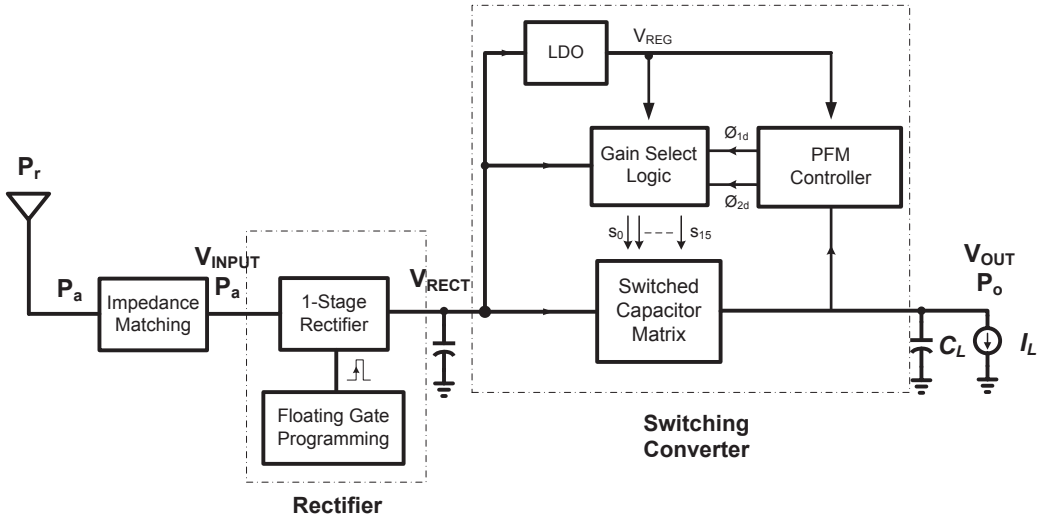


FIGURE 4.6: Architecture of the proposed RF energy scavenging system.

rectifier circuit. The switched capacitor converter consists of a switching matrix and a hysteretic mode PFM controller. The switched capacitor converter is chosen over an inductor based converter in order to realize a fully integrated on-chip solution. The PFM mode of output voltage regulation is typically used in switched capacitor switching converters. The digital controller consists of a gain select logic which selects the conversion ratio and the switching sequence in the switched capacitor series-parallel topology, depending upon the conversion gain selected.

The energy storage system after input voltage rectification and output voltage regulation, represented by C_L, can be a low leakage and high density super capacitor circuit [38] or it can be a rechargeable battery which gets trickle charged with the harvested power.

4.6. Circuit design of Switched Capacitor Buck-Boost Converter

The switched capacitor DC-DC converter operates on the rectified voltage, V_{RECT}, and regulates the output voltage, V_{OUT}, to 1.25 V. The converter consists of four blocks which perform the function of power management as given below.

1. A *switch matrix network* which forms the core of the converter. Different conversion gains are realized by rearranging the switches and capacitors of the matrix.

2. A *hysteretic PFM mode controller* modulates the converter switching frequency to achieve output voltage regulation. The output voltage (V_{OUT}) is regulated by a hysteretic comparison operation in a feedback loop around the switching matrix.

3. A *gain select logic* which selects the states of the switches in the switch matrix depending upon the input voltage (V_{RECT}) to the system.

4. A *linear voltage regulator* which provides the constant DC output voltage V_{reg} for supplying the sub-blocks in the controller, and the gain select logic. This circuit provides the start-up interface for the controller.

The switched capacitor converter is designed to operate in two voltage conversion modes: buck and boost. In the buck mode, the input voltage is higher than the output voltage and vice-versa for the boost mode of operation. The circuit operation of the converter can be explained by considering the operation in boost mode.

The rectified input voltage to the converter ($V_{RECT} < 1.25\ V$) is converted to a digital output by the analog to digital converter in the gain select logic. The digital output is phase encoded to select the switches in the switch matrix during different phases of the clock. The switches configure a gain setting greater than one for boosting operation ($VG_{DCDC} > 1$). The output voltage of the linear regulator (LDO) is V_{RECT} during boost mode and supplies the blocks in the PFM controller. The oscillator in the controller generates the non-overlapping clocks, ϕ_1 and ϕ_2, which control the output of the gain select logic.

The input voltage and the clocks help build up the charge across the output load capacitor, C_L, to $V_{RECT} * VG_{DCDC}$. If the output voltage exceeds 1.25 V the comparator compares the output with the bandgap references in the controller and modulates the clocks (ϕ_1 and ϕ_2) to (ϕ_{1d} and ϕ_{2d}). The modulated switching frequency is less than or equal to the oscillator output frequency. This frequency effectively changes the rate of charge transfer to the output load capacitor and ensures voltage regulation is achieved.

4.7. Hysteretic Mode Controller

The hysteretic mode controller is shown in Figure 4.7. The controller block forms the control loop around the switch matrix core as shown in Figure 4.6. The loop ensures that the steady state output voltage after conversion is fixed at a constant DC value.

The hysteretic comparator in the controller compares the output voltage with the two different bandgap reference voltages. Depending on the output of the comparator (V_{OUT}), the two-phase (ϕ_1 and ϕ_2) non-overlapping clock signals are turned

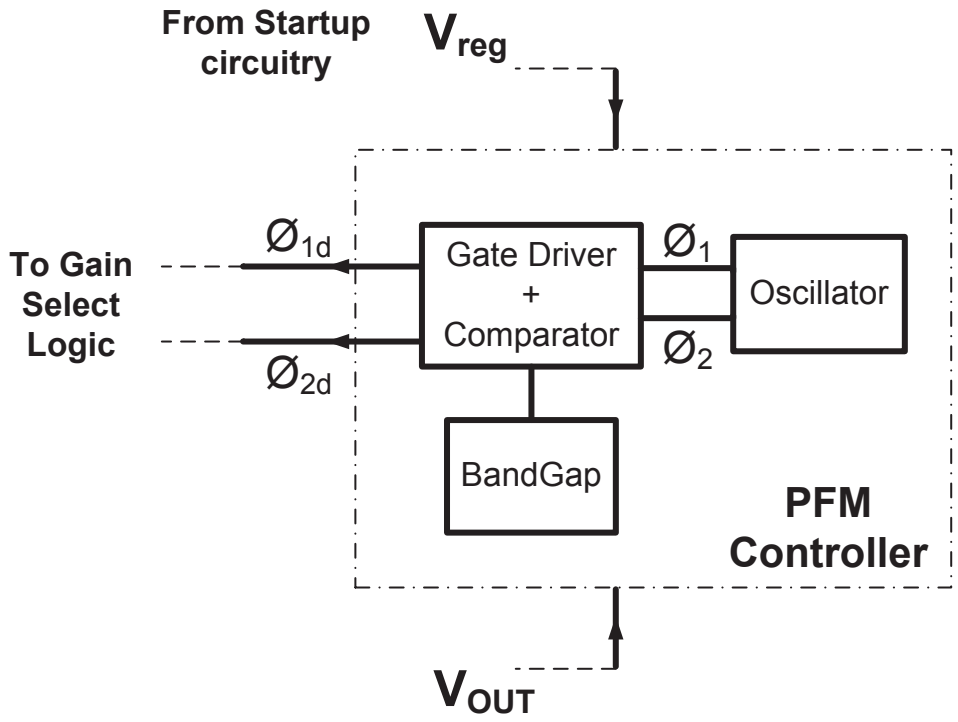
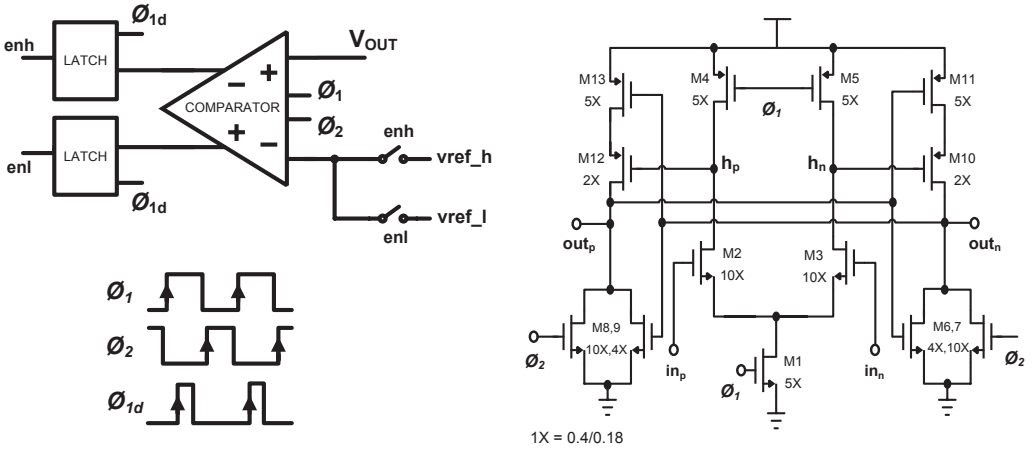


FIGURE 4.7: Hysteretic PFM mode controller block diagram.

on or off. The state of the switches in the switched capacitor matrix is decided by a gain select logic. This modulated two-phase (ϕ_{1d} and ϕ_{2d}) clock signal operates the switch matrix to ensure the output voltage is maintained within the hysteretic comparator voltage window. The width of the window is set by the supply voltage ripple specifications of the converter load. The oscillator circuit in the controller generates the clock signals for the switching converter.

The hysteretic mode of controlling the effective clock frequency (f_{sw}) and regulating the output is also referred to as the pulse frequency modulation (PFM) mode of the switching converter.



(a) (b)

FIGURE 4.8: Hysteretic comparator design. (a) Schematic of the hysteretic comparator. (b) Dynamic comparator circuit.

4.7.1. Hysteretic comparator

The hysteretic comparator performs the output voltage comparison with two different reference voltages ($vref_h$ and $vref_l$) in the controller. The design specification of the comparator is driven by the low power requirements of the converter. A high-speed, dynamic two-stage comparator shown in Figure 4.8(b) is chosen [39]. The design is based on the principle of an initial pre-charge phase in the first stage followed by a regeneration phase in the second stage.

Figure 4.8(a) shows two switches, enh and enl, controlled by the complementary outputs of the comparator. The reference voltage for comparison is selected by the output of the previous comparison cycle.

In the pre-charge phase, the intermediate nodes h_p and h_n of the dynamic comparator, are charged to a common mode voltage of the circuit, depending upon

the input voltages available at in_p and in_n, respectively. The regeneration phase sets in to regenerate the output nodes out_p and out_n of the comparator to either supply rails.

4.7.2. Bandgap reference

The low-power bandgap reference shown in Figure 4.9 is the complementary version of the weak inversion bandgap circuit by Tzanateas et. al. [40]. The circuit consists of five transistors operating in weak inversion. The transistors M1-M4 form a self-biased current mirror loop which is stabilized by setting the voltage V_{R3} across the resistance R3. The equation describing the relation of sizing (W/L) of transistors to the PTAT voltage V_{R3} is, [40]

$$V_{R3} = \frac{kT}{q}.\ln\left(\frac{(\frac{W}{L})_2}{(\frac{W}{L})_1}.\frac{(\frac{W}{L})_3}{(\frac{W}{L})_4}\right) \tag{4.27}$$

This voltage has a positive temperature coefficient $PTAT$ and is compensated by a negative temperature coefficient base-emitter voltage V_{BE} generated across a BJT device (B1). The temperature compensated reference is given by,

$$vref_h = \frac{(\frac{W}{L})_7}{(\frac{W}{L})_4}.\frac{V_{R3}}{R3}.(R1 + R2) + V_{BEB1} \tag{4.28}$$

The simulated temperature coefficient of the reference voltage across -40°C to 120°C is 300 $\frac{ppm}{°C}$ and the input power supply rejection (PSR) is 12 dB. The resistance R3 is sufficiently large to ensure a weak-inversion mode of operation. The overall power consumption of the circuit is about 165 nW.

A startup circuit is designed to ensure the circuit does not enter into the zero-current steady state from which it can never recover.

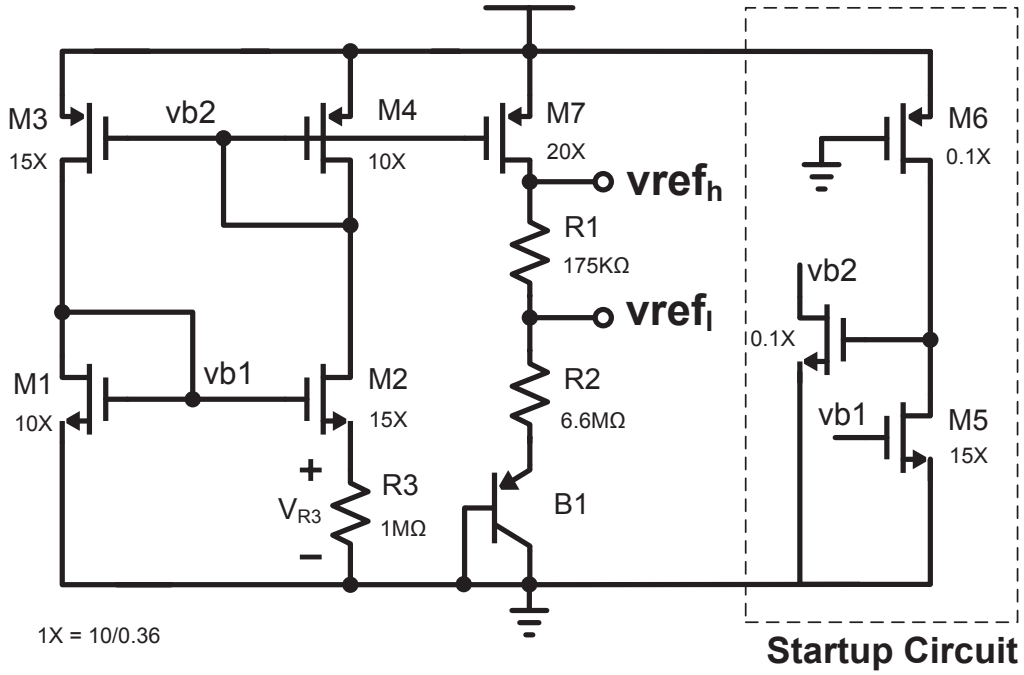


FIGURE 4.9: Bandgap reference with a start-up circuit.

4.7.3. Gate driving and clock generation circuit

The switches in the switched capacitor matrix core are driven by a gate driving circuitry. Figure 4.10 shows the gate driving circuit in the controller. The PFM controller controls the effective switching frequency. The hysteretic comparator output decides the state of the switches in the switched capacitor matrix. The switches in on-state are operated with one of the two non-overlapping clock phases. To avoid any losses due to short circuit current, a sufficiently large non-overlapping phase is ensured.

The dynamic clock level shifter in the gate driver consumes 300 nW (switching loss, P_{swit}) during the active level shifting operation. The non-overlapping clock signals and other timing signals for the converter are generated by a ring oscillator

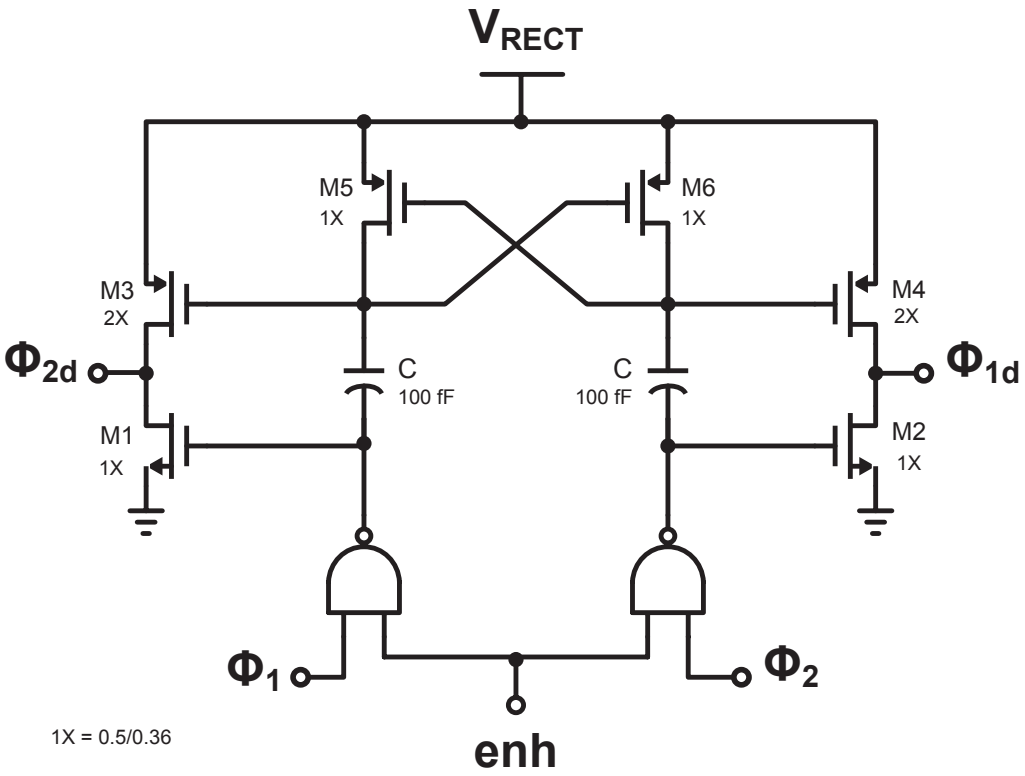


FIGURE 4.10: Gate driver circuitry in the PFM controller.

and logic circuits dissipating about 200 nW of power on a 0.85 V scaled regulated supply, V_{reg}.

4.8. Gain Select Logic and Digital Encoder

The switched capacitor DC-DC converter designed for energy harvesting applications requires conversion gain settings to boost or buck the input voltage to a fixed output voltage. In this converter design, eight different conversion gains are realized by restructuring the switched capacitor matrix shown in Figure 4.11 during

both the non-overlapping phases. The switch matrix structure has five capacitors and sixteen switches to realize the eight different conversion gain factors.

The selection of the optimal conversion gain for a selected input voltage range is done by a 3-bit analog to digital converter. The block diagram of the gain select logic with digital control is shown in Figure 4.12.

4.8.1. 3-bit Successive approximation ADC

A successive approximation logic based analog to digital converter is designed for selecting the conversion gains. The specifications of the converter are determined by the environment where the wireless sensor node is deployed. A sensor node in an application where the input received power level is continuously varying requires a high speed ADC. The ADC ensures faster gain selection to regulate the continuously changing rectifier output. However, in an application where the sensor node and the transmitting hub are stationary, the input power to the scavenger remains constant, a low speed ADC can be used for gain selection. The ADC can be put into sleep mode after conversion, reducing the quiescent power consumption of the harvester. In this work a low power, low speed SAR ADC is designed for a stationary sensor node application.

The SAR ADC circuit with a resistive DAC and an auto-zeroing comparator [41] is shown in Figure 4.13. The comparator is based on an inverter topology as in Figure 4.13b and operated in sub-threshold region for low power consumption. The reference voltage for comparison is generated from the resistive string operating on the V_{reg} power supply. The overall simulated power consumption of the logic and the comparator for a 3-bit conversion is 1.2 μW. The rate of conversion of the data converter is 360 kbps. The SAR logic is put into sleep mode using a $RESET$ signal,

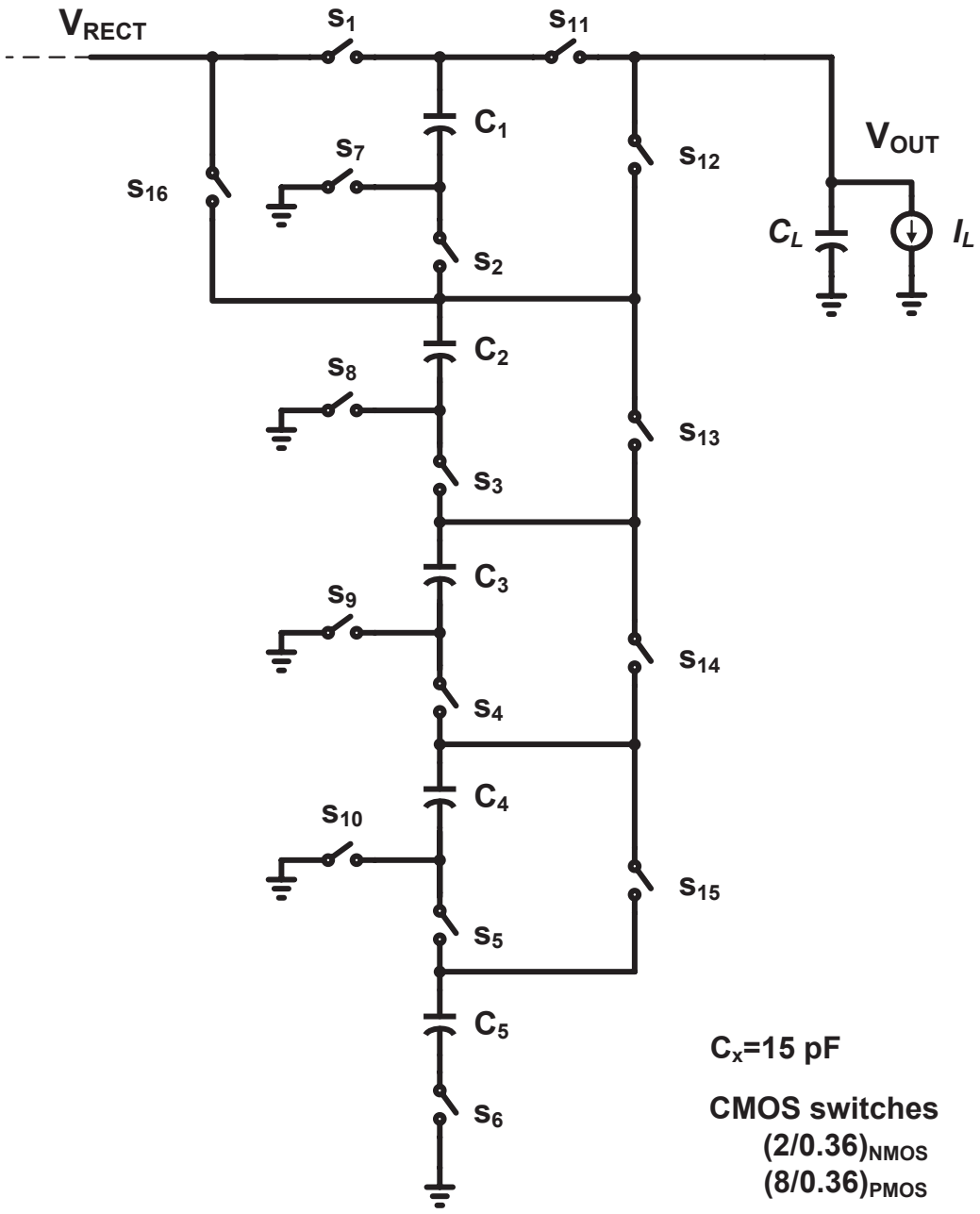


FIGURE 4.11: Switch matrix design with 5 capacitors and 16 CMOS switches.

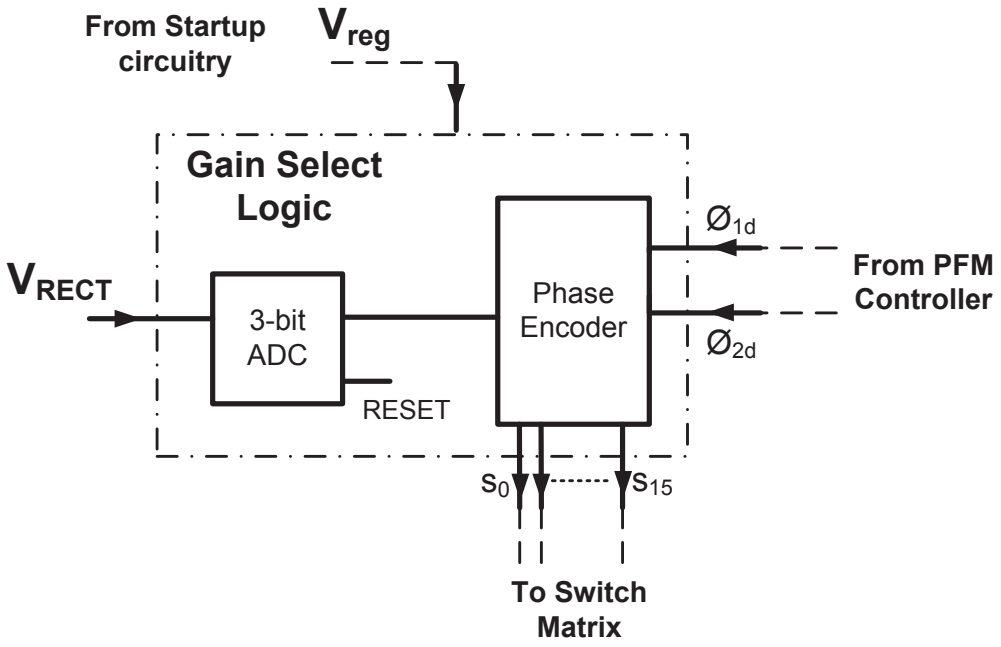


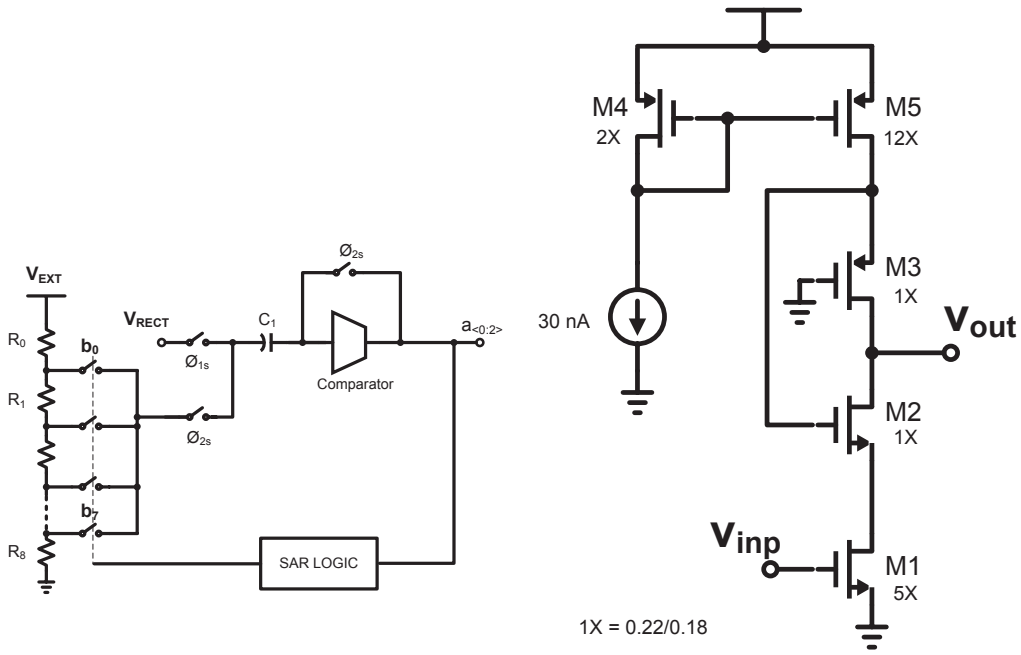
FIGURE 4.12: Block diagram of gain select logic and digital controller.

after the conversion is done.

4.8.2. Digital phase encoder

As the SAR ADC selects a particular gain setting for the conversion, the switches in the switched capacitor matrix need to be reconfigured and controlled by the two non-overlapping clock phases. A digital encoder is designed to control the selection of these phases.

Level shifters are designed to level shift the clock signals and DC signals controlling the switches. The circuit which performs this hybrid level shifting is shown in Figure 4.14 and consumes a dynamic power in the range of 150 nW on the V_{RECT} supply.



(a) (b)

FIGURE 4.13: Successive approximation analog to digital converter. (a) SAR ADC block diagram. (b) Inverter based comparator

4.9. Start-up circuit

The energy harvesting system has only one input for interfacing with the RF input signal around 2.4 GHz. The energy storage element, C_L, in the scavenger is charged to the output voltage (V_{OUT}) by the switching action of the converter. The switching converter requires non-overlapping clock signals to start building the output voltage from a rectified dc voltage at its input.

The operation of the scavenger at very low input voltages is constrained by the ring oscillator of the switching converter. The oscillator cannot build oscillations with a rectified DC output voltage less than 400 mV. The oscillator generates clock signals on rectified output supply beyond 400 mV. The switching converter builds and regulates the output voltage of the converter to 1.25 V with a boost mode conversion gain 1:4 on the 400 mV input (4X of 400 mV).

When the rectified output reaches 1.30 V or higher, the ring oscillator oscillation frequency is not optimal for the minimizing the converter losses. Hence, the supply for the converter circuitry, including the PFM controller and gain select logic, needs to be internally regulated. A low drop out (LDO) linear regulator in sub-threshold mode of operation ensures a regulated supply for the converter. The block diagram of the startup LDO circuitry is shown in Figure 4.15.

The LDO regulator is loaded by the converter circuitry consuming active power of less than 1.2 μW. Hence, the effective power lost across the pass transistor is sufficiently low so as to not affect the efficiency of the scavenger.

By providing the startup circuitry, with an ultra-low power sub-threshold LDO regulator compensated by an off-chip load capacitor (C_s), the scavenger can be operated as an autonomous self-powered system, requiring no external signal for its

TABLE 4.1: Power consumption of the low power switching converter circuit.

SC DC-DC internal circuitry	Power (μW)
Comparator	0.225
Gate Driver (Switching Loss)	0.300
Bandgap	0.165
Oscillator + Logic	0.200
Gain Select	0.150
Startup circuit	0.175
Total power consumption	1.215 μW

operation.

4.10. Simulated Efficiency of the DC-DC Converter

As discussed previously, a highly efficient switching converter is critical for realizing a high conversion efficiency in the harvester. The power efficiency of the converter, η_{dcdc}, is a function of the losses in the gate driving circuitry and the conduction losses. The quiescent power consumption of the switching converter is around 1.2 μW as shown from the power breakdown in Table 4.1.

The energy harvester operates under two widely categorized load conditions; *light loads* and *heavy loads*. The efficiency of the switching converter at the light load condition is maximized for achieving efficient far-field energy scavengers.

Under light load, the efficiency of the converter is influenced by both the

switching and conduction losses in the circuitry. The switching losses become comparable to the conduction losses. The switching loss and conduction loss across a wide input voltage range is shown in Figure 4.16 for a light load of 8.3 μW or 7 μA. (1.25 V across a resistive load of 180 kΩ).

The overall power efficiency of the switching converter at the light load of 8.3 μW, across a wide input voltage range is shown in Figure 4.17. The efficiency exhibits a discontinuous curve, the reason for which is attributed to the finite number of gain combinations available over the input range. The output voltage over the range is regulated at 1.25 V as shown Figure 4.18.

To explain the discontinuous nature of the efficiency curve, the input voltage range between 1.9 V and 2.5 V is considered. The output is regulated to 1.25 V (V_{NS}) with a voltage conversion gain of 2/3. The converter efficiency is highest at 82%, when the input is 1.9 V and the conduction losses are minimal ($\delta V_{OUT_{1.9}} = 1.9.\left(\frac{2}{3}\right) - V_{NS} = 67\ mV$). The efficiency gradually decreases to 65% when the input is 2.5 V, due to increased conduction losses ($\delta V_{OUT_{2.5}} = 2.5.\left(\frac{2}{3}\right) - V_{NS} = 416.67\ mV$) as shown in Figure 4.16.

The conversion gain of 1/2 is selected for an input voltage between 2.55 V and 3.2 V. The efficiency curve displays a linear nature between this voltage range, thereby showing the discontinuous nature of the curve.

The higher the difference between the actual output voltage and the ideal converter output voltage ($\delta V_{OUT_{2.3}} > \delta V_{OUT_{1.9}}$), the higher the conduction losses and the lower the maximum achievable efficiency η_{dcdc} of the converter.

4.11. Performance Summary of the Light-Load Switching Converter

The design approach and circuit design of various building blocks of the switched capacitor DC-DC converter for the RF energy scavenging application is presented. The simulated overall power efficiency of the converter at ultra-light loads is around 80% over a wide range of input voltage and output powers. The converter is 5% more efficient when compared to the most recent work in [25] on light-load switched capacitor converters.

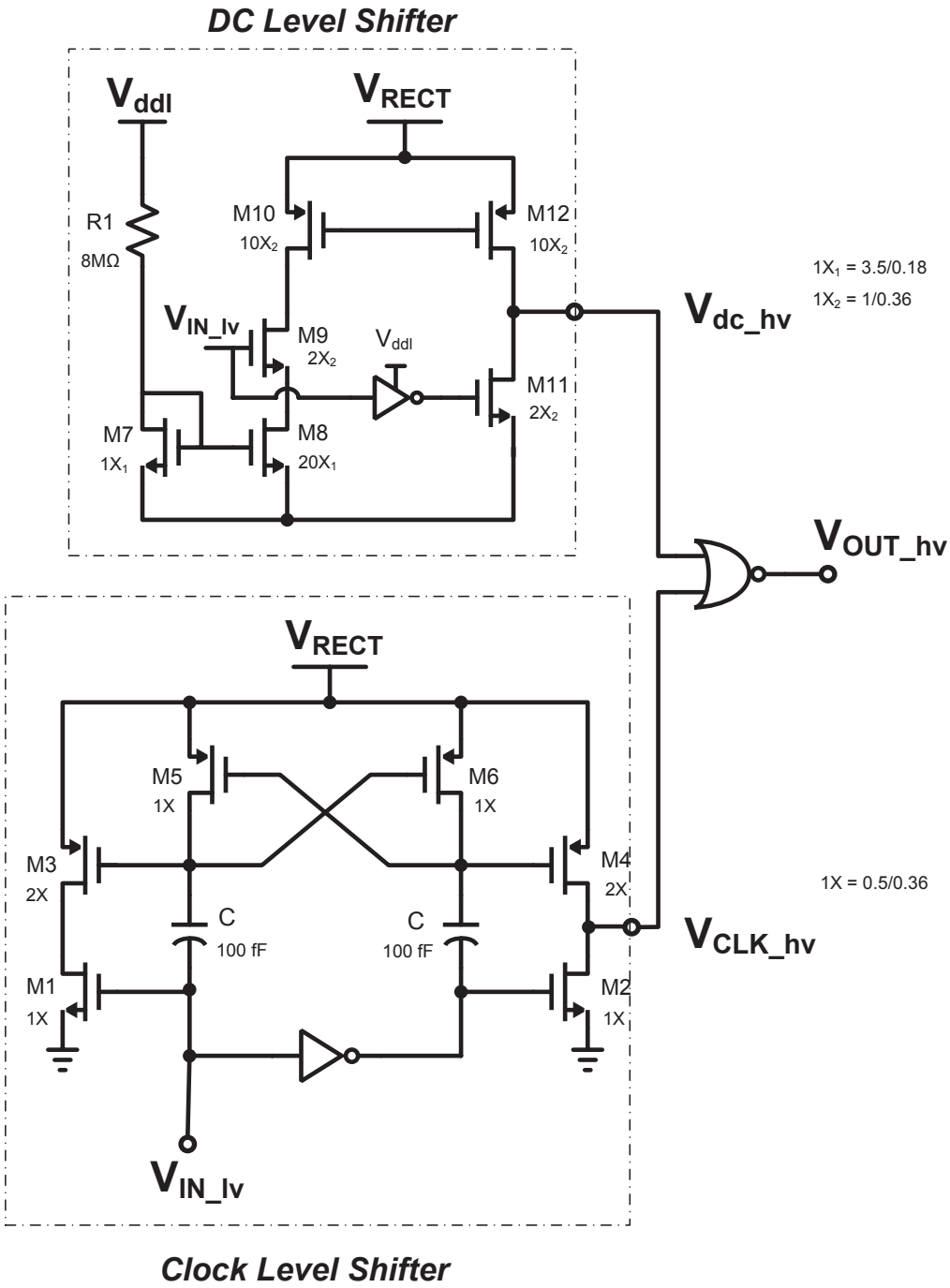


FIGURE 4.14: Hybrid level shifter for clock and DC level shifting.

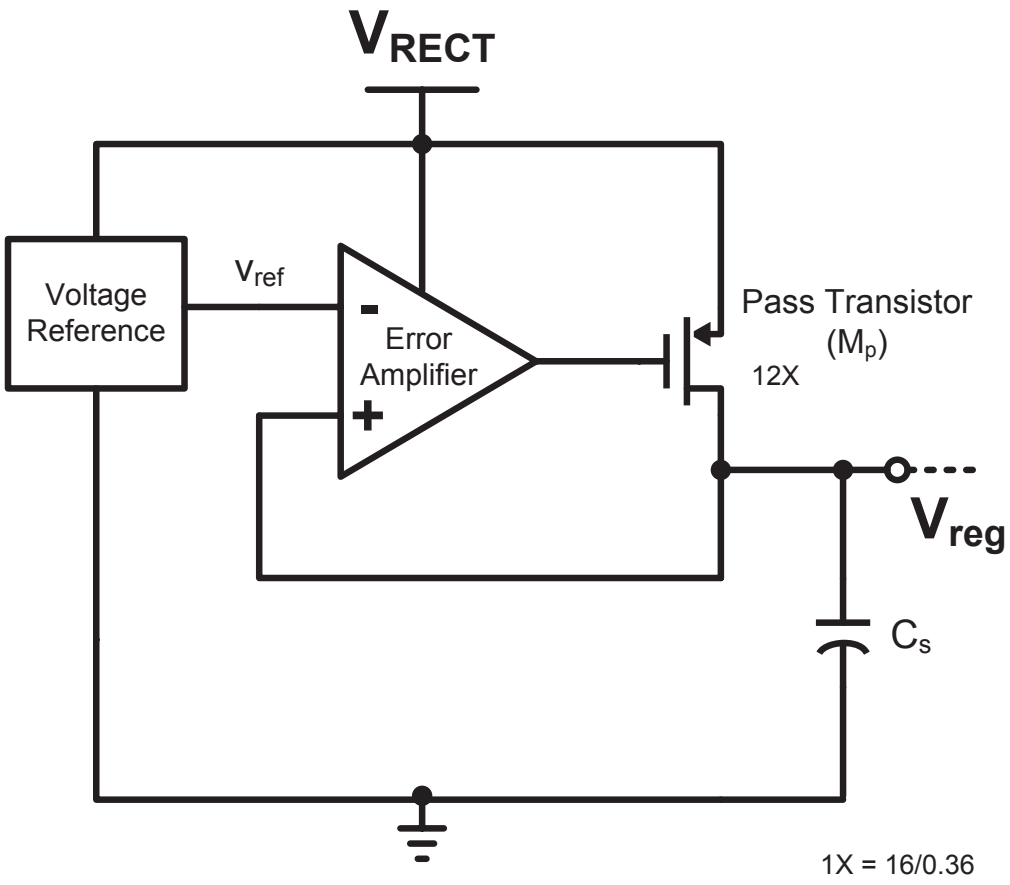


FIGURE 4.15: Linear LDO regulator as a startup circuit.

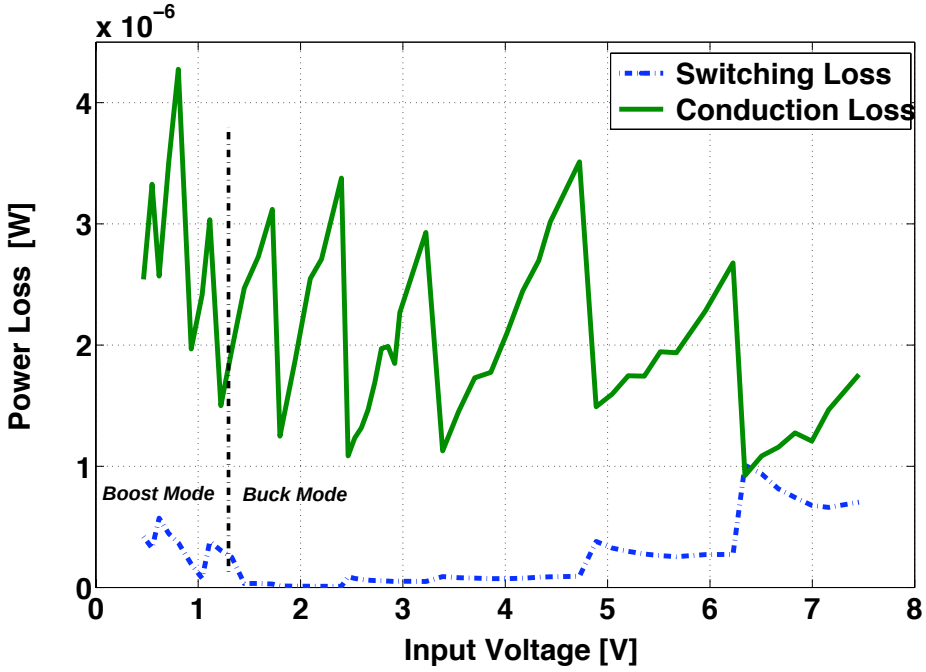


FIGURE 4.16: Losses in the switching converter under light loads.

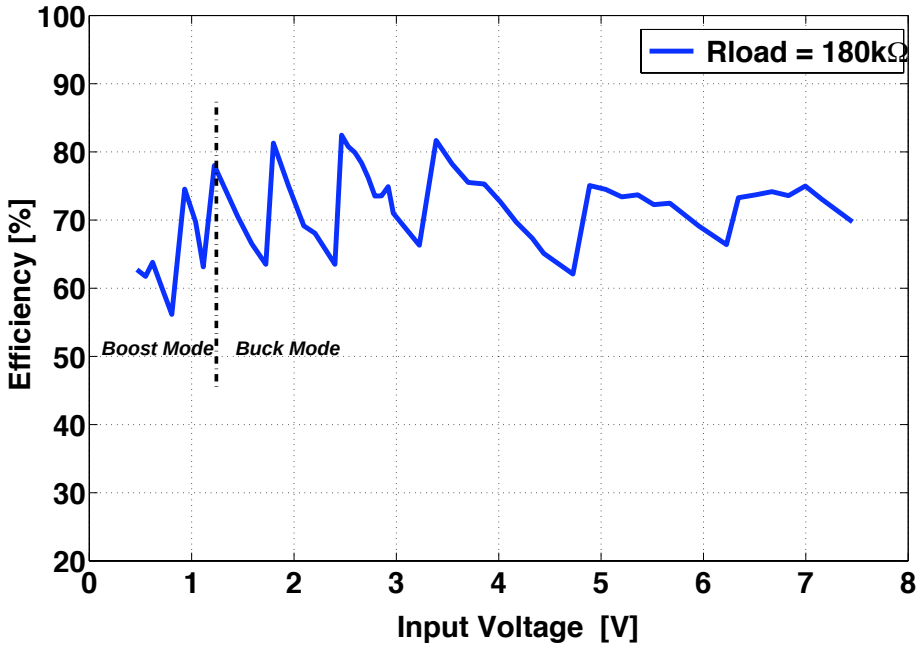


FIGURE 4.17: Power efficiency of the switching converter under light loads.

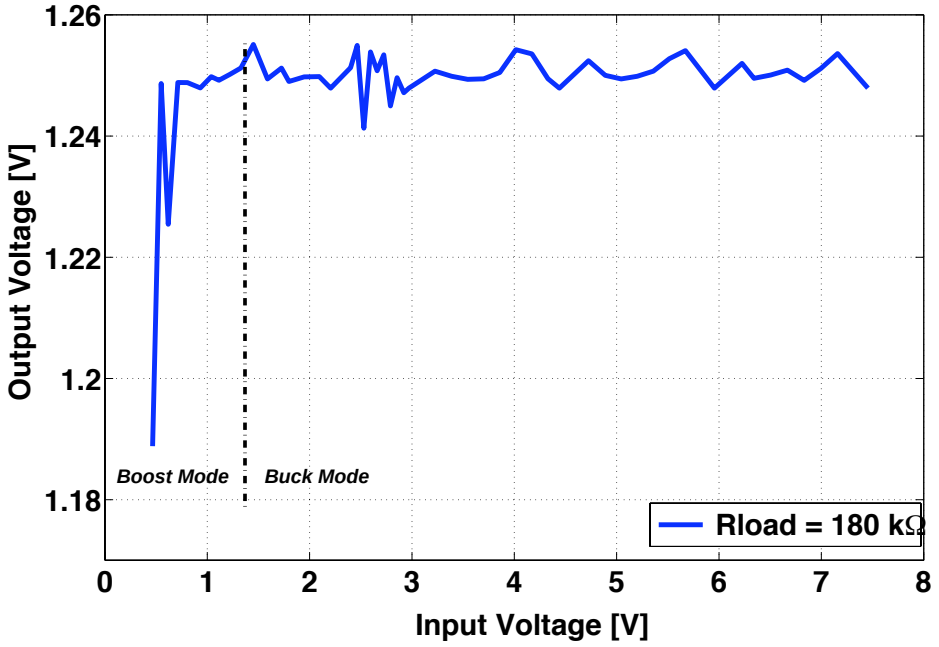


FIGURE 4.18: Output voltage of the switching converter under light loads.

5. SIMULATED RESULTS OF THE RF ENERGY SCAVENGER

5.1. Introduction

A RF energy scavenging solution with a reduced threshold RF rectifier front-end and a switched capacitor DC-DC converter back-end is designed in a 180 nm CMOS process. The single-stage floating-gate rectifier efficiently converts the input RF signal to DC voltage and the converter efficiently drives light loads. The die size estimate projects a chip area of 0.8 mm^2, with the five switching capacitors of 15 pF each occupying 0.55 mm^2. The complete solution is realizable on-chip and an external storage medium provides the energy storage. The simulated performance of the RF energy scavenging solution is presented.

5.2. Power Conversion Efficiency of Energy Scavenger

The system level implementation of the energy scavenging solution is shown in Figure 5.1.

The RF energy scavenger is a cascaded system of rectifier and switching converter. The scavenger power conversion efficiency, PCE, as a function of the efficiency of the rectifier and efficiency of the switching converter is given by,

$$PCE_{scavenger} = PCE_{RECT} * PCE_{DC-DC} = \eta_{rect} * \eta_{dcdc} \tag{5.1}$$

The overall system efficiency can be maximized by maximizing the efficiencies of the rectifier and switching converter.

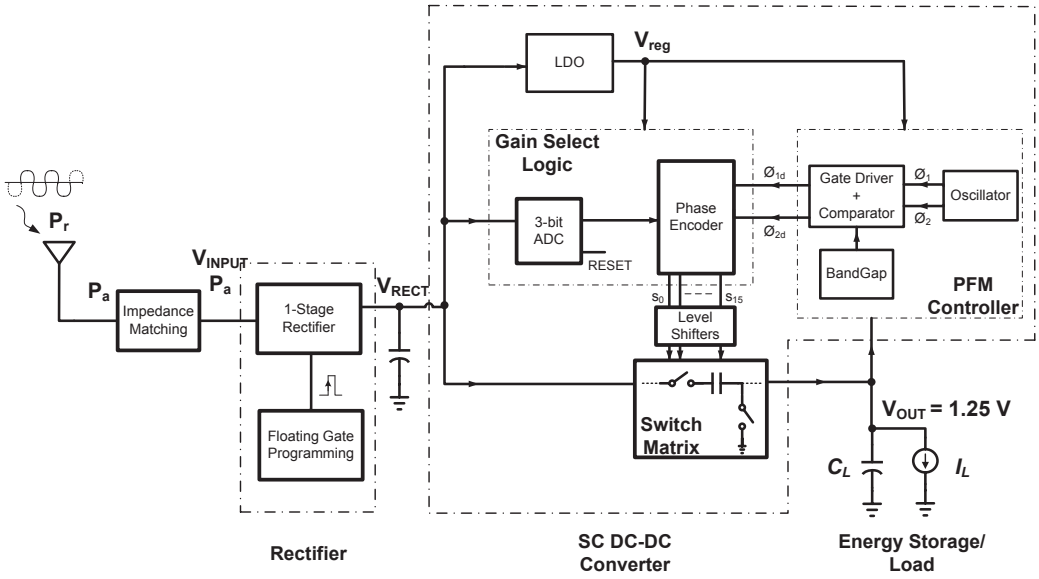


FIGURE 5.1: System level diagram including the SC DC-DC converter with the switch matrix, PFM controller, gain select logic, startup interface.

The conversion efficiency of the scavenger system plotted against input received power (P_r) is shown in Figure 5.2. The output load is kept constant at P_O = 8.7 μ W (1.25 V across 180 kΩ). The rectifier efficiency (η_{rect}) and the switching converter efficiency (η_{dcdc}) are superimposed on the same plot. Figure 5.3 shows the corresponding output voltage over the received power across a 180 kΩ load. The output is regulated around 1.25 V over a wide range of input received power.

The near-field performance of the scavenger, with a fixed load, is limited by the operation of the front-end RF rectifier. The scavenger conversion efficiency curve, $PCE_{scavenger}$, tracks the rectifier efficiency, η_{rect}, and the latter starts to roll off as the input power increases beyond -10 dBm. At higher input received power levels, the rectifier output voltage starts saturating as it reaches the breakdown voltage limits of the MOS diode transistors. The excess received input power is dissipated

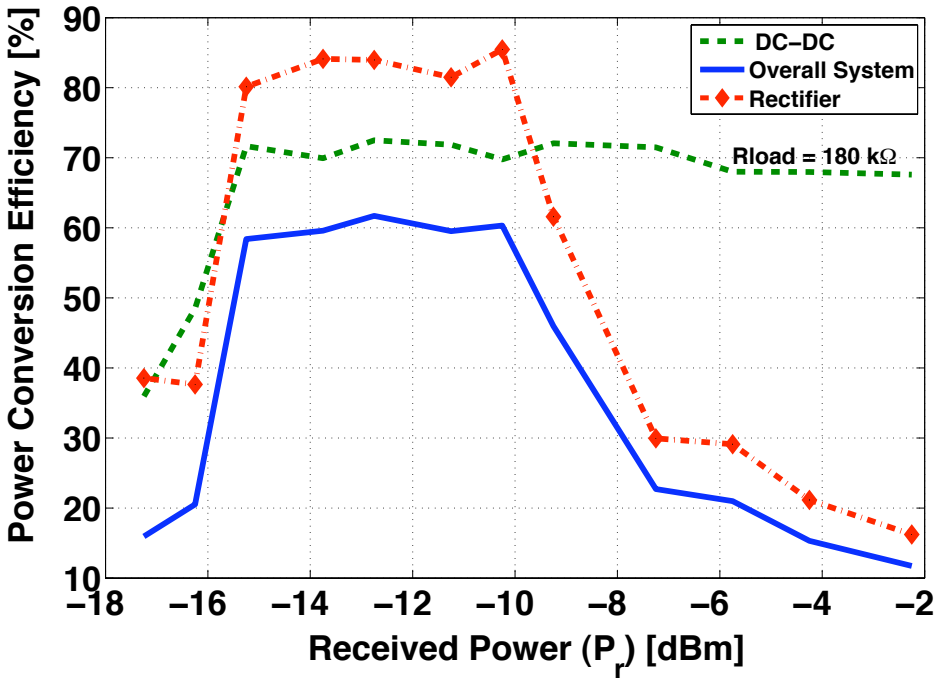


FIGURE 5.2: Conversion efficiency of the scavenger with 8.7 μW load at 1.25 V.

as loss in the rectifier. The switching converter changes its input impedance to maintain a higher power efficiency at 72%. The effective impedance offered by the switching converter on the rectifier output increases, allowing for a higher rectified output voltage.

The efficiency of harvester reaches about 60% at a received input power of -15.5 dBm. The plot follows a bell shaped curve with greater than 60% efficiency over a 5.5 dBm input power range (-15.5 dBm to -10 dBm) for a 180 kΩ load. The computation of power conversion efficiency of the scavenger from the simulated plots is shown in (5.2) and (5.3). Consider the power conversion efficiency at -15.5 dBm,

$$PCE_{scavenger} = \eta_{rect} * \eta_{dcdc} = 72\% * 85\% = 61.2\% \tag{5.2}$$

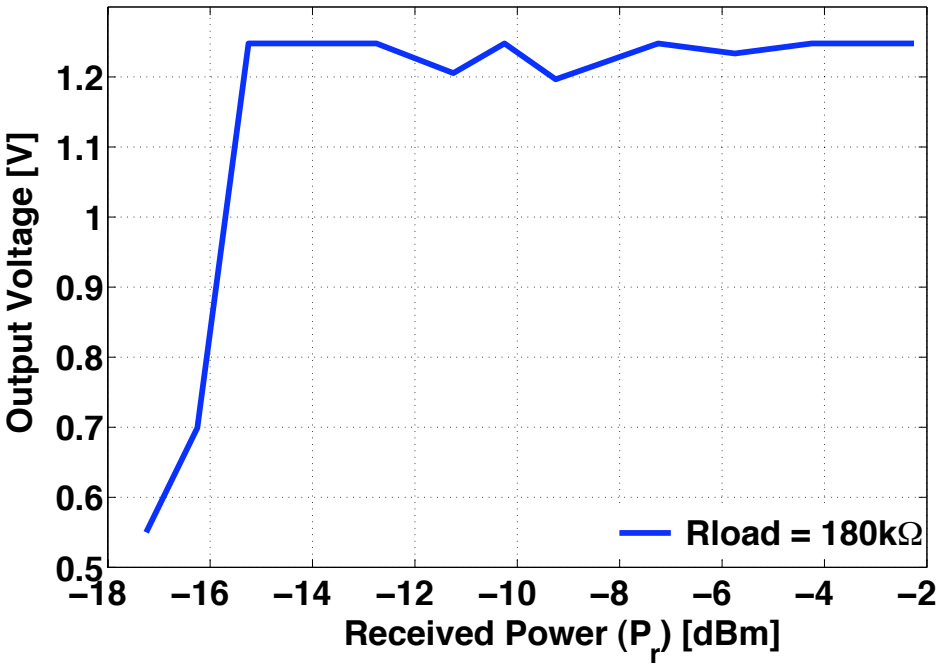


FIGURE 5.3: Output voltage of the scavenger with 8.7 μW load at 1.25 V.

Assuming ideal input matching, at received power (P_r) levels of -15.5 dBm or 28.2 μW, the available input power, P_a reaching the rectifier input terminals is -18.5 dBm or 14.1 μW.

$$PCE_{scavenger} = \frac{P_O}{P_a} = \frac{8.68\ \mu W}{14.1\ \mu W} = 61.5\% \tag{5.3}$$

Figure 5.4 shows a plot of the peak power conversion efficiency of the scavenger for various loads. The power conversion efficiency drops at higher input power levels around -6 dBm. This efficiency drop is due to the decrease in output voltage level at higher load current.

The plot in Figure 5.5 compares the current work with the most recent work on RF energy scavenging and power management in [36]. The conversion efficiency performance of the harvester architecture shown in this work is 10% better than

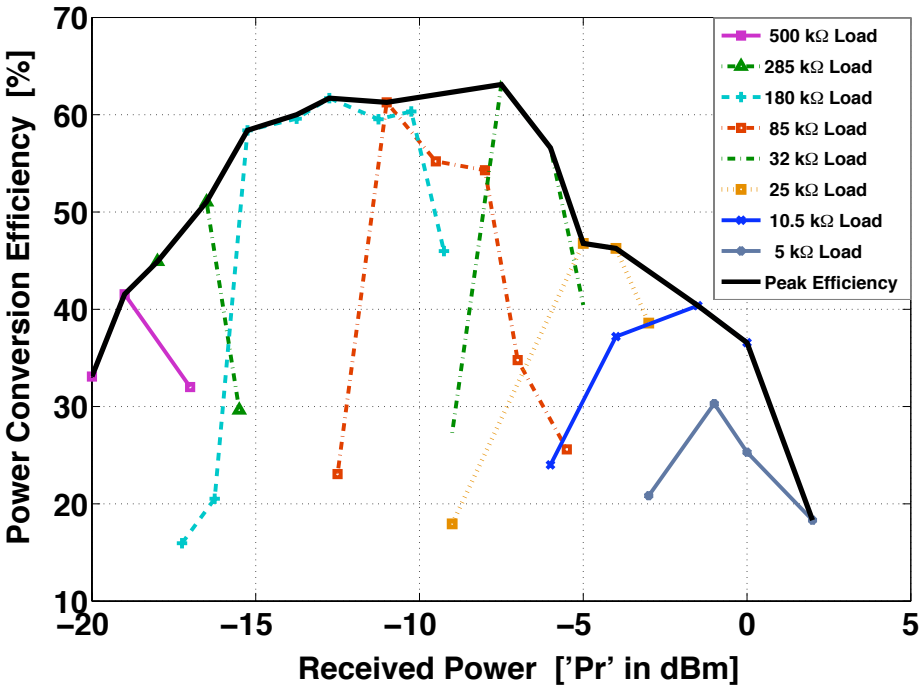


FIGURE 5.4: Peak conversion efficiency of the converter across various load power.

the previous work. The primary reason for this improvement is due to the reduced number of rectifier stages used in this design. The scavenger design with the switching regulator provides an efficient power conversion over a wide range of received power when compared to the previous work with the linear regulator in [36]. The output voltage regulation using switching converters is highly efficient over linear regulators.

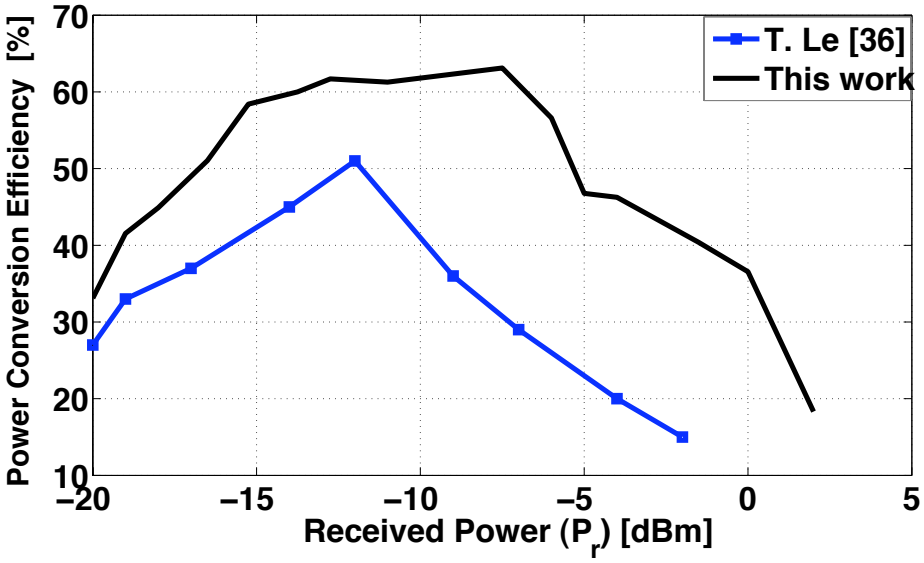


FIGURE 5.5: Efficiency performance of RF energy scavenging system.

5.3. Harvested Power of the RF Energy Scavenger

The most significant performance metric of the RF energy scavenging system is the measure of power harvested relative to the ambient RF received power. This research work has addressed the challenge of maximizing the harvested power.

Figure 5.6 shows the maximum extracted power from the RF received power using an antenna with a characteristic impedance of 50 Ω. The sensitivity is defined as the minimum received input power which can build and sustain a constant output voltage of 1.25 V at a maximum load current. It can be observed that a power as low as 3.2 μW can be harvested at an output voltage of 1.25 V, corresponding to a *scavenger sensitivity* of -17.5 dBm.

The extracted output power is plotted as a function of the calculated free-space distance [35] in Figure 5.7.

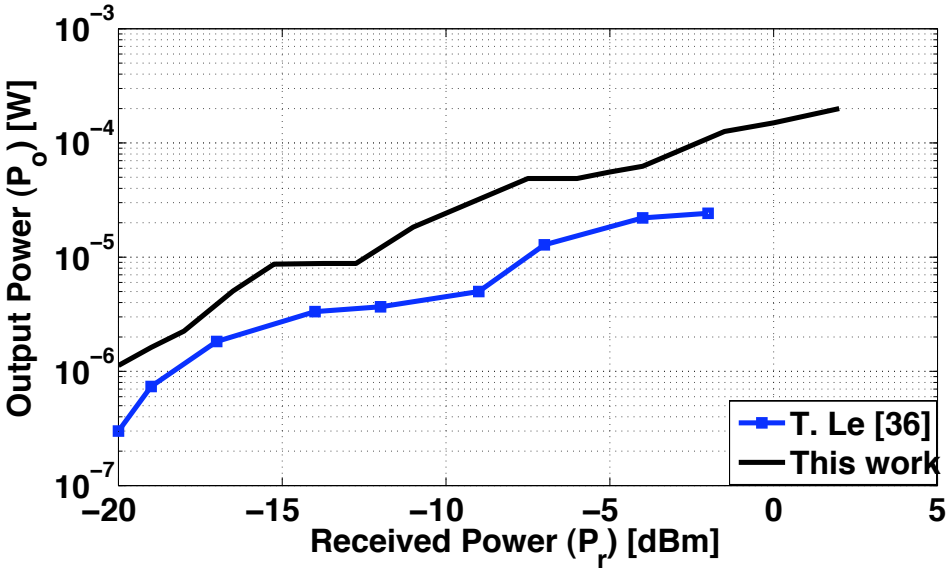


FIGURE 5.6: Harvested output power at an output voltage of 1.25 V.

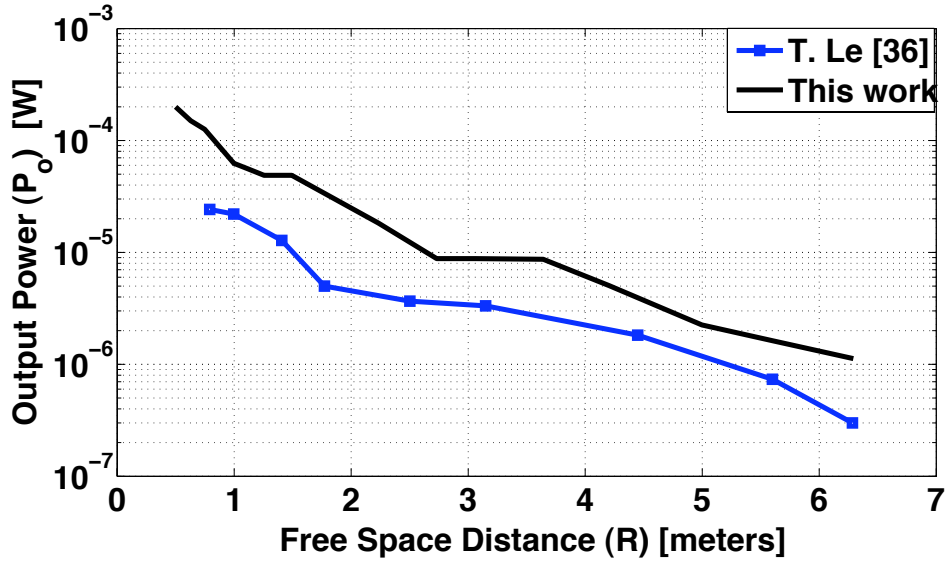


FIGURE 5.7: Harvested output power as a function of the free-space distance.

In practical wireless sensor applications, where the RF energy scavengers are deployed, the operable distance could possibly be less than the range as shown

in Figure 5.7 (6 meters at 2.4 GHz transmission). The presence of in-band RF interference will further reduce the received power density. The reduced received power decreases the effective output power harvested, thereby, decreasing the on-field operating range of the harvester.

5.4. Power Harvester Performance

This work summarizes the most recent work on RF energy scavenging and power management. Though the work presented here shows only simulated results, it is a promising approach for achieving higher performance of the scavenger compared to the previous work [36]. The simulated power conversion efficiency of 60% represents the highest reported to date.

6. CONCLUSION

In this work, a novel RF energy scavenging solution is proposed with a one-stage rectifier (AC-DC) and a highly efficient light load switching converter (DC-DC). The switched capacitor DC-DC converter operates in the hysteretic control mode and achieves the highest simulated efficiency reported for any integrated light-load converter to-date. The converter is capable of buck and boost conversion over a wide input voltage range, 400 mV to 8 V, for energy scavenging applications.

The design is implemented in a standard 180 nm CMOS process. The die area estimate for this design is 0.8 mm^2. The overall power conversion efficiency of the power harvester is 60% over a wide range of received power levels (-15.5 dBm to -6 dBm). The sensitivity of the scavenger is reported to be -17.5 dBm ($P_r \approx 17\ \mu$W). The range of free-space operation is calculated to be approximately 5 meters from an intentional RF transmitter operating under FCC specifications.

6.1. Future work

Future work in RF energy scavenging can be focused on increasing the incoming input power levels. In the interest of simplifying the analysis and design, the input impedance is assumed to be a constant, in this research. This is not generally true in a RF energy scavenging system, since the input impedance of the scavenger is a varying function of the received power. A reconfigurable matching network is needed to achieve resonance at the frequency of interest. The matching network should provide discrete or continuous tuning of the passive components in the net-

work. The concept of reconfigurable matching can be extended to implement input frequency tunability and scavenge the RF energy from multiple frequency bands using a multi-band antenna.

A disadvantage of the RF energy scavenging is the availability of very low input power levels for harvesting. An integrated universal micro-energy harvester which can extract power from multiple ambient sources can be developed. A hybrid inductive and capacitive switching converter is employed in the micro-energy harvester. The mode of operation of the harvester depends on the power density available in the environment for energy scavenging.

BIBLIOGRAPHY

1. Perpetual Power Solutions to Save $1 billion in Labor Costs [Online]. Available: http://www.onworld.com/html/newsperpower.htm

2. J. B. Lee, Z. Chen, M. G. Allen, A. Rohatgi, and R. Ayra, "A high voltage solar cell arrays as an electrostatic MEMS power supply," in *Proc. IEEE Workshop on Micro Electro Mechanical Systems*, Jan. 1994, pp. 331-336.

3. J. B. Lee, Z. Chen, M. G. Allen, A. Rohatgi, and R. Arya, "A miniaturized high voltage solar cell array as an electrostatic MEMS power supply," *IEEE/ASME Journal of Microelectromechanical Systems*, vol. 4, no. 3, pp. 102-108, Sep. 1995.

4. T. Le, J. Han, A. von Jouanne, K. Mayaram, and T.S. Fiez, "Piezoelectric power generation interface circuits," in *Proc. of IEEE Custom Integrated Circuit Conf. (CICC)*, Sep. 2003, pp. 489-492.

5. S. J. Roundy. "Energy scavenging for wireless sensor nodes with a focus on vibration to electricity conversion," *Ph.D. Thesis*, The University of California, Berkeley, Department of Mechanical Engineering, 2003.

6. M. Stordeur and I. Stark,"Low power thermoelectric generator self sufficient energy supply for micro systems," in *16th International Conference on Thermoelectrics*, Dec. 1997, pp. 575-577.

7. R. Venkatasubramanian, C. Watkins, D. Stokes, J. Posthill and C. Caylor,"Energy harvesting for electronics with thermoelectric devices using nanoscale materials," in *IEEE International Electron Devices Meeting*, Dec. 2007, pp. 367-370.

8. S. M. Gim, "Proposal on the conversion of room temperature thermal energy into useful form," in *Proc. IEEE Power Engineering Society Summer Meeting*, July 2001, pp. 1352-1356.

9. V. Leonov, T. Torfs, P. Fiorini and C. Van Hoof, "Thermoelectric converters of human warmth for self-powered wireless sensor nodes," *IEEE Sensors Journal*, vol. 7, no. 5, pp. 650-657, May 2007.

10. K. Fotopoulou and B. W. Flynn, "Wireless powering of implanted sensors using RF inductive coupling," in *5th IEEE Conference on Sensors*, Oct. 2006, pp. 765-768.

11. FCC Codes of Regulation, Part 15 [Online]. Available: http://www.access.gpo.gov/nara/cfr/waisidx 03/47cfr15 03.htm.

12. T. Umeda, H. Yoshida, S. Sekine, Y. Fuita, T. Suziki, and S. Otaka, "A 950-MHz rectifier circuit for sensor network tags with 10-m distance," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 35-41, Jan. 2006.

13. H. Nakamoto, D. Yamazaki, T. Yamamoto, H. Kurata, S. Yamada, K. Mukaida, T. Ninomiya, T. Ohkawa, S. Masui and K. Gotoh, "A passive UHF RFID tag LSI with 36.6% efficiency CMOS-only rectifier and current-mode demodulator in 0.35m FeRAM technology," in *International Solid State Circuits Conference*, Feb. 2006, pp. 310-311.

14. T. Le, K. Mayaram and T. S. Fiez, "Efficient far-field radio frequency energy harvesting for passively powered sensor networks," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1287-1302, May 2008.

15. T. H.Le, *The Design of CMOS Radio Frequency Integrated Circuits*, Cambridge University Press, 2004.

16. K. Ohsaki, N. Asamoto and S. Takagaki, "A single poly EEPROM Cell Structure for use in standard CMOS processes," *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 311- 316, March 1994.

17. J. Killen, "Utilizing standard CMOS process floating gate devices for analog design," *Masters Thesis*, Mississippi State University, Department of Electrical and Computer Engineering, Aug. 2001.

18. A. Shameli, A. Safarian, A. Rofougaran, M. Rofougaran and F. De Flaviis, "Power harvester design for passive UHF RFID tag using a voltage boosting technique," *IEEE Trans. Microwave Theory and Techniques*, vol. 55, no. 6, pp. 1089-1097, June 2007.

19. E. Bergeret, J. Gaubert, P. Pannier, and J. M. Gaultier, "Modeling and design of CMOS UHF voltage multiplier for RFID in an EEPROM compatible process," *IEEE Trans. Circuits Syst. II*, vol. 54, no. 10, pp. 833-837, Oct. 2007.

20. S. Mandal, "Far field RF power extraction circuits and systems," *Masters Thesis*, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, June 2004.

21. S. Mandal and R. Sarpeshkar, "Low-power CMOS rectifier design for RFID applications," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 6, pp. 1177-1188, June 2007.

22. T. Salter, K. Choi, M. Peckerar, G. Metze and N. Goldsman, "RF energy scavenging system utilising switched capacitor DC-DC converter," *IEEE Elec. Letters*, vol. 45, no. 7, pp. 374-376, March 2009.

23. P. Favrat, P. Deval, and M. J. Declercq, "A high efficiency CMOS voltage doubler," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 410-416, March 1998.

24. Application Note 737, "Choosing the right power-supply IC for your application," Maxim Semiconductor, Oct. 2009 [Online]. Available: http://www.maxim-ic.com.

25. Y. K. Ramadass and A. P. Chandrakasan, "Voltage scalable switched capacitor DC-DC converter for ultra-low-power on-chip applications," in *IEEE Power Electronics Specialists Conference*, June 2007, pp. 2353-2359.

26. J. Kwong, Y. K. Ramadass, N. Verma, and A. P. Chandrakasan, "A 65 nm sub-V_t microcontroller with integrated SRAM and switched capacitor DC-DC converter," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 115-126, January 2009.

27. M.D. Seeman, S.R. Sanders and J.M. Rabaey, "An ultra-low-power power management IC for energy-scavenged wireless sensor nodes," in *IEEE Power Electronics Specialists Conference*, June 2008, pp. 925-931.

28. T. Paing, E. Falkenstein, R. Zane and Z. Popovic, "Custom IC for ultra-low power RF energy harvesting," in *Applied Power Electronics Conference and Exposition*, Feb. 2009, pp. 1239-1245.

29. M. D. Seeman, "A design methodology for switched-capacitor DC-DC converters," *Ph.D. Thesis*, University of California, Berkeley, EECS Department, May 2009.

30. M.D. Seeman and S.R. Sanders, "Analysis and optimization of switched-capacitor DC-DC Converters," *IEEE Trans. Power Electronics*, vol. 23, no. 2, pp. 841-851, March 2008.

31. D. Maksimovic and S. Dhar, "Switched-capacitor DC-DC converters for low-power on-chip applications," in *IEEE Power Electronics Specialists Conference*, June 1999, pp. 54-59.

32. I. Oota, N. Hara, and F. Ueno, "A general method for deriving output resistances of serial fixed type switched-capacitor power supplies," in *IEEE International Symposium on Circuits and Systems*, vol. 3, May 2000, pp. 503-506.

33. M. S. Makowski and D. Maksimovic, "Performance limits of switched-capacitor dc-dc converters," in *IEEE Power Electronics Specialists Conference*, vol. 2, June 1995, pp. 1215-1221.

34. B. Arntzen and D. Maksimovic, "Switched-capacitor dc-dc converters with resonant gate drive," *IEEE Trans. Power Electronics*, vol. 13, no. 5, pp. 892-902, Sep. 1998.

35. H. T. Friis, "A note on a simple transmission formula," *Proceedings of the Institute of Radio Engineers*, vol. 34, no. 5, pp. 254-256, May 1946.

36. T. Le, "Efficient power conversion interface circuits for energy harvesting applications," *Ph.D. Thesis*, Oregon State University, Corvallis, EECS Department, Feb. 2008.

37. S. Chatterjee, K.P. Pun, Y. Tsividis, and P. Kinget, *Analog Circuit Design Techniques at 0.5 V*, Springer, 2007.

38. CAP-XX-HS206, "HS206 super-capacitor dataSheet," CAP-XX [Online]. Available: http://www.cap-xx.com

39. M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. Klumperink, and B. Nauta, "A 1.9 μW 4.4fJ/conversion-step 10b 1MS/s charge-redistribution ADC," in *IEEE International Solid-State Circuits Conference*, Feb. 2008, pp. 244-610.

40. G. Tzanateas, C. A. T. Salama, and Y. P. Tsividis, "A CMOS bandgap voltage reference," *IEEE J. Solid-State Circuits*, vol. 14, no. 3, pp. 655- 657, June 1979.

41. B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2001.