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Title: Design Techniques for Low Power ADCs

Abstract approved:

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Gabor C. Temes

This dissertation presents an incremental analog-to-digital converter (ADC) with digital digital-to-analog converter (DAC) mismatch correction. A theoretical time-domain analysis technique was developed to predict the noise performance of the incremental ADC, and a new optimization technique was proposed to minimize the output noise.

In the calibration mode, the incremental ADC itself is used to measure the mismatches of the internal multi-bit DAC. Three new calibration techniques, equation-solving calibration, inter-DAC mismatch calibration and modified "Sarhang-Nejad" calibration are proposed.

To verify the above techniques, a test chip was designed and fabricated in 0.18 μm CMOS process. The chip can work in single-sampling or double-sampling mode. Chopping with a fractal sequence is used to eliminate 1/f noise. The calibration circuit was implemented to calibrate the multi-bit DAC mismatches the in single-sampling mode and inter-DAC mismatches in the double-sampling mode.

Finally, two new design techniques for low-power ADCs, the two-step split-junction successive-approximation register (SAR) ADC and the hybrid cascaded ΔΣ ADC, are proposed.

Design Techniques for Low Power ADCs

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Wenhuan Yu, Author

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Chapter 1 Introduction

1.1 ADC Architectures and Applications

The analog-to-digital converter (A/D converter or ADC) is the interface between analog and digital circuits. ADCs can be divided into two categories: Nyquist-rate A/D converters and oversampling A/D converters. According to the Nyquist theorem, the sampling frequency needs to be at least twice the signal bandwidth, i.e., $f_s \geq 2f_B$, so that the original signal can be recovered from the sampled signal. The sampling rate of the Nyquist A/D converter is slightly greater than $2f_B$, while the sampling rate of the oversampling A/D converter is much higher than $2f_B$. In the oversampling ADC, the oversampled output signal is decimated to the Nyquist rate by a digital filter following the ADC.

As shown in Fig. 1-1, there exist many different ADC architectures for different applications. The flash and pipeline ADCs are mainly used for high speed, low resolution A/D conversions. The successive approximation ADC provides medium resolution and medium conversion speed. The delta-sigma (ΔΣ) ADC is usually used for high-resolution, medium or low speed A/D conversions. The dual-slope ADC is good for very high-resolution and very low-speed applications. The incremental ADC, which is the topic of this thesis, can be seen as a delta-sigma ADC with periodical reset. It can achieve higher resolution and faster speed than the dual-slope ADC.

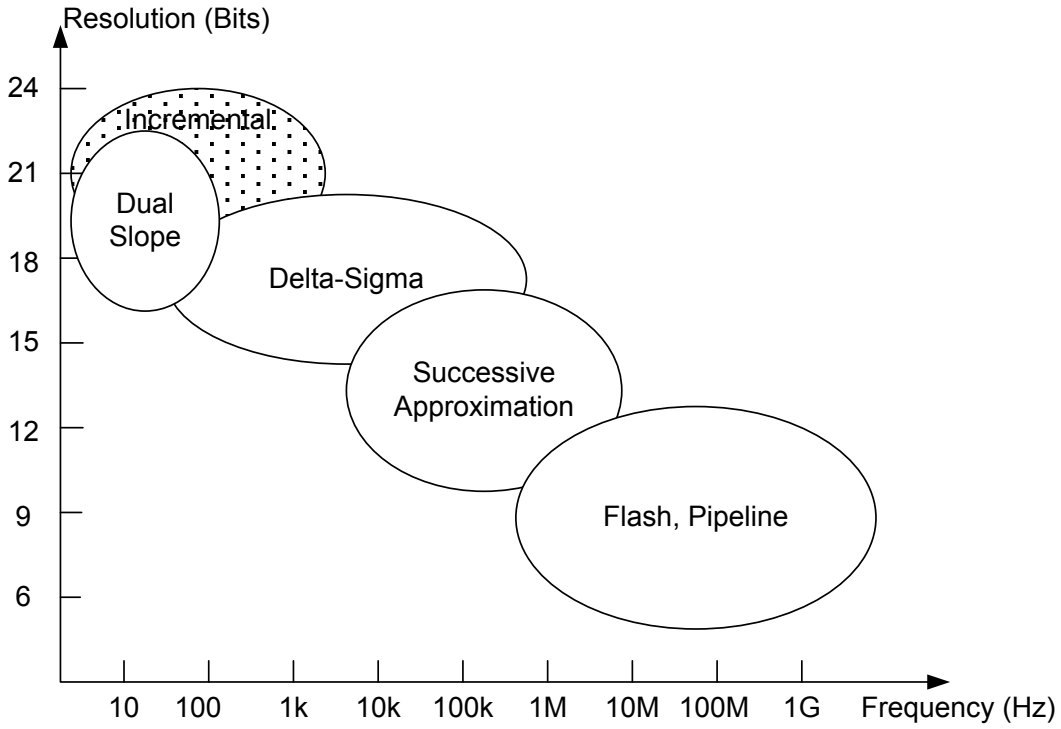


Fig. 1-1. ADC architectures for different applications [1-11].

1.2 History of Incremental ADCs

An incremental ADC is a ΔΣ ADC with periodical reset. The first incremental A/D converter was reported in 1978 [1-1]. Implemented in bipolar process, it was a first-order incremental A/D converter with 5-digit (with sign) resolution (about 17 bits).

Another first-order incremental ADC, shown in Fig. 1-2, was implemented in CMOS process [1-2], achieving 17 bits resolution. The name of "incremental ADC" was first proposed in this paper. In [1-3], an incremental ADC with multi-stage noise shaping (MASH) was proposed, consisting of two first-order ΔΣ loops.

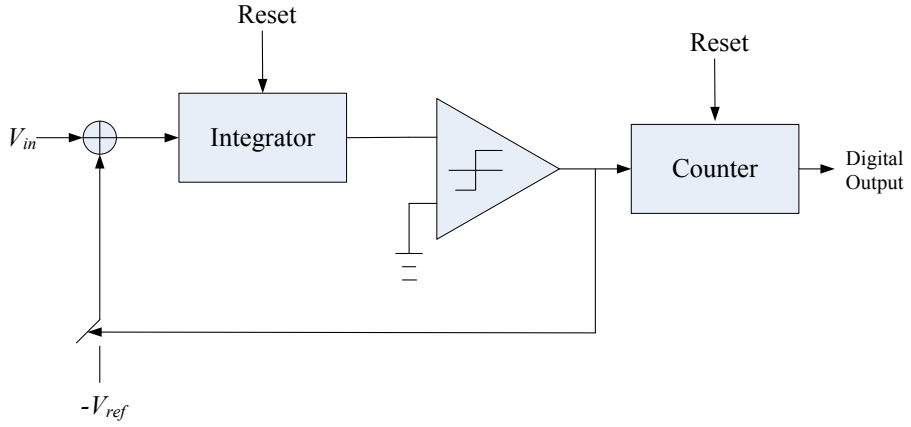


Fig. 1-2. A first-order incremental ADC.

More recently, a 22-bit 0.3 mW incremental ADC for DC measurement was reported in 2006 [1-4]. The incremental ADC for wideband application was discussed in [1-5]. An incremental ADC enhanced by a SAR ADC (extending counting) is presented in [1-6],

Some commercial products [1-7]–[1-10] may have used the incremental A/D converter architecture, sometimes called charge-balancing ΔΣ ADC, one-shot ΔΣ ADC or no-latency ΔΣ ADC.

Good overviews on incremental ADC can be found in [1-11] and [1-12].

1.3 Motivations of the Research on Incremental ADCs

One motivation of this research arises from the demand in biomedical applications. Recently, sensor arrays have been successfully used in acquiring

ExG signals, such as electroencephalographic (EEG) and electrocardiogram (ECG) signals [1-13]. The bandwidth of the ExG signal is low, but high-resolution ADC conversions are required. Since multiple sensors are used, it will save both power and cost to have a single ADC time-multiplexing between multiple channels.

The ΔΣ ADC is a good candidate because of its high signal-to-noise-and-distortion ratio (SNDR). However, a traditional ΔΣ ADC is not suitable for multiplexing between different channels.

Incremental ADCs inherit the high resolution of ΔΣ ADCs, and at the same time, provide the flexibility of time-multiplexing between different channels. Thus it is very suitable for ExG applications.

The other motivation of this research is the calibration of multi-bit DACs in double-sampling scheme using the incremental ADC itself. In double-sampling scheme, we need two feedback digital-to-analog converters (DACs) operating in opposite phases. The mismatch between these two DACs will fold the quantization noise into the signal band. It is called the "noise-folding" problem of the double-sampling scheme. Since incremental ADC is able to provide accurate measurement for DC input, we can use it to measure the inter-DAC mismatches. After we obtain the mismatch, digital compensation can be applied to eliminate the "noise-folding" problem in double sampling scheme. Also, the mismatches within each DAC can be digitally corrected as well.

1.4 Motivations of the Research on Low-Power ADCs

In power-limited applications, such as biomedical sensor and hearing aids, micro-power ADCs are needed. The successive-approximation registers ADCs (SAR ADCs) are good candidates for micro-power applications, because they have very few active devices. Based on the "split-junction" SAR ADC scheme, we propose an improved scheme that further reduces the power consumption.

We also propose a hybrid cascaded ΔΣ modulator scheme, which reduces the speed of the second stage drastically. In an *N*-0 cascaded structure, the second stage can now be implemented with a successive-approximation register (SAR) ADC instead of a pipeline ADC. The new scheme can achieve better performance with similar power consumption to the traditional scheme.

1.5 Structure of Thesis

Chapter 2 introduces the basics of multiplexed incremental ADCs, and presents a new analysis technique (proposed by J. Steensgaard) for incremental ADCs. Based on this, a new optimization technique for a decimation filter is presented.

Chapter 3 discusses the digital calibration techniques for double sampling ΔΣ and incremental ADCs with multi-bit DACs. First a new calibration scheme with linear equation solving is presented. Then a simplified calibration scheme without linear equation solving is proposed. Finally, an improvement for one existing calibration scheme is discussed.

Chapter 4 gives the details of the circuit implementation of the prototype incremental ADC. Measurement results are presented in this chapter.

Chapter 5 presents two new design techniques for low power ADCs. The first one is a new scheme that further reduces the power consumption of SAR ADCs. The second one is a hybrid cascaded ΔΣ ADC that reduces the speed of the second stage.

Chapter 6 summarizes the whole thesis.

Chapter 2 Analysis and Optimization of Incremental ADCs

2.1 Basics of Multiplexed Incremental ADCs

As shown in Fig. 2-1, the multiplexed incremental ADC is a delta-sigma ADC with reset. The signals u_1 to u_N are N input signals to be converted into the digital domain (e.g., signals of the sensor array in ExG applications). In the first conversion cycle, P1 is closed to connect u_1 to the incremental ADC. After M clock periods, we take the last output of the decimation filter as the conversion result of this conversion cycle (the decimation-by-M block in Fig. 2-1). Then we switch to the next input channel by opening P1 and closing P2. After all N channels are converted, we go back to channel 1 and start over again.

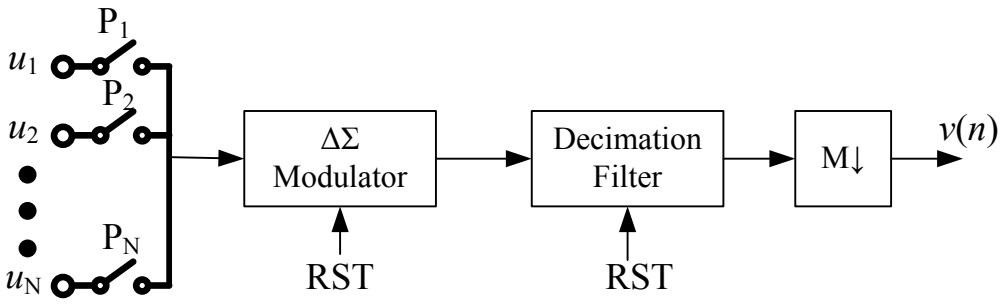


Fig. 2-1. Block diagram of multiplexed incremental ADC.

Because of the reset of the ΔΣ modulator and decimation filter, the ΔΣ ADC can now be time-multiplexed between multiple channels. To meet the Nyquist sampling requirement, the lowest clock frequency of the incremental ADC needs to be $f_s = N \cdot 2 \cdot f_B$, where f_B is the bandwidth of the signal in each channel. If we

look at one particular channel, the operation of the multiplexed incremental ADC is illustrated in Fig. 2-2.

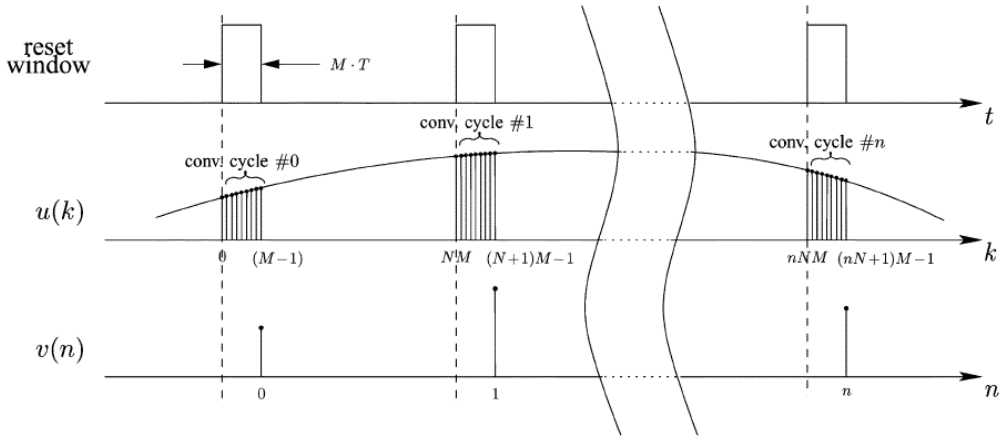


Fig. 2-2. Illustration of the operation of multiplexed incremental ADC [2-1].

2.2 Incremental ADC with Cascaded Integrator Decimation Filter [1-11]

As shown in Fig. 2-3, traditionally we can make a third-order incremental ADC by putting three digital integrators after a third-order ΔΣ modulator. The reason for doing this is given by the following analysis. Both the modulator and digital integrators are reset every *M* clock periods.

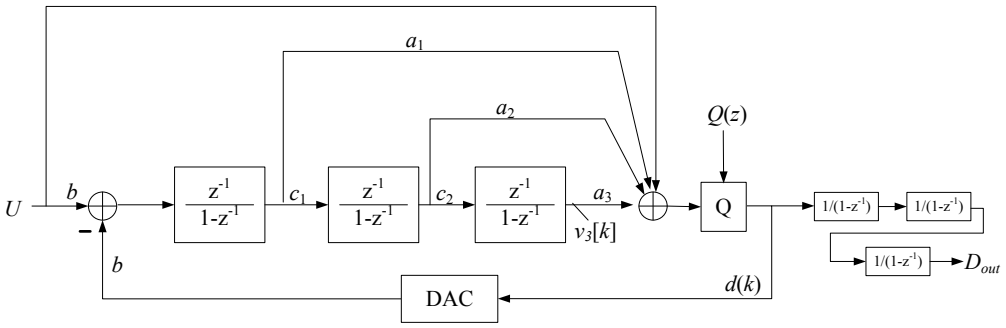


Fig. 2-3. A third-order incremental ADC with sinc^3 filter.

Assume the input is constant (or does not change much in one conversion cycle). In the time domain, the output of the loop filter at the M-th clock period is

$$\begin{aligned} & v_3(M) \\ &= \sum_{m=0}^{M-1}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1} U - \sum_{m=0}^{M-1}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1} d(k) \\ &= \frac{M(M-1)(M-2)}{6}U - \sum_{m=0}^{M-1}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1} d(k). \end{aligned} \tag{2-1}$$

Dividing both side by $M(M\text{-}1)(M\text{-}2)/6$, we get

$$\left\| U - \frac{6}{M(M-1)(M-2)}\sum_{m=0}^{M-1}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1} d(k) \right\| = \frac{6}{M(M-1)(M-2)}\left\| v_3(M) \right\|. \tag{2-2}$$

Since the ΔΣ modulator is stable, $v_3(M)$ is between $-V_{ref}$ and V_{ref}. We have

$$\left\| U - \frac{6}{M(M-1)(M-2)}\sum_{m=0}^{M-1}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1} d(k) \right\| \le \frac{6}{M(M-1)(M-2)}V_{ref}. \tag{2-3}$$

If we define $D_{out} = \dfrac{6}{M(M-1)(M-2)}\displaystyle\sum_{m=0}^{M-1}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1} d(k)$ as the digital conversion result, the conversion error satisfies

$$|\varepsilon| = |U - D_{out}| \le \frac{6 \cdot V_{ref}}{M(M-1)(M-2)}. \tag{2-4}$$

As shown in (2-4), the conversion error is approximately inversely proportional to M^3. Thus for $M = 100$, the conversion error is at microvolt level.

2.3 Noise Analysis of Incremental ADC [2-1]

The incremental ADC can be modeled as shown in Fig. 2-4, where $u(k)$ is the input signal, $t(k)$ is the input referred thermal noise and $q(k)$ is the quantization noise.

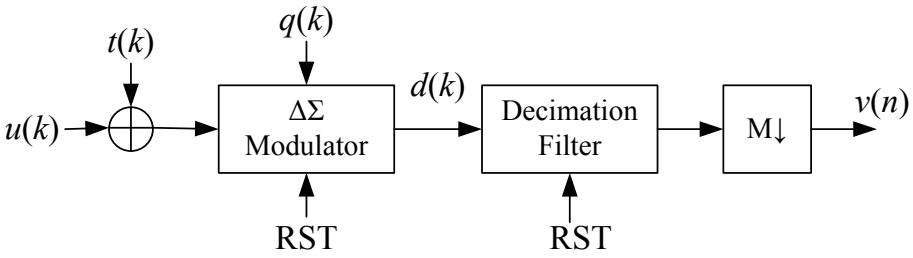


Fig. 2-4. Model of incremental ADC.

Due to the reset of the ADC, the impulse responses of the signal transfer function (*STF*) and noise transfer function (*NTF*) change from infinite length to finite length. Suppose that the incremental ADC is reset every M clock periods. The final result in the nth conversion cycle can be calculated as follows

$$v(n) = [stf'(k) * u(k)]_{M,n} + [stf'(k) * t(k)]_{M,n} + [ntf'(k) * q(k)]_{M,n} \tag{2-5}$$

where *stf'*(k) is the M sample impulse response of the overall signal transfer function $STF(z)H(z)$, and *ntf'*(k) is the M sample impulse response of the overall

noise transfer function $NTF(z)H(z)$. Here, $STF(z)$ and $NTF(z)$ are the signal transfer function and noise transfer function of the ΔΣ modulator without reset, respectively. $H(z)$ is the transfer function of the decimation filter without reset.

The first, second and third term in (2-5) represent the signal component, the thermal noise and the quantization noise in the output, respectively. The power of the input-referred thermal noise $t(k)$ can be estimated by $\gamma kT / C_{in}$, where k is the Boltzmann constant, T is the absolute temperature and C_{in} is the value of the input capacitors in the first integrator. The constant γ can be estimated from the input circuitry (γ = 5 is a good choice) [1-2]. The power of $q(k)$ can be estimated as $\Delta^2 / 12$, where Δ is the step size of the quantizer.

2.4 Noise Optimization of Incremental ADC [2-1]

As given by (2-5), the output noise (thermal and quantization noise) is related to $stf'(k)$ and $ntf'(k)$. The purpose of noise optimization is to choose M, C_{in} and the M-sample impulse response of the decimation filter, so that the output noise is minimized.

We denote $stf(k)$ and $ntf(k)$ as the M-sample impulse response of $STF(z)$ and $NTF(z)$, and $h(k)$ as the M-sample impulse response of $H(z)$. These impulse responses are given by

$$
\begin{aligned}
stf(k) &= \{s_0, s_1, \cdots, s_{M-1}\} \\
ntf(k) &= \{n_0, n_1, \cdots, n_{M-1}\} \\
stf'(k) &= \{s'_0, s'_1, \cdots, s'_{M-1}\} \\
ntf'(k) &= \{n'_0, n'_1, \cdots, n'_{M-1}\} \\
h(k) &= \{h_0, h_1, \cdots, h_{M-1}\}.
\end{aligned}
\tag{2-6}
$$

Because $stf'(k) = stf(k) * h(k)$ and $ntf'(k) = ntf(k) * h(k)$, the following vector relations hold

$$
\begin{aligned}
\mathbf{s}' &= \mathbf{S} \cdot \mathbf{h} \\
\mathbf{n}' &= \mathbf{N} \cdot \mathbf{h}
\end{aligned}
\tag{2-7}
$$

where

$$
\begin{aligned}
\mathbf{s}' &= \left[s'_0, s'_1, \cdots, s'_{M-1}\right]^T \\
\mathbf{n}' &= \left[n'_0, n'_1, \cdots, n'_{M-1}\right]^T \\
\mathbf{h} &= \left[h_0, h_1, \cdots, h_{M-1}\right]^T
\end{aligned}
$$

$$
\begin{aligned}
\mathbf{S} &= \begin{bmatrix}
s_0 & 0 & 0 & \cdots & 0 \\
s_1 & s_0 & 0 & \cdots & 0 \\
\vdots & \vdots & \vdots & \vdots & \vdots \\
s_{M-1} & s_{M-2} & s_{M-3} & \cdots & s_0
\end{bmatrix} \\
\mathbf{N} &= \begin{bmatrix}
n_0 & 0 & 0 & \cdots & 0 \\
n_1 & n_0 & 0 & \cdots & 0 \\
\vdots & \vdots & \vdots & \vdots & \vdots \\
n_{M-1} & n_{M-2} & n_{M-3} & \cdots & n_0
\end{bmatrix}.
\end{aligned}
\tag{2-8}
$$

From (2-5) to (2-8), the thermal noise power can be estimated as

$$
\begin{aligned}
\overline{v_t(n)^2} &= \frac{\gamma kT}{C_{in}}\left(s'^2_0 + s'^2_1 + \cdots + s'^2_{M-1}\right) \\
&= \frac{\gamma kT}{C_{in}} \mathbf{h}^T \cdot \mathbf{S}^T \cdot \mathbf{S} \cdot \mathbf{h}.
\end{aligned}
\tag{2-9}
$$

The quantization noise power can be estimated as

$$\begin{aligned}\overline{v_q(n)^2} &= \frac{\Delta^2}{6}\left(n_0'^2 + n_1'^2 + \cdots + n_{M-1}'^2\right) \\ &= \frac{\Delta^2}{6}\mathbf{h}^T \cdot \mathbf{N}^T \cdot \mathbf{N} \cdot \mathbf{h}\end{aligned} \tag{2-10}$$

Let the maximum peak-to-peak output sine wave amplitude be V_{pp}. The SNR of the incremental ADC is

$$SNR = 10\log\left[\frac{V_{pp}^2/2}{\overline{v_t(n)^2} + \overline{v_q(n)^2}}\right] = 10\log\left[\frac{V_{pp}^2/2}{\mathbf{h}^T \cdot \mathbf{O} \cdot \mathbf{h}}\right] \tag{2-11}$$

where

$$\mathbf{O} = \frac{\gamma kT}{C_{in}}\left[\mathbf{S}^T \cdot \mathbf{S} + \rho \cdot \mathbf{N}^T \cdot \mathbf{N}\right] \tag{2-12}$$

and

$$\rho = \frac{\Delta^2/6}{\gamma kT/C_{in}}. \tag{2-13}$$

Based on the above analysis, an SNR optimization technique is proposed. The overall noise is minimized for a given power consumption by choosing M, C_{in} and the impulse response of the decimation filter $h(k)$ properly.

For a given M and C_{in}, the optimization of the impulse response of the decimation filter can be formulated as follows

$$\begin{aligned}&\min\ \mathbf{h}^T \cdot \mathbf{O} \cdot \mathbf{h} \\ &\text{subject to } \mathbf{e}^T \cdot \mathbf{h} = 1\end{aligned} \tag{2-14}$$

where **O** is defined in (2-12) and **e** is $[1,1,\cdots,1]^T$. The objective function is the overall noise, and the constraint is to ensure $H(z) = 1$ for $z = 1$. Since $STF(z)$ is 1, the constraint ensures the overall signal transfer function to be 1 at DC.

The quadratic program (2-14) can be solved with Matlab. The analytical solution can also be found by the Lagrange multiplier technique as

$$\mathbf{h}^* = \frac{\mathbf{O}^{-1}\mathbf{e}}{\mathbf{e}^T\mathbf{O}^{-1}\mathbf{e}} \tag{2-15}$$

It is observed that the optimal **h** for thermal noise is simply **e**/M. When the quantization noise is taken into account, the optimal **h** turns into $\mathbf{h}^*$.

We define the thermal noise penalty factor as

$$\beta = \frac{\text{actual thermal noise power}}{\text{minimum thermal noise power}} = \frac{\sum_{i=0}^{M-1} 1/h_i^{*2}}{\sum_{i=0}^{M-1} 1/M^2}. \tag{2-16}$$

The typical value of β is around 1.5. It reflects the trade-off between the thermal noise and quantization noise.

Since the power consumption of the incremental ADC is inversely proportional to $M \cdot C_{in}$ (larger M means higher clock frequency, and larger C_{in} means larger OTA load), we choose the minimum $M \cdot C_{in}$ that meets the SNR specifications. Then we do a series of optimizations for different combinations of M and C_{in} and choose the one that gives the best SNR. It is found that larger M and smaller C_{in} usually gives better SNR.

2.5 Comparison between ΔΣ and Incremental ADCs

For an L-th order ΔΣ ADC, assuming a brick-wall decimation filter is used, the quantization noise after decimation is

$$\sigma_{q,\Delta\Sigma}^2 \approx \int_0^{1/2M} (2\pi f)^{2L} \cdot 2 \cdot \frac{\Delta^2}{12} df = \frac{\pi^4 \Delta^2}{12 \cdot (2L+1) \cdot M^{2L+1}}. \tag{2-17}$$

where M is the oversampling ratio (OSR) and Δ is the quantizer step size. If a sinc^L decimation filter is used, the signal-to-quantization-noise ratio (SQNR) is slightly higher [2-2].

In comparison, as suggested by (2-4), if an L-th order cascaded integrator decimation filter is used for an L-th order incremental ADC, the quantization noise after decimation is

$$\sigma_{q,incr}^2 \approx \frac{36 V_{ref}^2}{b^2 c_1^2 c_2^2 M^{2L}} = \frac{36 K^2 \Delta^2}{b^2 c_1^2 c_2^2 M^{2L}}. \tag{2-18}$$

where K is the total number of steps of the quantizer. Optimal decimation filter (section 2.4) usually gives slightly lower output quantization noise (decimation filter is optimized for the sum of the thermal noise and quantization noise).

It can be observed that the output quantization noise after decimation is inversely proportional to M^{2L+1} for an L-th order ΔΣ ADC, and is inversely proportional to M^{2L} for an L-th order incremental ADC. Thus incremental ADCs usually have lower SQNR than its ΔΣ counterparts. This is confirmed by the peak SQNR versus OSR graph (Fig. 2-5) for a second-order ΔΣ ADC with a sinc^3

decimation filter, a second-order incremental ADC with a cascaded integrator decimation filter and a second-order incremental ADC with an optimal decimation filter.

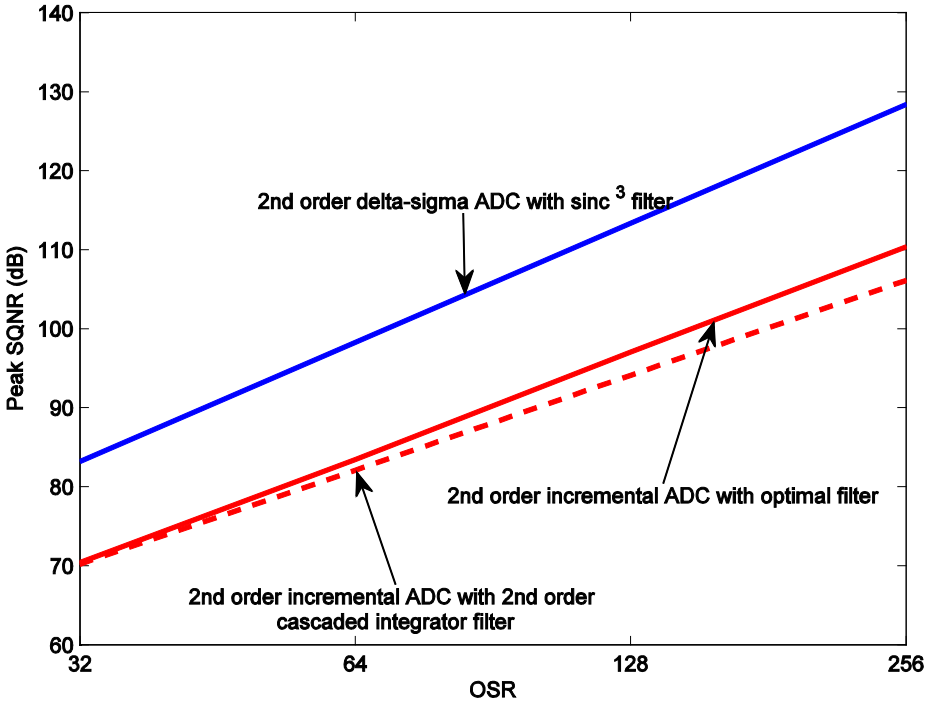


Fig. 2-5. A third-order incremental ADC with sinc^3 filter.

The performance degradation of incremental ADC is a trade-off for the ability to multiplex between multiple input channels. Because of the reset of ΔΣ modulators and decimation filter, the length of the impulse response of the incremental ADC is limited to M. In comparison, for a L-th order ΔΣ ADC, a $\text{sinc}^{(L+1)}$ filter is used. The length of the impulse response of a $\text{sinc}^{(L+1)}$ filter is $M^*(L+1)-(L-1)$, much longer than that of the incremental ADC.

Chapter 3 Digital Calibration and Compensation Techniques

3.1 Introductions

The use of multi-bit quantizer in ΔΣ modulators has many advantages, such as lower quantization noise and better stability [3-1]. However, the elements of a multi-bit DAC can not be made exactly same, and the mismatches between them are called DAC mismatches. As the DAC mismatches are added directly to the input of the modulator without noise-shaping (Fig. 3-1), the accuracy of the ΔΣ modulator is limited by the DAC mismatches.

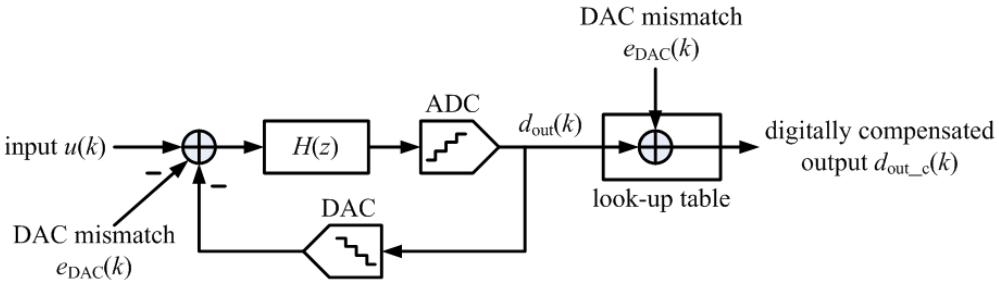


Fig. 3-1. Digital compensation scheme for multi-bit DAC mismatches.

In the double-sampling scheme, two DACs are operating in opposite phases. The mismatch between two DACs (inter-DAC mismatch) modulates the feedback signal going through the DACs. This effect, called noise-folding, folds the quantization noise back to the signal band and ruins the SNDR [3-2].

One way to eliminate the DAC mismatch problem is to use dynamic element matching (DEM), which shuffles the DAC elements and noise-shapes the DAC

mismatch errors. The most widely-used DEM technique is data-weighted averaging (DWA) [3-3]. Unfortunately, the DEM technique cannot be applied to eliminate the inter-DAC mismatch in double-sampling scheme.

To solve the noise-folding problem in double-sampling scheme, special integrators and circuits are proposed [3-2][3-4]. However, this either complicates the design procedure or introduces extra circuit elements.

As shown in Fig. 3-1, if we can measure the mismatches of the DAC elements, we can obtain the DAC mismatch sequence $e_{DAC}(k)$. Since the transfer function of the DAC mismatch is approximately 1 in the signal band, we can simply subtract $e_{DAC}(k)$ in the digital domain to compensate the DAC mismatch error. Both intra-DAC and inter-DAC mismatch can be calibrated and compensated digitally this way.

3.2 DAC Calibration with Equation Solving [3-5]

To measure the mismatches of the DAC elements, a calibration capacitor is added in the first integrator of a third-order ΔΣ modulator (Fig. 3-2) to add a constant input. Four capacitors are used in the DAC to feed the 5-level quantizer output back to the input. The input capacitors and DAC feedback capacitors are shared.

A log shifter is put after the quantizer. The log shifter, similar to that in DWA, shifts the quantizer output (in thermometer code) according to the pointer (PTR in

Fig. 3-2). However, in the calibration mode, the pointer is controlled by an off-chip signal (DACPTR1 and DACPTR0 pins), instead of by DWA logic.

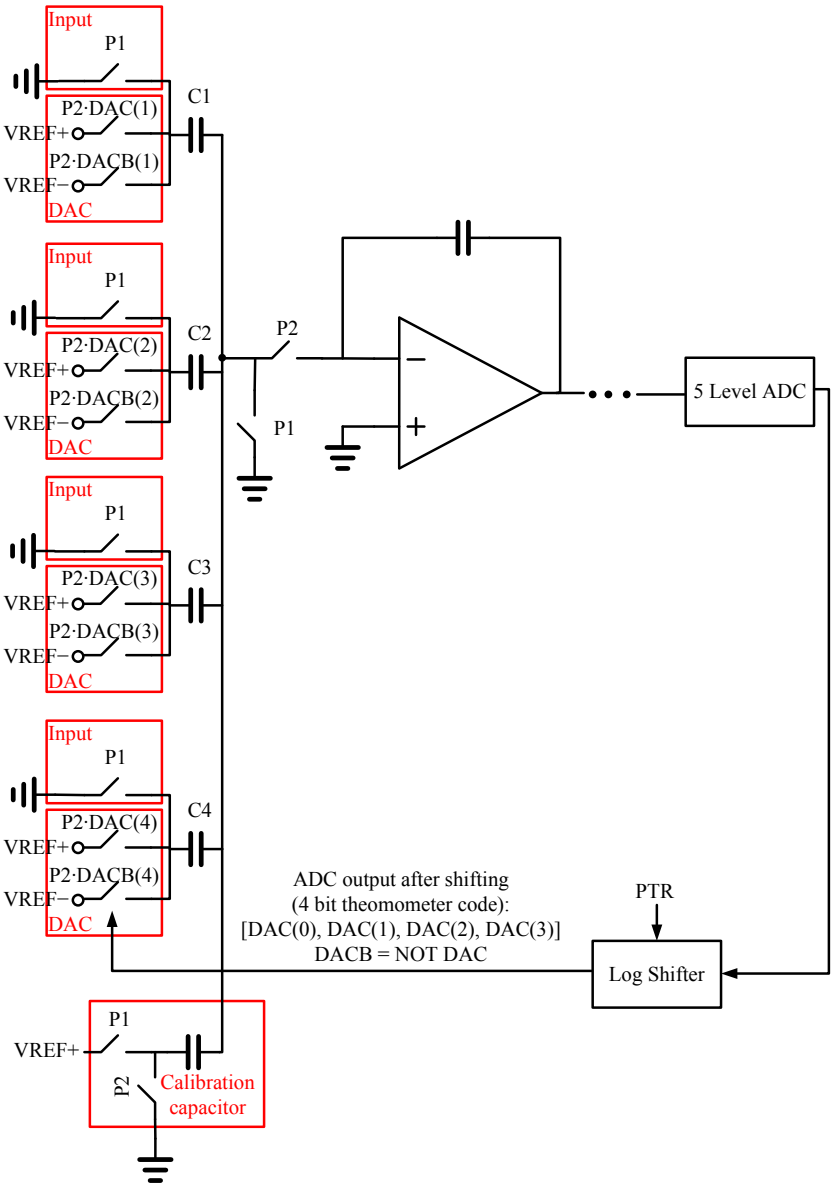


Fig. 3-2. The DAC and calibration capacitor in the first integrator.

In the calibration mode, the ΔΣ modulator is run as an incremental ADC. Four conversions are needed to obtain the DAC mismatch information. In each conversion, the PTR (DACPTR1 and DACPTR0) sets one of the DAC capacitors as the first DAC element.

Let $C_i = C(1+x_i)$, i = 1, 2, 3, 4, where C_i is the value of the DAC element capacitor and C is the value of the calibration capacitor. We take C as the desired value of the DAC element capacitors. The x_i (i = 1, 2, 3, 4) are the relative DAC mismatch errors.

In the calibration mode, we connect the input terminal to the common-mode voltage, and the calibration capacitor branch to VREF+ (Fig. 3-2). Effectively, we are applying an input voltage V_{ref} / 4.

The modulator runs as an incremental ADC, and hence each conversion takes M clock periods. Suppose PTR = 0 (DACPTR1 = 0 and DACPTR0 =0, which makes C1 the first capacitor of the DAC). If there are no DAC mismatches ($C_i = C$, i = 1, 2, 3, 4), half of the outputs will be 0, and the other half 1/2. According to section 2.2, if we assume V_{ref} = 1 V, we have

$$v_3(M) = bc_1c_2\left(\sum_{m=0}^{M-1}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1}\frac{1}{4} - \sum_{m=0}^{M-1}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1}d_{out}[k]\right).. \qquad (3\text{-}1)$$

If there are mismatches between the DAC elements and the calibration capacitor C, the modulator output stream will change and (3-1) turns into

$$
\begin{aligned}
& v_3(M) \\
&= bc_1c_2[\sum_{m=0}^{M-1}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1}\frac{1}{4} - \sum_{m=0}^{M-1}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1} d_{out}[k] - \frac{1}{4}\sum_{m=0}^{M-1}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1} s_0[k](x_1 + x_2 - x_3 - x_4) \\
&\quad - \frac{1}{4}\sum_{m=0}^{M-1}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1} s_{1/2}[k](x_1 + x_2 + x_3 - x_4)]
\end{aligned} \tag{3-2}
$$

where $s_0[k]$ and $s_{1/2}[k]$ are the output detection sequences

$$
s_i[k] = \begin{cases} 1 & d_{out}[k] = i \\ 0 & d_{out}[k] \neq i \end{cases}. \tag{3-3}
$$

The third and fourth term in (3-2) represent the DAC mismatch error feeding into the first integrator. The mismatch error is $x_1 + x_2 - x_3 - x_4$ when $d_{out}[k]$ = 0, and $x_1 + x_2 + x_3 - x_4$ when $d_{out}[k]$ = 1/2. Since $d_{out}[k]$ is either 0 or 1/2, (3-2) can be rearranged as

$$
\begin{aligned}
& v_3(M) \\
&= bc_1c_2[\sum_{l=0}^{M-1}\sum_{m=0}^{l-1}\sum_{k=0}^{m-1}\frac{1}{4} - \sum_{l=0}^{M-1}\sum_{m=0}^{l-1}\sum_{k=0}^{m-1} d_{out}[k] \\
&\quad - \frac{1}{4}\frac{M(M+1)(M+2)}{6}x_1 - \frac{1}{4}\frac{M(M+1)(M+2)}{6}x_2 \\
&\quad - \frac{1}{4}\sum_{l=0}^{M-1}\sum_{m=0}^{l-1}\sum_{k=0}^{m-1}(-s_0[k] + s_{1/2}[k])x_3 + \frac{1}{4}\frac{M(M+1)(M+2)}{6}x_4].
\end{aligned} \tag{3-4}
$$

Dividing both sides of (3-4) by $L = bc_1c_2M(M+1)(M+2)/6$ and ignoring $v_3(M)/L$ (since $v_3(M)/L$ is at the microvolt level for M = 100), we have the linear equation

$$
\frac{1}{4}x_1 + \frac{1}{4}x_2 + \frac{1}{4}a_1x_3 - \frac{1}{4}x_4 = b_1. \tag{3-5}
$$

where

$$
a_1 = \frac{1}{L}\sum_{l=0}^{M-1}\sum_{m=0}^{l-1}\sum_{k=0}^{m-1}(-s_0[k] + s_{1/2}[k]). \tag{3-6}
$$

$$b_1 = \frac{1}{4} - \frac{1}{L}\sum_{l=0}^{M-1}\sum_{m=0}^{l-1}\sum_{k=0}^{m-1} d_{out}[k]. \quad (3\text{-}7)$$

Next, we change the PTR to 1, and then to 2 and 3, and repeat the above process. The following set of equations results:

$$\begin{bmatrix} \frac{1}{4} & \frac{1}{4} & \frac{1}{4}a_1 & -\frac{1}{4} \\ -\frac{1}{4} & \frac{1}{4} & \frac{1}{4} & \frac{1}{4}a_2 \\ \frac{1}{4}a_3 & -\frac{1}{4} & \frac{1}{4} & \frac{1}{4} \\ \frac{1}{4} & \frac{1}{4}a_4 & -\frac{1}{4} & \frac{1}{4} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} = \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix}. \quad (3\text{-}8)$$

where a_i and b_i (i = 2, 3, 4) are obtained in the same way as in (3-6) and (3-7). Solving (3-8), we can obtain the DAC mismatches. To solve the linear equation, a simple arithmetic logic unit (ALU) is required.

After the DAC mismatches are obtained, we can compensate them with a look-up table in the digital domain (Fig. 3-3). Since the transfer function of the DAC mismatch errors is approximately 1 in the signal band, we can simply subtract the DAC mismatch error from the quantizer output.

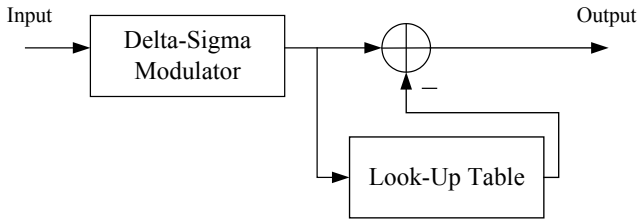


Fig. 3-3. Digital compensation of DAC mismatches.

In real implementation, the operational trans-conductance amplifier (OTA) non-idealities (finite DC gain, bandwidth, slew rate, and offset) will introduce error into the calibration process. The DC offset of the OTA can be eliminated by correlated double sampling (CDS) or chopping. It can be shown that if the DAC mismatches are the dominant source deteriorating the performance (which means that the incremental ADC can give accurate result without DAC mismatches), the described calibration is effective.

By calibrating two DACs separately with the same calibration capacitor, the above procedure can be used to measure and correct the inter-DAC mismatches in double-sampling architecture.

MATLAB simulation was used to verify the above calibration scheme. A double-sampling ΔΣ modulator with 5-level quantizer was used in the simulation. Each conversion in the calibration mode took M = 230 clock periods. The calibration of the modulator took 8 conversions in total.

The DC gain, slew rate, bandwidth and the offset of the OTAs were all considered in the simulation. The DC gains of the OTAs were assumed to be 40 dB, and the loop-gain unity-gain bandwidths (UGBW) 80 MHz, 65 MHz and 65 MHz, respectively. The DC offsets were assumed to be 10 mV and chopping was used. The clock frequency is 30 MHz.

The DAC mismatches and the estimation obtained from solving (3-8) are shown in Table 3-1. Around 0.5 % DAC mismatches were added in the simulation.

The calibration effectively reduces the DAC mismatches to 0.0005 %. The same simulation was performed with a transistor-level design. Results similar to those in Table 3-1 were obtained.

The effects of the digital compensation on the conversion accuracy were evaluated using an incremental ADC (with the same ΔΣ modulator as in the previous discussion). A DC input is used as the input signal in the test. The conversion error versus input DC voltage before and after calibration is shown in Fig. 3-4.

Table 3-1. DAC Mismatches and Estimations (Equation Solving Calibration)

	DAC Mismatches $[x_1, x_2, x_3, x_4]^T$	***Estimation from solving* (3-8)** $[x_1, x_2, x_3, x_4]^T$
DAC1	0.0015 0.0035 –0.0015 –0.0025	0.001503 0.003505 –0.001497 –0.002496
DAC2	0.0035 –0.0015 –0.0055 0.0025	0.003501 –0.001496 –0.005498 0.002503

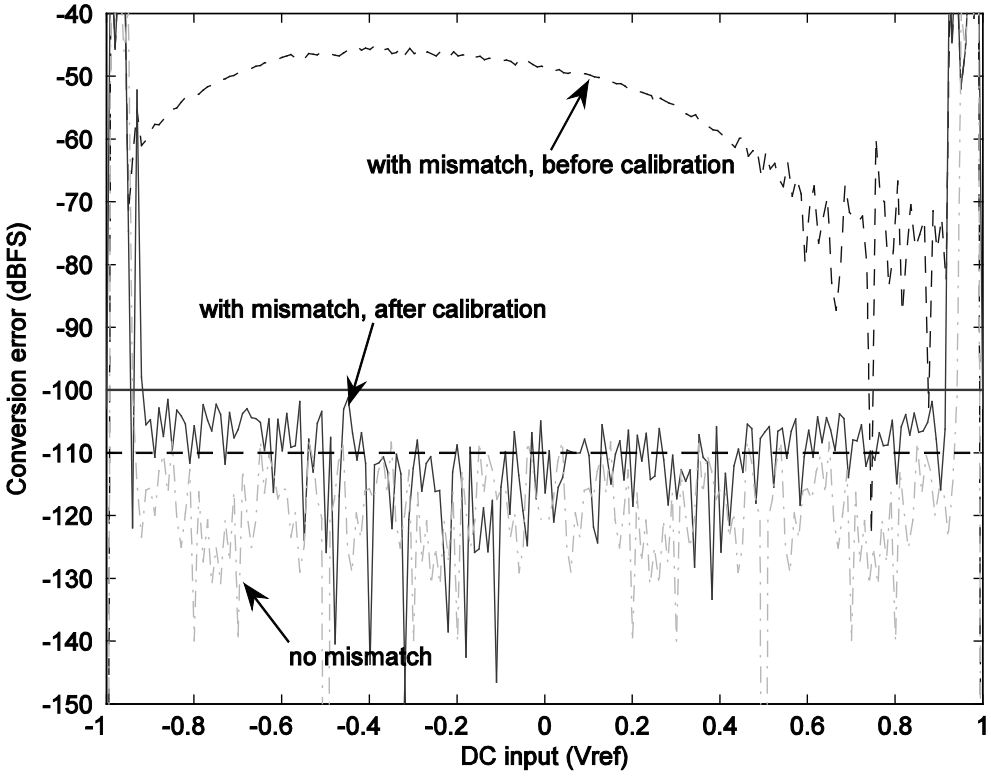


Fig. 3-4. Conversion error versus DC input.

3.3 DAC Calibration for Inter-DAC Mismatches [3-6]

As pointed out in [3-7], the double-sampling scheme effectively doubles the over-sampling ratio (OSR) of the ΔΣ modulator. However, as shown in Fig. 3-5, it also introduces the quantization noise folding problem due to the mismatch between two DACs operating in opposite phases (inter-DAC mismatch).

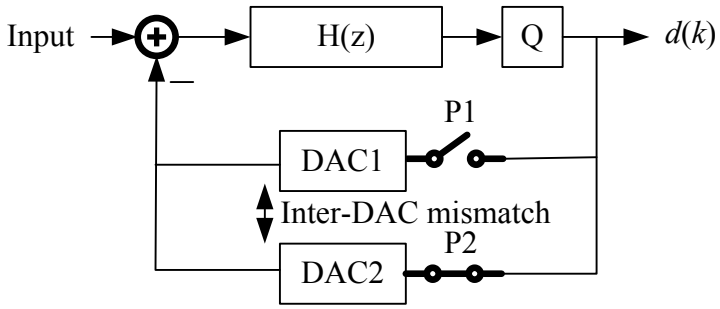


Fig. 3-5. Inter-DAC mismatch in double-sampling ΔΣ modulator.

To eliminate the inter-DAC mismatch in double-sampling ΔΣ modulator, we propose a new scheme which uses data-weighted averaging (DWA) to eliminate the mismatches inside each DAC (intra-DAC mismatch) and digital compensation to eliminate the mismatch between DAC1 and DAC2 (inter-DAC mismatch).

The scheme is based on the observation that the DC gain of the ΔΣ modulator is

$$STF(1) = b / b_1 . \tag{3-9}$$

where b and b_1 are the branch gain shown in Fig. 3-6. In calibration mode, the double-sampling ΔΣ modulator is run as a single-sampling incremental ADC, using either DAC1 or DAC2. We denote b_1 by $b_{1\text{-DAC1}}$ if DAC1 is used, and by $b_{1\text{-DAC2}}$ if DAC2 is used. As suggested by (3-9), if we keep the branch gain b the same, we can calibrate $b_{1\text{-DAC1}}$ and $b_{1\text{-DAC2}}$ against b.

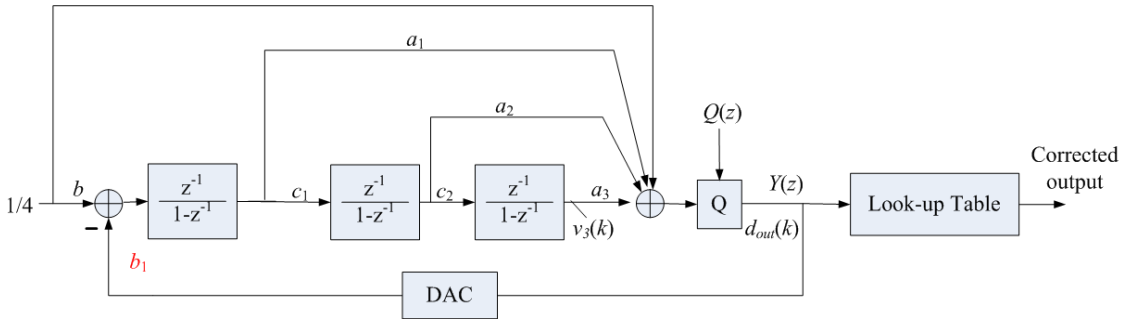


Fig. 3-6. A third-order ΔΣ modulator with a look-up table for digital correction.

The same calibration capacitor in the equation-solving calibration circuit is used (Fig. 3-2) to put a constant input of V_{ref} / 4 and a constant branch gain b. DWA is enabled to eliminate the "intra-DAC" mismatches in calibration. The gain of each DAC branch is calculated as

$$b_{1-DAC_i} = \frac{b}{STF(1)} = \frac{1/4}{v_i} b \,,\ i = 1, 2. \tag{3-10}$$

where v_i is the conversion result of the incremental ADC. Based on the estimated $b_{1\text{-DAC1}}$ and $b_{1\text{-DAC2}}$, we can calculate the corrected modulator outputs and store them in the look-up table. The inter-DAC mismatches are compensated by subtracting $(\frac{1}{4v_1} - 1)d_{out}$ in the clock phase 1 (when DAC1 is used as the feedback DAC) and $(\frac{1}{4v_2} - 1)d_{out}$ in the clock phase 2 (when DAC2 is used as the feedback DAC).

The calibration only takes two conversions. The Matlab simulation result of inter-DAC calibration is shown in Fig. 3-7.

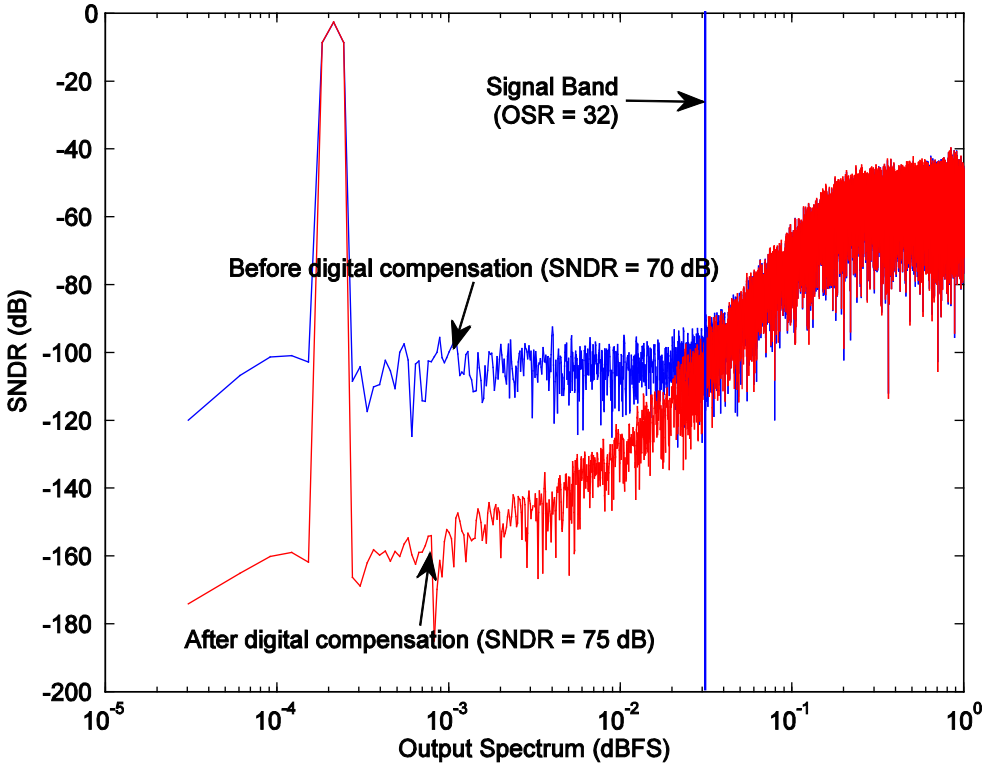


Fig. 3-7. The spectra of a third-order double-sampling modulator output with and without "inter-DAC" correction (around 0.5 % DAC mismatch is added, DWA is enabled for "intra-DAC" mismatches for both simulations).

3.4 Modified "Sarhang-Nejad" Calibration [3-8]

Another digital calibration scheme, which does not require equation solving, is to reconfigure the ΔΣ modulator into an incremental ADC with a two-level DAC, with which we calibrate the multi-level DAC [3-8].

As shown in Fig. 3-8, the 4-bit DAC is replaced by a 2-level DAC (switch connected to V_{ref}+ and V_{ref}–) in the calibration mode. The ΔΣ modulator with the 2-level DAC is run as an incremental ADC. Since an incremental ADC with a 2-

level DAC is accurate, it is used to measure the output of the 4-bit DAC. The calibration results are stored in a look-up table. After the calibration, the ΔΣ modulator runs with the multi-level DAC and the look-up table is used to compensate for DAC mismatches.

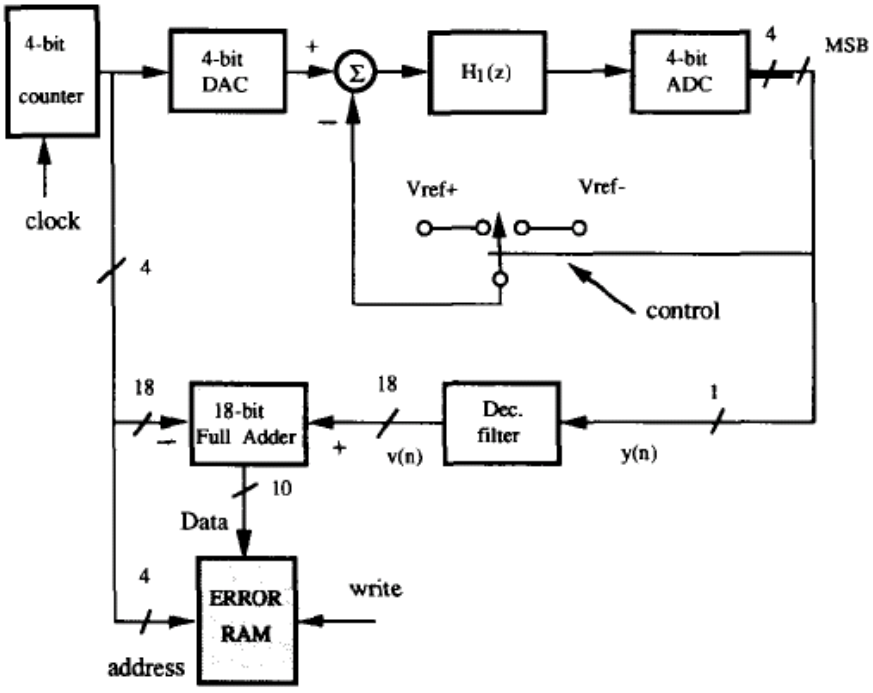


Fig. 3-8. Sarhang-Nejad calibration scheme for DAC mismatches [3-8].

One potential problem with this scheme is the stability in calibration mode for high-order ΔΣ modulator, especially when the input is close to ± V_{ref}. To solve this problem, we can feed only the difference between each DAC element and the calibration element, instead of all possible DAC output levels, to the incremental

ADC. Since this difference is usually small, the stability and the accuracy of the incremental ADC can be guaranteed.

Fig. 3-9 shows a 5-level DAC in the ΔΣ modulator under calibration. The ΔΣ modulator is reconfigured into an incremental ADC with a 2-level quantizer.

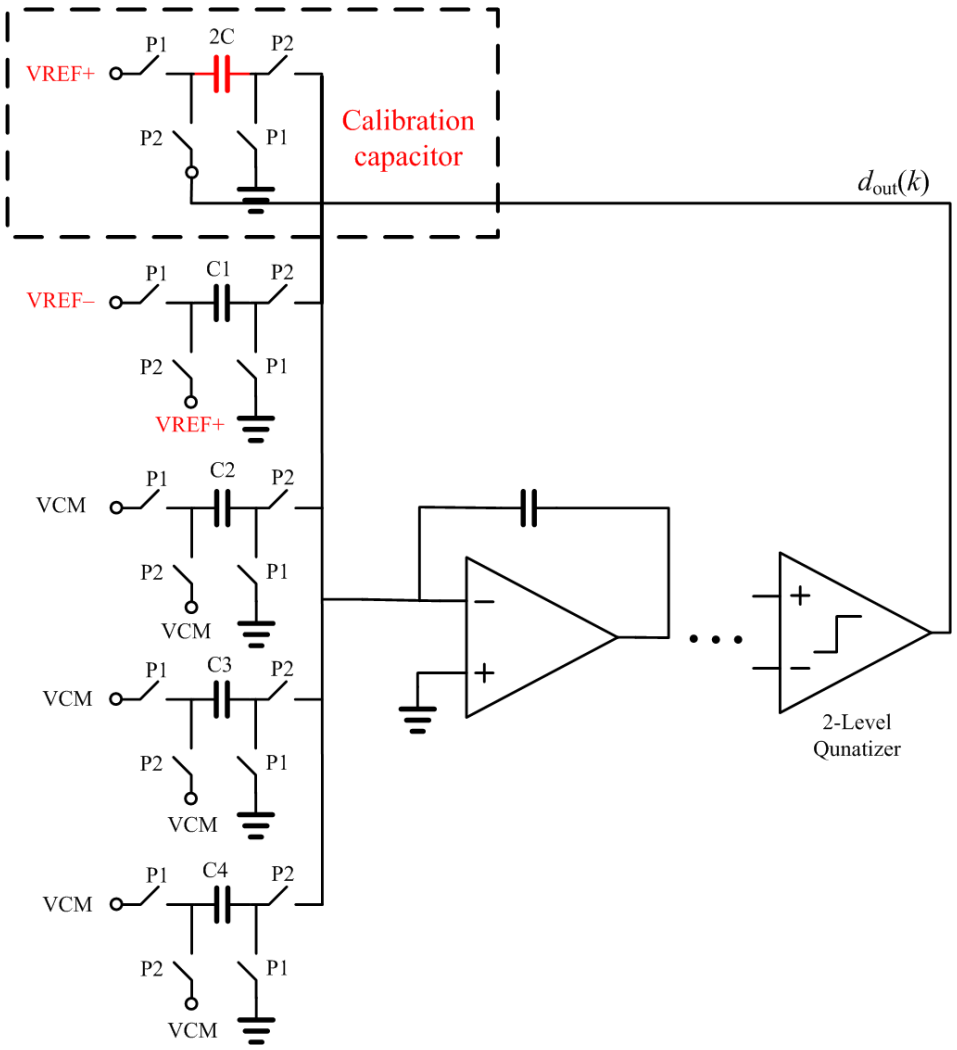


Fig. 3-9. Proposed DAC calibration circuit [3-6].

We denote the capacitors in the 5-level DAC by C_i (i = 1, 2, 3, 4). The value of the calibration capacitor is $2C$, where C is regarded as the accurate value of the

DAC element capacitors. We denote the relative mismatches of C_i by x_i, so $C_i = C(1+x_i)$ (i = 1, 2, 3, 4).

The DAC element capacitor under calibration (C1 in Fig. 3-9) is connected to V_{ref}^- in clock phase P1 and to V_{ref}^+ in clock phase P2. The calibration capacitor (2C in Fig. 3-9) is connected to V_{ref}^+ in clock phase P1 and to the 2-level DAC feedback in clock phase P2. Effectively, we are applying the mismatch signals $x_i \cdot (V_{ref}^+ - V_{ref}^-)$ (i = 1, 2, 3, 4) to the input of the incremental ADC. Usually this mismatch is a small DC input which allows the stable and accurate operation of the incremental ADC. Fig. 3-9 shows the conversion error as a function of the mismatch signal. After obtaining all mismatches x_i, the DAC nonlinearity errors at all output levels can be stored in the look-up table.

The results of calibration for the modulator of Fig. 3-9 are shown in Table 3-2. 0.5 % RMS DAC mismatches were assumed. MATLAB simulations with a sine-wave input (Fig. 3-10) show that the modified scheme gives much better results than the original Sarhang-Nejad scheme.

Table 3-2. DAC Mismatches and Estimations (Modified Sarhang-Nejad Calibration)

	DAC Mismatches $[x_1, x_2, x_3, x_4]^T$	**Estimation from Calibration** $[x_1, x_2, x_3, x_4]^T$
DAC1	0.0025 0.0035 0.0015 –0.0045	0.002503 0.003504 0.001501 –0.004504
DAC2	0.0055 –0.0045 –0.0065 –0.0035	0.005505 –0.004504 –0.006507 –0.003504

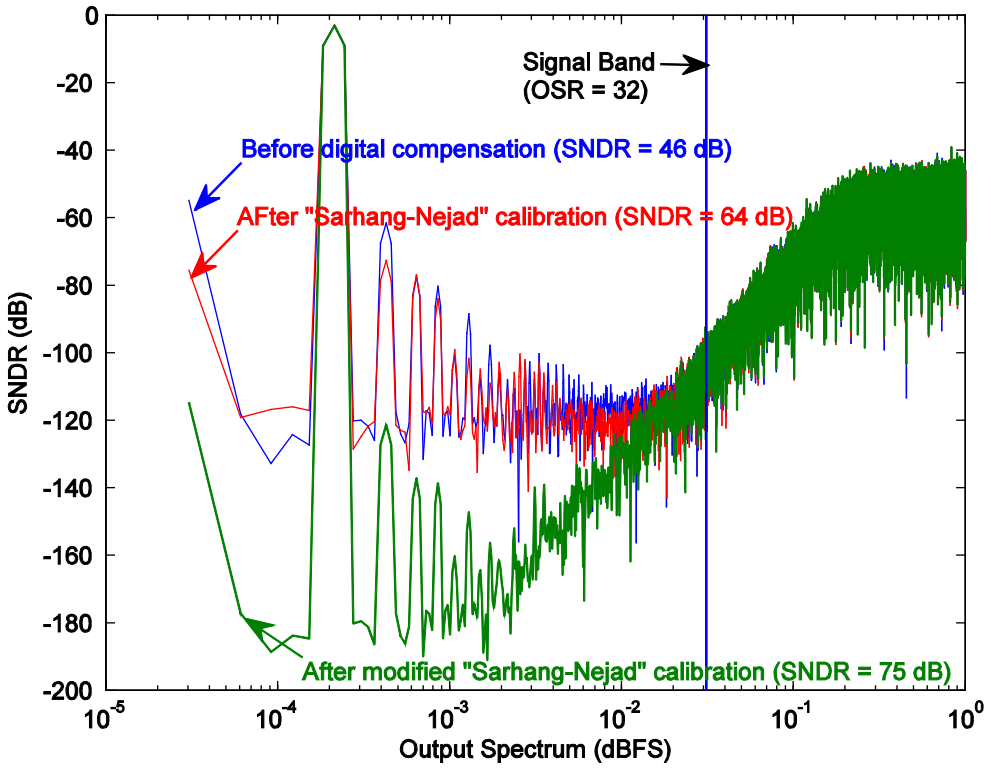


Fig. 3-10. Output spectra of a third-order double-sampling modulator with Sarhang-Nejad calibration, modified Sarhang Nejad calibration and without calibration.

Chapter 4 Circuit Design and Measurement Results

4.1 System Design

The design specifications of the incremental ADC are shown in Table 4- 1.

Table 4- 1. Design Specifications of the Incremental ADC

Specifications	Value
Number of channels (N)	20
Signal bandwidth (f_b)	3 kHz
Signal-to-noise ratio (SNR)	100 dB
Maximum output signal power (V_{max}^2)	1 V^2
Maximum sampling frequency (f_c)	30 MHz

The system design procedure is performed in the following steps:

Step 1. Calculate the maximum conversion time for one channel: $T_w = 1/(2Nf_b) = 8.33$ μs.

Step 2. Calculate the maximum clock cycles for one conversion: $M_{max} = T_w f_c = f_c/(2Nf_b) = 250$.

Step 3. A third order low distortion ΔΣ modulator with a 5-level quantizer [1-11] is designed with the ΔΣ toolbox for Matlab [4-1] (Fig. 4-1). The *NTF* of the modulator is $NTF = \frac{(z-1)^3}{(z-0.5701)(z^2-1.39z+0.6149)}$ and the *STF* is 1. The poles of the *NTF* is chosen so that the ΔΣ modulator is stable enough.

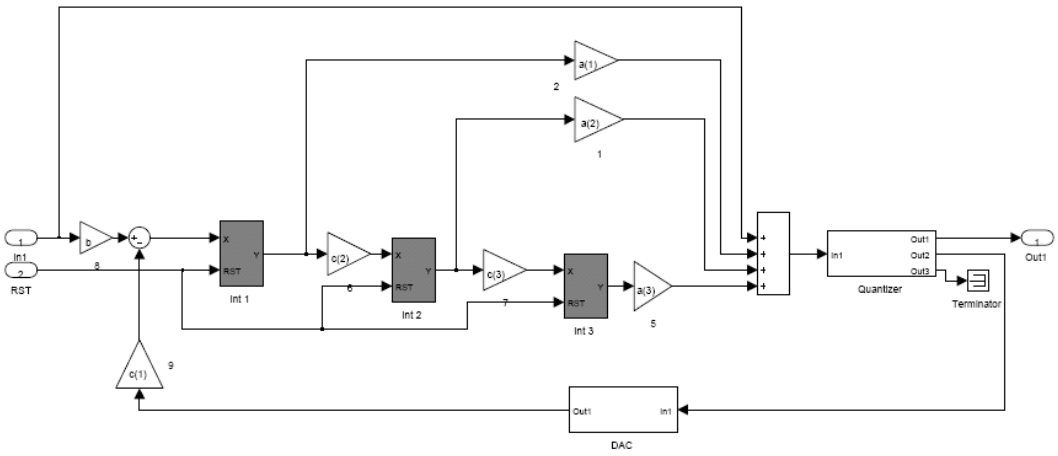


Fig. 4-1. The block diagram of the ΔΣ modulator.

Step 4. Determine the minimum value of MC_{in}. Since the SNR needs to be larger than 100 dB, the maximum total noise power is $P_{tot} = 10^{-10}$ V^2. If we allocate 90% of the noise budget to the thermal noise, the thermal noise must satisfy $\frac{\gamma kT\beta_{\max}}{MC_{in}} \le 0.9P_{tot}$, where $\beta_{\max} = 2$ and $\gamma = 5$ [2-1]. This gives $MC_{in} \ge 460\,\text{pF}$.

Step 5. Determine M and C_{in}. A series of optimizations for different M and C_{in} shows that larger M and smaller C_{in} gives better SNR. However, M is limited by the M_{max} calculated in *Step 2*. For our design, we chose M = 230 and C_{in} = 2 pF.

Step 6. Optimize the decimation filter by solving (2-14). The impulse response of the optimal decimation filter is shown in Fig. 4-2. The output

thermal noise and quantization noise are expected to be at −103 dBFS and −115 dBFS, respectively.

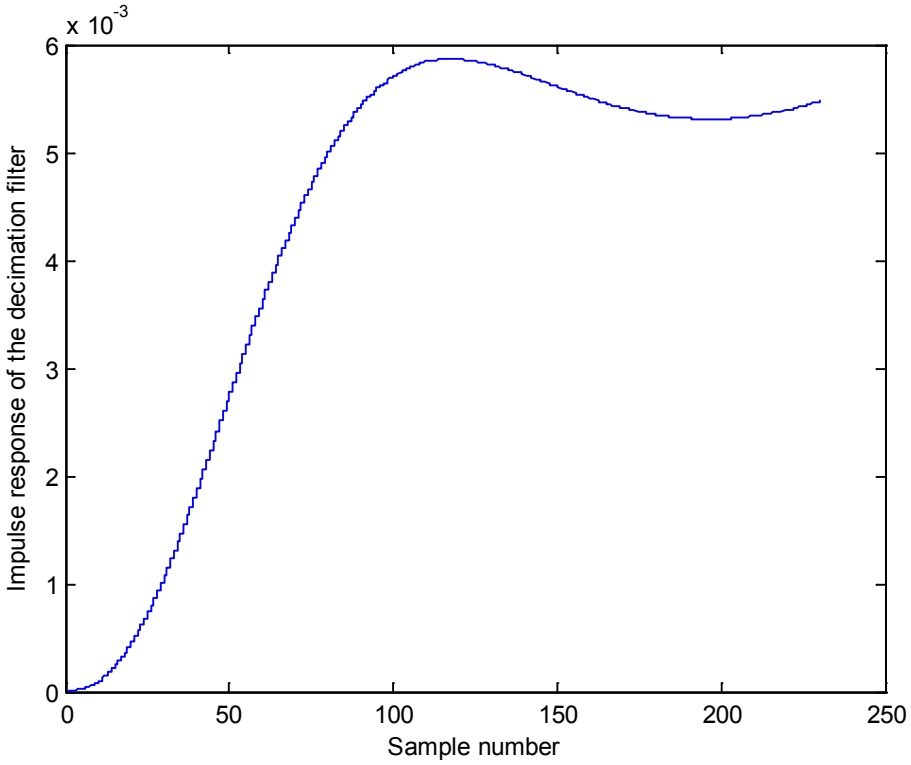


Fig. 4-2. The impulse response of the optimal decimation filter.

Matlab simulation shows that the output of the 3rd integrator exceeds the desirable opamp output swing (Fig. 4-3). So dynamic scaling is performed using the delta-sigma toolbox for Matlab [4-1].

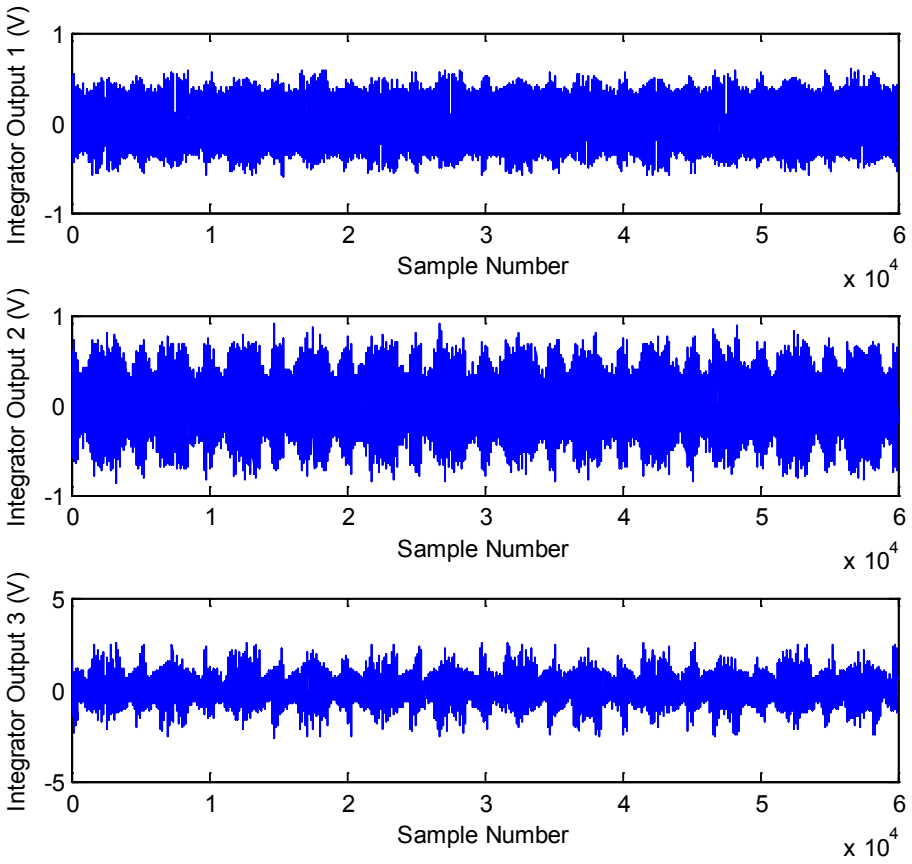


Fig. 4-3. The integrator outputs versus time for a 507 Hz, -1 dBFS sine wave input before dynamic scaling. The reference voltage is 1 V. The output of the third integrator exceeds the reference voltage.

The integrator outputs for the delta-sigma modulator after scaling are shown in Fig. 4-4. After the dynamic scaling, the coefficients of delta-sigma modulator are given as follows.

$$\mathbf{a} = [1.15, 0.9, 0.8]^T$$
$$\mathbf{b} = 0.9$$
$$\mathbf{c} = [0.9, 0.6, 0.2]^T.$$

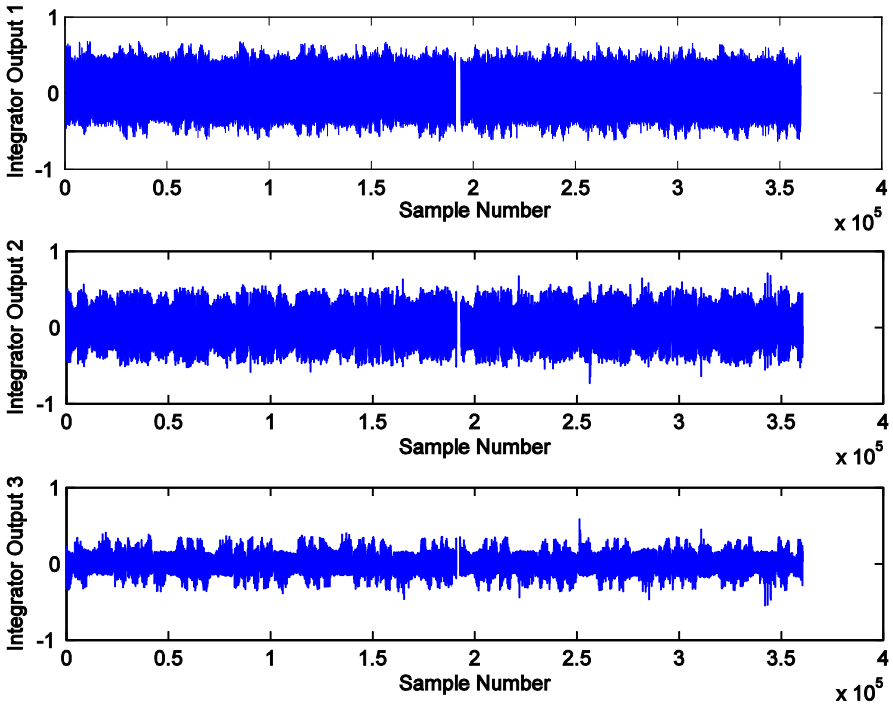


Fig. 4-4. The integrator outputs versus time for a 507 Hz, -1 dBFS sine wave after dynamic scaling. The reference voltage is 1 V. All integrator outputs are below 1 V.

Matlab simulations give the conversion error versus the DC input level for the incremental ADC (Fig. 4-5). The solid and dashed horizontal line shows the theoretical prediction for the thermal noise and the quantization noise using the analysis technique of section 2.3. The SQNR versus the sine wave input amplitude for one input frequency (507 Hz) is shown in Fig. 4-6.

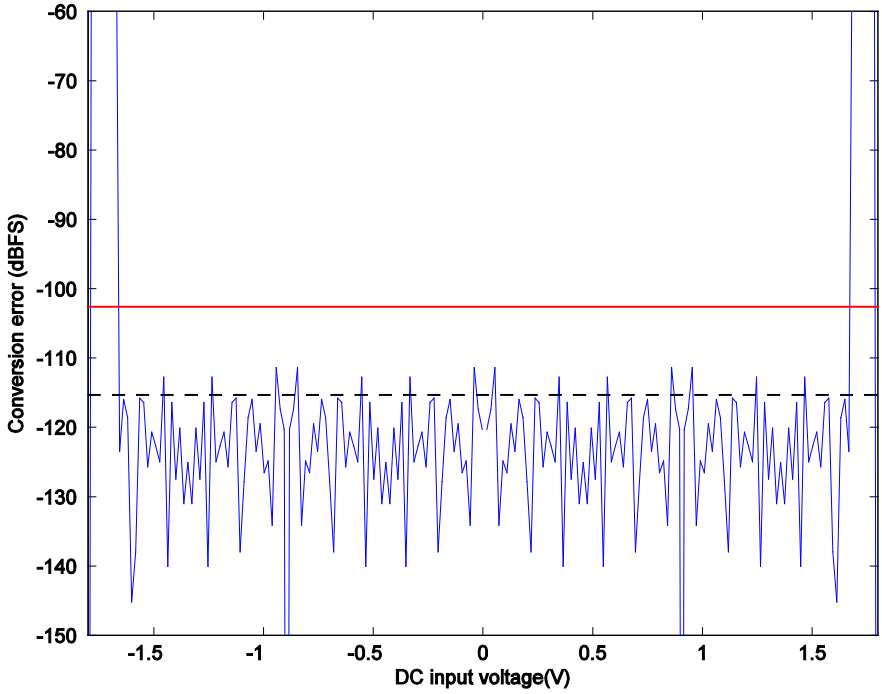


Fig. 4-5. The conversion error versus the DC input level (Matlab simulation).

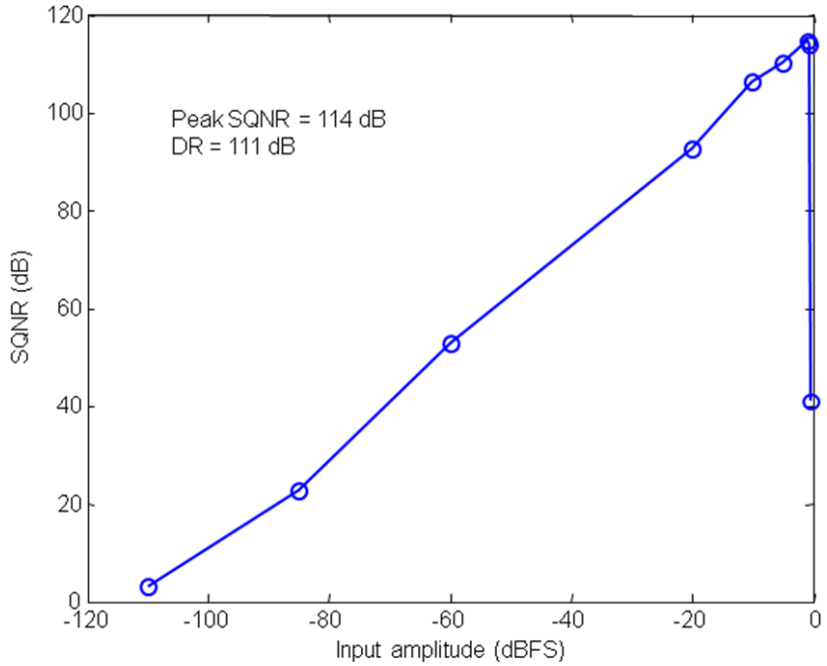


Fig. 4-6. SQNR versus input sine wave amplitude (Matlab simulation).

4.2 Top-Level Circuit Design

The top-level circuit of the incremental ADC is shown in Fig. 4-7. It consists of three integrators (INT1 to INT3), a passive adder, a 5-level quantizer pre-amplifier, comparator latches and DWA logic, output drivers, a clock generator and the biasing circuit. Double-sampling scheme is used to double the sampling frequency.

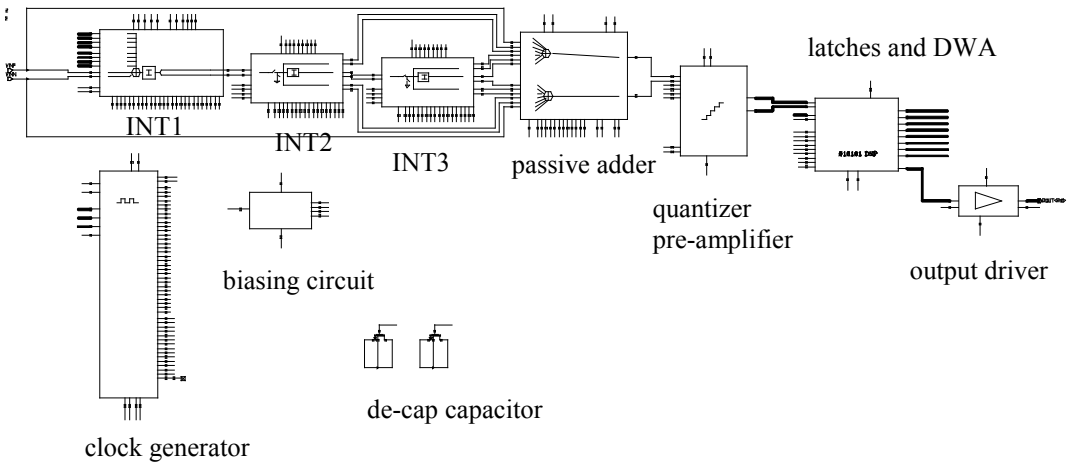


Fig. 4-7. The top-level circuit of the incremental ADC.

4.3 First Integrator

The first integrator (Fig. 4-8) consists of two input-and-DAC blocks (one for the positive side and the other for the negative side), an operational transconductance amplifier (OTA), chopping switches and reset switches.

A special fractal chopping sequence was used for better performance [1-4]. Instead of change the polarity of the OTA according to the sequence of (1, −1), we use the sequence of (1, −1, −1, 1, −1, 1, 1, −1).

The input common-mode voltage of the OTA is set to 0.3 V and the output common-mode voltage is set to 0.9 V. The chopping and reset switches at the OTA input side are implemented as NMOS transistors, while those at the OTA output side are implemented as transmission gates.

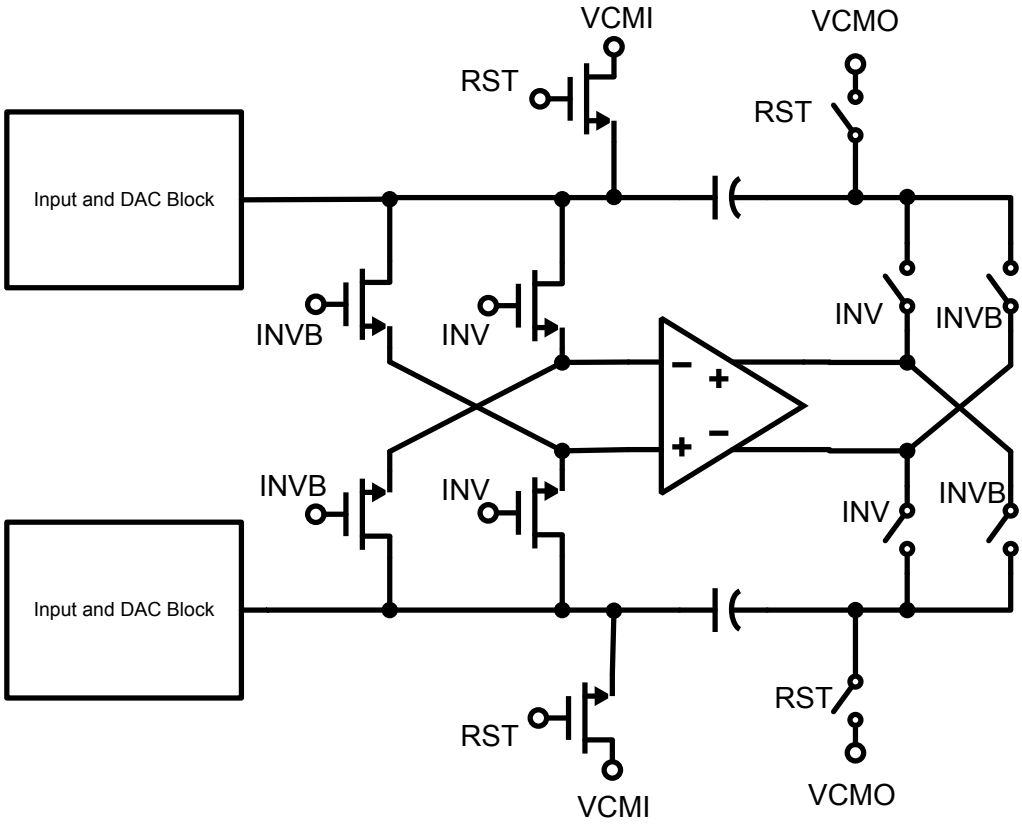


Fig. 4-8. The first integrator (INT1).

The input-and-DAC block is shown in Fig. 4-9. It consists of two input-and-DAC branches working in opposite clock phases (for double-sampling scheme) and a calibration capacitor branch. The input capacitors and feedback DAC capacitors are shared.

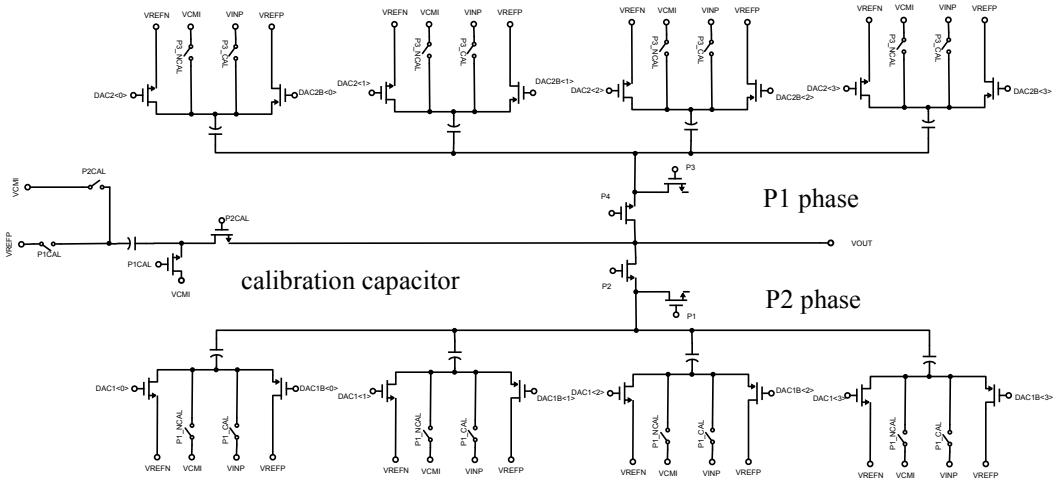


Fig. 4-9. The input-and-DAC block.

Because chopping is used, a gain-boosted OTA with high DC-gain (Fig. 4-10) was designed to suppress the quantization noise folding at the OTA virtual ground. Folded-cascode structure was chosen to accommodate low input common-mode voltage (0.3 V). Two transistors at the bottom (M25 and M26) work as the common-mode feedback (CMFB) circuit [4-2]. Two auxiliary amplifiers (Fig. 4-11) are used to boost the DC gain. They work in the triode region and sense the common-mode voltage of the OTA output.

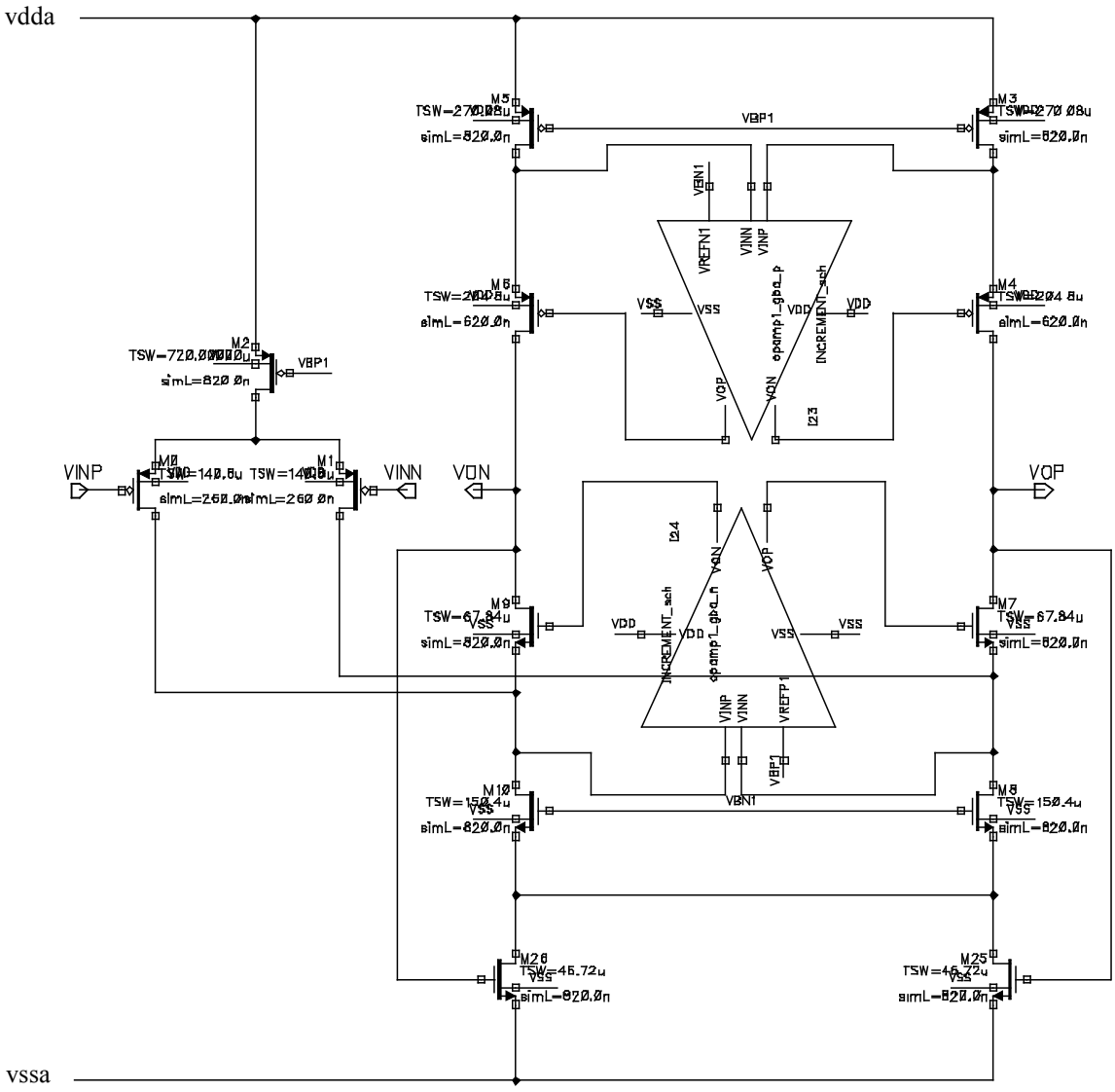
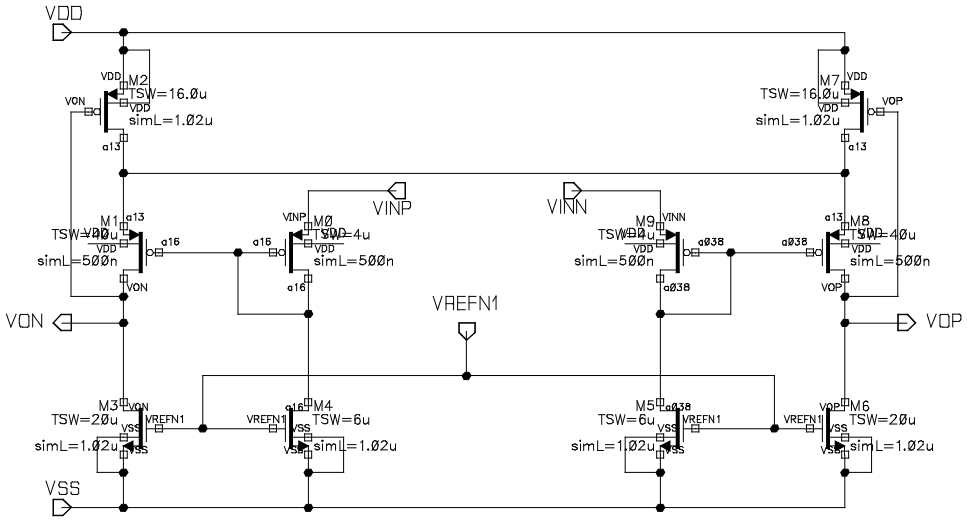
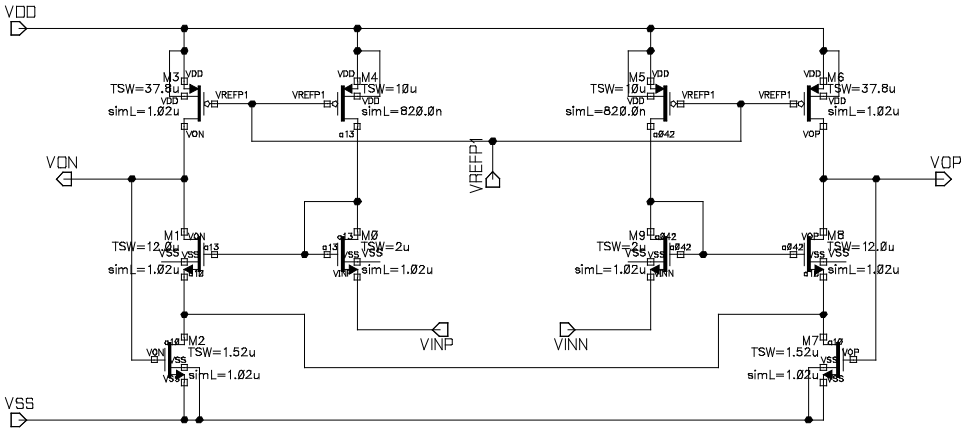


Fig. 4-10. The gain-boosted folded-cascode OTA in the 1st integrator.



a)



b)

Fig. 4-11. The auxiliary amplifier for gain boosting at a) PMOS side and b) NMOS side.

In order to get better linearity, bootstrapped switches [4-3] are used to sample the input signal. As shown in Fig. 4-12, the gate voltage of the main switch (M1) is raised to $V_{in} + V_{dd}$ to keep V_{GS} constant (V_{dd}).

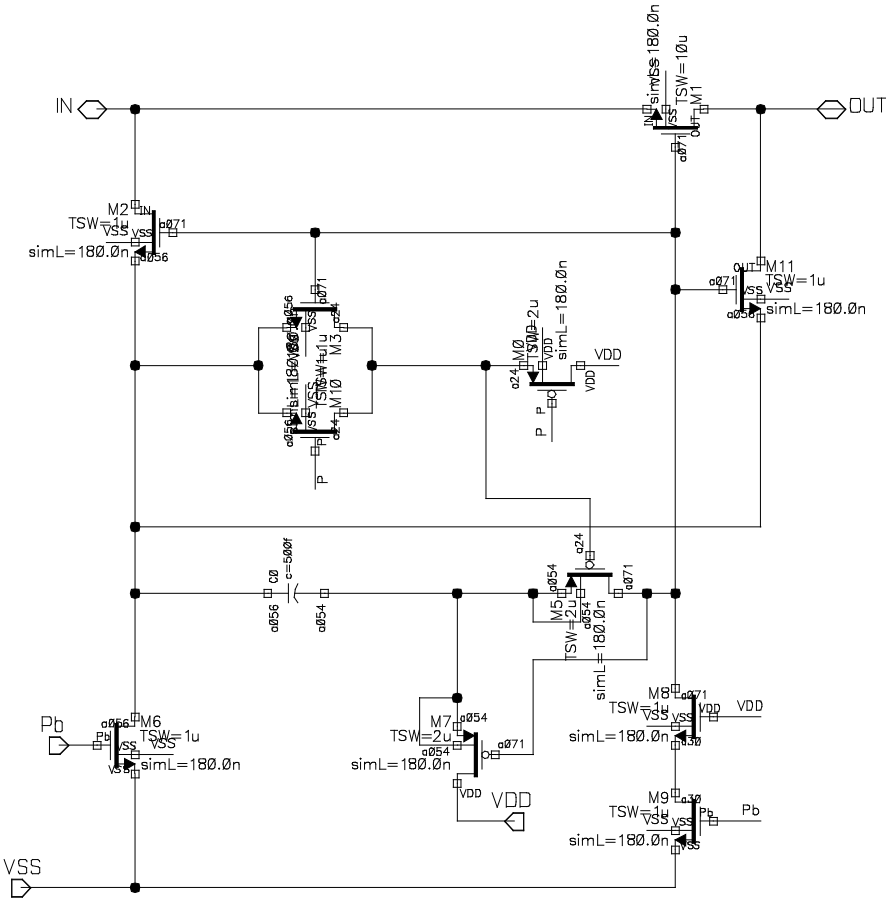


Fig. 4-12. The bootstrapped switches used to sample the input signal.

4.4 Second and Third Integrators

The circuitw of the second and the third integrators are shown in Fig. 4-13. There are two input branches operating in opposite clock phases (P1 and P2) due to the double-sampling scheme. Chopping is used to suppress the 1/*f* noise of the OTA. Folded-cascode OTAs (Fig. 4-14) are used in the integrators.

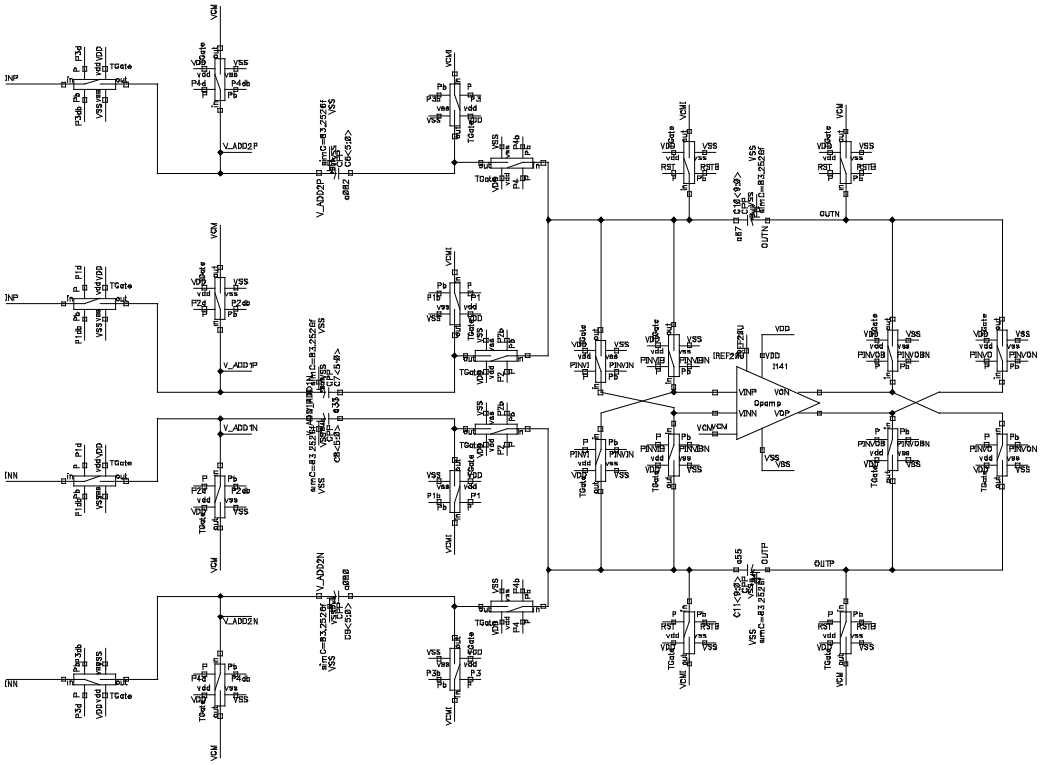


Fig. 4-13. The second and the third integrators.

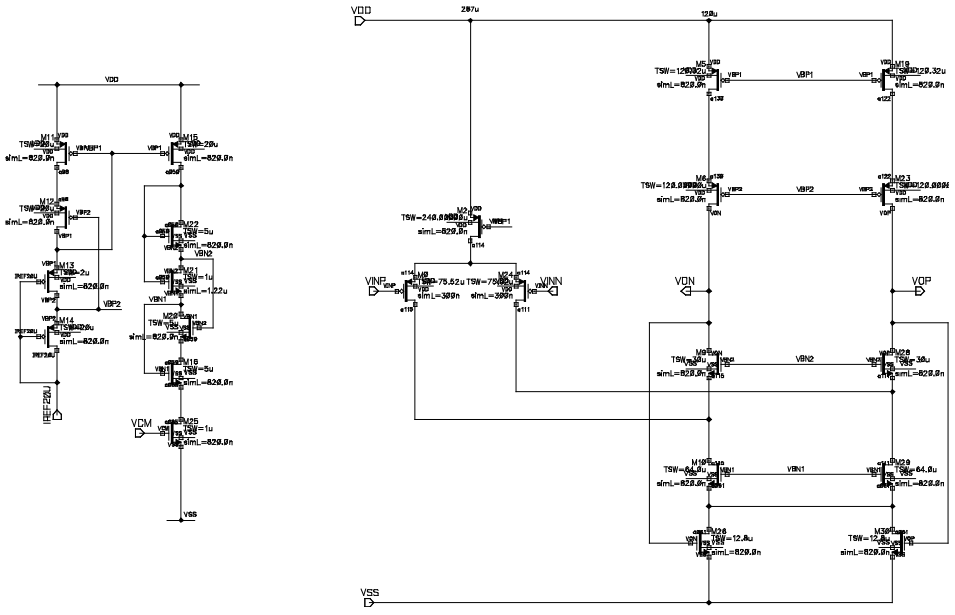


Fig. 4-14. The OTAs in the second and the third integrators.

4.5 Passive Adder

A passive adder (Fig. 4-15) is used to add up the input signal and the outputs of three integrators.

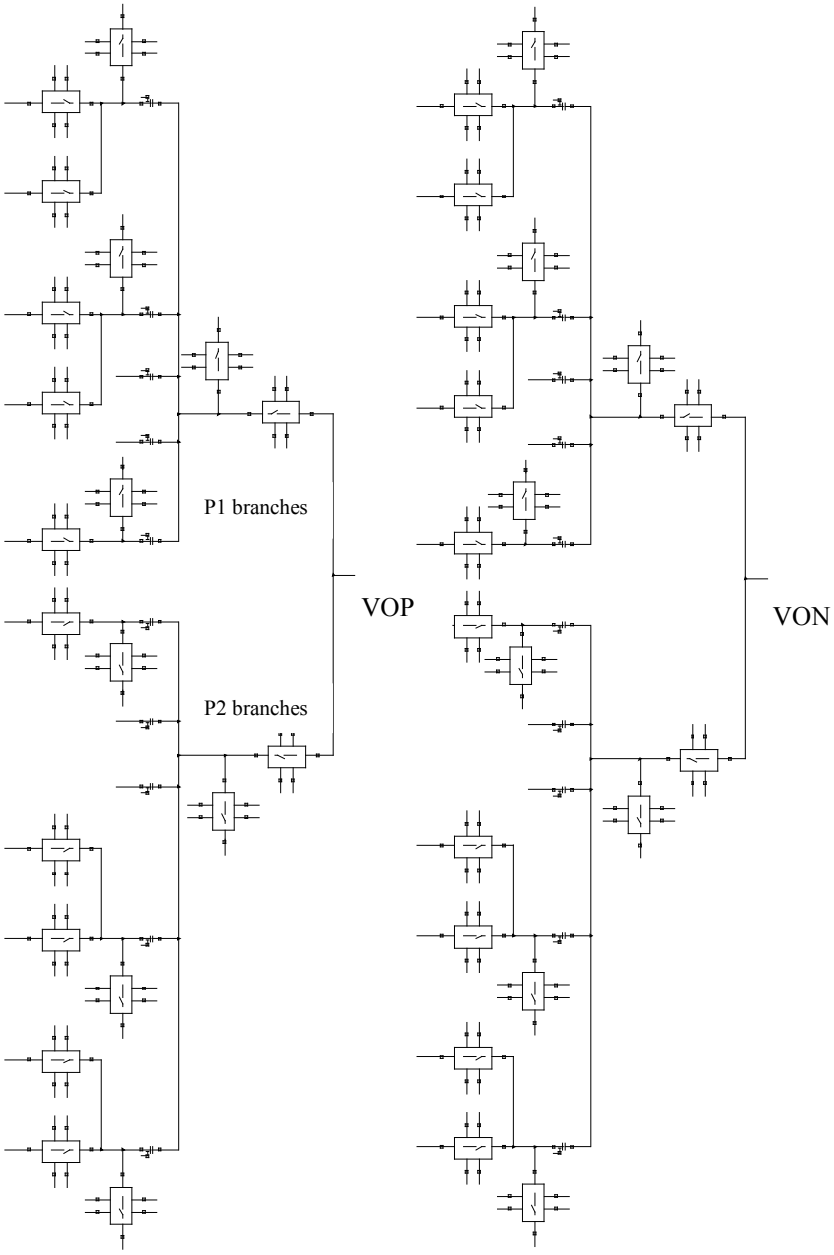


Fig. 4-15. The passive adder.

Two branches operating in opposite clock phases (P1 and P2) are used due to the double-sampling scheme. The use of a passive adder instead of an active adder saves power. However, the reference voltage in the following quantizer needs to be scaled down, and extra care is needed for the effect of the capacitance loading of the adder.

4.6 Quantizer Pre-amplifier

The 5-level quantizer pre-amplifier (Fig. 4-16) consists of a resistor string and four comparator pre-amplifiers. The total resistance of the each resistor string branch is 15 kΩ.

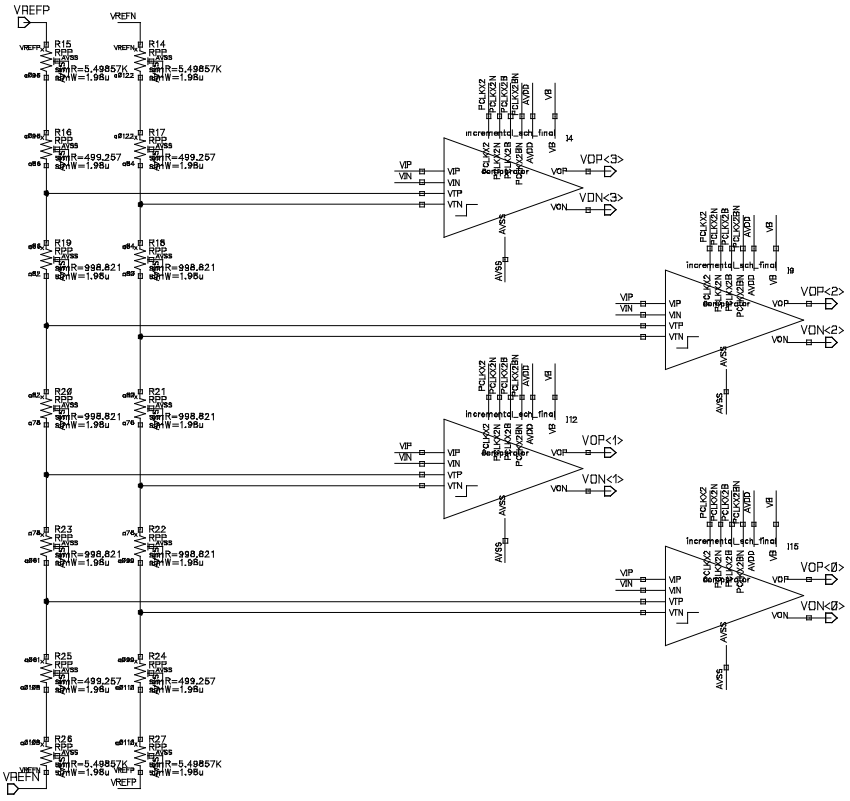


Fig. 4-16. The 5-level quantizer.

The comparator pre-amplifier relaxes the requirement on the offset of the comparator latch. The offset of the pre-amplifier itself is canceled by input offset storage (IOS) technique [4-4]. In the offset sampling phase, the comparator pre-amplifier (Fig. 4-17) is connected as a unity-gain buffer. The offset-cancelling capacitor samples $V_{comp} + V_{OS}$, where V_{comp} is the comparison voltage and V_{OS} is the offset voltage of the pre-amplifier. In the comparison phase, the pre-amplifier works in open-loop and amplifies the offset-compensated voltage $V_{in} - (V_{comp} + V_{OS}) + V_{OS} = V_{in} - V_{comp}$.

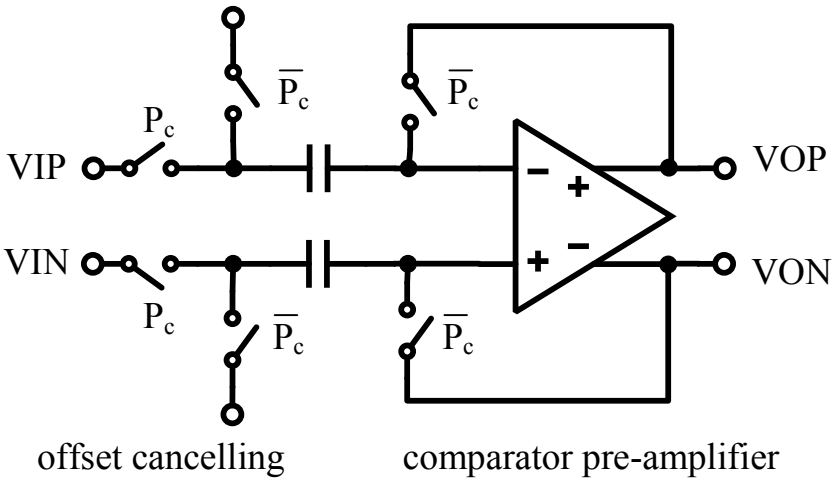
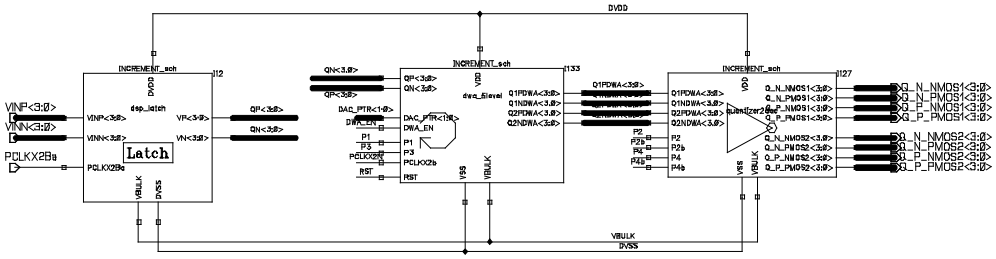


Fig. 4-17. Comparator pre-amplifier.

4.7 Latches and DWA Logics

As shown in Fig. 4-18, the latches take the output of comparator pre-amplifiers and latch the comparison result (thermometer quantizer output).



latches DWA logics buffers

Fig. 4-18. Latches and DWA logics.

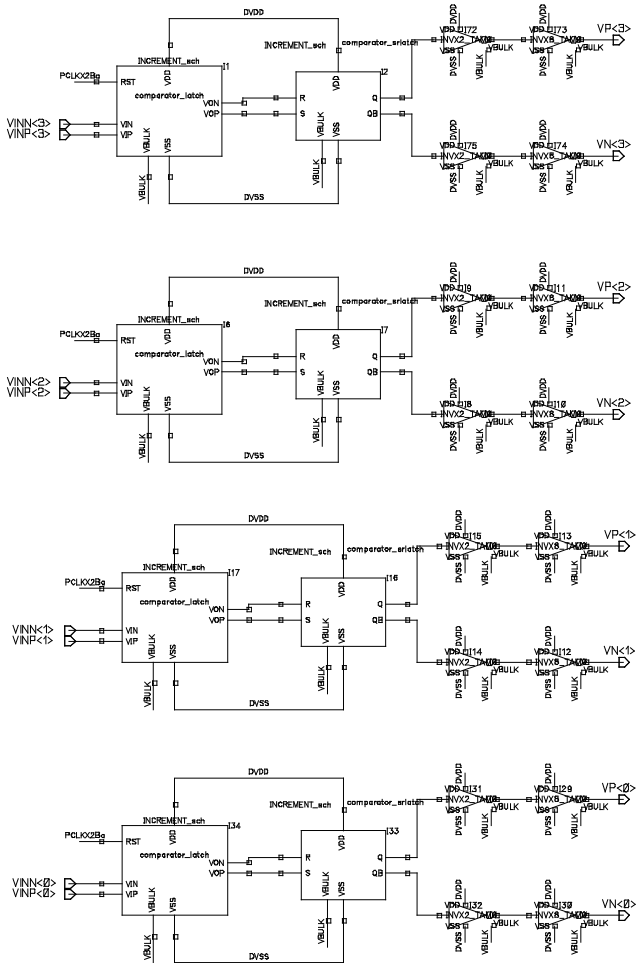


Fig. 4-19. Comparator latches and RS latches.

The latch block consists of four comparator latches followed by four RS latches (Fig. 4-19). When the RST signal goes low, the comparator latch (Fig. 4-20) generates the comparison result, and the RS latch (Fig. 4-21) holds the result until the next falling edge of RST.

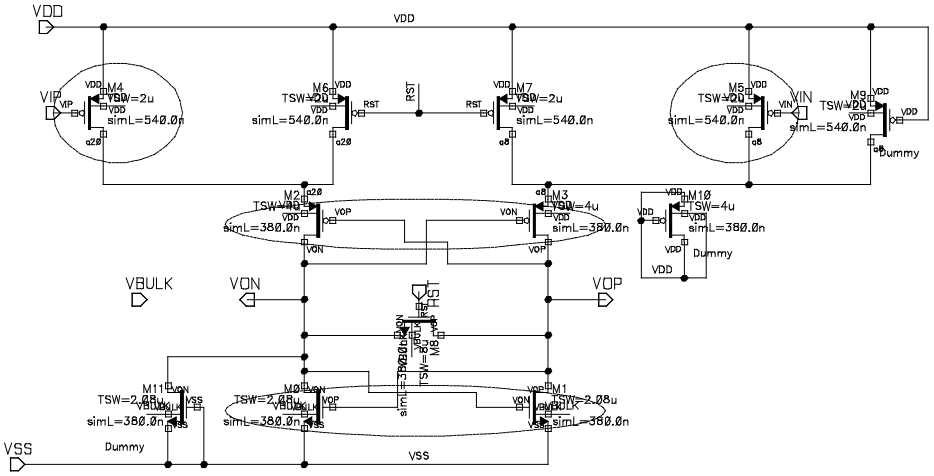


Fig. 4-20. The comparator latch.

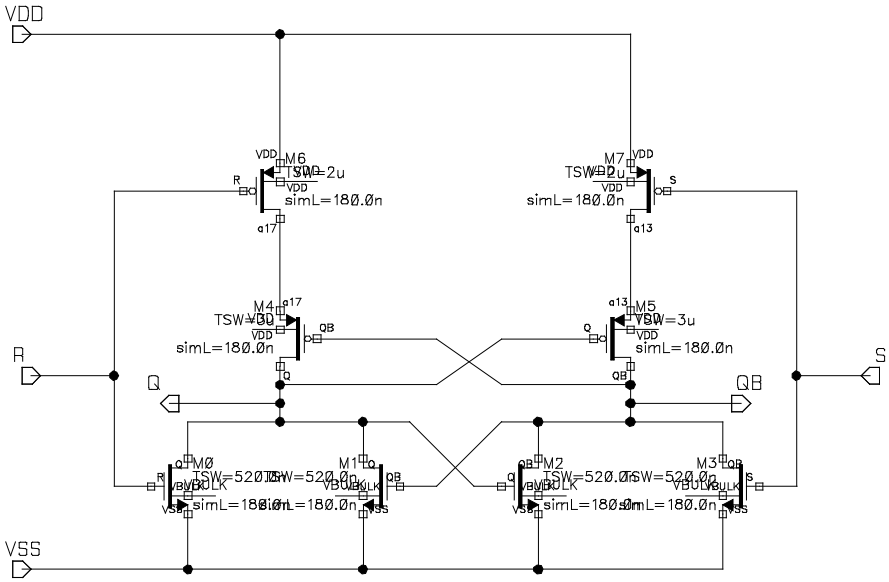


Fig. 4-21. The RS latch.

As shown in Fig. 4-22, the DWA circuit consists of a DWA pointer register, a MUX and a log-shifter. Two separate DWA pointer registers are used for the two opposite phases in double-sampling scheme. The MUX is used to select the source of DWA pointer according to the operation modes. In the digital calibration and compensation mode, the pointer comes from two pins of the chip (DACPTR1 and DACPTR0). In DWA mode, the pointer comes from the register in DWA logics.

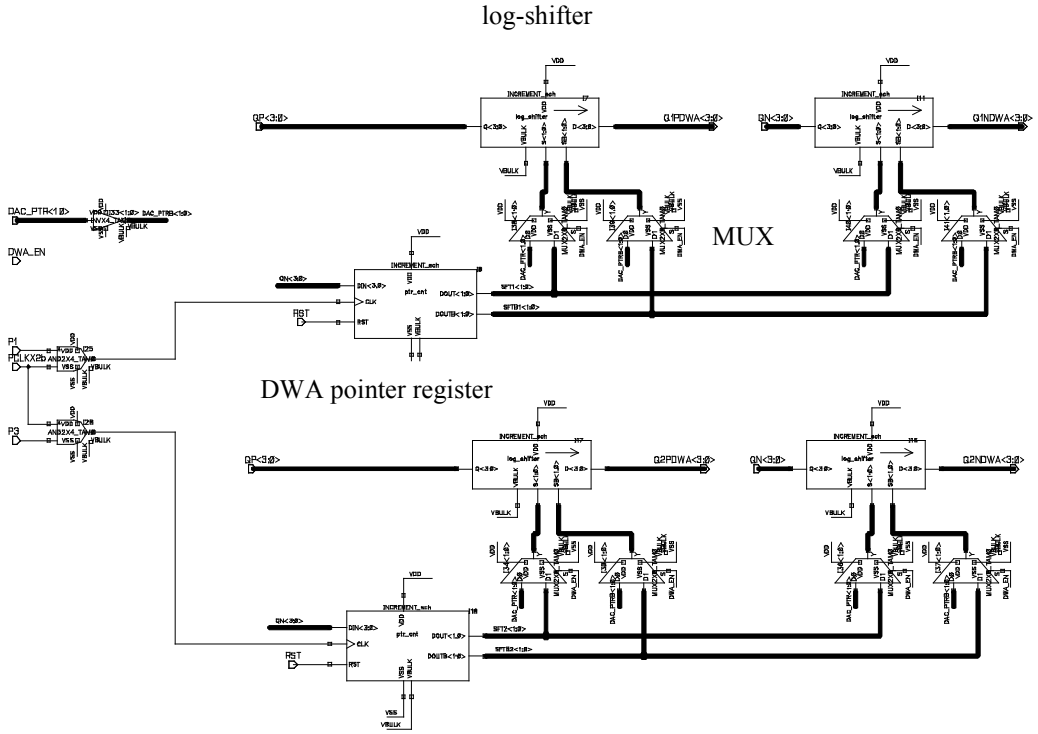


Fig. 4-22. The DWA circuit.

The DWA pointer register is made of an adder and several D flip-flops. According to the DWA algorithm, the next pointer value is the sum of the current value and the current modulator output.

The log-shifter (Fig. 4-23) shifts the thermometer modulator output according to the DWA pointer.

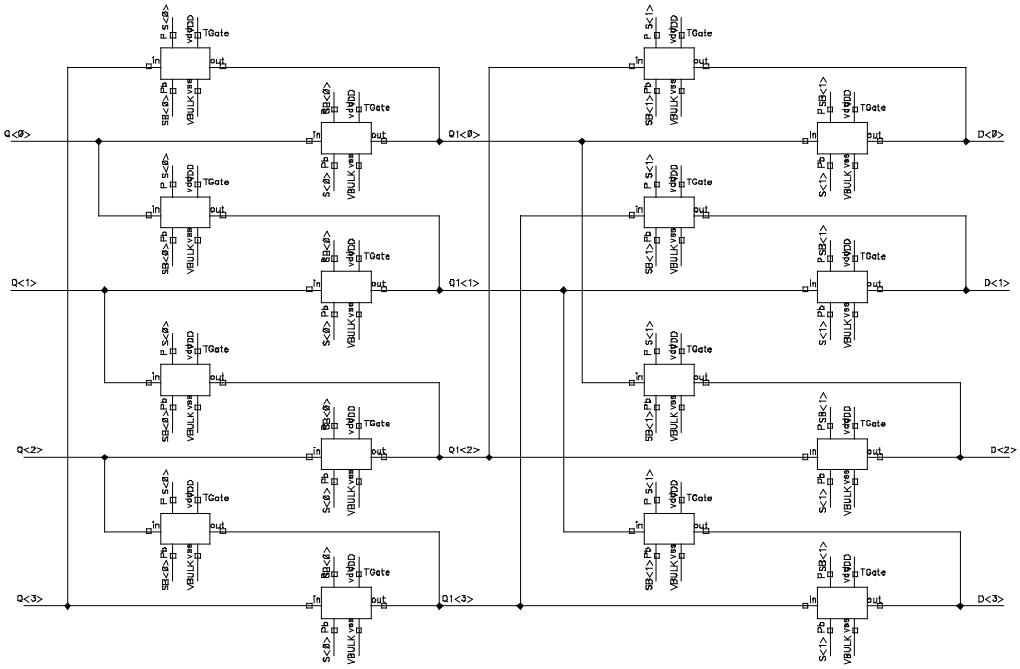


Fig. 4-23. The log-shifter.

4.8 Clock Generators

The clock generator (Fig. 4-24) provides the non-overlapping clock for the incremental ADC. It also provides other control signals, such as reset signals, chopping control signals and comparator clocking.

The off-chip clock is first divided by 2 in frequency by a D flip-flop. The frequency-divided clock is then used to generate the non-overlapping clock Q1 and Q2. The single/double sampling control generates four clock signal P1, P2, P3 and P4 from Q1 and Q2, according to the control signal DS_CTL. The clock signals P1 and P2 are used for the switched-capacitor branches in one double-sampling phase,

while the clock signals P3 and P4 are used for the other. The relationship between the DS_CTL and P1 ~ P4 clocks is shown in Table 4-2.

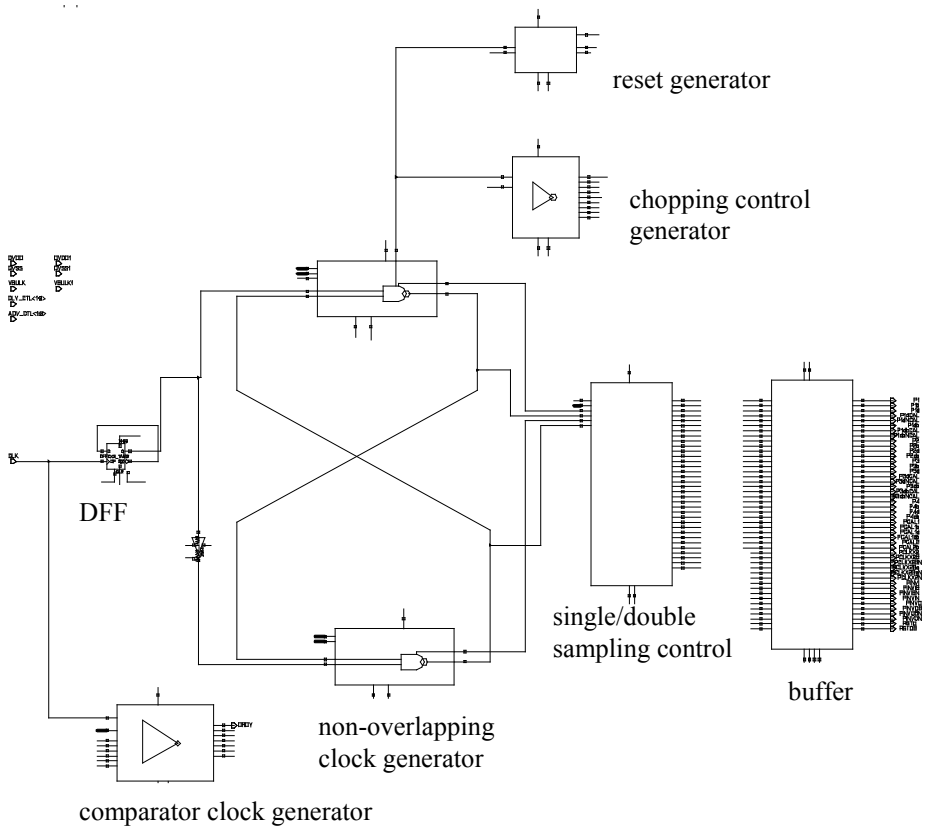


Fig. 4-24. The clock generator.

Table 4-2. Clock Generation Table

DS_CTL	P1	P2	P3	P4
00 (no use)	0	0	0	0
01 (single-sampling 1)	Q1	Q2	0	0
10 (single-sampling 2)	0	0	Q1	Q2
11 (double-sampling)	Q1	Q2	Q2	Q1

4.9 Measurement Results

The chip was fabricated in a double-poly/6-metal 0.18 μm CMOS process. The photo of the test board is shown in Fig. 4-25.

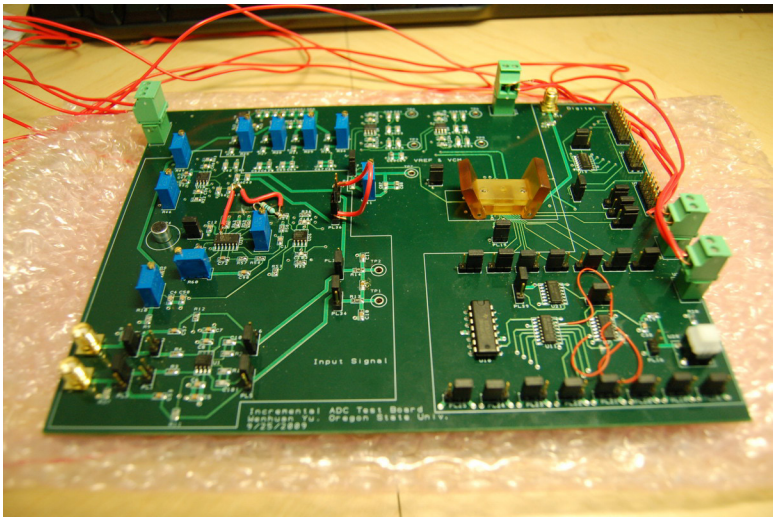


Fig. 4-25. The test board of the incremental ADC.

When the modulator runs as a continuously-running single-sampling ΔΣ modulator, the spectrum of the modulator output is as shown in Fig. 4-26. For a −2.5 dBFS sine wave input, the modulator achieves 86.8 dB SNR and 83.0 dB SNDR for an OSR of 230, running at a sampling frequency of 10 MHz. The total power consumption is 6.6 mW (3.8 mW for analog and 2.8 mW for digital).

The spectrum of the incremental ADC output (after decimation) with the optimal decimation filter and the traditional cascaded integrator decimation filter is shown in Fig. 4-27. The reset period of the incremental ADC is M = 230 clock periods. For a −3.4 dBFS sine wave input, it achieves 83.7 dB SNR and 81.5 dB

SNDR with the optimal decimation filter, and 82.3 dB SNR and 79.7 dB SNDR with the cascaded integrator decimation filter, running at a sampling frequency of 10 MHz. The total power consumption is 6.6 mW (3.8 mW for analog and 2.8 mW for digital).

Fig. 4-28 shows the effect of the equation-solving digital calibration and compensation technique (section 3.2). Based on the results of four incremental calibration conversions running in the calibration mode, the mismatch of DAC1 is calculated to be $[x_1, x_2, x_3, x_4]^T = [-0.0204, -0.0136, -0.0175, -0.0072]^T$. With the mismatch information obtained, a look-up table is constructed to digitally compensate the modulator output. As shown in Fig. 4-28, the modulator with digital compensation achieves 80.1 dB SNR and 73.4 dB SNDR, while the modulator without digital compensation achieves 71.3 dB SNR and 63.6 dB SNDR. Around 10 dB improvement is obtained by digital compensation and calibration.

The die micrograph of the incremental ADC is shown in Fig. 4-29. The performances are summarized in Table 4- 3.

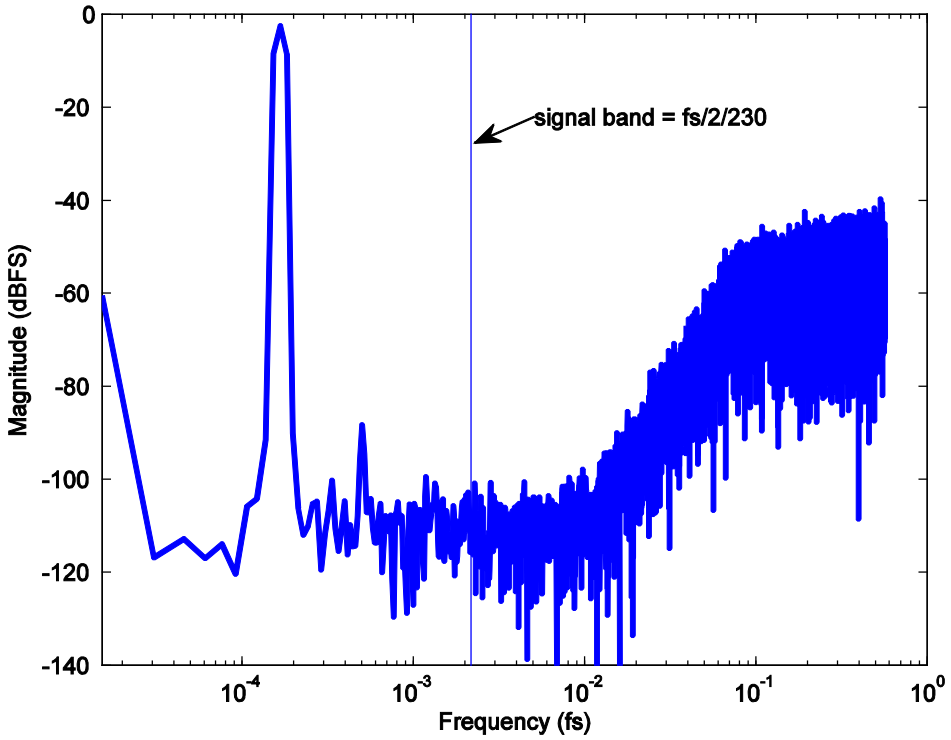


Fig. 4-26. The spectrum of the modulator output when the modulator is running as a conventional continuously-running single sampling ΔΣ modulator for a−2.5 dBFS sine wave input.

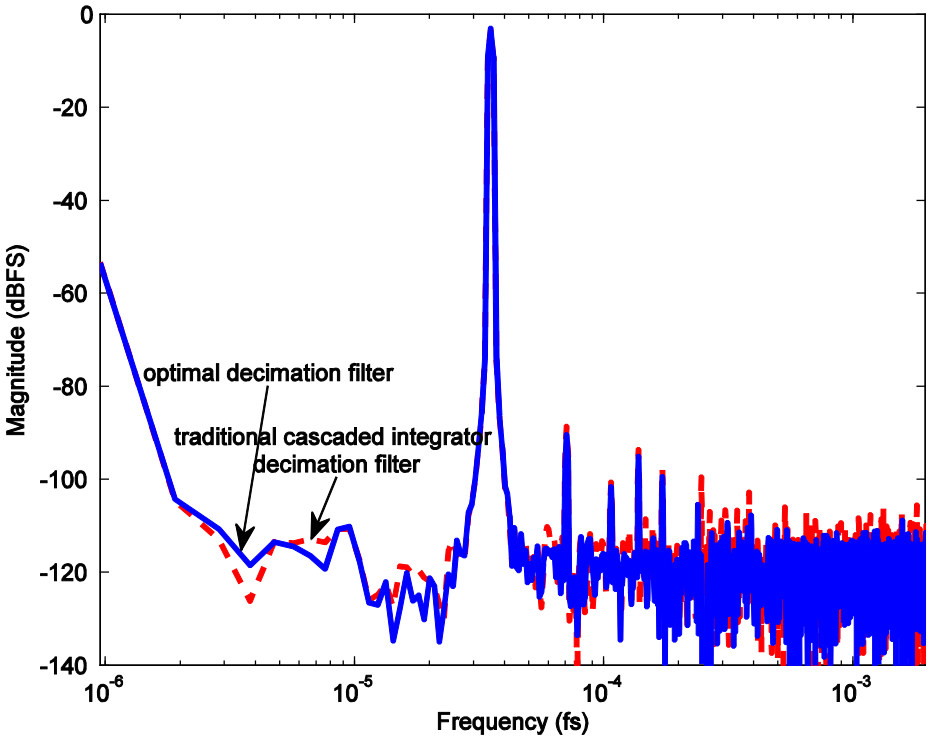


Fig. 4-27. The spectrum of the incremental ADC output (after decimation) with the optimal decimation filter (solid line) and the traditional cascaded integrator decimation filter (dashed line) for a −3.4 dBFS sine wave input.

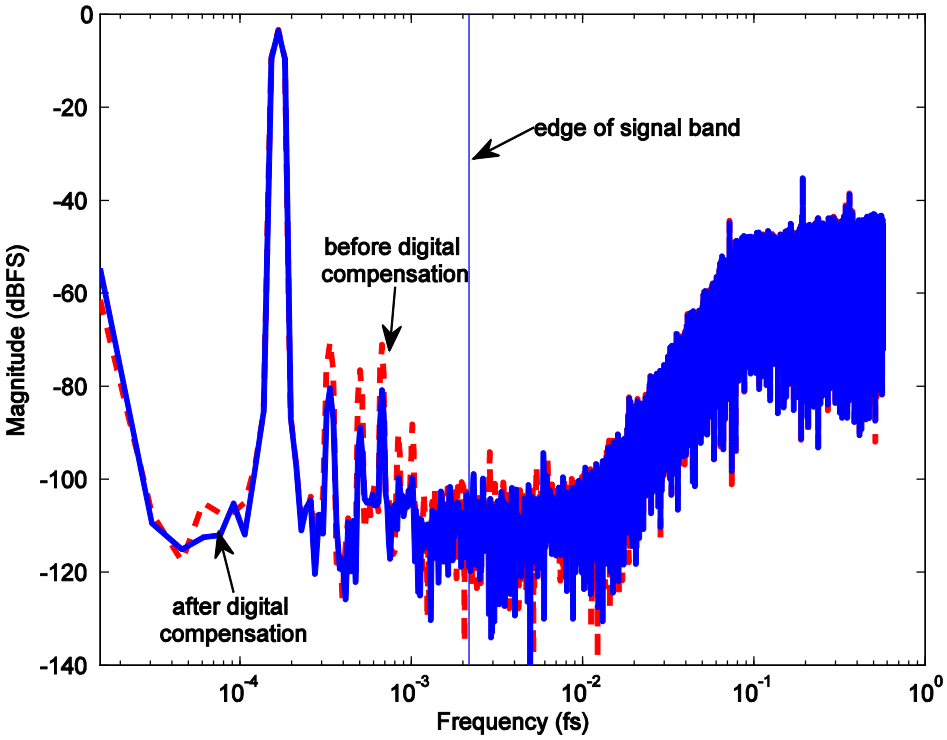


Fig. 4-28. The spectrum of the modulator output when the modulator is running as a conventional continuously-running single sampling ΔΣ modulator before (dashed line) and after digital compensation (solid line). The DWA is turned off.

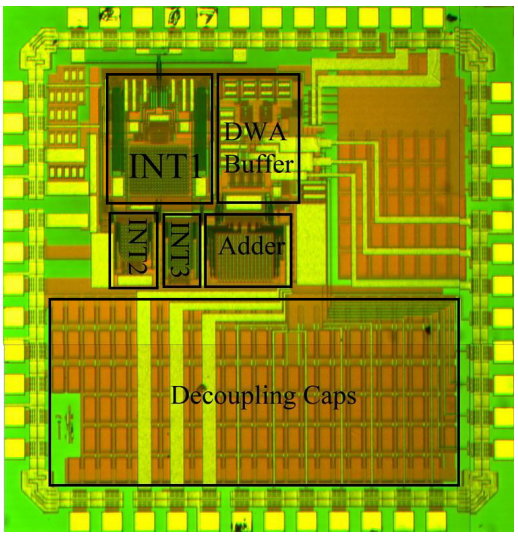


Fig. 4-29. Die micrograph of the incremental ADC.

Table 4- 3. Measured Performance of the Incremental ADC

Performance	Value
Sampling Frequency	10 MHz
Signal Bandwidth	21.7 kHz
Oversampling Ratio	230
Peak SNR	86.8 dB (ΔΣ), 83.7 dB (incremental)
Peak SNDR	83.0 dB (ΔΣ), 81.5 dB (incremental)
Input Range	2 Vpp (differential)
Power Consumption	3.8 mW (analog), 2.8 mW (digital)
Power Supply	1.8 V
Process	0.18 μm CMOS
Chip Area	6.25 mm^2 (core area: 1.2 mm^2)

Chapter 5 Design Techniques for Low-Power ADCs

5.1 Two-Step Split-Junction SAR ADC

Successive-approximation register analog-to-digital converters (SAR ADCs) are good candidates for low-power applications [5-1]. Recently, Park and Lee described a split-junction structure which drastically reduced the dynamic power dissipation of the SAR capacitor array compared to earlier realizations [5-2]. We propose a new scheme that further reduces both power consumption and capacitor area by a large factor, by performing the conversion in two phases using two smaller split-junction arrays (SJAs).

The proposed structure is illustrated in Fig. 5-1 for a 6-bit (N = 6) ADC. It contains two 3-bit (in general, N/2 bit) SJAs and a comparator. Let the input correspond to the digital word 101011. Initially, the input signal is sampled on all the capacitors in the two arrays (Fig. 5-1). Next, a coarse quantization is performed to generate the first N/2 = 3 bits using only the DAC1. During the coarse quantization, switch Si (which isolates the two DACs) will remain open.

Fig. 5-2 shows the circuit state when the 3rd bit is being generated. As soon as the 3rd bit is determined, DAC2 generates a voltage which is $V_{ref} / 2^{N/2} = V_{ref} / 8$ higher (lower) than the output of DAC1 if the 3rd bit is 1 (0). This is done by changing the bottom-plate voltages in the C/C block of DAC2, while setting all the other bottom-plate voltages in DAC2 to be the same as those in DAC1. In this

example, since the 3rd bit is 1, the output voltage of DAC2 will generate a voltage V_{ref} / 8 higher than the $3V_{ref}$ / 4 output of DAC1. This operation requires an extra clock phase, and thus N + 1 clock phases are needed for an N-bit conversion. When the coarse quantization is finished, all switches will be opened to prepare for the fine quantization phase.

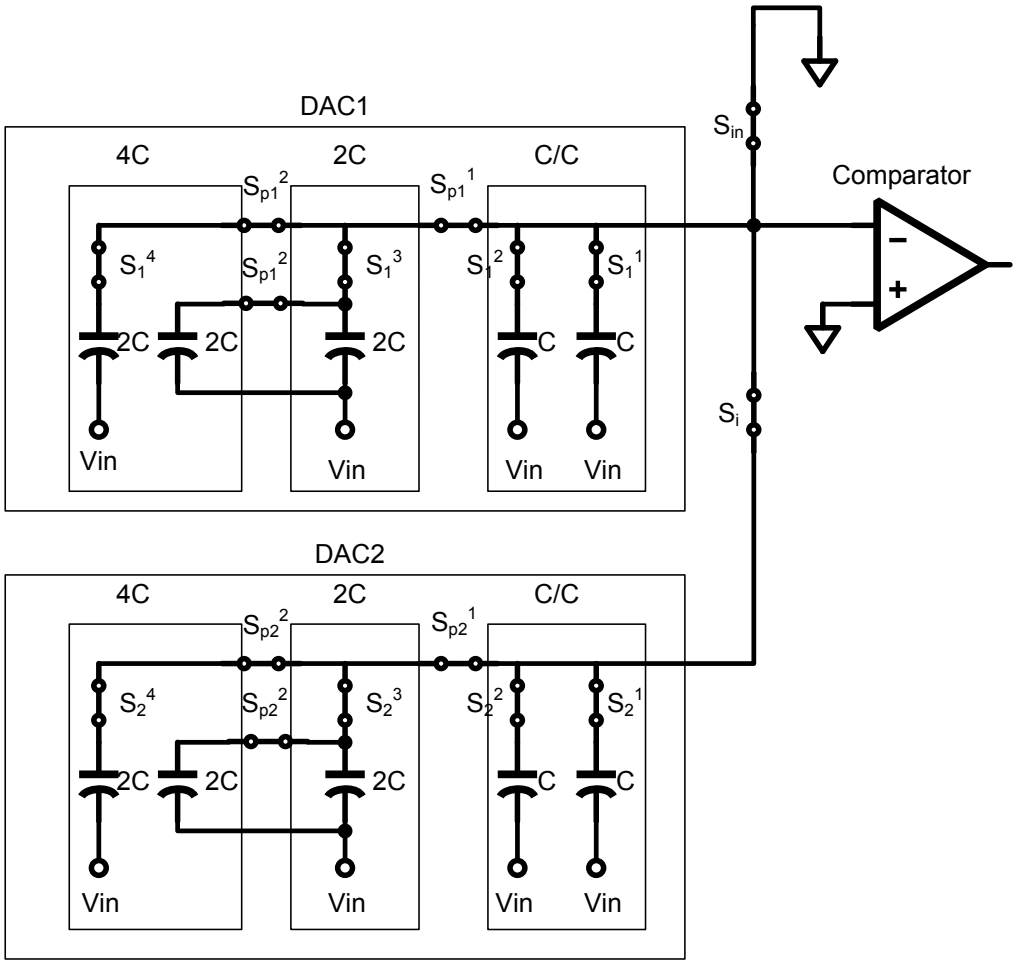


Fig. 5-1. The input sampling phase for a 6-bit SAR ADC.

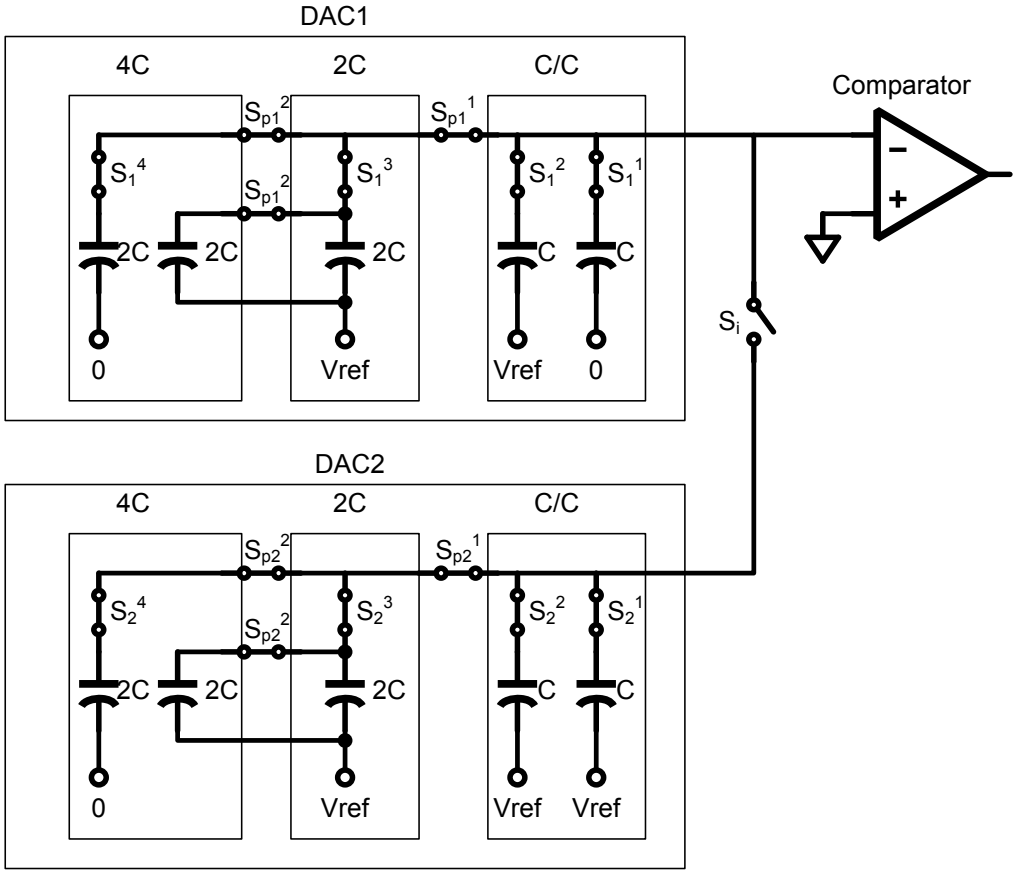


Fig. 5-2. Coarse quantization of the 3rd bit (DAC output 101) using the split-junction scheme.

After the coarse quantization is complete, the voltages at the outputs of DAC1 and DAC2 are upper and lower bounds of the input voltage. Switch Si closes, and stays closed during the fine quantization. As illustrated in Fig. 5-3 to Fig. 5-5, the capacitors in DAC1 and DAC2 are then connected in parallel, section by section, to generate comparison voltages of finer and finer resolution, by charge sharing.

During the fine quantization, the bottom-plate voltages are kept unchanged, and only the switches connected to the top plates are operated. First, switches S_1^1 and S_2^1 are closed to determine the 4th bit. After that, two larger identical capacitor blocks are added into the capacitor array for every new bit. In this example, first the two 2C blocks will be added to the capacitor array to generate the reference voltage for determining the 5th bit, and then the two 4C blocks will be for finding the 6th bit.

Each section has one switch inside (except the C/C blocks) connected with the top plate of 2C, which is controlled by the previous bit. The states of the two corresponding switches in the two identical sections in DAC1 and DAC2 are complementary when these blocks are appended to the capacitor array. The switch connecting the 2C capacitor in the DAC holding the higher voltage will be closed if the previous bit is 1, otherwise the switch connecting the 2C capacitor in the DAC holding the lower voltage will be closed. In this example, the output voltage of DAC2 is higher than that of DAC1 after the 3rd bit was found. Since the 4th bit is 0, when the two 2C blocks are connected to the capacitor array, S_1^3 is closed while S_2^3 is opened. When the two 4C blocks are added to the capacitor array, S_2^4 is closed and S_1^4 is opened, since the 5th bit is 1.

A digital controller is needed to control the switches of the ADC.

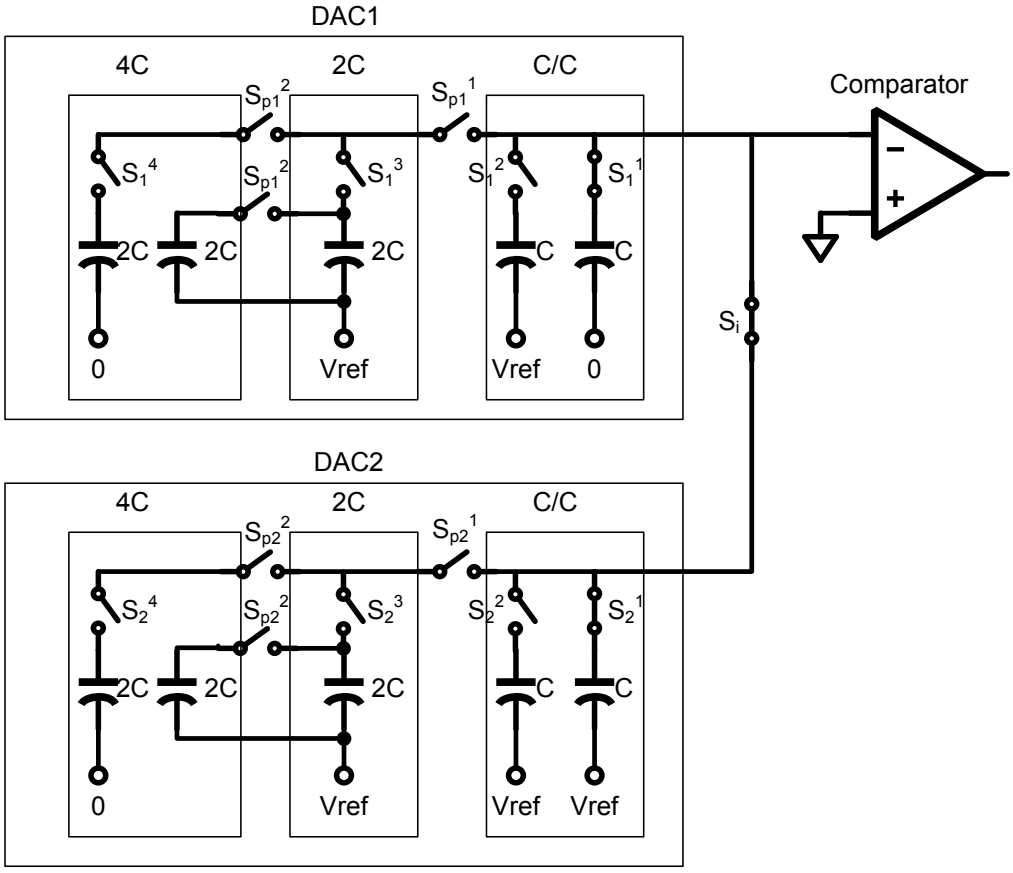


Fig. 5-3. Fine quantization of the 4th bit (DAC output 1011) using the proposed scheme.

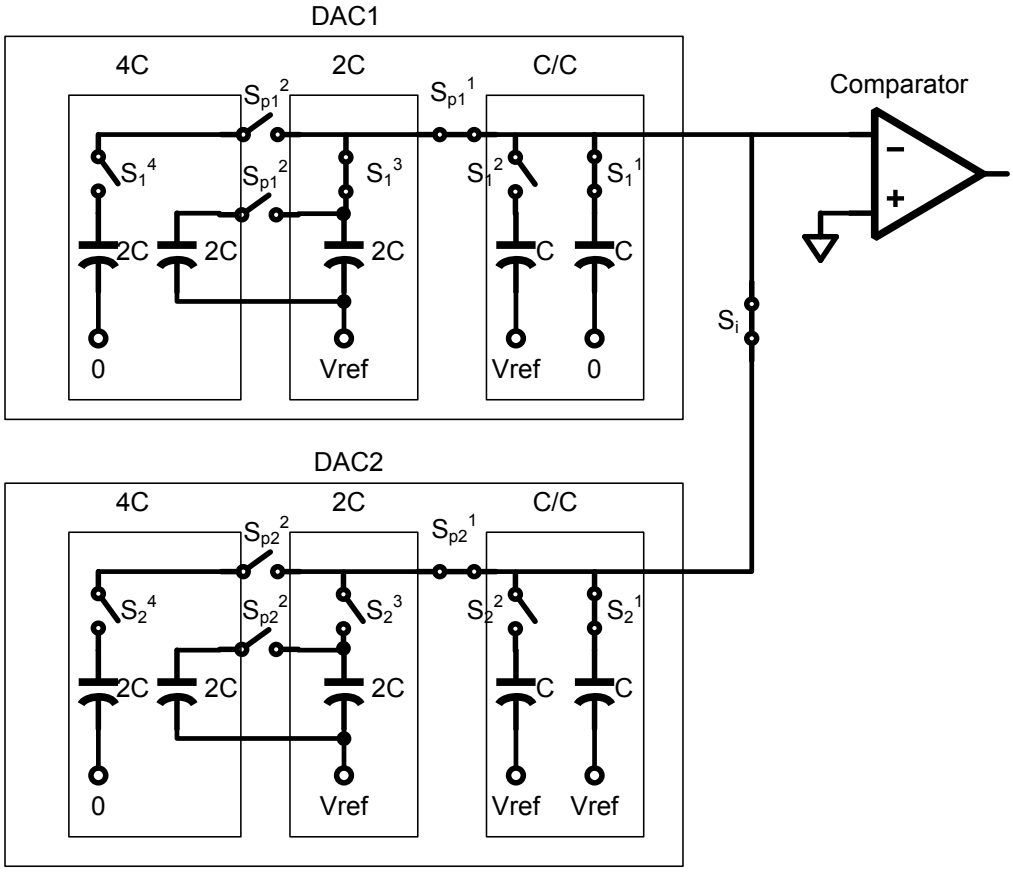


Fig. 5-4. Fine quantization of the 5th bit (DAC output 10101) using the proposed scheme.

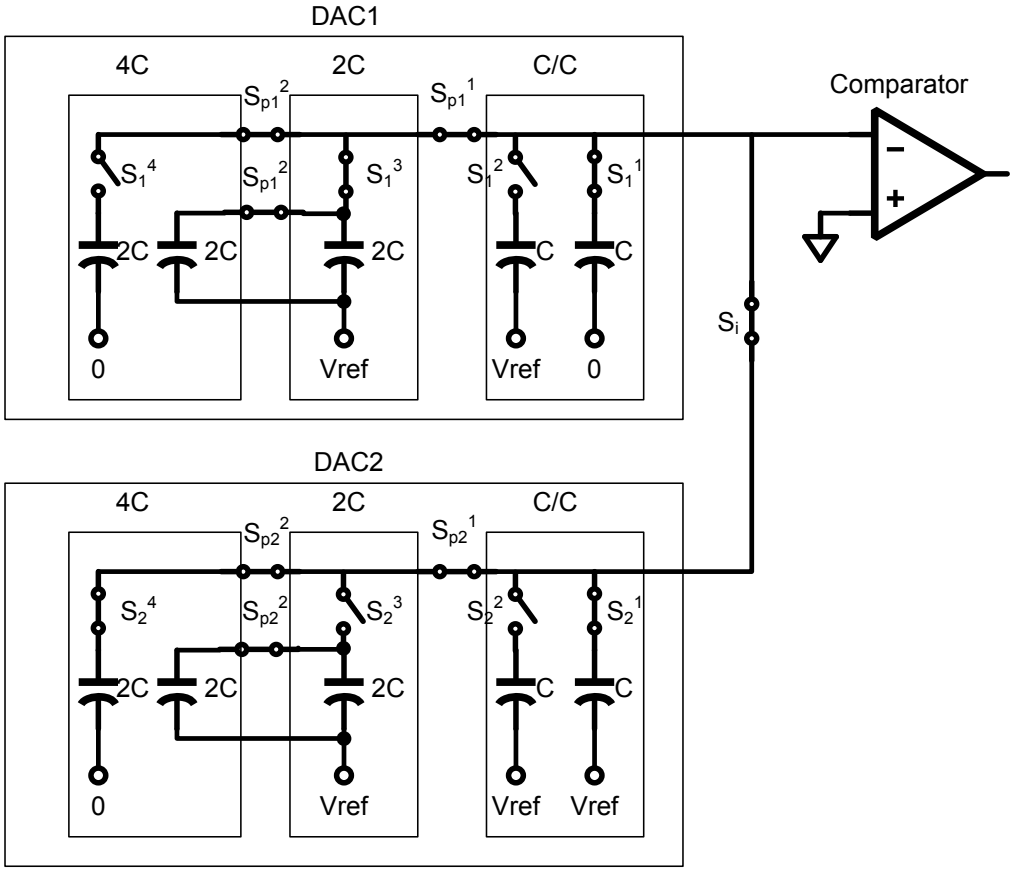


Fig. 5-5. Fine quantization of the 6th bit (DAC output 101011) using the proposed scheme.

Compared to the SJA [5-2] scheme, the new structure reduces both the dynamic power consumption and the capacitor area by reducing the total number of the unit capacitors needed from 2^N to $2^{N/2+1}$. For example, in a 10-bit SAR ADC, 1024 unit capacitors are needed in the earlier schemes [5-1][5-2], while only 64 units (32 for each DAC) are needed in the proposed structure. Since the power consumption is proportional to the total capacitance, a 93.75% saving in dynamic

power consumption can be achieved. Fig. 5-6 compares the energy requirements of the capacitor arrays for each code in a 10-bit ADC realized by classical SAR [5-1], split-junction SAR [5-2], and the proposed SAR.

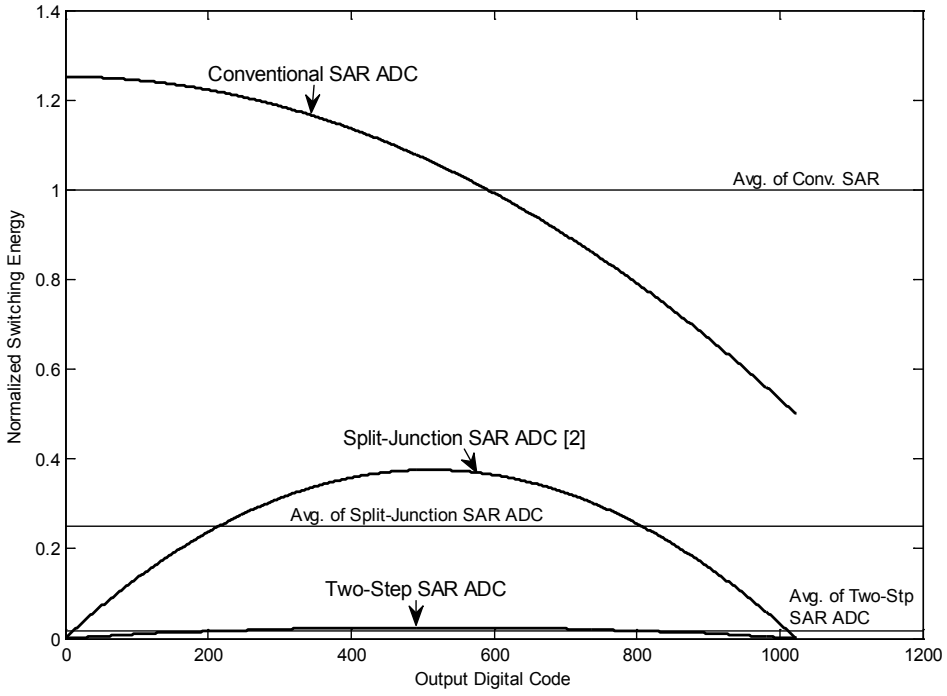


Fig. 5-6. Energy consumption versus output digital code for 10-bit SAR ADCs

5.2 Hybrid Cascade (MASH) ΔΣ Modulators

The cascade ΔΣ modulators, also known as Multi-stAge noise-SHaping (MASH) modulators, have many advantages, such as getting high-order noise shaping performance with the stability of low-order ΔΣ modulators [3-1].

As shown in Fig. 5-7, an L-0 MASH ΔΣ modulator has an L-th order ΔΣ modulator as the first stage, and a pipeline ADC as the second stage. If low-distortion structure is used in the first stage, we have

$$V_1(z) = U(z) + Q_1(z)(1 - z^{-1})^L \tag{5-1}$$

and

$$V_2(z) = Q_1(z)z^{-K} + Q_2(z) \tag{5-2}$$

where K is the number of clock delays introduced by the pipeline. If we make $H_1(z) = z^{-K}$ and $H_2(z) = (1 - z^{-1})^L$, the overall output $V(z)$ is

$$V(z) = V_1(z)H_1(z) - V_2(z)H_2(z) = U(z)z^{-k} - Q_2(z)(1 - z^{-1})^L . \tag{5-3}$$

From (5-3), we can see that $Q_1(z)$ is canceled and $Q_2(z)$ is noise-shaped. By doing low-pass filtering with a sinc^{L+1} filter and decimation on $V(z)$, we obtain the decimated output $V_d(z)$.

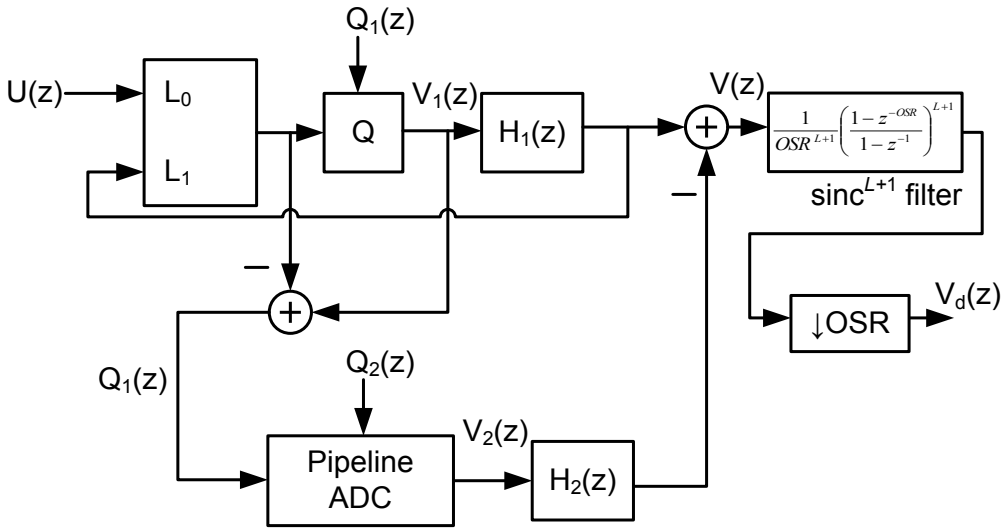


Fig. 5-7. A L-0 MASH ΔΣ modulator.

The purpose of the proposed hybrid MASH ΔΣ modulator is to replace the power-hungry pipeline ADC with the low-power SAR ADC. As shown in Fig. 5-8, the output of the first stage L-th order ΔΣ modulator $V_1(z)$ goes through a sinc^L filter (instead of the sinc^{L+1} filter used in a conventional ΔΣ modulator) and is decimated by a ratio of OSR. If $H_1(z)$ is kept to be z^{-K}, where K is the number of clock periods delay introduced by the SAR ADC, we have

$$\begin{aligned} & V_{1d}(z) \\ &= Deci\left[V_1(z)\frac{1}{OSR^L}\left(\frac{1-z^{-OSR}}{1-z^{-1}}\right)^L H_1(z)\right] \\ &= Deci\left[U(z)\frac{1}{OSR^L}\left(\frac{1-z^{-OSR}}{1-z^{-1}}\right)^L z^{-k}\right] + Deci\left[Q_1(z)\frac{1}{OSR^L}(1-z^{-OSR})^L z^{-k}\right]. \end{aligned} \tag{5-4}$$

where the *Deci* operator refers to decimation by OSR.

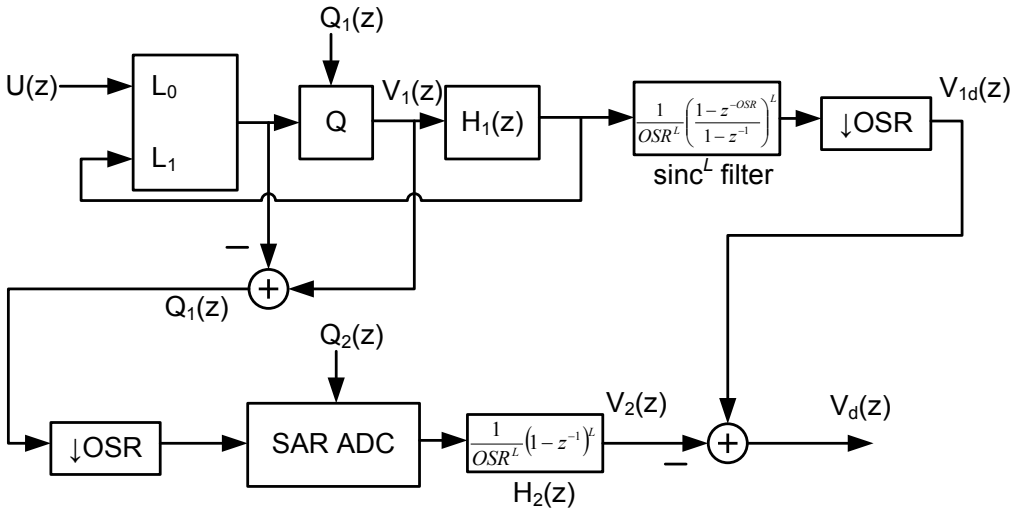


Fig. 5-8. A hybrid MASH ΔΣ modulator with a SAR ADC as the second stage.

From (5-4), we can see that only $Q_1(z)z^{-(k+n\cdot OSR)}, n=0,1,2,\cdots,L$ shows up in $V_{1d}(z)$, which implies that it is possible to cancel the Q_1 component with a decimated Q_1 sequence. As shown in Fig. 5-8, by using a SAR ADC to convert the decimated $Q_1(z)$ and choosing $\frac{1}{OSR^L}(1-z^{-1})^L$ as $H_2(z)$ (note that z^{-1} in $H_2(z)$ equals to z^{-OSR} before decimation), we have

$$V_2(z) = Deci\left[Q_1(z)\frac{1}{OSR^L}(1-z^{-OSR})^L z^{-k} \right] + \frac{1}{OSR^L}(1-z^{-1})^L Q_2(z). \tag{5-5}$$

By subtracting $V_2(z)$ from $V_{1d}(z)$, we cancel the Q_1 component and get

$$V_d(z) = Deci\left[U(z)\frac{1}{OSR^L}\left(\frac{1-z^{-OSR}}{1-z^{-1}}\right)^L z^{-k} \right] - \frac{1}{OSR^L}(1-z^{-1})^L Q_2(z). \tag{5-6}$$

We can calculate the powers of the quantization noise in the overall decimated output for the conventional and the hybrid MASH from (5-3) and (5-6), respectively. For simplicity, assume an ideal "brick-wall" filter (which gives slightly better result than a sinc^{L+1} filter) is used for $V(z)$ in the conventional MASH (Fig. 5-7). The power of the quantization noise after decimation can be obtained from the integration of the in-band quantization noise in (5-3)

$$\sigma_{q,conv}^2 \approx \int_0^{1/(2OSR)} (2\pi f)^{2L} \cdot 2 \cdot \sigma_{q2}^2 df = \frac{\pi^{2L}\sigma_{q2}^2}{(2L+1)OSR^{2L+1}} \tag{5-7}$$

where σ_{q2}^2 is the power of the quantization noise injected by the second stage ADC (the pipeline ADC). In the case of the hybrid MASH, as can be seen from (5-6), the quantization noise $Q_2(z)$ is noise-shaped as

$$V_{d,q}(z) = \frac{-1}{OSR^L}(1-z^{-1})^L Q_2(z) = \frac{-1}{OSR^L}(a_0 + a_1 z^{-1} + a_2 z^{-2} + \cdots a_L z^{-L}) Q_2(z). \quad (5\text{-}8)$$

From (5-8), the power of the quantization noise in $V_d(z)$ can be calculated as

$$\sigma^2_{q,hybrid} = \frac{1}{OSR^{2L}} \sigma^2_{q2} \sum_{i=0}^{L} a_i^2 \quad (5\text{-}9)$$

From (5-7) and (5-9), a comparison between conventional 2-0 MASH, hybrid 2-0 MASH, hybrid 3-0 MASH and conventional 2nd-order single-loop ΔΣ modulator with 3-bit quantizer is shown in Fig. 5-9. For the second stage ADC, an 8-bit SAR (pipeline) ADC is assumed.

Compared with the conventional 2nd-order single loop ΔΣ modulator with 3-bit quantizer, the hybrid 2-0 MASH gains significantly (approximately 20 dB) in SQNR, but consumes only a little more power due the additional SAR ADC.

Compared with the conventional 2-0 MASH, the hybrid 3-0 MASH achieves significant improvement in SQNR (approximately 20 dB). The power consumptions of the two schemes are estimated to be similar, because the hybrid 3-0 MASH needs one more OTA, but saves the power consumption of the pipeline ADC.

In both comparisons, the proposed hybrid MASH scheme can achieve higher SQNR with similar power consumption.

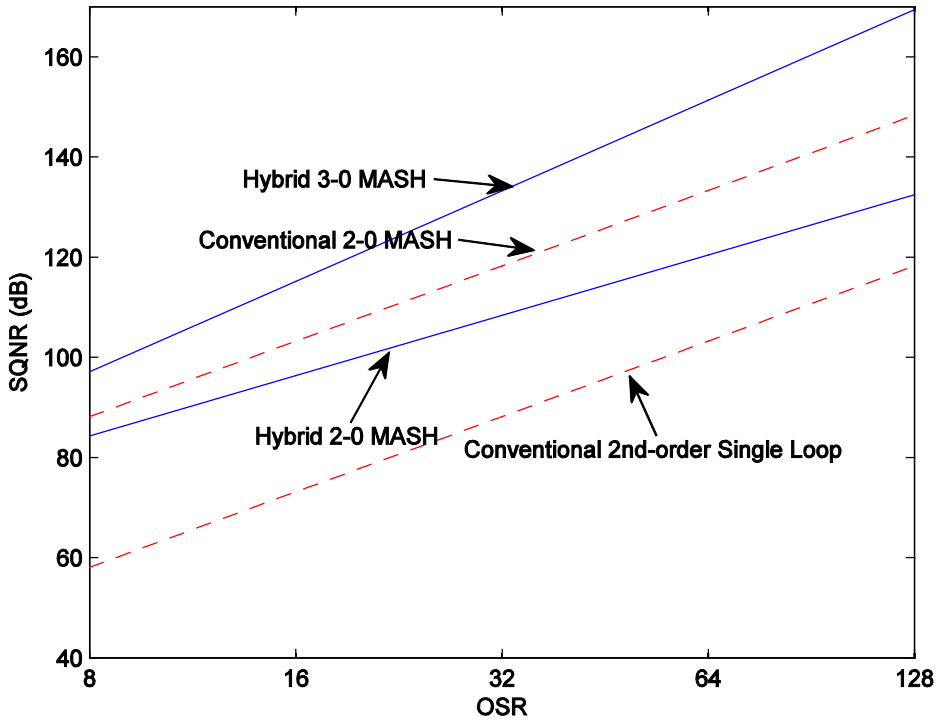


Fig. 5-9. SQNR versus OSR for conventional 2-0 MASH, hybrid 2-0 MASH, hybrid 3-0 MASH and conventional 2nd-order single-loop ΔΣ modulator with 3-bit quantizer.

Chapter 6 Conclusion

An incremental ADC with digital DAC mismatch correction was designed and fabricated in 0.18 μm CMOS process. The proposed analysis and optimization technique for incremental ADCs was verified by measurement results. With the proposed optimal decimation filter, around 2 dB improvement in SNDR was observed. Two new low-power design techniques, the two-step split-junction SAR ADC and the hybrid cascade ΔΣ modulator, were proposed.

In the future, the effect of capacitor mismatches in the two-step split-junction SAR ADC needs to be investigated. It is also interesting to find a hybrid cascade ΔΣ modulator scheme for the general situation, in which the noise transfer function has poles. Circuit implementations and measurements are needed to verify the above schemes.

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