AN ABSTRACT OF THE DISSERTATION OF

James S. Ayers for the degree of Doctor of Philosophy in
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Title: Ultra-Low Power Receivers for Wireless Sensor Networks

Abstract approved: _____

Terri S. Fiez Kartikeya Mayaram

In wireless sensor network applications, low-power operation of the wireless receiver is critical. To address this need an ultra-low power Binary Frequency Shift Keying (BFSK) receiver using the super-regenerative architecture is developed.

A prototype receiver is built and tested for operation in the 900 MHz ISM band. Lab measurements show power consumption as low as 244 μW with a sensitivity of -84 dBm while operating at 250 kbps. A second test chip designed to operate at 2.4 GHz improves on the previous design by adding full digital control and calibration. The 2.4 GHz receiver consumes 215 μW while operating at 250 kbps and shows a 12 dB improvement in sensitivity over the original design. The entire receiver has an energy consumption of only 0.175 nJ/b while operating at 2 Mbps.

Ultra-Low Power Receivers for Wireless Sensor Networks

by

James S. Ayers

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

James S. Ayers, Author

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

LIST OF TABLES

Chapter 1 – Ultra-Low Power Wireless Senssor Networks

1.1 The Future of Connectivity

In the past few decades technology has dramatically changed the world and the way that we lead our day to day lives. In the late 1970s and early 1980s the personal computer (PC) was introduced allowing people to easily create, process, and organize and store information in their own homes. This led to the fast growth of the internet in the 1990s which allowed vast amounts of this information to be shared with anyone connected around the world. As internet usage continued to grow, the number of users as well as the amount of information and commerce also continued to grow at an exponential rate [3]. In the 2000s, wireless connectivity via 802.11 and cell networks allowed users to use portable devices such as laptops and "smartphones" to access the web from anywhere wireless coverage is available. This has allowed people to connect to the web and share information on a constant basis from almost anywhere people travel.

Up until this decade the vast majority of the information found and distributed on the internet was created and requested by human users. This is slowly changing as wireless sensor networks (WSN) are currently being designed to autonomously monitor anything from personal health to home lighting to bridges and roads. The information collected by sensors is passed to a processing hub or the internet where it can be used to provide real-time information and feedback. As WSNs become more common, their

data will be used to not only monitor conditions, but provide feedback in systems that can autonomously adjust themselves based on specific conditions.

1.2 Wireless Sensor Network Overview

A WSN is generally made up of several sensor nodes that collect information about their environment and then communicate that information to a central hub. While the hub is usually assumed to have a large power source, the sensors are often powered by a small battery or energy scavenged from the environment. For this reason, minimizing energy consumption in the sensors is often the highest priority when designing the network.

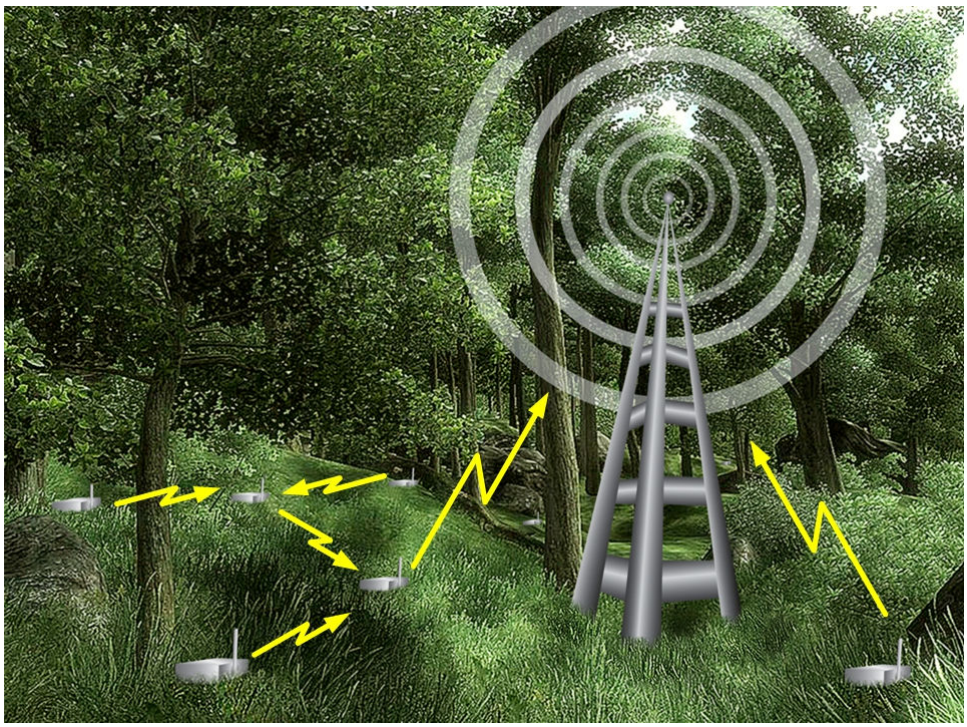

Figure 1.1: Wireless sensor network with peer-to-peer communication.

To achieve this low energy requirement, the WSN is often set up to communicate information to the hub in a peer-to-peer multi-hop fashion as shown in Fig. 1.1. In this configuration the power consumed by the nodes can be minimized by picking the optimal distance between the sensor nodes [4]. This allows the amount of power consumed by the wireless transceiver to be reduced as it only needs to communicate data over a short distance compared to the case where it communicates directly with the hub. Although in a dense network sensors closer to the hub will end up communicating more, the overall power consumed in the entire network as a whole will be less [5].

Another way the sensor power consumption is reduced is by allowing the hub to control the flow of data traffic in the network while keeping the sensors as "dumb" as possible. By doing this the amount of processing power needed on the sensor nodes is minimal as it only executes basic commands issued by the hub.

1.3 Anatomy of a Sensor Node

As mentioned in Section 1.2 the sensor node is designed to be as basic as possible in order to minimize its power consumption and hence, maximize its useful lifetime. Figure 1.2 shows examples of three sensor nodes from both the research and commercial fields [1, 6, 7]. Each sensor node is made up of four basic parts: (1) a sensor interface (the actual sensor may be either integrated or external), (2) a power supply and power conditioning circuitry, (3) a digital controller with data memory, and (4) a wireless interface.

The sensor node can either be powered by an on-board battery, energy harvested

from the surrounding environment, or a combination of the two. In either case the power from the energy storage device needs to be efficiently regulated to a specific voltage that is compatible with the other circuits in the sensor node [8]. The sensor interface connects the digital sensor node to the "analog" environment that it is sensing. The desired condition being sensed is converted to an electrical signal (voltage, current, capacitance, etc.) before being converted to a digital signal [9]. Once the digital signal has been generated it is stored in memory by the digital controller. The digital controller is also used to control the sensor node by telling the sensor interface when to take a measurement and when to transmit or receive data between itself and surrounding nodes (or the hub) using the wireless transceiver [10].

The current consumption of a commercially available sensor node [1] and a state-of-the-art two-chip sensor node solution [2] is shown in Fig. 1.3. The currents for each of the sensor nodes are shown when the sensor node is in receive mode. The overall power consumption of each node is dominated by the wireless communication circuitry and within this circuitry, the receiver consumes the largest amount of power. For this reason, it is critical for the wireless transceiver to consume the lowest amount of power possible while still maintaining the required performance. This will ensure that the sensor node will have the longest useful lifetime while also maximizing the amount of

Figure 1.2: Examples of sensor nodes used in a wireless sensor network.

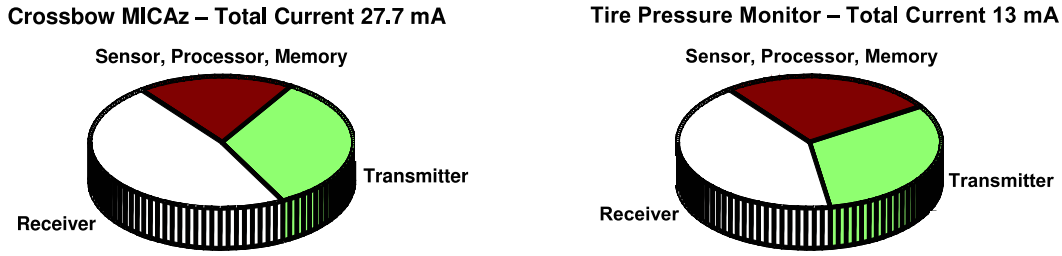

Figure 1.3: Power consumption of a commercially available sensor node [1] and a state-of-the-art wireless sensor node [2]. The total current is given for each sensor when it is in receive mode.

available power sources. This dissertation focuses on the power consumption of wireless receivers for wireless sensor networks.

1.4 Dissertation Organization

This dissertation develops an architecture for an ultra-low power wireless receiver for use in WSNs. Chapter 2 provides a review of recent ultra-low power designs for the classic direct conversion (homodyne) architecture and ideas to further improve the power consumption of receivers using the direct conversion architecture. In Chapter 3 the architecture for a new super-regenerative receiver that uses binary frequency shift keying (BFSK) modulation is presented and some key tradeoffs of the new architecture are discussed. A prototype receiver using the architecture described in Chapter 3 is presented in Chapter 4 along with measurement results and a comparison to other state-of-the-art receivers. Improvements to the receiver described in Chapter 4 along with a second test chip are shown in Chapter 5 and finally conclusions are given in Chapter 6.

Chapter 2 – Tradeoffs in the Design of CMOS Receivers for Low Power Wireless Sensor Networks

2.1 Abstract

Key issues in wireless receivers for wireless sensor networks are discussed and existing implementations are compared. On the system level, two different power allocation schemes are compared for use in low power systems. On the circuit level, several low power circuits are analyzed and recommendations are made for most promising candidates to be used in low power receivers for wireless sensor networks.

2.2 Introduction

Wireless sensor networks have recently been gaining more attention in the field of wireless data transmission and networking. Sensor networks serve an almost limitless number of applications including environmental monitoring [11], smart buildings and highways, factory automation, robotics, and entertainment [12]. Previous estimates report that over 1 billion mobile sensors are deployed in 20 million cars across the U.S. and in 10 years there will be over 60 trillion sensors deployed worldwide [13].

Although they serve a vastly different number of purposes, wireless sensor networks have several common similarities. Typically an area is densely populated with sensing

nodes that have extreme constraints on their energy consumption. As a result, data transmission takes place in a peer-to-peer fashion where data is transmitted short distances ($\sim$10 m) at relatively low data rates (between 10 kbps and 500 kbps). Sensor networks can be made up of hundreds or thousands of nodes, therefore each sensing node needs to be cheap and compact while still providing reliable and accurate sensing and data transmission.

Sensing nodes need to operate autonomously for time periods spanning years using power supplied by a single battery or energy scavenged from the surrounding environment [14]. Sensing nodes will typically contain a microprocessor, memory, power source, sensor and sensor interface, and a wireless transceiver [15]. In CMOS technology, the power consumed by digital circuits (microprocessor and memory) scales down with gate length while the analog circuitry (sensor, sensor interface, and transceiver) typically does not. The sensor and sensor interface operate at such a low duty cycle that their power dissipation is much less than that of the transceiver. For transmit distances greater than 10 m the transceiver power is dominated by the transmit power amplifier. When the transmit distance drops below 10 m the transmit power is reduced, resulting in the receiver consuming a large portion of the overall transceiver power [16]. Thus, it is essential that the receiver in wireless sensor networks be optimized for ultra low power on both the circuit and system level.

Section 2.3 will examine the receiver on the system level and compare different power allocation schemes. Section 2.4 will explore the different receiver blocks on the circuit level and Section 2.5 will summarize the findings and give ideas for further improvement in low power wireless receivers for sensor networks.

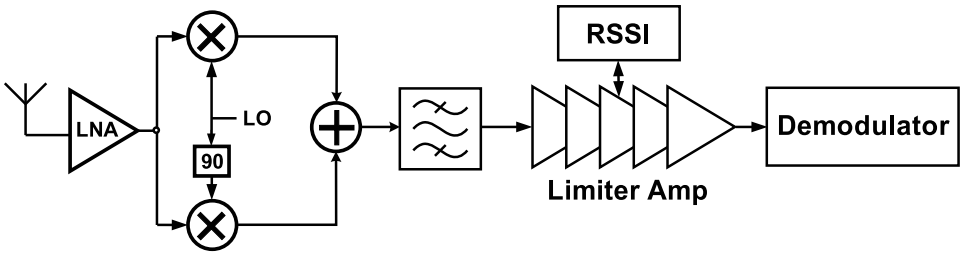

Figure 2.1: A low power receiver architecture.

2.3 Low Power Radio Architecture

A general receiver architecture used in low power wireless sensor networks is shown in Figure 2.1. The incoming radio frequency (RF) signal is amplified by a low noise amplifier (LNA) and down-converted to an intermediate frequency (IF) by a quadrature mixer whose local oscillators (LOs) are phase shifted by 90°. The baseband signal is then filtered to remove the image signal (in low-IF architectures) and any out of channel interferers before being amplified by the limiting amplifier and demodulated. The signal at the limiting amplifier is sensed by the received signal strength indicator (RSSI) to allow the limiting amplifier gain to be lowered when larger signals are present.

There are three main performance merits in a wireless receiver; gain, noise figure (NF), and 3rd order intercept (IP3). Each block in the receiver chain possesses these three specifications which, in turn, determine these specifications for the entire receiver chain.

The gain of the receiver describes how much the incoming signal is amplified before

being demodulated. The total gain of a system with N cascaded gain stages is given by

$$A = A_1 A_2 \cdots A_N \tag{2.1}$$

where A_N is the gain of the N^{th} stage.

The amount of noise added by the system is specified by the noise figure, which is the noise factor expressed in dB. The noise factor for a system with N cascaded stages is given by [17]

$$F = F_1 + \frac{F_2 - 1}{A_1} + \frac{F_3 - 1}{A_1 A_2} + \cdots + \frac{F_N - 1}{A_1 A_2 \cdots A_{N-1}} \tag{2.2}$$

where F_N is the noise factor for the N^{th} stage and A_N is the gain of the N^{th} stage.

The IP3 determines what power level will cause the 3^{rd} order intermodulation product (between two input tones with equal power) to become the same amplitude as the fundamental signal. The IIP3 of a cascaded system with N stages is given by [17]

$$IIP3 = \left(\frac{1}{IIP3_1} + \frac{A_1}{IIP3_2} + \cdots + \frac{A_1 A_2 \cdots A_{N-1}}{IIP3_N} \right)^{-1} \tag{2.3}$$

where $IIP3_N$ is the input referred IP3 of the N^{th} stage (in Watts) and A_N is the gain of the N^{th} stage.

By inspecting (2.2) we see that if a system has high gain in the first few blocks, the NF of the first block will determine the NF of the overall system. Conversely, a system aiming to minimize power by eliminating the LNA from the receiver front-end may suffer greatly from noise introduced by the mixer and the baseband circuits.

From (2.3) we see that the IP3 of the overall system depends greatly on the linearity of the later stages in the system, while the linearity of the earlier stages (LNA and mixer) is not as critical. Also, a high concentration of gain in the first stages of the receiver chain will degrade the IP3 performance more than if the gain is concentrated in the later baseband stages.

As stated previously, low power wireless sensor networks cover short distances ($\sim$10 m), therefore the noise figure requirements of the receiver can be relaxed without significantly sacrificing performance. Short range low power wireless networks that can accept noise figures of up to 20 dB have been proposed [18]. The majority of sensor networks operate in the license free ISM frequency bands (902-928 MHz, 2.4-2.4835 GHz, 5.725-5.85 GHz) which give the potential for receiving strong interferers from nearby wireless devices operating in the same band. This puts a higher constraint (than in a case with no interferers) on the distortion requirements of the receiver so that the system is not saturated by strong interferers in the same frequency band [19].

Table 2.1: Performance evaluation of two different receivers.

Arch.	Block	Gain (dB)	NF (dB)	IIP3 (dBm)
1	LNA	20	5	-15
	Mixer	10	15	10
	Filter	0	15	20
	Amp.	30	20	30
	Total	**60**	**5.5**	**-17**
2	LNA	0	0.5	30
	Mixer	-3	6	10
	Filter	20	15	20
	Amp.	43	30	30
	Total	**60**	**20**	**8**

Consider the two fictional[1] receiver chains outlined in Table 2.1. Receiver 1 is a classical receiver structure that is designed to distribute the gain in the receiver throughout the different blocks in order to balance noise and power. Much of the gain is concentrated in the receiver front-end in order to reduce the noise figure of the entire structure, while the remaining gain is placed in the baseband amplifier.

Receiver 2 adopts an architecture with a completely passive RF front-end that provides some voltage gain, but no power gain. All of the receiver's power gain is concentrated in the baseband circuitry where the signal is amplified by the filter and the IF amplifier. The passive front-end allows the signal to be mixed down to the IF without dissipating any power and adds very little noise to the incoming signal. The noise figure of the receiver is dominated by the baseband circuitry whose high noise figure is not suppressed by the passive front-end.

The IIP3 of receiver 2 is enhanced by the passive front-end. As a result of the front-end having no power gain, nonlinearity from the amplifying transistors is avoided giving the passive front-end very low distortion. In addition, because the front-end provides no gain the IIP3 of the overall system is not degraded as much as it would be in a structure with a high front-end gain.

By comparing the gain, noise figure, and IIP3 of the two receiver designs we find that structure 2 is much better suited for low power wireless sensor networks. By employing a front-end with low gain and low noise the IIP3 is increased over the more classic structure while the noise figure remains within the bounds suitable for a multi-hop wireless sensor network. Moreover, the power dissipation of the front-end has been

[1]The block specifications are based on the receivers summarized in Table 2.3.

greatly reduced which, as will be shown in Section 2.4, accounts for the majority of the power consumed in most RF receivers.

2.4 Low Power Receiver Circuits

As shown in Figure 2.1 the low power RF receiver is made up of two distinct sections; the RF front-end and the baseband circuitry. In this section the different circuit architectures for these two receiver subsections will be explored and comparisons will be made to identify the designs best suited for low power wireless sensor networks.

2.4.1 Low Power RF Front-Ends

Table 2.3 shows several low power RF front-ends published in recent years. Each of the table entries consists of an LNA and mixer combined to produce an RF front-end suitable for a low-IF or direct conversion receiver. Table 2.2 gives information on the entire receivers for the references in Table 2.3.

The three architectures used for the LNA are the common source amplifier, common gate amplifier, and the self-biased inverter (shown in Figure 2.2). Each of these structures has its own trade off between gain, noise figure, distortion, and power. The gain of each of the amplifiers is proportional to $g_m Z_0$ where g_m is the transconductance of the amplifier and Z_0 is the output impedance at the center frequency. For a given bias (V_{gs}), transistor size, and output impedance the common gate and common source am-

Table 2.2: Recent Low Power Receivers. Component Key: L=LNA, M=Mixer, V=VCO, FD=Freq. Divider, B=LO-Buffer, F=Filter, I=IF-Amp, FLL=Freq. Locked Loop, R=RSSI.[5]

REF.	Tech.	Year	Frequency	Components	Total Power (mW)	Bit Rate (kbps)
[20]	0.25 μm	2000	900 MHz	L,M,V,FD,F	4.5	6.4
[21]	0.5 μm	2001	434 MHz	L,M,F,I	1	24
[22]	0.35 μm	2002	900 MHz	L,M	N/R	N/R
[23]	0.18 μm	2002	2.4 GHz	L,M	N/R	N/R
[24]	0.18 μm	2003	2.4 GHz	L,M,F,I,R	9	200
[25]	0.25 μm	2004	900 MHz	L,M,I,FLL,D	1.2	20
[19]	0.13 μm	2004	900 MHz	L,M,F	3.24	20
[26]	0.18 μm[5]	2004	2.4 GHz	L,M,FD	8.8	N/A
[27]	0.13 μm	2005	2.4 GHz	L,M,B,F,I	3.24	N/R
[28]	0.13 μm	2006	2.4 GHz	M,F,R	0.33	300
[29]	0.18 μm	2006	2.4 GHz	L,M	N/R	N/R
[30]	0.18 μm	2006	900 MHz	L,M,F	3.6	250
[31]	0.13 μm	2006	2.2 GHz	L,M,B	12.7	N/R

Table 2.3: Recent low power receiver front-ends (LNA and Mixer).[2]

REF.	Year	IIP3(dBm)	NF(dB)	Gain(dB)	Power(mW)	Architecture - LNA / Mixer
[20]	2000	-25	6.3	41	1.5	Common Gate / Dual Conversion
[21]	2001	-33	15	32	0.24	Common Gate / Stacked Double Balanced
[22]	2002	-18	8.75	27.5	2.2	Common Gate / Dual Conversion
[23]	2002	-18	13.9	21.4	6.5	Common Source / Single Balanced
[24]	2003	-4	N/R	30	5.4	Common Source / MGTR Single Balanced
[25]	2004	N/R	9	20	0.32	Self-biased Inverter / Passive
[19]	2004	-11	20	28	1.92	Common Gate / Gilbert Cell
[26]	2004	-9	6.5	32	7	Common Source / Current Mirroring Dual
[27]	2005	-21	28	12.5	1.68	Common Gate / Stacked Double Balanced
[28]	2006	-7.5	6.7	15[4]	0	Input Match / Passive
[29]	2006	N/R	11.8	31.5	0.5	Common Source / Stacked Cascoded
[30]	2006	-5	3	30	3.6	Common Source / Passive Double Balanced
[31]	2006	0	11	4.5	8.64	Common Source / Passive Double balanced

plifiers will have equal gain for the same power consumption. The self-biased inverter

[2]The input match in [28] provides 15 dB of voltage gain, but no power gain.

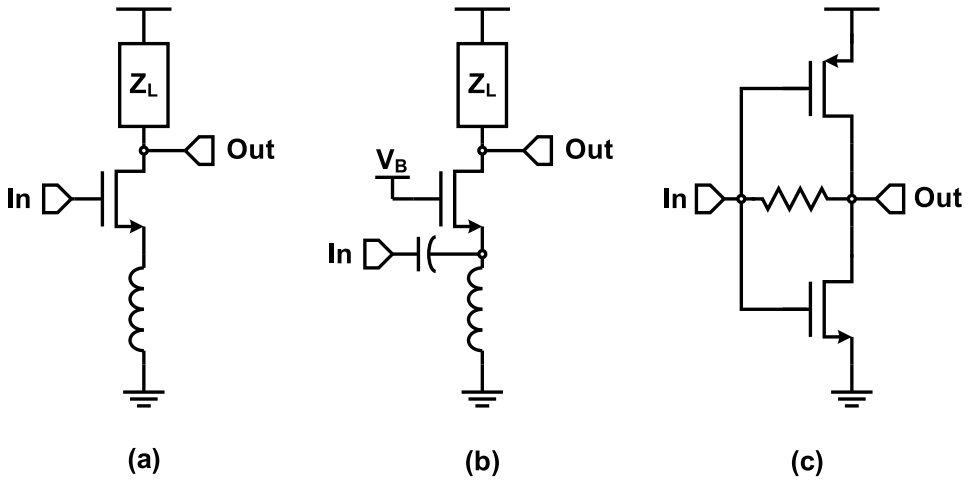

Figure 2.2: Three LNAs used in low power RF receivers; (a) common source, (b) common gate, and (c) self-biased inverter.

has twice the gain[3] of the common source and common gate amplifiers for the same power because its equivalent total g_m is given by $g_{m,N} + g_{m,P}$ [25].

The noise factor for the input matched common gate amplifier and the self-biased inverter is given by [32][4]

$$F_{min,CG,S-B} = 1 + \frac{\gamma}{\alpha} \tag{2.4}$$

where γ is the channel noise coefficient (2 for short-channel devices) and α is g_m/g_{d0}. The noise factor for an input matched common source amplifier is given by [33]

$$F_{min,CS} = F_{min} + \frac{\gamma}{\alpha g_m R_s}\left(1 - \frac{Q_{opt}}{Q_s}\right)^2 \tag{2.5}$$

[3] Assuming the condition where the transconductance of the NMOS and the PMOS transistors is equal.
[4] This expression neglects the noise contribution of the feedback resistor in the self-biased inverter.

where F_{min} is the minimum device noise factor, g_m is the device transconductance, R_s is the source impedance, Q_{opt} is the optimum quality factor, Q_s is the actual source quality factor, and γ and α are the same as above.

Figure 2.3 shows the ratio of $NF_{min,CS}$ over $NF_{min,CG}$ versus power consumption for the three different ISM frequency bands. The noise factors are calculated using parameters from a 0.25 μm CMOS process with a 1.5 V power supply.

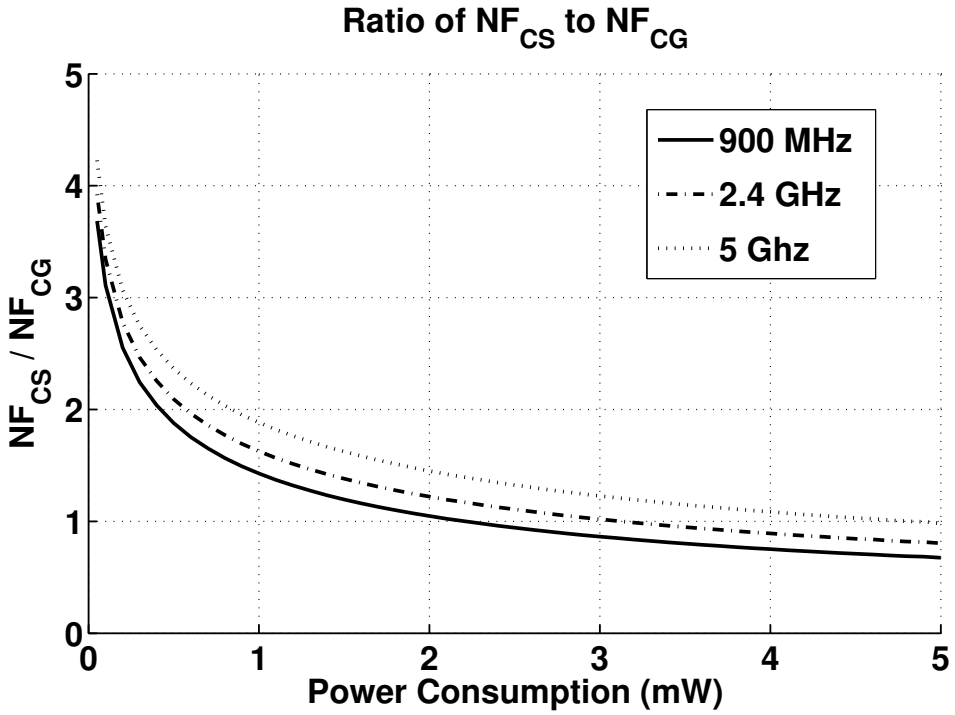

Figure 2.3: Noise figure comparison between common source and common gate amplifiers in a 0.25 μm process with a 1.5 V supply.

All three frequencies show that for very low power operation the common gate amplifier has a lower noise figure that the common source amplifier. The noise figure of

the common source amplifier is proportional to the ratio of the center frequency to the ω_T of the transistor. As the power consumption decreases the ω_T of the device also decreases, increasing the ω_0/ω_T ratio. As this ratio becomes larger the noise figure of the common source amplifier becomes larger that that of the common gate amplifier. For the 900 MHz, 2.4 GHz, and 5 GHz cases the power at which the common gate and common source noise figures are equal is 2.2 mW, 3.1 mW, 4.8 mW, respectively.

It should also be noted that for a given power consumption the self-biased inverter has a larger g_m than the common gate and common source amplifiers. This increases its α giving it a lower noise figure than both the common source and common gate amplifiers when operating under extremely low power conditions.

The distortion of all three amplifiers has a strong dependence on the overdrive voltage (V_{gs}- V_{th}). With the common source and common gate amplifiers there is a direct trade off between power, gain, and linearity. To increase the linearity, the bias voltage on the gate can be increased to provide a higher overdrive voltage. This results in the transistor sourcing more DC current and hence increasing the power consumption.

The self-biased inverter sets its own input bias (via the feedback resistor) and can only be adjusted by changing the size ratio of the NMOS and PMOS transistors. The maximum overdrive available for the two amplifiers is determined by the supply voltage. For each transistor the maximum available overdrive will be $(V_{dd} - V_{th,N} - V_{th,P})/2$ which means the linearity decreases with the supply voltage. RF front-ends using self-biased inverters have reported IIP3 values of -10 dBm [32] and P_{1dB} of -18 dBm [25].

There are three main types of mixers used in low power wireless front-ends; passive, active, and stacked. Passive mixers use transistors as switches driven at the LO

frequency to down-convert the incoming signal. These mixers have no DC current running through them so they generally have very low noise (compared to active mixers) at the cost of attenuating the input signal. Passive mixers have been reported with noise figures as low as 5.3 dB [34] and typically have a gain lower than $2/\pi$ [35].

Active mixers use a transconductance stage to amplify the incoming signal before translating it to the IF frequency. This transconductance stage provides extra gain at the cost of added $1/f$ noise from the DC current that flows through the mixer. The linearity in an active mixer is generally lower than in the passive mixer because the signal is passed through a nonlinear amplification stage before being translated to the IF.

The stacked mixer is a combination of the active and passive mixers. It is stacked above the LNA allowing a single tail current for the LNA and mixer. This method allows the elimination of an extra tail current in the receiver chain without sacrificing the gain of the active mixer.

The four RF front-ends in Table 2.3 that consume less than 1 mW use all three of the LNA designs discussed above as well as the stacked and passive mixer designs. The higher gain designs employ the common source and common gate LNAs with stacked mixers while the lower gain designs use the self-biased inverter and no LNA (just an input match) with passive mixers. Although the stacked mixers provide extra gain it is at the price of a higher noise figure for the overall front-end. The DC current flowing through the mixing transistors adds $1/f$ noise that severely degrades the noise figure compared to the front-ends with the passive mixers.

The linearity of the passive front-end [28] far exceeds that of the front-end with an active LNA and stacked mixer [21]. [21] uses a common gate amplifier with an off chip

matching network to provide maximum power transfer from the 50 Ω source to the 1 kΩ LNA input resistance. The stacked double balanced mixer shares the LNA bias current and the output signal is taken from an RC load that provides a single pole to filter any out of band signals. [28] uses a differential input match to provide 15 dB of voltage gain before mixing the signal down to the IF frequency using a passive double-balanced mixer. Although this design provides a negative gain, the absence of active devices results in a high linearity with low noise contribution.

The completely passive front-end design is the best choice for use in wireless sensor networks. Its extreme low power and high linearity provide the best combination of RF front-end characteristics for sensor applications. Its only downfall is its lack of power gain which will increase the noise and gain requirements of the baseband filter and amplifier.

2.4.2 Baseband Filters and IF Amplifiers

After the signal has been amplified and down-converted by the RF front-end it needs to be filtered and amplified again before being demodulated. The purpose of this filtering and amplification is to remove any interferers or adjacent channels before bringing the signal level up to an amplitude that is suitable for reliable demodulation.

The amount of filtering needed depends greatly on the communications protocol being used. The filter order is determined based on the filter response, ratio of channel spacing to channel bandwidth, and maximum ratio of the power in adjacent channels to the power in the desired channel. The baseband filter can also limit the dynamic range

of the entire system. For this reason the filter needs to be designed with a filter order that will not significantly degrade the overall system dynamic range [21]. In the case of a system that maximizes bandwidth efficiency the individual communication channels are closely spaced. In these systems, the the filter order needs to be increased to ensure proper attenuation of the closely spaced channels. In systems with very few channels (or only a single channel), the filter order can be reduced as the adjacent channel attenuation requirements are relaxed. A system with densely spaced channels can require filters with an order of 5 or 6 while systems that are less bandwidth efficient can use simpler and lower power first or second order filters.

Analog filtering can be performed with switched capacitor or continuous time circuits. Switched capacitor filters need to be sampled at at least twice the rate of the highest desired signal frequency and usually require an anti-aliasing filter to prevent out of band noise from being folded into the signal band [36]. Continuous time filters avoid sampling the incoming signal allowing the possibility of extremely low power operation while also eliminating the need for an anti-aliasing filter. The down side to continuous time filters is that they rely on matching of dissimilar components (resistors, capacitors, and transconductors) to obtain the desired frequency response. As a result, many continuous time filters adopt tuning schemes that can significantly increase the circuit complexity or die area.

The two main low power continuous time filter architectures are active-RC and g_m-C. Active-RC filters combine opamps with resistive and capacitive feedback and feedforward paths to realize the necessary poles and zeros. These filters tend to be more linear than g_m-C filters because they use high gain opamps, but also consume more power be-

Table 2.4: Recent low power continuous time filters. $FOM = P/(Order \cdot BW)$

Ref.	Year	Gain (dB)	Power (μW)	BW (kHz)	Order	Arch.	**FOM (nJ)**
[38]	1999	0	10.5	100	5	gm-C	**0.02**
[20]	2000	20	210	25	4	Active-RC	**2.10**
[21]	2001	0	100	100	5	gm-C	**0.20**
[24]	2003	12.4	2520	2200	5	Active-RC	**0.23**
[39]	2003	0	167	50	3	gm-C	**1.11**
[40]	2003	20	4000	500	4	gm-C	**2.00**
[41]	2004	55	4860	1000	6	Active-RC	**0.81**
[19]	2004	20	600	120	3	Active-RC	**1.67**
[27]	2005	9.5	78	550	3	gm-C	**0.05**

cause the opamps need to drive resistive loads [37]. G_m-C filters realize the filter poles and zeros using capacitors and transconductor blocks which can be designed to consume very low power.

Table 2.4 summarizes the lowest power filters recently published. The figure of merit (FOM) in Table 2.4 gives the energy consumed per pole for each of the filters. The two designs with the lowest power consumption are realized with g_m-C filters [38] [27]. The design in [38] is a pseudo-differential filter that uses differential transconductors to reduce the number of required circuit blocks by a factor of two. A similar architecture is used in [21] and both designs are tuned by controlling the tail currents of the transconductors.

In [24], an active-RC structure is used to realize a fully differential polyphase filter. This filter consumes more energy per pole than the g_m-C filter discussed above, but it also provides image rejection and signal gain. This signal gain is beneficial because it reduces the noise requirements on the following stages in the receiver. The active-RC filter is tuned using a 5-bit capacitor array resulting in a die area that is over 6 times that

of the g_m-C filter in [38].

The large area and higher power consumption of the active-RC filter do not fit well with the wireless sensor receiver. In order for the sensor nodes to remain cheap and have the longest possible autonomous operation, the die area consumed by each circuit block should be minimized along with its power consumption. For these reasons the g_m-C filter is the best choice because of its low power and low area design.

The limiting amplifier is made up of several cascaded gain stages that saturate the input signal to a constant value. For low power sensor networks the use of limiting amplifiers is preferred over automatic gain control (AGC) amplifiers because they can handle a much larger dynamic range while consuming much lower power [42]. The limiting amplifiers can be controlled by a received signal strength indicator (RSSI) that adjusts the bias on the limiting amplifier to reduce its power when the full scale gain is not needed.

Three limiting amplifier circuits are shown in Figure 2.4 [27, 28, 43]. The minimum supply voltage for the circuit in 2.4(a) is $V_{th2} + V_{th3} + 3V_{od} + V_{sw}$ where V_{thn} is the threshold voltage for M_n, V_{od} is the transistor overdrive voltage and V_{sw} is the output signal swing. This high minimum supply voltage makes the circuit not suitable for low power design and thus not a good choice for wireless sensor networks.

The circuits in 2.4(b) and 2.4(c) have been simulated in a 0.25 μm CMOS process and the results are shown in Figure 2.5. The number of stages in the limiting amplifier have been optimized to ensure the lowest power consumption for a given gain and bandwidth [44]. Each limiting amplifier consists of eight stages to produce 75 dB of gain and a -3 dB bandwidth of at least 5 MHz. Both amplifiers have a 25 pF AC coupling

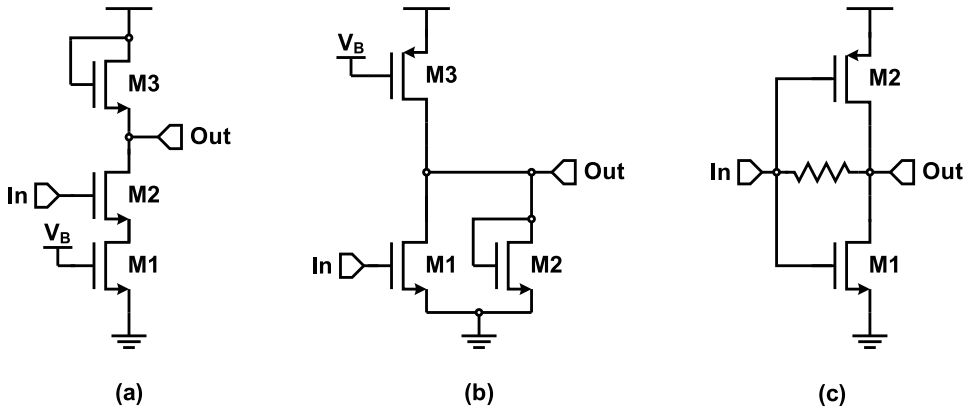

Figure 2.4: Three limiting amplifier circuits; (a) common source with NMOS load, (b) common source with diode tied load, and (c) self-biased inverter.

capacitor at the input to preserve the DC biasing. Each stage in the self-biased inverter design provides its own input bias point using the feedback resistor. The bias point in the common source amplifier is set by the first stage, which is in unity-gain configuration.

The common source limiter provides 75 dB of gain with only 36 μW while the self-biased limiter needs 99 μW. Although the common source limiter consumes less power its noise performance is also much worse than the self-biased design. The common source amplifier has an input referred noise power of -63 dB while the self-biased inverter amplifier has an input referred noise power of -84 dB. The high amount of noise in the common source limiter is due to the biasing used. As a result of the first stage being in unity-gain feedback configuration the flicker noise from the input transistor of the first two stages is coupled directly to the input. To reduce the input referred noise the input bias to the first stage can be provided by the output of the final stage via a low-pass RC filter [42]. This reduces the input referred noise power to -70 dB, but requires the

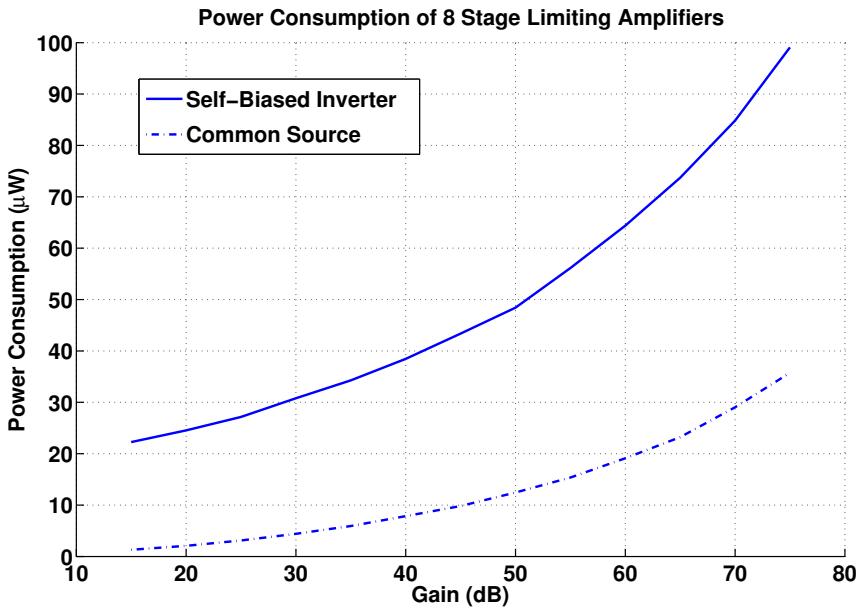

Figure 2.5: Gain versus power consumption for common source and self-biased inverter limiting amplifiers.

use of a large external capacitor.

Although the common source architecture consumes less power it is not necessarily the best choice for a low power wireless sensor receiver. If the passive front-end discussed in Section 2.4.1 is used, the baseband noise requirements are severely increased and the self-biased inverter architecture should be used. The common source architecture can be used only if sufficient gain is provided by the LNA, mixer, and baseband filter. It should be noted that although the self-biased inverter amplifier consumes more power than the common source amplifier, the combination of the passive front-end and

self-biased limiter provides the overall lowest power solution for a wireless sensor receiver.

2.5 Conclusion

Wireless receivers suitable for low power sensor networks have been examined on both the system and circuit level. It has been shown that significant power savings can be achieved by moving the the majority (if not all) of the receiver gain to the baseband filter and amplifier. Although this method reduces the sensitivity of the system, the linearity can be greatly increased while still maintaining the required noise specifications for multi-hop wireless sensor networks.

On the circuit level we have found that at extremely low power operation, self-biased and common gate LNAs provide the best noise performance. Completely passive front-ends also show a very promising approach for wireless sensor networks as they consume no power and add very little noise and distortion to the system.

G_m-C filters offer the lowest power consumption and area and can be tuned with currents rather than large capacitor arrays. The limiting amplifiers examined show a significant tradeoff between power consumption and noise. To allow the overall lowest power operation in the receiver, a limiting amplifier with higher power consumption and lower noise may need to be used.

Techniques to increase linearity in ultra low power active LNAs and mixers are important. In baseband circuits, low power and low area self-tuning schemes for continuous time g_m-C filters would greatly reduce the deployment time for large sensor

networks. Noise reduction and low area DC biasing for limiting amplifiers are also important considerations.

Chapter 3 – A BFSK Super-Regenerative Transceiver for Low-Power Applications

3.1 Abstract

A new super-regenerative transceiver for use in low power binary frequency shift keying (BFSK) digital communication systems is presented. The classic on/off keying (OOK) design is reviewed and motivation to extend the design to BFSK is given. The system is shown to preserve the low power qualities of the classic super-regenerative transceiver while obtaining the increased speed and reliability of BFSK modulation. Operation of the new system is explained on the system level and insight into the circuit design is also given. Simulations show the transceiver allows transmission rates on the order of 250 kbps with a link power of less than 1.4 mW.

3.2 Introduction

As wireless sensor networks become more common, the need for reliable data transfer and higher bandwidth is increased. Although networks are getting larger and processing higher amounts of data, the amount of power available still remains minimal. As a result, the functionality of each sensor node in large sensor networks is reduced to the sensor and sensor interface, data storage, and a wireless communications interface. The

low duty cycle of the sensor, along with improvements in non-volatile memory, give the wireless communication interface the largest power consumption in each sensor node. In order to maintain long periods of autonomous operation, the power consumption of the wireless interface needs to be minimized while not sacrificing performance.

Large scale wireless sensor networks contain hundreds or even thousands of nodes that need to communicate data quickly and efficiently to conserve energy. Typically, data is sent in a multi-hop peer-to-peer fashion until it reaches a hub where the data is stored. This multi-hop data transmission takes place among sensor nodes spaced within 10m of one another. These short hops allow large power savings as high gain power amplifiers are not needed and the transceiver power budget is more evenly distributed between the transmitter and receiver [14].

Super-regenerative transceivers have recently been proposed [45–48] that achieve very low power operation, but suffer from low bit rates or rely on specially processed off-chip resonators. This paper presents a new ultra low power super-regenerative transceiver that employs binary phase shift keying to increase bit rates without the need for expensive off-chip components.

3.3 The Classic OOK Super-Regenerative Receiver

Low power digital communication systems typically use simple binary modulation schemes such as on/off keying (OOK), binary frequency shift keying (BFSK), or binary phase shift keying (BPSK). The choice of modulation scheme then determines the architecture of the transceiver. Typically, as spectral efficiency and bandwidth increase, so does the

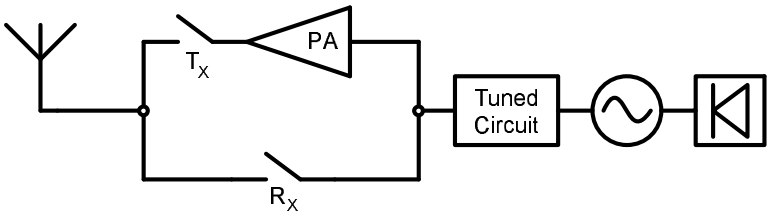

Figure 3.1: Block diagram for the classic super-regenerative transceiver.

power consumed by the transceiver.

BPSK allows very high spectral efficiency and high data rates, but usually requires an analog-to-digital converter and a stable reference frequency to demodulate the received signal; both of which consume large amounts of power [49]. If BFSK is used, the signal can be demodulated in the analog domain and, depending on the modulation index used, an accurate reference signal may or may not be necessary. This allows the receiver design to be simplified and power to be saved. OOK offers the lowest power solution because demodulation does not require an accurate reference signal nor does the signal need to be quantized before demodulation. Although an OOK modulation system can consume extremely low power, it is seldom used due to low data rates associated with long settling times and increased sensitivity to interferers [15].

OOK modulation allows extremely low power operation through the use of the super-regenerative transceiver, shown in Fig. 3.1. In transmit mode, the oscillator is modulated by the baseband data source. Therefore, when a '1' is to be transmitted, the power amplifier (PA) transmits the carrier frequency and when a '0' is to be transmitted, the oscillator and PA are turned off. This allows for power savings in the transmitter

because the oscillator and PA are turned off during parts of the transmission. While lowering the transmit duty cycle allows power savings, turning off the transmitter also greatly reduces the speed of OOK modulation because each bit period needs to be long enough for the oscillator to build up oscillations.

The super-regenerative receiver consists of a tuned circuit, an oscillator, and an envelope detector. In receive mode, the oscillator is held at the edge of oscillation and is reset periodically by a quench signal with a frequency that is at least twice the bit rate. If a '1' is transmitted, the oscillations quickly build due to the incoming signal. When the transmitter is turned off (a '0' being transmitted), the oscillations in the receiver take much more time to build. The envelope circuit then detects the oscillations in each quench cycle to determine whether the transmitted signal is a '0' or a '1'.

3.4 The BFSK Super-Regenerative Receiver

The proposed BFSK super-regenerative transceiver system is shown in Fig. 3.2. Like the classic system, the BFSK system uses the same antenna to transmit and receive. The transceiver core is interfaced to the antenna by a simple power amplifier on the transmit side and a duplexing switch on the receive side. The transmitter only transmits over distances on the order of 10 m so it can be realized by a simple on-chip push-pull amplifier.

In transmit mode, the oscillator runs continuously while its center frequency is modulated by the baseband data signal. The carrier signal is generated directly by an LC oscillator eliminating the need for external carrier generation. This preserves the poten-

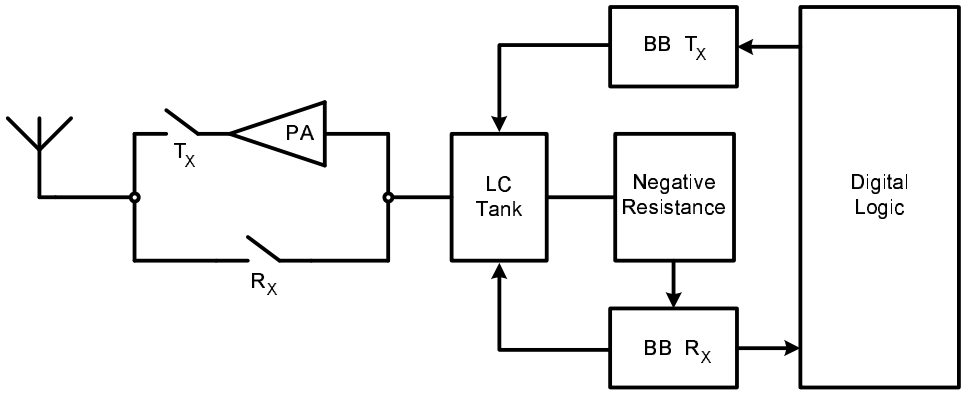

Figure 3.2: Block diagram for super-regenerative BFSK transceiver.

tial for low power signal transmission as in the OOK design, but with the higher data rates used in conventional BFSK systems.

In receive mode the LC tank is modulated between the two BFSK frequencies (f_H and f_L) at the same rate that the oscillator is quenched. When the received signal is matched to that of the tank frequency, the LC tank provides a voltage gain that in turn determines the time to build up oscillations (TTO). Figure 3.3 shows the time taken to build oscillations for a 920 MHz LC oscillator when excited by a sinusoidal source of varying amplitude. The very small input amplitudes in Fig. 3.3 represent the case when the received signal does not match the tank frequency. When the frequencies of the received signal and the oscillator tank match, the input signal voltage becomes larger and the TTO is decreased.

For the duration of a single bit, the input to the receiver will have a fixed amplitude and frequency. This input is sampled by the receiver at both f_H and f_L before the TTO of each tank is compared to determine the incoming bit. In order for the receiver to meet

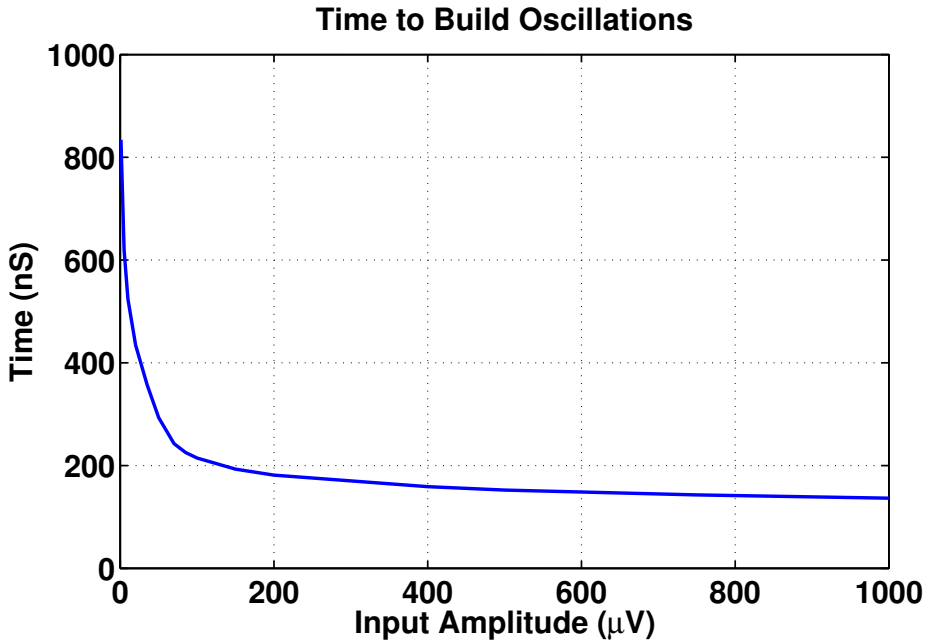

Figure 3.3: Time to oscillate for an LC oscillator with an f_0 of 920MHz excited by an input source of varying magnitude.

the required Nyquist criteria, the sampling rate needs to be at least twice the bit rate. Thus, the minimum quench rate for the receiver is four times the data rate; twice the bit rate for each tank frequency.

Figure 3.4 illustrates the receiver operation. When the V_{ctrl} signal is low the tank frequency is tuned to f_L and when V_{ctrl} is high, the tank is tuned to f_H. At the end of each cycle the quench signal goes high and the oscillator nodes are reset before the input is sampled again. In Fig. 3.4, the receiver is being excited with a source operating at f_H. When the receiver is tuned to f_L (the time period between 1.25 μs and 2.25 μs in

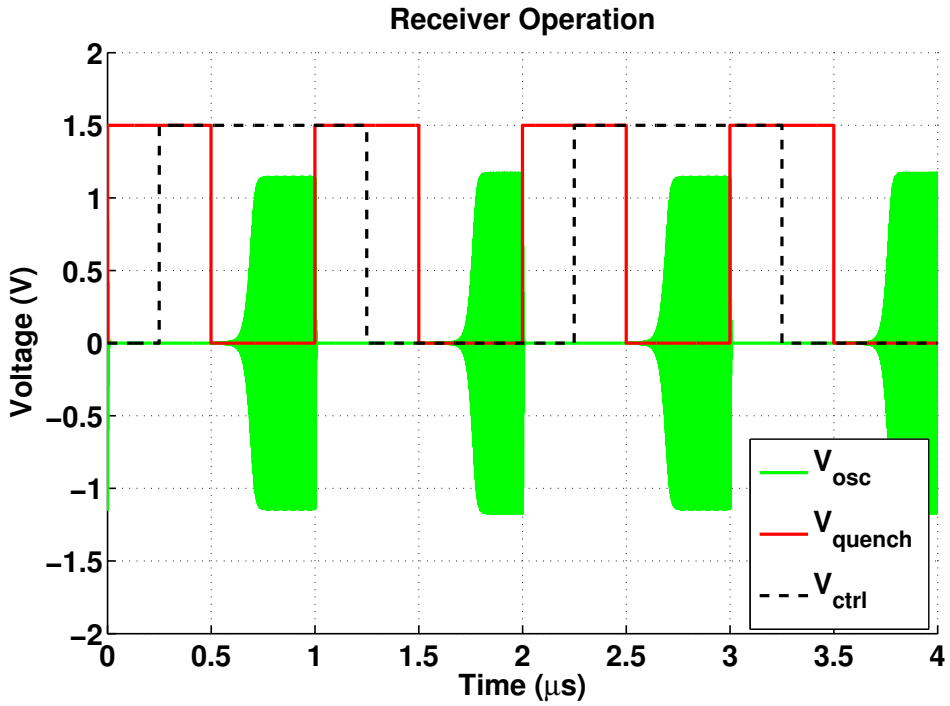

Figure 3.4: Operation of the super-regenerative BFSK receiver.

Fig. 3.4), the oscillators TTO is about 280 nS. After the oscillator is quenched and the tank is tuned to f_H (the time period between 2.25 μs and 3.25 μs in Fig. 3.4), the TTO drops to about 210 nS. By sensing that the TTO of f_H is less than the TTO of f_L, the decision that the incoming signal is at f_H is made.

This architecture allows the extreme low power capability of the super-regenerative receiver to be coupled with the speed and reliability of the BFSK system. Typically, a BFSK system would be constructed with the classic superheterodyne or homodyne structure that requires several circuit blocks and higher power consumption. Here, the

same low power circuitry is used for both the transmitter and receiver saving die area, design time, and power consumption.

3.5 Circuit Design

Figure 3.5 shows the circuit used for the super-regenerative core. The oscillation frequency is set by the LC tank combination along with the parasitic capacitances of the surrounding components. The ability for the oscillator to build oscillations quickly without consuming a large amount of power depends greatly on the Q of the tank inductor. This inductor should be realized with bondwires or an off chip component in order to minimize the series resistance [50].

The oscillators negative resistance is constructed by the complementary cross coupled pairs, made up of transistors M1 through M4. The oscillator is quenched with M6, which shorts the two oscillating nodes. The amount of time needed for each quench period depends on the RC time constant created by the closed switch resistance and the tank capacitance. The switch should be sized large enough to allow the oscillations to die quickly when quenched, but not so large that the charge injection causes premature build up of oscillations. Transistor M5 aids in quenching the circuit quickly, while also reducing the amount of current consumed. Appropriate sizing of M5 limits the current in the cross coupled pair when sampling while also allowing the current to be completely cutoff when the circuit is being quenched.

The speed at which the circuit can run as well as the minimum separation between the two frequencies depend on the Q factor of the tank circuit. The Q factor of a parallel

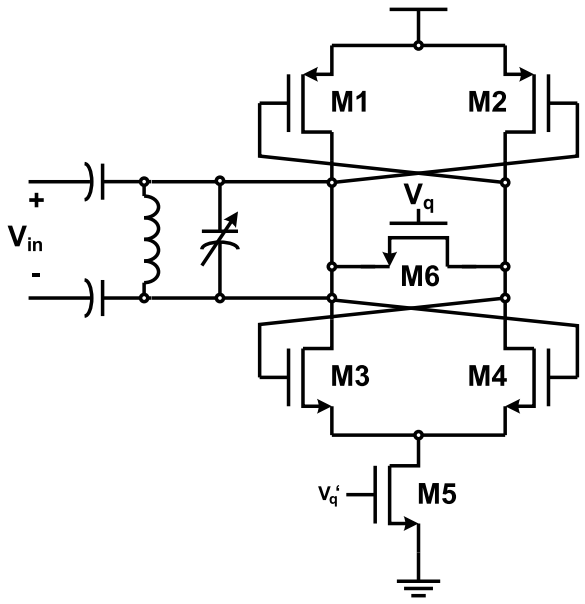

Figure 3.5: Ideal BFSK super-regenerative core circuit.

tank circuit is given by [33]

$$Q = \frac{R}{\sqrt{L/C}} \tag{3.1}$$

where L is the tank inductance, C is the tank capacitance, and R is the effective parallel resistance. As the Q of the tank is increased (by increasing the C/L ratio for a given center frequency) the minimum Δf ($f_H - f_L$) decreases. This allows for a more efficient use of the spectrum at the cost of either a slower sampling rate, or increased power.

The TTO values for f_H and f_L are converted to a voltage using a simple full wave rectifier. Two of the circuits in Fig. 3.6 are used to detect the signal; one for each of the tank frequencies. The two tank switches are connected to the oscillator nodes and closed when the tank is tuned to the correct frequency. The rectifier then charges the ca-

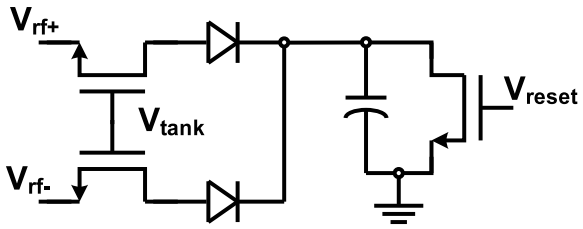

Figure 3.6: TTO conversion rectifier circuit.

pacitor to a value that is proportional to the amount of time for which the oscillations are sustained. The switches are then opened and the value is held while the other rectifier circuit samples the other tank frequency. When both tank frequencies have been sampled, the voltage stored on the two capacitors are compared to determine the frequency of the incoming signal. Once the comparison has been made, the reset switch removes the charge from the capacitor before the next comparison is made.

The signals stored on the capacitors are compared by the comparator shown in Fig. 3.7. The circuit is clocked by M1 which also acts as the current source. When M1 is turned on, transistors M2 and M3 amplify the incoming signal. M2 and M3 are realized with PMOS transistors in order to eliminate additional bias circuitry needed to keep the input pair in saturation. M4 and M5 form the cross coupled pair that latches the circuit to the correct output value. When the clock goes high and M1 is cutoff, M6 shorts the outputs together in order to remove any memory from the previous decision.

Table 3.1 summarizes the specifications and power estimation for the transceiver. The PA power is estimated based on the assumption that -10 dBm is transmitted with 25% efficiency. All other power estimates are based on circuit simulations in a 0.25

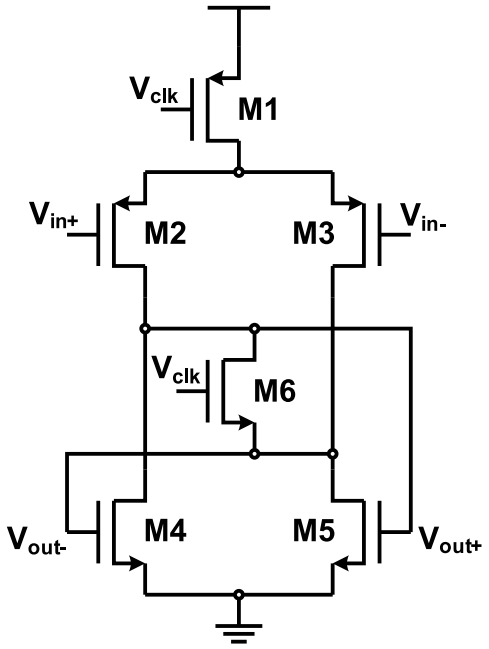

Figure 3.7: Low power comparator circuit.

μm process operating with a 1.5 V power supply. The transmitter signal generation is simulated with a center frequency of 910 MHz while the varactor is being modulated at a frequency of 250 kHz.

The receiver is simulated with a -73 dBm input signal power and a quench signal of 1 MHz, corresponding to a maximum received bit rate of 250 kbps. The receiver consumes about 366 μA with a peak current of 1.3 mA, but maintains an average current of 183 μA because the quench signal has a 50% duty cycle. The comparator sources a peak current of 17 μA and has an average current of 4 μA while operating with a 25% duty cycle.

A comparison between this work and other recent publications on super-regenerative

Table 3.1: Specifications and power estimation for the BFSK super-regenerative receiver.

Technology		0.25 μm	
Frequency Band		900 MHz-ISM	
Data Rate		250 kbps	
Quench Signal		1 MHz	
Power Supply		1.5 V	
Tx	Signal Gen.	PA	**Total**
	660 μW	400 μW	**1.06 mW**
Rx	Receiver Core	Comparator	**Total**
	275 μW	6 μW	**281 μW**

Table 3.2: Comparison to recent fabricated super-regenerative receiver designs.

Ref.	Year	Technology	Frequency	Data rate	Power
[45]	2000	0.8 μm BiCMOS	868 MHz	150 kb/s	2.7 mW
[46]	2001	0.35 μm	1 GHz	100 kb/s	1.2 mW
[47]	2005	0.13 μm	2.4 GHz	500 kb/s	3.6 mW
[48]	2005	0.13 μm/FBAR	1.9 GHz	5 kb/s	400 μW
—	**2006**	**0.25 μm**	**900 MHz**	**250 kb/s**	**281 μW**

receivers is shown in Table 3.2. This design provides one of the highest data rates of all the designs with the lowest power consumption. It is also designed in a standard CMOS process while other designs require more expensive BiCMOS or MEMs fabrication. It should be noted that the specifications from the other designs in Table 3.2 are based on measured data. The work presented here uses simulations to show the potential for increased data rates while greatly reducing the power consumption.

3.6 Conclusion

A new super-regenerative transceiver using BFSK modulation has been presented. The issue of slow data transmission usually associated with super-regenerative receivers has been avoided by allowing the oscillator to run continuously when data is transmitted. By modulating the oscillators tank frequency, data can be rapidly transmitted and received using the same core circuitry.

The transceiver requires only a single external inductor that can be realized with a bondwire or a discrete component, while the rest of the circuitry can be realized in a standard CMOS process. By carefully choosing the component values for the LC tank, the designer can trade power consumption for bandwidth and a lower modulation index. Simulations in a 0.25 μm process show a power consumption of just over 1 mW for the transmitter and less than 300 μW for the receiver giving a total link power of less than 1.4 mW.

Chapter 4 – A 0.4 nJ/b 900MHz CMOS BFSK Super-Regenerative Receiver

4.1 Abstract

An ultra low-power super-regenerative receiver for BFSK signals has been designed and fabricated in a standard 0.18 μm CMOS process. The use of BFSK allows the receiver to operate at higher data rates and also gives an approximate 3 dB SNR performance increase over the more traditional OOK modulation. At 1 Mb/s the receiver consumes 0.4 nJ/b making it the lowest energy integrated super-regenerative receiver to date.

4.2 Introduction

As the field of ultra low-power electronics progresses, wireless sensor networks (WSNs) are becoming more common in our daily lives. The amount of data these networks need to collect, process, and communicate continues to increase while the amount of power they consume needs to remain minimal. In addition, many networks need to operate autonomously for long lengths of time from a single battery, or energy scavenged from the surrounding environment [14].

The super-regenerative architecture has long been known to provide a good solution for low-power receivers. To date, several designs [46, 48, 51, 52] have demonstrated

very low power operation, but typically have low data rates or rely on special micro electromechanical systems (MEMS) processing. This is partially due to that fact that the designs all employ On / Off Keying (OOK) which suffers from low data rates due to issues both at the circuit and system levels.

On the system level, binary frequency-shift keying (BFSK) signaling is generally preferred over OOK because FSK is less susceptible to fading and noise. An OOK signal needs about 3 dB more signal-to-noise ratio (SNR) than a BFSK signal to achieve the same theoretical bit-error rate (BER) [53]. On the circuit level, the maximum data rate in an OOK system is determined by the amount of time the transmit oscillator needs to build oscillations when a '1' is being sent and also by the amount of time needed for the oscillations to die out when a '0' is being sent. In cases when a high-Q MEMS resonator is used to minimize power consumption, the turn-on and turn-off times of the oscillator increase which further reduces the data rate.

This paper describes a super-regenerative receiver for BFSK signals. The use of BFSK signaling allows this receiver to increase data rates and reliability over the traditional OOK approach while still maintaining extremely low-power operation with only a single external inductor. Section 4.3 describes the BFSK receiver operation and low power design techniques for the oscillator and baseband circuits. The measured results for a fabricated test chip are reported in Section 4.4 and finally Section 4.5 provides conclusions.

4.3 Circuit Design

A simplified block diagram for the BFSK super-regenerative receiver is shown in Figure 4.1. The BFSK super-regenerative receiver operates by comparing the amplified signal from two different frequencies rather than a single frequency as in the classic design. During each incoming bit period the oscillator is quenched twice, once when the tank is tuned to f_1 and again when the tank is tuned to f_2. Oscillations will build at both frequencies, but they will build much faster when the tank is tuned to the same frequency as the input signal. This is because the LC tank will provide voltage gain to the incoming signal when both the tank and the signal are at the same frequency. A complete system level analysis of the BFSK super-regenerative receiver can be found in Chapter 3.

The oscillations from both tank frequencies are then rectified and compared to determine the incoming data. The tank frequency with the largest rectified voltage is the frequency of the incoming signal. The receiver is made up of the core oscillator, baseband circuitry which consists of rectifiers and a comparator, and the digital control circuitry that provides the timing for all the circuit blocks and data alignment. The following subsections will describe the implementation of each of these blocks in detail.

4.3.1 Oscillator

A schematic of the core oscillator circuit and quench switch is shown in Figure 4.2. A differential input signal enters the oscillator through the two series capacitors that serve as part of the input matching network while also preserving the DC operating point of

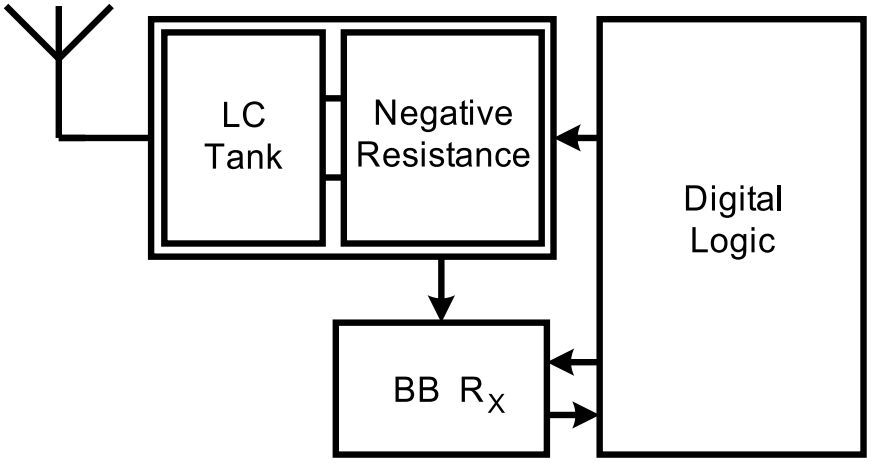

Figure 4.1: Simplified block diagram for BFSK super-regenerative receiver.

the oscillator.

The oscillator core is constructed using an LC tank architecture with both NMOS and PMOS cross-coupled pairs to maximize the total g_m. The LC tank is made up of a single external inductor and two integrated varactors, 1 large and 1 small. The large varactor is controlled by an off chip analog control voltage to allow the center frequency of the oscillator to be tuned anywhere in the 900 MHz ISM band. The smaller varactor is controlled by a digital signal that is switched continuously during operation to re-tune the oscillator between f_1 and f_2. Depending on the desired bandwidth and power requirements of the system the Δf (f_2-f_1) can be easily controlled by varying the amplitude of the digital control signal.

The negative resistance of the oscillator is made up of two sets of source degenerated cross-coupled pairs (M_1 - M_4). The source degeneration helps to regulate the g_m of the transistors while also providing a greater immunity to the g_m drift over temperature. A

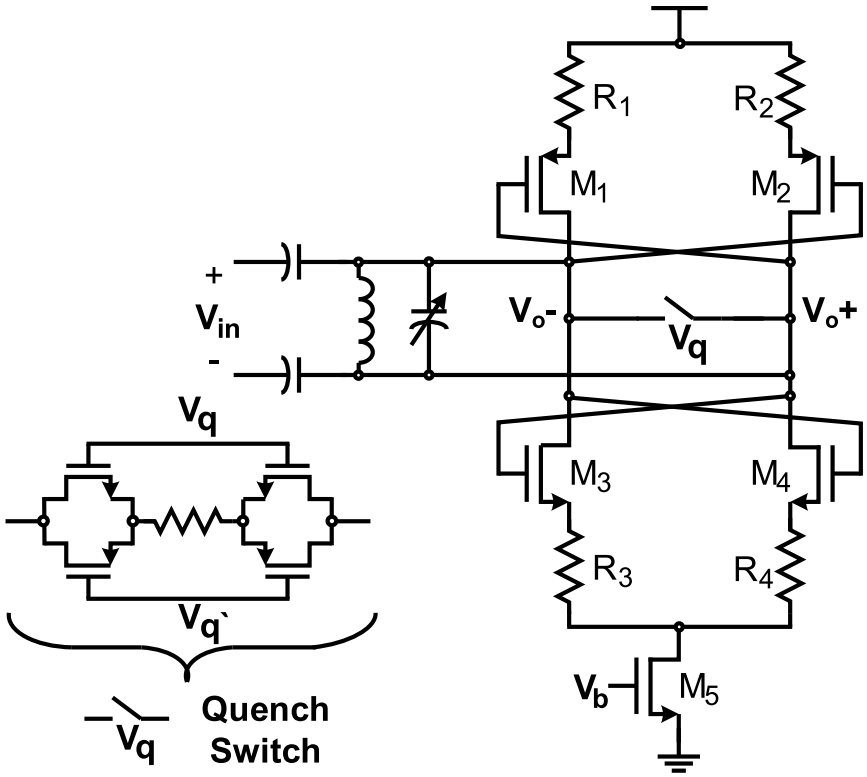

Figure 4.2: Schematic of the core oscillator.

triple-well process is used which allows the substrate connection of both sets of transistors to their sources in order to minimize the threshold voltages and hence, the amount of voltage headroom needed.

Transmission gates are used in the quench switch in order to minimize the variance in switch conductance across the entire range of oscillation. The resistor in the quench switch provides the signal that allows the oscillations to build when the switch is opened. When the oscillator is quenched (i.e., the switches are closed), the quench switch resistor dissipates all of the power in the input signal creating a small voltage across the

tank. When the switch opens, the small voltage generated by the resistor determines the amount of time the oscillator takes to build oscillations. The resistor value also determines how fast the oscillations die out when the circuit is quenched. Therefore, the resistor value must be optimized for both speed and sensitivity. If its value is large, the resulting voltage drop across the resistor will also be larger which will increase the receiver's sensitivity. If it is made too large the oscillator will take longer to quench, which will reduce the maximum quench rate, and hence the maximum data bandwidth.

The quench switch is driven digitally by the digital control logic. The differential control signal is generated by two capacitively loaded inverters. The capacitive loading creates a ramp function that reduces the amount of charge injection created by the quench switch in order to eliminate false triggering of the oscillator.

4.3.2 Baseband Circuitry

In order to determine the incoming signal frequency, the oscillations generated by the oscillator at f_1 and f_2 need to be "down-converted" and compared. This is accomplished by the use of two passive rectifiers and a comparator. The rectifier schematic is shown in Figure 4.3.

As in the quench switch, the rectifier switches are also realized using transmission gates to maximize switch conductance across the entire swing of the input oscillations. The rectification is performed by the diode-tied NMOS transistors M_1 and M_2 whose substrate connections are tied to their sources to maximize their efficiency. The charge that is collected from the oscillations is stored on a large capacitor. For the duration of

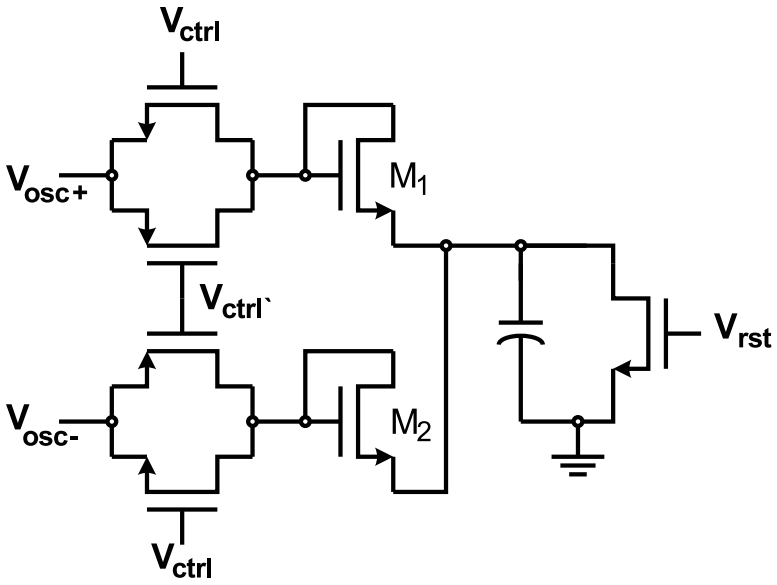

Figure 4.3: Schematic of the passive rectifier.

the rectification the capacitor charging remains in the linear (constant current) region and does not charge completely. This ensures an approximately linear relationship between the duration of the oscillations and the voltage stored on the capacitor which maximizes the voltage difference between the two rectified voltages.

Two rectifiers store the voltages for f_1 and f_2 so they can be compared. The v_{ctrl} signal for f_1 first closes the switches to allow the f_1 signal to be obtained, then the switches open and the signal is held while the signal for f_2 is obtained. Once the comparison has been made the reset signal is applied simultaneously to both of the reset switches and the capacitor is reset.

The comparison between the two rectified signals is performed by the latched comparator shown in Figure 4.4. The amount of offset that is present in the comparator will

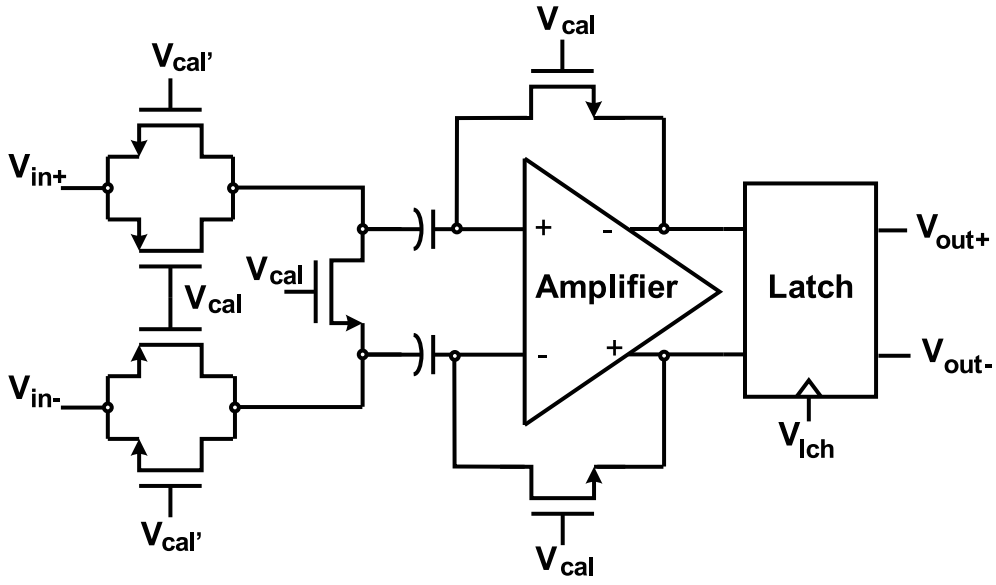

Figure 4.4: System level schematic of the comparator.

limit the overall sensitivity of the receiver as it will determine the smallest signal from the rectifier that can be resolved. To improve the overall sensitivity of the system, offset correction in the comparator is used. During the calibration stage the input of the comparator is disconnected from the rectifier and the calibration switches store the amplifier offset on the input capacitors where it will be subtracted from the input signal when it is sampled.

The comparator's preamplifier is shown in Figure 4.5. PMOS inputs are used in the amplifier to accommodate the low common mode voltage of the rectified signal. The impedance of the diode connected loads (M_4 and M_5) is boosted by the addition of the cross-coupled devices (M_6 and M_7). These cross-coupled devices are sized to be slightly smaller than the diode connected load to reduce their effective g_m (and increase

the amplifier gain) while still maintaining amplifier stability.

The cross-coupled latch is shown in Figure 4.6. When the V_{lch} signal is high the NMOS and PMOS cross-coupled pairs are disconnected and the outputs are both pulled low. When the V_{lch} signal goes low, the pull-down switches on the output open and the two cross-coupled pairs use positive feedback to amplify the signal from the preamplifier to force a binary decision. When the comparators decision is made the top two PMOS switches turn off to eliminate the DC current that flows while the output is valid.

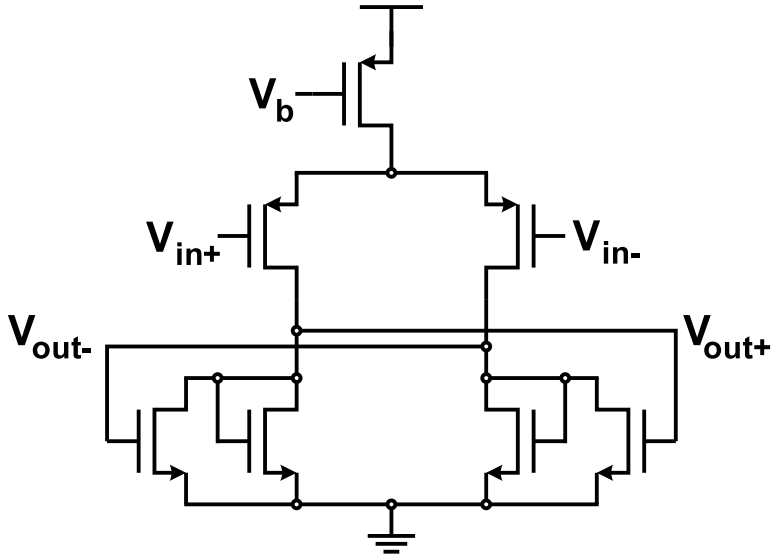

Figure 4.5: Preamplifier schematic for the latched comparator.

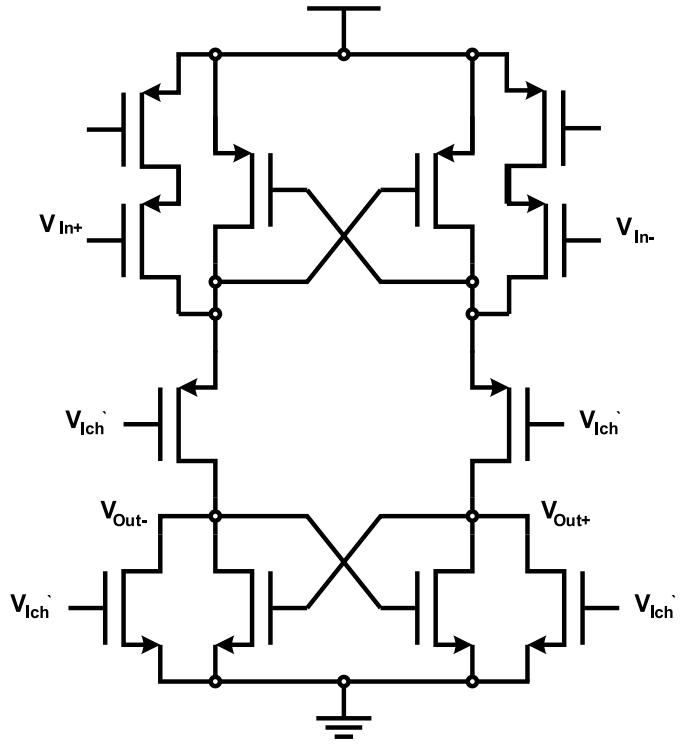

Figure 4.6: Latch schematic for the latched comparator.

4.4 Measurement Results

The receiver was fabricated in a 0.18 μm triple-well CMOS process and is shown in Figure 4.7. The digital logic is not shown in the photo because it was spaced away from the analog circuity (about 300 μm to the right) in order to minimize substrate noise coupling. The total active area of the receiver including the testing buffers and digital logic (excluding pads) is less than 0.15 mm^2.

Figure 4.8 shows the measured signals when the receiver is running at 500 kb/s (1 MHz quench). The bottom of Figure 4.8 shows the output of the two rectifiers while

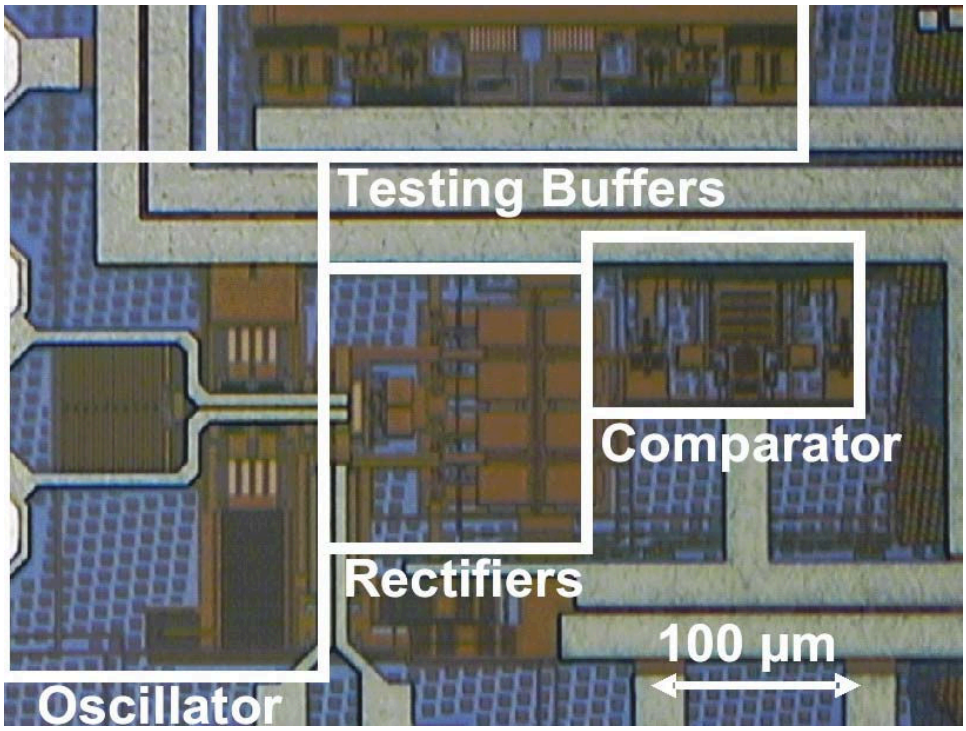

Figure 4.7: Chip photograph.

the top shows the resulting data. At 1 μs both of the rectifiers are reset and the rectifier corresponding to f_2 acquires the signal from the oscillations generated by the incoming signal. The voltage on the f_2 rectifier is held while the signal for f_1 is acquired. Since the input to the receiver is at f_1 the rectifier corresponding to f_1 builds a larger voltage and when the decision is made (at 3 μs) the data signal goes low.

The bit error rate (BER) measurements for the receiver are shown in Figure 4.9. For each point in Figure 4.9 a sequence of over 4 million normally distributed random points were collected. The receiver is most sensitive at low data rates as it has more

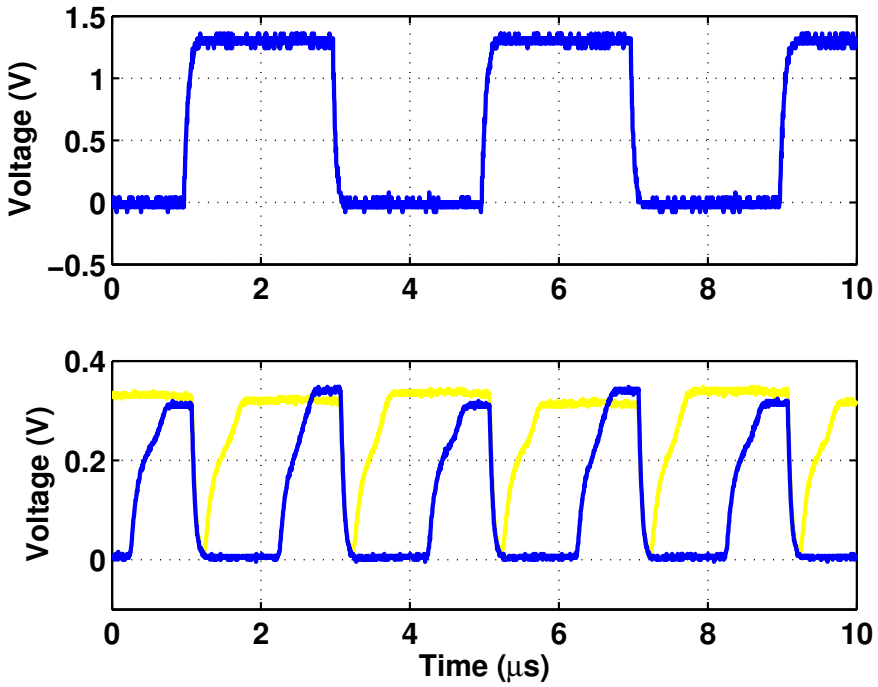

Figure 4.8: Measured receiver operation for a '1010' pattern at 500 kb/s.

time to build oscillations from small input signals. The minimum measured BER for the receiver is just under 5x10^{-7} and is achieved at all data rates for input power levels greater than or equal to -68 dBm. A maximum sensitivity of -90 dBm is achieved when operating at 250 kb/s.

The receiver consumes 244 μW, 300 μW, 340 μW, and 400 μW from a 1.3 V supply while operating at 250 kb/s, 500 kb/s, 750 kb/s, and 1 Mb/s, respectively. The highest efficiency is achieved at 1 Mb/s where the receiver consumes 400 pJ/b.

Table 4.1 compares the receiver to recently published super-regenerative receivers

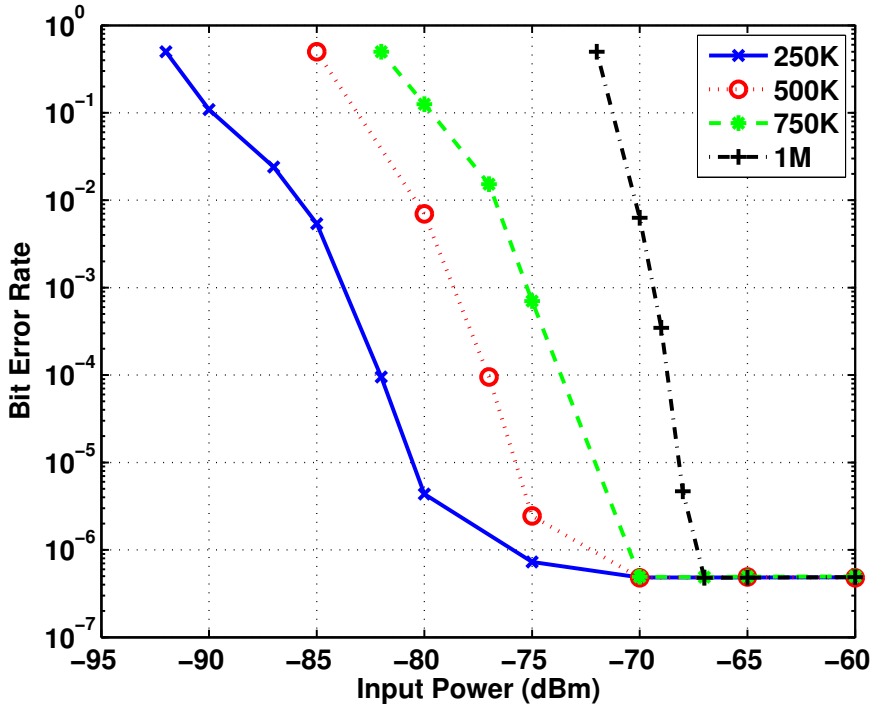

Figure 4.9: Measured bit error rate versus input power for different data rates.

Table 4.1: BFSK super-regenerative receiver compared to other recent super-regenerative designs.

	Vouilloz '01	**Otis '05**	**Chen '07**	**M.-Geniz '07**	**This Work**
Frequency	1 GHz	1.9 GHz	2.4 GHz	2.4 GHz	900 MHz
Modulation	OOK	OOK	OOK	OOK	BFSK
Data Rate	100 kb/s	5 kb/s	500 kb/s	11 Mb/s	1 Mb/s
Power	1.2 mW	400 μW	2.8 mW	2.1 mW	$\geq$ 244 μW
Energy	12 nJ/b	80 nJ/b	5.6 nJ/b	0.19 nJ/b	0.4 nJ/b
Sens. (BER$\leq 10^{-3}$)	-107.5 dBm	-100.5 dBm	-80 dBm	-80 dBm	-82 dBm
Technology	0.35μm CMOS	0.13μm CMOS	0.35μm CMOS	Discrete BJTs	0.18μm CMOS
Tank	External LC	BAW Resonator	Internal LC	Microstrip	External L

Table 4.2: Summary of measured results.

Min. Power	244 μW
Supply Voltage	1.3 V
Max. Data Rate	1 Mb/s
Min. Energy	400 pJ/b
Min. Sensitivity	-90 dBm
Frequency	900MHz ISM
Technology	0.18μm CMOS
Area	< 0.15 mm^2

and Table 4.2 summarizes the measured results. The design presented here is the lowest power super-regenerative receiver reported. It also has the highest data rate and the lowest energy per bit of any integrated super-regenerative receiver.

4.5 Conclusion

An ultra low-power BFSK super-regenerative receiver for wireless sensor networks has been presented. By quenching the receiver at twice the data rate and modulating the tank frequency BFSK can be used instead of the traditional OOK. This allows an increase in performance while still maintaining the ultra low-power design. In the oscillator, a single external inductor along with simple digital control enables low power operation. A completely passive rectifier and low power design techniques minimize the power consumed in the baseband circuitry. The prototype circuit demonstrates the smallest and lowest power integrated super-regenerative receiver.

Chapter 5 – An Ultra-Low Power Receiver for Battery-Free Wireless Sensor Networks

5.1 Abstract

An ultra low-power super-regenerative receiver for BFSK modulated signals has been designed and fabricated in a standard 0.18 μm CMOS process. The use of BFSK modulation allows the receiver to operate at higher data rates and also gives an approximate 3 dB SNR performance increase over the more traditional OOK modulation. A fast calibration scheme and the absence of an external inductor make it ideal for ultra-low power sensor networks. A power consumption of 215 μW from a 0.65 V supply and an area of 0.55 mm^2 make it ideal for highly integrated energy harvesting sensor nodes. At 2 Mb/s the receiver consumes 0.18 nJ/b making it the lowest energy integrated super-regenerative receiver to date.

5.2 Introduction

Wireless sensor networks (WSNs) have been in development for several years to be used in a variety of applications from data collection to building automation. As research and technology progresses, sensors are converging on a single chip solution. This creates an almost limitless number of applications as these tiny, low cost sensor nodes can be

placed in harsh or remote environments that cannot be readily accessed.

To further develop the autonomous nature of these WSNs, energy harvesting can be used to supplement or completely replace the sensors battery [54]. This will greatly extend the network lifetime while also greatly reducing (or completely eliminating) the need for human interaction. While the option for energy harvesting is available in most situations, the amount of power available is usually very low putting tight constraints on the power consumption of the sensor node. The lifetime of the sensor node is determined by the energy consumption making it critical for battery-free WSNs to be designed to consume the lowest amount of energy possible.

A typical WSN sensor node consists of a sensor, digital controller, memory, and a wireless transceiver. Of these four parts, the wireless transceiver typically consumes the greatest amount of power [14]. If the sensor node needs to sustain itself on energy harvested from the environment, then the wireless communication needs to operate on very low power while also minimizing the amount of energy consumed per bit.

Two solutions are currently used for low power and low energy wireless receivers. The first is the super-regenerative architecture which holds a tuned oscillator on the cusp of oscillation and allows oscillations to build when a signal is present [55]. Super-regenerative receivers typically use On-Off Keying (OOK) modulation and offer the lowest power solution due to their simple system architecture and demodulation [46, 48, 51, 56–61]. Because the signal amplification is nonlinear, super-regenerative receivers have lower data rates than the higher power direct-conversion architecture as only a single bit can be determined for each sampling period.

Ultra-Wide band (UWB) receivers have also recently been used to achieve low en-

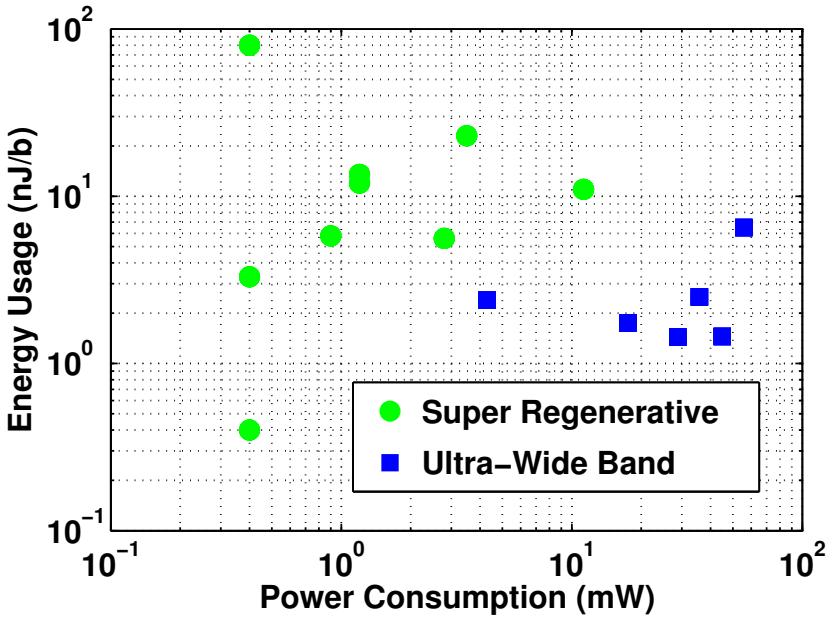

Figure 5.1: Comparison of power consumption and energy usage of several recently published low power wireless receivers.

ergy data reception. In these receivers a direct-conversion or low-IF RF front end is used along with a frequency shift keying (FSK), phase shift keying (PSK), or pulse position (PPM) modulation scheme [62–67]. These receivers generally consume much more power than the super-regenerative architecture, but have much higher data rates due to their linear signal amplification and more complex modulation schemes. These higher data rates allow the UWB receivers to have very efficient communication as they can transmit a large amount of data in a very short amount of time.

Fig. 5.1 shows several recently published super-regenerative and UWB receivers [46,

48, 51, 56–67]. As mentioned previously, the super-regenerative designs typically offer a very low power solution for wireless receivers, but due to their use of OOK most operate on the order of 10 nJ/b. Alternatively, the UWB receivers consume much more power than the super-regenerative receivers, but due to their high data-rates they offer more efficient operation with energy usage on the order of 1 nJ/b. In order to successfully operate in a battery-free WSN, it is critical to find a solution that combines the low-power operation of the super-regenerative architecture with the high efficiency of the UWB receiver.

This chapter describes a binary frequency shift keying (BFSK) super-regenerative receiver that is suitable for use in a battery-free WSN. Section 5.3 will describe the system architecture of the receiver and discuss performance tradeoffs. Section 5.4 describes the receiver's circuit implementation and measured results are discussed in Section 5.5.

5.3 The Super-Regenerative Architecture

The super-regenerative receiver is used in many low data rate, short range applications because of its simple design and low power consumption. Although recent work has shown impressive results using the super-regenerative architecture, it will never fully replace the more conventional super-heterodyne or direct conversion receivers because of basic architectural limitations.

The fundamental limitation of the super-regenerative architecture is that it relies on *nonlinear* amplification. In the more conventional super-heterodyne receiver the incoming signal is *linearly* amplified which allows either amplitude, frequency, or phase

information to be extracted from it. The super-regenerative receiver merely detects the presence of a signal at a specific frequency. When this signal goes through nonlinear amplification the exact amplitude, frequency, and phase information is lost and therefore rather than downconverting to the baseband signal (as done in a direct conversion receiver), the RF signal must be sampled at or above the desired data rate.

This fundamental limitation of the super-regenerative architecture is also the source of its strength. The nonlinear amplifier used in the super-regenerative receiver can consume much lower power than the linear circuits used in the direct-conversion receiver. In addition to this the demodulation of the sampled RF signal also becomes much simpler, although it is limited to a single bit per sample.

5.3.1 OOK Super-Regenerative Architecture

A block diagram for the basic super-regenerative architecture is shown in Fig. 5.2. It consists of an antenna, isolation amplifier, tuned oscillator and a simple demodulator.

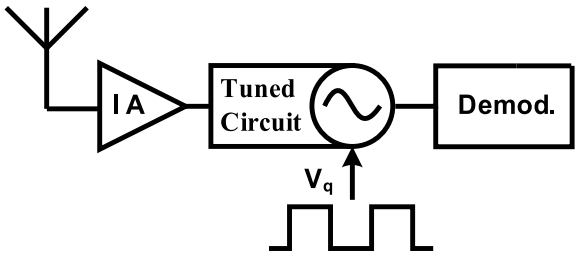

Figure 5.2: Block diagram for the basic super-regenerative receiver including isolation amplifier (IA), tuned oscillator, and demodulator.

During operation the oscillator repeatedly builds oscillations to detect the incoming signal. Initially, the oscillations are dampened so that the oscillator cannot build oscillations. In this mode of operation the oscillator is said to be “quenched”. While the oscillations are dampened in quench mode, the isolation amplifier amplifies the incoming signal. When the quench signal is released and the oscillator enters ”oscillation mode”. In oscillation mode, oscillations will build based on the input signal from the isolation amplifier. The oscillations will build quickly if a signal is present, but take a long time to build (or not build at all) if the input signal is absent. Each time the quench signal is released and oscillations build, the oscillations are rectified and compared to a reference to determine whether the incoming bit is a ‘0’ or ‘1’.

At the heart of the super-regenerative receiver is the oscillator. A conceptual schematic of a simple LC oscillator is shown in Fig. 5.3. The oscillator model contains an input excitation signal, resistor (R_p) to model the parasitic losses in the LC tank, inductor (L), capacitor (C), and an active element ($-g_m$) to represent the negative conductance added by the active devices. To find the voltage across the LC tank, we must first write the second order differential equation that describes the parallel RLC network given by:

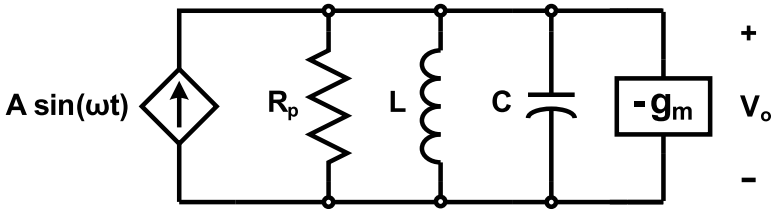

Figure 5.3: Conceptual schematic of an LC oscillator containing and inductor, capacitor, equivalent parallel resistance and a negative transconductance.

$$Asin(\omega t) = C\frac{dV_o}{dt} + \frac{1}{L}\int V_o d\tau + V_o G \tag{5.1}$$

where $G = R_p^{-1} + (-g_m)$, L is the tank inductance, C is the tank capacitance and $Asin(\omega t)$ is the input excitation current. Assuming an underdamped system and solving for V_o, the resulting voltage across the LC tank is given by [68]:

$$V_o = e^{-\alpha t}(A_1 cos(\omega_d t) + A_2 sin(\omega_d t)) + \frac{Asin(\omega t)}{\sqrt{G^2 + (\omega C - 1/\omega L)^2}} \tag{5.2}$$

where

$$\alpha = \frac{1}{2RC} \tag{5.3}$$

$$\omega_d = \sqrt{\omega_0^2 - \alpha^2} \tag{5.4}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{5.5}$$

$$A_1 = V_o(0^+) \tag{5.6}$$

$$A_2 = \frac{\frac{dV_o(0^+)}{dt} + \alpha A_1}{\omega_d} \tag{5.7}$$

and

$$R = 1/G. \tag{5.8}$$

The term proportional to the exponential function in (5.2) describes the circuit's natural response while the term proportional to the input describes the response to an

input signal.

The oscillator operates in two different modes: $\mid -g_m \mid < R_p$ and $\mid -g_m \mid \geq R_p$. When $\mid -g_m \mid < R_p$ the oscillator is in quench mode and the amount of energy put into the circuit by the active devices is not enough to overcome the losses in the tank and oscillations will not build up. Under this quenched condition, the natural response portion of the equation is negligible since the circuit was quenched and the previous oscillations were eliminated. This leaves the second term which describes the tank voltage resulting from the input signal.

When the quench signal is released $\mid -g_m \mid$ becomes greater than R_p resulting in α becoming negative. Now the exponential term in (5.2) becomes dominant and the circuit quickly builds oscillations. Under this condition the response from the input becomes negligible compared to the exponential term. To simplify the analysis we assume at the instance the quench signal is released the voltage on the tank is at its peak. Then,

$$A_1 = \frac{A}{\sqrt{R^{-2} + (\omega C - 1/\omega L)^2}} \tag{5.9}$$

$$A_2 = \frac{\alpha A_1}{\omega_d} \tag{5.10}$$

The above analysis gives two equations for the two different modes of operation in the super-regenerative oscillator. First, when the oscillator is quenched:

$$V_{o,qch} = \frac{A sin(\omega t)}{\sqrt{R^{-2} + (\omega C - 1/\omega L)^2}} \tag{5.11}$$

and when the quench signal is released and the oscillator can build oscillations:

$$V_{o,osc} = e^{-\alpha t}(A_1 cos(\omega_d t) + A_2 sin(\omega_d t)) \tag{5.12}$$

where A_1 and A_2 are given in (5.9) and (5.10), respectively.

Another important parameter in the super-regenerative oscillator is the LC tank Q. The Q of the LC tank is described by [33]:

$$Q = \frac{\omega_0}{BW_{3dB}} = \frac{|R|}{\sqrt{L/C}} \tag{5.13}$$

where BW_{3dB} is the 3 dB bandwidth of the LC tank and R, L, C, and ω_0 are as previously stated. (5.13) describes an important relationship between the 3 dB bandwidth of the tank circuit and the equivalent parallel resistance. A high Q results in a very narrow 3 dB bandwidth in the oscillator which improves the receivers selectivity while also providing a higher voltage gain to the incoming signal when the oscillator is quenched. Fig. 5.4 illustrates the effect on tank Q from sweeping the $-g_m$ value in the circuit shown in Fig. 5.3. The value for R_p was chosen to give a Q of 50 for a 2.4 GHz LC oscillator with no $-g_m$ applied, which is consistent with a bondwire inductor. When the magnitude of $-g_m$ is very small compared to R_p the resulting Q of the oscillator is determined by R_p. As the magnitude of $-g_m$ is increased the Q also increases approaching infinity as the magnitude of g_m approaches $1/R_p$. Finally, as the magnitude of $-g_m$ continues to increase beyond R_p, the Q decreases approaching 0 for very large values of $|-g_m|$.

The regions to the left and right of 10^0 in Fig. 5.4 correspond to the quench mode and oscillate mode, respectively. For a given input, the behavior of the oscillator can be

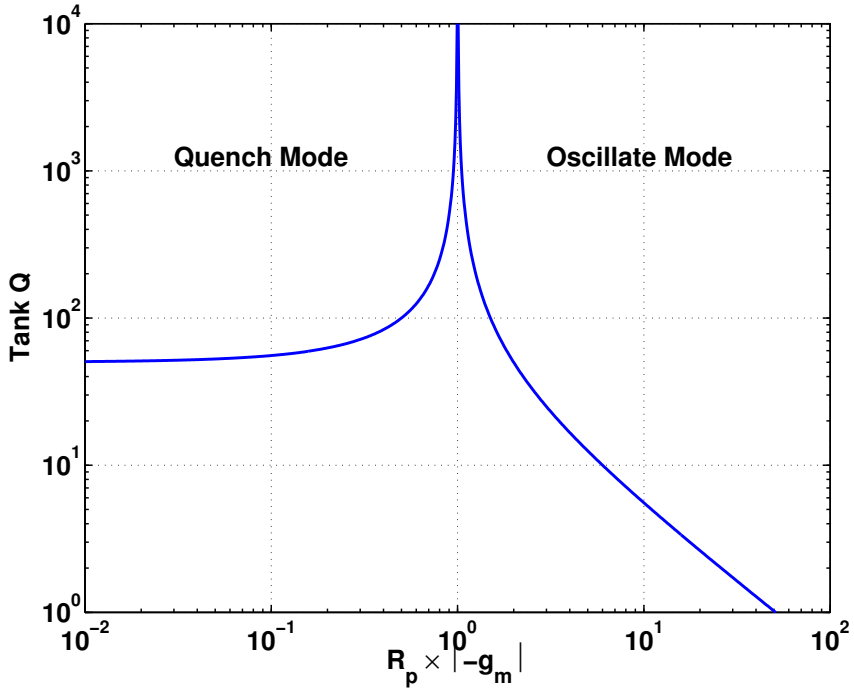

Figure 5.4: Tank Q for varying negative transconductance and a fixed R_p.

described in terms of the Q during quench mode (Q_{qch}) and the Q during oscillate mode (Q_{osc}). Fig 5.5 shows the time to build oscillations (TTO) to 1V versus Q_{qch}. This is plotted for typical values of Q_{osc} in a Q-enhanced system with a 4 nH inductor and a 1.06pF capacitor ($f_o = 2.45\ GHz$).

The speed at which the oscillations build has a much larger dependence on Q_{osc} than on Q_{qch}. A higher Q_{qch} results in a larger initial voltage on the LC tank when switched to oscillate mode and hence, oscillations build faster. The right side of Fig. 5.4 shows that Q_{osc} decreases when the negative transconductance increases (more power is added)

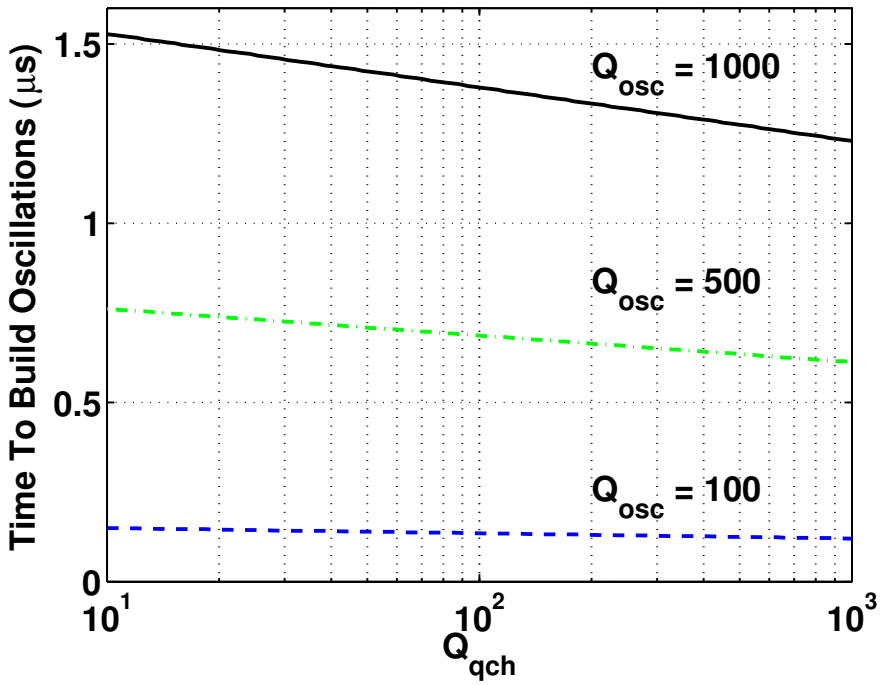

Figure 5.5: Time to build oscillations to 1V vs the oscillator quench mode Q with a -100 dBm input.

making oscillations build very quickly for lower Q_{osc} values. For high speed operation it is desirable that Q_{qch} is high, while Q_{osc} is low.

5.3.2 BFSK Super-Regenerative Architecture

The BFSK super-regenerative receiver architecture is similar to the OOK architecture but rather than having a single frequency channel, the BFSK architecture compares the oscillations at two different frequencies [69]. During each incoming bit period, the input

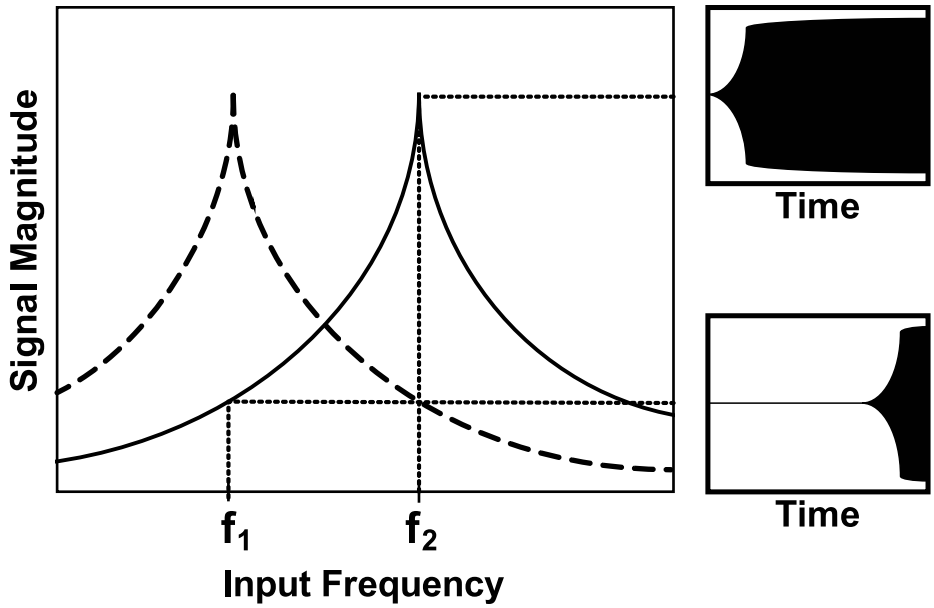

Figure 5.6: Frequency response of the LC oscillator when tuned to f_2 and the resulting oscillation from input signals at f_1 and f_2.

is sampled at two different frequencies (f_1 and f_2) and then the two are compared. First, the LC tank is tuned to f_1 and the resulting oscillations are rectified and stored. The oscillator is then tuned to f_2 and the oscillations that build at f_2 are also rectified and stored. Finally, the two rectified voltages are compared to see if the input frequency is f_1 or f_2 and hence if the input is '0' or '1'.

The signal resolved by the comparator represents the difference in the TTO when the oscillator is tuned to f_1 and the TTO when the oscillator is tuned to f_2. As shown in Fig. 5.6, if the incoming signal is at f_2 and the oscillator is tuned to f_2 oscillations will quickly build. When the oscillator is tuned to f_2 while the incoming signal is at f_1 the initial magnitude on the LC tank will be lower and the oscillations will take longer to

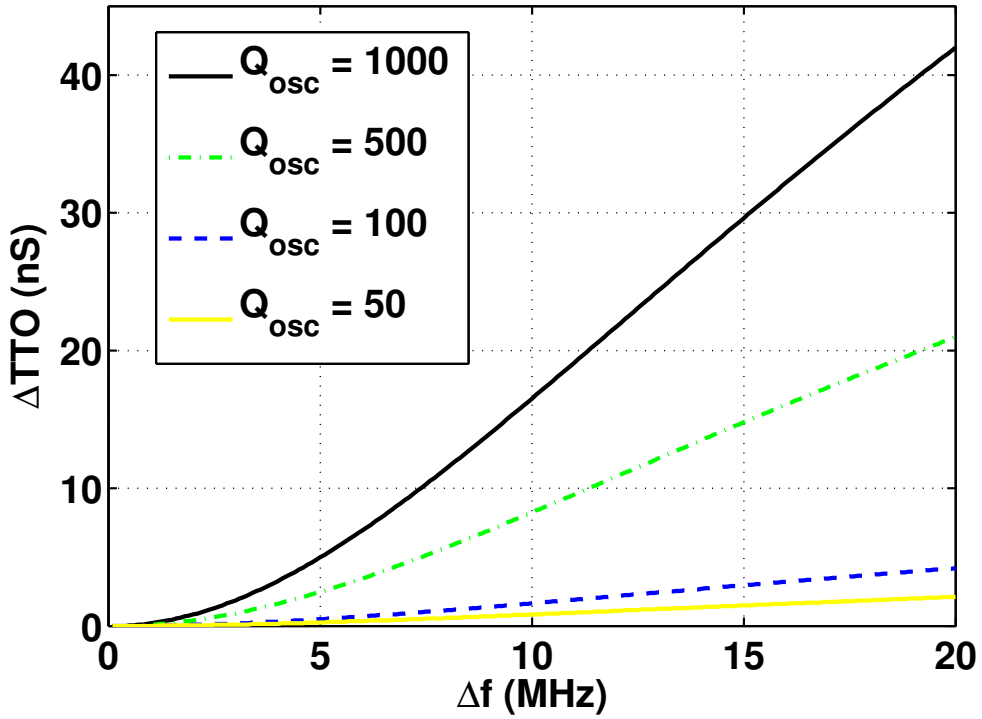

Figure 5.7: ΔTTO versus Δf for four different values of Q_{osc}.

build. The higher the Q_{qch}, the larger the difference in input magnitude at the instant the quench signal is released and oscillations build.

Fig 5.7 shows the ΔTTO (TTO_{f2} - TTO_{f1}) for different values of Δf ($f_2 - f_1$) and Q_{osc}. The plot is based on a -100 dBm input signal from a 50 Ω source and a Q_{qch} of 100. Larger values of Q_{osc} result in a larger ΔTTO for a given Δf. This translates directly into a higher receiver sensitivity since the comparator is resolving a signal that is proportional to ΔTTO. Fig. 5.7 also shows that greater sensitivity can be achieved by increasing the Δf. This occurs because as f_1 and f_2 are further apart, the tuned LC oscil-

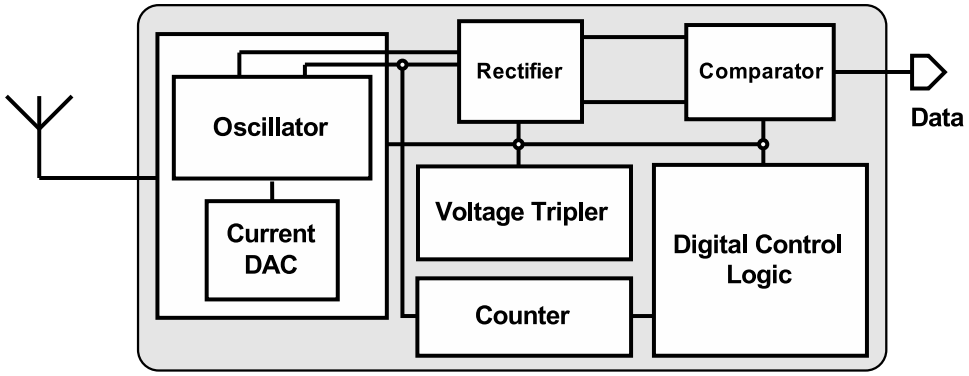

Figure 5.8: Bock diagram for the BFSK super-regenerative receiver.

lator provides more "filtering" to signals further away from the center frequency. This lack of spectral efficiency (compared to OOK) is leveraged by the design. As only loose frequency tolerances are needed, the receiver can use a comparatively coarse frequency calibration, described in Section 5.4.3, which will save power and calibration time compared to the use of a PLL. In addition, the communication channels can be overlapped due to the receivers in-band interference rejection which is described in Section 5.5.

5.4 Circuit Design

The system level block diagram for the BFSK super-regenerative receiver is shown in Fig. 5.8. The isolation amplifier is omitted as the high-Q LC tank provides input filtering and the oscillator power is low enough that the amount of power radiated when oscillations build is negligible. The quench signal is provided by the current mode digital to analog converter (DAC) which also serves as the current source for the oscillator. The

dual rectifier converts the oscillations to a baseband signal that is quantized by the comparator to produce the output data stream. All the digital control signals for the circuit as well as frequency and current calibration are provided by the on chip digital control logic.

5.4.1 Super-regenerative Oscillator

The external matching network is shown in Fig. 5.9. The input signal from the antenna is transformed to a differential signal using an on-board balun. The output impedance of the balun is matched to the input of the receiver using an L-match where the inductors are realized using packaging bondwires and the capacitors are mounted on the PCB. In order to sense the input signal, the receiver is matched to the antenna during quench mode. When the receiver enters oscillate mode, the input impedance of the receiver changes which breaks the input match to the balun and enables oscillations to build.

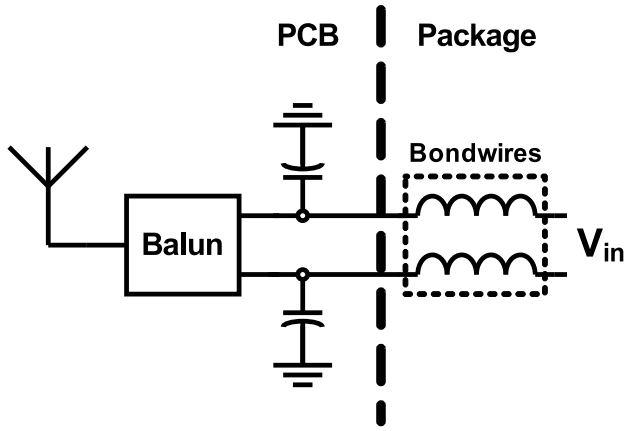

Figure 5.9: Schematic of the external matching network including discrete PCB components and packaging bondwires.

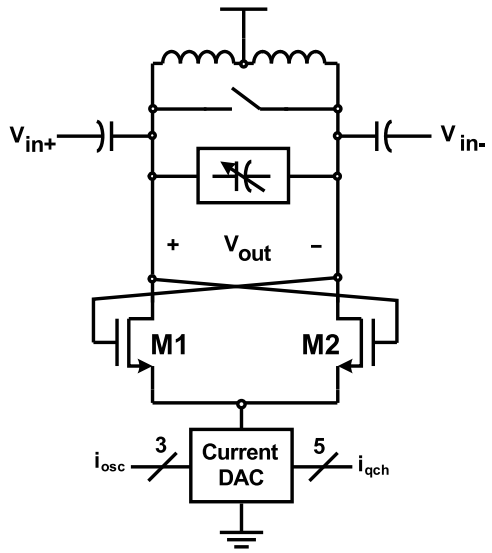

Figure 5.10: Schematic of the digitally controlled super-regenerative oscillator.

The super-regenerative oscillator is shown in Fig. 5.10. The differential input is capacitively coupled to the LC tank by two on-chip capacitors. Along with two external capacitors these coupling capacitors serve as part of the matching network while also isolating the DC bias from the antenna. The LC tank is made up of two bondwire inductors and a digital varactor. When the quench signal is applied, the switch is momentarily closed to quickly dampen the previous oscillations so the incoming signal can be sensed.

Bondwire inductors are used to minimize parasitic resistance and maximize the overall tank Q for a given power consumption. The digital varactor is realized using a binary weighted array of 9 MOS capacitors. The receiver is designed to operate at 1/3 of the nominal supply voltage to minimize power consumption and increase compatibility with a larger variety of energy harvesting methods [70]. As a result of this low voltage

operation, the range from the varactor is greatly reduced.

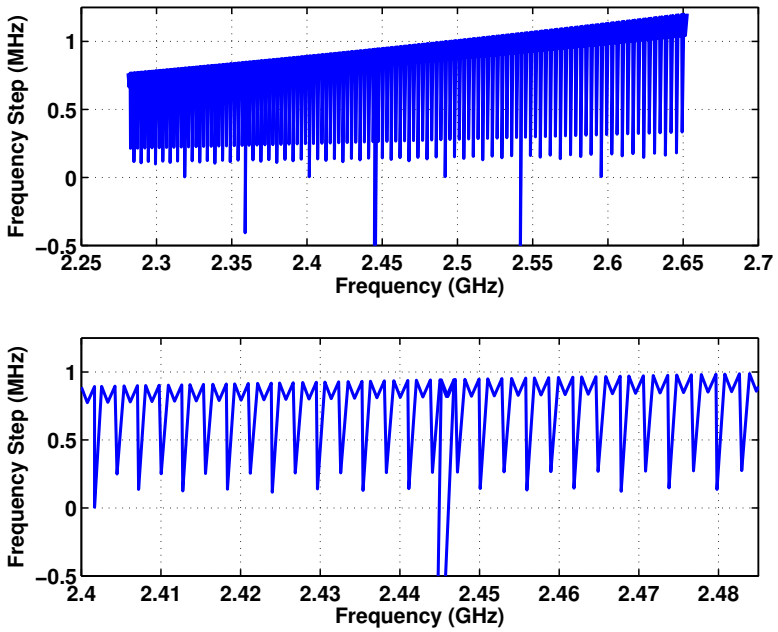

Figure 5.11: The simulated oscillator tuning range with boosted varactor voltages. In the 2.4GHz ISM band the tuning accuracy is better than 1 MHz.

To overcome the reduction in tuning range a voltage tripler similar to the one presented in [71] is implemented on chip. All of the control signals from the digital control and calibration block operate at the reduced supply voltage, but are boosted to the tripled voltage just before being applied to the varactor. The voltage tripler supplies only dynamic switching current which allows modestly sized capacitors to be used. The oscillator tuning range is shown in Fig. 5.11. With the boosted control signals more than 350 MHz of tuning range is achieved to account for process variation and the accuracy

is better than 1 MHz in the 2.4 GHz ISM band. A small amount of non-monotonicity is purposely placed around the MSB transition of the tuning range. This is to ensure there will be no missing frequencies due to varactor mismatch.

The $-g_m$ is provided by the cross-coupled NMOS transistors which are fabricated in their own deep N-well. This enables a zero bulk-source voltage to reduce their threshold voltages and maximize their efficiency. The amount of $-g_m$ they contribute to the LC tank is determined by the current DAC which controls the oscillator current and provides the quenching operation. The current DAC is made up of two sets of binary weighted current sources to set the quench mode current and the oscillate mode current. Each element in the two current sources is switched on or off by the digital logic to provide the current square wave tail current to the oscillator.

Since there is no isolation amplifier, the input must be matched to the oscillator when it is in quench mode. The 5-bit value for the quench mode current is set manually to accommodate the input matching network and the 3-bit value for the oscillate mode current is found during the calibration routine that is executed after the receiver is powered on. A more detailed description of the calibration process is described in Section 5.4.3.

5.4.2 Baseband Circuitry

When oscillations build based on the input signal they need to be rectified and compared to determine the incoming bit. Fig. 5.12 shows the passive rectifier used to convert the oscillations to the baseband data signal. The nodes marked V_{out} are connected directly to the LC tank in the oscillator and transistors M_1 and M_2 act as rectifying diodes. To

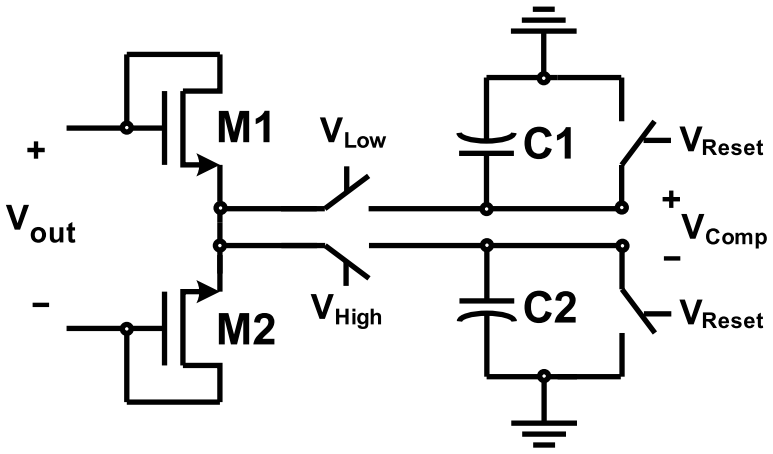

Figure 5.12: Schematic for the passive rectifier.

improve the efficiency of the diodes their V_t is reduced by using large length devices and by placing them in their own deep N-well to remove the body effect.

When the oscillator is tuned to f_1 and the quench signal is removed allowing oscillations to build, V_{low} goes high and the oscillations are rectified and held on C_1. V_{low} is then turned off when the oscillator is quenched and tuned to f_2. When the quench signal is released and oscillations build at f_2 the V_{high} signal is asserted and the oscillations f_2 are rectified and stored on C_2. Finally, the voltages stored on C_1 and C_2 are compared before the reset signal is applied to reset the capacitors.

The diodes created by M_1 and M_2 are chosen to have a W/L ratio close to 1. If they are sized too large the loading effects they have on the oscillator become apparent and the magnitude of oscillations is reduced. On the other hand, if they are too small insufficient current will pass through them and the resulting signal on C_1 and C_2 will be reduced. C_1 and C_2 must also be sized relatively large to stay in the constant current

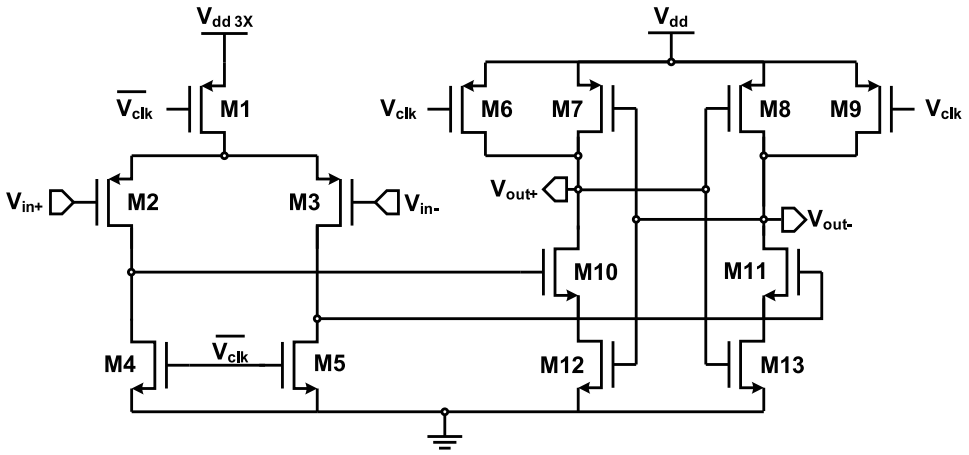

Figure 5.13: Schematic for the ultra-low power comparator.

mode of charging. If they are too small they will quickly charge up to the full oscillation voltage and lose the time dependent signal needed to determine the incoming bit.

The comparator used to compare the rectifier signal and determine the incoming data is shown in Fig. 5.13. It consumes no static current from either of the two supply voltages [72]. The first stage of the comparator operates on the boosted supply that is shared with the digital varactor. The input signal from the rectifier can create a voltage greater than V_{dd}, but will always be less than $2V_{dd}$. To accommodate this signal the boosted $3V_{dd}$ supply created for the varactor is used along with a PMOS input stage.

When $\overline{V_{clk}}$ is high M_1 is turned off while the gates of M_{10} and M_{11} are discharged to ground (through M_4 and M_5) and the latch is reset to V_{dd}. When $\overline{V_{clk}}$ is pulled low, the gates of M_{10} and M_{11} are slowly charged to V_{dd} proportional to the signal on M_2 and M_3. This results in one of them turning on just before the other. At this point the latch is enabled and a decision is made. Simulation results show that the comparator consumes

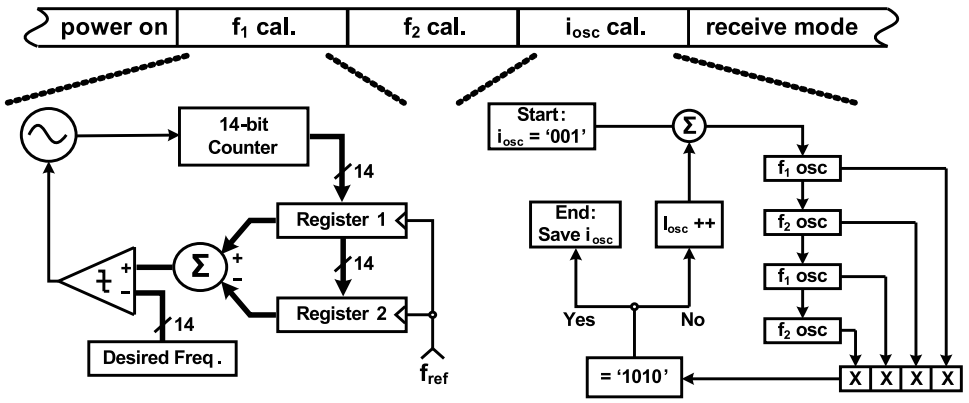

Figure 5.14: Calibration process executed upon startup. A SAR algorithm is used to calibrate f_1 and f_2 before the minimum value for i_{osc} is found.

a total power of less than 2.5 μW when clocked at 1 MHz.

5.4.3 Digital Calibration

Each time the receiver is powered up it goes through the digital calibration process shown in Fig. 5.14. The calibration starts by tuning the oscillator to the desired f_1 and f_2 using a SAR algorithm. An on-chip counter is used to count the oscillations during the reference period. This count is then compared to the desired number of oscillations before setting the MSB of the 9-bit digital varactor. This loop is then repeated 8 more times to calibrate each bit in the varactor. Once f_1 has been calibrated, the frequency calibration routine is repeated to calibrate f_2.

A block diagram of the 2.4 GHz counter used for frequency calibration is shown in Fig. 5.15. The input signal from the oscillator is amplified using a self-biased inverter

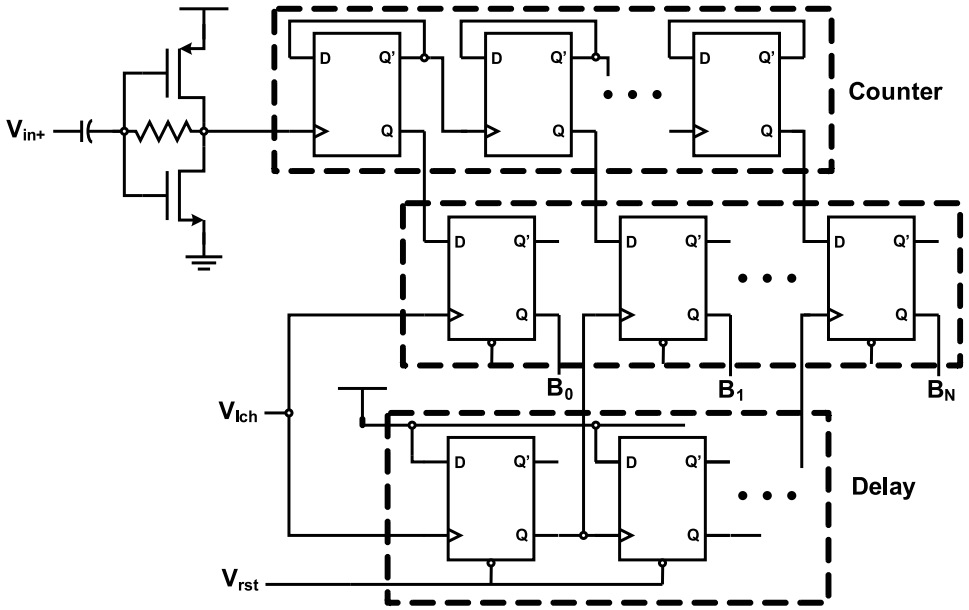

Figure 5.15: Block diagram of the 2.4 GHz counter.

and then fed to the counter. The counter is constructed of 14 cascaded high speed D flip-flops configured as dividers by connecting $\overline{Q}$ to D [73]. To reduce loading on the output of the counter, an additional 14 standard latched D flip-flops buffer the counter output to the digital calibration logic. During operation, each flip-flop in the counter adds a small amount of delay which results in a delay between the time that the least significant bit (lsb) and most significant bit (msb) of the counter output are valid. In order for the correct counter output to be presented to the digital calibration block, this delay needs to be introduced into the latch signal so that each bit of the counter output is read only after it has become valid. This is done with a third set of 13 dividers whose schematic is shown in Fig. 5.16. These are exactly the same as the dividers used in the

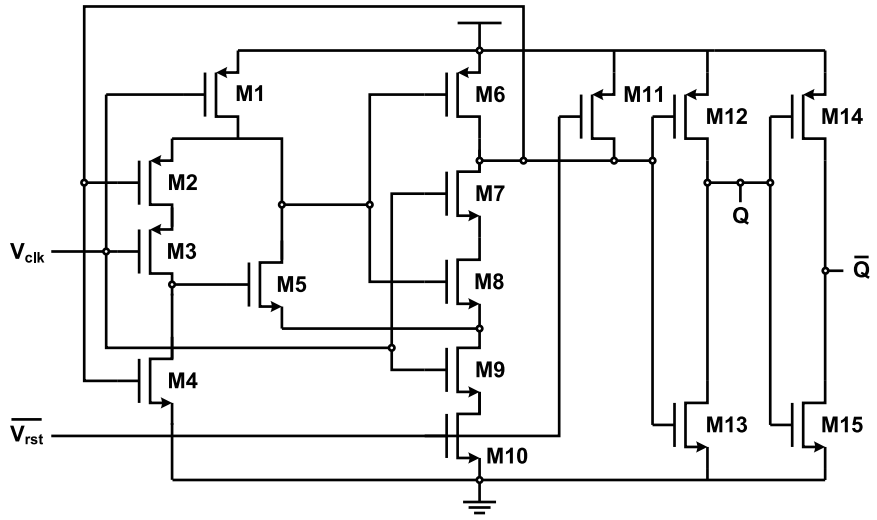

Figure 5.16: Schematic for the high speed D flip-flop with asynchronous reset.

counter with the exception of M_{10} and M_{11} which allow the flip flop to be reset. The reset capability is needed to reset the output of the delay flip flops to '0' before each new value is latched.

To accurately operate at frequencies above 2.4 GHz the counter requires a supply voltage of 1.3 V. This is provided by a second on-chip DC-DC converter. A separate DC-DC converter is used as the power requirements for the counter are much higher and the duration of operation is much shorter. This converter is powered up when the receiver is turned on and then is completely shut down when the frequency calibration is completed.

After f_1 and f_2 are found, the oscillation current is calibrated. To start this process the 3-bit value for i_{osc} is set to '001' and oscillations are allowed to build at f_1, but not at f_2. The rectified oscillations are then compared and the value is stored. The oscillations

are then allowed to build at f_2, but not at f_1 and the rectified outputs are again compared and stored. The entire process is repeated to obtain a 4 bit code that corresponds to oscillations building with the pattern $f_1\ f_2\ f_1\ f_2$. If i_{osc} is large enough for oscillations to build at both f_1 and f_2, the resulting 4-bit code will be '0101' where a '0' corresponds to oscillations building at f_1 and a '1' corresponds to oscillations building at f_2. The 4-bit code generated during the calibration is compared to '0101' and if it matches the current value of i_{osc} is stored. If the 4-bit calibration code does not match (implying that oscillations are not building at both frequencies), the value for i_{osc} is incremented and the process is repeated until it does.

The calibration of i_{osc} allows the minimum amount of power to be used in the oscillator while also maximizing the receiver sensitivity. Fig. 5.7 shows that larger values of Q_{osc} (the right side of Fig. 5.4) result in a larger ΔTTO for a given signal bandwidth. This larger ΔTTO directly translates to a larger signal presented to the comparator. The minimum value needed for i_{osc} corresponds to the maximum value of Q_{osc} and hence, maximizes the signal at the comparator for a given input signal power.

Both the frequency and the current calibration schemes allow the circuit to be calibrated at different data rates. The 14-bit counter allows frequency calibration to be executed with data rates as low as 150 kbps when operating at 2.4 GHz. The current calibration also enables a wide range of data rates to be used. At lower data rates the oscillator has more time to build oscillations so less current is needed. When a faster data rate is needed, the period to build oscillations is smaller and the resulting i_{osc} needs to be larger for oscillations to build. This also shows that the receiver is more sensitive at lower data rates. When a lower data rate is used, less current is needed to build

oscillations resulting in a larger value of Q_{osc}.

5.5 Measured Results

The receiver was fabricated in a standard triple-well 0.18 μm CMOS process. The entire receiver with the exception of the second DC-DC converter used to power the counter is shown Fig. 5.17 and occupies 0.55 mm^2. The LC tank inductors are made up of two bondwires that are each approximately 2.5 mm long connected between each of the two oscillator pads on the right side of Fig. 5.17 and a standard QFN package. Transient signals captured in the lab are shown in Fig. 5.18. The top signal in Fig. 5.18 shows the 1 Mb/s baseband data that is used to modulate an RF signal source. Below the baseband data are the output signals for the rectifiers that rectify the oscillations when the LC

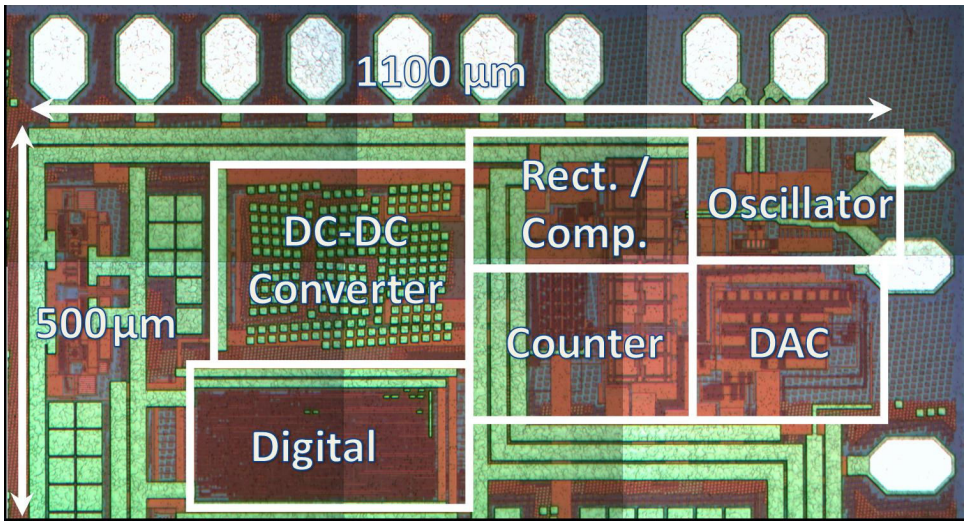

Figure 5.17: Die photograph for the 2.4 GHz BFSK super-regenerative receiver.

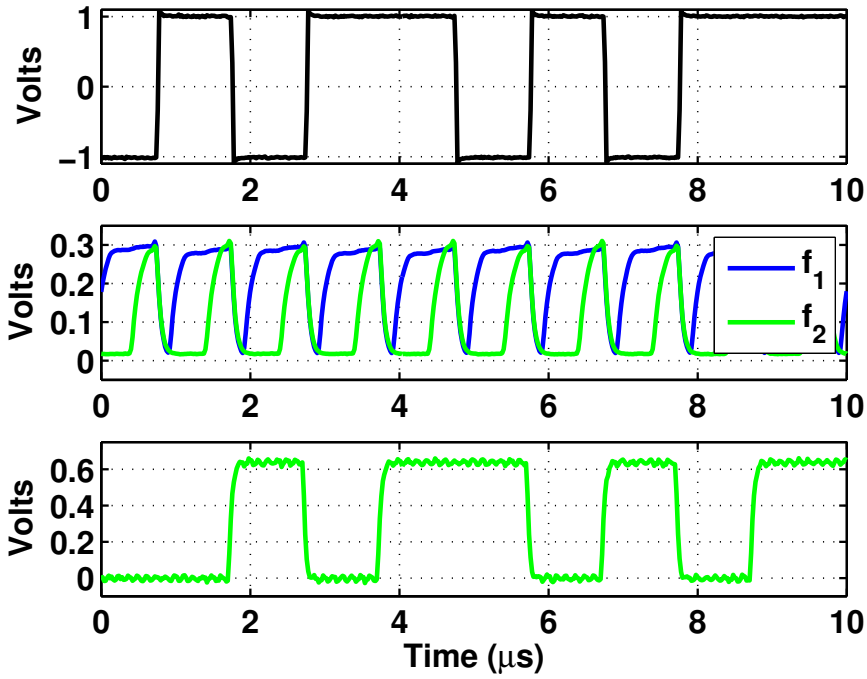

Figure 5.18: Measured transient data for the receiver. The baseband data is shown with the corresponding rectifier outputs. The output data has a latency of a signal clock period.

tank is tuned to f_1 and f_2. These are the two signals that are given to the comparator to determine the output data stream. The bottom part of Fig. 5.18 shows the output data stream that is generated by the comparator. When the baseband data is low, the signal source generates f_1 and when the baseband data is high the signal source generates f_2. Both f_1 and f_2 are sampled during each bit period and when the baseband data is low, the rectifier output for f_1 is higher while when the baseband data is high the rectified value for f_2 is greater. The output data is evaluated after oscillations have been rectified at

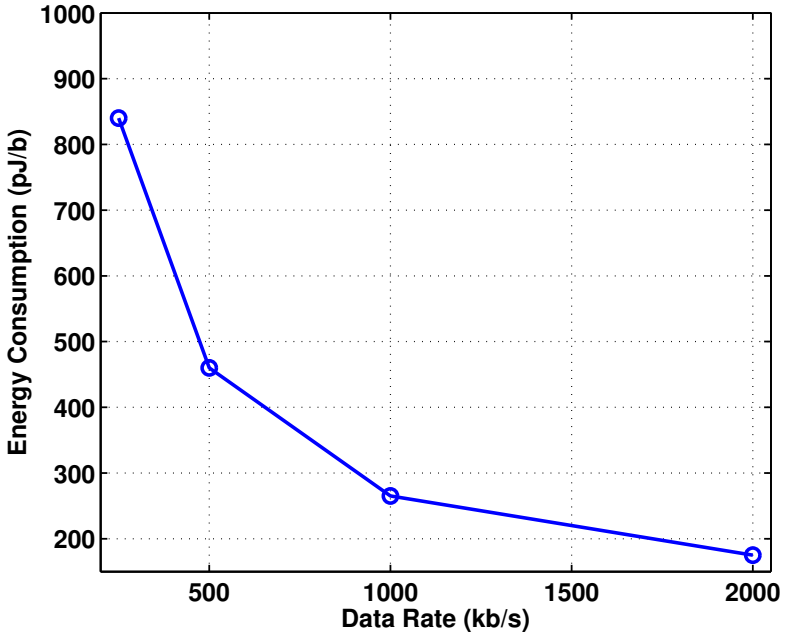

Figure 5.19: Total energy consumption for the receiver at different output data rates.

both f_1 and f_2 giving it a single clock cycle delay from the input. It is important to note that in Fig. 5.18 the reference clock for the receiver has been externally synchronized with the data clock. In reality the system is non-coherent and the receiver needs to be clocked at twice the input data rate to ensure the incoming data is received properly.

In order to fully characterize the receiver, testing was performed at data rates ranging from 250 kb/s up to 2 Mb/s. Fig. 5.19 shows the total energy consumption of the receiver in nJ/b while operating at different data rates. When operating at 250 kb/s the receiver achieves its lowest power consumption of 215 μW, but this corresponds to the highest energy consumption of 860 pJ/b. The highest energy efficiency is found at a data rate

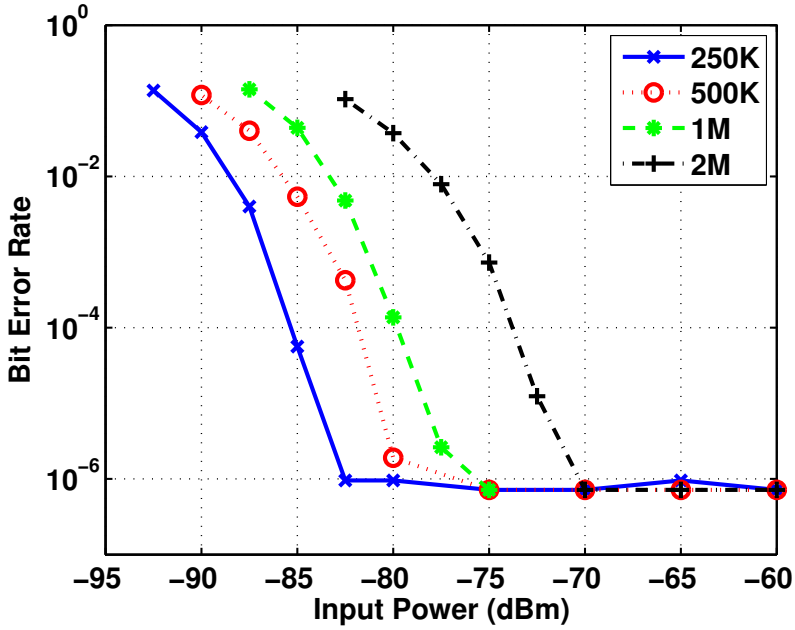

Figure 5.20: Bit error rate measurements for different data rates and input power levels.

of 2 Mb/s when the receiver consumes just 0.175 nJ/b. At this rate, oscillations need to build much faster (within 125 ns) which requires 350 μW. Because of the high output data rate, the energy usage is the least per bit of all the receiver data rates.

Bit error rate (BER) testing was performed by capturing over 4 million bits with a logic analyzer and comparing it with the known data sequence. The BER measurements shown in Fig. 5.20 show excellent performance with BERs lower than 10^{-6} at all data rates for input power levels greater than or equal to -70 dBm. The BER performance can likely exceed 10^{-6} for larger input power levels, but due to the limited amount of memory in the logic analyzer used this is the lowest reliable BER value that could be measured.

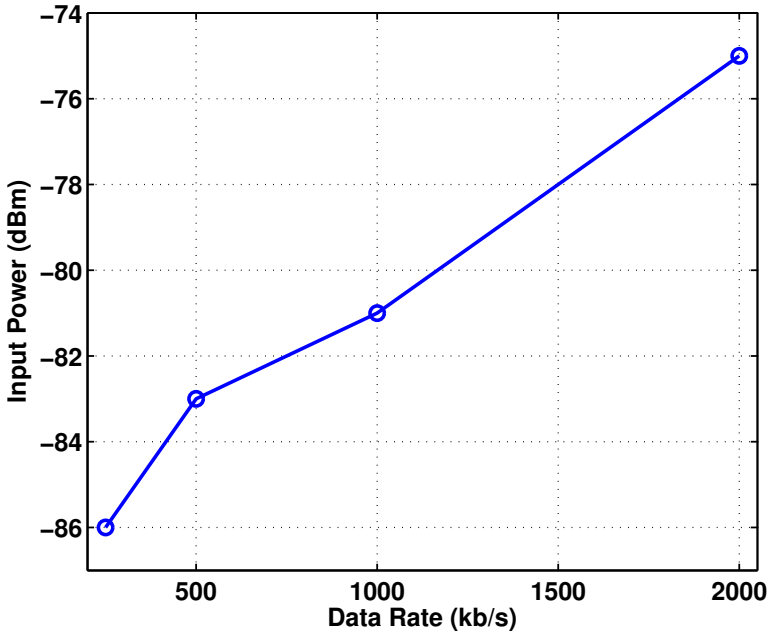

Figure 5.21: Receiver sensitivity for different data rates. The sensitivity is defined as the input power that corresponds to a 10^{-3} BER.

Fig. 5.21 illustrates the tradeoff between data rate and sensitivity that was discussed in Section 5.3.2. When operating at 2 Mb/s a small value of Q_{osc} is needed which limits the sensitivity to -75 dBm. As the data rate is decreased, larger values of Q_{osc} can be used and the sensitivity increases. At 250 kb/s the maximum sensitivity of -86 dBm is achieved. Additional measurements performed in the lab as well as outdoors show that these sensitivities will support communication from 10 m (-70 dBm) to more than 20 m (-82 dBm) when receiving a 2.4 GHz signal transmitted at -5.5 dBm.

Interference measurements were conducted to determine the receiver performance

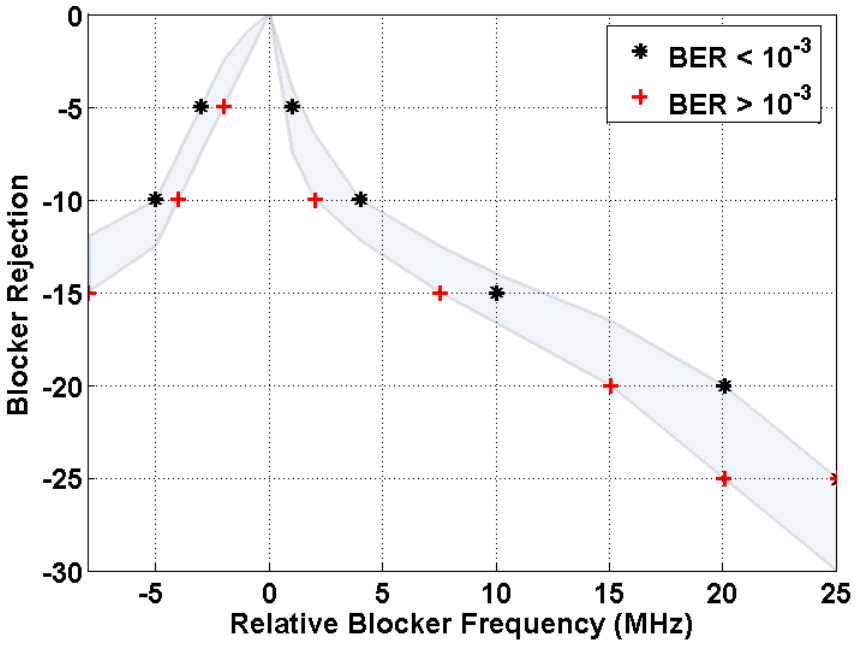

Figure 5.22: Blocker rejection relative to f_2 with a 16 MHz channel. The shaded region implies where the blocker causes the BER to fall to 10^{-3} while the points show measured data.

in the presence of large blocking signals. Fig. 5.22 shows the blocker rejection for large interference both in-band and out of band. The blocking signal is swept from the center of the 16 MHz channel toward f_2 and then 25 MHz beyond f_2. Multiple BER measurements were performed at varying power levels at each blocker frequency to determine when the BER falls to 10^{-3}. The rejection is -15 dB in the center of the channel and increases as the blocking signal approaches the channel edge. The receiver is less sensitive to out of band blocking signals with a rejection better than -10 dB at 5 MHz from f_2 and up to -30 dB for far out of band signals.

Table 5.1 summarizes the receiver's performance while Table 5.2 compares the receiver to several state of the art ultra-low power designs. The work presented here is the only super-regenerative receiver that utilizes BFSK modulation. In addition the power supply is almost half that of the other designs which increases its compatibility with battery-free energy harvesting applications while also allowing operation with only 215 μW of power dissipation. This low power consumption along with its high data rate make it the lowest power and lowest energy super-regenerative receiver to date.

The figure-of-merit (FOM) presented in Table 5.2 includes the receiver sensitivity along with the total power consumption and data rate in the following form

$$FOM = P_{rx}P_{sens}/DR \tag{5.14}$$

where P_{rx} is the total receiver power, P_{sens} is the power of the received signal that causes the BER to equal 10^{-3}, and DR is the output data rate. This allows all of the receivers main parameters to be included in a single performance metric. The FOM is calculated using the numbers listed in the table with the exception of [61] and the work presented here which are using the 250 kb/s ($P_{sens} = -82\ dBm$ and $P_{rx} = 244\ \mu W$) and 250 kb/s ($P_{sens} = -86\ dBm$ and $P_{rx} = 215\ \mu W$) operating points, respectively.

Table 5.1: Summary of measured results.

Technology	0.18 μm CMOS	
Frequency	2.4 GHz ISM	
Active Area	0.55 mm^2	
Supply Voltage	0.65 V	
Data Rate	2 Mb/s	250 kb/s
Power	350μW	215 μW
Energy	175 pJ/b	860 pJ/b
Sensitivity (BER$<10^{-3}$)	-75 dBm	-86 dBm
Calibration Time	116 μS	

Table 5.2: Comparison to recent ultra-low power super-regenerative receivers. (FOM = $P_{rx} * P_{sens}/DR$)

Ref.	**[56]**	**[51]**	**[48]**	**[60]**	**[61]**	**This Work**
Tech	90 nm	130 nm	130 nm	180 nm	180 nm	180 nm
Modulation	OOK	OOK	OOK	ASK	BFSK	BFSK
Frequency	402 MHz	2.4 GHz	2 GHz	402 MHz	900 MHz	2.4 GHz
Supply	1 V	1.2 V	0.9 V	1.3 V	1.3 V	0.65 V
Min. Power	400 μW	2.8 mW	400 μW	900 μW	244 μW	215 μW
Max. Data Rate	120 kb/s	500 kb/s	5 kb/s	156 kb/s	1 Mb/s	2 Mb/s
Min. Energy	3.3 nJ/b	5.6 nJ/b	80 nJ/b	5.8 nJ/b	400 pJ/b	175 pJ/b
Sensitivity	-93 dBm	-90 dBm	-100 dBm	-75 dBm	-83 dBm	-75 dBm*
FOM	208 dB	203 dB	201 dB	187 dB	202 dB	207 dB

* *The receiver achieves its best sensitivity of* -86 *dBm while operating at* 250 *kbps.*

Fig. 5.23 compares this work to several recent low-power and low energy super-regenerative [46, 48, 51, 56–60] and UWB [62–67] designs. As expected, the OOK super-regenerative designs tend to have very low power consumption but higher energy consumption. The UWB designs consume more power, but have energy consumptions closer to 1 nJ/b. The design presented here combines ultra-low power operation with highly efficient energy usage making it the lowest power and lowest energy per bit de-

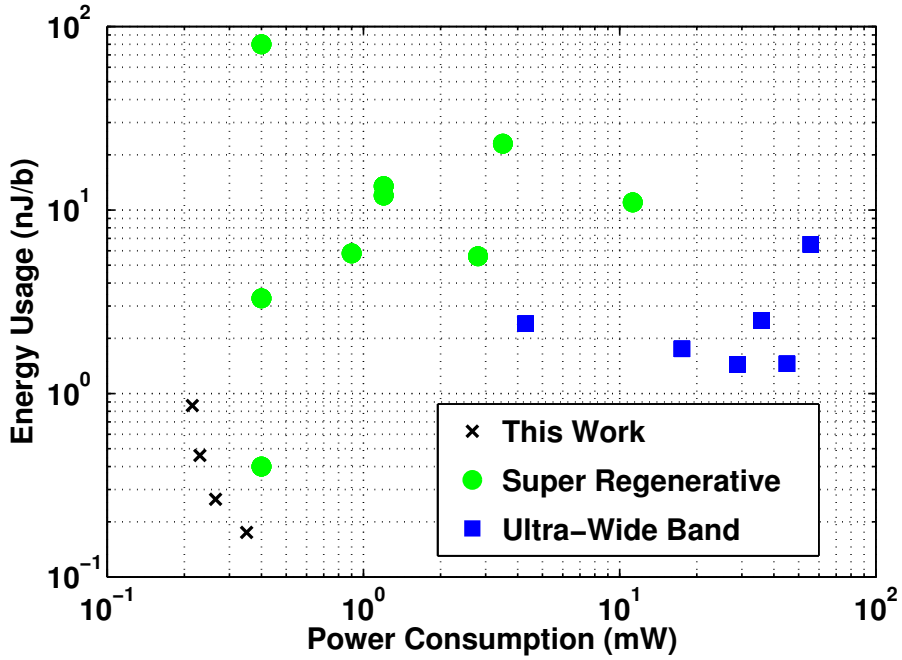

Figure 5.23: Comparison of power consumption and energy usage of several recently published low power wireless receivers and this work at four different data rates.

sign to date.

5.6 Conclusion

A BFSK super-regenerative architecture has been presented for use in battery-free WSNs. To be compatible with the energy harvesting network architecture, the receiver minimizes power consumption while also maintaining very high energy efficiency.

A system analysis shows that the basic operation of the receiver can be described

with the oscillator Q in quench mode (Q_{qch}) and in oscillate mode (Q_{osc}). A high value for Q_{qch} will result in better frequency selectivity and greater input signal amplification at the cost of burning more power. Q_{osc} should also be as high as possible for a given data rate in order to maximize the receiver sensitivity. A fundamental tradeoff between sensitivity and data rate is shown when varying the value of Q_{osc}.

In order to achieve the lowest possible power consumption the super-regenerative oscillator performs the input frequency selectivity and amplification which eliminates the need for an isolation amplifier. Low voltage circuit design along with passive rectifiers and a dynamic power comparator further reduce power consumption. A DC-DC voltage booster is used to extend the digital tuning range of the oscillator and is implemented on-chip with modestly sized capacitors as it does not need to provide static current. Startup calibration quickly recalibrates the frequency during each communication while also finding the lowest power and highest sensitivity for a given data rate.

The receiver is realized in a 0.18 μm standard CMOS process with triple-well capabilities. While operating at 2 Mb/s the receiver consumes 175 pJ/b with a sensitivity of -75 dBm. A minimum power consumption of 215 μW is achieved when operating with an output data rate of 250 kbps with a sensitivity of -86 dBm making it the lowest power fully integrated super-regenerative receiver to date.

Chapter 6 – Conclusion

As wireless sensor networks (WSNs) become prevalent, the need for smaller and lower power sensor nodes is quickly growing. When investigating the power consumption of these sensor nodes it is clear that the majority of the power is consumed by the wireless communication. In a typical sensor node the wireless receiver consumes the most power of all the components, thus dictating the nodes overall size and lifetime. Overcoming the challenge of developing ultra-low power wireless communication for WSNs will enable wireless sensors to be seemlessly integrated with our environment. This will enable an almost infinite number of applications from automated control to fault detection systems.

Currently, the direct conversion receiver architecture is most commonly used in commercial sensor node applications. Significant power reduction can be realized by reducing (or eliminating) the front-end low noise amplifier (LNA) gain at the cost of higher noise figure (NF). This is acceptable for short range communications which is typically needed in WSNs. On the circuit level, the self-biased and common gate LNAs provide the best noise performance when operating at extremely low power levels. Completely passive front-ends also show a very promising approach for wireless sensor networks as they consume no power and add very little noise and distortion to the system.

Although optimizing the direct conversion architecture can yield significant power savings, it still cannot be used to sustain a battery free WSN for a period of years on

harvested power. The super-regenerative receiver architecture enables receiver power levels to be reduced over the direct conversion architecture by an order of magnitude. In addition, enabling binary frequency shift keying (BFSK) to be used with this architecture increases the receiver sensitivity and data rate. Overall, this innovation in the super-regenerative architecture enables ultra-low power receiver operation with increased reliability and lower overall energy communication when compared with previous solutions.

A BFSK super-regenerative receiver has been designed and fabricated in a triple-well 0.18 μm process. To reduce power, the RF input is coupled directly to the tank of the LC oscillator eliminating the need for an LNA. A resistive CMOS switch is used to quench the oscillator and allows data rates up to 1 Mbps. A passive rectifier that consumes no additional power is used to convert the oscillations to a low frequency signal. Offset correction on the ultra-low power latched comparator improves the sensitivity of the receiver by allowing accurate quantization of very small signals. Lab measurements show power consumption lower than 250 μW from a 1.3 V supply when operating at 250 kbps and a sensitivity of -84 dBm (10^{-3} BER). When operating at 1 Mbps, the receiver consumes just 0.4 nJ/b.

To fully characterize the BFSK super-regenerative receiver architecture, a second receiver has been designed and fabricated in the same triple-well 0.18 μm process. Although the overall operation is similar to the first design, each block has been redesigned to simultaniously reduce power and improve performance. The oscillator is completely redesigned to use integrated bondwire inductors and the quench switch is replaced with a current DAC to further reduce power and improve sensitivity. A comparator that con-

sumes no static power shows a 5X power reduction over the original design while also eliminating the offset correction. A digital controller is implemented on chip to fully control the operation of the receiver from power-up to power-down. This controller enables the receiver to go though two fast calibration routines to select the proper communication channel while also finding the lowest possible current for a given data rate.

The new receiver operates on a single 0.65 V supply. It consumes 215 μW while operating at 250 kbps and at the maximum data-rate of 2 Mbps it consumes only 0.175 nJ/b. At 1 Mbps the receiver sensitivity improves by 12 dB compared to the previous design while consuming only two-thirds the power (270 μW). A comparison to recent state-of-the-art receivers shows that this is the lowest power and lowest energy fully integrated super-regenerative receiver to date.

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