AN ABSTRACT OF THE DISSERTATION OF

Weilun Shen for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on July 8, 2010.

Title: Low-Power Double-Sampled Delta-Sigma Modulator for Broadband Applications.

Abstract approved: _____

Gabor C. Temes

High speed and high resolution analog-to-digital converter (ADC) is a key building block for broadband wireless communications, high definition video applications, medical images and so on. By leveraging the down scaling of the latest CMOS technology and the noise shaping properties, delta-sigma (ΔΣ) ADCs are able to achieve wide-band operation and high accuracy simultaneously. In this thesis, two novel techniques, which can be applied to high performance ΔΣ ADC design, are proposed. The first one is a modulator architectural innovation that is able to effectively solve the feedback timing constraints in a double-sampled ΔΣ modulator. The second one is a transistor level improvement to reduce the hardware consumption in a standard Data Weighted Averaging (DWA) realization.

Next, charge-pump (CP) based switched-capacitor (SC) integrator is discussed. A cross-coupling technique is proposed to eliminate parasitic capacitor effect in a CP based SC integrator. Also, design methodologies are introduced to incorporate a modified CP based SC integrator into a low-distortion ΔΣ modulator. A second-order ΔΣ modulator was designed and simulated to verify the proposed modulator topology.

Finally, the design of a double-sampled broadband 12-bit ΔΣ modulator is presented. To achieve very low power consumption, this modulator utilizes the following two key design techniques:

1. Double sampled integrator to increase the effective over-sampling ratio.

2. Capacitor reset technique allows the use of only one feedback DAC at the front end of the modulator to completely eliminate the quantization noise folding back.

A 2+2 cascaded topology with 3-bit internal quantizer is used in this ΔΣ modulator to adequately suppress the quantization noise while guaranteeing the loop stability. This ΔΣ modulator was fabricated in a 90 nm digital CMOS process and achieves an SNDR of 70 dB within a 5 MHz signal bandwidth. The modulator occupies a silicon area of 0.5 mm^2 and consumes 10 mW with a supply voltage of 1.2 V.

Low-Power Double-Sampled Delta-Sigma Modulator

For Broadband Applications

by

Weilun Shen

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I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Weilun Shen, Author

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Working towards a Ph.D degree is so similar to a long journey full of zigzags that one might very easily get lost. In our modern daily life, people traveling to an unfamiliar destination could rely on a global positioning system device to avoid any unnecessary detour. However in the pursuit of a Ph.D degree, I am positively sure I would have never achieved my goal without the help and guidance of some specific people.

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I am proud of being a Ph.D student at EECS at Oregon State University. We have one of the best EECS departments in the world because we have the best research faculties, the best students, the best hardware and the best environment to study. I benefited so much from those excellent courses which offered by EECS department. Besides, all EECS main office staffs are appreciated for their kind help through my whole Ph.D study.

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DEDICATION

Here, I would like to express my deepest gratitude to my family. My wife, Linling made a tremendous sacrifice during my Ph.D study. This work would have never been possible without her love and patience. I thank my mother-in-law for her great help to my family. I also wish my little boy Kenneth the best and grow with good health and brightness.

To the memory of my mother

Low-Power Double-Sampled Delta-Sigma Modulator for Broadband Applications

CHAPTER 1. INTRODUCTION

1.1. Motivation

Every minute, ten hours of video is uploaded to YouTube. With hundreds of millions of videos watched and hundreds of thousands of videos uploaded every day, YouTube has emphasized an expectation among internet users: speed.

Watching films at home is one of the major recreational events in every family. Pursing high quality makes the video carriers evolved from cassettes at about twenty years ago to blue-ray DVDs nowadays. Hence, high-definition video emphasized an expectation among consumers: high performance.

It is not uncommon to see people surfing internet, receive and send their emails through their mobile phones. Battery-powered mobile devices can only be used for a limited time until its next recharge. So with more and more functionalities integrated on a single device, how long a particular device can work heavily depends on the power consumed by its constituent chips. As a result mobile devices emphasized an expectation among consumers: low power.

The price factors play a very important role in the consumer electronics market because people always want to pay less out of pocket. As a consequence, developing a

new product becomes mostly cost-driven. Market emphasized an expectation among consumers: low cost.

With everything in nature stubbornly remains analog such as the video we watch and the music we listen to, analog to digital and digital to analog data converters really become a critical building block in a complicated system design. In this thesis, we describe some new techniques and the design of a delta-sigma (ΔΣ) analog to digital data converter which fulfills the aforementioned expectations: speed, high performance, low power and low cost.

1.1.1. ADCs for Broadband Applications

With transistors becoming smaller and smaller, chips really become a system with both analog and digital portions inside. The fact that analog to digital data converters (ADCs) form a bridge between the two portions indicates that ADCs might become a performance bottleneck in such systems. Modern broadband communications also necessitate high speed ADCs with good resolution and low power consumption. For example, digital TV tuner requires baseband ADC to process a signal bandwidth of 8 MHz with a 13-bit resolution while in very-high-bitrate digital subscriber line (VDSL) a 17 MHz signal bandwidth ADC with 12-bit resolution is needed. Traditionally such high speed ADCs were dominated by Nyquist rate ADCs. However Nyquist rate ADCs with high resolution mandate precision analog components such as precise capacitor matching and very high gain operational amplifiers (opamps). Unfortunately, brute-force design effort to achieve high resolution for a Nyquist rate ADC in a deep sub-micron CMOS process tends to be extremely difficult. One way to improve the

accuracy of Nyquist rate ADCs is to utilize digital calibration [1] [2]. This method is very promising but adds complexity and design period.

Delta-Sigma (ΔΣ) ADCs have become more and more popular for broadband communication applications in the past couple of years. Modern advanced CMOS technology allows ΔΣ ADCs to be clocked at hundreds of mega hertz with reasonable power consumption, therefore input signal bandwidth can be extended to tens of MHz. Compared to Nyquist rate ADCs; ΔΣ ADCs have the ability to achieve high resolution with relaxed component matching and opamps' gain. The fact that the design of the preceding anti-aliasing filter is relaxed is another benefit of using a ΔΣ ADC. ΔΣ ADCs need a digital decimation filter to remove the out-of-band quantization noise and down-sample the digital bit stream to Nyquist rate. This is why, generally speaking, a ΔΣ ADC trades accuracy with area as well. However this area overhead reduces dramatically with the aggressive scaling of the CMOS process.

Designing a broadband low power high resolution ΔΣ ADC requires new techniques at both architectural and circuit level. So it becomes a really hot topic in recent years and is expected to continue in the next couple years [3] [4] [5] [6] [7] [8] [9] [10].

1.1.2. Design Challenge in Advanced CMOS Technologies

Analog designs in the advanced CMOS technology nodes like 90nm or below are facing a great deal of challenges [11].

A. Device physical scaling.

The most prevalent phenomenon in advanced processes is that devices continue to scale down. This results in higher transistors' intrinsic cutoff frequency but higher leakage current since the gate oxide thickness has to be thinner to accommodate the threshold voltage reduction. Large leakage current can be very problematic in circuit design. For instance, in mobile applications, the leakage current will increase the power consumption while the circuits are in stand-by mode. To overcome this problem, low power (LP) process is always chosen for leakage sensitive applications. However, transistors in an LP process are much slower than their counterparts in a general process. Therefore it is quite difficult to maintain the same performance. Another issue from the device scaling is the parasitic wiring capacitance makes up a high percentage of the overall capacitance in a circuit. It is not uncommon to see a considerable amount of speed degradation in a post-layout simulation. A possible solution is to intentionally add some capacitance at the pre-layout simulation. This solution nonetheless requires good design experiences.

B. Device matching.

In analog designs, devices matching properties are always of top interest mainly because they severely limit performances. Taking ADC design as an example, device matching properties can influence linearity and SNR (signal-to-noise ratio) directly while power consumption and area will be affected indirectly since an effective way to improve matching is to increase the device sizes. In advanced CMOS process, device matching becomes worse and matching oriented design tends to be complicated. Statistic analysis such as Monte-Carlo simulation is mandatory. A popular and

effective measure is to utilize digital calibration method [12]. It should be noted that the calibration mechanism to reduce offset can help lower the flicker noise at the same time.

C. Process variation, reliability and stress.

Advanced process also shows huge variation. For instance, a MOS transistor threshold voltage will vary from 200 mV to 500 mV over process and temperature in a 65 nm LP process. In a mass production design, simulation has to be done in hundreds or even thousands of corners to guarantee product yield. Maintaining performance in such a way is hard and oftentimes will drive a designer desperate.

Reliability is another important concern in a mass product design to ensure a product's lifetime. Voltage of every node in the circuit must not exceed the foundry specified voltage limits except for a very short amount of time during start-up. Electromigration simulation should also be performed after a circuit layout to check whether or not a metal wiring carries higher current density than the foundry specified value.

In process node 90 nm or below, transistors will "feel" stressed under a certain layout pattern. Two most prevalent phenomena are shallow trench isolation (STI) and well proximity effect (WPE). Stressed transistors usually have higher threshold voltage, lower transconductance and different model parameters compared to unstressed transistors resulting performance degradation and offset. Fortunately these phenomena can be easily tackled by careful layout.

D. Reduced supply voltage

. Advanced CMOS processes use low supply voltage for core thin oxide transistors. Low voltage poses unprecedented challenges for analog design. Telescopic amplifier topology becomes hardly practical without some special techniques. Design of MOS switches in a switched-capacitor circuit is affected badly as well. Appropriate system architecture together with novel design techniques and circuit innovation is the key to moving the analog design into the low voltage era.

E. Very low transistor intrinsic gain

Operational amplifiers are so critical that they can be seen almost everywhere in analog designs. DC gain of opamps determines the quality of the virtual ground in an opamp feedback configuration which affects the linearity directly. However, transistors' intrinsic gain is so poor that the DC gain of a simple two-stage opamp barely reaches 40 dB. At the same time, reduced power supply limits the effectiveness of trying to improve DC gain through traditional methods such as cascoding. Therefore we have to explore architectures which can tolerate low gain opamps or even operate without opamps.

The main purpose of this thesis is to develop novel system architectures and new circuit implementations to overcome the aforementioned design challenges. We will take the design of a broadband low power ΔΣ ADC as a platform to address these issues.

1.2. CONTRIBUTIONS OF THIS RESEARCH

The major contributions of this research can be summarized as follows:

[1] A novel double-sampled ΔΣ modulator is proposed to relax the critical feedback timing issue. In this new modulator topology, the speed of quantizer and dynamic element matching (DEM) logic can be greatly reduced.

[2] A new Data Weighted Averaging (DWA) realization is proposed to reduce the hardware complexity.

[3] A cross-coupling technique is proposed to eliminate parasitic capacitor effect in a charge-pump (CP) based switched-capacitor (SC) integrator. Design methodologies are introduced to incorporate a modified CP based SC integrator into a low-distortion ΔΣ modulator.

[4] A broadband low power switched capacitor ΔΣ modulator is designed and demonstrated in a 90 nm digital CMOS process. Through strategic design methodology at system and transistor level, this modulator achieves good performance and low power consumption.

1.3. Organization of the Dissertation

This thesis mainly deals with the design of a broadband low power ΔΣ modulator in advanced deep sub-micron CMOS process and techniques on how to improve the modulator performance. Both system level and circuit level designs are covered. Here is how this thesis is organized:

Chapter 2 introduces a novel double-sampled ΔΣ modulator topology to relax the critical feedback timing issue. The speed of quantizer and the DEM logic can be greatly reduced to save power and improve the design robustness.

Chapter 3 presents a new Date Weighted Averaging (DWA) realization. Compared to the popular implementation, the proposed one has less hardware complexity.

Chapter 4 covers the charge-pump (CP) based switched-capacitor (SC) integrator. A cross-coupling technique is proposed to eliminate parasitic capacitor effect in a CP based SC integrator. Also, design methodologies are introduced to incorporate a modified CP based SC integrator into a low-distortion ΔΣ modulator.

Chapter 5 focuses on the design of a low power double-sampled broadband ΔΣ modulator. Solutions to effectively design analog building blocks such as opamps, switches and comparators in low voltage, deep sub-micron CMOS process environment are presented.

Chapter 6 discusses the modulator floor plan, layout techniques and the modulator test results.

Chapter 7 summarizes the thesis and discusses some future work.

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CHAPTER 2. DOUBLE-SAMPLED ΔΣ MODULATER WITH RELAXED TIMING

A new double-sampled ΔΣ modulator topology is proposed to relax the critical timing constraints in the modulator feedback path, thus the speed requirement of the quantizer and DEM logic can be greatly reduced. To verify the proposed modulator topology, a second-order double-sampled delta-sigma modulator was designed and simulated.

2.1. Introduction

With the continuing down scaling of CMOS technology, delta-sigma (ΔΣ) analog-to-digital converters are becoming more and more popular in wideband applications such as wireless communication systems, high definition television, medical image, etc. There are two possible realizations of a delta-sigma modulator. One is based on discrete-time (DT) switched capacitor (SC) circuitry which traditionally was used to achieve very high resolution within low signal bandwidth. The other one employs continuous-time (CT) circuitry. Due to the exponential settling nature of its internal integrators, the maximum sampling frequency of a DT ΔΣ modulator is a lot lower than its CT counterparts especially when low power consumption is required. As a consequence, most of the recent ΔΣ ADCs incorporate CT modulators when the signal bandwidth goes beyond 10 MHz or more [1] [2]. However, compared to CT modulators, DT modulators do offer several advantages: 1. The performance is less

sensitive to clock jitter; 2. Signal transfer function (STF) and noise transfer function (NTF) rely on capacitor matching which can be made very accurate in modern CMOS technology; 3. It is very easy to scale the sampling frequency which makes the multi-standard applications possible; 4. Design methodology for a DT modulator is well established. Despite the aforementioned advantages, efforts must be taken to extend the signal bandwidth of a DT modulator in a low power design. Double sampling is a very powerful technique to achieve an effective sampling frequency that is twice the actual modulator clock frequency. Since the two clock phases are no longer distinguishable, the quantization operation is performed primarily during the non-overlapping times of the clocks. This situation gets even worse with the use of a multi-bit quantizer with dynamic element matching (DEM) algorithms. In order to make the modulator functional, the required speed for the quantizer and DEM logic should be much higher than the clock frequency of a ΔΣ modulator. In this chapter, a novel double-sampled ΔΣ modulator topology is proposed to solve this critical timing constraint.

2.2. Timing Issues In Double-Sampled ΔΣ Modulators

Fig. 2.1 illustrates a single-ended version of a double-sampled SC integrator that is controlled by two non-overlapping clock phases. During phase Φ1, Cs1 samples the input and Cs2 transfers the previously sampled charge to C_F. During phase Φ2, Cs1 transfers its charge to C_F and Cs2 samples the input. As a result, the output of the integrator is updated during both phases. The effective sampling frequency is twice the actual clock frequency. Note that double-sampling technique does not put any extra

requirements for opamp settling time.

Double-sampling is definitely desired when a DT SC ΔΣ modulator processes wide bandwidth input signal. For instance, with an input signal bandwidth of 10 MHz and an oversampling ratio (OSR) of 16, instead of having a sampling frequency of 320 MHz, only 160 MHz clock frequency can be used in a double-sampled SC ΔΣ modulator. Therefore, significant power savings can be anticipated.

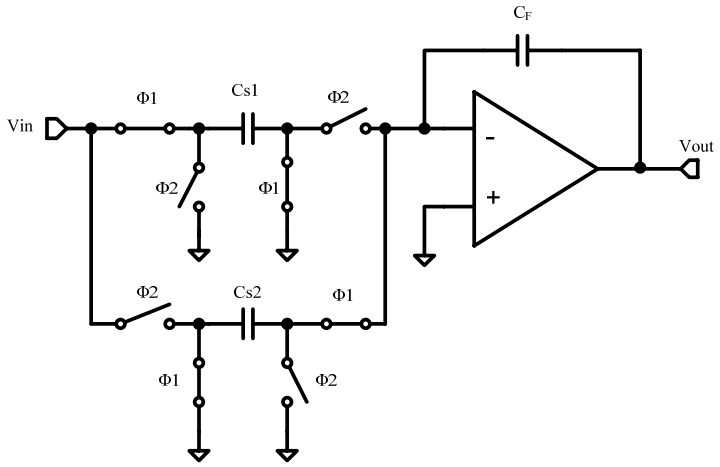

Figure 2.1 Single-ended version of a double-sampled SC integrator

However, double sampling has several disadvantages that limit its applications. One of them is caused by the capacitor mismatch in the feedback DAC. This problem can be tackled by either using a fully floating differential SC integrator [3] or its modified version [4]. Here, this problem is not discussed and for the feedback DAC, perfectly matched capacitors are assumed during phase Φ1 and phase Φ2.

The other major disadvantage is the feedback timing constraints. Fig. 2.2 shows a double-sampled SC ΔΣ modulator with a direct feed-forward path [5]. Currently this topology is widely employed in the design of wideband, low OSR SC ΔΣ modulators.

Because of the direct input signal feed-forward, the modulator has a unity STF. The loop filter has to process the quantization noise only. The removal of the input signal component reduces the voltage swing of the loop filter internal nodes allowing efficient opamp configurations. In addition, distortion becomes independent of the input signal resulting in an improvement of the modulator linearity.

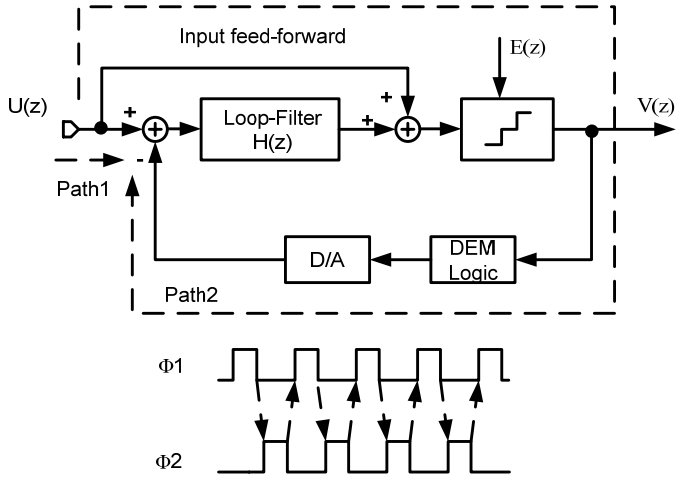

Figure 2.2 Double-sampled ΔΣ modulator with feed-forward path

In Fig. 2.2, the input signal is sampled on the corresponding sampling capacitors at the end of each clock phase Φ1 and phase Φ2 which is labeled as Path1. Meanwhile at the end of Φ1 and Φ2, the input signal and the output of the loop filter should be added. The result of this summation is then quantized and fed back to the input node of the loop filter to perform a subtraction with the input signal. These operations are labeled as Path2. Only when the delays of Path1 and Path2 are matched can the input signal be entirely cancelled in front of the loop filter. Due to double sampling, quantization and feedback operations must be done within the non-overlapping times

between clock phase Φ1 and Φ2. In wideband applications, low OSR is always chosen in order to save power consumption. Therefore a multi-bit quantizer is introduced to improve the resolution of a ΔΣ modulator. Under this circumstance, the multi-bit feedback DAC located at the input of the loop filter has to be linearized by some sorts of DEM logic so as to not degrade the overall performance. Data weighted averaging (DWA) is a popular way to linearize the DAC. A well designed DWA only adds a shifter in the modulator feedback path while the pointer calculation can be done outside the loop.

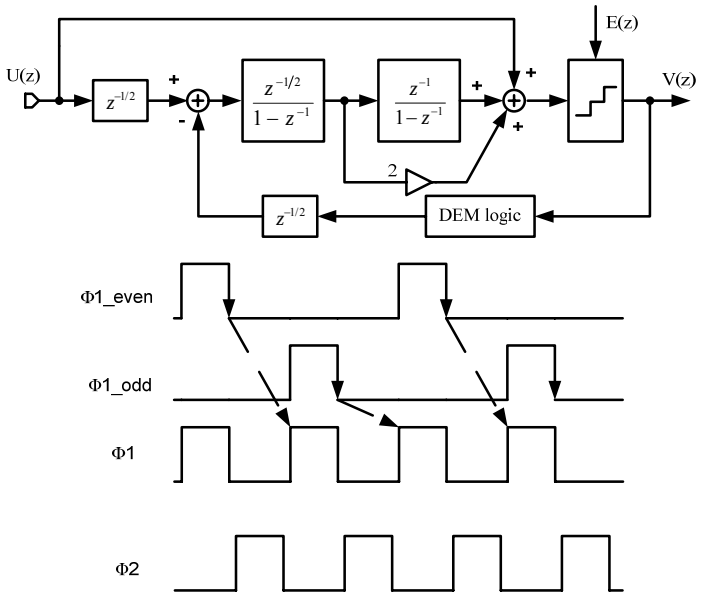

Figure 2.3 SC single-sampling ΔΣ modulator with relaxed feedback timing

Even so, the DWA logic will add extra delay in the feedback path. After the design is finished and laid out, this delay will be larger with the introduced parasitic capacitance. If the overall delay is longer than the non-overlapping time, the

performance of a ΔΣ modulator will be degraded, or it will not work at all. One simple solution is to increase the non-overlapping time. However it reduces the sampling and integration time. On other words, opamps in the loop filter need to be faster and consume more power.

In [6], a ΔΣ modulator employs two sets of capacitors to sample the input signal. The block diagram of the ΔΣ modulator is illustrated in Fig. 2.3, and Fig. 2.4 gives a detailed single-ended switched level diagram. This modulator topology allows inserting a half-cycle delay in both path1 and path2, thus half of the clock period can be allocated to the quantization and DEM logic. Note that the first integrator actually becomes a half-cycle delayed integrator. This method is very useful in the single-sampled ΔΣ modulators. Unfortunately there are no half-cycle delayed integrators in a double-sampled ΔΣ modulator. Therefore it is not straightforward to incorporate this technique in a double-sampled ΔΣ modulator.

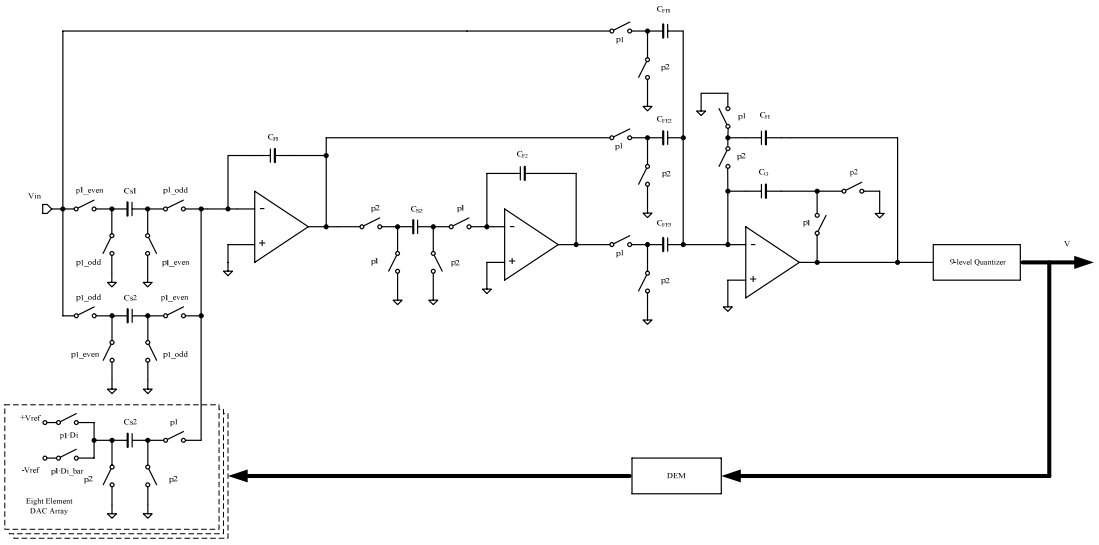

Figure 2.4 Diagram of SC single-sampled ΔΣ modulator with relaxed feedback timing (shown single-ended for simplicity)

It is also worthwhile to mention that a double-sampled ΔΣ modulator with feedback topology shown in Fig. 2.5 also suffers from feedback timing constraints: DEM logic and the quantization still have to be done during the non-overlapping times of the clock. A single-sampled ΔΣ modulator with the same block diagram, however, has a half clock period to perform quantization and DEM logic.

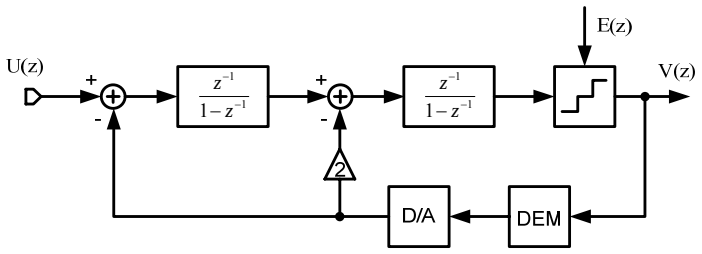

Figure 2.5 Double-sampled ΔΣ modulator with feedback topology

2.3. Proposed Double-Sampled Delta-Sigma Modulator

A new double-sampled ΔΣ modulator topology is proposed to relax the critical timing constraints [7]. This topology is based on the direct feed-forward topology in [5]. A second-order example is shown in Fig. 2.6. A full-cycle delay is inserted at both the input sampling path and the feedback path, thus a half-cycle clock period can be allocated to the quantization and DEM logic (note that in a double-sampled ΔΣ modulator, a half clock period is equivalent to an effective sampling period). In most cases, this half clock period is long enough for the quantization and DEM logic. This results in a relaxed speed requirement and robust operation. However the STF of the modulator is no longer equal to 1 and the low distortion property is lost. In order to maintain the unity STF, two full-cycle delayed branches can be added. One is from

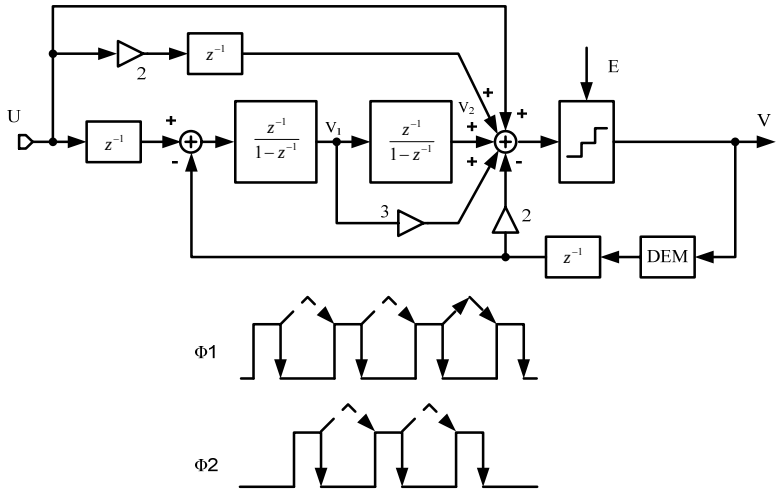

Figure 2.6 Proposed double-sampled ΔΣ modulator with relaxed feedback timing

modulator input, while the other is from modulator output. Both are connected to the summing node in front of the quantizer. Since there is already a summing node in the feed-forward topology, these two branches add only minor hardware complexity.

Linearized analysis of the system in Fig. 2.6 gives:

$$STF = \frac{V(z)}{U(z)} = 1 \tag{2.1}$$

$$NTF = \frac{V(z)}{E(z)} = (1 - z^{-1})^2 \tag{2.2}$$

$$V_1(z) = -z^{-2}(1 - z^{-1})E(z) \tag{2.3}$$

$$V_2(z) = -z^{-3}E(z) \tag{2.4}$$

where E(z) is the quantization noise from the internal quantizer. The unity STF is still maintained, while the NTF becomes a second-order pure differentiator high-pass function. The first opamp output v1 contains shaped quantization noise, and the second opamp output v2 contains only the delayed version of the quantization noise As a result, the output swing and linearity requirements of the opamps can be relaxed. Hence, the proposed modulator topology achieves the low-distortion property and relaxes the feedback timing constraints simultaneously.

The key operation of the proposed modulator topology can be expressed as follows: the input signal is sampled at the end of Φ1 (or Φ2), then held for the entire Φ2 (or Φ1) and processed at the next Φ1 (or Φ2). During the holding phase, the quantization and DEM logic can be operated. This process implies that the sampling capacitor is busy for three clock phases. But input signal must be sampled at the end of both Φ1 and Φ2 in a double-sampled ΔΣ modulator. So, instead of having two sets of sampling capacitors, in the proposed modulator topology, three sets of sampling capacitors should be used. The penalty for the proposed solution is a slightly increase in the chip area. An SC implementation for the first integrator in proposed modulator is shown in Fig.2.7 in the single-ended form for simplicity. Every sampling branch utilizes dedicated clock phases, shown as Φa, Φb and Φc, which can be generated from Φ1 and Φ2.

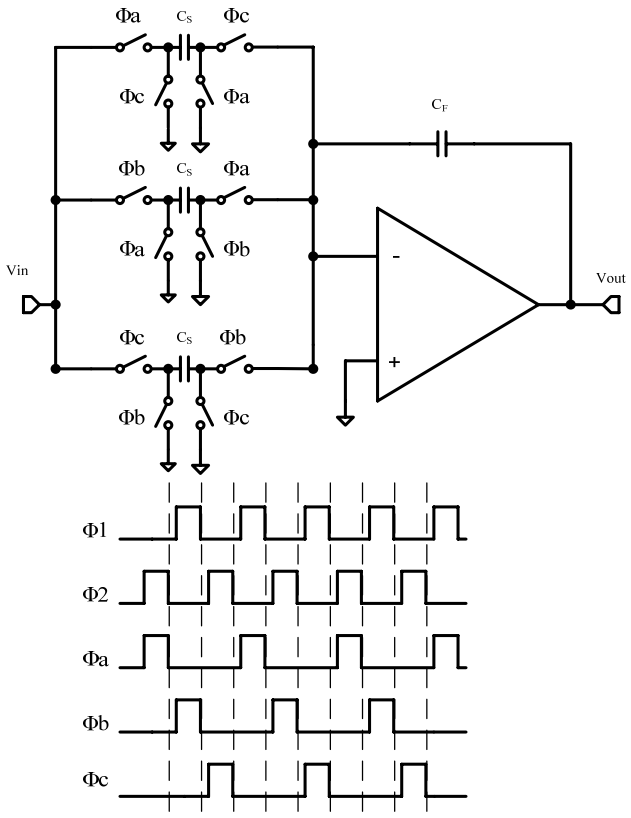

Figure 2.7 SC implementation of the first integrator

It is well known that double-sampled modulators are sensitive to the capacitor mismatch in the feedback DAC. This problem can be solved by using a modified fully-floating differential SC integrator [4]. In this design, the capacitors for the input sampling and the feedback DAC are separated to avoid the quantization noise folding back to the signal band.

2.4. Simulation Results

To verify the effectiveness of the proposed modulator topology shown in Fig.2.6, the transient behavior of a second order double-sampled SC ΔΣ modulator circuit was

simulated in Cadence Spectre simulator. The opamps were represented by macro models with finite gains (50dB). The output digital bits were sampled and processed in MATLAB.

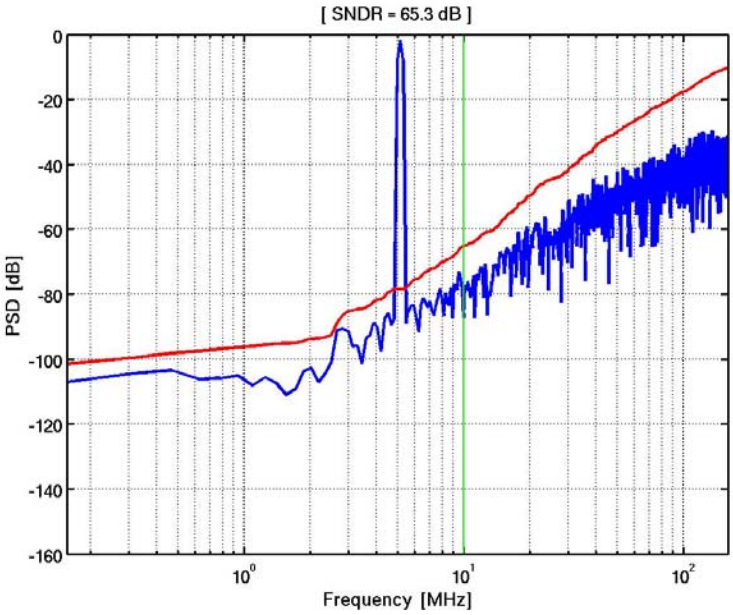

Figure 2.8 Simulated PSD of a second-order proposed double-sampled ΔΣ modulator.

Assume a 10 MHz signal bandwidth, an oversampling ratio of 16, and a 3-bit quantizer. Because of the double sampling, the actual modulator clock frequency is 160 MHz. Fig. 2.8 shows the simulated output spectrum of the proposed second-order double-sampled ΔΣ modulator with a -2 dBFS input signal. The simulated SNDR is 65.3 dB which does not include thermal noise and other circuit non-ideal effects.

As a comparison between the double-sampled ΔΣ modulator and single-sampled ΔΣ modulator, the second order ΔΣ modulator shown in Fig. 2.6 was also simulated in the single-sampling mode with the clock frequency of 160 MHz. This clock frequency

leads to the OSR of only 8 for a 10 MHz signal bandwidth. Fig.2.9 shows the simulated output spectrum of the single-sampled second order ΔΣ modulator with a -2 dBFS input signal. The simulated SNDR is 50.0 dB, which is about 15 dB lower than that of a double-sampled second order ΔΣ modulator. In order to achieve the same SQNR, a single-sampled second order ΔΣ modulator must be clocked at 320 MHz. However this will inevitably increase the overall modulator power consumption.

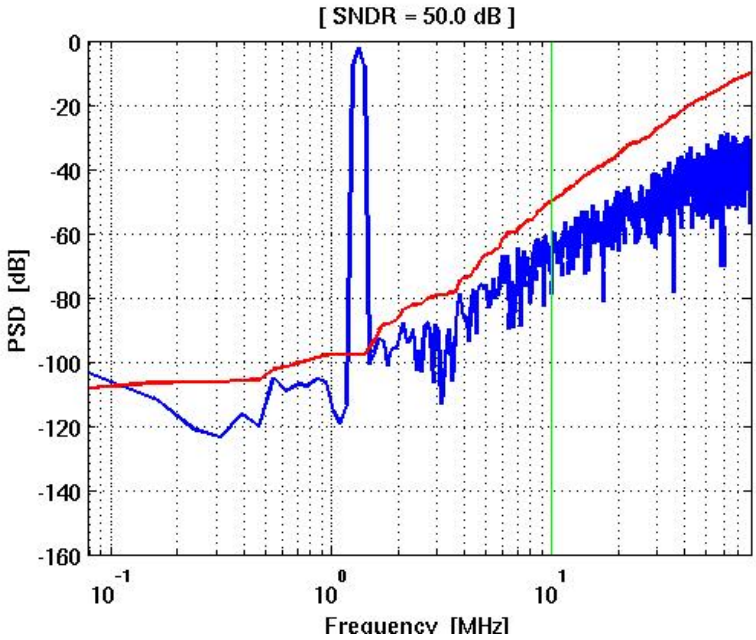

Figure 2.9 Simulated PSD of a second-order single-sampled ΔΣ modulator

2.5. Summary

A new double-sampled delta-sigma modulator topology was proposed to solve the feedback critical timing constraints. The speed requirement of the quantizer and DEM logic can be greatly relaxed. This new modulator topology also shows a unity signal transfer function, and the loop filter processes the quantization noise only. The above

features make it a good candidate for wideband, high linearity and low power applications.

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CHAPTER 3. A NEW DWA REALIZATION WITH HARDWARE REDUCTION

This chapter presents a new Data Weighted Averaging (DWA) realization. Compared to the popular implementation the proposed one has less hardware consumption.

3.1. Introduction

Delta-sigma (ΔΣ) modulators that process wide bandwidth input signals often utilize a multi-bit internal quantizer. The effect of this multi-bit quantizer to a ΔΣ modulator is two-fold. On one hand it improves the modulator stability. On the other hand, modulator SQNR will improve by 6 dB every time the quantizer doubles its resolution. However, the feedback DAC, especially the one at the modulator input must be linearized to maintain the overall modulator performance. Among various linearization methods, data-weighted-averaging (DWA) [1] is widely deployed at both research community and industry due largely to its simplicity and effectiveness.

The effectiveness of DWA to a ΔΣ modulator can be seen through behavioral level simulation in Matlab. In simulation, a randomly distributed 0.1% DAC unit element mismatch is added in the first DAC of a 12-bit ΔΣ modulator. Fig.3.1 shows the output spectrum of the modulator with the DWA disabled. As expected, the modulator SNDR drops to 62.3 dB. Fig.3.2 shows the output spectrum of the modulator with the DWA enabled. Now modulator SNDR is brought back to 73.2 dB.

3.2. A common DWA realization

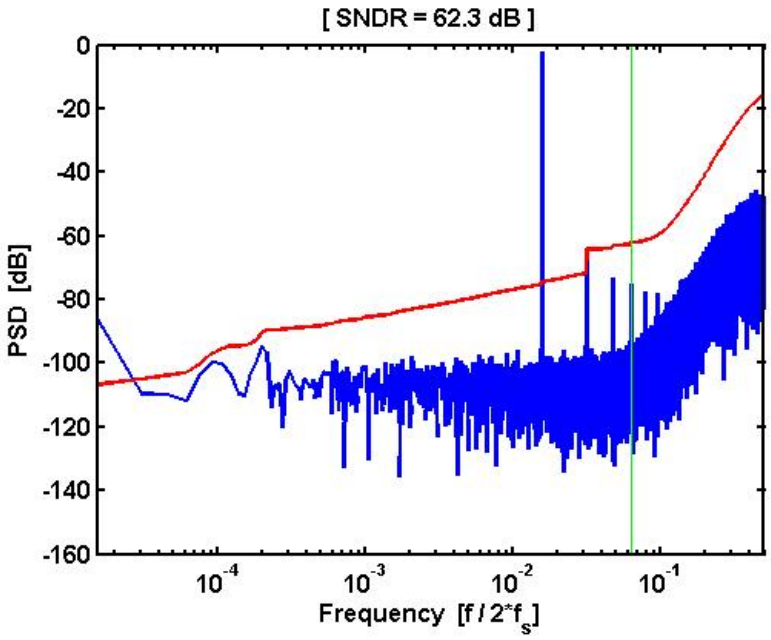

Figure 3.1 ΔΣ modulator output spectrum with 0.1% DAC mismatch without DWA

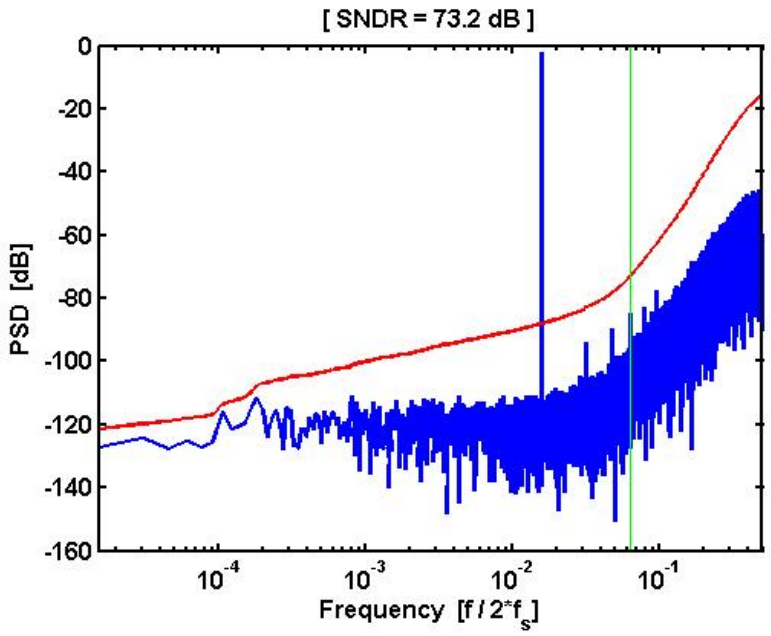

Figure 3.2 ΔΣ modulator output spectrum with 0.1% DAC mismatch with DWA

A general description of the DWA algorithm with a 9-level DAC is illustrated in Fig.3.3.

The DWA algorithm is simple and straightforward to understand. The DAC unit elements are in a rotated fashion. Each time the DAC elements are to be selected from the first unused element in the previous DAC operation. By performing rotation in such a way for a long time will result a first-order noise shaping for the DAC unit element error [2].

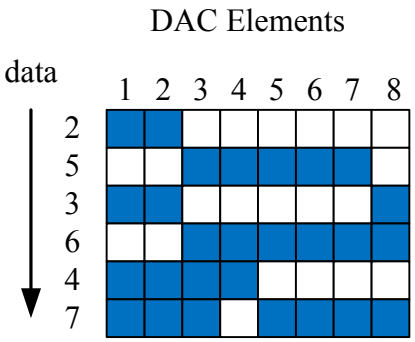

Figure 3.3 DWA algorithm

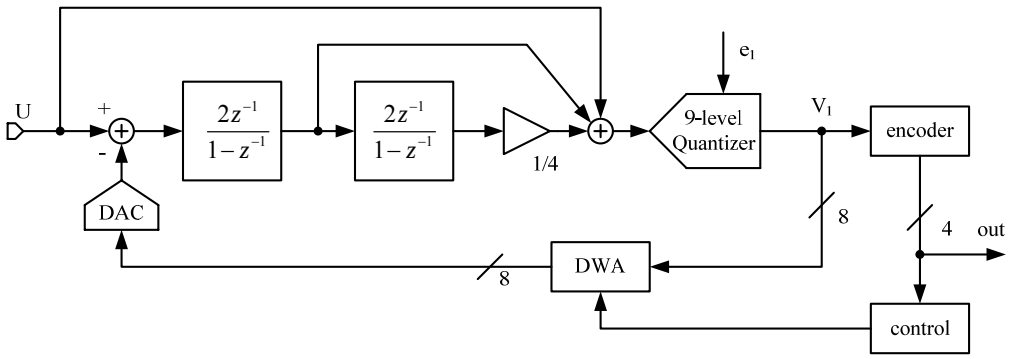

Figure 3.4 A second order 9-level ΔΣ modulator with DWA

A second order ΔΣ modulator with a 9-level quantizer and DWA is shown in Fig.3.4.

As we can see, a well designed DWA circuit adds only a shifter in the modulator feedback path [3]. The pointer calculation can be performed outside the modulator loop. Therefore, it is not necessary for the DWA control block to wait for the most recent quantizer result in order to determine the proper control word applying to the DWA scrambling block. This approach reduces the delay through the loop and enables a higher resolution quantizer. Fig.3.5 shows a simplified block diagram of the DWA system for the case of a 9-level DAC. The digital output of the quantizer is sent in a 8-bit thermometer-encoded format to a shifting block and to a pointer arithmetic block. The pointer arithmetic block converts the thermometer encoded word to binary format and performs 4-bit modulus integration of the binary word with a 4-bit adder with carryout and a 3-bit pointer register. The pointer register stores the pointer control word and applies it to the shifting block and to one input of the 4-bit adder. The pointer control word is updated each sampling cycle of the ADC. The shifting block shifts the 8-bit thermometer encoded word a fixed number of digital positions in response to the pointer control word that is received from the pointer arithmetic block. The shifting block is made up of three logarithmic shifter cells that each respond individually to a single digit of the 3-bit binary control word P. The logarithmic shifter resides within the loop of the modulator and adds a small amount of delay to the loop feedback path–the equivalent of three transmission gate delays for the case of a 9-level quantizer

Note that this kind of DWA scrambles the quantizer output while fixing the DAC elements. Also a binary coded accumulator is needed to calculate the pointer.

3.3. Proposed DWA realization

If we perform DWA in such a way that unit DAC elements are rotated while fixing the quantizer output, another DWA implementation exists. This section describes this new DWA implementation in detail. For sake of simplicity a 5-level DAC is used even though this implementation is applicable to any multi-bit DAC.

A general description of the new DWA implementation with a 5-level DAC is illustrated in Fig.3.6. As a comparison, conventional DWA implementation is also shown in the figure. It is clear that these two DWA implementations achieve the same functionality.

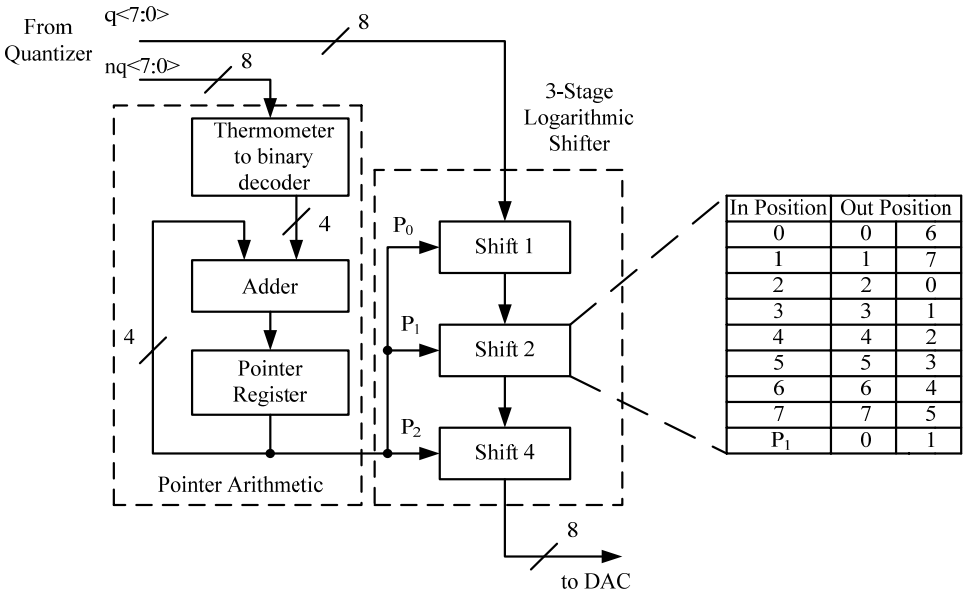

Figure 3.5 Detailed implementation of a DWA for 9-level DAC

Unlike conventional DWA implementation, in the proposed realization the pointer calculation is performed in the thermometer code domain. The pointer of the new implementation here only depends on the previous quantizer digital output. For example in Fig.3.6, if a pervious quantizer output is 3, with C2 is the first unused DAC element, and then next time C2 will be sitting in the bottom. Thus simpler circuit instead of digital accumulator can be used to save hardware consumption.

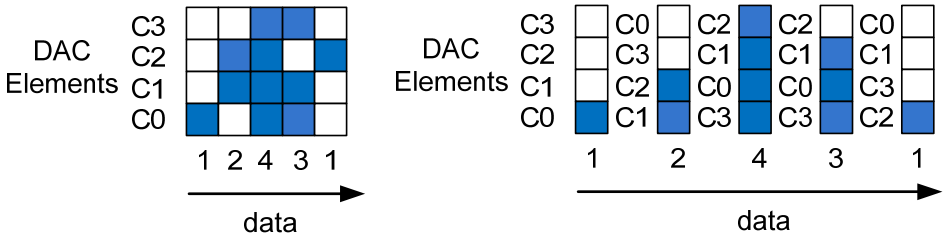

Figure 3.6 New DWA implementation compared with the conventional one

The mapping between DAC elements and the thermometer code can be realized by a barrel shifter as shown in Fig.3.7.

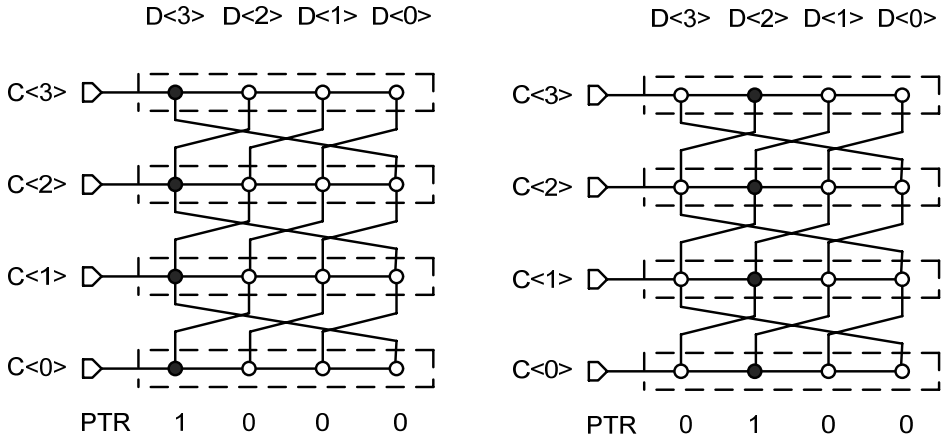

Figure 3.7 Barrel shifter mapping DAC elements and quantizer output digital code

There are only four possible pointer values for a 5-level DAC case. Fig.3.7 shows two of them. A complete mapping is shown in Fig.3.8.

Generating a new pointer is very easy in this DWA implementation. It only depends on the previous pointer and previous quantizer output. Their relationship is shown in Table.3.1.

PTR	1000	0100	0010	0001
D<3>	C<3>	C<0>	C<1>	C<2>
D<2>	C<2>	C<3>	C<0>	C<1>
D<1>	C<1>	C<2>	C<3>	C<0>
D<0>	C<0>	C<1>	C<2>	C<3>

Figure 3.8 Complete mapping between DAC elements and quantizer digital output code

Table 3.1 Complete mapping between DAC elements and quantizer digital output code

Quanntizer digital output / Previous PTR	0000/1111	0001	0011	0111
1000	1000	0100	0010	0001
0100	0100	0010	0001	1000
0010	0010	0001	1000	0100
0001	0001	1000	0100	0010

The key point to finding the new pointer is the extraction of 0-1 transition of the previous quantizer digital output. Then the new pointer can be shifted version of the previous pointer. As a result, another logarithmic shifter can be used to obtain the new pointer.

The complete new DWA implementation is illustrated in Fig.3.9.

The relationship between 4-bit quantizer digital output, 3-bit 0-1 transition detector output and 2-bit decoder output is shown in Table.3.2.

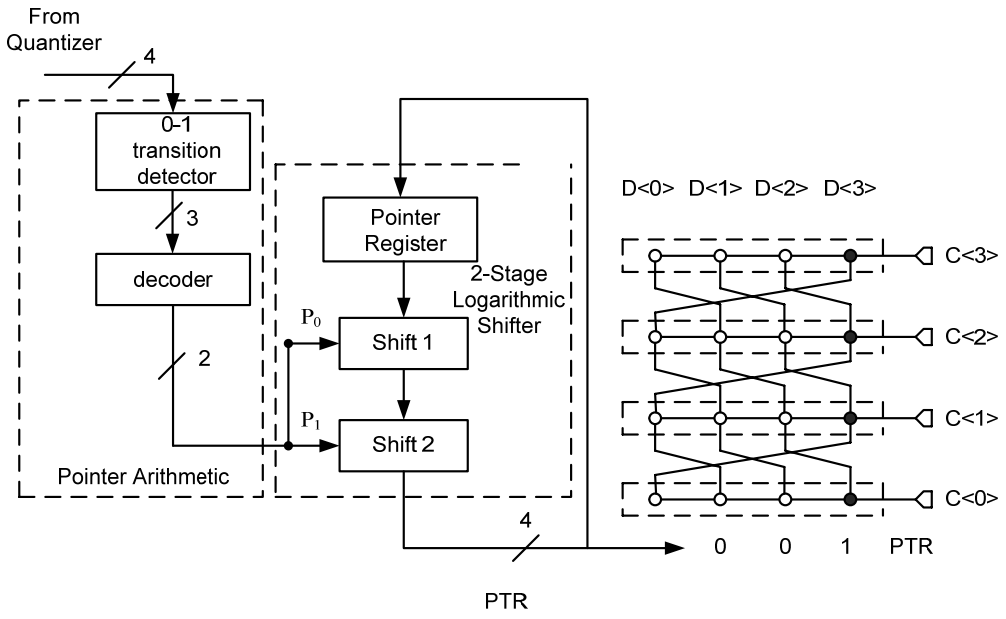

Figure 3.9 Block diagram of new DWA implementation (5-level DAC)

Table 3.2 Relationship of the pointer arithmetic

D<3>	D<2>	D<1>	D<0>	T<2>	T<1>	T<0>	P<1>	P<0>
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0	1
0	0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1	1
1	1	1	1	0	0	0	0	0

From the above table, the pointer arithmetic is simple and can be expressed using the logic expressions (3.1) - (3.5).

$$T<2>=\overline{D<3>}D<2>+D<3>\overline{D<2>} \tag{3.1}$$

$$T<1>=\overline{D<2>}D<1>+D<2>\overline{D<1>} \tag{3.2}$$

$$T<0>=\overline{D<1>}D<0>+D<1>\overline{D<0>} \tag{3.3}$$

$$P<1>=(\overline{T<2>}T<1>+T<2>\overline{T<1>})\cdot\overline{T<0>} \tag{3.4}$$

$$P<0>=(\overline{T<2>}T<0>+T<2>\overline{T<0>})\cdot\overline{T<1>} \tag{3.5}$$

The conventional DWA implementation is based on binary code domain. Therefore thermometer to binary conversion and accumulator are needed.

This new DWA implementation is done in the thermometer code domain. As a consequence, it can be realized very easily. The hardware consumption is expected to be greatly reduced when the quantizer resolution is around 3-5 bit.

3.4. Summary

Compared to the conventional DWA in Fig.3.5, the proposed DWA realization

achieves the same functionality. However, the thermometer to binary decoder and the accumulator is replaced with a simple 0-1 transition detector and another logarithmic shifter. As a consequence, the hardware consumption is greatly reduced which results a smaller die area.

It is interesting to note that this new DWA implementation can be used to shuffle the reference voltages in the multi-bit quantizer [4]. This method entirely eliminates the delay in the modulator feedback path. However, doing DWA in the multi-bit quantizer means reference voltage scrambling which is in the analog domain. In deep sub-micron CMOS process, MOS switches in the middle of the supply rail barely turn on. Even though boosted clock techniques can be utilized to reduce the switch-on resistance, switch design become more complicated. For high speed application, this nevertheless poses challenges in the circuit design. In our case, scrambling is done in the digital domain that is inherently a lot more robust over process, supply voltage and temperature variation.

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CHAPTER 4. CHARGE PUMP BASED SC INTEGRATOR

Charge-pump (SC) based switched-capacitor (SC) integrator is a promising technique to reduce opamp power consumption. In this chapter, a cross-coupling technique is proposed to eliminate parasitic capacitor effects in a CP based SC integrator. Also, design methodologies are introduced to incorporate a modified CP based SC integrator into a low-distortion ΔΣ modulator. A second-order ΔΣ modulator was designed and simulated to verify the proposed modulator topology.

4.1. Introduction

In recent years, broadband low power delta-sigma (ΔΣ) analog-to-digital converters are becoming more and more popular in applications such as wireless communication systems, high definition television, medical imaging, etc. There are two possible realizations of a ΔΣ modulator. One is based on discrete-time (DT) switched capacitor (SC) circuitry. The other employs continuous-time (CT) circuitry. SC ΔΣ modulators have some advantages over their CT counterparts, including having less sensitivity to clock jitter, and well defined signal transfer function (STF) and noise transfer function (NTF). There are ongoing efforts to effectively extend the bandwidth of an SC ΔΣ modulator while maintaining low power consumption. Basically, two approaches can be explored to achieve this commitment. The first one deals with architectural innovation. Amongst various new ΔΣ modulator architectures, low-distortion topology [1] is a very attractive one. The other approach focuses on transistor level design.

Recently, Nilchi and Johns came up with a charge-pump (CP) based SC integrator [2]. With the same thermal noise level as a conventional SC integrator, this CP based integrator offers smaller capacitive loading and larger feedback factor that makes it faster and consume less power. However the input full scale range of the ΔΣ modulator using CP based integrator has to be halved due to the double feedback DAC voltage. Therefore the modulator will lose dynamic range by as much as 6 dB. In order to conquer this potential drawback, a modified CP SC integrator [3] is proposed here to recover the modulator's full scale input range. But the fact that the input signal and feedback signal are sampled in the same clock phase makes it not very straightforward to incorporate the modified CP SC integrator into a low-distortion ΔΣ modulator topology.

In this chapter, a cross-coupling technique is proposed to eliminate parasitic capacitor effect in a CP based SC integrator. Then, design methodologies are introduced to incorporate a modified CP based SC integrator into a low-distortion ΔΣ modulator. A second-order ΔΣ modulator was designed and simulated to verify the proposed modulator topology.

4.2. Charge Pump Based Switched Capacitor Integrator

A CP based SC integrator [2] is shown in Fig.4.1 in a single–ended configuration. Vin is the input signal and Vdac comes from feedback DAC. Sampling capacitor Cs is divided into two halves with $C_{S1}=C_{S2}=C_S/2$. During the sampling phase p1, input signal is sampled on both capacitors. During the integration phase p2, C_{S1} and C_{S2} are

connected in series and discharge into the integrating capacitor C_F. Applying charge conservation, the transfer function of this CP based SC integrator can be expressed as,

$$V_{out}[n]-V_{out}[n-1]=\frac{1}{2}\frac{C_S}{C_F}\{(V_{in}[n-1])-\frac{1}{2}V_{DAC}\} \qquad (4.1)$$

As can be seen from (4.1), the integrator gain can be accurately set by the capacitor ratio. Compared to a conventional parasitic insensitive SC integrator, CP based SC integrator offers a smaller capacitive loading and a larger feedback factor when realizing the same integrator gain and same input thermal noise level. One potential drawback for this CP based SC integrator is that the 1/2Vdac term in (4.1) can reduce the modulator dynamic range by as much as 6dB which is truly undesired in a low supply voltage design.

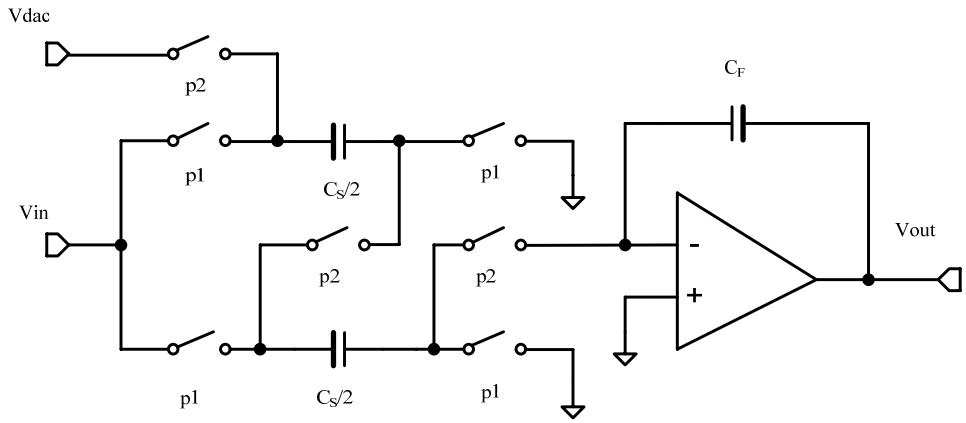

Figure 4.1 CP based SC integrator

A modified CP based SC integrator is proposed in [3] aiming to mitigate the input dynamic range reduction while maintaining all the other advantages of the CP based SC integrator. The circuit is shown in Fig.4.2 in a single-ended configuration.

Feedback DAC voltage is sampled during p1 instead of p2. Applying charge conservation, the transfer function of this modified CP based SC integrator can be expressed as,

$$V_{out}[n]-V_{out}[n-1]=\frac{1}{2}\frac{C_S}{C_F}\{(V_{in}[n-1])-V_{DAC}\} \tag{4.2}$$

The gain of the modified CP based SC integrator remains unchanged, but the 1/2 term before the Vdac is eliminated, which means ΔΣ modulator input full scale range is not limited to be less than half the Vdac.

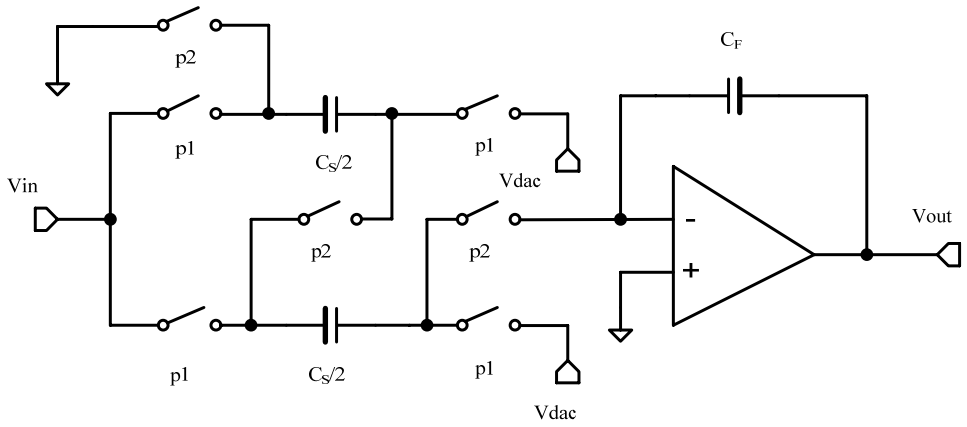

Figure 4.2 Modified CP based SC integrator

4.3.Parasitic Insensitive Charge-Pump-Based SC Integrator

The calculation of the integrator transfer function in the proceeding section ignored the parasitic capacitance due to the creation of the sampling capacitors as well as the nonlinear capacitance associated with the switches. The addition of such parasitic capacitance results in the circuit is shown in Fig.4.3. Here, C_{PT1} represents the parasitic capacitance of the top plate of the upper sampling capacitor as well as the

nonlinear capacitance associated with the switches. C_{PB1} represents the parasitic capacitance of the bottom plate of the upper sampling capacitor as well as the nonlinear capacitance associated with the switches. C_{PT2} represents the parasitic capacitance of the top plate of the lower sampling capacitor as well as the nonlinear capacitance associated with the switches. C_{PB2} represents the parasitic capacitance of the bottom plate of the lower sampling capacitor as well as the nonlinear capacitance associated with the switches.

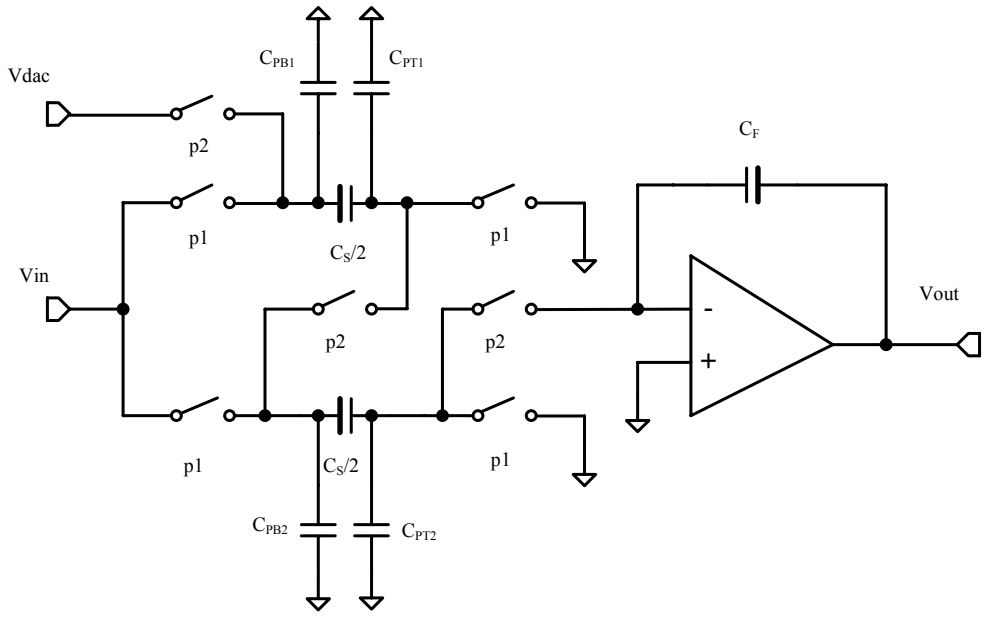

Figure 4.3 CP based SC integrator with parasitic capacitor

In accounting for these parasitic capacitances, we can immediately discard the effect of C_{PT2} since it connects to ground during p1 and virtual ground during p2. The effect of C_{PB1} is also not important. Even though this capacitor is charged to Vin

during p1, it will be discharged during p2. Applying again charge conservation with C_{PT1} and C_{PB2} the integrator transfer function can be expressed as:

$$V_{out}[n]-V_{out}[n-1]=\frac{1}{2}\frac{C_S}{C_F}\{\frac{C_S+C_{PT1}}{C_S+C_{PB2}+C_{PT1}}\cdot V_{in}[n-1]-\frac{C_S}{2(C_S+C_{PB2}+C_{PT1})}\cdot V_{DAC}\} \quad (4.3)$$

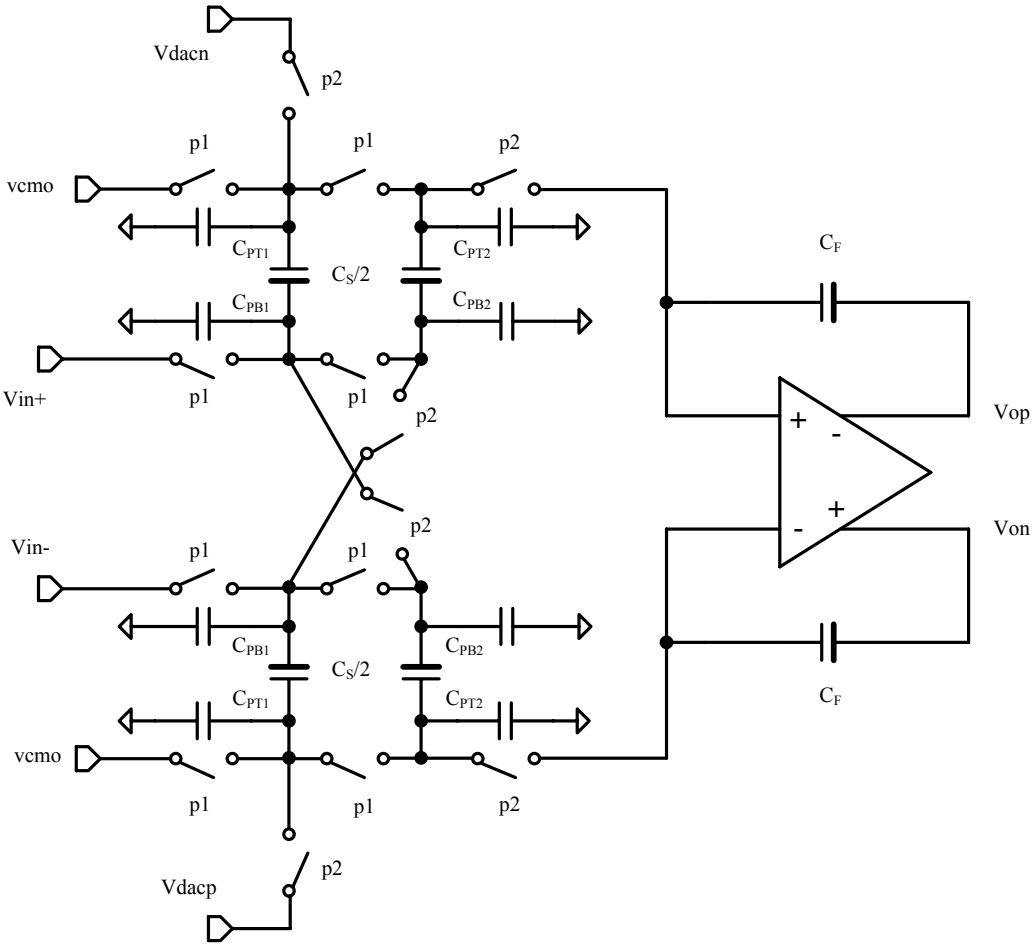

Figure 4.4 Fully differential CP based SC integrator with parasitic capacitors

From (4.3), we see that the gain coefficient is highly related to the parasitic coefficient C_{PT1} and C_{PB2} which is not well controlled and would be quite nonlinear

due to the use of large input sampling switches. Therefore this effect must be addressed in high linearity applications.

Modern integrated circuit design always employs fully differential circuit to mitigate supply and substrate noise, enhance common mode rejection and improve linearity. Fortunately, the parasitic effect in the CP based SC integrator can be completely eliminated in a fully differential configuration.

A fully differential CP based SC integrator with parasitic capacitors is shown in Fig.4.4. The key point here is to cross couple the sampling capacitor between the positive and negative sampling branch. Let us again check out the effect of parasitic capacitors one by one. Similar to the discussion before, we can discard the effect of C_{PT2}, since it connects to ground during p1 and virtual ground during p2. The effect of C_{PT1} is also unimportant. Even though this capacitor is charged to Vin during p1, it will be discharged during p2. Parasitic capacitors C_{PB1} and C_{PB2} in the positive sampling branch are charged to vin(n-1) C_{PB1} and vin(n-1) C_{PB2} respectively. Meanwhile, parasitic capacitors C_{PB1} and C_{PB2} at the negative sampling branch are charged to -vin(n-1) C_{PB1} and -vin(n-1) C_{PB2}. Therefore assuming perfect symmetry, by cross coupling the sampling capacitors in the positive and negative sampling branch results the complete cancellation of these parasitic charges. Without the parasitic charges, integrator transfer function shall be restored and linearity be improved.

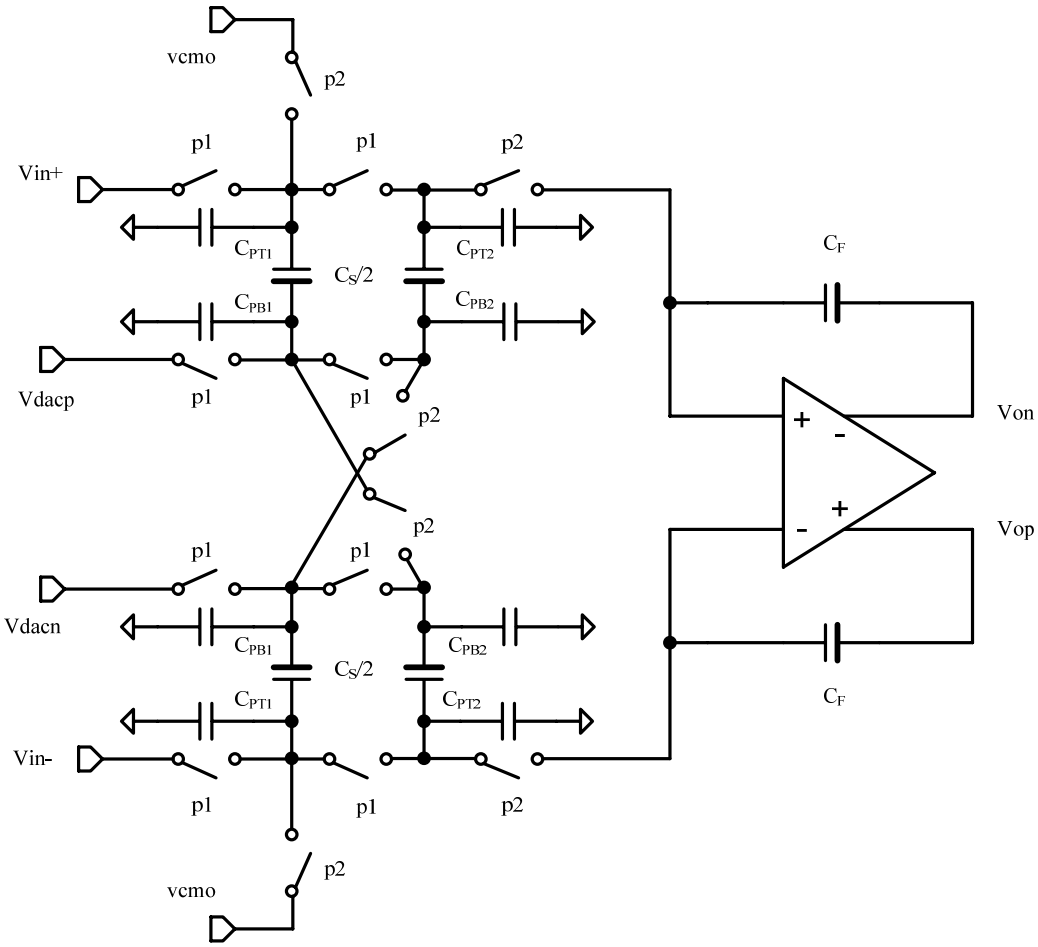

Figure 4.5 Modified CP based SC integrator insensitive to parasitic capacitance

This cross-coupling concept can be extended to the modified CP based SC integrators. A fully differential modified CP based SC integrator with parasitic capacitors is shown in Fig.4.5. In Fig.4.5, input signal and feedback DAC output are sampled simultaneously during p1. As is well known, feedback DAC output contains not only the signal content but also shaped quantization noise. In order to not degrade the integrator linearity, the top plate of the sampling capacitors is used to sample the input signal during p1 and to switch to the opamp virtual ground during p2. This

arrangement changes the polarity of the integrator transfer function which is not a problem in a fully differential implementation.

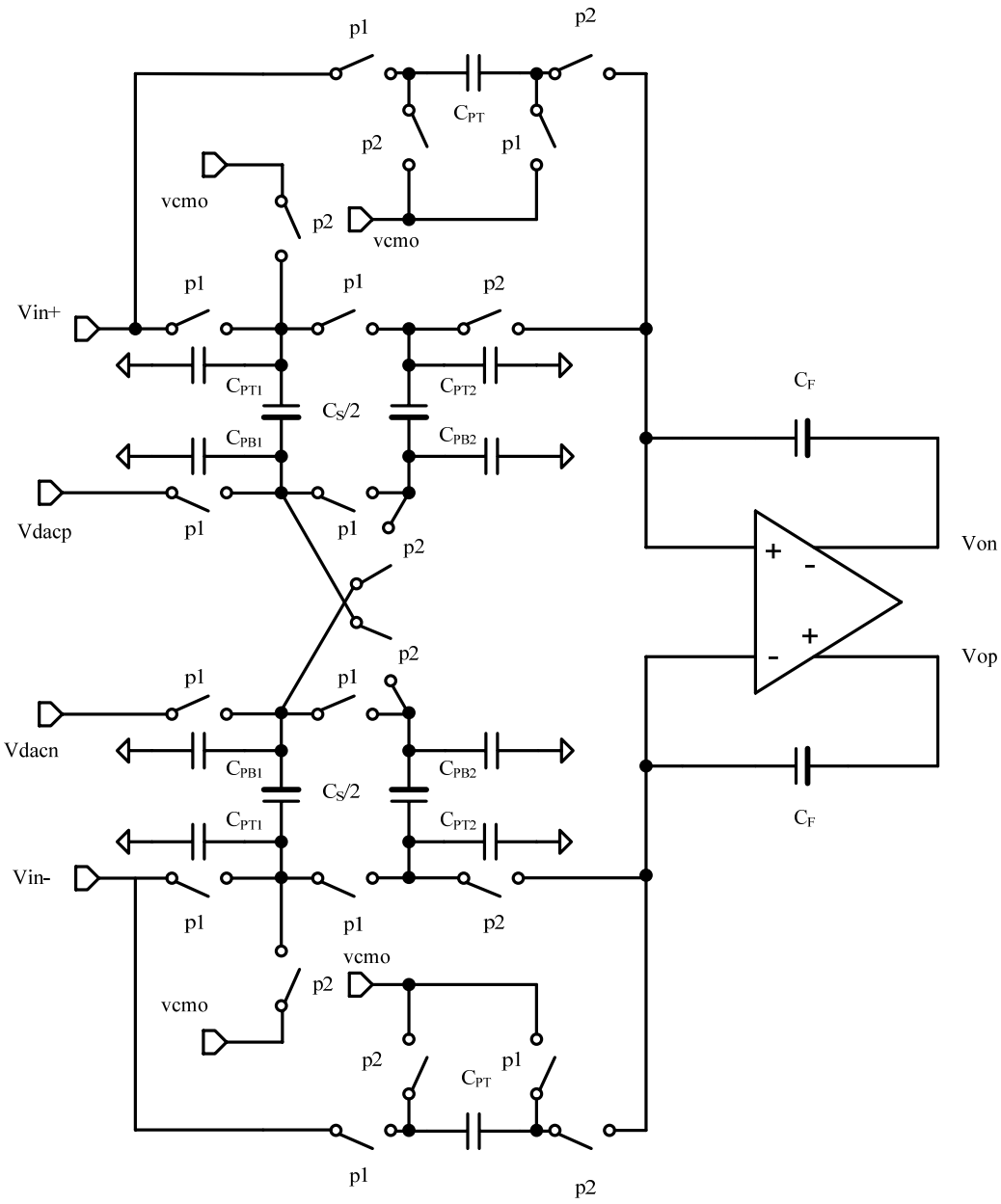

Figure 4.6 Modified CP based SC integrator insensitive to parasitic capacitor

In Fig.4.5, the effect of C_{PT1} is also unimportant as discussed before. Parasitic capacitors C_{PB1} and C_{PB2} in the positive sampling branch are charged to vdac(n-1) C_{PB1} and vdac(n-1) $C_{PB2,}$ respectively. Meanwhile, parasitic capacitors C_{PB1} and C_{PB2} at the negative sampling branch are charged to -vdac(n-1) C_{PB1} and -vdac(n-1) C_{PB2}. Therefore by cross coupling the sampling capacitors in the positive and negative sampling branch results the cancellation of these parasitic charges.

The parasitic capacitor C_{PT2} in Fig.4.5 is troublesome here. Its effect can be analyzed differently considering the particular CMOS process used for the design. In a mixed signal CMOS process where MIM (Metal-Insulator-Metal) capacitor is available, the top plate parasitic of a MIM capacitor is so small as to not cause significant nonlinearity and distortion. However, in the process node 130nm below, MOM (Metal-Oxide-Metal) capacitor is widely adopted. The reasons are two-fold. First, its capacitance density is higher than a normal MIM capacitor. Second, it does not require any additional process mask, which leads to a lower cost. Despite its advantages, MOM capacitors have larger parasitic capacitance at both plates. Hence, if MOM capacitors are used, the effect of C_{PT2} can not be ignored. Under most circumstances, the sampling capacitor Cs is large. Let Cs be 2pF. Assuming a reasonable percentage of the parasitic capacitance, at the top plate is 5%. Then C_{PT2} is 50fF. An elaborate way to cancel the parasitic charge on C_{PT2} is to assign a dedicated small capacitor C_{PT} as shown in Fig.4.6. C_{PT} is charged to -vin(n-1) C_{PT} during p1 and switched to the opamp virtual ground during p2 to cancel the parasitic charge vin(n-1) C_{PT2}. Complete charge cancellation is expected if C_{PT} is equal to C_{PT2} which is not a

very difficult task. Since C_{PT} is usually small, switches associated with it tend to be small as well. The only downside of this scheme is a slightly reduced feedback factor during the integrating phase.

4.4. Low Distortion ΔΣ Modulator Employing CP Based SC Integrator

Fig.4.7 illustrates a general structure of a single-quantizer ΔΣ modulator. This structure consists of two parts: the loop filter and the quantizer. The loop filter is a linear part, under most circumstances containing opamp based integrators. As the input signal goes directly through the loop filter, linearity requirement of the loop filter should be high enough to at least match the overall modulator's specification. In the actual design, such requirement mandates to use highly linear opamps. However, in deep sub-micron CMOS process under low supply voltage, it is a very demanding task to design an opamp with low power consumption and high linearity simultaneously.

Fig.4.8 shows the block diagram of a low-distortion ΔΣ modulator. The key feature of this topology is a direct feed-forward path from modulator input to the internal quantizer. By doing this way, loop filter contains no longer the input signal but only the filtered quantization noise. Since the loop filter does not need to process the input signal, its linearity requirement can be significantly relaxed which is a great advantage. Another benefit is the reduced integrator output swing. This fact allows the use of more power efficient telescopic or folded-cascode OTAs to greatly reduce the modulator power consumption. As a result, since its inception, many ΔΣ modulator

designs adopted this low-distortion topology and their experimental results demonstrated excellent linearity and power efficiency performances [4] [5].

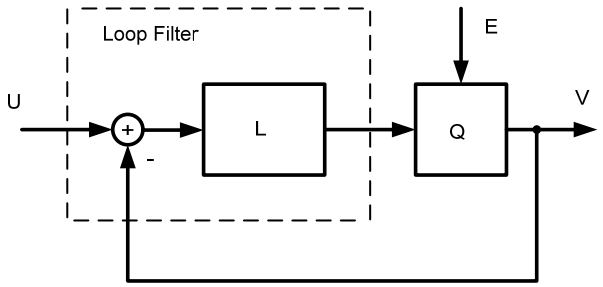

Figure 4.7 A structure of a single-quantizer ΔΣ modulator

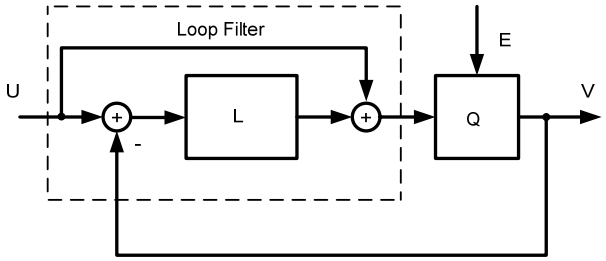

Figure 4.8 A general structure of a low-distortion feed-forward ΔΣ modulator

To achieve a broadband and low power ΔΣ modulator design, it is an effective measure to combine low distortion topology and CP based SC integrator. The original CP based SC integrator can fit into the low-distortion topology without any problem. However, employing the modified CP based SC integrator is not straightforward since there is an explicit half-cycle delay in the modulator feedback path due to the fact that input signal and the feedback DAC signal are sampled at the same clock phase. Adding this half-cycle delay into the feedback path of a feed-forward ΔΣ modulator

may cause instability. As a consequence, some measures should be taken to mitigate this additional half-cycle delay.

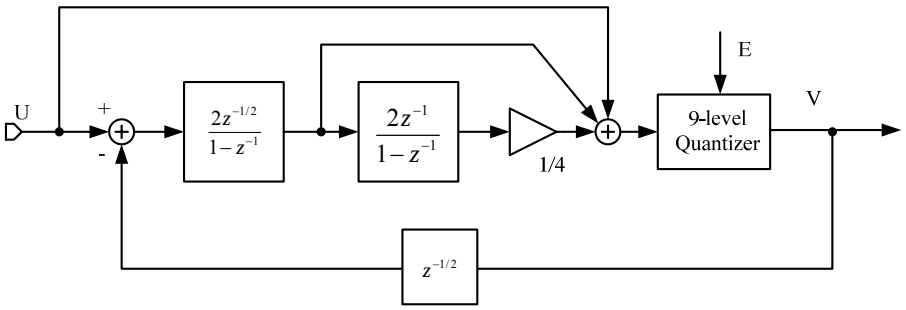

Figure 4.9 Proposed second order low-distortion ΔΣ modulator

Fig.4.9 shows the proposed low-distortion ΔΣ modulator topology which is able to adopt the modified CP based SC integrator as the very first integrator. A second order modulator is shown here for simplicity. Nevertheless, the concept hereby can be extended to arbitrary order of ΔΣ modulator. The key point here is to make the first integrator half-cycle delayed instead of one-cycle delayed. This modification restores the NTF of the ΔΣ modulator, which makes the modulator loop stable. Applying linear analysis, NTF of this particular second-order modulator is:

$$\frac{V(z)}{E(z)} = (1 - Z^{-1})^2 \qquad (4.4)$$

Strictly speaking, the proposed ΔΣ modulator topology is not able to achieve a perfect input signal cancellation at the input of the loop filter. So there is always a certain amount of signal energy entering the loop filter. Considering the over-sampling nature of a ΔΣ modulator, the difference of the input signal samples separated by a

half clock cycle will be very small even under moderate over-sampling ratio (such as 16 or lower). Therefore the signal content at the first integrator output remains very small. Signal content at the following integrator output will become larger due to the accumulation process of the SC integrator. Fortunately, the non-linearity appearing deep inside the loop filter will be noise shaped when referring it to the modulator input. In summary, the proposed modulator topology can still maintain most of the low-distortion property, while consuming less power compared to a similar low-distortion ΔΣ modulator employing conventional parasitic insensitive SC integrators.

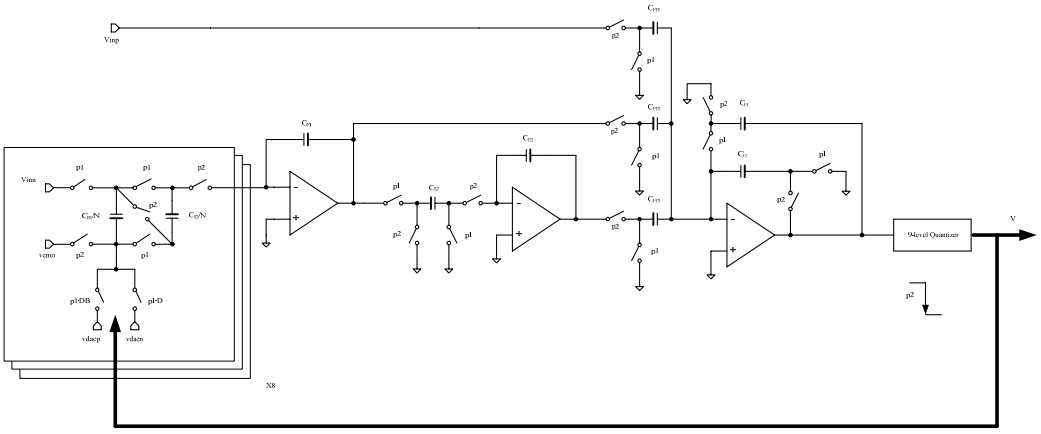

Figure 4.10 Switch level of the proposed second order low-distortion ΔΣ modulator

As a demonstration of the proposed topology, a feed-forward second order ΔΣ modulator with modified CP based SC integrator as the first integrator was designed. Its switch level diagram is shown in Fig.4.10 in a single-end configuration for simplicity. Note that the cross coupling technique mentioned above can be applied to the fully differential implementation. Opamps here were represented by macro models with finite DC gain (50 dB). The dynamic behavior of the proposed ΔΣ modulator was

simulated in Cadence Spectre simulator. The output digital bits were sampled and processed in MATLAB.

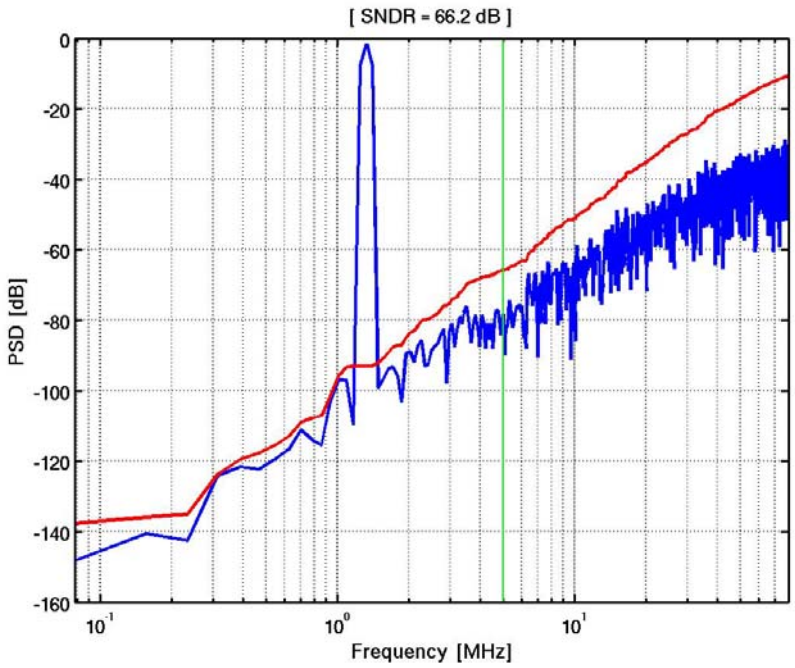

Figure 4.11 Simulated PSD of a ΔΣ modulator with modified CP based SC integrator

In the simulation, we assume a 5 MHz signal bandwidth, an input signal at 1.328125 MHz, an oversampling ratio of 16, and a 9-level internal quantizer. Fig. 4.11 shows the simulated output spectrum of the proposed second-order low-distortion ΔΣ modulator with a -1.6 dBFS input signal. The simulated SQNR was 66.2 dB which does not include thermal noise and other circuit non-ideal effects.

In order to verify the low-distortion property of the proposed ΔΣ modulator topology, the first integrator output was also sampled and converted into the frequency domain, as shown in Fig.4.12. It can be seen that the input signal power is 54 dB

below full scale which suggests the opamp involved in the first integrator only needs to process a very small input signal. This clearly implied that the low-distortion property is retained in the proposed ΔΣ modulator topology.

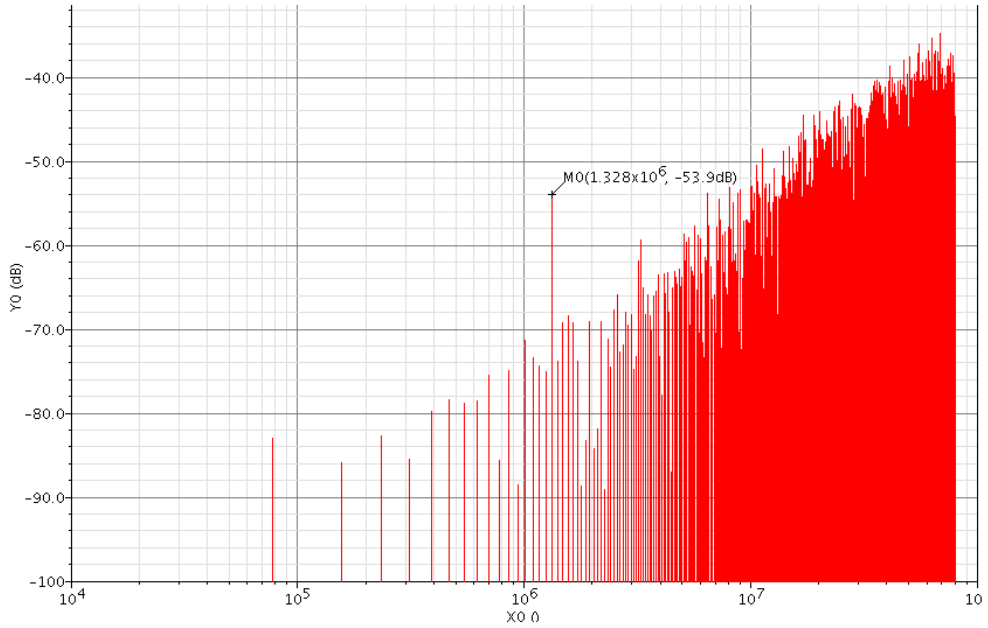

Figure 4.12 Simulated PSD of the first integrator output in the proposed ΔΣ modulator

4.5. Summary

A cross-coupling technique is proposed to eliminate parasitic capacitor effect in a CP based SC integrator. A new ΔΣ modulator topology is proposed to effectively employ the modified CP base SC integrator in a low-distortion configuration. A second order ΔΣ modulator with the proposed technique was designed and simulated to verify the effectiveness. The low power feature at both architecture level and transistor level makes it a good candidate for broadband, high linearity and low power applications.

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CHAPTER 5. DESIGN OF A LOW POWER DOUBLE-SAMPLED ΔΣ MODULATOR

The next two chapters will describe the design details of a low power broadband ΔΣ modulator. We will follow the widely adopted top-down design procedure: from system level design to transistor level design. Chapter 6 will cover some layout techniques in advanced deep sub-micron CMOS process and present the measurement results.

5.1. ΔΣ Modulator Specification

The rapid growth in both wired and wireless communication systems, high definition television (HDTV) and medical imaging has stimulated the development of data conversion interfaces that can be integrated in standard CMOS technologies while meeting stringent resolution and linearity requirements with increasing signal bandwidth. These converters should also be realized without any special analog option to offer low cost when they are integrated with large digital systems on a single die. Recently, communication standards show a trend toward increasing signal bandwidth. For example signal bandwidth is 10 MHz for IEEE 802.11a wireless LAN and 20/40 MHz for IEEE 802.11n [1]. It is believed that even higher bandwidth is required in the near future.

As discussed in chapter 1, ΔΣ ADCs have become a very popular architecture choice to realize a wide bandwidth low power data conversion in advanced deep sub-micron CMOS process. Fig.5.1 shows a basic diagram of a direct conversion wireless

receiver which employs a ΔΣ ADC. Fig.5.2 describes the relationship between the bandwidth and the dynamic range of the ADCs used in several popular wireless applications. A wideband ΔΣ ADC can be used in the WLAN applications to process a channel. In such cases, the relatively higher sampling frequency of a ΔΣ ADC is beneficiary for the whole receiver design since the specifications of the preceding baseband filter can be quite relaxed. In most existing solutions, the SNR of such a wideband ΔΣ ADC is around 60 dB. Raising the SNR specification helps lower the noise requirement of other building blocks inside the receiver before the ADC, but the ADC should be able to maintain reasonable power consumption.

On the other hand, a wideband ΔΣ ADC can also be incorporated in a cellular or Bluetooth receiver. Now the ADC can process the entire communication band. This leads to a great simplification of the receiver architecture, since now all the channel filtering could be moved into the digital domain.

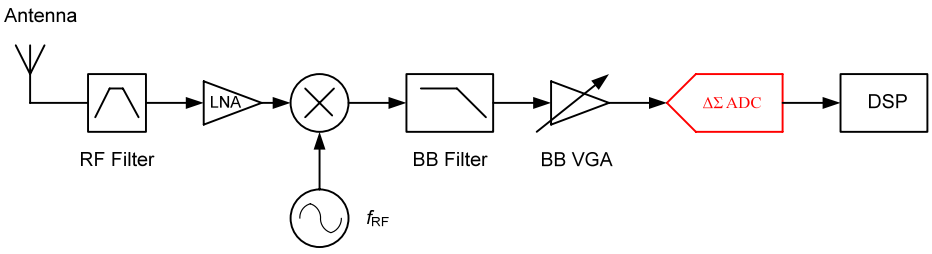

Figure 5.1 Basic diagram of a direct conversion wireless receiver

Ultimately, a wideband and high resolution ADC can be placed right after the antenna and the low noise amplifier to form a true software defined radio. However such a solution is not justified at the power consumption with the existing CMOS process and circuit design techniques at this time. The main specifications of the ΔΣ

ADC in this thesis is trying to accommodate the current wideband applications while surpassing the overall performance compared to the prior art design in terms of signal bandwidth, SNR and power consumption. Meanwhile this ADC is implemented in a standard digital CMOS process without any special analog option to offer low cost.

The target of the designed ΔΣ ADC is to achieve 12-bit resolution within a 20 MHz signal bandwidth and a 20 mW power consumption. This research only includes the ΔΣ modulator design. Interesting readers may refer to the literature regarding the design of a decimation filter [2].

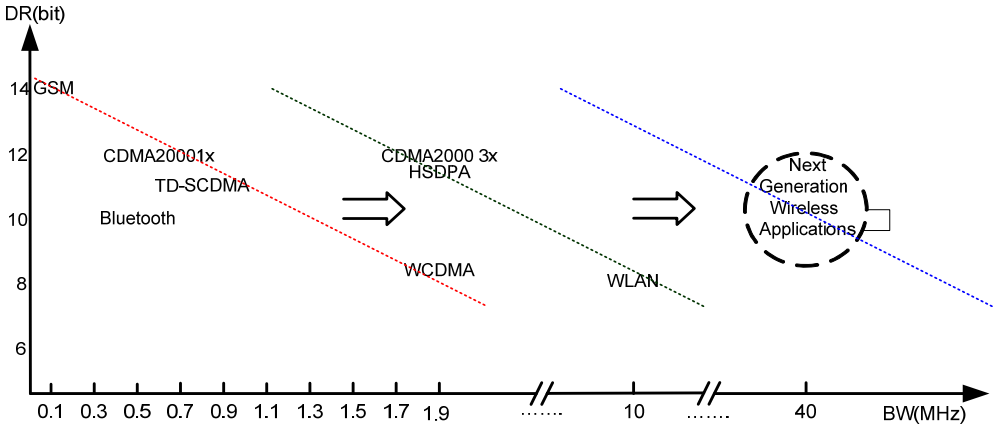

Figure 5.2 Bandwidth requirements of ADCs in some wireless applications

5.2. ΔΣ Modulator Architecture

There are two possible realizations of a delta-sigma modulator. One is based on discrete-time (DT) switched capacitor (SC) circuitry which traditionally was used to achieve very high resolution within a low signal bandwidth. The other one employs continuous-time (CT) circuitry. Due to the exponential settling nature of its internal

integrators, the maximum sampling frequency of a DT ΔΣ modulator is lower than its CT counterparts, especially when low power consumption is required. As a consequence, most of the recent ΔΣ ADCs incorporate CT modulators when the signal bandwidth goes beyond 10 MHz or more [3] [4]. However, compared to CT modulators, DT modulators do offer several advantages: 1. the performance is less sensitive to clock jitter; 2. the signal transfer function (STF) and the noise transfer function (NTF) rely on capacitor matching, which can be made very accurate in modern CMOS technology; 3. it is easy to scale the sampling frequency, which makes multi-standard applications possible; 4. the design methodology for a DT modulator is well established. As a matter of fact, some published DT wideband ΔΣ modulators show even better overall performance than CT ΔΣ modulators [5] [6] which clearly demonstrate the potential ability of a DT ΔΣ modulator to achieve wide bandwidth and high resolution simultaneously. Our design is also based on DT ΔΣ modulator architecture, and various efforts are made to take the overall performance to a new level.

The theoretical SQNR (Signal-to-Quantization noise ratio) of a ΔΣ modulator can be expressed as:

$$SQNR = 10\log[\frac{3}{2}(\frac{2L+1}{\pi^{2L}})R^{2L+1}] + 20\log(2^N - 1) \qquad (5.1)$$

where L is the order of a ΔΣ modulator, R is the over-sampling ratio and N is the number of bits of the internal quantizer. Various trade-offs should be investigated among the three parameters. Our investigation starts from the sampling rate of the ΔΣ

modulator. In a switched-capacitor circuit, the sampling rate directly determines the speed requirement of the constituent sub-blocks such as bandwidth and slew rate of an opamp, comparator speed as well as the speed of the distributed clock generators and buffers. Since the power consumption of these sub-blocks is highly correlated with speed, a reasonable modulator sampling rate should be chosen to make low power possible. In this particular 90 nm CMOS process, the initial circuit analysis shows that the modulator sampling rate must be no more than 320 MHz. The corollary of this practical constraint is that the oversampling ratio of the designed ΔΣ modulator attempting to achieve a 20-MHz effective signal bandwidth will be limited to eight, which is fairly low. This has important consequences for the choice of the ΔΣ modulator architecture. However, even under such a low over-sampling ratio, we will show in the following that a high SQNR can still be achieved through careful design.

With high over-sampling ratio (>64) on hand, ΔΣ modulators with a single-bit quantizer can achieve very high SQNR. Also, the single-bit quantizer is very easy to design and is inherently linear. Under low over-sampling ratio, due to the insufficient noise-shaping, the SQNR of ΔΣ modulators using a single-bit quantizer will be very low. Clearly, the resolution of the modulator is limited by the number of the output bits per Nyquist sample [7], which is simply:

$$\text{Bits/Nyquist sample} = M \times N \tag{5.2}$$

where M is the oversampling ratio and N is the number of output bits for each input sample. From equation (5.2), it can be found that with a single-bit quantizer and the over-sampling ratio of 8, it is impossible to achieve more than 9 bits resolution. Based

on this conclusion, multi-bit quantizer is mandatory in the low over-sampling ratio application.

The multi-bit quantizer has the following advantages: first, the quantization noise is reduced when the number of quantizer level increases. Second, its transfer function becomes much less nonlinear compared to a single-bit quantizer. Finally, the reduced quantization noise allows the noise transfer function of a ΔΣ modulator to be more aggressive to further improve the SQNR [8].

With a multi-bit quantizer and feedback D/A converter in the modulator feedback loop, ΔΣ modulators can no longer enjoy the inherent linearity of a two-level feedback DAC. Fortunately, various dynamic element matching techniques, such as Individual Level Averaging (ILA) and Data Weighted Averaging (DWA) have been proposed to improve the linearity of the feedback DAC [9] [10]. In Chapter 3, a new DWA implementation is presented to reduce the hardware complexity. Actually, a large number of ΔΣ modulators with excellent signal to noise ratio utilizing multi-bit quantizer and dynamic element matching techniques have been reported [11] [12] [13].

As can be seen from equation (5.1), in a low OSR design even with a multi-bit quantizer, a high order loop filter is still necessary to suppress the in-band quantization noise. In a single loop topology, this can be realized by simply adding more integrators into the loop filter. The main advantage of the single loop topology is that the requirements for opamp gain and capacitor matching can be quite relaxed [14] [15]. However, ΔΣ modulators with loop filter order higher than two has the potential to become unstable when the input signal level approaches the full-scale voltage. As a

result, the maximum input signal amplitude has to be reduced in order to not destabilize the loop. Most of the time, the SNR of a ΔΣ modulator is thermal noise limited. Larger input sampling capacitor should be used to meet the thermal noise requirement with smaller input amplitude which also leads to large area and higher power consumption.

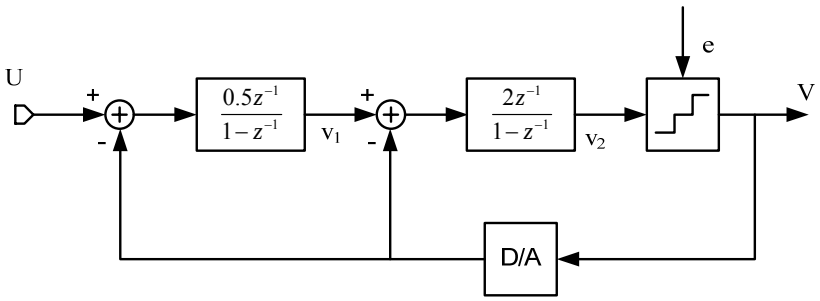

Figure 5.3 Block diagram of a conventional second order ΔΣ modulator

Unlike a single loop topology, high order noise shaping function can be realized by cascading low order loop filters. Using a low order loop filter (most likely first or second order) greatly improves the stability so that the maximum input amplitude can be increased to improve the SNR performance. What is more important in the cascaded structure is that when utilizing a multi-bit quantizer there can be an inter-stage gain between two adjacent stages. This inter-stage gain significantly improves the SQNR of the cascaded modulator. The theoretical SQNR for a cascaded modulator can be expressed as:

$$SQNR = 10\log[\frac{3}{2}(\frac{2L+1}{\pi^{2L}})R^{2L+1}] + 20\log(2^N - 1) + 20\log(A_1 A_2 \cdots A_n) \qquad (5.3)$$

For example: when two second order modulators are cascaded each using a 4-bit quantizer, then an inter-stage gain of 8 can be used resulting an 18dB SQNR improvement. This SQNR improvement is highly desirable in a low OSR design.

The SQNR improvement in the cascaded modulator is at the cost of increased number of comparators to be used in the quantizer, higher oapmp DC gain requirement and tighter capacitor mismatch tolerance in the first stage. In practical circuit design, capacitor mismatch in the first stage is not a very serious problem mainly because the capacitance there are always determined by the thermal noise which leads to a large capacitance, and hence its matching property can be guaranteed. It is quite surprising to see that the opamp DC gain requirement is not that stringent under the circumstance of a multi-bit quantizer. On the other hand, we shall see that the opamp DC gain requirement is fully determined by the modulator linearity issues rather than the quantization noise leakage. Solution to improve the linearity while reducing the opamp DC gain requirement will be addressed next.

One of the most popular ΔΣ modulator structures is cascaded integrator with distributed feed-back (Boser-Wooley structure) as shown in Fig.5.3 [16]. Although good for high OSR applications, it is pretty troublesome under wide-band low OSR implementations. The integrators inside the loop filter need to process the input signal as well as the quantization noise. Because of the nonlinear opamp gain and slew rate effects, harmonic components of the input signal will appear at the integrator output.

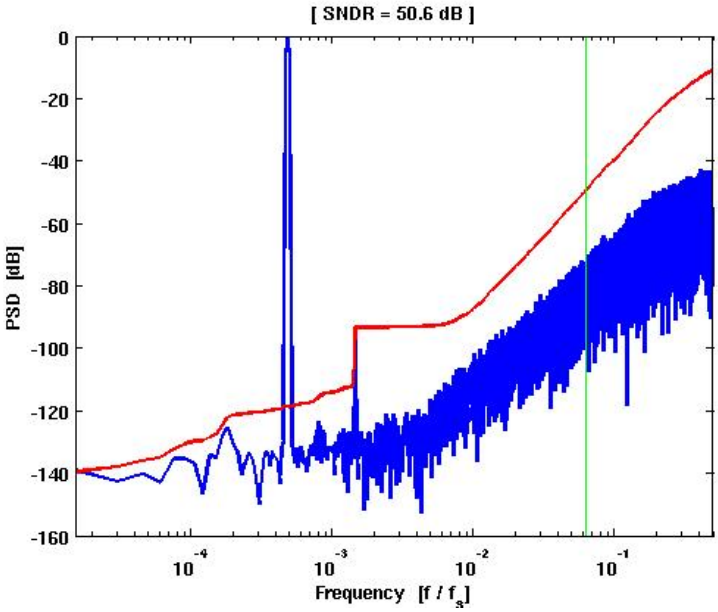

Figure 5.4 Output spectrum of a conventional second order ΔΣ modulator

Fig.5.4 shows the output spectrum of a conventional 2nd order ΔΣ modulator. During the simulation, the OSR is 8 and the opamps were modeled with a nonlinear 60dB gain. The third order harmonic is clearly visible. To eliminate this harmonic, high linearity opamps are needed, which are not only difficult to design but also power hungry in deep submicron CMOS technology.

In [17], a low-distortion ΔΣ modulator topology suitable for wide-band low OSR application was proposed. It is a fully feed-forward topology as shown in Fig.5.5. Analysis of the linear system leads to the conclusion that there is no signal component at the output of the integrator. So in other words, the integrators only need to process the quantization noise. Therefore the linearity requirements of the opamps are significantly relaxed.

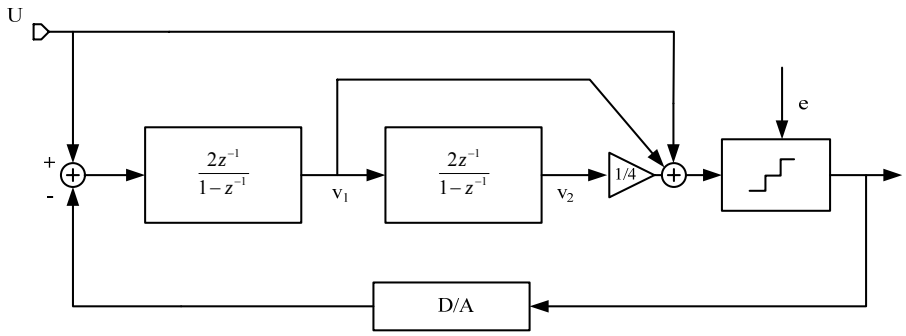

Figure 5.5 Block diagram of a low-distortion feed-forward second order ΔΣ modulator

There are several advantages for the low-distortion fully feed-forward topology:

The first one is the relaxed opamp requirements. This is very attractive in the deep-submicron CMOS technology where the transistors' intrinsic gain is very low. Fig.5.6 shows the output spectrum of a low-distortion fully feed-forward 2nd order ΔΣ modulator. The OSR is again 8 and the opamps were modeled with nonlinear 60 dB gain. No third order harmonics are visible. Besides, the opamp output swing is reduced so that more power efficient cascode OTAs could be used in the design. Finally, the reduced output swing makes the opamp settling mostly dominated by linear settling rather than by the nonlinear slew rate limited region. The slew rate of the opamp can be relaxed as well. All the above three lead to great power consumption reduction, while maintaining the whole modulator performance.

The second advantage is the reduced circuit complexity and chip area. Low-distortion fully feed-forward topology only needs one feed-back DAC to stabilize the loop. When utilizing multi-bit quantizer under low OSR application, the circuit

complexity and the chip area are greatly reduced. The gain factor of the integrators in the low-distortion fully feed-forward topology is larger than distributed feed-back topology due to the reduced opamp output swing. When the sampling capacitances are mainly determined by the thermal noise, the feed-back capacitor can then be reduced to save chip area as well

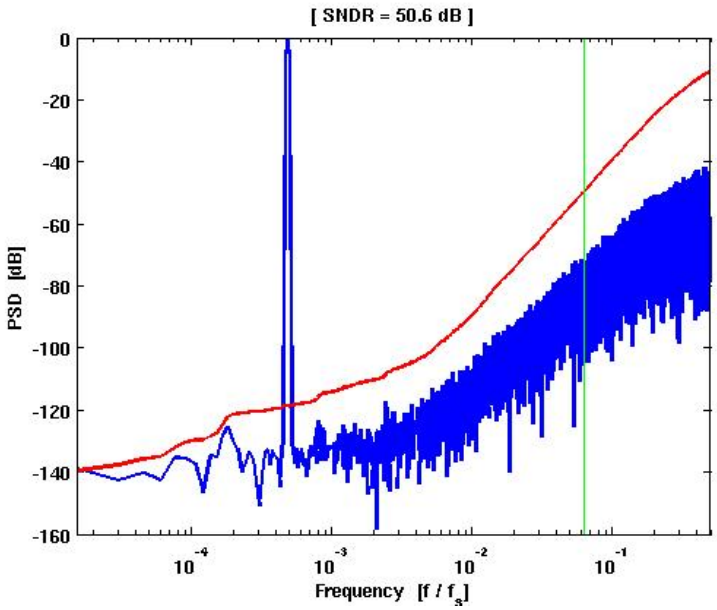

Figure 5.6 Output spectrum of a low-distortion feed-forward second order ΔΣ modulator

Finally, low-distortion fully feed-forward topology offers simplified cascaded architecture [18]. A subtraction operation is necessary in the conventional feed-back topology to let the next stage process the quantization noise generated by the previous stage. However, in Fig.5.5, the output of the second integrator is already a delayed version of the quantization noise. As a result it can be directly connected to the next stage.

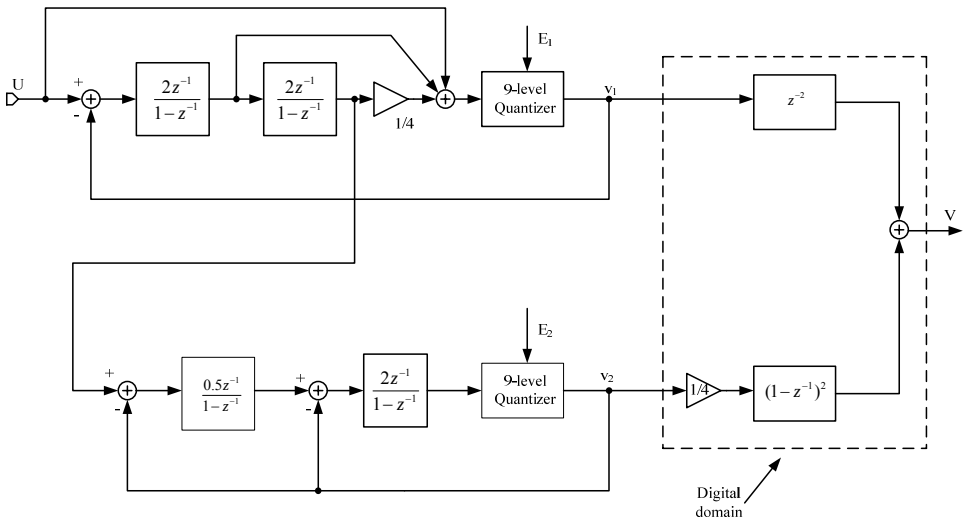

Figure 5.7 Block diagram of 2+2 cascaded modulator

The modulator architecture chosen in this design is shown in Fig.5.7. It is a 2+2 cascaded modulator with a 3-bit internal quantizer for both stages. At the first stage of the modulator, a low-distortion topology [17] is adopted to achieve high linearity while relaxing the opamp design. Since the second stage of the modulator only process the first stage quantization noise, a conventional feedback topology is used. By choosing the feedback topology, only two opamps are needed in the second stage.

Dynamic range scaling is always performed in the switched capacitor circuits to maximize the signal-to-noise ratio at every internal node. In this modulator, dynamic range scaling is performed not only for maximizing the internal node SNR, but also to simplify the circuit realization. Note that with the coefficients in the first stage shown in Fig.5.7, the output at the second integrator is exactly four times the quantization noise which can be directly fed to the second stage without any inter-stage

amplification. Therefore the sampling capacitor and the feedback capacitor of the first integrator in the second stage have the same value and can be shared. This leads to a larger feedback factor for the opamp closed loop configuration; as a result, some power can be saved.

If all the building blocks in the modulator are ideal, the output SQNR after the digital noise cancellation is 82 dB. This SQNR is almost 12 dB higher than the targeted SNR which means the quantization noise only contributes a very small portion to the overall SNR. This kind of noise allocation greatly relaxes the circuit design.

5.3. Transistor Level Design

Transistor level design of this low power broadband ΔΣ modulator will be presented in the following section.

5.3.1. Double Sampling Technique

Further power saving can be achieved by adopting double-sampling technique [19] which is able to effectively boost the over-sampling ratio of an SC ΔΣ modulator without extra requirements on the operational amplifier's settling time. By using double sampling technique, an effective OSR equals to 8 can be achieved with only 160 MHz sampling frequency in this particular design. If the modulator in our design is clocked directly at 160 MHz, the SQNR will lose as much as 27 dB.

Besides the benefit of a lot higher SQNR in the system level design, double sampling also helps to ease the design of the opamps inside the modulator [20], especially when two-stage opamps are used to maximize the output swing. By using

double sampling, the opamp closed-loop configuration remains the same during both clock phases, which greatly eases the opamp compensation.

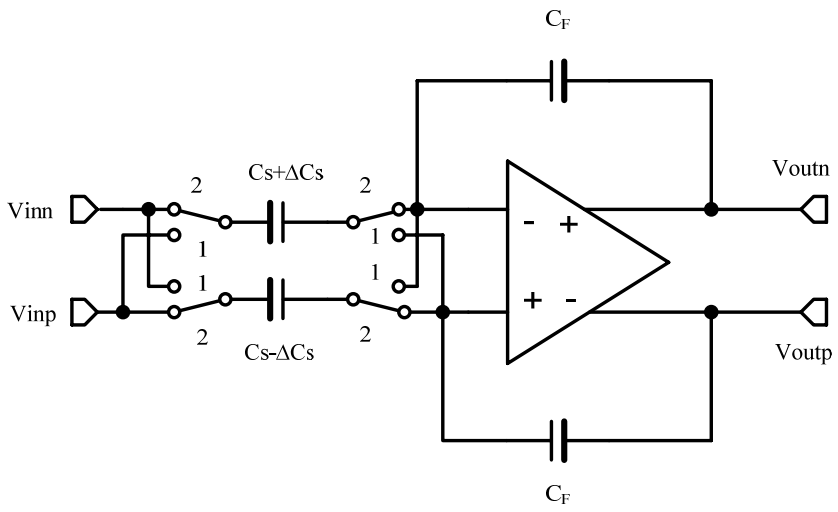

Figure 5.8 Fully floating switched capacitor integrator

If the double sampled integrator is to be realized in such a straightforward way that one of the two sampling capacitors is sampling the input signal while the other one is transferring charge to the integrating capacitor, any mismatches between these capacitors will cause a modulation by a frequency of Fs/2. For the input signal, because of the preceding anti-aliasing filter, the signal power at Fs/2 is greatly attenuated so this aliasing effect is of little effect. Even though there will be some input signals modulated to the frequency band around Fs/2, they will finally be filtered out by the decimation filter. Unlike the signal modulation just described, the feedback DAC output has a large high-frequency quantization noise power. If this noise power is mixed down to the baseband, the SNR of the ADC will be severely degraded.

There are several ways to solve this problem, such as additive error switching[21], individual level averaging[22], data weighted averaging[10], or through system level design to modify the noise transfer function of the modulator[23]. These designs will require more hardware, and they tend to be quite complicated. Another well-known solution to combat this noise folding back is to use a fully floating switched capacitor integrator [19] shown in Fig.5.8. Two capacitors are switched between the positive and the negative opamp input terminals from one phase to the other. The transfer function of the fully floating integrator is given by:

$$\frac{Vout}{Vin}(z) = (\frac{Cs}{Cf})\frac{1+z^{+1}}{1-z^{-1}} \tag{5.4}$$

As can be seen from equation (5.4), the differential output of this kind of integrator only depends on the mean value of the two capacitances. Therefore quantization noise will not fold back to the baseband. Even though it is a very simple and effective solution, there exists a potential problem from the transfer function of this integrator. Actually there is an extra $(1+z^{-1})$ and in the linear modeling of the loop transfer function this term should also be included. In fact, this extra $(1+z^{-1})$ term may cause instability in the modulator. In order to make sure the loop is stable, each integrator gain coefficient should be carefully chosen.

Usually, doing this will lose some of the SQNR improvement obtained by using double sampling. On the other hand, in a very low over-sampling ratio ΔΣ modulator, such as when the OSR is only 8, low distortion topology is highly desirable. Due to this extra $(1+z^{-1})$ term, it is now impossible to achieve a unity gain signal transfer

function. Therefore the integrators inside the loop filter need to process the input signal as well as the quantization noise. Because of the nonlinear opamp gain and slew rate effects, harmonic components of the input signal will appear at the integrator output. Thus, highly linear opamps should be designed to reduce the distortion level.

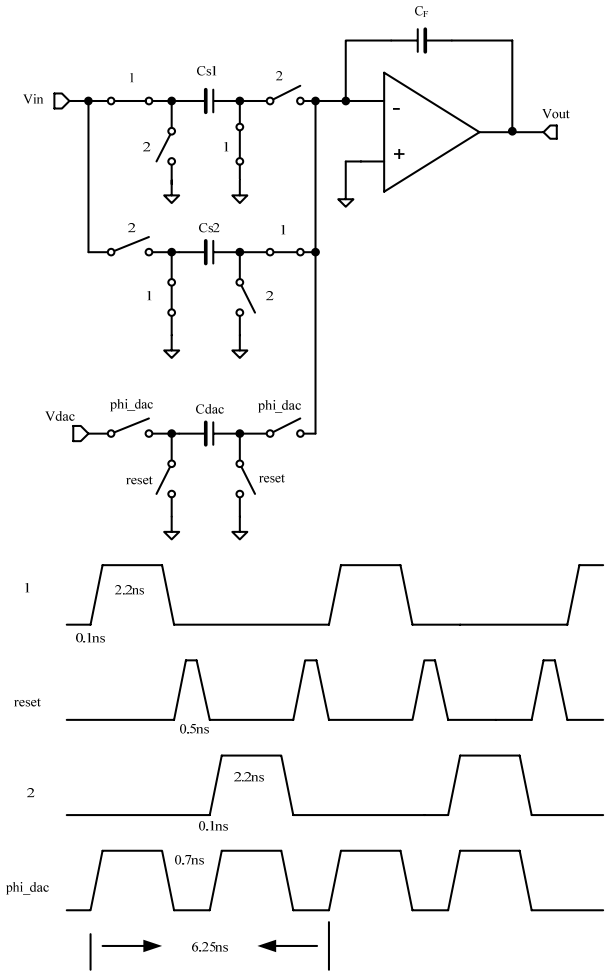

Figure 5.9 Double sampled integrator using capacitor reset

To overcome the disadvantages of the fully floating feedback DAC, a capacitor reset technique is used in this design as shown in Fig.5.9. The idea of this

configuration comes from the observation that if only one capacitor is to be used in the feedback DAC, then there will be no quantization noise folding back. In this configuration, only one capacitor is performing as a feedback DAC during both clock phases. Both terminals of the capacitor are reset to the common mode voltage during the non-overlapping time.

This capacitor reset technique is very simple. The only hardware change needed to realize its implementation is some minor changes in the clock circuitry to generate a short pulse. This short pulse is not very difficult to generate in 90 nm CMOS.

The width of this short pulse should be chosen carefully. During the reset phase, the capacitor associated with two reset switches form a first order RC low pass filter. How close could the capacitor be reset to the desired the common mode voltage depends not only on the RC time constant, but also on the pulse width. If the pulse width is too short, then the RC time constant needs to be very small. This means that for a constant capacitance, the switch on resistance must be small, which leads to a large transistor. As a result, the clock buffer to drive these switches will consume more power. If the pulse width is too wide, then the available time for the integrator to perform integration is reduced. Under this circumstance, the opamp power consumption must be increased to settle faster. Another important advantage to make the non-overlapping time longer is that it gives more time to the feedback Data Weighted Averaging logic to perform data rotation. Also considering the clock rising and falling time, the available time for the opamp to settle is around 2.2 ns. The opamp power consumption may be increased a little but the ability to double sampling the input

signal makes this solution still justified. In our design, considering all the fore-mentioned aspects, the reset pulse width is set to about 0.5 ns.

Unlike in a fully floating switched capacitor DAC, there is no extra $(1+z^{-1})$ term in the DAC transfer function, so that we still have a unity gain signal transfer function. Low distortion topology can still be used in our design which will result in good linearity of the whole modulator.

Applying a low distortion topology in a double sampled ΔΣ modulator offer other advantages than the ones previous mentioned. First of all, low distortion topology has only one feedback DAC. The capacitor reset technique need only be applied to the DAC at the modulator input. Second, for the cascaded architecture, the quantization noise of the first stage can be directly extracted from the output of the second integrator, thereby eliminating another DAC needed to obtain the quantization noise. Since the second stage of the modulator only has to process the first stage quantization noise, nonlinearities in the second stage feedback DACs are high-order noise shaped. As a result, two time-interleaved capacitors are used to simplify the circuit implementation [24]. Sampling and feedback DAC capacitors are shared in the second stage to save power consumption. Again, since the second stage only has to process the quantization noise, no signal-dependent charge will flow inside or outside the reference buffer.

5.3.2. Operational Amplifiers

An important phenomenon in a cascaded modulator is quantization noise leakage from the first stage to the final output, due to the mismatch between the analog loop

filter and the digital noise cancellation filter. The transfer function of a typical SC integrator can deviate from its ideal case mainly by the following three reasons: capacitor mismatch, finite opamp bandwidth and finite DC gain. In a modern deep sub-micron CMOS technology, 90nm or below, capacitors can be matched very well. Besides, the increased cut-off frequency of the MOS transistors makes it easy for an opamp to achieve wider bandwidth for a given load capacitor. However, the output impedance of the deep submicron transistors is very low; therefore an intrinsic gain of a single MOS transistor is typically lower than 20 dB. In this modulator design, MATLAB behavioral simulations show that the gain of the opamp for the first and second integrator in the first stage should be at least 60 dB to make the quantization noise leakage negligible compared to the thermal noise. Considering the process, temperature and supply voltage variations, a DC gain of at least 70 dB under nominal conditions is required. The DC gain of a conventional two-stage opamp with first stage folded cascode and a common source second stage is around 60 dB in this particular 90 nm CMOS, if nearly minimum channel length transistors are used to maximize the opamp bandwidth. In [25], a double gain boosting folded cascode opamp was designed in 0.13 um CMOS to achieve an 80 dB DC gain. This design is not only complicated but also the gain boosting auxiliary opamps will consume significant power since their bandwidths should be several times higher than that of the main opamp to avoid a slow transient[26].

Instead of using high-gain opamps to make the integrator transfer function as ideal as possible, digital adaptive calibration algorithm can be used in the design of a

cascaded modulator [27]. This algorithm is very useful but a drawback is it requires additional digital circuitry. The design overhead for the digital circuitry in 90nm CMOS is very small. But it increases the total time for the design.

Our design incorporates a two-stage opamp shown in Fig.5.10. It has the following design features: first, using PMOS input transistors to lower the input common mode voltage. A lower input common mode voltage allows the use of small NMOS switches to reduce the clock buffer loadings and less charge injection and clock feed-through. Second, a common source output stage is used to maximize the output swing under 1.2 V supply. Finally the opamp DC gain is boosted by using a current mirror OTA at the first stage. The mirror ratio increases both DC gain and AC bandwidth. For stability concerns, this mirror ratio can not be too large [28].

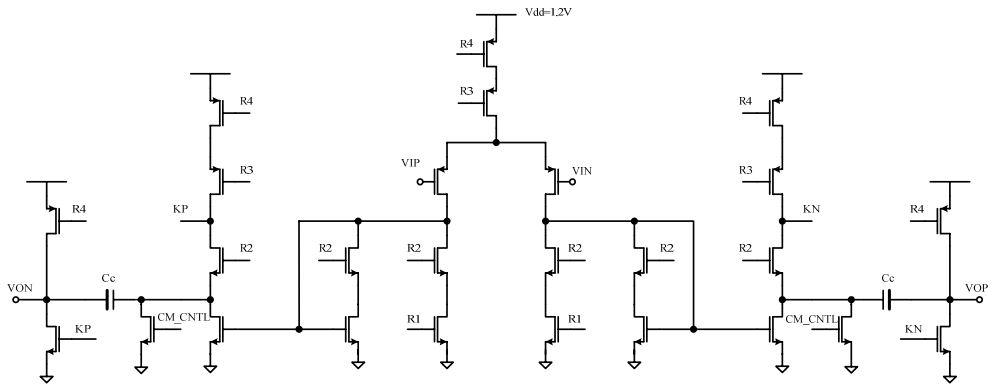

Figure 5.10 Schematic of the two-stage opamp

Since the opamp uses a common source output stage, continuous-time common-mode feedback circuitry is used to stabilize the output common mode voltage.

For the first opamp, during the integration phase, when the effective sampling capacitor is 1.6 pF, the feedback capacitor is 0.4 pF and the loading capacitor is 0.4 pF, the opamp has a nominal DC gain of 70 dB, a loop bandwidth of 500 MHz and loop phase margin of 63 degree while consuming only 5 mW under 1.2 V, including bias circuitry and common-mode feedback. The second opamp power consumption is 3 mW.

MATLAB behavioral simulations also show that the gain for the first and second opamp in the second stage and the active adder should be at least 50 dB. Considering the process, temperature and supply voltage variations, a DC gain of at least 60 dB under nominal condition is required. Similar but scaled opamps are used for these integrators and adders in our design. Power consumption for the first and second opamp in the second stage and the active adder are 1.5 mW, 1.5 mW and 2 mW, respectively.

5.3.3. Switch Design

Simple transmission gates are used for sampling switches in the integrator when the switch common-mode voltage is around the mid of the supply voltage. The ratio between the NMOS and PMOS in the transmission gate should be designed very carefully. Their ratio needs to be selected appropriately to minimize the on-resistance over the entire input signal range. For our design, a ratio of 2/4 between the NMOS and PMOS sizes is used.

The switch sizes needs to be selected large enough to provide a small on-resistance to meet the sampling linearity. On the other hand, the switch size should be

designed small to reduce the charge injection and clock feed-through. Extensive simulations were done to optimize the switch sizes [29].

For switches in the integration phase, simple NMOS transistors are used. Proper sizing of these switches can establish a critical damping condition to minimize the opamp settling time [30].

5.3.4. Quantizer and DWA

The experimental ΔΣ modulator employs 9-level quantizer for both stages. Each quantizer consists of eight identical comparators. For a double-sampled ΔΣ modulator, a comparator should be able to update its output twice in every clock cycle. In a conventional design, the comparator is clocked at two times the modulator clock frequency. This solution is straightforward but requires a fast comparator pre-amplifier. Furthermore, it might be difficult to allocate time to perform pre-amplifier input offset cancellation. Therefore in order to achieve low offset, the input devices of the pre-amplifier have to be sized large, resulting a larger parasitic loading for the preceding integrator or summation circuit.

A time-interleaved comparator is proposed in this design, as shown in Fig.5.11. Two pre-amplifiers are working in a time-interleaved fashion. Input offset cancellation helps to reduce comparator offset without using large input devices. The regenerative latch only works during the non-overlapping period, and during the p1 and p2 phases the outputs of the comparator remain unchanged. The timing is very simple, and can be directly obtained from the global clock generator.

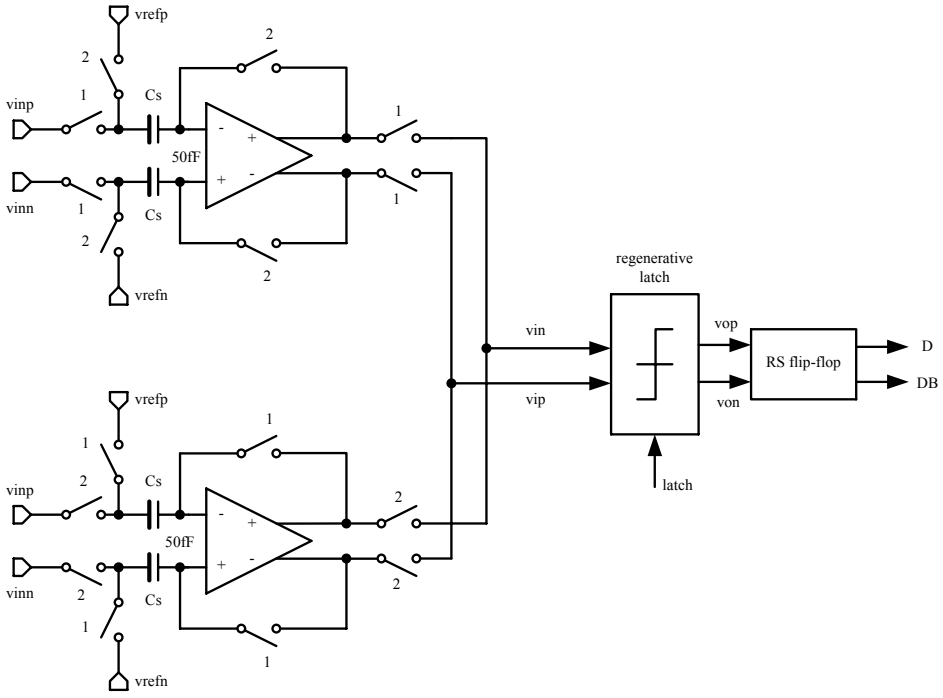

Figure 5.11 Block diagram of a comparator

Switches to sample the input signal and reference voltage are realized by transmission gates. PMOS switches are used in the feedback path and the paths connecting the pre-amplifier and the regenerative latch.

The pre-amplifier schematic is shown in Fig.5.12. It utilizes NMOS input devices with diode connected PMOS devices as load. As mentioned before, with the help of offset cancellation technique, the input devices do not have to be very large. However, in a feed-forward ΔΣ modulator, a fast comparator is necessary. So, a certain amount of bandwidth must be guaranteed over PVT variations.

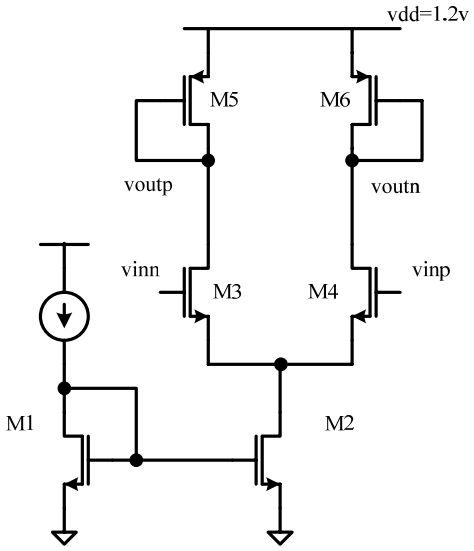

Figure 5.12 Schematic of a pre-amplifier

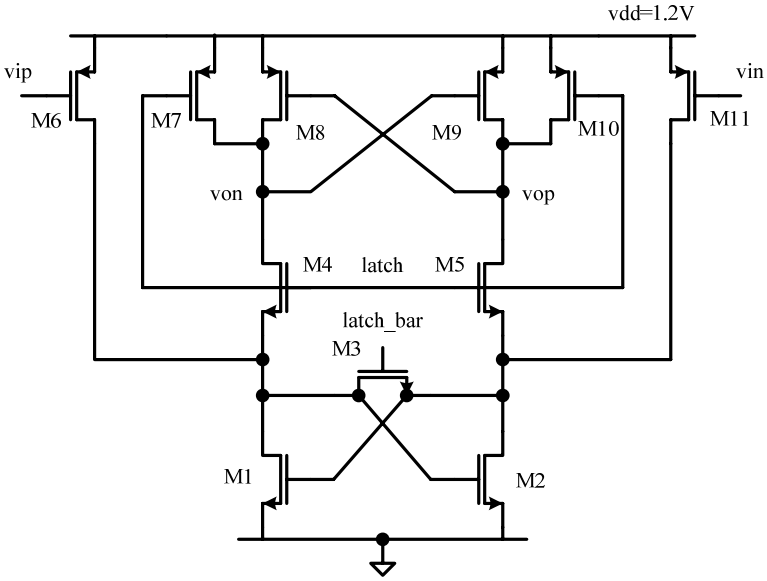

Figure 5.13 Schematic of the regeneration latch

A fast regeneration latch is shown in Fig.5.13 [30]. When latch_bar is high, the output of the pre-amplifier is converted into a current mode signal. The difference is

then established on the transistor M3. After latch_bar goes low and latch goes high, this voltage difference will be quickly amplified to logic levels by two positive cross-coupling pairs. An RS latch based on NAND gates is followed by the regenerative latch to keep the comparator's output stable during p1 and p2.

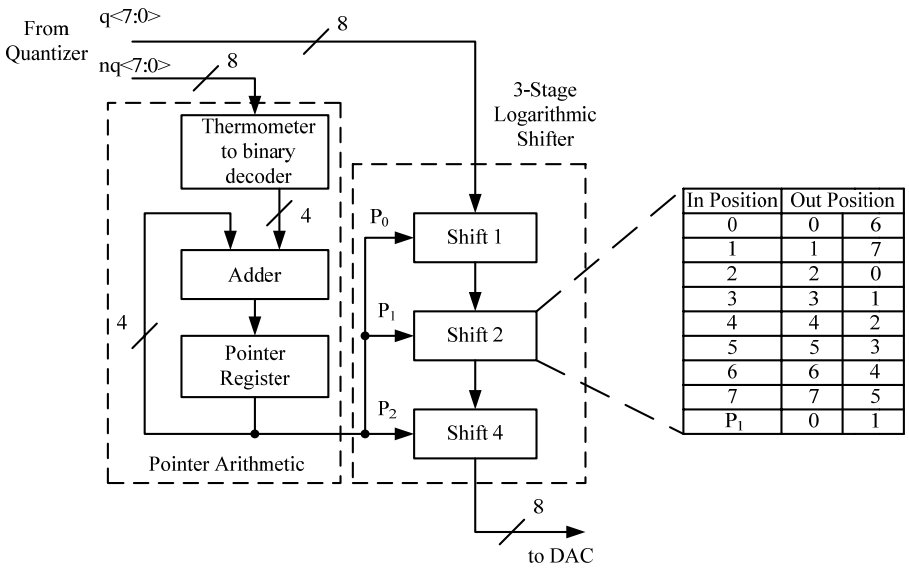

Figure 5.14 DWA implementation

Each comparator consumes 120 uA with a power supply of 1.2 V. Simple resistive divider is used to generate the reference voltages.

In order to shape the DAC unit element mismatch, DWA is adopted in this design due to its simplicity and effectiveness. A well-designed DWA implementation does not add any delay in the feedback path of a ΔΣ modulator. A conventional DWA implementation [31] was used because the new implementation proposed in Chapter 3 was not yet invented during the design.

Fig.5.14 shows the block diagram of the DWA implementation. A three-stage logarithmic shifter shuffled the input thermometer code. The thermometer to binary code converter is shown in Fig.5.15.

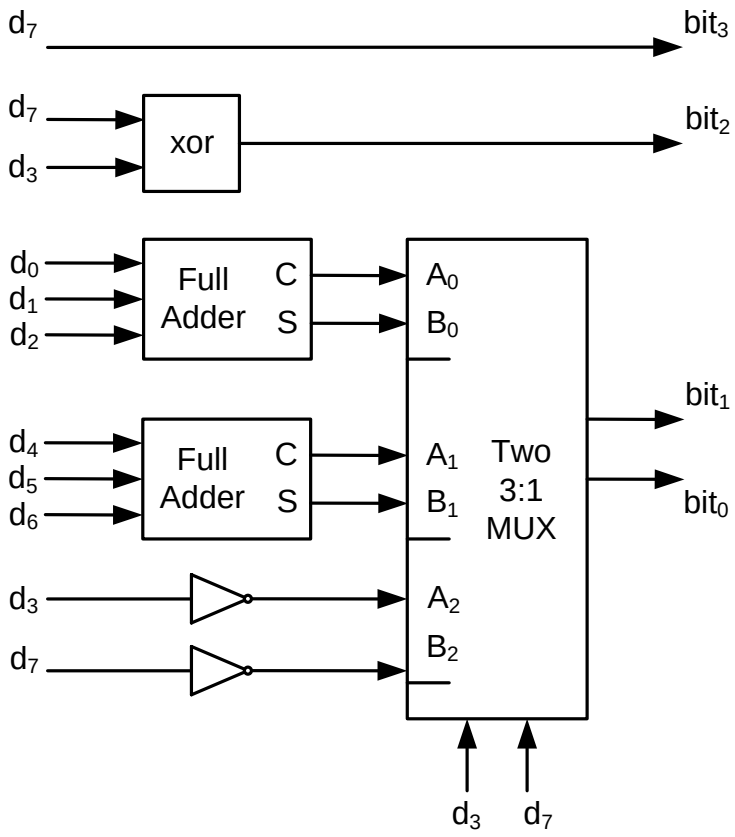

Figure 5.15 Thermometer to binary code converter

5.3.5. Clock Generator

The clock generator design is not trivial in this high-speed low-power SC ΔΣ modulator. Different clock signals have to be sent to various building blocks. In this design, a global clock generator shown in Fig.5.16 was used to generate 160 MHz

clock phases p1 and p2. To guarantee that their sampling edges are exactly 3.125 ns apart which is very critical in a double-sampled integrator, a 320 MHz off-chip clock signal is first divided by 2, using a D-type flip flop. A delay cell is inserted in the cross-coupling path to adjust the non-overlapping time between p1 and p2. The schematic of the delay cell is shown in Fig.5.17. The variable current source is realized by an on-chip 3-bit current DAC.

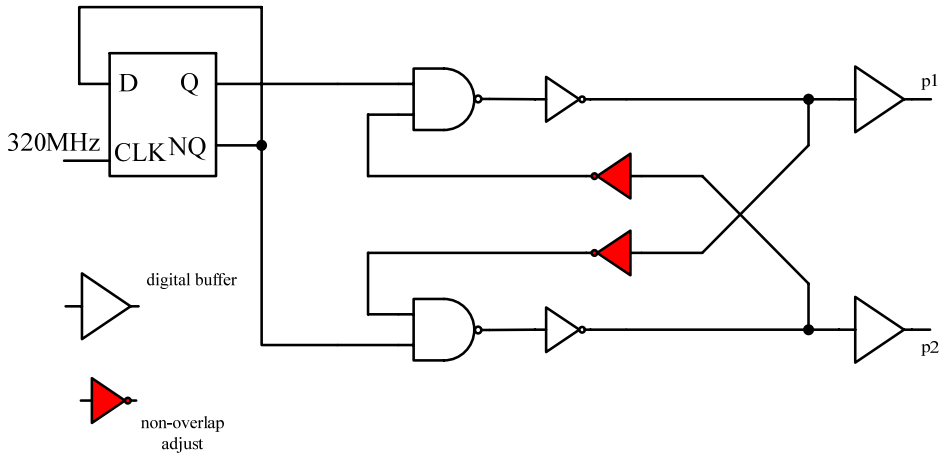

Figure 5.16 Global clock generator

All other clock signals, such as p1d, p1d_bar, p2d, p2d_bar, are generated and buffered locally. To reduce jitter sensitivity, all the local clock buffers are sized large to provide sufficiently fast rising and falling time over PVT variation.

5.3.6. Interface Circuit

The outputs of the two 9-level quantizers at the data rate of 320 MHz should be sent off-chip for modulator performance evaluation. The detailed interface circuit is shown in Fig.5.18. First of all, the 8-bit quantizer output thermometer code is converted to 4-

bit binary code using the same circuit already shown in Fig.5.15. Afterwards, the data rate of this 4-bit binary code is reduced to 160 MHz by means of a 1:2 DEMUX which consists of three D Flip-Flops clocked by two dedicated clocks p1 and p2. Finally 160 MHz rate data is buffered and sent off-chip.

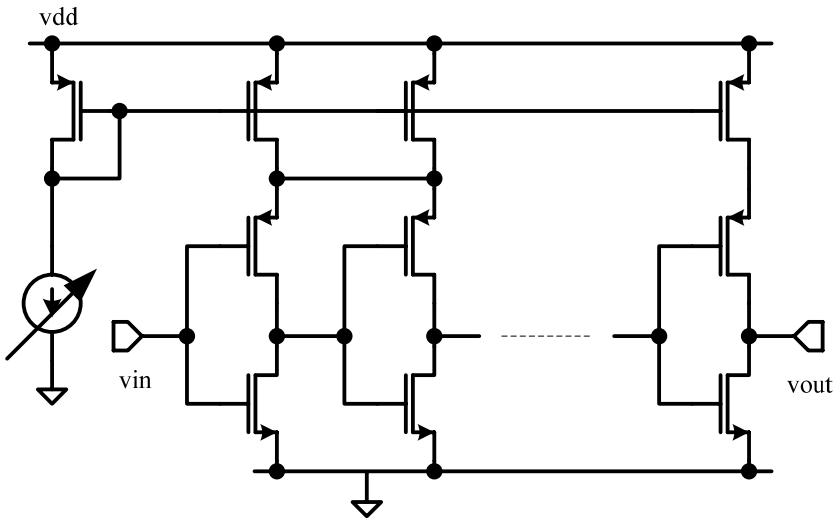

Figure 5.17 Delay cell in the global clock generator

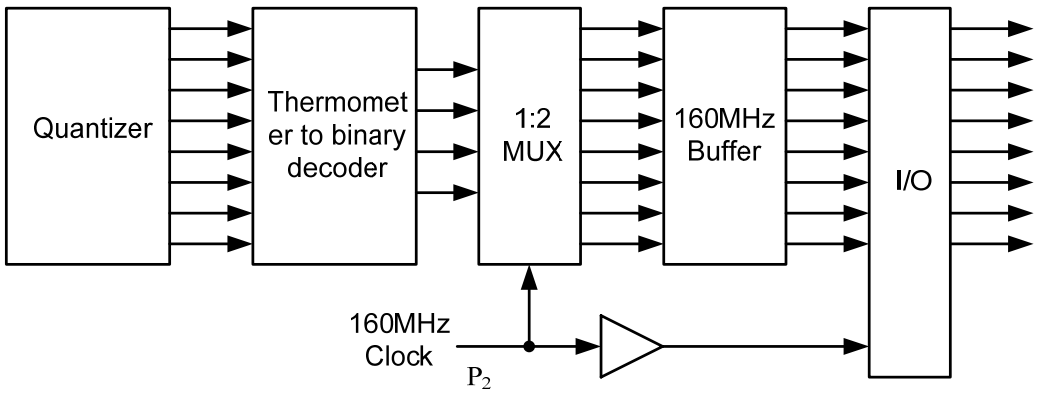

Figure 5.18 Block diagram of the interface circuit

5.4. Summary

The design of a 20 MHz signal bandwidth double-sampled DT ΔΣ modulator was described in this chapter. Strategies to achieve very low power consumption at both system and transistor level were presented. This modulator has been designed in a 90 nm digital CMOS process. Transistor level simulation shows that SNDR (actually without thermal nosie) is 76 dB within a 20 MHz signal bandwidth, while the power consumption is 19 mW with a 1.2 V supply voltage. Fig.19 shows the simulated output spectrum of the designed modulator.

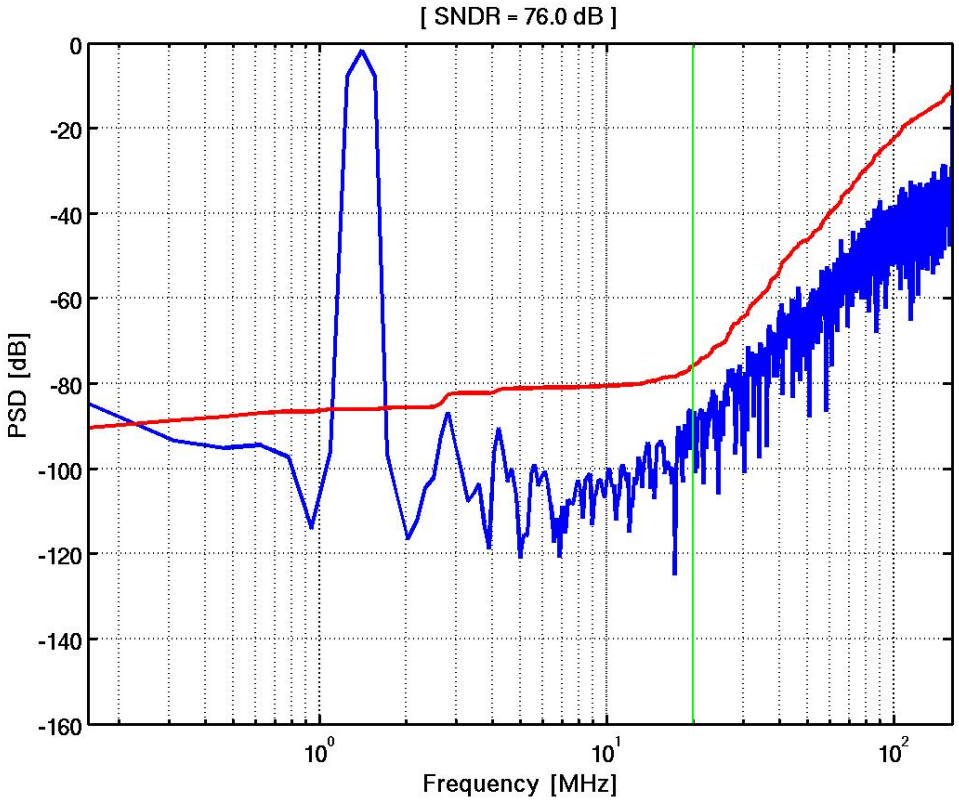

Figure 5.19 Simulated SNDR of the ΔΣ modulator

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CHAPTER 6. EXPERIMENTAL RESULTS

This chapter starts with physical design considerations in advanced deep sub-micron CMOS process and layout floor plan for this broadband low power ΔΣ modulator. Experimental results of the designed ΔΣ modulator are presented afterwards.

6.1. Layout Considerations

Advanced deep sub-micron CMOS processes pose great physical design challenges [1] [2]. There are several physical design concerns which did not exist in the previous generation technology. There are two common proximity effects, namely shallow trench isolation (STI) and well proximity effects. Designers must be aware of these phenomena to avoid catastrophic design failures.

Highly scaled bulk CMOS technologies make use of high energy implants to form the deep retrograde well profiles needed for latch-up protection and suppression of lateral punch-through [3]. During the implant process, atoms can scatter laterally from the edge of the photo resist mask and become embedded in the silicon surface in the vicinity of the well edge. The result is a well surface concentration that changes with lateral distance from the mask edge, over the range of l um or more. This lateral non-uniformity in well doping causes the MOSFET threshold voltages and other electrical characteristics to vary with the distance of the transistor to the well-edge. This phenomenon is commonly known as the well proximity effect (WPE).

For advanced CMOS technologies, the most prevalent isolation scheme is shallow trench isolation. The STI process leaves behind a silicon island that is in a non-uniform state of bi-axial compressive stress. STI induced stress has been shown to have an impact on device performance, introducing both Idsat and Vth offsets.

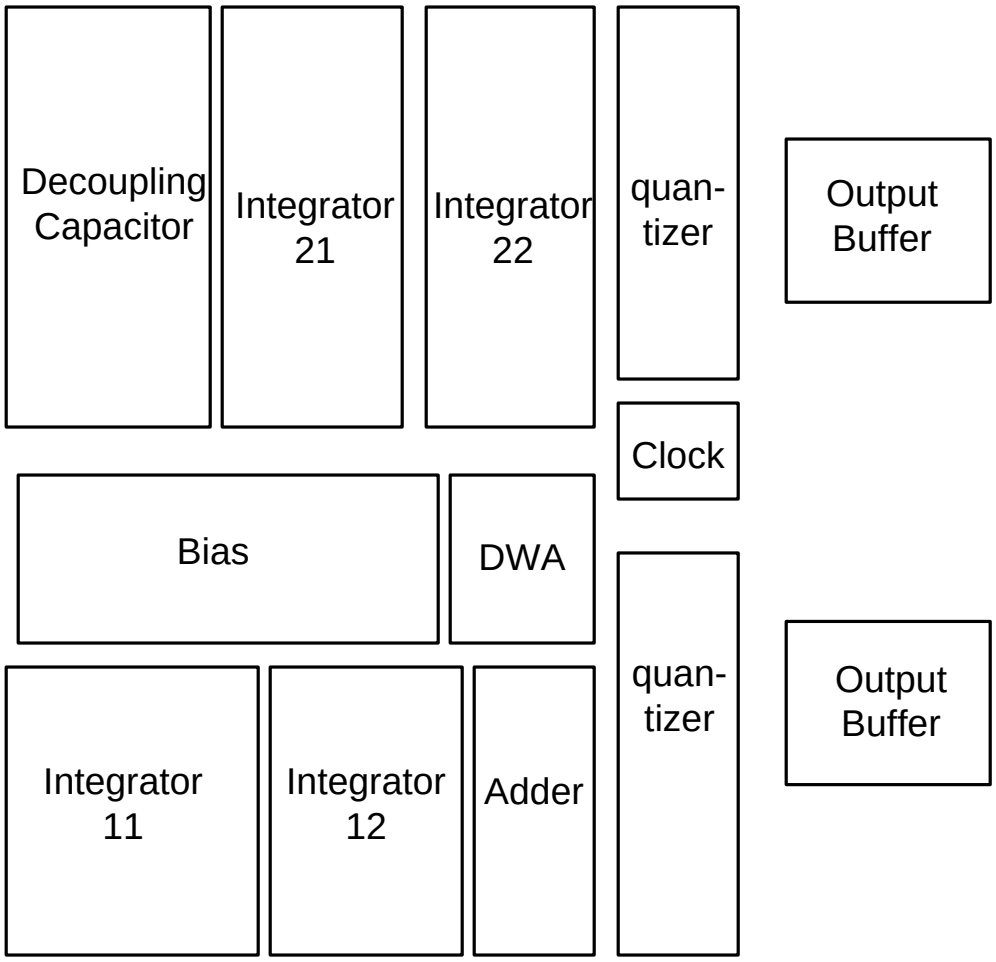

Figure 6.1 ΔΣ modulator floor plan

These effects are significant and must be included when modeling the performance of a transistor. The stress state within an active opening is both non-uniform and dependent on the overall size of the active opening, meaning that MOSFET

characteristics are once again a strong function of layout. STI under compressive stress affects the carrier mobility of nearby transistors by increasing the drain current of PMOS transistors and decreasing that of NMOS transistors. The effect of STI has been incorporated into existing SPICE models [4] to allow this phenomenon to be included in circuit simulations.

STI and well proximity effects affect analog design in advanced deep sub-micron CMOS process. Taking current mirror as an example, a pair of transistors having different STI and well proximity parameters suffers a systematic offset. This offset can be large if the difference is significant.

Surprisingly, STI and well proximity effects affect digital design as well. Standard digital cells having small transistors will encounter a great deal of proximity effects. Their post-layout electrical performance is far worse than that of in the pre-layout simulation. As a result, it is also essential to include these proximity effects even in the beginning of the digital circuit design.

Since most of our design is analog based, STI effects are mitigated by adding dummy devices in the transistor layout. Well proximity effect can be solved by either putting all the matching devices 3 um away from N-wells, or making their distances to N-wells equal. These methods are verified by post-layout simulations.

The layout of the ΔΣ modulator should be paid great attention to, since it is a mixed mode system. The key criterion of the modulator layout is to make it compact to reduce parasitic effect and interference. The ΔΣ modulator floor plan is shown in Fig.6.1. The first stage of the modulator was laid out at the bottom. The DWA is

placed at the left side of the quantizer to reduce the critical path delay. The second stage of the modulator was laid out at the upper side. Bias circuitries are sitting in the middle.

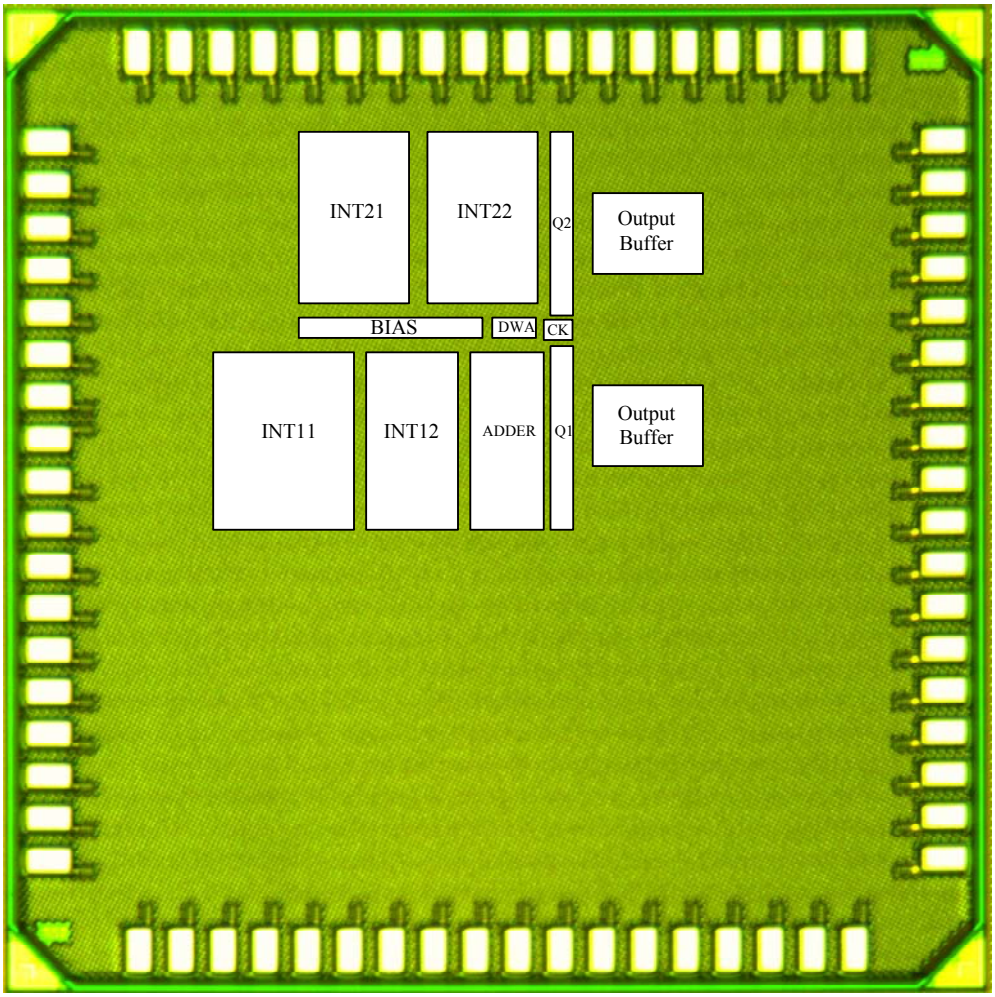

Figure 6.2 Die photo

To reduce digital switching noise coupling, separate digital and analog supplies are used. A dedicated power supply is used for the high speed output buffers, since they are driving a large loading capacitance. Metal lines for digital control signal

distribution are enclosed with metal shields, and sensitive analog nodes, such as the integrator opamp's virtual ground, are shielded to minimize undesired noise coupling. Empty layout spaces are filled with thick oxide MOS capacitors. The active area of the designed ΔΣ modulator, excluding output buffer, de-coupling capacitors and pads is approximately 0.5 mm^2.

The die micro photograph of the designed ΔΣ modulator is shown in Fig.6.2. The fabrication process is a 1P10M process. However, only six metal layers are utilized, and the dummy metal fills covered the rest of the four top metal layers. So the actual circuit is not visible from the die photo. The layout of the ΔΣ modulator is shown in Fig.6.3 in order to show details clearly.

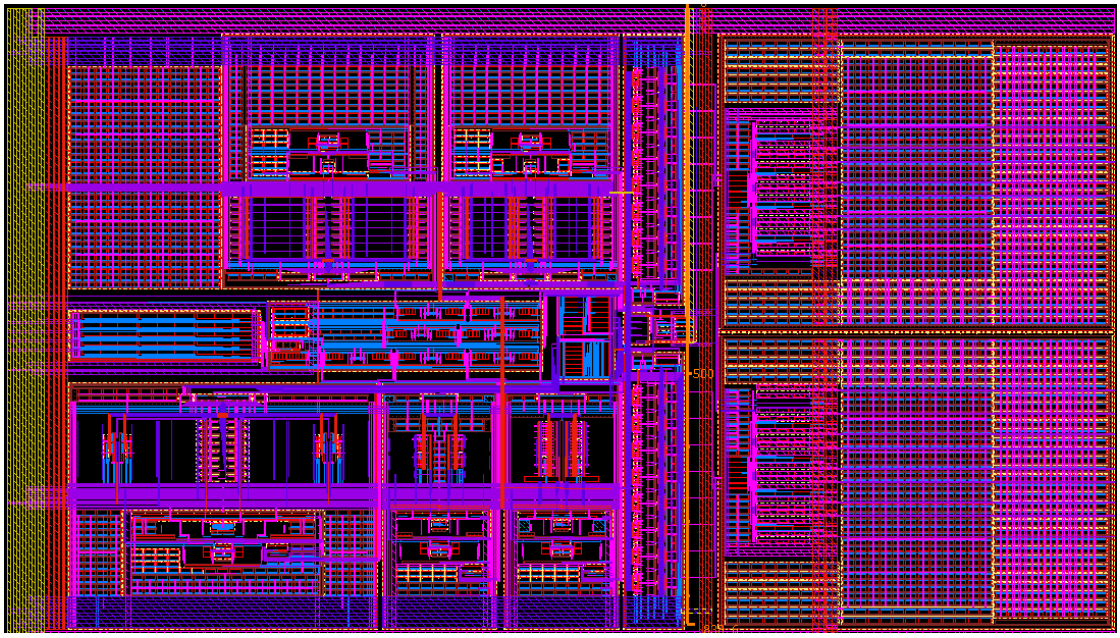

Figure 6.3 ΔΣ modulator layout

6.2. Test Set-up

To achieve the expected performance of the designed ΔΣ modulator, a good test board design is of utmost importance. A four-layer printed circuit board (PCB) was designed, which is shown in Fig.6.4. The top layer is mainly used to place the components and route signal traces. The second layer is the ground plane. The third layer is the power plane. Different power supply voltages can be distributed to various blocks in this layer. The bottom layer is used to place the rest of the components and to route the remaining signals.

While designing this test board, several criteria were applied to minimize the noise in the power supplies, the crosstalk between traces, and the parasitic capacitance and resistance. These are discussed next.

Every power supply is carefully decoupled by capacitors when they enter the test board. In addition, at each supply pin of the test chip, ceramic capacitors of 10 uF and 100uF are placed to decouple the high-frequency noise. All reference voltages are also generated by the regulators, which are buffered by high driving capacity commercial amplifiers. All power supplies are distributed evenly to the chip through the power planes. The power and ground pins are connected to the corresponding planes through the vias and wide traces which were made as short as possible to minimize the wire resistance. All differential signal traces are routed symmetrically. The distances between the signal traces are kept reasonably long to reduce crosstalk. The circuits which generate sensitive analog signals, e.g., the inputs of the modulator and the clock generator, are placed as close as possible to the test chip. The high frequency digital signal traces are also as short as possible to reduce electromagnetic interference (EMI).

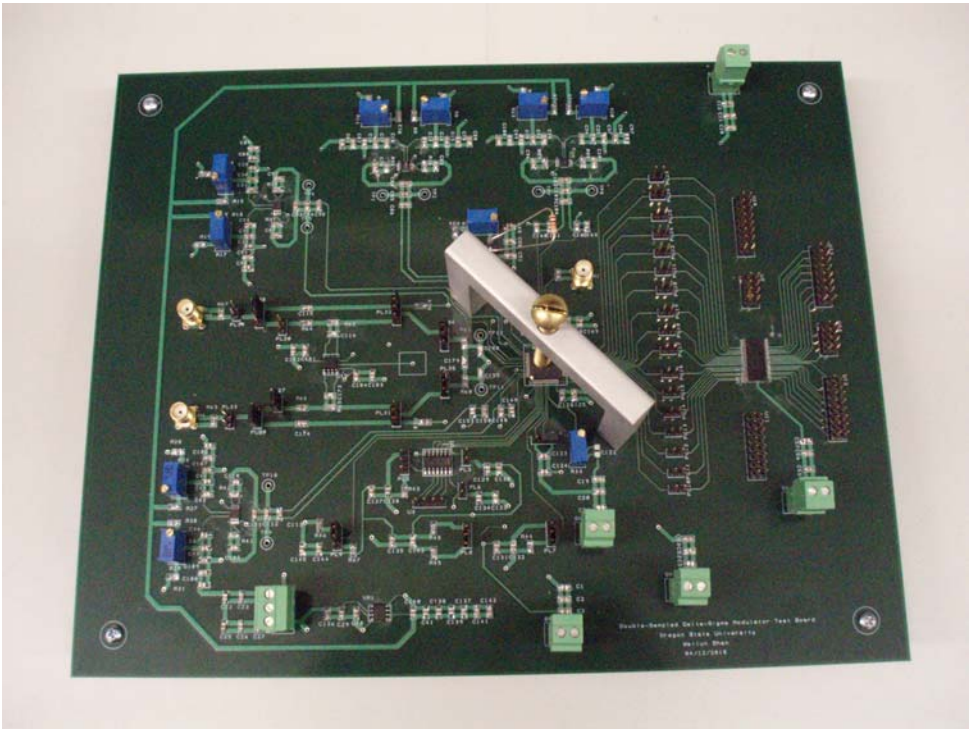

Figure 6.4 ΔΣ modulator test board

Fig.6.5 shows the test environment of the prototype chip. For the modulator input, two options are available. One is the low-frequency high-accuracy differential signal from the Audio Precision (AP), and the other is the high-frequency single-ended signal from the radio frequency (RF) signal generator. The latter one needs to be filtered by high performance passive band-pass filters and transformed into the differential signal by either using an on-board balun or a high-speed high-linearity amplifier before fed into the test chip. The clock signal is obtained from the RF signal generator, e.g., HP8665A. The power supply for the voltage reference and other commercial analog chips on the board is +5 and -5 V, which is provided by the DC power supply instrument.

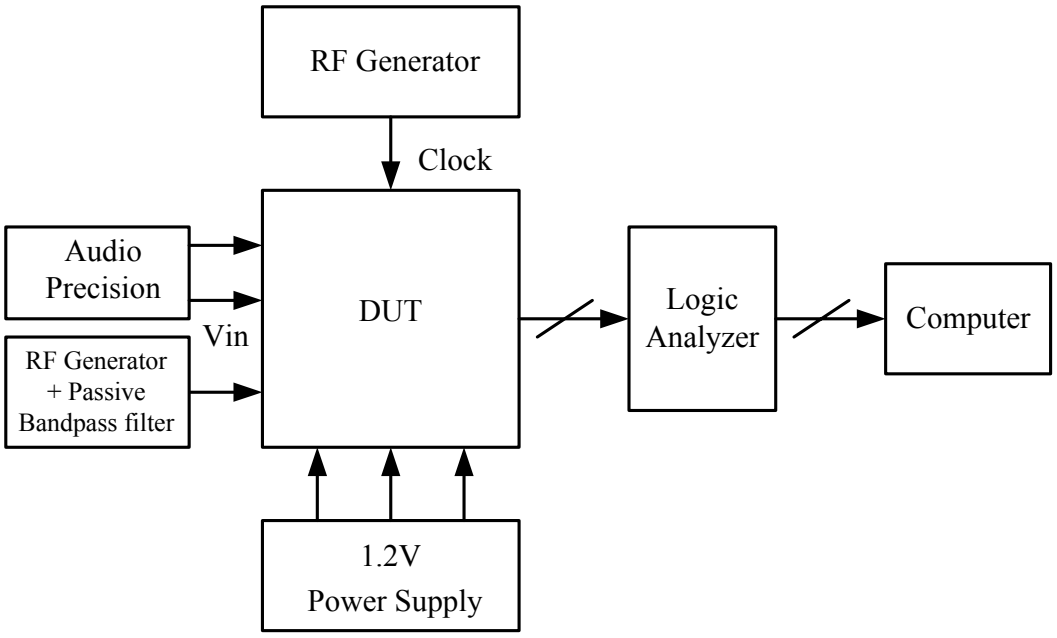

Figure 6.5 ΔΣ modulator test environment

The digital power supplies of the test chip as well as of other commercial digital chips are also directly provided by the instrument. The modulator outputs are buffered by the commercial bus driver on the board before they are sampled by the logic analyzer. The data acquired by the logic analyzer is transferred to the computer and analyzed by commercial software, e.g., spectrum analysis with MATLAB.

6.3. Measurement Results

For the test chip measurement, the supply voltage of the chip was set to 1.2 V, the input signal common-mode voltage was set to 0.4 V, and the output common mode level of the circuit was set to 0.6 V. External voltages VREFP and VREFN generated

by on-board drivers were used as the reference voltages of the internal quantizers and feedback DACs.

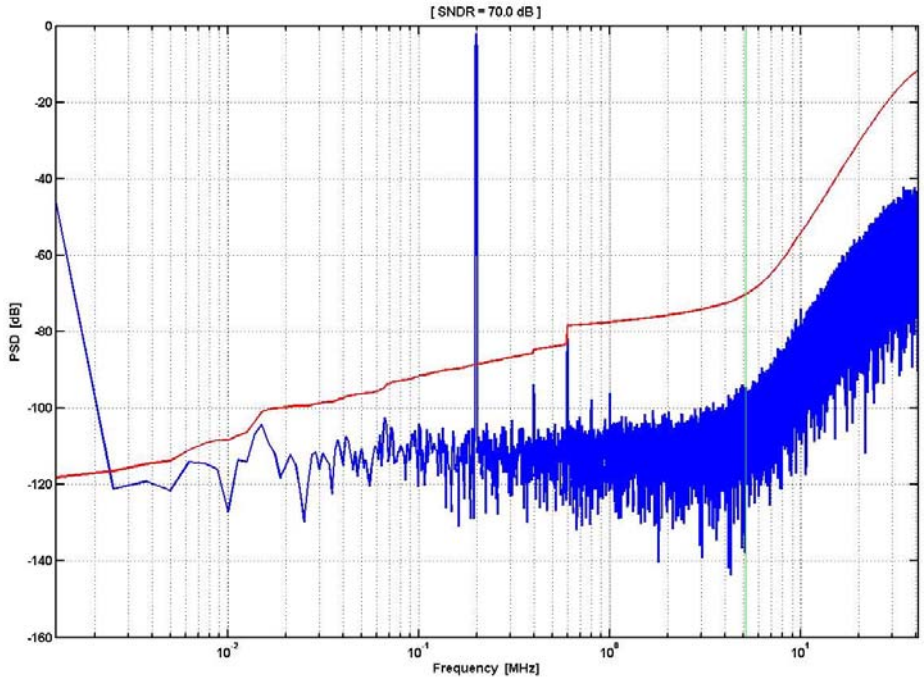

Figure 6.6 Measured output spectrum of the designed ΔΣ modulator

During the chip evaluation, the critical feedback path delay from the quantizer through the DWA to the first integrator feedback DAC was much larger than expected. Three possible reasons can account for this. One is the long metal wiring which results in substantial parasitics. The second is the reduced speed of the digital circuits after layout because of the STI and well proximity effect. The last one might be the dummy metal fill used for reliable process fabrication. Even though all the metal fills are floating they also added coupling paths and more parasitics.

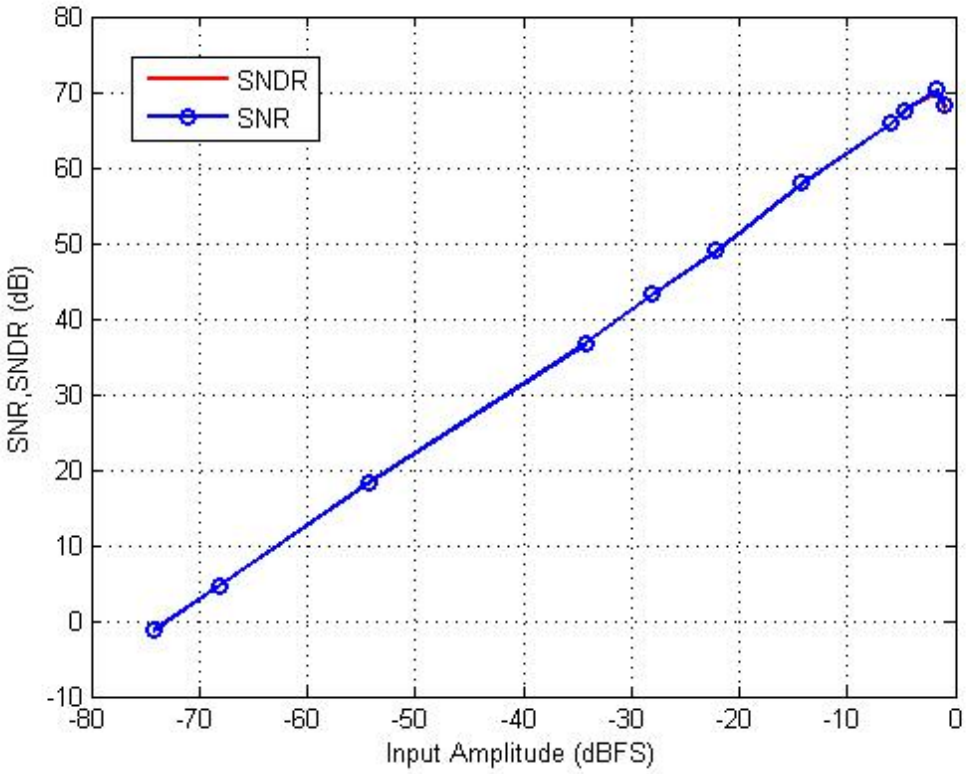

Figure 6.7 Measured SNR/SNDR with different input levels

As a consequence, the non-overlapping time between p1 and p2 had to be widened. This can be done by reducing the bias current. Unfortunately the bias current is also shared with the analog building blocks such as opamps and comparators. Therefore the clock rate of the experimental modulator had to be lowered.

The modulator's performance was evaluated by driving it with a fully differential sinusoidal signal, and capturing the output data through a logic analyzer. Then, the output spectrum of the modulator was evaluated by performing the Fast Fourier Transform (FFT) with Matlab. Fig. 6.6 shows the measured output spectrum for a -1.8

dBFS 200-kHz sine-wave input signal and 40 MHz clock signal. A 70 dB SNDR was achieved within a 5 MHz signal bandwidth. The measured SFDR was around 81 dB.

Fig. 6.7 shows the measured results with a 200-kHz input sine wave with different input amplitude. The test chip showed almost the same SNR and SNDR performance over the whole input range. The total power dissipation is around 10 mW.

The overall performance is summarized in Table 6.1.

Process	90nm 1P6M Digital CMOS
Sampling Frequency	80 MHz
Clock Frequency	40 MHz
Signal Bandwidth	5 MHz
OSR	8
Power Supply	1.2 V
SNDR/SFDR	70 dB/81 dB
FOM	0.39 pJ/Conversion
Power Consumption	10 mW
Core Area	0.5 mm^2

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CHAPTER 7. CONCLUSIONS

7.1. Summary

Inventions and new techniques are the main stimulus factors to push the human civilization moving forward. The same principle applies to the semiconductor industry. High performance analog to digital data converters have been proven to be among the crucial building blocks in a very large scale SOC (system on chip). Having the ability to possess low power, low noise, low cost, high speed and high resolution simultaneously becomes the ultimate demand for ADCs today. All these motivate circuit designers to come up with new solutions and practical techniques to improve the performance. In this thesis, innovations at both system level and transistor level are introduced to improve the performance of the broadband low power ΔΣ modulators in advanced deep sub-micron CMOS process.

First of all, a novel double-sampled ΔΣ modulator topology was proposed to relax the critical feedback timing issue. This new topology helps to mitigate the high speed requirement of the quantizer and the DEM logic to save power consumption and improve the design robustness.

Second, a new Data Weighted Averaging (DWA) realization was proposed to reduce the hardware consumption. With less chip area, the cost can be reduced.

Then, a cross-coupling technique was proposed to eliminate parasitic capacitor effect in a charge-pump based switched-capacitor integrator. Also, design

methodologies were introduced to incorporate a modified charge-pump based switched-capacitor integrator into a low-distortion ΔΣ modulator. A second-order ΔΣ modulator was designed and simulated to verify the proposed modulator topology.

The rest of the thesis covers the design of an experimental low power broadband double-sampled ΔΣ modulator. Combining innovative system level and circuit level design, the experimental ΔΣ modulator achieved 70 dB SNDR within a 5 MHz bandwidth. Fabricated in a 90 nm 1P6M digital CMOS process, the modulator consumes 10 mW with a 1.2 V power supply.

7.2. Future Work

1. Digital calibration: finer transistor size makes digital assisted analog circuits very practical and attractive. With the help of digital circuits, the vulnerabilities of analog circuits can be overcome. Digital calibration is also very useful in ΔΣ ADCs. Its application includes: feedback DAC accuracy and linearity calibration, to improve quantization noise cancellation in a cascaded modulator topology, and so on. Future research and development of a ΔΣ ADC should consider utilizing digital calibration techniques.

2. Embedding of a ΔΣ ADC with VGA: A variable gain amplifier function (VGA) can be considered for embedding in a ΔΣ ADC. Since a broadband ΔΣ ADC is usually integrated in a receiver, and a VGA is always inserted before the ADC to utilize the full dynamic range of the ADC. Integration of both parts into a single block can yield smaller chip area and more flexibility.

3. Digital trends to realize a ΔΣ ADC: Generally speaking, the operational amplifier is a critical and necessary building block of a ΔΣ ADC. However, designing and maintaining its performance under process, supply voltage and temperature (PVT) variations tends to be more and more difficult in advanced CMOS process. It has been proven that operational amplifiers can be replaced by inverters or comparators. These blocks are digital circuit based, and are insensitive to PVT variations. Also they consume less power than operational amplifiers. But this technique remains at the research level. Future work should consider how to make this technique more practical.

4. Broadband continuous-time (CT) ΔΣ ADCs: Compared with discrete-time (DT) ΔΣ ADCs, CT ΔΣ ADCs do not need an input buffer and oftentimes no reference voltage buffer either. Both of these buffers consume considerable amount of power consumption. Furthermore CT ΔΣ ADCs have some anti-aliasing abilities which simplify the system design. Despite the aforementioned advantages, CT ΔΣ ADCs do have a lot of disadvantages. Nevertheless its bright application perspective opens a door for circuit designers to explore for solutions and new techniques. Actually, CT ΔΣ ADCs have already become one of the hottest research fields in the past couple years.