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Kartikeya Mayaram Terri S. Fiez

The design of mobile wireless devices has always focused on reducing power, area, and cost. This dissertation proposes two techniques that are leveraged to save power and area and therefore cost. The first techniques reduces the noise in the receiver and results in a relaxed power requirement. The second technique filters the blocker on-chip and allows for the removal of bulky off-chip components in a wireless system.

In the first technique a two-path noise-cancellation architecture is used that reduces the noise in the receiver front end. A prototype ultra-wideband (UWB) receiver is designed and fabricated based on this idea in a 130 nm CMOS process. The fabricated prototype achieves an energy efficiency of 0.48 nJ/bit with a sensitivity of -82 dBm while operating across a wide data rate range of 0.1-25 Mb/s.

The second technique is a blocker filtering scheme that extracts the clock from the blocker and helps eliminate bulky off-chip surface acoustic wave (SAW) filter components. Implemented in a 65 nm CMOS process, the filter is able to track the blocker within 1 to 1.6 GHz and provides better than 10 dB of rejection at the notch frequency for blockers from -40 dBm to -10 dBm.

Noise and Blocker Cancellation Techniques for Power and Area Efficient Wireless Receivers

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APPROVED:

Co-Major Professor, representing Electrical and Computer Engineering

Co-Major Professor, representing Electrical and Computer Engineering

Director of the School of Electrical Engineering and Computer Science

Dean of the Graduate School

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Saeed Pourbagheri, Author

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CHAPTER 1. INTRODUCTION

Designs of today's radio frequency (RF) circuits and transceivers strive to achieve better power and area efficiency than previous generations. Despite many innovations that have been proposed in the literature to reduce the power consumption of RF circuits, battery life continues to be a major challenge in mobile wireless systems. Meanwhile, the cost of a mobile device is closely tied to the area and the number of off-chip components utilized to meet the aggressive wireless standard specifications.

Wireless sensor networks (WSNs) have been an important area of research recently due to their numerous applications [1]-[7]. Due to the low power nature of a WSN, energy efficiency is a critical metric in the design of such a system. Energy efficiency determines how efficiently the energy (from a battery or stored by an energy harvester) is being used for communication purposes within a sensor network. This metric can be improved by reducing the amount of power consumed to transmit and receive a single bit of data. One approach to

reduce this power is to relax the noise requirement at the receiver side of the sensor network. This approach is described in detail in Chapter 2.

Area and cost efficiency is another consideration for a wireless system. Significant efforts have been made towards reducing the real-estate and the cost associated with off-chip components. A high level of integration required to implement several standards in a single RF chip mandates minimizing the number of off-chip components such as SAW devices. A SAW filter is usually used in RF receivers to meet the stringent filtering requirements dictated by a wireless standard. These off-chip filters are responsible for attenuating the strong blockers at the input of a receiver. In Chapter 3, an on-chip blocker filtering solution is proposed that enables the removal of the off-chip SAW filter.

1.1 Dissertation Outline

The remainder of this dissertation is organized as follows. Chapter 2 presents an energy-efficient UWB receiver. A mathematical model and analysis of the conventional and the proposed two-path non-coherent receivers is provided. The system architecture of the overall receiver and the design of various blocks are described and the measurement results of a prototype test chip implemented

in a 130 nm CMOS technology are presented.

Chapter 3 focuses on a blocker filtering architecture that allows for the elimination of the off-chip SAW filter. The proposed blocker-filtering architecture and the circuit implementation of the filter along with the measurement results of a prototype test chip fabricated in a 65 nm CMOS technology are presented. Finally, Chapter 4 concludes the dissertation.

CHAPTER 2. A NOISE-CANCELING NON-COHERENT ENERGY DETECTION IR-UWB RECEIVER FOR WIRELESS SENSOR NETWORKS

2.1 Introduction

Impulse Radio UWB (IR-UWB) is a promising communication technique for low power and low complexity short-range wireless sensor network (WSN) applications [1]-[7]. This technique communicates with short duration RF pulses (on the order of nanoseconds) over a wide frequency bandwidth (e.g., 500 MHz) in the 3.1-10.6 GHz range [8]. In low data rate WSN applications, non-coherent reception schemes are more popular than coherent schemes because of their simplicity and superior energy efficiency. Additional power is needed for the phase tracking and timing synchronization in coherent schemes [9]. Meanwhile, aggressive duty cycling along with a simple baseband architecture of the IR-UWB receiver makes it a desirable technique for an energy efficient implementation [10].

Energy detection is the most prevalent architecture among non-coherent IR-UWB receivers [2]-[7]. These receivers are based on the simple idea of amplifying, squaring and integrating the pulse over large time durations

(several tens of nanoseconds). Their simple architecture makes these receivers suitable for low data rate WSNs. In a receiver for WSN applications, the goal is to achieve a minimal energy-per-bit. This can be achieved by either minimizing the power consumption in the receiver circuitry or increasing the effective data rate. Since WSNs are inherently low data rate applications, there is a limit to increasing the data rate. Therefore, a reduction in the receiver power consumption is required.

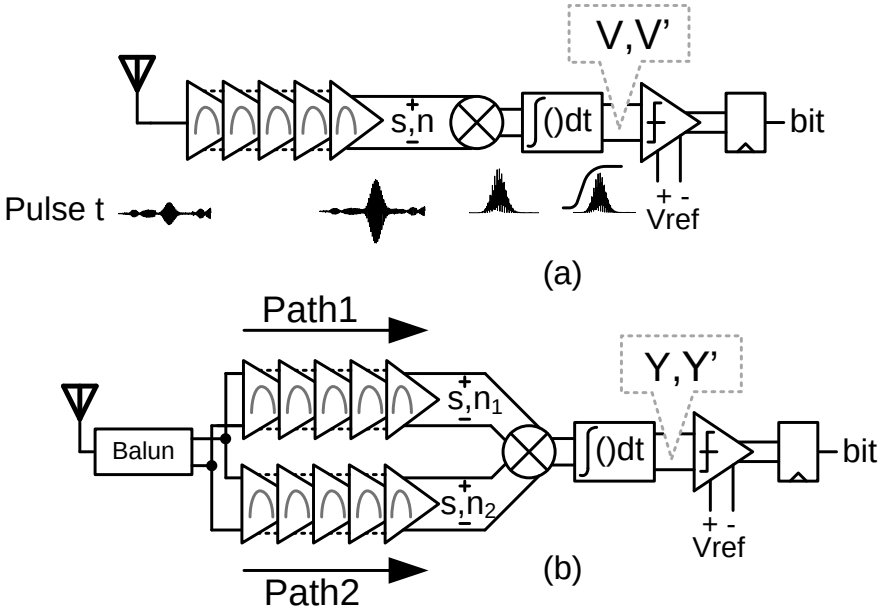


Figure 2.1: Block diagram of an energy detection receiver using (a) conventional architecture, and (b) proposed architecture.

In a conventional non-coherent ED architecture (Fig. 2.1(a)), the RF front-end generally requires a large gain prior to the self-mixing block. This is due to the non-linear nature of the squaring operation. This large gain is usually provided by a power-hungry wideband low noise amplifier (LNA). Since the LNA is the first block in the receiver front-end, it is the main contributor to the overall noise. The challenges in LNA design are low noise, high gain and wide bandwidth. All these requirements must be achieved with a low power dissipation. Based on the power consumption measurement results reported in [2]-[7], about 50% to 99% of the receiver power budget is spent in the gain stage to meet the wideband, high gain, and low noise requirements of the LNA. There is a close relationship between the noise performance and the power consumption in the design of an LNA [11]. Therefore, suppressing the noise by employing system-level enhancements can be advantageous in relaxing the LNA noise requirement. Due to a reduction in the noise requirements, power consumption can be reduced to improve the overall energy efficiency.

In this work, we propose an energy detection receiver that uses two identical paths in the gain stage to alleviate the noise (Fig. 2.1(b)). Two wideband, high-gain, band-selective paths (path1 and path2) amplify short UWB pulses. The random noise processes, n_1 and n_2, generated in the two independent paths are un-correlated and of equal power. The signal, *s*, on the other hand, is completely

correlated because both paths amplify the input signal to the same extent. The signal and noise from each path are mixed together and then integrated. The integration result of the squared signal (s^2) represents the energy of the signal. At the same time, the integration of the cross-mixing ($n_1 \times n_2$) of two un-correlated random processes will result in a random noise process with 3 dB less power compared to a conventional self-mixed (n^2) ED architecture. The suppressed noise power is utilized to relax the noise requirement of the LNA. The new architecture has two paths which would normally double the power consumption. However, by using low voltage circuit design and stacked circuits with current reuse the power consumption is not increased.

2.2 Mathematical Model of the Non-Coherent Energy Detection Receiver

A mathematical model that evaluates the energy of a band-limited signal is described here. The goal is to achieve a stochastic description of the signal and noise at the receiver and then calculate the detection error probability. Our focus is on detecting the energy of a signal with a limited bandwidth of W, and over a particular integration window of $[0, T]$ in the presence of random noise. The integration result of the signal over $[0, T]$ represents the energy, and accordingly the presence, of the signal over that time interval. On-off keying (OOK)

modulation is employed to achieve a superior energy efficiency. As opposed to pulse position modulation that needs two integration periods to detect a bit, in OOK, one data bit can be detected for every integration. W and T are decided based on the typical ED receiver implementation considerations to be 500 MHz and 30 ns, respectively. The wide bandwidth along with the long integration window allow the integration result to be approximated by a Gaussian process.

2.2.1 Conventional Architecture

It is known that a signal of duration, T, with bandwidth, W, can be represented by a set of $N_s = 2TW$ equally spaced samples, $1/2W$ apart. Moreover, the energy of the sampled signal can be approximated by a finite sum of the squared sample values. The accuracy of this approximation has been studied in [12]. The noise and signal are expressed as a sum of N_s samples:

$$n(t) = \sum_{i=1}^{2TW} a_i . sinc(2Wt - i) \tag{2.1}$$

$$s(t) = \sum_{i=1}^{2TW} \alpha_i . sinc(2Wt - i) \tag{2.2}$$

where a_i and α_i are the noise and signal sample values, respectively. We define $v(t)$ and $v'(t)$ as the energy over the $[0, T]$ time period in the absence and the

presence of the deterministic signal. In addition, the energy values $v(t)$ and $v'(t)$, normalized to the noise power spectral density, at the output of the integrator are defined as the random processes V and V' (Fig. 2.1(a)), respectively.

$$v = \int_0^T n(t)^2\, dt = \frac{1}{2W} \sum_{i=1}^{2TW} {a_i}^2 \tag{2.3}$$

$$v' = \int_0^T \big(n(t) + s(t)\big)^2\, dt = \frac{1}{2W} \sum_{i=1}^{2TW} (a_i + \alpha_i)^2 \tag{2.4}$$

$$V = \frac{2}{N_0} \int_0^T n(t)^2\, dt = \frac{1}{N_0 W} \sum_{i=1}^{2TW} a_i^2 = \sum_{i=1}^{2TW} b_i^2 \tag{2.5}$$

$$V' = \frac{2}{N_0} \int_0^T (n(t) + s(t))^2\, dt = \sum_{i=1}^{2TW} (b_i + \beta_i)^2 \tag{2.6}$$

where b_i and β_i are the normalized noise and the normalized signal sample values, respectively, and N_0 is the single-sided noise power spectral density. Each b_i is a Gaussian random variable with a zero mean and unity variance. Consequently, a finite sum of the squared b_i's in (2.5) results in a central chi-square distribution. If a deterministic signal $s(t)$ with energy E_b is present at the input of the energy detector along with the noise, the output random process has a noncentral chi-square distribution. Both chi-square processes have $2TW$

degrees of freedom (i.e., the time-bandwidth product). V' has a noncentrality parameter of $2E_b/N_0$ [13]. The noncentrality parameter is also an indication of the ratio of the signal power to the noise power.

$$\frac{2}{N_0}\int_0^T s(t)^2\,dt = \sum_{i=1}^{2TW}\beta_i^2 = \frac{2E_b}{N_0} = N_s \times SNR \tag{2.7}$$

Based on the central limit theorem, it is well known that if the number of degrees of freedom of a chi-square process becomes large, its probability density function (PDF) can be asymptotically approximated by a normal PDF. Since both V and V' are of $2TW = 30 \gg 1$ degrees of freedom, we represent them with normal PDFs. Fig. 2.2 shows the PDFs of V and V'. In Fig. 2.2, the left and right curves are the Gaussian approximation of the central and noncentral chi-square distributions of V and V', respectively. The means and variances of these PDFs are $\mu_V = 2TW = 30$ and $\sigma_V^2 = 4TW = 60$ for V and $\mu_{V'} = 2TW + 2\,E_b/N_0 = 60$ and $\sigma_{V'}^2 = 4TW + 8\,E_b/N_0 = 180$ for V'. As we will explain later in this section, the overlapping area between these two curves represents the detection error probability [14].

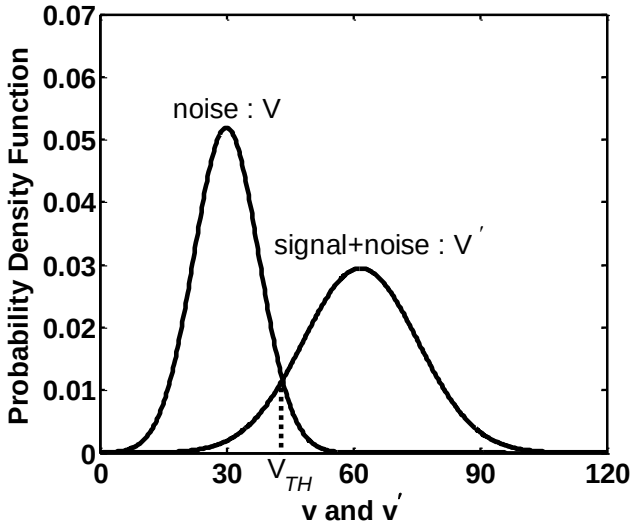


Figure 2.2: Chi-square distributions of V and V' for TW=15 and E_b/N_0=15.

2.2.2 Two-Path Uncorrelated Noise Architecture

As shown in Fig. 2.1(b), the two-path architecture includes two separate but identical gain paths. Each path generates noise which is independent and uncorrelated from the noise generated in the other path. Since the signal experiences an equal gain while passing through these independent paths, we expect to observe completely correlated and identical signals, $s(t)$, at the output of the two gain stages. Therefore, the output of the multiplier is the self-mixing of the signal, $s(t)^2$. The integration of the self-mixing of the signal over the time interval $[0, T]$ will result in the signal energy in that time interval. At the

same time, the multiplier cross-mixes the two noise processes. The integration of the cross-mixing of two uncorrelated Gaussian noise processes, $n_1(t)$ and $n_2(t)$, over the same time interval, $[0, T]$, will result in another Gaussian process.

Similar to the previous section, we express the signal and the noise with a set of N_s samples. We also define $y(t)$ and $y'(t)$ as the integration of the cross-mixing of $x_1(t)$ and $x_2(t)$ over the $[0, T]$ time interval, in the absence and the presence of the deterministic signal in (2.8) and (2.9), respectively. $x_1(t)$ and $x_2(t)$ represent the combination of the signal and the noise at the output of path1 and path2, respectively.

$$y(t) = \int_0^T n_1(t).n_2(t)\,dt = \frac{1}{2W}\sum_{i=1}^{2TW} a_{1i}.a_{2i} \tag{2.8}$$

$$y'(t) = \int_0^T x_1(t).x_2(t)\,dt = \frac{1}{2W}\sum_{i=1}^{2TW} (a_{1i}+\alpha_i).(a_{2i}+\alpha_i) \tag{2.9}$$

$$Y = \sum_{i=1}^{2TW} b_{1i}.b_{2i} \tag{2.10}$$

$$Y' = \sum_{i=1}^{2TW} (b_{1i}+\beta_i).(b_{2i}+\beta_i) = \sum_{i=1}^{2TW} (b_{1i}\,b_{2i} + \beta_i^2 + b_{1i}\beta_i + b_{2i}\beta_i) \tag{2.11}$$

where a_{1i} and a_{2i} are the noise sample values and b_{1i} and b_{2i} are the normalized noise sample values with a Gaussian random distribution of zero mean and

unity variance in path1 and path2, respectively. Y and Y' are random processes that represent the windowed integration results over N_s samples in the absence and the presence of the signal, respectively.

In order to evaluate the stochastic behavior of the two-path ED structure, we need to determine the PDF of Y and Y'. Following a line of reasoning similar to the conventional architecture, Y and Y' can also be approximated by normal distributions. Since b_{1i} and b_{2i} are independent uncorrelated processes, intuitively, the mean of Y is zero. Similarly, the three terms $\sum_{i=1}^{2TW} b_{1i}.b_{2i}$, $\sum_{i=1}^{2TW} b_{1i}.\beta_i$ and $\sum_{i=1}^{2TW} b_{2i}.\beta_i$ in (2.11) have a zero mean value. The mean value of the term $\sum_{i=1}^{2TW} \beta_i^2$ is $2E_b/N_0$ and is equal to the ratio of the signal power to the noise power. To determine the variances of Y and Y', MATLAB calculations are used. The Gaussian approximations of Y and Y' are plotted in Fig. 2.3.

Gaussian behavior of V, V', Y and Y' implies that the area under-the-curve for all four PDFs is the same. Comparing Y and Y' with the curves V and V' in Fig. 2.2, two observations can be made. First, the two PDFs are shifted left (smaller mean values) but the difference between their mean values is the same. Second, both curves are narrower (smaller variance values). To make this analogy more obvious, V, V' are shifted to the left by μ_V and plotted together with Y and Y' in Fig. 2.4. The same conclusion holds for

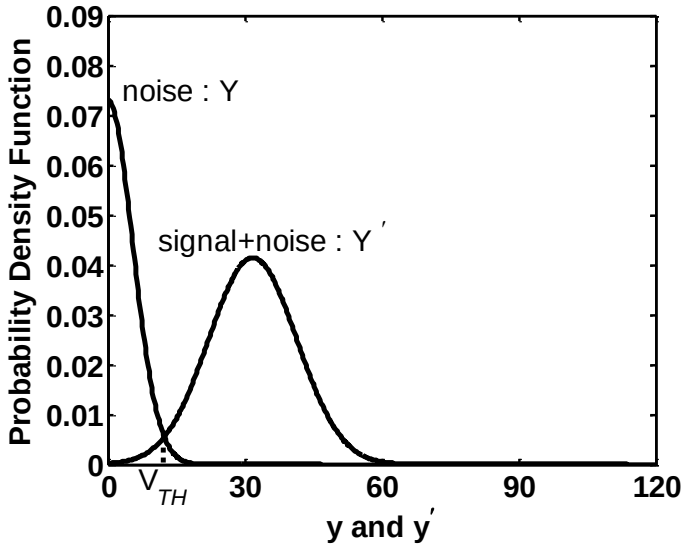


Figure 2.3: Gaussian distribution approximations of Y and Y' for TW=15 and E_b/N_0=15.

V' and Y'. Mathematical calculation shows that the variance of Y or Y' is half of the variance of V or V'. Since the variance of a Gaussian noise process represents the noise power, it can be concluded that the noise power in both the Y and Y' processes is 3 dB less than the noise power in V and V', respectively. In the next section, we will show how this 3 dB reduction in noise power manifests as a BER performance improvement in an OOK communication system.

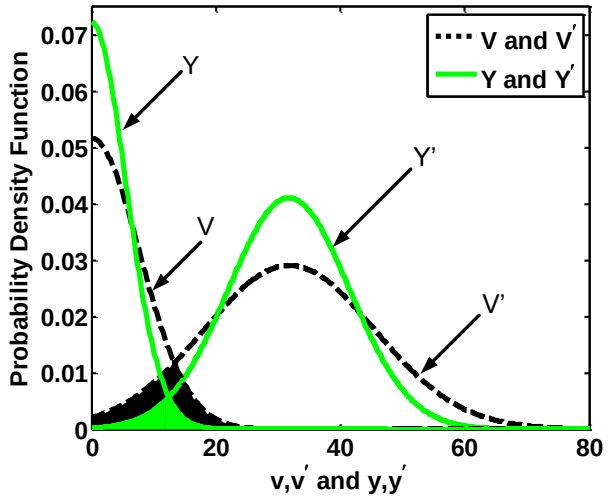


Figure 2.4: Overlaid plots of shifted V, V' and Y, Y' for TW=15 and E_b/N_0=15.

2.2.3 Error Probability in ED OOK Detection

In an OOK modulation, the absence of the signal represents bit "0" and the presence of the signal represents bit "1". An erroneous detection happens when the presence of the signal is detected as "0" or the absence of the signal is detected as "1". Assuming that 1's and 0's occur with equal probabilities, the probability of an error is:

$$P_{error} = \frac{1}{2} P(RX = 0|TX = 1) + \frac{1}{2} P(RX = 1|TX = 0) \qquad (2.12)$$

where RX and TX are the received bit and the transmitted bit, respectively. In our mathematical model, V and Y correspond to bit "0" (with a probability of P_N), while V' and Y' correspond to bit "1" (with a probability of P_{SN}). The shaded area in Fig. 2.4 represents samples of signal + noise that are detected as noise and samples of noise that are detected as signal + noise. Shown in Fig. 2.2 and Fig. 2.3, V_{TH} is the horizontal axis value at which the two curves intersect. This intersection point of the two curves represents the optimum threshold value where a minimum detection error occurs.

$$P_{err} = \frac{1}{2}\int_{-\infty}^{V_{TH}} P_{SN}(y)\,dy + \frac{1}{2}\int_{V_{TH}}^{+\infty} P_N(y)\,dy$$

$$= \frac{1}{2}\left[1 - Q\left(\frac{V_{TH} - \mu_{SN}}{\sigma_{SN}}\right) + Q\left(\frac{V_{TH} - \mu_N}{\sigma_N}\right)\right] \qquad (2.13)$$

The function $Q(x)$ is the tail integral of the unity variance, zero mean Gaussian PDF:

$$Q(x) = \frac{1}{\sqrt{2\pi}}\int_x^{\infty} e^{-z^2/2}\,dz = \frac{1}{2}erfc\left(\frac{x}{\sqrt{2}}\right) \qquad (2.14)$$

The detection errors for both conventional and two-path architectures are calculated from (2.13) and shown in Fig. 2.5. Depending upon the E_b/N_0, the overlap area between the two curves and, consequently, the BER varies. As a numerical example, for $E_b/N_0 = 16\ dB$, BW=500 MHz and T=30 ns, the BER

drops from 10^{-3} to 10^{-5} if we use the two-path architecture instead of the conventional ED architecture. Meanwhile, the E_b/N_0 needed to provide a BER of 10^{-3} is reduced by more than 2dB.

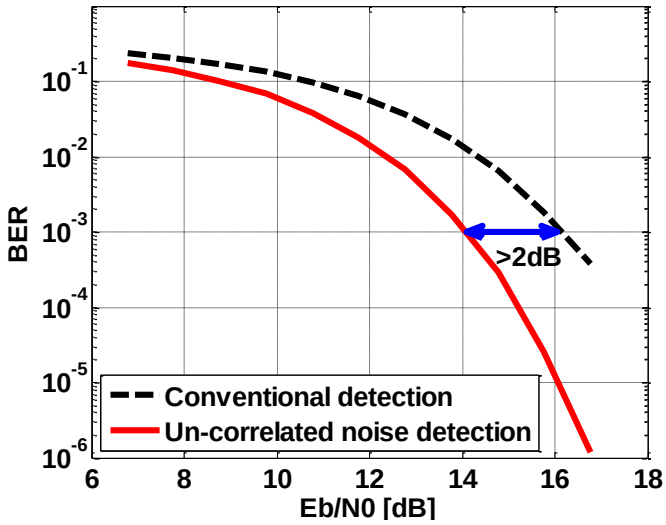


Figure 2.5: Bit error rate accounting for false detection in OOK modulation versus E_b/N_0.

The relationship between E_b/N_0 and the minimum desired SNR (SNR_{min}) for a target BER=10^{-3} is

$$SNR_{min} = \left(\frac{E_b}{N_0}\right)_{min} + 10log(\frac{DR}{BW}) \qquad (2.15)$$

where *DR* is the data rate of the receiver. The receiver sensitivity (P_{sen}) is given by

$$P_{sen} = -87dBm + NF + SNR_{min} \tag{2.16}$$

where -87 dBm is the noise power for a channel bandwidth of 500 MHz and *NF* is the noise figure of the receiver. Based on (2.15) and (2.16), any reduction in the required E_b/N_0 can be directly translated to a relaxed noise constraint (*NF*) of the receiver. In the IR-UWB receiver presented in this paper, due to more than a 2dB reduction in the required E_b/N_0 by leveraging the two-path technique, the acceptable noise figure could be as large as 11dB. This relaxed requirement results in a low power LNA and consequently a low power receiver design.

2.2.4 Impact of Correlation between Noise in The Two Paths

So far, we have assumed that noise in both paths is completely uncorrelated. In practice, however, there are noise sources that contribute to both paths. These common noise sources appear at the input of the multiplier as correlated noise. As shown earlier, the correlated noise at the input of the multiplier will not cancel after mixing and integration as the correlated noise experiences self-mixing instead of cross-mixing.

In order to estimate the impact of this unwanted correlated noise on the proposed noise-canceling technique, we introduce w and w' as the energy over the $[0, T]$ time period in the absence and the presence of the deterministic signal:

$$w = \int_0^T (n_{1-c} + n_{1-unc}) \times (n_{2-c} + n_{2-unc})\, dt \tag{2.17}$$

$$w' = \int_0^T (s + n_{1-c} + n_{1-unc}).(s + n_{2-c} + n_{2-unc})\, dt \tag{2.18}$$

where n_{1-c} and n_{2-c} represent the correlated portion of the noise and n_{1-unc} and n_{2-unc} represent the uncorrelated portion of the noise in path1 and path2, respectively. Correlated noise power ($\overline{n_c}^2$) is usually a percentage of the overall noise power ($\overline{n_c}^2 + \overline{n_{unc}}^2$). Error probability can be calculated similar to the previous section for different amounts of correlated noise. Fig. 2.6 shows BER plots where correlated noise power is 0%, 10%, and 20% of the overall noise power at the input of the multiplier.

From Fig. 2.6, it is observed that a higher percentage of noise correlation between the two paths results in a less effective cancellation of noise and the BER plot approaches that of the conventional detection scheme (100% noise correlation). For the receiver implemented in this paper, the correlated noise will be shown to be less than 5% and, therefore, the degradation is negligible.

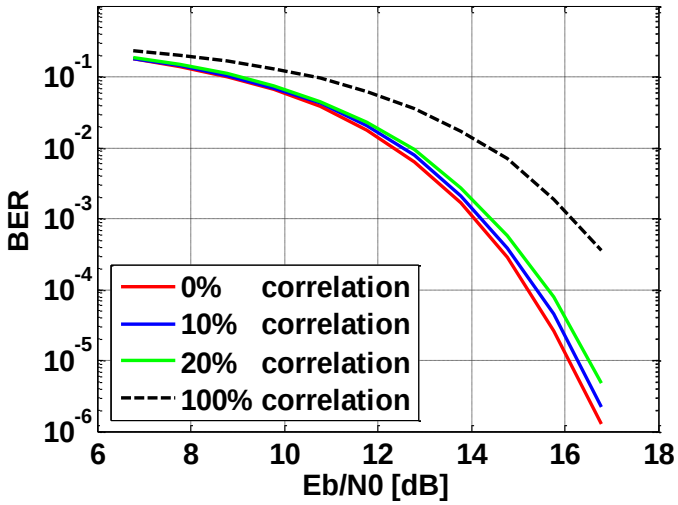


Figure 2.6: Bit error rate versus E_b/N_0 for different values of noise correlation between the two paths.

2.3 System Architecture Overview

The block diagram of the noise-canceling ED IR-UWB receiver for WSNs is shown in Fig. 2.7. The two-path system consists of a balun, two identical amplifying stages, an active multiplier, an integrator and a comparison/bit-detection block. In order to take advantage of the differential topology and suppress the power supply and substrate noise, a UWB balun is employed before the gain stage. Two parallel wideband, high-gain, band-selective paths amplify short UWB pulses corresponding to a 500 MHz signal bandwidth.

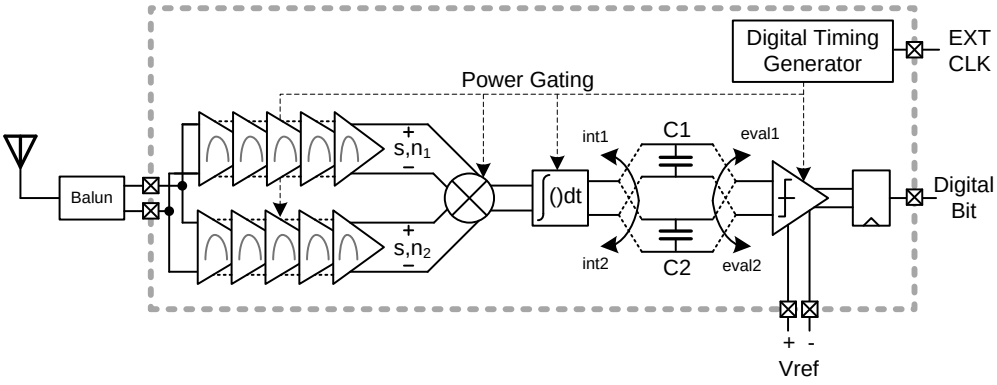


Figure 2.7: Block diagram of the noise-canceling ED receiver architecture.

The RF front-end is tuned to operate in the 3.5 GHz sub-band. Both upper and lower paths are tuned to this center frequency through external analog tuning pins. The signal is amplified by a gain greater than 35 dB while the out-of-band interferers are attenuated by the selectivity of the LNA. The multiplier block functions as a self-mixing and cross-mixing multiplier for the signal, s, and the noise, $n_1(t)$ and $n_2(t)$, respectively. The multiplier stage provides negligible loading on the previous amplifying stage. In addition, it has a pole at 250 MHz in order to low pass filter the self-mixed signal and reject the 7 GHz self-mixing product. The integrator stage integrates the low pass filtered envelope of the pulse over a time interval of 30 ns in order to collect 85% of the pulse energy spread over time because of the multi-path channel. The integrated value is then compared to an external differential reference in an

offset-compensated comparator to determine the presence (bit “1”) or the absence (bit “0”) of the signal.

Including the startup time, the entire receiver requires 40 ns for startup, integrating and detecting a single bit. This implies that a maximum data rate of 25 Mb/s is achievable with this architecture. To provide a continuous stream of bit decisions, two capacitors C_1 and C_2 store the integration results alternatively. During the integration/evaluation in C_1, a reset occurs in C_2 and vice versa. More details on the baseband timing are provided in Section III. All the necessary timing signals including integrate, evaluate, reset and power gating are generated in a digital timing generator block from an external reference clock. In order to optimally trade off the wide bandwidth of the IR-UWB technique for a better energy per bit in inherently low data rate WSN communication, aggressive duty cycling is necessary. Hence, all blocks must have the capability of switching on/off. Duty cycling will result in an average power that scales with the data rate while the instantaneous receiver power is constant. A scalable average power with data rate leads to constant energy per bit over a wide range of data rates (0.1-25 Mb/s in this receiver). The data rate can be simply scaled down by power gating the receiver and extending the receiver’s off period. Aggressive duty cycling along with band-selection in the gain stage and high pass filtering in the baseband reject the narrowband

interferers and thus achieve interference robustness. The receiver is designed so that it starts up in less than 7 ns. This specification is considered in the design of each individual block.

The proposed non-coherent receiver requires timing synchronization between incoming UWB pulses and the integration window. Due to the non-coherent nature of the energy detection architecture, a coarse synchronization, in the range of the integration window frequency of 1/40ns, suffices.

2.4 Receiver Circuit Description

The entire receiver is designed for a 1.2 V supply and implemented in a 130 nm CMOS process.

2.4.1 Gain Stage

The gain stage is composed of five cascaded differential amplifiers with an overall gain greater than 35 dB in both paths. This large gain is necessary to overcome the nonlinearity of the squaring operation and, furthermore, to relax the noise constraint of the following blocks (i.e., the multiplier and the integrator). A current reuse topology is utilized to stack the two paths and reuse the bias current in order to save power. Shown in Fig. 2.8, the first LNA's upper

and lower NMOS transistors are biased at VDD=1.2 V and 0.7 V, respectively, through the R_b resistors. Triple well NMOS devices are utilized in order to achieve better current efficiency and identical transconductances for both paths. Two parallel R_b=100 Ω resistors connected to the input pins are also responsible for providing the 50 Ω matching. Resistive termination for the first LNA is advantageous as this structure decouples input matching from the input device g_m and requires lower power while still providing a 50 Ω input impedance. Other wideband matching choices such as common-gate and shunt-feedback architectures generally require a g_m greater than 20 mA/V to provide the 50 Ω of input match [15]. In LNA design for low noise figure applications (NF < 6 dB), resistive termination structures do not usually satisfy the noise constraint. However, a system-level simulation shows that for a typical IR-UWB energy detection receiver, the front-end noise figure can be approximately as high as 8.5 dB for a BER of 10^{-3}. Hence, a low g_m first stage is more suitable when the focus is on low power design.

The following gain stages (Fig. 2.9) have a similar core architecture except that they are DC coupled to the previous stage so as to relax the bias settling required for power gating. In order to keep the upper and lower noise sources uncorrelated, a high density MOS capacitor is connected between the middle

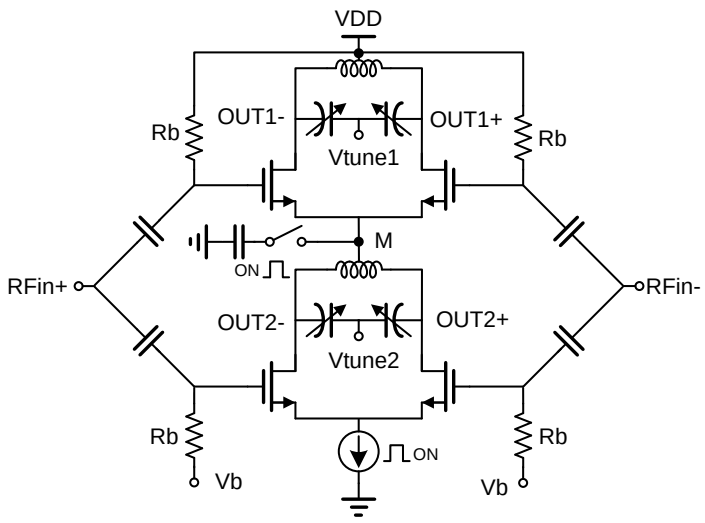


Figure 2.8: First stage stacked current-reuse LNA with resistive input matching.

node (M) and ground during the LNA active period. Power-gating is performed by switching the tail current source through ON pulses. The amplifier spends the initial 7 ns in startup mode and the remaining 30 ns in amplifying mode.

The stacked current reuse topology along with a 1.2 V supply voltage means that there is not enough voltage headroom to employ cascode transistors for isolation purpose. However, due to the differential structure of the amplifier, a low voltage neutralization technique can be utilized. This serves two purposes: i) it improves the reverse isolation, and ii) it eases the tuning of the center frequency for each stage. The principle of the

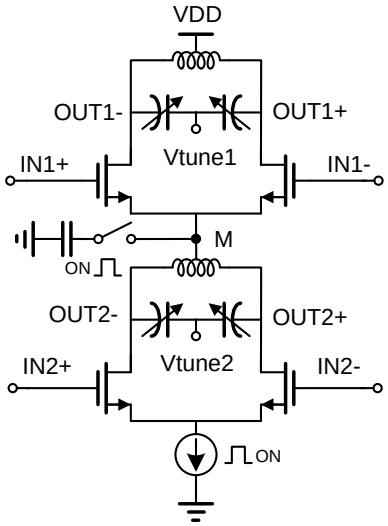


Figure 2.9: Second to fifth stacked current-reuse amplifying stages. Each stage is DC coupled to the preceding stage.

neutralization is to cancel the parasitic gate-drain capacitor effect with an equal and opposite transfer of charge [16], [17]. In a differential topology, both the signal and the inverted replica of the signal are available. Fig. 2.10 illustrates the neutralization scheme employed for both the upper and lower amplifiers.

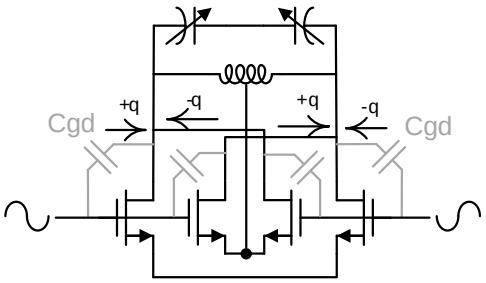


Figure 2.10: Low voltage differential neutralization technique.

The gain stage has a 500 MHz bandwidth at a center frequency of 3.5 GHz.

To adjust for process variation and also for tuning the front-end gain, load varactors are tunable through V_{tune}. The first amplifier is designed to provide 20 dB of voltage gain. All the following amplifiers are designed to have an identical gain of 10 dB with 400 MHz of bandwidth tunable over a range of 1 GHz. To obtain a gain greater than 35 dB over a bandwidth of 500 MHz, the first stage is tuned to the center frequency of f_c=3.5 GHz and the following stages are tuned to $f_c + \Delta f$ (2nd and 4th) and $f_c - \Delta f$ (3rd and 5th), respectively, where Δf is the frequency offset from f_c=3.5 GHz.

The overall noise at the output of the gain stage is simulated in order to measure the amount of correlated noise power between the two paths. Considering all noise sources, only the antenna noise is fully correlated between the two paths. In addition to the antenna, the noise from the input termination resistors (R_b) can partially leak from path1 to path2 and vice versa [18]. The combination of these two correlated noise sources is measured at the output of path1 and path2 and introduced in (2.17) and (2.18) as n_c. Since the gain stage is designed such that the uncorrelated noise dominates the overall noise, the percentage of correlated noise power ($\overline{n_c}^2$) to overall noise power ($\overline{n_c}^2 + \overline{n_{unc}}^2$) is less than 5%. Therefore, based on Fig. 2.6, the noise-canceling scheme provides better than 2 dB reduction in the overall required E_b/N_0.

2.4.2 Multiplier

The schematic of the fully differential four-quadrant $V_{gs} \times V_{ds}$ type multiplier used is shown in Fig. 2.11 [19]. Several considerations are taken into account in designing this circuit. A maximum possible input-to-output gain and minimal loading of the preceding gain stage are targeted. Furthermore, this circuit must be able to start up in a few nanoseconds. Due to the large gain in the previous amplifying stage, noise generated in the multiplier circuit is not a major design concern. In Fig. 2.11, the four bottom transistors, M1-M4, operate in the linear region while the top transistors, M5-M8, operate in the saturation region. Proper bias voltages are provided through the biasing $R_b C_b$ circuit with a HPF cut-off frequency of 120 MHz. The transconductances of M5-M8 are designed large enough so that the top transistors operate as unity-gain source followers. The bottom transistors in the triode region function as voltage-controlled resistors. They generate currents corresponding to the multiplication of the signals applied to the gates of the upper (M5-M8) and lower (M1-M4) transistors. The length of M1 to M4 devices is chosen to be 180 nm to achieve a better long-channel behavior.

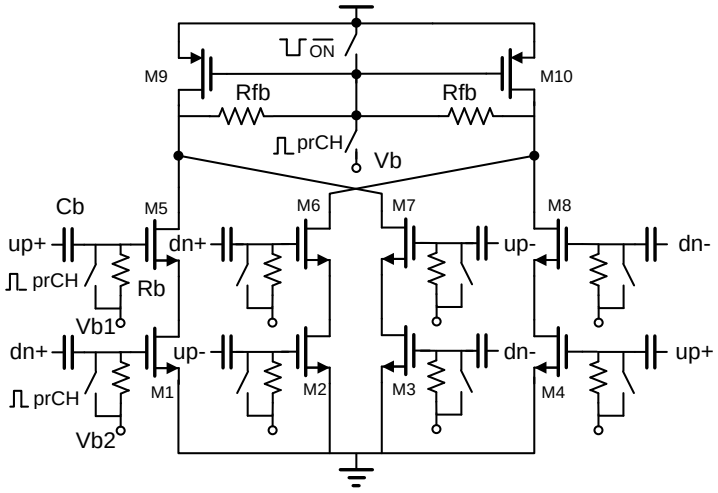


Figure 2.11: Fast start-up four quadrant multiplier.

The larger aspect ratio of the bottom devices provides higher multiplier gain. However, a large parasitic capacitance is introduced by the large input devices. This leads to a division of the signal between the input parasitic capacitors and the input biasing AC coupling capacitors, C_b's. In order to avoid the gain drop at the multiplier input, larger AC coupling capacitors are required. A larger C_b will slow down the charge and discharge rate of the input gate bias nodes during duty cycling and consequently will require a longer startup time. As a result, there is a trade-off between the multiplier gain and the startup speed. The optimum C_b for the gain-startup speed trade-off in our case is determined to be 220 fF from circuit simulations.

The combination of the parasitic capacitor, of the multiplier itself and the following integrator, and the multiplier output resistor form a pole at 250 MHz. This pole filters out the high frequency term of the squared signal and passes the 0-250 MHz envelope of the signal to the integrator. For fast startup, short pre-charging pulses (prCH in Fig. 2.11) are introduced so that the R_b biasing resistors can be bypassed for a few nanoseconds and the bias nodes can be pre-charged to their nominal values V_{b1} and V_{b2}. A similar idea is employed to charge the slow common-mode node to V_b. The input/output $K.V_{in}{}^2$ relationship of the multiplier circuit is obtained from simulation and is shown in Fig. 2.12.

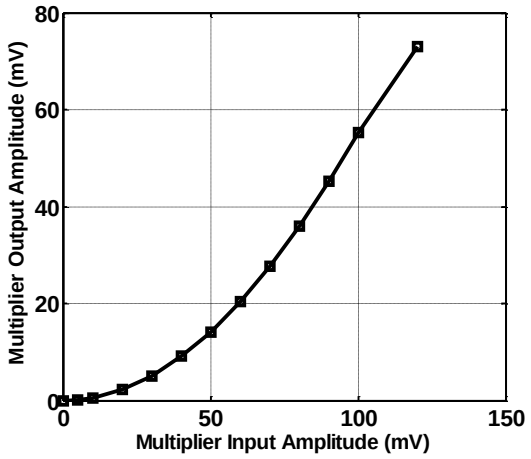


Figure 2.12: Squaring function of the multiplier for variable input pulse amplitudes.

2.4.3 Baseband Integrator

The core integrator is a simple fully-differential telescopic OTA. The integrator schematic with two differential integration capacitors is shown in Fig. 2.13. This structure achieves a continuous bit detection with a maximum data rate of 25 Mb/s. Two parallel tasks of integration/evaluation and reset are performed simultaneously in the 500 fF integration capacitors. A single bit detection cycle consists of three distinct modes: integration, evaluation and reset. Fig. 2.14 illustrates the timing diagram of these consecutive modes. Each capacitor experiences a 30 ns integration time window, 5 ns of evaluation/latch time, and a 30 ns reset period. All timing signals are generated from a 25 MHz reference clock in the digital block.

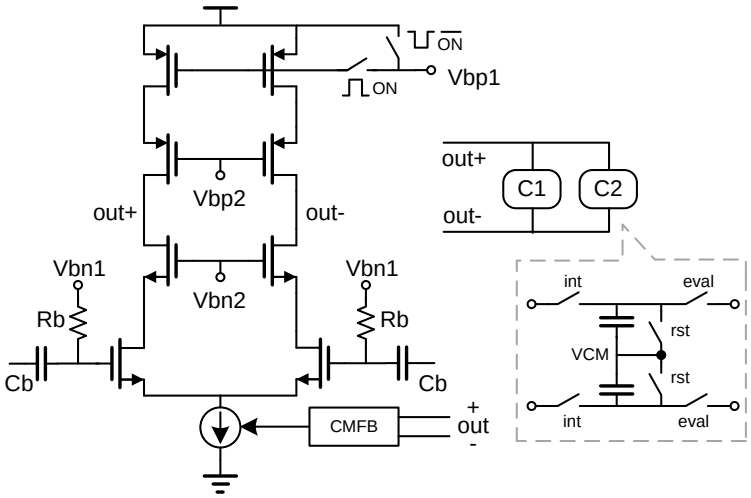


Figure 2.13: High output impedance telescopic integrator and integration capacitors.

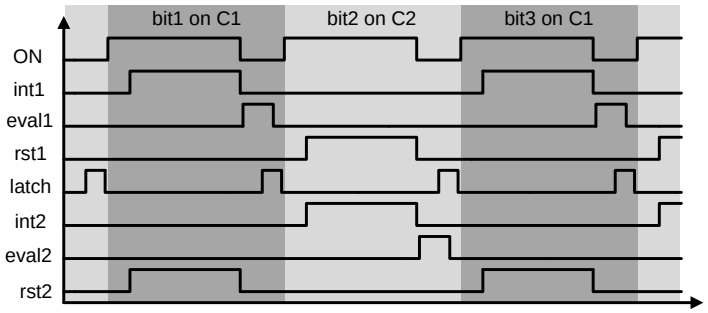


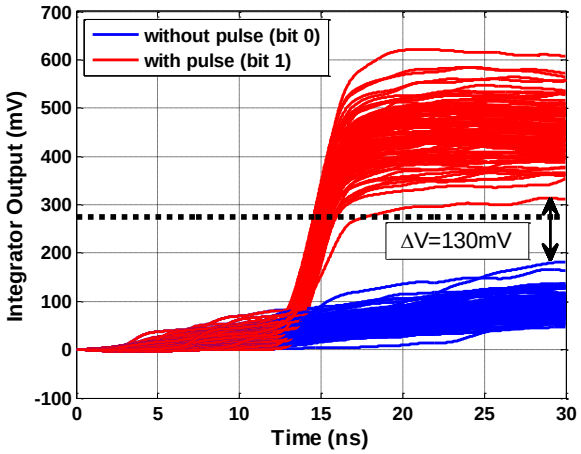
Figure 2.14: Bit detection timing diagram.

The input RC interface to the multiplier serves two functions: it AC-couples the multiplier to the integrator and filters out narrowband interferers that are squared and down-converted to a low frequency band of 0 to 10 MHz [4]. The long integration interval of 30 ns implies that a large discharge time constant is desired to hold the integrated charge. The telescopic topology provides a large output resistance and, hence, a large discharge time constant. The simulation shows a charge holding RC time constant over 100 ns in the hold capacitors. Figs. 2.15(a) and (b) show a transient noise simulation of the LNA, multiplier and the integrator for the conventional single-path architecture and the proposed two-path architecture, respectively. The single-path circuit is designed such that it provides the same amount of gain and consumes the same amount of current as the two-path circuit. For both architectures, the simulation was repeated in the presence (bit 1) and the absence (bit 0) of a 4 GHz UWB

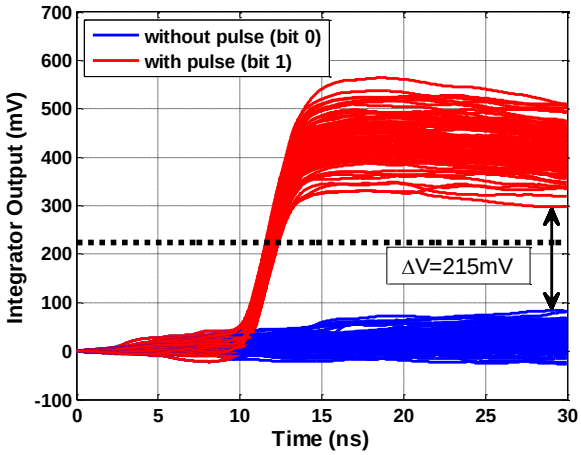
pulse with a 800 μV amplitude. Each simulation is run 100 times and the differential output voltage of the integrator is plotted and overlaid. Dashed lines in both figures represent the reference values that are used in the comparator to detect bit 1 or 0. These reference lines represent the threshold values, V_{TH}, in Fig. 2.2 and Fig. 2.3. A lower BER can be achieved if the integration of each bit results in a value farther from the reference line. In other words, the Y-axis separation between the bit 1 and bit 0 integration result translates to a better SNR. The two-path architecture clearly provides a better detection margin as opposed to its single-path counterpart.

2.4.4 Offset-Compensated Comparator

The combination of a preamplifier, Fig. 2.16(a), and a regenerative latch, Fig. 2.16(b), must achieve a low input referred offset that satisfy the receiver sensitivity requirements. Since the offset of this decision block can directly affect the final BER performance, offset reduction must be considered. Offset cancellation at the input is performed by employing the auto-zeroing technique. A simple differential pair pre-amplifier with resistive CMFB provides 12 V/V gain which reduces the offset of the following latch by an



(a)



(b)

Figure 2.15: Transient simulation results of integrating bit 0 and bit 1 for (a) conventional single-path architecture, and (b) proposed two-path architecture.

order of magnitude. The integration result from the integrator stage and the external reference voltage are both differential inputs to the comparator.

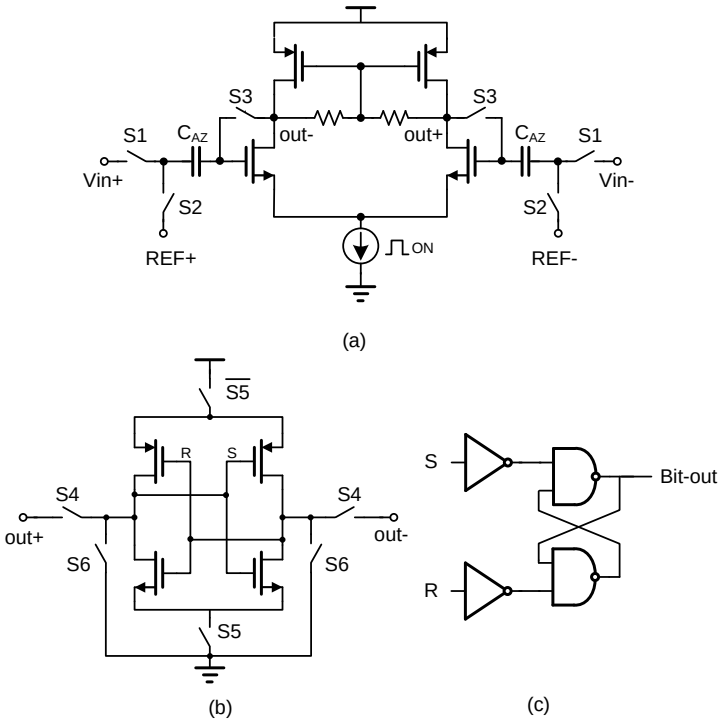


Figure 2.16: (a) Input offset-compensated pre-amplifier. (b) The clocked regenerative latch. (c) SR latch.

The procedure of resolving a single bit in the comparator is as follows: initially the comparator and the latch are in unity-gain and reset modes, respectively. In this state, S2, S3 and S6 are closed and the DC offset is sampled on the auto-zero capacitors (C_{AZ}). Once the integration result is available on the integration capacitors, S1 presents this value to the preamplifier and S2 and S3 are open. The preamplifier cancels the DC offset and boosts the difference between the integration result and the reference value and waits for the latch

command. Finally, S4 and S5 close consecutively and the latch starts regenerating the difference at the output of the preamplifier. A SR-latch, shown in Fig. 2.16(c), follows the comparator to hold the regeneration result over a bit period until new data arrives. Monte Carlo simulations of the entire comparator including all switching non-idealities shows an input-referred offset of 4 mV.

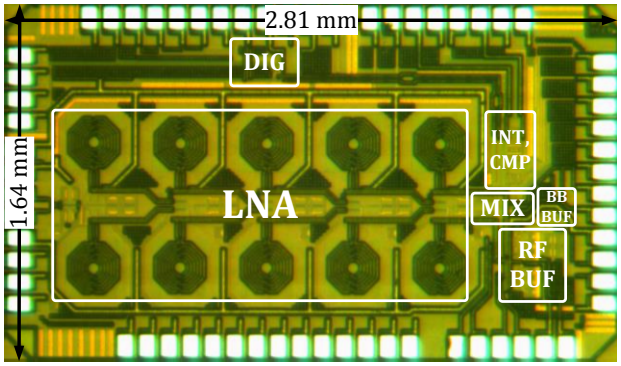


Figure 2.17: Die micrograph of the receiver.

2.5 Measurement Results

The fully integrated receiver has been designed and fabricated in an 8-metal 130-nm CMOS process. The micrograph of the chip is shown in Fig. 2.17. The chip active die area without including I/O pads and measurement buffers is 1.75 mm^2. For testing purpose, the receiver chip was bonded into a 64-pin leadless QFN package and mounted on a custom FR4 test PCB. Two high speed RF

buffers and a baseband buffer are implemented on-chip and connected to the outputs of the gain stages and the multiplier, respectively. The receiver was initially designed to operate at 4 GHz. In measurements, a 500 MHz shift in the gain stage center frequency was observed. Hence, the operating frequency was tuned to 3.5 GHz band. The measured transfer function of the gain stage is shown in Fig. 2.18. Both paths provide > 35 dB gain for the RF pulse. The band-selective front-end provides better than 45 dB rejection for the narrow band interferer (NBI) located at 2.45 GHz.

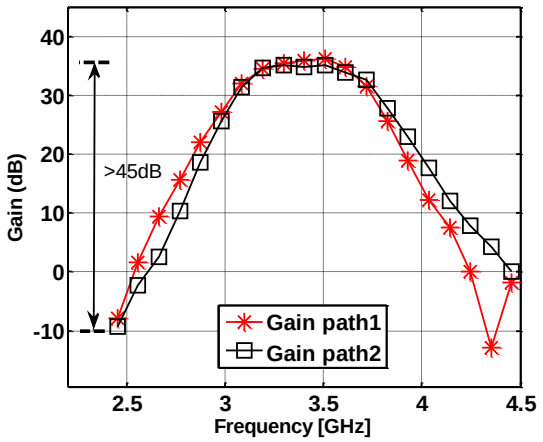


Figure 2.18: Measured gain of path1 and path2 gain stages.

Fig. 2.19(a) shows the buffered noise power spectrums at the output of both paths. It is observed that the noise in the two paths is uncorrelated and of equal power. The measured NF of both paths is presented in Fig. 2.19(b). The resistive

termination provides adequate wideband matching of better than -10 dB over 2-4.5 GHz.

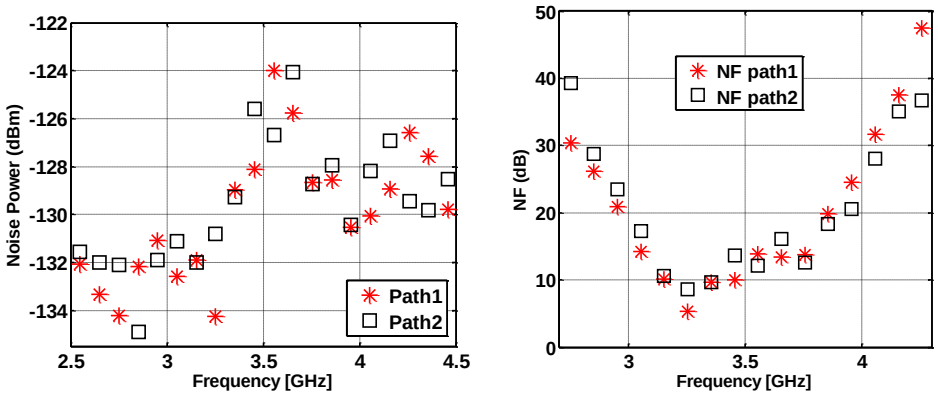


Figure 2.19: (a) Measured noise spectrum at the output of the path1 and path2. (b) Measured NF of path1 and path2.

The P_{1dB} is measured to be -46 dBm (Fig. 2.20). The gain stage is optimally tuned to achieve a maximum baseband pulse amplitude for a given input RF

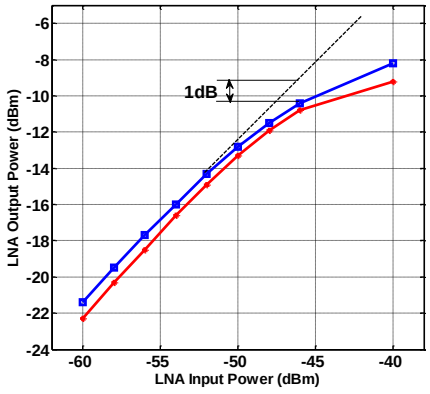


Figure 2.20: Measured P_{1dB} of the two parallel gain stages.

pulse. The front-end gain characteristic from the LNA input to the multiplier output is given in Fig. 2.21.

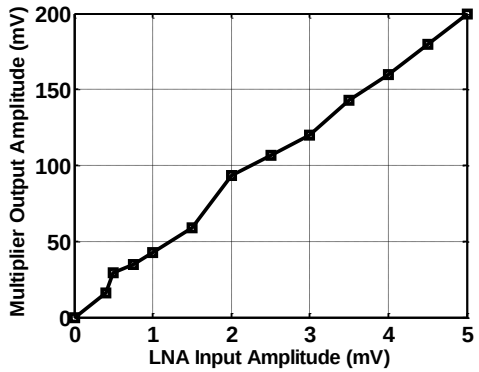


Figure 2.21: Measured receiver front-end input-output characteristic.

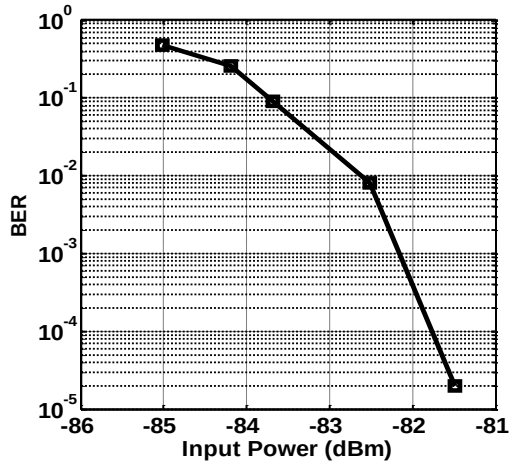


Figure 2.22: Measured BER @1Mb/s.

Bit error rate tests were performed at 1 Mb/s with a Tektronix arbitrary waveform generator AWG7122B generating PRBS data streams of 500 MHz wide pulses along with a synchronized reference clock. The generated signals

were input to the receiver and then detected by the receiver. The detected data is then compared to the sent data. A sensitivity of -82 dBm is achieved for a BER of 10^{-3} (Fig. 2.22). This sensitivity corresponds to a pulse amplitude of 420 μV. If the sensitivity is normalized to the data rate of $DR_{Mb/s}$, the sensitivity will scale by $10\log(DR_{Mb/s}/1)$. A BER measurement is also performed at a data rate of 25 Mb/s and a -69 dBm sensitivity is measured. This shows only 1 dB disagreement with the expected normalized value of -68 dBm. (-82dBm + 10log(25/1) = -68dBm).

The receiver tolerance to both in-band and out-of-band interferers is measured. In this measurement, the input is increased to the level that lowers the bit error rate to 10^{-6}. Then a 2.45 GHz interferer is added to the UWB pulses generated in the AWG. This is the worst case scenario among the 3 UWB sub-bands in 3-5 GHz in terms of interference tolerance. The receiver tolerates continuous-wave (CW) out-of-band and in-band interferers up to -42 dBm and -61 dBm, respectively, when the receiver operates at 1 Mb/s with a 30ns integration window.

At the maximum data rate of 25 Mb/s, the receiver is always on and the receiver consumes a continuous power of 11.59 mW. This corresponds to an energy consumption of 0.46 nJ/bit. The power consumption is mostly dominated by the LNA and the multiplier. The performance summary and the

power breakdown of the receiver are given in Table 2.1. For WSN applications, the receiver is intended to operate at low data rates. Hence, the aggressive duty cycling mode is enabled and power is measured at 1 Mb/s. The combination of the front-end, the baseband and the digital circuitry dissipate an average power of 0.48 mW at 1 Mb/s corresponding to an energy consumption of 0.48 nJ/bit. The slightly degraded energy efficiency is because of the leakage current during the off period. The digital circuitry, including the leakage current and digital buffers, dissipates an average power of 1.08 mW.

Table 2.1: Performance summary

Technology	130 nm	
Active Area	1.75 mm^2	
Modulation	OOK	
Supply Voltage	1.2 V	
Frequency Range	3-4 GHz	
Data Rate	0.1-25 Mb/s	
Power Consumption During Active Period (mW)	LNA	6.45
	Multiplier	4.22
	Integ/Preamp/Comparator	0.36
	Digital (including buffers and leakage)	1.08
	Total Active Power	12.11
Energy/bit	0.48 nJ/bit	
In-band / out-of-band tolerable Interference power for 10^{-3} BER (dBm)	-61 / -42	
Sensitivity@1Mb/s	-82 dBm	

In Table 2.2, the receiver performance is compared with some of the recently reported ED UWB receivers [2]-[7]. All sensitivities are scaled to 1 Mb/s. The

best energy efficiency is achieved for a comparable sensitivity. This is mainly because of the low power gain stage that can operate at a relatively high data rate. The energy consumption per bit can be further decreased by using shorter integration intervals as the receiver then needs to be on for shorter time intervals. However, the amount of energy that is accounted for in the integration will decrease and the sensitivity will degrade. Our entire measurements are based on the assumption of a 30 ns integration window because 85% of the UWB pulse energy lies within this time window [20].

The synchronization hardware was not implemented as a part of this design. However, an FPGA board can implement the timing acquisition using a method explained in [21]. In [21], 80 bits out of a 1024-bit packet is spent on synchronizing incoming pulses and the integration window. This translates to less than 8% energy consumption overhead.

Table 2.2: Comparison with recent state-of-the-art ED UWB RX

	Tech (nm)	Freq (GHz)	Data Rate (Mb/s)	Die Area (mm^2)	Integ. Window (nsec)	Avg. Power (mW)	Eng/bit (nJ/bit)	Sens. at Data Rate (dBm)	Sens. Scaled to 1Mb/s (dBm)
[2]	90	3-5	16.7	2.2	30	42	2.5	-77	-89
[3]	90	3-5	16	1.8	31.25	22.5	1.4	-76	-88
[4]	90	3.6-4.3	1	1	30	2.18	2.18	-66	-66
[5]	180	3.5-4.5	1	6.75	-	5.3	5.3	-82	-82
[6]	180	3.1-3.9	4	-	50	19.8	4.95	-84	-90
[7]	130	7.25-8.5	5	2.25	15	4.2	0.84	-70	-77
[22]	130	3-4	1	3.3	30	0.48	0.48	-82	-82

Acknowledgments

This work was supported in part by NSF grant EF-059223.

CHAPTER 3. A SELF-CLOCKED BLOCKER FILTERING TECHNIQUE FOR SAW-LESS WIRELESS APPLICATIONS

3.1 Introduction

Reconfigurable on-chip N-path filters have shown the potential to replace off-chip surface acoustic wave filters [23]-[25]. These filters can be easily integrated with radios leading to savings in cost and area associated with using off-chip bulky SAW filters. In addition to a high level of integration, such filters are tunable via the clock that drives them and can be utilized for filtering purposes in different standards from a few hundreds of MHz to several GHz. The tunability feature is important in multi-standard wideband receivers where a tunable filter is required to cover the entire spectrum of interest. Typically positioned in the early stages in a receiver chain, these RF filters serve the purpose of filtering strong undesired blockers coexisting with the desired signal. The presence of such large continuous wave (CW) blockers can lead to unwanted phenomena such as receiver gain compression and reciprocal mixing (RM).

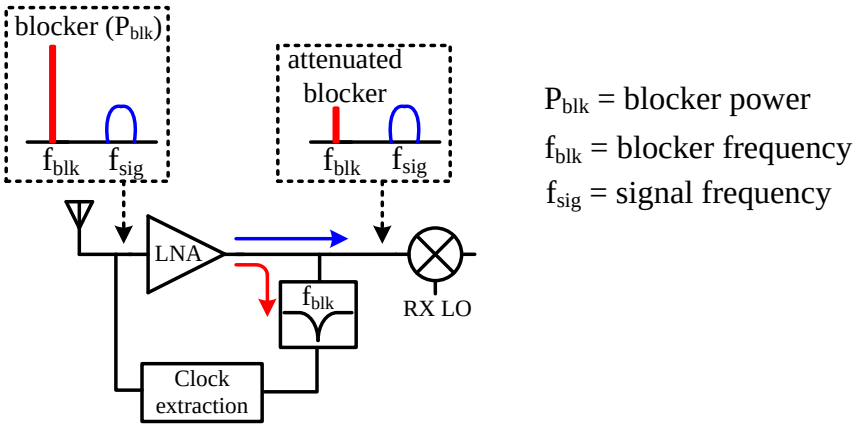


Figure 3.1: Blocker filtering scheme that utilizes a strong input blocker to generate the clock.

Considered as frequency-translational filters, N-path filters are fundamentally made of a set of clocked switches and a baseband filter. Depending upon the characteristic of the baseband filter, the N-path structure translates the baseband filter to RF and builds a high-Q bandpass or notch filter centered around the clock frequency that controls the switches. In the case of bandpass filters [26]-[29], the filter center frequency is generally equal to the desired signal frequency and, therefore, the receiver local oscillator sets the center frequency for the filter. On the other hand, in the notch filter cases [30], [31], the center frequency of the notch filter must be identical to the blocker frequency. Although the blocker frequency information may be available in some specific scenarios [30], generally, the notch filter does not have any knowledge of the frequency of the blocker. This problem can be addressed if

the receiver is able to extract the frequency content of a large blocker. This is possible due to the large voltage swing of the blocker tone at the antenna. For example, a -10 dBm single-tone blocker translates to a 100 mV peak-to-peak swing at the blocker frequency for a 50 Ω load. This voltage swing can be detected by a low swing differential signaling (LVDS) circuit and be used to extract the clock that runs at the blocker frequency. In this paper, we present a filtering scheme that detects the frequency information from the blocker prior to the low noise amplifier (LNA) and converts it to a clock that controls an N-phase notch filter located after the LNA (shown in Fig. 3.1). The blocker-tracking notch filter frequency is the same as the blocker and steers the blocker current away from the receiver main path. As a result, the following stage (for example, the mixer in Fig. 3.1) will experience an attenuated blocker.

3.2 Proposed Blocker Filtering Architecture

3.2.1 System-level Considerations

As mentioned in the previous section, the presence of a strong blocker can lead to degradation in the noise performance through an undesired phenomenon called reciprocal mixing. Reciprocal mixing can occur when a strong tone accompanies the signal during the mixing operation. While the

signal is mixed by the receiver local oscillator (RXLO) and down converted to the baseband, the blocker is also mixed by the LO and down converts to the same baseband frequency (Fig. 3.2(a)).

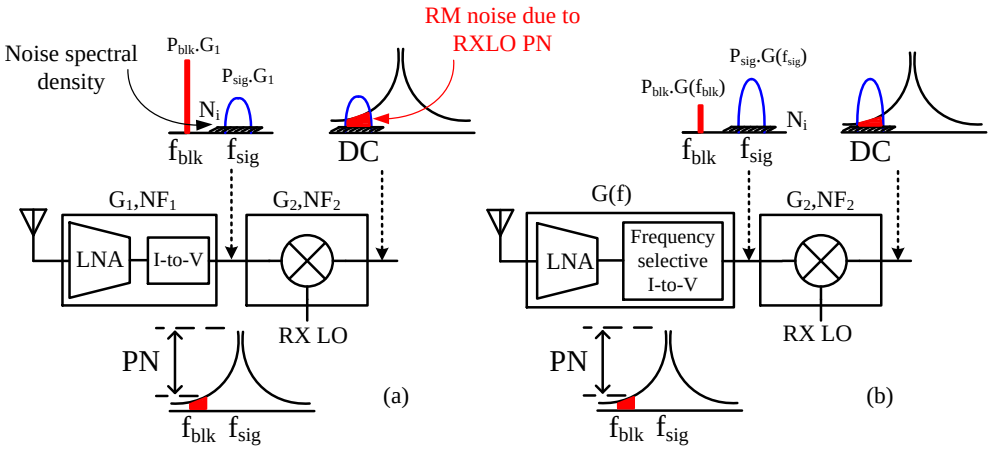


Figure 3.2: NF degradation due to the reciprocal mixing in the down-conversion mixer. (a) Both the signal and the blocker experience an equal gain in the LNA. (b) The signal is amplified by the LNA but the blocker is attenuated via the frequency-selective load at the LNA output.

Without any blocker filtering, the noise factor (NF_2) of the linear mixer in the presence of the blocker can be calculated to be

$$NF_2 = \frac{SNR_{in}}{SNR_{out}} = \frac{P_{sig}/N_i.B}{P_{sig}.G_2/(N_i.B.G_2 + P_{blk}.PN.G_2.B)}$$

$$= 1 + \frac{P_{blk}.PN}{N_i} \tag{3.1}$$

where G_2 and N_i are the mixer gain and the mixer input noise spectral density,

respectively, P_{sig} and P_{blk} are the signal and the blocker power, respectively, and PN and B represents the RXLO phase noise and the signal bandwidth, respectively. We assume that the noise contribution by the mixer circuitry itself is negligible compared to the noise contributed by reciprocal mixing. The gain stage prior to the mixer consists of a transconductor LNA and a current-to-voltage converting load that provides a gain of G_1. The total *NF*, $NF_{w/blk}$, for the combined gain stage and the mixer is given by

$$NF_{w/blk} = NF_1 + \frac{NF_2 - 1}{G_1} = NF_1 + \frac{P_{blk}.PN}{N_i} \times \frac{1}{G_1} \tag{3.2}$$

where NF_1 is the *NF* of the gain stage. In (3.2), G_1 is not frequency-selective and both the signal and the blocker experience a similar gain. If we replace the I-to-V load with a frequency-selective load (Fig. 3.2(b)), the gain will be dependent on the frequency. Hence, G_1 in (3.2) is replaced by $\frac{G(f_{blk})}{G(f_{sig})}$ that incorporates a gain of $G(f_{sig})$ at f_{sig} and an attenuation of $G(f_{blk})$ at f_{blk}. Eq. (3.2) can then be rewritten as

$$NF_{w/blk} = NF_1 + \frac{P_{blk}.PN}{N_i} \times \frac{G(f_{blk})}{G(f_{sig})} \tag{3.3}$$

The second term in (3.3), $NF_{w/blk\ (RM)}$, corresponds to the impact of reciprocal mixing noise and can be reduced if $\frac{G(f_{blk})}{G(f_{sig})}$ <1. $\frac{G(f_{blk})}{G(f_{sig})}$ represents the relative rejection of the blocker compared to the signal. In a mixer first receiver front-

end such as [32], $NF_{w/blk\,(RM)}$ can be simplified with the assumption that $G(f_{sig})$=1 and NF_1=1. In this scenario, N_i is equal to the theoretical noise floor and $NF_{w/blk\,(RM)}$ in logarithmic form can be calculated from

$$NF_{w/blk\,(RM)} = P_{blk} + PN + 174 - R_{notch} \tag{3.4}$$

where $R_{notch} = 10\log(1/G(f_{blk}))$ represents the amount of the blocker rejection. Fig. 3.3 shows $NF_{w/blk}$ versus the blocker attenuation for different *PN* values.

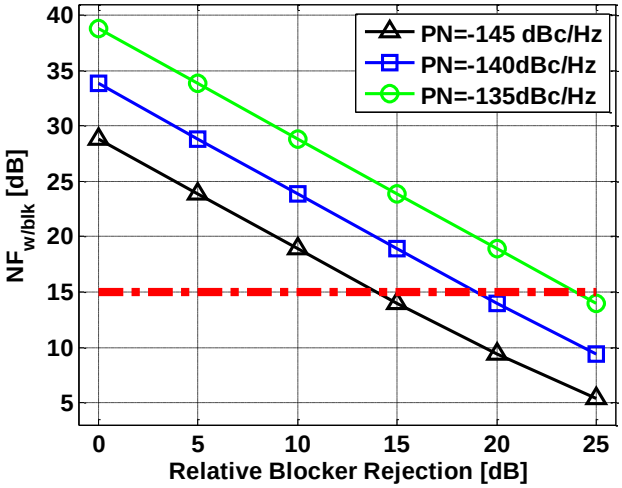


Figure 3.3: $NF_{w/blk}$ vs blocker rejection, R_{notch} =10log$(1/G(f_{blk}))$, with $G(f_{sig})$=1 in the presence of a 0 dBm blocker.

An off-chip SAW filter attenuates the blocker by approximately 20 dB with respect to the desired signal. In order to prevent the noise performance degradation due to the removal of the SAW filter in a SAW-less architecture, this 20 dB attenuation must be compensated either by suppressing the blocker

before the mixer or by lowering the *PN* in the RXLO. The estimated blocker *NF* requirement of the 3GPP standard is about 15 dB for blockers up to 0 dBm [23]. Assuming no gain at the LNA and a *PN* of -141 dBc/Hz [33] in the RXLO, without any blocker rejection before the mixer, $NF_{w/blk}$ can reach 33 dB for a 0 dBm blocker. From Fig. 3.3, it is obvious that even a rejection of R_{notch} =20 dB meets the noise requirement by a small margin. Equation (3.3) shows that higher signal gain, $G(f_{sig})$, reduces $NF_{w/blk}$. Fig. 3.4 presents $NF_{w/blk}$ after the addition of a gain stage with a moderate gain $G(f_{sig})$ =10 dB and NF_1 =3 dB.

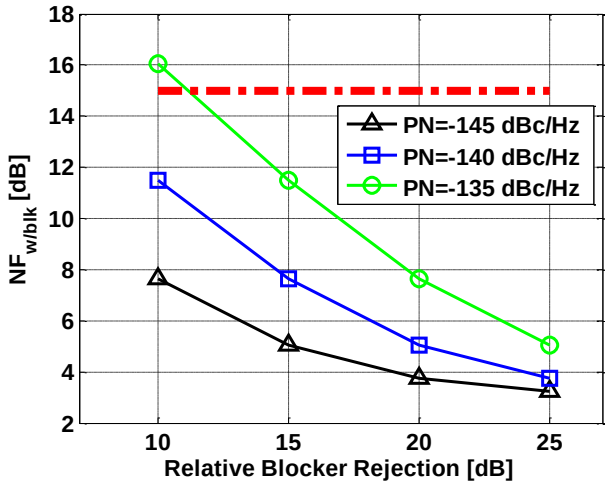


Figure 3.4: $NF_{w/blk}$ vs $\frac{G(f_{blk})}{G(f_{sig})}$ with 10 dB signal gain in the presence of a 0 dBm blocker.

In comparison to the case with $G(f_{sig})$ = 1, the architecture with a gain

stage before the mixer provides a better margin. For example, with 20 dB of blocker attenuation with respect to the signal and a similar *PN* of -141 dBc/Hz, the new architecture provides approximately 9 dB margin. It should be noted that 20 dB is a relative gain between the signal and the blocker. If we assume a 10 dB gain for the signal, the blocker must be attenuated by R_{notch} =10 dB.

3.2.2 Filter Implementation

The proposed filtering solution is illustrated in Fig. 3.5. The input is provided differentially to the front-end via an off-chip balun and an LC-matching circuit. The differential input RF voltage is then converted to a RF current within the transconductor based LNA. Wideband input matching for the LNA is provided by a resistive termination that resides within the poly-phase RC structure employed by the multi-phase clock extraction block. In addition to input matching, a multi-phase clock extraction block serves as the clock generation core. Contrary to conventional N-path circuits that require a dedicated LO and clock source, here, we extract the clock from the blocker. The frequency of the clock tracks the frequency of the blocker since it is obtained from the blocker itself. Details of the clock extraction circuitry are

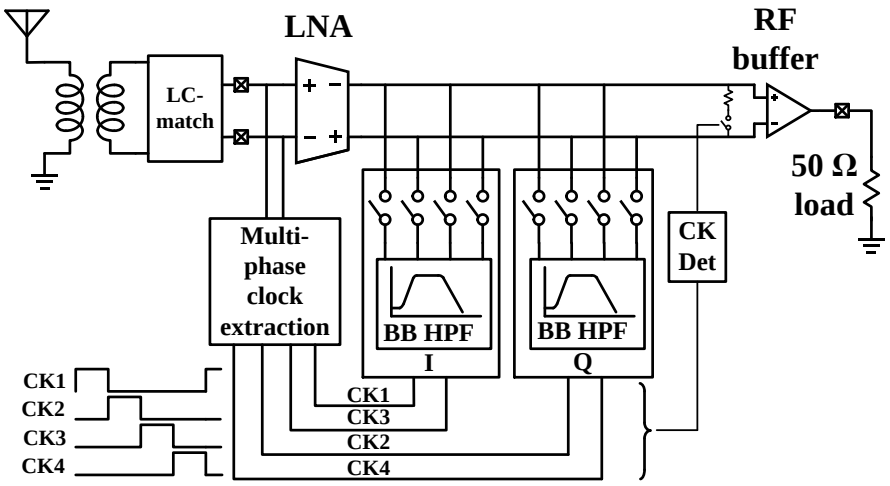


Figure 3.5: Four-phase blocker-rejecting receiver front-end block diagram.

described in Section 3.3.

The extracted quadrature 4-phase clocks, CK1-4, are routed to the switches of the 4-path filter. The LNA output current is directed to the 4-path filter that serves as a frequency-selective load. The impedance frequency response of the load is designed such that the blocker current sees a much smaller impedance than the signal current does. The frequency-translation comes from the impedance translation capability of the 4-path structure. Described in detail in [34] and [35], N-path structures are capable of up converting the impedance profile of their baseband terminal to their RF terminal and centering it around the clock frequency that drives the switches. Once the

baseband highpass profile is shifted to the RF frequency, a notch profile will be formed around the clock frequency. In this proposed scheme, the low impedance at the notch frequency will convert the blocker current back to the voltage domain. Similarly, the flat high impedance section of the impedance profile, with a $\Delta\omega$ offset from the notch frequency, will convert the signal back to the voltage domain. This frequency-selective current-to-voltage conversion results in a blocker voltage swing suppression with respect to the signal. Once the blocker is sufficiently attenuated, it can be processed by the following stage.

For a blocker power level below the sensitivity of the clock extraction circuit, CK1-4 will be low. Consequently, the notch filter will perform as an infinite load. Fortunately, this will not be much of a concern since aggressive blocker rejection is usually required only when a strong blocker is present. For a moderate blocker level, the notch filter can stay inactive as long as a proper load is provided at the LNA output for current-to-voltage conversion. In a complete front-end scenario, this load may come from the following mixer. In this work, a resistor is chosen as the load, as shown in Fig. 3.5. In order to add the resistive load to the LNA output when the blocker level is below the sensitivity of the clock extraction block, a clock activity detector is integrated with the filter. Finally, the differential voltage at the output of the LNA is converted to a single-ended voltage via an on-chip RF buffer and sent to an off-

chip 50 Ω load where it is measured.

3.3 Circuit Implementation

The fully differential implementation is designed for a 1.3 V supply in a 65 nm CMOS process.

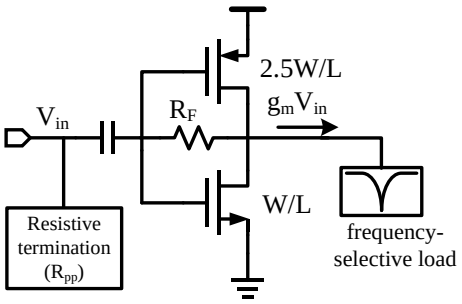


Figure 3.6: Inverter-based LNA converts input RF voltage to current.

3.3.1 LNA

Shown in Fig. 3.6, the LNA is an inverter-based CMOS low noise transconductor amplifier with a feedback resistor. This transconductor amplifier converts its RF input voltage signal to current and provides the RF output current to the following frequency-selective load. The input RF signal consists of the desired signal and a strong blocker. The LNA must be able to handle this blocker with a good linearity. A combination of NMOS and PMOS

devices supplied from a 1.3 V supply provides the required linearity. The output impedance of the LNA block needs to be large enough not to impact the pass band impedance of the following notch filter. Otherwise, the maximum achievable rejection by the notch filter will be degraded. Therefore, both NMOS and PMOS devices are designed to have a longer channel length of 180 nm. To provide the maximum possible bandwidth, no cascode device is used. Wideband input matching at the antenna interface is provided via the polyphase impedance, R_{PP}.

3.3.2 Multiphase Clock Extraction From Blocker

The clock extraction circuitry consists of a polyphase filter, a current mode logic (CML) amplifier, a CML-CMOS converter, a 4-phase clock generator and a clock level-shifter, shown in Fig. 3.7.

The input of the clock extraction chain is differential and receives a copy of the RF signal that is at the LNA input. The outputs of the clock chain are 25% duty-cycled 4-phase clocks. The first segment of the clock chain is a passive RC polyphase filter and serves two purposes. First, it provides input matching for the LNA and second, it generates quadrature phases from the input differential signal. The majority of quadrature phase generation techniques use frequency division. The clock extraction circuit in this work,

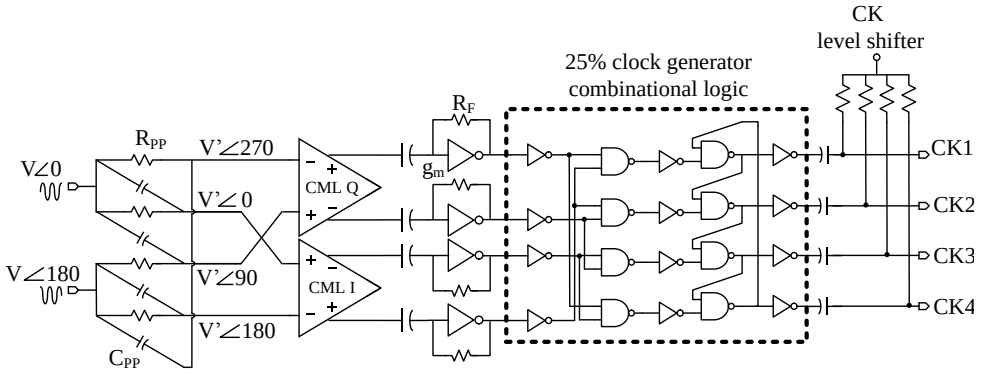


Figure 3.7: Schematic diagram of the clock extraction circuit that generates four quadrature non-overlapping clocks from a differential low swing input.

however, is intended to track the blocker frequency and deliver a clock that runs at the same frequency as the blocker. Therefore, frequency division based quadrature phase generation is not suited for our purpose.

The RC polyphase filter shown in Fig. 3.7, decomposes a differential input signal into four quadrature signals [36]. The phase shift in the polyphase filter depends on the values of R_{PP} and C_{PP}. The ideal quadrature phase shift occurs for a frequency of ω when $R_{PP}C_{PP}\omega$ equals unity. Although the exact quadrature phase shift is narrowband in nature, with a proper choice of R_{PP} and C_{PP}, the quadrature signals at the polyphase output maintain their relative phase shifts over a wide range of frequencies. In this work, we chose a polyphase center frequency of $\omega = 2\pi \times 1.1$ GHz. Any deviation from ω will lead to an

unwanted phase shift of $\Delta\varphi$ and, ultimately, result in distortion in

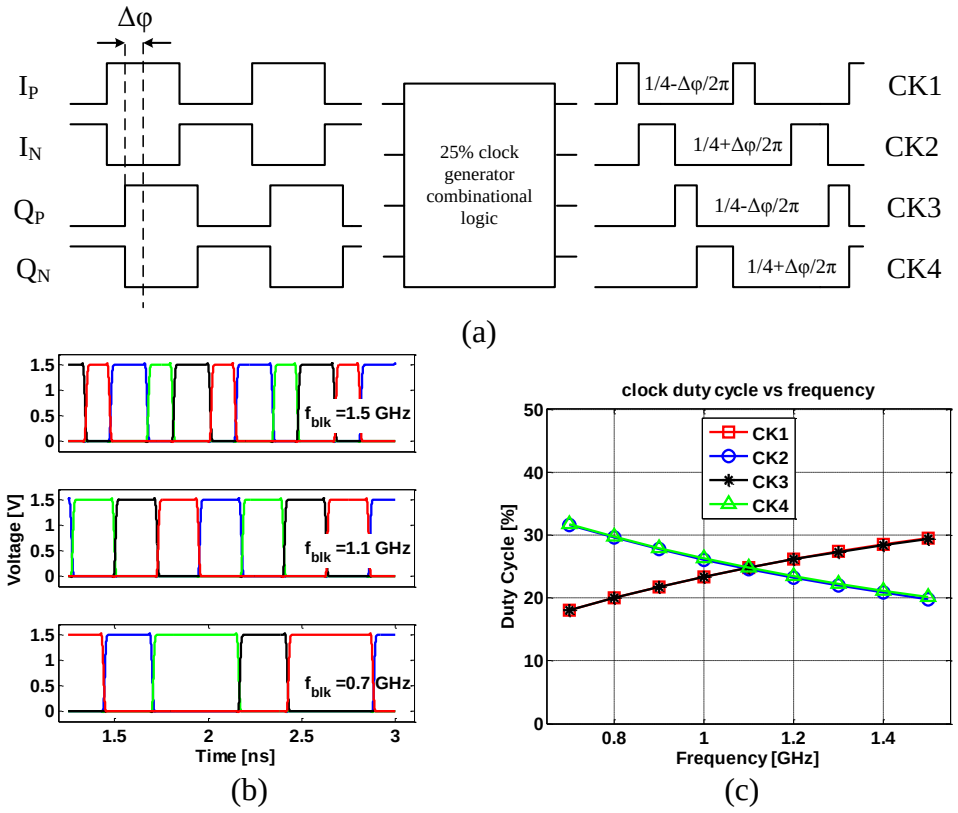


Figure 3.8: Quadrature error in a four phase filter. (a) Phase error ($\Delta\varphi$) causes a symmetric duty cycle distortion in extracted CK1-4. (b) Extracted four-phase clocks for three blocker frequencies; 0.7 GHz, 1.1 GHz, and 1.5 GHz. (c) Duty cycle of the four phases versus the blocker frequency.

the duty cycle of the extracted clock that goes to the filter switches. Fig. 3.8 illustrates the scenario of a quadrature error in a four phase filter. Shown in Fig. 3.8(a), the quadrature phase error, due to the offset from ω, tends to cause only a symmetric duty cycle distortion such that the duty cycle of $CK_{1,3}$ and $CK_{2,4}$

change by $+\Delta\varphi/2\pi$ and $-\Delta\varphi/2\pi$, respectively. The fundamental frequency and nonoverlapping shape of the 25% output clocks, however, are still intact. Furthermore, the quadrature relative phase shifts among the four clocks are maintained. Fig. 3.8(b) presents extracted four-phase clocks for three blocker frequencies; 0.7 GHz, 1.1 GHz, and 1.5 GHz, respectively. Fig. 3.8(c) shows the duty cycle of the four phases versus the blocker frequency. At a blocker frequency of $1/(RC) = 2\pi \times 1.1$ GHz, a 25% duty cycle is observed. At 0.7 GHz and 1.5 GHz, the duty cycle is distorted by 6% and 5%, respectively.

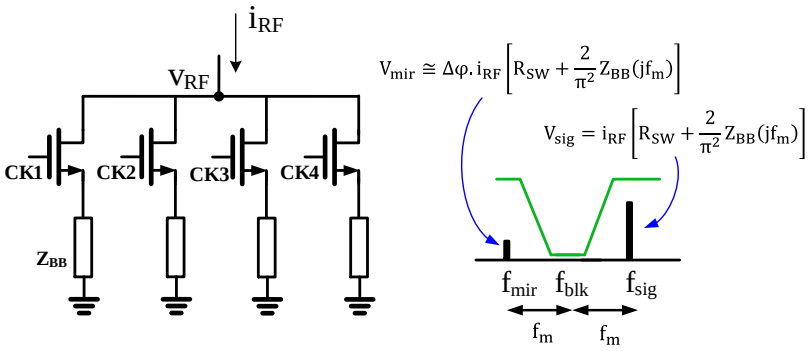


Figure 3.9: Duty cycle imperfection in $CK_{1\text{-}4}$ results in generation of an unwanted mirror voltage term in V_{RF}.

A simplified single-ended version of the notch filter, as shown in Fig. 3.9, is chosen in order to study the impact of the duty cycle distortion on the notch filter. Once a RF current is injected in this filter, duty cycle imperfection of the clock can lead to an unwanted mirror voltage term in addition to the wanted signal voltage [37]. Two frequency components f_{sig} and f_{mir} are shown

at RF at two sides of the notch. The first component represents the desired signal while the second component is caused by the duty cycle distortion in the clock. The amplitude of these two components are shown in Fig. 3.9 where the quadrature phase error of $\Delta\varphi$ manifests itself as an amplitude scaling factor. Since the frequency offset between the mirror term and the signal term, $f_{sig} - f_{mir}$, is twice the frequency offset between the signal and the blocker, $f_{sig} - f_{blk}$, any subsequent filtering in the receiver chain will further suppress the unwanted mirror component. Therefore, the filtering requirement for the mirror term is more relaxed than that of the blocker and the mirror term is not important. In order to serve as a multiband radio solution, a bank of RC polyphase filters can be employed to cover various bands of interest.

The polyphase filter is followed by the CML stage as shown in Fig. 3.7. This linear amplifier amplifies the low swing clock for the following CML-to-CMOS conversion. Before the sine-wave clock gets converted to a CMOS clock, the amplitude of the clock must be large enough to prevent high sensitivity to supply noise. In high frequency clocking circuits, CML amplifiers are more desirable because of their higher robustness to supply noise. In addition, CML amplifiers cause less perturbation on their supply voltage compared to CMOS amplifiers. The CML amplifier is AC-coupled to an inverter-based CMOS amplifier that further amplifies the clock signal by (1 −

$g_m R_F$) and delivers approximately a rail-to-rail clock at its output. The AC-coupled interface blocks low frequency nonidealities such as the DC-offset of the CML amplifier. The output of the CMOS amplifier will be full swing for the logic gates. In the next step, the quadrature differential 50% clocks are converted to 25% duty-cycled 4-phase clocks in the following combinational logic block that includes inverters and NAND gates as shown in Fig. 3.7. The cascade of logic gates are properly sized to provide appropriate drivability. NAND gates chained in the fashion shown in Fig. 3.7 guarantee that adjacent clock phases will not overlap with each other.

The non-overlapping clocks need to be level-shifted by a proper DC offset in order to ensure a low ON resistance in the filter switches. Since the common-mode level of switches is set to VDD/2 via the preceding LNA, the clock levels are boosted by VDD/2 through a passive clock level shifter to guarantee that the switches have sufficient overdrive in the ON state and, hence, very small R_{SW}. For the chosen switch size of 60um/0.6um, this overdrive

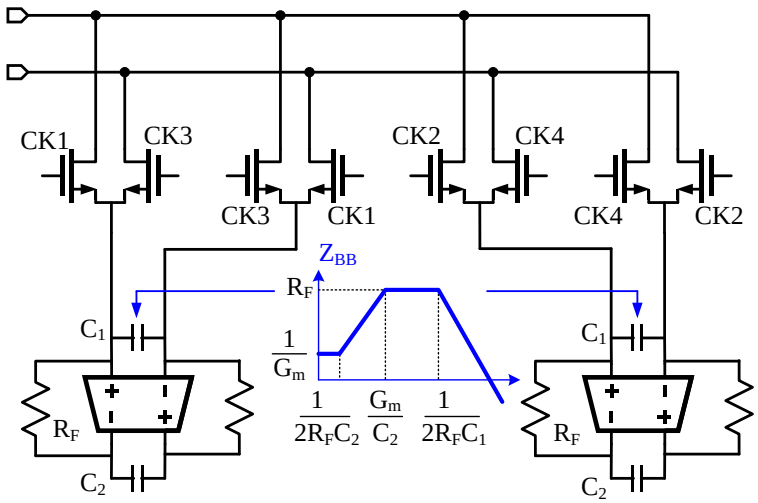


Figure 3.10: Notch filter schematic diagram.

provides less than 8 Ω per switch during its ON period.

3.3.3 Notch Filter

A frequency-translational notch filter that tracks the blocker is described here. As illustrated in Fig. 3.1, this filter precedes the mixer. The filter steers the blocker current out of the signal path, thereby preventing it from mixing with the RX LO. Hence, the degradation in performance due to reciprocal mixing, as described in Section 3.2.1, is suppressed. The notch filter architecture is presented in Fig. 3.10. The common-mode level for the switches

is determined via the preceding LNA. The source and drain of the switches are set to VDD/2 while the gate is controlled by the level shifted clock from the clock extraction circuitry. The impedance translation via switches must be done differentially to cancel the flicker noise contribution of the clock generation and buffer circuitry [25]. The baseband impedance, Z_{BB}, is realized by a TIA as shown in Fig. 3.10 along with the corresponding frequency response. The highpass profile of Z_{BB} is determined by the values of C_1, C_2, R_F and the G_m of the core transconductor stage. The output impedance of the transconductor must be much larger than R_F to ensure the depth of the notch is mainly determined by the transconductance of the TIA cell. A folded cascode TIA is chosen to provide this large output impedance. A larger G_m provides a lower impedance path for the downconverted components around DC. Meanwhile, components with a frequency offset from DC will experience the feedback resistor, R_F. Once this highpass characteristic is frequency-translated to the clock frequency, the blocker and the signal face a low impedance ($1/G_m$) and a high impedance (R_F), respectively. Hence, the impedance difference between R_F and $1/G_m$ will determine the amount of rejection achievable by the notch filter. Since the N-path structure upconverts the notch characteristics and centers them around the clock frequency and its odd harmonics, a second pole is needed to suppress the residual impact of the higher order notches on the fundamental clock frequency

notch. This second pole is introduced by the capacitor C_1. In practice, due to the residual impact of notches at higher harmonics and also the inherent impedance of the N-path structure [30], the achievable rejection is slightly less than $g_m R_F$. A differential folded cascode structure with complementary input devices and a common-mode feedback is chosen as the transconductor amplifier to provide a wider input dynamic range and a higher voltage-to-current conversion. A common-mode feedback loop sets the output voltage to VDD/2. The input signal is also biased around VDD/2 through a DC coupling to the LNA.

3.3.4 Extracted Clock Phase Noise

In addition to providing the wanted attenuation, the 4-path notch structure itself contributes some noise in the system. This extra noise must be taken into consideration while calculating the overall $NF_{w/blk}$. The nature of this noise is similar to reciprocal mixing and originates from the phase noise of the extracted clock. Since the filter is positioned after the LNA, this extra noise contributed by the filter will be suppressed by the LNA gain before it is referred to the antenna. Fig. 3.11 describes how the clock phase noise of the notch filter degrades the signal to noise ratio during the blocker filtering operation. As shown in Fig. 3.11(a), the notch filter is fundamentally made of two sets of frequency-translation switches and a highpass filter. After down converting

both the signal and the blocker to the baseband through the first set of switches, the highpass filter attenuates components around the DC frequency. This attenuation is experienced by the blocker which is mixed by an ideal clock that is at the blocker frequency. On the other hand, the signal experiences the passband part of the highpass characteristic. The second set of switches up converts the baseband components back to the RF. This process results in an attenuation of the blocker with respect to the signal.

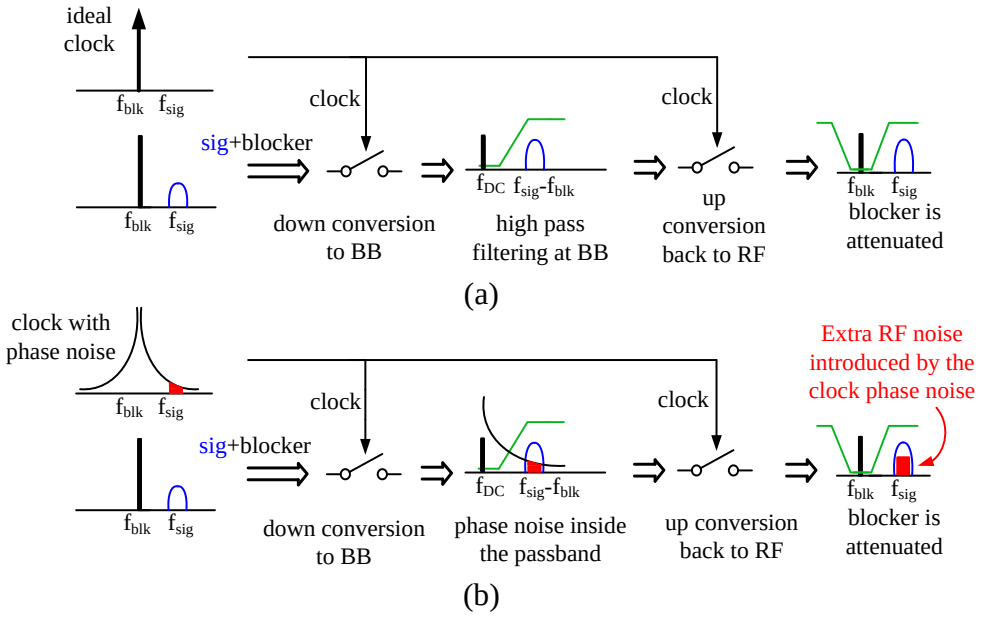


Figure 3.11: Blocker rejection mechanism in a frequency-translational notch filter. (a) Switches are driven by an ideal clock. (b) Switches are driven by a clock with phase noise.

Fig. 3.11(b) illustrates the same filtering process with the addition of the clock

phase noise. Throughout the down conversion, in addition to the signal and the blocker, some portion of the phase noise cross mixes with the strong blocker. The mixing products are at $f_{sig} + f_{blk}$ and $f_{sig} - f_{blk}$. The term at $f_{sig} - f_{blk}$ represents a part of the phase noise that is down converted by the single-tone blocker. Since it is located at the same frequency as the signal, this term will raise the noise floor. The extra noise will be up converted to the RF frequency along with the signal and hence will degrade the signal to noise ratio. It should be noted that all N-path filter solutions, bandpass or notch, need to cope with the phase noise in their clock source. In a conventional N-path solution, the clock is provided by a dedicated LO with a constant phase noise profile. In the proposed clock extraction scheme, however, the phase noise in the extracted clock scales with the blocker power level. A stronger blocker leads to a lower phase noise for the extracted clock. The improved phase noise can be explained by comparing the clock extraction circuit to a CMOS oscillator [38] which follows Eq. (3.5)

$$Relative\ Phase\ Noise \propto \frac{1}{{V_{swing}}^2} \propto \frac{1}{P_{blk}} \tag{3.5}$$

where V_{swing} is the blocker voltage swing at the input of the clock extraction unit. Eq. (3.5) shows that the relative phase noise is inversely proportional to the blocker power. For example, for every 10 dB increase in the blocker power, the phase noise is expected to reduce by 10 dB. Fig. 3.12 shows the phase noise

of the extracted CK1 from simulation. As shown in the figure, *PN*

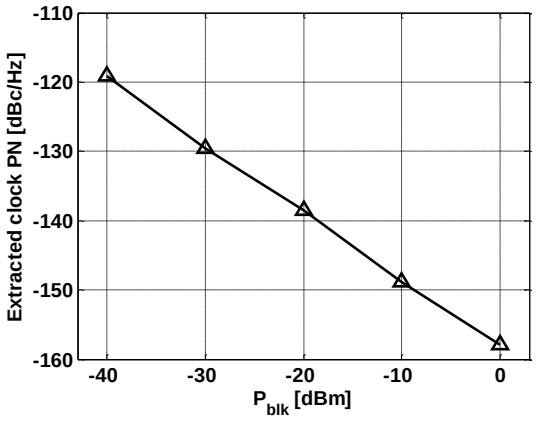


Figure 3.12: Extracted clock phase noise versus the blocker power.

is inversely proportional to the blocker power.

As shown in Fig. 3.11(b), intuitively, the amount of the extra noise is expected to be dependent on the strength of the blocker and the phase noise of the extracted clock. From Eq. (3.5), the clock phase noise itself is a function of the blocker power. Therefore, the extra noise depends primarily on the blocker power. It should be noted that for weak blockers below the sensitivity of the clock extraction circuit, this extra noise is not present since the clock is not available. Eq. (3.4) can, therefore, be rewritten as

$$NF_{w/blk\,(RM)} = P_{blk} + PN - N_i - R_{notch} + N_{add}$$

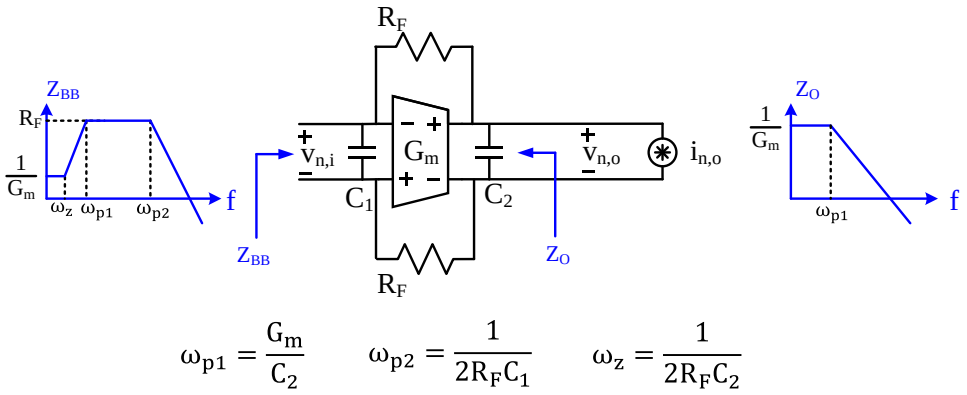
$$= P_{blk} + PN - N_i - \Delta_{RM} \qquad (3.6)$$

with the extra term Δ_{RM} that represents the amount of reduction in $NF_{w/blk\,(RM)}$. As long as the rejection provided by the notch filter (R_{notch}) exceeds the noise added by the notch filter (N_{add}), $NF_{w/blk\,(RM)}$ and, hence, the overall $NF_{w/blk}$ will decrease. In other words, any positive value for Δ_{RM} will translate to a reduction in $NF_{w/blk}$.

It should be noted that an improvement in $NF_{w/blk}$ is only achieved for blockers whose power is large enough to result in an extraction of the clock. For weaker blockers, Δ_{RM} and NF_{add} are both zero and the entire notch filter circuitry will be inactive while the receiver noise requirement is more relaxed.

3.3.5 Baseband TIA Noise Contribution

The impact of the baseband TIA noise on the receiver main path must be negligible. The noise contribution of the baseband TIA is evaluated in this section. As the first step, the input referred noise voltage and the impedance of the TIA seen at the baseband needs to be determined. Next, we will upconvert the noise and the impedance to the RF and evaluate the contribution to the noise of the main path.



$$\omega_{p1} = \frac{G_m}{C_2} \qquad \omega_{p2} = \frac{1}{2R_F C_1} \qquad \omega_z = \frac{1}{2R_F C_2}$$

Figure 3.13: Input and output frequency response of the baseband TIA.

The simplified schematic diagram of the baseband TIA is shown in Fig. 3.13. As illustrated in Fig. 3.10, the highpass frequency response of Z_{BB} is given by

$$Z_{BB} = \frac{1 + 2R_F C_2 s}{G_m + C_2 s} || \frac{1}{C_1 s} \tag{3.7}$$

and includes two poles at G_m/C_2 and $1/2R_F C_1$ and a zero at $1/2R_F C_2$. The impedance seen at the output of the TIA is defined by Z_O

$$Z_O = \frac{1 + 2R_F C_1 s}{G_m + C_1 s} || \frac{1}{C_2 s} = \frac{1 + 2R_F C_1 s}{2R_F C_1 C_2 s^2 + (C_1 + C_2)s + G_m} \tag{3.8}$$

and has a lowpass frequency response with two poles and one zero. The dominant pole is located at G_m/C_2 while the second pole is very close to the zero (at $1/2R_F C_1$) for $C_2 \gg C_1$.

The overall TIA noise is modeled by a current source ($i_{n,o}^2$) at the output. The lowpass frequency response of Z_O shapes the power spectral density of $i_{n,o}^2$ and

results in a lowpass voltage noise spectral density ($v_{n,o}^2 = |Z_O|^2 \times i_{n,o}^2$) that is plotted in Fig. 3.14.

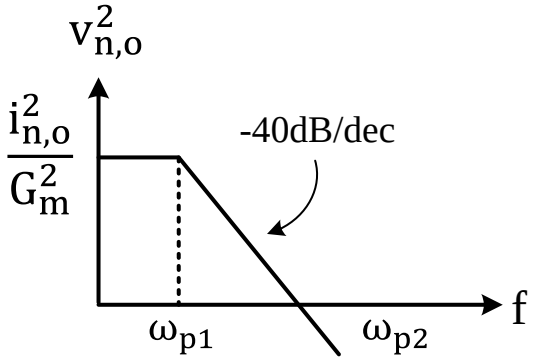


Figure 3.14: Power spectral density of the equivalent noise voltage at the output of the TIA.

$v_{n,o}^2$ is transferred to the input with a gain of

$$\frac{v_{n,i}^2}{v_{n,o}^2} = \left|\frac{1}{1 + 2R_F C_1 s}\right|^2 \tag{3.9}$$

For $|2R_F C_1 \omega| \ll 1$, $v_{n,i} \approx v_{n,o}$. $v_{n,i}$ represents the input-referred differential noise of each one of the quadrature branches. The four phase diagram of the notch filter with noiseless Z_{BB} and equivalent input-referred noise of each branch is shown in Fig. 3.15. $v_{n,i,I}$ and $v_{n,i,Q}$ are the equivalent noise voltage of the I and Q branches, respectively.

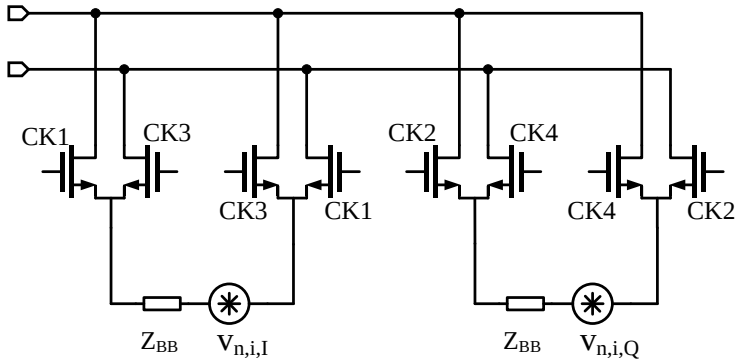


Figure 3.15: Simplified notch filter schematic diagram with equivalent noise and impedance of the baseband TIA.

In the next step, the baseband noise voltages and Z_{BB} must be upconverted to RF. For simplicity of the analysis, we chose the single-ended version of the filter as shown in Fig. 3.16.

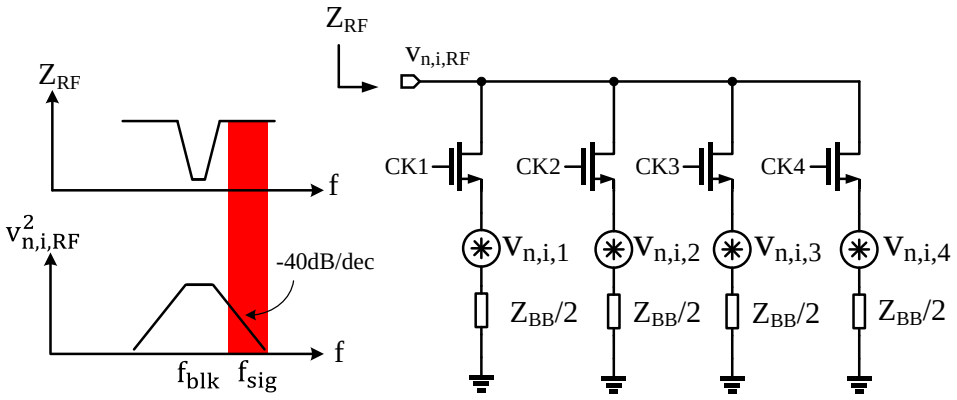


Figure 3.16: Single-ended equivalent of the notch filter with TIA overall noise frequency response.

$v_{n,i,1-4}$ are the single-ended equivalent of $v_{n,i,I}$ and $v_{n,i,Q}$ and can be calculated from

$$v_{n,i,1} = v_{n,i,3} = \frac{v_{n,i,I}}{2} \quad \text{and} \quad v_{n,i,2} = v_{n,i,4} = \frac{v_{n,i,Q}}{2} \tag{3.10}$$

$v_{n,i,RF}$ represents the RF equivalent of $v_{n,i,1-4}$ after upconversion. *CK1-4* are periodic 25% clocks. $v_{n,i,RF}$ can be written in term of $v_{n,i,1-4}$

$$v_{n,i,RF} = CK1.\, v_{n,i,1} + CK2.\, v_{n,i,2} + CK3.\, v_{n,i,3} + CK4.\, v_{n,i,4} \tag{3.11}$$

where $v_{n,i,RF}$ equals $v_{n,i,j}$, j=1,2,3,4 for a 25% of a clock period when *CKj* is high (Fig. 3.5). Fig. 3.16 suggests that both the baseband noise voltage ($v_{n,i,j}$) and the baseband impedance (Z_{BB}) upconvert from the baseband to RF [37] and result in a RF noise voltage ($v_{n,i,RF}$) and a RF impedance (Z_{RF}). The ultimate equivalent input-referred voltage and impedance are also plotted in Fig. 3.16. In frequencies where the signal is located, the equivalent power spectral density of the noise is attenuated by -40 dB/dec whereas the noise power spectral density in the blocker frequency is maximized. If we convert $v_{n,i,RF}$ and Z_{RF} to a Norton equivalent, the amount of noise injected in the main path is given by $v_{n,i,RF}/Z_{RF}$. This term clearly shows that the baseband TIA noise current contribution to the main path is minimized at f_{sig} where $v_{n,i,RF}$ is attenuated and Z_{RF} is maximized. Simulations confirm that the overall noise contribution of the baseband TIA is less than 0.4 dB.

3.4 Measurement Results

The fully integrated filter solution has been designed and fabricated in a 9-metal, 65-nm CMOS process. The micrograph of the chip is shown in Fig. 3.17. The active chip die area including I/O pads and decoupling capacitors is 0.86 mm^2.

For testing purposes, the receiver chip was bonded into a 28-pin leadless QFN package and mounted on a custom FR4 test PCB. A high speed RF buffer and a digital buffer were implemented on-chip and connected to the

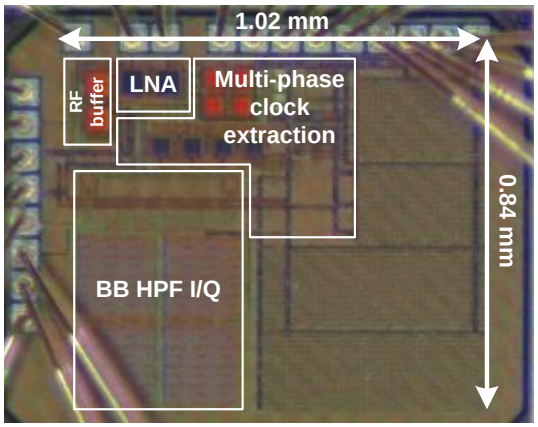


Figure 3.17: Chip micrograph.

outputs of the filter stage and the clock extraction block, respectively. The gain, NF and S_{11} of the standalone LNA when the blocker level is below the sensitivity of the clock extraction circuit are shown in Fig. 3.18.

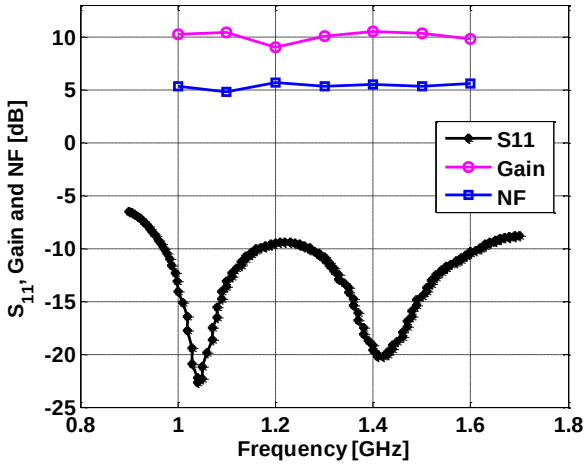


Figure 3.18: S_{11}, gain and NF of the LNA without the blocker.

The measured transfer function of the blocker-tracking filter is shown in Fig. 3.19 for various blocker frequencies. The signal sees approximately 10 dB gain, whereas the blocker located 100 MHz from the signal experiences more than 10 dB rejection.

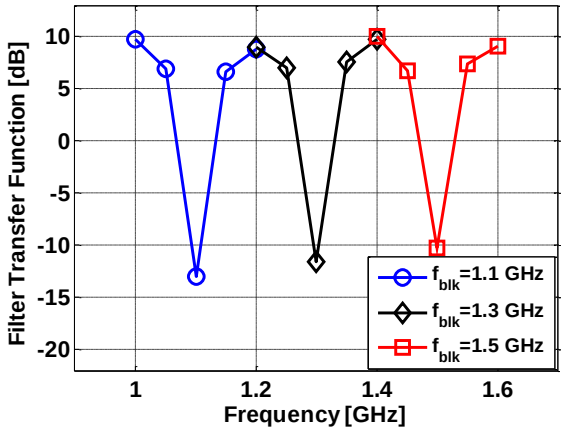


Figure 3.19: Notch filter rejection transfer function from 1 GHz to 1.6 GHz.

Fig. 3.20 shows the amount of rejection measured at the notch frequency of 1.1 GHz for various blocker levels. The sensitivity of the clock extraction circuit is -40 dBm. For blockers stronger than -10 dBm, the limited dynamic range of the baseband TIA degrades the transconductance of the TIA and consequently the highpass characteristic of the baseband filter. At a blocker power of -5 dBm, the rejection drops to 6 dB whereas the added noise (N_{add}) rises to 9 dB.

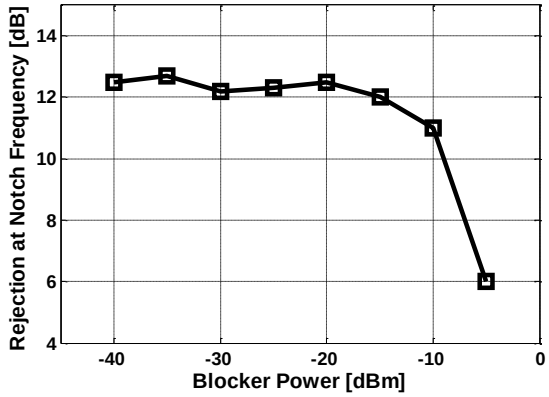


Figure 3.20: Notch filter rejection (R_{notch}) vs blocker power.

Fig. 3.21 shows the measured Δ_{RM} and N_{add} at the output of the LNA versus the blocker power. For any blocker in the -40 dBm to -10 dBm range, the proposed notch filter reduces the degradation due to reciprocal mixing by Δ_{RM} dB.

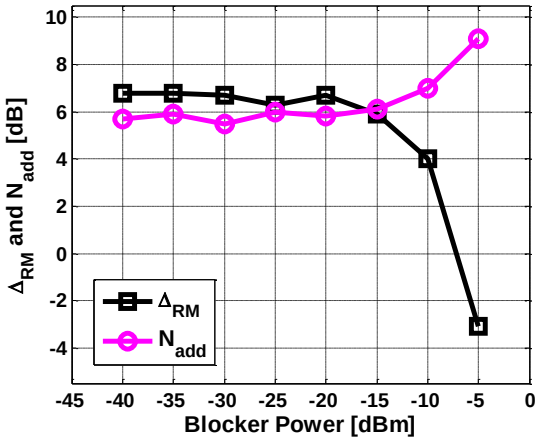


Figure 3.21: Δ_{RM} and N_{add} vs blocker power.

The filtering structure proposed in Fig. 3.5 achieves a R_{notch} better than 11 dB for blockers stronger than -40 dBm with N_{add} of less than 7 dB. This translates to a greater than 4 dB improvement in $NF_{w/blk}$ for blockers up to -10 dBm.

Table 3.1 summarizes the proposed blocker-rejecting technique and compares it with other recently published papers. In [31] and [39] a frequency-translational filter is used and places the notch filter in series with the signal path. In this paper, the notch filter is in shunt with the signal path as illustrated in Fig. 3.1. The results are summarized for a filter that is aimed for use with blocker powers up to -10 dBm before the filter nonlinearity degrades the rejection. In order to compare the noise performance of the frequency-translational filters, the phase noise of the clock oscillator should be taken into account. For [31] and [39], we assume that the clock that drives the filter is

generated on-chip and achieves a similar phase noise of -149 dBc/Hz at 100 MHz offset (Fig. 3.12). From Eq. (4), this amount of PN would give rise to a phase noise induced NF equal to 15 dB when a -10 dBm blocker is present. For architectures such as [31] and [39] with no LNA preceding the filter, this 15 dB can directly add to the overall NF. The proposed filtering technique benefits from the 10 dB gain preceding the filter. This helps in reducing the impact of the clock PN. With a -10 dBm blocker, the measured NF is 11.8 dB.

The entire design including clock buffers and the RF buffer consumes 30mW, of which 4.5 mW is consumed by the LNA, 9 mW by the filter, and 16.5 mW in the clock extraction/distribution circuitry.

Table 3.1: Comparison with Other Filter Designs

	[31]	[39]	This Work
Technology	65nm	65nm	65nm
Filter Type	Notch series	Notch + BPF	Notch shunt
Frequency [GHz]	0.1-1.2	0.1-1	1-1.6
Gain [dB]	-2.8	23	10
NF with no blocker [dB]	2.5	7.6	5
NF with -10 dBm blocker and clock PN [dB]	17.5	22.6	11.8
Rejection (relative to the signal) [dB]	18	38	19
Active Area [mm^2]	0.87	2.1	0.86
Power Consumption [mW]	30	50	30

CHAPTER 4. CONCLUSION

This work presented two techniques to reduce the power and area/cost of RF receivers.

In Chapter 2, an energy efficient non-coherent ED IR-UWB receiver with a front-end noise reduction technique was presented. Since the power dissipation in the front-end generally dominates the receiver power budget, the relaxed noise requirements of the front-end are utilized to lower the power consumption of the gain stage. A comprehensive mathematical analysis of the conventional and the proposed architecture has been provided. The analysis forms the basis for the receiver design. The fully integrated receiver was implemented in a 130 nm CMOS process and achieves an energy efficiency of 0.48 nJ/bit. The entire receiver operates from a 1.2 V supply, and supports data rates up to 25 Mb/s. The best case sensitivity of -82 dBm is achieved at 1 Mb/s for a BER of 10^{-3}. Targeted for short-range WSN applications, the proposed receiver achieves the best energy efficiency for a comparable sensitivity.

In Chapter 3, a new blocker-filtering technique is described that allows for the elimination of the off-chip SAW filter. SAW filters in current receiver architectures are mainly utilized to attenuate the out-of-band blockers. The proposed technique attenuates the blocker on-chip and, therefore, enables the

removal of the SAW filter. This filter extracts the clock from the blocker and utilizes it to suppress the blocker. Hence, it does not require any prior information of the exact location of the blocker. The extracted clock runs at the blocker frequency and drives a notch filter. Positioned after the LNA, the notch filter provides a low impedance path for the blocker current and steers it away from the signal path, hence, suppressing the blocker. The implemented filter tracks the blocker within 1 to 1.6 GHz and provides better than 10 dB of rejection at the notch frequency. It is shown that despite the narrowband nature of the clock extraction circuit, the extracted 4-phase clock duty cycle distortion has a negligible impact on the filter performance. This prototype has been demonstrated to be effective for blockers from -40 dBm to -10 dBm with a noise performance that is comparable to prior work.

Future work in noise-cancelling ED receiver improvement incorporates eliminating the noise sources that are correlated between the two paths. In addition, inductor-less architectures can be explored to save the on-chip area.

Future work in clock extraction from the blocker incorporates reducing the phase noise of the clock. Extending the blocker-tracking range of the clock extraction circuit can also be explored.

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